



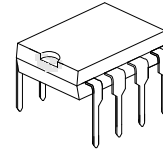
PRIMARY-SIDE REGULATION PWM POWER SWITCH

DESCRIPTION

The UTC **US1652** is a primary control switch mode charger and adapter applications. The controlled variable is transferred by an auxiliary winding from the secondary to the primary side. The device integrates PWM controller to enhance the performance of discontinuous conduction mode (DCM) flyback converters.

The UTC **US1652** operates in primary-side sensing and regulation. Opto-coupler and TL431 could be eliminated. It operates in fixed frequency mode at large load conditions, frequency reduction mode at light/medium load and 'Extended burst mode' at No/light load conditions. So that low standby power can be achieved.

The UTC **US1652** achieves high precision CV/CC regulation and high power efficiency. It offers comprehensive protection coverage with auto-recovery features including Cycle-by-cycle current limiting, V_{DD} over voltage protection, V_{DD} clamp, OTP, leading edge blanking, V_{DD} under voltage lockout, etc.



DIP-8

FEATURES

- * Programmable CV and CC regulation
- * Primary-side sensing and regulation with No TL431 and opto-coupler
- * Multi-mode operation for high efficiency
- * Adjustable constant current and output power setting
- * Power on soft-start time (4ms)
- * Frequency shuffling and adjustable gate drive greatly improving EMI
- * "Extended burst mode control" for improved efficiency and minimum standby design
- * Built-in leading edge blanking (LEB)
- * V_{DD} under voltage lockout
- * V_{DD} over voltage shutdown and clamp
- * Cycle-by-Cycle current limiting
- * Fail-safe protection for open loop fault condition
- * Auto-restart in over voltage condition

ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
US1652L-D08-T	US1652G-D08-T	DIP-8	Tube

US1652L-D08-T	(1)Packing Type (2)Package Type (3)Green Package	(1) T: Tube (2) D08: DIP-8 (3) L: Lead Free, G: Halogen Free and Lead Free
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The diagram shows the US1652 component with pins 1 through 8. Pin 5 is connected to the Date Code. Pin 6 is connected to L: Lead Free. Pin 7 is connected to G: Halogen Free. Pin 8 is connected to the Lot Code.

Pin diagram of the 74VHC04 hex inverters. The package is shown with pins 1 through 8. Pin 1 is labeled V_{DDG} , pin 2 is V_{DD} , pin 3 is INV, and pin 4 is CS. On the right side, pin 8 is GND, pin 7 is GND, pin 6 is Drain, and pin 5 is Drain. A small circle is shown on the top edge of the package.

PIN NO.	PIN NAME	DESCRIPTION
1	V _{DDG}	Internal gate driver power supply
2	V _{DD}	IC DC power supply input
3	INV	Inverting input of error amplifier (EA). Connected to resistor divider from primary sensing winding reflecting output voltage. PWM duty cycle is determined by EA output and current sense signal at pin 4.
4	CS	Current sense input
5, 6	Drain	HV MOSFET Drain Pin. The Drain pin is connected to the primary lead of the transformer
7, 8	GND	Ground

The block diagram illustrates the internal architecture of the power management IC. Key components include:

- Regulator & Vref:** Connected to V_{DD} (pin 2) and provides a Por (Power-On Reset) signal to the Logic core.
- OVP (Over-Voltage Protection):** A comparator with its non-inverting input (+) connected to $30V$ and its inverting input (-) connected to V_{DD} (pin 2). Its output is connected to the Logic core.
- CC/CV controller:** Connected to V_{DD} (pin 2) and provides a signal to the Logic core.
- PWM (Pulse Width Modulation):** Receives a $1.25V$ reference at its non-inverting input (+) and a feedback signal from the CS (Current Sense) pin (pin 4) at its inverting input (-). Its output is connected to the Logic core.
- Logic core:** The central processing unit that coordinates the Regulator & Vref, OVP, CC/CV controller, Drive, Softstart, LEB, and PWM blocks.
- Drive:** Receives a signal from the Logic core and drives the **Power MOSFET**.
- Softstart:** Provides a soft-start signal to the Drive block.
- LEB (Load Error Block):** Receives a signal from the Logic core and provides feedback to the PWM block.
- Power MOSFET:** The output stage, with its Drain connected to V_{DDG} (pin 1) and its Source connected to the CS pin (pin 4).
- CS (Current Sense):** Pin 4, which senses the load current and provides feedback to the PWM block.
- External Connections:**
 - V_{DD} (pin 2) is the main power supply.
 - V_{DDG} (pin 1) is the gate drive supply.
 - INV (pin 3) is an inverting input.
 - GND (pin 7/8) is the ground connection.
 - $5/6$ Drain is the MOSFET drain connection.

■ ABSOLUTE MAXIMUM RATING ($T_A=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Drain Voltage (Off State)	$B_{V_{DS}}$	-0.3~650	V
V_{DD} Voltage	V_{DD}	-0.3~33	V
V_{DDG} Voltage	V_{DDG}	-0.3~33	V
V_{DD} Zener Clamp Continuous Current	$I_{DD\ clamp}$	10	mA
CS Input Voltage	V_{CS}	-0.3~7	V
INV Input Voltage	V_{inv}	-0.3~7	V
Operating Junction Temperature	T_J	-20~150	$^{\circ}\text{C}$
Storage Temperature	T_{STG}	-55~150	$^{\circ}\text{C}$

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.
Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ ELECTRICAL CHARACTERISTICS ($T_A=25^{\circ}\text{C}$, $V_{DD}=V_{DDG}=16\text{V}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage (V _{DD}) Section						
Standby Current	I _{DD ST}	V _{DD} =13V		5	10	μA
Operation Current	I _{DD op}	Operation Supply Current I _{NV} =1.25V, C _S =0V, V _{DD} =V _{DDG} =20V		1.0	2.0	mA
V _{DD} Under Voltage Lockout Enter	U _{VLO(ON)}		7.5	8.5	9.5	V
V _{DD} Under Voltage Lockout Exit	U _{VLO(OFF)}		14.0	15	16.0	V
Over Voltage Protection Voltage	O _{VP(ON)}	C _S =0V, I _{NV} =1V Ramp up V _{DD} Until Gate Clock is Off	28.5	30.0	31.5	V
I _{DD} =10mA	V _{DD_clamp}			33		V
Current Sense Input Section						
LEB Time	T _{LEB}			1.2		μs
V _{TH_OC_test}	V _{th_oc}		780	820	860	mV
Propagation Delay	T _{d_oc}			300		ns
Input Impedance	Z _{SENSE_IN}			50		KΩ
Soft Start Time	T _{ss}			4		ms
CV Section						
Normal Mode Frequency	F _{req}		45	50	55	KHz
Burst Mode Base Frequency	F _{req_Burst}			22		KHz
Frequency Shuffling Range	Δf/F _{req}			±4		%
CC Section						
Oscillation Frequency	F _{req}	Minimum frequency		12		KHz
		Maximum frequency		50		KHz
Error Amplifier section						
Reference Voltage for EA	V _{REF_EA}		1.21	1.25	1.29	V
DC Gain of the EA	G _{dc}			50		dB
Unity Gain Bandwidth	G _{BW}			37.5		kHz
Power MOSFET Section						
Mos Drain-Source Breakdown Voltage	BV _{DSS}			650		V
Static Drain to Source On Resistance	R _{DS(ON)}			6		Ω
OTP SECTION						
Threshold Temperature of OTP (Note)	T _{OTP}			+150		°C

■ OPERATION DESCRIPTION

The UTC **US1652** is a primary control switch mode charger and adapter applications. It operates in primary-side sensing and regulation. Opto-coupler and TL431 could be eliminated. Proprietary built-in CV and CC control can achieve good CV/CC performance. The device integrates PWM controller to enhance the performance of discontinuous conduction mode (DCM) flyback converters.

Startup Current and Start up Control

The V_{DD} pin of UTC **US1652** is connected to the line input through a resistor. A large value startup resistor can be used to minimize the power loss in application because the start current of UTC **US1652** is very low. When the V_{DD} voltage reaches $V_{TH(ON)}$, the internal startup circuit is disabled and the IC turns on.

Operating Current

The Operating current of UTC **US1652** is as low as 1mA. Good efficiency and very low standby power can be achieved.

Soft Start Control

The UTC **US1652** features an internal 4ms soft start to minimize the component electrical over-stress during power on startup. As soon as V_{DD} reaches UVLO (OFF), the control algorithm will ramp peak current voltage threshold gradually from nearly zero to normal setting of 0.82V. Every restart is a soft start.

Constant Voltage Operation

The UTC **US1652** is designed to produce good CC/CV control characteristic as shown in the Fig. 1.

To support UTC **US1652** proprietary CC/CV control, system needs to be designed in DCM mode for flyback system. When INV is equivalent or larger than 1.25V, the system works in CV control, In CV operation, the output voltage is sensed on the primary side and the sensed signal controls the duty cycle through a built-in error amplifier (EA). Connected to a resistor divider from the primary side sensing winding, the inverting input of the Error Amplifier (EA) is compared to an internal reference voltage of 1.25V to regulate the output voltage. The EA output is internally connected to the PWM generator and controls the duty cycle.

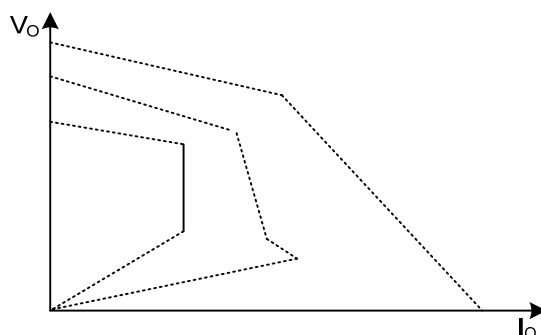


Fig 1. Typical CC/CV Curve

■ OPERATION DESCRIPTION (Cont.)

Constant Current Operation

When INV lower than 1.25V, the system works in CC control. In CC operation, the CC point and maximum output power can be externally adjusted by external current sense resistor R_{cs} . The larger R_{cs} , the smaller CC point is, and the smaller output power becomes, and vice versa as shown in Fig.2.

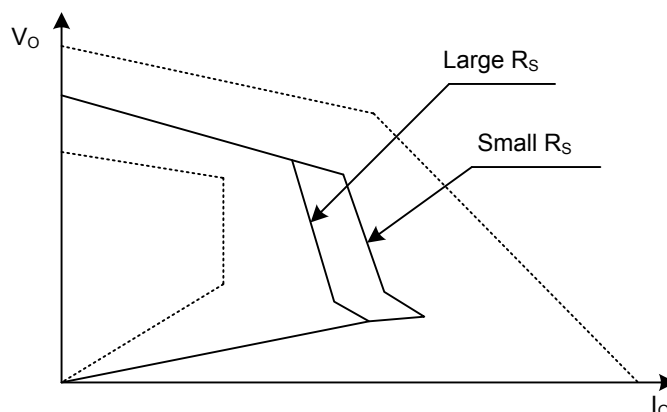


Fig 2. Adjustable output power by changing R_{cs}

In charger applications, a discharged battery charging starts in the CC portion of the curve until it is nearly full charged and smoothly switches to operate in CV portion of the curve.

In an AC/DC adapter, the normal operation occurs only on the CV portion of the curve. The CC portion provides added cycle-by-cycle current limiting protection.

Extended Burst Mode Operation

At light load or zero load condition, most of the power dissipation in a switching mode power supply is from switching loss, the core loss of the transformer and the loss on the snubber circuit. The magnitude of power loss is in proportion to the switching frequency. Lower switching frequency leads to the reduction on the power loss and thus conserves the energy.

The UTC **US1652** self adjusts the switching frequency according to the loading condition. The switch frequency is reduced at light/no load condition to improve the conversion efficiency. At light load/no load condition, the output of the Error amplifier (EA) drops below the burst mode threshold level and device enters Burst Mode control. The frequency control also eliminates the audio noise at any loading conditions.

Operation switching frequency

The switching frequency of UTC **US1652** is internally set and adjusted according to CC/CV operation. No external frequency setting components are required.

Frequency shuffling for EMI improvement

The frequency Shuffling/jittering (switching frequency modulation) is implemented in UTC **US1652**. The oscillation frequency is modulated with a pseudo random source so that the tone energy is spread out. The spread spectrum minimizes the conduction band EMI and therefore eases the system design.

Current Sensing and Leading Edge Blanking

Cycle-by-cycle current limiting is offered in UTC **US1652**. The switch current is detected by a sense resistor into the CS pin. When the power switch is turned on, a turn-on spike will occur on this resistor. A 500ns leading-edge blanking is built in to avoid false-termination of the switching pulse so that the external RC filtering is no longer needed.

■ OPERATION DESCRIPTION (Cont.)

Adjustable Drive Capability

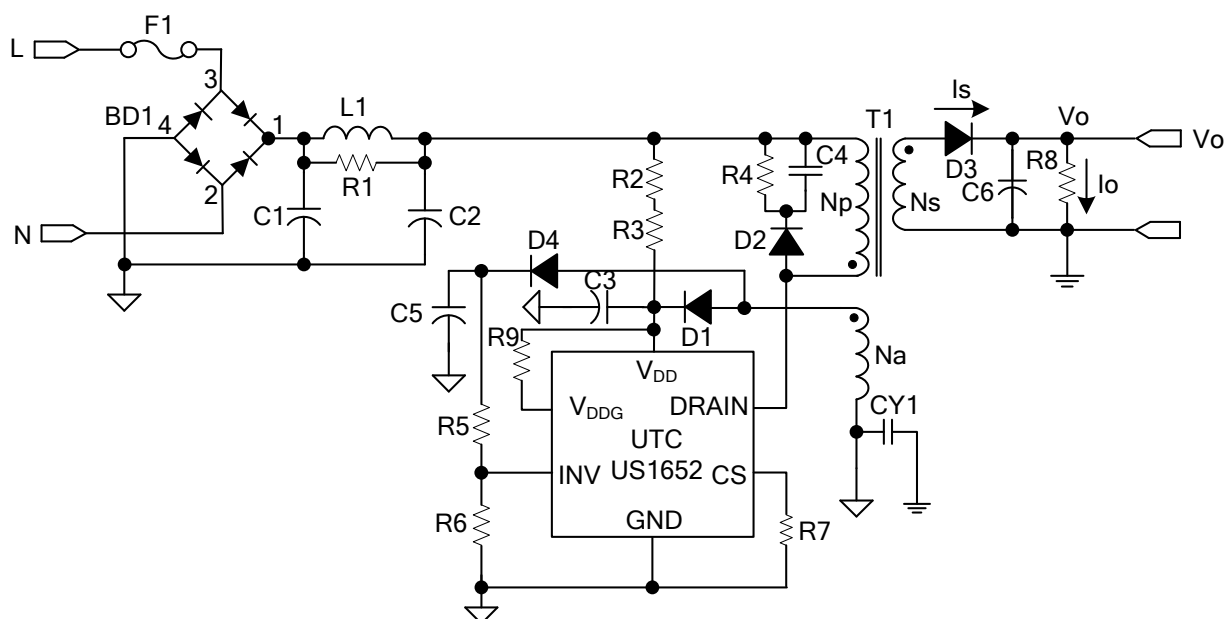
The internal power MOSFET in UTC **US1652** is driven by a dedicated gate driver for power switch control. Too weak the gate drive strength results in higher conduction and switch loss of MOSFET while too strong gate drive compromises EMI. A good tradeoff is achieved through the built-in totem pole gate design with right output strength control. The gate drive strength can be adjusted externally by a resistor connected between V_{DD} and V_{DDG} . The low idle loss and good EMI system design is possible with this dedicated control scheme.

Protection Control

Good power supply system reliability is achieved with its comprehensive protection features including V_{DD} over-voltage protection, V_{DD} Clamp, GATE Clamp, Power on soft start, Cycle-by-cycle current limiting, short circuit protection, leading edge blanking, OTP and UVLO, etc.

V_{DD} is supplied by transformer auxiliary winding output. The output of UTC **US1652** is shutdown when V_{DD} drops below $V_{TH(OFF)}$ and the power converter enters power on start-up sequence thereafter.

■ TYPICAL APPLICATION CIRCUIT (9V/0.5A)



BOM

Reference	Component	Reference	Component
BD1	BD 1A/600V	R2,R3	R 1.5MΩ 1206 ±5%
L1	1mH 6x8mm	R4	R 200KΩ 1206 ±5%
C1,C2	EC 4.7μF 400V 105°C	R5	R 47KΩ 0805 ±1%
C3	EC 4.7μF 50V 105°C	R6	R 3KΩ 0805 ±1%
C4	CC 1n F 1000V 1206	R7	R 3Ω 1206 ±5%
C5	CC 0.33μF 50V 0805	R8	R 2.4KΩ 1206 ±5%
C6	EC 560μF 10V 105°C	R9	R 470Ω 0805 ±5%
D1, D2, D4	Diode UTC 1N4007	T1	EE-16
D3	Diode UTC SB360	F1	FUSE 1A 250VAC
R1	R 2.4KΩ 1206 ±5%	CY1	Y/C 1000p F 250V

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