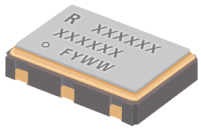
RVX7050P VCXO

SMD Voltage Controlled Crystal Oscillator



High performance VCXO in 7 x 5 mm Surface Mount Package

Product description

The RVX7050P VCXO combines very low RMS phase jitter and low supply current in an industry standard 7 x 5 mm SMD package. Available in hundreds of industry standard frequencies from 8 to 800 MHz for fast delivery and reduced inventory levels.

Applications

- Basestation
- Communications
- Ethernet
- Consumer Products
- SONET/SDH
- WiMAX/WLAN

Features

- 0.5 ps integrated RMS phase jitter (12 kHz to 20 MHz)
- Fast sample turnaround available
- LVCMOS, LVPECL, or LVDS Output options
- Wide frequency range
- Low power differential outputs

Specifications

1.0 SPECIFICATION REFERENCES

Line	Parameter	Description
1.1	Model Description	RVX7050P VCXO
1.2	Reference Number	
1.3	Rakon Part Number	

2.0 FREQUENCY CHARACTERISTICS

Line	Parameter	Test Condition	Value	Unit
2.1	Frequency		8 to 1500	MHz
2.2	Operating Temperature Range		-40 to 85	°C
2.3	Frequency Stability	Including Temperature range, Supply variation, Load variation & 15 years aging at 25°C	±30 to 50	ppm
2.4	Temperature Stability	Temperature range only	±10 to 20	ppm

3.0 POWER SUPPLY

Line	Parameter	Test Condition	Value	Unit
3.1	Supply Voltage (VDD)	With a tolerance of ±10%	3.3	V
3.2	Supply Voltage (VDD)	With a tolerance of ±5%	2.5	V
3.3	Supply Current	For LVCMOS	30 max	mA
3.4	Supply Current	For LVPECL	65 max	mA
3.5	Supply Current	For LVDS	40 max	mA

4.0 CONTROL VOLTAGE (VCO)

Line	Parameter	Test Condition	Value	Unit
4.1	Absolute Pull Range (APR)		±50 min	ppm
4.2	Total Pull Range	Frequency shift from minimum to maximum control voltage	50 to 250	ppm
4.3	Control Voltage	Nominal 1.65V	0 to 3.3	V
4.4	Linearity	Control voltage 0.3 to 3V	10 max	%
4.5	Slope	Positive only		
4.6	Modulation BW	Control voltage 0.3 to 3V	10 min	kHz
4.7	Input Impedance		1 min	MΩ

5.0 OUTPUT CHARACTERISTICS - LVCMOS (UP TO 200 MHz)

Line	Parameter	Test Condition	Value	Unit
5.1	Output Voltage (Vol)	15pF load	10 max	%VDD
5.2	Output Voltage (Voh)	15pF load	90 min	%VDD
5.3	Duty Cycle	@ 50% VDD	48 to 52	%
5.4	Rise Time / Fall Time	90%/10%	3 max	ns
5.5	RMS Phase Jitter	Typical integrated 12 kHz to 20 MHz	0.5	ps

6.0 OUTPUT CHARACTERISTICS - LVPECL ONLY

Line	Parameter	Test Condition	Value	Unit
6.1	Output Voltage (Vol)	50Ω nominal load. (VDD - 1.6V) max.		
6.2	Output Voltage (Voh)	50Ω nominal load. (VDD - 1.03V) min.		
6.3	Duty Cycle	@ VDD-1.3V (45 to 55% over 600MHz)	48 to 52	%
6.4	Rise Time / Fall Time	80%/20%	0.6 max	ns
6.5	RMS Phase Jitter	Typical integrated 12kHz to 20MHz	0.5	ps

7.0 OUTPUT CHARACTERISTICS - LVDS ONLY

Line	Parameter	Test Condition	Value	Unit
7.1	Differential Output: Voltage Swing (Vod)		350	mV
7.2	Duty Cycle	Measured at 1.25V (45 to 55% over 150MHz)	48 to 52	%
7.3	Rise Time / Fall Time	RL = 100 Ω / CL = 10 pF	0.6 max	ns
7.4	RMS Phase Jitter	Typical integrated 12kHz to 20MHz	0.5	ps

8.0 SSB PHASE NOISE

Line	Parameter	Test Condition	Value	Unit
8.1	SSB Phase Noise Power Density @ 10 Hz Offset	Typical value for a 77.76 MHz VCXO @ 25 °C	-68	dBc/Hz
8.2	SSB Phase Noise Power Density @ 100 Hz Offset	Typical value for a 77.76 MHz VCXO @ 25 °C	-95	dBc/Hz
8.3	SSB Phase Noise Power Density @ 1kHz Offset	Typical value for a 77.76 MHz VCXO @ 25 °C	-120	dBc/Hz
8.4	SSB Phase Noise Power Density @ 10 kHz Offset	Typical value for a 77.76 MHz VCXO @ 25 °C	-125	dBc/Hz
8.5	SSB Phase Noise Power Density @ 100 kHz Offset	Typical value for a 77.76 MHz VCXO @ 25 °C	-128	dBc/Hz

9.0 SSB PHASE NOISE

Line	Parameter	Test Condition	Value	Unit
9.1	SSB Phase Noise Power Density @ 10 Hz Offset	Typical value for a 155.52 MHz VCXO @ 25°C	-62	dBc/Hz
9.2	SSB Phase Noise Power Density @ 100 Hz Offset	Typical value for a 155.52 MHz VCXO @ 25°C	-90	dBc/Hz
9.3	SSB Phase Noise Power Density @ 1 kHz Offset	Typical value for a 155.52 MHz VCXO @ 25°C	-112	dBc/Hz
9.4	SSB Phase Noise Power Density @ 10 kHz Offset	Typical value for a 155.52 MHz VCXO @ 25°C	-118	dBc/Hz
9.5	SSB Phase Noise Power Density @ 100 kHz Offset	Typical value for a 155.52 MHz VCXO @ 25°C	-120	dBc/Hz

10.0 SSB PHASE NOISE

Line	Parameter	Test Condition	Value	Unit
10.1	SSB Phase Noise Power Density @ 10 Hz Offset	Typical value for a 622.08 MHz VCXO @ 25°C	-48	dBc/Hz
10.2	SSB Phase Noise Power Density @ 100 Hz Offset	Typical value for a 622.08 MHz VCXO @ 25°C	-78	dBc/Hz
10.3	SSB Phase Noise Power Density @ 1 kHz Offset	Typical value for a 622.08 MHz VCXO @ 25°C	-101	dBc/Hz
10.4	SSB Phase Noise Power Density @ 10 kHz Offset	Typical value for a 622.08 MHz VCXO @ 25°C	-107	dBc/Hz
10.5	SSB Phase Noise Power Density @ 100 kHz Offset	Typical value for a 622.08 MHz VCXO @ 25°C	-108	dBc/Hz

11.0 PIN CONNECTIONS

Line	Parameter	Description
11.1	Pin 1	VCO
11.2	Pin 2	E/D* or NC
11.3	Pin 3	GND
11.4	Pin 4	OUTPUT
11.5	Pin 5	COMPLIMENTARY OUTPUT (LVPECL/LVDS only), or E/D*, or NC
11.6	Pin 6	VDD
11.7	* Output Enabled	>70% of VDD on E/D pin, or E/D pin left open (connected to internal pull-up resistor)
11.8	* Output Disabled	<30% of VDD on E/D pin, or E/D pin to GND

12.0 PACKAGE DETAILS

Line	Parameter	Description
12.1	Package	B
12.2	Top line	[R ######] Part identifier
12.3	Middle line	[######] Part information
12.4	Bottom line	[o FYWW] Pin 1, Manufacturing code, Year code* and Week code**
12.5	* Year code	A = 2010, B = 2011, C = 2012, D = 2013, ... Z = 2035
12.6	** Week Code	WW = 01 = Week of first Monday of the year

13.0 ENVIRONMENTAL SPECIFICATIONS

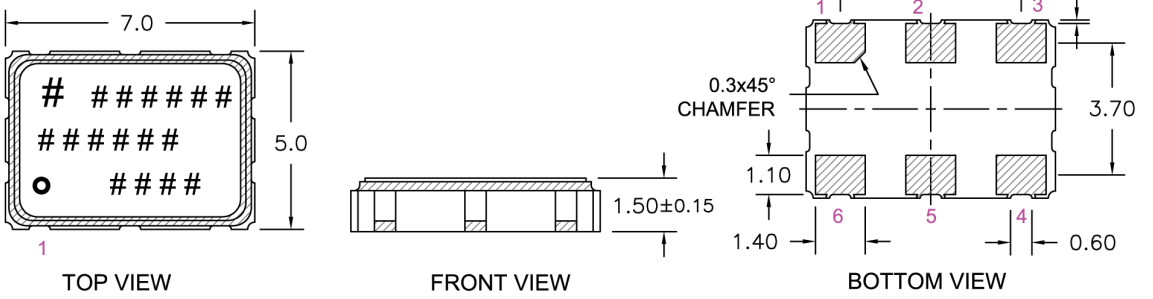
Line	Parameter	Description
13.1	Mechanical Shock	MIL-STD-883, Method 2002
13.2	Storage Temperature range	-55 to 125 °C
13.3	Humidity	After 48 hours at 85 °C ± 2 °C 85% relative humidity non-condensing
13.4	Thermal Shock	MIL-STD-883, Method 1011
13.5	Vibration	MIL-STD-883, Method 2007
13.6	Gross and Fine Leak	MIL-STD-883, Method 1014
13.7	RoHS Compliant	Yes

14.0 MANUFACTURING INFORMATION

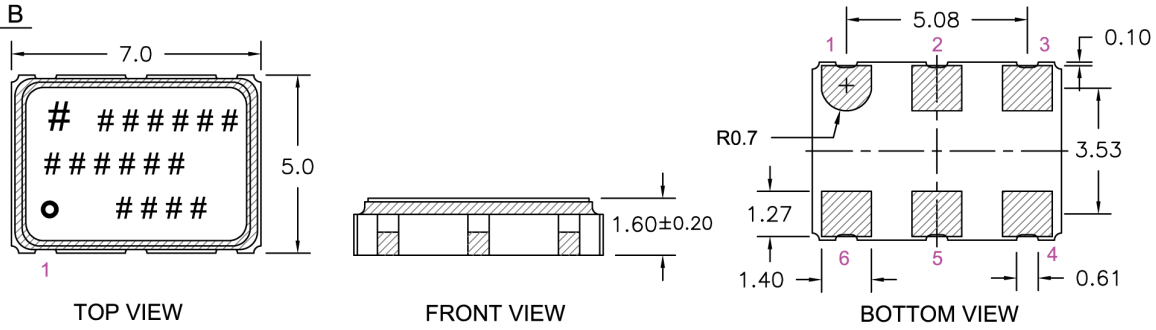
Line	Parameter	Description
14.1	Packaging Description	Tape and reel. Standard packing quantity is 2000 per reel
14.2	Reflow	Solder reflow process as per attached profile

Drawing Name: XO/VCXO 7050 Model Drawing

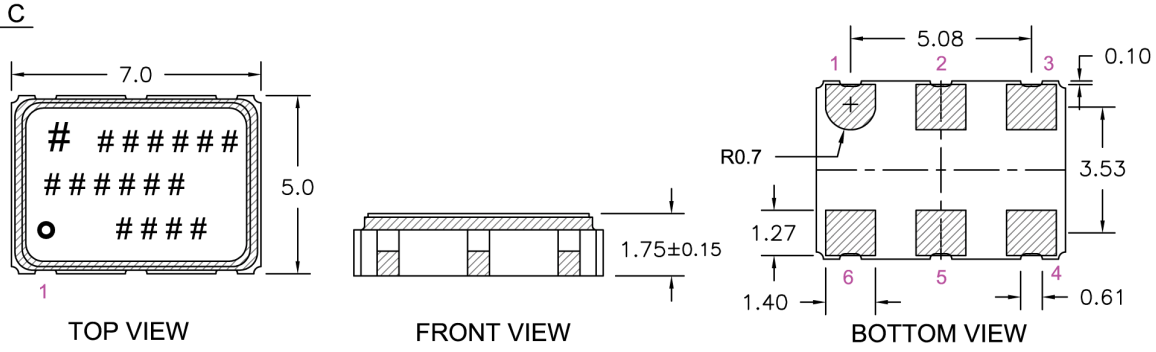
PACKAGE A



PACKAGE B

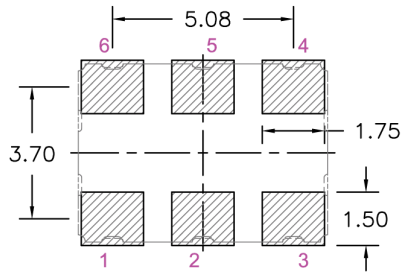


PACKAGE C



RECOMMENDED PAD LAYOUT

- TOP VIEW



NOTE :

1. PIN CONNECTIONS ARE DETAILED IN THE SPECIFICATION.
2. MARKING INFORMATION IS DETAILED IN THE SPECIFICATION.

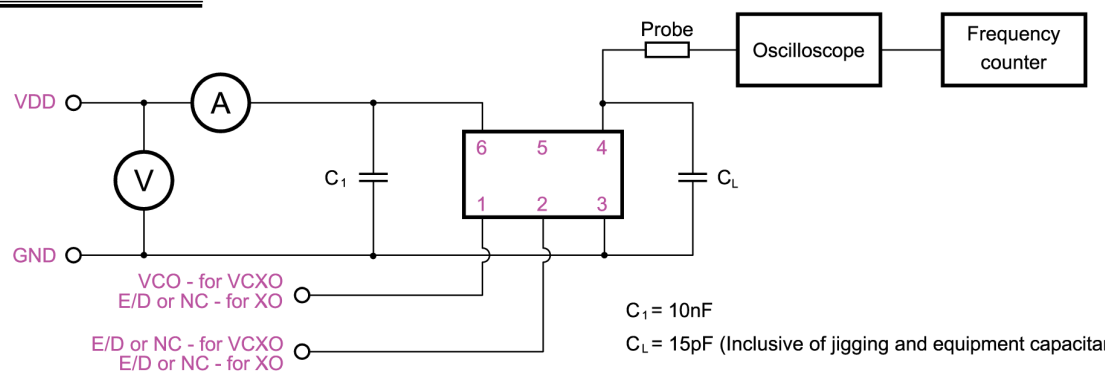
TITLE: XO/VCXO 7050 SERIES MODEL	FILENAME: CAT207	TOLERANCES:
RELATED DRAWINGS:	REVISION: J	XX =
	DATE: 03-Apr-12	X.X = ±0.15
	SCALE: 5 : 1	X.XX = ±0.10
	Millimetres	X.XXX =
		X° =
		Hole =

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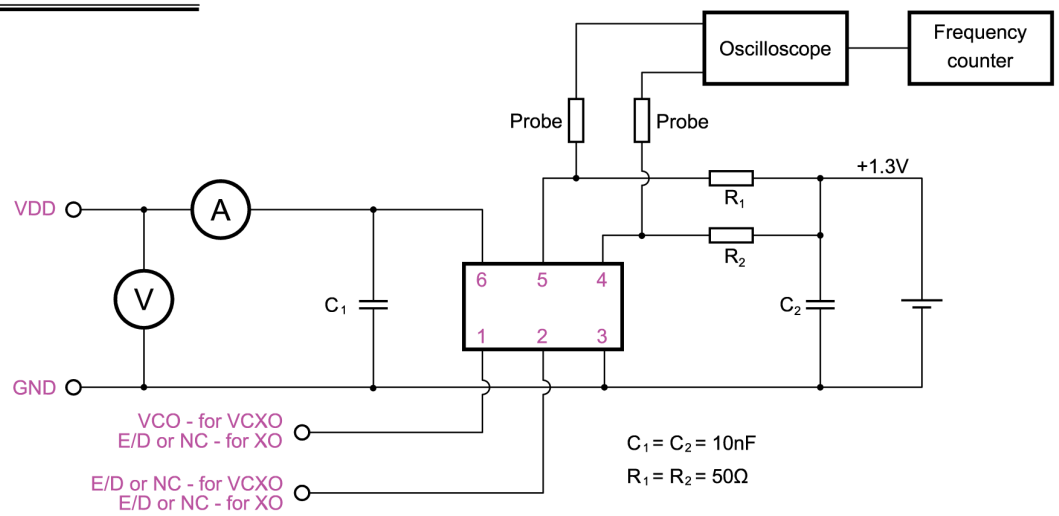
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Drawing Name: XO/VCXO 6 Pin Series Test Circuit

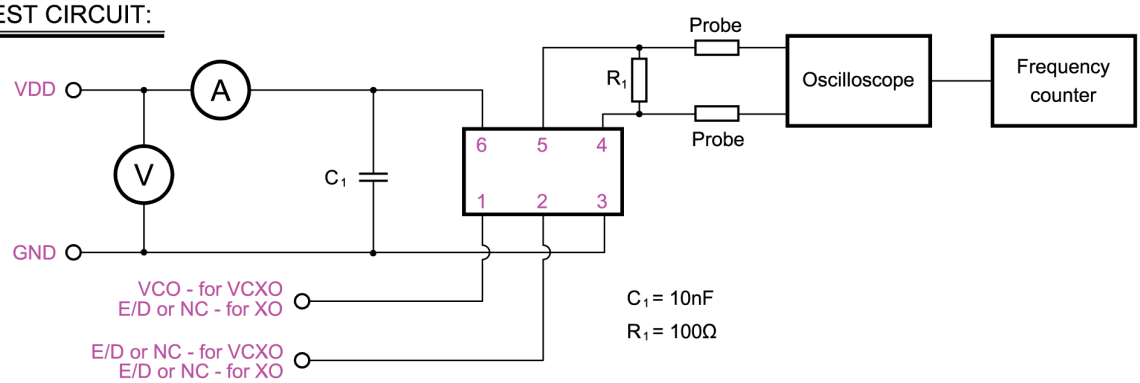
LVCMOS TEST CIRCUIT:



LVPECL TEST CIRCUIT:



LVDS TEST CIRCUIT:

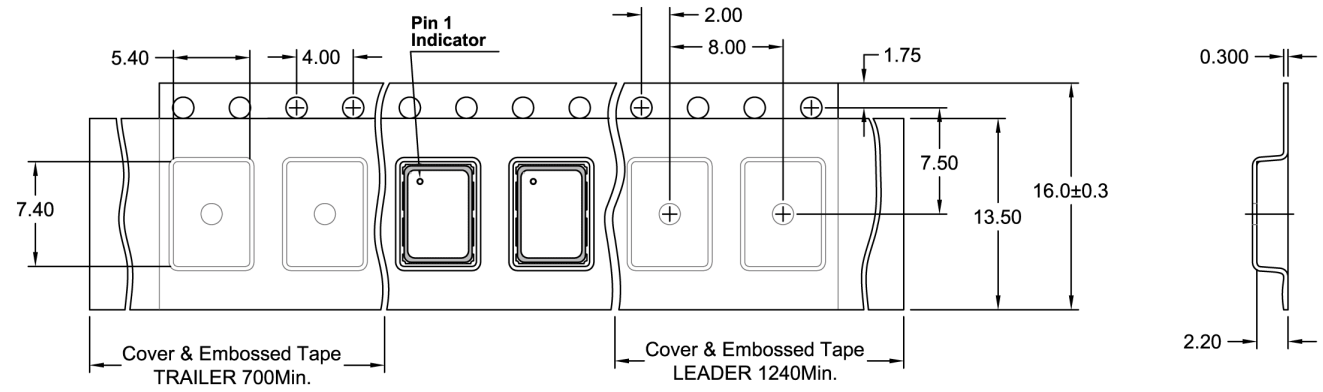


TITLE: XO/VCXO 6 PIN SERIES TEST CIRCUIT	FILENAME: CAT088
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	Millimetres

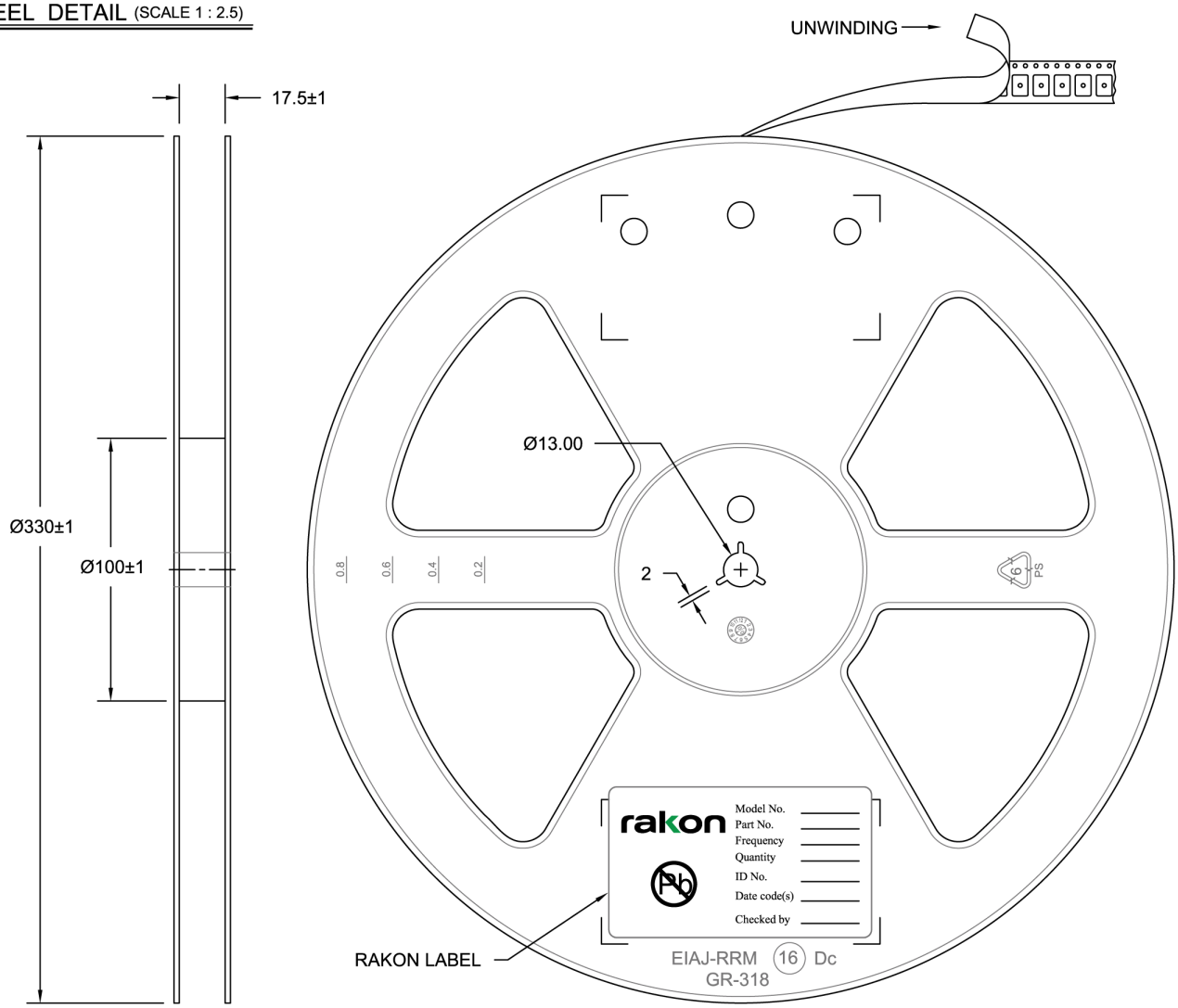
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Drawing Name: XO/VCXO 7050 Series Tape & Reel

TAPE DETAIL (SCALE 2 : 1)



REEL DETAIL (SCALE 1 : 2.5)

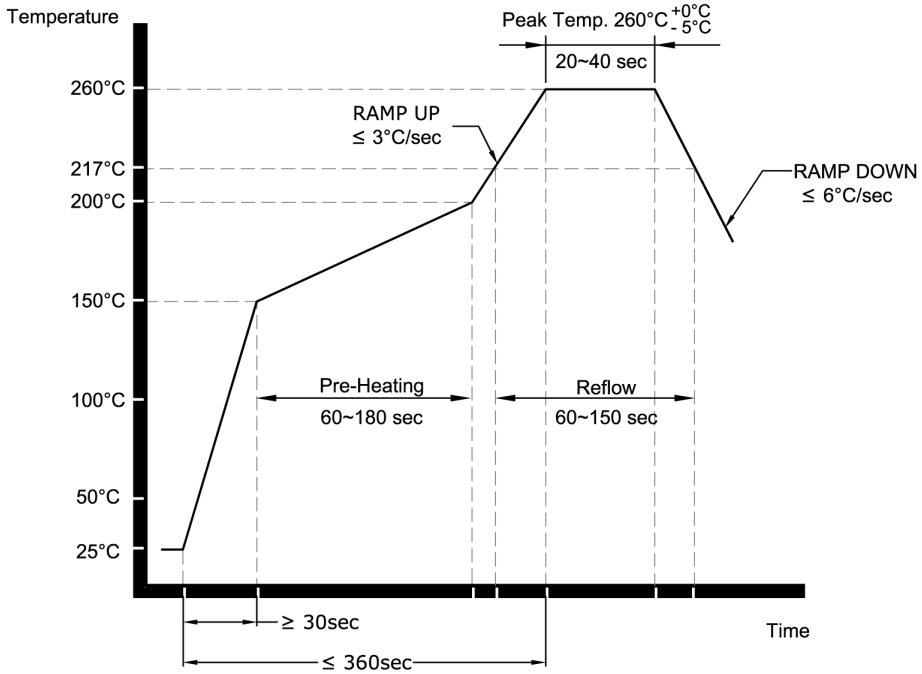


TITLE: XO/VCXO 7050 SERIES TAPE & REEL	FILENAME: CAT032	TOLERANCES:	
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	SCALE: 2 : 1	X.XX = ±0.10	
	Millimetres	X.XXX = ±0.05	
		X° =	
		Hole =	

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Drawing Name: Pb-Free Reflow



NOTE:
The product has been tested to withstand the Reflow Profile shown. The Reflow Profile used to solder Rakon products is determined by the solder paste Manufacturer's specification. It is recommended that the Reflow Profile used does not exceed the one shown above.

TITLE: Pb-FREE REFLOW	FILENAME: CAT541
RELATED DRAWINGS:	REVISION: B
	DATE: 05-Sep-11
	SCALE: NTS
	Millimetres

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