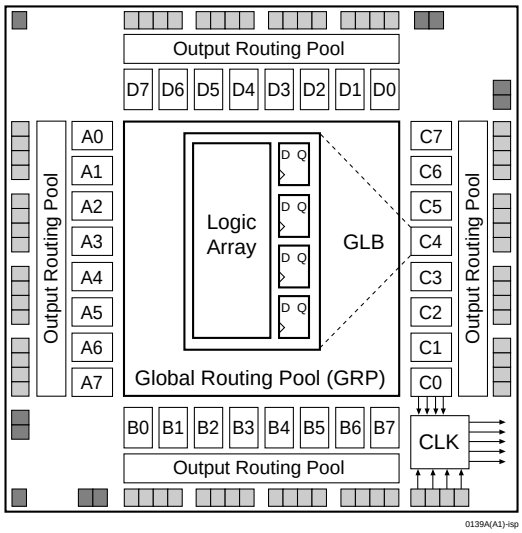
ispLSI® 1032EA

In-System Programmable High Density PLD

Features

- **HIGH DENSITY PROGRAMMABLE LOGIC**
  - **— 6000 PLD Gates**
  - **— 64 I/O Pins, Four Dedicated Inputs**
  - **— 192 Registers**
  - **— High Speed Global Interconnect**
  - **— Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.**
  - **— Small Logic Block Size for Random Logic**
  - **— Functionally and Pinout Compatible with ispLSI 1032E**
- **NEW FEATURES**
  - **— 100% IEEE 1149.1 Boundary Scan Testable**
  - **— ispJTAG™ In-System Programmable via IEEE 1149.1 (JTAG) Test Access Port**
  - **— User Selectable 3.3V or 5V I/O Supports Mixed-Voltage Systems (V_{CCIO} Pin)**
  - **— Open-Drain Output Option**
- **HIGH PERFORMANCE E^2CMOS® TECHNOLOGY**
  - **— f_{max} = 200 MHz Maximum Operating Frequency**
  - **— t_{pd} = 4.0 ns Propagation Delay**
  - **— TTL Compatible Inputs and Outputs**
  - **— Electrically Erasable and Reprogrammable**
  - **— Non-Volatile**
  - **— 100% Tested at Time of Manufacture**
  - **— Unused Product Term Shutdown Saves Power**
- **IN-SYSTEM PROGRAMMABLE**
  - **— Increased Manufacturing Yields, Reduced Time-to-Market and Improved Product Quality**
  - **— Reprogram Soldered Devices for Faster Prototyping**
- **OFFERS THE EASE OF USE AND FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEXIBILITY OF FIELD PROGRAMMABLE GATE ARRAYS**
  - **— Complete Programmable Device Can Combine Glue Logic and Structured Designs**
  - **— Enhanced Pin Locking Capability**
  - **— Four Dedicated Clock Input Pins**
  - **— Synchronous and Asynchronous Clocks**
  - **— Programmable Output Slew Rate Control to Minimize Switching Noise**
  - **— Flexible Pin Placement**
  - **— Optimized Global Routing Pool Provides Global Interconnectivity**
- **ispDesignEXPERT™ – LOGIC COMPILER AND COMPLETE ISP DEVICE DESIGN SYSTEMS FROM HDL SYNTHESIS THROUGH IN-SYSTEM PROGRAMMING**
  - **— Superior Quality of Results**
  - **— Tightly Integrated with Leading CAE Vendor Tools**
  - **— Productivity Enhancing Timing Analyzer, Explore Tools, Timing Simulator and ispANALYZER™**
  - **— PC and UNIX Platforms**

Functional Block Diagram



Description

The ispLSI 1032EA is a High Density Programmable Logic Device containing 192 Registers, 64 Universal I/O pins, four Dedicated Input pins, four Dedicated Clock Input pins and a Global Routing Pool (GRP). The GRP provides complete interconnectivity between all of these elements. The ispLSI 1032EA features 5V in-system programmability (ISP™) and in-system diagnostic capabilities via IEEE 1149.1 Test Access Port. The ispLSI 1032EA device offers non-volatile reprogrammability of the logic, as well as the interconnects to provide truly reconfigurable systems. A functional superset of the ispLSI 1032 architecture, the ispLSI 1032EA device adds user selectable 3.3V or 5V I/O and open-drain output options.

The basic unit of logic on the ispLSI 1032EA device is the Generic Logic Block (GLB). The GLBs are labeled A0, A1…D7 (Figure 1). There are a total of 32 GLBs in the ispLSI 1032EA device. Each GLB has 18 inputs, a programmable AND/OR/Exclusive OR array, and four outputs which can be configured to be either combinatorial or registered. Inputs to the GLB come from the GRP and dedicated inputs. All of the GLB outputs are brought back into the GRP so that they can be connected to the inputs of any other GLB on the device.

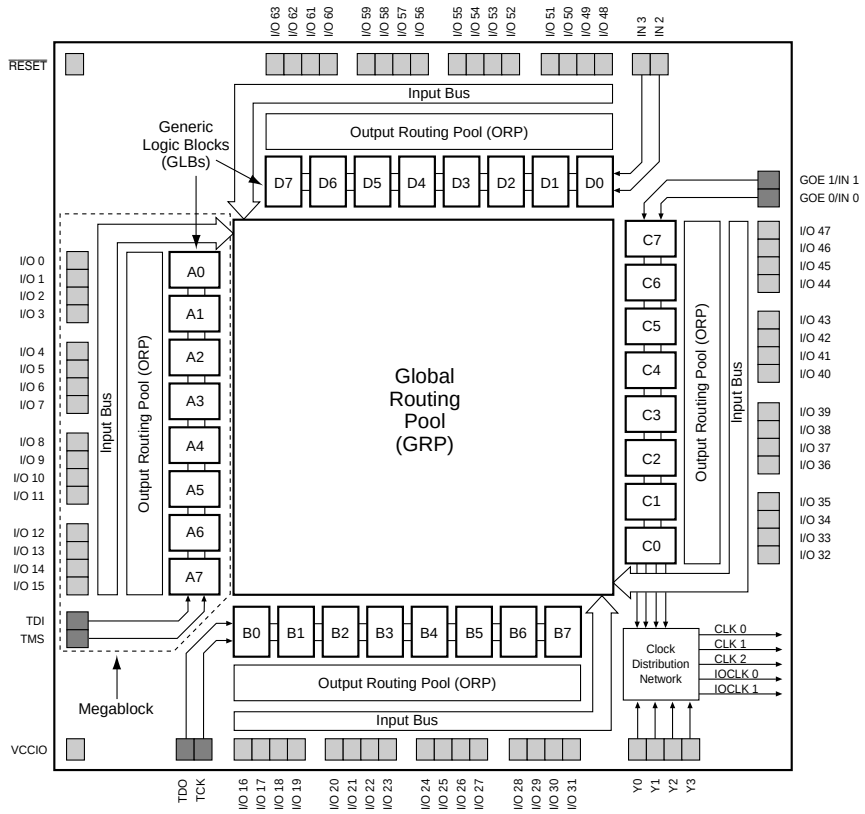
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January 2000

Functional Block Diagram

Figure 1. ispLSI 1032EA Functional Block Diagram



The device also has 64 I/O cells, each of which is directly connected to an I/O pin. Each I/O cell can be individually programmed to be a combinatorial input, registered input, latched input, output or bi-directional I/O pin with 3-state control. The signal levels are TTL compatible voltages and the output drivers can source 4 mA or sink 8 mA. Each output can be programmed independently for fast or slow output slew rate to minimize overall output switching noise. By connecting the VCCIO pin to a common 5V or 3.3V power supply, I/O output levels can be matched to 5V or 3.3V-compatible voltages.

Eight GLBs, 16 I/O cells, dedicated inputs (if available) and one ORP are connected together to make a Megablock (Figure 1). The outputs of the eight GLBs are connected to a set of 16 universal I/O cells by the ORP. Each ispLSI 1032EA device contains four Megablocks.

The GRP has, as its inputs, the outputs from all of the GLBs and all of the inputs from the bi-directional I/O cells. All of these signals are made available to the inputs of the GLBs. Delays through the GRP have been equalized to minimize timing skew.

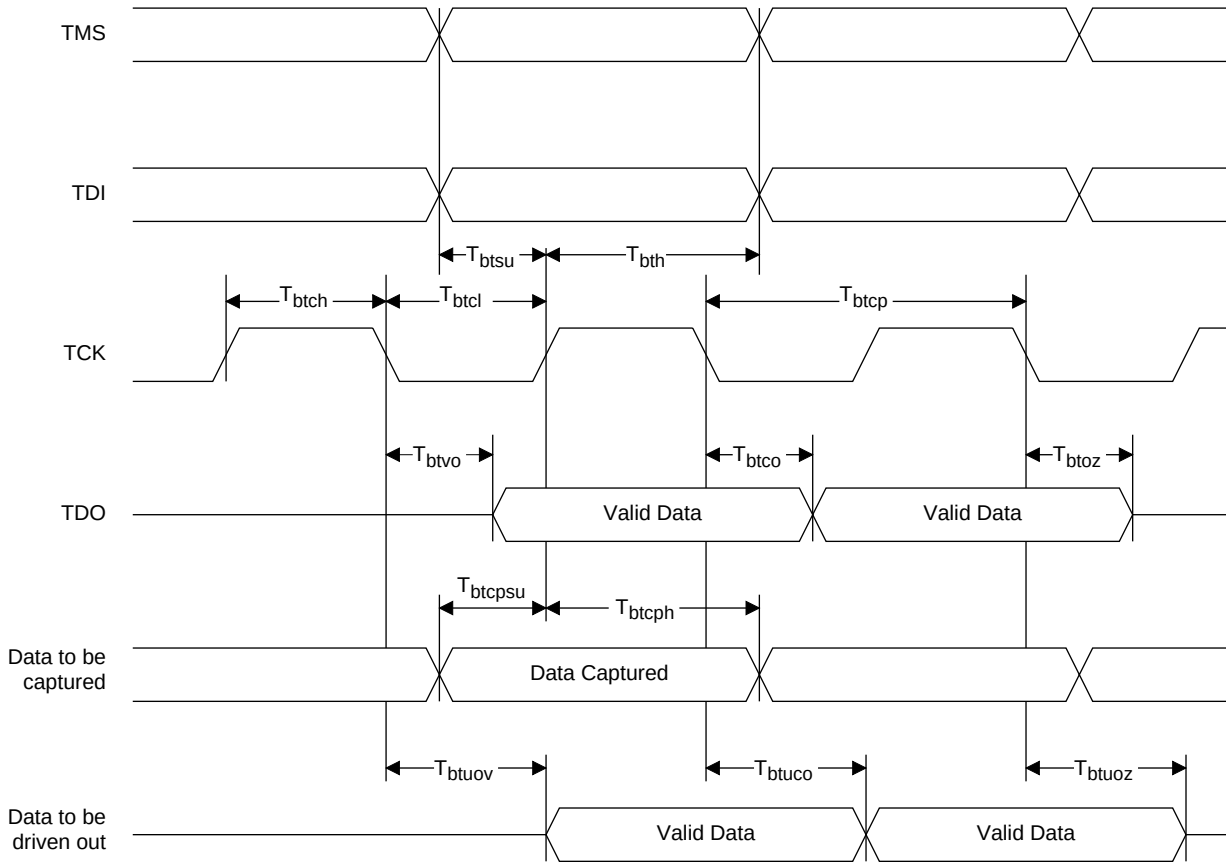
Clocks in the ispLSI 1032EA device are selected using the Clock Distribution Network. Four dedicated clock pins (Y0, Y1, Y2 and Y3) are brought into the distribution network, and five clock outputs (CLK 0, CLK 1, CLK 2, IOCLK 0 and IOCLK 1) are provided to route clocks to the GLBs and I/O cells. The Clock Distribution Network can also be driven from a special clock GLB (C0 on the ispLSI 1032EA device). The logic of this GLB allows the user to create an internal clock from a combination of internal signals within the device.

Programmable Open-Drain Outputs

In addition to the standard output configuration, the outputs of the ispLSI 1032EA are individually programmable, either as a standard totem-pole output or an open-drain output. The totem-pole output drives the specified Voh and Vol levels, whereas the open-drain output drives only the specified Vol. The Voh level on the open-drain output depends on the external loading and pull-up. This output configuration is controlled by a programmable fuse. The default configuration when the device is in bulk erased state is totem-pole configuration. The open-drain/totem-pole option is selectable through the ispDesignEXPERT software tools.

Boundary Scan

Figure 2. Boundary Scan Waveforms and Timing Specifications



Symbol	Parameter	Min	Max	Units
t_{btcp}	TCK [BSCAN test] clock pulse width	100	–	ns
t_{btch}	TCK [BSCAN test] pulse width high	50	–	ns
t_{btcl}	TCK [BSCAN test] pulse width low	50	–	ns
t_{btsu}	TCK [BSCAN test] setup time	20	–	ns
t_{bth}	TCK [BSCAN test] hold time	25	–	ns
t_{rf}	TCK [BSCAN test] rise and fall time	50	–	mV/ns
t_{btco}	TAP controller falling edge of clock to valid output	–	25	ns
t_{btoz}	TAP controller falling edge of clock to data output disable	–	25	ns
t_{btvo}	TAP controller falling edge of clock to data output enable	–	25	ns
t_{btcpsu}	BSCAN test Capture register setup time	40	–	ns
t_{btcph}	BSCAN test Capture register hold time	25	–	ns
t_{btuco}	BSCAN test Update reg, falling edge of clock to valid output	–	50	ns
t_{btuoz}	BSCAN test Update reg, falling edge of clock to output disable	–	50	ns
t_{btuov}	BSCAN test Update reg, falling edge of clock to output enable	–	50	ns

Absolute Maximum Ratings [1]

Supply Voltage V_{cc} ..... -0.5 to +7.0V

Input Voltage Applied ..... -2.5 to V_{CC} +1.0V

Off-State Output Voltage Applied ..... -2.5 to V_{CC} +1.0V

Storage Temperature ..... -65 to 150°C

Case Temp. with Power Applied ..... -55 to 125°C

Max. Junction Temp. (T_J) with Power Applied ... 150°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

DC Recommended Operating Conditions

SYMBOL	PARAMETER		MIN.	MAX.	UNITS
V_{CC}	Supply Voltage	Commercial T_A = 0°C to + 70°C	4.75	5.25	V
V_{CCIO}	Supply Voltage: Output Drivers	5V	4.75	5.25	V
		3.3V	3.0	3.6	V
V_{IL}	Input Low Voltage		0	0.8	V
V_{IH}	Input High Voltage		2.0	V_{cc}+1	V

Table 2-0005/1032EA

Capacitance (T_A=25°C, f=1.0 MHz)

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
C_1	Dedicated Input, I/O, Y1, Y2, Y3, Clock Capacitance (Commercial/Industrial)	8	pf	V_{CC} = 5.0V, V_{PIN} = 2.0V
C_2	Y0 Clock Capacitance	10	pf	V_{CC} = 5.0V, V_{PIN} = 2.0V

Table 2-0006/1032EA

Erase/Reprogram Specifications

PARAMETER	MINIMUM	MAXIMUM	UNITS
Erase/Reprogram Cycles	10000	–	Cycles

Table 2-0008/1032EA

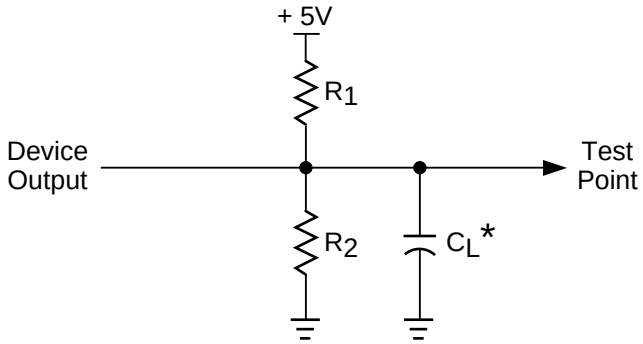
Switching Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Time 10% to 90%	1.5ns
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure 3

Table 2-0003/1032EA

3-state levels are measured 0.5V from steady-state active level.

Figure 3. Test Load



*C_L includes Test Fixture and Probe Capacitance.

0213a

Output Load Conditions (see Figure 3)

TEST CONDITION		R1	R2	CL
A		470Ω	390Ω	35pF
B	Active High	∞	390Ω	35pF
	Active Low	470Ω	390Ω	35pF
C	Active High to Z at V_{OH} -0.5V	∞	390Ω	5pF
	Active Low to Z at V_{OL} +0.5V	470Ω	390Ω	5pF

Table 2-0004/1032EA

DC Electrical Characteristics

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[3]	MAX.	UNITS
V_{OL}	Output Low Voltage	I_{OL} = 8 mA	—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4 mA	2.4	—	—	V
I_{IL}	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (Max.)	—	—	-10	µA
I_{IH}	Input or I/O High Leakage Current	$(V_{CCIO} - 0.2)V \le V_{IN} \le V_{CCIO}$	—	—	10	µA
		$V_{CCIO} \le V_{IN} \le 5.25V$	—	—	10	µA
I_{IL-PU}	I/O Active Pull-Up Current	$0V \le V_{IN} \le 2.0V$	-10	—	-250	µA
I_{OS}[1]	Output Short Circuit Current	V_{CCIO} = 5.0V or 3.3V, V_{OUT} = 0.5V	—	—	-240	mA
I_{CC}[2, 4, 5]	Operating Power Supply Current	V_{IL} = 0.0V, V_{IH} = 3.0V f_{TOGGLE} = 1 MHz	—	153	—	mA

Table 2-0007/1032EA

1. One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems by tester ground degradation. Characterized but not 100% tested.
2. Meaured using eight 16-bit counters.
3. Typical values are at V_{CC} = 5V and T_A = 25°C.
4. Unused inputs held at 0.0V.
5. Maximum I_{CC} varies widely with specific device configuration and operating frequency. Refer to the Power Consumption section of this data sheet and the Thermal Management section of the Lattice Semiconductor Data Book CD-ROM to estimate maximum I_{CC}.

External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST COND.[4]	#[2]	DESCRIPTION[1]	-200		-170		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{pd1}	A	1	Data Propagation Delay, 4PT Bypass, ORP Bypass	—	4.0	—	5.0	ns
t_{pd2}	A	2	Data Propagation Delay, Worst Case Path	—	5.5	—	7.0	ns
f_{max} (Int.)	A	3	Clock Frequency with Internal Feedback[3]	200	—	170	—	MHz
f_{max} (Ext.)	—	4	Clock Frequency with External Feedback $\left(\frac{1}{tsu2 + tco1}\right)$	167	—	125	—	MHz
f_{max} (Tog.)	—	5	Clock Frequency, Max. Toggle $\left(\frac{1}{twh + twl}\right)$	250	—	222	—	MHz
t_{su1}	—	6	GLB Reg. Setup Time before Clock,4 PT Bypass	3.0	—	3.5	—	ns
t_{co1}	A	7	GLB Reg. Clock to Output Delay, ORP Bypass	—	2.5	—	3.5	ns
t_{h1}	—	8	GLB Reg. Hold Time after Clock, 4 PT Bypass	0.0	—	0.0	—	ns
t_{su2}	—	9	GLB Reg. Setup Time before Clock	3.5	—	4.5	—	ns
t_{co2}	—	10	GLB Reg. Clock to Output Delay	—	3.0	—	4.5	ns
t_{h2}	—	11	GLB Reg. Hold Time after Clock	0.0	—	0.0	—	ns
t_{r1}	A	12	Ext. Reset Pin to Output Delay	—	5.5	—	7.0	ns
t_{rw1}	—	13	Ext. Reset Pulse Duration	3.5	—	4.0	—	ns
t_{ptoeen}	B	14	Input to Output Enable	—	7.0	—	9.0	ns
$t_{ptoedis}$	C	15	Input to Output Disable	—	7.0	—	9.0	ns
t_{goeen}	B	16	Global OE Output Enable	—	4.5	—	6.5	ns
t_{goedis}	C	17	Global OE Output Disable	—	4.5	—	6.5	ns
t_{wh}	—	18	External Synchronous Clock Pulse Duration, High	2.0	—	2.25	—	ns
t_{wl}	—	19	External Synchronous Clock Pulse Duration, Low	2.0	—	2.25	—	ns
t_{su3}	—	20	I/O Reg. Setup Time before Ext. Sync Clock (Y2, Y3)	3.0	—	3.0	—	ns
t_{h3}	—	21	I/O Reg. Hold Time after Ext. Sync. Clock (Y2, Y3)	0.0	—	0.0	—	ns

Table 2-0030A/1032EA

1. Unless noted otherwise, all parameters use the GRP, 20 PTXOR path, ORP and Y0 clock.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-bit counter using GRP feedback.
4. Reference Switching Test Conditions section.

External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST COND.[4]	#[2]	DESCRIPTION[1]	-125		-100		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{pd1}	A	1	Data Propagation Delay, 4PT Bypass, ORP Bypass	–	7.5	–	10.0	ns
t_{pd2}	A	2	Data Propagation Delay, Worst Case Path	–	10.0	–	12.5	ns
f_{max} (Int.)	A	3	Clock Frequency with Internal Feedback[3]	125	–	100	–	MHz
f_{max} (Ext.)	–	4	Clock Frequency with External Feedback $\left(\frac{1}{t_{su2} + t_{co1}}\right)$	100	–	77	–	MHz
f_{max} (Tog.)	–	5	Clock Frequency, Max. Toggle $\left(\frac{1}{t_{wh} + t_{wl}}\right)$	167	–	125	–	MHz
t_{su1}	–	6	GLB Reg. Setup Time before Clock,4 PT Bypass	4.5	–	6.0	–	ns
t_{co1}	A	7	GLB Reg. Clock to Output Delay, ORP Bypass	–	4.5	–	6.0	ns
t_{h1}	–	8	GLB Reg. Hold Time after Clock, 4 PT Bypass	0.0	–	0.0	–	ns
t_{su2}	–	9	GLB Reg. Setup Time before Clock	5.5	–	7.0	–	ns
t_{co2}	–	10	GLB Reg. Clock to Output Delay	–	5.5	–	7.0	ns
t_{h2}	–	11	GLB Reg. Hold Time after Clock	0.0	–	0.0	–	ns
t_{r1}	A	12	Ext. Reset Pin to Output Delay	–	10.0	–	13.5	ns
t_{rw1}	–	13	Ext. Reset Pulse Duration	5.0	–	6.5	–	ns
t_{ptoeen}	B	14	Input to Output Enable	–	12.0	–	15.0	ns
$t_{ptoedis}$	C	15	Input to Output Disable	–	12.0	–	15.0	ns
t_{goeen}	B	16	Global OE Output Enable	–	7.0	–	9.0	ns
t_{goedis}	C	17	Global OE Output Disable	–	7.0	–	9.0	ns
t_{wh}	–	18	External Synchronous Clock Pulse Duration, High	3.0	–	4.0	–	ns
t_{wl}	–	19	External Synchronous Clock Pulse Duration, Low	3.0	–	4.0	–	ns
t_{su3}	–	20	I/O Reg. Setup Time before Ext. Sync Clock (Y2, Y3)	3.0	–	3.5	–	ns
t_{h3}	–	21	I/O Reg. Hold Time after Ext. Sync. Clock (Y2, Y3)	0.0	–	0.0	–	ns

Table 2-0030B/1032EA

1. Unless noted otherwise, all parameters use the GRP, 20 PTXOR path, ORP and Y0 clock.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-bit counter using GRP feedback.
4. Reference Switching Test Conditions section.

Internal Timing Parameters[1]

PARAM.	#[2]	DESCRIPTION	-200		-170		UNITS
			MIN.	MAX.	MIN.	MAX.	
Inputs							
t_{iobp}	22	I/O Register Bypass	—	0.3	—	0.3	ns
t_{iolat}	23	I/O Latch Delay	—	4.0	—	4.0	ns
t_{iosu}	24	I/O Register Setup Time before Clock	3.0	—	3.0	—	ns
t_{ioh}	25	I/O Register Hold Time after Clock	0.0	—	0.0	—	ns
t_{ioco}	26	I/O Register Clock to Out Delay	—	4.0	—	4.6	ns
t_{ior}	27	I/O Register Reset to Out Delay	—	4.0	—	4.6	ns
t_{din}	28	Dedicated Input Delay	—	1.1	—	1.8	ns
GRP							
t_{grp1}	29	GRP Delay, 1 GLB Load	—	1.3	—	1.4	ns
t_{grp4}	30	GRP Delay, 4 GLB Loads	—	1.5	—	1.6	ns
t_{grp8}	31	GRP Delay, 8 GLB Loads	—	1.7	—	1.8	ns
t_{grp16}	32	GRP Delay, 16 GLB Loads	—	2.1	—	2.2	ns
t_{grp32}	33	GRP Delay, 32 GLB Loads	—	2.9	—	3.0	ns
GLB							
t_{4ptbpc}	34	4 ProductTerm Bypass Path Delay (Combinatorial)	—	1.4	—	2.1	ns
t_{4ptbpr}	35	4 Product Term Bypass Path Delay (Registered)	—	1.5	—	2.0	ns
t_{1ptxor}	36	1 ProductTerm/XOR Path Delay	—	1.6	—	2.3	ns
$t_{20ptxor}$	37	20 Product Term/XOR Path Delay	—	1.6	—	2.2	ns
t_{xoradj}	38	XOR Adjacent Path Delay[3]	—	1.6	—	2.2	ns
t_{gbp}	39	GLB Register Bypass Delay	—	0.8	—	1.0	ns
t_{gsu}	40	GLB Register Setup Time before Clock	0.3	—	0.3	—	ns
t_{gh}	41	GLB Register Hold Time after Clock	1.0	—	2.0	—	ns
t_{gco}	42	GLB Register Clock to Output Delay	—	1.1	—	1.4	ns
t_{gro}	43	GLB Register Reset to Output Delay	—	4.2	—	4.7	ns
t_{ptre}	44	GLB Product Term Reset to Register Delay	—	2.2	—	2.7	ns
t_{ptoe}	45	GLB Product Term Output Enable to I/O Cell Delay	—	2.3	—	3.6	ns
t_{ptck}	46	GLB Product Term Clock Delay	1.2	2.2	1.7	2.7	ns
t_{gfb}	47	GLB Feedback Delay	—	0.1	—	0.1	ns
ORP							
t_{orp}	48	ORP Delay	—	0.6	—	1.0	ns
t_{orpbp}	49	ORP Bypass Delay	—	0.1	—	0.1	ns

Table 2-0036A/1032EA

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR adjacent path can only be used by hard macros.

Internal Timing Parameters[1]

PARAM.	#	DESCRIPTION	-200		-170		UNITS
			MIN.	MAX.	MIN.	MAX.	
Outputs							
t_{ob}	50	Output Buffer Delay	—	0.7	—	0.9	ns
t_{sl}	51	Output Buffer Delay, Slew Limited Adder	—	5.0	—	5.0	ns
t_{oen}	52	I/O Cell OE to Output Enabled	—	2.9	—	3.3	ns
t_{odis}	53	I/O Cell OE to Output Disabled	—	2.9	—	3.3	ns
t_{goe}	54	Global OE	—	1.6	—	2.6	ns
Clocks							
t_{gy0}	55	Clock Delay, Y0 to Global GLB Clock Line (Ref. clk)	0.6	0.6	0.9	0.9	ns
$t_{gy1/2}$	56	Clock Delay, Y1 or Y2 to Global GLB Clock Line	0.9	0.9	0.9	0.9	ns
t_{gcp}	57	Clock Delay, Clock GLB to Global GLB Clock Line	0.8	1.8	0.8	1.8	ns
$t_{ioy2/3}$	58	Clock Delay, Y2 or Y3 to I/O Cell Global Clock Line	0.0	0.0	0.0	0.0	ns
t_{iocp}	59	Clock Delay, Clock GLB to I/O Cell Global Clock Line	0.8	2.8	0.8	2.8	ns
Global Reset							
t_{gr}	60	Global Reset to GLB and I/O Registers	—	0.0	—	0.4	ns

1. Internal Timing Parameters are not tested and are for reference only.

Table 2-0037A/1032EA

Internal Timing Parameters[1]

PARAM.	#[2]	DESCRIPTION	-125		-100		UNITS
			MIN.	MAX.	MIN.	MAX.	
Inputs							
t_{iobp}	22	I/O Register Bypass	–	0.3	–	0.4	ns
t_{iolat}	23	I/O Latch Delay	–	4.0	–	4.0	ns
t_{iosu}	24	I/O Register Setup Time before Clock	3.0	–	3.4	–	ns
t_{ioh}	25	I/O Register Hold Time after Clock	0.0	–	0.0	–	ns
t_{ioco}	26	I/O Register Clock to Out Delay	–	4.6	–	5.0	ns
t_{ior}	27	I/O Register Reset to Out Delay	–	4.6	–	5.0	ns
t_{din}	28	Dedicated Input Delay	–	1.9	–	2.2	ns
GRP							
t_{grp1}	29	GRP Delay, 1 GLB Load	–	1.7	–	2.1	ns
t_{grp4}	30	GRP Delay, 4 GLB Loads	–	1.9	–	2.3	ns
t_{grp8}	31	GRP Delay, 8 GLB Loads	–	2.1	–	2.5	ns
t_{grp16}	32	GRP Delay, 16 GLB Loads	–	2.5	–	2.9	ns
t_{grp32}	33	GRP Delay, 32 GLB Loads	–	3.3	–	3.7	ns
GLB							
t_{4ptbpc}	34	4 Product Term Bypass Path Delay (Combinatorial)	–	3.4	–	4.9	ns
t_{4ptbpr}	35	4 Product Term Bypass Path Delay (Registered)	–	3.1	–	4.9	ns
t_{1ptxor}	36	1 Product Term/XOR Path Delay	–	3.6	–	4.3	ns
$t_{20ptxor}$	37	20 Prod. Term/XOR Path Delay	–	3.6	–	4.3	ns
t_{xoradj}	38	XOR Adjacent Path Delay[3]	–	3.6	–	4.3	ns
t_{gbp}	39	GLB Register Bypass Delay	–	1.2	–	2.1	ns
t_{gsu}	40	GLB Register Setup Time before Clock	0.3	–	0.3	–	ns
t_{gh}	41	GLB Register Hold Time after Clock	3.5	–	4.8	–	ns
t_{gco}	42	GLB Register Clock to Output Delay	–	1.4	–	1.7	ns
t_{gro}	43	GLB Register Reset to Output Delay	–	4.9	–	5.0	ns
t_{ptre}	44	GLB Product Term Reset to Register Delay	–	3.8	–	4.5	ns
t_{ptoe}	45	GLB Product Term Output Enable to I/O Cell Delay	–	5.2	–	7.2	ns
t_{ptck}	46	GLB Product Term Clock Delay	2.8	3.9	3.5	4.7	ns
t_{gfb}	47	GLB Feedback Delay	–	0.6	–	1.4	ns
ORP							
t_{orp}	48	ORP Delay	–	1.3	–	1.4	ns
t_{orpbp}	49	ORP Bypass Delay	–	0.2	–	0.4	ns

Table 2-0036B/1032EA

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR adjacent path can only be used by hard macros.

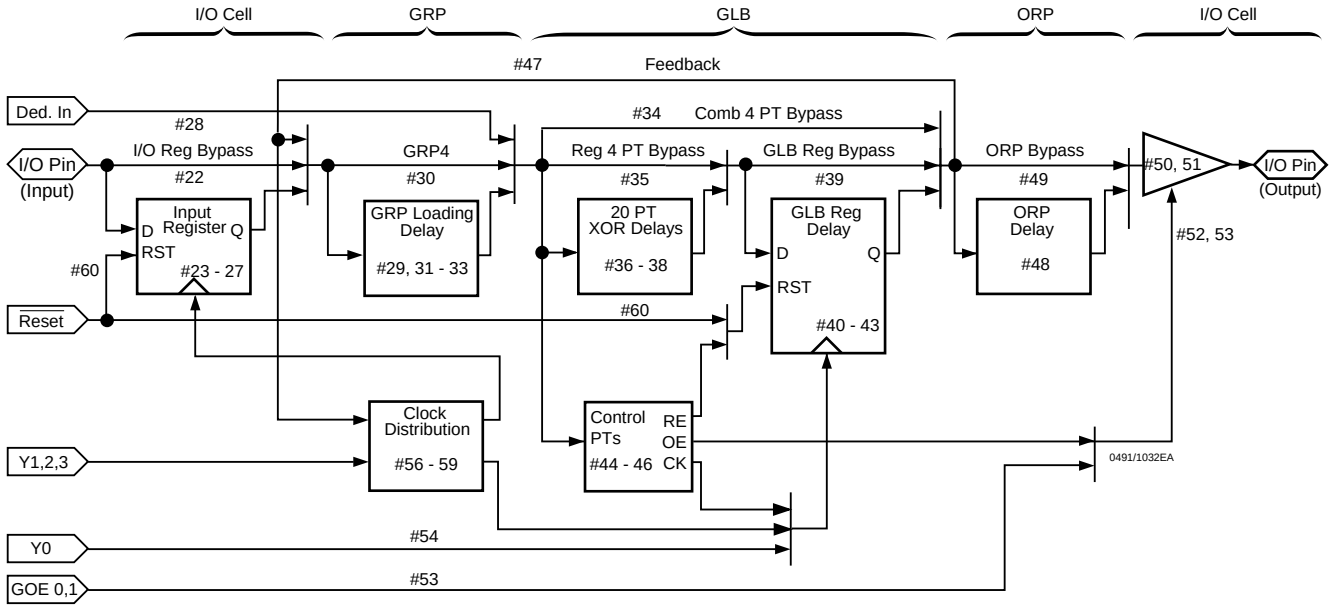
Internal Timing Parameters[1]

PARAM.	#	DESCRIPTION	-125		-100		UNITS
			MIN.	MAX.	MIN.	MAX.	
Outputs							
t_{ob}	50	Output Buffer Delay	—	1.7	—	2.0	ns
t_{sl}	51	Output Buffer Delay, Slew Limited Adder	—	5.0	—	5.0	ns
t_{oen}	52	I/O Cell OE to Output Enabled	—	4.0	—	5.1	ns
t_{odis}	53	I/O Cell OE to Output Disabled	—	4.0	—	5.1	ns
t_{goe}	54	Global OE	—	3.0	—	3.9	ns
Clocks							
t_{gy0}	55	Clock Delay, Y0 to Global GLB Clk Line (Ref. Clock)	1.1	1.1	1.9	1.9	ns
$t_{gy1/2}$	56	Clock Delay, Y1 or Y2 to Global GLB Clock Line	0.9	0.9	1.5	1.5	ns
t_{gcp}	57	Clock Delay, Clock GLB to Global GLB Clock Line	0.8	1.8	0.8	1.8	ns
$t_{ioy2/3}$	58	Clock Delay, Y2 or Y3 to I/O Cell Global Clock Line	0.0	0.0	0.0	0.0	ns
t_{iocp}	59	Clock Delay, Clock GLB to I/O Cell Global Clock Line	0.8	2.8	0.8	2.8	ns
Global Reset							
t_{gr}	60	Global Reset to GLB and I/O Registers	—	2.1	—	5.1	ns

1. Internal Timing Parameters are not tested and are for reference only.

Table 2-0037B/1032EA

ispLSI 1032EA Timing Model



Derivations of tsu, th and tco from the Product Term Clock[1]

tsu = Logic + Reg su - Clock (min)
= (**t**iobp + **t**grp4 + **t**20ptxor) + (**t**gsu) - (**t**iobp + **t**grp4 + **t**ptck(min))
= (#22 + #30 + #37) + (#40) - (#22 + #30 + #46)
0.7 = (0.3 + 1.5 + 1.6) + (0.3) - (0.3 + 1.5 + 1.2)

th = Clock (max) + Reg h - Logic
= (**t**iobp + **t**grp4 + **t**ptck(max)) + (**t**gh) - (**t**iobp + **t**grp4 + **t**20ptxor)
= (#22 + #30 + #46) + (#41) - (#22 + #30 + #37)
1.6 = (0.3 + 1.5 + 2.2) + (1.0) - (0.3 + 1.5 + 1.6)

tco = Clock (max) + Reg co + Output
= (**t**iobp + **t**grp4 + **t**ptck(max)) + (**t**gco) + (**t**orp + **t**ob)
= (#22 + #30 + #46) + (#42) + (#48 + #50)
6.7 = (0.3 + 1.5 + 2.2) + (1.4) + (0.6 + 0.7)

Derivations of tsu, th and tco from the Clock GLB[1]

tsu = Logic + Reg (setup) - Clock (min)
= (**t**iobp + **t**grp4 + **t**20ptxor) + (**t**gsu) - (**t**gy0(min) + **t**gco + **t**gcp(min))
= (#22 + #30 + #37) + (#40) - (#55 + #42 + #57)
0.9 = (0.3 + 1.5 + 1.6) + (0.3) - (0.6 + 1.4 + 0.8)

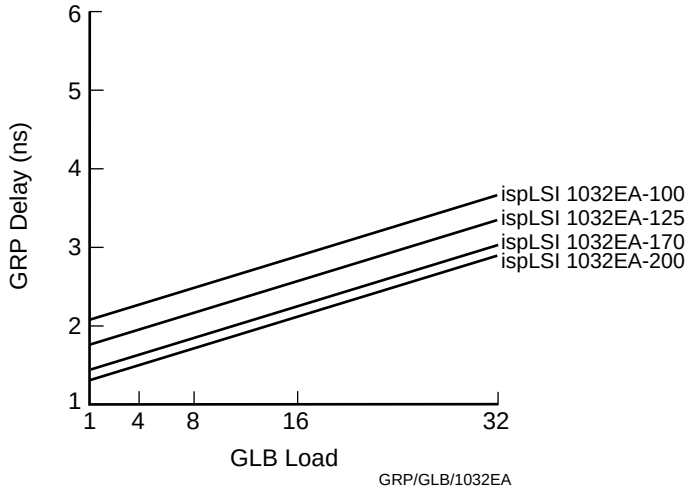
th = Clock (max) + Reg (hold) - Logic
= (**t**gy0(max) + **t**gco + **t**gcp(max)) + (**t**gh) - (**t**iobp + **t**grp4 + **t**20ptxor)
= (#55 + #42 + #57) + (#41) - (#22 + #30 + #37)
1.1 = (0.6 + 1.1 + 1.8) + (1.0) - (0.3 + 1.5 + 1.6)

tco = Clock (max) + Reg (clock-to-out) + Output
= (**t**gy0(max) + **t**gco + **t**gcp(max)) + (**t**gco) + (**t**orp + **t**ob)
= (#55 + #42 + #57) + (#42) + (#48 + #50)
5.9 = (0.6 + 1.1 + 1.8) + (1.1) + (0.6 + 0.7)

1. Calculations are based upon timing specifications for the ispLSI 1032EA-200.

Table 2-0042a/1032EA

Maximum GRP Delay vs GLB Loads

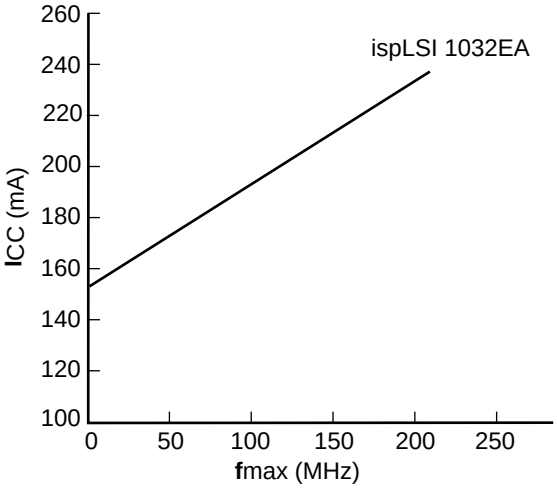


GRP/GLB/1032EA

Power Consumption

Power consumption in the ispLSI 1032EA device depends on two primary factors: the speed at which the device is operating, and the number of product terms used. Figure 4 shows the relationship between power and operating speed.

Figure 4. Typical Device Power Consumption vs fmax



Notes: Configuration of eight 16-bit counters
Typical current at 5V, 25°C

Icc can be estimated for the ispLSI 1032EA using the following equation:

Icc = 20mA + (# of PTs * .52) + (# of nets * Max Freq * .003)

Where:

# of PTs = Number of Product Terms used in design
# of nets = Number of Signals used in device
Max freq = Highest Clock Frequency to the device (in MHz)

The Icc estimate is based on typical conditions (Vcc = 5.0V, room temperature) and an assumption of four GLB loads on average exists. These values are for estimates only. Since the value of Icc is sensitive to operating conditions and the program in the device, the actual Icc should be verified.

0127/1032EA

Pin Description

NAME	TQFP PIN NUMBERS	DESCRIPTION
I/O 0 - I/O 3 I/O 4 - I/O 7 I/O 8 - I/O 11 I/O 12 - I/O 15 I/O 16 - I/O 19 I/O 20 - I/O 23 I/O 24 - I/O 27 I/O 28 - I/O 31 I/O 32 - I/O 35 I/O 36 - I/O 39 I/O 40 - I/O 43 I/O 44 - I/O 47 I/O 48 - I/O 51 I/O 52 - I/O 55 I/O 56 - I/O 59 I/O 60 - I/O 63	17, 18, 19, 20, 21, 22, 23, 28, 29, 30, 31, 32, 33, 34, 35, 36, 40, 41, 42, 43, 44, 45, 46, 47, 48, 53, 54, 55, 56, 57, 58, 59, 67, 68, 69, 70, 71, 72, 73, 78, 79, 80, 81, 82, 83, 84, 85, 86, 90, 91, 92, 93, 94, 95, 96, 97, 98, 3, 4, 5, 6, 7, 8, 9	Input/Output Pins - These are the general purpose I/O pins used by the logic array.
GOE 0/IN 0[2]	66	This is a dual function pin. It can be used either as Global Output Enable for all I/O cells or it can be used as a dedicated input pin.
GOE 1/IN 1[2]	87	This is a dual function pin. It can be used either as Global Output Enable for all I/O cells or it can be used as a dedicated input pin.
IN 2, IN 3	89, 10	Dedicated input pins to the device.
TDI	16	Input - Functions as an input pin to load programming data into the device and also used as one of the two control pins for the ispJTAG state machine.
TMS	37	Input - Controls the operation of the ISP state machine.
TDO	39	Output - Functions as an output pin to read serial shift register data.
TCK	60	Input - Functions as a clock pin for the Serial Shift Register.
$\overline{\text{RESET}}$	15	Active Low (0) Reset pin which resets all of the GLB and I/O registers in the device.
Y0	11	Dedicated Clock input. This clock input is connected to one of the clock inputs of all of the GLBs on the device.
Y1	65	Dedicated Clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB on the device.
Y2	62	Dedicated Clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB and/or any I/O cell on the device.
Y3	61	Dedicated Clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any I/O cell on the device.
GND	13, 38, 63, 88	Ground (GND)
VCC	12, 64	Vcc
VCCIO	14	Supply voltage for output drivers, 5V or 3.3V.
NC[1]	1, 2, 24, 25, 26, 27, 49, 50, 51, 52, 74, 75, 76, 77, 99, 100	No connect.

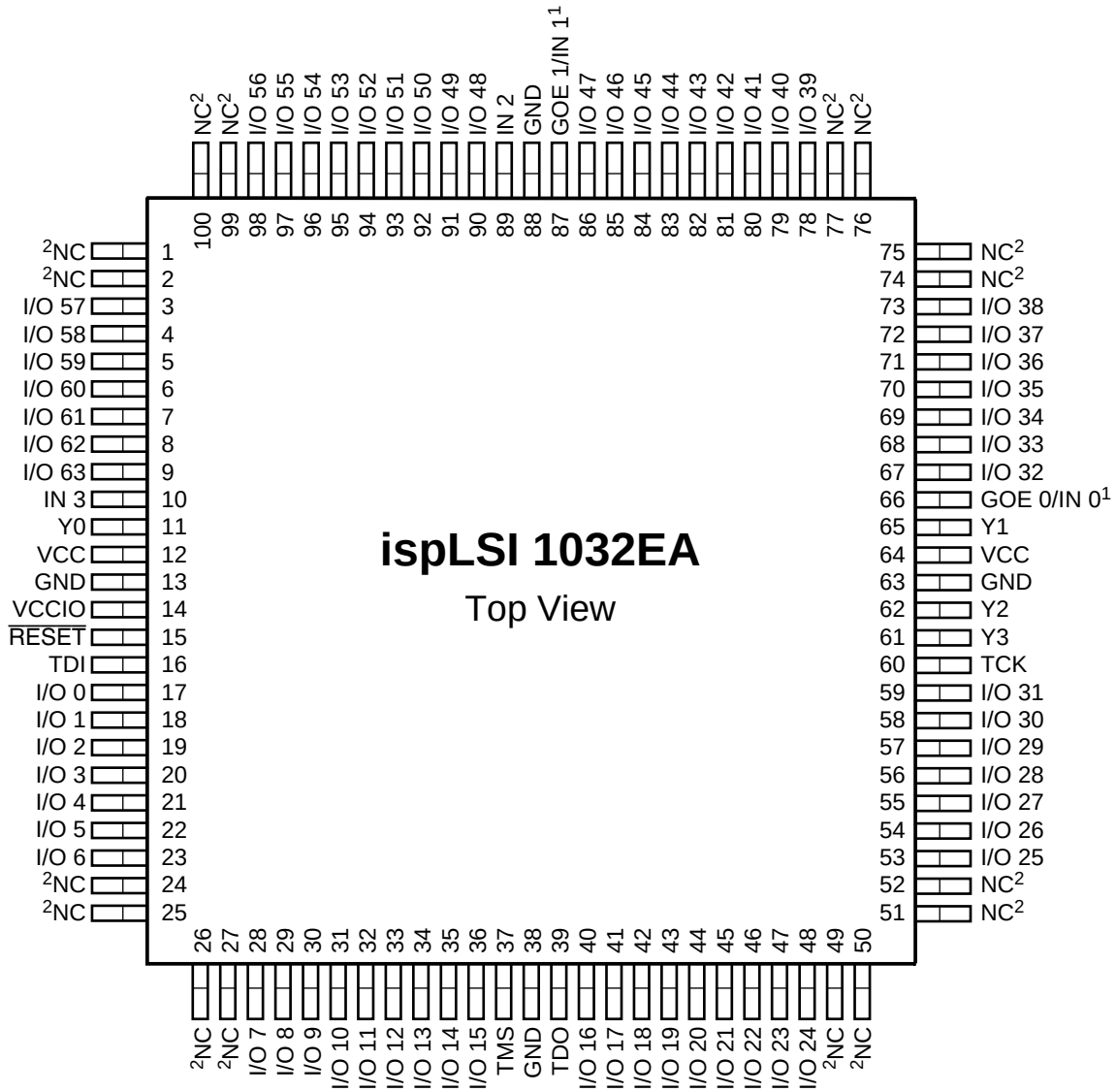
1. NC pins are not to be connected to any active signals, Vcc or GND.

Table 2-0002A/1032EA

2. Pins have dual function capability which is software selectable.

Pin Configurations

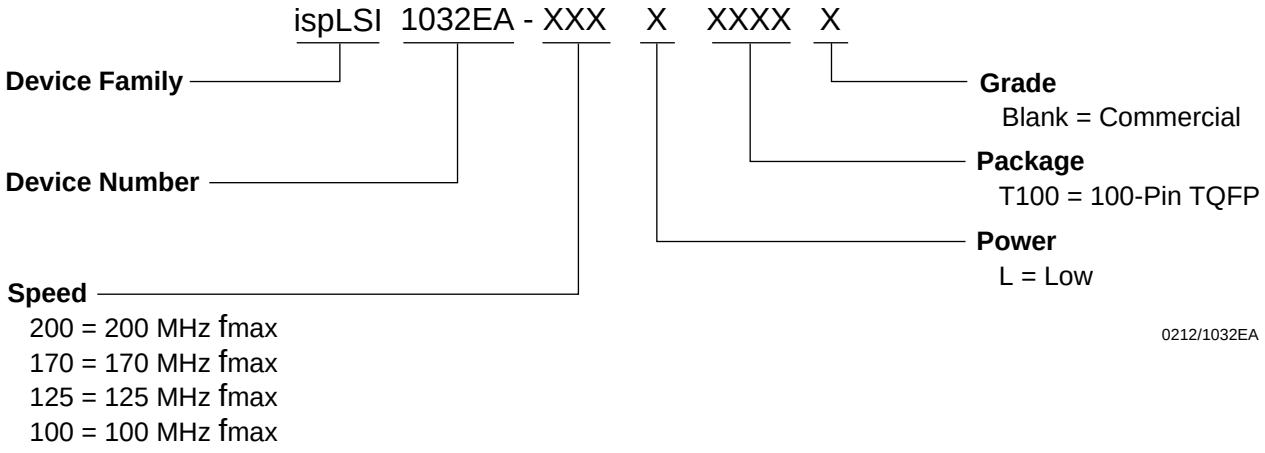
ispLSI 1032EA 100-Pin TQFP Pinout Diagram



1. Pins have dual function capability which is software selectable.
2. NC pins are not to be connected to any active signal, VCC or GND.

100-TQFP/1032EA

Part Number Description



ispLSI 1032EA Ordering Information

COMMERCIAL

FAMILY	fmax (MHz)	tpd (ns)	ORDERING NUMBER	PACKAGE
ispLSI	200	4.0	ispLSI 1032EA-200LT100	100-Pin TQFP
	170	5.0	ispLSI 1032EA-170LT100	100-Pin TQFP
	125	7.5	ispLSI 1032EA-125LT100	100-Pin TQFP
	100	10	ispLSI 1032EA-100LT100	100-Pin TQFP

Table 2-0041A/1032EA