Dolby ADM digital audio decoder NE5241

DESCRIPTION

The NE5241 is a complete stereo digital to audio converter for the Dolby ADM digital audio system, which allows CD quality stereo audio to be delivered with data rates on the order of 400 to 600kb/s. The NE5241 is intended for use in high quality consumer digital audio equipment for the reproduction of broadcast (or pre-recorded) digital audio. The IC contains channel de-multiplexing data input latches, control signal filter drivers and buffers, variable gain integrators, and variable de-emphasis filters. Precision, temperature compensated voltage reference circuitry assures accurate performance over temperature. The IC is implemented in a bipolar process to achieve low noise, low distortion, and wide dynamic range. The NE5241 is an improved version of the NE5240, which has been discontinued.

Note:
The NE5241 is available only to licensees of Dolby Laboratories Licensing Corporation, from who licensing and applications information must be obtained. Dolby is a registered trademark of Dolby Laboratories Licensing Corporation, San Francisco, California.

APPLICATIONS

- High quality digital audio transmission systems
- Pre-recorded digital audio
- Satellite delivered digital audio
- Cable TV delivered digital audio
- Microwave delivered digital audio
- Terrestrial delivered digital audio
- Digital audio for advanced television sound

PIN CONFIGURATION

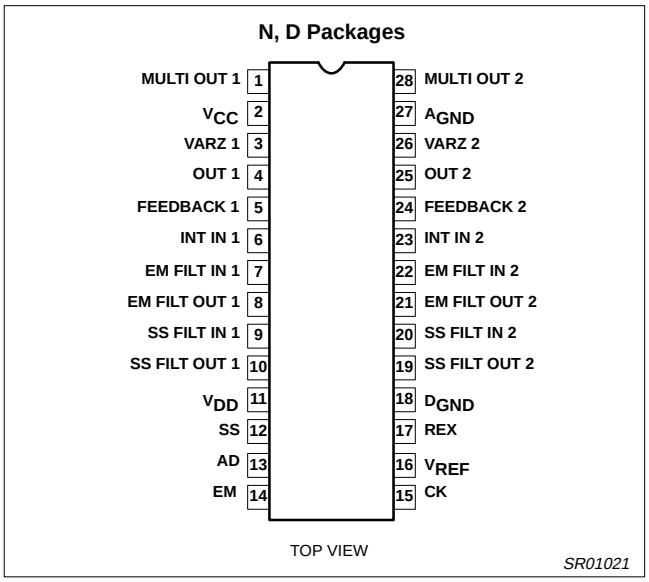


Figure 1. Pin Configuration

FEATURES

- Wide dynamic range: >95dB
- Low distortion: <0.1% @ 1kHz, 0dB
- TTL, CMOS compatible logic inputs
- Wide bandwidth: DC to > 20kHz
- Complete decoder implementation in one IChip

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
28-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE5241N	SOT117-2
28-Pin Small Outline Large (SOL) Package	0 to +70°C	NE5241D	SOT136-1

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Analog supply voltage	+15	V
V_{DD}	Logic supply voltage	+7	V
T_A	Operating ambient temperature range	0 to +70	°C
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Junction temperature	–65 to +150	°C
T_{SOLD}	Lead temperature (soldering 60 sec)	+300	°C
θ_{JA}	Thermal impedance N package D package	 48 70	 °C/W °C/W

PIN DESCRIPTIONS

PIN #	SYMBOL	DESCRIPTION
1	MULTI OUT 1	Multiplier output, channel 1
2	V_{CC}	Analog supply voltage
3	VARZ 1	Variable impedance, channel 1
4	OUT 1	Main output, channel 1
5	FEEDBACK 1	Summing amp input, channel 1
6	INT IN 1	Integrator amp input, channel 1
7	EM FILTER IN 1	Emphasis filter buffer input, channel 1
8	EM FILTER OUT 1	Emphasis filter driver output, channel 1
9	SS FILTER IN 1	Step-size filter buffer input, channel 1
10	SS FILTER OUT 1	Step-size filter driver output, channel 1
11	V_{DD}	Logic supply voltage
12	SS	Step-size data input
13	AD	Audio data input
14	EM	Emphasis data input
15	CK	Data clock input
16	V_{REF}	Reference voltage bypass
17	REX	Variable impedance reference resistor
18	D_{GND}	Digital ground
19	SS FILTER OUT 2	Step-size filter driver output, channel 2
20	SS FILTER IN 2	Step-size filter buffer input, channel 2
21	EM FILTER OUT 2	Emphasis filter driver output, channel 2
22	EM FILTER IN 2	Emphasis filter buffer input, channel 2
23	INT IN 2	Integrator amp input, channel 2
24	FEEDBACK 2	Summing amp input, channel 2
25	OUT 2	Main output, channel 2
26	VARZ 2	Variable impedance, channel 2
27	A_{GND}	Analog ground
28	MULT OUT 2	Multiplier output, channel 2

DC ELECTRICAL CHARACTERISTICS

All specifications are at T_A=25°C, V_{DD}=5V, V_{CC}=12V. Test circuit Figure 1.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Analog supply voltage		10.8	12	13.2	V
V_{DD}	Digital supply voltage		4.7	5	5.3	V
I_{CC}	Analog supply current			25	40	mA
I_{DD}	Digital supply current			12	20	mA
V_{IH}	HIGH level input voltage		2.0			V
V_{IL}	LOW level input voltage	Pins SS, AD, EM			0.8	V
I_{IH}	HIGH level input current	Pins SS, AD, EM = 2V		1	10	µA
I_{IL}	LOW level input current	Pins SS, AD, EM = 0.8V		1	5	µA
t_S	Data setup time		150			ns
t_H	Data hold time		150			ns
I_B	Control signal buffer bias current			10	30	nA
	Integrating amp gain			22		dB

AC ELECTRICAL CHARACTERISTICS

All specifications are at T_A=25°C, V_{DD}=5V, V_{CC}=12V, Audio data rate = 204kHz. 0dB is defined as 0.775V_{RMS}. Test circuit Figure 4.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Output voltage (reference level)[1]		–6	–4.5	–2.5	dBu
	Channel balance (reference level)[1]			0.2	1.2	dB
	Channel balance change[2]	20% < SS < 80%		0.2	1.0	dB
	Channel balance change[2]	10% < SS < 90%		0.4	1.5	dB
	Step-size tracking error[3]	20% < SS < 80%		0.5	3.0	dB
	Step-size tracking error[3]	10% < SS < 90%		1.0	4.0	dB
	Headroom[4]		13			
	Noise[5]	20Hz – 20kHz		–80	–78	dBu
	Noise[5]	CCIR/ARM		–89	–85	dBu
	Mute noise[6]	CCIR/ARM		–93	–88	dBu
	Dynamic range[7]			98		
THD	Total harmonic distortion[1]	0dB (ref level)		0.8	0.2	%
THD	Total harmonic distortion[8]	+13dB (max level)		0.13	0.5	%
	Variable de-emph calibration error[9]	8kHz E_M = 40%	–1	0.2	1	dB
	Freq. response error	2kHz E_M = 10%	–1.8	0.2	1.5	dB
	Freq. response error	12kHz E_M = 60%	–2.3	0.25	2.3	dB
	Freq. response error	15kHz E_M = 70%	–2.5	0.5	2.5	dB
	Dynamic offset, emphasis[10]	AC measurement		–43	–30	dB
	Dynamic offset, step-size[11]	AC measurement		–39	–24	dB
	Channel separation	1kHz		75		dB

NOTES: Test patterns referred to are produced by the Dolby Cat. No. 346 ADM Test Data Generator.

1. Dolby ADM reference level, Dolby test pattern 00. This is 10dB below the nominal 100% modulation level.
2. The channel balance may change over the operating range. This specification is the channel balance change from the intial channel balance which was measured at reference level.
3. The gain should change by 36.12dB as the step-size data is changed from 20% to 80% duty cycle, or 48.16dB as the data changes from 10% to 90%. The tracking error is the amount by which the gain change deviates from the desired value.
4. This is headroom over Dolby ADM reference level.
5. Idling data patterns, Dolby test pattern 02 with respect to test 01.
6. Muted data patterns, Dolby test pattern 04.
7. Difference between output voltage plus headroom, and CCIR/ARM weighted mute noise level.
8. Test level is 13dB over Dolby ADM reference level. Dolby test pattern 08.
9. Measured at 8.00kHz, with emphasis data at 40% duty cycle. This may be trimmed to zero by adjusting the resistor at Pin 17.
10. Dolby test pattern 48 relative to test 00. Duty cycle alternates from 10 to 70%.
11. Dolby test pattern 49 relative to test 00. Duty cycle alternates from 10 to 70%.

APPLICATIONS INFORMATION

The application diagram shows the complete Dolby ADM decoder using the NE5241. The decoder is followed by a line driving amplifier, which, depending on the application, may not be necessary. For best frequency response accuracy, the following parts should be tight tolerance: R13 to R21 should be 1%, and C13 to C20 should be 2.5%. The variable de-emphasis pole position may be trimmed by adjusting the value of R17. The variable impedance Pins 3 and 26 are very sensitive to noise pickup. Keep the lead to C15 and C18 as short as possible. Excessive stray capacitance on the multiplier output, Pins 1 and 28, will adversely affect performance. Keep the leads to R13 and R19 short. It is desirable to place a ground plane under the NE5241. This reduces the inevitable cross-talk of the digital data (with several volts of swing) into the audio (which has a noise level on the order of 40μV). A ground plane is necessary to obtain the ultimate in noise performance.

The timing diagram illustrates how the data is clocked into the NE5241. The two audio channels share the three data input lines: audio data, step-size data, and emphasis data. During the low-to-high clock transition, the data is clocked into channel 1. During the high-to-low clock transition, the data is clocked into channel 2. The data must be stable during the clock transition.

TIMING DIAGRAM

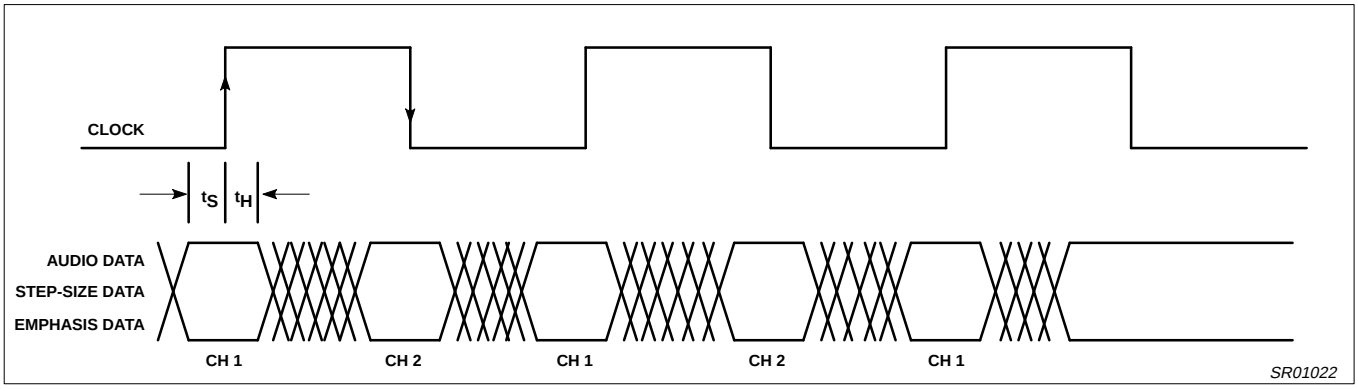


Figure 2. Timing Diagram

BLOCK DIAGRAM AND TEST CIRCUIT

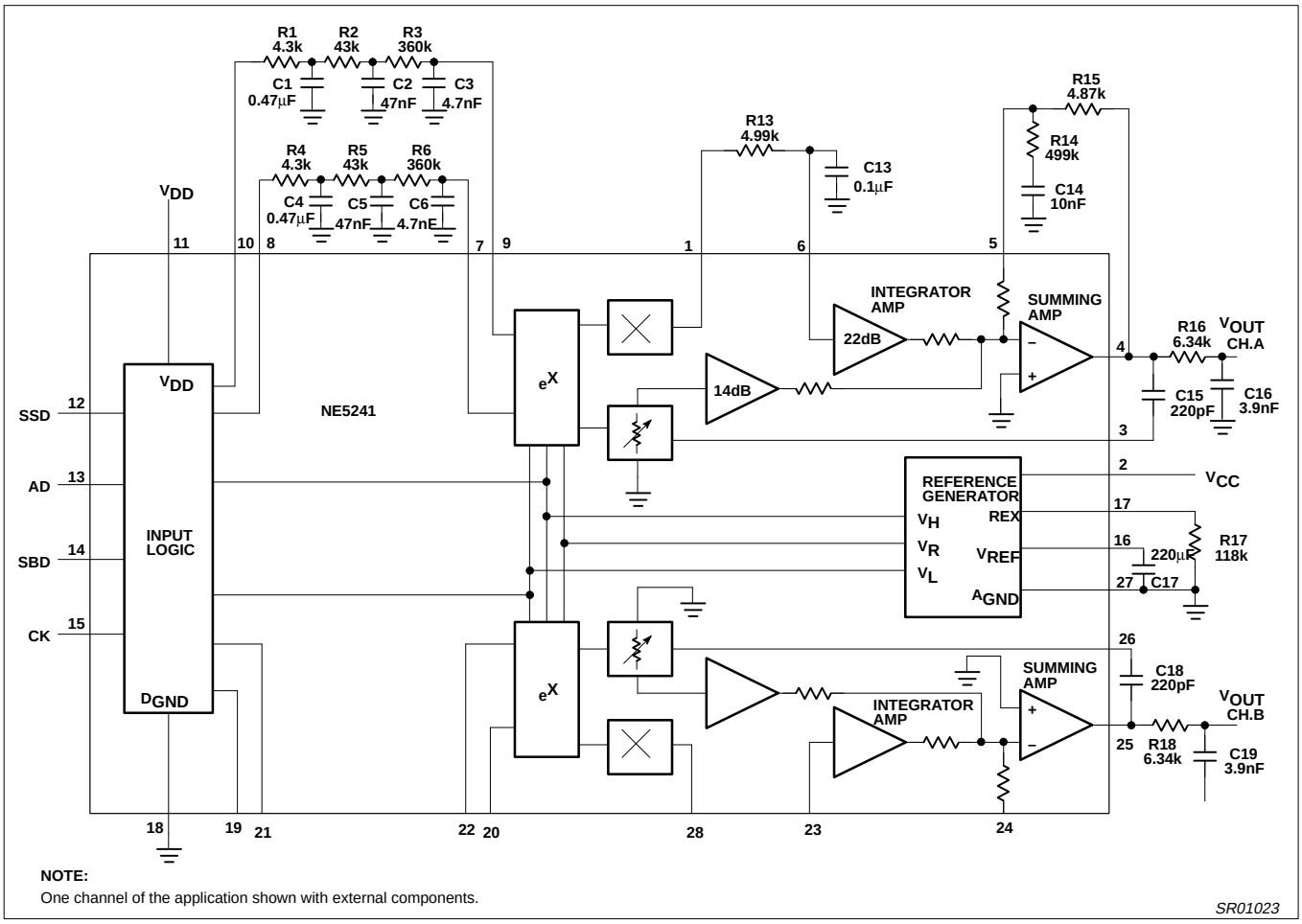


Figure 3. Block Diagram and Test Circuit

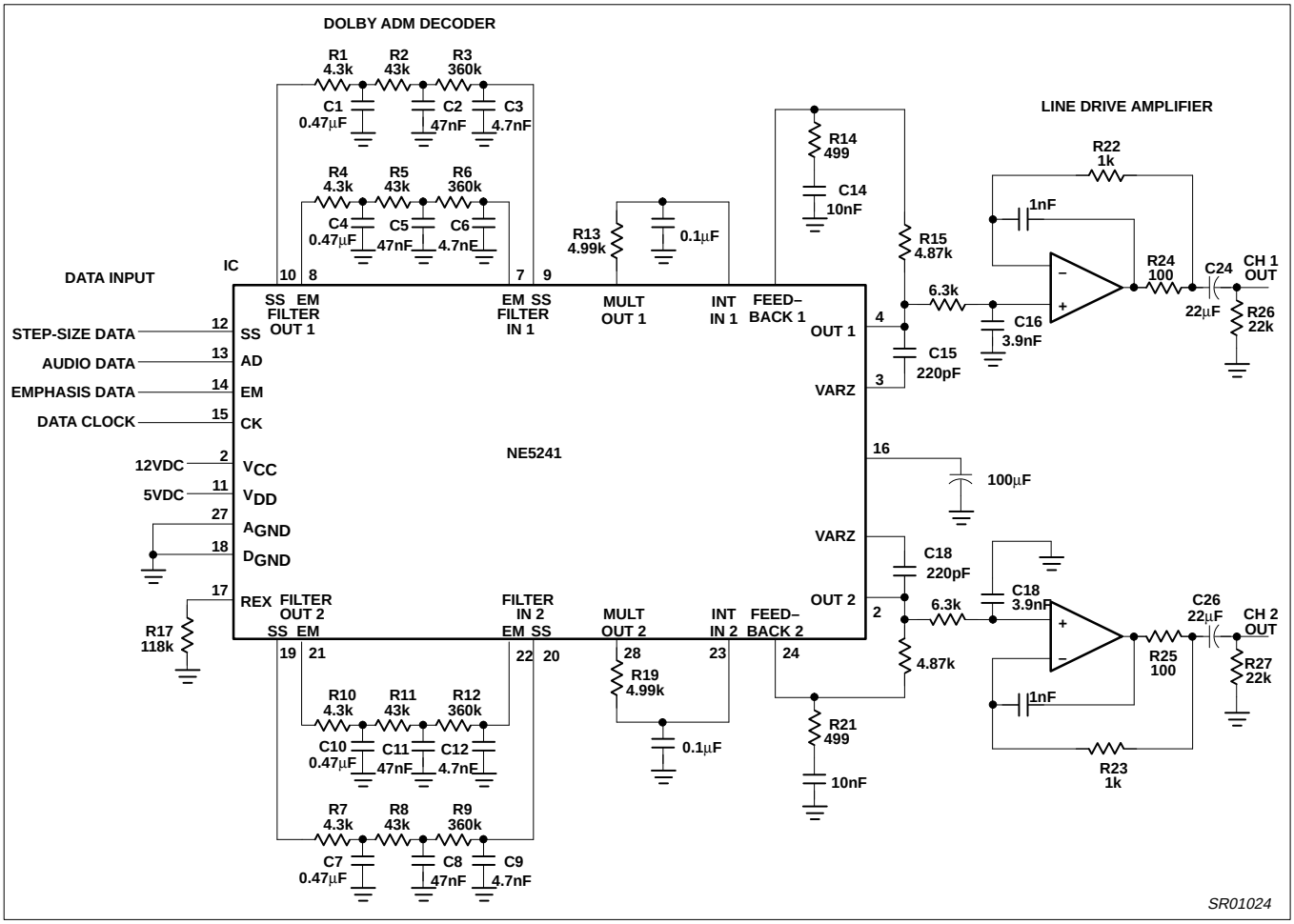


Figure 4. NE5241 Application Circuit