DUAL P-CHANNEL MATCHED MOSFET PAIR

GENERAL DESCRIPTION

The ALD1102 is a monolithic dual P-channel matched transistor pair intended for a broad range of analog applications. These enhancement-mode transistors are manufactured with Advanced Linear Devices' enhanced ACMOS silicon gate CMOS process.

The ALD1102 offers high input impedance and negative current temperature coefficient. The transistor pair is matched for minimum offset voltage and differential thermal response, and it is designed for switching and amplifying applications in +2V to +12V systems where low input bias current, low input capacitance and fast switching speed are desired. Since these are MOSFET devices, they feature very large (almost infinite) current gain in a low frequency, or near DC, operating environment. When used with an ALD1101, a dual CMOS analog switch can be constructed. In addition, the ALD1102 is intended as a building block for differential amplifier input stages, transmission gates, and multiplexer applications.

The ALD1102 is suitable for use in precision applications which require very high current gain, beta, such as current mirrors and current sources. The high input impedance and the high DC current gain of the Field Effect Transistors result in extremely low current loss through the control gate. The DC current gain is limited by the gate input leakage current, which is specified at 50pA at room temperature. For example, DC beta of the device at a drain current of 5mA at 25°C is = 5mA/50pA = 100,000,000.

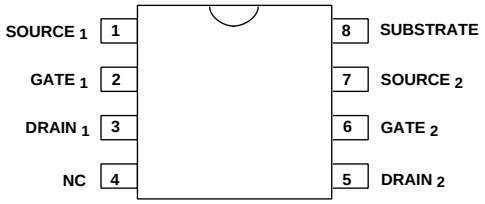
FEATURES

- Low threshold voltage of 0.7V
- Low input capacitance
- Low Vos grades -- 2mV, 5mV, 10mV
- High input impedance -- $10^{12}\Omega$ typical
- Low input and output leakage currents
- Negative current (I_{DS}) temperature coefficient
- Enhancement-mode (normally off)
- DC current gain 10^9
- RoHS compliant

APPLICATIONS

- Precision current mirrors
- Precision current sources
- Analog switches
- Choppers
- Differential amplifier input stage
- Voltage comparator
- Data converters
- Sample and Hold
- Analog inverter

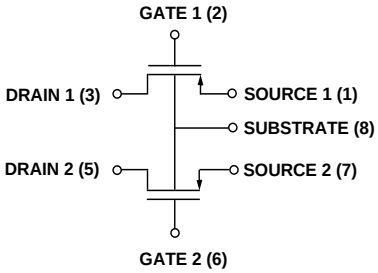
PIN CONFIGURATION



TOP VIEW
SAL, PAL, DA PACKAGES

* NC pin is internally connected. Do not connect externally.

BLOCK DIAGRAM



ORDERING INFORMATION ("L" suffix denotes lead-free (RoHS))

Operating Temperature Range		
0°C to +70°C	0°C to +70°C	-55°C to +125°C
8-Pin Small Outline Package (SOIC)	8-Pin Plastic Dip Package	8-Pin CERDIP Package
ALD1102ASAL	ALD1102APAL	
ALD1102BSAL	ALD1102BPAL	
ALD1102SAL	ALD1102PAL	ALD1102DA

* Contact factory for leaded (non-RoHS) or high temperature versions.

ABSOLUTE MAXIMUM RATINGS

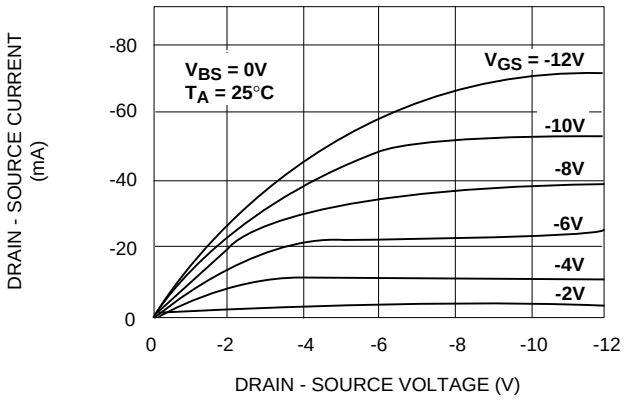
Drain-source voltage, V_{DS} ____ -10.6V
Gate-source voltage, V_{GS} ____ -10.6V
Power dissipation ____ 500mW
Operating temperature range SAL, PALpackages ____ 0°C to +70°C
DA package ____ -55°C to +125°C
Storage temperature range ____ -65°C to +150°C
Lead temperature, 10 seconds ____ +260°C
CAUTION: ESD Sensitive Device. Use static control procedures in ESD controlled environment.

OPERATING ELECTRICAL CHARACTERISTICS
T_A = 25°C unless otherwise specified

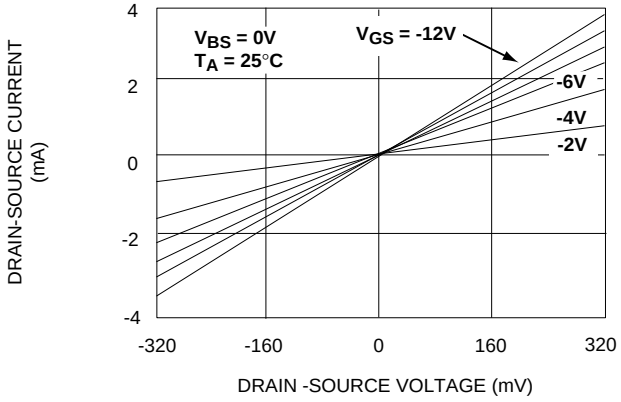
Parameter	Symbol	1102A			1102B			1102			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
Gate Threshold Voltage	V_T	-0.4	-0.7	-1.2	-0.4	-0.7	-1.2	-0.4	-0.7	-1.2	V	I_{DS} = -10µA V_{GS} = V_{DS}
Offset Voltage V_{GS1} - V_{GS2}	V_{OS}			2			5			10	mV	I_{DS} = -100µA V_{GS} = V_{DS}
Gate Threshold Temperature Drift	TC_{VT}		-1.3			-1.3			-1.3		mV/°C	
On Drain Current	$I_{DS\ (ON)}$	-8	-16		-8	-16		-8	-16		mA	V_{GS} = V_{DS} = -5V
Transconductance	G_{fs}	2	4		2	4		2	4		mmho	V_{DS} = -5V I_{DS}= -10mA
Mismatch	ΔG_{fs}		0.5			0.5			0.5		%	
Output Conductance	G_{OS}		500			500			500		µmho	V_{DS} = -5V I_{DS} = -10mA
Drain Source ON Resistance	$R_{DS(ON)}$		180	270		180	270		180	270	Ω	V_{DS} = -0.1V V_{GS} = -5V
Drain Source ON Resistance Mismatch	$\Delta R_{DS(ON)}$		0.5			0.5			0.5		%	V_{DS} = -0.1V V_{GS} = -5V
Drain Source Breakdown Voltage	BV_{DSS}	-12			-12			-12			V	I_{DS} = -10µA V_{GS} =0V
Off Drain Current	$I_{DS(OFF)}$		0.1	4 4		0.1	4 4		0.1	4 4	nA µA	V_{DS} =-12V V_{GS} = 0V T_A = 125°C
Gate Leakage Current	I_{GSS}		1	50 10		1	50 10		1	50 10	pA nA	V_{DS} =0V V_{GS} =-12V T_A = 125°C
Input Capacitance	C_{ISS}		6	10		6	10		6	10	pF	

TYPICAL PERFORMANCE CHARACTERISTICS

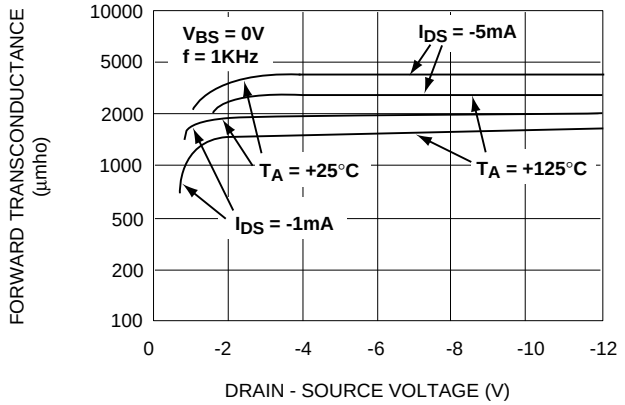
OUTPUT CHARACTERISTICS



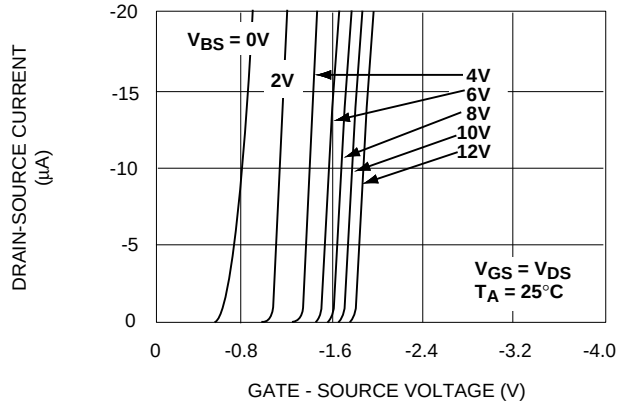
LOW VOLTAGE OUTPUT CHARACTERISTICS



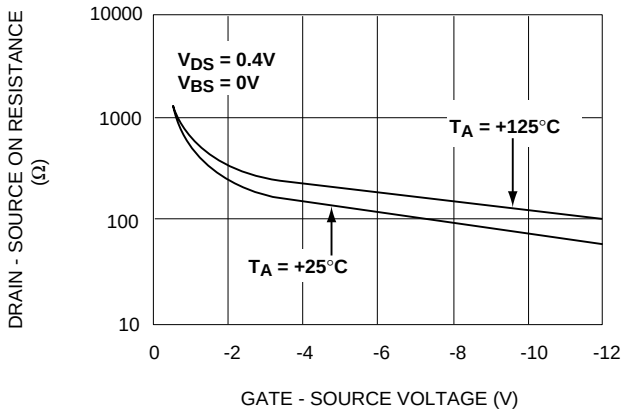
FORWARD TRANSCONDUCTANCE vs. DRAIN - SOURCE VOLTAGE



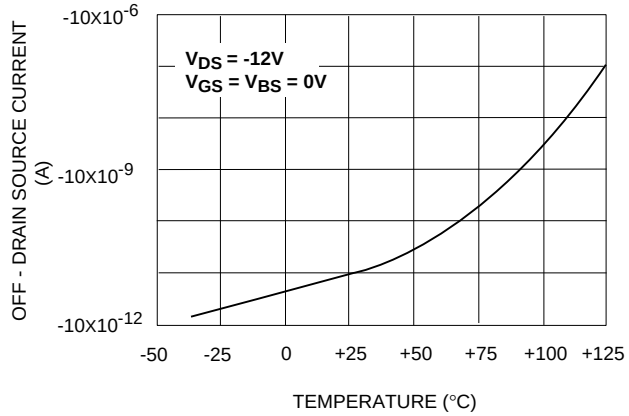
TRANSFER CHARACTERISTIC WITH SUBSTRATE BIAS



$R_{DS\ (ON)}$ vs. GATE - SOURCE VOLTAGE

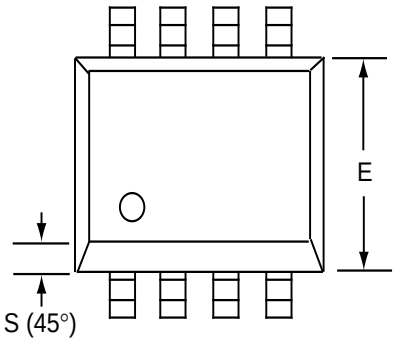


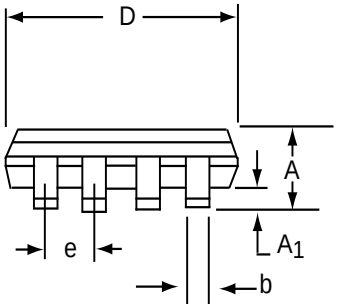
OFF DRAIN - CURRENT vs. TEMPERATURE

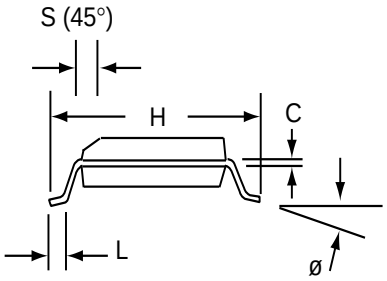


SOIC-8 PACKAGE DRAWING

8 Pin Plastic SOIC Package



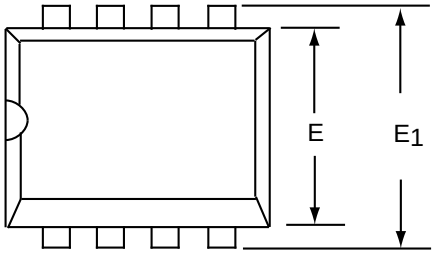


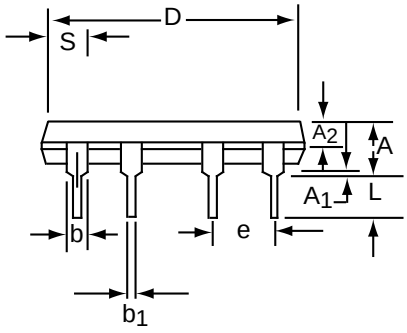


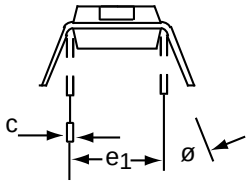
Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A_1	0.10	0.25	0.004	0.010
b	0.35	0.45	0.014	0.018
C	0.18	0.25	0.007	0.010
D-8	4.69	5.00	0.185	0.196
E	3.50	4.05	0.140	0.160
e	1.27 BSC		0.050 BSC	
H	5.70	6.30	0.224	0.248
L	0.60	0.937	0.024	0.037
Ø	0°	8°	0°	8°
S	0.25	0.50	0.010	0.020

PDIP-8 PACKAGE DRAWING

8 Pin Plastic DIP Package



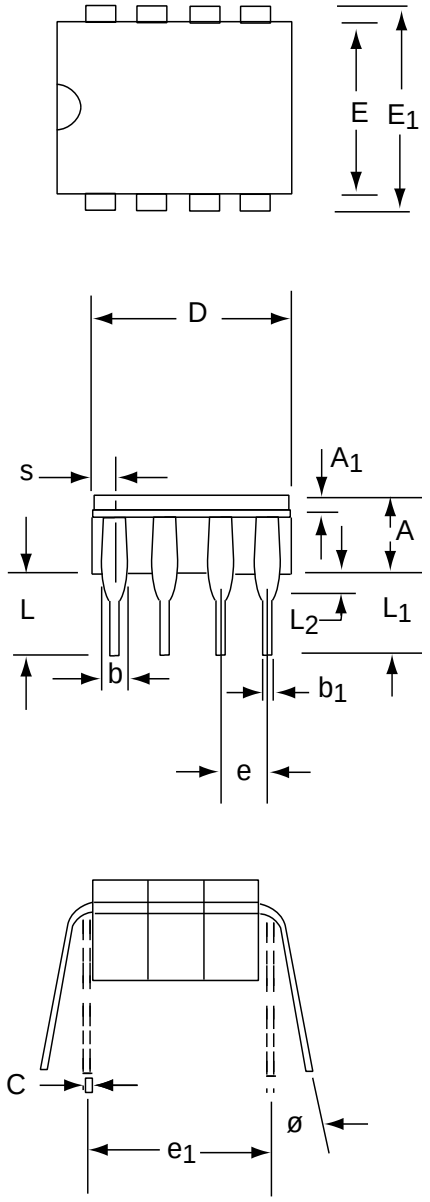




Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	3.81	5.08	0.105	0.200
A_1	0.38	1.27	0.015	0.050
A_2	1.27	2.03	0.050	0.080
b	0.89	1.65	0.035	0.065
b_1	0.38	0.51	0.015	0.020
c	0.20	0.30	0.008	0.012
D-8	9.40	11.68	0.370	0.460
E	5.59	7.11	0.220	0.280
E_1	7.62	8.26	0.300	0.325
e	2.29	2.79	0.090	0.110
e_1	7.37	7.87	0.290	0.310
L	2.79	3.81	0.110	0.150
S-8	1.02	2.03	0.040	0.080
ø	0°	15°	0°	15°

CERDIP-8 PACKAGE DRAWING

8 Pin CERDIP Package



Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	3.55	5.08	0.140	0.200
A_1	1.27	2.16	0.050	0.085
b	0.97	1.65	0.038	0.065
b_1	0.36	0.58	0.014	0.023
C	0.20	0.38	0.008	0.015
D-8	--	10.29	--	0.405
E	5.59	7.87	0.220	0.310
E_1	7.73	8.26	0.290	0.325
e	2.54 BSC		0.100 BSC	
e_1	7.62 BSC		0.300 BSC	
L	3.81	5.08	0.150	0.200
L_1	3.18	--	0.125	--
L_2	0.38	1.78	0.015	0.070
S	--	2.49	--	0.098
Ø	0°	15°	0°	15°