STRUCTURE Silicon Monolithic Integrated Circuit

TYPE Reference Voltage Regulator

PRODUCT SERIES **BD3931HFP**

FEATURES
1. High output voltage precision: 5.0V±2%(Ta=25℃)/ Low dropout voltage/ Low quiescent current: 30μA.
2. Built-in Overcurrent protection circuit/ Thermal shutdown circuit / Overvoltage protection circuit/ Reverse polarity circuit.

○ABSOLUTE MAXIMUM RATINGS (Ta=25℃)

Parameter	Symbol	Limit	Unit
Positive Supply Voltage	VccP	36 ※1	V
Negative Supply Voltage	VccN	-15	V
Power Dissipation	Pd	1.6 ※2	W
Operating Temperature Range	Topr	-40～+125	℃
Storage Temperature Range	Tstg	-55～+150	℃
Peak Supply Voltage	Vcc Peak	50 ※3	V
Maximum Junction Temperature	Tjmax	150	℃

※1 Not to exceed Pd.
※2 Reduced by 12.8mW/℃ over Ta=25℃ , when mount on a glass epoxy board:70mm×70mm×1.6mm.
※3 Applied voltage is less than 200ms (tr≧1ms)

○OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	Vcc	6.2	25.0	V
Output Current	Io	—	500	mA

NOTE) The product described in this specification is a strategic product (and/or service) subject to COCOM regulations. It should not be exported without authorization from the appropriate government.

Status of this document
The Japanese version of this document is the formal specification.
A customer may use this translation version only for a reference to help reading the formal version.
If there are any differences in translation version of this document, formal version takes priority.

○ELECTRICAL CHARACTERISTICS(Unless otherwise specified, Ta=25℃, Vcc=13.2V, Io=200mA)

Parameter	Symbol	Limits			Unit	Conditions
		MIN	Typ	MAX		
Bias Current 1	Ib1	—	30	40	μA	Io=0mA
Bias Current 2	Ib2	—	30	—	μA	Io=200mA
Output Voltage	Vo	4.900	5.000	5.100	V	
Output Current	Io	0.5	—	—	A	
Dropout Voltage	⊿Vd	—	0.78	1.1	V	Vcc=4.75V, Io=200mA
Ripple Rejection	R.R.	45	55	—	dB	f=120Hz, ein=1Vrms, Io=100mA
Line Regulation	Reg. I	—	10	30	mV	Vcc=6.2V→25V
Load Regulation	Reg. L	—	20	60	mV	Io=0mA→200mA

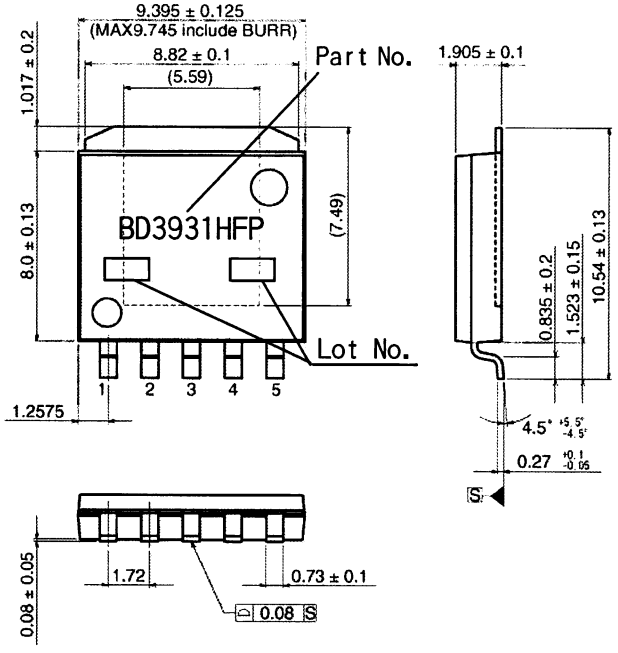
○ELECTRICAL CHARACTERISTICS(Unless otherwise specified, Ta=-40～125℃, Vcc=13.2V, Io=200mA)

Parameter	Symbol	Limits			Unit	Conditions
		MIN	Typ	MAX		
Bias Current 1	Ib1	—	30	40	μA	Io=0mA
Bias Current 2	Ib2	—	30	—	μA	Io=200mA
Output Voltage	Vo	4.800	5.000	5.100	V	
Output Current	Io	0.5	—	—	A	
Dropout Voltage	⊿Vd	—	—	1.5	V	Vcc=4.75V, Io=200mA
Ripple Rejection	R.R.	45	55	—	dB	f=120Hz, ein=1Vrms Io=100mA
Line Regulation	Reg. I	—	10	45	mV	Vcc=6.2V→25V
Load Regulation	Reg. L	—	20	60	mV	Io=0mA→200mA

This product is not designed for protection against radio active rays.

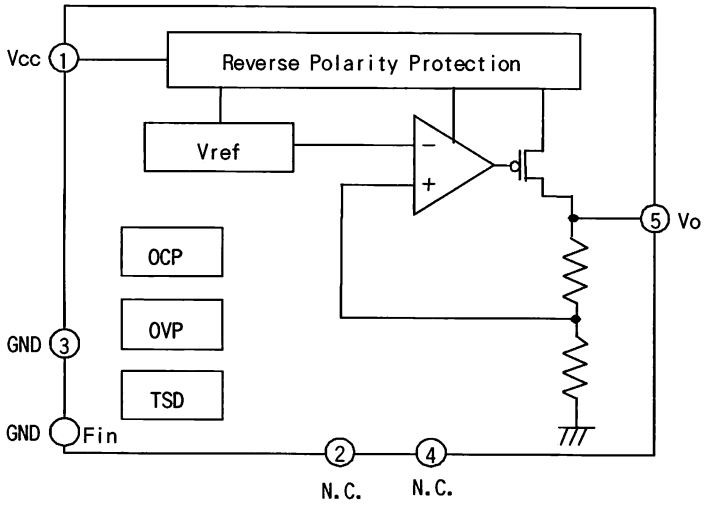
Note: All characteristics are measured with 0.33μF and 0.1μF capacitors connected to input and output pins, respectly Because measurements (pulse measurements) were taken when Ta=Tj, data other than the temperature coefficient of Output voltage does not include fluctuations due to temperature variations.

○PHYSICAL DIMENSIONS・MARKING



HRP-5 (Unit : mm)

○BLOCK DIAGRAM



※Refer to the Technical Note about the details of the application.

○PIN No. • PIN NAME

Pin No.	Pin Name
1	Vcc
2	N.C.
3	GND
4	N.C
5	Vo
Fin	GND

○OPERATING NOTES

1) Absolute maximum ratings
Use of the IC in excess of absolute maximum ratings such as the applied voltage or operating temperature range may result in IC damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered. A physical safety measure such as a fuse should be implemented when use of the IC in a special mode where the absolute maximum ratings may be exceeded is anticipated.

2) GND potential
Ensure a minimum GND pin potential in all operating conditions.

3) Thermal design
Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

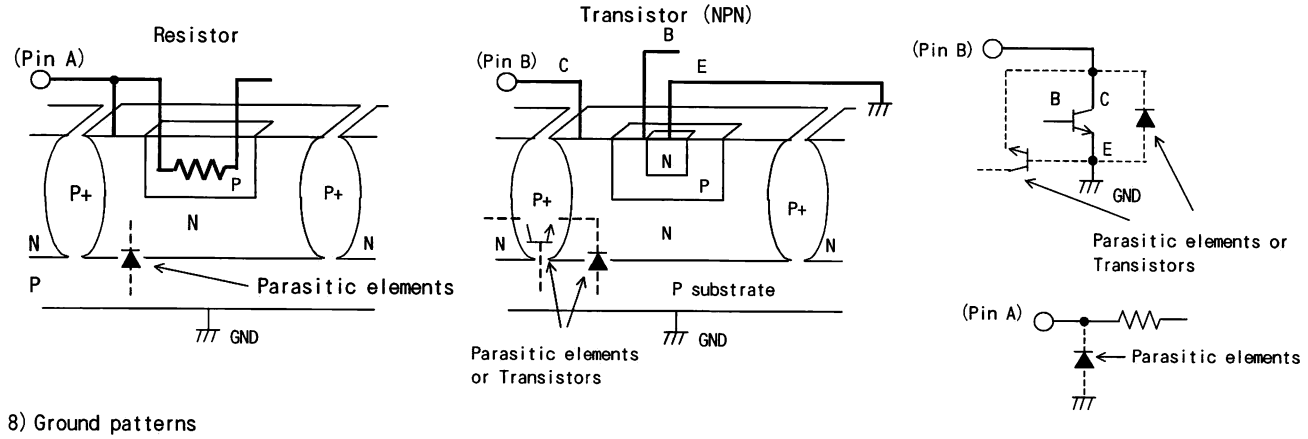
4) Pin short and mistake mounting
Use caution when orienting and positioning the IC for mounting on printed circuit boards. Improper mounting may result in damage to the IC. Shorts between output pins and the power supply and GND pins caused by the presence of a foreign object may result in damage to the IC. Ensure a minimum GND pin potential in all operating conditions.

5) Actions in strong magnetic field
Keep in mind that the IC may malfunction in strong magnetic fields.

6) Testing on application boards
When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process. Ground the IC during assembly steps as an antistatic measure, and use similar caution when transporting or storing the IC.

7) This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P/N junctions are formed at the intersection of these P layers with the N layers of other elements to create a variety of parasitic elements. For example, when the resistors and transistors are connected to the pins as shown in the following figure,
○The P/N junction functions as a parasitic diode when GND > Pin A for the resistor or GND > Pin B for the transistor(NPN).
○Similarly, when GND > Pin B for the transistor (NPN), the parasitic diode described above combines with the N layer of other adjacent elements to operate as a parasitic NPN transistor.

The formation of parasitic elements as a result of the relationships of the potentials of different pins is an inevitable result of the IC's architecture. The operation of parasitic elements can cause interference with circuit operation as well as IC malfunction and damage. For these reasons, it is necessary to use caution so that the IC is not used in a way that will trigger the operation of parasitic elements, such as by the application of voltages lower than the GND (P substrate) voltage to input pins. Keep in mind that the IC may malfunction in strong magnetic fields.



8) Ground patterns

When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the application's reference point so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring pattern of any external parts, either.

9) Thermal shutdown circuit (TSD)

This IC incorporates a built-in TSD circuit for the protection from thermal destruction. The IC should be used within the specified power dissipation range. However, in the event that the IC continues to be operated in excess of its power dissipation limits, the attendant rise in the junction temperature (Tj) will trigger the TSD circuit to turn off all output power elements. The circuit automatically resets once the junction temperature (Tj) drops. Operation of the TSD circuit presumes that the IC's absolute maximum ratings have been exceeded. Application designs should never make use of the TSD circuit.

10) Overcurrent protection circuit (OCP)

The IC incorporates a built-in overcurrent protection circuit that operates according to the output current capacity. This circuit serves to protect the IC from damage when the load is shorted. The protection circuit is designed to limit current flow by not latching in the event of a large and instantaneous current flow originating from a large capacitor or other component. This protection circuits is effective in preventing damage due to sudden and unexpected accidents. However, the IC should not be used in applications characterized by the continuous operation or transitioning of the protection circuits. At the time of thermal designing, keep in mind that the current capacity has negative characteristics to temperatures.

11) Overvoltage protection circuit (OVP)

Overvoltage protection is designed to turn off output voltages when the voltage between Vcc and GND pins exceeds approximately 30V(Typ.). Use caution when determining the supply voltage range to use.

12) Negative surge application to Vcc pin

The IC incorporates a built-in reverse connection breakdown prevention circuit that prevents IC damage even if Vcc carries a lower voltage than the GND pin. However, note that the absolute maximum rating for the negative power supply voltage is -15V.

13) Back current flow when the Vcc power supply is suddenly interrupted

These ICs limit generation of back current flow when the Vcc power supply is suddenly interrupted to protect the IC from damage. Sinking current is also limited, making the series compatible with designs where high-capacitance capacitors are used to lengthen the amount of time over which the output voltage can be maintained.

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