NEC

COMPOUND TRANSISTOR
μPA104

HIGH FREQUENCY NPN TRANSISTOR ARRAY

FEATURES

- **9 GHz CONFIGURABLE TRANSISTOR BASED OR/NOR CIRCUITRY**
- **OUTSTANDING h_{FE} LINEARITY**
- **TWO PACKAGE OPTIONS:**
  μPA104B: Studded ceramic package provides superior thermal dissipation
  μPA104G: Reduced circuit size due to 14-pin plastic SOP package for surface mounting
- **EXCELLENT FOR ANALOG ADDITIONS & FORMATION OF 2-INPUT OR/NOR GATES**

DESCRIPTION AND APPLICATIONS

The μPA104 is a user-configurable, Si bipolar transistor array for formation of high speed OR/NOR gates. Its internal transistor configuration and external connection options allow the user considerable flexibility in its application. Its high gain bandwidth product (f_T = 9 GHz) make it applicable for electro-optical, signal processing, cellular telephone systems, instrumentation, and high speed gigabit logic circuits.

ORDERING INFORMATION

PART NUMBER	PACKAGE
μPA104B-E1	14-pin ceramic package
μPA104G-E1	14-pin plastic SOP (225 mil)

ABSOLUTE MAXIMUM RATINGS (T_A = +25 °C)

SYMBOLS	PARAMETERS	UNITS	RATINGS
V_{CBO}*	Collector to Base Voltage	V	15
V_{CEO}*	Collector to Emitter Voltage	V	6
V_{EBO}*	Emitter to Base Voltage	V	2.5
I_C*	Collector Current	mA	40
P_T	Power Dissipation μPA104B μPA104G	 mW mW	 650 350
T_J	Junction Temperature μPA104B μPA104G	 °C °C	 200 125
T_{STG}	Storage Temperature μPA104B μPA104G	 °C °C	 –55 to +200 –55 to +125

***** Absolute maximum ratings for each transistor.

Caution electro-static sensitive devices

The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.
Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

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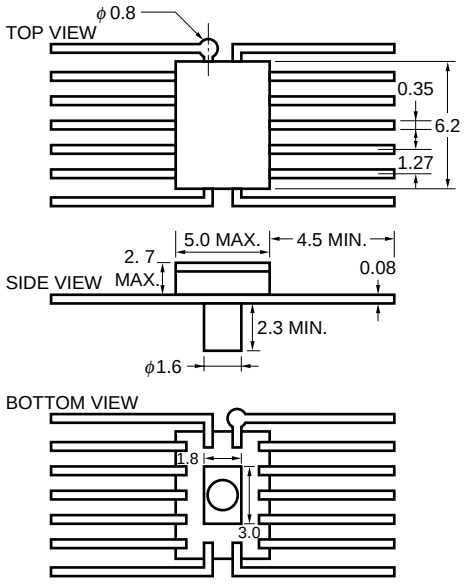
The mark ★ shows major revised points.

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PACKAGE DIMENSIONS (UNIT: mm)

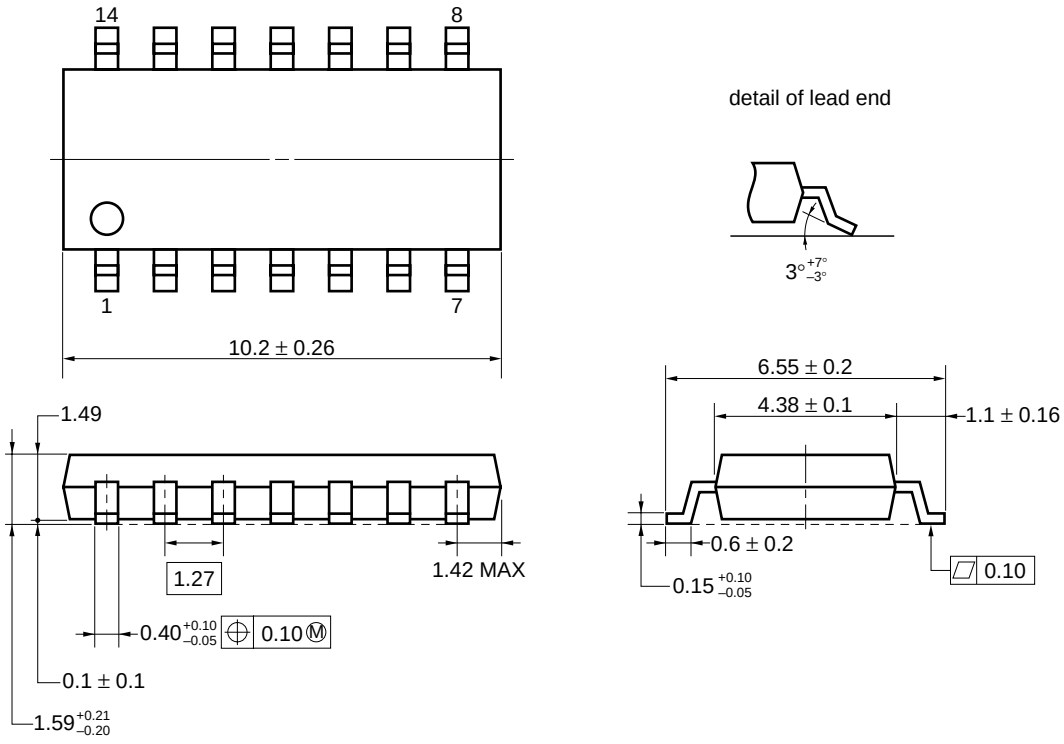
μPA104B

14 PIN CERAMIC PACKAGE



μPA104G

★ **14 PIN PLASTIC SOP (225 mil)**



NOTE Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.

See connection diagram for description of leads.

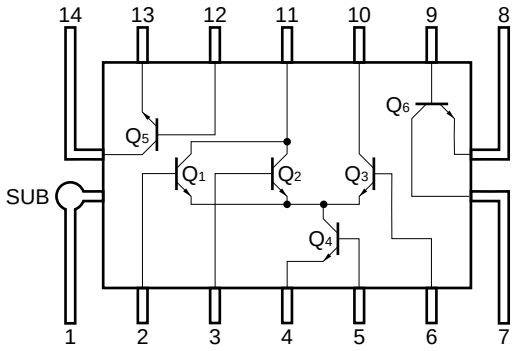
ELECTRICAL CHARACTERISTICS (Unless otherwise specified T_A = +25 °C μPA104B, μPA104G common)

SYMBOLS	PARAMETERS AND CONDITIONS	UNITS	MIN.	TYP.	MAX.
I_{CBO}	Collector Cutoff Current at V_{CB} = 5 V, I_E = 0 (Q1 thru Q6)	μA			1.0
I_{EBO}	Emitter Cutoff Current at V_{EB} = 1 V, I_C = 0 (Q4 thru Q6)	μA			1.0
h_{FE}	Direct Current Amplification at V_{CE} = 3 V, I_C = 5 mA (Q4 and Q6)		40	100	250
C_{CB}	Collector to Base Capacitance at V_{CB} = 3 V, f = 1 MHz (Q3, Q5, Q6)	pF		0.9	1.8
C_{EB}	Emitter to Base Capacitance at V_{EB} = 0, f = 1 MHz (Q4 thru Q6)	pF		1.4	2.8
C_{CS}	Collector/Substrate Capacitance, V_{CS} = 3 V, f = 1 MHz (Q3, Q5, Q6)	pF		1.4	2.8
f_T	Gain Bandwidth Product* at V_{CE} = 3 V, I_C = 10 mA	GHz		9.0	

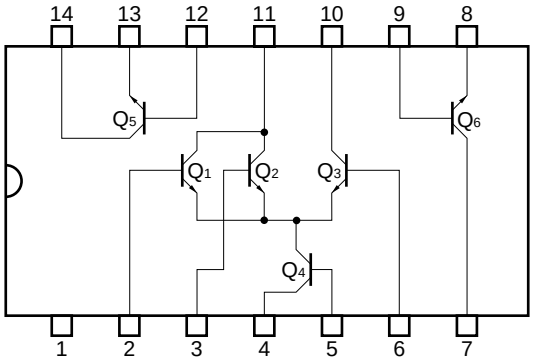
***** Measured by installing a single transistor in a Micro-X package: the value shown is a reference value.

CONNECTION DIAGRAM (Top View)

μPA104B



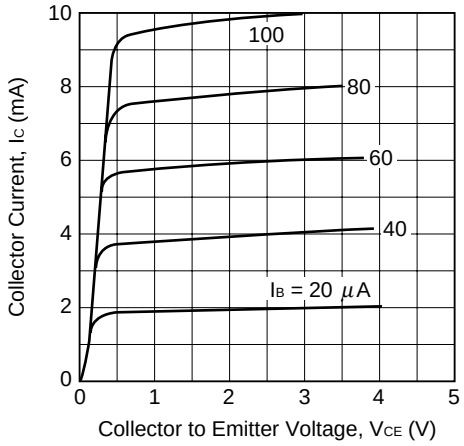
μPA104G



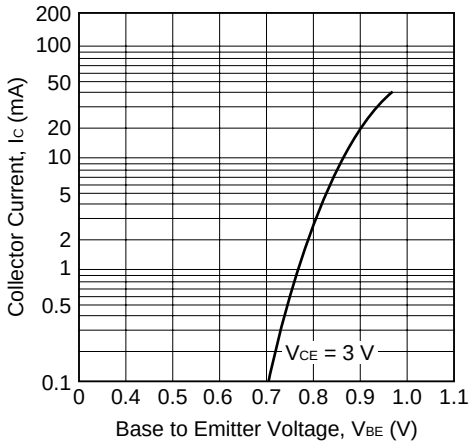
Note: Substrate should be connected to the lowest voltage point in order to prevent latch-up.

TYPICAL PERFORMANCE CHARACTERISTICS (T_A = +25 °C)

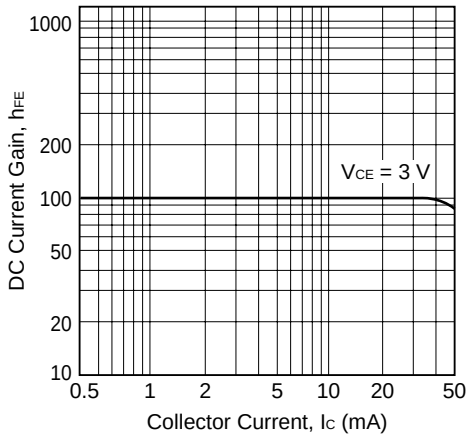
COLLECTOR CURRENT vs.
COLLECTOR TO EMITTER VOLTAGE



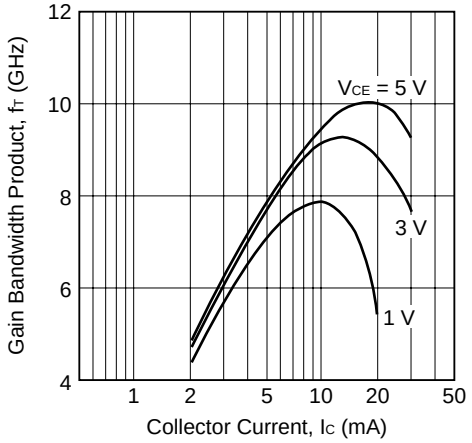
COLLECTOR CURRENT vs.
BASE TO EMITTER VOLTAGE



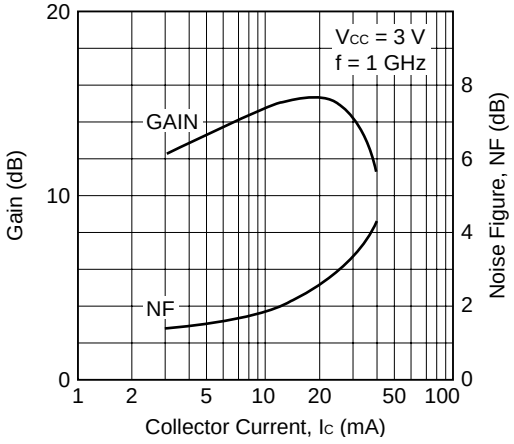
DC CURRENT GAIN vs.
COLLECTOR CURRENT



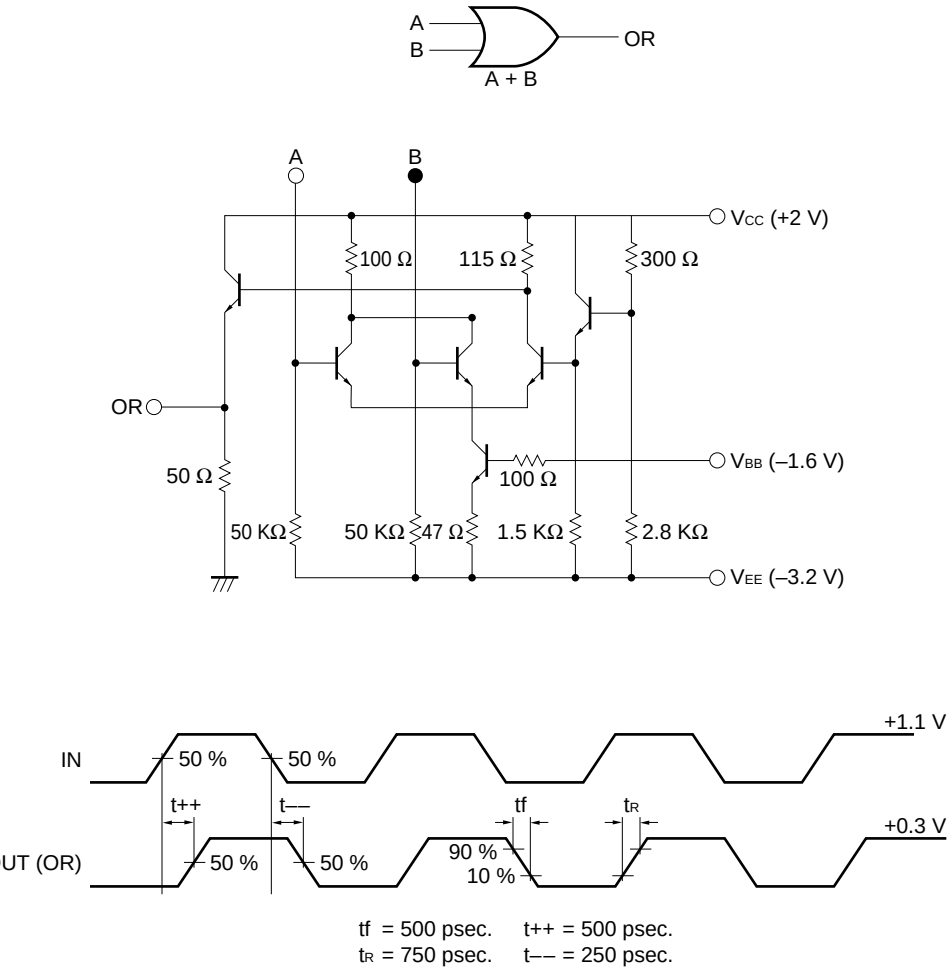
GAIN BANDWIDTH PRODUCT vs.
COLLECTOR CURRENT



GAIN AND NOISE FIGURE OF
INDIVIDUAL TRANSISTOR



TYPICAL APPLICATION



tf = 500 psec. t++ = 500 psec.
tR = 750 psec. t–– = 250 psec.

The application circuits and their parameters are for references only and are not intended for use in actual design-in's.

NOTES ON CORRECT USE

(1) Observe precautions for handling because of electro-static sensitive devices.

(2) Form a ground pattern as wide as possible to maintain the minimum ground impedance (to prevent undesired oscillation).

(3) Design circuits connected Sub pin to the lowest voltage to prevent latch-up.

(4) Design circuits as each pin voltage difference within 15 V maximum.

RECOMMENDED SOLDERING CONDITIONS

This product should be soldered in the following recommended conditions. Other soldering methods and conditions than the recommended conditions are to be consulted with our sales representatives.

μPA104G

Soldering process	Soldering conditions	Recommended condition symbol
Infrared ray reflow	Package peak temperature: 235 °C, Hour: within 30 s. (more than 210 °C), Time: 2 times, Limited days: no.[Note]	IR35-00-2
VPS	Package peak temperature: 215 °C, Hour: within 40 s. (more than 200 °C), Time: 2 times, Limited days: no.[Note]	VP15-00-2
Wave soldering	Soldering tub temperature: less than 260 °C, Hour: within 10 s. Time: 1 time, Limited days: no.[Note]	WS60-00-1
Pin part heating	Pin area temperature: less than 300 °C, Hour: within 3 s./pin Limited days: no.[Note]	

μPA104B

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak package's surface temperature: 230 °C or below, Reflow time: 10 seconds or below (210 °C or higher), Number of reflow process: 1, Exposure limit*: None	
Partial heating method	Terminal temperature: 260 °C or below, Flow time: 10 seconds or below, Exposure limit*: None	

Note It is the storage days after opening a dry pack, the storage conditions are 25 °C, less than 65 % RH.

Caution The combined use of soldering method is to be avoided (However, except the pin area heating method).

For details of recommended soldering conditions for surface mounting, refer to information document SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL (C10535E).

[MEMO]

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