CAT5270

Dual Digitally Programmable Potentiometers (DPP™) with 256 Taps & I²C Compatible Interface

Description

The CAT5270 is a volatile 256−tap by two channels, digitally programmable potentiometer (DPP™) with an I²C compatible interface. Each DPP consists of a linear taper series of resistive elements connected between two externally accessible end points. The tap points between each resistive element are connected to the wiper outputs with CMOS switches. On power up the wiper position goes to mid scale.

The CAT5270 can be used as a potentiometer or as a two terminal, variable resistor. It is available in a 14−lead TSSOP package operating over the industrial temperature range (−40°C to 85°C).

Features

- Two Linear Taper Digitally Programmable Potentiometers
- 256 Resistor Taps per Potentiometer
- End to End Resistance 50 kΩ, 100 kΩ
- I²C Compatible Interface
- Low Wiper Resistance 75 Ω (typ.)
- 2.5 V to 5.5 V Operation
- Standby Current Less than 1 μA
- Power On to Mid Scale
- 14−lead TSSOP Package
- Industrial Temperature Range

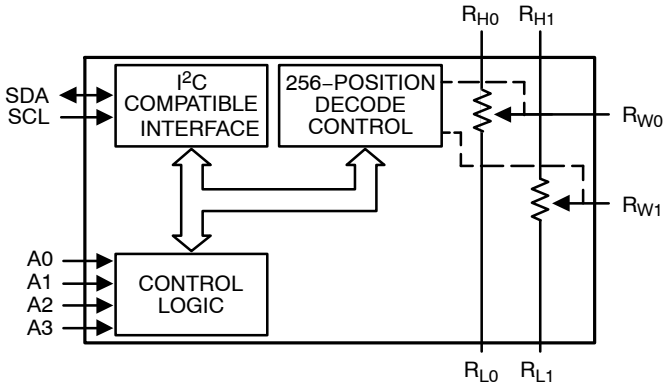
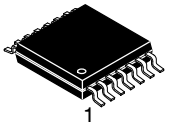


Figure 1. Functional Diagram

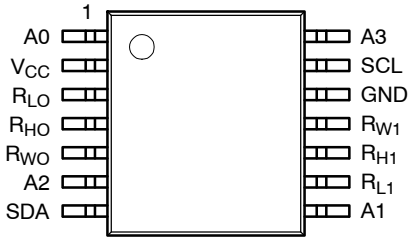
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TSSOP−14
Y SUFFIX
CASE 948AM

PIN CONNECTION



TSSOP−14 (Y)
(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

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Pin Description

SCL: Serial Clock

The CAT5270 serial clock input pin is used to clock all data transfers into or out of the device.

SDA: Serial Data

The CAT5270 bidirectional serial data pin is used to transfer data into and out of the device. The SDA pin is an open drain output and can be wire−OR'd with the other open drain or open collector I/Os.

A0, A1, A2, A3: Device Address Inputs

These inputs set the device address when addressing multiple devices. A total of sixteen devices can be addressed on a single bus. A match in the slave address must be made with the address input in order to initiate communication with the CAT5270.

R_H, R_L: Resistor End Points

The two sets of R_H and R_L pins are equivalent to the terminal connections on a mechanical potentiometer.

R_W: Wiper

The R_W pins are equivalent to the wiper terminal of a mechanical potentiometer.

Table 1. PIN DESCRIPTION

Pin # TSSOP−14	Name	Function
1	A0	Device Address, LSB
2	V_{CC}	Supply Voltage
3	R_{L0}	Low Reference Terminal for Potentiometer 0
4	R_{H0}	High Reference Terminal for Potentiometer 0
5	R_{W0}	Wiper Terminal for Potentiometer 0
6	A2	Device Address
7	SDA	Serial Data Input/Output
8	A1	Device Address
9	R_{L1}	Low Reference Terminal for Potentiometer 1
10	R_{H1}	High Reference Terminal for Potentiometer 1
11	R_{W1}	Wiper Terminal for Potentiometer 1
12	GND	Ground
13	SCL	Bus Serial Clock
14	A3	Device Address

Device Operation

The CAT5270 is two resistor arrays integrated with an I^2C compatible interface and two 8−bit wiper control registers. Each resistor array contains 255 separate resistive elements connected in series. The physical ends of each array are equivalent to the fixed terminals of a mechanical potentiometer (R_H and R_L). The tap positions between and at the ends of the series resistors are connected to the output wiper terminals (R_W) by a CMOS transistor switch. Only one tap point for each potentiometer is connected to its wiper terminal at a time and is determined by the value of the wiper control register. Data can be read or written to the wiper control register via the I^2C compatible interface. Also, the device can be instructed to operate in an "increment/decrement" mode.

Table 2. ABSOLUTE MAXIMUM RATINGS

Parameters	Ratings	Units
Temperature Under Bias	−55 to +125	°C
Storage Temperature	−65 to +150	°C
Voltage on Any Pin with Respect to V_{SS} (Note 1)	−2.0 to +V_{CC} + 2.0	V
V_{CC} with Respect to Ground	−2.0 to +6.0	V
Package Power Dissipation Capability (T_A = 25°C)	1.0	W
Lead Soldering Temperature (10 sec)	300	°C
Wiper Current	±6	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. The minimum DC input voltage is −0.5 V. During transitions, inputs may undershoot to −2.0 V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5 V, which may overshoot to V_{CC} +2.0 V for periods of less than 20 ns.

Table 3. RECOMMENDED OPERATING CONDITIONS

Parameters	Ratings	Units
V_{CC}	+2.5 to +5.5	V
Industrial Temperature	−40 to +85	°C

Table 4. POTENTIOMETER CHARACTERISTICS (V_{CC} = +2.5 V to +5.5 V, unless otherwise specified.)

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ	Max	
R_{POT}	Potentiometer Resistance (100 kΩ)			100		kΩ
R_{POT}	Potentiometer Resistance (50 kΩ)			50		kΩ
	Potentiometer Resistance Tolerance				±20	%
	R_{POT} Matching				1	%
	Power Rating	25°C, each pot			50	mW
I_W	Wiper Current				±3	mA
R_W	Wiper Resistance	I_W = ±3 mA @ V_{CC} = 3 V		200	300	Ω
R_W	Wiper Resistance	I_W = ±3 mA @ V_{CC} = 5 V		75	150	Ω
V_{TERM}	Voltage on any R_H or R_L Pin	V_{SS} = 0 V	V_{SS}		V_{CC}	V
	Resolution			0.4		%
	Absolute Linearity (Note 4)	$R_{w(n)(actual)} - R_{(n)(expected)}$ (Note 7)			±1	LSB (Note 6)
	Relative Linearity (Note 5)	$R_{w(n+1)} - R_{[w(n)+LSB]}$ (Note 7)			±0.2	LSB (Note 6)
TC_{RPOT}	Temperature Coefficient of R_{POT}	(Note 3)		±100		ppm/°C
TC_{RATIO}	Ratiometric Temp. Coefficient	(Note 3)			20	ppm/°C
$C_H/C_L/C_W$	Potentiometer Capacitances	(Note 3)		10/10/25		pF
fc	Frequency Response	R_{POT} = 50 kΩ (Note 3)		0.4		MHz

2. Latch−up protection is provided for stresses up to 100 mA on address and data pins from −1 V to V_{CC} +1 V.
3. This parameter is tested initially and after a design or process change that affects the parameter.
4. Absolute linearity is utilized to determine actual wiper voltage versus expected voltage as determined by wiper position when used as a potentiometer.
5. Relative linearity is utilized to determine the actual change in voltage between two successive tap positions when used as a potentiometer. It is a measure of the error in step size.
6. LSB = R_{TOT} / 255 or (R_H − R_L) / 255, single pot
7. n = 0, 1, 2, ..., 255

Table 5. D.C. OPERATING CHARACTERISTICS (V_{CC} = +2.5 V to +5.5 V, unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min	Max	Units
I_{CC}	Power Supply Current	f_{SCL} = 400 kHz, SDA = Open V_{CC} = 5.5 V, Inputs = GND		1	mA
I_{SB}	Standby Current (V_{CC} = 5.0 V)	V_{IN} = GND or V_{CC}, SDA = Open		5	μA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}		10	μA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}		10	μA
V_{IL}	Input Low Voltage		−1	V_{CC} x 0.3	V
V_{IH}	Input High Voltage		V_{CC} x 0.7	V_{CC} + 1.0	V
V_{OL1}	Output Low Voltage (V_{CC} = 2.5 V)	I_{OL} = 3 mA		0.4	V

Table 6. CAPACITANCE (T_A = 25°C, f = 1.0 MHz, V_{CC} = 5 V)

Symbol	Test	Conditions	Max	Units
$C_{I/O}$ (Note 8)	Input/Output Capacitance (SDA)	$V_{I/O}$ = 0 V	8	pF
C_{IN} (Note 8)	Input Capacitance (A0, A1, A2, A3, SCL, $\overline{WP}$)	V_{IN} = 0 V	6	pF

Table 7. A.C. CHARACTERISTICS

Symbol	Parameter	2.5 V – 5.5 V		Units
		Min	Max	
f_{SCL}	Clock Frequency		400	kHz
T_I (Note 8)	Noise Suppression Time Constant at SCL, SDA Inputs		200	ns
t_{AA}	SLC Low to SDA Data Out and ACK Out		1	μs
t_{BUF} (Note 8)	Time the bus must be free before a new transmission can start	1.2		μs
$t_{HD:STA}$	Start Condition Hold Time	0.6		μs
t_{LOW}	Clock Low Period	1.2		μs
t_{HIGH}	Clock High Period	0.6		μs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	0.6		μs
$t_{HD:DAT}$	Data in Hold Time	0		ns
$t_{SU:DAT}$	Data in Setup Time	50		ns
t_R (Note 8)	SDA and SCL Rise Time		0.3	μs
t_F (Note 8)	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	0.6		μs
t_{DH}	Data Out Hold Time	100		ns

Table 8. POWER UP TIMING (Notes 8 and 9)

Symbol	Parameter	Max	Units
t_{PUR}	Power−up to Read Operation	1	ms
t_{PUW}	Power−up to Write Operation	1	ms

Table 9. WIPER TIMING

Symbol	Parameter	Max	Units
t_{WRPO}	Wiper Response Time After Power Supply Stable	10	μs
t_{WRL}	Wiper Response Time After Instruction Issued	10	μs

8. This parameter is tested initially and after a design or process change that affects the parameter.
9. t_{PUR} and t_{PUW} are delays required from the time V_{CC} is stable until the specified operation can be initiated.

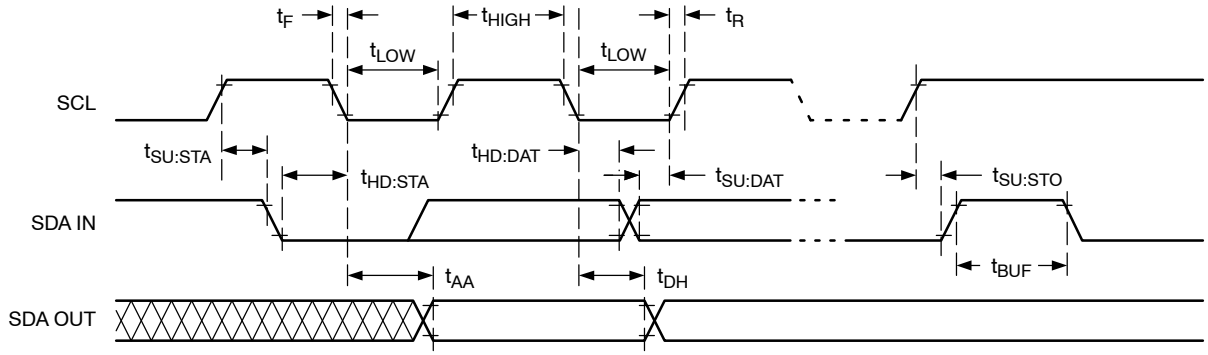


Figure 2. Bus Timing

Serial Bus Protocol

The following defines the features of the I^2C compatible interface protocol:

1. Data transfer may be initiated only when the bus is not busy.
2. During a data transfer, the data line must remain stable whenever the clock line is high. Any changes in the data line while the clock is high will be interpreted as a START or STOP condition.

The device controlling the transfer is a master, typically a processor or controller, and the device being controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the CAT5270 will be considered a slave device in all applications.

START Condition

The START Condition precedes all commands to the device, and is defined as a HIGH to LOW transition of SDA when SCL is HIGH (see Figure 3). The CAT5270 monitors the SDA and SCL lines and will not respond until this condition is met.

STOP Condition

A LOW to HIGH transition of SDA when SCL is HIGH determines the STOP condition (see Figure 3). All operations must end with a STOP condition.

Device Addressing

The bus Master begins a transmission by sending a START condition. The Master then sends the Slave Addres Byte which contains the address of the particular slave device it is requesting. The four most significant bits of the 8−bit slave address are fixed as 0101 for the CAT5270. The next four significant bits (A3, A2, A1, A0) are the device address bits and define which device the Master is accessing (see Figure 5). Up to sixteen devices may be individually addressed by the system. Typically, +5 V (V_{CC}) and ground are hard−wired to these pins to establish the device's address.

After the Master sends a START condition and the slave address byte, the CAT5270 monitors the bus and responds with an acknowledge (on the SDA line) when its address matches the transmitted slave address.

Slave Address Byte

The most significant four bits of the slave address are a device type identifier. These bits for the CAT5270 are fixed at 0101[B] (refer to Figure 5).

The next four bits, A3 – A0, are the internal slave address and must match the physical device address which is defined by the state of the A3 – A0 input pins for the CAT5270 to successfully continue the command sequence. Only the device which slave address matches the incoming device address sent by the master executes the instruction. The A3 – A0 inputs can be actively driven by CMOS input signals or tied to V_{CC} or V_{SS}.

Acknowledge

After a successful data transfer, each receiving device is required to generate an acknowledge. The Acknowledging device pulls down the SDA line during the ninth clock cycle, signaling that it received the 8 bits of data (see Figure 4).

The CAT5270 responds with an acknowledge after receiving a START condition and its slave address. If the device has been selected along with a write operation, it responds with an acknowledge after receiving each 8−bit byte.

When the CAT5270 is in a READ mode it transmits 8 bits of data, releases the SDA line, and monitors the line for an acknowledge. Once it receives this acknowledge, the CAT5270 will continue to transmit data. If no acknowledge is sent by the Master, the device terminates data transmission and waits for a STOP condition.

If the device has been selected with an IN/DEC operation it will no longer responds with acknoleadge as the received data it is not in a byte format.

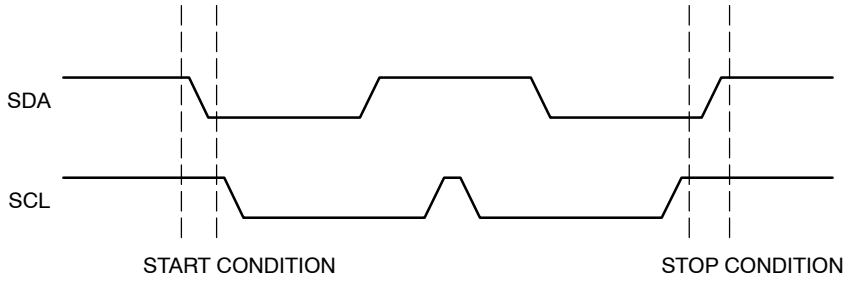


Figure 3. Start/Stop Condition

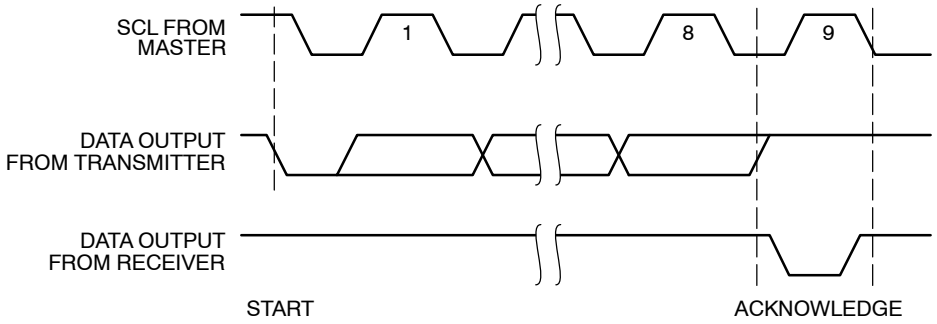


Figure 4. Acknowledge Condition

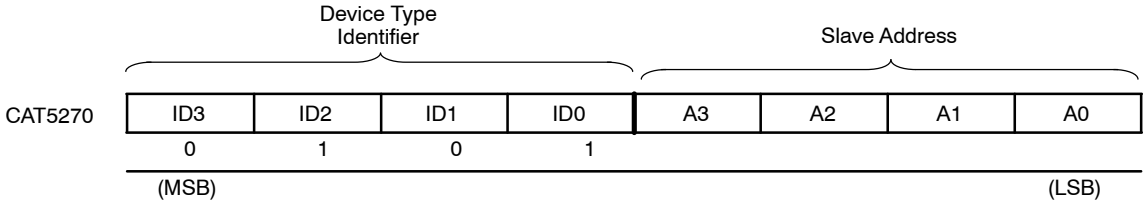


Figure 5. Identification Format for Slave Address Byte

Instruction and Register Description

Instruction Byte

The next byte sent to the CAT5270 contains the instruction and register pointer information. The four most significant bits used provide the instruction opcode I3 – I0.

Instructions

Instructions are three bytes in length. These instructions are:

- **Read Wiper Control Register** – read the current wiper position of the selected potentiometer in the WCR
- **Write Wiper Control Register** – change current wiper position in the WCR of the selected potentiometer
- **Increment/Decrement Wiper Control Register** – change step by step the current wiper position in the WCR of the selected potentiometer

The basic sequence of the three byte instructions is illustrated in Figure 8.

Write Operation

In the Write mode, the Master device sends the START condition and the slave address information to the Slave device. After the Slave generates an acknowledge, the Master sends the instruction byte that defines the requested operation of CAT5270. The instruction byte consists of a seven−bit opcode followed by pot/register selection bit. After receiving another acknowledge from the Slave, the Master device transmits the data to be written into the selected register. The CAT5270 acknowledges once more and the Master generates the STOP condition.

Increment/Decrement Command

The last command is Increment/Decrement (Figures 9 and 10). The Increment/Decrement command is different from the other commands. Once the instruction is issued and the CAT5270 has responded with an acknowledge, the master can clock the selected wiper up and/or down in one segment steps; thereby providing a fine tuning capability to the host. For each SCL clock pulse (t_{HIGH}) while SDA is HIGH, the selected wiper will move one resistor segment towards the R_H terminal. Similarly, for each SCL clock pulse while SDA is LOW, the selected wiper will move one resistor segment towards the R_L terminal.

See Instructions format for more details.

Wiper Control Register (WCR)

The CAT5270 contains two 8−bit Wiper Control Registers, one for each potentiometer. The Wiper Control Register output is decoded to select one of 256 switches along its resistor array. The contents of the WCR can be altered in two ways: it may be written by the host via Write Wiper Control Register instruction; or it can be modified one step at a time by the Increment/decrement instruction (see Instruction section for more details).

P	WCR
0	Set R0 wiper position
1	Set R1 wiper position

The Wiper Control Register is a volatile register that loses its contents when the CAT5270 is powered−down. Upon power−up, the wiper is set to midspan and may be repositioned anytime after the power has become stable.

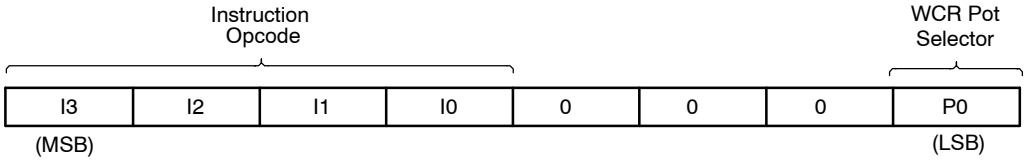


Figure 6. Instruction Byte Format

Table 10. INSTRUCTION SET

Instruction	Instruction Set (Note 10)								Operation
	I3	I2	I1	I0	F2	F1	F0	WCR/P	
Read Wiper Control Register	1	0	0	1	0	0	0	1/0	Read the contents of the Wiper Control Register pointed to by P
Write Wiper Control Register	1	0	1	0	0	0	0	1/0	Write new value to the Wiper Control Register pointed to by P
Increment/Decrement Wiper Control Register	0	0	1	0	0	0	0	1/0	Enable Increment/decrement of the Control Latch pointed to by P

10. 1/0 = data is one or zero

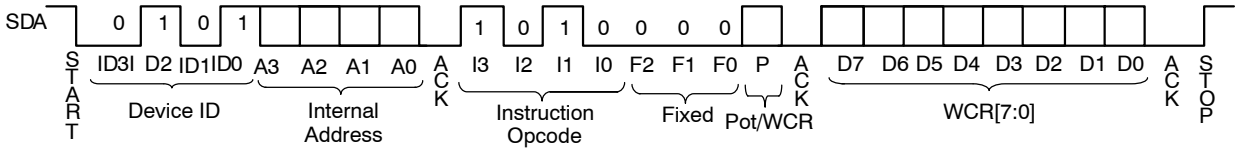


Figure 7. Write Instruction Sequence

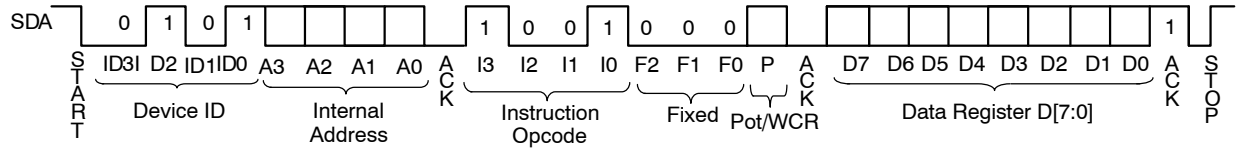


Figure 8. Read Instruction Sequence

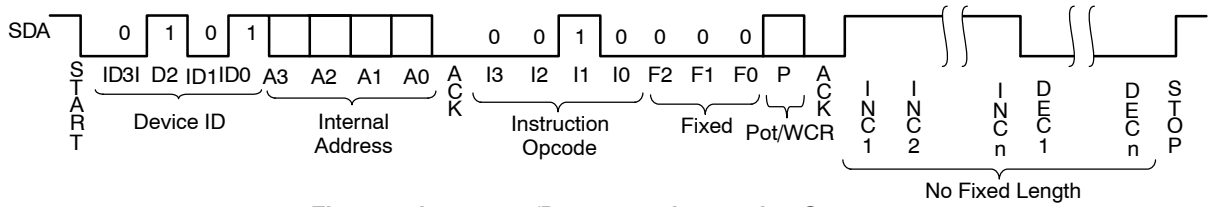


Figure 9. Increment/Decrement Instruction Sequence

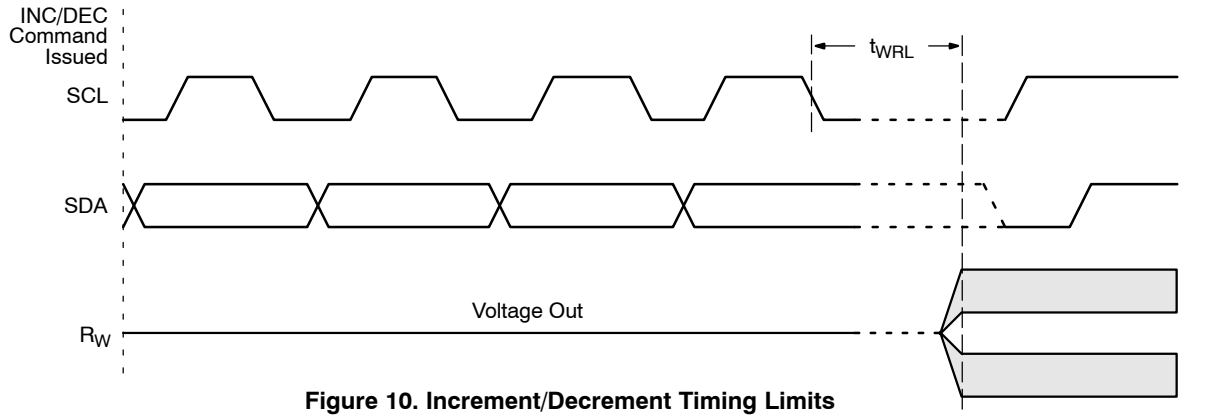


Figure 10. Increment/Decrement Timing Limits

Instruction Format

Read Wiper Control Register (WCR)

S T A R T	DEVICE ADDRESSES								A C K	INSTRUCTION								A C K	DATA								A C K	S T O P
	0	1	0	1	A3	A2	A1	A0		1	0	0	1	0	0	0	P		7	6	5	4	3	2	1	0		

Write Wiper Control Register (WCR)

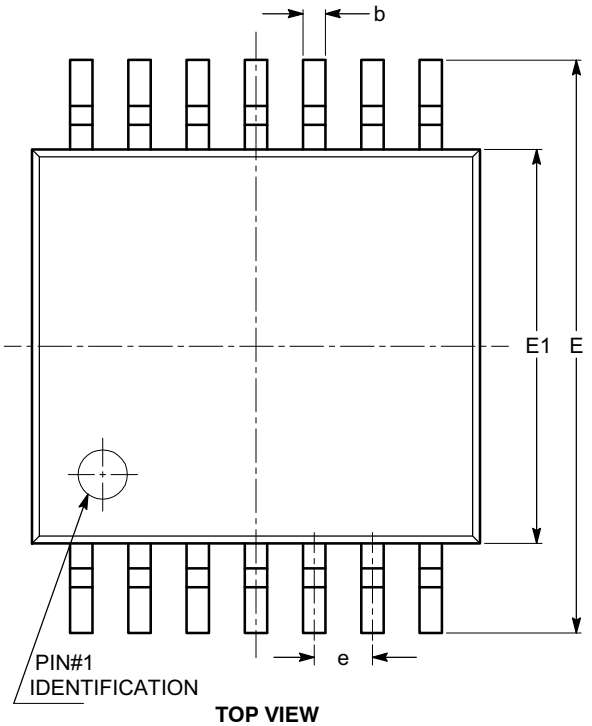
S T A R T	DEVICE ADDRESSES								A C K	INSTRUCTION								A C K	DATA								A C K	S T O P
	0	1	0	1	A3	A2	A1	A0		1	0	1	0	0	0	0	P		7	6	5	4	3	2	1	0		

Increment (I)/Decrement (D) Wiper Control Register (WCR)

S T A R T	DEVICE ADDRESSES								A C K	INSTRUCTION								A C K	DATA					S T O P
	0	1	0	1	A3	A2	A1	A0		0	0	1	0	0	0	0	P		I / D	I / D	. . .	I / D	I / D	

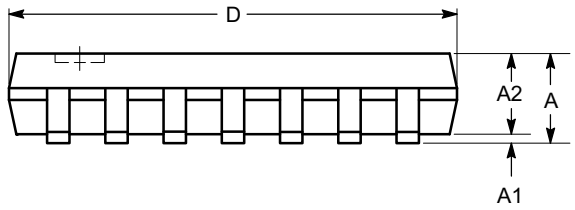
PACKAGE DIMENSIONS

TSSOP14, 4.4x5
CASE 948AM−01
ISSUE O

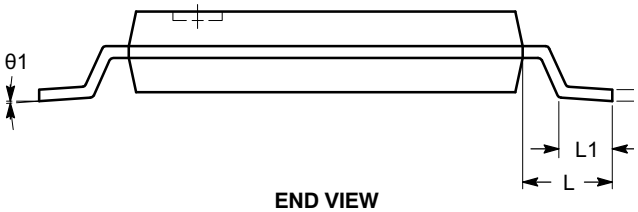


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.10
A1	0.05		0.15
A2	0.85		0.95
b	0.19		0.30
c	0.13		0.20
D	4.90		5.10
E	6.30		6.50
E1	4.30		4.50
e	0.65 BSC		
L	1.00 REF		
L1	0.45		0.75
θ	0º		8º



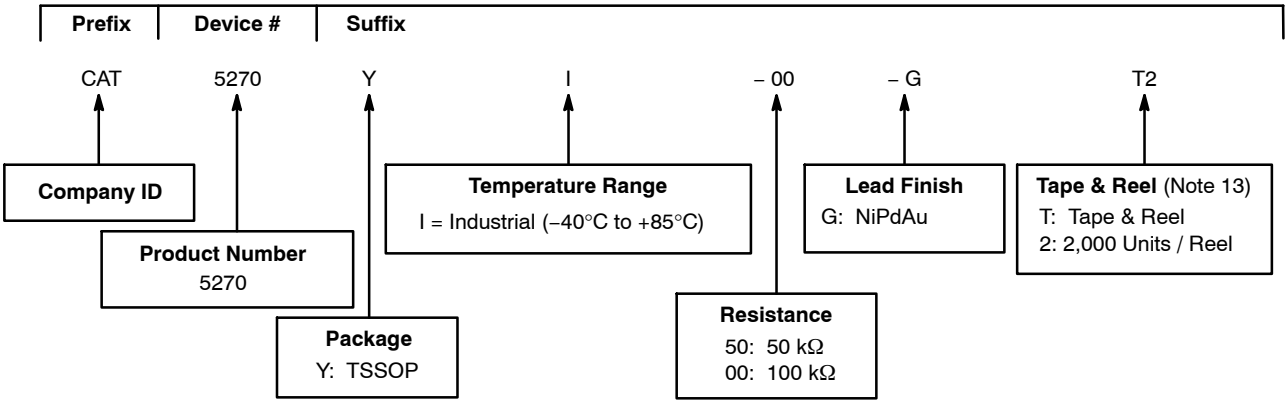
SIDE VIEW



END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-153.

Example of Ordering Information (Notes 11 and 12)



ORDERING INFORMATION

Part Number	Resistance	Package	Lead Finish
CAT5270YI–50–GT2	50 kΩ	TSSOP–14	NiPdAu
CAT5270YI–00–GT2	100 kΩ		

11. All packages are RoHS–compliant (Lead–free, Halogen–free).
12. The device used in the following example: CAT5270YI–00–GT2 is a TSSOP, Industrial Temperature, 100 kΩ, NiPdAu (TSSOP–14), Tape & Reel, 2,000/Reel.
13. For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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