MP8060

16V, 3.5A Quad Channel Power Half-Bridge

The Future of Analog IC Technology

DESCRIPTION

The MP8060 is a configurable dual channel full-bridge or quad channel half-bridge used as the output stage of a Class-D audio amplifier. Each full-bridge can be driven independently as stereo single ended audio amplifiers or driven complementary in a bridge tied load (BTL) audio amplifier configuration.

The MP8060 features a low current shutdown mode, standby mode, input under voltage protection, thermal shutdown and fault flag signal output. All channels of drivers interface with standard logic signals.

The MP8060 is available in a 32 lead QFN 5X5 package.

FEATURES

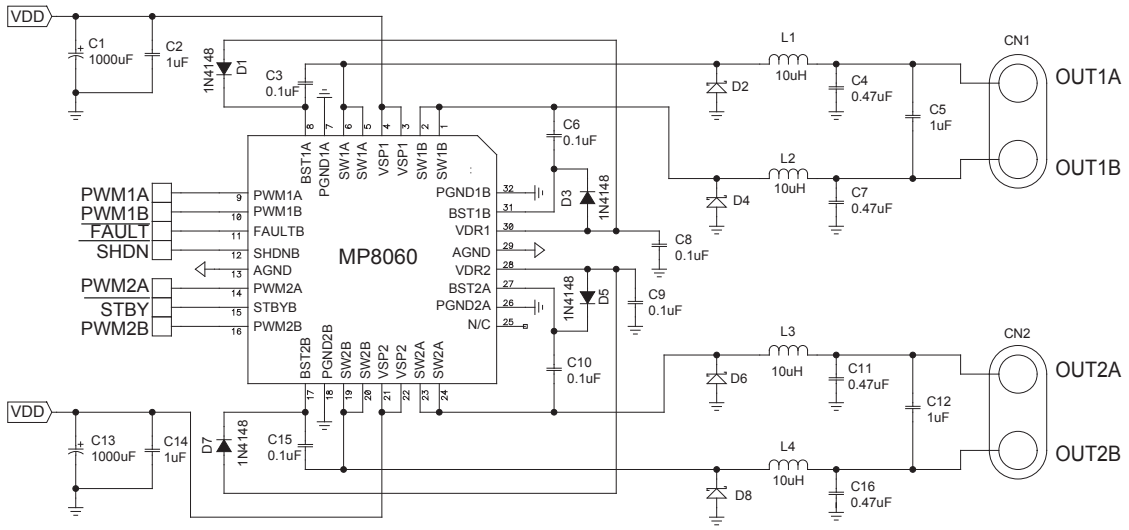
- 3.5A Peak Current Output
- Up to 600KHz Switching Frequency
- Integrated Power 0.4Ω Switches
- 30ns Switch Dead Time
- All Switches have Over-Current Protection
- Internal Under Voltage Protection
- Internal Thermal Protection
- 2.6mA Operating Current
- Fault Output Flag
- Single Ended: 4W/Channel at 16V, 8Ω Load
- Bridge Tied Load Output Power: 16W/Channel at 16V, 8Ω Load

APPLICATIONS

- Class D Audio Drivers
- Motor Drivers

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TYPICAL APPLICATION



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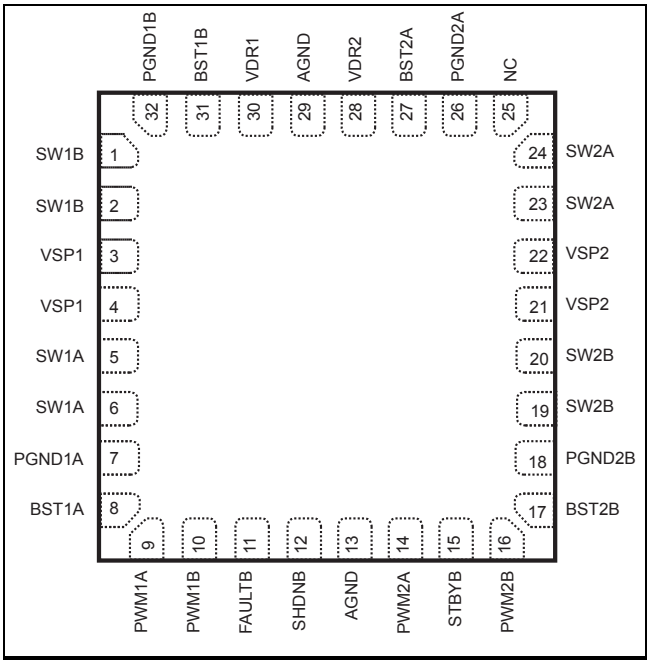
ORDERING INFORMATION

Part Number*	Package	Top Marking	Free Air Temperature (T_A)
MP8060EU	QFN 5x5 – 32L	MP8060EU	-20°C to +85°C

*For Tape & Reel, add suffix –Z (e.g. MP8060EU–Z);

For RoHS compliant packaging, add suffix –LF (e.g. MP8060EU–LF–Z).

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

VSP Supply Voltage 18.5V
SW1/2 Pin Voltage..... -0.3V to V_{SP} + 0.3V
SW1/2 to BST1/2 .....-0.3V to +6V
Voltage at All Other Pins.....-0.3V to +6V
Continuous Power Dissipation (T_A = +25°C)(2)
..... 3.5W
Storage Temperature..... -55°C to +150°C
Junction Temperature.....150°C
Lead Temperature .....260°C

Recommended Operating Conditions (3)

VSP Supply Voltage .....4.5V to 16V
Peak Output Current.....3.5A Maximum
Operating Junct. Temp (T_J)..... -20°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN32 (5x5) .....36 ..... 8 .... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{SP} = 12V, V_{SHDNB} = 5V, T_A = +25°C, unless otherwise specified.

Parameters	Symbol	Condition	Min	Typ	Max	Units
VSP Operating Current		I_{LOAD} = 0A， PWM1,2=0		2.6	5	mA
VSP Shutdown Current		V_{SHDNB} = 0V		2.5	10	μA
Operating VSP Threshold Low				3.8		V
Operating VSP Threshold High				4.0		V
STBYB Threshold Low			0.8	1.1		V
STBYB Threshold High				1.9	2.2	V
PWM Input Bias Current				0.1	1.0	μA
SHDNB Threshold Low			0.8	1.1		V
SHDNB Threshold High				1.9	2.2	V
PWM1,2 Threshold Low			0.9	1.4		V
PWM1,2 Threshold High				1.8	2.2	V
SW1/2 On Resistance		V_{SP} = 7.5V, High-Side and Low-Side		0.4		Ω
SW1/2 Current Limit (5)		V_{PWM} = 0V, Sinking		3.5		A
		V_{PWM} = 5V, Sourcing		3.5		A
SW1/2 Switching Frequency		V_{PWM} = 0 to 5V, 50% Duty Cycle			0.6	MHz
SW1/2 Maximum Duty Cycle (6)		V_{SP} = 7.5V, V_{PWM} = 5V, C_{BST} = 100nF, f_{SW} = 3.3kHz		99.5		%
SW1/2 Rise/Fall Time		V_{PWM} = 0V to 5V		10		ns
PWM Pulse Width		V_{PWM} = 0V to 5V, High or Low Pulse		40		ns
Dead Time (5)		I_{OUT}= ±100mA		30		ns
PWM1,2 to SW1,2 Delay Time Rising		V_{PWM} = 0V to 5V		35		ns
PWM1,2 to SW1,2 Delay Time Falling		V_{PWM} = 5V to 0V		35		ns
Thermal Shutdown Temperature (5)		T_J Rising, Hysteresis = 20°C		150		°C

Notes:

5) Not production tested.

6) OUT drives low for 1.5μs every 300μs to charge the BST to SW capacitor.

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PIN FUNCTIONS

Pin #	Name	Description
1,2	SW1B	Switched Output 1B. Connect the output LC filter to SW1B. SW1B is valid approximately 100µs after VSP goes high.
3, 4	VSP1	Power Supply Input. Connect VSP1 to the positive side of the input power supply. Bypass VSP1 to PGND as close to the IC as possible.
5,6	SW1A	Switched Output 1A. Connect the output LC filter to SW1A. SW1A is valid approximately 100µs after VSP goes high.
7	PGND1A	Power Ground of Channel 1A. Connect the exposed pad on bottom side to the ground plane.
8	BST1A	Bootstrap Supply. BST1A powers the high-side gate of the SW1A stage. Connect a 0.1µF or greater capacitor between BST1A and SW1A.
9	PWM1A	Driver Logic Input 1A. Drive PWM1A with the signal that controls the MP8060 SW1A. Drive PWM1A high to turn on the high side switch; drive PWM1A low to turn on the low-side switch.
10	PWM1B	Driver Logic Input 1B. Drive PWM1B with the signal that controls the MP8060 SW1B. Drive PWM1B high to turn on the high side switch; drive PWM1B low to turn on the low-side switch.
11	FAULTB	Fault Output. A low output at FAULTB indicates that the MP8060 has detected an over temperature or over current condition. This output is open drain.
12	SHDNB	Shutdown Input. When low, the IC will be shut off.
13,29	AGND	Analog Ground.
14	PWM2A	Driver Logic Input 2A. Drive PWM2A with the signal that controls the MP8060 SW2A. Drive PWM2A high to turn on the high side switch; drive PWM2A low to turn on the low-side switch
15	STBYB	Standby Input. Default low (internal pull-down). If driven high, the output of the drivers is determined by the PWM1A/1B/2A/2B. If driven low, the output of both drivers is high impedance.
16	PWM2B	Driver Logic Input 2B. Drive PWM2B with the signal that controls the MP8060 SW2B. Drive PWM2B high to turn on the high side switch; drive PWM2B low to turn on the low-side switch
17	BST2B	Bootstrap Supply. BST2B powers the high-side gate of the SW2B stage. Connect a 0.1µF or greater capacitor between BST2B and SW2B.
18	PGND2B	Power Ground of Channel 2B. Connect the exposed pad on the bottom side to the ground plane.
19,20	SW2B	Switched Output 2B. Connect the output LC filter to SW2B. SW2B is valid approximately 100µs after VSP goes high.
21, 22	VSP2	Power Supply Input. Connect VSP2 to the positive side of the input power supply. Bypass VSP2 to PGND as close to the IC as possible.
23, 24	SW2A	Switched Output 2A. Connect the output LC filter to SW1A. SW1A is valid approximately 100µs after VSP goes high.
25	NC	No connect.
26	PGND2A	Power Ground of Channel 2A. Connect the exposed pad on the bottom side to the ground plane.
27	BST2A	Bootstrap Supply. BST2A powers the high-side gate of the SW2A stage. Connect a 0.1µF or greater capacitor between BST2A and SW2A.

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PIN FUNCTIONS *(continued)*

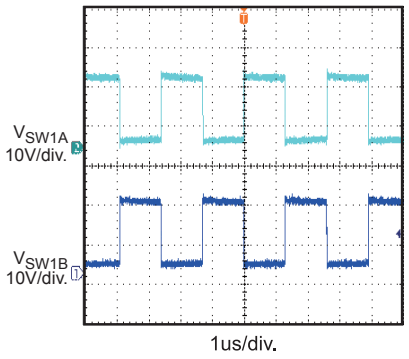
Pin #	Name	Description
28	VDR2	Gate Drive Supply Bypass. The voltage at VDR2 is supplied from an internal regulator from its respective VSP. VDR2 powers the internal circuitry and internal MOSFET gate drive for SW2A and SW2B stage. Bypass VDR2 to AGND with a 0.1µF to 10µF capacitor.
30	VDR1	Gate Drive Supply Bypass. The voltage at VDR1 is supplied from an internal regulator from its respective VSP. VDR1 powers the internal circuitry and internal MOSFET gate drive for SW1A and SW1B stage. Bypass VDR1 to AGND with a 0.1µF to 10µF capacitor.
31	BST1B	Bootstrap Supply. BST1B powers the high-side gate of the SW1B stage. Connect a 0.1µF or greater capacitor between BST1B and SW1B.
32	PGND1B	Power Ground of Channel 1B. Connect the exposed pad on the bottom side to the ground plane.

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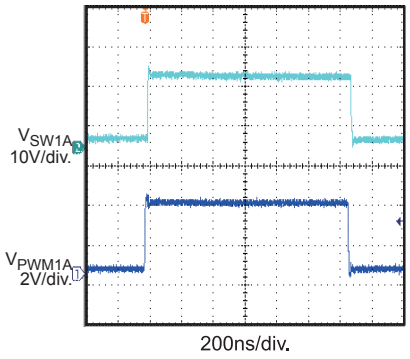
TYPICAL PERFORMANCE CHARACTERISTICS

V_{SP} = 16V, V_{SHDNB} = 5V, R_{LOAD} = 8Ω, T_A = +25°C, unless otherwise noted.

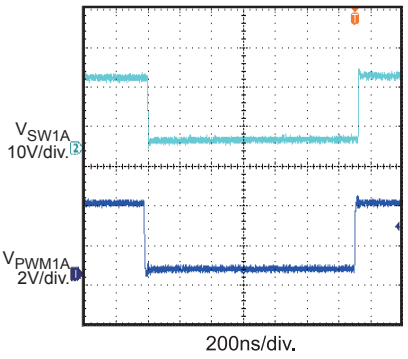
Normal Switch Waveform



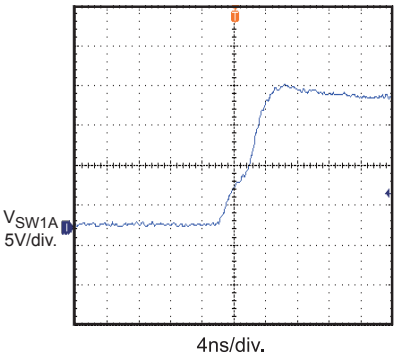
Input/Output Waveform Positive Pulse



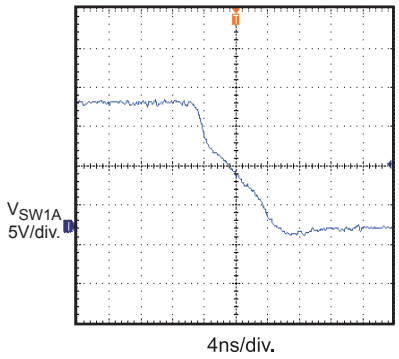
Input/Output Waveform Negative Pulse



Output Rise-Time

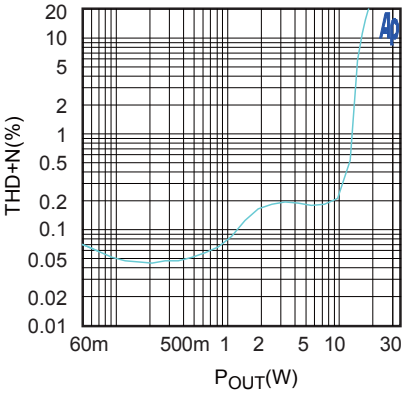


Output Fall-Time



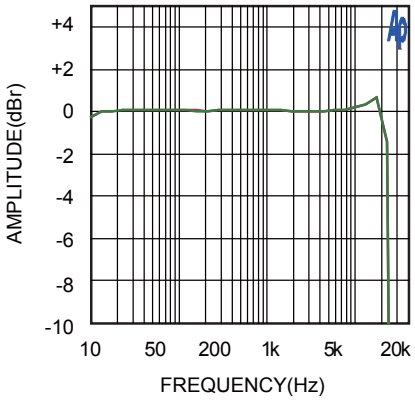
THD+N vs. P_{OUT}

16V, 8Ω, 1kHz

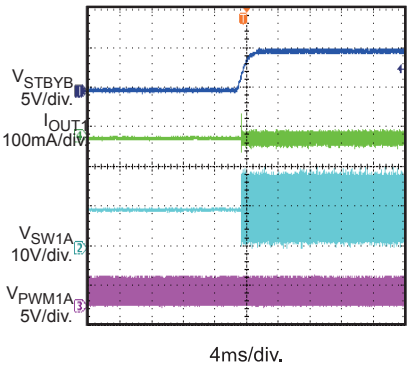


Frequency Response

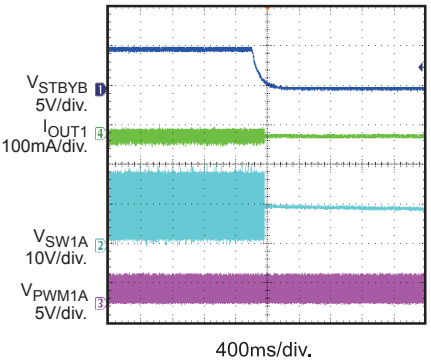
16V, 8Ω, 1W



Startup



Standby

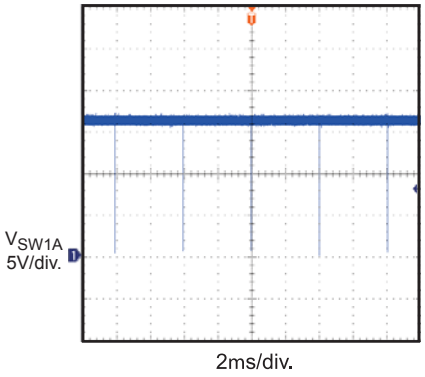


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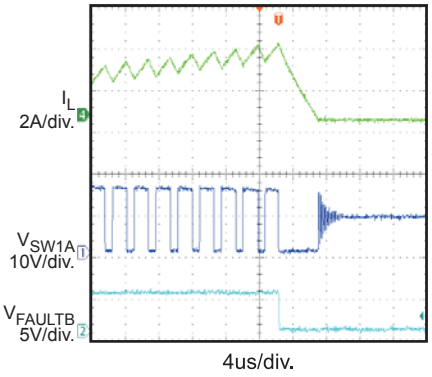
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{SP} = 16V, V_{SHDNB} = 5V, R_{LOAD} = 8Ω, T_A = +25°C, unless otherwise noted.

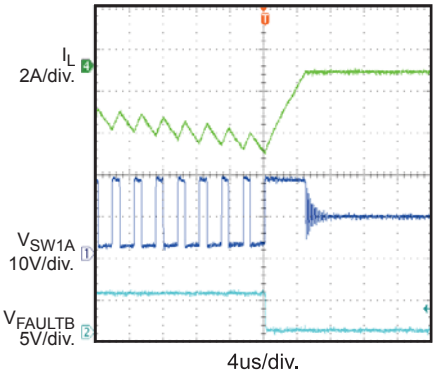
BS Recharge Cycling (16V,No load)



Short Circuit Positive Current

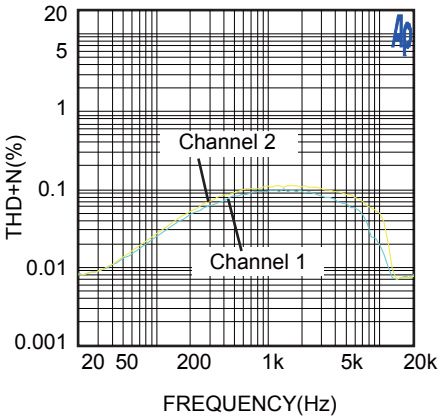


Short Circuit Negative Current



THD+N vs. Frequency

16V, 8Ω, 1W, A-wtd



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OPERATION

The MP8060 is a quad channel power half-bridge driver that can be configured as the output of a Class D amplifier. The output is in phase with the input and the dead time is optimized for symmetrical performance, regardless of load conditions.

When the shutdown (SHDNB) pin is low, all channels will be off. When the standby (STBYB) is pulled low, it causes the outputs of all channels to go into high impedance. However, when the voltage across the BST1A/1B/2A/2B and SW1A/1B/2A/2B pins drops sufficiently low, the bottom MOSFET will be turned on to refresh the external bootstrap capacitor. For a bootstrap capacitor of 100nF, the refresh time is approximately 300ns.

In order to prevent erratic operation, two under voltage lockout (UVLO) circuits are used. One of them is to ensure that the supply for the bottom gate drive circuit is sufficiently high and the other is for the top gate driver.

Fault Protection

To protect the power MOSFETs, an internal current limit of 3.5A is set for all MOSFETs. When this limit is reached, all MOSFETs will go into high impedance for a fixed duration before resuming normal operation.

Thermal monitoring is also integrated into the MP8060. If the die temperature rises above 150°C, all switches are turned off. The temperature must fall below 130°C before normal operation resumes.

To enhance the robustness of the device under short circuit condition, a capacitor can be connected to the FaultB pin, as shown in figure 1. The time constant of the RC is selected to be greater than 50ms for the FaultB node to reach 1V. Under short circuit condition, the FaultB node will be reset to zero and the part will be place in standby mode until the voltage at the STBYB pin is above 1V.

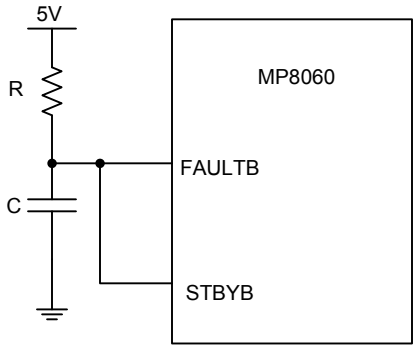


Figure 1

Fault Output

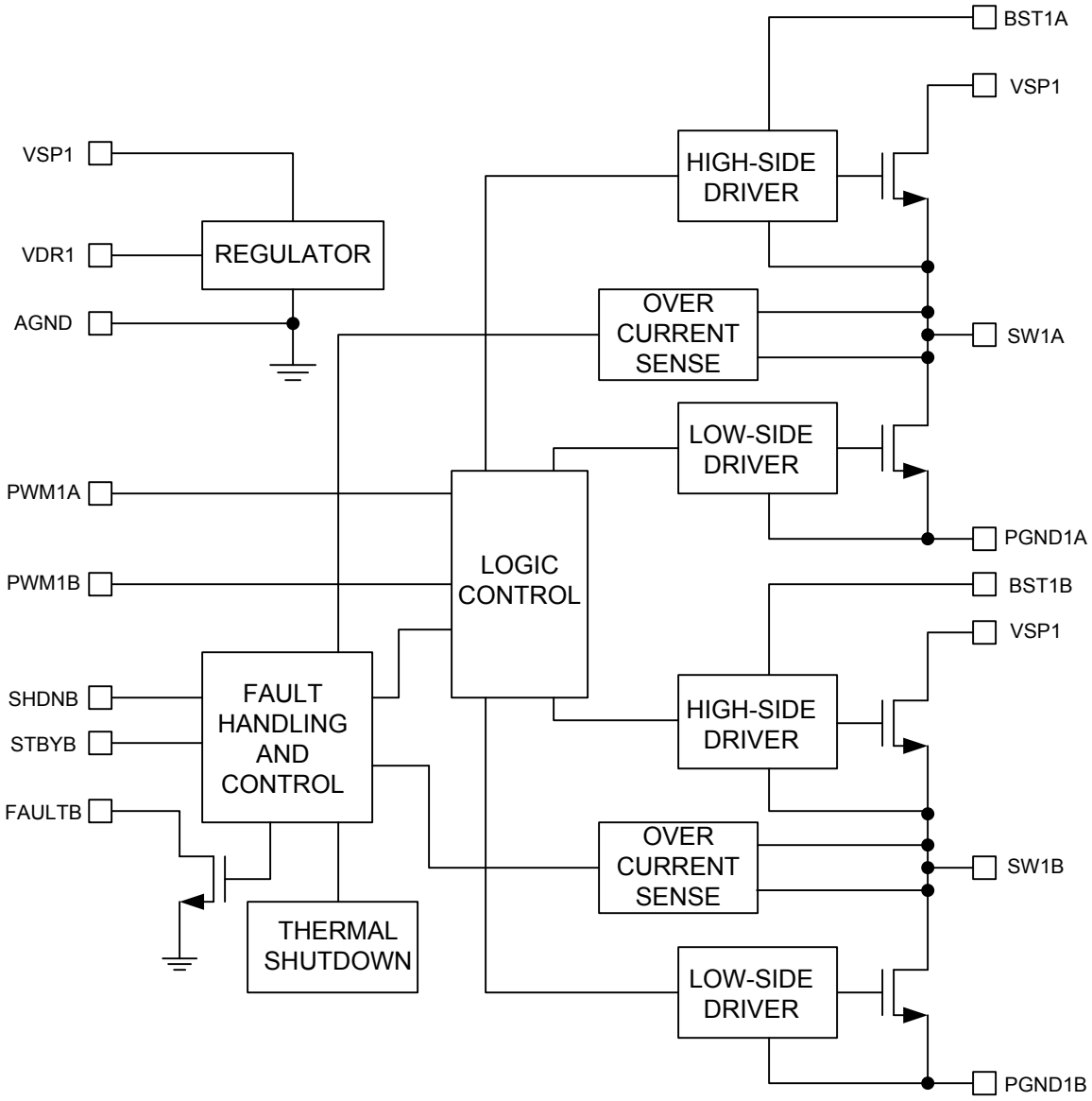
The MP8060 includes an open drain, active low fault indicator output (FAULTB). A fault will be indicated if one of the following conditions is detected: the current limit is tripped or the thermal shutdown is tripped.

A fault on any channel will cause the FAULTB pin to be pulled low. A fault on either channel will cause the outputs (SW1A, SW1B, SW2A, SW2B) to go into high impedance. When the fault goes away, the MP8060 will resume normal operation.

Do not apply more than 6V to the FAULTB pin.

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BLOCK DIAGRAM



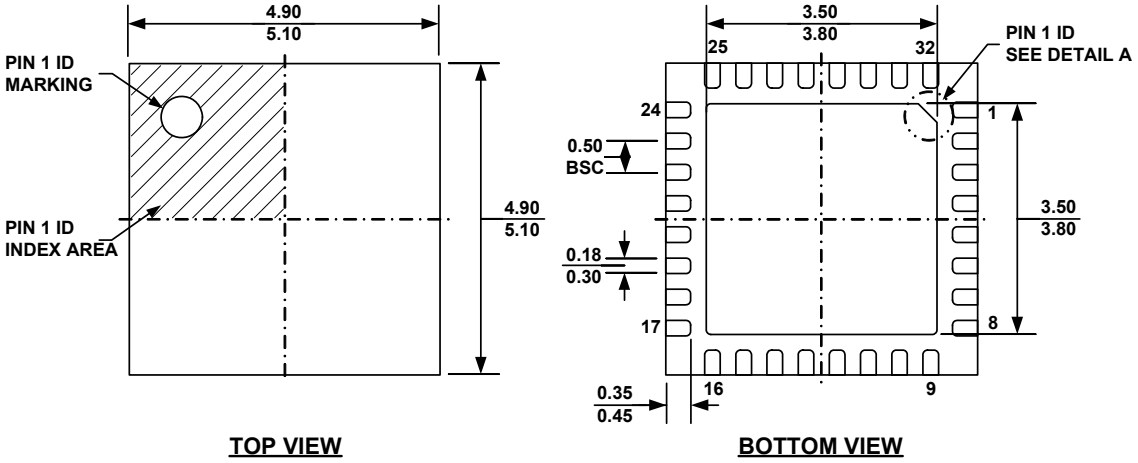
1 full bridge channel only

Figure 2—Functional Block Diagram

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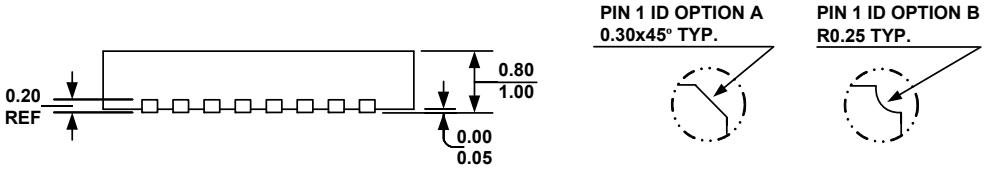
PACKAGE INFORMATION

QFN32 (5mm x 5mm)



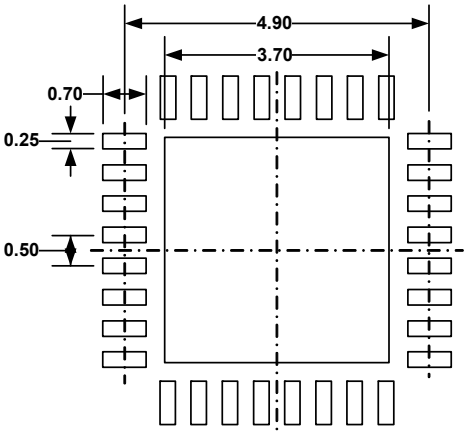
TOP VIEW

BOTTOM VIEW



SIDE VIEW

DETAIL A



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) DRAWING CONFIRMS TO JEDEC MO-220, VARIATION VHHC-2.
5) DRAWING IS NOT TO SCALE.

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