

# RZ/G Series

User's Manual: Hardware

for Rich Graphics Applications



Specifications Common to RZ/G Series Products

RZ/G1H

RZ/G1M

RZ/G1N

RZ/G1E

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## General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

### 1. Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

### 2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.  
In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

### 3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

### 4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable.

When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

### 5. Differences between Products

Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

- The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

# How to Use This Manual

## 1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the hardware functions of the MCU. It is intended for users designing application systems incorporating the MCU. A basic knowledge of electric circuits, logical circuits, and MCUs is necessary in order to use this manual.

The manual comprises the following contents; an address map, general-purpose I/O port pins, clock, reset, core functions, graphics, video processing, sound processing, and network modules, serial interfaces, storage, timers, other on-chip peripheral functions, testing, debugging, and usage notes.

For the sections on an overview of hardware, pin assignments, pin multiplexing, and pin function controller, see the user's manual for specifications of individual RZ/G series product.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

We provide the following three types of user's manual for RZ/G series products.

Make sure to refer to the latest versions of these documents.

Document Type	Description	Document Title	Document No.
User's manual for specifications of individual RZ/G series product	Overview of hardware, pin assignments, pin multiplexing, and pin function controller	RZ/G1M User's Manual: Hardware	—*
		RZ/G1N User's Manual: Hardware	
		RZ/G1H User's Manual: Hardware	
		RZ/G1E User's Manual: Hardware	
User's manual for specifications common to RZ/G series products	Hardware specifications (address map, general-purpose I/O port pins, clock, reset, core functions, graphics, video processing, sound processing, and network modules, serial interfaces, storage, timers, other on-chip peripheral functions, testing, and debugging) and descriptions of operation	RZ/G Series User's Manual: Hardware	R01UH0543EJ 0100 Rev.1.00 (This user's manual)
User's manual for electrical characteristics	Electrical characteristics of the RZ/G series products	Provided as separate technical information.	

Note: \* For the document number of each product, contact your local Renesas sales representative.

## 2. Notation for the Individual Specifications by Product

### (1) Notation for Presence or Absence of On-Chip Modules by Product

The presence or absence of on-chip modules by product is shown in the upper right hand corner of the first pages of each section.

Example:

## 50. Serial-ATA Interface

RZ/G1H	RZ/G1N
RZ/G1M	RZ/G1E

### 50.1 Overview

The serial-ATA interface provides a serial ATA physical interface which complies with the serial-ATA standard.

The example above indicates that the SATA is present in the RZ/G1H, RZ/G1M, and RZ/G1N but not in the RZ/G1E.

### (2) Notation for Presence or Absence of Pins by Product

The presence or absence of pins by product is shown in the pin configuration table in each section and section 4, Pin Multiplexing.

Example:

### 50.1.3 Input/Output Pins

Table 50.1 shows the external pins of the SATA interface.

**Table 50.1 External Pins**

Name	Pin Name	SATA Symbol	I/O	Description	RZ/G Series Products			
					RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Reference clock	CICREFP0_SATA	—	Input	Reference clock input to the PLL circuit in the Serial-ATA module (differential input). Apply a 100-MHz clock.	√	√	√	—
	CICREFN0_SATA							
	CICREFP1_SATA							
	CICREFN1_SATA							
Transmit data	TODP0_SATA	TX+	Output	Pins for data transmission pins. A 3.0-GHz (second generation) signal or 1.5-GHz (first generation) signal is transmitted through these pins.  The pins with names ending in P and N are combined to provide a differential signal.	√	√	√	—
	TODN0_SATA							
	TODP1_SATA							
	TODN1_SATA							

The example above indicates that the CICREFP0\_SATA pin is present in the RZ/G1H, RZ/G1M, and RZ/G1N but not in the RZ/G1E.

### (3) Notation for Presence or Absence of Registers by Product

The presence or absence of registers by product is shown in the list of registers and the descriptions of registers in each section.

Example:

50.2.2 ATAPI Control Register (ATAPI_CONTROL1)			
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

The example above indicates that the ATAPI\_CONTROL1 register is present in the RZ/G1H, RZ/G1M, and RZ/G1N but not in the RZ/G1E.

### 3. Notation of Numbers and Symbols

Bit notation : Bits are shown in high-to-low order from left to right.

Number notation: Binary numbers are given as B'XXXX, hexadecimal numbers are given as H'XXXX, and decimal numbers are given as XXXX.

Signal notation: A number sign (#) after the name indicates that a signal or pin is active-low, unless otherwise specified.

Example: PRESET#

## 4. Register Notation

Each register description includes a bit chart, illustrating the arrangement of bits, and a table of bits, describing the meanings of the bit settings.

**[Bit Chart]**

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	ASID2	ASID1	ASID0	—	—	—	—	—	Q	ACMP2	ACMP1	ACMP0	IFE	
Initial value:	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

(1) (2) (3) (4) (5)

**[Table of Bits]**

Bit	Bit Name	Initial Value	R/W	Description
15	—	0	R	Reserved
14	—	0	R	These bits are always read as 0.
13 to 11	ASID2 to ASID0	All 0	R/W	Address Identifier These bits enable or disable the pin function.
10	—	0	R	Reserved This bit is always read as 0.
9	—	1	R	Reserved This bit is always read as 1.
8 to 0	—	0	—	—

Note: The bit names and sentences in the above figure are examples, and have nothing to do with the contents of this manual.

- (1) Bit  
Indicates the bit number or numbers.  
In the case of a 32-bit register, the bits are arranged in order from 31 to 0. In the case of a 16-bit register, the bits are arranged in order from 15 to 0.
- (2) Bit name  
Indicates the name of the bit or bit field.  
When the number of bits has to be clearly indicated in the field, appropriate notation is included (e.g., ASID[3:0]).  
A reserved bit is indicated by "—".  
Certain kinds of bits, such as those of timer counters, are not assigned bit names. In such cases, the entry under Bit Name is blank.
- (3) Initial value  
Indicates the value of each bit immediately after a power-on reset, i.e., the initial value.  
0: The initial value is 0.  
1: The initial value is 1.  
—: The initial value is undefined
- (4) R/W  
For each bit and bit field, this entry indicates whether the bit or field is readable or writable, or both writing to and reading from the bit or field are impossible.  
The notation is as follows:  
R/W: The bit or field is readable and writable.  
R/(W): The bit or field is readable and writable.  
However, writing is only performed to flag clearing.  
R/WC0: The bit or field is readable and writable. Writing 0 to the bit initializes the bit.  
Writing 1 to the bit is ignored.  
R/WC1: The bit or field is readable and writable. Writing 1 to the bit initializes the bit.  
Writing 0 to the bit is ignored.  
R: The bit or field is readable.  
"R" is indicated for all reserved bits. When writing to the register, write the value under Initial Value in the bit chart to reserved bits or fields.  
W: The bit or field is writable.  
Note that values read from write-only bits are not guaranteed, unless they are specified in the chart of bits.
- (5) Description  
Describes the function of the bit or field and specifies the values for writing.

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## 1. Overview

See section 1, Overview in the user's manual for specifications of individual RZ/G series product.

## 2. Area Map

<b>RZ/G1H</b>	<b>RZ/G1N</b>
<b>RZ/G1M</b>	<b>RZ/G1E</b>

**Table 2.1 Address Space (Over 4-Gbyte Space)**

Address	Space	Description	RZ/G Series Products			
			RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
H'00_00000000 to H'00_FFFFFFFF	Legacy 4-Gbyte space	LBSC, DBSC3, etc.	√	√	√	√
H'01_00000000 to H'01_FFFFFFFF	DDR0/DBSC3 (DDR0)	DBSC3	√	√	√	√
H'02_00000000 to H'02_FFFFFFFF	DDR1*	DBSC3 [H, M]	√	√	—	—
	Reserved	—	—	—	√	√
H'03_00000000 to H'03_FFFFFFFF (H'03_40000000 to H'03_BFFFFFFF)	DBSC3 (DDR0) shadow	DBSC3 (up to 2 Gbytes)	√	√	√	√
H'04_00000000 to H'04_FFFFFFFF	DDR0 shadow	DBSC3 [H, M, N, E]	√	√	√	√
H'05_00000000 to H'05_FFFFFFFF	DDR1 shadow*	[H, M]	√	√	—	—
	Reserved	[M, N, E]	—	—	√	√
H'06_00000000 to H'06_FFFFFFFF	Reserved	[H, M, N]	√	√	√	—
	DDR0 shadow	[E]	—	—	—	√
H'07_00000000 to H'07_FFFFFFFF	Reserved	—	√	√	√	√
H'08_00000000 to H'08_FFFFFFFF	CCI-AXI	CCI-AXI	√	√	√	√
H'09_00000000 to H'09_FFFFFFFF	Reserved	—	√	√	√	√
H'0A_00000000 to H'0A_FFFFFFFF	Reserved	—	√	√	√	√
H'0B_00000000 to H'0B_FFFFFFFF	Reserved	—	√	√	√	√
H'0C_00000000 to H'0C_FFFFFFFF	Reserved	—	√	√	√	√
H'0D_00000000 to H'0D_FFFFFFFF	Reserved	—	√	√	√	√
H'0E_00000000 to H'0E_FFFFFFFF	Reserved	—	√	√	√	√
H'0F_00000000 to H'0F_0FFFFFFF	uTLB (IPMMUS0 slave)	IPMMUv7 slave for uTLB (SYS0)	√	√	√	√
H'0F_10000000 to H'0F_1FFFFFFF	uTLB (IPMMUS1 slave)	IPMMUv7 slave for uTLB (SYS1)	√	√	√	√
H'0F_20000000 to H'0F_2FFFFFFF	uTLB (IPMMUMP slave)	IPMMUv7 slave for uTLB (MP)	√	√	√	√
H'0F_30000000 to H'0F_3FFFFFFF	Reserved	—	√	√	√	√
H'0F_40000000 to H'0F_4FFFFFFF	uTLB (IPMMUDS slave)	IPMMUv7 slave for uTLB (SYS-DMA)	√	√	√	√
H'0F_50000000 to H'0F_5FFFFFFF	uTLB (IPMMUM slave)	IPMMUv7 slave for uTLB (Media)	√	√	√	√
H'FF_00000000 to H'FF_FFFFFFFF	Reserved	—	√	√	√	√

Notes: Access to the reserved spaces is prohibited.

- \* These DDR1 spaces cannot be accessed in 32-bit address mode regardless of the sizes of the memories. Access to these DDR1 spaces should always proceed in the 40-bit address mode of the Cortex-A15/Cortex-A7 or G6400 and other modules. For details, refer to section 15, External Bus Controller for DDR3-SDRAM (DBSC3).

Table 2.2 Address Space (Legacy 4-Gbyte Space)

Address	Space	Description	RZ/G Series Products			
			RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
H'00_0000000 to H'00_03FFFFFF	LBSC	Area 0 asynchronous memory	√	√	√	√
H'00_0400000 to H'00_07FFFFFF		Area 1 asynchronous memory	√	√	√	√
H'00_0800000 to H'00_0BFFFFFF		Reserved	√	√	√	√
H'00_0C00000 to H'00_0FFFFFFF		Reserved	√	√	√	√
H'00_1000000 to H'00_13FFFFFF		Reserved	√	√	√	√
H'00_1400000 to H'00_15FFFFFF		Reserved	√	√	√	√
H'00_1600000 to H'00_17FFFFFF		Reserved	√	√	√	√
H'00_1800000 to H'00_19FFFFFF		Area 6A asynchronous memory	√	√	√	√
H'00_1A00000 to H'00_1BFFFFFF		Area 6B asynchronous memory	√	√	√	√
H'00_1C00000 to H'00_1FFFFFFF		Reserved	√	√	√	√
H'00_2000000 to H'00_2FFFFFFF		Reserved	√	√	√	√
H'00_3000000 to H'00_37FFFFFF	PCIEC	PCI express memory 2	√	√	√	—
	Reserved	[E]	—	—	—	√
H'00_3800000 to H'00_3FFFFFFF	PCIEC	PCI express memory 3	√	√	√	—
	Reserved	[E]	—	—	—	√
H'00_4000000 to H'00_5FFFFFFF	DBSC3 (DDR0)	SDRAM Area	√	√	√	√
H'00_6000000 to H'00_7FFFFFFF		(over 4-Gbyte mirror space)	√	√	√	√
H'00_8000000 to H'00_BFFFFFFF			√	√	√	√
H'00_C000000 to H'00_E5FFFFFF	Reserved	—	√	√	√	√
H'00_E600000 to H'00_E61FFFFFFF	SYS-APB1	System-domain peripheral bus (CP)	√	√	√	√
H'00_E620000 to H'00_E6BFFFFFFF	SYS-APB2	System-domain peripheral bus (HP)	√	√	√	√
H'00_E6C0000 to H'00_E6FFFFFFF	SYS-APB3	System-domain peripheral bus (MP)	√	√	√	√
H'00_E700000 to H'00_E7FFFFFFF	Reserved		√	√	√	√
H'00_E800000 to H'00_E807FFFFFFF	S3 cache	IPMMU, ICB control register	√	√	√	√
H'00_E808000 to H'00_E827FFFFFFF	S3 cache	On-chip RAM (S3 cache used as RAM: 1 MB)	√	—	—	—
	Reserved	[M, N, E]	—	√	√	√
H'00_E828000 to H'00_E8FFFFFFF	Reserved	—	√	√	√	√
H'00_E900000 to H'00_E9FFFFFFF	CDBGTOP STM	CoreSight STM	√	√	√	√
H'00_EA00000 to H'00_EA0FFFFFFF	Reserved	—	√	√	√	√
H'00_EA10000 to H'00_EA1FFFFFFF	Reserved	—	√	√	√	√
H'00_EA20000 to H'00_EAFFFFFFF	Reserved	—	√	√	√	√
H'00_EB00000 to H'00_EB3FFFFFFF	Reserved	—	√	√	√	√
H'00_EB40000 to H'00_EB7FFFFFFF	Reserved	—	√	√	√	√

					<b>RZ/G Series Products</b>			
<b>Address</b>			<b>Space</b>	<b>Description</b>	<b>RZ/G1H</b>	<b>RZ/G1M</b>	<b>RZ/G1N</b>	<b>RZ/G1E</b>
H'00_EB800000	to	H'00_EBBFFFFFFF	Reserved	—	√	√	√	√
H'00_EBC00000	to	H'00_EBFFFFFFF	Reserved	—	√	√	√	√
H'00_EC000000	to	H'00_EC0FFFFFFF	MP-APB1	SRC/CMD	√	√	√	√
H'00_EC100000	to	H'00_EC1FFFFFFF	MP-APB2	SSIU	√	√	√	√
H'00_EC200000	to	H'00_EC2FFFFFFF	MP-APB3	SSI0-9	√	√	√	√
H'00_EC300000	to	H'00_EC3FFFFFFF	MP-APB4	SRC/CMD	√	√	√	√
H'00_EC400000	to	H'00_EC4FFFFFFF	MP-APB5	SSIU	√	√	√	√
H'00_EC500000	to	H'00_EC5FFFFFFF	MP-APB6	SRC/CMD/SSIU/SSI/ADG	√	√	√	√
H'00_EC600000	to	H'00_EC9FFFFFFF	MP-APB7	SYS-DMAC/Audio-DMAC	√	√	√	√
				Audio-DMAC-P-P	√	√	√	√
H'00_ECA00000	to	H'00_ECBFFFFFFF	Reserved	—	√	√	√	√



					<b>RZ/G Series Products</b>			
<b>Address</b>		<b>Space</b>	<b>Description</b>	<b>RZ/G1H</b>	<b>RZ/G1M</b>	<b>RZ/G1N</b>	<b>RZ/G1E</b>	
H'00_ECC00000	to	H00_ECFFFFFF	Reserved	—	√	√	√	√
H'00_ED000000	to	H'00_EDFFFFFF	S3 cache	On-chip RAM mirror address for MP-domain	√	√	√	√
H'00_EE000000	to	H'00_EE03FFFF	USB3	USB3.0 (Host) [H, M, N]	√	√	√	—
			Reserved	[E]	—	—	—	√
H'00_EE040000	to	H'00_EE07FFFF	Reserved	—	√	√	√	√
H'00_EE080000	to	H'00_EE09FFFF	USB0	USB (EHCI)	√	√	√	√
H'00_EE0A0000	to	H'00_EE0BFFFF	USB1	[H]	√	—	—	—
			Reserved	[M, N, E]	—	√	√	√
H'00_EE0C0000	to	H'00_EE0DFFFF	USB2	[H]	√	—	—	—
			USB1	[M, N, E]	—	√	√	√
H'00_EE0E0000	to	H'00_EE0E7FFF	Reserved	—	√	√	√	√
H'00_EE0E8000	to	H'00_EE0EBFFF	STBE	SRAM area (16 KB) for the EtherAVB descriptor	√	√	√	√
H'00_EE0EC000	to	H'00_EE0EFFFF	Reserved	—	√	√	√	√
H'00_EE100000	to	H'00_EE1FFFFFF	SDHI	SDHI	√	√	√	√
H'00_EE200000	to	H'00_EE2FFFFFF	eMMC	eMMC	√	√	√	√
H'00_EE300000	to	H'00_EE4FFFFFF	SATA0	[H, M, N]	√	√	√	—
			Reserved	[E]	—	—	—	√
H'00_EE500000	to	H'00_EE6FFFFFF	SATA1	[H, M]	√	√	—	—
			Reserved	[N, E]	—	—	√	√
H'00_EE700000	to	H'00_EE8FFFFFF	EtherMAC	EtherMAC	√	√	√	√
H'00_EE900000	to	H'00_EFFFFFFF	Reserved	—	√	√	√	√
(H'00_F0000000	to	H'00_F0FFFFFF)	Reserved	—	√	√	√	√

				<b>RZ/G Series Products</b>				
<b>Address</b>		<b>Space</b>	<b>Description</b>	<b>RZ/G1H</b>	<b>RZ/G1M</b>	<b>RZ/G1N</b>	<b>RZ/G1E</b>	
H'00_F1000000	to	H'00_F10FFFFFF	GIC	GIC	√	√	√	√
(H'00_F1000000	to	H'00_FBFFFFFF)	Reserved	—	√	√	√	√
H'00_F1100000	to	H'00_FBFFFFFF	Reserved	—	√	√	√	√
H'00_FC000000	to	H'00_FCFFFFFF	DBG	Debug module (JTAG)	√	√	√	√
H'00_FD000000	to	H'00_FD7FFFFF	3DG	3D accelerator control register (32 bit) PowerVR G6400 [H]	√	—	—	—
			Reserved	[M, N, E]	—	√	√	√
H'00_FD800000	to	H'00_FDFFFFFF	3DG	3D accelerator control register (128 bit) PowerVR G6400 [H], SGX544MP2 [M, N], SGX540 [E]	√	√	√	√
H'00_FE000000	to	H'00_FE0FFFFF	PCIEC	PCI express configuration [H, M, N]	√	√	√	—
			Reserved	[E]	—	—	—	√
H'00_FE100000	to	H'00_FE1FFFFF	PCIEC	PCI express memory 0 [H, M, N]	√	√	√	—
			Reserved	[E]	—	—	—	√
H'00_FE200000	to	H'00_FE3FFFFF	PCIEC	PCI express memory 1 [H, M, N]	√	√	√	—
			Reserved	[E]	—	—	—	√
H'00_FE400000	to	H'00_FE5FFFFF	Reserved	—	√	√	√	√
H'00_FE600000	to	H'00_FE67FFFF	MXT	Image accelerator control registers	√	√	√	√
H'00_FE680000	to	H'00_FE6FFFFF						
H'00_FE700000	to	H'00_FE77FFFF						
H'00_FE780000	to	H'00_FE82FFFF		Reserved				
H'00_FE830000	to	H'00_FE85FFFF		Reserved	√	√	√	√
H'00_FE860000	to	H'00_FE86FFFF		IMR-LSX2-0 (optional)	√	—	—	—
				Reserved	—	√	√	√

					<b>RZ/G Series Products</b>			
<b>Address</b>			<b>Space</b>	<b>Description</b>	<b>RZ/G1H</b>	<b>RZ/G1M</b>	<b>RZ/G1N</b>	<b>RZ/G1E</b>
H'00_FE870000	to	H'00_FE87FFFF	MXT	IMR-LSX2-1(optional)	√	—	—	—
					—	√	√	—
H'00_FE880000	to	H'00_FE8FFFFF		Reserved	√	√	√	√
H'00_FE900000	to	H'00_FE93FFFF	SYS-APB7	Image accelerator control	√	√	√	√
H'00_FE940000	to	H'00_FE95FFFF		register				
H'00_FE960000	to	H'00_FEA0FFFF						
H'00_FEAB0000	to	H'00_FEACFFFF	Reserved	—	√	√	√	√
H'00_FEAD0000	to	H'00_FEADFFFF	MXT	IMR-X2-0 [H] (optional)	√	—	—	—
H'00_FEA00000	to	H'00_FEA0FFFF	Reserved	—	√	√	√	√
H'00_FEAF0000	to	H'00_FEB0FFFF	MXT	IMR-X2-1 [H] (optional)	√	—	—	—
H'00_FEC00000	to	H'00_FEC0FFFF	LBSC	Asynchronous memory controller control register	√	√	√	√
(H'00_FF000000	to	H'00_FF50FFFF)	Reserved	—	√	√	√	√
H'00_FF000000	to	H'00_FF10FFFF	SYS-APB8	AXI router	√	√	√	√
H'00_FF600000	to	H'00_FF60FFFF	Reserved	—	√	√	√	√
H'00_FF700000	to	H'00_FF70FFFF	Reserved	—	√	√	√	√
H'00_FF800000	to	H'00_FF80FFFF	SYS-APB8	AXI-bus register	√	√	√	√
H'00_FFC00000	to	H'00_FFC0FFFF	RT-APB1/ RT-AHB4	Realtime-domain low-speed peripheral bus	√	√	√	√
H'00_FFD00000	to	H'00_FFD0FFFF	RT-APB2/ RT-AHB5	Realtime-domain high-speed peripheral bus	√	√	√	√
H'00_FFF00000	to	H'00_FFF0FFFF	RT-APB3/ RT-AHB6	Realtime-domain high-speed peripheral bus	√	√	√	√

Note: Access to reserved spaces and reserved addresses is prohibited.

**Table 2.3 List of Module Base Address in each Domain (CP, HP, MP and other Clock Domains)**

Domain	Address[31:24]	Address[23:0]	Module	RZ/G Series Products			
				RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
SYS-APB1 (cpck)	H'E6	H'00 1000	APB REG	√	√	√	√
		H'02 0000	RWDT	√	√	√	√
		H'05 0000	GPIO0	√	√	√	√
		H'05 1000	GPIO1	√	√	√	√
		H'05 2000	GPIO2	√	√	√	√
		H'05 3000	GPIO3	√	√	√	√
		H'05 4000	GPIO4	√	√	√	√
		H'05 5000	GPIO5	√	√	√	√
		H'05 5400	GPIO6	—	√	√	√
		H'05 5800	GPIO7	—	√	√	√
		H'06 0000	PFC	√	√	√	√
		H'08 0000	ARM Generic Counter	√	√	√	√
		H'0B 0000	IIC3 (I2C6) (DVFS)	√	√	√	—
		H'0F 0000	TPU0	√	√	√	√
		H'10 0000	DBG	√	√	√	√
		H'13 0000	CMT1	√	√	√	√
		H'15 0000	CPGA	√	√	√	√
		H'16 0000	RESET	√	√	√	√
		H'18 0000	SYSC	√	√	√	√
		H'1C 0000	IRQC	√	√	√	√
H'1E 0000	TMU0 (channels 0 to 2)	√	√	√	√		
H'1F 0000	Thermal sensor	√	√	√	—		

Domain	Address[31:24]	Address[23:0]	Module	RZ/G Series Products			
				RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
SYS-APB2 (hpck)	H'E6	H'28 0000	IPMMUS0	√	√	√	√
		H'29 0000	IPMMUS1	√	√	√	√
		H'2A 0000	IPMMUGP	—	√	√	√
		H'2C 0000	HSCIF0	√	√	√	√
		H'2C 8000	HSCIF1	√	√	√	√
		H'2D 0000	HSCIF2	—	√	√	√
		H'36 0000	PublicROM	√	√	√	—
		H'37 0000	PublicROM	√	√	√	—
		H'3A 0000	Inter-connect RAM 0	√	√	√	√
		H'3B 0000	Inter-connect RAM 0	√	√	√	√
		H'3C 0000	Inter-connect RAM 1	√	√	√	√
		H'50 0000	IIC0 ([M/N]: I2C7, [E]: I2C6)	√	√	√	√
		H'50 8000	I2C0	√	√	√	√
		H'51 0000	IIC1 ([M/N]: I2C8, [E]: I2C7)	√	√	√	√
		H'51 8000	I2C1	√	√	√	√
		H'52 0000	IIC2	√	—	—	—
			I2C4	—	√	√	√
		H'52 8000	I2C5	—	√	√	√
		H'53 0000	I2C2	√	√	√	√
		H'54 0000	I2C3	√	√	√	√

Domain	Address[31:24]	Address[23:0]	Module	RZ/G Series Products			
				RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
SYS-APB2 (hpck)	H'E6	H'59 0000	USBHS	√	√	√	√
		H'5A 0000	USBHS-DMAC	√	√	√	√
		H'5B 0000	USBHS-DMAC	√	√	√	√
		H'5C 0000	USBHS-DMAC (DDM)	√	√	√	√
		H'70 0000	SYS-DMAC (0 to 14)	√	√	√	√
		H'72 0000	SYS-DMAC (15 to 29)	√	√	√	√
		H'74 0000	IPMMUDS	√	√	√	√
		H'78 0000	S3CTRL	√	√	√	√
		H'79 0000	DBSC0	√	√	√	√
		H'7A 0000	DBSC1	√	√	—	—
SYS-Ether	H'E6	H'80 0000	EtherAVB	√	√	√	√
SYS-QSPI	H'E6	H'B1 0000	QSPI	√	√	√	√
SYS-APB3 (mpck)	H'E6	H'C2 0000	SCIFB0	√	√	√	√
		H'C3 0000	SCIFB1	√	√	√	√
		H'C4 0000	SCIFA0	√	√	√	√
		H'C5 0000	SCIFA1	√	√	√	√
		H'C6 0000	SCIFA2	√	√	√	√
		H'C7 0000	SCIFA3	—	√	√	√
		H'C7 8000	SCIFA4	—	√	√	√
		H'C8 0000	SCIFA5	—	√	√	√
		H'C9 0000	MSIOF3	√	—	—	—
		H'CE 0000	SCIFB2	√	√	√	√
		H'E0 0000	MSIOF2	√	√	√	√
		H'E1 0000	MSIOF1	√	√	√	√
		H'E2 0000	MSIOF0	√	√	√	√

Domain	Address[31:24]	Address[23:0]	Module	RZ/G Series Products					
				RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E		
65 MHz clock module	H'E6	H'E3 0000	PWM0	√	√	√	√		
		H'E3 1000	PWM1	√	√	√	√		
		H'E3 2000	PWM2	√	√	√	√		
		H'E3 3000	PWM3	√	√	√	√		
		H'E3 4000	PWM4	√	√	√	√		
		H'E3 5000	PWM5	√	√	√	√		
		H'E3 6000	PWM6	√	√	√	√		
		H'E5 6000	SCIF2 [H]	√	—	—	—		
		H'E5 8000	SCIF2 [M/N, E]	—	√	√	√		
		H'E6 0000	SCIF0	√	√	√	√		
		H'E6 8000	SCIF1	√	√	√	√		
		H'E8 0000	CAN0	√	√	√	√		
		H'E8 8000	CAN1	√	√	√	√		
		H'EA 8000	SCIF3	—	√	√	√		
		H'EB 0000	GL2	√	√	√	√		
		H'EC 0000	R-GP2D	√	—	—	—		
		H'EE 0000	SCIF4	—	√	√	√		
		H'EE 8000	SCIF5	—	√	√	√		
		H'EF 0000	VIN0	√	√	√	√		
		H'EF 1000	VIN1	√	√	√	√		
		H'EF 2000	VIN2	√	√	√	—		
		H'EF 3000	VIN3	√	—	—	—		
		SYS-APB2	H'E6	H'F0 0000	CoreSight APB bridge	√	√	√	√
				H'F1 0000	CoreSight APB bridge				
				H'F2 0000	CoreSight APB bridge				
				:	CoreSight APB bridge				
H'FD 0000	CoreSight APB bridge								
H'FE 0000	CoreSight APB bridge								
H'FF 0000	CoreSight APB bridge								

Domain	Address[31:24]	Address[23:0]	Module	RZ/G Series Products			
				RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
MP-APB1	H'EC	H'00 0000	SRC_CMD_BUSIF (window)	√	√	√	√
MP-APB2	H'EC	H'10 0000	SSIU (window)	√	√	√	√
MP-APB3	H'EC	H'24 1000	SSI0 to SSI9 (window)	√	√	√	√
MP-APB4	H'EC	H'30 0000	SRC_CMD_BUSIF (window)	√	√	√	√
MP-APB5	H'EC	H'40 0000	SSIU (window)	√	√	√	√
MP-APB6	H'EC	H'50 0000	SRC0 to SRC9, CMD0, and CMD1 (apb)	√	√	√	√
		H'54 0000	SSIU	√	√	√	√
		H'54 1000	SSI0 to SSI9 (apb)	√	√	√	√
		H'5A 0000	ADG (apb)	√	√	√	√
MP-APB7	H'EC	H'68 0000	IPMMUMP	√	√	√	√
		H'70 0000	Audio-DMAC (0 to 12, apb)	√	√	√	√
		H'72 0000	Audio-DMAC (13 to 25, apb)	√	√	√	—
		H'74 0000	Audio DMAC-P-P (apb)	√	√	√	√
SDHI	H'EE	H'10 0000	SDHI0	√	√	√	√
		H'12 0000	SDHI1	√	—	—	—
eMMC	H'EE	H'20 0000	MMC0	√	√	√	√
		H'22 0000	MMC1	√	—	—	—



Domain	Address[31:24]	Address[23:0]	Module	RZ/G Series Products					
				RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E		
MXT	H'FE	H'86 0000	IMR-LSX2-0 [H] (optional)	√	—	—	—		
		H'87 0000	IMR-LSX2-1 [H] (optional)	√	—	—	—		
		H'90 0000	VLC (VCP)	√	√	√	√		
		H'90 0200	CE (VCP)	√	√	√	√		
		H'90 8000	VPC0	√	√	√	√		
		H'91 0000	VLC (VCP1)	√	—	—	—		
		H'91 0200	CE (VCP1)	√	—	—	—		
		H'91 8000	VPC1	√	—	—	—		
		H'92 0000	VSPR [H] DCU [M/N, E]	√	√	√	√		
		H'92 8000	VSPS	√	√	√	√		
		H'93 0000	VSPD0	√	√	√	√		
		H'93 8000	VSPD1	√	√	√	—		
		H'94 0000	FDP1-0	√	√	√	√		
		H'94 4000	FDP1-1	√	√	√	—		
		H'94 8000	FDP1-2	√	—	—	—		
		H'95 1000	IPMMUI	√	√	√	√		
		H'96 0000	MXI	√	√	√	√		
		MXT	H'FE	H'A0 0000	2D-DMAC	√	√	√	√
				H'AD 0000	IMR-X2-0 [H] (optional)	√	—	—	—
				H'AF 0000	IMR-X2-1 [H] (optional)	√	—	—	—
H'B0 0000	DU0-0			√	√	√	√		
H'B4 0000	DU0-1			√	—	—	—		
H'B8 8000	DRC0			√	—	—	—		
H'B9 0000	LVDS0			√	√	√	—		
H'B9 4000	LVDS1			√	—	—	—		
SYS-APB8	H'FF	H'00 0044	PRR	√	√	√	√		
		H'80 0000	SYS-AXIRouter	√	√	√	√		
		H'82 0000	MP-AXIRouter	√	√	√	√		
		H'84 0000	Audio-AXIRouter	√	√	√	√		
		H'85 0000	DM-AXIRouter	√	√	√	√		
		H'86 0000	SYS-AXIRouter256	√	√	√	√		
		H'87 0000	MediaTarget	√	√	√	√		
		H'88 0000	CCI-AXI	√	√	√	√		
RT-APB1 (bck)	H'FF	H'CA 0000	CMT0	√	√	√	√		

Domain	Address[31:24]	Address[23:0]	Module	RZ/G Series Products			
				RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
RT-APB2 (hpck)	H'FF	H'E8 0000	TSIF0	—	√	—	—
RT-APB3 (pclk)	H'FF	H'F6 0000	TMU1 (channels 3 to 5)	√	√	√	√
		H'F7 0000	TMU2 (channels 6 to 8)	√	√	√	√
		H'F8 0000	TMU3 (channels 9 to 11)	√	√	√	√

- Notes: 1. "—": Undefined address  
 2. Addresses other than the above are reserved and access to reserved or undefined addresses is prohibited.  
 3. Some modules are internal and unused.  
 Contact your local sales representative regarding modules listed as "optional" in the table.

## 3. Pin Assignment

See section 3, Pin Assignment in the user's manual for specifications of individual RZ/G series product.

## 4. Pin Multiplexing

See section 4, Pin Multiplexing in the user's manual for specifications of individual RZ/G series product.

## 5. Pin Function Controller (PFC)

See section 5, Pin Function Controller (PFC) in the user's manual for specifications of individual RZ/G series product.

## 6. General-Purpose Input/Output Ports (GPIO)

RZ/G1H	RZ/G1N
RZ/G1M	RZ/G1E

### 6.1 Overview

The RZ/G series products have up to eight GPIO blocks\*<sup>1</sup>, each of which is a functional block that supports up to 32 port pins for general input/output and interrupt input. (A maximum of 188 to 244 ports\*<sup>2</sup> pins in total can be used. Note that the port pins are multiplexed.) When the relevant register is written to, a signal is output via the corresponding general output port pin. When a signal is input via the general input port pin, the corresponding register indicates the value of the input signal; specifically, when an interrupt is input via a general port pin, the relevant register indicates that it is currently receiving an interrupt input, and an interrupt is also requested to the CPU core via the interrupt control block. The functions (modes) can be assigned to each port pin as desired by some setting the corresponding registers. It is also possible to select the signal polarity (positive or negative logic) and the interrupt detection condition (one edge/both edge or level) for each port. In this LSI, general output data mode of GPIO can be set in normal mode (outputting data as normal) or high/low level data output mode. Particularly, a filtering function to prevent external chattering is also available for port pins 0 to 3 in input modes for each GPIO block.

- Notes: 1. The number of the dedicated GPIO blocks varies depending on the product; 6 in the RZ/G1H, 8 in the RZ/G1M and RZ/G1N, and 7 in the RZ/G1E.
2. 188 ports [RZ/G1H], 244 ports [RZ/G1M and RZ/G1N], 208 ports. [RZ/G1E]

6.1.1 GPIO Block Diagram (block n)

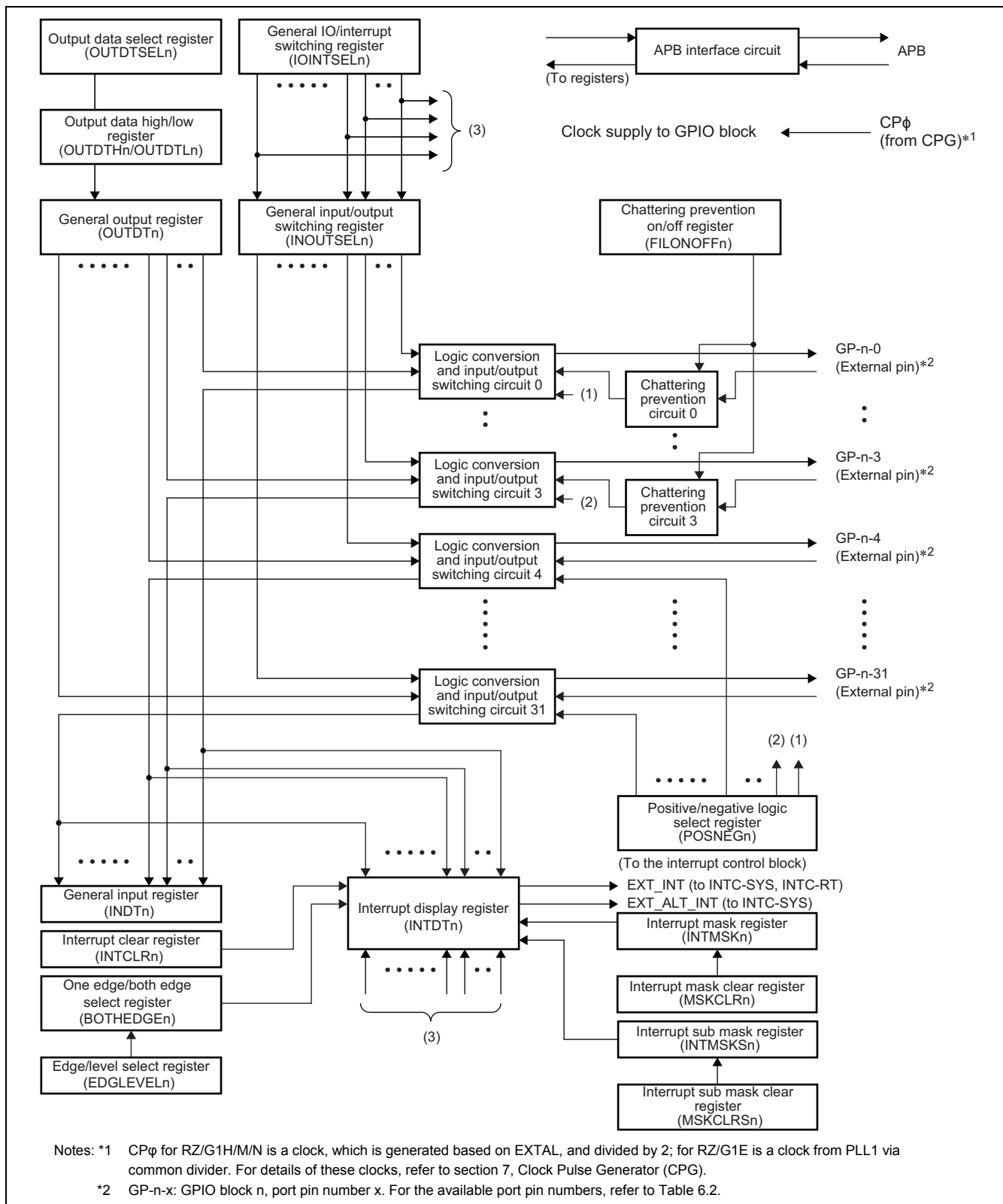


Figure 6.1 GPIO Block Configuration

### 6.1.2 I/O Pins

Table 6.1 shows the pin configuration of the GPIO.

**Table 6.1 Pin Configuration**

Function	Pin Name	I/O	Descriptions	RZ/G Series Products			
				RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
IO/interrupt input ports	GP-0-0 to GP-5-31	I/O	General input/output and interrupt input	√	–	–	–
IO/interrupt input ports	GP-0-0 to GP-7-25	I/O	General input/output and interrupt input	–	√	√	–
IO/interrupt input ports	GP-0-0 to GP-6-25	I/O	General input/output and interrupt input	–	–	–	√



## 6.2 Port Pin Specifications

Each GPIO block is provided with up to 32 port pins for general input/output and external interrupt input ports. Table 6.2 specifies these pins.

**Table 6.2 Port Pin Specifications (1)**

**RZ/G1H**

Block	Number	Abbreviation	Name	Descriptions
GPIO-0  Applicable registers: IOINTSEL0 INOUTSEL0 OUTDT0 INDT0 INTDT0 INTCLR0 INTMSK0 MSKCLR0 POSNEG0 EDGLEVELO FILONOFF0 INTMSKS0 MSKCLRS0 OUTDTSEL0 OUTDTH0 OUTDTL0 BOTHEDGE0	1	GP-0-0	IO/interrupt input port A0	<ul style="list-style-type: none"> <li>• Either general input/output mode or interrupt input mode can be set for each port.</li> <li>• In general input mode, the polarity of input signals can be set for each port.</li> <li>• In general output mode, the polarity of output signals can be set for each port.</li> <li>• In interrupt input mode, the polarity of interrupt signal can be set for each port.</li> <li>• In interrupt input mode, the detection conditions of interrupt signals can be set for each port.</li> </ul>
	2	GP-0-1	IO/interrupt input port A1	
	3	GP-0-2	IO/interrupt input port A2	
	4	GP-0-3	IO/interrupt input port A3	
	5	GP-0-4	IO/interrupt input port A4	
	6	GP-0-5	IO/interrupt input port A5	
	7	GP-0-6	IO/interrupt input port A6	
	8	GP-0-7	IO/interrupt input port A7	
	9	GP-0-8	IO/interrupt input port A8	
	10	GP-0-9	IO/interrupt input port A9	
	11	GP-0-10	IO/interrupt input port A10	
	12	GP-0-11	IO/interrupt input port A11	
	13	GP-0-12	IO/interrupt input port A12	
	14	GP-0-13	IO/interrupt input port A13	
	15	GP-0-14	IO/interrupt input port A14	
	16	GP-0-15	IO/interrupt input port A15	
	17	GP-0-16	IO/interrupt input port A16	
	18	GP-0-17	IO/interrupt input port A17	
	19	GP-0-18	IO/interrupt input port A18	
	20	GP-0-19	IO/interrupt input port A19	
	21	GP-0-20	IO/interrupt input port A20	
	22	GP-0-21	IO/interrupt input port A21	
	23	GP-0-22	IO/interrupt input port A22	
	24	GP-0-23	IO/interrupt input port A23	
	25	GP-0-24	IO/interrupt input port A24	
	26	GP-0-25	IO/interrupt input port A25	
	27	GP-0-26	IO/interrupt input port A26	
	28	GP-0-27	IO/interrupt input port A27	
	29	GP-0-28	IO/interrupt input port A28	
	30	GP-0-29	IO/interrupt input port A29	
	31	GP-0-30	IO/interrupt input port A30	
	32	GP-0-31	IO/interrupt input port A31	

Block	Number	Abbreviation	Name	Descriptions	
GPIO-1	33	GP-1-0	IO/interrupt input port B0		
	34	GP-1-1	IO/interrupt input port B1		
Applicable registers:	35	GP-1-2	IO/interrupt input port B2		
	36	GP-1-3	IO/interrupt input port B3		
	IOINTSEL1	37	GP-1-4	IO/interrupt input port B4	
	INOUTSEL1	38	GP-1-5	IO/interrupt input port B5	
	OUTDT1	39	GP-1-6	IO/interrupt input port B6	
	INDT1	40	GP-1-7	IO/interrupt input port B7	
	INTDT1	41	GP-1-8	IO/interrupt input port B8	
	INTCLR1	42	GP-1-9	IO/interrupt input port B9	
	INTMSK1	43	GP-1-10	IO/interrupt input port B10	
	MSKCLR1	44	GP-1-11	IO/interrupt input port B11	
	POSNEG1	45	GP-1-12	IO/interrupt input port B12	
	EDGLEVEL1	46	GP-1-13	IO/interrupt input port B13	
	FILONOFF1	47	GP-1-14	IO/interrupt input port B14	
	INTMSKS1	48	GP-1-15	IO/interrupt input port B15	
	MSKCLRS1	49	GP-1-16	IO/interrupt input port B16	
	OUTDTSEL1	50	GP-1-17	IO/interrupt input port B17	
	OUTDTH1	51	GP-1-18	IO/interrupt input port B18	
	OUTDTL1	52	GP-1-19	IO/interrupt input port B19	
	BOTHEDGE1	53	GP-1-20	IO/interrupt input port B20	
		54	GP-1-21	IO/interrupt input port B21	
		55	GP-1-22	IO/interrupt input port B22	
		56	GP-1-23	IO/interrupt input port B23	
		57	GP-1-24	IO/interrupt input port B24	
		58	GP-1-25	IO/interrupt input port B25	
		59	GP-1-26	IO/interrupt input port B26	
		60	GP-1-27	IO/interrupt input port B27	
		61	GP-1-28	IO/interrupt input port B28	
		62	GP-1-29	IO/interrupt input port B29	
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Block	Number	Abbreviation	Name	Descriptions
GPIO-2  Applicable registers: IOINTSEL2 INOUTSEL2 OUTDT2 INDT2 INTDT2 INTCLR2 INTMSK2 MSKCLR2 POSNEG2 EDGLEVEL2 FILONOFF2 INTMSKS2 MSKCLRS2 OUTDTSEL2 OUTDTH2 OUTDTL2 BOTHEDGE2	63	GP-2-0	IO/interrupt input port C0	
	64	GP-2-1	IO/interrupt input port C1	
	65	GP-2-2	IO/interrupt input port C2	
	66	GP-2-3	IO/interrupt input port C3	
	67	GP-2-4	IO/interrupt input port C4	
	68	GP-2-5	IO/interrupt input port C5	
	69	GP-2-6	IO/interrupt input port C6	
	70	GP-2-7	IO/interrupt input port C7	
	71	GP-2-8	IO/interrupt input port C8	
	72	GP-2-9	IO/interrupt input port C9	
	73	GP-2-10	IO/interrupt input port C10	
	74	GP-2-11	IO/interrupt input port C11	
	75	GP-2-12	IO/interrupt input port C12	
	76	GP-2-13	IO/interrupt input port C13	
	77	GP-2-14	IO/interrupt input port C14	
	78	GP-2-15	IO/interrupt input port C15	
	79	GP-2-16	IO/interrupt input port C16	
	80	GP-2-17	IO/interrupt input port C17	
	81	GP-2-18	IO/interrupt input port C18	
	82	GP-2-19	IO/interrupt input port C19	
	83	GP-2-20	IO/interrupt input port C20	
	84	GP-2-21	IO/interrupt input port C21	
	85	GP-2-22	IO/interrupt input port C22	
	86	GP-2-23	IO/interrupt input port C23	
	87	GP-2-24	IO/interrupt input port C24	
	88	GP-2-25	IO/interrupt input port C25	
	89	GP-2-26	IO/interrupt input port C26	
	90	GP-2-27	IO/interrupt input port C27	
	91	GP-2-28	IO/interrupt input port C28	
92	GP-2-29	IO/interrupt input port C29		
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Block	Number	Abbreviation	Name	Descriptions
GPIO-3  Applicable registers: IOINTSEL3 INOUTSEL3 OUTDT3 INDT3 INTDT3 INTCLR3 INTMSK3 MSKCLR3 POSNEG3 EDGLEVEL3 FILONOFF3 INTMSK3 MSKCLRS3 OUTDTSEL3 OUTDTH3 OUTDTL3 BOTHEDGE3	93	GP-3-0	IO/interrupt input port D0	
	94	GP-3-1	IO/interrupt input port D1	
	95	GP-3-2	IO/interrupt input port D2	
	96	GP-3-3	IO/interrupt input port D3	
	97	GP-3-4	IO/interrupt input port D4	
	98	GP-3-5	IO/interrupt input port D5	
	99	GP-3-6	IO/interrupt input port D6	
	100	GP-3-7	IO/interrupt input port D7	
	101	GP-3-8	IO/interrupt input port D8	
	102	GP-3-9	IO/interrupt input port D9	
	103	GP-3-10	IO/interrupt input port D10	
	104	GP-3-11	IO/interrupt input port D11	
	105	GP-3-12	IO/interrupt input port D12	
	106	GP-3-13	IO/interrupt input port D13	
	107	GP-3-14	IO/interrupt input port D14	
	108	GP-3-15	IO/interrupt input port D15	
	109	GP-3-16	IO/interrupt input port D16	
	110	GP-3-17	IO/interrupt input port D17	
	111	GP-3-18	IO/interrupt input port D18	
	112	GP-3-19	IO/interrupt input port D19	
	113	GP-3-20	IO/interrupt input port D20	
	114	GP-3-21	IO/interrupt input port D21	
	115	GP-3-22	IO/interrupt input port D22	
	116	GP-3-23	IO/interrupt input port D23	
	117	GP-3-24	IO/interrupt input port D24	
	118	GP-3-25	IO/interrupt input port D25	
	119	GP-3-26	IO/interrupt input port D26	
	120	GP-3-27	IO/interrupt input port D27	
	121	GP-3-28	IO/interrupt input port D28	
	122	GP-3-29	IO/interrupt input port D29	
	123	GP-3-30	IO/interrupt input port D30	
124	GP-3-31	IO/interrupt input port D31		

Block	Number	Abbreviation	Name	Descriptions
GPIO-4  Applicable registers: IOINTSEL4 INOUTSEL4 OUTDT4 INDT4 INTDT4 INTCLR4 INTMSK4 MSKCLR4 POSNEG4 EDGLEVEL4 FILONOFF4 INTMSKS4 MSKCLRS4 OUTDTSEL4 OUTDTH4 OUTDTL4 BOTHEDGE4	125	GP-4-0	IO/interrupt input port E0	
	126	GP-4-1	IO/interrupt input port E1	
	127	GP-4-2	IO/interrupt input port E2	
	128	GP-4-3	IO/interrupt input port E3	
	129	GP-4-4	IO/interrupt input port E4	
	130	GP-4-5	IO/interrupt input port E5	
	131	GP-4-6	IO/interrupt input port E6	
	132	GP-4-7	IO/interrupt input port E7	
	133	GP-4-8	IO/interrupt input port E8	
	134	GP-4-9	IO/interrupt input port E9	
	135	GP-4-10	IO/interrupt input port E10	
	136	GP-4-11	IO/interrupt input port E11	
	137	GP-4-12	IO/interrupt input port E12	
	138	GP-4-13	IO/interrupt input port E13	
	139	GP-4-14	IO/interrupt input port E14	
	140	GP-4-15	IO/interrupt input port E15	
	141	GP-4-16	IO/interrupt input port E16	
	142	GP-4-17	IO/interrupt input port E17	
	143	GP-4-18	IO/interrupt input port E18	
	144	GP-4-19	IO/interrupt input port E19	
	145	GP-4-20	IO/interrupt input port E20	
	146	GP-4-21	IO/interrupt input port E21	
	147	GP-4-22	IO/interrupt input port E22	
	148	GP-4-23	IO/interrupt input port E23	
	149	GP-4-24	IO/interrupt input port E24	
	150	GP-4-25	IO/interrupt input port E25	
	151	GP-4-26	IO/interrupt input port E26	
	152	GP-4-27	IO/interrupt input port E27	
	153	GP-4-28	IO/interrupt input port E28	
	154	GP-4-29	IO/interrupt input port E29	
	155	GP-4-30	IO/interrupt input port E30	
156	GP-4-31	IO/interrupt input port E31		

Block	Number	Abbreviation	Name	Descriptions
GPIO-5	157	GP-5-0	IO/interrupt input port F0	
	158	GP-5-1	IO/interrupt input port F1	
Applicable registers:	159	GP-5-2	IO/interrupt input port F2	
	160	GP-5-3	IO/interrupt input port F3	
IOINTSEL5	161	GP-5-4	IO/interrupt input port F4	
INOUTSEL5	162	GP-5-5	IO/interrupt input port F5	
OUTDT5	163	GP-5-6	IO/interrupt input port F6	
INDT5	164	GP-5-7	IO/interrupt input port F7	
INTDT5	165	GP-5-8	IO/interrupt input port F8	
INTCLR5	166	GP-5-9	IO/interrupt input port F9	
INTMSK5	167	GP-5-10	IO/interrupt input port F10	
MSKCLR5	168	GP-5-11	IO/interrupt input port F11	
POSNEG5	169	GP-5-12	IO/interrupt input port F12	
EDGLEVEL5	170	GP-5-13	IO/interrupt input port F13	
FILONOFF5	171	GP-5-14	IO/interrupt input port F14	
INTMSKS5	172	GP-5-15	IO/interrupt input port F15	
MSKCLRS5	173	GP-5-16	IO/interrupt input port F16	
OUTDTSEL5	174	GP-5-17	IO/interrupt input port F17	
OUTDTH5	175	GP-5-18	IO/interrupt input port F18	
OUTDTL5	176	GP-5-19	IO/interrupt input port F19	
BOTHEDGE5	177	GP-5-20	IO/interrupt input port F20	
	178	GP-5-21	IO/interrupt input port F21	
	179	GP-5-22	IO/interrupt input port F22	
	180	GP-5-23	IO/interrupt input port F23	
	181	GP-5-24	IO/interrupt input port F24	
	182	GP-5-25	IO/interrupt input port F25	
	183	GP-5-26	IO/interrupt input port F26	
	184	GP-5-27	IO/interrupt input port F27	
	185	GP-5-28	IO/interrupt input port F28	
	186	GP-5-29	IO/interrupt input port F29	
	187	GP-5-30	IO/interrupt input port F30	
	188	GP-5-31	IO/interrupt input port F31	

Note: "—" indicates the port pin is not in use.

Table 6.2 Port Pin Specifications (2)

RZ/G1M

RZ/G1N

Block	Number	Abbreviation	Name	Descriptions
GPIO-0  Applicable registers: IOINTSEL0 INOUTSEL0 OUTDT0 INDT0 INTDT0 INTCLR0 INTMSK0 MSKCLR0 POSNEG0 EDGLEVELO FILONOFF0 INTMSKS0 MSKCLRS0 OUTDTSEL0 OUTDTH0 OUTDTL0 BOTHEDGE0	1	GP-0-0	IO/interrupt input port A0	<ul style="list-style-type: none"> <li>• Either general input/output mode or interrupt input mode can be set for each port.</li> <li>• In general input mode, the polarity of input signals can be set for each port.</li> <li>• In general output mode, the polarity of output signals can be set for each port.</li> <li>• In interrupt input mode, the polarity of interrupt signal can be set for each port.</li> <li>• In interrupt input mode, the detection conditions of interrupt signals can be set for each port.</li> </ul>
	2	GP-0-1	IO/interrupt input port A1	
	3	GP-0-2	IO/interrupt input port A2	
	4	GP-0-3	IO/interrupt input port A3	
	5	GP-0-4	IO/interrupt input port A4	
	6	GP-0-5	IO/interrupt input port A5	
	7	GP-0-6	IO/interrupt input port A6	
	8	GP-0-7	IO/interrupt input port A7	
	9	GP-0-8	IO/interrupt input port A8	
	10	GP-0-9	IO/interrupt input port A9	
	11	GP-0-10	IO/interrupt input port A10	
	12	GP-0-11	IO/interrupt input port A11	
	13	GP-0-12	IO/interrupt input port A12	
	14	GP-0-13	IO/interrupt input port A13	
	15	GP-0-14	IO/interrupt input port A14	
	16	GP-0-15	IO/interrupt input port A15	
	17	GP-0-16	IO/interrupt input port A16	
	18	GP-0-17	IO/interrupt input port A17	
	19	GP-0-18	IO/interrupt input port A18	
	20	GP-0-19	IO/interrupt input port A19	
	21	GP-0-20	IO/interrupt input port A20	
	22	GP-0-21	IO/interrupt input port A21	
	23	GP-0-22	IO/interrupt input port A22	
	24	GP-0-23	IO/interrupt input port A23	
	25	GP-0-24	IO/interrupt input port A24	
	26	GP-0-25	IO/interrupt input port A25	
	27	GP-0-26	IO/interrupt input port A26	
	28	GP-0-27	IO/interrupt input port A27	
	29	GP-0-28	IO/interrupt input port A28	
	30	GP-0-29	IO/interrupt input port A29	
	31	GP-0-30	IO/interrupt input port A30	
	32	GP-0-31	IO/interrupt input port A31	

Block	Number	Abbreviation	Name	Descriptions
GPIO-1	33	GP-1-0	IO/interrupt input port B0	
	34	GP-1-1	IO/interrupt input port B1	
Applicable registers:	35	GP-1-2	IO/interrupt input port B2	
	36	GP-1-3	IO/interrupt input port B3	
IOINTSEL1	37	GP-1-4	IO/interrupt input port B4	
INOUTSEL1	38	GP-1-5	IO/interrupt input port B5	
OUTDT1	39	GP-1-6	IO/interrupt input port B6	
INDT1	40	GP-1-7	IO/interrupt input port B7	
INTDT1	41	GP-1-8	IO/interrupt input port B8	
INTCLR1	42	GP-1-9	IO/interrupt input port B9	
INTMSK1	43	GP-1-10	IO/interrupt input port B10	
MSKCLR1	44	GP-1-11	IO/interrupt input port B11	
POSNEG1	45	GP-1-12	IO/interrupt input port B12	
EDGLEVEL1	46	GP-1-13	IO/interrupt input port B13	
FILONOFF1	47	GP-1-14	IO/interrupt input port B14	
INTMSKS1	48	GP-1-15	IO/interrupt input port B15	
MSKCLRS1	49	GP-1-16	IO/interrupt input port B16	
OUTDTSEL1	50	GP-1-17	IO/interrupt input port B17	
OUTDTH1	51	GP-1-18	IO/interrupt input port B18	
BOTHEDGE1	52	GP-1-19	IO/interrupt input port B19	
	53	GP-1-20	IO/interrupt input port B20	
	54	GP-1-21	IO/interrupt input port B21	
	55	GP-1-22	IO/interrupt input port B22	
	56	GP-1-23	IO/interrupt input port B23	
	57	GP-1-24	IO/interrupt input port B24	
	58	GP-1-25	IO/interrupt input port B25	
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Block	Number	Abbreviation	Name	Descriptions
GPIO-2	59	GP-2-0	IO/interrupt input port C0	
	60	GP-2-1	IO/interrupt input port C1	
Applicable registers:	61	GP-2-2	IO/interrupt input port C2	
	62	GP-2-3	IO/interrupt input port C3	
IOINTSEL2	63	GP-2-4	IO/interrupt input port C4	
INOUTSEL2	64	GP-2-5	IO/interrupt input port C5	
OUTDT2	65	GP-2-6	IO/interrupt input port C6	
INDT2	66	GP-2-7	IO/interrupt input port C7	
INTDT2	67	GP-2-8	IO/interrupt input port C8	
INTCLR2	68	GP-2-9	IO/interrupt input port C9	
INTMSK2	69	GP-2-10	IO/interrupt input port C10	
MSKCLR2	70	GP-2-11	IO/interrupt input port C11	
POSNEG2	71	GP-2-12	IO/interrupt input port C12	
EDGLEVEL2	72	GP-2-13	IO/interrupt input port C13	
FILONOFF2	73	GP-2-14	IO/interrupt input port C14	
INTMSKS2	74	GP-2-15	IO/interrupt input port C15	
MSKCLRS2	75	GP-2-16	IO/interrupt input port C16	
OUTDTSEL2	76	GP-2-17	IO/interrupt input port C17	
OUTDTH2	77	GP-2-18	IO/interrupt input port C18	
OUTDTL2	78	GP-2-19	IO/interrupt input port C19	
BOTHEDGE2	79	GP-2-20	IO/interrupt input port C20	
	80	GP-2-21	IO/interrupt input port C21	
	81	GP-2-22	IO/interrupt input port C22	
	82	GP-2-23	IO/interrupt input port C23	
	83	GP-2-24	IO/interrupt input port C24	
	84	GP-2-25	IO/interrupt input port C25	
	85	GP-2-26	IO/interrupt input port C26	
	86	GP-2-27	IO/interrupt input port C27	
	87	GP-2-28	IO/interrupt input port C28	
	88	GP-2-29	IO/interrupt input port C29	
	89	GP-2-30	IO/interrupt input port C30	
	90	GP-2-31	IO/interrupt input port C31	

Block	Number	Abbreviation	Name	Descriptions
GPIO-3	91	GP-3-0	IO/interrupt input port D0	
	92	GP-3-1	IO/interrupt input port D1	
Applicable registers:	93	GP-3-2	IO/interrupt input port D2	
	94	GP-3-3	IO/interrupt input port D3	
IOINTSEL3	95	GP-3-4	IO/interrupt input port D4	
INOUTSEL3	96	GP-3-5	IO/interrupt input port D5	
OUTDT3	97	GP-3-6	IO/interrupt input port D6	
INDT3	98	GP-3-7	IO/interrupt input port D7	
INTDT3	99	GP-3-8	IO/interrupt input port D8	
INTCLR3	100	GP-3-9	IO/interrupt input port D9	
INTMSK3	101	GP-3-10	IO/interrupt input port D10	
MSKCLR3	102	GP-3-11	IO/interrupt input port D11	
POSNEG3	103	GP-3-12	IO/interrupt input port D12	
EDGLEVEL3	104	GP-3-13	IO/interrupt input port D13	
FILONOFF3	105	GP-3-14	IO/interrupt input port D14	
INTMSKS3	106	GP-3-15	IO/interrupt input port D15	
MSKCLRS3	107	GP-3-16	IO/interrupt input port D16	
OUTDTSEL3	108	GP-3-17	IO/interrupt input port D17	
OUTDTH3	109	GP-3-18	IO/interrupt input port D18	
OUTDTL3	110	GP-3-19	IO/interrupt input port D19	
BOTHEDGE3	111	GP-3-20	IO/interrupt input port D20	
	112	GP-3-21	IO/interrupt input port D21	
	113	GP-3-22	IO/interrupt input port D22	
	114	GP-3-23	IO/interrupt input port D23	
	115	GP-3-24	IO/interrupt input port D24	
	116	GP-3-25	IO/interrupt input port D25	
	117	GP-3-26	IO/interrupt input port D26	
	118	GP-3-27	IO/interrupt input port D27	
	119	GP-3-28	IO/interrupt input port D28	
	120	GP-3-29	IO/interrupt input port D29	
	121	GP-3-30	IO/interrupt input port D30	
	122	GP-3-31	IO/interrupt input port D31	

Block	Number	Abbreviation	Name	Descriptions
GPIO-4	123	GP-4-0	IO/interrupt input port E0	
	124	GP-4-1	IO/interrupt input port E1	
Applicable registers:	125	GP-4-2	IO/interrupt input port E2	
	126	GP-4-3	IO/interrupt input port E3	
IOINTSEL4	127	GP-4-4	IO/interrupt input port E4	
INOUTSEL4	128	GP-4-5	IO/interrupt input port E5	
OUTDT4	129	GP-4-6	IO/interrupt input port E6	
INDT4	130	GP-4-7	IO/interrupt input port E7	
INTDT4	131	GP-4-8	IO/interrupt input port E8	
INTCLR4	132	GP-4-9	IO/interrupt input port E9	
INTMSK4	133	GP-4-10	IO/interrupt input port E10	
MSKCLR4	134	GP-4-11	IO/interrupt input port E11	
POSNEG4	135	GP-4-12	IO/interrupt input port E12	
EDGLEVEL4	136	GP-4-13	IO/interrupt input port E13	
FILONOFF4	137	GP-4-14	IO/interrupt input port E14	
INTMSKS4	138	GP-4-15	IO/interrupt input port E15	
MSKCLRS4	139	GP-4-16	IO/interrupt input port E16	
OUTDTSEL4	140	GP-4-17	IO/interrupt input port E17	
OUTDTH4	141	GP-4-18	IO/interrupt input port E18	
BOTHEDGE4	142	GP-4-19	IO/interrupt input port E19	
	143	GP-4-20	IO/interrupt input port E20	
	144	GP-4-21	IO/interrupt input port E21	
	145	GP-4-22	IO/interrupt input port E22	
	146	GP-4-23	IO/interrupt input port E23	
	147	GP-4-24	IO/interrupt input port E24	
	148	GP-4-25	IO/interrupt input port E25	
	149	GP-4-26	IO/interrupt input port E26	
	150	GP-4-27	IO/interrupt input port E27	
	151	GP-4-28	IO/interrupt input port E28	
	152	GP-4-29	IO/interrupt input port E29	
	153	GP-4-30	IO/interrupt input port E30	
	154	GP-4-31	IO/interrupt input port E31	

Block	Number	Abbreviation	Name	Descriptions
GPIO-5	155	GP-5-0	IO/interrupt input port F0	
	156	GP-5-1	IO/interrupt input port F1	
Applicable registers:	157	GP-5-2	IO/interrupt input port F2	
	158	GP-5-3	IO/interrupt input port F3	
IOINTSEL5	159	GP-5-4	IO/interrupt input port F4	
INOUTSEL5	160	GP-5-5	IO/interrupt input port F5	
OUTDT5	161	GP-5-6	IO/interrupt input port F6	
INDT5	162	GP-5-7	IO/interrupt input port F7	
INTDT5	163	GP-5-8	IO/interrupt input port F8	
INTCLR5	164	GP-5-9	IO/interrupt input port F9	
INTMSK5	165	GP-5-10	IO/interrupt input port F10	
MSKCLR5	166	GP-5-11	IO/interrupt input port F11	
POSNEG5	167	GP-5-12	IO/interrupt input port F12	
EDGLEVEL5	168	GP-5-13	IO/interrupt input port F13	
FILONOFF5	169	GP-5-14	IO/interrupt input port F14	
INTMSKS5	170	GP-5-15	IO/interrupt input port F15	
MSKCLRS5	171	GP-5-16	IO/interrupt input port F16	
OUTDTSEL5	172	GP-5-17	IO/interrupt input port F17	
OUTDTH5	173	GP-5-18	IO/interrupt input port F18	
BOTHEDGE5	174	GP-5-19	IO/interrupt input port F19	
	175	GP-5-20	IO/interrupt input port F20	
	176	GP-5-21	IO/interrupt input port F21	
	177	GP-5-22	IO/interrupt input port F22	
	178	GP-5-23	IO/interrupt input port F23	
	179	GP-5-24	IO/interrupt input port F24	
	180	GP-5-25	IO/interrupt input port F25	
	181	GP-5-26	IO/interrupt input port F26	
	182	GP-5-27	IO/interrupt input port F27	
	183	GP-5-28	IO/interrupt input port F28	
	184	GP-5-29	IO/interrupt input port F29	
	185	GP-5-30	IO/interrupt input port F30	
	186	GP-5-31	IO/interrupt input port F31	

Block	Number	Abbreviation	Name	Descriptions
GPIO-6	187	GP-6-0	IO/interrupt input port G0	
	188	GP-6-1	IO/interrupt input port G1	
Applicable registers:	189	GP-6-2	IO/interrupt input port G2	
	190	GP-6-3	IO/interrupt input port G3	
IOINTSEL6	191	GP-6-4	IO/interrupt input port G4	
INOUTSEL6	192	GP-6-5	IO/interrupt input port G5	
OUTDT6	193	GP-6-6	IO/interrupt input port G6	
INDT6	194	GP-6-7	IO/interrupt input port G7	
INTDT6	195	GP-6-8	IO/interrupt input port G8	
INTCLR6	196	GP-6-9	IO/interrupt input port G9	
INTMSK6	197	GP-6-10	IO/interrupt input port G10	
MSKCLR6	198	GP-6-11	IO/interrupt input port G11	
POSNEG6	199	GP-6-12	IO/interrupt input port G12	
EDGLEVEL6	200	GP-6-13	IO/interrupt input port G13	
FILONOFF6	201	GP-6-14	IO/interrupt input port G14	
INTMSKS6	202	GP-6-15	IO/interrupt input port G15	
MSKCLRS6	203	GP-6-16	IO/interrupt input port G16	
OUTDTSEL6	204	GP-6-17	IO/interrupt input port G17	
OUTDTH6	205	GP-6-18	IO/interrupt input port G18	
BOTHEDGE6	206	GP-6-19	IO/interrupt input port G19	
	207	GP-6-20	IO/interrupt input port G20	
	208	GP-6-21	IO/interrupt input port G21	
	209	GP-6-22	IO/interrupt input port G22	
	210	GP-6-23	IO/interrupt input port G23	
	211	GP-6-24	IO/interrupt input port G24	
	212	GP-6-25	IO/interrupt input port G25	
	213	GP-6-26	IO/interrupt input port G26	
	214	GP-6-27	IO/interrupt input port G27	
	215	GP-6-28	IO/interrupt input port G28	
	216	GP-6-29	IO/interrupt input port G29	
	217	GP-6-30	IO/interrupt input port G30	
	218	GP-6-31	IO/interrupt input port G31	

Block	Number	Abbreviation	Name	Descriptions
GPIO-7	219	GP-7-0	IO/interrupt input port H0	
	220	GP-7-1	IO/interrupt input port H1	
Applicable registers:	221	GP-7-2	IO/interrupt input port H2	
	222	GP-7-3	IO/interrupt input port H3	
IOINTSEL7	223	GP-7-4	IO/interrupt input port H4	
INOUTSEL7	224	GP-7-5	IO/interrupt input port H5	
OUTDT7	225	GP-7-6	IO/interrupt input port H6	
INDT7	226	GP-7-7	IO/interrupt input port H7	
INTDT7	227	GP-7-8	IO/interrupt input port H8	
INTCLR7	228	GP-7-9	IO/interrupt input port H9	
INTMSK7	229	GP-7-10	IO/interrupt input port H10	
MSKCLR7	230	GP-7-11	IO/interrupt input port H11	
POSNEG7	231	GP-7-12	IO/interrupt input port H12	
EDGLEVEL7	232	GP-7-13	IO/interrupt input port H13	
FILONOFF7	233	GP-7-14	IO/interrupt input port H14	
INTMSKS7	234	GP-7-15	IO/interrupt input port H15	
MSKCLRS7	235	GP-7-16	IO/interrupt input port H16	
OUTDTSEL7	236	GP-7-17	IO/interrupt input port H17	
OUTDTH7	237	GP-7-18	IO/interrupt input port H18	
BOTHEDGE7	238	GP-7-19	IO/interrupt input port H19	
	239	GP-7-20	IO/interrupt input port H20	
	240	GP-7-21	IO/interrupt input port H21	
	241	GP-7-22	IO/interrupt input port H22	
	242	GP-7-23	IO/interrupt input port H23	
	243	GP-7-24	IO/interrupt input port H24	
	244	GP-7-25	IO/interrupt input port H25	
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Note: "—" indicates the port pin is not in use.

**Table 6.2 Port Pin Specifications (3)****RZ/G1E**

Block	Number	Abbreviation	Name	Descriptions
GPIO-0  Applicable registers: IOINTSEL0 INOUTSEL0 OUTDT0 INDT0 INTDT0 INTCLR0 INTMSK0 MSKCLR0 POSNEG0 EDGLEVELO FILONOFF0 INTMSKS0 MSKCLRS0 OUTDTSEL0 OUTDTH0 OUTDTL0 BOTHEDGE0	1	GP-0-0	IO/interrupt input port A0	<ul style="list-style-type: none"> <li>• Either general input/output mode or interrupt input mode can be set for each port.</li> <li>• In general input mode, the polarity of input signals can be set for each port.</li> <li>• In general output mode, the polarity of output signals can be set for each port.</li> <li>• In interrupt input mode, the polarity of interrupt signal can be set for each port.</li> <li>• In interrupt input mode, the detection conditions of interrupt signals can be set for each port.</li> </ul>
	2	GP-0-1	IO/interrupt input port A1	
	3	GP-0-2	IO/interrupt input port A2	
	4	GP-0-3	IO/interrupt input port A3	
	5	GP-0-4	IO/interrupt input port A4	
	6	GP-0-5	IO/interrupt input port A5	
	7	GP-0-6	IO/interrupt input port A6	
	8	GP-0-7	IO/interrupt input port A7	
	9	GP-0-8	IO/interrupt input port A8	
	10	GP-0-9	IO/interrupt input port A9	
	11	GP-0-10	IO/interrupt input port A10	
	12	GP-0-11	IO/interrupt input port A11	
	13	GP-0-12	IO/interrupt input port A12	
	14	GP-0-13	IO/interrupt input port A13	
	15	GP-0-14	IO/interrupt input port A14	
	16	GP-0-15	IO/interrupt input port A15	
	17	GP-0-16	IO/interrupt input port A16	
	18	GP-0-17	IO/interrupt input port A17	
	19	GP-0-18	IO/interrupt input port A18	
	20	GP-0-19	IO/interrupt input port A19	
	21	GP-0-20	IO/interrupt input port A20	
	22	GP-0-21	IO/interrupt input port A21	
	23	GP-0-22	IO/interrupt input port A22	
	24	GP-0-23	IO/interrupt input port A23	
	25	GP-0-24	IO/interrupt input port A24	
	26	GP-0-25	IO/interrupt input port A25	
	27	GP-0-26	IO/interrupt input port A26	
	28	GP-0-27	IO/interrupt input port A27	
	29	GP-0-28	IO/interrupt input port A28	
	30	GP-0-29	IO/interrupt input port A29	
	31	GP-0-30	IO/interrupt input port A30	
	32	GP-0-31	IO/interrupt input port A31	

Block	Number	Abbreviation	Name	Descriptions
GPIO-1	33	GP-1-0	IO/interrupt input port B0	
	34	GP-1-1	IO/interrupt input port B1	
Applicable registers:	35	GP-1-2	IO/interrupt input port B2	
	36	GP-1-3	IO/interrupt input port B3	
IOINTSEL1	37	GP-1-4	IO/interrupt input port B4	
INOUTSEL1	38	GP-1-5	IO/interrupt input port B5	
OUTDT1	39	GP-1-6	IO/interrupt input port B6	
INDT1	40	GP-1-7	IO/interrupt input port B7	
INTDT1	41	GP-1-8	IO/interrupt input port B8	
INTCLR1	42	GP-1-9	IO/interrupt input port B9	
INTMSK1	43	GP-1-10	IO/interrupt input port B10	
MSKCLR1	44	GP-1-11	IO/interrupt input port B11	
POSNEG1	45	GP-1-12	IO/interrupt input port B12	
EDGLEVEL1	46	GP-1-13	IO/interrupt input port B13	
FILONOFF1	47	GP-1-14	IO/interrupt input port B14	
INTMSKS1	48	GP-1-15	IO/interrupt input port B15	
MSKCLRS1	49	GP-1-16	IO/interrupt input port B16	
OUTDTSEL1	50	GP-1-17	IO/interrupt input port B17	
OUTDTH1	51	GP-1-18	IO/interrupt input port B18	
BOTHEDGE1	52	GP-1-19	IO/interrupt input port B19	
	53	GP-1-20	IO/interrupt input port B20	
	54	GP-1-21	IO/interrupt input port B21	
	55	GP-1-22	IO/interrupt input port B22	
	56	GP-1-23	IO/interrupt input port B23	
	57	GP-1-24	IO/interrupt input port B24	
	58	GP-1-25	IO/interrupt input port B25	
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Block	Number	Abbreviation	Name	Descriptions	
GPIO-2	59	GP-2-0	IO/interrupt input port C0		
	60	GP-2-1	IO/interrupt input port C1		
Applicable registers:	61	GP-2-2	IO/interrupt input port C2		
	62	GP-2-3	IO/interrupt input port C3		
	IOINTSEL2	63	GP-2-4	IO/interrupt input port C4	
	INOUTSEL2	64	GP-2-5	IO/interrupt input port C5	
	OUTDT2	65	GP-2-6	IO/interrupt input port C6	
	INDT2	66	GP-2-7	IO/interrupt input port C7	
	INTDT2	67	GP-2-8	IO/interrupt input port C8	
	INTCLR2	68	GP-2-9	IO/interrupt input port C9	
	INTMSK2	69	GP-2-10	IO/interrupt input port C10	
	MSKCLR2	70	GP-2-11	IO/interrupt input port C11	
	POSNEG2	71	GP-2-12	IO/interrupt input port C12	
	EDGLEVEL2	72	GP-2-13	IO/interrupt input port C13	
	FILONOFF2	73	GP-2-14	IO/interrupt input port C14	
	INTMSKS2	74	GP-2-15	IO/interrupt input port C15	
	MSKCLRS2	75	GP-2-16	IO/interrupt input port C16	
	OUTDTSEL2	76	GP-2-17	IO/interrupt input port C17	
	OUTDTH2	77	GP-2-18	IO/interrupt input port C18	
	OUTDTL2	78	GP-2-19	IO/interrupt input port C19	
	BOTHEDGE2	79	GP-2-20	IO/interrupt input port C20	
		80	GP-2-21	IO/interrupt input port C21	
		81	GP-2-22	IO/interrupt input port C22	
		82	GP-2-23	IO/interrupt input port C23	
		83	GP-2-24	IO/interrupt input port C24	
		84	GP-2-25	IO/interrupt input port C25	
		85	GP-2-26	IO/interrupt input port C26	
		86	GP-2-27	IO/interrupt input port C27	
		87	GP-2-28	IO/interrupt input port C28	
		88	GP-2-29	IO/interrupt input port C29	
		89	GP-2-30	IO/interrupt input port C30	
		90	GP-2-31	IO/interrupt input port C31	

Block	Number	Abbreviation	Name	Descriptions
GPIO-3  Applicable registers: IOINTSEL3 INOUTSEL3 OUTDT3 INDT3 INTDT3 INTCLR3 INTMSK3 MSKCLR3 POSNEG3 EDGLEVEL3 FILONOFF3 INTMSKS3 MSKCLRS3 OUTDTSEL3 OUTDTH3 OUTDTL3 BOTHEDGE3	91	GP-3-0	IO/interrupt input port D0	
	92	GP-3-1	IO/interrupt input port D1	
	93	GP-3-2	IO/interrupt input port D2	
	94	GP-3-3	IO/interrupt input port D3	
	95	GP-3-4	IO/interrupt input port D4	
	96	GP-3-5	IO/interrupt input port D5	
	97	GP-3-6	IO/interrupt input port D6	
	98	GP-3-7	IO/interrupt input port D7	
	99	GP-3-8	IO/interrupt input port D8	
	100	GP-3-9	IO/interrupt input port D9	
	101	GP-3-10	IO/interrupt input port D10	
	102	GP-3-11	IO/interrupt input port D11	
	103	GP-3-12	IO/interrupt input port D12	
	104	GP-3-13	IO/interrupt input port D13	
	105	GP-3-14	IO/interrupt input port D14	
	106	GP-3-15	IO/interrupt input port D15	
	107	GP-3-16	IO/interrupt input port D16	
	108	GP-3-17	IO/interrupt input port D17	
	109	GP-3-18	IO/interrupt input port D18	
	110	GP-3-19	IO/interrupt input port D19	
	111	GP-3-20	IO/interrupt input port D20	
	112	GP-3-21	IO/interrupt input port D21	
	113	GP-3-22	IO/interrupt input port D22	
	114	GP-3-23	IO/interrupt input port D23	
	115	GP-3-24	IO/interrupt input port D24	
	116	GP-3-25	IO/interrupt input port D25	
	117	GP-3-26	IO/interrupt input port D26	
	118	GP-3-27	IO/interrupt input port D27	
	119	GP-3-28	IO/interrupt input port D28	
	120	GP-3-29	IO/interrupt input port D29	
	121	GP-3-30	IO/interrupt input port D30	
122	GP-3-31	IO/interrupt input port D31		

Block	Number	Abbreviation	Name	Descriptions
GPIO-4  Applicable registers: IOINTSEL4 INOUTSEL4 OUTDT4 INDT4 INTDT4 INTCLR4 INTMSK4 MSKCLR4 POSNEG4 EDGLEVEL4 FILONOFF4 INTMSKS4 MSKCLRS4 OUTDTSEL4 OUTDTH4 OUTDTL4 BOTHEDGE4	123	GP-4-0	IO/interrupt input port E0	
	124	GP-4-1	IO/interrupt input port E1	
	125	GP-4-2	IO/interrupt input port E2	
	126	GP-4-3	IO/interrupt input port E3	
	127	GP-4-4	IO/interrupt input port E4	
	128	GP-4-5	IO/interrupt input port E5	
	129	GP-4-6	IO/interrupt input port E6	
	130	GP-4-7	IO/interrupt input port E7	
	131	GP-4-8	IO/interrupt input port E8	
	132	GP-4-9	IO/interrupt input port E9	
	133	GP-4-10	IO/interrupt input port E10	
	134	GP-4-11	IO/interrupt input port E11	
	135	GP-4-12	IO/interrupt input port E12	
	136	GP-4-13	IO/interrupt input port E13	
	137	GP-4-14	IO/interrupt input port E14	
	138	GP-4-15	IO/interrupt input port E15	
	139	GP-4-16	IO/interrupt input port E16	
	140	GP-4-17	IO/interrupt input port E17	
	141	GP-4-18	IO/interrupt input port E18	
	142	GP-4-19	IO/interrupt input port E19	
	143	GP-4-20	IO/interrupt input port E20	
	144	GP-4-21	IO/interrupt input port E21	
	145	GP-4-22	IO/interrupt input port E22	
	146	GP-4-23	IO/interrupt input port E23	
	147	GP-4-24	IO/interrupt input port E24	
	148	GP-4-25	IO/interrupt input port E25	
	149	GP-4-26	IO/interrupt input port E26	
	150	GP-4-27	IO/interrupt input port E27	
	151	GP-4-28	IO/interrupt input port E28	
	152	GP-4-29	IO/interrupt input port E29	
	153	GP-4-30	IO/interrupt input port E30	
154	GP-4-31	IO/interrupt input port E31		

Block	Number	Abbreviation	Name	Descriptions
GPIO-5	155	GP-5-0	IO/interrupt input port F0	
	156	GP-5-1	IO/interrupt input port F1	
Applicable registers:	157	GP-5-2	IO/interrupt input port F2	
	158	GP-5-3	IO/interrupt input port F3	
IOINTSEL5	159	GP-5-4	IO/interrupt input port F4	
INOUTSEL5	160	GP-5-5	IO/interrupt input port F5	
OUTDT5	161	GP-5-6	IO/interrupt input port F6	
INDT5	162	GP-5-7	IO/interrupt input port F7	
INTDT5	163	GP-5-8	IO/interrupt input port F8	
INTCLR5	164	GP-5-9	IO/interrupt input port F9	
INTMSK5	165	GP-5-10	IO/interrupt input port F10	
MSKCLR5	166	GP-5-11	IO/interrupt input port F11	
POSNEG5	167	GP-5-12	IO/interrupt input port F12	
EDGLEVEL5	168	GP-5-13	IO/interrupt input port F13	
FILONOFF5	169	GP-5-14	IO/interrupt input port F14	
INTMSKS5	170	GP-5-15	IO/interrupt input port F15	
MSKCLRS5	171	GP-5-16	IO/interrupt input port F16	
OUTDTSEL5	172	GP-5-17	IO/interrupt input port F17	
OUTDTH5	173	GP-5-18	IO/interrupt input port F18	
OUTDTL5	174	GP-5-19	IO/interrupt input port F19	
BOTHEDGE5	175	GP-5-20	IO/interrupt input port F20	
	176	GP-5-21	IO/interrupt input port F21	
	177	GP-5-22	IO/interrupt input port F22	
	178	GP-5-23	IO/interrupt input port F23	
	179	GP-5-24	IO/interrupt input port F24	
	180	GP-5-25	IO/interrupt input port F25	
	181	GP-5-26	IO/interrupt input port F26	
	182	GP-5-27	IO/interrupt input port F27	
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Block	Number	Abbreviation	Name	Descriptions
GPIO-6	183	GP-6-0	IO/interrupt input port G0	
	184	GP-6-1	IO/interrupt input port G1	
Applicable registers:	185	GP-6-2	IO/interrupt input port G2	
	186	GP-6-3	IO/interrupt input port G3	
IOINTSEL6	187	GP-6-4	IO/interrupt input port G4	
INOUTSEL6	188	GP-6-5	IO/interrupt input port G5	
OUTDT6	189	GP-6-6	IO/interrupt input port G6	
INDT6	190	GP-6-7	IO/interrupt input port G7	
INTDT6	191	GP-6-8	IO/interrupt input port G8	
INTCLR6	192	GP-6-9	IO/interrupt input port G9	
INTMSK6	193	GP-6-10	IO/interrupt input port G10	
MSKCLR6	194	GP-6-11	IO/interrupt input port G11	
POSNEG6	195	GP-6-12	IO/interrupt input port G12	
EDGLEVEL6	196	GP-6-13	IO/interrupt input port G13	
FILONOFF6	197	GP-6-14	IO/interrupt input port G14	
INTMSKS6	198	GP-6-15	IO/interrupt input port G15	
MSKCLRS6	199	GP-6-16	IO/interrupt input port G16	
OUTDTSEL6	200	GP-6-17	IO/interrupt input port G17	
OUTDTH6	201	GP-6-18	IO/interrupt input port G18	
OUTDTL6	202	GP-6-19	IO/interrupt input port G19	
BOTHEDGE6	203	GP-6-20	IO/interrupt input port G20	
	204	GP-6-21	IO/interrupt input port G21	
	205	GP-6-22	IO/interrupt input port G22	
	206	GP-6-23	IO/interrupt input port G23	
	207	GP-6-24	IO/interrupt input port G24	
	208	GP-6-25	IO/interrupt input port G25	
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Note: "—" indicates the port pin is not in use.

## 6.3 Operations in Each Mode

### 6.3.1 Mode Switching

Two registers are used to switch modes of the general IO/interrupt input pins of the GPIO blocks. Each register is provided with up to 32 bits each controlling one of the GPIO<sub>n</sub>\* port pins. The general IO/interrupt switching register is first used to select either general input/output mode or interrupt input mode for each port pin. When general input/output mode is selected, the setting of the relevant bit in the second register, i.e., the general input/output switching register, is used. Specifically, when a bit in the general input/output switching register is set for general output mode, the corresponding port pin is turned to the output direction and the route is formed so that the set value in the corresponding bit in the general output register should be output via the pin. Likewise, when set for the general input mode, the corresponding port pin is turned to the input direction and the route is formed so that the value received via the pin should be indicated by the corresponding bit in the general input register. When interrupt input mode is selected, the corresponding port pin is turned to the input direction and the route is formed so that the reception of the signal input via the pin should be indicated by the interrupt display register. Here, the setting of the second register, i.e., the general input/output switching register, is invalid.

Note: \* n = 0 to 5 [RZ/G1H], n = 0 to 7 [RZ/G1M and RZ/G1N], n = 0 to 6 [RZ/G1E]

### 6.3.2 General Input/Output Mode

When a port is set for general input/output mode using the corresponding bit in the general IO/interrupt switching register, the corresponding port serves as a general input/output pin. In general input/output mode, either mode can be selected using the corresponding bit in the general input/output switching register. When a port is set for general output mode, the port outputs the value set in the corresponding bit in the general output register or output data high/output data low register with appropriate configuring in output data select register. Here, the polarity of the actual output signal is determined by the setting of the corresponding bit in the positive/negative logic select register. When a port is set for general input mode, the polarity of the input signal is also determined by the setting of the corresponding bit in the positive/negative logic select register. The general input register indicates the value accordingly. Note that the general input register does not hold the input signal using the FF.

### 6.3.3 Interrupt Input Mode

When a port is set for interrupt input mode using the corresponding bit in the general IO/interrupt switching register, the corresponding port serves as an interrupt input pin. In interrupt input mode, when the port receives an external interrupt, the corresponding bit in the interrupt display register indicates the input of an interrupt signal on the corresponding port pin, and an interrupt signal is output to the interrupt control block. In this mode, the polarity and detection conditions (edge or level) of the external input signal can be set for each port. The corresponding bits in the positive/negative logic select register and edge/level select register, one edge/both edge select register should be used to set the polarity and detection conditions, respectively.

If a port is set for edge detection using the corresponding bit in the edge/level select register, even when an external pulse interrupt signal is input, the corresponding bit in the interrupt display register holds the input using the FF and allows the level interrupt signal to be output to the interrupt control block. To stop all the interrupt signal outputs, all the bits in the interrupt clear register corresponding to the bits in the interrupt display register currently indicating the reception of the corresponding interrupt signals should be cleared to 0. Note that if a port is set for level detection using the corresponding bit in the edge/level select register and an external level interrupt signal is input, the corresponding bit in the interrupt display register does not use the FF to hold the input.

Interrupts indicated by the interrupt display register can be separately masked using the corresponding bits in the interrupt mask register and the interrupt sub mask register. When all the bits currently indicating the reception of the interrupt signals are masked, no interrupt signals are output to the interrupt control block. Masks can be canceled by writing 1 to the corresponding bits in the interrupt mask clear register or the interrupt sub mask clear register depending on the interrupt mask register or the interrupt sub mask register is used.

## 6.4 Registers in GPIO Blocks

Each GPIO block incorporates seventeen 32-bit registers. These registers can be accessed via the APB interface. Table 6.3 describes all the GPIO block registers.

Do not write to any addresses other than listed below. Operations cannot be guaranteed if writing is attempted. Values read from addresses other than those listed below are undefined.

**Table 6.3 Register Configuration**

Register Name	Abbreviation	R/W	Value after Reset	Address	Access Size	RZ/G series Products			
						RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
General IO/interrupt switching register 0	IOINTSEL0	R/W	H'0000 0000	H'E6050000	32	√	√	√	√
General input/output switching register 0	INOUTSEL0	R/W	H'0000 0000	H'E6050004	32	√	√	√	√
General output register 0	OUTDT0	R/W	H'0000 0000	H'E6050008	32	√	√	√	√
General input register 0	INDT0	R	State of the port pins	H'E605000C	32	√	√	√	√
Interrupt display register 0	INTDT0	R	H'0000 0000	H'E6050010	32	√	√	√	√
Interrupt clear register 0	INTCLR0	R/W	H'0000 0000	H'E6050014	32	√	√	√	√
Interrupt mask register 0	INTMSK0	R/W	H'0000 0000	H'E6050018	32	√	√	√	√
Interrupt mask clear register 0	MSKCLR0	R/W	H'0000 0000	H'E605001C	32	√	√	√	√
Positive/negative logic select register 0	POSNEG0	R/W	H'0000 0000	H'E6050020	32	√	√	√	√
Edge/level select register 0	EDGLEVELO	R/W	H'0000 0000	H'E6050024	32	√	√	√	√
Chattering prevention on/off register 0	FILONOFF0	R/W	H'0000 0000	H'E6050028	32	√	√	√	√
Interrupt sub mask register 0	INTMSKS0	R/W	H'0000 0000	H'E6050038	32	√	√	√	√
Interrupt sub mask clear register 0	MSKCLRS0	R/W	H'0000 0000	H'E605003C	32	√	√	√	√
Output data select register 0	OUTDTSEL0	R/W	H'0000 0000	H'E6050040	32	√	√	√	√
Output data high register 0	OUTDTH0	R/W	H'0000 0000	H'E6050044	32	√	√	√	√
Output data low register 0	OUTDTL0	R/W	H'0000 0000	H'E6050048	32	√	√	√	√
One edge/both edge select register 0	BOTHEDEG0	R/W	H'0000 0000	H'E605004C	32	√	√	√	√
General IO/interrupt switching register 1	IOINTSEL1	R/W	H'0000 0000	H'E6051000	32	√	√	√	√
General input/output switching register 1	INOUTSEL1	R/W	H'0000 0000	H'E6051004	32	√	√	√	√
General output register 1	OUTDT1	R/W	H'0000 0000	H'E6051008	32	√	√	√	√
General input register 1	INDT1	R	State of the port pins	H'E605100C	32	√	√	√	√
Interrupt display register 1	INTDT1	R	H'0000 0000	H'E6051010	32	√	√	√	√
Interrupt clear register 1	INTCLR1	R/W	H'0000 0000	H'E6051014	32	√	√	√	√
Interrupt mask register 1	INTMSK1	R/W	H'0000 0000	H'E6051018	32	√	√	√	√
Interrupt mask clear register 1	MSKCLR1	R/W	H'0000 0000	H'E605101C	32	√	√	√	√
Positive/negative logic select register 1	POSNEG1	R/W	H'0000 0000	H'E6051020	32	√	√	√	√
Edge/level select register 1	EDGLEVELO1	R/W	H'0000 0000	H'E6051024	32	√	√	√	√

						RZ/G series Products			
Register Name	Abbreviation	R/W	Value after Reset	Address	Access Size	RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Chattering prevention on/off register 1	FILONOFF1	R/W	H'0000 0000	H'E6051028	32	√	√	√	√
Interrupt sub mask register 1	INTMSKS1	R/W	H'0000 0000	H'E6051038	32	√	√	√	√
Interrupt sub mask clear register 1	MSKCLRS1	R/W	H'0000 0000	H'E605103C	32	√	√	√	√
Output data select register 1	OUTDTSEL1	R/W	H'0000 0000	H'E6051040	32	√	√	√	√
Output data high register 1	OUTDTH1	R/W	H'0000 0000	H'E6051044	32	√	√	√	√
Output data low register 1	OUTDTL1	R/W	H'0000 0000	H'E6051048	32	√	√	√	√
One edge/both edge select register 1	BOTHEGE1	R/W	H'0000 0000	H'E605104C	32	√	√	√	√
General IO/interrupt switching register 2	IOINTSEL2	R/W	H'0000 0000	H'E6052000	32	√	√	√	√
General input/output switching register 2	INOUTSEL2	R/W	H'0000 0000	H'E6052004	32	√	√	√	√
General output register 2	OUTDT2	R/W	H'0000 0000	H'E6052008	32	√	√	√	√
General input register 2	INDT2	R	State of the port pins	H'E605200C	32	√	√	√	√
Interrupt display register 2	INTDT2	R	H'0000 0000	H'E6052010	32	√	√	√	√
Interrupt clear register 2	INTCLR2	R/W	H'0000 0000	H'E6052014	32	√	√	√	√
Interrupt mask register 2	INTMSK2	R/W	H'0000 0000	H'E6052018	32	√	√	√	√
Interrupt mask clear register 2	MSKCLR2	R/W	H'0000 0000	H'E605201C	32	√	√	√	√
Positive/negative logic select register 2	POSNEG2	R/W	H'0000 0000	H'E6052020	32	√	√	√	√
Edge/level select register 2	EDGLEVEL2	R/W	H'0000 0000	H'E6052024	32	√	√	√	√
Chattering prevention on/off register 2	FILONOFF2	R/W	H'0000 0000	H'E6052028	32	√	√	√	√
Interrupt sub mask register 2	INTMSKS2	R/W	H'0000 0000	H'E6052038	32	√	√	√	√
Interrupt sub mask clear register 2	MSKCLRS2	R/W	H'0000 0000	H'E605203C	32	√	√	√	√
Output data select register 2	OUTDTSEL2	R/W	H'0000 0000	H'E6052040	32	√	√	√	√
Output data high register 2	OUTDTH2	R/W	H'0000 0000	H'E6052044	32	√	√	√	√
Output data low register 2	OUTDTL2	R/W	H'0000 0000	H'E6052048	32	√	√	√	√
One edge/both edge select register 2	BOTHEGE2	R/W	H'0000 0000	H'E605204C	32	√	√	√	√
General IO/interrupt switching register 3	IOINTSEL3	R/W	H'0000 0000	H'E6053000	32	√	√	√	√
General input/output switching register 3	INOUTSEL3	R/W	H'0000 0000	H'E6053004	32	√	√	√	√
General output register 3	OUTDT3	R/W	H'0000 0000	H'E6053008	32	√	√	√	√
General input register 3	INDT3	R	State of the port pins	H'E605300C	32	√	√	√	√
Interrupt display register 3	INTDT3	R	H'0000 0000	H'E6053010	32	√	√	√	√
Interrupt clear register 3	INTCLR3	R/W	H'0000 0000	H'E6053014	32	√	√	√	√
Interrupt mask register 3	INTMSK3	R/W	H'0000 0000	H'E6053018	32	√	√	√	√
Interrupt mask clear register 3	MSKCLR3	R/W	H'0000 0000	H'E605301C	32	√	√	√	√
Positive/negative logic select register 3	POSNEG3	R/W	H'0000 0000	H'E6053020	32	√	√	√	√
Edge/level select register 3	EDGLEVEL3	R/W	H'0000 0000	H'E6053024	32	√	√	√	√



						RZ/G series Products			
Register Name	Abbreviation	R/W	Value after Reset	Address	Access Size	RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Chattering prevention on/off register 3	FILONOFF3	R/W	H'0000 0000	H'E6053028	32	√	√	√	√
Interrupt sub mask register 3	INTMSKS3	R/W	H'0000 0000	H'E6053038	32	√	√	√	√
Interrupt sub mask clear register 3	MSKCLRS3	R/W	H'0000 0000	H'E605303C	32	√	√	√	√
Output data select register 3	OUTDTSEL3	R/W	H'0000 0000	H'E6053040	32	√	√	√	√
Output data high register 3	OUTDTH3	R/W	H'0000 0000	H'E6053044	32	√	√	√	√
Output data low register 3	OUTDTL3	R/W	H'0000 0000	H'E6053048	32	√	√	√	√
One edge/both edge select register 3	BOTHEdge3	R/W	H'0000 0000	H'E605304C	32	√	√	√	√
General IO/interrupt switching register 4	IOINTSEL4	R/W	H'0000 0000	H'E6054000	32	√	√	√	√
General input/output switching register 4	INOUTSEL4	R/W	H'0000 0000	H'E6054004	32	√	√	√	√
General output register 4	OUTDT4	R/W	H'0000 0000	H'E6054008	32	√	√	√	√
General input register 4	INDT4	R	State of the port pins	H'E605400C	32	√	√	√	√
Interrupt display register 4	INTDT4	R	H'0000 0000	H'E6054010	32	√	√	√	√
Interrupt clear register 4	INTCLR4	R/W	H'0000 0000	H'E6054014	32	√	√	√	√
Interrupt mask register 4	INTMSK4	R/W	H'0000 0000	H'E6054018	32	√	√	√	√
Interrupt mask clear register 4	MSKCLR4	R/W	H'0000 0000	H'E605401C	32	√	√	√	√
Positive/negative logic select register 4	POSNEG4	R/W	H'0000 0000	H'E6054020	32	√	√	√	√
Edge/level select register 4	EDGLEVEL4	R/W	H'0000 0000	H'E6054024	32	√	√	√	√
Chattering prevention on/off register 4	FILONOFF4	R/W	H'0000 0000	H'E6054028	32	√	√	√	√
Interrupt sub mask register 4	INTMSKS4	R/W	H'0000 0000	H'E6054038	32	√	√	√	√
Interrupt sub mask clear register 4	MSKCLRS4	R/W	H'0000 0000	H'E605403C	32	√	√	√	√
Output data select register 4	OUTDTSEL4	R/W	H'0000 0000	H'E6054040	32	√	√	√	√
Output data high register 4	OUTDTH4	R/W	H'0000 0000	H'E6054044	32	√	√	√	√
Output data low register 4	OUTDTL4	R/W	H'0000 0000	H'E6054048	32	√	√	√	√
One edge/both edge select register 4	BOTHEdge4	R/W	H'0000 0000	H'E605404C	32	√	√	√	√
General IO/interrupt switching register 5	IOINTSEL5	R/W	H'0000 0000	H'E6055000	32	√	√	√	√
General input/output switching register 5	INOUTSEL5	R/W	H'0000 0000	H'E6055004	32	√	√	√	√
General output register 5	OUTDT5	R/W	H'0000 0000	H'E6055008	32	√	√	√	√
General input register 5	INDT5	R	State of the port pins	H'E605500C	32	√	√	√	√
Interrupt display register 5	INTDT5	R	H'0000 0000	H'E6055010	32	√	√	√	√
Interrupt clear register 5	INTCLR5	R/W	H'0000 0000	H'E6055014	32	√	√	√	√
Interrupt mask register 5	INTMSK5	R/W	H'0000 0000	H'E6055018	32	√	√	√	√
Interrupt mask clear register 5	MSKCLR5	R/W	H'0000 0000	H'E605501C	32	√	√	√	√
Positive/negative logic select register 5	POSNEG5	R/W	H'0000 0000	H'E6055020	32	√	√	√	√
Edge/level select register 5	EDGLEVEL5	R/W	H'0000 0000	H'E6055024	32	√	√	√	√

						RZ/G series Products			
Register Name	Abbreviation	R/W	Value after Reset	Address	Access Size	RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Chattering prevention on/off register 5	FILONOFF5	R/W	H'0000 0000	H'E6055028	32	√	√	√	√
Interrupt sub mask register 5	INTMSKS5	R/W	H'0000 0000	H'E6055038	32	√	√	√	√
Interrupt sub mask clear register 5	MSKCLRS5	R/W	H'0000 0000	H'E605503C	32	√	√	√	√
Output data select register 5	OUTDTSEL5	R/W	H'0000 0000	H'E6055040	32	√	√	√	√
Output data high register 5	OUTDTH5	R/W	H'0000 0000	H'E6055044	32	√	√	√	√
Output data low register 5	OUTDTL5	R/W	H'0000 0000	H'E6055048	32	√	√	√	√
One edge/both edge select register 5	BOTHEdge5	R/W	H'0000 0000	H'E605504C	32	√	√	√	√
General IO/interrupt switching register 6	IOINTSEL6	R/W	H'0000 0000	H'E6055400	32	—	√	√	√
General input/output switching register 6	INOUTSEL6	R/W	H'0000 0000	H'E6055404	32	—	√	√	√
General output register 6	OUTDT6	R/W	H'0000 0000	H'E6055408	32	—	√	√	√
General input register 6	INDT6	R	State of the port pins	H'E605540C	32	—	√	√	√
Interrupt display register 6	INTDT6	R	H'0000 0000	H'E6055410	32	—	√	√	√
Interrupt clear register 6	INTCLR6	R/W	H'0000 0000	H'E6055414	32	—	√	√	√
Interrupt mask register 6	INTMSK6	R/W	H'0000 0000	H'E6055418	32	—	√	√	√
Interrupt mask clear register 6	MSKCLR6	R/W	H'0000 0000	H'E605541C	32	—	√	√	√
Positive/negative logic select register 6	POSNEG6	R/W	H'0000 0000	H'E6055420	32	—	√	√	√
Edge/level select register 6	EDGELEVEL6	R/W	H'0000 0000	H'E6055424	32	—	√	√	√
Chattering prevention on/off register 6	FILONOFF6	R/W	H'0000 0000	H'E6055428	32	—	√	√	√
Interrupt sub mask register 6	INTMSKS6	R/W	H'0000 0000	H'E6055438	32	—	√	√	√
Interrupt sub mask clear register 6	MSKCLRS6	R/W	H'0000 0000	H'E605543C	32	—	√	√	√
Output data select register 6	OUTDTSEL6	R/W	H'0000 0000	H'E6055440	32	—	√	√	√
Output data high register 6	OUTDTH6	R/W	H'0000 0000	H'E6055444	32	—	√	√	√
Output data low register 6	OUTDTL6	R/W	H'0000 0000	H'E6055448	32	—	√	√	√
One edge/both edge select register 6	BOTHEdge6	R/W	H'0000 0000	H'E605544C	32	—	√	√	√
General IO/interrupt switching register 7	IOINTSEL7	R/W	H'0000 0000	H'E6055800	32	—	√	√	√
General input/output switching register 7	INOUTSEL7	R/W	H'0000 0000	H'E6055804	32	—	√	√	√
General output register 7	OUTDT7	R/W	H'0000 0000	H'E6055808	32	—	√	√	√
General input register 7	INDT7	R	State of the port pins	H'E605580C	32	—	√	√	√
Interrupt display register 7	INTDT7	R	H'0000 0000	H'E6055810	32	—	√	√	√
Interrupt clear register 7	INTCLR7	R/W	H'0000 0000	H'E6055814	32	—	√	√	√
Interrupt mask register 7	INTMSK7	R/W	H'0000 0000	H'E6055818	32	—	√	√	√
Interrupt mask clear register 7	MSKCLR7	R/W	H'0000 0000	H'E605581C	32	—	√	√	√
Positive/negative logic select register 7	POSNEG7	R/W	H'0000 0000	H'E6055820	32	—	√	√	√
Edge/level select register 7	EDGELEVEL7	R/W	H'0000 0000	H'E6055824	32	—	√	√	√

## RZ/G series Products

Register Name	Abbreviation	R/W	Value after Reset	Address	Access Size	RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Chattering prevention on/off register 7	FILONOFF7	R/W	H'0000 0000	H'E6055828	32	—	√	√	√
Interrupt sub mask register 7	INTMSKS7	R/W	H'0000 0000	H'E6055838	32	—	√	√	√
Interrupt sub mask clear register 7	MSKCLRS7	R/W	H'0000 0000	H'E605583C	32	—	√	√	√
Output data select register 7	OUTDTSEL7	R/W	H'0000 0000	H'E6055840	32	—	√	√	√
Output data high register 7	OUTDTH7	R/W	H'0000 0000	H'E6055844	32	—	√	√	√
Output data low register 7	OUTDTL7	R/W	H'0000 0000	H'E6055848	32	—	√	√	√
One edge/both edge select register 7	BOTHEDGE7	R/W	H'0000 0000	H'E605584C	32	—	√	√	√

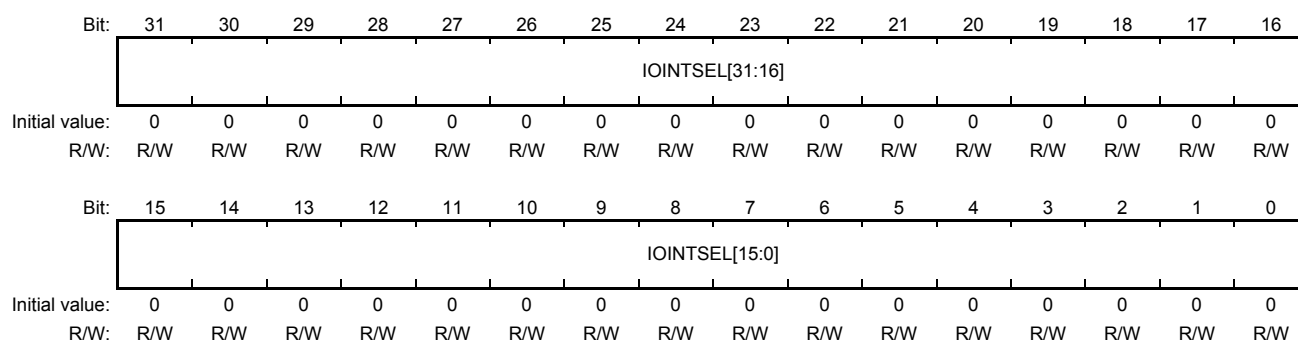
### 6.4.1 General IO/Interrupt Switching Register n (IOINTSEL0 to IOINTSELn)

Note: n = 5 [RZ/G1H], n = 7 [RZ/G1M/N], n = 6 [RZ/G1E]

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

IOINTSEL selects either general input/output mode or interrupt input mode for each of the port pins 0 to 31 of the GPIO block. When general input/output mode is selected for a port, it is also necessary to select either input or output mode for the port using the corresponding bit in the general input/output switching register. When interrupt input mode is selected for a port, the setting of the general input/output switching register for the port is ignored.

[Hardware default value: H'00000000 = general input/output mode is selected for all the ports.]



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	IOINTSEL [31:0]	All 0	R/W	Selects either general input/output mode or interrupt input mode for each port using the bits corresponding to the port numbers. 0: General input/output mode. 1: Interrupt input mode.

Note: Unused bits should be set to the initial values.

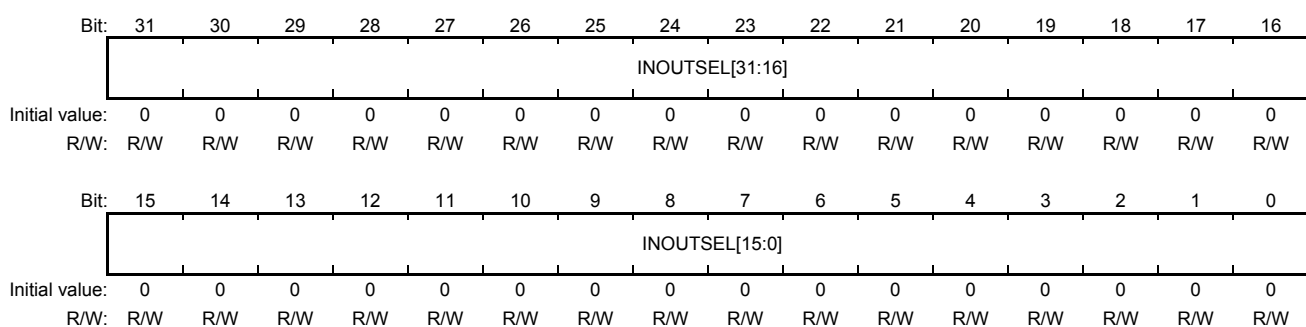
### 6.4.2 General Input/Output Switching Register n (INOUTSEL0 to INOUTSELn)

Note: n = 5 [RZ/G1H], n = 7 [RZ/G1M/N], n = 6 [RZ/G1E]

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

INOUTSEL is valid only for the ports for which general input/output mode is selected by the general IO/interrupt switching register. Specifically, INOUTSEL selects either general input or general output mode for a port using the bit corresponding to the port number. The INOUTSEL bits can be written to only when the corresponding bits in the general IO/interrupt switching register are 0. Note that after general input/output mode is changed to interrupt input mode, INOUTSEL retains the setting but is read as 0.

[Hardware default value: H'00000000 = general input mode is selected for all the ports.]



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	INOUTSEL [31:0]	All 0	R/W	Selects either general input mode or general output mode for each port using the bits corresponding to the port numbers. 0: General input mode 1: General output mode

Note: Unused bits should be set to the initial values.

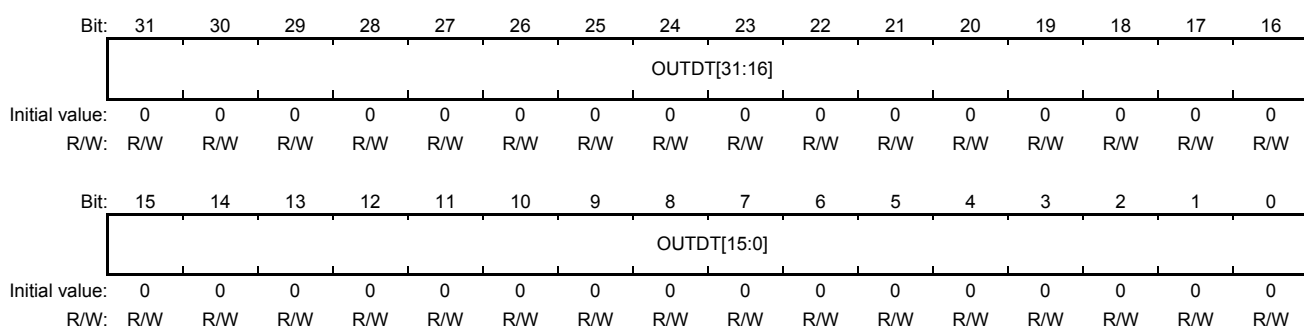
### 6.4.3 General Output Register n (OUTDT0 to OUTDTn)

Note: n = 5 [RZ/G1H], n = 7 [RZ/G1M/N], n = 6 [RZ/G1E]

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

OUTDT is valid only for the ports for which general input/output mode is selected by the general IO/interrupt switching register and then general output mode is selected by the general input/output switching register. Specifically, the value of the bit in OUTDT corresponding to the port number is inverted or not inverted depending on the setting of the positive/negative logic select register before being output from the corresponding port pin. Note that the polarity of the output signal should previously be set using the corresponding bit in the positive/negative logic select register. This register must be set after the output data select register is appropriately set to choose level of output data.

[Hardware default value: H'00000000 = 0 is output from all the ports.]



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	OUTDT[31:0]	All 0	R/W	Allows the port to output the value set in the bit corresponding to the port number when the port is appropriately set by IOINTSEL0 to IOINTSELn, INOUTSEL0 to INOUTSELn and OUTDTSEL0 to OUTDTSELn. (n = 5 [H], n = 7 [M/N], n = 6 [E]) 0: 0 is output. 1: 1 is output.

Note: The values set in OUTDT are not directly output from the GPIO pins; the above set values are processed according to the settings of the positive/negative logic select register before being output. Unused bits should be set to the initial values.

### 6.4.4 General Input Register n (INDT0 to INDTn)

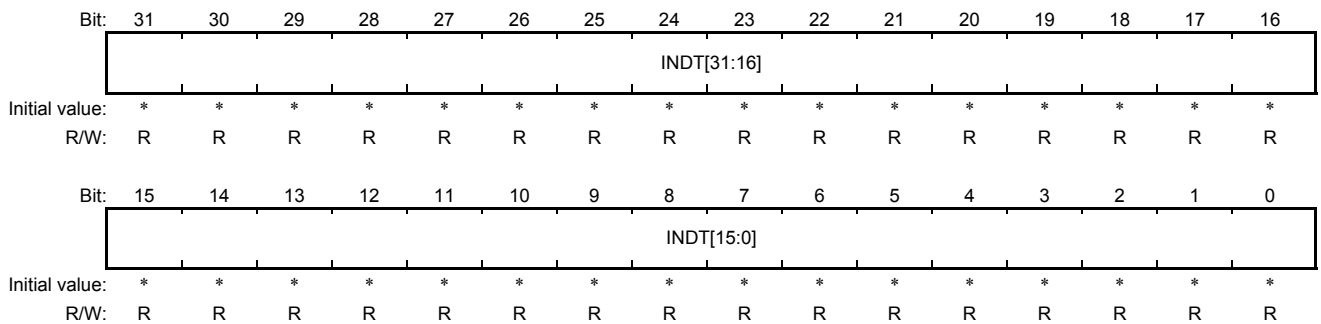
Note: n = 5 [RZ/G1H], n = 7 [RZ/G1M/N], n = 6 [RZ/G1E]

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

INDT is valid only for the ports for which general input/output mode is selected by the general IO/interrupt switching register and then general input mode is selected by the general input/output switching register. Each bit reflects the value received through the corresponding port pin.

Note that when a bit in the positive/negative logic select register is 1, the corresponding bit in INDT indicates the inverted value of the input signal.

[Hardware default value: state of the signals input to the port pins.]



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	INDT[31:0]	*	R	Each bit reflects the value received through the corresponding port pin. 0: Input is 0. (assuming positive logic) 1: Input is 1. (assuming positive logic)

Note: Unused bits should be set to the initial values.  
\* State of the signals input to the port pins.

Usage Note: The GPIO input function is still enabled even if after the pin function has been set for any modules other than the GPIO; if the module pin setting is input, the input signal is also propagated to the GPIO block and the GPIO input related registers are updated by the latest input of the corresponding pin. An unexpected GPIO interrupt may occur unless the GPIO interrupt is masked.

### 6.4.5 Interrupt Display Register n (INTDT0 to INTDTn)

Note: n = 5 [RZ/G1H], n = 7 [RZ/G1M/N], n = 6 [RZ/G1E]

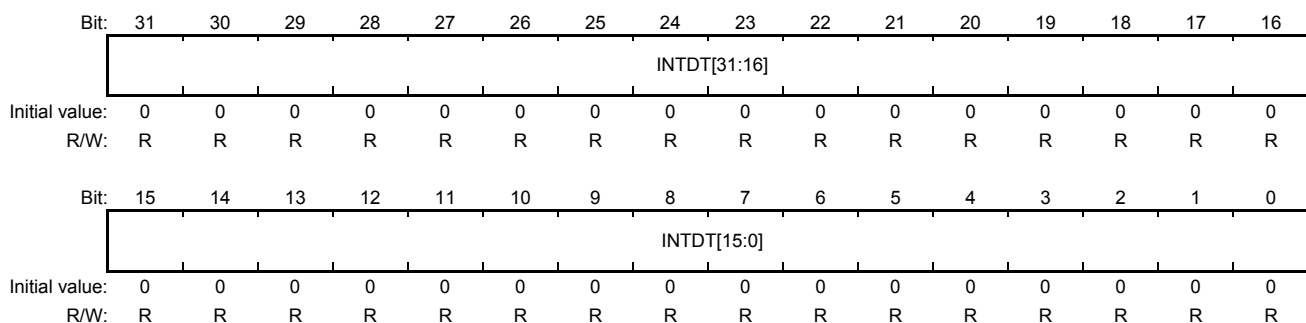
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

INTDT is valid only when interrupt input mode is selected by the general IO/interrupt switching register. Specifically, when an interrupt is input via a port pin when INTDT is valid, the bit in INTDT corresponding to the port indicates whether the port has received an interrupt input or not. In interrupt input mode, the polarity and detection conditions (one edge/both edge or level) of the external input signal can be set for each port pin. Before using a port pin for interrupt input, the corresponding bits in the positive/negative logic select register and edge/level select register (one edge/both edge register should be appropriately configured if edge detection mode is selected) should be set, respectively.

If a port is set for edge detection using the corresponding bit in the edge/level select register, even when an external pulse interrupt signal is input, the corresponding bit in INTDT holds the input using the FF and allows the level interrupt signal to be output to the interrupt control block.

To stop all the interrupt signal outputs, all the bits in the interrupt clear register corresponding to the bits in INTDT currently indicating the reception of the corresponding interrupt signals should be cleared to 0. Note that if a port is set for level detection using the corresponding bit in the edge/level select register and an external level interrupt signal is input, the corresponding bit in INTDT does not use the FF to hold the input. Therefore, when an external input signal is stopped, the corresponding bit in INTDT is cleared automatically. When all the bits in INTDT are turned off (= 0), the GPIO stops outputting all the interrupt signals.

[Hardware default value: H'00000000 = no interrupt signals are input from ports.]



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	INTDT[31:0]	All 0	R	Each bit indicates the input of an interrupt signal on the corresponding port pin. 0: No interrupt signal has been input. 1: Interrupt signal has been input.

Conditions of Indicating Interrupt Input:

- For level-sensitive interrupt input (EDGLEVEL = 0)
  - External input signals are constantly monitored and indicated. (When the negative logic is selected, the inverted value of the external input signal is indicated.)
- For edge-sensitive interrupt input (EDGLEVEL = 1)
  - Clearing condition: When the interrupt clear register is cleared, indication is cleared regardless of the positive/negative logic select register.



- Setting condition: With the positive logic (POSNEG = 0), when the rising edge of an external interrupt signal is detected, the interrupt input is indicated. With the negative logic (POSNEG = 1), when the falling edge is detected, the interrupt input is indicated. With both edge mode (BOTHEDGE = 1), when either the rising or falling edge, the interrupt input is indicated.

Usage Note: The GPIO input function is still enabled even if after the pin function has been set for any modules other than the GPIO; if the module pin setting is input, the input signal is also propagated to the GPIO block and the GPIO input related registers are updated by the latest input of the corresponding pin. An unexpected GPIO interrupt may occur unless the GPIO interrupt is masked.

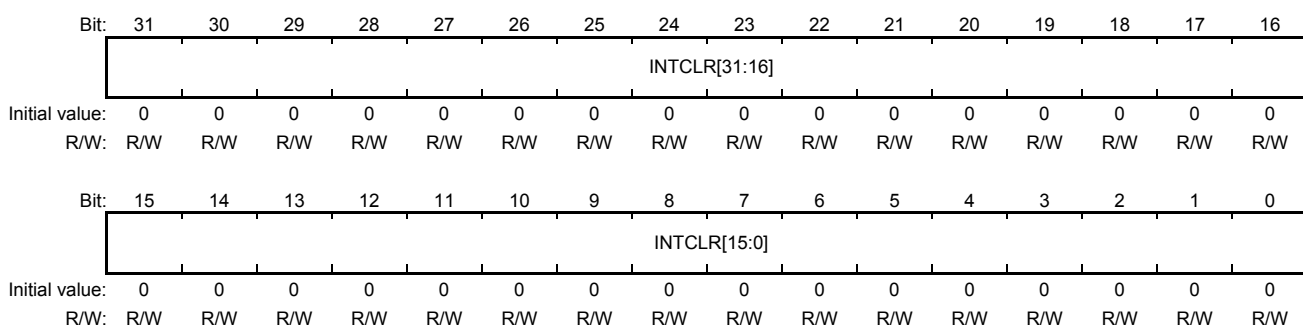
### 6.4.6 Interrupt Clear Register n (INTCLR0 to INTCLRn)

Note: n = 5 [RZ/G1H], n = 7 [RZ/G1M/N], n = 6 [RZ/G1E]

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

When the interrupt display register is currently indicates the reception of the interrupt input on the port for which the edge detection is selected by the edge/level select register (with configuring for one edge/both edge select register) in interrupt input mode, INTCLR clears the indication. Specifically, writing 1 to the bits in INTCLR corresponding to port numbers can clear the corresponding bits in the interrupt display register. However, when the interrupt display register is currently indicates the reception of the interrupt input on the port for which the level detection is selected by the edge/level select register, writing 1 to the corresponding bits in INTCLR cannot clear the corresponding bits in the interrupt display register. Only writing 1 to INTCLR is effective; INTCLR is always read as 0.

[Hardware default value: H'00000000 = interrupt indication is cleared for no ports.]



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	INTCLR [31:0]	All 0	R/W	Writing 1 to bits corresponding to port numbers clears the corresponding bits in the interrupt display register. 0: No effect 1: Interrupt display register bit is cleared.

Note: Unused bits should be set to the initial values.

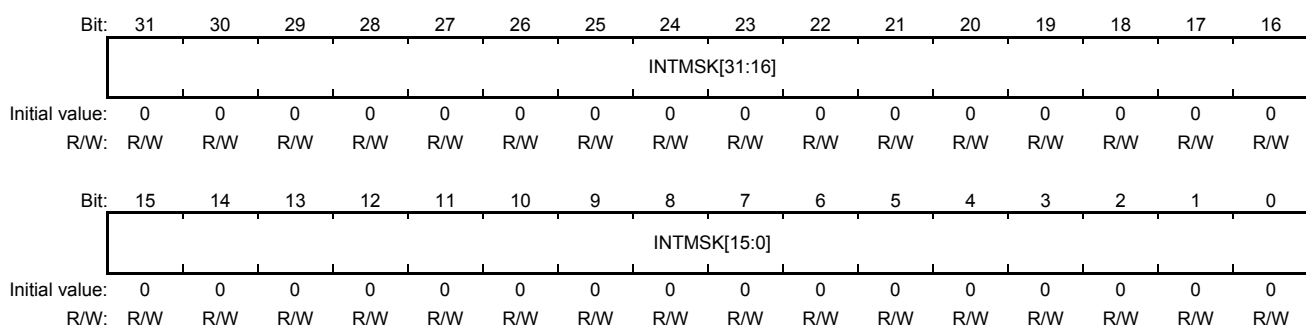
### 6.4.7 Interrupt Mask Register n (INTMSK0 to INTMSKn)

Note: n = 5 [RZ/G1H], n = 7 [RZ/G1M/N], n = 6 [RZ/G1E]

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

INTMSK masks the interrupt requests indicated by the interrupt display register. Interrupts can be separately masked using the corresponding bits in INTMSK. When all the bits currently indicating the reception of the interrupt signals are masked, no interrupt signals are output to the interrupt control block. Masks can be canceled by writing 1 to the corresponding bits in the interrupt mask clear register. Only writing 0 to this register is effective.

[Hardware default value: H'00000000 = all the ports are masked.]



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	INTMSK [31:0]	All 0	R/W	Setting a mask to the bit disables the corresponding interrupt signal to be output to the interrupt control block. 0: Interrupt is masked. 1: Interrupt is not masked.

Note: Unused bits should be set to the initial values.

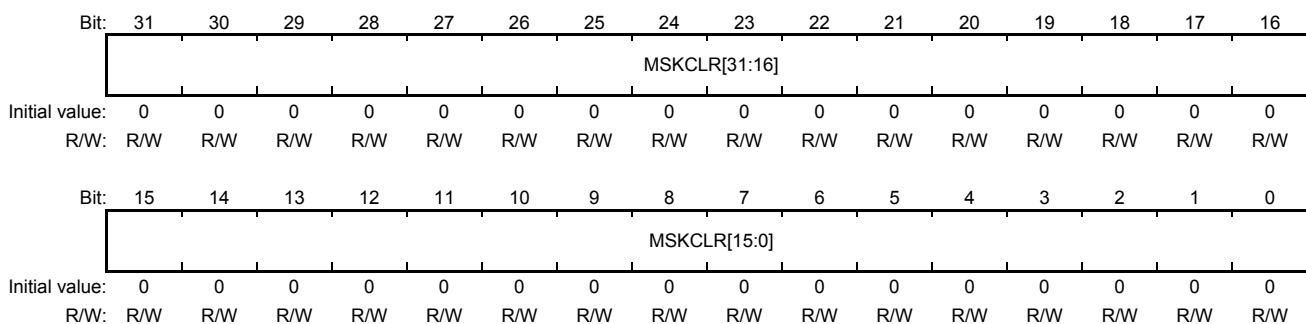
**6.4.8 Interrupt Mask Clear Register n (MSKCLR0 to MSKCLRn)**

Note: n = 5 [RZ/G1H], n = 7 [RZ/G1M/N], n = 6 [RZ/G1E]

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

MSKCLR cancels masks that are set by the interrupt mask register. Each mask can be canceled (cleared) by writing 1 to the corresponding bit in MSKCLR. Only writing 1 to MSKCLR is effective; MSKCLR is always read as 0.

[Hardware default value: H'00000000 = interrupt masks are cleared for no ports.]



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	MSKCLR [31:0]	All 0	R/W	Setting a mask to the bit disables the corresponding interrupt signal to be output to the interrupt control block. 0: No effect 1: Interrupt is not masked.

Note: Unused bits should be set to the initial values. (When GPIO is not selected by the pin multiplex settings, do not cancel the interrupt mask.)

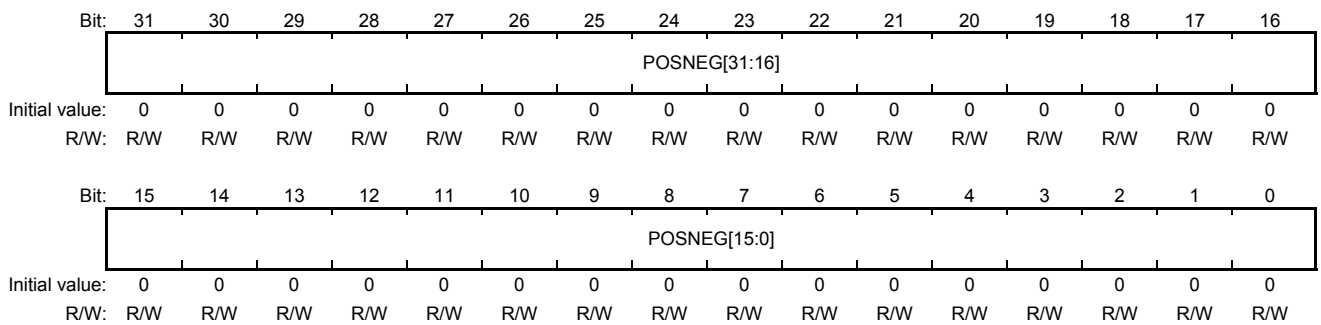
**6.4.9 Positive/Negative Logic Select Register n (POSNEG0 to POSNEGn)**

Note: n = 5 [RZ/G1H], n = 7 [RZ/G1M/N], n = 6 [RZ/G1E]

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

POSNEG selects the polarity (positive or negative logic) of each port pin in general input mode, general output mode, or interrupt input mode. POSNEG should be set before mode selection.

[Hardware default value: H'00000000 = positive logic is selected for all the ports.]



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	POSNEG [31:0]	All 0	R/W	Selects the polarity (positive or negative logic) of each port pin. 0: Positive logic 1: Negative logic

Note: Unused bits should be set to the initial values.

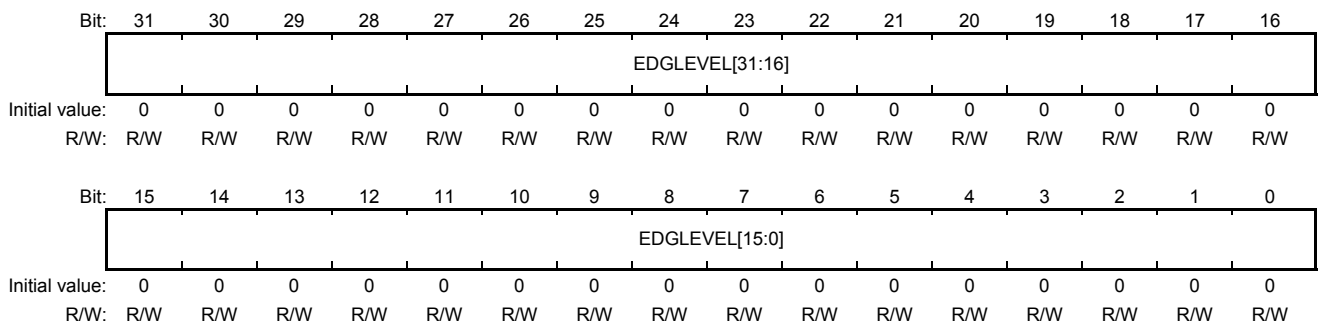
**6.4.10 Edge/level Select Register n (EDGLEVEL0 to EDGLEVELn)**

Note: n = 5 [RZ/G1H], n = 7 [RZ/G1M/N], n = 6 [RZ/G1E]

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

EDGLEVEL is valid only for the ports for which interrupt input mode is selected by the general IO/interrupt switching register. Specifically, EDGLEVEL selects the detection conditions (edge or level) of the interrupt input signal on each port pin for which interrupt input mode is selected. EDGLEVEL should be set before selection of interrupt input mode.

[Hardware default value: H'00000000 = level detection is selected for all the ports.]



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	EDGLEVEL [31:0]	All 0	R/W	Selects the level or edge as detection conditions of the interrupt input signal on each port pin for which interrupt input mode is selected. 0: Level 1: Edge

Note: Unused bits should be set to the initial values.

### 6.4.11 Chattering Prevention On/Off Register n (FILONOFF0 to FILONOFFn)

Note: n = 5 [RZ/G1H], n = 7 [RZ/G1M/N], n = 6 [RZ/G1E]

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√*	√	√	√

Note: \* Some restrictions apply.

FILONOFF prevents chattering input to the port pins 0 to 3 of each GPIO block and controls frequency of filter clock (generated from peripheral clock CP $\phi$ ) for chattering prevention function. For details, refer to section 6.5, Handling of Input Signals on Port Pins.

[Hardware default value: H'00000000 = chattering prevention function is turned off for all the ports.]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CLKSEL[1:0]		—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	FILONOFF[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31, 30	CLKSEL[1:0]	00	R/W	Filter clock frequency setting. 00: CP $\phi$ /2500. ([H], [M/N], [E]) 01: CP $\phi$ /1250. ([M/N], [E]). Setting prohibited. ([H]) 10: CP $\phi$ /625. ([M/N], [E]). Setting prohibited. ([H]) 11: CP $\phi$ /312.5. ([M/N], [E]). Setting prohibited. ([H])
29 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3 to 0	FILONOFF [3:0]	All 0	R/W	Enables or disables the chattering prevention function. 0: Chattering prevention function is disabled. 1: Chattering prevention function is enabled. The bits FILONOFF[n] (n = 0 to 3) are used to control the port pin n.

Note: Unused bits should be set to the initial values.

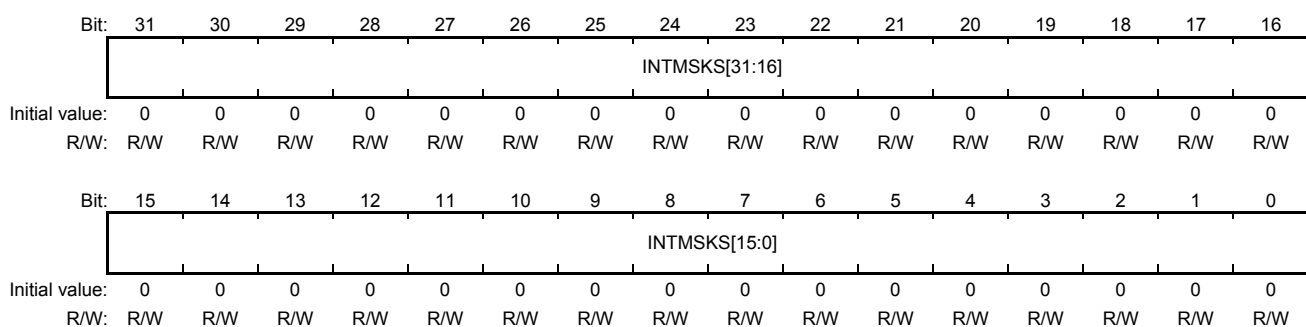
### 6.4.12 Interrupt Sub Mask Register n (INTMSKS0 to INTMSKSn)

Note: n = 5 [RZ/G1H], n = 7 [RZ/G1M/N], n = 6 [RZ/G1E]

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

INTMSKS masks the alternative interrupt requests indicated by the interrupt display register. Interrupts can be separately masked using the corresponding bits in INTMSKS. When all the bits currently indicating the reception of the interrupt signals are masked, no alternative interrupt signals are output to the interrupt control block. Masks can be canceled by writing 1 to the corresponding bits in the interrupt sub mask clear register. Only writing 0 to this register is effective.

[Hardware default value: H'00000000 = all the ports are masked.]



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	INTMSKS [31:0]	All 0	R/W	Setting a mask to the bit disables the corresponding alternative interrupt signal to be output to the interrupt control block. 0: Interrupt is masked. 1: Interrupt is not masked.

Note: Unused bits should be set to the initial values.



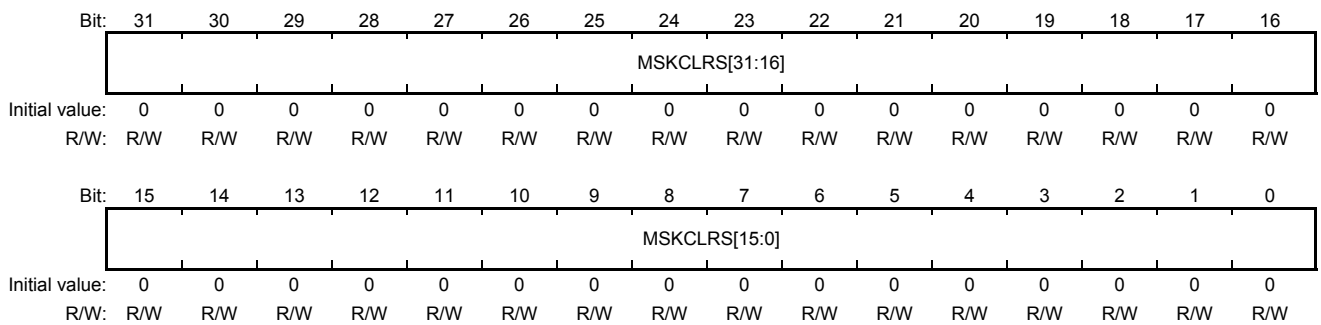
**6.4.13 Interrupt Sub Mask Clear Register n (MSKCLRS0 to MSKCLRSn)**

Note: n = 5 [RZ/G1H], n = 7 [RZ/G1M/N], n = 6 [RZ/G1E]

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

MSKCLRS cancels masks that are set by the interrupt sub mask register. Each mask can be canceled (cleared) by writing 1 to the corresponding bit in MSKCLRS. Only writing 1 to MSKCLRS is effective; MSKCLRS is always read as 0.

[Hardware default value: H'00000000 = alternative interrupt masks are cleared for no ports.]



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	MSKCLRS [31:0]	All 0	R/W	Setting a mask to the bit disables the corresponding alternative interrupt signal to be output to the interrupt control block. 0: No effect 1: Interrupt is not masked.

Note: Unused bits should be set to the initial values. (When GPIO is not selected by the pin multiplex settings, do not cancel the alternative interrupt mask.)

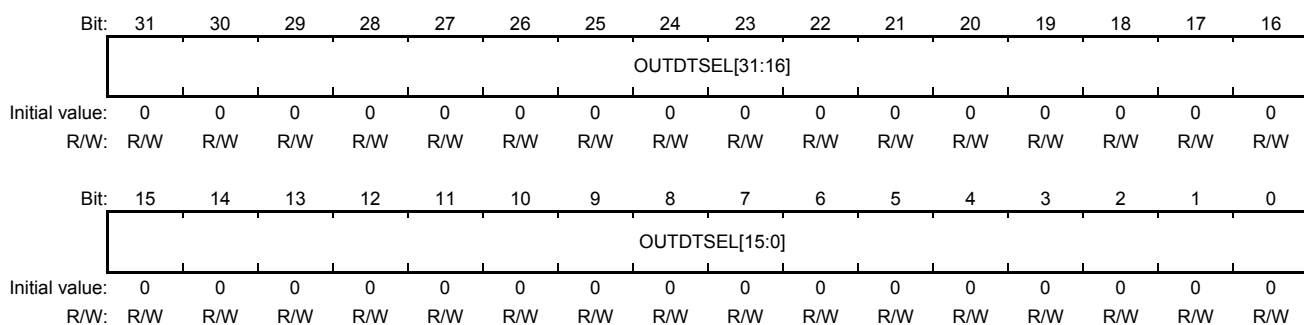
### 6.4.14 Output Data Select Register n (OUTDTSEL0 to OUTDTSELn)

Note: n = 5 [RZ/G1H], n = 7 [RZ/G1M/N], n = 6 [RZ/G1E]

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

OUTDTSEL is valid only for the ports for which general input/output mode is selected by the general IO/interrupt switching register and then general output mode is selected by the general input/output switching register. OUTDTSEL selects if OUTDT or OUTDTH/OUTDTL will be the output data of GPIO. When choosing OUTDT, configuration is performed as described in section 6.4.3, General Output Register n (OUTDT0 to OUTDTn). When choosing OUTDTH/OUTDTL, output data will be output by writing the appropriate data to the corresponding bits in OUTDTH or OUTDTL. Note that the polarity of the output signal should be previously set using the corresponding bit in the positive/negative logic select register. Furthermore, this register should be set before writing data to OUTDTH/OUTDTL registers.

[Hardware default value: H'00000000 = Out data register is used to output data.]



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	OUTDTSEL [31:0]	All 0	R/W	Choosing whether output data is output by general output register OUTDT or output data high register OUTDTH/output data low register OUTDTL.  0: General output register is used to output the data. 1: Output data high register and output data low register is used to output the data.

Note: Unused bits should be set to the initial values.

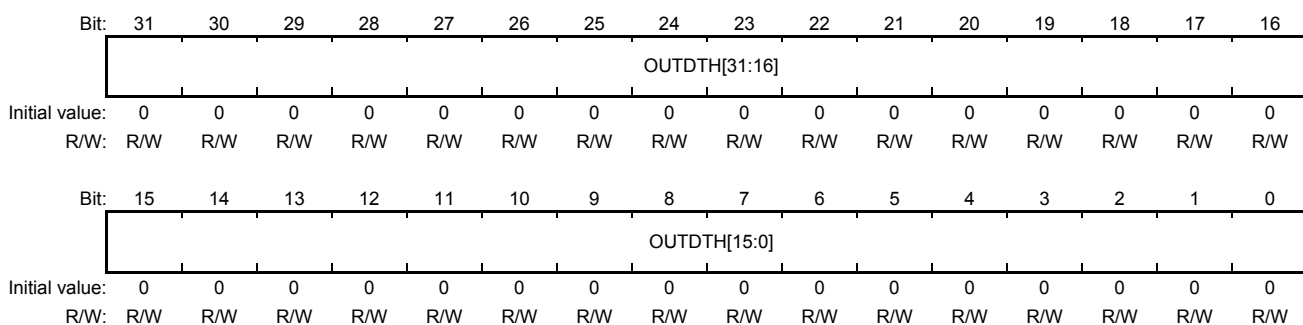
### 6.4.15 Output Data High Register n (OUTDTH0 to OUTDTHn)

Note: n = 5 [RZ/G1H], n = 7 [RZ/G1M/N], n = 6 [RZ/G1E]

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

OUTDTH is valid only for the ports for which general input/output mode is selected by the general IO/interrupt switching register and then general output mode is selected by the general input/output switching register, and the output data select register OUTDTSSEL is configured to choose OUTDTH/OUTDTL register to output the data of GPIO. Only writing 1 to OUTDTH is effective. Otherwise, setting makes no changes. Reading OUTDTH returns the values of the latest data set to OUTDTH or OUTDTL right before that. Note that the polarity of the output signal should be previously set using the corresponding bit in the positive/negative logic select register. Furthermore, this register should be written and read after output data select register OUTDTSSEL is set. Reading OUTDTH without appropriately configuring OUTDTSSEL can return value of OUTDT register.

[Hardware default value: H'00000000 = 0 is output from all the ports with setting OUTDTSSEL.]



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	OUTDTH [31:0]	All 0	R/W	Outputting high value data. 0: Invalid data. 1: Valid data.

Note: Unused bits should be set to the initial values.

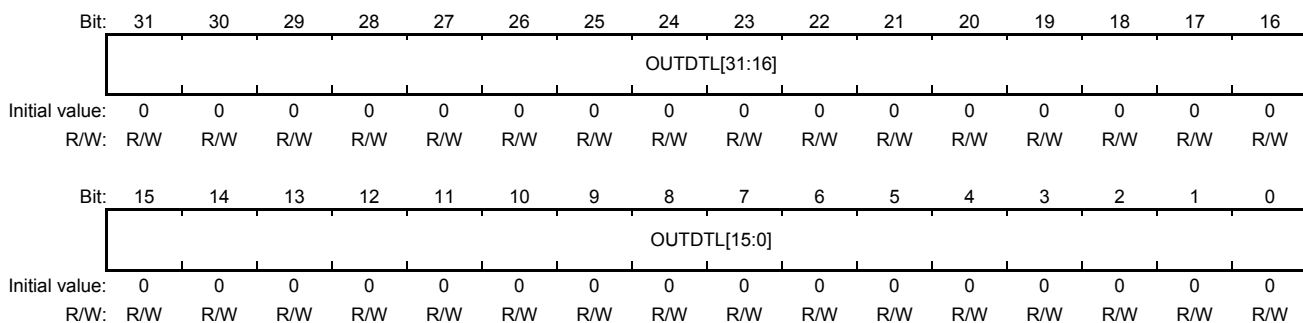
### 6.4.16 Output Data Low Register n (OUTDTL0 to OUTDTLn)

Note: n = 5 [RZ/G1H], n = 7 [RZ/G1M/N], n = 6 [RZ/G1E]

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

OUTDTL is valid only for the ports for which general input/output mode is selected by the general IO/interrupt switching register and then general output mode is selected by the general input/output switching register, and the output data select register OUTDTSSEL is configured to choose OUTDTH/OUTDTL register to output the data of GPIO. Only writing 0 to OUTDTL is effective. Otherwise, setting makes no changes. Reading OUTDTL returns the values of the latest data set to OUTDTL or OUTDTH right before that. Note that the polarity of the output signal should be previously set using the corresponding bit in the positive/negative logic select register. Furthermore, this register should be written or read after output data select registers OUTDTSSEL is set. Reading OUTDTH without appropriately configuring OUTDTSSEL can return value of OUTDT register.

[Hardware default value: H'00000000 = 0 is output from all the ports with setting OUTDTSSEL.]



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	OUTDTL [31:0]	All 0	R/W	Outputting low value data. 0: Valid data. 1: Invalid data.

Note: Unused bits should be set to the initial values.

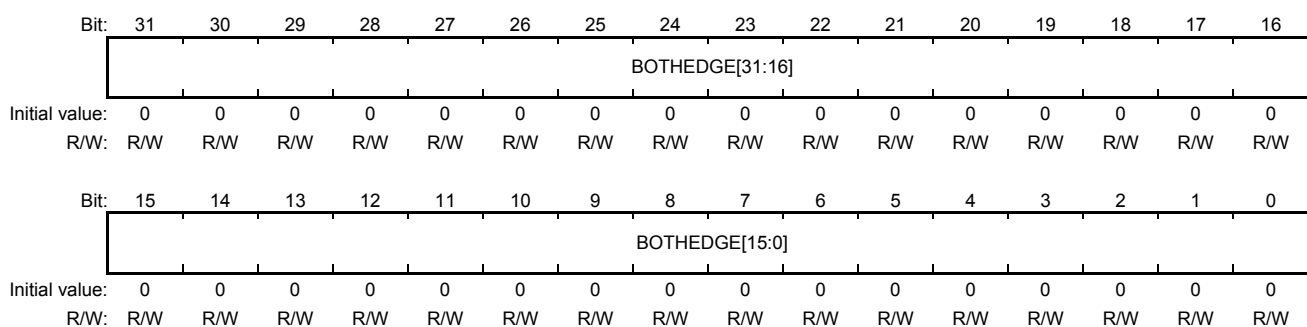
### 6.4.17 One Edge/Both Edge Select Register n (BOTHEDGE0 to BOTHEDGEN)

Note: n = 5 [RZ/G1H], n = 7 [RZ/G1M/N], n = 6 [RZ/G1E]

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

BOTHEDGE is valid only when the edge detection mode is selected by the edge/level select registers. Specially, BOTHEDGE selects the detection condition (one edge or both edges) of the interrupt input signal on each port pin for which interrupt input mode (selected by the general IO/interrupt switching registers) and edge detection mode are selected. BOTHEDGE should be set before selection of interrupt input mode.

[Hardware default value: H'00000000 = both edge detection mode is disabled for all the ports.]



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	BOTHEDGE [31:0]	All 0	R/W	Selecting one edge or both edge detection condition of the interrupt input signal on each port pin for which interrupt input mode and edge detection mode are selected. 0: One edge. 1: Both edges.

Note: Unused bits should be set to the initial values.

## 6.5 Handling of Input Signals on Port Pins

### 6.5.1 Chattering

In general input mode and interrupt input modes, a filtering function can be used for the port pins 0 to 3 of each GPIO block to prevent external chattering input. Specifically, when a bit in the chattering prevention on/off register is set to use the function, the external input to the corresponding port pin is sampled four consecutive times based on the filter clock signal, which is internally generated by the GPIO. The external input is canceled except when the active input is detected four consecutive times. Therefore, when a filtering function is used, input to the port pins 0 to 3 of each GPIO block need to be at least four sampling clock cycles long (with the peripheral clock (CP $\phi$ )).

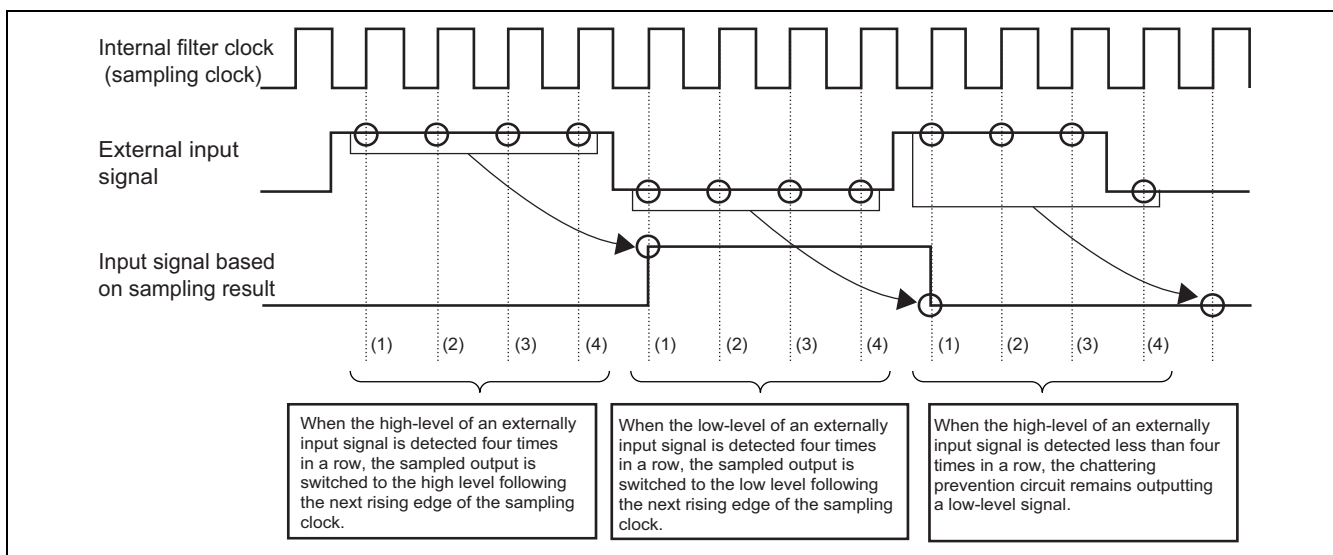


Figure 6.2 Sampling Timing Chart

### 6.5.2 Input Signal Synchronization

In general input mode and interrupt input mode, external input signals on all port pins are synchronized with the GPIO clock (CP $\phi$ ).

### 6.6 Interrupt Display Timing Charts

Figure 6.3 shows the interrupt display timing and Figure 6.4 shows the note on the timing. In both figures, the positive logic and edge-sensitive input are assumed.

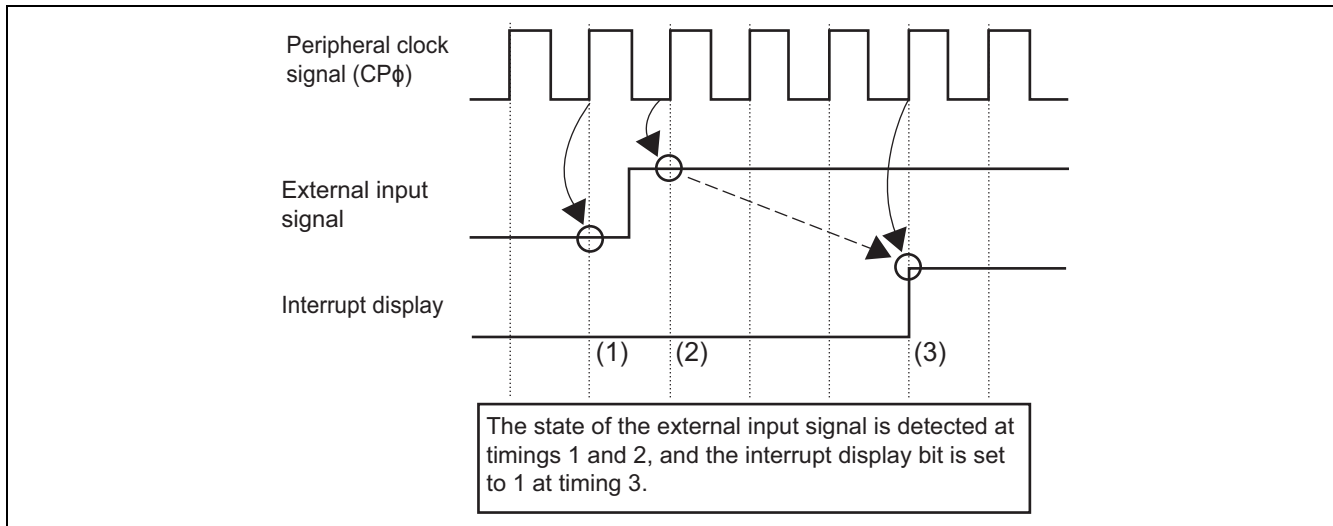


Figure 6.3 Interrupt Display Timing

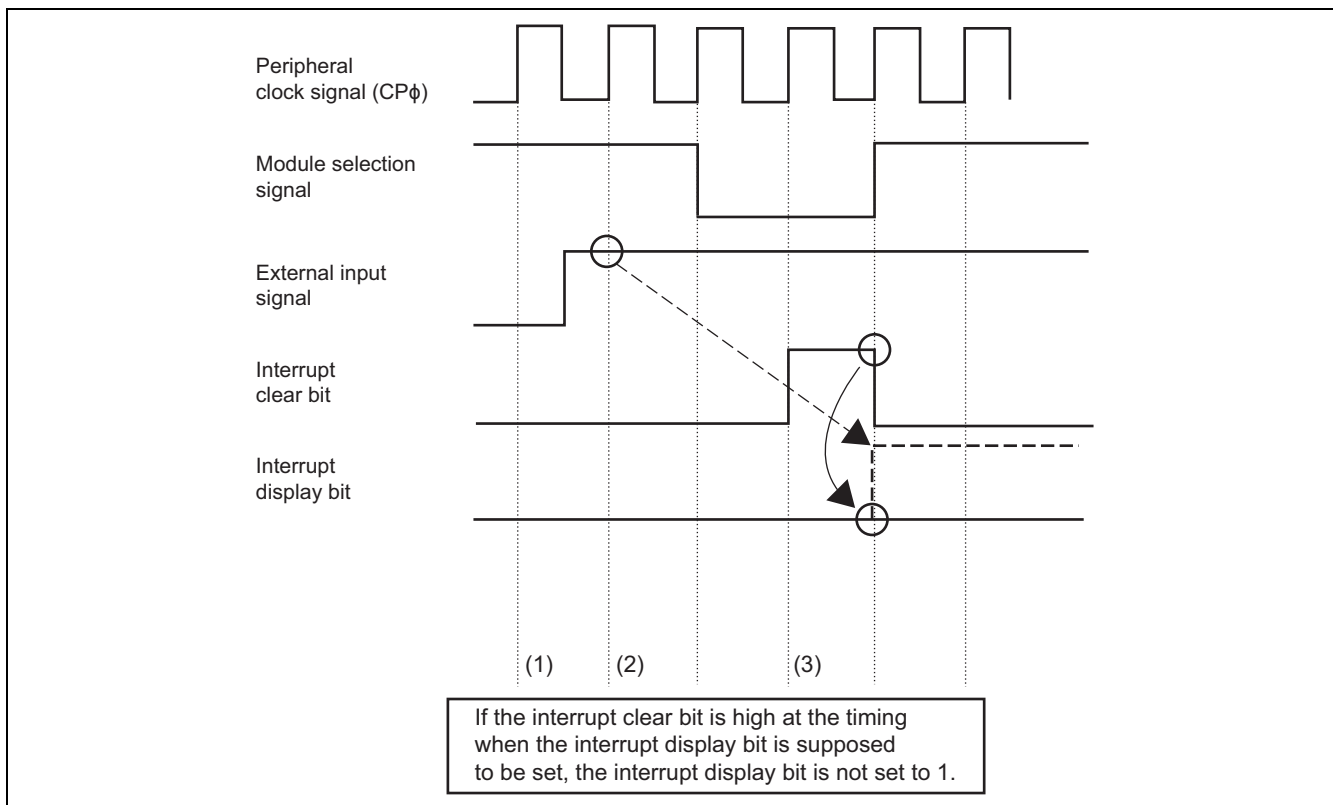


Figure 6.4 Note on Interrupt Display Timing

## 6.7 Using GPIO

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

The following sections describe how to use the GPIO. If the GPIO is not used according to the procedures shown here, operations are not guaranteed.

### 6.7.1 Setting Edge-Sensitive Interrupt Input Mode

For setting edge-sensitive interrupt input mode, refer to the procedure shown in Figure 6.5.

Note that an unexpected interrupt might be generated in the module if setting (1), (2), (3) or (4) in the flowchart is changed. When changing the setting, (5) and (6) should be done.

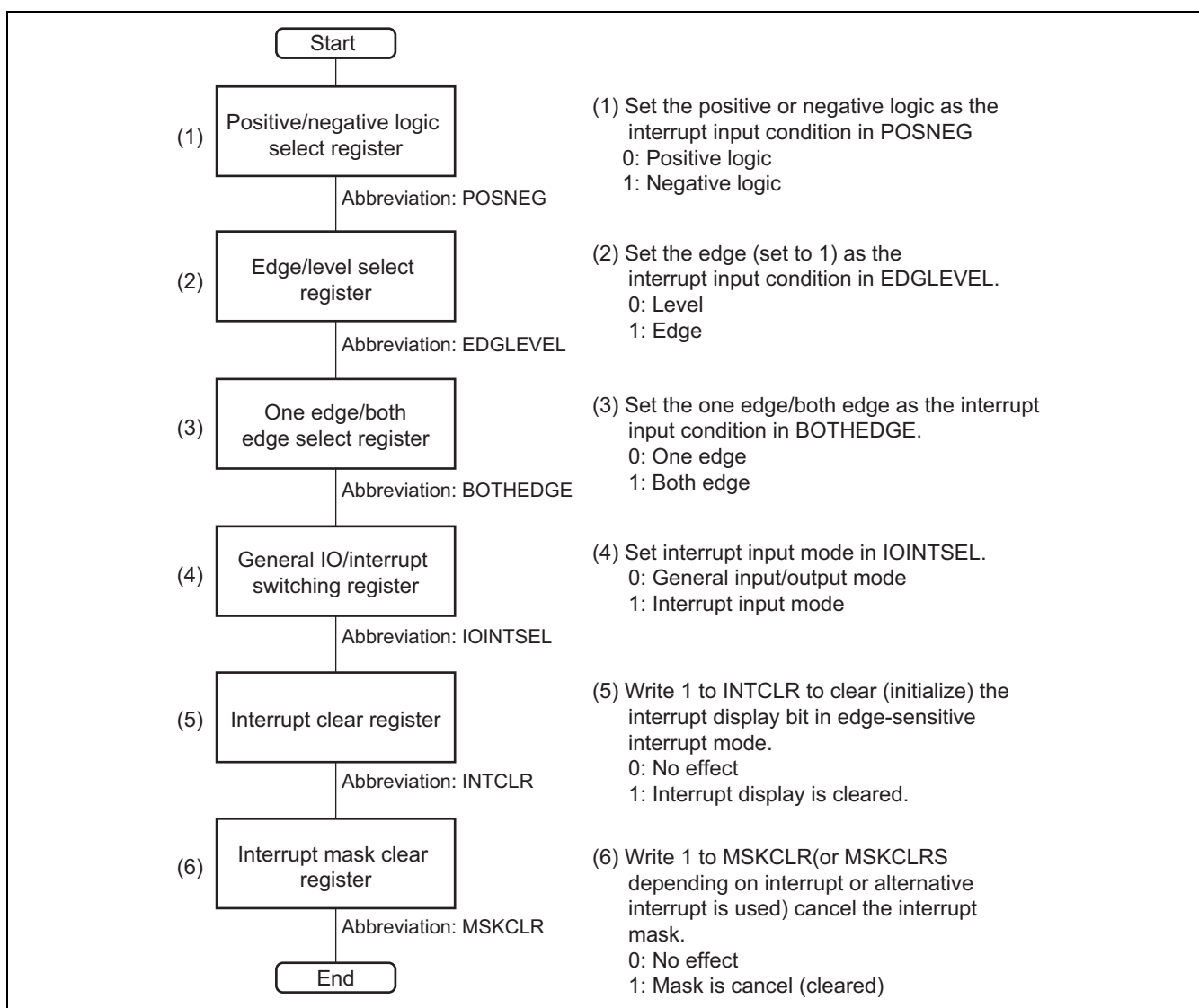


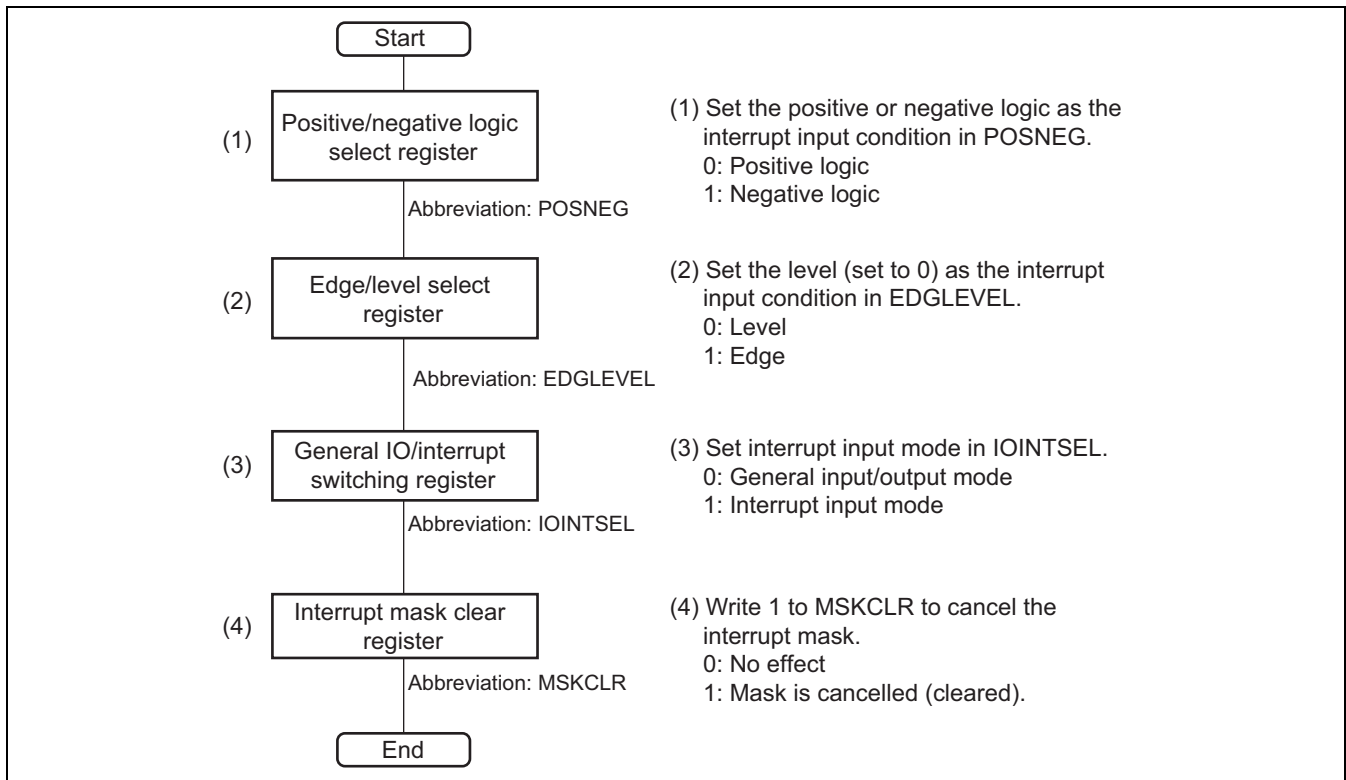
Figure 6.5 Flowchart of Setting the GPIO to Edge-Sensitive Interrupt Input Mode



### 6.7.2 Setting Level-Sensitive Interrupt Input Mode

For setting level-sensitive interrupt input mode, refer to the procedure shown in Figure 6.6.

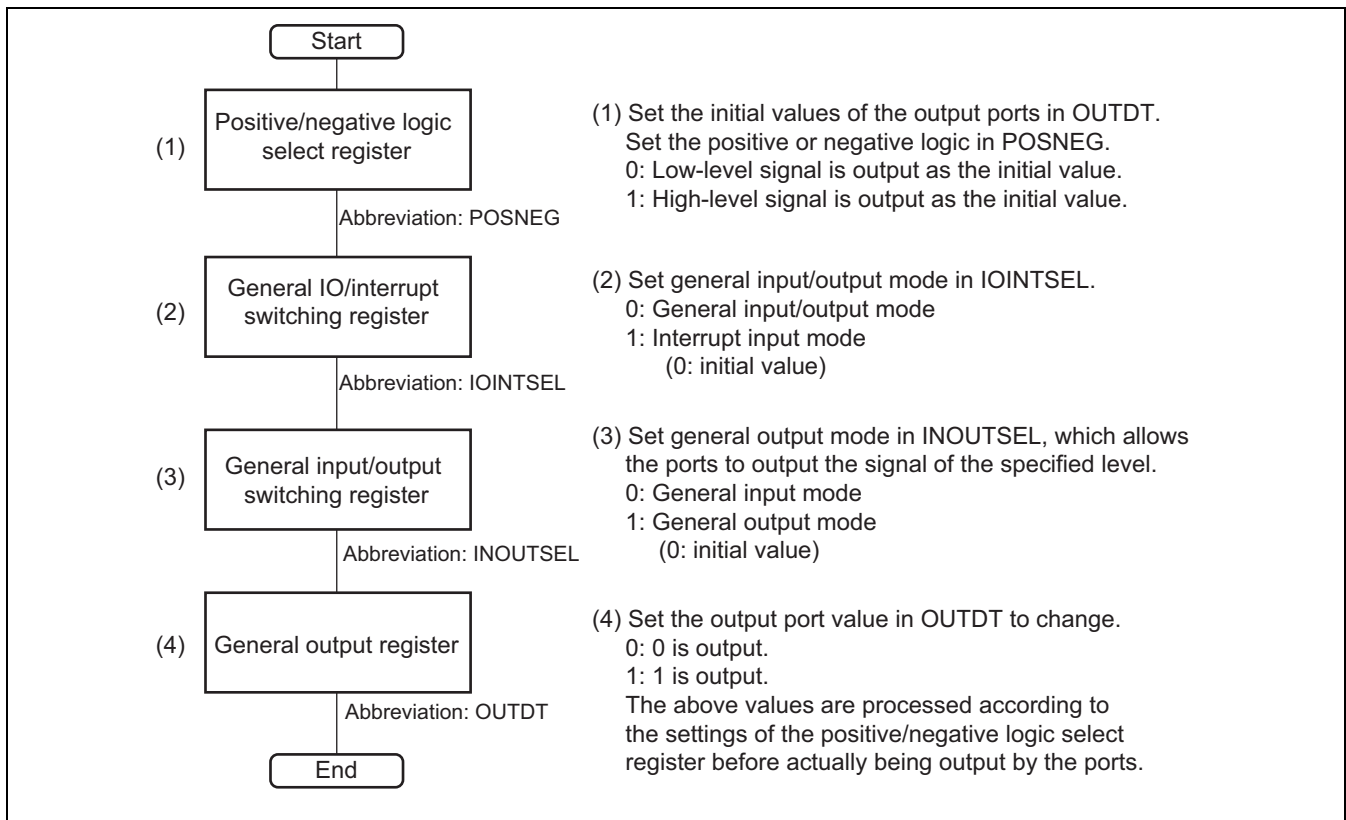
Note that when an external level-sensitive interrupt input signal is stopped, the corresponding interrupt is canceled automatically. In level-sensitive interrupt input mode, the interrupt clear register is invalid.



**Figure 6.6 Flowchart of Setting the GPIO to Level-Sensitive Interrupt Input Mode**

### 6.7.3 Setting General Output Mode

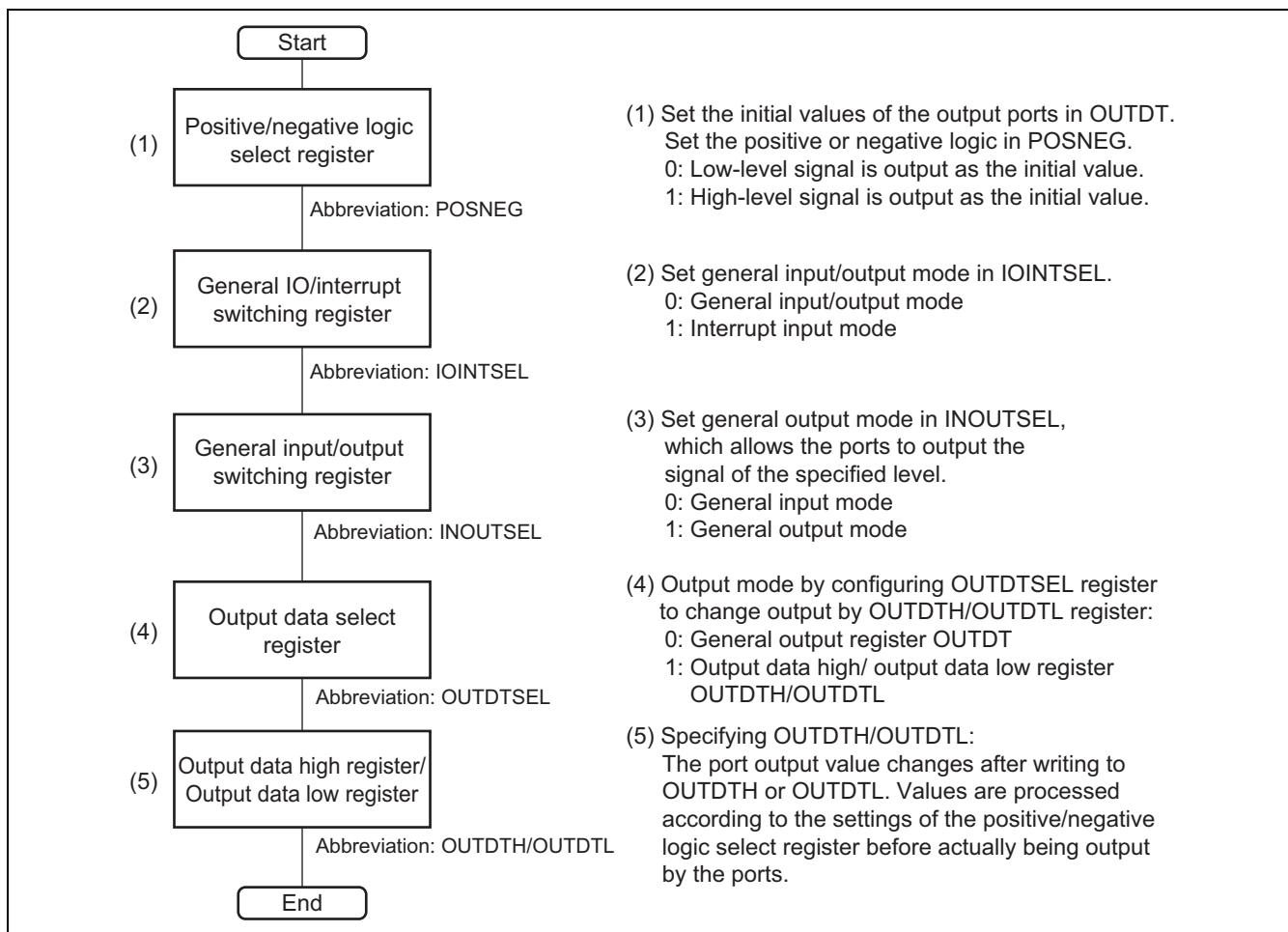
For setting general output mode, refer to the procedure shown in Figure 6.7.



**Figure 6.7 Flowchart of Setting the GPIO to General Output Mode**

### 6.7.4 Setting Output data high/Output data low Mode

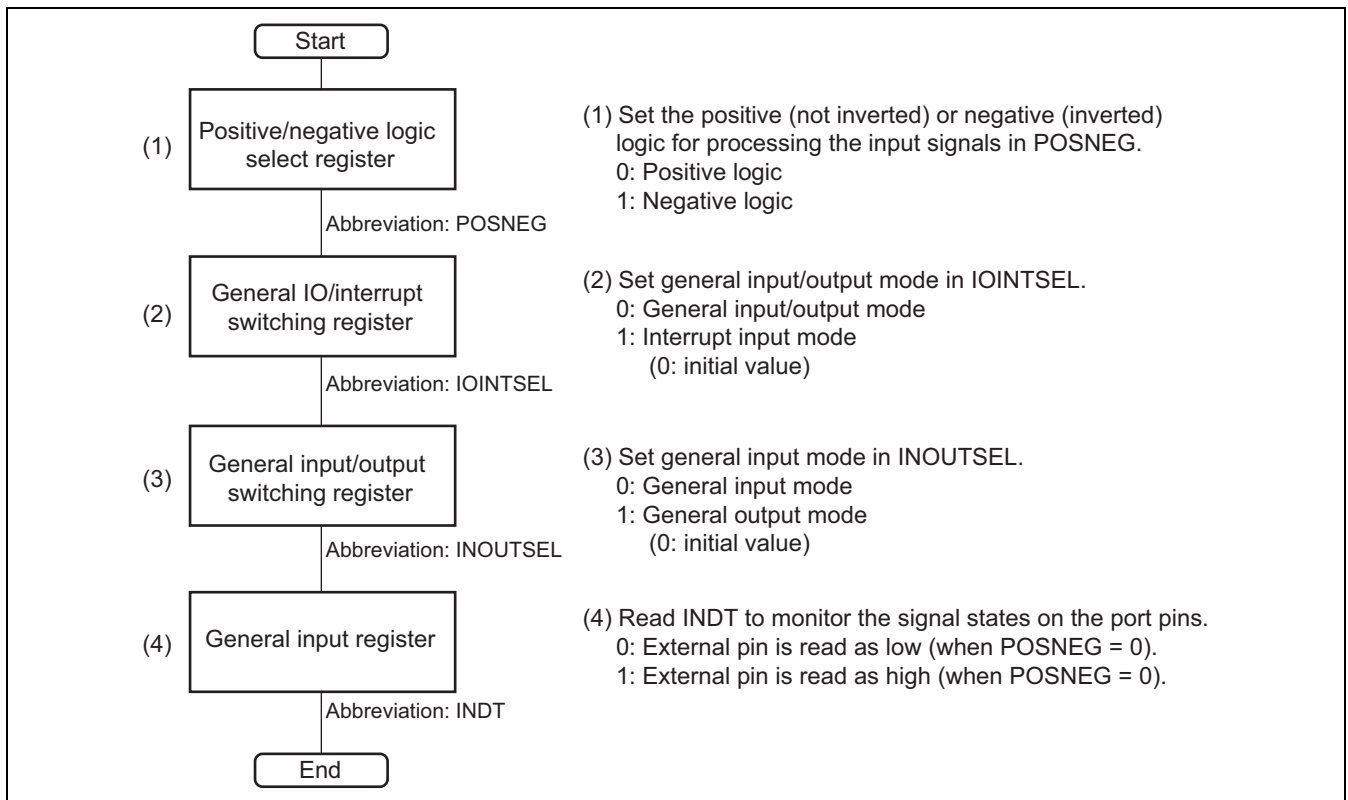
For setting output data high/output data low mode, refer to the procedure shown in Figure 6.8.



**Figure 6.8 Flowchart of Setting the GPIO to Output data high/ Output data low Mode**

### 6.7.5 Setting General Input Mode

For setting general input mode, refer to the procedure shown in Figure 6.9.



**Figure 6.9 Flowchart of Setting the GPIO to General Input Mode**

## 7. Clock Pulse Generator (CPG)

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

This LSI has a clock pulse generator (CPG). The CPG consists of oscillators, PLL circuit 0, PLL circuit 1, PLL circuit 3, clock dividers, and the control circuit. The CPG generates various clocks used by this LSI.

### 7.1 Features

- Generates various clocks for LSI internal operation.
  - 3 PLLs for common/application part modules
  - SYS-CPU divider, common divider and DDR divider for system basic operation.
  - Dedicated dividers for special clock
- Controls clock supply to modules according to the module status (power supply status, etc.)

A block diagram of the CPG is shown in Figure 7.1.

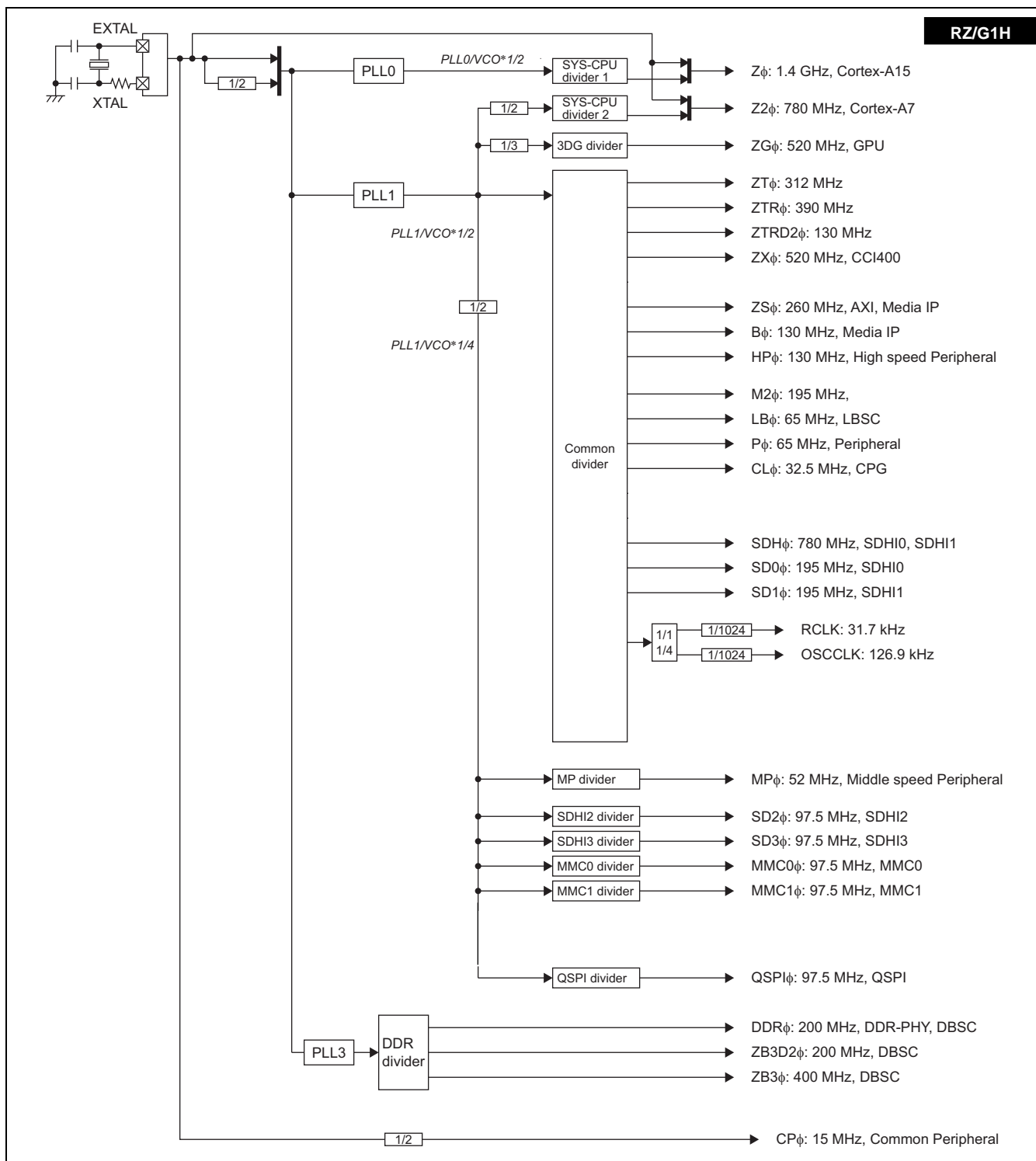


Figure 7.1a Block Diagram of CPG [RZ/G1H]

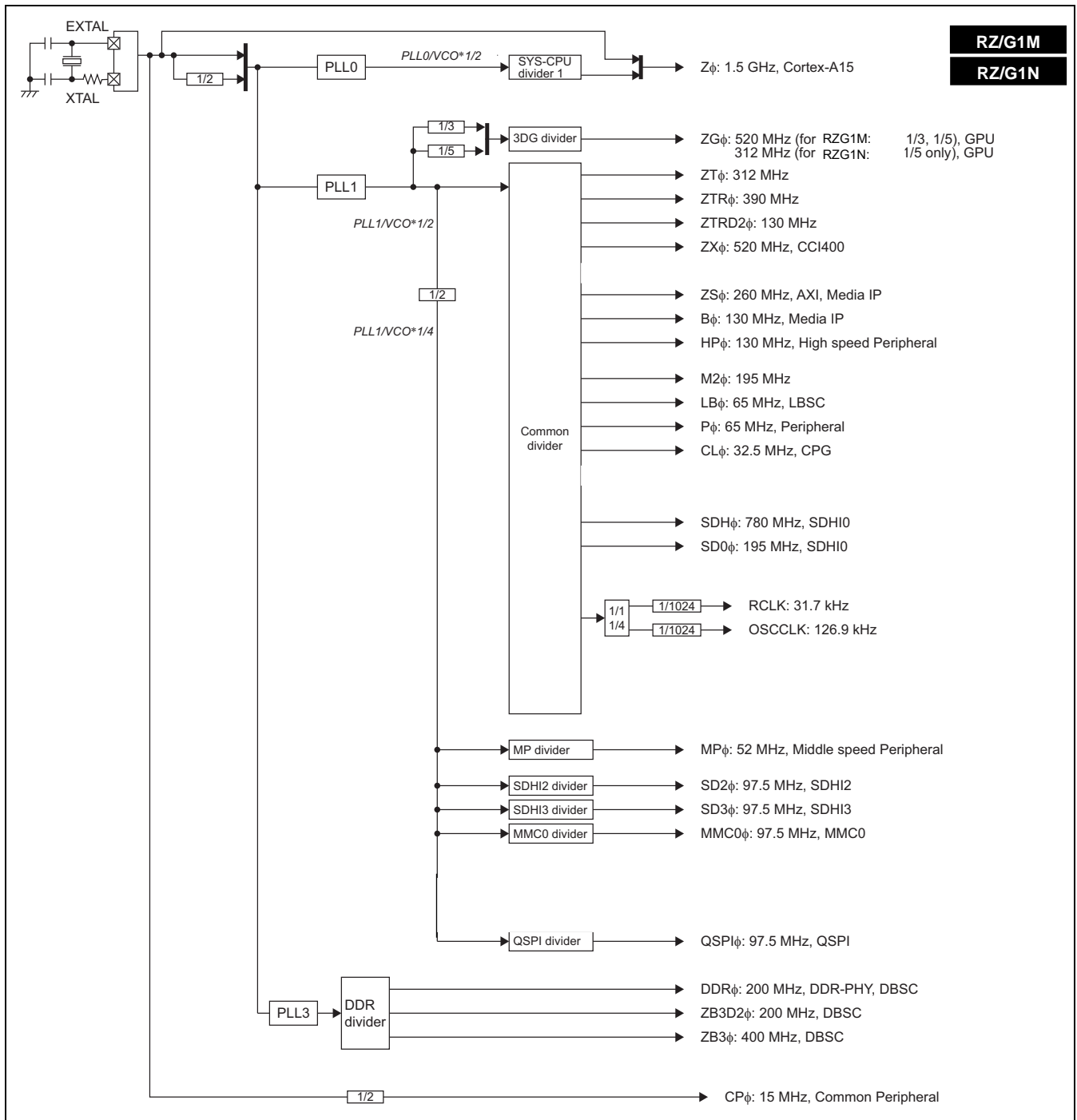


Figure 7.1b Block Diagram of CPG [RZ/G1M/N]

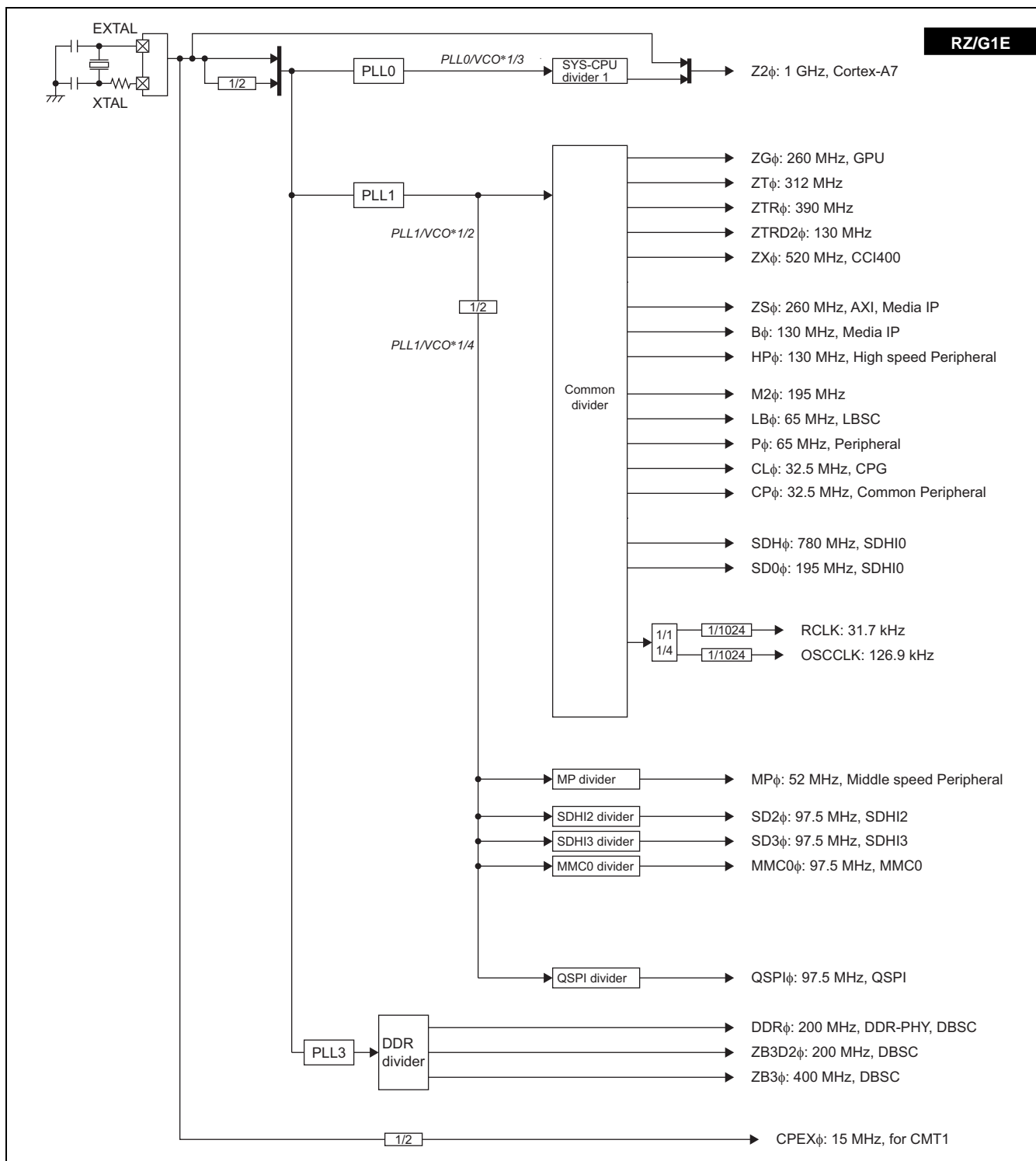


Figure 7.1c Block Diagram of CPG [RZ/G1E]



Followings are the functions of each block of CPG.

<b>RZ/G1H</b>	<b>RZ/G1N</b>
<b>RZ/G1M</b>	<b>RZ/G1E</b>

**(1) PLL circuit 0 (PLL0)**

**[RZ/G1H/M/N]:**

PLL circuit 0 multiplies EXTAL or EXTAL/2 clock. The multiplication ratio is set by the PLL0CR.

**[RZ/G1E]:**

PLL circuit 0 multiplies EXTAL or EXTAL/2 clock.

**(2) PLL circuit 1 (PLL1)**

PLL circuit 1 multiplies the input clock from EXTAL (EXTAL or EXTAL/2) by the multiplication ratio shown in Table 7.5 (Tables 7.5a, and 7.5b).

**(3) PLL Circuit 3 (PLL3)**

PLL circuit 3 multiplies the input clock from EXTAL (EXTAL or EXTAL/2) by the multiplication ratio shown in Table 7.5 (Tables 7.5a, and 7.5b).

**(4) SYS-CPU clock divider 1**

**[RZ/G1H/M/N]:**

The SYS-CPU clock divider 1 divides PLL0 output clock. This divider generates the AP-System core clocks ( $Z\phi$ ). The division ratio is set by the frequency control register C (FRQCRC).

**[RZ/G1E]:**

The SYS-CPU clock divider 1 divides PLL0 output clock. This divider generates the AP-System core clocks ( $Z2\phi$ ).

**(5) SYS-CPU clock divider 2 [RZ/G1H]**

The SYS-CPU clock divider 2 divides PLL1 output clock. This divider generates the AP-System core clocks ( $Z2\phi$ ).

**(6) GPU clock divider [RZ/G1H/M/N]**

The GPU clock divider divides PLL1 output clock. This divider generates the system GPU clock ( $ZG\phi$ ).

**(7) Common clock divider**

The common clock divider divides PLL1 output clock. This divider generates various system clocks. The division ratio is set by the frequency control register B (FRQCRB).

**(8) DDR clock divider**

The DDR clock divider divides PLL3 output clock, and generates DDR-PHY clock and DBSC clock.

**(9) Dedicated dividers**

The each dedicated divider generates special clock for the related modules.

## 7.2 Input/Output Pins

Table 7.1 lists the CPG pin configuration.

**Table 7.1 Pin Configuration and Functions of CPG**

Pin Name	Function	I/O	Description
XTAL	Clock input pins	Output	Outputs amplified negative feedback of EXTAL
EXTAL		Input	Used as an external clock input pin
CLKOUT	External Bus Clock output pin	Output	Used as an external clock output pin
MD0	Mode 0	Input	Free running mode/Step up mode
MD9	Mode 9	Input	EXTAL/XTAL pin setting
MD13	Mode 13	Input	PLL multiplication ratio setting
MD14	Mode 14	Input	PLL multiplication ratio setting
MD19	Mode 19	Input	DDR clock frequency setting
MD18 [RZ/G1H/E]	Mode 18	Input	[RZ/G1H]: External bus clock frequency setting [RZ/G1E]: DDR clock frequency setting Be sure to set MD18 to 0 (MD18 doesn't have external pin).
MD15 [RZ/G1H]	Mode 15	Input	Be sure to set MD15 to 0.

### 7.3 List of Clock Outputs

RZ/G1H	RZ/G1N
RZ/G1M	RZ/G1E

Table 7.2 lists the clock output of CPG.

**Table 7.2a List of Clocks [RZ/G1H]**

Name	Clock Source	Frequency			Clock Domain, Function
		Dividing ratio	Maximum	Initial	
Z $\phi$	SYS-CPU divider 1	Variable	1.4 GHz	~1.3 GHz	System CPU (Cortex-A15) clock
Z2 $\phi$	SYS-CPU divider 2	Fixed	780 MHz	780 MHz	System CPU (Cortex-A7) clock
ZG $\phi$	3DG divider	Fixed	520 MHz	520 MHz	GPU clock
ZTR $\phi$	Common divider	Variable	390 MHz	260 MHz	Trace interface clock
ZTRD2 $\phi$	Common divider	Variable	130 MHz	130 MHz	System trace interface clock
ZT $\phi$	Common divider	Variable	312 MHz	312 MHz	Internal trace clock
ZX $\phi$	Common divider	Fixed	520 MHz	520 MHz	Cache coherent interconnect clock
ZS $\phi$	Common divider	Fixed	260 MHz	260 MHz	AXI clock/media IP clock
HP $\phi$	Common divider	Fixed	130 MHz	130 MHz	High-speed peripheral clock
B $\phi$	Common divider	Fixed	130 MHz	130 MHz	Media clock
LB $\phi$	Common divider	Fixed	65 MHz	*1	LBSC clock
P $\phi$	Common divider	Fixed	65 MHz	65 MHz	Peripheral clock
CL $\phi$	Common divider	Fixed	32.5 MHz	32.5 MHz	
M2 $\phi$	Common divider	Fixed	195 MHz	195 MHz	Media clock 2
ZB3 $\phi$	DDR divider	Fixed	400 MHz	400 MHz *6	DBSC clock
ZB3D2 $\phi$	DDR divider	Fixed	200 MHz	200 MHz *6	DBSC clock
DDR $\phi$	DDR divider	Fixed	200 MHz	200 MHz *6	DDR-PHY clock
SDH $\phi$	Common divider	Variable	780 MHz	780 MHz	SDHI clock H
SD0 $\phi$	Common divider	Variable	195 MHz	97.5 MHz	SDHI clock 0
SD1 $\phi$	Common divider	Variable	195 MHz	97.5 MHz	SDHI clock 1
SD2 $\phi$	SDHI2 divider	Variable	97.5 MHz	48.75 MHz	SDHI clock 2
SD3 $\phi$	SDHI3 divider	Variable	97.5 MHz	48.75 MHz	SDHI clock 3
MMC0 $\phi$	MMC0 divider	Variable	97.5 MHz	12.18 MHz	MMC clock 0
MMC1 $\phi$	MMC1 divider	Variable	97.5 MHz	12.18 MHz	MMC clock 1
MP $\phi$	MP divider	Fixed	52 MHz	52 MHz	MP clock
QSPI $\phi$	QSPI divider	Variable	97.5 MHz	*2	QSPI clock
CP $\phi$	EXTAL	Fixed	15 MHz	*3	Common peripheral clock, EXTAL $\times$ 1/2
RCAN $\phi$	USB_EXTAL	Fixed	8 MHz *5	*4	RCAN clock USB_EXTAL $\times$ 1/6
RCLK	Common divider	Fixed	31.7 kHz	31.7 kHz	
OSCCLK	Common divider	Fixed	126.9 kHz	126.9 kHz	

- Notes:
1. The frequency of  $LB\phi$  depends on the value of MD18.
  2. The frequency of  $QSPI\phi$  depends on the value of MD3, MD2 and MD1.  
When MD3 = L, MD2 = H, MD1 = L,  $QSPI\phi = 97.5$  MHz.  
In the other cases of MD3, MD2 and MD1 setting,  $QSPI\phi = 78$  MHz.
  3. The frequency of  $CP\phi$  is equal to  $EXTAL \times 1/2$ . For example, when the frequency of EXTAL is equal to 20 MHz, the frequency of  $CP\phi$  is equal to 10 MHz.
  4. The frequency of  $RCAN\phi$  is equal to  $USB\_EXTAL \times 1/6$ .
  5. The maximum value of the RCAN clock frequency is derived by frequency-dividing the USB clock by 6. Note that input of an external clock signal through the USB\_EXTAL pin is not supported; use the crystal resonator for the USB clock. is not supported; use the crystal resonator for the USB clock.
  6. The initial frequency of  $ZB3\phi$ ,  $ZB3D2\phi$ , and  $DDR\phi$  depend the setting of MD19. The values shown in the above table corresponds to the case of MD19 = 0.

**Table 7.2b List of Clocks [RZ/G1M/N]**

Name	Clock Source	Frequency			Clock Domain, Function
		Dividing ratio	Maximum	Initial	
Z $\phi$	SYS-CPU divider 1	Variable	1.5 GHz	~1.3 GHz	System CPU (Cortex-A15) clock
ZG $\phi$	3DG divider	Selectable	520/312 MHz	520/312 MHz	GPU clock (520/312 MHz)
ZTR $\phi$	Common divider	Variable	390 MHz	260 MHz	Trace interface clock
ZTRD2 $\phi$	Common divider	Variable	130 MHz	130 MHz	System trace interface clock
ZT $\phi$	Common divider	Variable	312 MHz	312 MHz	Internal trace clock
ZX $\phi$	Common divider	Fixed	520 MHz	520 MHz	Cache coherent interconnect clock
ZS $\phi$	Common divider	Fixed	260 MHz	260 MHz	AXI clock/media IP clock
HP $\phi$	Common divider	Fixed	130 MHz	130 MHz	High-speed peripheral clock
B $\phi$	Common divider	Fixed	130 MHz	130 MHz	Media clock
LB $\phi$	Common divider	Fixed	65 MHz	65 MHz	LBSC clock
P $\phi$	Common divider	Fixed	65 MHz	65 MHz	Peripheral clock
CL $\phi$	Common divider	Fixed	32.5 MHz	32.5 MHz	
M2 $\phi$	Common divider	Fixed	195 MHz	195 MHz	Media clock 2
ZB3 $\phi$	DDR divider	Fixed	400 MHz	400 MHz* <sup>5</sup>	DBSC clock
ZB3D2 $\phi$	DDR divider	Fixed	200 MHz	200 MHz* <sup>5</sup>	DBSC clock
DDR $\phi$	DDR divider	Fixed	200 MHz	200 MHz* <sup>5</sup>	DDR-PHY clock
SDH $\phi$	Common divider	Variable	780 MHz	780 MHz	SDHI clock H
SD0 $\phi$	Common divider	Variable	195 MHz	97.5 MHz	SDHI clock 0
SD2 $\phi$	SDHI2 divider	Variable	97.5 MHz	48.75 MHz	SDHI clock 2
SD3 $\phi$	SDHI3 divider	Variable	97.5 MHz	48.75 MHz	SDHI clock 3
MMC0 $\phi$	MMC0 divider	Variable	97.5 MHz	12.18 MHz	MMC clock 0
MP $\phi$	MP divider	Fixed	52 MHz	52 MHz	MP clock
QSPI $\phi$	QSPI divider	Variable	97.5 MHz	* <sup>1</sup>	QSPI clock
CP $\phi$	EXTAL	Fixed	15 MHz	* <sup>2</sup>	Common peripheral clock, EXTAL $\times$ 1/2
RCAN $\phi$	USB_EXTAL	Fixed	8 MHz * <sup>4</sup>	* <sup>3</sup>	RCAN clock USB_EXTAL $\times$ 1/6
RCLK	Common divider	Fixed	31.7 kHz	31.7 kHz	
OSCCLK	Common divider	Fixed	126.9 kHz	126.9 kHz	

Notes: 1. The frequency of QSPI $\phi$  depends on the value of MD3, MD2 and MD1.

When MD3 = L, MD2 = H, MD1 = L, QSPI $\phi$  = 97.5 MHz.

In the other cases of MD3, MD2 and MD1 setting, QSPI $\phi$  = 78 MHz.

- The frequency of CP $\phi$  is equal to EXTAL  $\times$  1/2. For example, when the frequency of EXTAL is equal to 20 MHz, the frequency of CP $\phi$  is equal to 10 MHz.
- The frequency of RCAN $\phi$  is equal to USB\_EXTAL  $\times$  1/6.
- The maximum value of the RCAN clock frequency is derived by frequency-dividing the USB clock by 6. Note that input of an external clock signal through the USB\_EXTAL pin is not supported; use the crystal resonator for the USB clock.
- The initial frequency of ZB3 $\phi$ , ZB3D2 $\phi$ , and DDR $\phi$  depend the setting of MD19. The values shown in the above table corresponds to the case of MD19 = 0.

Table 7.2c List of Clocks [RZ/G1E]

Name	Clock Source	Frequency			Clock Domain, Function
		Dividing ratio	Maximum	Initial	
Z2 $\phi$	SYS-CPU divider 1	Fixed	1 GHz	~1 GHz	System CPU (Cortex-A7) clock
ZG $\phi$	3DG divider	Fixed	260 MHz	260 MHz	GPU clock
ZTR $\phi$	Common divider	Variable	390 MHz	260 MHz	Trace interface clock
ZTRD2 $\phi$	Common divider	Variable	130 MHz	130 MHz	System trace interface clock
ZT $\phi$	Common divider	Variable	312 MHz	312 MHz	Internal trace clock
ZX $\phi$	Common divider	Fixed	520 MHz	520 MHz	Cache coherent interconnect clock
ZS $\phi$	Common divider	Fixed	260 MHz	260 MHz	AXI clock/media IP clock
HP $\phi$	Common divider	Fixed	130 MHz	130 MHz	High-speed peripheral clock
B $\phi$	Common divider	Fixed	130 MHz	130 MHz	Media clock
LB $\phi$	Common divider	Fixed	65 MHz	65 MHz	LBSC clock
P $\phi$	Common divider	Fixed	65 MHz	65 MHz	Peripheral clock
CL $\phi$	Common divider	Fixed	32.5 MHz	32.5 MHz	
CP $\phi$	Common divider	Fixed	32.5 MHz	32.5 MHz	
M2 $\phi$	Common divider	Fixed	195 MHz	195 MHz	Media clock 2
ZB3 $\phi$	DDR divider	Fixed	400 MHz	400 MHz* <sup>1</sup>	DBSC clock
ZB3D2 $\phi$	DDR divider	Fixed	200 MHz	200 MHz* <sup>1</sup>	DBSC clock
DDR $\phi$	DDR divider	Fixed	200 MHz	200 MHz* <sup>1</sup>	DDR-PHY clock
SDH $\phi$	Common divider	Variable	780 MHz	780 MHz	SDHI clock H
SD0 $\phi$	Common divider	Variable	195 MHz	97.5 MHz	SDHI clock 0
SD2 $\phi$	SDHI2 divider	Variable	97.5 MHz	48.75 MHz	SDHI clock 2
SD3 $\phi$	SDHI3 divider	Variable	97.5 MHz	48.75 MHz	SDHI clock 3
MMC0 $\phi$	MMC0 divider	Variable	97.5 MHz	12.18 MHz	MMC clock 0
MP $\phi$	MP divider	Fixed	52 MHz	52 MHz	MP clock
QSPI $\phi$	QSPI divider	Variable	97.5 MHz	* <sup>2</sup>	QSPI clock
CPEX $\phi$	EXTAL	Fixed	15 MHz	* <sup>3</sup>	EXTAL $\times$ 1/2
RCAN $\phi$	USB_EXTAL	Fixed	8 MHz * <sup>5</sup>	* <sup>4</sup>	RCAN clock USB_EXTAL $\times$ 1/6
RCLK	Common divider	Fixed	31.7 kHz	31.7 kHz	
OSCCLK	Common divider	Fixed	126.9 kHz	126.9 kHz	

Notes: 1. The frequency of ZB3 $\phi$ , ZB3D2 $\phi$  and DDR $\phi$  depends on the value of MD19.

2. The frequency of QSPI $\phi$  depends on the value of MD3, MD2 and MD1.

When MD3=L, MD2 = H, MD1 = L, QSPI $\phi$  = 97.5 MHz.

In the other cases of MD3, MD2 and MD1 setting, QSPI $\phi$  = 78 MHz.

3. The frequency of CPEX $\phi$  is equal to EXTAL  $\times$  1/2. For example, when the frequency of EXTAL is equal to 20 MHz, the frequency of CPEX $\phi$  is equal to 10 MHz.

4. The frequency of RCAN $\phi$  is equal to USB\_EXTAL  $\times$  1/6.

5. The maximum value of the RCAN clock frequency is derived by frequency-dividing the USB clock by 6. Note that input of an external clock signal through the USB\_EXTAL pin is not supported; use the crystal resonator for the USB clock.

## 7.4 Clock Operating Modes

RZ/G1H	RZ/G1N
RZ/G1M	RZ/G1E

**Table 7.4 MD9 Settings**

MD9	EXTAL/XTAL Pin Settings
0	Inputs an external clock to the EXTAL pin.
1	Connects the crystal resonator to the EXTAL and XTAL pins.

**Table 7.5a PLL Multiplication Ratio [RZ/G1H/M/N]**

MD14	MD13	MD19	EXTAL Input Frequency (MHz)	Divider Setting of EXTAL Input	PLL0* <sup>1</sup> Multiplication Ratio	PLL1* <sup>3</sup> Multiplication Ratio	PLL3* <sup>2</sup> Multiplication Ratio
0	0	0	15	× 1	× 172	× 208	× 106
0	0	1	15	× 1	× 172	× 208	× 88
0	1	0	20	× 1	× 130	× 156	× 80
0	1	1	20	× 1	× 130	× 156	× 66
1	0	0	26	× 1/2	× 200	× 240	× 122
1	0	1	26	× 1/2	× 200	× 240	× 102
1	1	0	30	× 1/2	× 172	× 208	× 106
1	1	1	30	× 1/2	× 172	× 208	× 88

Notes: 1. PLL to create Z $\phi$  for Cortex-A15

Example of frequency calculation (in the case MD14 = H, MD13 = H)

VCO output frequency of PLL0 = 30 MHz × 1/2 × 172 = 2580 MHz

Maximum frequency of Z $\phi$  = 2580 MHz × 1/2 (fixed divider) × 32/32 = 1290 MHz

2. PLL to create clocks related to DBSC & DDR-PHY
3. PLL to create the other clocks

**Table 7.5b PLL Multiplication Ratio [RZ/G1E]**

MD14	MD13	MD19	MD18	EXTAL Input Frequency (MHz)	Divider Setting of EXTAL Input	PLL0* <sup>1</sup> Multiplication Ratio	PLL1* <sup>3</sup> Multiplication Ratio	PLL3* <sup>2</sup> Multiplication Ratio
0	0	1	0	15	× 1	× 200	× 208	× 88
0	1	1	0	20	× 1	× 150	× 156	× 66
1	0	1	0	26	× 1/2	× 230	× 240	× 102
1	1	1	0	30	× 1/2	× 200	× 208	× 88

Notes: 1. PLL to create Z2 $\phi$  for Cortex-A7.

Example of frequency calculation (in the case MD14 = H, MD13 = H)

VCO output frequency of PLL0 = 30 MHz × 1/2 × 200 = 3000 MHz

Maximum frequency of Z2 $\phi$  = 3000 MHz × 1/3 (fixed divider) = 1000 MHz

2. PLL to create clocks related to DBSC & DDR-PHY
3. PLL to create the other clocks
4. Be sure to set MD18 to 0.

**Table 7.6a MD19 Settings [RZ/G1H/M/N]**

MD19	DDR Clock Frequency Setting
0	DDR3-1600 mode
1	DDR3-1333 mode

Note: See Table 7.5 along with this table.

**Table 7.6b MD19 and MD18 Settings [RZ/G1E]**

MD19	MD18	DDR Clock Frequency Setting
0	0	Setting prohibited
1	0	DDR3-1333 mode
0	1	Setting prohibited
1	1	Setting prohibited

Note: See Table 7.5 along with this table.

**Table 7.7 MD18 Settings [RZ/G1H]**

MD18	External Bus Clock (CLKOUT) Frequency Setting
0	Division ratio = 1/24 of the PLL1 oscillation frequency
1	Division ratio = 1/36 of the PLL1 oscillation frequency

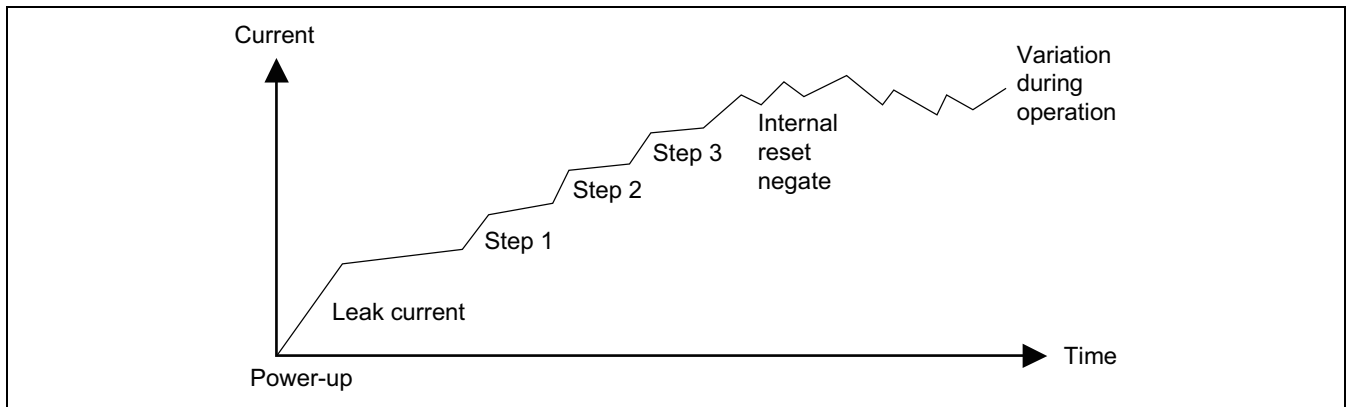


The MD0 pin selects either free-running mode or step-up mode. In step-up mode, the frequency of the LSI-internal clocks is increased step by step at booting up of the LSI by the PRESET# pin so that the power consumption increases gradually.

**Table 7.8 MD0 Settings**

MD0	Description
0	Free-running mode
1	Step-up mode*

Note: \* Not available in the RZ/G1H, M, and N when MD14 = 1 (high).



**Figure 7.2 Current Change in Step-Up Mode**

**Table 7.9 MD15 Settings [RZ/G1H]**

MD15	MD15 Settings
0	Be sure to set MD15 to 0.
1	Setting prohibited

## 7.5 Register Descriptions

Table 7.10 shows the CPG register configuration block. Table 7.11 shows the register states in each operating mode.

32bit-width access is only available when access to this register.

**Table 7.10 Register Configurations**

Register Name	Abbreviation	R/W	Address	Access Size	RZ/G Series Products			
					RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Frequency control register B	FRQCRB	R/W	H'E615 0004	32	√	√	√	√
Frequency control register C	FRQCRC	R/W	H'E615 00E0	32	√	√	√	—
PLL Enable Control Register	PLLECR	R	H'E615 00D0	32	√	√	√	—
PLL0 control register	PLL0CR	R/W	H'E615 00D8	32	√	√	√	—
RGX control register	RGXCR	R/W	H'E615 00B4	32	√	√	√	—
SDHI clock frequency control register	SDCKCR	R/W	H'E615 0074	32	√	√	√	√
SDHI2 clock frequency control register	SD2CKCR	R/W	H'E615 0078	32	√	√	√	√
SDHI3 clock frequency control register	SD3CKCR	R/W	H'E615 026C	32	√	√	√	√
GPU clock frequency control register	GPUCKCR	R/W	H'E615 0234	32	—	√	√	—
MMC0 clock frequency control register	MMC0CKCR	R/W	H'E615 0240	32	√	√	√	√
MMC1 clock frequency control register	MMC1CKCR	R/W	H'E615 0244	32	√	—	—	—
RCAN clock frequency control register	RCANCKCR	R/W	H'E615 0270	32	√	√	√	√

Note: Do not write to any addresses other than listed above. Operations cannot be guaranteed if writing is attempted. Values read from addresses other than those listed above are undefined.

**Table 7.11 Register States in Each Operating Mode**

Register	Power-On Reset
All Registers	Initialized

**7.5.1 Frequency Control Register B (FRQCRB)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

FRQCRB is a 32-bit readable/writable register. This registers specifies the frequency division ratios of debug trace port clock (ZTRφ), debug trace bus clock (ZTφ), and debug clock (ZTRD2φ).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	KICK	—	—	—	—	—	—	—	ZTRFC[3:0]			ZTFC[3:0]				
Initial value:	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0
R/W:	R/W	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	ZTRD2FC[3:0]			
Initial value:	0	0	0	1	0	0	1	1	0	1	0	1	0	1	0	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	KICK	0	R/W	<p>KICK bit</p> <p>Setting 1 to this register activates the FRQCRB and FRQCRC setting.</p> <p>0: Does not activate the FRQCRB and FRQCRC settings.</p> <p>1: Activates the FRQCRB, FRQCRC settings.</p> <p>This bit is automatically cleared to 0 when the frequency division setting is completed after 1 is written to this bit.</p>
30 to 24	—	All 0	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>
23 to 20	ZTRFC[3:0]	0011	R/W	<p>Debug Trace port Clock (ZTRφ) Frequency Division Ratio</p> <p>0010: × 1/4</p> <p>1100: × 1/5</p> <p>0011: × 1/6</p> <p>0100: × 1/8</p> <p>0101: × 1/12</p> <p>0110: × 1/16</p> <p>0111: × 1/18</p> <p>1000: × 1/24</p> <p>Other values: Setting prohibited</p> <p>Note: ZTRφ is supplied only in debugging mode.</p>

Bit	Bit Name	Initial Value	R/W	Description
19 to 16	ZTFC[3:0]	1100	R/W	Debug Trace bus Clock (ZT $\phi$ ) Frequency Division Ratio 1100: $\times 1/5$ 0011: $\times 1/6$ 0100: $\times 1/8$ 0101: $\times 1/12$ 0110: $\times 1/16$ 0111: $\times 1/18$ 1000: $\times 1/24$ Other values: Setting prohibited Note: ZT $\phi$ is supplied only in debugging mode.
15 to 12	—	0001	R	These bits are always read as 0001. The write value should always be 0001.
11 to 8	—	0011	R	These bits are always read as 0011. The write value should always be 0011.
7 to 4	—	0101	R	These bits are always read as 0101. The write value should always be 0101.
3 to 0	ZTRD2FC[3:0]	0101	R/W	Debug Clock (ZTRD2 $\phi$ ) Frequency Division Ratio 0101: $\times 1/12$ 0110: $\times 1/16$ 0111: $\times 1/18$ 1000: $\times 1/24$ Other values: Setting prohibited Note: ZTR $\phi$ is supplied only in debugging mode.

### 7.5.2 Frequency Control Register C (FRQCRC)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

FRQCRC is a 32-bit readable/writable register. This register specifies the frequency division ratios of the System CPU (Cortex-A15) clock ( $Z\phi$ ).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	ZFC[4:0]				—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 18	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
17	—	1	R	Reserved This bit is always read as 1. The write value should always be 1.
16 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12 to 8	ZFC[4:0]	00000	R/W	AP-System Core (Cortex-A15) Clock ( $Z\phi$ ) Frequency Division Ratio 00000: $\times 32/32$ 00001: $\times 31/32$ : 11110: $\times 2/32$ 11111: $\times 1/32$ Other values: Setting prohibited
7 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

### 7.5.3 PLL Enable Control Register (PLLECR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

PLLECR is a 32-bit readable register that indicates the state of PLL0.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	PLL0 T	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	1	0	1	1	0	0	0	0	1	0	1	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
11	—	1	R	Reserved This bit is always read as 1. The write value should always be 1.
10	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
9	—	1	R	Reserved This bit is always read as 1. The write value should always be 1.
8	PLL0ST	1	R	PLL circuit 0 status Displays PLL circuit 0 status (on or off). 0: PLL circuit 0 is turned off. The main clock is supplied as a clock output. 1: PLL circuit 0 is turned on. The output from PLL circuit 0 is supplied as a clock output.
7 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
3	—	1	R	Reserved This bit is always read as 1. The write value should always be 1.
2	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
1	—	1	R	Reserved This bit is always read as 1. The write value should always be 1.
0	—	1	R	Reserved This bit is always read as 1. The write value should always be 1.

## 7.5.4 PLL0 Control Register (PLL0CR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

PLL0CR is a 32-bit readable/writable register. This register specifies the multiplication ratio of PLL circuit 0. When writing to this register, change only bits STC[6:0] (Read-modify-write).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
	—	STC[6:0]						—	—	—	—	—	—	—	—	—	—
Initial value:	0	*1	*1	*1	*1	*1	*1	*1	0	0	0	0	0	0	0	0	
R/W:	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R	
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
Initial value:	0	0	0	MD14	0	0	0	1	0	0	0	0	0	0	0	0	
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	

Bit	Bit Name	Initial Value	R/W	Description
31	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
30 to 24	STC[6:0]	*1	R/W	PLL Circuit 0 Multiplication Ratio*2 PLL circuit 0 performs multiplication with a ratio of (setting + 1) The realized frequency has the following relationship. $(\text{PLL0}/\text{VCO}) = (\text{PLL0 reference clock}) \times (\text{setting} + 1) \times 2$ $(\text{PLL0 output}) = (\text{SYS-CPU divider1 input}) = \text{PLL0}/\text{VCO} \times 1/2$ $= (\text{PLL0 reference clock}) \times (\text{setting} + 1)$  0111111: $\times 64$ 1000000: $\times 65$ (Ex: 20 MHz $\times 65 = 1300$ MHz ) : 1000101: $\times 70$ (Ex: 20 MHz $\times 70 = 1400$ MHz ) 1001010: $\times 75$ ((Ex: 20 MHz $\times 75 = 1500$ MHz ) [RZ/G1M and RZ/G1N] 1101010: $\times 107$ (Ex: 13 MHz $\times 107 = 1391$ MHz )  [RZ/G1H] Set the PLL circuit 0 frequency (PLL0 output frequency) between 1250 MHz to 1400 MHz. [RZ/G1M and RZ/G1N] Set the PLL circuit 0 frequency (PLL0 output frequency) between 1250 MHz to 1500 MHz.
23 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12	—	MD14	R	Reserved This bit is always read as the same value with MD14. The write value should always be the same value with MD14.

Bit	Bit Name	Initial Value	R/W	Description
11 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	—	1	R	Reserved These bits are always read as 1. The write value should always be 1.
7 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

- Notes:
1. Initial value of STC[6:0] is determined by MD14 and MD13 as shown in Table 7.6.
  2. Actual multiplication ratio of PLL0 VCO to the reference clock of PLL0 is  $(\text{setting} + 1) \times 2$ . The factor "2" is derived from the fixed divider in the PLL feedback loop. The input clock to the SYS-CPU divider 1 is generated by dividing PLL0 VCO by 2. That is why the input clock frequency to the SYS-CPU divider 1 is expressed as  $(\text{STC}[6:0] + 1) \times (\text{reference clock of PLL0})$ .



### 7.5.5 RGX Control Register (RGXCR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

RGXCR is a 32-bit readable/writable register. This register enables/disables the external logic for SGX Series5.

[Usage Note]

Bit 16 in RGXCR should be set to 1 before enabling the GPU (3DG/3DGE) of the RZ/G1H, M and N.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SGXEX
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 17	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
16	SGXEX	0	R/W	Disable external logic for SGX Series5 0: Enable external logic for SGX Series5 1: Disable external logic for SGX Series5 Note: When using the GPU, set this bit to 1 before enabling the GPU.
15 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

### 7.5.6 SDHI Clock Frequency Control Register (SDCKCR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SDCKCR is a 32-bit readable/writable register. This register controls SDH clock (SDH $\phi$ ), SDHI0 clock (SD0 $\phi$ ) and SDHI1 clock (SD1 $\phi$ ) frequency. This register should be set before SDHI modules are operated. Do not access SDHI0 and SDHI1 modules during changing the clock frequency of SDH $\phi$ , SD0 $\phi$ , and SD1 $\phi$  or stopping these clocks.

#### [RZ/G1H]:

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	SDHFC[3:0]			SD0FC[3:0]			SD1FC[3:0]			—	—	—
Initial value:	1	1	1	1	0	0	0	0	0	1	1	0	0	1	1	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

#### [RZ/G1M/N/E]:

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	SDHFC[3:0]			SD0FC[3:0]			—	—	—	—	—	—
Initial value:	1	1	1	1	0	0	0	0	0	1	1	0	0	1	1	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 12	—	All 1	R	Reserved These bits are always read as 1. The write value should always be 1.

Bit	Bit Name	Initial Value	R/W	Description
11 to 8	SDHFC [3:0]	0000	R/W	SDH clock (SDH $\phi$ ) Frequency Division Ratio 0000: $\times 1/2$ 0001: $\times 1/3$ 0010: $\times 1/4$ 0011: $\times 1/6$ 0100: $\times 1/8$ 0101: $\times 1/12$ 0110: $\times 1/16$ 0111: $\times 1/18$ 1000: $\times 1/24$ 1010: $\times 1/36$ 1011: $\times 1/48$ Other values: Setting prohibited
7 to 4	SD0FC [3:0]	0110	R/W	SDHI0 clock (SD0 $\phi$ ) Frequency Division Ratio 0100: $\times 1/8$ 1100: $\times 1/10$ 0101: $\times 1/12$ 0110: $\times 1/16$ 0111: $\times 1/18$ 1000: $\times 1/24$ 1010: $\times 1/36$ 1011: $\times 1/48$ Other values: Setting prohibited
3 to 0	SD1FC [3:0]	0110	R/W	SDHI1 clock (SD1 $\phi$ ) Frequency Division Ratio [RZ/G1H] 0100: $\times 1/8$ 1100: $\times 1/10$ 0101: $\times 1/12$ 0110: $\times 1/16$ 0111: $\times 1/18$ 1000: $\times 1/24$ 1010: $\times 1/36$ 1011: $\times 1/48$ Other values: Setting prohibited
—		0110	R	Reserved [RZ/G1M/N/E] These bits are always read as 0110. The write value should always be 0110.

### 7.5.7 SDHI2 Clock Frequency Control Register (SD2CKCR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SD2CKCR is a 32-bit readable/writable register. This register controls SDHI2 clock (SD2 $\phi$ ) frequency. Do not access SDHI2 module during changing the clock frequency of SD2 $\phi$  or stopping this clock.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	—	—	—	—	—	—	—	CKSTP	—	—	DIV[5:0]						
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
R/W:	R	R	R	R	R	R	R	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	CKSTP	0	R/W	Clock Stop 0: Supplies SDHI2 clock 1: Stops SDHI2 clock
7, 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5 to 0	DIV[5:0]	001111	R/W	Division Ratio These bits set the frequency division ratio of SDHI2 clock divider. The clock source is divided by the division ratio of 1/(setting + 1).

**7.5.8 SDHI3 Clock Frequency Control Register (SD3CKCR)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SD3CKCR is a 32-bit readable/writable register. This register controls SDHI3 clock (SD3φ) frequency. Do not access SDHI3 module during changing the clock frequency of SD3φ or stopping this clock.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	—	—	—	—	—	—	—	CKSTP	—	—	DIV[5:0]						
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
R/W:	R	R	R	R	R	R	R	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	CKSTP	0	R/W	Clock Stop 0: Supplies SDHI3 clock 1: Stops SDHI3 clock
7, 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5 to 0	DIV[5:0]	001111	R/W	Division Ratio These bits set the frequency division ratio of SDHI3 clock divider. The clock source is divided by the division ratio of 1/(setting + 1).

**7.5.9 MMC0 Clock Frequency Control Register (MMC0CKCR)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

MMC0CKCR is a 32-bit readable/writable register. This register controls MMC0 clock (MMC0φ) frequency. Do not access MMC0 module during changing the clock frequency of MMC0φ or stopping this clock.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	CKSTP	—	—	DIV[5:0]					
Initial value:	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
R/W:	R	R	R	R	R	R	R	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	CKSTP	0	R/W	Clock Stop 0: Supplies MMC0 clock 1: Stops MMC0 clock
7, 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5 to 0	DIV[5:0]	111111	R/W	Division Ratio These bits set the frequency division ratio of MMC0 clock divider. The clock source is divided by the division ratio of 1/(setting + 1).

**7.5.10 MMC1 Clock Frequency Control Register (MMC1CKCR)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	—	—	—

MMC1CKCR is a 32-bit readable/writable register that controls MMC1 clock (MMC1φ) frequency. Do not access MMC1 module during changing the clock frequency of MMC1φ or stopping this clock.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	CKSTP	—	—	DIV[5:0]					
Initial value:	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
R/W:	R	R	R	R	R	R	R	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	CKSTP	0	R/W	Clock Stop 0: Supplies MMC1 clock 1: Stops MMC1 clock
7, 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5 to 0	DIV[5:0]	111111	R/W	Division Ratio These bits set the frequency division ratio of MMC1 clock divider. The clock source is divided by the division ratio of 1/(setting + 1).

### 7.5.11 GPU Clock Frequency Control Register (GPUCKCR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
—	√	√	—

GPUCKCR is a 32-bit readable/writable register. This register controls the input clock to the 3DG divider to create ZGφ. This register should be modified before using the GPU.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ZGCK SEL	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0/1	0	0	0	0	0	0	0	1	1	1	1	0	0	1	0
R/W:	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15	ZGCKSEL	0/1	R/W	Clock Select Selects clock source of GPU clock 0: $(PLL1/VCO \times 1/2) \times 1/3$ (initial value for [M]; setting prohibited for [N]) 1: $(PLL1/VCO \times 1/2) \times 1/5$ (initial value for [N])
14 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7 to 4	—	All 1	R	Reserved These bits are always read as 1. The write value should always be 1.
3, 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	—	1	R	Reserved This bit is always read as 1. The write value should always be 1.
0	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.



**7.5.12 RCAN Clock Frequency Control Register (RCANCKCR)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

RCANCKCR is a 32-bit readable/writable register. This register controls the RCAN clock.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	CKSTP	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1
R/W:	R	R	R	R	R	R	R	R/W	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	CKSTP	1	R/W	Clock Stop 0: Supplies clock to RCAN 1: Stops clock to RCAN
7 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	—	1	R	Reserved This bit is always read as 1. The write value should always be 1.

## 7.6 Changing Frequency

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

### [RZ/G1H/M/N]:

The clock frequencies controlled by the frequency control registers can be changed either by changing the multiplication ratio of PLL circuits 0 or by changing the division ratio of the dividers. They are controlled by software through the frequency control registers. The methods are described below.

### [RZ/G1E]:

The clock frequencies controlled by the frequency control registers can be changed by changing the division ratio of the dividers. They are controlled by software through the frequency control registers. The methods are described below.

### 7.6.1 Changing Multiplication Ratio of PLL circuit 0

#### [RZ/G1H/M/N]:

Changing the multiplication ratio of PLL circuit 0 can be done by modifying the STC [6:0] bits in PLL0CR. The PLL oscillation settling time is internally detected automatically. If the oscillation of PLL circuits is settled, 1 can be read through PLL0ST bit of PLLECR.

### 7.6.2 Changing Division Ratio

#### [RZ/G1H/M/N]:

Changing the frequency of  $Z\phi$ ,  $ZT\phi$ ,  $ZTR\phi$ , and  $ZTRD2\phi$  can be done by modifying each set of bits for setting the division ratio in FRQCRB and FRQCRC. After setting new ratio, write 1 to the KICK bit in FRQCRB to start the division ratio change. Before changing the division ratio, the KICK bit must be checked for 0. After 1 is written to the KICK bit in FRQCRB, 0 can be read when the change of new division ratio is completed. While the setting is being changed with the KICK bit being 1, do not modify FRQCRB and FRQCRC. When the KICK bit is read as 1, do not write 0 into the KICK bit.

#### [RZ/G1E]:

Changing the frequency of  $ZT\phi$ ,  $ZTR\phi$ , and  $ZTRD2\phi$  can be done by modifying each set of bits for setting the division ratio in FRQCRB. After setting new ratio, write 1 to the KICK bit in FRQCRB to start the division ratio change. Before changing the division ratio, the KICK bit must be checked for 0. After 1 is written to the KICK bit in FRQCRB, 0 can be read when the change of new division ratio is completed. While the setting is being changed with the KICK bit being 1, do not modify FRQCRB. When the KICK bit is read as 1, do not write 0 into the KICK bit.

## 7.7 Notes on Board Designing

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

### 7.7.1 Bypass Capacitor

Insert laminated ceramic capacitors as bypass capacitors for each  $V_{SS}/V_{CC}$  pair. Mount the bypass capacitor near the power supply pins of the LSI. Use components with a frequency characteristic suitable for the operating frequency of the LSI, as well as a suitable capacitance value.

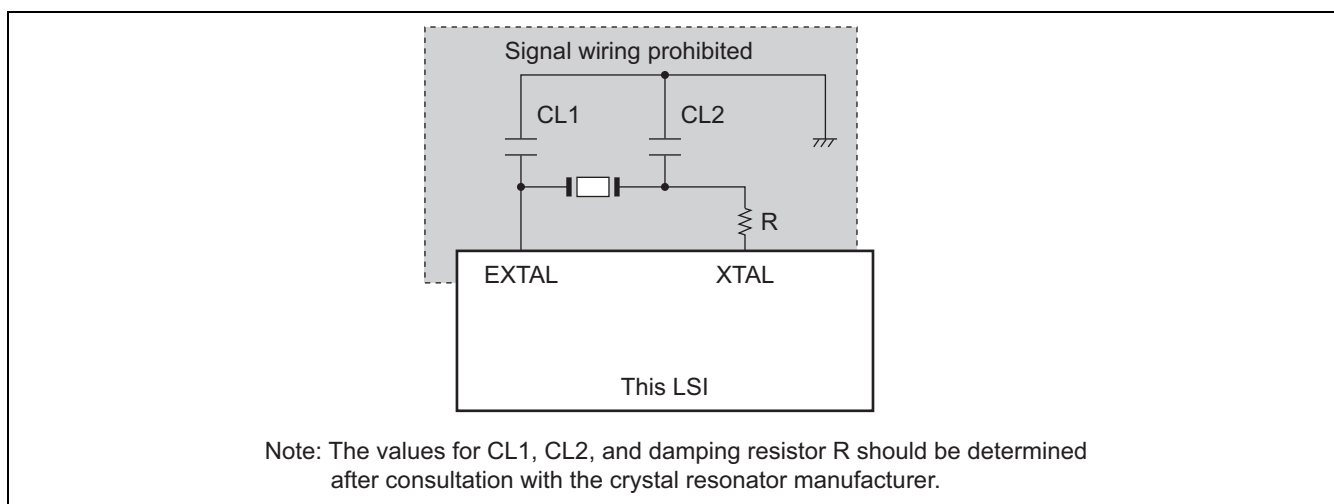
### 7.7.2 Notes on Using a PLL Oscillation Circuit

Keep the wiring from the PLL  $V_{DD}$  and  $V_{SS}$  connection pattern to the power supply pins short, and make the pattern width large, to minimize the inductance component.

The analog power supply system of the PLL circuits is sensitive to noise. Therefore system malfunction may occur by the intervention with another power supply. Do not supply the analog power supply with the same resource as the digital power supply of  $V_{DD}$  and  $V_{CCQ}$ .

### 7.7.3 When Using an External Crystal Resonator

Place the crystal resonator, capacitors CL1 and CL2, and damping resistor R as close to the XTAL, and EXTAL pins as possible. To minimize induction and thus obtain oscillation at the correct frequency, the capacitors to be attached to the resonator must be grounded to the same ground. Do not bring wiring patterns close to these components.



**Figure 7.3 Note on Using a Crystal Resonator**

### 7.7.4 When Supplying External Clock from EXTAL Pin

Leave the XTAL pin open.

## 7A. Module Standby and Software Reset

RZ/G1H	RZ/G1N
RZ/G1M	RZ/G1E

The CPG functions related to module control are explained in this section. Under software control, the CPG is capable of turning the supply of clock signals to individual modules on or off and of resetting individual modules.

### 7A.1 Features

- Module standby  
Clock supply to specified modules is stopped by setting the module stop control register bits.  
Two registers (MSTPSR and SMSTPCR) for one module, and supply of the clock signal to a module is stopped when all two register bits are set to 'stop'.
- Software Reset  
Initialize the specified module by setting the software reset register bit.

### 7A.2 Input/Output Pins

There is no input/output pin related with this function.

### 7A.3 Register Descriptions

Table 7A.1 lists of the CPG registers for module standby and software reset. Table 7A.2 lists the register states in response to a reset.

**Table 7A.1 Register Configurations**

Register Name	Abbreviation	R/W	Address	Access Size	RZ/G Series Products			
					RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Module stop status register 0	MSTPSR0	R	H'E615 0030	32	√	√	√	√
Module stop status register 1	MSTPSR1	R	H'E615 0038	32	√	√	√	√
Module stop status register 2	MSTPSR2	R	H'E615 0040	32	√	√	√	√
Module stop status register 3	MSTPSR3	R	H'E615 0048	32	√	√	√	√
Module stop status register 4	MSTPSR4	R	H'E615 004C	32	√	√	√	√
Module stop status register 5	MSTPSR5	R	H'E615 003C	32	√	√	√	√
Module stop status register 7	MSTPSR7	R	H'E615 01C4	32	√	√	√	√
Module stop status register 8	MSTPSR8	R	H'E615 09A0	32	√	√	√	√
Module stop status register 9	MSTPSR9	R	H'E615 09A4	32	√	√	√	√
Module stop status register 10	MSTPSR10	R	H'E615 09A8	32	√	√	√	√
Module stop status register 11	MSTPSR11	R	H'E615 09AC	32	√	√	√	√
System module stop control register 0	SMSTPCR0*	R/W	H'E615 0130	32	√	√	√	√
System module stop control register 1	SMSTPCR1*	R/W	H'E615 0134	32	√	√	√	√
System module stop control register 2	SMSTPCR2*	R/W	H'E615 0138	32	√	√	√	√
System module stop control register 3	SMSTPCR3*	R/W	H'E615 013C	32	√	√	√	√
System module stop control register 4	SMSTPCR4*	R/W	H'E615 0140	32	√	√	√	√
System module stop control register 5	SMSTPCR5*	R/W	H'E615 0144	32	√	√	√	√
System module stop control register 7	SMSTPCR7*	R/W	H'E615 014C	32	√	√	√	√
System module stop control register 8	SMSTPCR8*	R/W	H'E615 0990	32	√	√	√	√
System module stop control register 9	SMSTPCR9*	R/W	H'E615 0994	32	√	√	√	√
System module stop control register 10	SMSTPCR10*	R/W	H'E615 0998	32	√	√	√	√
System module stop control register 11	SMSTPCR11*	R/W	H'E615 099C	32	√	√	√	√
Software reset register 0	SRCR0	R/W	H'E615 00A0	32	√	√	√	√
Software reset register 1	SRCR1	R/W	H'E615 00A8	32	√	√	√	√
Software reset register 2	SRCR2	R/W	H'E615 00B0	32	√	√	√	√
Software reset register 3	SRCR3	R/W	H'E615 00B8	32	√	√	√	√
Software reset register 4	SRCR4	R/W	H'E615 00BC	32	√	√	√	√
Software reset register 5	SRCR5	R/W	H'E615 00C4	32	√	√	√	√
Software reset register 7	SRCR7	R/W	H'E615 01CC	32	√	√	√	√
Software reset register 8	SRCR8	R/W	H'E615 0920	32	√	√	√	√
Software reset register 9	SRCR9	R/W	H'E615 0924	32	√	√	√	√
Software reset register 10	SRCR10	R/W	H'E615 0928	32	√	√	√	√
Software reset register 11	SRCR11	R/W	H'E615 092C	32	√	√	√	√
Software reset clearing register 0	SRSTCLR0	W	H'E615 0940	32	√	√	√	√

Register Name	Abbreviation	R/W	Address	Access Size	RZ/G Series Products			
					RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Software reset clearing register 1	SRSTCLR1	W	H'E615 0944	32	√	√	√	√
Software reset clearing register 2	SRSTCLR2	W	H'E615 0948	32	√	√	√	√
Software reset clearing register 3	SRSTCLR3	W	H'E615 094C	32	√	√	√	√
Software reset clearing register 4	SRSTCLR4	W	H'E615 0950	32	√	√	√	√
Software reset clearing register 5	SRSTCLR5	W	H'E615 0954	32	√	√	√	√
Software reset clearing register 7	SRSTCLR7	W	H'E615 095C	32	√	√	√	√
Software reset clearing register 8	SRSTCLR8	W	H'E615 0960	32	√	√	√	√
Software reset clearing register 9	SRSTCLR9	W	H'E615 0964	32	√	√	√	√
Software reset clearing register 10	SRSTCLR10	W	H'E615 0968	32	√	√	√	√
Software reset clearing register 11	SRSTCLR11	W	H'E615 096C	32	√	√	√	√

Notes: Do not write to any addresses other than listed above. Operations cannot be guaranteed if writing is attempted. Values read from addresses other than those listed above are undefined.

\* SMSTPCRn are collectively indicated as MSTPCRn.

**Table 7A.2 Register States in Response to a Reset**

Register	Power-On Reset
All Registers	Initialized

### 7A.3.1 Module Stop Status Register (MSTPSRn (n = 0 to 5, 7 to 11))

MSTPSRn is a 32-bit readable register that indicates whether the on-chip modules are in the module standby state.

Setting a bit in this register to 1 stops supply of the clock signal to the corresponding module and the setting a bit to 0 enables clock supply to the corresponding module.

Positions, names and initial values of each bit are shown below. The Tables from 7A.3 to 7A.13 show the assignment of modules to bits.

**7A.3.1.1 Module Stop Status Register 0 (MSTPSR0)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	MSTP ST000
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

0: Supply of the clock signal to the corresponding module is enabled.

1: Supply of the clock signal to the corresponding module is stopped.

**Table 7A.3 Assignment of Modules to Bits in MSTPSR0**

Assignment of Modules to Bits in MSTPSR0			
Bit	RZ/G1H	RZ/G1M and RZ/G1N	RZ/G1E
31	—	—	—
30	—	—	—
29	—	—	—
28	—	—	—
27	—	—	—
26	—	—	—
25	—	—	—
24	—	—	—
23	—	—	—
22	—	—	—
21	—	—	—
20	—	—	—
19	—	—	—
18	—	—	—
17	—	—	—
16	—	—	—
15	—	—	—
14	—	—	—
13	—	—	—
12	—	—	—
11	—	—	—
10	—	—	—
9	—	—	—
8	—	—	—
7	—	—	—



Assignment of Modules to Bits in MSTPSR0

Bit	RZ/G1H	RZ/G1M and RZ/G1N	RZ/G1E
6	—	—	—
5	—	—	—
4	—	—	—
3	—	—	—
2	—	—	—
1	—	—	—
0	MSIOF0	MSIOF0	MSIOF0

Note: "—" indicates the bit is reserved. Set the value read from the bit.

## 7A.3.1.2 Module Stop Status Register 1 (MSTPSR1)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	MSTP ST131	—	—	MSTP ST128	MSTP ST127	—	MSTP ST125	MSTP ST124	—	MSTP ST122	MSTP ST121	—	MSTP ST119	MSTP ST118	MSTP ST117	—
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSTP ST115	—	—	MSTP ST112	MSTP ST111	—	—	MSTP ST108	—	MSTP ST106	—	—	MSTP ST103	MSTP ST102	MSTP ST101	MSTP ST100
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

0: Supply of the clock signal to the corresponding module is enabled.

1: Supply of the clock signal to the corresponding module is stopped.

Table 7A.4 Assignment of Modules to Bits in MSTPSR1

Assignment of Modules to Bits in MSTPSR1			
Bit	RZ/G1H	RZ/G1M and RZ/G1N	RZ/G1E
31	VSP1 (SY)	VSP1 (SY)	VSP1 (SY)
30	—	—	—
29	—	—	—
28	VSP1DU0	VSP1DU0	VSP1DU0
27	VSP1DU1	VSP1DU1	—
26	—	—	—
25	TMU0	TMU0	TMU0
24	CMT0	CMT0	CMT0
23	—	—	—
22	TMU2	TMU2	TMU2
21	TMU3	TMU3	TMU3
20	—	—	—
19	FDP1-0	FDP1-0	FDP1-0
18	FDP1-1	FDP1-1	—
17	FDP1-2	—	—
16	—	—	—
15	2D-DMAC	2D-DMAC	2D-DMAC
14	—	—	—
13	—	—	—
12	3DG	3DG	3DG
11	TMU1	TMU1	TMU1
10	—	—	—
9	—	—	—
8	—	TSIF0*1	—
7	—	—	—

Assignment of Modules to Bits in MSTPSR1

Bit	RZ/G1H	RZ/G1M and RZ/G1N	RZ/G1E
6	ADG (M2 $\phi$ )*2	ADG (M2 $\phi$ )*2	ADG (M2 $\phi$ )*2
5	—	—	—
4	—	—	—
3	VPC0	VPC0	VPC0
2	VPC1	—	—
1	VCP0	VCP0	VCP0
0	VCP1	—	—

Note: "—" indicates the bit is reserved. Set the value read from the bit.

1. Only for RZ/G1M.
2. This bit indicates the state of the clock signal (M2 $\phi$ ) for the ADG.

**7A.3.1.3 Module Stop Status Register 2 (MSTPSR2)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	MSTP ST219	MSTP ST218	—	MSTP ST216
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSTP ST215	—	—	—	—	—	—	MSTP ST208	MSTP ST207	MSTP ST206	MSTP ST205	MSTP ST204	MSTP ST203	MSTP ST202	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

0: Supply of the clock signal to the corresponding module is enabled.

1: Supply of the clock signal to the corresponding module is stopped.

**Table 7A.5 Assignment of Modules to Bits in MSTPSR2**

Assignment of Modules to Bits in MSTPSR2			
Bit	RZ/G1H	RZ/G1M and RZ/G1N	RZ/G1E
31	—	—	—
30	—	—	—
29	—	—	—
28	—	—	—
27	—	—	—
26	—	—	—
25	—	—	—
24	—	—	—
23	—	—	—
22	—	—	—
21	—	—	—
20	—	—	—
19	SYS-DMAC0	SYS-DMAC0	SYS-DMAC0
18	SYS-DMAC1	SYS-DMAC1	SYS-DMAC1
17	—	—	—
16	SCIFB2	SCIFB2	SCIFB2
15	MSIOF3	—	—
14	—	—	—
13	—	—	—
12	—	—	—
11	—	—	—
10	—	—	—
9	—	—	—
8	MSIOF1	MSIOF1	MSIOF1
7	SCIFB1	SCIFB1	SCIFB1

**Assignment of Modules to Bits in MSTPSR2**

<b>Bit</b>	<b>RZ/G1H</b>	<b>RZ/G1M and RZ/G1N</b>	<b>RZ/G1E</b>
6	SCIFB0	SCIFB0	SCIFB0
5	MSIOF2	MSIOF2	MSIOF2
4	SCIFA0	SCIFA0	SCIFA0
3	SCIFA1	SCIFA1	SCIFA1
2	SCIFA2	SCIFA2	SCIFA2
1	—	—	—
0	—	—	—

Note: "—" indicates the bit is reserved. Set the value read from the bit.

## 7A.3.1.4 Module Stop Status Register 3 (MSTPSR3)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	MSTP ST331	MSTP ST330	MSTP ST329	MSTP ST328	—	—	—	—	MSTP ST323	—	—	—	MSTP ST319	MSTP ST318	—	—
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSTP ST315	MSTP ST314	MSTP ST313	MSTP ST312	MSTP ST311	—	—	—	—	—	MSTP ST305	MSTP ST304	—	—	—	MSTP ST300
Initial value:	1	1	1	1	1	1	1	1	*	*	1	1	1	1	1	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

0: Supply of the clock signal to the corresponding module is enabled.

1: Supply of the clock signal to the corresponding module is stopped.

Note: \* Undefined. The read value of bits 7 and 6 is always undefined.

Table 7A.6 Assignment of Modules to Bits in MSTPSR3

Bit	Assignment of Modules to Bits in MSTPSR3		
	RZ/G1H	RZ/G1M and RZ/G1N	RZ/G1E
31	USBHS-DMAC1	USBHS-DMAC1	USBHS-DMAC1
30	USBHS-DMAC0	USBHS-DMAC0	USBHS-DMAC0
29	CMT1	CMT1	CMT1
28	USB3.0	USB3.0	—
27	—	—	—
26	—	—	—
25	—	—	—
24	—	—	—
23	IIC1	IIC1	IIC1
22	—	—	—
21	—	—	—
20	—	—	—
19	PCIEC	PCIEC	—
18	IIC0	IIC0	IIC0
17	—	—	—
16	—	—	—
15	MMC0	MMC0	MMC0
14	SDHI0	SDHI0	SDHI0
13	SDHI1	—	—
12	SDHI2	SDHI2	SDHI2
11	SDHI3	SDHI3	SDHI3
10	SCIF2	—	—
9	—	—	—
8	—	—	—

Assignment of Modules to Bits in MSTPSR3

Bit	RZ/G1H	RZ/G1M and RZ/G1N	RZ/G1E
7	—	—	—
6	—	—	—
5	MMC1	—	—
4	TPU0	TPU0	TPU0
3	—	—	—
2	—	—	—
1	—	—	—
0	IIC2	—	—

Note: "—" indicates the bit is reserved. Set the value read from the bit.

**7A.3.1.5 Module Stop Status Register 4 (MSTPSR4)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	MSTP ST408	MSTP ST407	MSTP ST406	—	—	—	MSTP ST402	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

0: Supply of the clock signal to the corresponding module is enabled.

1: Supply of the clock signal to the corresponding module is stopped.

**Table 7A.7 Assignment of Modules to Bits in MSTPSR4**

Assignment of Modules to Bits in MSTPSR4			
Bit	RZ/G1H	RZ/G1M and RZ/G1N	RZ/G1E
31	—	—	—
30	—	—	—
29	—	—	—
28	—	—	—
27	—	—	—
26	—	—	—
25	—	—	—
24	—	—	—
23	—	—	—
22	—	—	—
21	—	—	—
20	—	—	—
19	—	—	—
18	—	—	—
17	—	—	—
16	—	—	—
15	—	—	—
14	—	—	—
13	—	—	—
12	—	—	—
11	—	—	—
10	—	—	—
9	—	—	—
8	INTC-SYS	INTC-SYS	INTC-SYS
7	IRQC	IRQC	IRQC



Assignment of Modules to Bits in MSTPSR4

Bit	RZ/G1H	RZ/G1M and RZ/G1N	RZ/G1E
6	—	USB DDM	USB DDM
5	—	—	—
4	—	—	—
3	—	—	—
2	RWDT	RWDT	RWDT
1	—	—	—
0	—	—	—

Note: "—" indicates the bit is reserved. Set the value read from the bit.

## 7A.3.1.6 Module Stop Status Register 5 (MSTPSR5)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	MSTP ST530	—	—	—	MSTP ST526	—	—	MSTP ST523	MSTP ST522	—	—	—	—	—	—
Initial value:	1	0	0	0	0	0	1	0	0	0	*	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	MSTP ST502	MSTP ST501	—
Initial value:	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

0: Supply of the clock signal to the corresponding module is enabled.

1: Supply of the clock signal to the corresponding module is stopped.

Note: \* Undefined. The read value of bit 21 is always undefined.

**Table 7A.8 Assignment of Modules to Bits in MSTPSR5**

Bit	Assignment of Modules to Bits in MSTPSR5		
	RZ/G1H	RZ/G1M and RZ/G1N	RZ/G1E
31	—	—	—
30	—	—	—
29	—	—	—
28	—	—	—
27	—	—	—
26	Public boot ROM	Public boot ROM	—
25	—	—	—
24	—	—	—
23	PWM	PWM	PWM
22	Thermal Sensor	Thermal Sensor	—
21	—	—	—
20	—	—	—
19	—	—	—
18	—	—	—
17	—	—	—
16	—	—	—
15	—	—	—
14	—	—	—
13	—	—	—
12	—	—	—
11	—	—	—
10	—	—	—
9	—	—	—
8	—	—	—

Assignment of Modules to Bits in MSTPSR5

Bit	RZ/G1H	RZ/G1M and RZ/G1N	RZ/G1E
7	—	—	—
6	—	—	—
5	—	—	—
4	—	—	—
3	—	—	—
2	Audio-DMAC0	Audio-DMAC0	Audio-DMAC0
1	Audio-DMAC1	Audio-DMAC1	—
0	—	—	—

Note: "—" indicates the bit is reserved. Set the value read from the bit.

**7A.3.1.7 Module Stop Status Register 7 (MSTPSR7)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	MSTP ST726	MSTP ST725	MSTP ST724	MSTP ST723	MSTP ST722	MSTP ST721	MSTP ST720	MSTP ST719	MSTP ST718	MSTP ST717	MSTP ST716
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSTP ST715	MSTP ST714	MSTP ST713	—	—	—	—	—	—	—	—	MSTP ST704	MSTP ST703	—	—	—
Initial value:	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

- 0: Supply of the clock signal to the corresponding module is enabled.
- 1: Supply of the clock signal to the corresponding module is stopped.

**Table 7A.9 Assignment of Modules to Bits in MSTPSR7**

Assignment of Modules to Bits in MSTPSR7			
Bit	RZ/G1H	RZ/G1M and RZ/G1N	RZ/G1E
31	—	—	—
30	—	—	—
29	—	—	—
28	—	—	—
27	—	—	—
26	LVDS0	LVDS0	—
25	LVDS1	—	—
24	DU0	DU0	DU0
23	DU1	DU1	DU1
22	DU2	—	—
21	SCIF0	SCIF0	SCIF0
20	SCIF1	SCIF1	SCIF1
19	—	SCIF2	SCIF2
18	—	SCIF3	SCIF3
17	HSCIF0	HSCIF0	HSCIF0
16	HSCIF1	HSCIF1	HSCIF1
15	—	SCIF4	SCIF4
14	—	SCIF5	SCIF5
13	—	HSCIF2	HSCIF2
12	—	—	—
11	—	—	—
10	—	—	—
9	—	—	—
8	—	—	—
7	—	—	—

Assignment of Modules to Bits in MSTPSR7

Bit	RZ/G1H	RZ/G1M and RZ/G1N	RZ/G1E
6	—	—	—
5	—	—	—
4	USBHS	USBHS	USBHS
3	USB (EHCI)	USB (EHCI)	USB (EHCI)
2	—	—	—
1	—	—	—
0	—	—	—

Note: "—" indicates the bit is reserved. Set the value read from the bit.

### 7A.3.1.8 Module Stop Status Register 8 (MSTPSR8)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	MSTP ST830	—	MSTP ST828	MSTP ST827	MSTP ST826	MSTP ST825	—*	MSTP ST823	MSTP ST822	MSTP ST821	MSTP ST820	—	—	—	—
Initial value:																
H:	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0
M/N:								1								
E:								1								
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSTP ST815	MSTP ST814	MSTP ST813	MSTP ST812	MSTP ST811	MSTP ST810	MSTP ST809	MSTP ST808	MSTP ST807	—	MSTP ST805	MSTP ST804	—	—	—	MSTP ST800
Initial value:	1	1	1	1	1	1	1	1	1	0	0	0	0	1	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Note: \* The initial value of bit 24 vary depending on the products.

0: Supply of the clock signal to the corresponding module is enabled.

1: Supply of the clock signal to the corresponding module is stopped.

**Table 7A.10 Assignment of Modules to Bits in MSTPSR8**

Assignment of Modules to Bits in MSTPSR8			
Bit	RZ/G1H	RZ/G1M and RZ/G1N	RZ/G1E
31	—	—	—
30	—	DCU	DCU
29	—	—	—
28	—	—	—
27	—	—	—
26	—	—	—
25	—	—	—
24	—	—	—
23	IMR-LSX2 0	—	—
22	IMR-LSX2 1	—	—
21	IMR-X2 0	—	—
20	IMR-X2 1	—	—
19	—	—	—
18	—	—	—
17	—	—	—
16	—	—	—
15	SATA0	SATA0	—
14	SATA1	SATA1	—
13	Ether	Ether	Ether
12	EtherAVB	EtherAVB	EtherAVB
11	VIN0	VIN0	VIN0

Assignment of Modules to Bits in MSTPSR8

Bit	RZ/G1H	RZ/G1M and RZ/G1N	RZ/G1E
10	VIN1	VIN1	VIN1
9	VIN2	VIN2	—
8	VIN3	—	—
7	R-GP2D	—	—
6	—	—	—
5	—	—	—
4	—	—	—
3	—	—	—
2	—	—	—
1	—	—	—
0	—	IPMMU-SGX	IPMMU-SGX

Note: "—" indicates the bit is reserved. Set the value read from the bit.

**7A.3.1.9 Module Stop Status Register 9 (MSTPSR9)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	MSTP ST931	MSTP ST930	MSTP ST929	MSTP ST928	MSTP ST927	MSTP ST926	MSTP ST925	—	—	—	—	—	—	—	MSTP ST917	MSTP ST916
Initial value:	0	0	0	0	0	0	0	1	1	1	0	1	0	1	0	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSTP ST915	—	—	MSTP ST912	MSTP ST911	MSTP ST910	MSTP ST909	MSTP ST908	MSTP ST907	—	MSTP ST905	MSTP ST904	—	—	—	—
Initial value:	1	1	1	0	0	0	0	0	0	1	0	0	0	1	1	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

0: Supply of the clock signal to the corresponding module is enabled.

1: Supply of the clock signal to the corresponding module is stopped.

**Table 7A.11 Assignment of Modules to Bits in MSTPSR9**

Assignment of Modules to Bits in MSTPSR9			
Bit	RZ/G1H	RZ/G1M and RZ/G1N	RZ/G1E
31	I2C0	I2C0	I2C0
30	I2C1	I2C1	I2C1
29	I2C2	I2C2	I2C2
28	I2C3	I2C3	I2C3
27	—	I2C4	I2C4
26	IICDVFS	IICDVFS	—
25	—	I2C5	I2C5
24	—	—	—
23	—	—	—
22	—	—	—
21	—	—	—
20	—	—	—
19	—	—	—
18	—	—	—
17	QSPI	QSPI	QSPI
16	CAN0	CAN0	CAN0
15	CAN1	CAN1	CAN1
14	—	—	—
13	—	—	—
12	GPIO0	GPIO0	GPIO0
11	GPIO1	GPIO1	GPIO1
10	GPIO2	GPIO2	GPIO2
9	GPIO3	GPIO3	GPIO3
8	GPIO4	GPIO4	GPIO4
7	GPIO5	GPIO5	GPIO5



Assignment of Modules to Bits in MSTPSR9

Bit	RZ/G1H	RZ/G1M and RZ/G1N	RZ/G1E
6	—	—	—
5	—	GPIO6	GPIO6
4	—	GPIO7	—
3	—	—	—
2	—	—	—
1	—	—	—
0	—	—	—

Note: "—" indicates the bit is reserved. Set the value read from the bit.

### 7A.3.1.10 Module Stop Status Register 10 (MSTPSR10)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	MSTP ST1031	MSTP ST1030	MSTP ST1029	MSTP ST1028	MSTP ST1027	MSTP ST1026	MSTP ST1025	MSTP ST1024	MSTP ST1023	MSTP ST1022	MSTP ST1021	MSTP ST1020	MSTP ST1019	MSTP ST1018	MSTP ST1017	—
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSTP ST1015	MSTP ST1014	MSTP ST1013	MSTP ST1012	MSTP ST1011	MSTP ST1010	MSTP ST1009	MSTP ST1008	MSTP ST1007	MSTP ST1006	MSTP ST1005	—	—	—	—	—
Initial value:	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

0: Supply of the clock signal to the corresponding module is enabled.

1: Supply of the clock signal to the corresponding module is stopped.

**Table 7A.12 Assignment of Modules to Bits in MSTPSR10**

Assignment of Modules to Bits in MSTPSR10			
Bit	RZ/G1H	RZ/G1M and RZ/G1N	RZ/G1E
31	SCU (SRC0)	SCU (SRC0)	—
30	SCU (SRC1)	SCU (SRC1)	SCU (SRC1)
29	SCU (SRC2)	SCU (SRC2)	SCU (SRC2)
28	SCU (SRC3)	SCU (SRC3)	SCU (SRC3)
27	SCU (SRC4)	SCU (SRC4)	SCU (SRC4)
26	SCU (SRC5)	SCU (SRC5)	SCU (SRC5)
25	SCU (SRC6)	SCU (SRC6)	SCU (SRC6)
24	SCU (SRC7)	SCU (SRC7)	—
23	SCU (SRC8)	SCU (SRC8)	—
22	SCU (SRC9)	SCU (SRC9)	—
21	SCU (CTU00, CTU01, CTU02, CTU03, MIX0)	SCU (CTU00, CTU01, CTU02, CTU03, MIX0)	SCU (CTU00, CTU01, CTU02, CTU03, MIX0)
20	SCU (CTU10, CTU11, CTU12, CTU13, MIX1)	SCU (CTU10, CTU11, CTU12, CTU13, MIX1)	SCU (CTU10, CTU11, CTU12, CTU13, MIX1)
19	SCU (DVC0)	SCU (DVC0)	SCU (DVC0)
18	SCU (DVC1)	SCU (DVC1)	SCU (DVC1)
17	SCU (all)*1	SCU (all)*1	SCU (all)*1
16	—	—	—
15	SSI0	SSI0	SSI0
14	SSI1	SSI1	SSI1
13	SSI2	SSI2	SSI2
12	SSI3	SSI3	SSI3
11	SSI4	SSI4	SSI4
10	SSI5	SSI5	SSI5
9	SSI6	SSI6	SSI6
8	SSI7	SSI7	SSI7

Assignment of Modules to Bits in MSTPSR10

Bit	RZ/G1H	RZ/G1M and RZ/G1N	RZ/G1E
7	SSI8	SSI8	SSI8
6	SSI9	SSI9	SSI9
5	SSI (all)*2	SSI (all)*2	SSI (all)*2
4	—	—	—
3	—	—	—
2	—	—	—
1	—	—	—
0	—	—	—

Notes: "—" indicates the bit is reserved. Set the value read from the bit.

1. When the MSTP1017 bit is set to 1, supply of the clock signal to the circuits assigned to bits MSTP1031 to MSTP1018 is stopped simultaneously without writing 1 to these bits. When supply of the clock signal to any of the circuits assigned to bits MSTP1031 to MSTP1018 is to be enabled, clear the MSTP1017 bit.
2. When the MSTP1005 bit is set to 1, supply of the clock signal to the SSI0 to SSI9 modules is stopped simultaneously without setting bits MSTP1015 to MSTP1006 to 1. When supply of the clock signal to any of the SSI0 to SSI9 modules is to be enabled, clear the MSTP1005 bit.

**7A.3.1.11 Module Stop Status Register 11 (MSTPSR11)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	MSTPST 1108*	MSTPST 1107*	MSTPST 1106*	—	—	—	—	—	—
Initial value:																
H:	0	0	0	0	0	0	0	0	0	0	1	1	0	1	1	1
M/N:								1	1	1						
E:								1	1	1						
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Note: \* The initial values of bits 8 to 6 vary depending on the products.

0: Supply of the clock signal to the corresponding module is enabled.

1: Supply of the clock signal to the corresponding module is stopped.

**Table 7A.13 Assignment of Modules to Bits in MSTPSR11**

Bit	Assignment of Modules to Bits in MSTPSR11		
	RZ/G1H	RZ/G1M and RZ/G1N	RZ/G1E
31	—	—	—
30	—	—	—
29	—	—	—
28	—	—	—
27	—	—	—
26	—	—	—
25	—	—	—
24	—	—	—
23	—	—	—
22	—	—	—
21	—	—	—
20	—	—	—
19	—	—	—
18	—	—	—
17	—	—	—
16	—	—	—
15	—	—	—
14	—	—	—
13	—	—	—
12	—	—	—
11	—	—	—

Assignment of Modules to Bits in MSTPSR11

Bit	RZ/G1H	RZ/G1M and RZ/G1N	RZ/G1E
10	—	—	—
9	—	—	—
8	—	SCIFA5	SCIFA5
7	—	SCIFA4	SCIFA4
6	—	SCIFA3	SCIFA3
5	—	—	—
4	—	—	—
3	—	—	—
2	—	—	—
1	—	—	—
0	—	—	—

Note: "—" indicates the bit is reserved. Set the value read from the bit.

### 7A.3.2 Module Stop Control Register (SMSTPCRn (n = 0 to 5, 7 to 11))

SMSTPCRn is 32-bit readable/writable register which control supply of the clock signal to the modules assigned to the corresponding bits. SMSTPCRn register is for the AP system CPU core. When the control bit in SMSTPCRn is set to 1 (halt), input of the clock signal to the module is halted (the module is on standby). When a corresponding control bit in SMSTPCRn is 0, the clock signal is supplied. Whether the module is stopped or not can be checked through a corresponding bit in MSTPSRn register.

Setting a bit in this register to 1 requests that the module be placed on standby and setting a bit to 0 requests that the module operate.

The reserved bits should be set to the values read from the bits. Positions, names and initial values of each bit are shown below. The Tables from 7A.14 to 7A.24 show the assignment of modules to bits.

**7A.3.2.1 System Module Stop Control Register 0 (SMSTPCR0)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	MSTP 000
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

0: Enables supply of the clock signal to the corresponding module.  
 1: Stops supply of the clock signal to the corresponding module.

**Table 7A.14 Assignment of Modules to Bits in SMSTPCR0**

Bit	Assignment of Modules to Bits in SMSTPCR0		
	RZ/G1H	RZ/G1M and RZ/G1N	RZ/G1E
31	—	—	—
30	—	—	—
29	—	—	—
28	—	—	—
27	—	—	—
26	—	—	—
25	—	—	—
24	—	—	—
23	—	—	—
22	—	—	—
21	—	—	—
20	—	—	—
19	—	—	—
18	—	—	—
17	—	—	—
16	—	—	—
15	—	—	—
14	—	—	—
13	—	—	—
12	—	—	—
11	—	—	—
10	—	—	—
9	—	—	—
8	—	—	—
7	—	—	—

Assignment of Modules to Bits in SMSTPCR0

Bit	RZ/G1H	RZ/G1M and RZ/G1N	RZ/G1E
6	—	—	—
5	—	—	—
4	—	—	—
3	—	—	—
2	—	—	—
1	—	—	—
0	MSIOF0	MSIOF0	MSIOF0

Note: "—" indicates the bit is reserved. Set the value read from the bit.



### 7A.3.2.2 System Module Stop Control Register 1 (SMSTPCR1)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	MSTP 131	—	—	MSTP 128	MSTP 127	—	MSTP 125	MSTP 124	—	MSTP 122	MSTP 121	—	MSTP 119	MSTP 118	MSTP 117	—
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W*	R	R/W	R/W*	R	R/W	R/W	R	R/W	R/W	R	R/W	R/W*	R/W*	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSTP 115	—	—	MSTP 112	MSTP 111	—	—	MSTP 108	—	MSTP 106	—	—	MSTP 103	MSTP 102	MSTP 101	MSTP 100
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R	R	R/W	R/W	R	R	R/W*	R	R/W*	R	R	R/W	R/W*	R/W	R/W*

0: Enables supply of the clock signal to the corresponding module.

1: Stops supply of the clock signal to the corresponding module.

Note: \* Writing to a bit is only possible if the product actually has the corresponding module.

**Table 7A.15 Assignment of Modules to Bits in SMSTPCR1**

Bit	Assignment of Modules to Bits in SMSTPCR1		
	RZ/G1H	RZ/G1M and RZ/G1N	RZ/G1E
31	VSP1 (SY)	VSP1 (SY)	VSP1 (SY)
30	—	—	—
29	—	—	—
28	VSP1DU0	VSP1DU0	VSP1DU0
27	VSP1DU1	VSP1DU1	—
26	—	—	—
25	TMU0	TMU0	TMU0
24	CMT0	CMT0	CMT0
23	—	—	—
22	TMU2	TMU2	TMU2
21	TMU3	TMU3	TMU3
20	—	—	—
19	FDP1-0	FDP1-0	FDP1-0
18	FDP1-1	FDP1-1	—
17	FDP1-2	—	—
16	—	—	—
15	2D-DMAC	2D-DMAC	2D-DMAC
14	—	—	—
13	—	—	—
12	3DG	3DG	3DG
11	TMU1	TMU1	TMU1
10	—	—	—
9	—	—	—
8	—	TSIF0*1	—

Assignment of Modules to Bits in SMSTPCR1

Bit	RZ/G1H	RZ/G1M and RZ/G1N	RZ/G1E
7	—	—	—
6	ADG (M2 $\phi$ )* <sup>2</sup>	ADG (M2 $\phi$ )* <sup>2</sup>	ADG (M2 $\phi$ )* <sup>2</sup>
5	—	—	—
4	—	—	—
3	VPC0	VPC0	VPC0
2	VPC1	—	—
1	VCP0	VCP0	VCP0
0	VCP1	—	—

Notes: "—" indicates the bit is reserved. Set the value read from the bit.

1. Only for RZ/G1M.
2. This bit indicates the state of the clock signal (M2 $\phi$ ) for the ADG.

**7A.3.2.3 System Module Stop Control Register 2 (SMSTPCR2)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	MSTP 219	MSTP 218	—	MSTP 216
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSTP 215	—	—	—	—	—	—	MSTP 208	MSTP 207	MSTP 206	MSTP 205	MSTP 204	MSTP 203	MSTP 202	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W*	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R

0: Enables supply of the clock signal to the corresponding module.

1: Stops supply of the clock signal to the corresponding module.

Note: \* Writing to a bit is only possible if the product actually has the corresponding module.

**Table 7A.16 Assignment of Modules to Bits in SMSTPCR2**

Bit	Assignment of Modules to Bits in SMSTPCR2		
	RZ/G1H	RZ/G1M and RZ/G1N	RZ/G1E
31	—	—	—
30	—	—	—
29	—	—	—
28	—	—	—
27	—	—	—
26	—	—	—
25	—	—	—
24	—	—	—
23	—	—	—
22	—	—	—
21	—	—	—
20	—	—	—
19	SYS-DMAC0	SYS-DMAC0	SYS-DMAC0
18	SYS-DMAC1	SYS-DMAC1	SYS-DMAC1
17	—	—	—
16	SCIFB2	SCIFB2	SCIFB2
15	MSIOF3	—	—
14	—	—	—
13	—	—	—
12	—	—	—
11	—	—	—
10	—	—	—
9	—	—	—
8	MSIOF1	MSIOF1	MSIOF1

**Assignment of Modules to Bits in SMSTPCR2**

<b>Bit</b>	<b>RZ/G1H</b>	<b>RZ/G1M and RZ/G1N</b>	<b>RZ/G1E</b>
7	SCIFB1	SCIFB1	SCIFB1
6	SCIFB0	SCIFB0	SCIFB0
5	MSIOF2	MSIOF2	MSIOF2
4	SCIFA0	SCIFA0	SCIFA0
3	SCIFA1	SCIFA1	SCIFA1
2	SCIFA2	SCIFA2	SCIFA2
1	—	—	—
0	—	—	—

Notes: "—" indicates the bit is reserved. Set the value read from the bit.

**7A.3.2.4 System Module Stop Control Register 3 (SMSTPCR3)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	MSTP 331	MSTP 330	MSTP 329	MSTP 328	—	—	—	—	MSTP 323	—	—	—	MSTP 319	MSTP 318	—	—
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W*	R	R	R	R	R/W	R	R	R	R/W*	R/W	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSTP 315	MSTP 314	MSTP 313	MSTP 312	MSTP 311	—	—	—	—	—	MSTP 305	MSTP 304	—	—	—	MSTP 300
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W*	R/W	R/W	R	R	R	R	R	R/W*	R/W	R	R	R	R/W*

0: Enables supply of the clock signal to the corresponding module.

1: Stops supply of the clock signal to the corresponding module.

Note: \* Writing to a bit is only possible if the product actually has the corresponding module.

**Table 7A.17 Assignment of Modules to Bits in SMSTPCR3**

Bit	Assignment of Modules to Bits in SMSTPCR3		
	RZ/G1H	RZ/G1M and RZ/G1N	RZ/G1E
31	USBHS-DMAC1	USBHS-DMAC1	USBHS-DMAC1
30	USBHS-DMAC0	USBHS-DMAC0	USBHS-DMAC0
29	CMT1	CMT1	CMT1
28	USB3.0	USB3.0	—
27	—	—	—
26	—	—	—
25	—	—	—
24	—	—	—
23	IIC1	IIC1	IIC1
22	—	—	—
21	—	—	—
20	—	—	—
19	PCIEC	PCIEC	—
18	IIC0	IIC0	IIC0
17	—	—	—
16	—	—	—
15	MMC0	MMC0	MMC0
14	SDHI0	SDHI0	SDHI0
13	SDHI1	—	—
12	SDHI2	SDHI2	SDHI2
11	SDHI3	SDHI3	SDHI3
10	SCIF2	—	—
9	—	—	—
8	—	—	—

Assignment of Modules to Bits in SMSTPCR3

Bit	RZ/G1H	RZ/G1M and RZ/G1N	RZ/G1E
7	—	—	—
6	—	—	—
5	MMC1	—	—
4	TPU0	TPU0	TPU0
3	—	—	—
2	—	—	—
1	—	—	—
0	IIC2	—	—

Note: "—" indicates the bit is reserved. Set the value read from the bit.

**7A.3.2.5 System Module Stop Control Register 4 (SMSTPCR4)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	MSTP 408	MSTP 407	MSTP 406	—	—	—	MSTP 402	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R/W	R/W*	R	R	R	R/W	R	R

0: Enables supply of the clock signal to the corresponding module.

1: Stops supply of the clock signal to the corresponding module.

Note: \* Writing to a bit is only possible if the product actually has the corresponding module.

**Table 7A.18 Assignment of Modules to Bits in SMSTPCR4**

Bit	Assignment of Modules to Bits in SMSTPCR4		
	RZ/G1H	RZ/G1M and RZ/G1N	RZ/G1E
31	—	—	—
30	—	—	—
29	—	—	—
28	—	—	—
27	—	—	—
26	—	—	—
25	—	—	—
24	—	—	—
23	—	—	—
22	—	—	—
21	—	—	—
20	—	—	—
19	—	—	—
18	—	—	—
17	—	—	—
16	—	—	—
15	—	—	—
14	—	—	—
13	—	—	—
12	—	—	—
11	—	—	—
10	—	—	—
9	—	—	—
8	INTC-SYS	INTC-SYS	INTC-SYS

**Assignment of Modules to Bits in SMSTPCR4**

Bit	RZ/G1H	RZ/G1M and RZ/G1N	RZ/G1E
7	IRQC	IRQC	IRQC
6	—	USB DDM	USB DDM
5	—	—	—
4	—	—	—
3	—	—	—
2	RWDT	RWDT	RWDT
1	—	—	—
0	—	—	—

Notes: "—" indicates the bit is reserved. Set the value read from the bit.



**7A.3.2.6 System Module Stop Control Register 5 (SMSTPCR5)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	MSTP 526	—	—	MSTP 523	MSTP 522	—	—	—	—	—	—
Initial value:	1	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0
R/W:	R	R/W	R	R	R	R/W*	R	R	R/W	R/W	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	MSTP 502	MSTP 501	—
Initial value:	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W*	R

0: Enables supply of the clock signal to the corresponding module.

1: Stops supply of the clock signal to the corresponding module.

Note: \* Writing to a bit is only possible if the product actually has the corresponding module.

**Table 7A.19 Assignment of Modules to Bits in SMSTPCR5**

Bit	Assignment of Modules to Bits in SMSTPCR5		
	RZ/G1H	RZ/G1M and RZ/G1N	RZ/G1E
31	—	—	—
30	—	—	—
29	—	—	—
28	—	—	—
27	—	—	—
26	Public boot ROM	Public boot ROM	—
25	—	—	—
24	—	—	—
23	PWM	PWM	PWM
22	Thermal Sensor	Thermal Sensor	—
21	—	—	—
20	—	—	—
19	—	—	—
18	—	—	—
17	—	—	—
16	—	—	—
15	—	—	—
14	—	—	—
13	—	—	—
12	—	—	—
11	—	—	—
10	—	—	—
9	—	—	—
8	—	—	—

Assignment of Modules to Bits in SMSTPCR5

Bit	RZ/G1H	RZ/G1M and RZ/G1N	RZ/G1E
7	—	—	—
6	—	—	—
5	—	—	—
4	—	—	—
3	—	—	—
2	Audio-DMAC0	Audio-DMAC0	Audio-DMAC0
1	Audio-DMAC1	Audio-DMAC1	—
0	—	—	—

Note: "—" indicates the bit is reserved. Set the value read from the bit.

**7A.3.2.7 System Module Stop Control Register 7 (SMSTPCR7)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	MSTP 726	MSTP 725	MSTP 724	MSTP 723	MSTP 722	MSTP 721	MSTP 720	MSTP 719	MSTP 718	MSTP 717	MSTP 716
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R	R	R	R	R	R/W*	R/W*	R/W	R/W*	R/W*	R/W	R/W	R/W*	R/W*	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSTP 715	MSTP 714	MSTP 713	—	—	—	—	—	—	—	—	MSTP 704	MSTP 703	—	—	—
Initial value:	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1
R/W:	R/W*	R/W*	R/W*	R	R	R	R	R	R	R	R	R/W	R/W	R	R	R

0: Enables supply of the clock signal to the corresponding module.

1: Stops supply of the clock signal to the corresponding module.

Note: \* Writing to a bit is only possible if the product actually has the corresponding module.

**Table 7A.20 Assignment of Modules to Bits in SMSTPCR7**

Bit	Assignment of Modules to Bits in SMSTPCR7		
	RZ/G1H	RZ/G1M and RZ/G1N	RZ/G1E
31	—	—	—
30	—	—	—
29	—	—	—
28	—	—	—
27	—	—	—
26	LVDS0	LVDS0	—
25	LVDS1	—	—
24	DU0	DU0	DU0
23	DU1	DU1	DU1
22	DU2	—	—
21	SCIF0	SCIF0	SCIF0
20	SCIF1	SCIF1	SCIF1
19	—	SCIF2	SCIF2
18	—	SCIF3	SCIF3
17	HSCIF0	HSCIF0	HSCIF0
16	HSCIF1	HSCIF1	HSCIF1
15	—	SCIF4	SCIF4
14	—	SCIF5	SCIF5
13	—	HSCIF2	HSCIF2
12	—	—	—
11	—	—	—
10	—	—	—
9	—	—	—
8	—	—	—

Assignment of Modules to Bits in SMSTPCR7

Bit	RZ/G1H	RZ/G1M and RZ/G1N	RZ/G1E
7	—	—	—
6	—	—	—
5	—	—	—
4	USBHS	USBHS	USBHS
3	USB (EHCI)	USB (EHCI)	USB (EHCI)
2	—	—	—
1	—	—	—
0	—	—	—

Note: "—" indicates the bit is reserved. Set the value read from the bit.

**7A.3.2.8 System Module Stop Control Register 8 (SMSTPCR8)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	MSTP 830	—	—	—	—	—	—	MSTP 823	MSTP 822	MSTP 821	MSTP 820	—	—	—	—
Initial value:	Bit 24 vary with the products.															
H:	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0
M/N:									1							
E:									1							
R/W:	R	R/W*	R	R	R	R	R	R	R/W	R/W*	R/W*	R/W*	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSTP 815	MSTP 814	MSTP 813	MSTP 812	MSTP 811	MSTP 810	MSTP 809	MSTP 808	MSTP 807	—	—	—	—	—	—	MSTP 800
Initial value:	1	1	1	1	1	1	1	1	1	0	0	0	0	1	0	0
R/W:	R/W*	R/W*	R/W	R/W	R/W	R/W	R/W*	R/W*	R/W*	R	R	R	R	R	R	R/W*

0: Enables supply of the clock signal to the corresponding module.

1: Stops supply of the clock signal to the corresponding module.

Note: \* Writing to a bit is only possible if the product actually has the corresponding module.

**Table 7A.21 Assignment of Modules to Bits in SMSTPCR8**

Bit	Assignment of Modules to Bits in SMSTPCR8		
	RZ/G1H	RZ/G1M and RZ/G1N	RZ/G1E
31	—	—	—
30	—	DCU	DCU
29	—	—	—
28	—	—	—
27	—	—	—
26	—	—	—
25	—	—	—
24	—	—	—
23	IMR-LSX2 0	—	—
22	IMR-LSX2 1	—	—
21	IMR-X2 0	—	—
20	IMR-X2 1	—	—
19	—	—	—
18	—	—	—
17	—	—	—
16	—	—	—
15	SATA0	SATA0	—
14	SATA1	SATA1	—
13	Ether	Ether	Ether
12	EtherAVB	EtherAVB	EtherAVB
11	VIN0	VIN0	VIN0
10	VIN1	VIN1	VIN1

Assignment of Modules to Bits in SMSTPCR8

Bit	RZ/G1H	RZ/G1M and RZ/G1N	RZ/G1E
9	VIN2	VIN2	—
8	VIN3	—	—
7	R-GP2D	—	—
6	—	—	—
5	—	—	—
4	—	—	—
3	—	—	—
2	—	—	—
1	—	—	—
0	—	IPMMU-SGX	IPMMU-SGX

Note: "—" indicates the bit is reserved. Set the value read from the bit.

## 7A.3.2.9 System Module Stop Control Register 9 (SMSTPCR9)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	MSTP 931	MSTP 930	MSTP 929	MSTP 928	MSTP 927	MSTP 926	MSTP 925	—	—	—	—	—	—	—	MSTP 917	MSTP 916
Initial value:	0	0	0	0	0	0	0	1	1	1	0	1	0	1	0	1
R/W:	R/W	R/W	R/W	R/W	R/W*	R/W*	R/W*	R	R	R	R	R	R	R	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSTP 915	—	—	MSTP 912	MSTP 911	MSTP 910	MSTP 909	MSTP 908	MSTP 907	—	MSTP 905	MSTP 904	—	—	—	—
Initial value:	1	1	1	0	0	0	0	0	0	1	0	0	0	1	1	1
R/W:	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W*	R/W*	R	R	R	R

0: Enables supply of the clock signal to the corresponding module.

1: Stops supply of the clock signal to the corresponding module.

Note: \* Writing to a bit is only possible if the product actually has the corresponding module.

Table 7A.22 Assignment of Modules to Bits in SMSTPCR9

Bit	Assignment of Modules to Bits in SMSTPCR9		
	RZ/G1H	RZ/G1M and RZ/G1N	RZ/G1E
31	I2C0	I2C0	I2C0
30	I2C1	I2C1	I2C1
29	I2C2	I2C2	I2C2
28	I2C3	I2C3	I2C3
27	—	I2C4	I2C4
26	IICDVFS	IICDVFS	—
25	—	I2C5	I2C5
24	—	—	—
23	—	—	—
22	—	—	—
21	—	—	—
20	—	—	—
19	—	—	—
18	—	—	—
17	QSPI	QSPI	QSPI
16	CAN0	CAN0	CAN0
15	CAN1	CAN1	CAN1
14	—	—	—
13	—	—	—
12	GPIO0	GPIO0	GPIO0
11	GPIO1	GPIO1	GPIO1
10	GPIO2	GPIO2	GPIO2
9	GPIO3	GPIO3	GPIO3
8	GPIO4	GPIO4	GPIO4

**Assignment of Modules to Bits in SMSTPCR9**

<b>Bit</b>	<b>RZ/G1H</b>	<b>RZ/G1M and RZ/G1N</b>	<b>RZ/G1E</b>
7	GPIO5	GPIO5	GPIO5
6	—	—	—
5	—	GPIO6	GPIO6
4	—	GPIO7	—
3	—	—	—
2	—	—	—
1	—	—	—
0	—	—	—

Note: "—" indicates the bit is reserved. Set the value read from the bit.



**7A.3.2.10 System Module Stop Control Register 10 (SMSTPCR10)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	MSTP 1031	MSTP 1030	MSTP 1029	MSTP 1028	MSTP 1027	MSTP 1026	MSTP 1025	MSTP 1024	MSTP 1023	MSTP 1022	MSTP 1021	MSTP 1020	MSTP 1019	MSTP 1018	MSTP 1017	—
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSTP 1015	MSTP 1014	MSTP 1013	MSTP 1012	MSTP 1011	MSTP 1010	MSTP 1009	MSTP 1008	MSTP 1007	MSTP 1006	MSTP 1005	—	—	—	—	—
Initial value:	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R

0: Enables supply of the clock signal to the corresponding module.  
 1: Stops supply of the clock signal to the corresponding module.

**Table 7A.23 Assignment of Modules to Bits in SMSTPCR10**

Assignment of Modules to Bits in SMSTPCR10			
Bit	RZ/G1H	RZ/G1M and RZ/G1N	RZ/G1E
31	SCU (SRC0)	SCU (SRC0)	—
30	SCU (SRC1)	SCU (SRC1)	SCU (SRC1)
29	SCU (SRC2)	SCU (SRC2)	SCU (SRC2)
28	SCU (SRC3)	SCU (SRC3)	SCU (SRC3)
27	SCU (SRC4)	SCU (SRC4)	SCU (SRC4)
26	SCU (SRC5)	SCU (SRC5)	SCU (SRC5)
25	SCU (SRC6)	SCU (SRC6)	SCU (SRC6)
24	SCU (SRC7)	SCU (SRC7)	—
23	SCU (SRC8)	SCU (SRC8)	—
22	SCU (SRC9)	SCU (SRC9)	—
21	SCU (CTU00, CTU01, CTU02, CTU03, MIX0)	SCU (CTU00, CTU01, CTU02, CTU03, MIX0)	SCU (CTU00, CTU01, CTU02, CTU03, MIX0)
20	SCU (CTU10, CTU11, CTU12, CTU13, MIX1)	SCU (CTU10, CTU11, CTU12, CTU13, MIX1)	SCU (CTU10, CTU11, CTU12, CTU13, MIX1)
19	SCU (DVC0)	SCU (DVC0)	SCU (DVC0)
18	SCU (DVC1)	SCU (DVC1)	SCU (DVC1)
17	SCU (all)*1	SCU (all)*1	SCU (all)*1
16	—	—	—
15	SSI0	SSI0	SSI0
14	SSI1	SSI1	SSI1
13	SSI2	SSI2	SSI2
12	SSI3	SSI3	SSI3
11	SSI4	SSI4	SSI4
10	SSI5	SSI5	SSI5
9	SSI6	SSI6	SSI6
8	SSI7	SSI7	SSI7

Assignment of Modules to Bits in SMSTPCR10

Bit	RZ/G1H	RZ/G1M and RZ/G1N	RZ/G1E
7	SSI8	SSI8	SSI8
6	SSI9	SSI9	SSI9
5	SSI (all)*2	SSI (all)*2	SSI (all)*2
4	—	—	—
3	—	—	—
2	—	—	—
1	—	—	—
0	—	—	—

Notes: "—" indicates the bit is reserved. Set the value read from the bit.

1. When the MSTP1017 bit is set to 1, supply of the clock signal to the circuits assigned to bits MSTP1031 to MSTP1018 is stopped simultaneously without writing 1 to these bits. When supply of the clock signal to any of the circuits assigned to bits MSTP1031 to MSTP1018 is to be enabled, clear the MSTP1017 bit.
2. When the MSTP1005 bit is set to 1, supply of the clock signal to the SSI0 to SSI9 modules is stopped simultaneously without setting bits MSTP1015 to MSTP1006 to 1. When supply of the clock signal to any of the SSI0 to SSI9 modules is to be enabled, clear the MSTP1005 bit.

**7A.3.2.11 System Module Stop Control Register 11 (SMSTPCR11)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	MSTP 1108	MSTP 1107	MSTP 1106	—	—	—	—	—	—
Initial value:	Bits 8, 7, and 6 vary with the products.															
H:	0	0	0	0	0	0	0	0	0	0	1	1	0	1	1	1
M/N:								1	1	1						
E:								1	1	1						
R/W:	R	R	R	R	R	R	R	R/W*	R/W*	R/W*	R	R	R	R	R	R

0: Enables supply of the clock signal to the corresponding module.

1: Stops supply of the clock signal to the corresponding module.

Note: \* Writing to a bit is only possible if the product actually has the corresponding module.

**Table 7A.24 Assignment of Modules to Bits in SMSTPCR11**

Bit	Assignment of Modules to Bits in SMSTPCR11		
	RZ/G1H	RZ/G1M and RZ/G1N	RZ/G1E
31	—	—	—
30	—	—	—
29	—	—	—
28	—	—	—
27	—	—	—
26	—	—	—
25	—	—	—
24	—	—	—
23	—	—	—
22	—	—	—
21	—	—	—
20	—	—	—
19	—	—	—
18	—	—	—
17	—	—	—
16	—	—	—
15	—	—	—
14	—	—	—
13	—	—	—
12	—	—	—
11	—	—	—

Assignment of Modules to Bits in SMSTPCR11

Bit	RZ/G1H	RZ/G1M and RZ/G1N	RZ/G1E
10	—	—	—
9	—	—	—
8	—	SCIFA5	SCIFA5
7	—	SCIFA4	SCIFA4
6	—	SCIFA3	SCIFA3
5	—	—	—
4	—	—	—
3	—	—	—
2	—	—	—
1	—	—	—
0	—	—	—

Note: "—" indicates the bit is reserved. Set the value read from the bit.

### 7A.3.3 Software Reset Register (SRCRn (n = 0 to 5, 7 to 11))

Each SRCRn is a 32-bit readable/writable register. Each effective bit is assigned to a module in the chip. Writing 1 to a given bit resets the corresponding module. Writing 1 to a given bit of the software reset clearing register (SRSTCLRn (n = 0 to 11)) clears the corresponding bit of SRCRn and releases the module from the reset state. SRCRn is written in a read-modify-write sequence but writing to SRSTCLRn can proceed by simply setting the target bits to 1. After writing 1 to a software reset bit in SRCRn, ensure that the module has actually been initialized by waiting for at least one cycle of the RCLK clock before writing 1 to the corresponding bit of SRSTCLRn to release the module from the reset state. Before applying a software reset to a module connected to the AXI, make sure that any data transfer to the module is complete.

Positions, names and initial values of each bit are shown below. The Tables from 7A.25 to 7A.35 show the assignment of modules to bits.

**7A.3.3.1 Software Reset Register 0 (SRCR0)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SRT 000
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

**Table 7A.25 Assignment of Modules to Bits in SRCR0**

Bit	Assignment of Modules to Bits in SRCR0		
	RZ/G1H	RZ/G1M and RZ/G1N	RZ/G1E
31	—	—	—
30	—	—	—
29	—	—	—
28	—	—	—
27	—	—	—
26	—	—	—
25	—	—	—
24	—	—	—
23	—	—	—
22	—	—	—
21	—	—	—
20	—	—	—
19	—	—	—
18	—	—	—
17	—	—	—
16	—	—	—
15	—	—	—
14	—	—	—
13	—	—	—
12	—	—	—
11	—	—	—
10	—	—	—
9	—	—	—
8	—	—	—
7	—	—	—
6	—	—	—
5	—	—	—
4	—	—	—

Assignment of Modules to Bits in SRCR0

Bit	RZ/G1H	RZ/G1M and RZ/G1N	RZ/G1E
3	—	—	—
2	—	—	—
1	—	—	—
0	MSIOF0	MSIOF0	MSIOF0

Note: "—" indicates the bit is reserved. Set the value read from the bit.

### 7A.3.3.2 Software Reset Register 1 (SRCR1)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SRT 131	—	—	SRT 128	SRT 127	—	SRT 125	SRT 124	—	SRT 122	SRT 121	—	SRT 119	SRT 118	SRT 117	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W*	R	R/W	R/W*	R	R/W	R/W	R	R/W	R/W	R	R/W	R/W*	R/W*	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SRT 115	—	—	SRT 112	SRT 111	—	—	SRT 108	—	—	—	—	SRT 103	SRT 102	SRT 101	SRT 100
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R/W	R/W	R	R	R/W*	R	R	R	R	R/W	R/W*	R/W	R/W*

Note: \* Writing to a bit is only possible if the product actually has the corresponding module.

**Table 7A.26 Assignment of Modules to Bits in SRCR1**

Bit	Assignment of Modules to Bits in SRCR1		
	RZ/G1H	RZ/G1M and RZ/G1N	RZ/G1E
31	VSP1 (SY)	VSP1 (SY)	VSP1 (SY)
30	—	—	—
29	—	—	—
28	VSP1DU0	VSP1DU0	VSP1DU0
27	VSP1DU1	VSP1DU1	—
26	—	—	—
25	TMU0	TMU0	TMU0
24	CMT0	CMT0	CMT0
23	—	—	—
22	TMU2	TMU2	TMU2
21	TMU3	TMU3	TMU3
20	—	—	—
19	FDP1-0	FDP1-0	FDP1-0
18	FDP1-1	FDP1-1	—
17	FDP1-2	—	—
16	—	—	—
15	2D-DMAC	2D-DMAC	2D-DMAC
14	—	—	—
13	—	—	—
12	3DG	3DG	3DG
11	TMU1	TMU1	TMU1
10	—	—	—
9	—	—	—
8	—	TSIF0*1	—
7	—	—	—
6	—	—	—



Assignment of Modules to Bits in SRCR1

Bit	RZ/G1H	RZ/G1M and RZ/G1N	RZ/G1E
5	—	—	—
4	—	—	—
3	VPC0	VPC0	VPC0
2	VPC1	—	—
1	VCP0	VCP0	VCP0
0	VCP1	—	—

Notes: "—" indicates the bit is reserved. Set the value read from the bit.

1. Only for RZ/G1M.

**7A.3.3.3 Software Reset Register 2 (SRCR2)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	SRT 219	SRT 218	—	SRT 216
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SRT 215	—	—	—	—	—	—	SRT 208	SRT 207	SRT 206	SRT 205	SRT 204	SRT 203	SRT 202	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W*	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R

Note: \* Writing to a bit is only possible if the product actually has the corresponding module.

**Table 7A.27 Assignment of Modules to Bits in SRCR2**

Bit	Assignment of Modules to Bits in SRCR2		
	RZ/G1H	RZ/G1M and RZ/G1N	RZ/G1E
31	—	—	—
30	—	—	—
29	—	—	—
28	—	—	—
27	—	—	—
26	—	—	—
25	—	—	—
24	—	—	—
23	—	—	—
22	—	—	—
21	—	—	—
20	—	—	—
19	SYS-DMAC0	SYS-DMAC0	SYS-DMAC0
18	SYS-DMAC1	SYS-DMAC1	SYS-DMAC1
17	—	—	—
16	SCIFB2	SCIFB2	SCIFB2
15	MSIOF3	—	—
14	—	—	—
13	—	—	—
12	—	—	—
11	—	—	—
10	—	—	—
9	—	—	—
8	MSIOF1	MSIOF1	MSIOF1
7	SCIFB1	SCIFB1	SCIFB1
6	SCIFB0	SCIFB0	SCIFB0

**Assignment of Modules to Bits in SRCR2**

Bit	RZ/G1H	RZ/G1M and RZ/G1N	RZ/G1E
5	MSIOF2	MSIOF2	MSIOF2
4	SCIFA0	SCIFA0	SCIFA0
3	SCIFA1	SCIFA1	SCIFA1
2	SCIFA2	SCIFA2	SCIFA2
1	—	—	—
0	—	—	—

Notes: "—" indicates the bit is reserved. Set the value read from the bit.

## 7A.3.3.4 Software Reset Register 3 (SRCR3)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SRT 331	SRT 330	SRT 329	SRT 328	—	—	—	—	SRT 323	—	—	—	SRT 319	SRT 318	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W*	R	R	R	R	R/W	R	R	R	R/W*	R/W	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SRT 315	SRT 314	SRT 313	SRT 312	SRT 311	—	—	—	—	—	SRT 305	SRT 304	—	—	—	SRT 300
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W*	R/W	R/W	R	R	R	R	R	R/W*	R/W	R	R	R	R/W*

Note: \* Writing to a bit is only possible if the product actually has the corresponding module.

Table 7A.28 Assignment of Modules to Bits in SRCR3

Bit	Assignment of Modules to Bits in SRCR3		
	RZ/G1H	RZ/G1M and RZ/G1N	RZ/G1E
31	USBHS-DMAC1	USBHS-DMAC1	USBHS-DMAC1
30	USBHS-DMAC0	USBHS-DMAC0	USBHS-DMAC0
29	CMT1	CMT1	CMT1
28	USB3.0	USB3.0	—
27	—	—	—
26	—	—	—
25	—	—	—
24	—	—	—
23	IIC1	IIC1	IIC1
22	—	—	—
21	—	—	—
20	—	—	—
19	PCIEC	PCIEC	—
18	IIC0	IIC0	IIC0
17	—	—	—
16	—	—	—
15	MMC0	MMC0	MMC0
14	SDHI0	SDHI0	SDHI0
13	SDHI1	—	—
12	SDHI2	SDHI2	SDHI2
11	SDHI3	SDHI3	SDHI3
10	SCIF2	—	—
9	—	—	—
8	—	—	—
7	—	—	—
6	—	—	—

Assignment of Modules to Bits in SRCR3

Bit	RZ/G1H	RZ/G1M and RZ/G1N	RZ/G1E
5	MMC1	—	—
4	TPU0	TPU0	TPU0
3	—	—	—
2	—	—	—
1	—	—	—
0	IIC2	—	—

Note: "—" indicates the bit is reserved. Set the value read from the bit.

**7A.3.3.5 Software Reset Register 4 (SRCR4)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	SRT 408	SRT 407	SRT 406	—	—	—	SRT 402	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R/W	R/W*	R	R	R	R/W	R	R

Note: \* Writing to a bit is only possible if the product actually has the corresponding module.

**Table 7A.29 Assignment of Modules to Bits in SRCR4**

Bit	Assignment of Modules to Bits in SRCR4		
	RZ/G1H	RZ/G1M and RZ/G1N	RZ/G1E
31	—	—	—
30	—	—	—
29	—	—	—
28	—	—	—
27	—	—	—
26	—	—	—
25	—	—	—
24	—	—	—
23	—	—	—
22	—	—	—
21	—	—	—
20	—	—	—
19	—	—	—
18	—	—	—
17	—	—	—
16	—	—	—
15	—	—	—
14	—	—	—
13	—	—	—
12	—	—	—
11	—	—	—
10	—	—	—
9	—	—	—
8	INTC-SYS	INTC-SYS	INTC-SYS
7	IRQC	IRQC	IRQC
6	—	USB DDM	USB DDM

Assignment of Modules to Bits in SRCR4

Bit	RZ/G1H	RZ/G1M and RZ/G1N	RZ/G1E
5	—	—	—
4	—	—	—
3	—	—	—
2	RWDT	RWDT	RWDT
1	—	—	—
0	—	—	—

Notes: "—" indicates the bit is reserved. Set the value read from the bit.

**7A.3.3.6 Software Reset Register 5 (SRCR5)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	SRT 523	SRT 522	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W*	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	SRT 508	—	—	—	—	—	SRT 502	SRT 501	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R	R	R	R	R	R/W	R/W*	R

Note: \* Writing to a bit is only possible if the product actually has the corresponding module.

**Table 7A.30 Assignment of Modules to Bits in SRCR5**

Bit	Assignment of Modules to Bits in SRCR5		
	RZ/G1H	RZ/G1M and RZ/G1N	RZ/G1E
31	—	—	—
30	—	—	—
29	—	—	—
28	—	—	—
27	—	—	—
26	—	—	—
25	—	—	—
24	—	—	—
23	PWM	PWM	PWM
22	Thermal Sensor	Thermal Sensor	—
21	—	—	—
20	—	—	—
19	—	—	—
18	—	—	—
17	—	—	—
16	—	—	—
15	—	—	—
14	—	—	—
13	—	—	—
12	—	—	—
11	—	—	—
10	—	—	—
9	—	—	—
8	SCU	SCU	SCU
7	—	—	—
6	—	—	—



Assignment of Modules to Bits in SRCR5

Bit	RZ/G1H	RZ/G1M and RZ/G1N	RZ/G1E
5	—	—	—
4	—	—	—
3	—	—	—
2	Audio-DMAC0	Audio-DMAC0	Audio-DMAC0
1	Audio-DMAC1	Audio-DMAC1	—
0	—	—	—

Note: "—" indicates the bit is reserved. Set the value read from the bit.

**7A.3.3.7 Software Reset Register 7 (SRCR7)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	SRT 726	SRT 725	SRT 724	—	—	SRT 721	SRT 720	SRT 719	SRT 718	SRT 717	SRT 716
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W*	R/W*	R/W	R	R	R/W	R/W	R/W*	R/W*	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SRT 715	SRT 714	SRT 713	—	—	—	—	—	—	—	—	SRT 704	SRT 703	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W*	R/W*	R/W*	R	R	R	R	R	R	R	R	R/W	R/W	R	R	R

Note: \* Writing to a bit is only possible if the product actually has the corresponding module.

**Table 7A.31 Assignment of Modules to Bits in SRCR7**

Bit	Assignment of Modules to Bits in SRCR7		
	RZ/G1H	RZ/G1M and RZ/G1N	RZ/G1E
31	—	—	—
30	—	—	—
29	—	—	—
28	—	—	—
27	—	—	—
26	LVDS0	LVDS0	—
25	LVDS1	—	—
24	DU0, DU1, DU2	DU0, DU1	DU0, DU1
23	—	—	—
22	—	—	—
21	SCIF0	SCIF0	SCIF0
20	SCIF1	SCIF1	SCIF1
19	—	SCIF2	SCIF2
18	—	SCIF3	SCIF3
17	HSCIF0	HSCIF0	HSCIF0
16	HSCIF1	HSCIF1	HSCIF1
15	—	SCIF4	SCIF4
14	—	SCIF5	SCIF5
13	—	HSCIF2	HSCIF2
12	—	—	—
11	—	—	—
10	—	—	—
9	—	—	—
8	—	—	—
7	—	—	—
6	—	—	—

**Assignment of Modules to Bits in SRCR7**

<b>Bit</b>	<b>RZ/G1H</b>	<b>RZ/G1M and RZ/G1N</b>	<b>RZ/G1E</b>
5	—	—	—
4	USBHS	USBHS	USBHS
3	USB (EHCI)	USB (EHCI)	USB (EHCI)
2	—	—	—
1	—	—	—
0	—	—	—

Note: "—" indicates the bit is reserved. Set the value read from the bit.

**7A.3.3.8 Software Reset Register 8 (SRCR8)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	SRT 823	SRT 822	SRT 821	SRT 820	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W*	R/W*	R/W*	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SRT 815	SRT 814	SRT 813	SRT 812	SRT 811	SRT 810	SRT 809	SRT 808	SRT 807	—	—	—	—	—	—	SRT 800
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W*	R/W*	R/W*	R/W	R/W	R/W	R/W*	R/W*	R/W*	R	R	R	R	R	R	R/W*

Note: \* Writing to a bit is only possible if the product actually has the corresponding module.

**Table 7A.32 Assignment of Modules to Bits in SRCR8**

Bit	Assignment of Modules to Bits in SRCR8		
	RZ/G1H	RZ/G1M and RZ/G1N	RZ/G1E
31	—	—	—
30	—	—	—
29	—	—	—
28	—	—	—
27	—	—	—
26	—	—	—
25	—	—	—
24	—	—	—
23	IMR-LSX2 0	—	—
22	IMR-LSX2 1	—	—
21	IMR-X2 0	—	—
20	IMR-X2 1	—	—
19	—	—	—
18	—	—	—
17	—	—	—
16	—	—	—
15	SATA0	SATA0	—
14	SATA1	SATA1	—
13	Ether	Ether	Ether
12	EtherAVB	EtherAVB	EtherAVB
11	VIN0	VIN0	VIN0
10	VIN1	VIN1	VIN1
9	VIN2	VIN2	—
8	VIN3	—	—
7	R-GP2D	—	—
6	—	—	—

Assignment of Modules to Bits in SRCR8

Bit	RZ/G1H	RZ/G1M and RZ/G1N	RZ/G1E
5	—	—	—
4	—	—	—
3	—	—	—
2	—	—	—
1	—	—	—
0	—	IPMMU-SGX	IPMMU-SGX

Note: "—" indicates the bit is reserved. Set the value read from the bit.

**7A.3.3.9 Software Reset Register 9 (SRCR9)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SRT 931	SRT 930	SRT 929	SRT 928	SRT 927	SRT 926	SRT 925	—	—	SRT 922	—	—	—	—	SRT 917	SRT 916
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W*	R/W*	R/W*	R	R	R/W	R	R	R	R	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SRT 915	—	—	SRT 912	SRT 911	SRT 910	SRT 909	SRT 908	SRT 907	—	SRT 905	SRT 904	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W*	R/W*	R	R	R	R

Note: \* Writing to a bit is only possible if the product actually has the corresponding module.

**Table 7A.33 Assignment of Modules to Bits in SRCR9**

Bit	Assignment of Modules to Bits in SRCR9		
	RZ/G1H	RZ/G1M and RZ/G1N	RZ/G1E
31	I2C0	I2C0	I2C0
30	I2C1	I2C1	I2C1
29	I2C2	I2C2	I2C2
28	I2C3	I2C3	I2C3
27	—	I2C4	I2C4
26	IICDVFS	IICDVFS	—
25	—	I2C5	I2C5
24	—	—	—
23	—	—	—
22	ADG	ADG	ADG
21	—	—	—
20	—	—	—
19	—	—	—
18	—	—	—
17	QSPI	QSPI	QSPI
16	CAN0	CAN0	CAN0
15	CAN1	CAN1	CAN1
14	—	—	—
13	—	—	—
12	GPIO0	GPIO0	GPIO0
11	GPIO1	GPIO1	GPIO1
10	GPIO2	GPIO2	GPIO2
9	GPIO3	GPIO3	GPIO3
8	GPIO4	GPIO4	GPIO4
7	GPIO5	GPIO5	GPIO5
6	—	—	—

Assignment of Modules to Bits in SRCR9

Bit	RZ/G1H	RZ/G1M and RZ/G1N	RZ/G1E
5	—	GPIO6	GPIO6
4	—	GPIO7	—
3	—	—	—
2	—	—	—
1	—	—	—
0	—	—	—

Note: "—" indicates the bit is reserved. Set the value read from the bit.

**7A.3.3.10 Software Reset Register 10 (SRCR10)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SRT 1015	SRT 1014	SRT 1013	SRT 1012	SRT 1011	SRT 1010	SRT 1009	SRT 1008	SRT 1007	SRT 1006	SRT 1005	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R

**Table 7A.34 Assignment of Modules to Bits in SRCR10**

Assignment of Modules to Bits in SRCR10			
Bit	RZ/G1H	RZ/G1M and RZ/G1N	RZ/G1E
31	—	—	—
30	—	—	—
29	—	—	—
28	—	—	—
27	—	—	—
26	—	—	—
25	—	—	—
24	—	—	—
23	—	—	—
22	—	—	—
21	—	—	—
20	—	—	—
19	—	—	—
18	—	—	—
17	—	—	—
16	—	—	—
15	SSI0	SSI0	SSI0
14	SSI1	SSI1	SSI1
13	SSI2	SSI2	SSI2
12	SSI3	SSI3	SSI3
11	SSI4	SSI4	SSI4
10	SSI5	SSI5	SSI5
9	SSI6	SSI6	SSI6
8	SSI7	SSI7	SSI7
7	SSI8	SSI8	SSI8
6	SSI9	SSI9	SSI9
5	SSI (all)	SSI (all)	SSI (all)
4	—	—	—



**Assignment of Modules to Bits in SRCR10**

Bit	RZ/G1H	RZ/G1M and RZ/G1N	RZ/G1E
3	—	—	—
2	—	—	—
1	—	—	—
0	—	—	—

Note: "—" indicates the bit is reserved. Set the value read from the bit.

**7A.3.3.11 Software Reset Register 11 (SRCR11)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	SRT 1108	SRT 1107	SRT 1106	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W*	R/W*	R/W*	R	R	R	R	R	R

Note: \* Writing to a bit is only possible if the product actually has the corresponding module.

**Table 7A.35 Assignment of Modules to Bits in SRCR11**

Bit	Assignment of Modules to Bits in SRCR11		
	RZ/G1H	RZ/G1M and RZ/G1N	RZ/G1E
31	—	—	—
30	—	—	—
29	—	—	—
28	—	—	—
27	—	—	—
26	—	—	—
25	—	—	—
24	—	—	—
23	—	—	—
22	—	—	—
21	—	—	—
20	—	—	—
19	—	—	—
18	—	—	—
17	—	—	—
16	—	—	—
15	—	—	—
14	—	—	—
13	—	—	—
12	—	—	—
11	—	—	—
10	—	—	—
9	—	—	—
8	—	SCIFA5	SCIFA5
7	—	SCIFA4	SCIFA4
6	—	SCIFA3	SCIFA3

Assignment of Modules to Bits in SRCR11

Bit	RZ/G1H	RZ/G1M and RZ/G1N	RZ/G1E
5	—	—	—
4	—	—	—
3	—	—	—
2	—	—	—
1	—	—	—
0	—	—	—

Note: "—" indicates the bit is reserved. Set the value read from the bit.

### 7A.3.4 Software Reset Clearing Register n (SRSTCLRn (n = 0 to 5, 7 to 11))

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Each SRSTCLRn is a 32-bit write-only register. Each effective bit is assigned to a module in this chip. Writing 1 to a given bit clears the corresponding bit of SRCRn and releases the corresponding module from the reset state in which it was placed by writing 1 to the bit of SRCRn. Write 0 to the reserved bits of these registers.

Positions, names and initial values of each bit are shown below. The Tables from 7A.35 to 7A.45 show the assignment of modules to bits.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SRTCL Rn31	SRTCL Rn30	SRTCL Rn29	SRTCL Rn28	SRTCL Rn27	SRTCL Rn26	SRTCL Rn25	SRTCL Rn24	SRTCL Rn23	SRTCL Rn22	SRTCL Rn21	SRTCL Rn20	SRTCL Rn19	SRTCL Rn18	SRTCL Rn17	SRTCL Rn16
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SRTCL Rn15	SRTCL Rn14	SRTCL Rn13	SRTCL Rn12	SRTCL Rn11	SRTCL Rn10	SRTCL Rn09	SRTCL Rn08	SRTCL Rn07	SRTCL Rn06	SRTCL Rn05	SRTCL Rn04	SRTCL Rn03	SRTCL Rn02	SRTCL Rn01	SRTCL Rn00
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

Table 7A.35 Assignment of Modules to Bits in SRSTCLR0

Bit	Assignment of Modules to Bits in SRSTCLR0		
	RZ/G1H	RZ/G1M and RZ/G1N	RZ/G1E
31	—	—	—
30	—	—	—
29	—	—	—
28	—	—	—
27	—	—	—
26	—	—	—
25	—	—	—
24	—	—	—
23	—	—	—
22	—	—	—
21	—	—	—
20	—	—	—
19	—	—	—
18	—	—	—
17	—	—	—
16	—	—	—
15	—	—	—
14	—	—	—
13	—	—	—
12	—	—	—
11	—	—	—
10	—	—	—
9	—	—	—
8	—	—	—
7	—	—	—
6	—	—	—
5	—	—	—
4	—	—	—
3	—	—	—
2	—	—	—
1	—	—	—
0	MSIOF0	MSIOF0	MSIOF0

Note: "—" indicates the bit is reserved. Set the value read from the bit.

**Table 7A.36** Assignment of Modules to Bits in SRSTCLR1

Bit	Assignment of Modules to Bits in SRSTCLR1		
	RZ/G1H	RZ/G1M and RZ/G1N	RZ/G1E
31	VSP1 (SY)	VSP1 (SY)	VSP1 (SY)
30	—	—	—
29	—	—	—
28	VSP1DU0	VSP1DU0	VSP1DU0
27	VSP1DU1	VSP1DU1	—
26	—	—	—
25	TMU0	TMU0	TMU0
24	CMT0	CMT0	CMT0
23	—	—	—
22	TMU2	TMU2	TMU2
21	TMU3	TMU3	TMU3
20	—	—	—
19	FDP1-0	FDP1-0	FDP1-0
18	FDP1-1	FDP1-1	—
17	FDP1-2	—	—
16	—	—	—
15	2D-DMAC	2D-DMAC	2D-DMAC
14	—	—	—
13	—	—	—
12	3DG	3DG	3DG
11	TMU1	TMU1	TMU1
10	—	—	—
9	—	—	—
8	—	TSIF0*1	—
7	—	—	—
6	—	—	—
5	—	—	—
4	—	—	—
3	VPC0	VPC0	VPC0
2	VPC1	—	—
1	VCP0	VCP0	VCP0
0	VCP1	—	—

Notes: "—" indicates the bit is reserved. Set the value read from the bit.

1. Only for RZ/G1M.

Table 7A.37 Assignment of Modules to Bits in SRSTCLR2

Bit	Assignment of Modules to Bits in SRSTCLR2		
	RZ/G1H	RZ/G1M and RZ/G1N	RZ/G1E
31	—	—	—
30	—	—	—
29	—	—	—
28	—	—	—
27	—	—	—
26	—	—	—
25	—	—	—
24	—	—	—
23	—	—	—
22	—	—	—
21	—	—	—
20	—	—	—
19	SYS-DMAC0	SYS-DMAC0	SYS-DMAC0
18	SYS-DMAC1	SYS-DMAC1	SYS-DMAC1
17	—	—	—
16	SCIFB2	SCIFB2	SCIFB2
15	MSIOF3	—	—
14	—	—	—
13	—	—	—
12	—	—	—
11	—	—	—
10	—	—	—
9	—	—	—
8	MSIOF1	MSIOF1	MSIOF1
7	SCIFB1	SCIFB1	SCIFB1
6	SCIFB0	SCIFB0	SCIFB0
5	MSIOF2	MSIOF2	MSIOF2
4	SCIFA0	SCIFA0	SCIFA0
3	SCIFA1	SCIFA1	SCIFA1
2	SCIFA2	SCIFA2	SCIFA2
1	—	—	—
0	—	—	—

Notes: "—" indicates the bit is reserved. Set the value read from the bit.

**Table 7A.38** Assignment of Modules to Bits in SRSTCLR3

Bit	Assignment of Modules to Bits in SRSTCLR3		
	RZ/G1H	RZ/G1M and RZ/G1N	RZ/G1E
31	USBHS-DMAC1	USBHS-DMAC1	USBHS-DMAC1
30	USBHS-DMAC0	USBHS-DMAC0	USBHS-DMAC0
29	CMT1	CMT1	CMT1
28	USB3.0	USB3.0	—
27	—	—	—
26	—	—	—
25	—	—	—
24	—	—	—
23	IIC1	IIC1	IIC1
22	—	—	—
21	—	—	—
20	—	—	—
19	PCIEC	PCIEC	—
18	IIC0	IIC0	IIC0
17	—	—	—
16	—	—	—
15	MMC0	MMC0	MMC0
14	SDHI0	SDHI0	SDHI0
13	SDHI1	—	—
12	SDHI2	SDHI2	SDHI2
11	SDHI3	SDHI3	SDHI3
10	SCIF2	—	—
9	—	—	—
8	—	—	—
7	—	—	—
6	—	—	—
5	MMC1	—	—
4	TPU0	TPU0	TPU0
3	—	—	—
2	—	—	—
1	—	—	—
0	IIC2	—	—

Note: "—" indicates the bit is reserved. Set the value read from the bit.



**Table 7A.39** Assignment of Modules to Bits in SRSTCLR4

Bit	Assignment of Modules to Bits in SRSTCLR4		
	RZ/G1H	RZ/G1M and RZ/G1N	RZ/G1E
31	—	—	—
30	—	—	—
29	—	—	—
28	—	—	—
27	—	—	—
26	—	—	—
25	—	—	—
24	—	—	—
23	—	—	—
22	—	—	—
21	—	—	—
20	—	—	—
19	—	—	—
18	—	—	—
17	—	—	—
16	—	—	—
15	—	—	—
14	—	—	—
13	—	—	—
12	—	—	—
11	—	—	—
10	—	—	—
9	—	—	—
8	INTC-SYS	INTC-SYS	INTC-SYS
7	IRQC	IRQC	IRQC
6	—	USB DDM	USB DDM
5	—	—	—
4	—	—	—
3	—	—	—
2	RWDT	RWDT	RWDT
1	—	—	—
0	—	—	—

Notes: "—" indicates the bit is reserved. Set the value read from the bit.

**Table 7A.40** Assignment of Modules to Bits in SRSTCLR5

Bit	Assignment of Modules to Bits in SRSTCLR5		
	RZ/G1H	RZ/G1M and RZ/G1N	RZ/G1E
31	—	—	—
30	—	—	—
29	—	—	—
28	—	—	—
27	—	—	—
26	—	—	—
25	—	—	—
24	—	—	—
23	PWM	PWM	PWM
22	Thermal Sensor	Thermal Sensor	—
21	—	—	—
20	—	—	—
19	—	—	—
18	—	—	—
17	—	—	—
16	—	—	—
15	—	—	—
14	—	—	—
13	—	—	—
12	—	—	—
11	—	—	—
10	—	—	—
9	—	—	—
8	SCU	SCU	SCU
7	—	—	—
6	—	—	—
5	—	—	—
4	—	—	—
3	—	—	—
2	Audio-DMAC0	Audio-DMAC0	Audio-DMAC0
1	Audio-DMAC1	Audio-DMAC1	—
0	—	—	—

Note: "—" indicates the bit is reserved. Set the value read from the bit.

Table 7A.41 Assignment of Modules to Bits in SRSTCLR7

Bit	Assignment of Modules to Bits in SRSTCLR7		
	RZ/G1H	RZ/G1M and RZ/G1N	RZ/G1E
31	—	—	—
30	—	—	—
29	—	—	—
28	—	—	—
27	—	—	—
26	LVDS0	LVDS0	—
25	LVDS1	—	—
24	DU0, DU1, DU2	DU0, DU1	DU0, DU1
23	—	—	—
22	—	—	—
21	SCIF0	SCIF0	SCIF0
20	SCIF1	SCIF1	SCIF1
19	—	SCIF2	SCIF2
18	—	SCIF3	SCIF3
17	HSCIF0	HSCIF0	HSCIF0
16	HSCIF1	HSCIF1	HSCIF1
15	—	SCIF4	SCIF4
14	—	SCIF5	SCIF5
13	—	HSCIF2	HSCIF2
12	—	—	—
11	—	—	—
10	—	—	—
9	—	—	—
8	—	—	—
7	—	—	—
6	—	—	—
5	—	—	—
4	USBHS	USBHS	USBHS
3	USB (EHCI)	USB (EHCI)	USB (EHCI)
2	—	—	—
1	—	—	—
0	—	—	—

Note: "—" indicates the bit is reserved. Set the value read from the bit.

**Table 7A.42** Assignment of Modules to Bits in SRSTCLR8

Bit	Assignment of Modules to Bits in SRSTCLR8		
	RZ/G1H	RZ/G1M and RZ/G1N	RZ/G1E
31	—	—	—
30	—	DCU	DCU
29	—	—	—
28	—	—	—
27	—	—	—
26	—	—	—
25	—	—	—
24	—	—	—
23	IMR-LSX2 0	—	—
22	IMR-LSX2 1	—	—
21	IMR-X2 0	—	—
20	IMR-X2 1	—	—
19	—	—	—
18	—	—	—
17	—	—	—
16	—	—	—
15	SATA0	SATA0	—
14	SATA1	SATA1	—
13	Ether	Ether	Ether
12	EtherAVB	EtherAVB	EtherAVB
11	VIN0	VIN0	VIN0
10	VIN1	VIN1	VIN1
9	VIN2	VIN2	—
8	VIN3	—	—
7	R-GP2D	—	—
6	—	—	—
5	—	—	—
4	—	—	—
3	—	—	—
2	—	—	—
1	—	—	—
0	—	IPMMU-SGX	IPMMU-SGX

Note: "—" indicates the bit is reserved. Set the value read from the bit.

**Table 7A.43** Assignment of Modules to Bits in SRSTCLR9

Bit	Assignment of Modules to Bits in SRSTCLR9		
	RZ/G1H	RZ/G1M and RZ/G1N	RZ/G1E
31	I2C0	I2C0	I2C0
30	I2C1	I2C1	I2C1
29	I2C2	I2C2	I2C2
28	I2C3	I2C3	I2C3
27	—	I2C4	I2C4
26	IICDVFS	IICDVFS	—
25	—	I2C5	I2C5
24	—	—	—
23	—	—	—
22	ADG	ADG	ADG
21	—	—	—
20	—	—	—
19	—	—	—
18	—	—	—
17	QSPI	QSPI	QSPI
16	CAN0	CAN0	CAN0
15	CAN1	CAN1	CAN1
14	—	—	—
13	—	—	—
12	GPIO0	GPIO0	GPIO0
11	GPIO1	GPIO1	GPIO1
10	GPIO2	GPIO2	GPIO2
9	GPIO3	GPIO3	GPIO3
8	GPIO4	GPIO4	GPIO4
7	GPIO5	GPIO5	GPIO5
6	—	—	—
5	—	GPIO6	GPIO6
4	—	GPIO7	—
3	—	—	—
2	—	—	—
1	—	—	—
0	—	—	—

Note: "—" indicates the bit is reserved. Set the value read from the bit.

**Table 7A.44** Assignment of Modules to Bits in SRSTCLR10

Bit	Assignment of Modules to Bits in SRSTCLR10		
	RZ/G1H	RZ/G1M and RZ/G1N	RZ/G1E
31	—	—	—
30	—	—	—
29	—	—	—
28	—	—	—
27	—	—	—
26	—	—	—
25	—	—	—
24	—	—	—
23	—	—	—
22	—	—	—
21	—	—	—
20	—	—	—
19	—	—	—
18	—	—	—
17	—	—	—
16	—	—	—
15	SSI0	SSI0	SSI0
14	SSI1	SSI1	SSI1
13	SSI2	SSI2	SSI2
12	SSI3	SSI3	SSI3
11	SSI4	SSI4	SSI4
10	SSI5	SSI5	SSI5
9	SSI6	SSI6	SSI6
8	SSI7	SSI7	SSI7
7	SSI8	SSI8	SSI8
6	SSI9	SSI9	SSI9
5	SSI (all)	SSI (all)	SSI (all)
4	—	—	—
3	—	—	—
2	—	—	—
1	—	—	—
0	—	—	—

Note: "—" indicates the bit is reserved. Set the value read from the bit.

**Table 7A.45** Assignment of Modules to Bits in SRSTCLR11

Bit	Assignment of Modules to Bits in SRSTCLR11		
	RZ/G1H	RZ/G1M and RZ/G1N	RZ/G1E
31	—	—	—
30	—	—	—
29	—	—	—
28	—	—	—
27	—	—	—
26	—	—	—
25	—	—	—
24	—	—	—
23	—	—	—
22	—	—	—
21	—	—	—
20	—	—	—
19	—	—	—
18	—	—	—
17	—	—	—
16	—	—	—
15	—	—	—
14	—	—	—
13	—	—	—
12	—	—	—
11	—	—	—
10	—	—	—
9	—	—	—
8	—	SCIFA5	SCIFA5
7	—	SCIFA4	SCIFA4
6	—	SCIFA3	SCIFA3
5	—	—	—
4	—	—	—
3	—	—	—
2	—	—	—
1	—	—	—
0	—	—	—

Note: "—" indicates the bit is reserved. Set the value read from the bit.

## 7B. Advanced Power Management Unit for AP-System Core (APMU)

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

### 7B.1 Overview

The AP-system core power management unit (APMU) is a module to control power supply and clock supply to the AP-system core.

This module includes the following function:

- Controls power supply to each CPU core and L2 cache area.

The APMU includes the following submodule:

- Power supply control unit (PCCU) which controls the power supply to each CPU core and L2 cache area.

### 7B.2 Input/Output Pins

There is no input/output pin related with this function.



### 7B.3 Register Descriptions

Table 7B.1 lists the registers of the APMU. All registers listed in this table are cleared by the reset.

**Table 7B.1 Register Configurations**

Register Name	Abbreviation	R/W	Address	Access Size	RZ/G Series Products			
					RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
PCCU registers								
Cortex-A7 CPU wake up control register	CA7WUPCR	R/W	H'E615 1010/H'E615 4010* <sup>1</sup>	32	√	—	—	√
Cortex-A7 power status register	CA7PSTR	R	H'E615 1040/H'E615 4040* <sup>1</sup>	32	√	—	—	√
Cortex-A7 CPU0 power status control register	CA7CPU0CR	R/W	H'E615 1100/H'E615 4100* <sup>1</sup>	32	√	—	—	√
Cortex-A7 CPU1 power status control register	CA7CPU1CR	R/W	H'E615 1110/H'E615 4110* <sup>1</sup>	32	√	—	—	√
Cortex-A7 CPU2 power status control register	CA7CPU2CR	R/W	H'E615 1120/H'E615 4120* <sup>1</sup>	32	√	—	—	—
Cortex-A7 CPU3 power status control register	CA7CPU3CR	R/W	H'E615 1130/H'E615 4130* <sup>1</sup>	32	√	—	—	—
Cortex-A7 debug resource reset control register	CA7DBGRCR	R/W	H'E615 1180	32	√	—	—	√
Cortex-A7 common power control register	CA7CPUCMCR	R/W	H'E615 1184/H'E615 4184* <sup>1</sup>	32	√	—	—	√
Cortex-A15 CPU wake up control register	CA15WUPCR	R/W	H'E615 2010/H'E615 4010* <sup>2</sup>	32	√	√	√	—
Cortex-A15 power status register	CA15PSTR	R	H'E615 2040/H'E615 4040* <sup>2</sup>	32	√	√	√	—
Cortex-A15 CPU0 power status control register	CA15CPU0CR	R/W	H'E615 2100/H'E615 4100* <sup>2</sup>	32	√	√	√	—
Cortex-A15 CPU1 power status control register	CA15CPU1CR	R/W	H'E615 2110/H'E615 4110* <sup>2</sup>	32	√	√	√	—
Cortex-A15 CPU2 power status control register	CA15CPU2CR	R/W	H'E615 2120/H'E615 4120* <sup>2</sup>	32	√	—	—	—
Cortex-A15 CPU3 power status control register	CA15CPU3CR	R/W	H'E615 2130/H'E615 4130* <sup>2</sup>	32	√	—	—	—
Cortex-A15 debug resource reset control register	CA15DBGRCR	R/W	H'E615 2180	32	√	√	√	—
Cortex-A15 common power control register	CA15CPUCMCR	R/W	H'E615 2184/H'E615 4184* <sup>2</sup>	32	√	√	√	—

Notes: The register address map "H'E615 4xxx" is to share the same address between registers for Cortex-A15 and registers for Cortex-A7.

1. Cortex-A7 access to this address is access to this register for RZ/G1H.  
Cortex-A7 access to the address H'E615 4xxx is prohibited for RZ/G1E.  
Use the address H'E615 1xxx to access these registers for RZ/G1E.
2. Cortex-A15 access to this address is access to this register.

**7B.3.1 Cortex-A7/Cortex-A15 CPU<sub>n</sub> Power Status Control Register (CA7CPU<sub>n</sub>CR, CA15CPU<sub>n</sub>CR (n = 0 to 3))**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Cortex-A7/Cortex-A15 CPU<sub>n</sub> power status control registers are 32-bit readable/writable registers of PCCU. These registers define the operation of related CPU when the CPU<sub>n</sub> core issues WFI instruction. Please write to these registers while the power of related CPU is ON.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CPUPWR
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1, 0	CPUPWR	00	R/W	CPU <sub>n</sub> PWR Bit Defines the power supply of corresponding CPU <sub>n</sub> when the CPU <sub>n</sub> issues WFI instruction. 00: Sleep mode 11: CoreStandby mode (power-cut of CPU core, L1\$) Other than above: Setting prohibited These bits are automatically cleared to 00 when the PCCU completes CoreStandby instruction after 11 is written to these bits.

### 7B.3.2 Cortex-A7/Cortex-A15 Common Power Control Register (CA7CPUCMCR, CA15CPUCMCR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Cortex-A7/Cortex-A15 common power control registers are 32-bit readable/writable registers. These registers define power supply control of CPU peripheral (SCU and L2 cache controller) of AP-system core (Cortex-A7) and CPU peripheral (SCU and L2 cache controller) of AP-system core (Cortex-A15). The CMPWR bits of this register define the operation when all CPU cores are in the CoreStandby state.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	L2RST	—	—	CMPWR	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	L2RST	0	R/W	CPU L2 Reset Control Bit Defines the power supply when all of the CPUs in the cluster are in CoreStandby mode (power-off). 0: Normal mode 1: L2 dormant mode
3, 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1, 0	CMPWR	00	R/W	CPU Common Power Control Bit Defines the power supply when all of the CPUs in the cluster are in CoreStandby mode (power-off). 00: Normal mode, CPU peripheral (SCU and L2 cache controller) ON 01: Setting prohibited 10: L2 dormant mode, CPU peripheral (SCU and L2 cache controller) OFF 11: Setting prohibited

### 7B.3.3 Cortex-A7/Cortex-A15 CPU Wake Up Control Register (CA7WUPCR, CA15WUPCR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Cortex-A7/Cortex-A15 CPU wake up control registers are 32-bit readable/writable registers of PCCU. These registers request power on of each CPU core. Writing 1 to the CPU<sub>n</sub>WUP bit wakes up the corresponding CPU<sub>n</sub>, and the CPU<sub>n</sub> starts operation from the reset vector. Each bit is automatically cleared to 0 after the wake up procedure is finished.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	CPU3 WUP	CPU2 WUP	CPU1 WUP	CPU0 WUP
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3	CPU3WUP	0	R/W	[RZ/G1H]: CPU3 Wake Up Bit Write access: 0: Ignores. 1: Requests wake up of CPU3 (CPU3 power on). Read access: 0: CPU3 wakeup sequence is completed. 1: CPU3 wakeup sequence is in progress.
				[RZ/G1M/N/E]: Reserved This bit is always read as 0. The write value should always be 0.
2	CPU2WUP	0	R/W	[RZ/G1H]: CPU2 Wake Up Bit Write access: 0: Ignores. 1: Requests wake up of CPU2 (CPU2 power on). Read access: 0: CPU2 wakeup sequence is completed. 1: CPU2 wakeup sequence is in progress.
				[RZ/G1M/N/E]: Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
1	CPU1WUP	0	R/W	<p>CPU1 Wake Up Bit</p> <p>Write access:</p> <ul style="list-style-type: none"><li>0: Ignores.</li><li>1: Requests wake up of CPU1 (CPU1 power on).</li></ul> <p>Read access:</p> <ul style="list-style-type: none"><li>0: CPU1 wakeup sequence is completed.</li><li>1: CPU1 wakeup sequence is in progress.</li></ul>
0	CPU0WUP	0	R/W	<p>CPU0 Wake Up Bit</p> <p>Write access:</p> <ul style="list-style-type: none"><li>0: Ignores.</li><li>1: Requests wake up of CPU0 (CPU0 power on).</li></ul> <p>Read access:</p> <ul style="list-style-type: none"><li>0: CPU0 wakeup sequence is completed.</li><li>1: CPU0 wakeup sequence is in progress.</li></ul>

### 7B.3.4 Cortex-A7/Cortex-A15 Power Status Register (CA7PSTR, CA15PSTR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Cortex-A7/Cortex-A15 power status registers are 32-bit readable registers of PCCU. These registers show power status of AP-system CPU cores.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	—	0	0	0	—	0	0	0	—	0	0	0	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	CPU3ST[1:0]	—	—	CPU2ST[1:0]	—	—	CPU1ST[1:0]	—	—	CPU0ST[1:0]	—	—	—	—
Initial value:	0	0	1	1	0	0	1	1	0	0	1	1	0	0	00/11*	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Note: X (-) stands for unknown value.

\* See the table note overleaf.

Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	All 0	R	Reserved These bits are always read as 0.
28	—	Undefined	R	Reserved This bit is always read as unknown value.
27 to 25	—	All 0	R	Reserved These bits are always read as 0.
24	—	Undefined	R	Reserved This bit is always read as unknown value.
23 to 21	—	All 0	R	Reserved These bits are always read as 0.
20	—	Undefined	R	Reserved This bit is always read as unknown value.
19 to 17	—	All 0	R	Reserved These bits are always read as 0.
16	—	Undefined	R	Reserved This bit is always read as unknown value.
15, 14	—	All 0	R	Reserved These bits are always read as 0.

Bit	Bit Name	Initial Value	R/W	Description
13, 12	CPU3ST [1:0]	11	R	[RZ/G1H]: CPU3 Status Bit Displays CPU3 status. 00: Run mode 11: CoreStandby mode Other than above: Invalid [RZ/G1M/N/E]: Reserved These bits are always read as 11.
11, 10	—	All 0	R	Reserved These bits are always read as 0.
9, 8	CPU2ST [1:0]	11	R	[RZ/G1H]: CPU2 Status Bit Displays CPU2 status. 00: Run mode 11: CoreStandby mode Other than above: Invalid [RZ/G1M/N/E]: Reserved These bits are always read as 11.
7, 6	—	All 0	R	Reserved These bits are always read as 0.
5, 4	CPU1ST [1:0]	11	R	CPU1 Status Bit Displays CPU1 status. 00: Run mode 11: CoreStandby mode Other than above: Invalid
3, 2	—	All 0	R	Reserved These bits are always read as 0.
1, 0	CPU0ST [1:0]	00/11*	R	CPU0 Status Bit Displays CPU0 status. 00: Run mode 11: CoreStandby mode Other than above: Invalid

Note: \* RZ/G1H/CA7PSTR: The initial value is 00 when (MD7, MD6) = (L, H) for the Cortex-A7 booting.  
The initial value is 11 when (MD7, MD6) = (L, L) for the Cortex-A15 booting.  
RZ/G1H/CA15PSTR: The initial value is 00 when (MD7, MD6) = (L, L) for the Cortex-A15 booting.  
The initial value is 11 when (MD7, MD6) = (L, H) for the Cortex-A7 booting.  
RZ/G1M/CA15PSTR: The initial value is 00 when (MD7, MD6) = (L, L) for the Cortex-A15 booting.  
RZ/G1N/CA15PSTR: The initial value is 00 when (MD7, MD6) = (L, L) for the Cortex-A15 booting.  
RZ/G1E/CA7PSTR: The initial value is 00 when (MD7, MD6) = (L, H) for the Cortex-A7 booting.  
The MD[7:6] settings other than above are prohibited.

### 7B.3.5 Cortex-A7/Cortex-A15 Debug Resource Reset Control Register (CA7DBGRCR, CA15DBGRCR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Cortex-A7/Cortex-A15 debug resource reset control registers are 32-bit readable/writable registers of PCCU. These registers enable the reset requests derived from power-shutoff to the AP-system CPU cores in the debug mode. When you write to these registers, please modify only the target bits you want to change (read-modify-write). In the debug mode, bits 24 to 19 must be set to all 1 before the AP-system cores first resume from power-shutoff. In the normal mode (i.e. not debug mode), writing all 1 to bits 24 to 19 doesn't disturb normal operation. Therefore the same code to write these registers can be applied for both debug mode and normal mode.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	DBGCP UREN	DBGCP U3REN	DBGCP U2REN	DBGCP U1REN	DBGCP U0REN	DBGCP UPREN	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	—	—
R/W:	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	—	—	0	0	—	—	0	0	—	—	0	0	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 25	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
24	DBGCPURE N	0	R/W	Enable the reset request derived from power-shutoff to the circuits other than CPU cores in the debug mode. 0: Disables the reset request derived from power-shutoff to the circuits other than CPU cores in the debug mode. 1: Enables the reset request derived from power-shutoff to the circuits other than CPU cores in the debug mode.
23	DBGCPU3R EN	0	R/W	[RZ/G1H]: Enable the reset request derived from power-shutoff to CPU3 in the debug mode. 0: Disables the reset request derived from power-shutoff to CPU3 in the debug mode. 1: Enables the reset request derived from power-shutoff to CPU3 in the debug mode. [RZ/G1M/N/E]: Reserved The initial value of this bit is 0. The value of this bit doesn't affect the operation of RZ/G1M/N. Therefore the write value can be either 0 or 1.



Bit	Bit Name	Initial Value	R/W	Description
22	DBGCPU2REN	0	R/W	<p>[RZ/G1H]:</p> <p>Enable the reset request derived from power-shutoff to CPU2 in the debug mode.</p> <p>0: Disables the reset request derived from power-shutoff to CPU2 in the debug mode.</p> <p>1: Enables the reset request derived from power-shutoff to CPU2 in the debug mode.</p> <hr/> <p>[RZ/G1M/N/E]:</p> <p>Reserved</p> <p>The initial value of this bit is 0. The value of this bit doesn't affect the operation of RZ/G1M/N. Therefore the write value can be either 0 or 1.</p>
21	DBGCPU1REN	0	R/W	<p>Enable the reset request derived from power-shutoff to CPU1 in the debug mode.</p> <p>0: Disables the reset request derived from power-shutoff to CPU1 in the debug mode.</p> <p>1: Enables the reset request derived from power-shutoff to CPU1 in the debug mode.</p>
20	DBGCPU0REN	0	R/W	<p>Enable the reset request derived from power-shutoff to CPU0 in the debug mode.</p> <p>0: Disables the reset request derived from power-shutoff to CPU0 in the debug mode.</p> <p>1: Enables the reset request derived from power-shutoff to CPU0 in the debug mode.</p>
19	DBGCPUPREN	0	R/W	<p>Enable the reset request derived from power-shutoff to CPU Peripheral (SCU and L2 cache controller) in the debug mode.</p> <p>0: Disables the reset request derived from power-shutoff to CPU Peripheral (SCU and L2 cache controller) in the debug mode.</p> <p>1: Enables the reset request derived from power-shutoff to CPU Peripheral (SCU and L2 cache controller) in the debug mode.</p>
18	—	0	R	<p>Reserved</p> <p>This bit is always read as 0. The write value should always be 0.</p>
17, 16	—	Undefined	R	<p>Reserved</p> <p>These bits are always read as unknown values. The write value should always be the same as read values (read-modify-write).</p>
15, 14	—	All 0	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>
13, 12	—	Undefined	R	<p>Reserved</p> <p>These bits are always read as unknown values. The write value should always be the same as read values (read-modify-write).</p>
11, 10	—	All 0	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>
9, 8	—	Undefined	R	<p>Reserved</p> <p>These bits are always read as unknown values. The write value should always be the same as read values (read-modify-write).</p>
7, 6	—	All 0	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>

Bit	Bit Name	Initial Value	R/W	Description
5, 4	—	Undefined	R	Reserved These bits are always read as unknown values. The write value should always be the same as read values (read-modify-write).
3, 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1, 0	—	Undefined	R	Reserved These bits are always read as unknown values. The write value should always be the same as read values (read-modify-write).

## 7B.4 PCCU Function

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

### 7B.4.1 Power Control

The PCCU manages the CPU power supply when the CPU issues WFI instruction, and recovers from the low power state. Table 7B.2 shows power status of CPU.

**Table 7B.2 CPU Power Mode**

Power Mode	CPU# <i>n</i> Clock	CPU# <i>n</i> Power	CPU Peripheral (SCU and L2 Cache Controller) Power
Run mode	ON	ON	ON
Sleep mode	OFF	ON	ON
CoreStandby mode	OFF	OFF [RZ/G1H/M/N] ON (Pseudo Power OFF) [RZ/G1E]	ON
L2 dormant mode	OFF	OFF [RZ/G1H/M/N] ON (Pseudo Power OFF) [RZ/G1E]	OFF [RZ/G1H/M/N] ON (Pseudo Power OFF) [RZ/G1E]

**The following is method to enter each mode. [RZ/G1H]**

#### Sleep mode

Issue WFI instruction when the CPUPWR bits of CA7CPU<sub>n</sub>CR/CA15CPU<sub>n</sub>CR are B'00.

#### CoreStandby mode

Issue WFI instruction when the CPUPWR bits of CA7CPU<sub>n</sub>CR/CA15CPU<sub>n</sub>CR are B'11.

The CPUPWR bits of CA7CPU<sub>n</sub>CR/CA15CPU<sub>n</sub>CR are automatically cleared to B'00 when the PCCU completes CoreStandby operation. So the interrupt to CPU<sub>n</sub> is masked while CPUPWR bits of CA7CPU<sub>n</sub>CR/CA15CPU<sub>n</sub>CR are B'11. In the case of cancel, it is cancelled by setting B'00 to the CPUPWR bits of CA7CPU<sub>n</sub>CR/CA15CPU<sub>n</sub>CR.

#### L2 dormant mode

Issue WFI instruction when all of the conditions below are met:

Other CPU cores in the same CPU cluster are in the CoreStandby mode.

The CMPWR bits of CA7CPUCMCR/CA15CPUCMCR are B'10.

The L2RST bit of CA7CPUCMCR/CA15CPUCMCR is 1.

The CPUPWR bits of CA7CPU<sub>n</sub>CR/CA15CPU<sub>n</sub>CR are B'11, the other CPU

#### Run mode

Interrupt and reset of CPU recovers each CPU to the RUN mode.

**The following is method to enter each mode. [RZ/G1M/RZ/G1N]**

#### Sleep mode

Issue WFI instruction when the CPUPWR bits of CA15CPU<sub>n</sub>CR are B'00.

#### CoreStandby mode

Issue WFI instruction when the CPUPWR bits of CA15CPU<sub>n</sub>CR are B'11.

The CPUPWR bits of CA15CPUUnCR are automatically cleared to B'00 when the PCCU completes CoreStandby operation. So the interrupt to CPU is masked while CPUPWR bits of CA15CPUUnCR are B'11. In the case of cancel, it is cancelled by setting B'00 to the CPUPWR bits of CA15CPUUnCR.

#### L2 dormant mode

Issue WFI instruction when all of the conditions below are met:

Other CPU cores in the same CPU cluster are in the CoreStandby mode.

The CMPWR bits of CA15CPUCMCR are B'10.

The L2RST bit of CA15CPUCMCR is 1.

The CPUPWR bits of CA15CPUUnCR are B'11, the other CPU

#### Run mode

Interrupt and reset of CPU recovers each CPU to the RUN mode.

**The following is method to enter each mode. [RZ/G1E]**

#### Sleep mode

Issue WFI instruction when the CPUPWR bits of CA7CPUUnCR are B'00.

#### CoreStandby mode

Issue WFI instruction with the CPUPWR bits of CA7CPUUnCR are B'11.

The CPUPWR bits of CA7CPUUnCR are automatically cleared to B'00 when the PCCU completes CoreStandby operation. So the interrupt to CPU is masked while CPUPWR bits of CA7CPUUnCR are B'11. In the case of cancel, it is cancelled by setting B'00 to the CPUPWR bits of CA7CPUUnCR.

#### L2 dormant mode

Issue WFI instruction when all of the conditions below are met:

Other CPU cores in the same CPU cluster are in the CoreStandby mode.

The CMPWR bits of CA7CPUCMCR are B'10.

The L2RST bit of CA7CPUCMCR is 1.

The CPUPWR bits of CA7CPUUnCR are B'11, the other CPU

#### Run mode

Interrupt and reset of CPU recovers each CPU to the RUN mode.

# 8. Reset (RST)

RZ/G1H	RZ/G1N
RZ/G1M	RZ/G1E

The reset (RST) consists of the bus interface block and registers related to reset control. Timing of the bus interface block is based on CPφ.

## 8.1 Features

The following functions are implemented by RST.

- Register-based reset control for the Cortex-A15 (present in the RZ/G1H, RZ/G1M, and RZ/G1N), and Cortex-A7 (present in the RZ/G1H and RZ/G1E)
- Latching of the levels on mode pins when PRESET# is negated
- Mode monitoring register
- Boot address registers for the Cortex-A15, and Cortex-A7

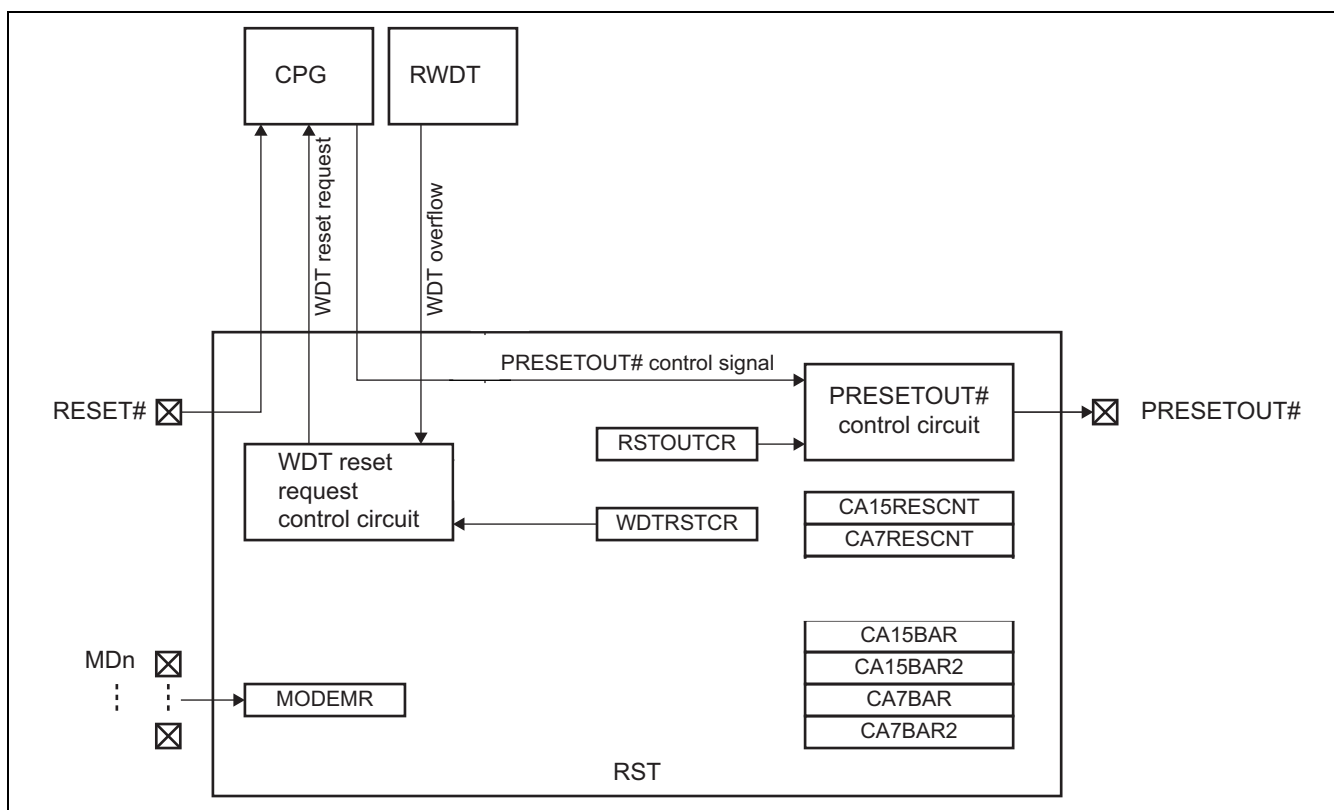


Figure 8.1 Block Diagram of RST

## 8.2 WDT reset

- WDT resets can be issued by the RWDT.
- WDRSTCR controls the permission or prohibition of WDT resets.
- The reset (RST) module is not initialized by a WDT reset.

### 8.3 LSI Pins Connected to RST

The following table lists the pins connected to the RST.

**Table 8.1 External Pins for RST**

Pin Name	Function	Direction	Remarks	RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
MD0 to MD14	Mode pins	IN	Mode pins	√	√	√	√
MD15				√	—	—	—
MD16				√	—	—	—
MD17	(Mode pins)	(IN)	(Mode pins)	√	—	—	—
MD18				√	—	—	√
MD19 to MD21				√	√	√	√
MD22 to MD24				√	√	√	—
MD25, MD26	(Mode Pins)	(IN)	(Mode pins)	√	—	—	—
MD27, MD28				√	√	√	—
MDT0, MDT1				√	√	√	√
PRESET#	Power-on-reset	IN	Power-on-reset The low-level input on this pin places the LSI in the power-on-reset state.	√	√	√	√
PRESETOUT#	Indicates internal reset	OUT	Reset output	√	√	√	√

## 8.4 Register Descriptions

**Table 8.2 RST Register Details**

Register Name	Mnemonic	R/W	Address	Access Size	Access Permission	RZ/G Series Products			
						RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Mode monitoring register	MODEMR	R	H'E616 0060	32	All	√	√	√	√
Cortex-A15 reset control register	CA15RESCNT	R/W	H'E616 0040	32	All	√	√	√	—
Cortex-A7 reset control register	CA7RESCNT	R/W	H'E616 0044	32	All	√	—	—	√
Watchdog timer reset control register	WDRSTCR	R/W	H'E616 0054	32	All	√	√	√	√
PRESETOUT control register	RSTOUTCR	R/W	H'E616 0058	32	All	√	√	√	√
SYS boot address register	SBAR	R/W	H'E616 0010	32	Cortex-A7/Cortex-A15	√	√	√	—
SYS boot address register 2	SBAR2	R/W	H'E616 0014	32	Cortex-A7/Cortex-A15	√	√	√	—
Cortex-A7 boot address register	CA7BAR	R/W	H'E616 0030	32	All	√	—	—	√
Cortex-A7 boot address register 2	CA7BAR2	R/W	H'E616 0034	32	All	√	—	—	√
Cortex-A15 boot address register	CA15BAR	R/W	H'E616 0020	32	All	√	√	√	—
Cortex-A15 boot address register 2	CA15BAR2	R/W	H'E616 0024	32	All	√	√	√	—

Note: Do not write to any addresses other than listed above. Operations cannot be guaranteed if writing is attempted. Values read from addresses other than those listed above are undefined.

**Table 8.3 State of the Registers on Reset**

Mnemonic	Power-On Reset	RZ/G Series Products			
		RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
MODEMR	Initialized*	√	√	√	√
CA15RESCNT	Initialized*	√	√	√	—
CA7RESCNT	Initialized*	√	—	—	√
WDTRSTCR	Initialized*	√	√	√	√
RSTOUTCR	Initialized*	√	√	√	√
SBAR	Initialized*	√	√	√	—
SBAR2	Initialized*	√	√	√	—
CA7BAR	Initialized*	√	—	—	√
CA7BAR2	Initialized*	√	—	—	√
CA15BAR	Initialized*	√	√	√	—
CA15BAR2	Initialized*	√	√	√	—

Note: \* Initialized only on power-on reset caused by PRESET#.



### 8.4.1 Mode Monitoring Register (MODEMR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

MODEMR is a 32-bit read-only register, which can be accessed only in longwords.

#### [RZ/G1H]:

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	MDT1	MDT0	MD28	MD27	MD26	MD25	MD24	MD23	MD22	MD21	MD20	MD19	MD18	MD17	MD16
Initial value:	0	0	0	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MD15	MD14	MD13	MD12	MD11	MD10	MD09	MD08	MD07	MD06	MD05	MD04	MD03	MD02	MD01	MD00
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31	—	0	R	Reserved When read, returns 0.
30, 29	MDT[1:0]	00	R	Reserved The read value is illegal (always 00).
28 to 0	MD[28:00]	Depend on mode setting	R	The value of MD28 to MD0

#### [RZ/G1M/N]:

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	MDT1	MDT0	MD28	MD27	—	—	MD24	MD23	MD22	MD21	MD20	MD19	—	—	—
Initial value:	0	—	—	—	—	0	—	—	—	—	—	—	—	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	MD14	MD13	MD12	MD11	MD10	MD09	MD08	MD07	MD06	MD05	MD04	MD03	MD02	MD01	MD00
Initial value:	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31	—	0	R	Reserved When read, returns 0.
30, 29	MDT[1:0]	Depend on mode setting	R	The value of MDT0 and MDT1
28, 27	MD[28:27]	Depend on mode setting	R	The value of MD28 and MD27
26, 25	—	All 0	R	Reserved These bits are always read as 0. Writing is inhibited.
24 to 19	MD[24:19]	Depend on mode setting	R	The value of MD24 to MD19

Bit	Bit Name	Initial Value	R/W	Description
18 to 15	—	All 0	R	Reserved. These bits are always read as 0. Writing is inhibited.
14 to 0	MD[14:00]	Depend on mode setting	R	The value of MD14 to MD0

**[RZ/G1E]:**

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	MDT1	MDT0	—	—	—	—	—	—	—	MD21	MD20	MD19	MD18	—	—
Initial value:	0	—	—	0	0	0	0	0	0	0	—	—	—	—	1	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	MD14	MD13	MD12	MD11	MD10	MD09	MD08	MD07	MD06	MD05	MD04	MD03	MD02	MD01	MD00
Initial value:	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31	—	0	R	Reserved. When read, returns 0.
30, 29	MDT[1:0]	Depend on mode setting	R	The value of MDT0 and MDT1
28 to 22	—	All 0	R	Reserved. These bits are always read as 0. Writing is inhibited.
21 to 18	MD[21:18]	Depend on mode setting	R	The value of MD21 to MD18
17, 16	—	11	R	Reserved. These bits are always read as 11. Writing is inhibited.
15	—	0	R	Reserved. This bit is always read as 0. Writing is inhibited.
14 to 0	MD[14:00]	Depend on mode setting	R	The value of MD14 to MD0

### 8.4.2 Cortex-A15 Reset Control Register (CA15RESCNT)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

CA15RESCNT is a 32-bit readable/writable register, which can be accessed only in longwords.

This register specifies whether the reset is issued to Cortex-A15 CPU<sub>n</sub> (n = 0 to 3) or not. The upper word of the write value should always be the code value H'A5A5. If the code value is read, it is always read as 0.

This register is initialized on power on reset caused by PRESET#.

#### [RZ/G1H]:

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Code value (H'A5A5)															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	CA15 CPU0R	CA15 CPU1R	CA15 CPU2R	CA15 CPU3R
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	MD7   MD6	1	1	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	Code value	H'0000	R/W	Code value (H'A5A5) When read, returns 0.
15 to 4	—	All 0	R	Reserved When read, returns 0. The write value should always be 0.
3	CA15CPU0R	MD7   MD6	R/W	Issue reset to Cortex-A15 CPU0 0: Not assert the reset to Cortex-A15 CPU0 1: Assert the reset to Cortex-A15 CPU0
2	CA15CPU1R	1	R/W	Issue reset to Cortex-A15 CPU1 0: Not assert the reset to Cortex-A15 CPU1 1: Assert the reset to Cortex-A15 CPU1
1	CA15CPU2R	1	R/W	Issue reset to Cortex-A15 CPU2 0: Not assert the reset to Cortex-A15 CPU2 1: Assert the reset to Cortex-A15 CPU2
0	CA15CPU3R	1	R/W	Issue reset to Cortex-A15 CPU3 0: Not assert the reset to Cortex-A15 CPU3 1: Assert the reset to Cortex-A15 CPU3

**[RZ/G1M/N]:**

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Code value (H'A5A5)															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	CA15 CPU0R	CA15 CPU1R	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	MD7   MD6	1	1	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	Code value	H'0000	R/W	Code value (H'A5A5) When read, returns 0.
15 to 4	—	All 0	R	Reserved When read, returns 0. The write value should always be 0.
3	CA15CPU0R	MD7   MD6	R/W	Issue reset to Cortex-A15 CPU0 0: Not assert the reset to Cortex-A15 CPU0 1: Assert the reset to Cortex-A15 CPU0
2	CA15CPU1R	1	R/W	Issue reset to Cortex-A15 CPU1 0: Not assert the reset to Cortex-A15 CPU1 1: Assert the reset to Cortex-A15 CPU1
1, 0	—	All 1	R	Reserved When read, returns 1. The write value should always be 1.

### 8.4.3 Cortex-A7 Reset Control Register (CA7RESCNT)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	—	—	√

CA7RESCNT is a 32-bit readable/writable register, which can be accessed only in longwords.

This register specifies whether the reset is issued to Cortex-A7 CPU<sub>n</sub> (n = 0 to 3) or not. The upper word of the write value should always be the code value H'5A5A. If the code value is read, it is always read as 0.

This register is initialized on power on reset caused by PRESET#.

#### [RZ/G1H]:

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Code value (H'5A5A)															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	CA7 CPU0R	CA7 CPU1R	CA7 CPU2R	CA7 CPU3R
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	MD7   ~MD6	1	1	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	Code value	H'0000	R/W	Code value (H'5A5A) When read, returns 0.
15 to 4	—	All 0	R	Reserved When read, returns 0. The write value should always be 0.
3	CA7CPU0R	MD7   ~MD6	R/W	Issue reset to Cortex-A7 CPU0 0: Not assert the reset to Cortex-A7 CPU0 1: Assert the reset to Cortex-A7 CPU0
2	CA7CPU1R	1	R/W	Issue reset to Cortex-A7 CPU1 0: Not assert the reset to Cortex-A7 CPU1 1: Assert the reset to Cortex-A7 CPU1
1	CA7CPU2R	1	R/W	Issue reset to Cortex-A7 CPU2 0: Not assert the reset to Cortex-A7 CPU2 1: Assert the reset to Cortex-A7 CPU2
0	CA7CPU3R	1	R/W	Issue reset to Cortex-A7 CPU3 0: Not assert the reset to Cortex-A7 CPU3 1: Assert the reset to Cortex-A7 CPU3

**[RZ/G1E]:**

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Code value (H'5A5A)															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	CA7 CPU0R	CA7 CPU1R	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	MD7   ~MD6	1	1	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	Code value	H'0000	R/W	Code value (H'5A5A) When read, returns 0.
15 to 4	—	All 0	R	Reserved When read, returns 0. The write value should always be 0.
3	CA7CPU0R	MD7  ~MD6	R/W	Issue reset to Cortex-A7 CPU0 0: Not assert the reset to Cortex-A7 CPU0 1: Assert the reset to Cortex-A7 CPU0
2	CA7CPU1R	1	R/W	Issue reset to Cortex-A7 CPU1 0: Not assert the reset to Cortex-A7 CPU1 1: Assert the reset to Cortex-A7 CPU1
1, 0	—	All 1	R	Reserved When read, returns 1. The write value should always be 1.

#### 8.4.4 Watchdog Timer Reset Control Register (WDTRSTCR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

WDTRSTCR is a 32-bit readable/writable register, which can be accessed only in longwords.

This register specifies whether the watchdog timer overflow should be masked or not as a reset trigger. The upper word of the write value should always be the code value H'A55A. If the code value is read, it is always read as 0.

This register is initialized on power on reset caused by PRESET#.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Code value (H'A55A)															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RWDT_ RSTMSK
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	Code value	H'0000	R/W	Code value (H'A55A) When read, returns 0.
15 to 2	—	All 0	R	Reserved When read, returns 0. The write value should always be 0.
1	—	1	R	Reserved When read, returns 1. The write value should always be 1.
0	RWDT_ RSTMSK	1	R/W	RWDT Reset Mask This bit is used to mask the detection of RWDT overflow. 0: Reset request 1: Not reset request

### 8.4.5 PRESETOUT Control Register (RSTOUTCR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

RSTOUTCR is a 32-bit readable/writable register, which can be accessed only in longwords.

This register controls the output level of external LSI pin RESETOUT# by software.

This register is initialized on power on reset caused by PRESET#.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RES OUT
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	RW

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved When read, returns 0. The write value should always be 0.
0	RESOUT	1	R/W	PRESETOUT# control by software This bit is used to specify the output level of PRESETOUT#. 0: PRESETOUT# is asserted 1: PRESETOUT# is negated



#### 8.4.6 SYS Boot Address Register (SBAR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

SBAR is a link to CA7BAR\* or CA15BAR\*. SBAR is write-only register. Therefore read access to SBAR is prohibited.

If System CPU (Cortex-A7\*) accesses to SBAR, System CPU (Cortex-A7\*) can write to CA7BAR\*.

If System CPU (Cortex-A15\*) accesses to SBAR, System CPU (Cortex-A15\*) can write to CA15BAR\*.

Note: \* Cortex-A7 is not supported by RZ/G1M, and RZ/G1N. Cortex-A15 is not supported by RZ/G1E.

#### 8.4.7 SYS Boot Address Register2 (SBAR2)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

SBAR2 is a link to CA7BAR2\* or CA15BAR2\*. SBAR2 is write-only register. Therefore read access to SBAR2 is prohibited.

If System CPU (Cortex-A7\*) accesses to SBAR2, System CPU (Cortex-A7\*) can write to CA7BAR2\*.

If System CPU (Cortex-A15\*) accesses to SBAR2, System CPU (Cortex-A15\*) can write to CA15BAR2\*.

Note: \* Cortex-A7 is not supported by RZ/G1M, and RZ/G1N. Cortex-A15 is not supported by RZ/G1E.

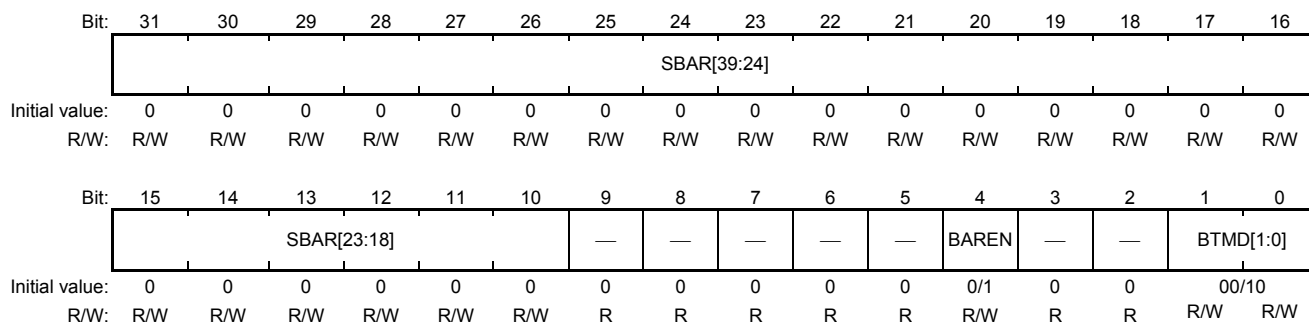
### 8.4.8 Cortex-A7 Boot Address Register (CA7BAR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	—	—	√

CA7BAR is a 32-bit readable/writable register, which can be accessed only in longwords.

This register specifies the boot space of the System CPU (Cortex-A7).

This register is initialized on power on reset caused by PRESET#.



Bit	Bit Name	Initial Value	R/W	Description
31 to 10	SBAR[39:18]	{H'00000, B'00}	R/W	System CPU (Cortex-A7) Boot Address When System CPU (Cortex-A7) accesses to the range of physical address from H'00 0000 0000 to H'00 0003 FFFF, the address bit in [39:18] is replaced by SBAR[39:18].
9 to 5	—	All 0	R	Reserved When read, returns 0. The write value should always be 0.
4	BAREN*2	0/1*1	R/W	BAREN bit 0: SBAR is not valid. 1: SBAR is valid.
3, 2	—	All 0	R	Reserved When read, returns 0. The write value should always be 0.
1, 0	BTMD[1:0]	00/10*1	R/W	Specifies the Boot area of System CPU (Cortex-A7) During Hardware Power On Reset the initial value of these bits depends upon MD3, MD2 and MD1 pin setting. 00: SBAR[39:18] is assigned to Boot address, set SBAR[17:0] to 0. 01: Prohibited. 10: Boots from Built-in memory. 11: Prohibited.

- Note:
- Initial value depends upon MD3, MD2 and MD1 pin setting.
  - Do not rewrite BAREN = 1 simultaneously with SBAR and BTMD. After completing the setting of SBAR and BTMD with BAREN = 0, set only BAREN = 1.  
For example: Change SBAR[39:18] from A to B, and BTMD[1:0] = 00  
Step 1: Write SBAR[39:18] = B, BAREN = 0, BTMD[1:0] = 00  
Step 2: Write SBAR[39:18] = B, BAREN = 1, BTMD[1:0] = 00

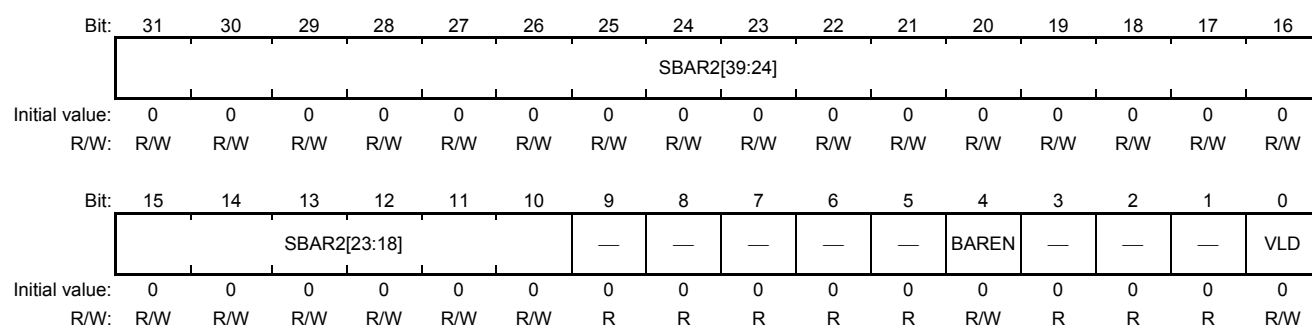
### 8.4.9 Cortex-A7 Boot Address Register2 (CA7BAR2)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	—	—	√

CA7BAR2 is a 32-bit readable/writable register, which can be accessed only in longwords. This register can be changed only in the secure mode.

This register specifies the boot space of the System CPU (Cortex-A7).

This register is initialized on power on reset caused by PRESET#.



Bit	Bit Name	Initial Value	R/W	Description
31 to 10	SBAR2[39:18]	{H'00000, B'00}	R/W	System CPU (Cortex-A7) Boot Address2 When System CPU (Cortex-A7) accesses to the range of physical address from H'00 0000 0000 to H'00 0003 FFFF, the address bit in [39:18] is replaced by SBAR2[39:18].
9 to 5	—	All 0	R	Reserved When read, returns 0. The write value should always be 0.
4	BAREN*	0	R/W	BAREN bit 0: SBAR2 is not valid. 1: SBAR2 is valid.
3 to 1	—	All 0	R	Reserved When read, returns 0. The write value should always be 0.
0	VLD	0	R/W	VALID bit When 1 is set to this bit, System CPU (Cortex-A7) starts only from the address set to SBAR2. 0: System CPU (Cortex-A7) starts from the address set to SBAR. 1: System CPU (Cortex-A7) starts from the address set to SBAR2.

Note: \* Do not rewrite BAREN=1 simultaneously with SBAR2 and VLD. After completing the setting of SBAR2 and VLD with BAREN = 0, set only BAREN = 1.

For example: Change SBAR2[39:18] from A to B, and VLD = 1

Step 1: Write SBAR2[39:18] = B, BAREN = 0, VLD = 1

Step 2: Write SBAR2[39:18] = B, BAREN = 1, VLD = 1

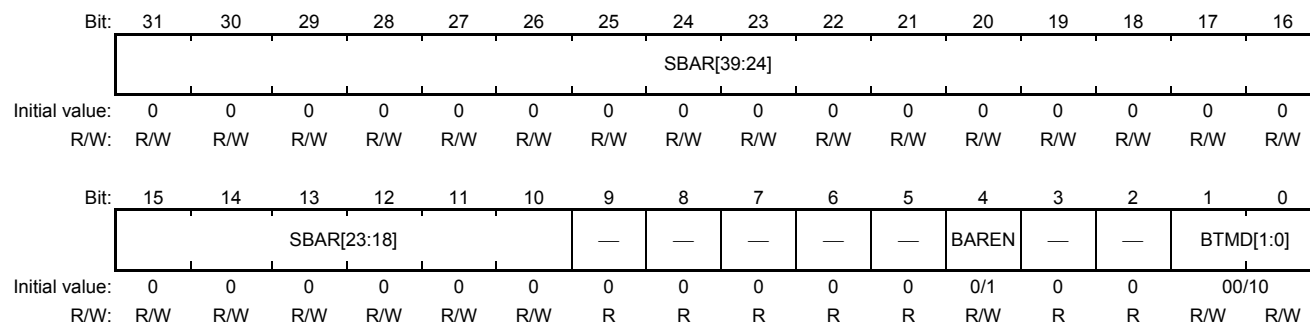
### 8.4.10 Cortex-A15 Boot Address Register (CA15BAR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

CA15BAR is a 32-bit readable/writable register, which can be accessed only in longwords.

This register specifies the boot space of the System CPU (Cortex-A15).

This register is initialized on power on reset caused by PRESET#.



Bit	Bit Name	Initial Value	R/W	Description
31 to 10	SBAR[39:18]	{H'00000, B'00}	R/W	System CPU (Cortex-A15) Boot Address When System CPU (Cortex-A15) accesses to the range of physical address from H'00 0000 0000 to H'00 0003 FFFF, the address bit in [39:18] is replaced by SBAR[39:18].
9 to 5	—	All 0	R	Reserved When read, returns 0. The write value should always be 0.
4	BAREN*2	0/1*1	R/W	BAREN bit 0: SBAR is not valid. 1: SBAR is valid.
3, 2	—	All 0	R	Reserved When read, returns 0. The write value should always be 0.
1, 0	BTMD[1:0]	00/10*1	R/W	Specifies the Boot area of System CPU (Cortex-A15) During Hardware Power On Reset the initial value of these bits depends upon MD3, MD2 and MD1 pin setting. 00: SBAR[39:18] is assigned to Boot address, set SBAR[17:0] to 0. 01: Prohibited. 10: Boots from Built-in memory. 11: Prohibited.

- Note:
- Initial value depends upon MD3, MD2 and MD1 pin setting.
  - Do not rewrite BAREN = 1 simultaneously with SBAR and BTMD. After completing the setting of SBAR and BTMD with BAREN = 0, set only BAREN = 1.  
For example: Change SBAR[39:18] from A to B, and BTMD[1:0] = 00  
Step 1: Write SBAR[39:18] = B, BAREN = 0, BTMD[1:0] = 00  
Step 2: Write SBAR[39:18] = B, BAREN = 1, BTMD[1:0] = 00

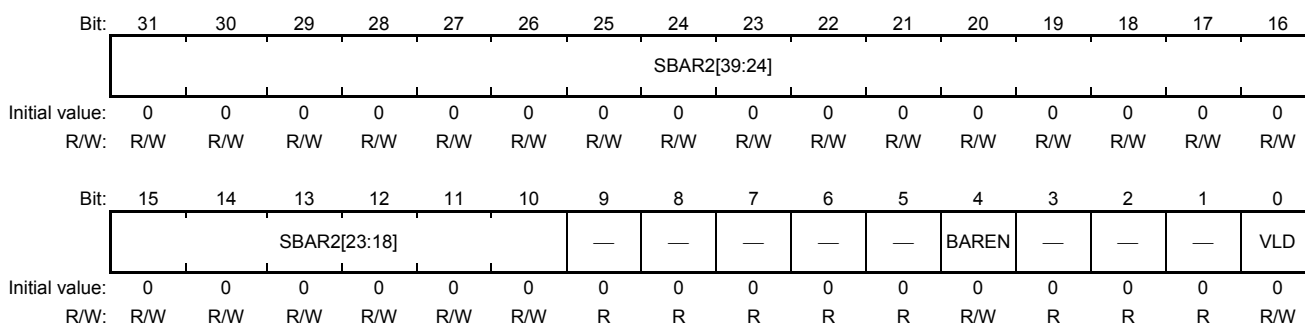
### 8.4.11 Cortex-A15 Boot Address Register2 (CA15BAR2)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

CA15BAR2 is a 32-bit readable/writable register, which can be accessed only in longwords. This register can be changed only in the secure mode.

This register specifies the boot space of the System CPU (Cortex-A15).

This register is initialized on power on reset caused by PRESET#.



Bit	Bit Name	Initial Value	R/W	Description
31 to 10	SBAR2[39:18]	{H'00000, B'00}	R/W	System CPU (Cortex-A15) Boot Address2 When System CPU (Cortex-A15) accesses to the range of physical address from H'00 0000 0000 to H'00 0003 FFFF, the address bit in [39:18] is replaced by SBAR2[39:18].
9 to 5	—	All 0	R	Reserved When read, returns 0. The write value should always be 0.
4	BAREN*1	0	R/W	BAREN bit 0: SBAR2 is not valid. 1: SBAR2 is valid.
3 to 1	—	All 0	R	Reserved When read, returns 0. The write value should always be 0.
0	VLD	0	R/W	VALID bit When 1 is set to this bit, System CPU (Cortex-A15) starts only from the address set to SBAR2. 0: System CPU (Cortex-A15) starts from the address set to SBAR. 1: System CPU (Cortex-A15) starts from the address set to SBAR2.

Note: \* Do not rewrite BAREN = 1 simultaneously with SBAR2 and VLD. After completing the setting of SBAR2 and VLD with BAREN = 0, set only BAREN = 1.  
For example: Change SBAR2[39:18] from A to B, and VLD = 1  
Step 1: Write SBAR2[39:18] = B, BAREN = 0, VLD = 1  
Step 2: Write SBAR2[39:18] = B, BAREN = 1, VLD = 1

## 8.5 Reset Timing

RZ/G1H	RZ/G1N
RZ/G1M	RZ/G1E

### 8.5.1 Power-On Reset by PRESET# Pin

Since the PLL circuit is initialized when the LSI enters the power-on reset state, the PLL oscillation settling time needs to be secured. This means that a high level must not be input to the PRESET# pin during the PLL oscillation settling time. For the power-on oscillation settling time ( $t_{OSC}$ ), see section 63, Electrical Characteristics.

After the state on the PRESET# pin input is changed from a low level to high level, the internal reset state continues until the flash ROM reset time (longer than 50  $\mu s$ ), the flash ROM holding time (longer than 5  $\mu s$ ) and the reset holding time elapse.

#### (1) Sequence for Turning on the Power

When the power is turned on, ensure that a low level is input to the PRESET# pin. A low level input is also needed on the TRST# pin.

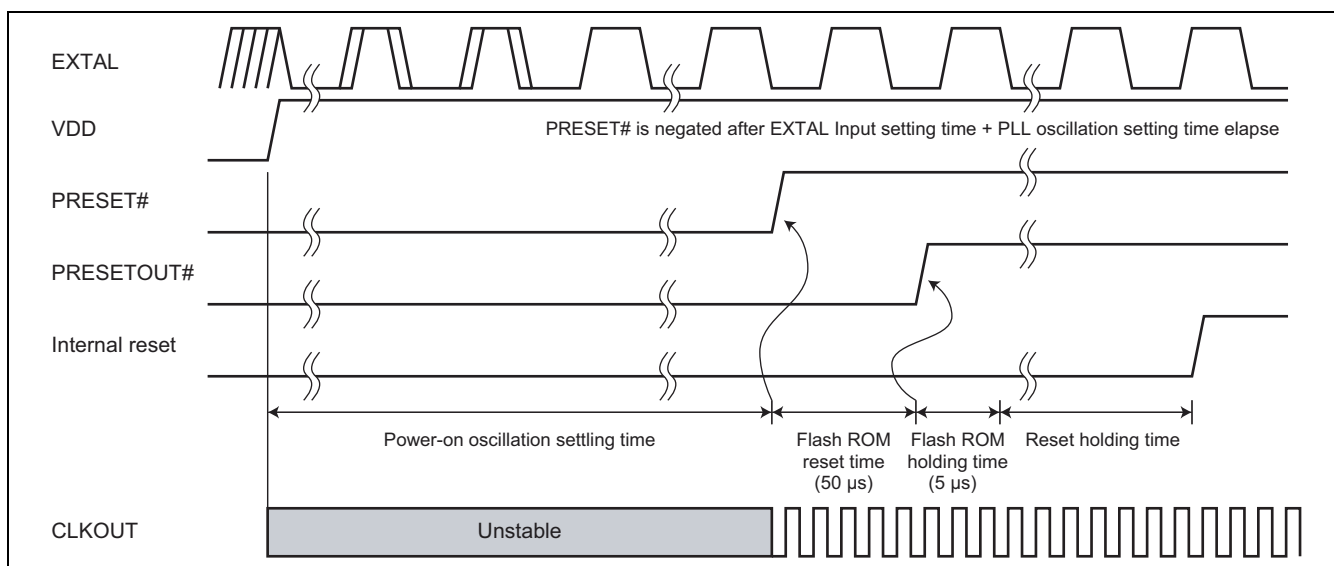


Figure 8.2 Free-Running Mode

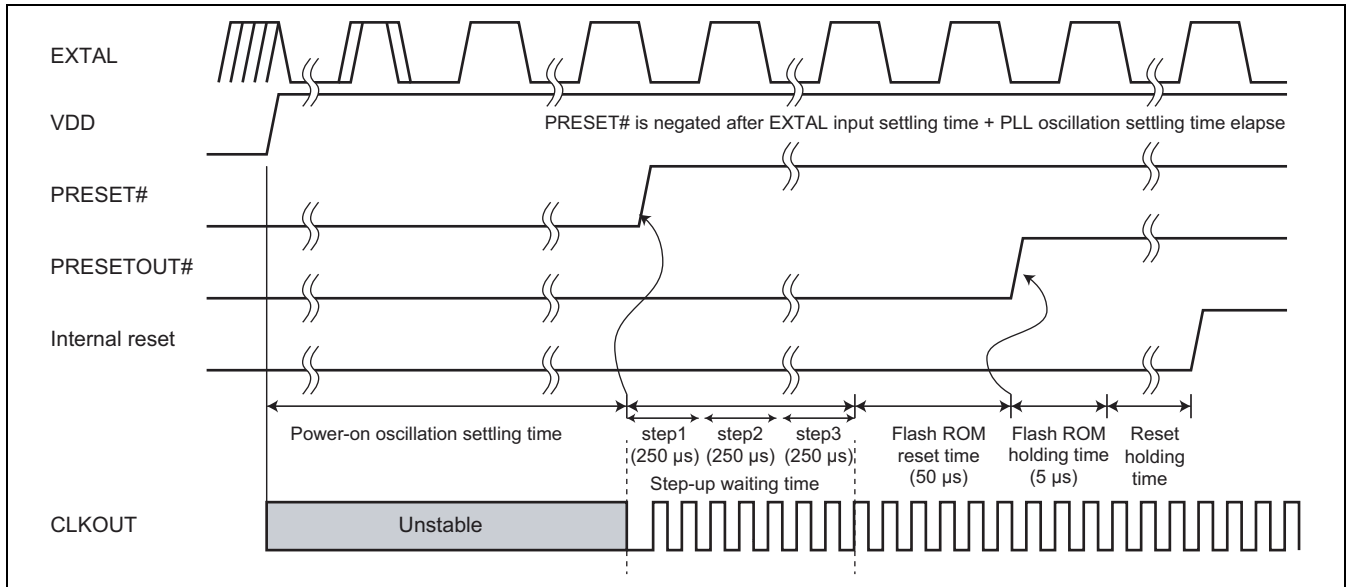


Figure 8.3 Step-Up Mode

## 8.6 Usage Notes

RZ/G1H	RZ/G1N
RZ/G1M	RZ/G1E

### 8.6.1 Usage of SYS Boot Address Register (SBAR) and SYS Boot Address Register 2 (SBAR2)

The SYS boot address register (SBAR) and SYS boot address register 2 (SBAR2) are write-only registers. Therefore read access to these registers is prohibited. Read CA7BAR\*/CA15BAR\* and CA7BAR2\*/CA15BAR2\*, if read access is required.

Note: \* Cortex-A7 is not supported by the RZ/G1M, and RZ/G1N. Cortex-A15 is not supported by the RZ/G1E.

### 8.6.2 Usage of Boot Address Register and Boot Address Register 2 (SBAR, SBAR2, CA15BAR, CA15BAR2, CA7BAR, and CA7BAR2)

The boot address register and boot address register 2 (SBAR, SBAR2, CA15BAR\*<sup>1</sup>, CA15BAR2\*<sup>1</sup>, CA7BAR\*<sup>1</sup> and CA7BAR2\*<sup>1</sup>) are not initialized by WDT reset. In the case of changing these boot address registers, the boot address must point to the address of internal RAMs. Because the internal RAMs are not initialized by WDT reset, the master boot processor can boot from them regardless of the selected boot device.

Notes: 1. Cortex-A7 is not supported by the RZ/G1M, and RZ/G1N. Cortex-A15 is not supported by the RZ/G1E.

Read WOVF bit in the register RWTCSSRA of RWDT by the program allocated on the internal RAMs pointed by the boot address registers and judge whether the cause of reset is WDT overflow or not. When the cause of reset is judged as WDT reset, apply appropriate processing, for example jump to the top address of mask ROM.



## 9. AP-System Core



RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

### 9.1 Overview

The AP-System core is a core block equipped with ARM Cortex-A7\* and ARM Cortex-A15\*. For details on the functions of Cortex-A7 and Cortex-A15, see the relevant Technical Reference Manual.

**Table 9.1 Feature of the AP-System Core Block (Cortex-A15)**

	RZ/G1H	RZ/G1M/N
Version	r3p2	r3p2
Cluster Number	Cluster 0	Cluster 0
Number of CPUs	Quad CPU	Dual CPU
L1 cache	I/ 32 KB (16 KB × 2 way) D/32 KB (16 KB × 2 way)	I/ 32 KB (16 KB × 2 way) D/32 KB (16 KB × 2 way)
L2 cache	2 MB (128 KB × 16 way)	1 MB (64 KB × 16 way)
ECC	Not supported	Not supported
MMU	Supported	Supported
NEON/VFP	NEON supported (SIMDv2) VFP supported (VFPv4)	
Operating clock	CPU core: 1.4 GHz (Zφ)	CPU core: 1.5 GHz (Zφ)
	L2-Tag RAMs: 3-divided clock of Zφ L2-Data RAMs: 4-divide clock of Zφ ACE bus: 520 MHz (ZXφ)	
Low power mode	Sleep mode (each CPU) Core standby mode (each CPU) AP-system core power down mode (CPUs and L2 cache shutdown: A3SM = OFF)	
Private peripherals	ARM Generic Timer supported	

Note: Cortex-A15 is not supported by the RZ/G1E.

**Table 9.2 Features of the AP-System Core Block (Cortex-A7)**

	<b>RZ/G1H</b>	<b>RZ/G1E</b>
Version	r0p3	r0p5
Cluster number	Cluster 1	Cluster 0
Number of CPUs	Quad CPU	Dual CPU
L1 cache (per CPU)	I/ 32 KB (16 KB × 2 way) D/32 KB (8 KB × 4 way)	I/ 32 KB (16 KB × 2 way) D/32 KB (8 KB × 4 way)
L2 cache	512 KB (64 KB × 8 way)	512 KB (64 KB × 8 way)
ECC	Not supported	Not supported
MMU	Supported	Supported
NEON/VFP	NEON supported (SIMDv2) VFP supported (VFPv4)	
Operating clock	CPU core: 780 MHz (Z2φ) L2-Tag RAMs: Z2φ L2-Data RAMs: 2-divde clock of Z2φ ACE bus: 520 MHz (ZXφ)	CPU core: 1 GHz (Z2φ)
Low power mode	Sleep mode (each CPU) Core standby mode (each CPU) AP-system core power down mode (CPUs and L2 cache shutdown: A2KL = OFF)	
Private peripherals	ARM Generic Timer supported	

Note: Cortex-A7 is not supported by the RZ/G1M, and RZ/G1N.

## 9.2 Generic Counter

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

For the general explanation about Generic Counter, and the details of the relation between Generic Counter and Generic Timer, refer to the ARM manual. In this section, it is explained that the frequency for count-up of the Generic Counter.

### 9.2.1 Frequency for Counting Up

The generic timer counts up by one every clock edge of the following frequency continuously.

**Table 9.3** Frequency for count-up

	RZ/G1H	RZ/G1M/N	RZ/G1E
Count-up clock frequency	EXTAL × 1/2	EXTAL × 1/2	ZSφ × 1/8

The operating frequency of EXTAL is decided by mode pin setting. For details, see Table 7.5, PLL Multiplication Ratio in section 7, Clock Pulse Generator (CPG).

### 9.2.2 Counter Module Control and Status Registers

The base address of counter module control and status registers is H'E6080000.

For the details of these registers, refer to the ARM manual shown below.

DDI0406C2c\_arm\_architecture\_reference\_manual Appendix D.3 Counter module control and status registers.

### 9.2.3 How to Start a Generic Counter

Set bit 0 in CNTCR to 1 to start the Generic Counter when the CPU is placed in the secure mode.

### 9.2.4 Relation with a CoreSight Timestamp

The Generic Counter serves as the CoreSight Timestamp function.

For details, refer to the ARM manual shown below.

DDI0406C2c\_arm\_architecture\_reference\_manual Appendix D.1.2 Generic Timer relationship with CoreSight Timestamp counter.

## 9.3 Power-Down Mechanism

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

### 9.3.1 Overview

The AP-System core supports the following three power-down modes.

- AP-System core power down mode  
(CPUs and L2 Cache shutdown: A3SM = OFF (Cortex-A15)/A2KL = OFF (Cortex-A7))
- Core standby mode (each CPU)\*
- Sleep mode (clock stop, each CPU)
- L2 shutdown mode

In AP-System core power down mode, the power of the AP-System core area is shut down. This mode is intended to be used at long-time wait, and achieves the reduction of power consumption including leakage current cut-off. The system boots up from the reset vector at its return from AP-System core power down mode. For detail of the AP-system core power down control, see section 61, System Controller (SYSC).

In Core standby mode, all memories including L1 cache of the relevant CPU do not keep its contents, but the power of the SRAM of level 2 cache is supplied to keep its contents.

In L2 shutdown mode, all power of CPUs and L2 is shut down. So contents of both L1s and L2 are not to be retained.

For details of Core standby mode and L2 shutdown mode, see section 7B, Advanced Power Management Unit for AP-System Core (APMU).

Note: \* In RZ/G1E case, if each CPU enter into the core standby mode, the clock supply for each CPU is stopped even if CPU core is always supplied power. After the power-on reset, the CPU other than the master CPU is in the core standby mode. When using the CPU in the core standby mode, follow the power-on sequence in order to start supply of the clock.

## 9.4 Cache Coherent Interconnect (CCI-400)

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

Cache coherent interconnect combines interconnect and coherency function. It can connect two ACE masters, three ACE-Lite masters and three ACE-Lite slaves.

### 9.4.1 Functional Registers of CCI-400

Base address of the functional registers of CCI-400 is H'F0000000. For the details of these registers, refer to the following document.

CoreLink CCI-400 Cache Coherent Interconnect Revision r0p4 Technical Reference Manual  
(DDI0470D\_cci400\_r0p4\_trm.pdf).

### 9.4.2 Maximum Outstanding Setting

CCI-400 can adjust maximum number of outstanding request as shown in Table 9.4. You must set the same or lower value listed in Table 9.4.

**Table 9.4 Maximum Number of Outstanding Request**

		RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Slave port 0	Read	32	32	32	32
	Write	32	16	16	16
Slave port 1	Read	32	32	32	32
	Write	32	16	16	16
Slave port 2	Read	32	32	32	32
	Write	32	32	32	32
Slave port 3	Read	16	16	16	16
	Write	16	16	16	16
Slave port 4	Read	32	32	32	32
	Write	32	32	32	32

### 9.4.3 System Address Map

The CCI-400 has the system address map. The address spaces defined in this map are split into 16 regions. The connection to each master port is defined by the value of ADDRMAPx[1:0] (x = 0 to 15) in advance. Table 9.5 shows System Address MAP of CCI-400. For the detail of address map, see the following document.

CoreLink CCI-400 Cache Coherent Interconnect Revision r0p4 Technical Reference Manual  
(DDI0470D\_cci400\_r0p4\_trm.pdf). 3.4 Address map

**Table 9.5 System Address Map for CCI-400**

Address Region	Address Range	Decode Value	Destination
ADDRMAP0	H'00_00000000 to H'00_1FFFFFFF	B'00	Master port 0 (SYS-AXI)
ADDRMAP1	H'00_20000000 to H'00_3FFFFFFF	B'00	Master port 0 (SYS-AXI)
ADDRMAP2	H'00_40000000 to H'00_5FFFFFFF	B'11	Master port 1/2 (DBSC3)
ADDRMAP3	H'00_60000000 to H'00_7FFFFFFF	B'11	Master port 1/2 (DBSC3)
ADDRMAP4	H'00_80000000 to H'00_9FFFFFFF	B'11	Master port 1/2 (DBSC3)
ADDRMAP5	H'00_A0000000 to H'00_BFFFFFFF	B'11	Master port 1/2 (DBSC3)
ADDRMAP6	H'00_C0000000 to H'00_DFFFFFFF	B'00	Master port 0 (SYS-AXI)
ADDRMAP7	H'00_E0000000 to H'00_FFFFFFFF	B'00	Master port 0 (SYS-AXI)
ADDRMAP8	H'01_00000000 to H'01_FFFFFFFF	B'11	Master port 1/2 (DBSC3)
ADDRMAP9	H'02_00000000 to H'03_FFFFFFFF	B'11	Master port 1/2 (DBSC3)
ADDRMAP10	H'04_00000000 to H'07_FFFFFFFF	B'11	Master port 1/2 (DBSC3)
ADDRMAP11	H'08_00000000 to H'0F_FFFFFFFF	B'00	Master port 0 (SYS-AXI)
ADDRMAP12	H'10_00000000 to H'1F_FFFFFFFF	B'00	Master port 0 (SYS-AXI)
ADDRMAP13	H'20_00000000 to H'3F_FFFFFFFF	B'00	Master port 0 (SYS-AXI)
ADDRMAP14	H'40_00000000 to H'7F_FFFFFFFF	B'00	Master port 0 (SYS-AXI)
ADDRMAP15	H'80_00000000 to H'FF_FFFFFFFF	B'00	Master port 0 (SYS-AXI)

## 9.5 Notes

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

### 9.5.1 L2 Cache Setting for Cortex-A15

Notes for L2 cache setting for Cortex-A15 are follows:

- The default value of “Tag RAM latency” is 2 cycles. You must change it to 3 cycles by accessing L2CTLR.
- The default value of “Data RAM setup” is 0 cycles. In case of RZ/G1H, you must change it to 1 cycle by accessing L2CTLR.
- The default value of “Data RAM latency” is 2 cycles. You must change it to 4 cycles by accessing L2CTLR.

**Table 9.6 L2 Cache Setting for Cortex-A15**

	RZ/G1H	RZ/G1M	RZ/G1N
Tag RAM latency (cycle)	3	3	3
Data RAM latency (cycle)	4	4	4
Data RAM setup (cycle)	1	0	0

Note: Cortex-A15 is not supported by the RZ/G1E.

## 10. Inter Connect RAM

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

### 10.1 Overview

Each RZ/G series products, RZ/G1H, RZ/G1M, RZ/G1N, and RZ/G1E provide a set of the Inter connect RAM.

### 10.2 Features

- Memory size:
  - Inter connect RAM0 : 72 Kbytes
  - Inter connect RAM1 : 4 Kbytes
  - Inter connect RAM2 : 256 Kbytes
- Undefined on power-on reset. Retained on other resets.
- Inter connect RAM take charge of buffer between CPUs.

**Table 10.1 Address Maps**

Register Name	R/W	Address	Access Size
Inter connect RAM2 direct access space	R/W	H'E630 0000 to H'E633 FFFF	8, 16, 32
Inter connect RAM0 direct access space	R/W	H'E63A 0000 to H'E63B 1FFF	8, 16, 32
Inter connect RAM1 direct access space	R/W	H'E63C 0000 to H'E63C 0FFF	8, 16, 32

Note: Do not write to any addresses other than listed above. Operations cannot be guaranteed if writing is attempted. Values read from addresses other than those listed above are undefined.



# 11. Interrupt Controller for AP-System Core (INTC-SYS)

RZ/G1H	RZ/G1N
RZ/G1M	RZ/G1E

This module handles system domain interrupt events.

## 11.1 Features

### (1) INTC-SYS

- Interrupt controller for AP-system core
- 32 programmable priority levels
- ARM-IRQ interrupt generation
- INTC-SYS peripheral interrupt

### (2) IRQC

- Common module to handle the external NMI/IRQ inputs
- Edge-triggered on rising, falling or both
- Level-sensitive on high or low values
- IRQ signal debouncing

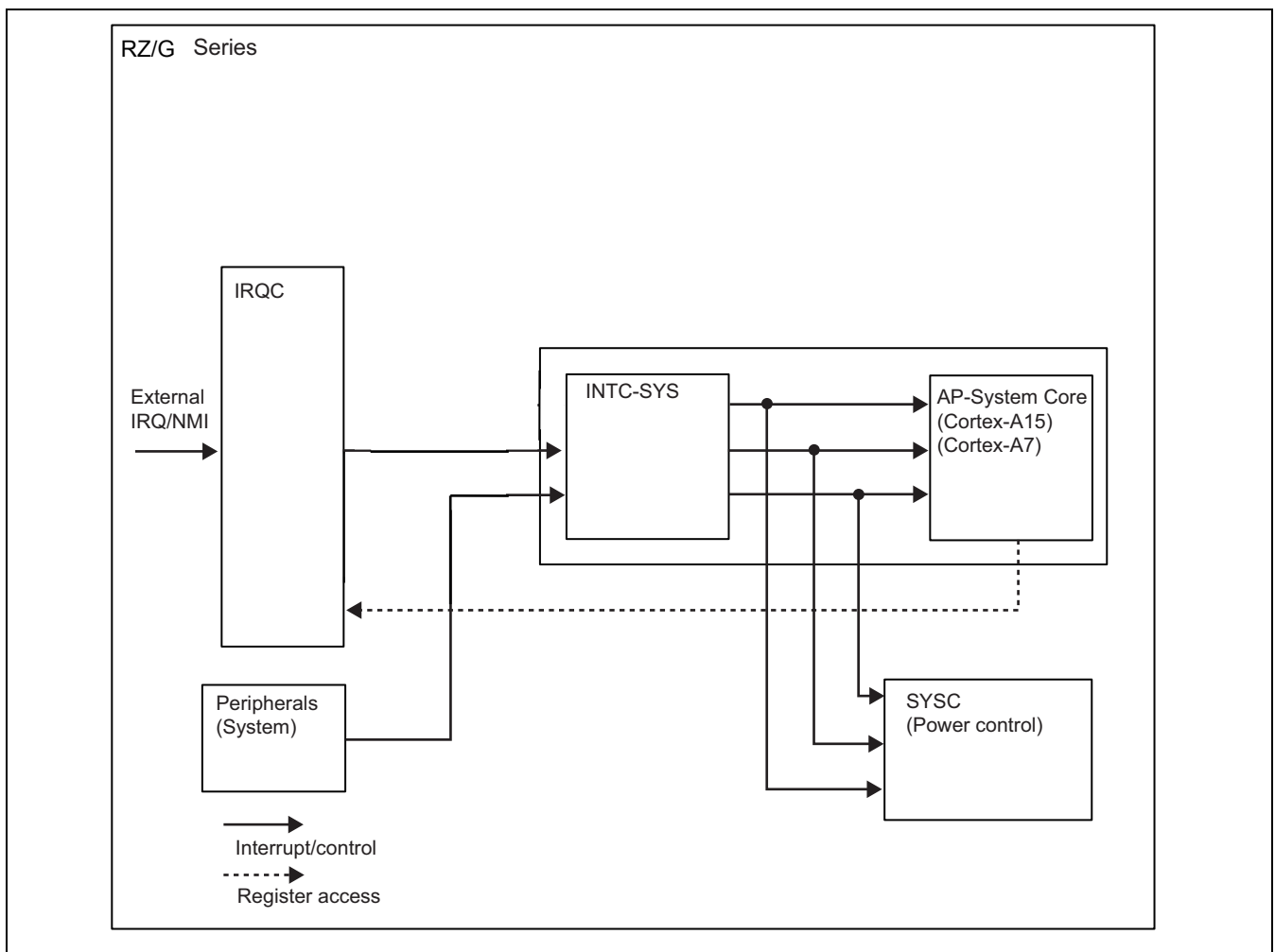


Figure 11.1 Block diagram of INTC

## 11.2 Interrupt Requests to AP-SYSTEM core

INTC-SYS is based on ARM Generic Interrupt Controller. For more information, see ARM Generic Interrupt Controller Architecture Specification and section 9, AP-System Core.

### 11.2.1 Interrupts Mapping

Table 11.1 shows the AP-system core interrupt controller (INTC-SYS) interrupt mapping.

Note: All interrupts should be level-sensitive configuration.

**Table 11.1 AP-System core (INTC-SYS) Interrupt Mapping**

SPI#	Source			
	RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
0	IRQ0	IRQ0	IRQ0	IRQ0
1	IRQ1	IRQ1	IRQ1	IRQ1
2	IRQ2	IRQ2	IRQ2	IRQ2
3	IRQ3	IRQ3	IRQ3	IRQ3
4	GPIO0	GPIO0	GPIO0	GPIO0
5	GPIO1	GPIO1	GPIO1	GPIO1
6	GPIO2	GPIO2	GPIO2	GPIO2
7	GPIO3	GPIO3	GPIO3	GPIO3
8	GPIO4	GPIO4	GPIO4	GPIO4
9	GPIO5	GPIO5	GPIO5	GPIO5
10	Reserved	GPIO6	GPIO6	GPIO6
11	Reserved	GPIO7	GPIO7	Reserved
12	Reserved	IRQ4	IRQ4	IRQ4
13	Reserved	IRQ5	IRQ5	IRQ5
14	Reserved	IRQ6	IRQ6	IRQ6
15	Reserved	IRQ7	IRQ7	IRQ7
16	Reserved	IRQ8	IRQ8	IRQ8
17	Reserved	IRQ9	IRQ9	IRQ9
18	Reserved	DCU	DCU	DCU
19	Reserved	I2C4	I2C4	I2C4
20	Reserved	I2C5	I2C5	I2C5
21	Reserved	HSCIF2	HSCIF2	HSCIF2
22	Reserved	SCIF2	SCIF2	SCIF2
23	Reserved	SCIF3	SCIF3	SCIF3
24	Reserved	SCIF4	SCIF4	SCIF4
25	Reserved	SCIF5	SCIF5	SCIF5
26	Reserved	Reserved	Reserved	Reserved
27	Reserved	Reserved	Reserved	Reserved
28	Reserved	Reserved	Reserved	Reserved
29	Reserved	SCIFA3	SCIFA3	SCIFA3
30	Reserved	SCIFA4	SCIFA4	SCIFA4
31	Reserved	SCIFA5	SCIFA5	SCIFA5

SPI#	Source			
	RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
32	Reserved	Reserved	Reserved	Reserved
33	Reserved	Reserved	Reserved	Reserved
34	Reserved	Reserved	Reserved	Reserved
35	Reserved	Reserved	Reserved	Reserved
36	Reserved	Reserved	Reserved	Reserved
37	Reserved	Reserved	Reserved	Reserved
38	Reserved	Reserved	Reserved	Reserved
39	Reserved	Reserved	Reserved	Reserved
40	Reserved	Reserved	Reserved	Reserved
41	Reserved	Reserved	Reserved	Reserved
42	Reserved	Reserved	Reserved	Reserved
43	Reserved	Reserved	Reserved	Reserved
44	Reserved	Reserved	Reserved	Reserved
45	Reserved	Reserved	Reserved	Reserved
46	Reserved	Reserved	Reserved	Reserved
47	Reserved	Reserved	Reserved	Reserved
48	Reserved	Reserved	Reserved	Reserved
49	Reserved	Reserved	Reserved	Reserved
50	Reserved	Reserved	Reserved	Reserved
51	Reserved	Reserved	Reserved	Reserved
52	Reserved	Reserved	Reserved	Reserved
53	Reserved	Reserved	Reserved	Reserved
54	Reserved	Reserved	Reserved	Reserved
55	Reserved	Reserved	Reserved	Reserved
56	Reserved	Reserved	Reserved	Reserved
57	Reserved	Reserved	Reserved	Reserved
58	Reserved	Reserved	Reserved	Reserved
59	Reserved	Reserved	Reserved	Reserved
60	Reserved	Reserved	Reserved	Reserved
61	Reserved	Reserved	Reserved	Reserved
62	Reserved	Reserved	Reserved	Reserved
63	Reserved	Reserved	Reserved	Reserved
64	Reserved	Reserved	Reserved	Reserved
65	Reserved	Reserved	Reserved	Reserved
66	Reserved	Reserved	Reserved	Reserved
67	Reserved	Reserved	Reserved	Reserved
68	Reserved	Reserved	Reserved	Reserved
69	THS	THS	THS	Reserved
70	Reserved	Reserved	Reserved	Reserved
71	Reserved	Reserved	Reserved	Reserved
72	CA15_IRQPNU- Core0	CA15_IRQPNU- Core0	CA15_IRQPNU- Core0	Reserved

SPI#	Source			
	RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
73	CA15_IRQPNU-Core1	CA15_IRQPNU-Core1	CA15_IRQPNU-Core1	Reserved
74	CA15_IRQPNU-Core2	Reserved	Reserved	Reserved
75	CA15_IRQPNU-Core3	Reserved	Reserved	Reserved
76	CA15_CTIIRQ-Core0	CA15_CTIIRQ-Core0	CA15_CTIIRQ-Core0	Reserved
77	CA15_CTIIRQ-Core1	CA15_CTIIRQ-Core1	CA15_CTIIRQ-Core1	Reserved
78	CA15_CTIIRQ-Core2	Reserved	Reserved	Reserved
79	CA15_CTIIRQ-Core3	Reserved	Reserved	Reserved
80	CA15_nINTERRIRQ	CA15_nINTERRIRQ	CA15_nINTERRIRQ	Reserved
81	CA15_nAXIERRIRQ	CA15_nAXIERRIRQ	CA15_nAXIERRIRQ	Reserved
82	CA7_IRQPMU-Core0	Reserved	Reserved	CA7_IRQPMU-Core0
83	CA7_IRQPMU-Core1	Reserved	Reserved	CA7_IRQPMU-Core1
84	CA7_IRQPMU-Core2	Reserved	Reserved	Reserved
85	CA7_IRQPMU-Core3	Reserved	Reserved	Reserved
86	CA7_CTIIRQ-Core0	Reserved	Reserved	CA7_CTIIRQ-Core0
87	CA7_CTIIRQ-Core1	Reserved	Reserved	CA7_CTIIRQ-Core1
88	CA7_CTIIRQ-Core2	Reserved	Reserved	Reserved
89	CA7_CTIIRQ-Core3	Reserved	Reserved	Reserved
90	Reserved	Reserved	Reserved	Reserved
91	CA7_nAXIERRIRQ	Reserved	Reserved	CA7_nAXIERRIRQ
92	CCI400	CCI400	CCI400	CCI400
93	CCI400_OVF	CCI400_OVF	CCI400_OVF	CCI400_OVF
94	Reserved	Reserved	Reserved	Reserved
95	Reserved	Reserved	Reserved	Reserved
96	LBSC-WT0	LBSC-WT0	LBSC-WT0	LBSC-WT0
97	LBSC-ATA	LBSC-ATA	LBSC-ATA	LBSC-ATA
98	LBSC-DMAC0	LBSC-DMAC0	LBSC-DMAC0	LBSC-DMAC0
99	LBSC-DMAC1	LBSC-DMAC1	LBSC-DMAC1	LBSC-DMAC1
100	LBSC-DMAC2	LBSC-DMAC2	LBSC-DMAC2	LBSC-DMAC2
101	USB3.0H_HOST	USB3.0H_HOST	USB3.0H_HOST	Reserved
102	Reserved	Reserved	Reserved	Reserved
103	Reserved	Reserved	Reserved	Reserved
104	Reserved	Reserved	Reserved	Reserved
105	SATA0	SATA0	SATA0	Reserved
106	SATA1	SATA1	SATA1	Reserved
107	USB2.0_597 (OTG)	USB2.0_597 (OTG)	USB2.0_597 (OTG)	USB2.0_597 (OTG)

SPI#	Source			
	RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
108	USB2.0 HOST 0	USB2.0 HOST 0	USB2.0 HOST 0	USB2.0 HOST 0
109	USB-DMAC ch.0	USB-DMAC ch.0	USB-DMAC ch.0	USB-DMAC ch.0
110	USB-DMAC ch.1	USB-DMAC ch.1	USB-DMAC ch.1	USB-DMAC ch.1
111	USB-DMAC (DDM)	USB-DMAC (DDM)	USB-DMAC (DDM)	USB-DMAC (DDM)
112	USB2.0 HOST 1	Reserved	Reserved	Reserved
113	USB2.0 HOST 2	USB2.0 HOST 1	USB2.0 HOST 1	USB2.0 HOST 1
114	R-GP2D	Reserved	Reserved	Reserved
115	Reserved	Reserved	Reserved	Reserved
116	PCIEC	PCIEC	PCIEC	Reserved
117	PCIEC_DMA	PCIEC_DMA	PCIEC_DMA	Reserved
118	PCIEC_ERROR	PCIEC_ERROR	PCIEC_ERROR	Reserved
119	PowerVR G6400	SGX544MP2	SGX544MP2	SGX540
120	CMT1_0	CMT1_0	CMT1_0	CMT1_0
121	CMT1_1	CMT1_1	CMT1_1	CMT1_1
122	CMT1_2	CMT1_2	CMT1_2	CMT1_2
123	CMT1_3	CMT1_3	CMT1_3	CMT1_3
124	CMT1_4	CMT1_4	CMT1_4	CMT1_4
125	CMT1_5	CMT1_5	CMT1_5	CMT1_5
126	CMT1_6	CMT1_6	CMT1_6	CMT1_6
127	CMT1_7	CMT1_7	CMT1_7	CMT1_7
128	TMU1_TUNI0	TMU1_TUNI0	TMU1_TUNI0	TMU1_TUNI0
129	TMU1_TUNI1	TMU1_TUNI1	TMU1_TUNI1	TMU1_TUNI1
130	TMU1_TUNI2	TMU1_TUNI2	TMU1_TUNI2	TMU1_TUNI2
131	TMU3_TUNI0	TMU3_TUNI0	TMU3_TUNI0	TMU3_TUNI0
132	TMU3_TUNI1	TMU3_TUNI1	TMU3_TUNI1	TMU3_TUNI1
133	TMU3_TUNI2	TMU3_TUNI2	TMU3_TUNI2	TMU3_TUNI2
134	Reserved	Reserved	Reserved	Reserved
135	TPU	TPU	TPU	TPU
136	TMU0_TUNI0	TMU0_TUNI0	TMU0_TUNI0	TMU0_TUNI0
137	TMU0_TUNI1	TMU0_TUNI1	TMU0_TUNI1	TMU0_TUNI1
138	TMU0_TUNI2	TMU0_TUNI2	TMU0_TUNI2	TMU0_TUNI2
139	Reserved	Reserved	Reserved	Reserved
140	RWDT	RWDT	RWDT	RWDT
141	Reserved	Reserved	Reserved	Reserved
142	CMT0_0	CMT0_0	CMT0_0	CMT0_0
143	CMT0_1	CMT0_1	CMT0_1	CMT0_1
144	SCIFA0	SCIFA0	SCIFA0	SCIFA0
145	SCIFA1	SCIFA1	SCIFA1	SCIFA1
146	Reserved	Reserved	Reserved	Reserved
147	TMU1_TUNI3	TMU1_TUNI3	TMU1_TUNI3	TMU1_TUNI3
148	SCIFB0	SCIFB0	SCIFB0	SCIFB0
149	SCIFB1	SCIFB1	SCIFB1	SCIFB1
150	SCIFB2	SCIFB2	SCIFB2	SCIFB2

SPI#	Source			
	RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
151	SCIFA2	SCIFA2	SCIFA2	SCIFA2
152	SCIF0	SCIF0	SCIF0	SCIF0
153	SCIF1	SCIF1	SCIF1	SCIF1
154	HSCIF0	HSCIF0	HSCIF0	HSCIF0
155	HSCIF1	HSCIF1	HSCIF1	HSCIF1
156	MSIOF0	MSIOF0	MSIOF0	MSIOF0
157	MSIOF1	MSIOF1	MSIOF1	MSIOF1
158	MSIOF2	MSIOF2	MSIOF2	MSIOF2
159	MSIOF3	Reserved	Reserved	Reserved
160	Reserved	Reserved	Reserved	Reserved
161	Reserved	Reserved	Reserved	Reserved
162	Ethernet MAC (Fast Ether)	Ethernet MAC (Fast Ether)	Ethernet MAC (Fast Ether)	Ethernet MAC (Fast Ether)
163	Ethernet AVB	Ethernet AVB	Ethernet AVB	Ethernet AVB
164	SCIF2	Reserved	Reserved	Reserved
165	SDHI0	SDHI0	SDHI0	SDHI0
166	SDHI1	Reserved	Reserved	Reserved
167	SDHI2	SDHI2	SDHI2	SDHI2
168	SDHI3	SDHI3	SDHI3	SDHI3
169	MMC0	MMC0	MMC0	MMC0
170	MMC1	Reserved	Reserved	Reserved
171	Reserved	Reserved	Reserved	Reserved
172	Reserved	Reserved	Reserved	Reserved
173	IIC3	IIC3	IIC3	Reserved
174	IIC0	IIC0	IIC0	IIC0
175	IIC1	IIC1	IIC1	IIC1
176	IIC2	Reserved	Reserved	Reserved
177	Reserved	Reserved	Reserved	Reserved
178	Reserved	Reserved	Reserved	Reserved
179	Reserved	Reserved	Reserved	Reserved
180	Reserved	Reserved	Reserved	Reserved
181	Reserved	Reserved	Reserved	Reserved
182	Reserved	Reserved	Reserved	Reserved
183	Reserved	Reserved	Reserved	Reserved
184	QSPI	QSPI	QSPI	QSPI
185	Reserved	Reserved	Reserved	Reserved
186	CAN interface 0	CAN interface 0	CAN interface 0	CAN interface 0
187	CAN interface 1	CAN interface 1	CAN interface 1	CAN interface 1
188	VIN0	VIN0	VIN0	VIN0
189	VIN1	VIN1	VIN1	VIN1
190	VIN2	VIN2	VIN2	VIN2
191	VIN3	Reserved	Reserved	Reserved
192	IMR-X2_0	Reserved	Reserved	Reserved

SPI#	Source			
	RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
193	IMR-X2_1	Reserved	Reserved	Reserved
194	IMR-LSX2_0	Reserved	Reserved	Reserved
195	IMR-LSX2_1	Reserved	Reserved	Reserved
196	Reserved	Reserved	Reserved	Reserved
197	SYS-DMAC0_ERR	SYS-DMAC0_ERR	SYS-DMAC0_ERR	SYS-DMAC0_ERR
198	IPMMUDS0	IPMMUDS0	IPMMUDS	IPMMUDS
199	IPMMUDS0(SEC)	IPMMUDS0(SEC)	IPMMUDS(SEC)	IPMMUDS(SEC)
200	SYS-DMAC_DEI0	SYS-DMAC_DEI0	SYS-DMAC_DEI0	SYS-DMAC_DEI0
201	SYS-DMAC_DEI1	SYS-DMAC_DEI1	SYS-DMAC_DEI1	SYS-DMAC_DEI1
202	SYS-DMAC_DEI2	SYS-DMAC_DEI2	SYS-DMAC_DEI2	SYS-DMAC_DEI2
203	SYS-DMAC_DEI3	SYS-DMAC_DEI3	SYS-DMAC_DEI3	SYS-DMAC_DEI3
204	DMAC_DEI4	SYS-DMAC_DEI4	SYS-DMAC_DEI4	SYS-DMAC_DEI4
205	SYS-DMAC_DEI5	SYS-DMAC_DEI5	SYS-DMAC_DEI5	SYS-DMAC_DEI5
206	SYS-DMAC_DEI6	SYS-DMAC_DEI6	SYS-DMAC_DEI6	SYS-DMAC_DEI6
207	SYS-DMAC_DEI7	SYS-DMAC_DEI7	SYS-DMAC_DEI7	SYS-DMAC_DEI7
208	SYS-DMAC_DEI8	SYS-DMAC_DEI8	SYS-DMAC_DEI8	SYS-DMAC_DEI8
209	SYS-DMAC_DEI9	SYS-DMAC_DEI9	SYS-DMAC_DEI9	SYS-DMAC_DEI9
210	SYS-DMAC_DEI10	SYS-DMAC_DEI10	SYS-DMAC_DEI10	SYS-DMAC_DEI10
211	SYS-DMAC_DEI11	SYS-DMAC_DEI11	SYS-DMAC_DEI11	SYS-DMAC_DEI11
212	SYS-DMAC_DEI12	SYS-DMAC_DEI12	SYS-DMAC_DEI12	SYS-DMAC_DEI12
213	SYS-DMAC_DEI13	SYS-DMAC_DEI13	SYS-DMAC_DEI13	SYS-DMAC_DEI13
214	SYS-DMAC_DEI14	SYS-DMAC_DEI14	SYS-DMAC_DEI14	SYS-DMAC_DEI14
215	Reserved	Reserved	Reserved	Reserved
216	SYS-DMAC_DEI15	SYS-DMAC_DEI15	SYS-DMAC_DEI15	SYS-DMAC_DEI15
217	SYS-DMAC_DEI16	SYS-DMAC_DEI16	SYS-DMAC_DEI16	SYS-DMAC_DEI16
218	SYS-DMAC_DEI17	SYS-DMAC_DEI17	SYS-DMAC_DEI17	SYS-DMAC_DEI17
219	SYS-DMAC_DEI18	SYS-DMAC_DEI18	SYS-DMAC_DEI18	SYS-DMAC_DEI18
220	SYS-DMAC1_ERR	SYS-DMAC1_ERR	SYS-DMAC1_ERR	SYS-DMAC1_ERR
221	IPMMU_M (SEC)	IPMMU_M (SEC)	IPMMU_M (SEC)	IPMMU_M (SEC)
222	IPMMU_M	IPMMU_M	IPMMU_M	IPMMU_M
223	IPMMU_SY0	IPMMU_SY0	IPMMU_SY0	IPMMU_SY0
224	IPMMU_SY0 (SEC)	IPMMU_SY0 (SEC)	IPMMU_SY0 (SEC)	IPMMU_SY0 (SEC)
225	IPMMU_SY1	IPMMU_SY1	IPMMU_SY1	IPMMU_SY1
226	IPMMU_MP	IPMMU_MP	IPMMU_MP	IPMMU_MP
227	Reserved	Reserved	Reserved	Reserved
228	Reserved	Reserved	Reserved	Reserved
229	Reserved	Reserved	Reserved	Reserved
230	Reserved	Reserved	Reserved	Reserved
231	Reserved	Reserved	Reserved	Reserved
232	Reserved	Reserved	Reserved	Reserved
233	CoreSight (RT)	CoreSight (RT)	CoreSight (RT)	CoreSight (RT)
234	APMU1	APMU1	APMU1	APMU1
235	Reserved	Reserved	Reserved	Reserved

SPI#	Source			
	RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
236	Reserved	Reserved	Reserved	Reserved
237	Reserved	Reserved	Reserved	Reserved
238	Reserved	Reserved	Reserved	Reserved
239	Reserved	Reserved	Reserved	Reserved
240	Reserved	Reserved	Reserved	Reserved
241	Reserved	Reserved	Reserved	Reserved
242	Reserved	Reserved	Reserved	Reserved
243	Reserved	Reserved	Reserved	Reserved
244	CPG	CPG	CPG	CPG
245	APMU0	APMU0	APMU0	APMU0
246	VSPD0	VSPD0	VSPD0	VSPD0
247	VSPD1	VSPD1	VSPD1	VSPD1
248	GPIO0 (ALT)	GPIO0 (ALT)	GPIO0 (ALT)	GPIO0 (ALT)
249	GPIO1 (ALT)	GPIO1 (ALT)	GPIO1 (ALT)	GPIO1 (ALT)
250	GPIO2 (ALT)	GPIO2 (ALT)	GPIO2 (ALT)	GPIO2 (ALT)
251	GPIO3 (ALT)	GPIO3 (ALT)	GPIO3 (ALT)	GPIO3 (ALT)
252	GPIO4 (ALT)	GPIO4 (ALT)	GPIO4 (ALT)	GPIO4 (ALT)
253	GPIO5 (ALT)	GPIO5 (ALT)	GPIO5 (ALT)	GPIO5 (ALT)
254	Reserved	GPIO6 (ALT)	GPIO6 (ALT)	GPIO6 (ALT)
255	Reserved	GPIO7 (ALT)	GPIO7 (ALT)	Reserved
256	DU0	DU0	DU0	DU0
257	DRC	Reserved	Reserved	Reserved
258	VCP3_VLC ch.0	VCP3_VLC ch.0	VCP3_VLC ch.0	VCP3_VLC ch.0
259	VCP3_CE ch.0	VCP3_CE ch.0	VCP3_CE ch.0	VCP3_CE ch.0
260	VCP3_VLC ch.1	IPMMU-GP	IPMMU-GP	IPMMU-GP
261	VCP3_CE ch.1	IPMMU-GP (SEC)	IPMMU-GP (SEC)	IPMMU-GP (SEC)
262	FDP1 ch.0	FDP1 ch.0	FDP1 ch.0	FDP1 ch.0
263	FDP1 ch.1	FDP1 ch.1	FDP1.ch.1	Reserved
264	FDP1 ch.2	Reserved	Reserved	Reserved
265	Reserved	Reserved	Reserved	Reserved
266	VSPR	Reserved	Reserved	Reserved
267	VSPS	VSPS	VSPS	VSPS
268	DU1	DU1	DU1	DU1
269	DU2	Reserved	Reserved	Reserved
270	Reserved	Reserved	Reserved	Reserved
271	Reserved	Reserved	Reserved	Reserved
272	Reserved	Reserved	Reserved	Reserved
273	Reserved	Reserved	Reserved	Reserved
274	Reserved	Reserved	Reserved	Reserved
275	Reserved	Reserved	Reserved	Reserved
276	Reserved	Reserved	Reserved	Reserved
277	Reserved	Reserved	Reserved	Reserved
278	Reserved	Reserved	Reserved	Reserved



SPI#	Source			
	RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
279	Reserved	Reserved	Reserved	Reserved
280	Reserved	Reserved	Reserved	Reserved
281	Reserved	Reserved	Reserved	Reserved
282	Reserved	Reserved	Reserved	Reserved
283	Reserved	TSIF0	Reserved	Reserved
284	Reserved	Reserved	Reserved	Reserved
285	2D-DMAC	2D-DMAC	2D-DMAC	2D-DMAC
286	I2C2	I2C2	I2C2	I2C2
287	I2C0	I2C0	I2C0	I2C0
288	I2C1	I2C1	I2C1	I2C1
289	Reserved	Reserved	Reserved	Reserved
290	I2C3	I2C3	I2C3	I2C3
291	Reserved	Reserved	Reserved	Reserved
292	Reserved	Reserved	Reserved	Reserved
293	Reserved	Reserved	Reserved	Reserved
294	Reserved	Reserved	Reserved	Reserved
295	Reserved	Reserved	Reserved	Reserved
296	Reserved	Reserved	Reserved	Reserved
297	SYSC	SYSC	SYSC	SYSC
298	Reserved	Reserved	Reserved	Reserved
299	Reserved	Reserved	Reserved	Reserved
300	Reserved	Reserved	Reserved	Reserved
301	Reserved	Reserved	Reserved	Reserved
302	Reserved	Reserved	Reserved	Reserved
303	TMU2_TUNI0	TMU2_TUNI0	TMU2_TUNI0	TMU2_TUNI0
304	TMU2_TUNI1	TMU2_TUNI1	TMU2_TUNI1	TMU2_TUNI1
305	TMU2_TUNI2	TMU2_TUNI2	TMU2_TUNI2	TMU2_TUNI2
306	TMU2_TUNI3	TMU2_TUNI3	TMU2_TUNI3	TMU2_TUNI3
307	Reserved	Reserved	Reserved	Reserved
308	SYS-DMAC_DEI19	SYS-DMAC_DEI19	SYS-DMAC_DEI19	SYS-DMAC_DEI19
309	SYS-DMAC_DEI20	SYS-DMAC_DEI20	SYS-DMAC_DEI20	SYS-DMAC_DEI20
310	SYS-DMAC_DEI21	SYS-DMAC_DEI21	SYS-DMAC_DEI21	SYS-DMAC_DEI21
311	SYS-DMAC_DEI22	SYS-DMAC_DEI22	SYS-DMAC_DEI22	SYS-DMAC_DEI22
312	SYS-DMAC_DEI23	SYS-DMAC_DEI23	SYS-DMAC_DEI23	SYS-DMAC_DEI23
313	SYS-DMAC_DEI24	SYS-DMAC_DEI24	SYS-DMAC_DEI24	SYS-DMAC_DEI24
314	SYS-DMAC_DEI25	SYS-DMAC_DEI25	SYS-DMAC_DEI25	SYS-DMAC_DEI25
315	SYS-DMAC_DEI26	SYS-DMAC_DEI26	SYS-DMAC_DEI26	SYS-DMAC_DEI26
316	SYS-DMAC_DEI27	SYS-DMAC_DEI27	SYS-DMAC_DEI27	SYS-DMAC_DEI27
317	SYS-DMAC_DEI28	SYS-DMAC_DEI28	SYS-DMAC_DEI28	SYS-DMAC_DEI28
318	SYS-DMAC_DEI29	SYS-DMAC_DEI29	SYS-DMAC_DEI29	SYS-DMAC_DEI29
319	Reserved	Reserved	Reserved	Reserved
320	AUDIO-DMAC_DEI0	AUDIO-DMAC_DEI0	AUDIO-DMAC_DEI0	AUDIO-DMAC_DEI0

SPI#	Source			
	RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
321	AUDIO-DMAC_DEI1	AUDIO-DMAC_DEI1	AUDIO-DMAC_DEI1	AUDIO-DMAC_DEI1
322	AUDIO-DMAC_DEI2	AUDIO-DMAC_DEI2	AUDIO-DMAC_DEI2	AUDIO-DMAC_DEI2
323	AUDIO-DMAC_DEI3	AUDIO-DMAC_DEI3	AUDIO-DMAC_DEI3	AUDIO-DMAC_DEI3
324	AUDIO-DMAC_DEI4	AUDIO-DMAC_DEI4	AUDIO-DMAC_DEI4	AUDIO-DMAC_DEI4
325	AUDIO-DMAC_DEI5	AUDIO-DMAC_DEI5	AUDIO-DMAC_DEI5	AUDIO-DMAC_DEI5
326	AUDIO-DMAC_DEI6	AUDIO-DMAC_DEI6	AUDIO-DMAC_DEI6	AUDIO-DMAC_DEI6
327	AUDIO-DMAC_DEI7	AUDIO-DMAC_DEI7	AUDIO-DMAC_DEI7	AUDIO-DMAC_DEI7
328	AUDIO-DMAC_DEI8	AUDIO-DMAC_DEI8	AUDIO-DMAC_DEI8	AUDIO-DMAC_DEI8
329	AUDIO-DMAC_DEI9	AUDIO-DMAC_DEI9	AUDIO-DMAC_DEI9	AUDIO-DMAC_DEI9
330	AUDIO-DMAC_DEI10	AUDIO-DMAC_DEI10	AUDIO-DMAC_DEI10	AUDIO-DMAC_DEI10
331	AUDIO-DMAC_DEI11	AUDIO-DMAC_DEI11	AUDIO-DMAC_DEI11	AUDIO-DMAC_DEI11
332	AUDIO-DMAC_DEI12	AUDIO-DMAC_DEI12	AUDIO-DMAC_DEI12	AUDIO-DMAC_DEI12
333	AUDIO-DMAC_DEI13	AUDIO-DMAC_DEI13	AUDIO-DMAC_DEI13	Reserved
334	AUDIO-DMAC_DEI14	AUDIO-DMAC_DEI14	AUDIO-DMAC_DEI14	Reserved
335	AUDIO-DMAC_DEI15	AUDIO-DMAC_DEI15	AUDIO-DMAC_DEI15	Reserved
336	AUDIO-DMAC_DEI16	AUDIO-DMAC_DEI16	AUDIO-DMAC_DEI16	Reserved
337	AUDIO-DMAC_DEI17	AUDIO-DMAC_DEI17	AUDIO-DMAC_DEI17	Reserved
338	AUDIO-DMAC_DEI18	AUDIO-DMAC_DEI18	AUDIO-DMAC_DEI18	Reserved
339	AUDIO-DMAC_DEI19	AUDIO-DMAC_DEI19	AUDIO-DMAC_DEI19	Reserved
340	AUDIO-DMAC_DEI20	AUDIO-DMAC_DEI20	AUDIO-DMAC_DEI20	Reserved
341	AUDIO-DMAC_DEI21	AUDIO-DMAC_DEI21	AUDIO-DMAC_DEI21	Reserved
342	AUDIO-DMAC_DEI22	AUDIO-DMAC_DEI22	AUDIO-DMAC_DEI22	Reserved
343	AUDIO-DMAC_DEI23	AUDIO-DMAC_DEI23	AUDIO-DMAC_DEI23	Reserved
344	AUDIO-DMAC_DEI24	AUDIO-DMAC_DEI24	AUDIO-DMAC_DEI24	Reserved
345	AUDIO-DMAC_DEI25	AUDIO-DMAC_DEI25	AUDIO-DMAC_DEI25	Reserved

SPI#	Source			
	RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
346	AUDIO-DMAC0_ERR	AUDIO-DMAC0_ERR	AUDIO-DMAC0_ERR	AUDIO-DMAC0_ERR
347	AUDIO-DMAC1_ERR	AUDIO-DMAC1_ERR	AUDIO-DMAC1_ERR	Reserved
348	Reserved	Reserved	Reserved	Reserved
349	Reserved	Reserved	Reserved	Reserved
350	Reserved	Reserved	Reserved	Reserved
351	Reserved	Reserved	Reserved	Reserved
352	SCU0	SCU0	SCU0	Reserved
353	SCU1	SCU1	SCU1	SCU1
354	SCU2	SCU2	SCU2	SCU2
355	SCU3	SCU3	SCU3	SCU3
356	SCU4	SCU4	SCU4	SCU4
357	SCU5	SCU5	SCU5	SCU5
358	SCU6	SCU6	SCU6	SCU6
359	SCU7	SCU7	SCU7	Reserved
360	SCU8	SCU8	SCU8	Reserved
361	SCU9	SCU9	SCU9	Reserved
362	Reserved	Reserved	Reserved	Reserved
363	Reserved	Reserved	Reserved	Reserved
364	Reserved	Reserved	Reserved	Reserved
365	Reserved	Reserved	Reserved	Reserved
366	Reserved	Reserved	Reserved	Reserved
367	Reserved	Reserved	Reserved	Reserved
368	Reserved	Reserved	Reserved	Reserved
369	Reserved	Reserved	Reserved	Reserved
370	SSI0	SSI0	SSI0	SSI0
371	SSI1	SSI1	SSI1	SSI1
372	SSI2	SSI2	SSI2	SSI2
373	SSI3	SSI3	SSI3	SSI3
374	SSI4	SSI4	SSI4	SSI4
375	SSI5	SSI5	SSI5	SSI5
376	SSI6	SSI6	SSI6	SSI6
377	SSI7	SSI7	SSI7	SSI7
378	SSI8	SSI8	SSI8	SSI8
379	SSI9	SSI9	SSI9	SSI9
380	S3\$ Controller	S3\$ Controller	S3\$ Controller	S3\$ Controller
381	Reserved	Reserved	Reserved	Reserved
382	Reserved	Reserved	Reserved	Reserved
383	Reserved	Reserved	Reserved	Reserved

## 11.3 Register Descriptions

This section describes the registers of INTC-SYS.

Module Name	Base Address
INTC-SYS CPU-IF	H'F100_2000
INTC-SYS Distributer-IF	H'F100_1000

### 11.3.1 INTC-SYS Register Configuration and Function Description

384 SPI interrupts are integrated into ID[415:32].

The INTC-SYS supports two CPU cores which are mapped as shown below.

	RZ/G1H	RZ/G1M/N	RZ/G1E
CPU0 interface	AP-System core (Cortex-A15) CPU0	AP-System core (Cortex-A15) CPU0	AP-System core (Cortex-A7) CPU0
CPU1 interface	AP-System core (Cortex-A15) CPU1	AP-System core (Cortex-A15) CPU1	AP-System core (Cortex-A7) CPU1
CPU2 interface	AP-System core (Cortex-A15) CPU2	Reserved	Reserved
CPU3 interface	AP-System core (Cortex-A15) CPU3	Reserved	Reserved
CPU4 interface	AP-System core (Cortex-A7) CPU0	Reserved	Reserved
CPU5 interface	AP-System core (Cortex-A7) CPU1	Reserved	Reserved
CPU6 interface	AP-System core (Cortex-A7) CPU2	Reserved	Reserved
CPU7 interface	AP-System core (Cortex-A7) CPU3	Reserved	Reserved

For more information of these registers, see ARM Cortex-A15/Cortex-A7 Technical Reference Manual and ARM GIC-400 Generic Interrupt Controller Technical Reference Manual.

## 11.4 External Interrupt Controller (IRQC)

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

The IRQC is a common sub-module of interrupt controllers. This sub-module provides interrupt from external device and inter-domain communication.

### 11.4.1 Input/Output Pins

Table 11.2 shows the INTC pin configuration.

**Table 11.2 Pin Configuration**

Pin Name	Function	I/O	Description
IRQn (n = 0 to 3) RZ/G1H (n = 0 to 9) RZ/G1M/N, E	External interrupt input pins	Input	Input of IRQn interrupt request signals from external device. All IRQ signals are always active.
NMI	External non maskable Interrupt input pins	Input	Input of NMI interrupt request signal from external device.

### 11.4.2 Clocking and Pulse Width

This module uses 2 clocks:

Module clock: CP $\phi$ .

Debounce clock: RCLK.

Because of sampling operation, the minimum pulse width on IRQ request signal is five module clock cycles.

### 11.4.3 Block Diagram

Figures 11.2 and 11.3 are block diagrams of IRQC.

The event detector block detects external IRQn, and supports noise reduction and edge detection.

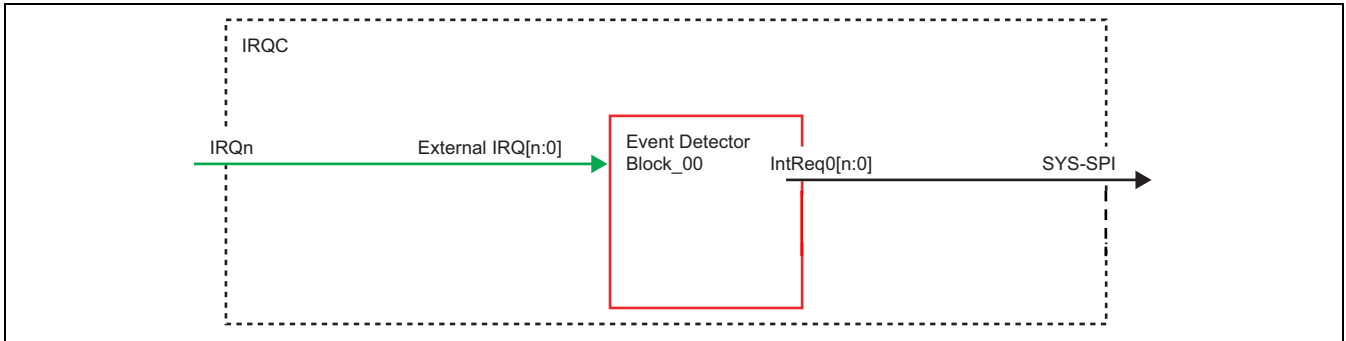


Figure 11.2 IRQC Block Diagram1

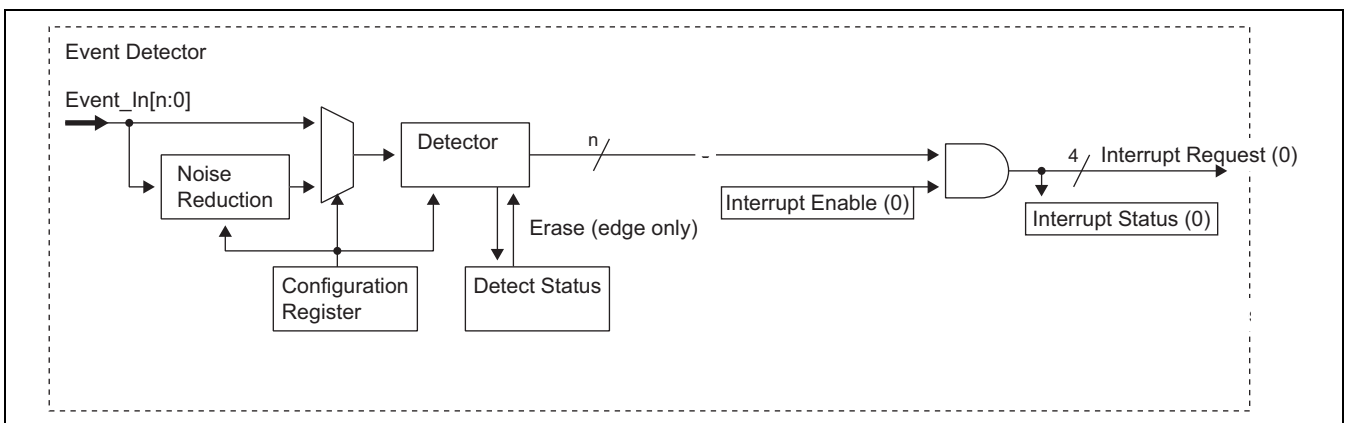


Figure 11.3 IRQC Event Detector

### 11.4.4 Register Descriptions

Table 11.3 shows the base address of each block and Tables 11.4 to 11.6 show register configuration.

**Table 11.3 IRQC Base Address**

Module Name	Base Address
IRQC	H'E61C 0000
IRQC event detector block	H'E61C 0000
NMI event detector block	H'E61C 0400
NMI mask lock block	H'E61C 0A00

**Table 11.4 IRQC Event Detector Register Configuration**

Register Name	Abbreviation	R/W	Address Offset	Access Size	RZ/G Series Products			
					RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Interrupt request status register 0	INTREQ_STS0	R	H'000	32	√	√	√	√
Interrupt enable status register 0	INTEN_STS0	R/WC1	H'004	32	√	√	√	√
Interrupt enable set register 0	INTEN_SET0	W	H'008	32	√	√	√	√
IRQn detect status register	DETECT_STATUS	R/WC1	H'100	32	√	√	√	√
IRQn signal level monitor register	MONITOR	R	H'104	32	√	√	√	√
IRQn high level detect status register	HLVL_STS	R	H'108	32	√	√	√	√
IRQn low level detect status register	LLVL_STS	R	H'10C	32	√	√	√	√
IRQn sync rising edge detect status register	S_R_EDGE_STS	R	H'110	32	√	√	√	√
IRQn sync falling edge detect status register	S_F_EDGE_STS	R	H'114	32	√	√	√	√
IRQn async rising edge detect status register	A_R_EDGE_STS	R	H'118	32	√	√	√	√
IRQn async falling edge detect status register	A_F_EDGE_STS	R	H'11C	32	√	√	√	√
IRQn Chattering reduction status register	CHTEN_STS	R	H'120	32	√	√	√	√
IRQ0 configuration register	CONFIG_00	R/W	H'180	32	√	√	√	√
IRQ1 configuration register	CONFIG_01	R/W	H'184	32	√	√	√	√
IRQ2 configuration register	CONFIG_02	R/W	H'188	32	√	√	√	√
IRQ3 configuration register	CONFIG_03	R/W	H'18C	32	√	√	√	√
IRQ4 configuration register	CONFIG_04	R/W	H'190	32	—	√	√	√
IRQ5 configuration register	CONFIG_05	R/W	H'194	32	—	√	√	√
IRQ6 configuration register	CONFIG_06	R/W	H'198	32	—	√	√	√
IRQ7 configuration register	CONFIG_07	R/W	H'19C	32	—	√	√	√
IRQ8 configuration register	CONFIG_08	R/W	H'1A0	32	—	√	√	√
IRQ9 configuration register	CONFIG_09	R/W	H'1A4	32	—	√	√	√

**Table 11.5 NMI Event Detector Register Configuration**

					<u>RZ/G Series Products</u>			
Register Name	Abbreviation	R/W	Address Offset	Access Size	RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
NMI request status register 0	NMIREQ_STS0	R	H'000	32	√	√	√	√
NMI enable status register 0	NMIEN_STS0	R/WC1	H'004	32	√	√	√	√
NMI enable set register 0	NMIEN_SET0	W	H'008	32	√	√	√	√
NMI detect status register	DETECT_STATUS_NMI	R/WC1	H'100	32	√	√	√	√
NMI signal level monitor register	MONITOR_NMI	R	H'104	32	√	√	√	√
NMI high level detect status register	HLVL_STS_NMI	R	H'108	32	√	√	√	√
NMI low level detect status register	LLVL_STS_NMI	R	H'10C	32	√	√	√	√
NMI sync rising edge detect status register	S_R_EDGE_STS_NMI	R	H'110	32	√	√	√	√
NMI sync falling edge detect status register	S_F_EDGE_STS_NMI	R	H'114	32	√	√	√	√
NMI async rising edge detect status register	A_R_EDGE_STS_NMI	R	H'118	32	√	√	√	√
NMI async falling edge detect status register	A_F_EDGE_STS_NMI	R	H'11C	32	√	√	√	√
NMI Chattering reduction status register	CHTEN_STS_NMI	R	H'120	32	√	√	√	√
NMI debounce setting register	DEB_SET_NMI	R/W	H'140	32	√	√	√	√
NMI configuration 0 register	CONFIG0_NMI	R/W	H'180	32	√	√	√	√
NMI configuration 1 register	CONFIG1_NMI	R/W	H'184	32	√	√	√	√
NMI configuration 2 register	CONFIG2_NMI	R/W	H'188	32	√	—	—	—
NMI configuration 3 register	CONFIG3_NMI	R/W	H'18C	32	√	—	—	—
NMI configuration 4 register	CONFIG4_NMI	R/W	H'190	32	√	—	—	—
NMI configuration 5 register	CONFIG5_NMI	R/W	H'194	32	√	—	—	—
NMI configuration 6 register	CONFIG6_NMI	R/W	H'198	32	√	—	—	—
NMI configuration 7 register	CONFIG7_NMI	R/W	H'19C	32	√	—	—	—

**Table 11.6 NMI Lock Register Configuration**

					<u>RZ/G Series Products</u>			
Register Name	Abbreviation	R/W	Address Offset	Access Size	RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
NMI mask lock set register	NMI_LCK	R/W*	H'000	32	√	√	√	√
NMI lock code register	NMI_LCKCODE	R/W*	H'004	32	√	√	√	√
NMI debug control enable register	NMI_DBG	R/W	H'008	32	√	√	√	√
NMI debug code register	NMI_DBGCODE	R/W	H'00C	32	√	√	√	√

Note: \* It cannot update register value during lock.



**11.4.4.1 Interrupt Request Status Register (INTREQ\_STSx [x = 0])**

Note: x = 0: for INTC-SYS.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

This register shows interrupt request status.

**[RZ/G1H]**

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	INTREQ				
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

**[RZ/G1M/N/E]**

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	INTREQ										
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to n+1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
n to 0	INTREQ[n:0]	All 0	R	Interrupt Status 0: Interrupt not generation 1: Interrupt generation

Note: n = 3 for RZ/G1H, n = 9 for RZ/G1M/N/E.

**11.4.4.2 Interrupt Enable Status register (INTEN\_STSx [x = 0])**

Note: x = 0: for INTC-SYS.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

This register shows interrupt enable status and clear interrupt enable.

**[RZ/G1H]**

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	INTEN				
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/WC1	R/WC1	R/WC1	R/WC1

**[RZ/G1M/N/E]**

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	—	—	—	—	—	—	INTEN									—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
R/W:	R	R	R	R	R	R	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	

Bit	Bit Name	Initial Value	R/W	Description
31 to n+1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
n to 0	INTEN[n:0]	All 0	R/WC1	Interrupt Enable Read 0: Interrupt generation is disabled Read 1: Interrupt generation is enabled Write 0: No functional effect Write 1: Interrupt enable clear

Note: n = 3 for RZ/G1H, n = 9 for RZ/G1M/N/E.

**11.4.4.3 Interrupt Enable Set register (INTEN\_SETx [x = 0])**

Note: x = 0: for INTC-SYS.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

This register set interrupt enable.

**[RZ/G1H]**

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	INTENS				
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	W	W	W	W

**[RZ/G1M/N/E]**

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	INTENS									
Initial value:	0	0	0	0	0	0	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	W	W	W	W	W	W	W	W	W	W

Bit	Bit Name	Initial Value	R/W	Description
31 to n+1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
n to 0	INTENS[n:0]	—	W	Interrupt Enable Set Write 0: No functional effect Write 1: Interrupt enable set

Note: n = 3 for RZ/G1H, n = 9 for RZ/G1M/N/E.

**11.4.4.4 IRQn Chattering Reduction Status Register (CHTEN\_STS)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

This register shows noise reduction enable status.

[RZ/G1H]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	CHTEN			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

[RZ/G1M/N/E]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	CHTEN									
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to n+1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
n to 0	CHTEN[n:0]	All 0	R	Noise Reduction Enable Status 0: Debouncing disabled 1: Debouncing enabled

Note: This bits need to reflect 3 rclk clock cycle.  
n = 3 for RZ/G1H, n = 9 for RZ/G1M/N/E.

**11.4.4.5 IRQn Detect Status Register (DETECT\_STATUS)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

This register shows IRQn event detection status and provides the function to clear edge-triggered event. The status bit is cleared by writing 1 to the corresponding bit in edge-triggered mode. Writing 0 to this register bits does not affect to the register value.

**[RZ/G1H]**

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	IRQnDET			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/WC1	R/WC1	R/WC1	R/WC1

**[RZ/G1M/N/E]**

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	IRQnDET									
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1

Bit	Bit Name	Initial Value	R/W	Description
31 to n+1	Reserved	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
n to 0	IRQnDET [n:0]	All 0	R/WC1	IRQn Event Detection Status Edge-triggered mode: Read 0: No interrupt request occurred Read 1: Interrupt request occurred Write 0: No functional effect Write 1: Cleared detection. Level-sensitive mode: Read 0: No interrupt request occurred. Read 1: Interrupt request occurred Write 0: No functional effect. Write 1: No functional effect.

Note: n = 3 for RZ/G1H, n = 9 for RZ/G1M/N/E.

**11.4.4.6 IRQn Signal Level Monitor Register (MONITOR)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

This register provide external signal monitor.

[RZ/G1H]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	IRQnMON			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

[RZ/G1M/N/E]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	—	—	—	—	—	—	IRQnMON										—
Initial value:	0	0	0	0	0	0	—	—	—	—	—	—	—	—	—	—	
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	

Bit	Bit Name	Initial Value	R/W	Description
31 to n+1	Reserved	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
n to 0	IRQnMON [n:0]	—	R	IRQn External Signal Level Monitor This function show input value of external PINS. 0: IRQn is low level 1: IRQn is high level

Note: n = 3 for RZ/G1H, n = 9 for RZ/G1M/N/E.

**11.4.4.7 IRQn High Level Detect Status Register (HLVL\_STS)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

This register provides interrupt detail detect status.

[RZ/G1H]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	IRQnHSTS			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

[RZ/G1M/N/E]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	—	—	—	—	—	—	IRQnHSTS									—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	

Bit	Bit Name	Initial Value	R/W	Description
31 to n+1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
n to 0	IRQnHSTS[n:0]	All 0	R	IRQn High Level Interrupt Status 0: IRQn high level interrupt request not occurred 1: IRQn high level interrupt request occurred

Note: n = 3 for RZ/G1H, n = 9 for RZ/G1M/N/E.

**11.4.4.8 IRQn Low Level Detect Status Register (LLVL\_STS)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

This register provides interrupt detail detect status.

[RZ/G1H]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	IRQnLSTS			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

[RZ/G1M/N/E]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	—	—	—	—	—	—	IRQnLSTS									—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	

Bit	Bit Name	Initial Value	R/W	Description
31 to n+1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
n to 0	IRQnLSTS[n:0]	All 0	R	IRQn Low Level Interrupt Status 0: IRQn low level interrupt request not occurred 1: IRQn low level interrupt request occurred

Note: n = 3 for RZ/G1H, n = 9 for RZ/G1M/N/E.



**11.4.4.9 IRQn Sync Rising Edge Detect Status Register (S\_R\_EDGE\_STS)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

This register provides interrupt detail detect status.

[RZ/G1H]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	IRQnSRSTS			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

[RZ/G1M/N/E]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	—	—	—	—	—	—	IRQnSRSTS									—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	

Bit	Bit Name	Initial Value	R/W	Description
31 to n+1	—	All 0	R	Reserved
n to 0	IRQnSRSTS [n:0]	All 0	R	IRQn Synchronous Rise Edge Interrupt Status 0: IRQn rise edge interrupt request not occurred 1: IRQn rise edge interrupt request occurred

Note: n = 3 for RZ/G1H, n = 9 for RZ/G1M/N/E.

**11.4.4.10 IRQn Sync Falling Edge Detect Status Register (S\_F\_EDGE\_STS)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

This register provides interrupt detail detect status.

[RZ/G1H]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	IRQnSFSTS			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

[RZ/G1M/N/E]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	—	—	—	—	—	—	IRQnSFSTS									—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	

Bit	Bit Name	Initial Value	R/W	Description
31 to n+1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
n to 0	IRQnSFSTS [n:0]	All 0	R	IRQn Synchronous Fall Edge Interrupt Status 0: IRQn fall edge interrupt request not occurred 1: IRQn fall edge interrupt request occurred

Note: n = 3 for RZ/G1H, n = 9 for RZ/G1M/N/E.

**11.4.4.11 IRQn Async Rising Edge Detect Status Register (A\_R\_EDGE\_STS)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

This register provides interrupt detail detect status.

[RZ/G1H]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	IRQnARSTS			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

[RZ/G1M/N/E]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	—	—	—	—	—	—	IRQnARSTS									—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	

Bit	Bit Name	Initial Value	R/W	Description
31 to n+1	—	All 0	R	Reserved
n to 0	IRQnARSTS [n:0]	All 0	R	IRQn Asynchronous Rise Edge Interrupt Status 0: IRQn rise edge interrupt request not occurred 1: IRQn rise edge interrupt request occurred

Note: n = 3 for RZ/G1H, n = 9 for RZ/G1M/N/E.

**11.4.4.12 IRQn Async Falling Edge Detect Status Register (A\_F\_EDGE\_STS)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

This register provides interrupt detail detect status.

[RZ/G1H]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	IRQnAFSTS			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

[RZ/G1M/N/E]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	IRQnAFSTS									
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to n+1	—	All 0	R	Reserved
n to 0	IRQnAFSTS [n:0]	All 0	R	IRQn Asynchronous Fall Edge Interrupt Status 0: IRQn fall edge interrupt request not occurred 1: IRQn fall edge interrupt request occurred

Note: n = 3 for RZ/G1H, n = 9 for RZ/G1M/N/E.

### 11.4.4.13 IRQn Configuration Register (CONFIG\_n)

Note: n = 0 to 3 [RZ/G1H], n = 0 to 9 [RZ/G1M/N/E]

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

This register provides detection mode and noise reduction setting.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CHTEN	—	—	—	—	—	—	—	STS1		STS2					
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	SS					
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	CHTEN	0	R/W	Chattering Reduction Enable 0: Chattering reduction disabled 1: Chattering reduction enabled
30 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23, 22	STS1	00	R/W	IRQn Scan Timing These bits provide chattering reduction timing. 00: 1 ms 01: 2 ms 10: 4 ms 11: 8 ms
21 to 16	STS2	H'00	R/W	IRQn Chattering Reduction Period The chattering reduction period is defined by STS1 × STS2. H'00: No reduction H'01 to H'3F: STS1 × STS2 Notes: 1. These bits should not be set to H'00 when chattering reduction enable. 2. Check chattering reduction is disabled completely with corresponding bit of chattering reduction status register (CHTEN_STS) when this bit change.
15 to 6	—	All 0	R	Reserved These bits are always read as 0. The writing value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
5 to 0	SS	000000	R/W	<p>Sense Selection</p> <p>000000: Disable event detection</p> <p>000001: Enable low level sensitive</p> <p>000010: Enable high level sensitive</p> <p>000100: Enable synchronous falling edge triggered</p> <p>001000: Enable synchronous rising edge triggered</p> <p>001100: Enable synchronous both edge triggered</p> <p>010000: Enable asynchronous falling edge triggered</p> <p>100000: Enable asynchronous rising edge triggered</p> <p>110000: Enable asynchronous both edge triggered</p> <p>Others : setting prohibit</p> <p>Note: The Asynchronous edge triggered can use only as follow conditions.</p> <p>+ EXTAL1 off</p> <p>+ Chattering reduction not use.</p> <p>The synchronous edge triggered can use always.</p>

**11.4.4.14 NMI Request Status Register (NMIREQ\_STSx [x = 0])**

Note: x = 0: for INTC-SYS.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

This register shows external NMI request status.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	CnSTS							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	Reserved	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7 to 0	CnSTS	All 0	R	NMI Status (n = 0 to 7)* 0: not during NMI service 1: during NMI service

Note: \* x = 0, n = 0 CPU0 interface (INTC-SYS)  
 n = 1 CPU1 interface (INTC-SYS)  
 n = 2 CPU2 interface (INTC-SYS)  
 n = 3 CPU3 interface (INTC-SYS)  
 n = 4 CPU4 interface (INTC-SYS)  
 n = 5 CPU5 interface (INTC-SYS)  
 n = 6 CPU6 interface (INTC-SYS)  
 n = 7 CPU7 interface (INTC-SYS)

For the CPU<sub>n</sub> interface, see section 11.3.1, INTC-SYS Register Configuration and Function Description.

**11.4.4.15 NMI Enable Status Register n (NMIEN\_STSx [x = 0])**

Note: x = 0: for INTC-SYS.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

This register shows NMI interrupt enable status and clears NMI interrupt enable.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	CnIEN							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	Reserved	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7 to 0	CnIEN	All 0	R/WC1	Interrupt Enable (n = 0 to 7)* Read 0: NMI interrupt generation is disabled Read 1: NMI interrupt generation is enabled Write 0: No functional effect Write 1: NMI interrupt enable clear

Note: \* x = 0, n = 0 CPU0 interface (INTC-SYS)  
 n = 1 CPU1 interface (INTC-SYS)  
 n = 2 CPU2 interface (INTC-SYS)  
 n = 3 CPU3 interface (INTC-SYS)  
 n = 4 CPU4 interface (INTC-SYS)  
 n = 5 CPU5 interface (INTC-SYS)  
 n = 6 CPU6 interface (INTC-SYS)  
 n = 7 CPU7 interface (INTC-SYS)  
 For the CPU<sub>n</sub> interface, see section 11.3.1, INTC-SYS Register Configuration and Function Description.



**11.4.4.16 NMI Enable Set Register n (NMIEN\_SETx [x = 0])**

Note: x = 0: for INTC-SYS.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

This register enables the NMI interrupt to each CPU.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	CnSET							
Initial value:	0	0	0	0	0	0	0	0	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	W	W	W	W	W	W	W	W

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	Reserved	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7 to 0	CnSET	—	W	Interrupt Enable Set (n = 0 to 7)* Write 0: No functional effect Write 1: Interrupt enable set

Note: \* x = 0, n = 0 CPU0 interface (INTC-SYS)  
 n = 1 CPU1 interface (INTC-SYS)  
 n = 2 CPU2 interface (INTC-SYS)  
 n = 3 CPU3 interface (INTC-SYS)  
 n = 4 CPU4 interface (INTC-SYS)  
 n = 5 CPU5 interface (INTC-SYS)  
 n = 6 CPU6 interface (INTC-SYS)  
 n = 7 CPU7 interface (INTC-SYS)  
 For the CPU<sub>n</sub> interface, see section 11.3.1, INTC-SYS Register Configuration and Function Description.

**11.4.4.17 NMI Chattering Reduction Status Register (CHTEN\_STS\_NMI)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

This register shows noise reduction enable status.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CHTEN
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	Reserved	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	CHTEN	0	R	Noise Reduction Enable Status 0: Debouncing disabled 1: Debouncing enabled

Note: This bits need to reflect 3 rclk clock cycle.

**11.4.4.18 NMI Detect Status Register (DETECT\_STATUS\_NMI)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

This register shows NMI event detection status and provides the function to clear edge-triggered event. The status bit is cleared by writing 1 to the corresponding bit in edge-triggered mode. Writing 0 to this register bits does not affect to the register value.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R		
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
	—	—	—	—	—	—	—	NMIDET									—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
R/W:	R	R	R	R	R	R	R	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1		

Bit	Bit Name	Initial Value	R/W	Description
31 to 9	Reserved	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8 to 0	NMIDET	All 0	R/WC1	NMI Event Detection Status (n = 0 to 8)* Edge-triggered mode: Read 0: No interrupt request occurred Read 1: Interrupt request occurred Write 0: No functional effect Write 1: Cleared detection Level-sensitive mode: Read 0: No interrupt request occurred Read 1: Interrupt request occurred Write 0: No functional effect Write 1: No functional effect

- Note: \*
- n = 0 CPU0 interface (INTC-SYS)
  - n = 1 CPU1 interface (INTC-SYS)
  - n = 2 CPU2 interface (INTC-SYS)
  - n = 3 CPU3 interface (INTC-SYS)
  - n = 4 CPU4 interface (INTC-SYS)
  - n = 5 CPU5 interface (INTC-SYS)
  - n = 6 CPU6 interface (INTC-SYS)
  - n = 7 CPU7 interface (INTC-SYS)
  - n = 8 Reserved

For the CPU<sub>n</sub> interface, see section 11.3.1, INTC-SYS Register Configuration and Function Description.

**11.4.4.19 NMI Signal Level Monitor Register (MONITOR\_NMI)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

This register provide external signal monitor.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	NMIM ON
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	Reserved	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	NMIMON	—	R	NMI External Signal Level Monitor This function show input value of external PINS 0: NMI is low level 1: NMI is high level

### 11.4.4.20 NMI Debounce Setting Register (DEB\_SET\_NMI)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

This register provides noise reduction setting.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CHTEN	—	—	—	—	—	—	—	STS1		STS2					
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31	CHTEN	0	R/W	Chattering Reduction Enable 0: Chattering reduction disabled 1: Chattering reduction enabled
30 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23, 22	STS1	00	R/W	NMI Scan Timing These bits provide chattering reduction timing. 00: 1 ms 01: 2 ms 10: 4 ms 11: 8 ms
21 to 16	STS2	H'00	R/W	NMI Chattering Reduction Period The chattering reduction period is defined by STS1 × STS2. H'00: No reduction H'01 to H'3F: STS1 × STS2 Note 1. These bits should not be set H'00 when chattering reduction enable. 2. Check chattering reduction is disabled completely with bit of chattering reduction status register (CHTEN_STS) when this bit change.
15 to 0	—	All 0	R	Reserved These bits are always read as 0. The writing value should always be 0.

**11.4.4.21 NMI High Level Detect Status Register (HLVL\_STS\_NMI)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

This register provides interrupt detail detect status.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	—	—	—	—	—	—	NMI <sub>n</sub> HSTS									—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	

Bit	Bit Name	Initial Value	R/W	Description
31 to 9	Reserved	All 0	R	Reserved These bits are always read as 0. The writing value should always be 0.
8 to 0	NMI <sub>n</sub> HSTS	All 0	R	NMI <sub>n</sub> High Level Interrupt Status (n = 0 to 8)* 0: NMI <sub>n</sub> high level interrupt request not occurred 1: NMI <sub>n</sub> high level interrupt request occurred

- Note: \*
- n = 0 CPU0 interface (INTC-SYS)
  - n = 1 CPU1 interface (INTC-SYS)
  - n = 2 CPU2 interface (INTC-SYS)
  - n = 3 CPU3 interface (INTC-SYS)
  - n = 4 CPU4 interface (INTC-SYS)
  - n = 5 CPU5 interface (INTC-SYS)
  - n = 6 CPU6 interface (INTC-SYS)
  - n = 7 CPU7 interface (INTC-SYS)
  - n = 8 Reserved

For the CPU<sub>n</sub> interface, see section 11.3.1, INTC-SYS Register Configuration and Function Description.

**11.4.4.22 NMI Low Level Detect Status Register (LLVL\_STS\_NMI)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

This register provides interrupt detail detect status.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R		
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
	—	—	—	—	—	—	—	NMI <sub>n</sub> LSTS									—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R		

Bit	Bit Name	Initial Value	R/W	Description
31 to 9	Reserved	All 0	R	Reserved These bits are always read as 0. The writing value should always be 0.
8 to 0	NMI <sub>n</sub> LSTS	All 0	R	NMI <sub>n</sub> Low Level Interrupt Status (n = 0 to 8)* 0: NMI <sub>n</sub> low level interrupt request not occurred 1: NMI <sub>n</sub> low level interrupt request occurred

- Note: \*
- n = 0 CPU0 interface (INTC-SYS)
  - n = 1 CPU1 interface (INTC-SYS)
  - n = 2 CPU2 interface (INTC-SYS)
  - n = 3 CPU3 interface (INTC-SYS)
  - n = 4 CPU4 interface (INTC-SYS)
  - n = 5 CPU5 interface (INTC-SYS)
  - n = 6 CPU6 interface (INTC-SYS)
  - n = 7 CPU7 interface (INTC-SYS)
  - n = 8 Reserved

For the CPU<sub>n</sub> interface, see section 11.3.1, INTC-SYS Register Configuration and Function Description.

**11.4.4.23 NMI Sync Rising Edge Detect Status Register (S\_R\_EDGE\_STS\_NMI)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

This register provides interrupt detail detect status.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R		
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
	—	—	—	—	—	—	—	NMIInSRSTS									—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R		

Bit	Bit Name	Initial Value	R/W	Description
31 to 9	Reserved	All 0	R	Reserved These bits are always read as 0. The writing value should always be 0.
8 to 0	NMIInSRSTS	All 0	R	NMIIn Synchronous Rise Edge Interrupt Status (n = 0 to 8)* 0: NMIIn rise edge interrupt request not occurred 1: NMIIn rise edge interrupt request occurred

- Note: \*
- n = 0 CPU0 interface (INTC-SYS)
  - n = 1 CPU1 interface (INTC-SYS)
  - n = 2 CPU2 interface (INTC-SYS)
  - n = 3 CPU3 interface (INTC-SYS)
  - n = 4 CPU4 interface (INTC-SYS)
  - n = 5 CPU5 interface (INTC-SYS)
  - n = 6 CPU6 interface (INTC-SYS)
  - n = 7 CPU7 interface (INTC-SYS)
  - n = 8 Reserved

For the CPU<sub>n</sub> interface, see section 11.3.1, INTC-SYS Register Configuration and Function Description.



**11.4.4.24 NMI Sync Falling Edge Detect Status Register (S\_F\_EDGE\_STS\_NMI)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

This register provides interrupt detail detect status.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	—	—	—	—	—	—	NMInSFSTS									—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	

Bit	Bit Name	Initial Value	R/W	Description
31 to 9	Reserved	All 0	R	Reserved These bits are always read as 0. The writing value should always be 0.
8 to 0	NMInSFSTS	All 0	R	NMIn Synchronous Fall Edge Interrupt Status (n = 0 to 8)* 0: NMIn fall edge interrupt request not occurred 1: NMIn fall edge interrupt request occurred

- Note: \*
- n = 0 CPU0 interface (INTC-SYS)
  - n = 1 CPU1 interface (INTC-SYS)
  - n = 2 CPU2 interface (INTC-SYS)
  - n = 3 CPU3 interface (INTC-SYS)
  - n = 4 CPU4 interface (INTC-SYS)
  - n = 5 CPU5 interface (INTC-SYS)
  - n = 6 CPU6 interface (INTC-SYS)
  - n = 7 CPU7 interface (INTC-SYS)
  - n = 8 Reserved

For the CPU<sub>n</sub> interface, see section 11.3.1, INTC-SYS Register Configuration and Function Description.

**11.4.4.25 NMI Async Rising Edge Detect Status Register (A\_R\_EDGE\_STS\_NMI)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

This register provides interrupt detail detect status.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	—	—	—	—	—	—	NMI <sub>n</sub> ARSTS									—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	

Bit	Bit Name	Initial Value	R/W	Description
31 to 9	Reserved	All 0	R	Reserved These bits are always read as 0. The writing value should always be 0.
8 to 0	NMI <sub>n</sub> ARSTS	All 0	R	NMI <sub>n</sub> Asynchronous Rise Edge Interrupt Status (n = 0 to 8)* 0: NMI <sub>n</sub> rise edge interrupt request not occurred 1: NMI <sub>n</sub> rise edge interrupt request occurred

- Note: \*
- n = 0 CPU0 interface (INTC-SYS)
  - n = 1 CPU1 interface (INTC-SYS)
  - n = 2 CPU2 interface (INTC-SYS)
  - n = 3 CPU3 interface (INTC-SYS)
  - n = 4 CPU4 interface (INTC-SYS)
  - n = 5 CPU5 interface (INTC-SYS)
  - n = 6 CPU6 interface (INTC-SYS)
  - n = 7 CPU7 interface (INTC-SYS)
  - n = 8 Reserved

For the CPU<sub>n</sub> interface, see section 11.3.1, INTC-SYS Register Configuration and Function Description.

**11.4.4.26 NMI Async Falling Edge Detect Status Register (A\_F\_EDGE\_STS\_NMI)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

This register provides interrupt detail detect status.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R		
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
	—	—	—	—	—	—	—	NMInAFSTS									—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R		

Bit	Bit Name	Initial Value	R/W	Description
31 to 9	Reserved	All 0	R	Reserved These bits are always read as 0. The writing value should always be 0.
8 to 0	NMInAFSTS	All 0	R	NMIn Asynchronous Fall Edge Interrupt Status (n = 0 to 8)* 0: NMIn fall edge interrupt request not occurred 1: NMIn fall edge interrupt request occurred

- Note: \*
- n = 0 CPU0 interface (INTC-SYS)
  - n = 1 CPU1 interface (INTC-SYS)
  - n = 2 CPU2 interface (INTC-SYS)
  - n = 3 CPU3 interface (INTC-SYS)
  - n = 4 CPU4 interface (INTC-SYS)
  - n = 5 CPU5 interface (INTC-SYS)
  - n = 6 CPU6 interface (INTC-SYS)
  - n = 7 CPU7 interface (INTC-SYS)
  - n = 8 Reserved

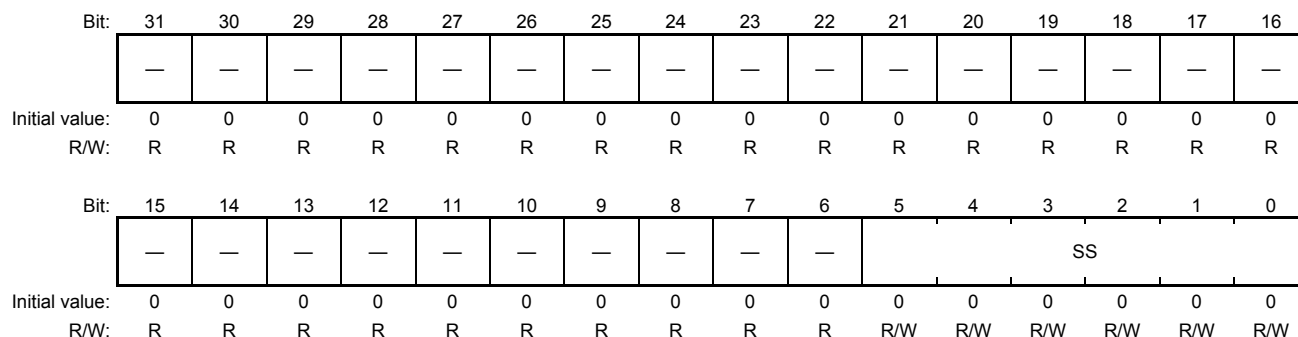
For the CPU<sub>n</sub> interface, see section 11.3.1, INTC-SYS Register Configuration and Function Description.

**11.4.4.27 NMI Configuration n Register (CONFIGn\_NMI)**

Note: n = 0 CPU0 interface (INTC-SYS)  
 n = 1 CPU1 interface (INTC-SYS)  
 n = 2 CPU2 interface (INTC-SYS)  
 n = 3 CPU3 interface (INTC-SYS)  
 n = 4 CPU4 interface (INTC-SYS)  
 n = 5 CPU5 interface (INTC-SYS)  
 n = 6 CPU6 interface (INTC-SYS)  
 n = 7 CPU7 interface (INTC-SYS)  
 For the CPU<sub>n</sub> interface, see section 11.3.1, INTC-SYS Register Configuration and Function Description.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

This register provides detection mode and noise reduction setting.

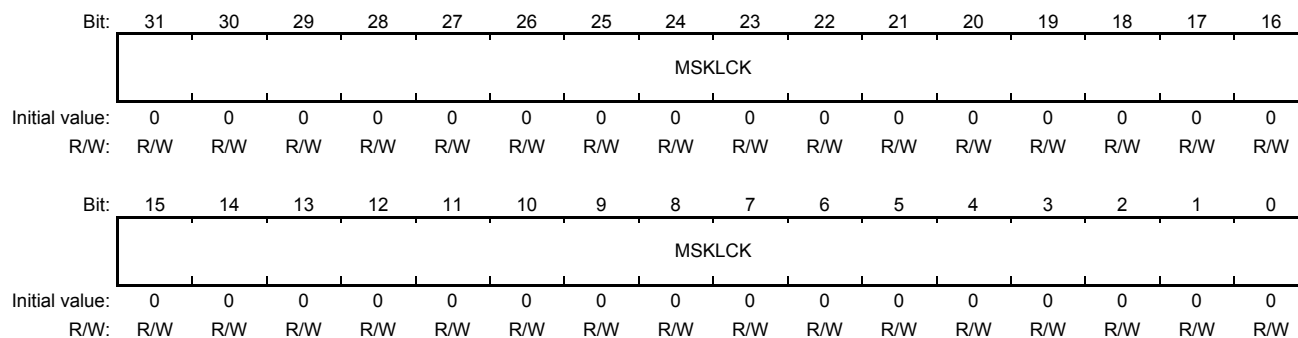


Bit	Bit Name	Initial Value	R/W	Description
31 to 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5 to 0	SS	000000	R/W	Sense Selection 000000: Disable event detection 000001: Enable low level sensitive 000010: Enable high level sensitive 000100: Enable synchronous falling edge triggered 001000: Enable synchronous rising edge triggered 001100: Enable synchronous both edge triggered 010000: Enable asynchronous falling edge triggered 100000: Enable asynchronous rising edge triggered 110000: Enable asynchronous both edge triggered Others: setting prohibit Note: The Asynchronous edge triggered can be used only following conditions. - EXTAL1 off - Chattering reduction not be used. - Only low level sensitive can be used for ARM.

**11.4.4.28 NMI Mask Lock Set Register (NMI\_LCK)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

This register provides NMI mask locking feature. When set the same value as NMI\_LCKCODE, then NMI cannot be masked by software (always accept NMI interrupt).

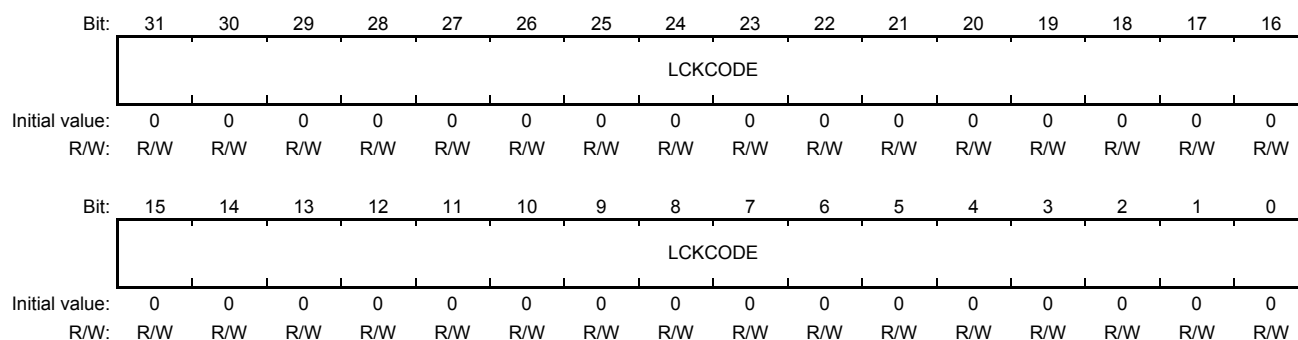


Bit	Bit Name	Initial Value	R/W	Description
31 to 0	MSKLCK	All 0	R/W	Lock code setting

**11.4.4.29 NMI Lock Code Register (NMI\_LCKCODE)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

This register sets the value for lock code of NMI mask.



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	LCKCODE	All 0	R/W	NMI mask lock code setting

**11.4.4.30 NMI Debug Control Enable Register (NMI\_DBG)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

This register enables the debug feature for NMI mask lock.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DBGEN
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved
0	DBGEN	0	R/W	Enable debug for NMI mask lock feature

**11.4.4.31 NMI Debug Code Register (NMI\_DBGCODE)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

This register sets value for debug code of NMI mask lock. When set the following value, then unlock this mask feature.

Debug code[31:0] = ~(lock code [0:31] (bit reversed))

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DBGCODE															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DBGCODE															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	DBGCODE	All 0	R/W	NMI mask lock debug code setting

### 11.4.5 NMI Mask Lock Feature

NMI can be masked by setting NMI mask register. If you set the lock code to NMI lock code register and set the same lock code to NMI lock set register, then NMI cannot be masked by software (locked NMI mask). If you want to unlock NMI mask, you need to set DBGEN bit of NMI debug control register and set the unlock code to the NMI debug code register.

### 11.4.6 Procedure of NMI Mask Lock

- Lock feature
  1. Write the lock code to NMI lock code register  
ex) Write32 (IRQC\_BASE + H'0A04), H'00ACCE55
  2. Write the lock code to NMI mask lock set register  
ex) Write32 (IRQC\_BASE + H'0A00), H'00ACCE55
  3. Write access to NMI lock code register and NMI mask lock set register  
— Check whether these registers cannot be updated
- Unlock feature
  1. Set enable bit to NMI debug control register  
ex) Write32 (IRQC\_BASE + H'0A08), H'00000001
  2. Write unlock code to NMI debug code register  
ex) Write32 (IRQC\_BASE + H'0A0C), H'558CCAFF
  3. Write access to NMI lock code register and NMI mask lock register  
— Check whether these registers can be updated

## 11.5 Usage Note

### 11.5.1 Under the particular condition, there is a possibility to be delayed to enter into the interrupt handler for AP-System Core.

[Description]

Figure 11.4 shows the internal logic of INTC-SYS. When INTC-SYS receive the interrupt from each peripheral IPs or internal registers are accessed by software, the clock controller in INTC-SYS module can start the clock supply to the internal logic.

After sixteen cycles of starting clock supply, the clock controller stops clock supply automatically.

If both the timing of being stopped clock supply (after sixteen cycle of clock supply) in INTC-SYS, and the timing of receiving the asynchronous interrupt are conflicted, clock supply sometimes stops unnecessarily. Then the corresponding interrupt are blocked unless another interrupts are received. As a result, the timing entering into the interrupt handler for AP-System core is delayed.

[Alternative]

In order to avoid this condition, it is necessary to resume clock supply periodically by accessing the internal registers of INTC-SYS.

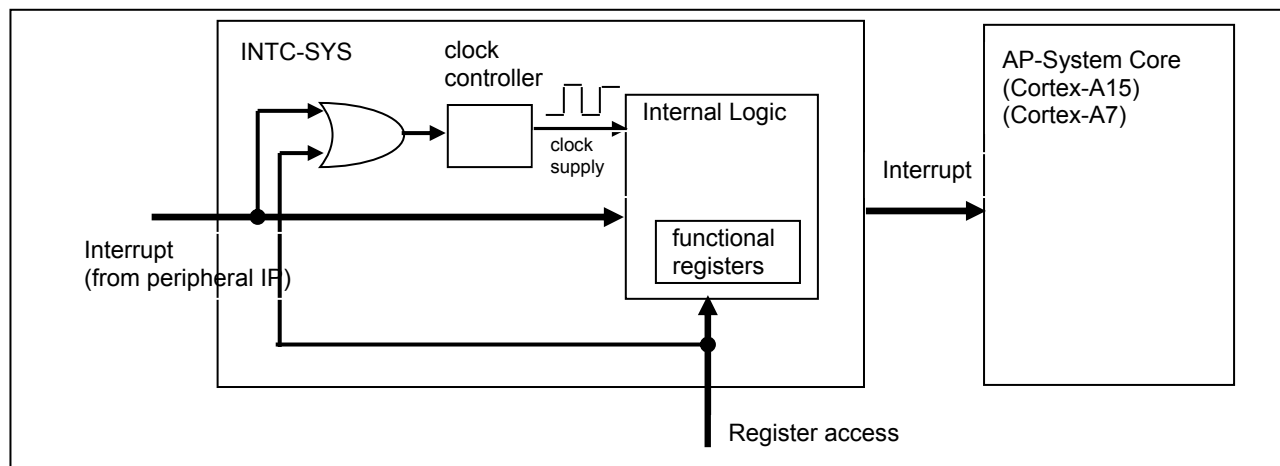


Figure 11.4 internal logic of INTC-SYS



## 12. AXI-bus

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

### 12.1 Overview

The AXI-bus is an on-chip interconnect bus based on the AMBA® Advanced eXtensible Interface (AXI) protocol specification. The AXI-bus has the following domains arranged in a hierarchical structure.

- Media domain AXI (MXI)
- Audio domain AXI
- System domain AXI
- CPU domain AXI
- DMA domain AXI

#### 12.1.1 Features

The AXI-bus has the following features.

- Frequency: 260 MHz
- Bus width: 256 bits or 128 bits
- High bandwidth and low latency
- Split transaction
- Separate data channels for reading and writing
- Quality-of-Service (QoS)
- Low-power function
- Secure access function

QoS is an extension to the standard AXI4 functionality, and allows control over the latency and bandwidth for the main memory.

### 12.1.2 Block Diagram

Figure 12.1 is a block diagram of the AXI-bus.

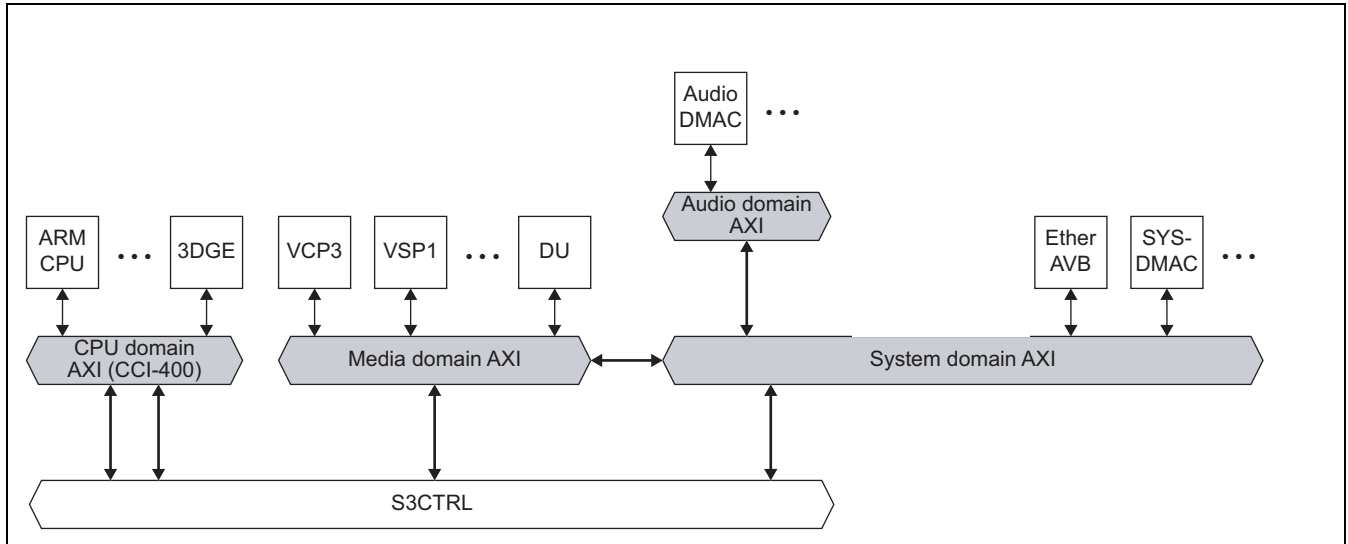


Figure 12.1 Block Diagram of AXI-bus

### 12.1.3 Input/Output Pins

No external pins are supported.

#### 12.1.4 Register Base Address of AXI-bus

Base address of registers is allocated to following address. The method of setting is provided separately.

- H'FF80\_0300 to H'FF80\_21FF (system domain)
- H'FF82\_0100 to H'FF82\_21FF (audio domain)
- H'FF84\_0100 to H'FF84\_21FF (DMA domain)
- H'FF85\_0100 to H'FF84\_21FF (DMA domain)
- H'FF86\_0100 to H'FF86\_21FF (system domain)
- H'FF87\_2000 to H'FF87\_21FF (media domain)
- H'FF88\_0100 to H'FF88\_21FF (CPU domain)
- H'FE96\_4100 to H'FE96\_7FFF (media domain)

### 12.1.5 Register Configuration

Table 12.1 shows a part of register configuration. Do not write to any addresses other than listed below. Operations cannot be guaranteed if writing is attempted. Values read from addresses other than those listed below are undefined. Access the register in longword (32-bit) units. Operation cannot be guaranteed if access to a register is not in longword units.

**Table 12.1 Register Configuration**

Name	Abbreviation	R/W	Address	Initial Value	Access Size	RZ/G Series Products			
						RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
MXI SDRAM address allocation register 0	MXSAAR0	R/W	H'FE96 0000	H'004000C0	32	√	√	√	√
MXI SDRAM address allocation register 1	MXSAAR1	R/W	H'FE96 0004	H'01000800	32	√	√	√	√
MXI read transaction control register	MXRTCR	R/W	H'FE96 0040	H'00000000	32	√	√	√	√
MXI write transaction control register	MXWTCCR	R/W	H'FE96 0044	H'00000000	32	√	√	√	√

## 12.2 Register Description

### Legend for Register Description

Initial value: Register value after a reset. H'xxxx represents a hexadecimal number. Others are represented in binary numbers.

—: Undefined value

R/W: Readable/writable. The written value can be read.

R: Read-only. The write value should always be 0.

R/WC0: Readable/writable. Writing 0 initializes the bit. Writing 1 is ignored.

R/WC1: Readable/writable. Writing 1 initializes the bit. Writing 0 is ignored.

W: Write-only. Reading this bit is prohibited. When the bit is reserved, the write value should always be 0.

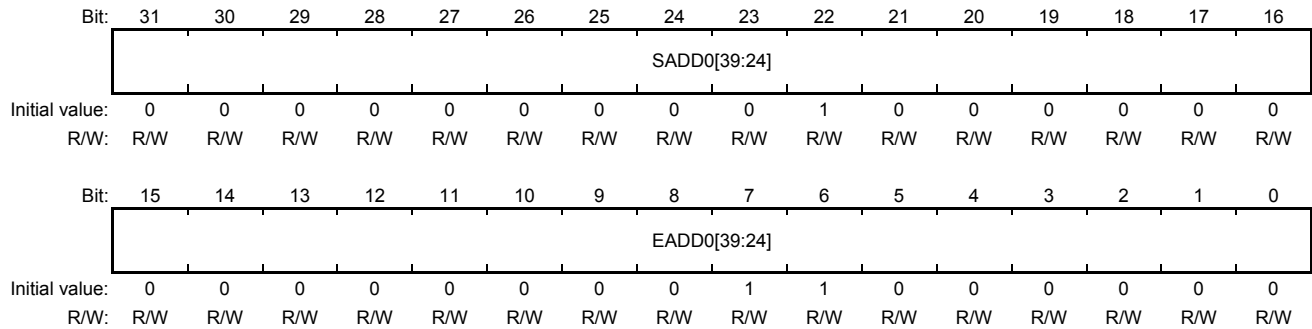
—/W: Write-only. The read value is undefined.

All access to registers must be in longword units.

### 12.2.1 MXI SDRAM Address Allocation Register 0 (MXSAAR0)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: The media domain AXI (MXI) can control the target port of transaction for DRAM access. The transaction of the address between SADD0 and EADD0 is issued to S3CTRL. Others are issued to the system domain AXI.

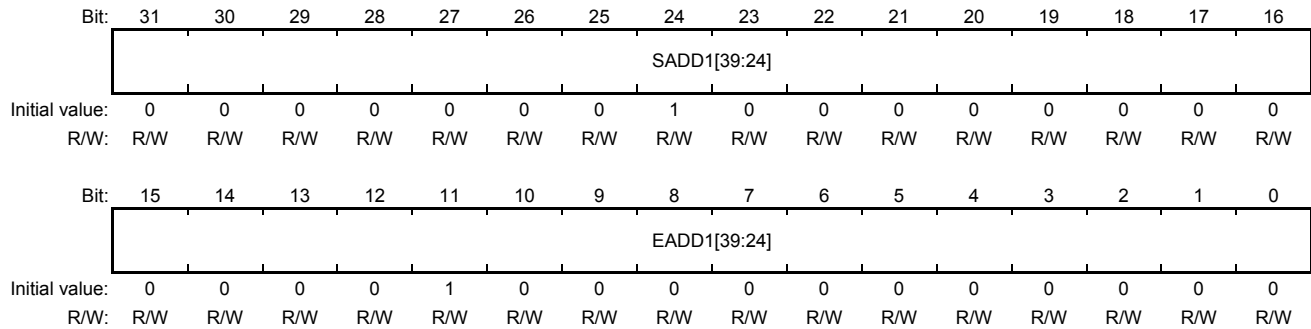


Bit	Bit Name	Initial Value	R/W	Description
31 to 16	SADD0[39:24]	H'0040	R/W	Start Address 0 [39:24].
15 to 0	EADD0[39:24]	H'00C0	R/W	End Address 0 [39:24].

### 12.2.2 MXI SDRAM Address Allocation Register 1 (MXSAAR1)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: The media domain AXI (MXI) can control the target port of transaction for DRAM access. The transaction of the address between SADD1 and EADD1 is issued to S3CTRL. Others are issued to the system domain AXI.



Bit	Bit Name	Initial Value	R/W	Description
31 to 16	SADD1[39:24]	H'0100	R/W	Start Address 1 [39:24].
15 to 0	EADD1[39:24]	H'0800	R/W	End Address 1 [39:24].

### 12.2.3 MXI Read Transaction Control Register (MXRTPCR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: This register controls the read transaction of the media domain AXI (MXI).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	RQPUSHEN	—	RTHRES		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5	—	0	R/W	Reserved This bit is always read as 0. The write value should always be 0.
4	RQPUSHEN	0	R/W	This bit should be set to 1.
3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
2 to 0	RTHRES	000	R/W	These bits specify the unit of transaction threshold at which QoS arbitration is performed. The appropriate configuration depends on the system. 000: No limit 001: 1 010: 2 011: 4 100: 8 101: 16 110: 32 111: Reserved



### 12.2.4 MXI Write Transaction Control Register (MXWTCCR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: This register controls the write transaction of the media domain AXI (MXI).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	WQPUSHEN	—	WTHRES		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5	—	0	R/W	Reserved This bit is always read as 0. The write value should always be 0.
4	WQPUSHEN	0	R/W	This bit should be set to 1.
3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
2 to 0	WTHRES	000	R/W	These bits specify the unit of transaction threshold at which QoS arbitration is performed. The appropriate configuration depends on the system. 000: No limit 001: 1 010: 2 011: 4 100: 8 101: 16 110: 32 111: Reserved

## 12.3 Operation

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

### 12.3.1 Media Domain AXI Access Control

The media domain AXI (MXI) can control the target port of transaction for DRAM access. One of the target ports of S3CTRL or system domain AXI can be chosen for DRAM access through MXSAAR0 and MXSAAR1 registers. The transaction of the address through MXSAAR0 or MXSAAR1 register is issued to S3CTRL port.

## 13. IPMMU

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

### 13.1 Overview

The IPMMU is a Memory Management Unit (MMU) which provides address translation and access protection functionalities to processing units and interconnect networks.

#### 13.1.1 Features

IPMMU includes the following main features.

- MMU architecture compatible with ARMv7 VMSA including the Large Physical Address Extension (LPAAE), the Security Extensions and the Multiprocessing Extensions
- PMB address translation
- Caching recently used page table entries in translation look-aside buffer (TLB)
- ACE-Lite support with Distributed Virtual Memory (DVM) messages through Cache Coherent Interconnect (CCI)
- Performance monitoring for ARMv7 LPAAE, VMSA and DVM operations

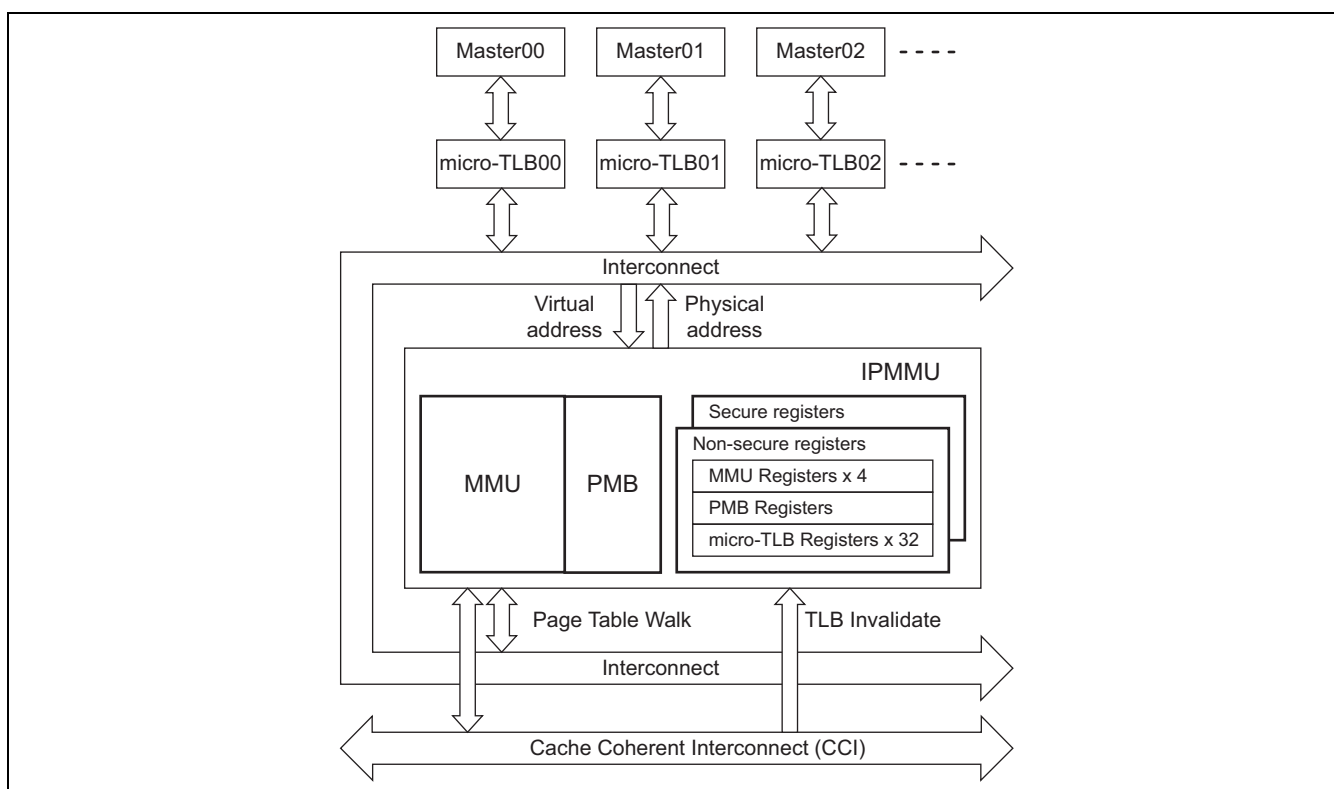
Note: All RZ/G series products other than the RZ/G1H support IPMMU for 3D graphics module (IPMMU-GP). IPMMU-GP supports the 40-bit translation system with the ARMv7 long-descriptor translation table format and the PMB address translation, and the IPMMU-GP doesn't support address translation of short-descriptor formats.

For more information about ARMv7 VMSA, see ARM Architecture Reference Manual ARMv7-A and ARMv7-R edition.

## 13.2 IPMMU System Integration

Figure 13.1 shows the IPMMU system integration. When a master (a processing unit or an interconnect) issues a transaction, a micro-TLB connected to the master sends a virtual address to the IPMMU. If the virtual address is not cached in a main TLB of the IPMMU, the IPMMU performs a page table walk through an interconnect or Cache Coherent Interconnect (CCI) and returns a physical address to the micro-TLB.

The IPMMU supports ACE-Lite protocol which makes it possible to share page table entries and keep coherency between System CPUs without software TLB maintenance.



**Figure 13.1 IPMMU System Integration**

Note: For IPMMU-GP, there is only path for a page table walk through the CCI.

### 13.3 Register Description

Table 13.1 shows the IPMMU registers.

These registers are 32-bit access registers. When modifying reserved bits or read-only bits, write 0 to the bits.

**Table 13.1 Register Configuration**

Register Name	Abbreviation	R/W	Address	RZ/G Series Products			
				RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
MMU Control Register N (N = 0 to 3: * For IPMMU-GP, only N = 0)	IMCTRn IMSCTRn	R/W	H'0000 + H'40 × n	√	√	√	√
MMU CCI Address Allocation Register N	IMCAARn IMSCAARn	R/W	H'0004 + H'40 × n	√	√	√	√
MMU Translation Table Base Control Register N	IMTTBCRn IMSTTBCRn	R/W	H'0008 + H'40 × n	√	√	√	√
MMU Bus Control Register N	IMBUSCRn IMSBUSCRn	R/W	H'000C + H'40 × n	√	√	√	√
MMU Translation Table Lower Base Register 0N	IMTTLBR0n IMSTTLBR0n	R/W	H'0010 + H'40 × n	√	√	√	√
MMU Translation Table Upper Base Register 0N	IMTTUBR0n IMSTTUBR0n	R/W	H'0014 + H'40 × n	√	√	√	√
MMU Translation Table Lower Base Register 1N	IMTTLBR1n IMSTTLBR1n	R/W	H'0018 + H'40 × n	√	√	√	√
MMU Translation Table Upper Base Register 1N	IMTTUBR1n IMSTTUBR1n	R/W	H'001C + H'40 × n	√	√	√	√
MMU Status Register N	IMSTRn IMSSTRn	R/W	H'0020 + H'40 × n	√	√	√	√
MMU Memory Attribute Indirection Register 0N	IMMAIR0n IMSMAIR0n	R/W	H'0028 + H'40 × n	√	√	√	√
MMU Memory Attribute Indirection Register 1N	IMMAIR1n IMSMAIR1n	R/W	H'002C + H'40 × n	√	√	√	√
MMU Error Address Register N	IMEARn IMSEARn	R	H'0030 + H'40 × n	√	√	√	√
PMB Control Register	IMPCTR IMPSCTR	R/W	H'0200	√	√	√	√
PMB Status Register	IMPSTR IMPSSTR	R/W	H'0208	√	√	√	√
PMB Error Address Register	IMPEAR IMPSEAR	R	H'020C	√	√	√	√
PMB Address Array N (N = 0 to 15)	IMPMBAn IMPMBSAAn	R/W	H'0280 to H'02BC	√	√	√	√

Register Name	Abbreviation	R/W	Address	RZ/G Series Products			
				RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
PMB Data Array N	IMPMBDn IMPMBSDn	R/W	H'02C0 to H'02FC	√	√	√	√
uTLB Control Register N (N = 0 to 31: * For IPMMU-GP, only N = 0)	IMUCTRn IMUSCTRn	R/W	H'0300 + H'10 × n	√	√	√	√
uTLB ASID Register N	IMUASIDn IMUSASIDn	R/W	H'0308 + H'10 × n	√	√	√	√
MMU Performance Monitor Control Register	IMPFCMTR	R/W	H'0580	—	—	—	√
DVM Performance Monitor Control Register	IMPFCMCTR	R/W	H'0584	—	—	—	√
MMU Performance Monitor Total Transaction Counter	IMPFCMMTOTAL	R	H'0590	—	—	—	√
MMU Performance Monitor Hit Counter	IMPFCMMHIT	R	H'0594	—	—	—	√
MMU Performance Monitor L3 Miss Counter	IMPFCMML3MISS	R	H'0598	—	—	—	√
MMU Performance Monitor L2 Miss Counter	IMPFCMML2MISS	R	H'059C	—	—	—	√
DVM Performance Monitor Total Transaction Counter	IMPFCMDTOTAL	R	H'05B0	—	—	—	√
DVM Performance Monitor User Counter	IMPFCMDUSER	R	H'05B4	—	—	—	√
DVM Performance Monitor Last TLB Invalidate 0	IMPFCMDLINV0	R	H'05B8	—	—	—	√
DVM Performance Monitor Last TLB Invalidate 1	IMPFCMDLINV1	R	H'05BC	—	—	—	√
Address alias of Non-secure registers *	—	R/W	H'0800 to H'0FFF	√	√	√	√

Note: \* Non-secure registers (H'0000 to H'07FF) can be accessed through this address space in Secure state. In Non-secure state, this address space is always read as 0.

Table 13.2 shows the each IPMMU base address. This table also shows which IPMMU is supported to each RZ/G product. Basically, each IPMMU is connected to the each BUS modules. But the number of IPMMU is different between each RZ/G product.

**Table 13.2 IPMMU Base Address**

MMU	Base Address	RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
IPMMU-SY0	H'E6280000	√	√	√	√
IPMMU-SY1	H'E6290000	√	√	√	√
IPMMU-DS	H'E6740000	√	√	√	√
IPMMU-MP	H'EC680000	√	√	√	√
IPMMU-MX	H'FE951000	√	√	√	√
IPMMU-GP	H'E62A0000	—	√	√	√

Note: √: Supported, —: Not Supported

Table 13.3 shows the register state in each processing mode.

Table 13.3 Register State in Each Processing Mode

Register Abbreviation	Reset*	Initial value	Module Standby	RZ/G Series Products			
				RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
IMCTRn IMSCTRn	Initialized	H'00000000	Retained	√	√	√	√
IMCAARn IMSCAARn	Initialized	H'00000000	Retained	√	√	√	√
IMTTBCRn IMSTTBCRn	Initialized	H'00000000	Retained	√	√	√	√
IMBUSCRn IMSTTLBR0n IMSTTLBR0n	Initialized	H'00000000	Retained	√	√	√	√
IMTTUBR0n IMSTTUBR0n	Initialized	H'00000000	Retained	√	√	√	√
IMTTLBR1n IMSTTLBR1n	Initialized	H'00000000	Retained	√	√	√	√
IMTTUBR1n IMSTTUBR1n	Initialized	H'00000000	Retained	√	√	√	√
IMSTRn IMSSTRn	Initialized	H'00000000	Retained	√	√	√	√
IMMAIR0n IMSMAIR0n	Initialized	H'00000000	Retained	√	√	√	√
IMMAIR1n IMSMAIR1n	Initialized	H'00000000	Retained	√	√	√	√
IMELARn IMSELARn	Initialized	H'00000000	Retained	√	√	√	√
IMEUARn IMSEUARn	Initialized	H'00000000	Retained	√	√	√	√
IMEWIDn IMSEWIDn	Initialized	H'00000000	Retained	√	√	√	√
IMERIDn IMSERIDn	Initialized	H'00000000	Retained	√	√	√	√
IMPCTR IMPSCTR	Initialized	H'00000000	Retained	√	√	√	√
IMPSTR IMPSSTR	Initialized	H'00000000	Retained	√	√	√	√
IMPEAR IMPSEAR	Initialized	H'00000000	Retained	√	√	√	√
IMPBA00 to 15 IMPBSA00 to 15	Initialized	H'00000000	Retained	√	√	√	√
IMPBD00 to 15 IMPBSD00 to 15	Initialized	H'00000000	Retained	√	√	√	√

Register Abbreviation	Reset*	Initial value	Module Standby	RZ/G Series Products			
				RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
IMUCTRn	Initialized	H'00000000	Retained	√	√	√	√
IMUSCTRn							
IMUASIDn	Initialized	H'00000000	Retained	√	√	√	√
IMUSASIDn							
IMPFMMCTR	Initialized	H'00000000	Retained	—	—	—	√
IMPFMDCTR	Initialized	H'00000000	Retained	—	—	—	√
IMPFMMTOTAL	Initialized	H'00000000	Retained	—	—	—	√
IMPFMHIT	Initialized	H'00000000	Retained	—	—	—	√
IMPFML3MISS	Initialized	H'00000000	Retained	—	—	—	√
IMPFML2MISS	Initialized	H'00000000	Retained	—	—	—	√
IMPFMDTOTAL	Initialized	H'00000000	Retained	—	—	—	√
IMPFMDUSER	Initialized	H'00000000	Retained	—	—	—	√
IMPFMDLINV0	Initialized	H'00000000	Retained	—	—	—	√
IMPFMDLINV1	Initialized	H'00000000	Retained	—	—	—	√

Note: \* Refer to section 8, Reset (RST).



### 13.3.1 MMU Control Register N (IMCTRn)

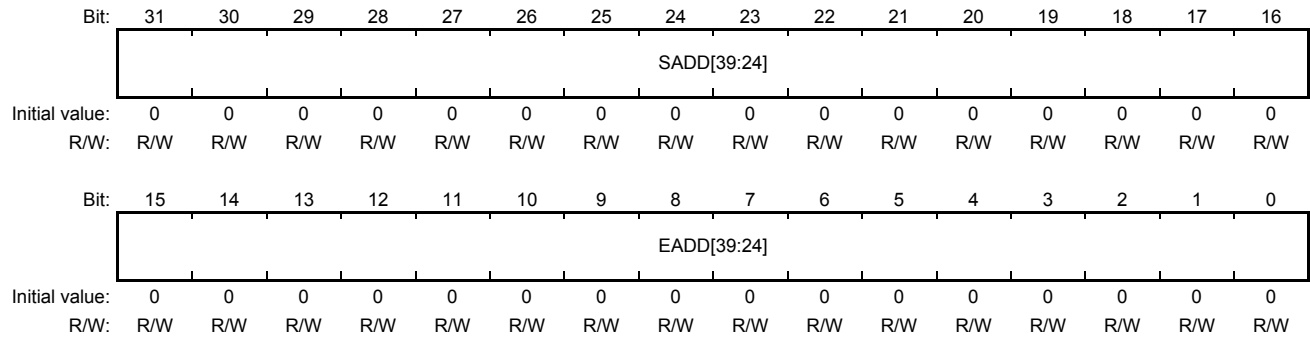
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TRE	AFE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	RTSEL[1:0]	TREN	INTEN	FLUSH	MMUE N	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 18	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
17	TRE	0	R/W	TEX Remap Enable This field is used when EAE is 0. 0: TEX remap disabled. 1: TEX remap enabled. Note: For IPMMUGP, set 0 to this bit
16	AFE	0	R/W	Access Flag Enable 0: Behave as if AF bit is always set to 1. 1: Enable software management of the Access Flag.
15 to 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5, 4	RTSEL[1:0]	00	R/W	Retranslation Table Select When TREN is 1, RTSEL indicates the table number to retranslate. Note: For IPMMUGP, set 0 to this bit
3	TREN	0	R/W	MMU Retranslation Enable 0: Output PA as a physical address. 1: Output PA as an intermediate physical address to retranslate through 40-bit TLB. Note: For IPMMUGP, set 0 to this bit
2	INTEN	0	R/W	Interrupt Enable 0: Don't assert an interrupt when an error occurs. 1: Assert an interrupt when an error occurs.
1	FLUSH	0	R/W	TLB Invalidate This bit is automatically cleared to 0. 1: Invalidate all TLB entries.
0	MMUEN	0	R/W	MMU Enable 0: MMU disabled 1: MMU enabled

### 13.3.2 MMU CCI Address Allocation Register N (IMCAARn)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√



Bit	Bit Name	Initial Value	R/W	Description
31 to 16	SADD[39:24]	H'0000	R/W	A start physical address via CCI interconnect
15 to 0	EADD[39:24]	H'0000	R/W	A end physical address via CCI interconnect

### 13.3.3 MMU Bus Control Register N (IMBUSCRn)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	DVM	BUSSEL[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31, 30	—	All 1	R	Reserved These bits are always read as 1. The write value should always be 1.
29, 28	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
27, 26	—	All 1	R	Reserved These bits are always read as 1. The write value should always be 1.
25 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2	DVM	0	R/W	Broadcast TLB maintenance operations through CCI 0: This table is not managed by DVM messages. 1: This table is managed by DVM messages.
1, 0	BUSSEL [1:0]	00	R/W	Bus Select 00: Always issue a page table walk request to a system interconnect. 01: Issue a page table walk request to CCI when its memory attribute is shareable. 10: Issue a page table walk request in the range of IMCAARn. 11: Issue a page table walk request to CCI in the range of IMCAARn and when its memory attribute is shareable.

### 13.3.4 MMU Translation Table Base Control Register N (IMTTBCRn)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

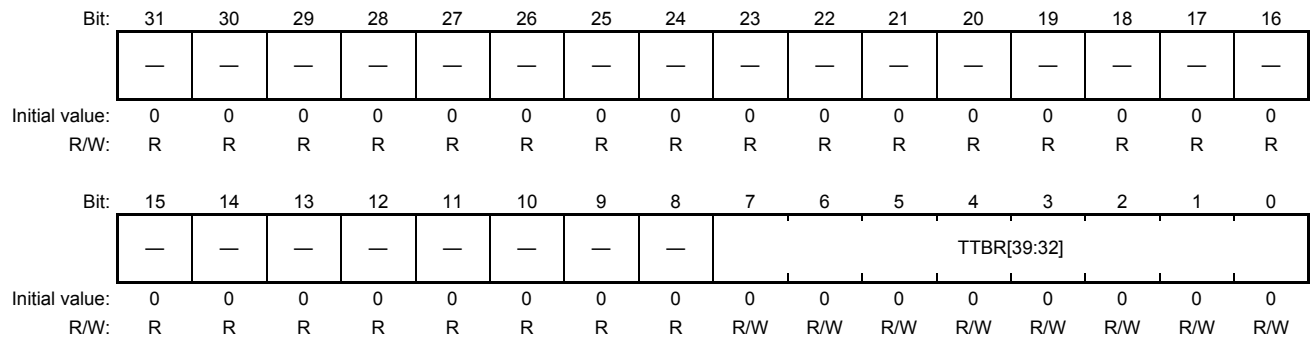
Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	EAE	PMB	SH1[1:0]		ORGN1[1:0]		IRGN1[1:0]		—	—	—	—	—	TSZ1[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	SH0[1:0]		ORGN0[1:0]		IRGN0[1:0]		—	—	—	SL0	—	TSZ0[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R/W	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	EAE	0	R/W	Extended Address Enable 0: Enable the 32-bit translation system with the ARMv7 Short-descriptor translation table format or PMB address translation. 1: Enable the 40-bit translation System with the ARMv7 Long-descriptor translation table format. Note: IPMMU-GP, set this bit to 1 (default).
30	PMB	0	R/W	PMB Enable 0: Disable PMB address translation. 1: Enable PMB address translation in the virtual address range from H'80000000 to H'BFFFFFFF. This field is used when EAE is 0.
29, 28	SH1[1:0]	00	R/W	Share ability attributes for the memory associated with the translation table walks using TTBR1n. 00: Non-shareable 01: Reserved 10: Outer shareable 11: Inner shareable
27, 26	ORGN1[1:0]	00	R/W	Outer Cache ability attributes for the memory associated with the translation table walks using TTBR1n. 00: Normal memory, Outer Non-cacheable 01: Normal memory, Outer Write-Back Write-Allocate Cacheable 10: Normal memory, Outer Write-Through Cacheable 11: Normal memory, Outer Write-Back no Write-Allocate Cacheable
25, 24	IRGN1[1:0]	00	R/W	Inner Cache ability attributes for the memory associated with the translation table walks using TTBR1n. 00: Normal memory, Inner Non-cacheable 01: Normal memory, Inner Write-Back Write-Allocate Cacheable 10: Normal memory, Inner Write-Through Cacheable 11: Normal memory, Inner Write-Back no Write-Allocate Cacheable
23 to 19	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
18 to 16	TSZ1[2:0]	000	R/W	The size offset of the TTBR1n addressed region, encoded as a 3-bit unsigned number, giving the size of the region as $2^{(32-TSZ1)}$ .

Bit	Bit Name	Initial Value	R/W	Description
15, 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13, 12	SH0[1:0]	00	R/W	Share ability attributes for the memory associated with the translation table walks using TTBR0n. 00: Non-shareable 01: Reserved 10: Outer shareable 11: Inner shareable
11, 10	ORGN0[1:0]	00	R/W	Outer Cache ability attributes for the memory associated with the translation table walks using TTBR0n. 00: Normal memory, Outer Non-cacheable 01: Normal memory, Outer Write-Back Write-Allocate Cacheable 10: Normal memory, Outer Write-Through Cacheable 11: Normal memory, Outer Write-Back no Write-Allocate Cacheable
9, 8	IRGN0[1:0]	00	R/W	Inner Cache ability attributes for the memory associated with the translation table walks using TTBR0n.. 00: Normal memory, Inner Non-cacheable 01: Normal memory, Inner Write-Back Write-Allocate Cacheable 10: Normal memory, Inner Write-Through Cacheable 11: Normal memory, Inner Write-Back no Write-Allocate Cacheable
7 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	SL0	0	R/W	Starting level for translation table walks. 0: Start at second level 1: Start at first level
3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
2 to 0	TSZ0[2:0]	000	R/W	The size offset of the TTBR0n addressed region, encoded as a 3-bit unsigned number, giving the size of the region as $2^{(32-TSZ0)}$ .

**13.3.5 MMU Translation Table Upper Base Register 0/1N (IMTTUBR0/1n)**

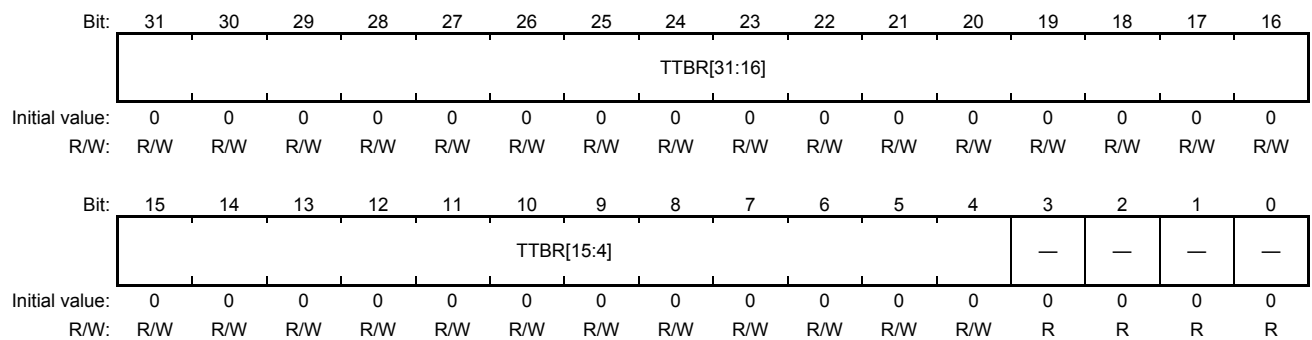
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√



Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7 to 0	TTBR[39:32]	H'00	R/W	Bits [39:32] of translation table base address This field is used when EAE is 1.

**13.3.6 MMU Translation Table Lower Base Register 0/1N (IMTTLBR0/1n)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√



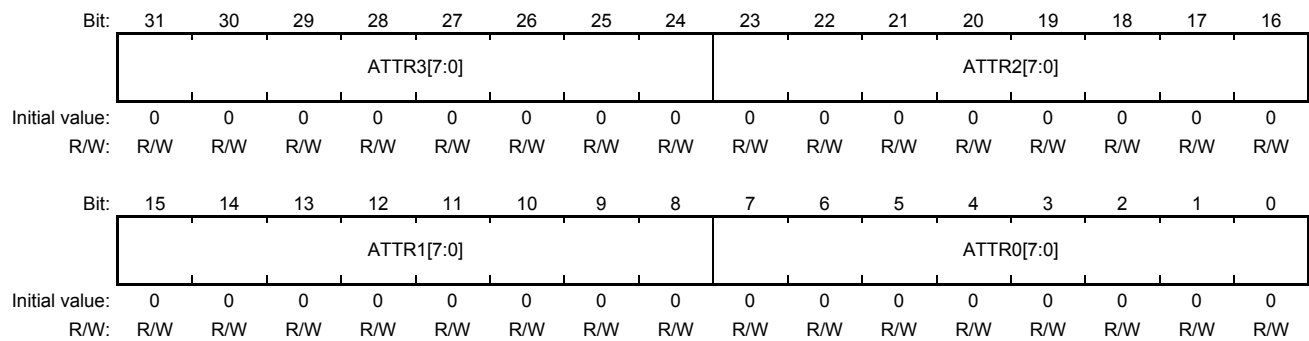
Bit	Bit Name	Initial Value	R/W	Description
31 to 4	TTBR[31:4]	All 0	R/W	Bits [31:4] of translation table base address
3 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

### 13.3.7 MMU Memory Attribute Indirection Register 0N (IMMAIR0n)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

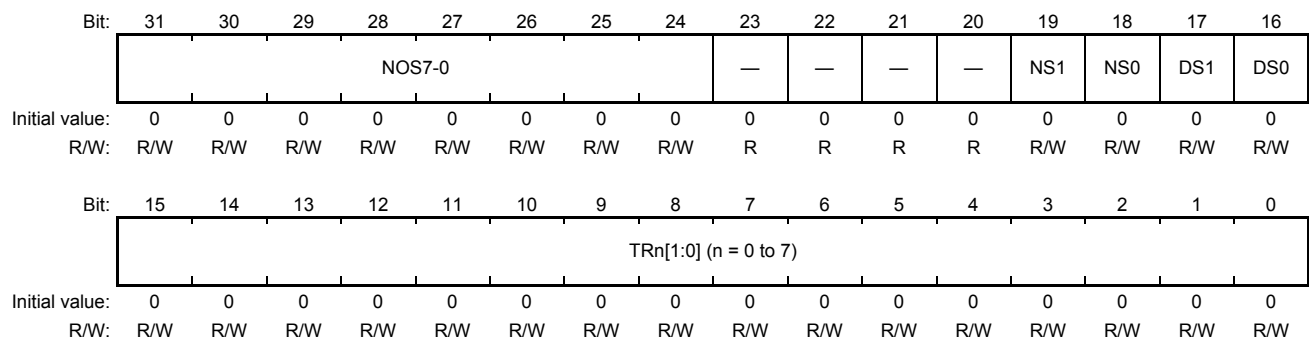
When using the Long-descriptor translation format, this register works as MAIR0, Memory Attribute Indirection Register in ARMv7 VMSA. When using the Short-descriptor translation format, this register works as PRRR, Primary Region Remap Register in ARMv7 VMSA.

(Long-descriptor translation format)



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	ATTR3[7:0]	H'00	R/W	The memory attribute encoding for an AttrIdx[2:0] entry.
23 to 16	ATTR2[7:0]	H'00	R/W	
15 to 8	ATTR1[7:0]	H'00	R/W	
7 to 0	ATTR0[7:0]	H'00	R/W	

(Short-descriptor translation format)



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	NOS7-0	All 0	R/W	Outer Shareable property mapping for memory attributes n. 0: Memory region is outer shareable. 1: Memory region is inner shareable.
23 to 20	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
19	NS1	0	R/W	Mapping of S = 1 attribute for Normal memory. 0: Region is not shareable. 1: Region is shareable.
18	NS0	0	R/W	Mapping of S = 0 attribute for Normal memory. 0: Region is not shareable. 1: Region is shareable.
17	DS1	0	R/W	Mapping of S = 1 attribute for Device memory. 0: Region is not shareable. 1: Region is shareable.
16	DS0	0	R/W	Mapping of S = 0 attribute for Device memory. 0: Region is not shareable. 1: Region is shareable.
15 to 0	TRn[1:0] (n = 0 to 7)	All 0	R/W	Primary TEX mapping for memory attributes n. n is the value of TEX[0], C and B bits. 00: Strongly-ordered 01: Device 10: Normal memory 11: Reserved

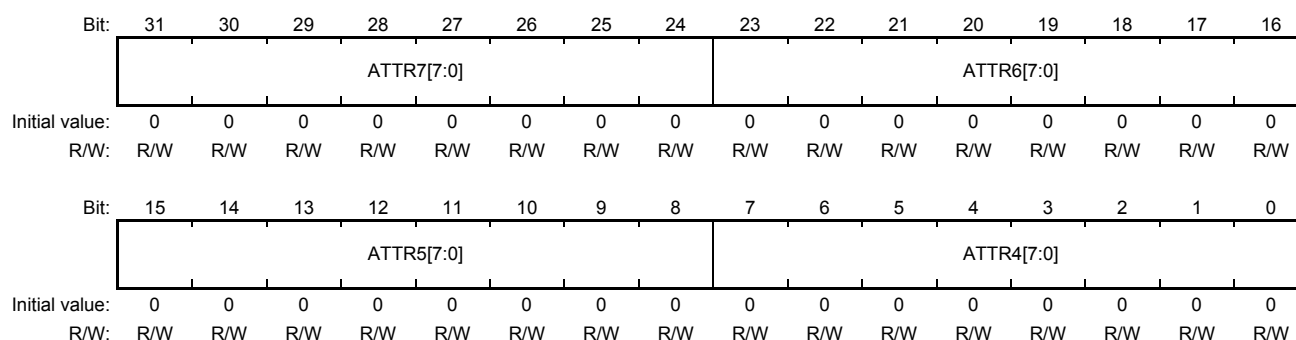


### 13.3.8 MMU Memory Attribute Indirection Register 1N (IMMAIR1n)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

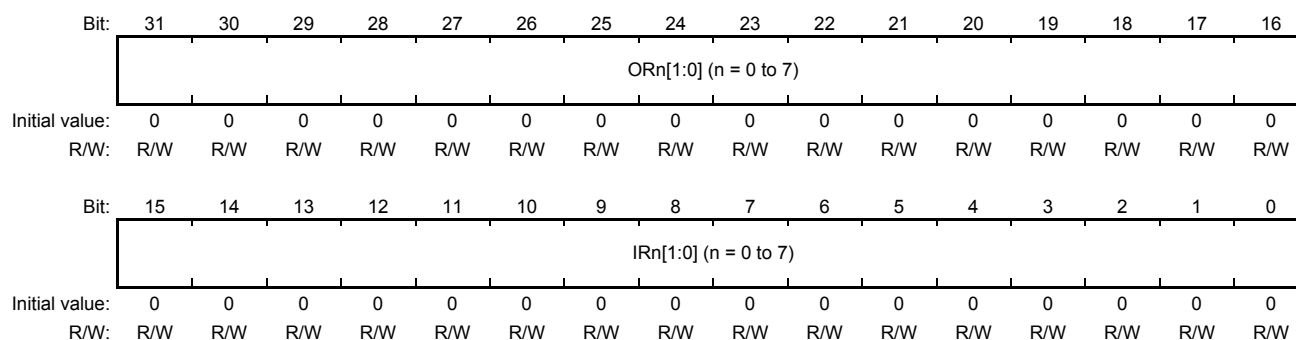
When using the Long-descriptor translation format, this register works as MAIR1, Memory Attribute Indirection Register in ARMv7 VMSA. When using the Short-descriptor translation format, this register works as NMRR, Normal Memory Remap Register in ARMv7 VMSA.

(Long-descriptor translation format)



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	ATTR7[7:0]	H'00	R/W	The memory attribute encoding for an AttrIdx[2:0] entry.
23 to 16	ATTR6[7:0]	H'00	R/W	
15 to 8	ATTR5[7:0]	H'00	R/W	
7 to 0	ATTR4[7:0]	H'00	R/W	

(Short-descriptor translation format)



Bit	Bit Name	Initial Value	R/W	Description
31 to 16	ORn[1:0] (n = 0 to 7)	All 0	R/W	Outer Cacheable property mapping for memory attributes n. 00: Region is non-cacheable. 01: Region is write-back, write-allocate. 10: Region is write-through, no write-allocate. 11: Region is write-back, no write-allocate.

---

<b>Bit</b>	<b>Bit Name</b>	<b>Initial Value</b>	<b>R/W</b>	<b>Description</b>
15 to 0	IRn[1:0] (n = 0 to 7)	All 0	R/W	Inner Cacheable property mapping for memory attributes n. 00: Region is non-cacheable. 01: Region is write-back, write-allocate. 10: Region is write-through, no write-allocate. 11: Region is write-back, no write-allocate.

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### 13.3.9 MMU Error Status Register N (IMSTRn)

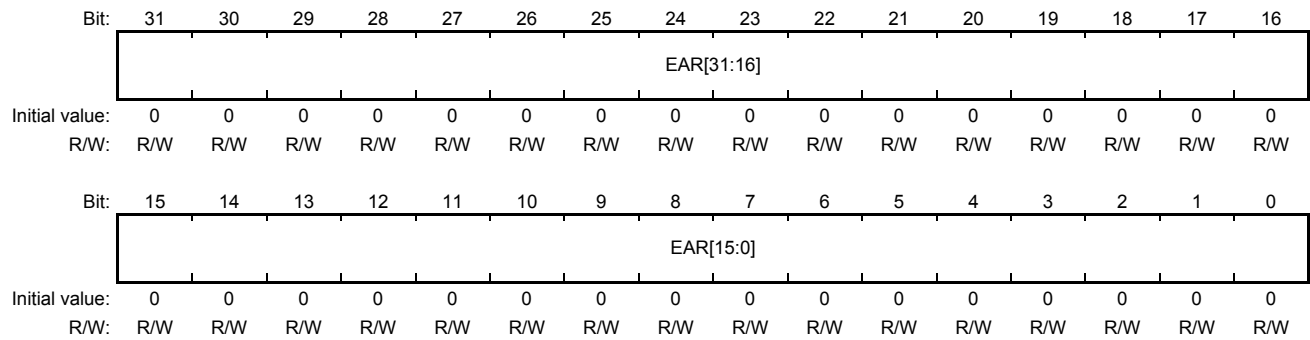
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	ERRLVL[1:0]	—	ERRCODE[2:0]			—	—	—	MHIT	—	ABORT	PF	TF	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13, 12	ERRLVL [1:0]	00	R	indicate which level of page table walk caused the error
11	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
10 to 8	ERRCODE [2:0]	000	R	Indicate error type 001: TLB format error (except “block” or “table” ) 100: access permission error 101: secure access error Others: reserved
7 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	MHIT	0	R/W	Indicate that multiple TLB hits occurred.
3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
2	ABORT	0	R/W	This bit is set to 1 when the IPMMU received an error response during a page table walk.
1	PF	0	R/W	Page Fault This bit is set to 1 when an access right violation occurred.
0	TF	0	R/W	Translation Fault This bit is set to 1 when a translation fault occurred during a page table walk.

**13.3.10 MMU Error Address Register N (IMEARn)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	EAR[31:0]	All 0	R/W	The faulting virtual address is set when an address translation error occurred.

### 13.3.11 PMB Control Register (IMPCTR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	TTSEL[1:0]	TTEN	INTEN	—	PMBEN	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5, 4	TTSEL[1:0]	00	R/W	Translation Table Select Note: For IPMMU-GP, set 00 to this bit.
3	TTEN	0	R/W	TLB Translation Enable 0: Output PPN as a physical address. 1: Output PPN as an intermediate physical address to retranslate through 40-bit TLB. PPN[39:32] is not used in retranslation. Note: For IPMMU-GP, set 0 to this bit.
2	INTEN	0	R/W	Interrupt Enable 0: Don't assert an interrupt when an error occurred. 1: Assert an interrupt when an error occurred.
1	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
0	PMBEN	0	R/W	PMB Enable 0: PMB disabled 1: PMB enabled

### 13.3.12 PMB Address Array N (IMPMBAn)

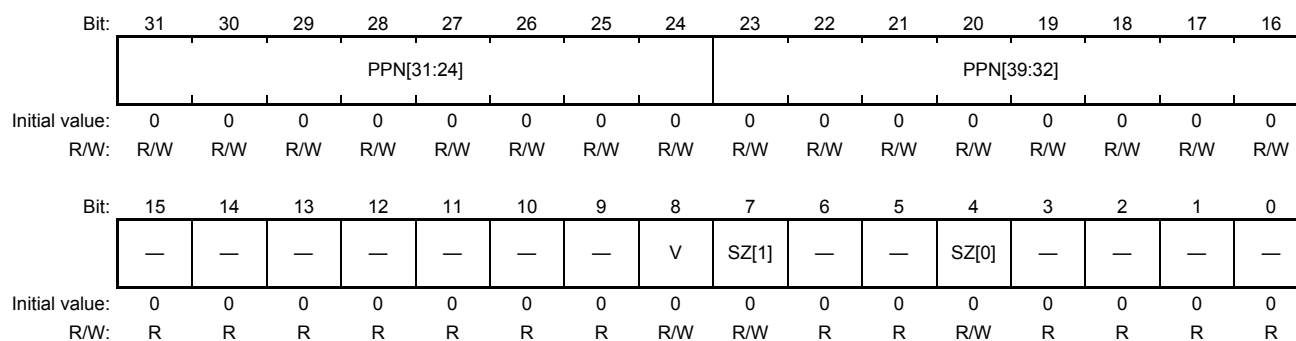
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	VPN[31:24]								—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	V	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	VPN[31:24]	All 0	R/W	Virtual Page Number For 16-Mbyte page, VPN[31:24] is used. For 64-Mbyte page, VPN[31:26] is used. For 128-Mbyte page, VPN[31:27] is used. For 512-Mbyte page, VPN[31:29] is used.
23 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	V	0	R/W	Enable this page translation.
7 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

## 13.3.13 PMB Data Array N (IMPMBDn)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	PPN[31:24]	All 0	R/W	Physical Page Number For 16-Mbyte page, PPN[31:24] is used. For 64-Mbyte page, PPN[31:26] is used. For 128-Mbyte page, PPN[31:27] is used. For 512-Mbyte page, PPN[31:29] is used.
23 to 16	PPN[39:32]	All 0	R/W	Upper Physical Page Number
15 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	V	0	R/W	Enable this page translation.
7	SZ[1]	0	R/W	This bit and SZ[0] (bit 4) specify the page size. SZ[1:0] = 00: 16-Mbyte page 01: 64-Mbyte page 10: 128-Mbyte page 11: 512-Mbyte page
6, 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	SZ[0]	0	R/W	Page Size See the description of SZ[1] (bit 7).
3 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

### 13.3.14 PMB Status Register (IMPSTR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

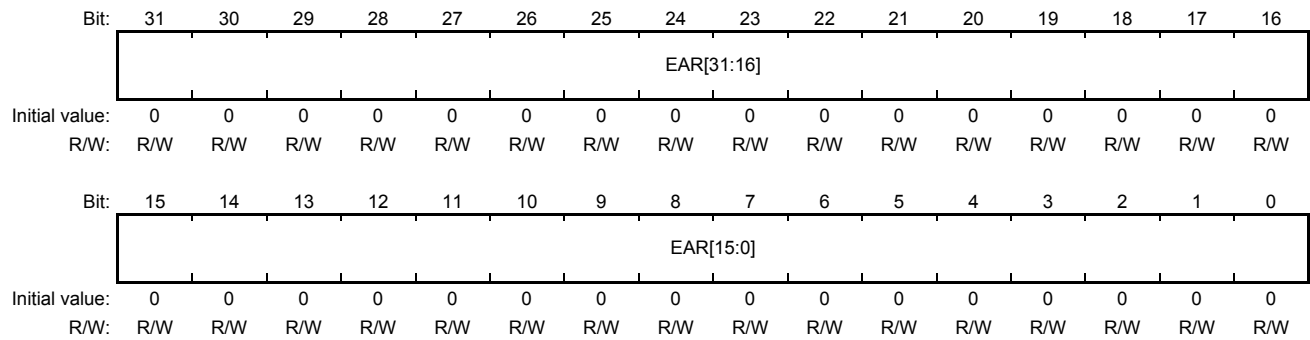
Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	MHIT	—	—	—	TF
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	MHIT	0	R/W	Multiple hit Indicate that multiple PMB hits occurred.
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	TF	0	R/W	Translation Fault This bit is set to 1 when a translation fault occurred during a PMB translation.



**13.3.15 PMB Error Address Register (IMPEAR)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	EAR[31:0]	All 0	R/W	The faulting virtual address is set when an address translation error occurred.

## 13.3.16 uTLB Control Register N (IMUCTRn)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	FIXAD DEN	—	—	—	—	—	—	—	FIXADD[39:32]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	TTSEL[3:0]				—	—	FLUSH	MMUE N
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	FIXADDEN	0	R/W	Fix the upper 8 bits of physical address Always output the upper 8 bits of physical address as FIXADD[39:32]. This bit must be used only in 32-bit translation mode. 0: Disable FIXADD[39:32] 1: Enable FIXADD[39:32]
30 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 16	FIXADD [39:32]	All 0	R/W	When FIXADDEN is 1, the upper 8bit of physical address is FIXADD[39:32]. This bit must be used only in 32-bit translation mode.
15 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7 to 4	TTSEL[3:0]	0000	R/W	Translation Table 0000 to 0011: MMUn 0100 to 0111: Reserved 1000: PMB 1001 to 1111: Reserved Note: For IPMMU-GP, set 0000 or 1000 to these bits.
3, 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	FLUSH	0	R/W	micro-TLB Invalidate Invalidate all entries in the micro-TLB. This bit is automatically cleared to 0. 1: Invalidate all entries.
0	MMUEN	0	R/W	Address Translation Enable 0: Disable address translation 1: Enable address translation

### 13.3.17 uTLB ASID Register N (IMUASIDn)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ASID1[7:0]								ASID0[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 8	ASID1[7:0]	H'00	R/W	ASID1 This field indicates the ASID which the micro-TLB uses in the 2nd translation stage.
7 to 0	ASID0[7:0]	H'00	R/W	ASID0 This field indicates the ASID which the micro-TLB uses in the 1st translation stage.

**13.3.18 MMU Performance Monitor Control Register (IMPFMMCTR)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	MD[1:0]	—	—	SEL[1:0]	—	—	—	—	—	—	—	RST	EN	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R	R	R/W	R/W	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13, 12	MD[1:0]	00	R/W	Monitor Mode 00: Monitor all 40-bit MMUs 01: Monitor all 32-bit MMUs 10: Reserved 11: Monitor only MMUn (specified by the SEL bits)
11, 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9, 8	SEL[1:0]	00	R/W	When MD is B'11, SEL indicates the MMU table number to be monitored.
7 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	RST	0	R/W	Reset all status and counter values. This bit is valid when EN = 1.
0	EN	0	R/W	Performance Monitor Enable 0: Stop to count 1: Start to count All counters stop and EN is set to 1 when TOTAL bits get full.

### 13.3.19 DVM Performance Monitor Control Register (IMPFMDCTR)

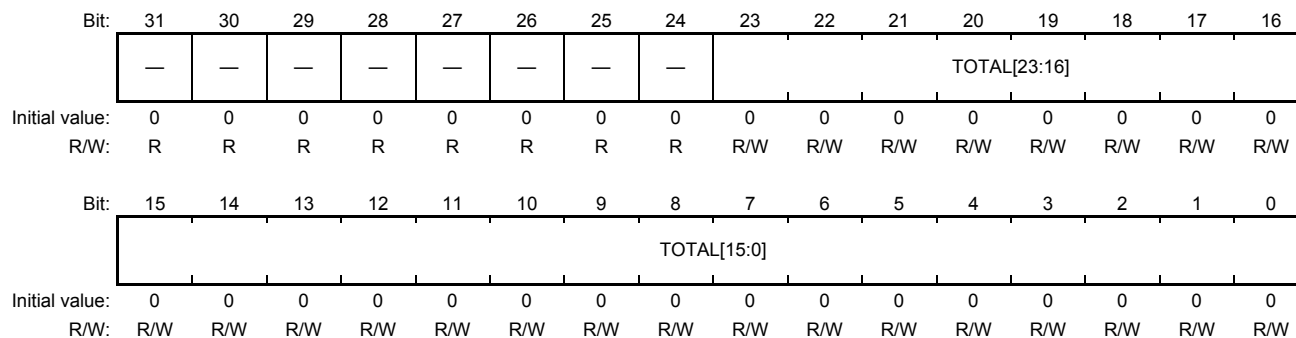
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
—	—	—	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DVMSEL1[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	DVMSEL0[1:0]		—	—	—	—	—	—	—	—	—	—	RST	EN
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 18	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
17, 16	DVMSEL1 [1:0]	00	R/W	Monitor Mode 1 00: ASID 01: VA 10: ERR 11: Reserved
15, 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13, 12	DVMSEL0 [1:0]	00	R/W	Monitor Mode 0 00: ASID 01: VA 10: ERR 11: Reserved
11 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	RST	0	R/W	Reset all status and counter values. This bit is valid when EN = 1.
0	EN	0	R/W	Performance Monitor Enable 0: Stop to count 1: Start to count All counters stop to count when TOTAL bits get full.

### 13.3.20 MMU Performance Monitor Total Translation Counter (IMPFMMTOTAL)

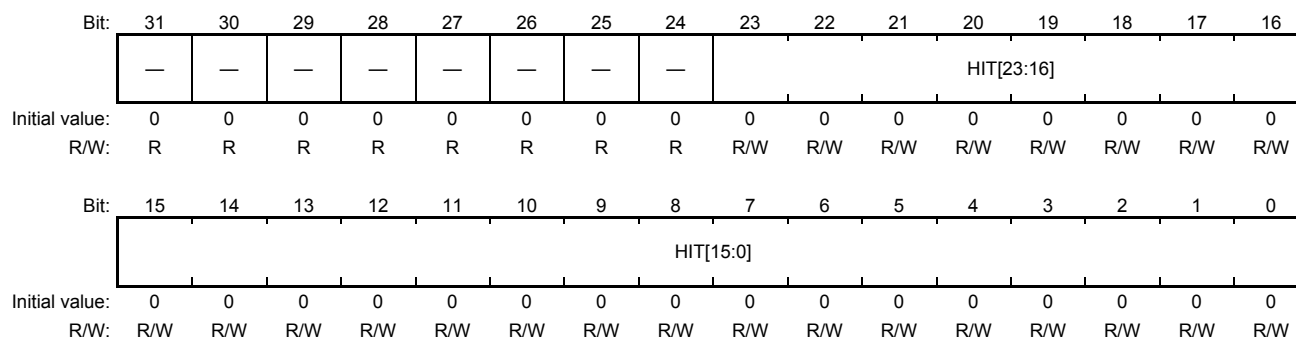
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
—	—	—	√



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	TOTAL[23:0]	H'00 0000	R/W	The total number of translation requests

### 13.3.21 MMU Performance Monitor Hit Counter (IMPFMHIT)

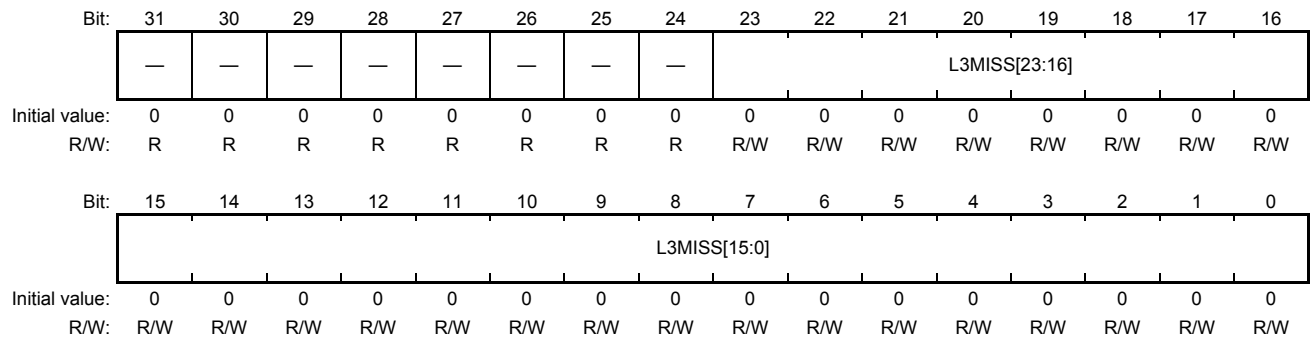
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
—	—	—	√



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	HIT[23:0]	H'00 0000	R/W	The total number of TLB hit requests = L3 TLB hit

**13.3.22 MMU Performance Monitor L3 Miss Counter (IMPFML3MISS)**

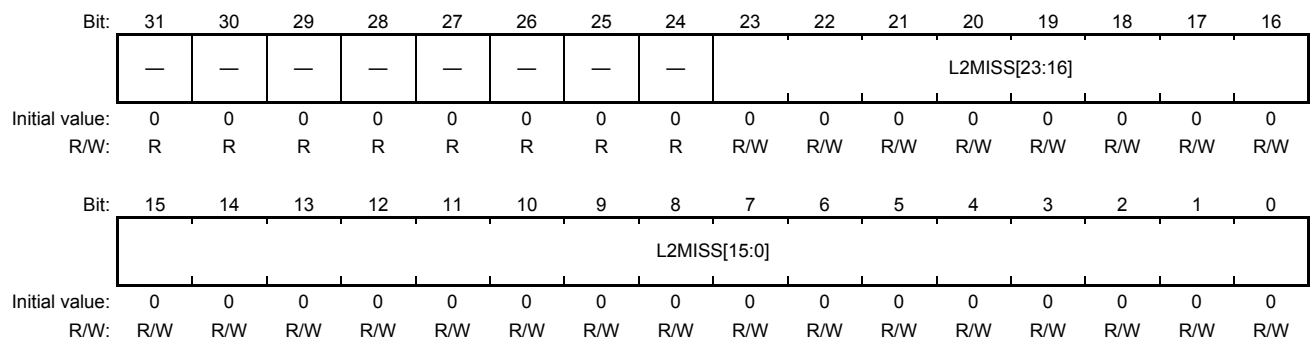
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
—	—	—	√



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	L3MISS [23:0]	H'00 0000	R/W	The total number of L3 miss requests (not including L2 miss and L1 miss) = L2 TLB hit

**13.3.23 MMU Performance Monitor L2 Miss Counter (IMPFML2MISS)**

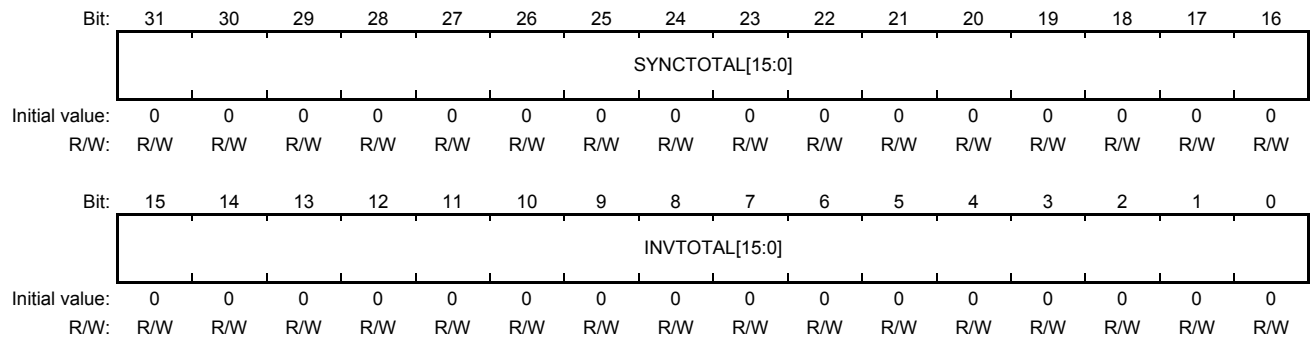
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	L2MISS [23:0]	H'00 0000	R/W	The total number of L2 miss requests (not including L1 miss) = Page Table Walk

### 13.3.24 DVM Monitor Total Transaction Counter (IMPFMDTOTAL)

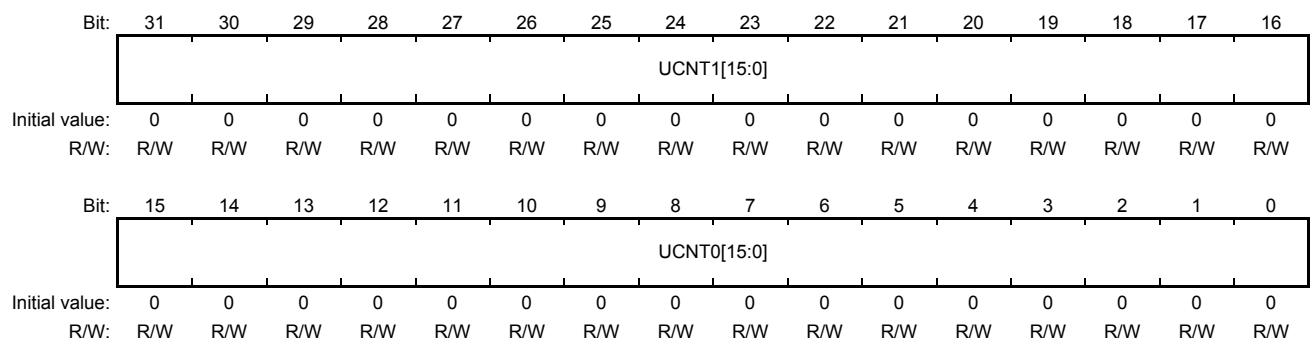
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
—	—	—	√



Bit	Bit Name	Initial Value	R/W	Description
31 to 16	SYNCTOTAL [15:0]	H'0000	R/W	The total number of DVM Sync transactions.
15 to 0	INVTOTAL [15:0]	H'0000	R/W	The total number of TLB Invalidate transactions.

### 13.3.25 DVM Monitor User Counter (IMPFMDUSER)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
—	—	—	√

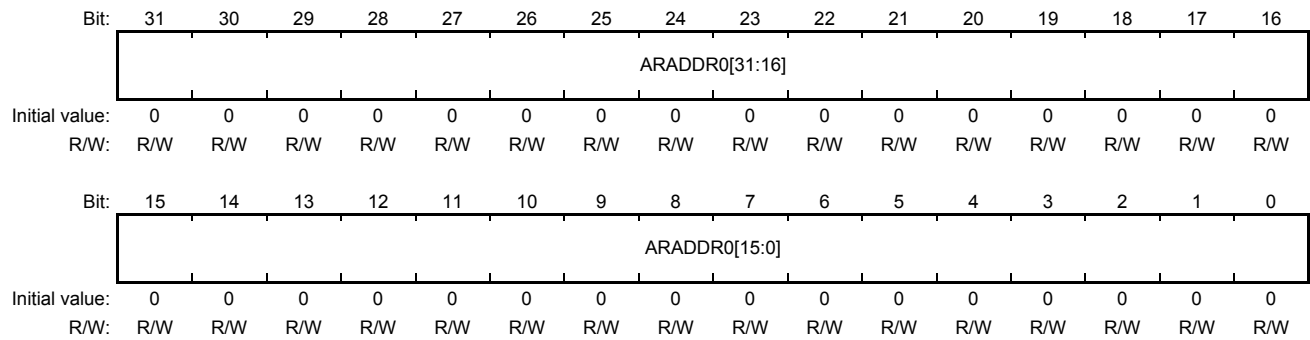


Bit	Bit Name	Initial Value	R/W	Description
31 to 16	UCNT1[15:0]	H'0000	R/W	The total number of TLB Invalidate transactions chosen by DVMSEL1.
15 to 0	UCNT0[15:0]	H'0000	R/W	The total number of TLB Invalidate transactions chosen by DVMSEL0.



**13.3.26 DVM Monitor Last TLB Invalidate 0 (IMPFMDLINV0)**

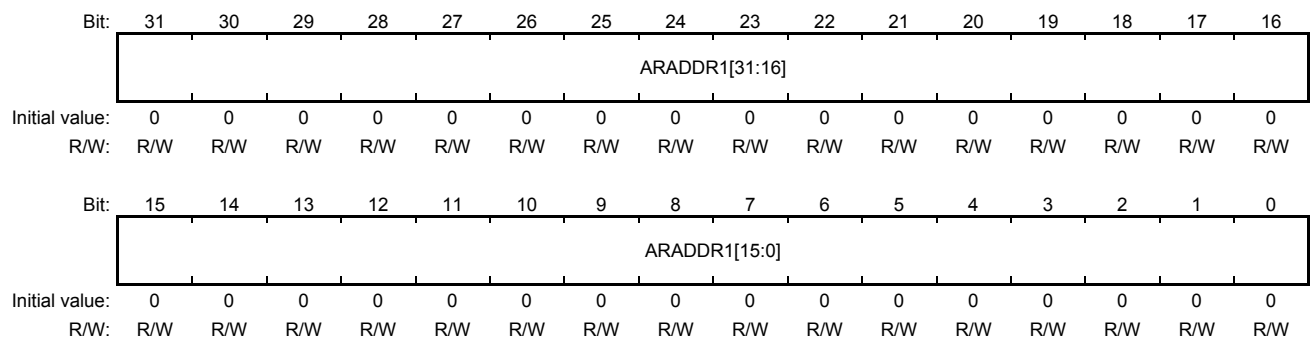
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
—	—	—	√



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	ARADDR0 [31:0]	H'0000 0000	R/W	Display the last TLB Invalidate ARADDR[31:0].

**13.3.27 DVM Monitor Last TLB Invalidate 1 (IMPFMDLINV1)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
—	—	—	√



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	ARADDR1 [31:0]	H'0000 0000	R/W	Display the 2nd ARADDR[31:0] of the last TLB Invalidate when the last TLB Invalidate operation is a multi-part DVM Message.

RZ/G1H	RZ/G1N
RZ/G1M	RZ/G1E

## 13.4 Operation

### 13.4.1 Address Translation Sequence in micro-TLBs

Each micro-TLB has independent entries and can translate from a virtual address to a physical address without sending translation requests to the IPMMU if the virtual address is cached in the micro-TLB.

When a translation error occurred in address translation, the micro-TLB blocks subsequent transactions until a valid page entry is registered. Set IMUCTRn.FLUSH = 1 after the entry registration.

Figure 13.2 shows the micro-TLB address translation sequence.

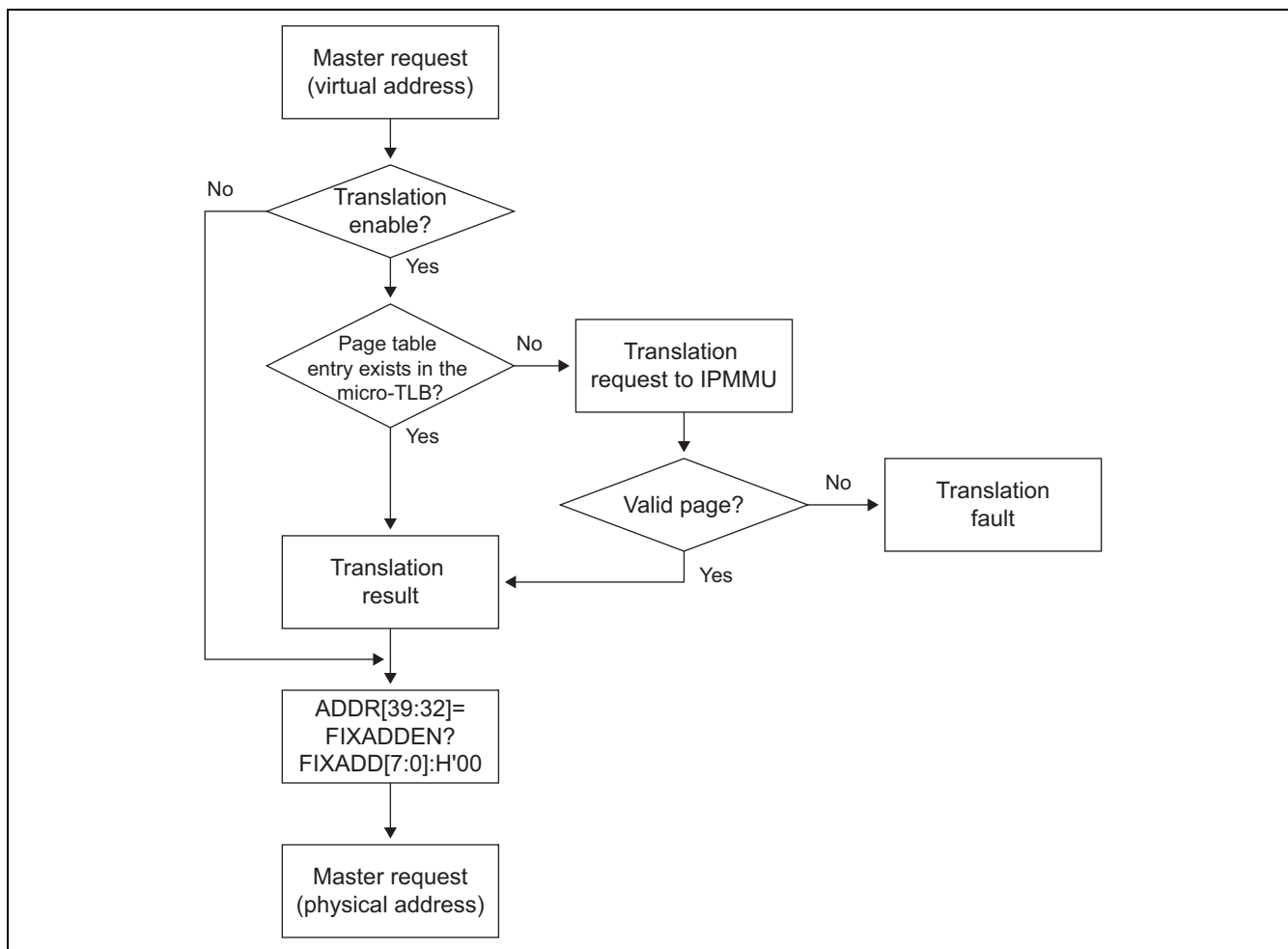


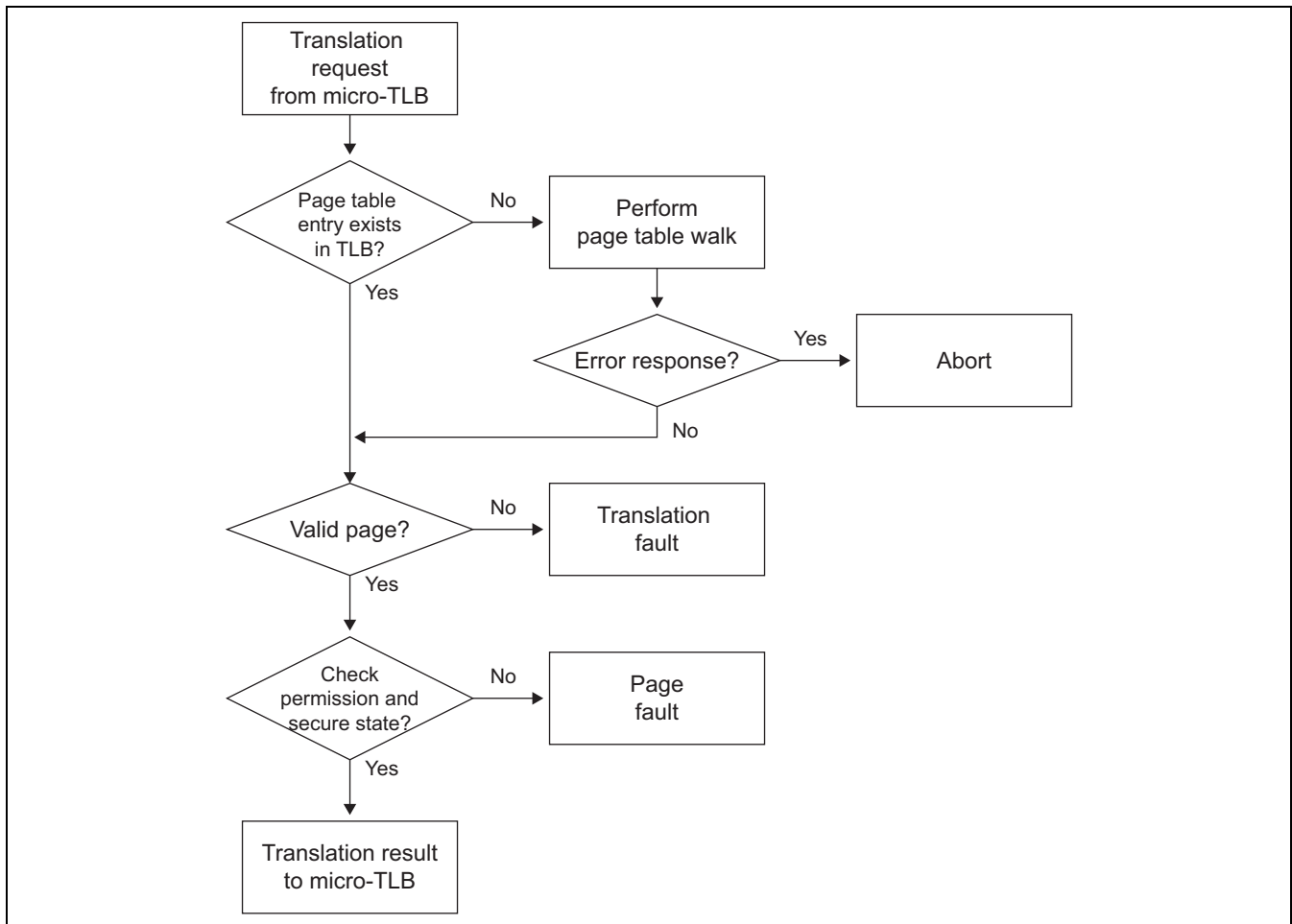
Figure 13.2 micro-TLB Address Translation Sequence

### 13.4.2 Address Translation Sequence in the IPMMU

#### (1) MMU Address Translation

The IPMMU has independent four non-secure page tables and four secure page tables which support two page table formats, the Short-descriptor format and the Long-descriptor format. When the IPMMU receives an address translation request from a micro-TLB, the IPMMU starts address translation sequence based on the page table specified by IMUCTRn.TTSEL.

Figure 13.3 shows the MMU address translation sequence.



**Figure 13.3 MMU Address Translation Sequence**

## (2) PMB Address Translation

PMB address translation is performed in two ways. When PMB address translation is chosen in IMUCTRn.TTSEL, all virtual addresses are translated by PMB. When PMB address translation is performed in a part of MMU translation (IMTTBCRn.PMB = 1), virtual addresses within H'80000000 to H'BFFFFFFF are translated to physical addresses by PMB.

Figure 13.4 shows the PMB translation flow.

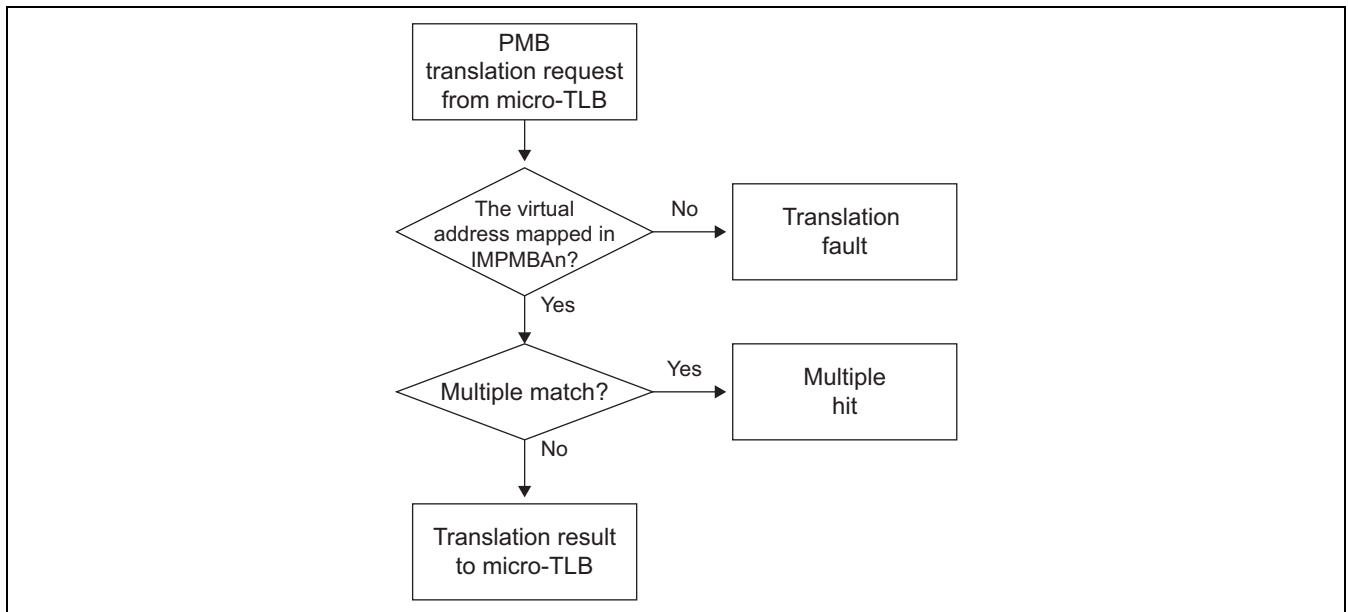


Figure 13.4 PMB Translation Flow

### 13.4.3 Address Space

#### (1) Short-descriptor

In the short-descriptor format, 32-bit virtual address space is translated to 32-bit physical address space managed by TTBR0/1. When IMTTBCRn.PMB = 1, translation address space is compatible with our previous products. In this mode, a virtual address within H'80000000 to H'BFFFFFFF is translated by PMB and a virtual address within H'C0000000 to H'FFFFFFF is mapped to a physical address of the same value.

Note: IPMMU-GP doesn't support the Short-descriptor translation format.

Figure 13.5 shows the Short-descriptor address space.

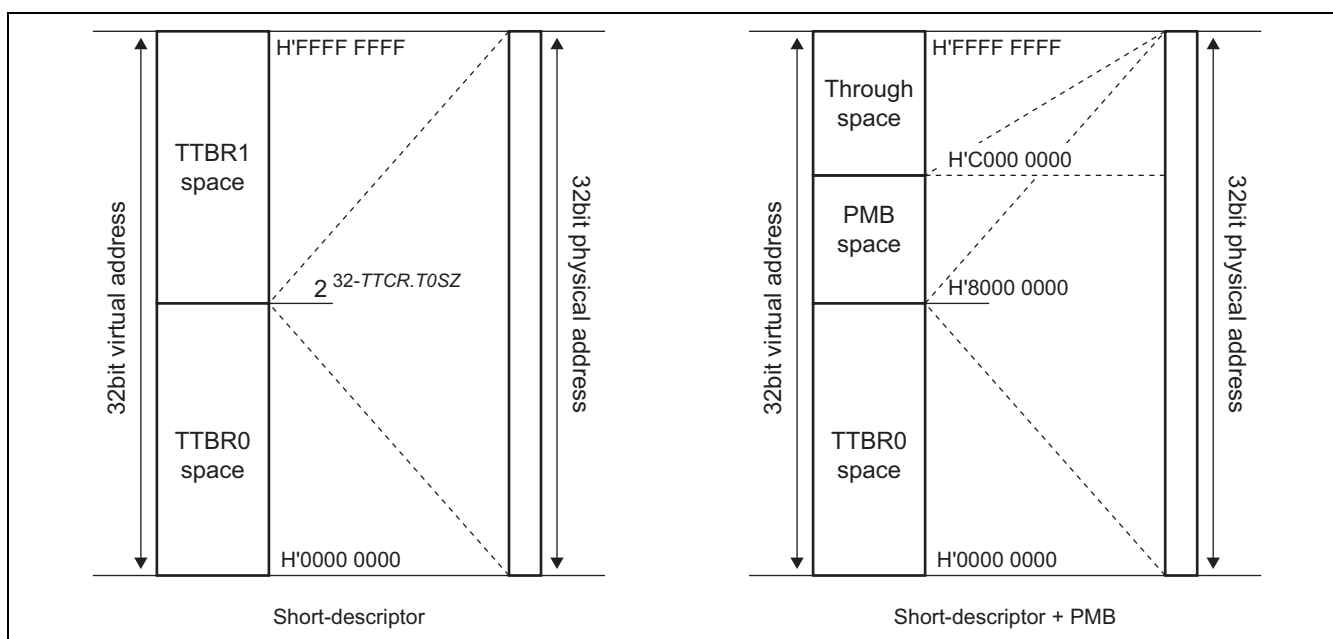


Figure 13.5 Short-descriptor Address Space

#### (2) Long-descriptor

In the long-descriptor format, 32-bit virtual address space is translated to 40-bit physical address space managed by TTBR0/1. The IPMMU supports the Secure PL1 and PL0 stage 1 translation and the Non-secure PL1 and PL0 stage 1 translation. The IPMMU doesn't support the Virtualization Extensions.

Figure 13.6 shows the Long-descriptor address space.

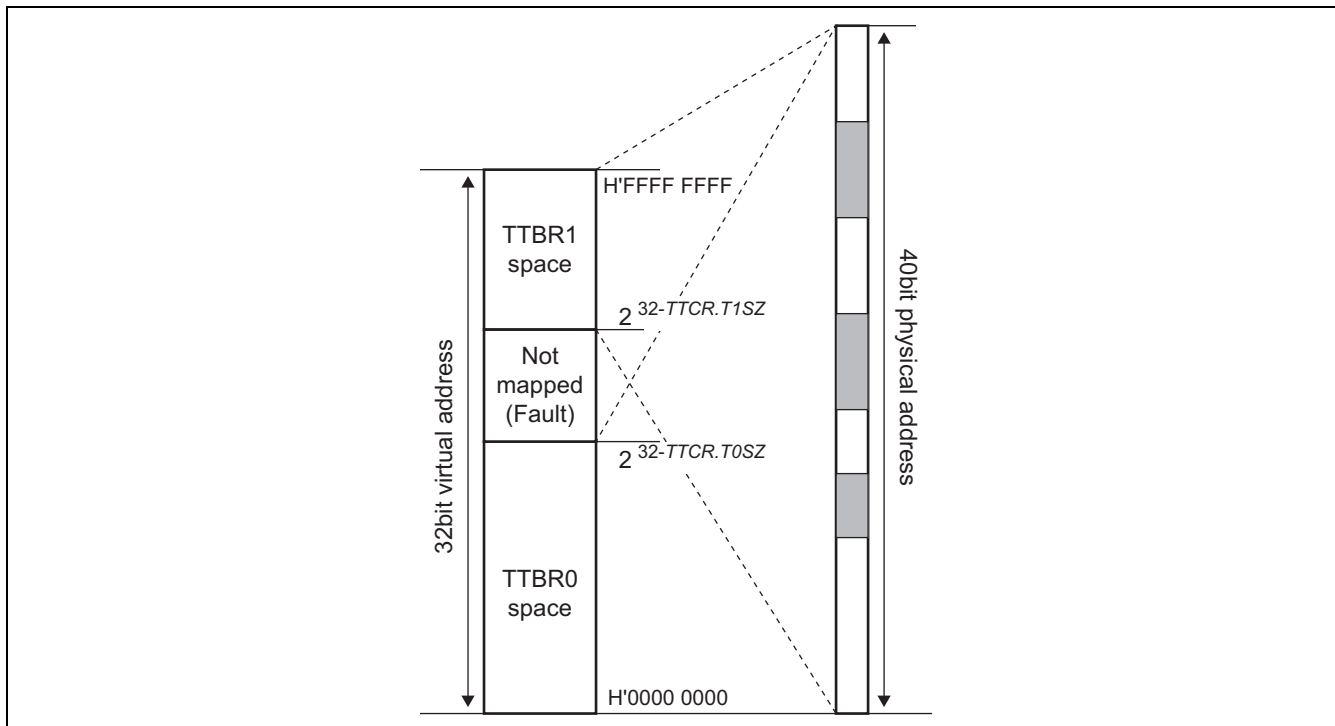


Figure 13.6 Long-descriptor Address Space

(3) PMB

The IPMMU supports the PMB address translation system. Figure 13.7 shows the PMB address space.

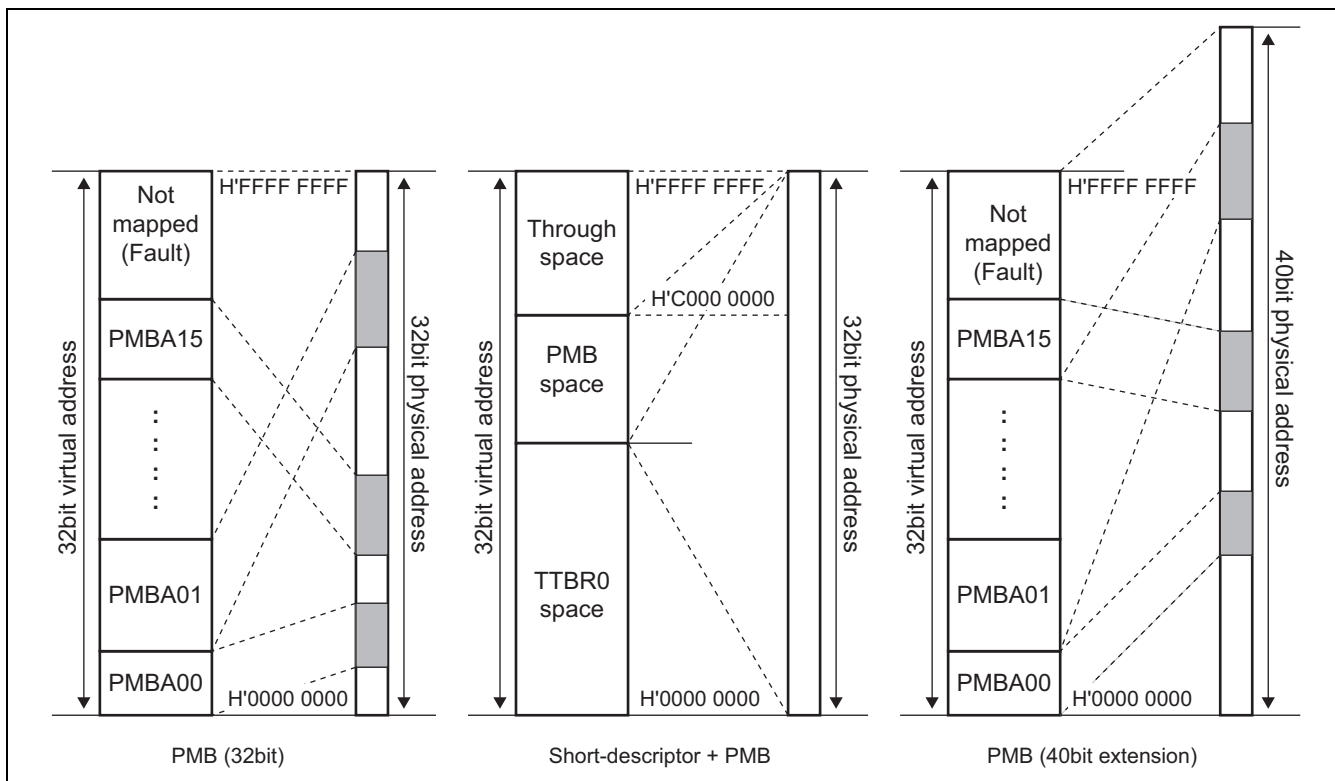


Figure 13.7 PMB Address Space

#### (4) 2-Stage Translation

The IPMMU supports 2-stage translation. At the 1st-stage, 32-bit address space is translated to 32-bit intermediate physical address (IPA) space. At the 2nd-stage, 32-bit IPA space is translated to 40-bit physical address space. In order to enable the 2-stage translation, set 1 to IMCTRn.TREN and set its 2nd-stage page table to IMCTRn.RTSEL.

Note: IPMMU-GP doesn't support the 2-stage translation.

Figure 13.8 shows the 2-stage translation address space.

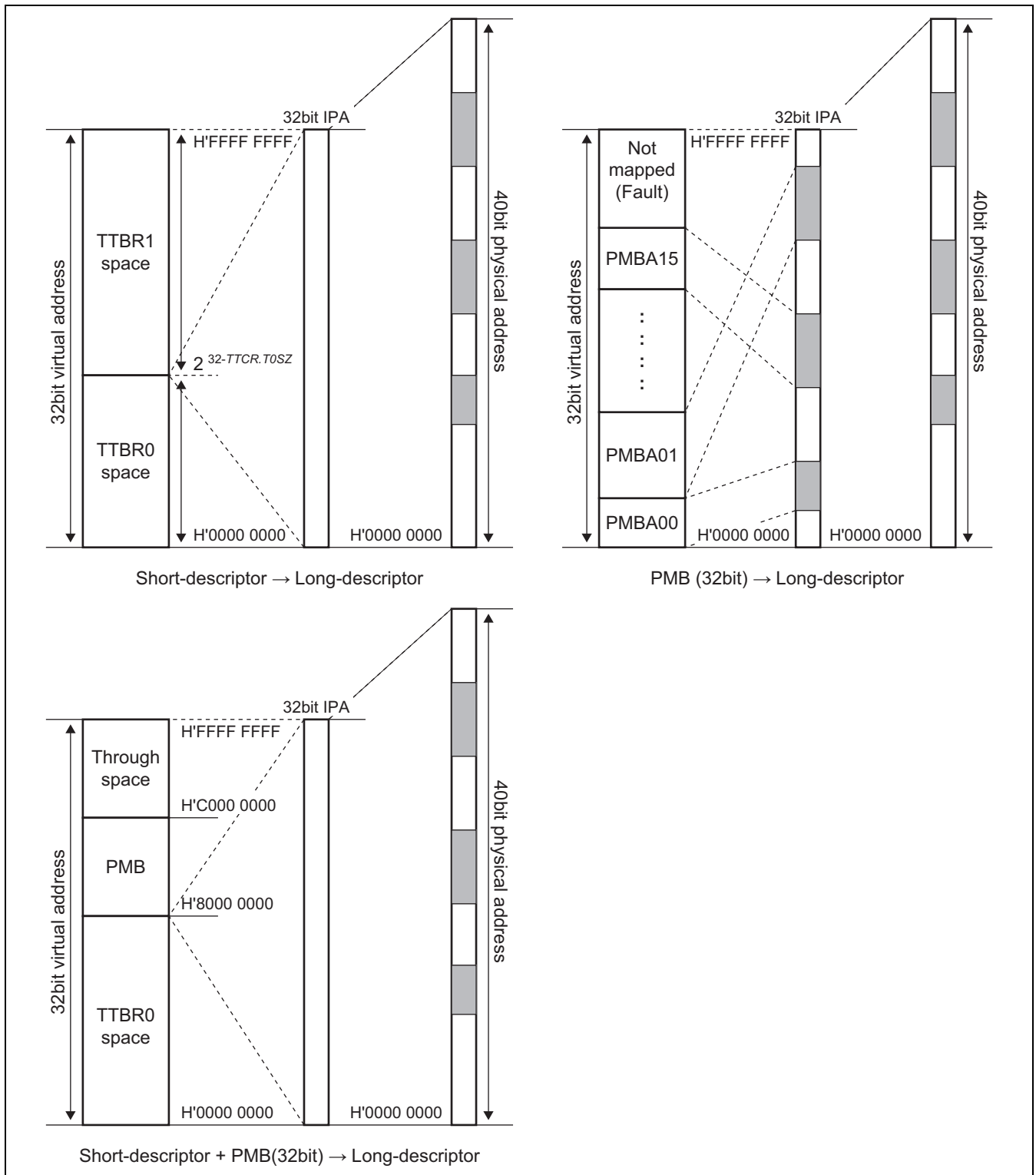


Figure 13.8 2-Stage Translation Address Space



### 13.4.4 Initialization Sequence

This section describes the initialization sequence of the IPMMU.

#### (1) Module Stop

The IPMMU doesn't support module stop control. The IPMMU can be used whenever a master requires address translation through the IPMMU. When a master doesn't require address translation, the corresponding IMUCTRn MMUEN must be disabled.

#### (2) micro-TLB

Before a master access, the corresponding micro-TLB registers which includes the translation mode and ASIDs must be configured.

### 13.4.5 TLB Maintenance

Some TLB maintenances between an IPMMU and the connected micro-TLBs are performed automatically by hardware. When DVM operation is permitted (IMBUSCRn.DVM = 1), coherency between System CPUs and IPMMUs can be maintained automatically through CCI.

**Table 13.4 TLB Maintenance**

Category	Software operation	TLB maintenance in IPMMU	TLB maintenance in micro-TLB
MMU Page Table (DVM is disabled)	First entry registration	Not required	Not required
	Entry update	Invalidate the target TLB (IMCTRn.FLUSH = 1)	Automatically invalidated
	Entry release	Invalidate the target TLB (IMCTRn.FLUSH = 1)	Automatically invalidated
MMU Page Table (DVM is enabled)	First entry registration	Not required	Not required
	Entry update	Automatically invalidated	Automatically invalidated
	Entry release	Automatically invalidated	Automatically invalidated
ASID	ASID update	Automatically invalidated	Automatically invalidated
MMU registers	MMU register values update	Invalidate the target TLB (IMCTRn.FLUSH = 1)	Automatically invalidated
PMB	PMB entry registration	Not required	Not required
	PMB entry update	Not required	Invalidate the target micro-TLB
	PMB entry release	Not required	Invalidate the target micro-TLB

### 13.4.6 Security Extensions

The IPMMU supports the ARMv7 Security Extensions and additional extensions.

#### (1) Banked Registers

The IPMMU has two copies of a register at the same address. They are banked with secure and non-secure. A Non-secure access can read and write only non-secure registers and a secure access can read and write secure registers. A secure access can also read and write non-secure registers through the alias address space to non-secure registers (from H'0800 to H'0FFF).

#### (2) Secure-Group

Besides Secure access, some IPMMUs support another secure access called accelerator. The IPMMU which supports Accelerator treats it as secure and performs its page table walk in secure mode. Table 13.5 shows the supported secure mode of IPMMU.

**Table 13.5 Supported Secure Mode**

IPMMU	Secure	Accelerator
IPMMUSY0	√	√
IPMMUSY1	√	√
IPMMUDS	√	√
IPMMUMP	√	√
IPMMUMX	√	√
IPMMUGP	√	√

#### (3) Address Translation

When a Secure/Accelerator master sends a translation request to an IPMMU through a micro-TLB, Secure MMU registers are referred to perform its page table walk. The Secure page table walk can read secure page table entries (NS = 0). In the case of a Non-secure translation request, Non-secure MMU registers are referred and the access to secure page table entries is ignored.

### 13.4.7 Coherency Support

The IPMMU provides the two ways to keep TLB coherency between System CPUs. They are controlled by IMBUSCRn registers.

#### (1) Shared Page Table Access

When IMBUSCRn.BUSSEL = 1 and the memory attribute of page table is shareable, the IPMMU issues transactions to perform page table walk through CCI which ensures to keep TLB coherency between System CPUs. If data hits in the CPU cache, then its response is returned directly to the IPMMU without SDRAM access. It also allows system CPUs not to flush their cache.

#### (2) Distributed Virtual Memory (DVM) Messages

DVM messages are the broadcast messages which send the information of TLB Invalidation. DVM messages are issued by system CPUs through CCI when they no longer use a TLB entry and invalidate it. When IMBUSCRn.DVM = 1 and the IPMMU has the entry specified by the DVM operation, the IPMMU invalidate it in its main TLB and the connected micro-TLBs' entries. It allows system CPUs to keep TLB coherency without software TLB maintenance.

### 13.4.8 Error Handling

#### (1) IPMMU Interrupt Requests

Table 13.6 shows the error events which can cause interrupts. The errors in secure access are set in IMSSTRn registers and the errors in non-secure access are set in IMSTRn registers.

**Table 13.6 IPMMU Error Events**

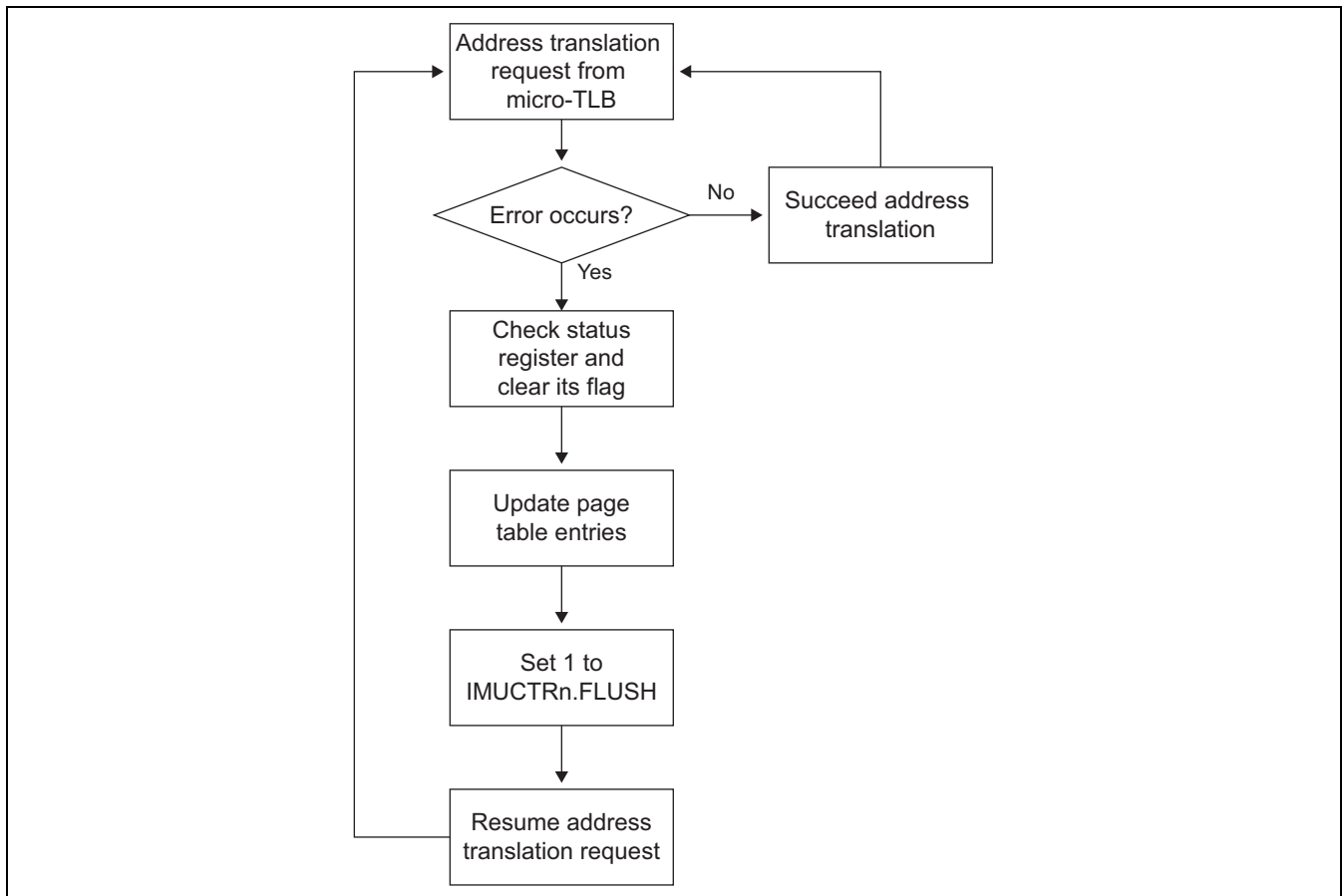
Category	Error	Description
Long-descriptor Short-descriptor	Translation Fault	A virtual address was not mapped in the region defined by TTBR0 and TTBR1.*
		A descriptor was neither Table nor Block format
	Page Fault	AP (access permissions) / AF (access flag) bit mismatch occurred. NS bit mismatch occurred. Non-secure master read a Secure page table entry.
	Abort	The IPMMU got an error response from an Interconnect during a page table walk.
PMB	Multiple Hit (MHIT)	Multiple TLB hits occurred.
	Translation Fault	A virtual address was not mapped in IMPMBAn.
	Multiple Hit (MHIT)	Multiple PMB hits occurred.

Note: \* This factor is only for long-descriptor.

## (2) Error Handling Flow

When the micro-TLB cannot translate its virtual address because of some IPMMU errors, the micro-TLB stops to issue the following transactions. When the IPMMU detects an error, IMCTRn.FLUSH must be set after the IMSTRn/IMSSTRn register is cleared and page table entries are updated. After the TLB invalidation, the micro-TLB resumes to issue transactions.

Figure 13.9 shows the error handling flow.



**Figure 13.9 Error Handling Flow**

## 13.5 micro-TLB Assignment

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

The assignment of micro-TLB varies with the RZ/G series products. Refer to the following sections.

### 13.5.1 micro-TLB Assignment

**Table 13.7 micro-TLB Assignment in IPMMUSY0**

micro-TLB	Master Module		
	[RZ/G1H]	[RZ/G1M/N]	[RZ/G1E]
00	Reserved	Reserved	Reserved
01	Reserved	Reserved	Reserved
02	Reserved	Reserved	Reserved
03	R-GP2D	Reserved	Reserved
04	Reserved	Reserved	Reserved
05	Reserved	Reserved	Reserved
06	Reserved	Reserved	Reserved
07	Reserved	Reserved	Reserved
08	SATA 0	SATA 0	Reserved
09	SATA 1	SATA 1	Reserved
10	Reserved	Reserved	Reserved
11	Reserved	Reserved	Reserved
12	LBSC	LBSC	LBSC

**Table 13.8 micro-TLB Assignment in IPMMUSY1**

micro-TLB	Master Module		
	[RZ/G1H]	[RZ/G1M/N]	[RZ/G1E]
00	USB-DMAC ch.0	USB-DMAC ch.0	USB-DMAC ch.0
01	USB-DMAC ch.1	USB-DMAC ch.1	USB-DMAC ch.1
02	Reserved	Reserved	Reserved
03	Reserved	Reserved	Reserved
04	USB3.0H Host	USB3.0H Host	Reserved
05	Reserved	Reserved	Reserved
06	USB2.0H Host ch.0	USB2.0H Host ch.0	USB2.0H Host ch.0
07	PCIEC	PCIEC	Reserved
08	USB2.0H Host ch.1	Reserved	Reserved
09	USB2.0H Host ch.2	USB2.0H Host ch.1	USB2.0H Host ch.1
10	Ethernet AVB	Ethernet AVB	Ethernet AVB
11	Ethernet MAC	Ethernet MAC	Ethernet MAC
12	USB-DMAC (DDM)	USB-DMAC (DDM)	USB-DMAC (DDM)
13	Reserved	Reserved	Reserved

**Table 13.9** micro-TLB Assignment in IPMMUDS

micro-TLB	Master Module
	[RZ/G1H/M/N/E]
00	SYS-DMAC ch.0
01	SYS-DMAC ch.1
02	SYS-DMAC ch.2
03	SYS-DMAC ch.3
04	SYS-DMAC ch.4
05	SYS-DMAC ch.5
06	SYS-DMAC ch.6
07	SYS-DMAC ch.7
08	SYS-DMAC ch.8
09	SYS-DMAC ch.9
10	SYS-DMAC ch.10
11	SYS-DMAC ch.11
12	SYS-DMAC ch.12
13	SYS-DMAC ch.13
14	SYS-DMAC ch.14
15	SYS-DMAC ch.15
16	SYS-DMAC ch.16
17	SYS-DMAC ch.17
18	SYS-DMAC ch.18
19	SYS-DMAC ch.19
20	SYS-DMAC ch.20
21	SYS-DMAC ch.21
22	SYS-DMAC ch.22
23	SYS-DMAC ch.23
24	SYS-DMAC ch.24
25	SYS-DMAC ch.25
26	SYS-DMAC ch.26
27	SYS-DMAC ch.27
28	SYS-DMAC ch.28
29	SYS-DMAC ch.29
30	Reserved
31	Reserved

**Table 13.10** micro-TLB Assignment in IPMMUMP

micro-TLB	Master Module		
	[RZ/G1H]	[RZ/G1M/N]	[RZ/G1E]
00	Reserved	Reserved	Reserved
01	Reserved	Reserved	Reserved
02	Reserved	Reserved	Reserved
03	Reserved	Reserved	Reserved
04	Audio DMAC ch.0	Audio DMAC ch.0	Audio DMAC ch.0
05	Audio DMAC ch.1	Audio DMAC ch.1	Audio DMAC ch.1
06	Audio DMAC ch.2	Audio DMAC ch.2	Audio DMAC ch.2
07	Audio DMAC ch.3	Audio DMAC ch.3	Audio DMAC ch.3
08	Audio DMAC ch.4	Audio DMAC ch.4	Audio DMAC ch.4
09	Audio DMAC ch.5	Audio DMAC ch.5	Audio DMAC ch.5
10	Audio DMAC ch.6	Audio DMAC ch.6	Audio DMAC ch.6
11	Audio DMAC ch.7	Audio DMAC ch.7	Audio DMAC ch.7
12	Audio DMAC ch.8	Audio DMAC ch.8	Audio DMAC ch.8
13	Audio DMAC ch.9	Audio DMAC ch.9	Audio DMAC ch.9
14	Audio DMAC ch.10	Audio DMAC ch.10	Audio DMAC ch.10
15	Audio DMAC ch.11	Audio DMAC ch.11	Audio DMAC ch.11
16	Audio DMAC ch.12	Audio DMAC ch.12	Audio DMAC ch.12
17	Audio DMAC ch.13	Audio DMAC ch.13	Reserved
18	Audio DMAC ch.14	Audio DMAC ch.14	Reserved
19	Audio DMAC ch.15	Audio DMAC ch.15	Reserved
20	Audio DMAC ch.16	Audio DMAC ch.16	Reserved
21	Audio DMAC ch.17	Audio DMAC ch.17	Reserved
22	Audio DMAC ch.18	Audio DMAC ch.18	Reserved
23	Audio DMAC ch.19	Audio DMAC ch.19	Reserved
24	Audio DMAC ch.20	Audio DMAC ch.20	Reserved
25	Audio DMAC ch.21	Audio DMAC ch.21	Reserved
26	Audio DMAC ch.22	Audio DMAC ch.22	Reserved
27	Audio DMAC ch.23	Audio DMAC ch.23	Reserved
28	Audio DMAC ch.24	Audio DMAC ch.24	Reserved
29	Audio DMAC ch.25	Audio DMAC ch.25	Reserved

**Table 13.11 micro-TLB Assignment in IPMMUMX**

micro-TLB	Master Module		
	[RZ/G1H]	[RZ/G1M/N]	[RZ/G1E]
00	Reserved	Reserved	Reserved
01	Reserved	Reserved	Reserved
02	Reserved	Reserved	Reserved
03	2D-DMAC	2D-DMAC	2D-DMAC
04	VSPR-CTU/VSPS-CTU	VSPS-CTU	VSPS-CTU
05	VSPD-CTU ch.0/1	VSPD-CTU ch.0/1	VSPD-CTU ch.0
06	VSPR	Reserved	Reserved
07	FDP1 ch.0	FDP1 ch.0	FDP ch.0
08	IMR-LSX2	Reserved	Reserved
09	FDP1 ch.2	Reserved	Reserved
10	VSPS	VSPS	VSPS
11	FDP1 ch.1	FDP1 ch.1	Reserved
12	IMR-X2	Reserved	Reserved
13	VSPD ch.0	VSPD ch.0	VSPD ch.0
14	VSPD ch.1	VSPD ch.1	Reserved
15	DU0	DU0	DU0
16	DU1	Reserved	Reserved
17	VCP3-CE ch.0	VCP3-CE ch.0	VCP3-CE ch.0
18	VCP3-VLC ch.0	VCP3-VLC ch.0	VCP3-VLC ch.0
19	VPC ch.0	VPC ch.0	VPC ch.0
20	VCP3-CE ch.1	Reserved	Reserved
21	VCP3-VLC ch.1	Reserved	Reserved
22	VPC ch.1	Reserved	Reserved
23	VIN ch.0/1/2/3	VIN ch.0/1/2	VIN ch.0/1

**Table 13.12 micro-TLB Assignment in IPMMUGP**

micro-TLB	Master Module		
	[RZ/G1H]	[RZ/G1M/N]	[RZ/G1E]
00	Reserved	SGX544MP2 master I/F (ch.0)	SGX540 master I/F (ch.0)
01	Reserved	SGX544MP2 master I/F (ch.1)	SGX540 master I/F (ch.1)



## 14. LBSC within Bus Bridge

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

### 14.1 Overview

The LBSC performs bus arbitration and necessary interface conversion for the accesses from the CPU (AXI bus) and DMA accesses from LBSC-DMAC channels 0 to 2 and outputs them to the external buses. Further, for external bus access, various settings can be specified in the LBSC control registers for the selection of a connection interface type for each area on the external bus or for the adjustment of number of setup/hold cycles on addresses and chip select signals with respect to read/write enable signals. Thus, the LBSC configuration allows diversity in methodology for accessing various external devices that are assigned to their corresponding areas.

The frequency of the external bus clock CLKOUT signal is up to 65.0 MHz. The LBSC outputs bus signals in synchronization with the external bus clock.

### 14.2 Features

The key features of the LBSC include:

- Support for areas 0, 1, and 6
  - Each area is allocated to EX-BUS, and SRAM, ATA, or byte-control SRAM bus protocol can be selected.
  - Controls 64 Mbytes of area 6 divided into up to six areas (each area capacity is variable).
  - Interface, bus size, and wait-cycle insertion can be controlled in each area.
  - Provides bus signals in synchronization with the CLKOUT signal (65.0 MHz/43.33 MHz).
    - Note: Both of clocks at 65.0 MHz and 43.33 MHz are available only for the RZ/G1H.
- External DMA transfer (for details on DMAC, refer to section 17, LBSC-DMAC).
  - Three channels
  - Support of devices with the DACK signal
  - Support of edge-detection and level-detection external request signals
  - Synchronous/asynchronous DREQ and the polarity of DREQ, DACK, and DRACK can be inverted through register settings.
- SRAM interface
  - Wait-cycle insertion can be controlled through register settings.
  - Wait cycles can be inserted with the EX\_WAIT pins.
  - Connectable bus size: 16 or 8 bits.
- Burst ROM interface (area 0 and CPU access only)
  - Wait-cycle insertion can be controlled through register settings.
  - Burst count can be specified through register settings (cases where this reaches an address branching point are automatically detected, after which the access is broken off).
  - Connectable bus size: 16 or 8 bits
- Byte-control SRAM interface (areas 1 and 6 only)
  - SRAM interface with byte control
  - Wait-cycle insertion can be controlled through register settings.
  - Wait cycles can be inserted with the EX\_WAIT pins.
  - Connectable bus size: 16 or 8 bits

- ATA interface (areas 1 and 6 only)
  - Two ports
  - Wait-cycle insertion can be controlled through register settings.
  - Support for PIO modes 0 to 4
  - Support for multi-word transfer
  - Ready timeout detection (detection time in ns = period in ns at EX-BUS operating frequency × 100 clock cycles)
- Wait timeout
  - Wait timeout detection
    - Detection time in ns = period in ns at EX-BUS operating frequency × (the time specified in the EX-BUS wait timeout base counter register (EXBCT) and EX-BUS wait timeout detection counter register (EXTCT))

### 14.3 Block Diagram

Figure 14.1 is a block diagram of the LBSC. Placed on the AXI bus, the LBSC outputs accesses from the CPU in sequence to an external bus according to the settings that are provided in internal registers of the LBSC. For the external bus EX-BUS, either of the SRAM or ATA bus protocol can be selected. In addition, the LBSC incorporates three LBSC-DMAC channels that control DMA transfers between an external bus and the DDR3-SDRAM. For details on the LBSC-DMAC, see the relevant section. Since the CPU and the LBSC-DMAC generate access contention for an external bus, the BSC uses an arbiter unit to arbitrate such access requests. The access request that was selected by means of arbitration is converted into an external bus waveform by the bus interface unit before being output. The LBSC has an external wait control input that controls the pulse width. When a request for access is received by an external device, the external device uses this to control the wait for a response to suit the situation at the time of access-request reception.

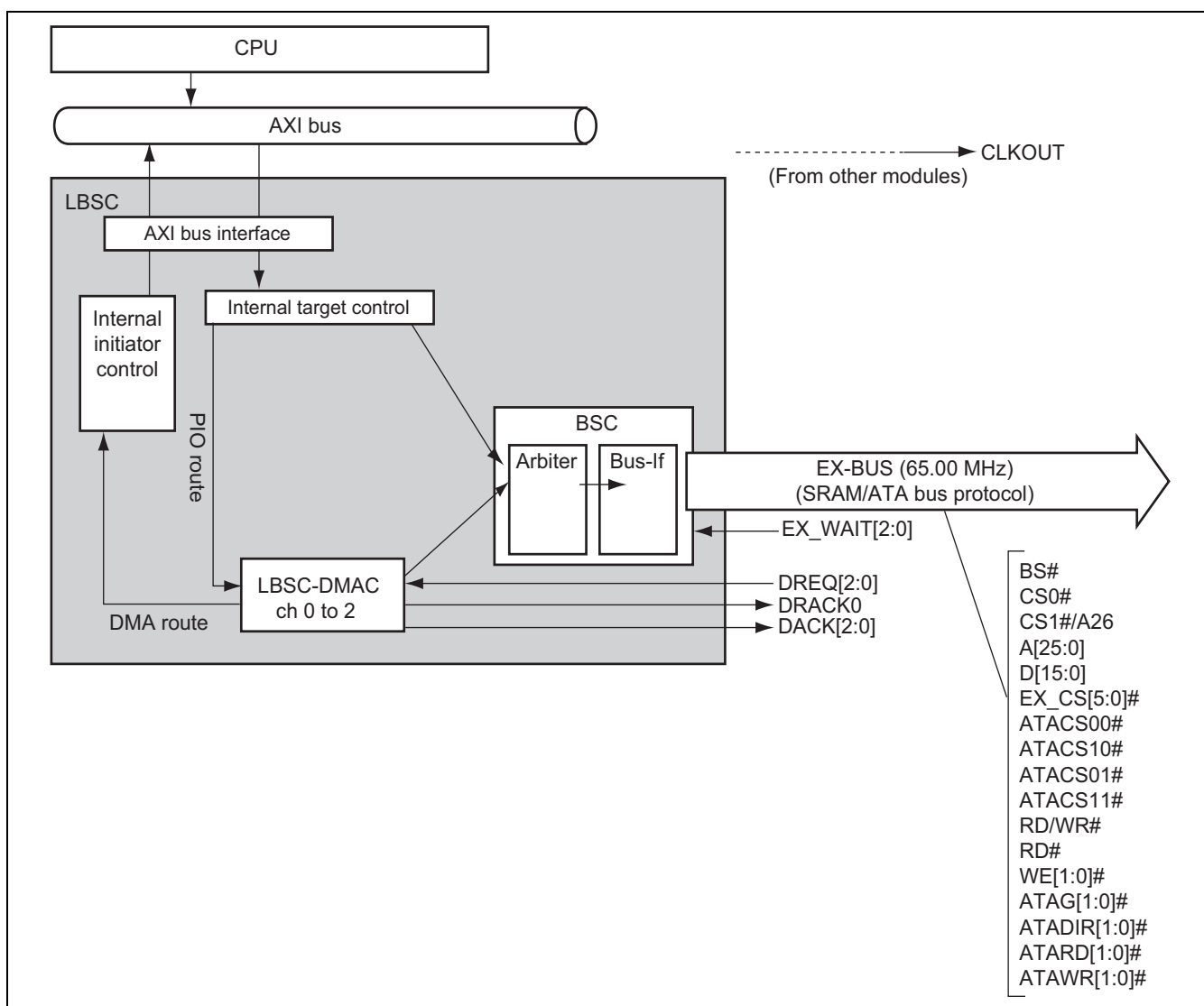


Figure 14.1 Block Diagram of LBSC

## 14.4 LBSC Areas

### 14.4.1 LBSC Support Areas

Figure 14.2 shows LBSC response support areas from the CPU.

The basic configuration of the LBSC supports area 0 and area 1 as external spaces; and area 6 as an expansion I/O space. Area 6 can be subdivided into a maximum of six units, each having a maximum of 64 Mbytes as determined by register settings. The total capacity for area 6 is also up to 64 Mbytes. For area 0 can be made into a 128-Mbyte space depending on the specific LSI startup mode (MD4 mode pin) in use (the MD4 mode pin = 1). In this case, however, area 1 is completely allocated as a space in area 0, and the CS1# signal is changed to the signal equivalent to A[26] in a bus address (addition of one bit to the address signal changes the capacity from 64 Mbytes to 128 Mbytes).

Registers of the BSC and LBSC-DMAC are provided in the internal register space of the LBSC.

LBSC response support area		[MD4 = 0]		[MD4 = 1]	
H'0000 0000 to	Area 0 CS0 64 Mbytes	Area 0 CS0 128 Mbytes			
H'03FF FFFF					
H'0400 0000 to H'07FF FFFF	Area 1 CS1 64 Mbytes				
H'0800 0000 to H'17FF FFFF	Other module space		Other module space		
H'1800 0000 to	Area 6 Expansion area 0 EX_CS0 0 to 64 Mbytes	Area 6 Expansion area 0 EX_CS0 0 to 64 Mbytes	Expansion area 1 EX_CS1 0 to 64 Mbytes	Expansion area 1 EX_CS1 0 to 64 Mbytes	Expansion area 2 EX_CS2 0 to 64 Mbytes
	External expansion I/O area	External expansion I/O area	Expansion area 3 EX_CS3 0 to 64 Mbytes	Expansion area 3 EX_CS3 0 to 64 Mbytes	Expansion area 4 EX_CS4 0 to 64 Mbytes
	Expansion area 4 EX_CS4 0 to 64 Mbytes	Expansion area 5 EX_CS5 0 to 64 Mbytes	Expansion area 5 EX_CS5 0 to 64 Mbytes		
H'1BFF FFFF	64 Mbytes	64 Mbytes			
H'1C00 0000 to H'FEFB FFFF	Other module space		Other module space		
H'FEC0 0000 to H'FEFF FFFF	Space for LBSC internal registers		BSC: from H'FEC0 0000, LBSC-DMAC: from H'FEC0 1000		

Figure 14.2 LBSC Response Support Areas from the CPU

### 14.4.2 Functionality Supported in Each Area

Table 14.1 lists the functions supported by the LBSC in each area on the EX-BUS.

**Table 14.1 Functions Supported in Each Area on EX-BUS**

Area	Bus	Capacity	Operating Mode	Guard interval	WAIT Function	
0	8/16 bits	64/128 Mbytes selectable Area 0 divided MD4 pin specified	SRAM DMA Burst ROM	Disabled	Enabled	
1	8/16 bits	Fixed to 64 Mbytes When area 0 = 128 Mbytes, no space exists.	SRAM DMA ATA (PIO) Byte-control SRAM	Enabled	Enabled	
Expansion area	0	8/16 bits	0 to 64 Mbytes Total capacity of expansion areas: 64 Mbytes	SRAM DMA ATA (PIO) Byte-control SRAM	Enabled	Enabled
	1	8/16 bits	0 to 64 Mbytes Total capacity of expansion areas: 64 Mbytes	SRAM DMA ATA (PIO) Byte-control SRAM	Enabled	Enabled
	2	8/16 bits	0 to 64 Mbytes Total capacity of expansion areas: 64 Mbytes	SRAM DMA ATA (PIO) Byte-control SRAM	Enabled	Enabled
	3	8/16 bits	0 to 64 Mbytes Total capacity of expansion areas: 64 Mbytes	SRAM DMA ATA (PIO) Byte-control SRAM	Enabled	Enabled
	4	8/16 bits	0 to 64 Mbytes Total capacity of expansion areas: 64 Mbytes	SRAM DMA ATA (PIO) Byte-control SRAM	Enabled	Enabled
	5	8/16 bits	0 to 64 Mbytes Total capacity of expansion areas: 64 Mbytes	SRAM DMA ATA (PIO) Byte-control SRAM	Enabled	Enabled

- Notes:
1. The bus size for area 0 is specified with the LSI mode pins (MD8 = 0: 8 bits, MD8 = 1: 16 bits).
  2. When using area 0 in 128-Mbyte mode (MD4 = 1), no space exists for area 1.
  3. When accessing through EX-BUS, A[0] is output as byte address even if 16-bit bus is selected.
  4. One DMAC channel cannot be allocated to two areas simultaneously.
  5. The capacity of one expansion area is a maximum of 64 Mbytes. Total capacity of expansion areas is also a maximum of 64 Mbytes.

## 14.5 Register Descriptions

The LBSC set registers to control the interface, bus size, RD/WE# signal pulse cycles, and setup and hold cycles for the CS# signal with respect to the RD/WE# signal, for each of externally connected devices. Table 14.2 lists registers of the LBSC. Note that correct operation is not guaranteed in principle if each register is modified during external bus access (for register modification in other cases, refer to the note under specific register description).

**Table 14.2 LBSC Register Configuration**

Register Name	Abbreviation	Access Type	Value after Power-On Reset	Address	Access Size	Remarks	RZ/G Series Products			
							RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Area 0 control register	CS0CTRL	R/W	Undefined	H'FEC0 0200	32		√	√	√	√
Area 1 control register	CS1CTRL	R/W	H'0000 0020	H'FEC0 0204	32		√	√	√	√
Expansion area x control register	ECSxCTRL	R/W	H'0000 0020	H'FEC0 0208 to H'FEC0 021C	32	x = 0 to 5	√	√	√	√
Area 0 RD/WE pulse control register	CSWCR0	R/W	H'077F 077F [RZ/G1H] H'FF70 FF70 [RZ/G1M/N/E]	H'FEC0 0230	32		√	√	√	√
Area 1 RD/WE pulse control register	CSWCR1	R/W	H'077F 077F [RZ/G1H] H'FF70 FF70 [RZ/G1M/N/E]	H'FEC0 0234	32		√	√	√	√
Expansion area x RD/WE pulse control register	ECSWCRx	R/W	H'077F 077F [RZ/G1H] H'FF70 FF70 [RZ/G1M/N/E]	H'FEC0 0238 to H'FEC0 024C	32	x = 0 to 5	√	√	√	√
LBSC-DMAC channel y RD/WE pulse control register	EXDMAWCry	R/W	H'077F 077F [RZ/G1H] H'FF70 FF70 [RZ/G1M/N/E]	H'FEC0 0250 to H'FEC0 0258	32	y = 0 to 2	√	√	√	√
Area 0 external wait control register	CSPWCR0	R/W	H'0000 0000	H'FEC0 0280	32		√	√	√	√
Area 1 external wait control register	CSPWCR1	R/W	H'0000 0000	H'FEC0 0284	32		√	√	√	√
Expansion area x external wait control register	ECSPWCRx	R/W	H'0000 0000	H'FEC0 0288 to H'FEC0 029C	32	x = 0 to 5	√	√	√	√
External wait input control register	EXWTSYNC	R/W	H'0000 0000	H'FEC0 02A0	32		√	√	√	√
Area 0 burst control register	CS0BSTCTL	R/W	H'0000 0000	H'FEC0 02B0	32		√	√	√	√
Area 0 burst pitch set register	CS0BTPH	R/W	H'0000 00F7	H'FEC0 02B4	32		√	√	√	√
Area 1 guard setting register	CS1GDST	R/W	H'0000 0000	H'FEC0 02C0	32		√	√	√	√

Register Name	Abbreviation	Access Type	Value after Power-On Reset	Address	Access Size	Remarks	RZ/G Series Products			
							RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Expansion area x guard setting register	ECSxGDST	R/W	H'0000 0000	H'FEC0 02C4 to H'FEC0 02D8	32	x = 0 to 5	√	√	√	√
LBSC-DMAC channel y area allocation register	EXDMASETy	R/W	H'0000 0000	H'FEC0 02F0 to H'FEC0 02F8	32	y = 0 to 2	√	√	√	√
LBSC-DMAC channel y control register	EXDMCRy	R/W	H'0000 0000	H'FEC0 0310 to H'FEC0 0318	32	y = 0 to 2	√	√	√	√
BSC interrupt source status register	BCINTSR	R	H'0000 0000	H'FEC0 0330	32		√	√	√	√
BSC interrupt source clear register	BCINTCR	—/WC1	H'0000 0000	H'FEC0 0334	32		√	√	√	√
BSC interrupt enable register	BCINTMR	R/W	H'0000 0000	H'FEC0 0338	32		√	√	√	√
EX-BUS priority level set register	EXBATLV	R/W	H'0000 0000	H'FEC0 0340	32		√	√	√	√
External wait status register	EXWTSTS	R	Undefined	H'FEC0 0344	32		√	√	√	√
ATACS control register	ATACCTRL	R/W	H'0000 0000	H'FEC0 0380	32		√	√	√	√
EX-BUS wait timeout detection base counter register	EXBCT	R/W	H'0000 0000	H'FEC0 03C0	32		√	√	√	√
EX-BUS wait timeout detection counter register	EXTCT	R/W	H'0000 0000	H'FEC0 03C4	32		√	√	√	√
EX-BUS wait timeout detection access source indication register	EXTSR	R/WC1	H'0000 0000	H'FEC0 0010	32		√	√	√	√
EX-BUS wait timeout detection address indication register	EXTADR	R/W	H'0000 0000	H'FEC0 0014	32		√	√	√	√

Notes: Do not write to any addresses other than listed above. Operations cannot be guaranteed if writing is attempted. Values read from addresses other than those listed above are undefined.

#### [Legend]

Initial value: Register value after a reset

—: Undefined value

R/W: Readable/writable. The written value can be read.

R/WC1: Readable/writable. Writing 1 initializes the bit. Writing 0 is ignored.

- R: Read-only. The write value should always be 0.
- /W: Write-only. The read value is undefined.
- /WC1: Write-only. Writing 1 initializes the bit. Writing 0 is ignored.



**14.5.1 Area 0 Control Register (CS0CTRL)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: CS0CTRL specifies the interface in area 0 (EX-BUS).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	128B	—	—	CS0SZ		—	—	CS0IF	
Initial value:	1	0	0	0	0	0	0	—	0	0	—	—	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15	—	1	R	Reserved These bits are always read as 1. The write value should always be 1.
14 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	128B	—	R	Area 0 Capacity Indication (These bits indicate the value specified by the LSI mode pin MD4.) 0: 64 Mbytes 1: 128 Mbytes
7, 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5, 4	CS0SZ	—	R	Area 0 Bus Size Indication (These bits indicate the value specified by the LSI mode pin MD8.) 00: Setting prohibited 01: 8 bits 10: 16 bits 11: Setting prohibited
3, 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1, 0	CS0IF	00	R/W	Area 0 Interface Selection 00: Standard (SRAM) 01: Burst ROM 10: Setting prohibited 11: Setting prohibited

- Notes:
1. Even when the burst ROM interface is selected by setting CS0IF = B'01, burst ROM operation is not available unless appropriate setting is made in CS0BSTCTL. Be sure to specify both CS0BSTCTL and CS0BTPH before using the burst ROM interface.
  2. Setting of burst ROM is valid for CPU access only. For DMA transfer access to area 0, SRAM interface (enabled when EXDMAWCR/CSPWCR0 is valid) is usually selected.

### 14.5.2 Area 1 Control Register (CS1CTRL)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

**Function:** CS1CTRL specifies the interface in area 1 (EX-BUS).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	CS1SZ		—	CS1BRM	CS1IF	
Initial value:	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 17	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
16	—	0	R/W	Reserved This bit is always read as 0. The write value should always be 0.
15 to 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5, 4	CS1SZ	10	R/W	Area 1 Bus Size Selection 00: Setting prohibited 01: 8 bits 10: 16 bits 11: Setting prohibited
3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
2	CS1BRM	0	R/W	Area 1 Byte-Control SRAM Mode Selection (valid only when CS1IF = 01) 0: Same cycle as CS# 1: Same cycle as RD#
1, 0	CS1IF	00	R/W	Area 1 Interface Selection 00: Standard (SRAM) 01: Byte-control SRAM 10: ATA 11: Setting prohibited

### 14.5.3 Expansion Area x Control Register (ECSxCTRL (x = 0 to 5))

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

**Function:** ECSxCTRL specifies the interface and area capacity for expansion areas 0 to 5 (EX-BUS).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	ECSxCP						—	—	ECSxSZ		—	ECSxBRM	ECSxIF		
Initial value:	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 17	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
16	—	0	R/W	Reserved This bit is always read as 0. The write value should always be 0.
15	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
14 to 8	ECSxCP	H'00	R/W	Expansion Area x Capacity Setting (see the notes below.) The value set in these bits × 1 Mbyte is the capacity of the respective expansion area.
7, 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5, 4	ECSxSZ	10	R/W	Expansion Area x Bus Size Selection 00: Setting prohibited 01: 8 bits 10: 16 bits 11: Setting prohibited
3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
2	ECSxBRM	0	R/W	Expansion Area x Byte-Control SRAM Mode Selection (valid only when ECSxIF = 01) 0: Same cycle as CS# 1: Same cycle as RD#
1, 0	ECSxIF	00	R/W	Expansion Area x Interface Selection 00: Standard (SRAM) 01: Byte-control SRAM 10: ATA 11: Setting prohibited

- Notes:
1. If the sum of all ECSxCP setting values exceeds 64 (= 64 Mbytes), the excess capacity is ignored.  
Example: When the registers are set to ECS0CP = 40 Mbytes, ECS1CP = 30 Mbytes, and ECS2CP = 20 Mbytes, the excess capacity is ignored. That is, ECS0CP = 40 Mbytes, ECS1CP = 24 Mbytes, and ECS2CP = 0 Mbytes.
  2. The area-capacity setting in the ECS5CTRL register (ECS5CP bits) has no effect. Regardless of the setting, the capacity of expansion area 5 will be 64 Mbytes – (sum of capacities for ECS0CP to ECS4CP). Accordingly, if the sum of the ECS0CP to ECS4CP settings exceeds 64 Mbytes, the capacity for expansion area 5 will be 0 Mbytes.
  3. Intermediate areas can be set to 0 Mbytes. Specify 0 Mbytes for the area where the CS# signal cannot be used by selecting the pin multiplex exclusive signal. If the capacity other than 0 Mbytes is specified for the area, the allocated area cannot be used.
  4. For the expansion area capacity setting and area division, refer to section 14.6.1 (1), Address Generation/Alignment.

### 14.5.4 Area 0 RD/WE Pulse Control Register (CSWCR0)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

**Function:** CSWCR0 specifies the RD/WE# pulse cycles and setup and hold cycles for the CS# signal and address during access to area 0 (EX-BUS). (The settings for read access are ignored when the burst ROM interface is selected.)

[RZ/G1H]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	WRITE CS SETUP CYCLE			—	WRITE CS HOLD CYCLE			WRITE CS PULSE CYCLE			
Initial value:	0	0	0	0	0	1	1	1	0	1	1	1	1	1	1	1
R/W:	R	R	R	R	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	READ CS SETUP CYCLE			—	READ CS HOLD CYCLE			READ CS PULSE CYCLE			
Initial value:	0	0	0	0	0	1	1	1	0	1	1	1	1	1	1	1
R/W:	R	R	R	R	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[RZ/G1M/N/E]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	WRITE PULSE CYCLE					WRITE CS SETUP CYCLE			—	WRITE CS HOLD CYCLE			—	—	—	—
Initial value:	1	1	1	1	1	1	1	1	0	1	1	1	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	READ PULSE CYCLE					READ CS SETUP CYCLE			—	READ CS HOLD CYCLE			—	—	—	—
Initial value:	1	1	1	1	1	1	1	1	0	1	1	1	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 27	—	00000	R	Reserved [RZ/G1H] These bits are always read as 0. The write value should always be 0.
	WRITE PULSE CYCLE	11111	R/W	These bits specify the WE# pulse cycles during writing to area 0. [RZ/G1M/N/E] 00000: Setting prohibited 00001: 1-cycle pulse 00010: 2-cycle pulse 00011: 3-cycle pulse 00100: 4-cycle pulse : 11101: 29-cycle pulse 11110: 30-cycle pulse 11111: 31-cycle pulse

Bit	Bit Name	Initial Value	R/W	Description
26 to 24	WRITE CS SETUP CYCLE	111	R/W	These bits specify the CS# and address setup cycles with respect to the WE# signal during writing to area 0. 000: 0 cycle for setup period 001: 1 cycle for setup period 010: 2 cycles for setup period : 110: 6 cycles for setup period 111: 7 cycles for setup period
23	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
22 to 20	WRITE CS HOLD CYCLE	111	R/W	These bits specify the CS# and address hold cycles with respect to the WE# signal during writing to area 0. 000: 0 cycle for hold period 001: 1 cycle for hold period 010: 2 cycles for hold period : 110: 6 cycles for hold period 111: 7 cycles for hold period
19 to 16	WRITE PULSE CYCLE	1111	R/W	These bits specify the WE pulse cycles during writing to area 0. [RZ/G1H] 0000: Setting prohibited 0001: 1-cycle pulse 0010: 2-cycle pulse 0011: 3-cycle pulse 0100: 4-cycle pulse : 1110: 14-cycle pulse 1111: 15-cycle pulse
	—	0000	R	Reserved [RZ/G1M/N/E] These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
15 to 11	—	00000	R	Reserved [RZ/G1H] These bits are always read as 0. The write value should always be 0.
	READ PULSE CYCLE	11111	R/W	These bits specify the RD# pulse cycles during reading from area 0. [RZ/G1M/N/E] 00000: Setting prohibited 00001: 1-cycle pulse 00010: 2-cycle pulse 00011: 3-cycle pulse 00100: 4-cycle pulse : 11101: 29-cycle pulse 11110: 30-cycle pulse 11111: 31-cycle pulse
10 to 8	READ CS SETUP CYCLE	111	R/W	These bits specify the CS# and address setup cycles with respect to the RD# signal during reading from area 0. 000: 0 cycle for setup period 001: 1 cycle for setup period 010: 2 cycles for setup period : 110: 6 cycles for setup period 111: 7 cycles for setup period
7	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
6 to 4	READ CS HOLD CYCLE	111	R/W	These bits specify the CS# and address hold cycles with respect to the RD# signal during reading from area 0. 000: 0 cycle for hold period 001: 1 cycle for hold period 010: 2 cycles for hold period : 110: 6 cycles for hold period 111: 7 cycles for hold period
3 to 0	READ PULSE CYCLE	1111	R/W	These bits specify the RD# pulse cycles during reading from area 0. [RZ/G1H] 0000: Setting prohibited 0001: 1-cycle pulse 0010: 2-cycle pulse 0011: 3-cycle pulse 0100: 4-cycle pulse : 1110: 14-cycle pulse 1111: 15-cycle pulse
	—	0	R	Reserved [RZ/G1M/N/E] These bits are always read as 0. The write value should always be 0.

Notes: 1. A minimum of two clock cycles are required for one EX-BUS access cycle and therefore, the setting must satisfy this lower limit.  
Setting less than two clock cycles for one access cycle is not expected in the design of this LSI, and if attempted correct operation is not guaranteed.



Example: When CSSetupCycle = B'000, CSHoldCycle = B'000, and PulseCycle = B'00001, correct operation is not guaranteed.

2. When controlling wait insertion through LSI external pins (EX\_WAIT2 to EX\_WAIT0), set PulseCycle to B'00010 or a larger value. If B'00001 or a smaller value is specified, wait insertion through an external pin is disabled.
3. When the burst ROM interface is specified for area 0, the read access-related settings for area 0 in this register is ignored and settings in CS0BTPH are enabled.
4. DMA transfer access is performed according to the settings in the RD/WE pulse control register (EXDMAWCry (y = 0 to 2)) for the respective LBSC-DMAC channel.
5. For details, refer to section 14.6.1, SRAM Interface (Basic Functionality).

### 14.5.5 Area 1 RD/WE Pulse Control Register (CSWCR1)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

**Function:** CSWCR1 specifies the RD/WE# pulse cycles and setup and hold cycles for the CS# signal and address during access to area 1 (EX-BUS).

[RZ/G1H]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	WRITE CS SETUP CYCLE			—	WRITE CS HOLD CYCLE			WRITE CS PULSE CYCLE			
Initial value:	0	0	0	0	0	1	1	1	0	1	1	1	1	1	1	1
R/W:	R	R	R	R	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	READ CS SETUP CYCLE			—	READ CS HOLD CYCLE			READ CS PULSE CYCLE			
Initial value:	0	0	0	0	0	1	1	1	0	1	1	1	1	1	1	1
R/W:	R	R	R	R	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[RZ/G1M/N/E]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	WRITE PULSE CYCLE					WRITE CS SETUP CYCLE			—	WRITE CS HOLD CYCLE			—	—	—	—
Initial value:	1	1	1	1	1	1	1	1	0	1	1	1	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	READ PULSE CYCLE					READ CS SETUP CYCLE			—	READ CS HOLD CYCLE			—	—	—	—
Initial value:	1	1	1	1	1	1	1	1	0	1	1	1	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 27	—	00000	R	Reserved [RZ/G1H] These bits are always read as 0. The write value should always be 0.
	WRITE PULSE CYCLE	11111	R/W	These bits specify the WE pulse cycles during writing to area 0. [RZ/G1M/N/E] 00000: Setting prohibited 00001: 1-cycle pulse 00010: 2-cycle pulse 00011: 3-cycle pulse 00100: 4-cycle pulse : 11101: 29-cycle pulse 11110: 30-cycle pulse 11111: 31-cycle pulse

Bit	Bit Name	Initial Value	R/W	Description
26 to 24	WRITE CS SETUP CYCLE	111	R/W	These bits specify the CS# and address setup cycles with respect to the WE# signal during writing to area 1. 000: 0 cycle for setup period 001: 1 cycle for setup period 010: 2 cycles for setup period : 110: 6 cycles for setup period 111: 7 cycles for setup period
23	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
22 to 20	WRITE CS HOLD CYCLE	111	R/W	These bits specify the CS# and address hold cycles with respect to the WE# signal during writing to area 1. 000: 0 cycle for hold period 001: 1 cycle for hold period 010: 2 cycles for hold period : 110: 6 cycles for hold period 111: 7 cycles for hold period
19 to 16	WRITE PULSE CYCLE	1111	R/W	These bits specify the WE# pulse cycles during writing to area 0. [RZ/G1H] 0000: Setting prohibited 0001: 1-cycle pulse 0010: 2-cycle pulse 0011: 3-cycle pulse 0100: 4-cycle pulse : 1110: 14-cycle pulse 1111: 15-cycle pulse
	—	0000	R	Reserved [RZ/G1M/N/E] These bits are always read as 0. The write value should always be 0.
15 to 11	—	00000	R	Reserved [RZ/G1H] These bits are always read as 0. The write value should always be 0.
	READ PULSE CYCLE	11111	R/W	These bits specify the RD# pulse cycles during reading from area 0. [RZ/G1M/N/E] 00000: Setting prohibited 00001: 1-cycle pulse 00010: 2-cycle pulse 00011: 3-cycle pulse 00100: 4-cycle pulse : 11101: 29-cycle pulse 11110: 30-cycle pulse 11111: 31-cycle pulse

Bit	Bit Name	Initial Value	R/W	Description
10 to 8	READ CS SETUP CYCLE	111	R/W	These bits specify the CS# and address setup cycles with respect to the RD# signal during reading from area 1. 000: 0 cycle for setup period 001: 1 cycle for setup period 010: 2 cycles for setup period : 110: 6 cycles for setup period 111: 7 cycles for setup period
7	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
6 to 4	READ CS HOLD CYCLE	111	R/W	These bits specify the CS# and address hold cycles with respect to the RD# signal during reading from area 1. 000: 0 cycle for hold period 001: 1 cycle for hold period 010: 2 cycles for hold period : 110: 6 cycles for hold period 111: 7 cycles for hold period
3 to 0	READ CS PULSE CYCLE	1111	R/W	These bits specify the RD# pulse cycles during reading from area 0. [RZ/G1H] 0000: Setting prohibited 0001: 1-cycle pulse 0010: 2-cycle pulse 0011: 3-cycle pulse 0100: 4-cycle pulse : 1110: 14-cycle pulse 1111: 15-cycle pulse
	—	0000	R	Reserved [RZ/G1M/N/E] These bits are always read as 0. The write value should always be 0.

- Notes:
1. A minimum of two clock cycles are required for one EX-BUS access cycle and therefore, the setting must satisfy this lower limit.  
Setting less than two clock cycles for one access cycle is not expected in the design of this LSI, and if attempted correct operation is not guaranteed.  
Example: When CSSetupCycle = B'000, CSHoldCycle = B'000, and PulseCycle = B'00001, correct operation is not guaranteed.
  2. When controlling wait insertion through LSI external pins (EX\_WAIT2 to EX\_WAIT0), set PulseCycle to B'00010 or a larger value. If B'00001 or a smaller value is specified, wait insertion through an external pin is disabled.
  3. DMA transfer access to area 1 is performed according to the settings in the RD/WE pulse control register (EXDMAWCry (y = 0 to 2)) for the respective LBSC-DMAC channel.
  4. For details, refer to section 14.6.1, SRAM Interface (Basic Functionality).

**14.5.6 Expansion Area x RD/WE Pulse Control Register (ECSWCRx (x = 0 to 5))**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

**Function:** ECSWCRx specifies the RD/WE# pulse cycles and setup and hold cycles for the CS# signal and address during access to expansion area x (x = 0 to 5) (EX-BUS).

**[RZ/G1H]**

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	WRITE CS SETUP CYCLE			—	WRITE CS HOLD CYCLE			WRITE CS PULSE CYCLE			
Initial value:	0	0	0	0	0	1	1	1	0	1	1	1	1	1	1	1
R/W:	R	R	R	R	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	READ CS SETUP CYCLE			—	READ CS HOLD CYCLE			READ CS PULSE CYCLE			
Initial value:	0	0	0	0	0	1	1	1	0	1	1	1	1	1	1	1
R/W:	R	R	R	R	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**[RZ/G1M/N/E]**

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	WRITE PULSE CYCLE					WRITE CS SETUP CYCLE			—	WRITE CS HOLD CYCLE			—	—	—	—
Initial value:	1	1	1	1	1	1	1	1	0	1	1	1	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	READ PULSE CYCLE					READ CS SETUP CYCLE			—	READ CS HOLD CYCLE			—	—	—	—
Initial value:	1	1	1	1	1	1	1	1	0	1	1	1	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 27	—	00000	R	Reserved [RZ/G1H] These bits are always read as 0. The write value should always be 0.
	WRITE PULSE CYCLE	11111	R/W	These bits specify the WE# pulse cycles during writing to area 0. [RZ/G1M/N/E] 00000: Setting prohibited 00001: 1-cycle pulse 00010: 2-cycle pulse 00011: 3-cycle pulse 00100: 4-cycle pulse : 11101: 29-cycle pulse 11110: 30-cycle pulse 11111: 31-cycle pulse

Bit	Bit Name	Initial Value	R/W	Description
26 to 24	WRITE CS SETUP CYCLE	111	R/W	These bits specify the CS# and address setup cycles with respect to the WE# signal during writing to expansion area x. 000: 0 cycle for setup period 001: 1 cycle for setup period 010: 2 cycles for setup period : 110: 6 cycles for setup period 111: 7 cycles for setup period
23	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
22 to 20	WRITE CS HOLD CYCLE	111	R/W	These bits specify the CS# and address hold cycles with respect to the WE# signal during writing to expansion area x. 000: 0 cycle for hold period 001: 1 cycle for hold period 010: 2 cycles for hold period : 110: 6 cycles for hold period 111: 7 cycles for hold period
19 to 16	WRITE PULSE CYCLE	1111	R/W	These bits specify the WE# pulse cycles during writing to area 0. [RZ/G1H] 0000: Setting prohibited 0001: 1-cycle pulse 0010: 2-cycle pulse 0011: 3-cycle pulse 0100: 4-cycle pulse : 1110: 14-cycle pulse 1111: 15-cycle pulse
	—	0000	R	Reserved [RZ/G1M/N/E] These bits are always read as 0. The write value should always be 0.
15 to 11	—	00000	R	Reserved [RZ/G1H] These bits are always read as 0. The write value should always be 0.
	READ PULSE CYCLE	11111	R/W	These bits specify the RD# pulse cycles during reading from area 0. [RZ/G1M/N/E] 00000: Setting prohibited 00001: 1-cycle pulse 00010: 2-cycle pulse 00011: 3-cycle pulse 00100: 4-cycle pulse : 11101: 29-cycle pulse 11110: 30-cycle pulse 11111: 31-cycle pulse

Bit	Bit Name	Initial Value	R/W	Description
10 to 8	READ CS SETUP CYCLE	111	R/W	These bits specify the CS# and address setup cycles with respect to the RD# signal during reading from expansion area x. 000: 0 cycle for setup period 001: 1 cycle for setup period 010: 2 cycles for setup period : 110: 6 cycles for setup period 111: 7 cycles for setup period
7	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
6 to 4	READ CS HOLD CYCLE	111	R/W	These bits specify the CS# and address hold cycles with respect to the RD# signal during reading from expansion area x. 000: 0 cycle for hold period 001: 1 cycle for hold period 010: 2 cycles for hold period : 110: 6 cycles for hold period 111: 7 cycles for hold period
3 to 0	READ CS PULSE CYCLE	1111	R/W	These bits specify the RD# pulse cycles during reading from area 0. [RZ/G1H] 0000: Setting prohibited 0001: 1-cycle pulse 0010: 2-cycle pulse 0011: 3-cycle pulse 0100: 4-cycle pulse : 1110: 14-cycle pulse 1111: 15-cycle pulse
		0000	R	Reserved [RZ/G1M/N/E] These bits are always read as 0. The write value should always be 0.

- Notes:
1. A minimum of two clock cycles are required for one EX-BUS access cycle and therefore, the setting must satisfy this lower limit.  
Setting less than two clock cycles for one access cycle is not expected in the design of this LSI, and if attempted correct operation is not guaranteed.  
Example: When CSSetupCycle = B'000, CSHoldCycle = B'000, and PulseCycle = B'00001, correct operation is not guaranteed.
  2. When controlling wait insertion through LSI external pins (EX\_WAIT2 to EX\_WAIT0), set PulseCycle to B'00010 or a larger value. If B'00001 or a smaller value is specified, wait insertion through an external pin is disabled.
  3. DMA transfer access to expansion area x is performed according to the settings in the RD/WE pulse control register (EXDMAWCRy (y = 0 to 2)) for the respective LBSC-DMAC channel.
  4. For details, refer to section 14.6.1, SRAM Interface (Basic Functionality).

**14.5.7 LBSC-DMAC Channel y RD/WE Pulse Control Register (EXDMAWCry (y = 0 to 2))**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

**Function:** EXDMAWCry specifies the RD/WE# pulse cycles and setup and hold cycles for the CS# signal and address during access to EX-BUS in LBSC-DMAC channel y (y = 0 to 5).

[RZ/G1H]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	WRITE CS SETUP CYCLE			—	WRITE CS HOLD CYCLE			WRITE CS PULSE CYCLE			
Initial value:	0	0	0	0	0	1	1	1	0	1	1	1	1	1	1	1
R/W:	R	R	R	R	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	READ CS SETUP CYCLE			—	READ CS HOLD CYCLE			READ CS PULSE CYCLE			
Initial value:	0	0	0	0	0	1	1	1	0	1	1	1	1	1	1	1
R/W:	R	R	R	R	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[RZ/G1M/N/E]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	WRITE PULSE CYCLE					WRITE CS SETUP CYCLE			—	WRITE CS HOLD CYCLE			—	—	—	—
Initial value:	1	1	1	1	1	1	1	1	0	1	1	1	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	READ PULSE CYCLE					READ CS SETUP CYCLE			—	READ CS HOLD CYCLE			—	—	—	—
Initial value:	1	1	1	1	1	1	1	1	0	1	1	1	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 27	—	00000	R	Reserved [RZ/G1H] These bits are always read as 0. The write value should always be 0.
	WRITE PULSE CYCLE	11111	R/W	These bits specify the WE# pulse cycles during writing to area 0. [RZ/G1M/N/E] 00000: Setting prohibited 00001: 1-cycle pulse 00010: 2-cycle pulse 00011: 3-cycle pulse 00100: 4-cycle pulse : 11101: 29-cycle pulse 11110: 30-cycle pulse 11111: 31-cycle pulse



Bit	Bit Name	Initial Value	R/W	Description
26 to 24	WRITE CS SETUP CYCLE	111	R/W	These bits specify the CS# and address setup cycles with respect to the WE# signal during write in channel y. 000: 0 cycle for setup period 001: 1 cycle for setup period 010: 2 cycles for setup period : 110: 6 cycles for setup period 111: 7 cycles for setup period
23	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
22 to 20	WRITE CS HOLD CYCLE	111	R/W	These bits specify the CS# and address hold cycles with respect to the WE# signal during write in channel y. 000: 0 cycle for hold period 001: 1 cycle for hold period 010: 2 cycles for hold period : 110: 6 cycles for hold period 111: 7 cycles for hold period
19 to 16	WRITE PULSE CYCLE	1111	R/W	These bits specify the WE# pulse cycles during writing to area 0. [RZ/G1H] 0000: Setting prohibited 0001: 1-cycle pulse 0010: 2-cycle pulse 0011: 3-cycle pulse 0100: 4-cycle pulse : 1110: 14-cycle pulse 1111: 15-cycle pulse
	—	0000	R	Reserved [RZ/G1M/N/E] These bits are always read as 0. The write value should always be 0.
15 to 11	—	00000	R	Reserved [RZ/G1H] These bits are always read as 0. The write value should always be 0.
	READ PULSE CYCLE	11111	R/W	These bits specify the RD# pulse cycles during reading from area 0. [RZ/G1M/N/E] 00000: Setting prohibited 00001: 1-cycle pulse 00010: 2-cycle pulse 00011: 3-cycle pulse 00100: 4-cycle pulse : 11101: 29-cycle pulse 11110: 30-cycle pulse 11111: 31-cycle pulse

Bit	Bit Name	Initial Value	R/W	Description
10 to 8	READ CS SETUP CYCLE	111	R/W	These bits specify the CS# and address setup cycles with respect to the RD# signal during read in channel y. 000: 0 cycle for setup period 001: 1 cycle for setup period 010: 2 cycles for setup period : 110: 6 cycles for setup period 111: 7 cycles for setup period
7	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
6 to 4	READ CS HOLD CYCLE	111	R/W	These bits specify the CS# and address hold cycles with respect to the RD# signal during read in channel y. 000: 0 cycle for hold period 001: 1 cycle for hold period 010: 2 cycles for hold period : 110: 6 cycles for hold period 111: 7 cycles for hold period
3 to 0	READ CS PULSE CYCLE	1111	R/W	These bits specify the RD# pulse cycles during reading from area 0. [RZ/G1H] 0000: Setting prohibited 0001: 1-cycle pulse 0010: 2-cycle pulse 0011: 3-cycle pulse 0100: 4-cycle pulse : 1110: 14-cycle pulse 1111: 15-cycle pulse
	—	0000	R	Reserved [RZ/G1M/N/E] These bits are always read as 0. The write value should always be 0.

- Notes:
1. A minimum of two clock cycles are required for one EX-BUS access cycle and therefore, the setting must satisfy this lower limit.  
Setting less than two clock cycles for one access cycle is not expected in the design of this LSI, and if attempted correct operation is not guaranteed.  
Example: When CSSetupCycle = B'000, CSHoldCycle = B'000, and PulseCycle = B'00001, correct operation is not guaranteed.
  2. When controlling wait insertion through LSI external pins (EX\_WAIT2 to EX\_WAIT0), set PulseCycle to B'00010 or a larger value. If B'00001 or a smaller value is specified, wait insertion through an external pin is disabled.
  3. External wait insertion is controlled according to the external wait control register for the area where the DMAC channel (0 to 2) is assigned.
  4. For details, refer to section 14.6.3, LBSC-DMAC → DMA Interface.

**14.5.8 Area 0 External Wait Control Register (CSPWCR0)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

**Function:** CSPWCR0 makes settings for external wait signal during access to area 0 (EX-BUS) (the settings are ignored when the burst ROM interface is selected).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	V	RB	WINV	EXWT2	EXWT1	EXWT0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5	V	0	R/W	Area 0 External Wait Signal Enable/Disable 0: Disabled 1: Enabled
4	RB	0	R/W	Area 0 READY/BUSY Logic Selection 0: BUSY logic 1: READY logic
3	WINV	0	R/W	Area 0 External Wait Signal Polarity 0: Does not invert the polarity of the area 0 external wait signal. 1: Inverts the polarity of the area 0 external wait signal.

Bit	Bit Name	Initial Value	R/W	Description
2	EXWT2	0	R/W	Area 0 EX_WAIT2 Enable 0: Disables EX_WAIT2 for area 0. 1: Enables EX_WAIT2 for area 0.
1	EXWT1	0	R/W	Area 0 EX_WAIT1 Enable 0: Disables EX_WAIT1 for area 0. 1: Enables EX_WAIT1 for area 0.
0	EXWT0	0	R/W	Area 0 EX_WAIT0 Enable 0: Disables EX_WAIT0 for area 0. 1: Enables EX_WAIT0 for area 0.

- Notes:
1. When this register setting is made valid (bit V = 1), any one of bits EXWT0 to EXWT2 must be set to 1. Simultaneously setting more than one of EXWT0 to EXWT2 to 1 is not expected in the design of this LSI, and attempted correct operation is not guaranteed.
  2. When bit V = 0, the settings in EXWT0 to EXWT2 are ignored. In area 0, this register setting is ignored in read access when the burst ROM interface is selected. For details on wait control, refer to section 14.6.1, SRAM Interface (Basic Functionality).

**14.5.9 Area 1 External Wait Control Register (CSPWCR1)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

**Function:** CSPWCR1 makes settings for external wait input pins during access to area 1 (EX-BUS).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	V	RB	WINV	EXWT2	EXWT1	EXWT0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5	V	0	R/W	Area 1 External Wait Signal Enable/Disable 0: Disabled 1: Enabled
4	RB	0	R/W	Area 1 READY/BUSY Logic Selection 0: BUSY logic 1: READY logic
3	WINV	0	R/W	Area 1 External Wait Signal Polarity 0: Does not invert the polarity of the area 1 external wait signal. 1: Inverts the polarity of the area 1 external wait signal.

Bit	Bit Name	Initial Value	R/W	Description
2	EXWT2	0	R/W	Area 1 EX_WAIT2 Enable 0: Disables EX_WAIT2 for area 1. 1: Enables EX_WAIT2 for area 1.
1	EXWT1	0	R/W	Area 1 EX_WAIT1 Enable 0: Disables EX_WAIT1 for area 1. 1: Enables EX_WAIT1 for area 1.
0	EXWT0	0	R/W	Area 1 EX_WAIT0 Enable 0: Disables EX_WAIT0 for area 1. 1: Enables EX_WAIT0 for area 1.

- Notes:
1. When this register setting is made valid (bit V = 1), any one of bits EXWT0 to EXWT2 must be set to 1. Simultaneously setting more than one of EXWT0 to EXWT2 to 1 is not expected in the design of this LSI, and attempted correct operation is not guaranteed.
  2. When bit V = 0, the settings in EXWT0 to EXWT2 are ignored. For details on wait control, refer to section 14.6.1, SRAM Interface (Basic Functionality).

### 14.5.10 Expansion Area x External Wait Control Register (ECSPWCRx (x = 0 to 5))

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

**Function:** ECSPWCRx makes settings for external wait input pins during access to expansion area x (x = 0 to 5) (EX-BUS).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	V	RB	WINV	EXWT2	EXWT1	EXWT0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5	V	0	R/W	Expansion Area x External Wait Signal Enable/Disable 0: Disabled 1: Enabled
4	RB	0	R/W	Expansion Area x READY/BUSY Logic Selection 0: BUSY logic 1: READY logic
3	WINV	0	R/W	Expansion Area x External Wait Signal Polarity 0: Does not invert the polarity of the expansion area x external wait signal. 1: Inverts the polarity of the expansion area x external wait signal.

Bit	Bit Name	Initial Value	R/W	Description
2	EXWT2	0	R/W	Expansion Area x EX_WAIT2 Enable 0: Disables EX_WAIT2 for expansion area x. 1: Enables EX_WAIT2 for expansion area x.
1	EXWT1	0	R/W	Expansion Area x EX_WAIT1 Enable 0: Disables EX_WAIT1 for expansion area x. 1: Enables EX_WAIT1 for expansion area x.
0	EXWT0	0	R/W	Expansion Area x EX_WAIT0 Enable 0: Disables EX_WAIT0 for expansion area x. 1: Enables EX_WAIT0 for expansion area x.

- Notes:
1. When this register setting is made valid (bit V = 1), any one of bits EXWT0 to EXWT2 must be set to 1. Simultaneously setting more than one of EXWT0 to EXWT2 to 1 is not expected in the design of this LSI, and attempted correct operation is not guaranteed.
  2. When bit V = 0, the settings in EXWT0 to EXWT2 are ignored. For details on wait control, refer to section 14.6.1, SRAM Interface (Basic Functionality).



**14.5.11 External Wait Input Control Register (EXWTSYNC)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

**Function:** EXWTSYNC controls whether or not to synchronize the external wait pins (EX\_WAIT2 to EXWAIT0).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	EXWT SYNC2	EXWT SYNC1	EXWT SYNC0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	—	0	R/W	Reserved The write value should always be 0.
3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
2	EXWTSYNC2	0	R/W	0: Does not synchronize EX_WAIT2 (the original EX_WAIT2 is synchronous with CLKOUT). 1: Synchronizes EX_WAIT2 (the original EX_WAIT2 is asynchronous with CLKOUT).
1	EXWTSYNC1	0	R/W	0: Does not synchronize EX_WAIT1 (the original EX_WAIT1 is synchronous with CLKOUT). 1: Synchronizes EX_WAIT1 (the original EX_WAIT1 is asynchronous with CLKOUT).
0	EXWTSYNC0	0	R/W	0: Does not synchronize EX_WAIT0 (the original EX_WAIT0 is synchronous with CLKOUT). 1: Synchronizes EX_WAIT0 (the original EX_WAIT0 is asynchronous with CLKOUT).

**Note:** For details on wait control, refer to section 14.6.1, SRAM Interface (Basic Functionality).

### 14.5.12 Area 0 Burst Control Register (CS0BSTCTL)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

**Function:** CS0BSTCTL specifies the burst length for area 0 when the burst ROM interface is selected.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	A0BST[2:0]			—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13 to 11	A0BST[2:0]	000	R/W	Area 0 Burst Length for Burst ROM Interface 001: 4 access cycles 010: 8 access cycles 011: 16 access cycles 100: 32 access cycles Others: No burst transfer
10 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

- Notes:
1. This register is valid only when the burst ROM interface is selected (CS0IF = B'01 in CS0CTRL).
  2. Set bits A0BST2 to A0BST0 to an appropriate value so that (area 0 bus size) x (burst length set in this register) becomes 32 bytes or less.
  3. For details, refer to section 14.6.2, CPU (AXI Bus) → Burst ROM Interface.

**14.5.13 Area 0 Burst Pitch Set Register (CS0BTPH)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

**Function:** CS0BTPH specifies the burst pitches for the first access cycle and the second and later cycles for area 0 when the burst ROM interface is selected.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	A0H	A0W[3:0]			—	A0B[2:0]			
Initial value:	0	0	0	0	0	0	0	0	1	1	1	1	0	1	1	1
R/W:	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	A0H	0	R/W	Specifies the CS# and address hold cycles with respect to the RD# signal for area 0 in the burst ROM interface. 0: 0 cycle for hold period 1: 1 cycle for hold period
7 to 4	A0W[3:0]	1111	R/W	These bits specify the burst pitch (wait cycles to be inserted) after the first burst cycle for area 0 in the burst ROM interface. 0000: Setting prohibited 0001: Setting prohibited 0010: 2 cycles 0011: 3 cycles 0100: 4 cycles : 1101: 13 cycles 1110: 14 cycles 1111: 15 cycles
3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
2 to 0	A0B[2:0]	111	R/W	These bits specify the burst pitch (wait cycles to be inserted) after the second burst cycle for area 0 in the burst ROM interface. 000: Setting prohibited 001: 1 cycle 010: 2 cycles : 110: 6 cycles 111: 7 cycles

- Notes: 1. Be sure to specify this register before specifying CS0BSTCTL.  
2. For details, refer to section 14.6.2, CPU (AXI Bus) → Burst ROM Interface.

#### 14.5.14 Area 1 Guard Setting Register (CS1GDST)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

**Function:** CS1GDST specifies the guard interval (period of access prohibition) between sequential access cycles in area 1.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	CS1GD	TIMER_SET			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	CS1GD	0	R/W	0: Makes the TIMER_SET setting invalid. 1: Makes the TIMER_SET setting valid.
3 to 0	TIMER_SET	0000	R/W	Guard Interval (Period of Access Prohibition) between Sequential Access Cycles for Area 1 0000: 0 clock cycle 0001: 1 clock cycle 0010: 2 clock cycles 0011: 3 clock cycles 0100: 4 clock cycles : 1101: 13 clock cycles 1110: 14 clock cycles 1111: 15 clock cycles

- Notes: 1. The TIMER\_SET setting is ignored when CS1GD = 0.  
2. This register must not be dynamically modified regardless of whether area 1 is being accessed.  
3. The actual guard interval between sequential access cycles on the EX-BUS is (register setting) + (idle cycles due to hardware processing and EX-BUS arbitration).  
4. For details, refer to section 14.6.1 (4), Controlling Guard Intervals

**14.5.15 Expansion Area x Guard Setting Register (ECSxGDST (x = 0 to 5))**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

**Function:** ECSxGDST specifies the guard interval (period of access prohibition) between sequential access cycles in expansion area x (x = 0 to 5) (valid for both SRAM and MPX buses).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	ECSxGD	TIMER_SET			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	ECSxGD	0	R/W	0: Makes the TIMER_SET setting invalid. 1: Makes the TIMER_SET setting valid.
3 to 0	TIMER_SET	0000	R/W	Guard Interval (Period of Access Prohibition) between Sequential Access Cycles for Expansion Area x 0000: 0 clock cycle 0001: 1 clock cycle 0010: 2 clock cycles 0011: 3 clock cycles : 1101: 13 clock cycles 1110: 14 clock cycles 1111: 15 clock cycles

- Notes:
1. The TIMER\_SET setting is ignored when ECSxGD = 0.
  2. This register must not be dynamically modified regardless of whether the expansion area is being accessed.
  3. The actual guard interval between sequential access cycles on the EX-BUS is (register setting) + (idle cycles due to hardware processing and EX-BUS arbitration).
  4. For details, refer to section 14.6.1 (4), Controlling Guard Intervals.

### 14.5.16 LBSC-DMAC Channel y Area Assignment Register (EXDMASETy (y = 0 to 2))

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

**Function:** EXDMASETy specifies the area where LBSC-DMAC channel y is assigned (y = 0 to 2).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	DMyECS5	DMyECS4	DMyECS3	DMyECS2	DMyECS1	DMyECS0	DMyCS1	DMyCS0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7	DMyECS5	0	R/W	0: Does not assign LBSC-DMAC channel y to expansion area 5. 1: Assigns LBSC-DMAC channel y to expansion area 5.
6	DMyECS4	0	R/W	0: Does not assign LBSC-DMAC channel y to expansion area 4. 1: Assigns LBSC-DMAC channel y to expansion area 4.
5	DMyECS3	0	R/W	0: Does not assign LBSC-DMAC channel y to expansion area 3. 1: Assigns LBSC-DMAC channel y to expansion area 3.
4	DMyECS2	0	R/W	0: Does not assign LBSC-DMAC channel y to expansion area 2. 1: Assigns LBSC-DMAC channel y to expansion area 2.
3	DMyECS1	0	R/W	0: Does not assign LBSC-DMAC channel y to expansion area 1. 1: Assigns LBSC-DMAC channel y to expansion area 1.
2	DMyECS0	0	R/W	0: Does not assign LBSC-DMAC channel y to expansion area 0. 1: Assigns LBSC-DMAC channel y to expansion area 0.
1	DMyCS1	0	R/W	0: Does not assign LBSC-DMAC channel y to area 1. 1: Assigns LBSC-DMAC channel y to area 1.
0	DMyCS0	0	R/W	0: Does not assign LBSC-DMAC channel y to area 0. 1: Assigns LBSC-DMAC channel y to area 0.

- Notes:
- Setting more than one bit to 1 in this register is prohibited. Such a setting is not expected in the design of this LSI, and if attempted correct operation is not guaranteed.
  - For an expansion area whose capacity is 0 Mbytes, DMAC channel must not be assigned.
  - Be sure to specify this register before starting LBSC-DMAC access. If an LBSC-DMAC channel starts access before specifying this register, correct operation is not guaranteed (such access is not expected in the design of this LSI).
  - When CS0 area is used as a 128-Mbyte space, DMAC channel must not be assigned to CS1 area.
  - For details, refer to section 14.6.3, LBSC-DMAC → DMA Interface.

### 14.5.17 LBSC-DMAC Channel y Control Register (EXDMCRy (y = 0 to 2))

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

**Function:** EXDMCRy specifies conversion of DREQ[y], DACK[y], and DRACK[0] in the area where LBSC-DMAC channel y is assigned.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DRST	—	DSTS	DBST	—	EXQL	EXDY	EXDS	—	—	EXRS	EXRL	—	EXAL	DAKCTL	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	W	R	R	R/W	R	R/W	R/W	R/W	R	R	R/W	R/W	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15	DRST	0	W	DACK Signal Forcible Negation (Enabled when DBST = 1) 0: Writing 0 is ignored. 1: Forcibly negates the DACK signal being continuously asserted for 1 CLKOUT cycle.
14	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
13	DSTS	0	R	DACK Signal Assert State Indication 0: The DACK signal is not currently asserted. 1: The DACK signal is currently asserted.
12	DBST	0	R/W	Specifies whether or not to continuously assert the DACK signal if DREQ is continuously asserted during the intervals between DMA bus transfers (in ATA mode only). 0: Negates DACK after each bus transfer. 1: Continuously asserts DACK even during the intervals between bus transfers if DREQ is continuously asserted. (When negation of DREQ is detected, DACK is also negated.)
11	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
10	EXQL	0	R/W	0: Receives DREQ[y] signal at a low level. 1: Receives DREQ[y] signal at a high level.
9	EXDY	0	R/W	0: Does not synchronize the DREQ[y] signal. 1: Synchronizes the DREQ[y] signal.
8	EXDS	0	R/W	0: Detects DREQ[y] signal at a level. 1: Detects DREQ[y] signal at an edge.
7, 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
5	EXRS	0	R/W	0: Asserts DRACK[0] one clock cycle before CS#/DACK[0] is asserted. 1: Asserts DRACK[0] two clock cycles before CS#/DACK[0] is asserted.
4	EXRL	0	R/W	0: Outputs DRACK[0] as a high-active signal. 1: Outputs DRACK[0] as a low-active signal.
3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
2	EXAL	0	R/W	0: Outputs DACK[y] as a high-active signal. 1: Outputs DACK[y] as a low-active signal.
1, 0	DAKCTL	00	R/W	Signals asserted for area where LBSC-DMAC channel y is assigned 00 and 11: Asserts the CS# signal and DACK[y] signal together for the area. 01: Asserts only the CS# signal for the area. 10: Asserts only the DACK[y] signal for the area.

- Notes:
1. This register except for DRST bit must not be dynamically modified regardless of whether the respective area is being accessed.
  2. The EXRL and EXRS settings are valid only for LBSC-DMAC channel 0 (DRACK[0]). LBSC-DMAC channels 1 and 2 do not have the DRACK signal.
  3. For details on the DMA interface, refer to section 14.6.3, LBSC-DMAC → DMA Interface.



**14.5.18 BSC Interrupt Source Status Register (BCINTSR)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

**Function:** BCINTSR indicates the status of the BSC interrupt source.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	EXWTE	ATTE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	EXWTE	0	R	EX-BUS Wait Timeout Error Status 0: The EX-BUS is working correctly. 1: An EX-BUS timeout error has occurred. (A timeout error occurs when an EX-BUS clock (CLKOUT) cycle of EXBCT and EXTCT setting values have elapsed.)
0	ATTE	0	R	ATA Wait Timeout Error Status 0: The ATA interface is working correctly. 1: A timeout error has occurred in the ATA interface. (A timeout error occurs when 100 EX-BUS clock (CLKOUT) cycles of wait time have elapsed.)

- Notes:
1. No interrupt signal is output with only the ATTE bit being set to 1 in this register. To output an interrupt signal, BCINTMR must be appropriately specified.
  2. For details on the ATA interface, refer to section 14.6.5, CPU (AXI Bus) → ATA Device Interface.

**14.5.19 BSC Interrupt Source Clear Register (BCINTCR)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: BCINTCR clears the state of the BSC interrupt indicator.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	EXWTE C	ATTEC
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	-/WC1	-/WC1

Bit	Bit Name	Initial Value	R/W	Description
31 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	EXWTEC	0	-/WC1	EX-BUS Wait Timeout Error Status Clear 0: Writing 0 is ignored. 1: Clears the EX-BUS wait timeout error state.
0	ATTEC	0	-/WC1	ATA Wait Timeout Error Status Clear 0: Writing 0 is ignored. 1: Clears the ATA wait timeout error state.

- Notes: 1. This register is always read as 0.  
2. For details on the ATA interface, refer to section 14.6.5, CPU (AXI Bus) → ATA Device Interface.

**14.5.20 BSC Interrupt Enable Register (BCINTMR)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: BCINTMR enables or disables the BSC interrupt.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	EXWTE M	ATTEM
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	EXWTEM	0	R/W	EX-BUS Wait Timeout Error Interrupt Enable 0: Disables output of an interrupt signal for this interrupt source. 1: Enables output of an interrupt signal for this interrupt source.
0	ATTEM	0	R/W	ATA Wait Timeout Error Interrupt Enable 0: Disables output of an interrupt signal for this interrupt source. 1: Enables output of an interrupt signal for this interrupt source.

**14.5.21 EX-BUS Priority Level Set Register (EXBATLV)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

**Function:** Specifies the priority levels for EX-BUS arbitration.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	EX-BLV
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	EX-BLV	0	R/W	Priority Level Setting for EX-BUS Arbitration (Access Selection) 0: Higher priority: PIO (AXI access) Lower priority: LBSC-DMAC 1: Higher priority: LBSC-DMAC Lower priority: PIO (AXI access)

- Notes:
- EX-BLV sets a fixed priority between PIO and LBSC-DMAC.
  - This register must not be dynamically modified except for initial setting.
  - For details on external bus arbitration, refer to section 14.6.7, EX-BUS Arbitration.

**14.5.22 External Wait Status Register (EXWTSTS)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: EXWTSTS indicates the state of the external wait pins EX\_WAITn.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	EXWT2 STS	EXWT1 STS	EXWT0 STS
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2	EXWT2STS	—	R	Indicates the EX_WAIT2 pin state.
1	EXWT1STS	—	R	Indicates the EX_WAIT1 pin state.
0	EXWT0STS	—	R	Indicates the EX_WAIT0 pin state.

### 14.5.23 ATACS Control Register (ATACCTRL)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

**Function:** ATACCTRL specifies the ATA port 0 (pins ATACS00# and ATACS10#) and ATA port 1 (pins ATACS01# and ATACS11#) signal settings.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	ATAECS 5_EN	ATAECS 4_EN	ATAECS 3_EN	ATAECS 2_EN	ATAECS 1_EN	ATAECS 0_EN	ATACS1 _EN
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 7	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
6	ATAECS5_EN	0	R/W	Setting of the ATACS signal when expansion area 5 is accessed in ATA mode 0: The ATACS0 signal (pins ATACS00# and ATACS10#) is asserted. 1: The ATACS1 signal (pins ATACS01# and ATACS11#) is asserted.
5	ATAECS4_EN	0	R/W	Setting of the ATACS signal when expansion area 4 is accessed in ATA mode 0: The ATACS0 signal (pins ATACS00# and ATACS10#) is asserted. 1: The ATACS1 signal (pins ATACS01# and ATACS11#) is asserted.
4	ATAECS3_EN	0	R/W	Setting of the ATACS signal when expansion area 3 is accessed in ATA mode 0: The ATACS0 signal (pins ATACS00# and ATACS10#) is asserted. 1: The ATACS1 signal (pins ATACS01# and ATACS11#) is asserted.
3	ATAECS2_EN	0	R/W	Setting of the ATACS signal when expansion area 2 is accessed in ATA mode 0: The ATACS0 signal (pins ATACS00# and ATACS10#) is asserted. 1: The ATACS1 signal (pins ATACS01# and ATACS11#) is asserted.

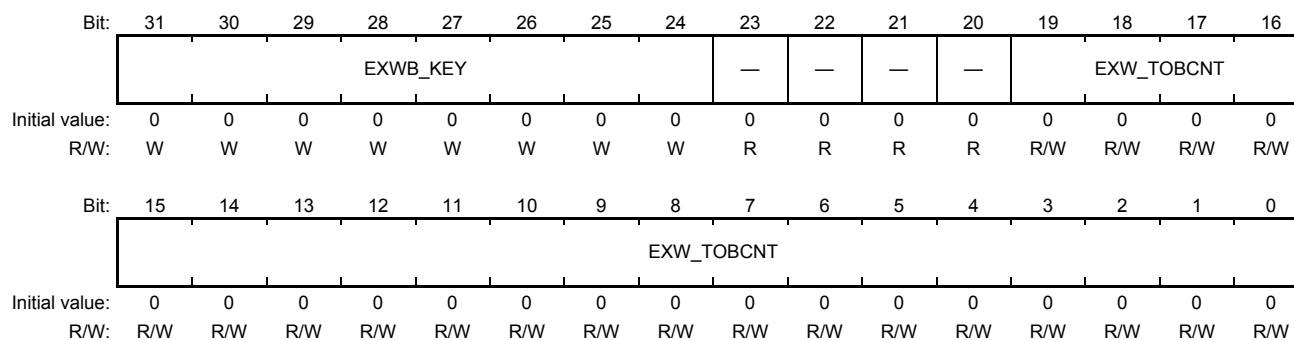
Bit	Bit Name	Initial Value	R/W	Description
2	ATAECS1_EN	0	R/W	Setting of the ATACS signal when expansion area 1 is accessed in ATA mode 0: The ATACS0 signal (pins (pins ATACS00# and ATACS10#) is asserted. 1: The ATACS1 signal (pins ATACS01# and ATACS11#) is asserted.
1	ATAECS0_EN	0	R/W	Setting of the ATACS signal when expansion area 0 is accessed in ATA mode 0: The ATACS0 signal (pins (pins ATACS00# and ATACS10#) is asserted. 1: The ATACS1 signal (pins ATACS01# and ATACS11#) is asserted.
0	ATACS1_EN	0	R/W	Setting of the ATACS signal when area 1 is accessed in ATA mode 0: The ATACS0 signal (pins (pins ATACS00# and ATACS10#) is asserted. 1: The ATACS1 signal (pins ATACS01# and ATACS11#) is asserted.

Note: If the ATA mode is selected with the CS1IF bit of the CS1CTRL register and the ECSxIF bit of the ECSxCTRL register, and the ATACS1\_EN and ATAECsx\_EN bits of this register are set to 1, ATACS00#, ATACS10#, ATACS01#, or ATACS11# is asserted in accord with the value being output as address bit 4 on the external bus. For details, refer to section 14.6.5, CPU (AXI Bus) → ATA Device Interface.

**14.5.24 EX-BUS Wait Timeout Detection Base Counter Register (EXBCT)**

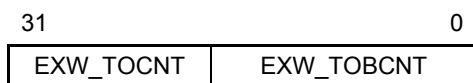
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

**Function:** EXBCT specifies the lower-order part of the value for counting to detect a timeout in waiting for access to the EX-BUS, which is monitored through pins EX\_WAIT0, EX\_WAIT1, and EX\_WAIT2.



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	EXWB_KEY	H'00	W	EX-BUS Wait Timeout Detection Base Counter Register Write Key  For writing to this register to be effective, the value H'5A must be written to these bits. Values read from these bits are meaningless.
23 to 20	—	All 0	R	Reserved  These bits are always read as 0. The write value should always be 0.
19 to 0	EXW_TOBCNT	H'0 0000	R/W	EX-BUS Wait Timeout Counter Setting  Maximum value: H'0 0000 Minimum value: H'0 0001

**Note:** Counting to detect a timeout in waiting for access to the EX-BUS is handled by a 32-bit counter, which is formed by the EXW\_TOBCNT bits in the EXBCT register and the EXW\_TOCNT bits in the EXTCT register as shown below.

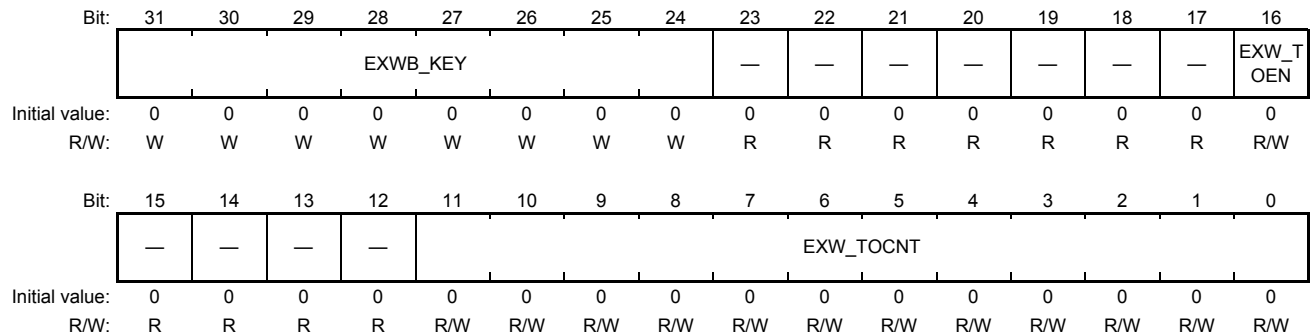




**14.5.25 EX-BUS Wait Timeout Detection Counter Register (EXTCT)**

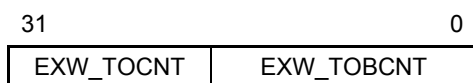
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

**Function:** EXTCT specifies the higher-order part of the value for counting to detect a timeout in waiting for access to the EX-BUS, which is monitored through pins EX\_WAIT0, EX\_WAIT1, and EX\_WAIT2, and enables or disables the detection.



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	EXWB_KEY	H'00	W	EX-BUS Wait Timeout Detection Counter Register Write Key For writing to this register to be effective, the value H'5A must be written to these bits. Values read from these bits are meaningless.
23 to 17	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
16	EXW_TOEN	0	R/W	EX-BUS Wait Timeout Enable 0: Timeout in waiting for access to the EX-BUS has not been detected. 1: Timeout in waiting for access to the EX-BUS has been detected.
15 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11 to 0	EXW_TOCNT	H'000	R/W	EX-BUS Wait Timeout Counter Setting Maximum value: H'000 Minimum value: H'001

**Note:** Counting to detect a timeout in waiting for access to the EX-BUS is handled by a 32-bit counter, which is formed by the EXW\_TOBCNT bits in the EXBCT register and the EXW\_TOCNT bits in the EXTCT register as shown below.



**14.5.26 EX-BUS Wait Timeout Detection Access Source Indication Register (EXTSR)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

**Function:** EXTSR indicates the source of attempted access to the EX-BUS that reached timeout as detected through the EX\_WAIT0, EX\_WAIT1, and EX\_WAIT2 pins.

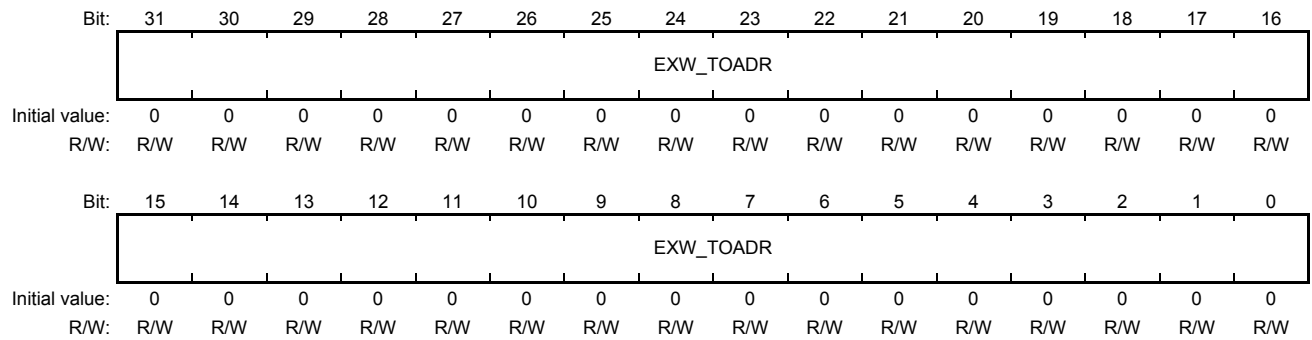
Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	EXW_T OSHW
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/WC1
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	EXW_T ODC2	EXW_T ODC1	EXW_T ODC0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R/WC1	R/WC1	R/WC1

Bit	Bit Name	Initial Value	R/W	Description
31 to 17	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
16	EXW_TOSHW	0	R/WC1	Indication of timeout in waiting for access to the EX-BUS from the AXI bus. 0: Timeout has not been reached. 1: Timeout has been reached. To clear this bit, write 1 to it.
15 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2	EXW_TODC2	0	R/WC1	Indication of timeout in waiting for access to the EX-BUS by channel 2 of the LBSC-DMAC. 0: Timeout has not been reached. 1: Timeout has been reached. To clear this bit, write 1 to it.
1	EXW_TODC1	0	R/WC1	Indication of timeout in waiting for access to the EX-BUS by channel 1 of the LBSC-DMAC. 0: Timeout has not been reached. 1: Timeout has been reached. To clear this bit, write 1 to it.
0	EXW_TODC0	0	R/WC1	Indication of timeout in waiting for access to the EX-BUS by channel 0 of the LBSC-DMAC. 0: Timeout has not been reached. 1: Timeout has been reached. To clear this bit, write 1 to it.

**14.5.27 EX-BUS Wait Timeout Detection Address Indication Register (EXTADR)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

**Function:** EXTADR indicates the address at which access to the EX-BUS was attempted but timeout was detected through pins EX\_WAIT0, EX\_WAIT1, and EX\_WAIT2.



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	EXW_ TOADR	H'0000 0000	R/W	Indication of the address for which attempted access to the EX-BUS by the AXI bus reached timeout

- Notes:
1. This register is readable and writable. To clear this register, write 0s to all bits.
  2. This register only indicates the address to which access was attempted if this was from the AXI bus (i.e. addresses are not indicated if access was attempted from the LBSC-DMAC).

## 14.6 Operation

RZ/G1H	RZ/G1N
RZ/G1M	RZ/G1E

### 14.6.1 SRAM Interface (Basic Functionality)

The BSC reads access requests from the CPU stored in the FIFO mounted in the LBSC module and writes them to the EX-BUS. By default, all spaces, areas 0 and 1, and expansion areas 0 to 5 are all set for SRAM interface. The pulse width for access signals in this SRAM access interface can be varied according to register settings. Thus, the SRAM interface has functionality for easily accommodating devices with various access specifications, connected on the EX-BUS. In addition, to support low-speed external devices, the guard-interval control functionality is provided for insertion of the appropriate interval for each bus access; and the SRAM interface receives wait-for-response requests (or access complete signals) from external devices on a synchronous/asynchronous-selectable and polarity-selectable basis, thus ensuring flexibility in bus design. Figures 14.3 and 14.4 show SRAM interface timing charts for AXI → EX-BUS conversions.

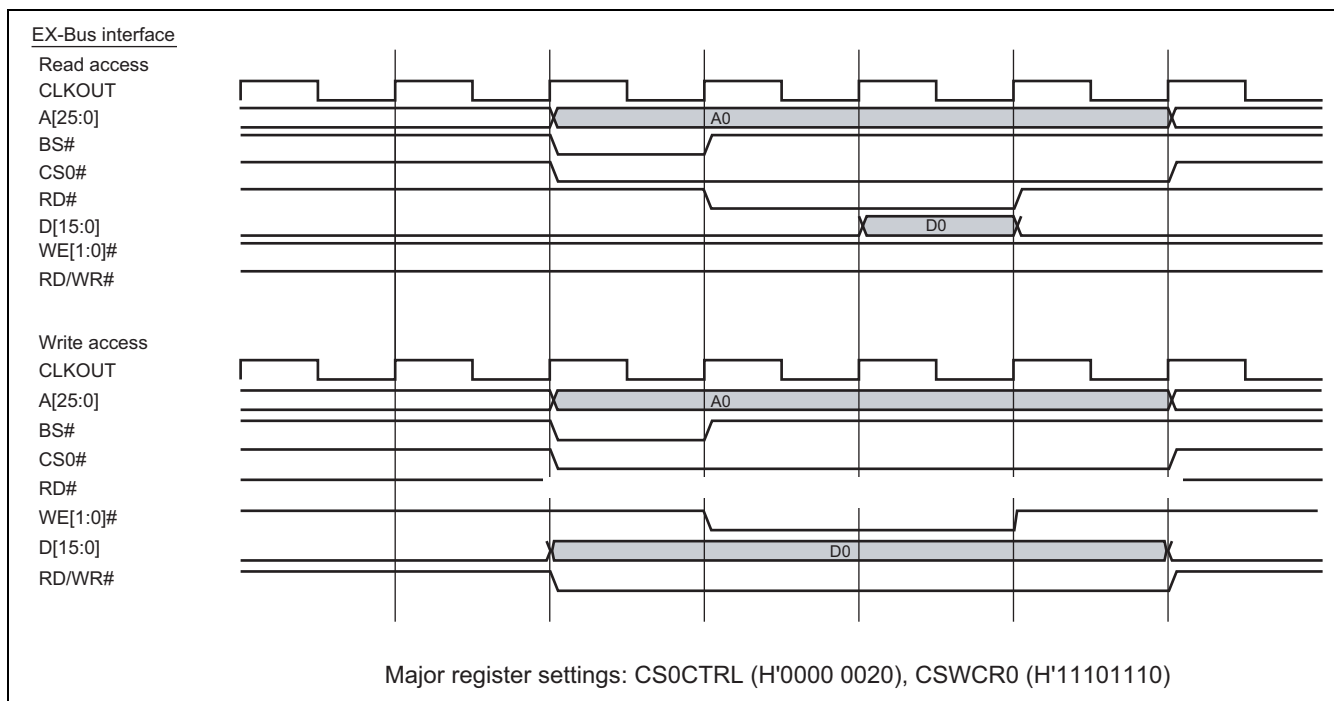
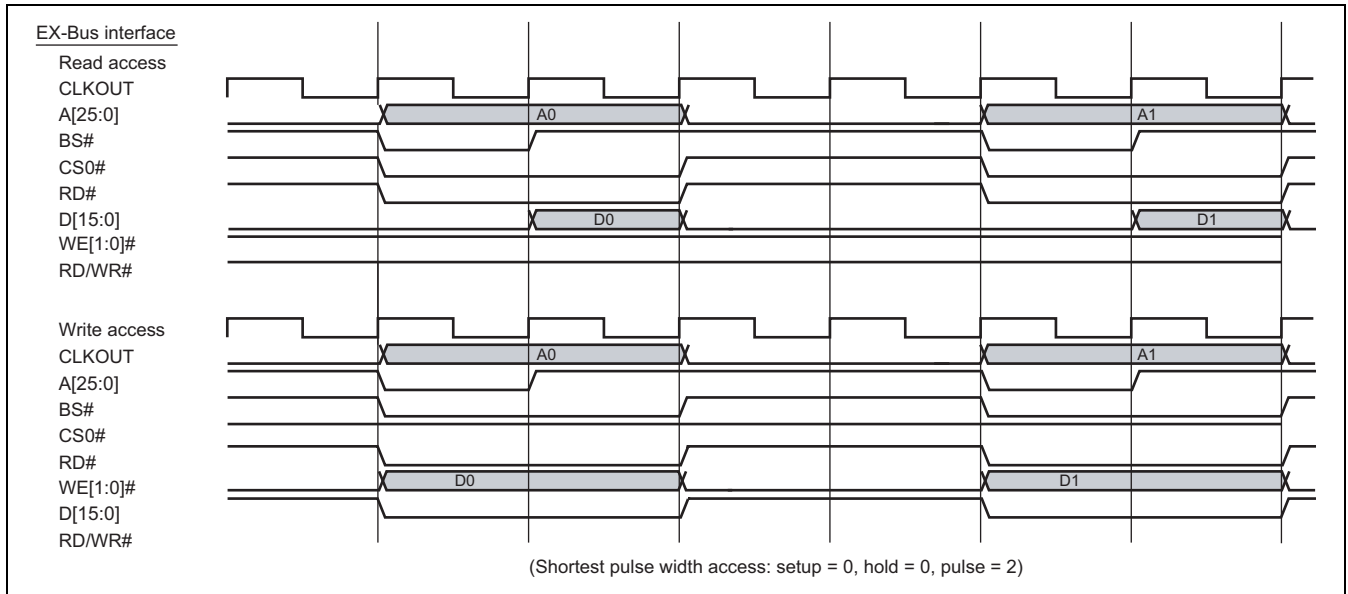


Figure 14.3 Basic Timing Chart for Access from AXI to SRAM (Area 0)



**Figure 14.4 Basic Timing Chart for Access from AXI to SRAM (Shortest Pulse Width × Shortest PIO Consecutive Accesses)**

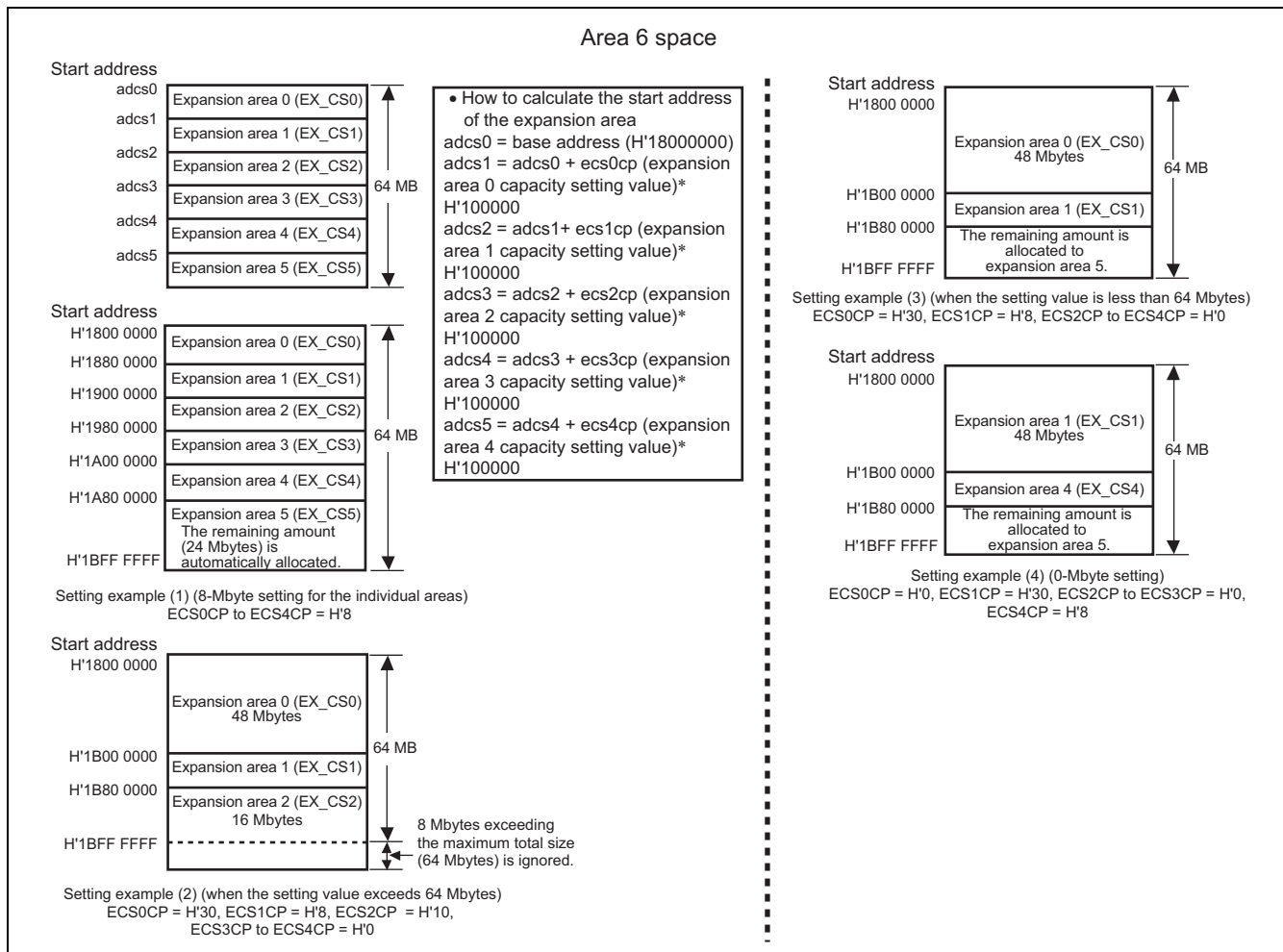
Figure 14.4 is an example of the basic SRAM interface waveform with the shortest pulse width, wherein the same waveform occurs twice in succession.

If consecutive PIO access requests are made from the CPU (AXI bus), the access interval will be 2 clock cycles, as indicated in the above waveforms, regardless of whether the preceding or succeeding access request is for the same area or for different areas. If a switching occurs, such as PIO → DMA or DMA → PIO, however, the access interval will be 1 clock cycle.

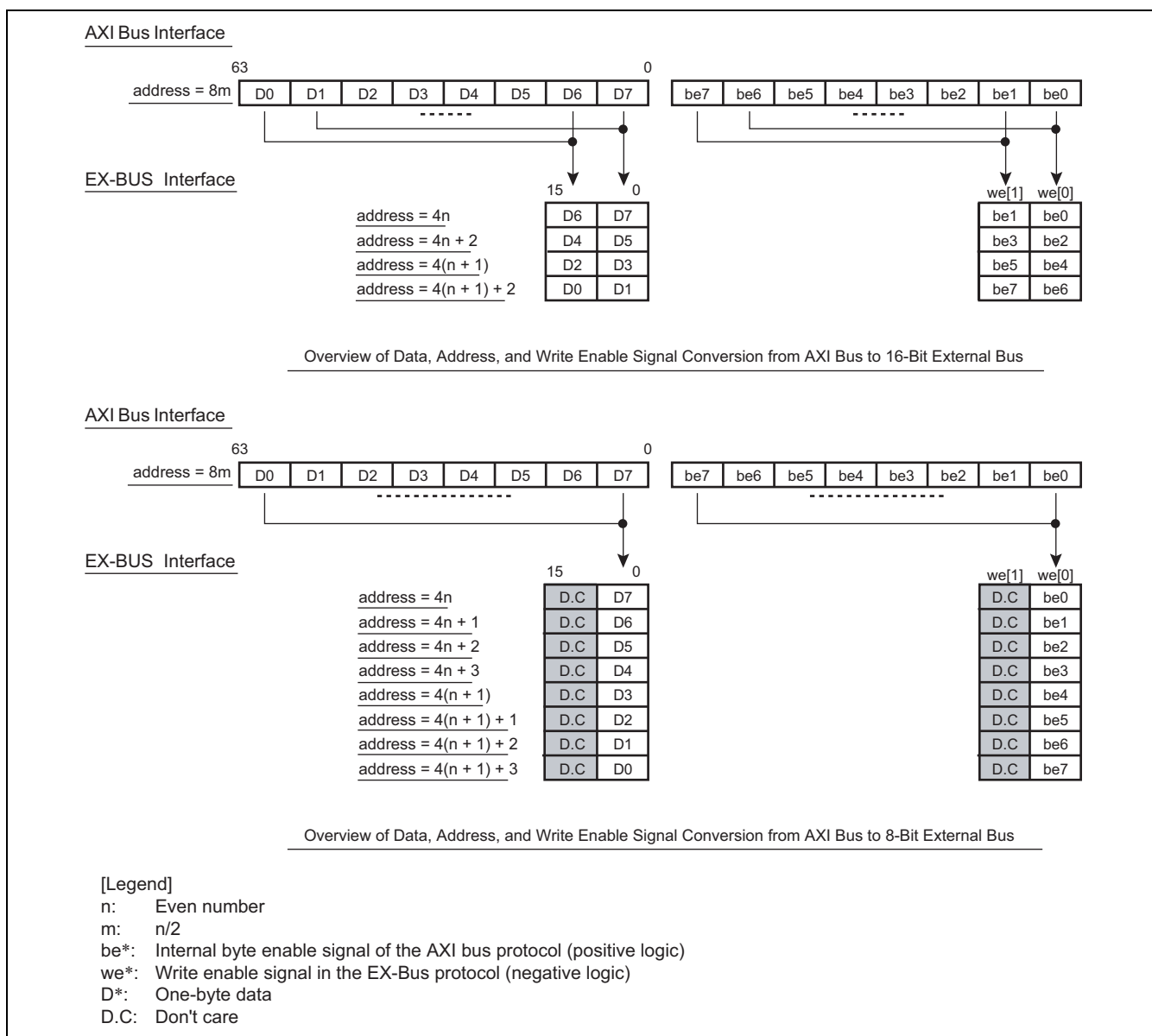
The access interval can be extended by means of the guard setting registers.

**(1) Address Generation/Alignment**

When making access to the EX-BUS as an SRAM interface, the LBSC generates addresses and performs data alignment conversions in addition to determining which area is to be accessed according to how the expansion area space is partitioned by register settings. Figure 14.5 shows the method by which the expansion area is partitioned. Figure 14.6 provides an overview of address generation and data alignment/write enable conversions.



**Figure 14.5 Expansion Area Partition**



**Figure 14.6 Overview of Data, Address, and Write Enable Signal Conversion from CPU (64-Bit AXI Bus) to External Bus**

**(2) Setting the Pulse Width for an Access Signal**

When making access to the EX-BUS, the LBSC can set the setup or hold time for addresses, RD/WR#, and CS# signals based on WE# signals and RD# signals, and the pulse width for WE# and RD# signals in units of clock cycles, according to the values that are set for each area by means of the CSWCR0, CSWCR1, or ECSWCRx (x = 0 to 5) registers. (During a burst ROM read operation, however, the LBSC conforms to CS0BTPH settings rather than CSWCR0 settings. Similarly, during a DMA operation, it conforms to EXDMAWCR0 to EXDMAWCR2 settings rather than CSWCR0, CSWCR1 or ECSWCRx (x = 0 to 5) settings.) The pulse width for WE# or RD# signal that is stored in a register can be extended by an externally supplied EX\_WAIT signal. The minimum total value that is set should be two clock cycles.

### (3) External Wait Control

The LBSC controls the external wait signal (EX\_WAIT) from a device connected to the EX-BUS based on settings that are provided on external wait control registers (CSPWCR0, CSPWCR1, or ECSPWCR<sub>x</sub> (x = 0 to 5)) and the external wait input control register (EXWTSYNC). The external wait control registers permit the selection of the four types of interfaces to accommodate various types of specifications, whether the wait signal input from an external device is based on the READY logic (posting a READY status) or BUSY logic (posting a BUSY status), or which signal polarity is in effect.

Figure 14.7 shows waveforms for the four wait signal patterns that can be input and the waveforms for the wait signals internal to the LBSC after conversion according to the register settings.

The external wait input control register allows the switching between the synchronous/asynchronous handling of external wait input signals. The default is to treat such signals on a synchronous basis. Figure 14.8 shows external wait input timings for synchronization/asynchronization. In the figure, the position indicated by the symbol \* represents the point at which the LBSC determines whether or not external wait is in effect. Specifically, for synchronization, the position is one clock cycle before the point at which the WE# and RD# signals would normally be negated by pulse width settings. If external wait is in effect at this position, the pulse width for the WE# or RD# signal continues to extend until the wait status becomes the ready status. If the pulse width for the WE# or RD# signal is extended by the EX\_WAIT signal, the address and the RD/WR# and CS# signals are negated when the hold time is satisfied. If the synchronization setting is switched to the asynchronization setting, any external wait is nullified unless there is an external wait two clock cycles before the \* position, or three clock cycles before the point in which the WE# and RD# signals would normally be negated.



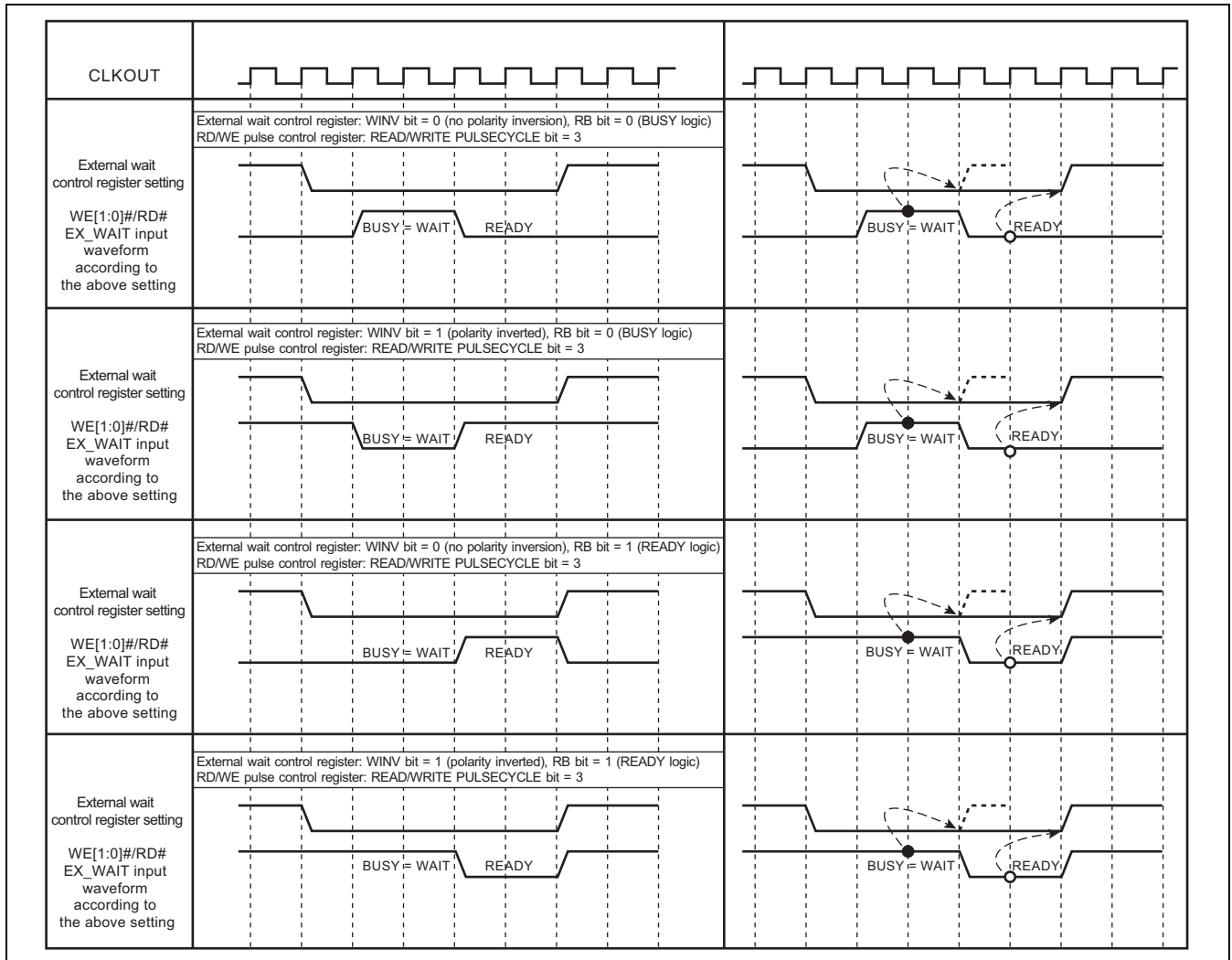


Figure 14.7 Waveforms of Converted External Wait Interface

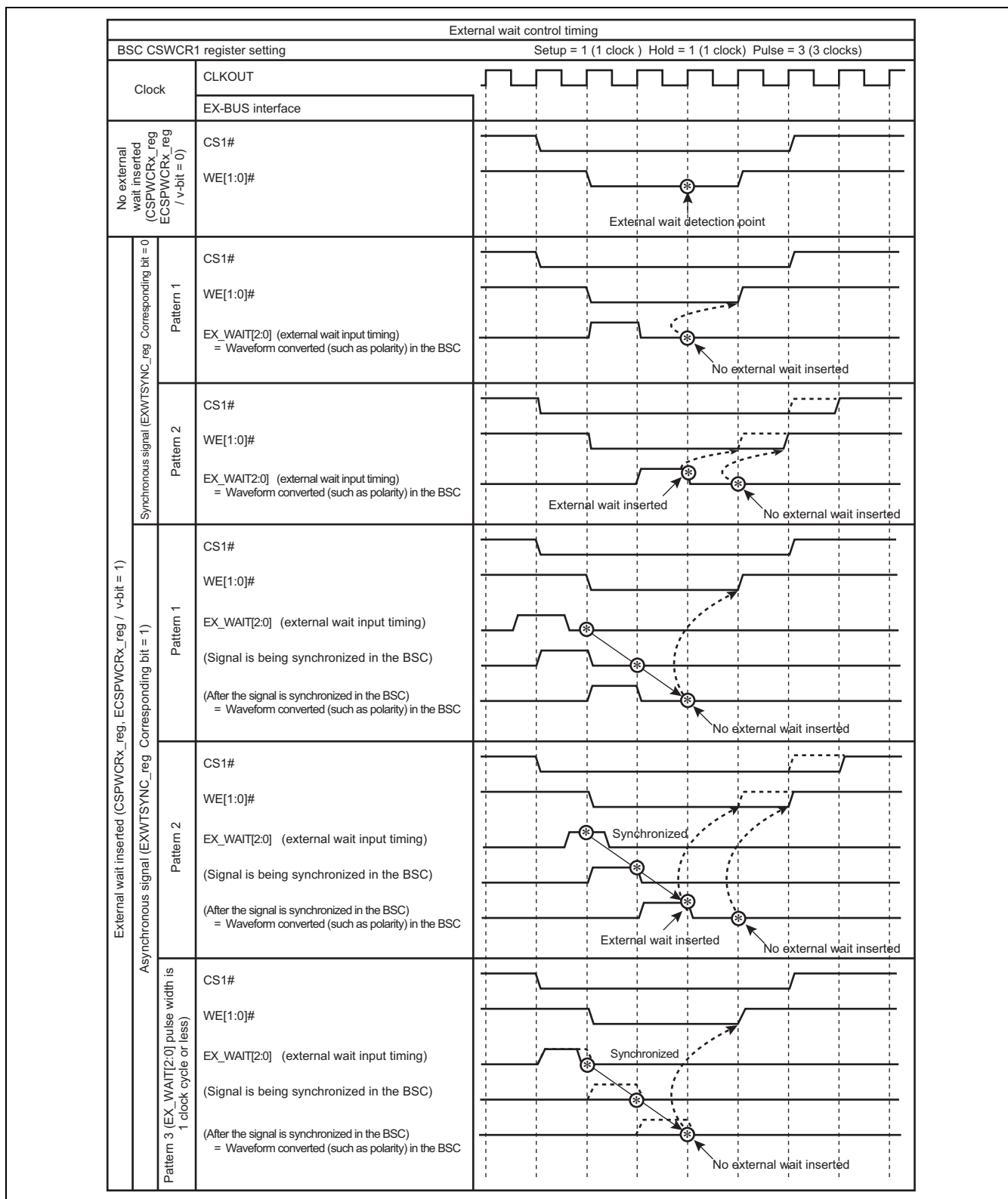


Figure 14.8 Waveforms of External Wait Input Signals

#### (4) Controlling Guard Intervals

For some external devices, the transition of the data lines to the high-Z state after completion of read access takes a relatively long time. To prevent any contention for the data bus when further access over the EX-BUS proceeds immediately after a read operation for such a device, the LBSC supports a function to guard against further access over a given interval following each bus access. The function is also effective for external devices that have difficulty coping with consecutive reception of access requests. Specifically, set the number of clock cycles over which guarding against access applies in the guard setting register (CS1GDST, ECS0GDST to ECS5GDST) for the given area. (Even if the value assigned to the guard setting register is 0, hardware processing before a further bus access request is issued requires at least 2 clock cycles between PIO and PIO, and at least 1 clock cycle between PIO and DMA. Therefore, in PIO accesses, the actual interval on the EX-BUS is 2 clock cycles when value in the guard setting register is 0 or 1. And it is 1 clock cycles plus the setting for number of clock cycles in the guard setting register when the setting value is 2 or more.)

After access to a given area, the guard interval is assigned corresponding to the register for that area, regardless of the kind of access or target space of the next access request. Note, however, that there is no guard setting register for area 0. Therefore, guard intervals are not set up for access that immediately follows access to this area. Since area 0 is supposed to be for the connection of general-purpose memory such as ROM, SRAM, or flash-ROM, guard intervals should not be necessary for this area. Figure 14.9 is a basic timing chart to illustrate the concept of guard-interval control.

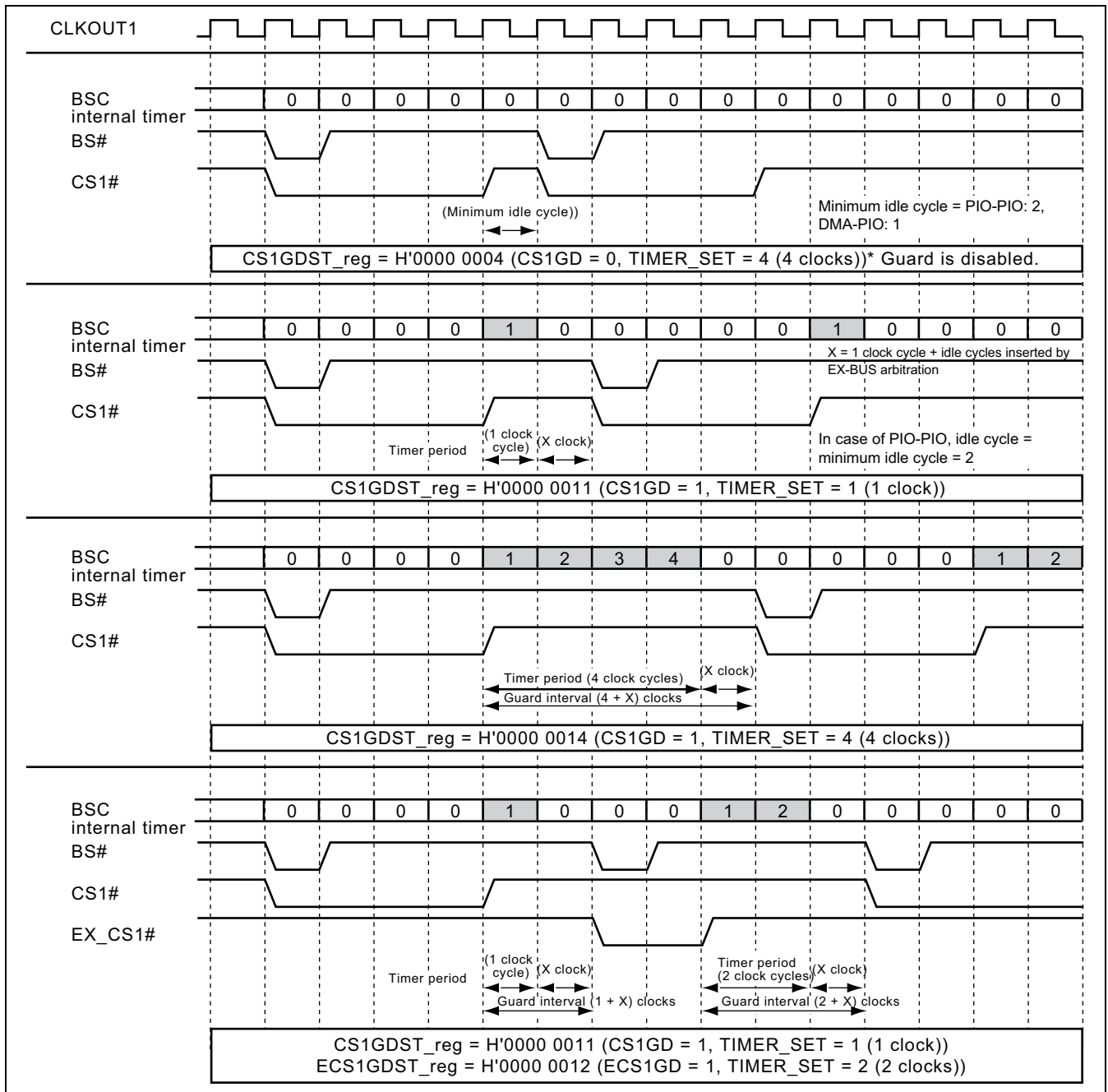


Figure 14.9 Concept of Guard-Interval Control

### 14.6.2 CPU (AXI Bus) → Burst ROM Interface

For area 0 on the EX-BUS, the BSC supports a page-mode read burst ROM interface. Switching to the burst ROM interface is performed by CS0CTRL settings. Because burst ROM access operations begin immediately after setting CS0CTRL, values must be pre-assigned to the CS0BTPH and CS0BSTCTL. In CS0BTPH, burst ROM access waveforms can be assigned, such as a first-cycle burst pitch, second and subsequent cycle burst pitches, and CS# signal hold cycles on the RD# signal. A burst access count (burst length) can be assigned to CS0BSTCTL. A burst access count should be assigned according to the component specifications for the actual external ROM that is connected.

In two kinds of exceptional cases, however, the BSC handles access with a burst count less than the specified burst count. The first are those cases where the CPU requests access to fewer data than the specified burst count. In such cases, access is terminated on completion of processing for the number of bytes requested by the CPU, even though the specified burst count has not been reached. The second are those cases where a variable burst address boundary is crossed in the midst of a specified burst count. In such cases, access is terminated immediately before the boundary is crossed, and the burst access is divided up, with the remainder of the access executed in a second round. The reason for this behavior is that the variable address boundaries for burst ROM devices, by which the LBSC must abide, are defined. Table 14.3 shows the LBSC's methodology for breaking off burst access.

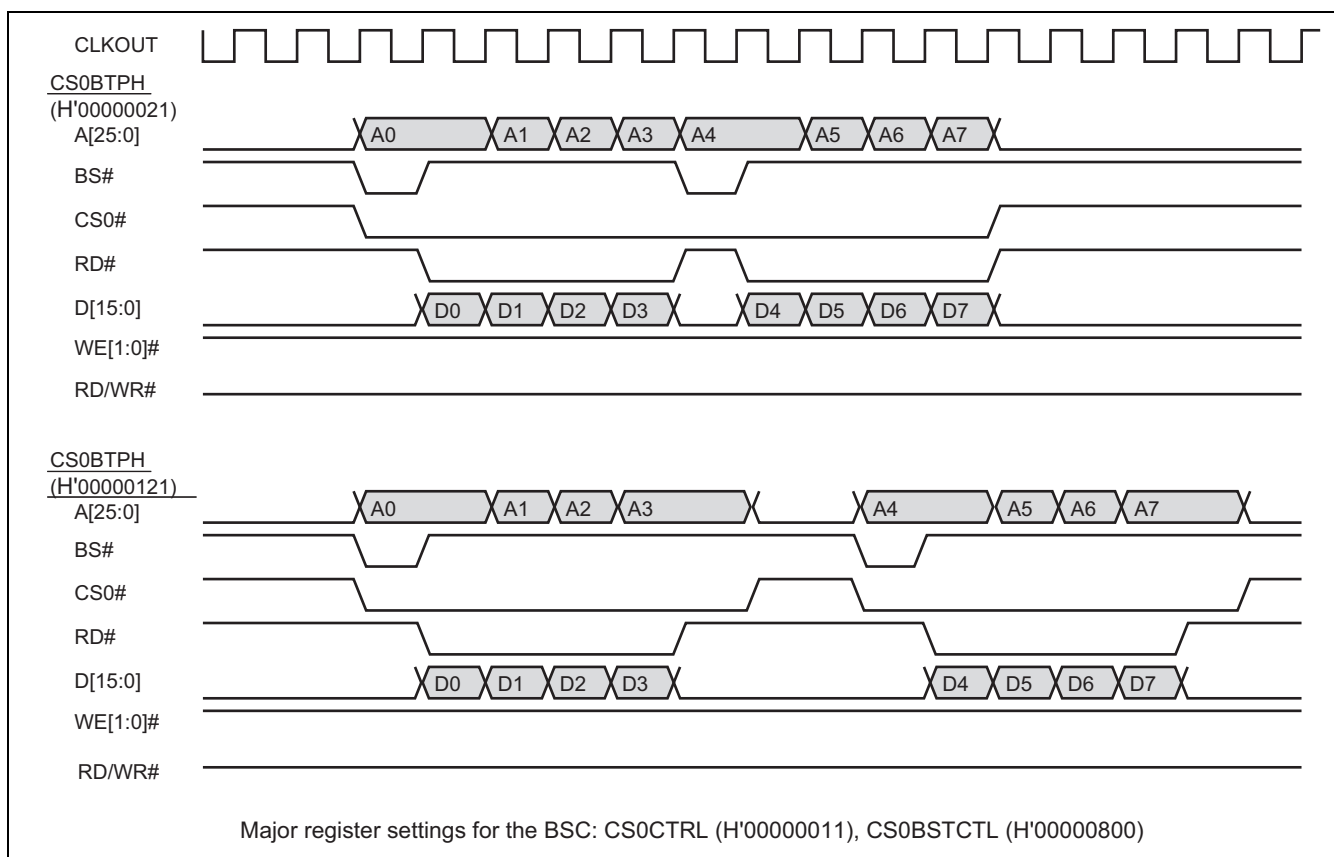
**Table 14.3 Methodology for Breaking off Bust Access**

Burst Count Assigned in CS0BSTCTL	Bus Width	
	8-Bit Bus Width	16-Bit Bus Width
4	Break at a change of A2	Break at a change of A3 (A0 not connected)
8	Break at a change of A3	Break at a change of A4 (A0 not connected)
16	Break at a change of A4	Break at a change of A5* (A0 not connected)
32	Break at a change of A5*	(Setting prohibited)

Note: \* Since A5 never changes in the midst of a 32-byte burst operation (a 32-byte boundary), access is not broken off in the case indicated by \*, and the specified number of access operations proceed.

As described above, in burst ROM access, the LBSC performs a maximum of 32-byte access to accommodate CPU cache fill while performing access breakup. However, because this operation involves access on 32-byte boundaries, for setting a burst ROM device, the user should specify wrap-around settings instead of continuous burst operations.

Depending on the mode of burst ROM connection, burst operations can also be accommodated in the synchronous burst mode. When using the LBSC in synchronous burst mode, the user should not receive the Wait signals that are output by the burst ROM. Instead, a first-word data output latency should be assigned to the configuration register of the burst ROM, and CS0BTPH should be set as the pitch for the first word and this latency. For the second and subsequent words, a pitch count of 2 should be assigned to both the configuration register of the burst ROM and CS0BTPH. Subject to the AC characteristics of the burst ROM and given frequency for the EX-BUS, if a pitch count of 1 is assigned to, data reception timing can lag behind due to the fact that the burst ROM has a data output delay of approximately 13ns. Figure 14.10 shows a basic timing chart for the burst ROM interface.



**Figure 14.10 Timing Chart for Burst ROM Interface**

**14.6.3 LBSC-DMAC → DMA Interface**

On the EX-BUS, three LBSC-DMAC channels (0 to 2) are assigned as DMACs that have external pins DREQ, DRACK, and DACK to support DMA transfer operations. Among these, channels 0 and 1 also support DMA with a burst length of 8.

All DMA channels operate in dual address mode. Table 14.4 provides a list of DMA pins by channel.

When operating a DMAC channel, first each DMAC should be assigned to the applicable area by using area assignment registers (EXDMASET0 to EXDMASET2) for the LBSC-DMAC channels. Also, in RD/WE pulse control registers (EXDMAWCR0 to EXDMAWCR2) for LBSC-DMAC channels, waveform pulse widths to be used during DMA bus access should be assigned (LBSC-DMAC channels 0 to 2 operate by the settings provided in EXDMAWCR0 to EXDMAWCR2, not by pulse width settings that are provided in CSWCR0, CSWCR1 or ECSWCR0 to ECSWCR5. In addition, methods by which DREQ, DACK, and DRACK signals are to be sent and received should be specified with the LBSC-DMAC channel control registers (EXDMCR0 to EXDMCR2).

**Table 14.4 List of DMA Pins by Channel**

DMAC Channel Number	Operating Mode	Pins			Remarks
		DREQ	DRACK	DACK	
Channel 0	Dual address mode (with 8-burst function)	DREQ0 (polarity and edge/level detection selectable)	DRACK0 (output timing adjustable and polarity selectable)	DACK0 (polarity selectable)	The burst count (8) does not depend on the access size; 8 consecutive bus accesses are executed for 8-bit and 16-bit bus widths equally.
Channel 1	Dual address mode (with 8-burst function)	DREQ1 (polarity and edge/level detection selectable)	—	DACK1 (polarity selectable)	DRACK1 does not exist as an LSI pin. The burst count (8) does not depend on the access size; 8 consecutive bus accesses are executed for 8-bit and 16-bit bus widths equally.
Channel 2	Dual address mode	DREQ2 (polarity and edge/level detection selectable)	—	DACK2 (polarity selectable)	DRACK2 does not exist as an LSI pin.

**(1) Data Alignment during LBSC-DMAC Access**

When receiving an access request from the LBSC-DMAC, the BSC translates the LBSC-DMAC interface into the EX-BUS protocol. During this operation, the BSC determines the area to be accessed based on the settings provided in the LBSC-DMAC area assignment registers (EXDMASET0 to EXDMASET2), and generates a chip select signal. For the data alignment of DMAC channels, one of two modes can be selected based on DMAC register settings.

- Fixed Alignment Mode

In this operating mode, when performing a DMA transfer with a device on the EX-BUS, the LBSC determines that the access size from the LBSC-DMAC is equal to the data width used by the external device (not bound by the bus width specified in the CS0CTRL, CS1CTRL or ECS0CTRL to ECS5CTRL). In the fixed alignment mode, no alignment translation is performed in the BSC. Instead, data is output using the alignment received from the LBSC-DMAC. The LBSC, however, generates the WE1# to WE0# signals, depending on the access size received from the LBSC-DMAC. In the initial state, the LBSC operates in this mode. Table 14.5 shows the relationship between data widths and access sizes.

**Table 14.5 Relationship between Data Widths and Access Sizes in Fixed Alignment Mode**

Access Size Set in DMAC (Assumed to be Bus Width)	Data Bus Read/Write Position		Write Enable Signal Output Position	
	D15 to D8	D7 to D0	WE1#	WE0#
16 bits	Data 15 to 8	Data 7 to 0	Assert	Assert
8 bits	—	Data 7 to 0	—	Assert

- Variable Alignment Mode

If the access size set in the DMAC is smaller than the bus width set in the BSC, variable alignment mode can be set up by DMAC register settings. In this case, the BSC changes byte lanes according to the specific access address to be serviced. Table 14.6 shows the relationship between data widths and access sizes in variable alignment mode. If the bus width set in the LBSC is equal to the DMAC access size, variable alignment mode operates in the same way as fixed mode.

**Table 14.6 Relationship between Data Widths and Access Sizes in Variable Alignment Mode (Little Endian)**

Bus Width Set in BSC	Access Size Set in DMAC	Data Bus Read/Write Position		Write Enable Signal Output Position	
		D15 to D8	D7 to D0	WE1#	WE0#
16 bits	16 bits	2n address		2n address	
	8 bits	2n+1 address	2n address	2n+1 address	2n address
8 bits	8 bits	—	n address	—	n address

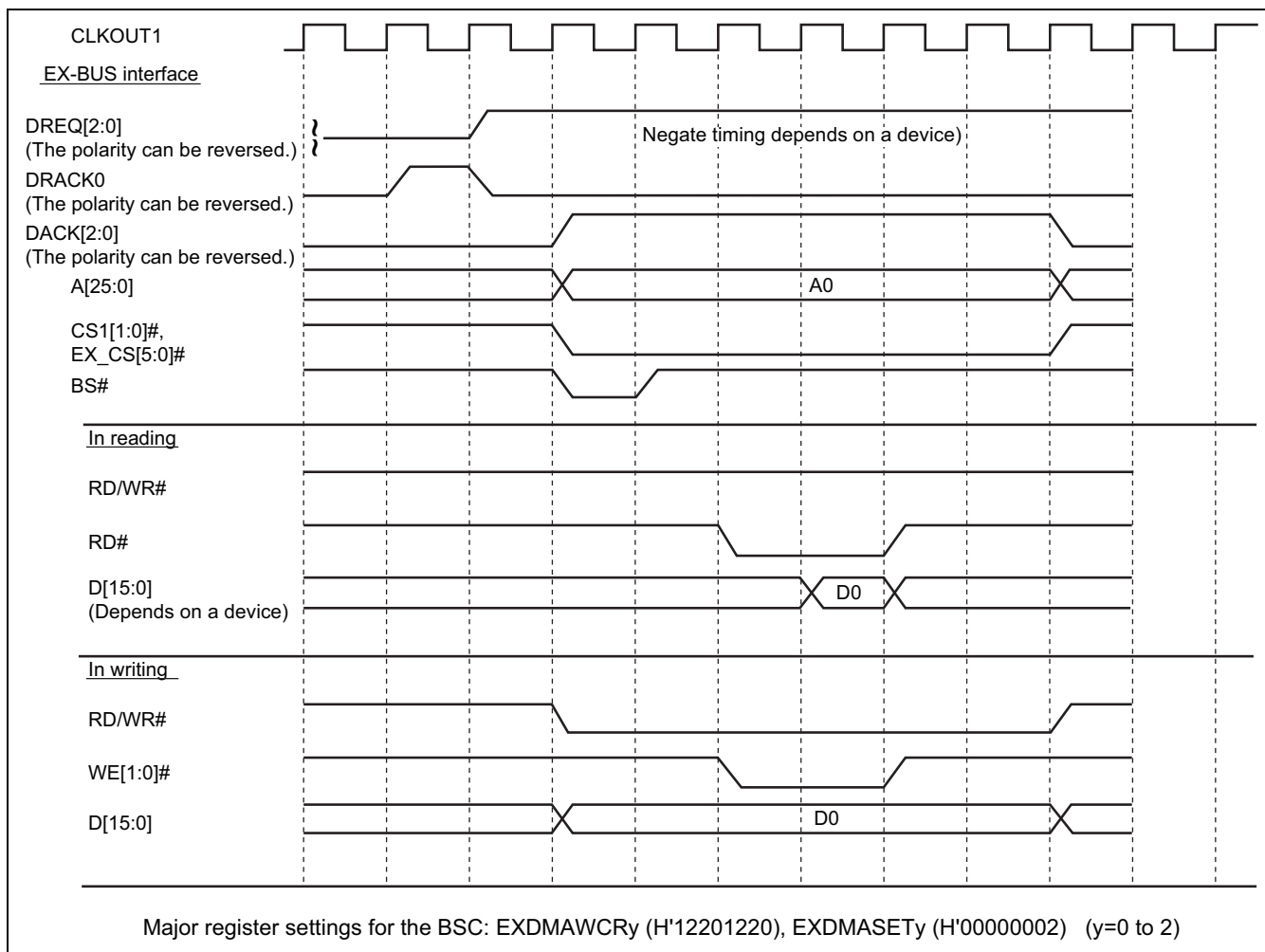
**(2) External Device DMA Transfer Request Detection Function**

To provide generality, the LBSC supports a polarity and level/edge selection function as a method for the reception of external device DMA transfer request signals (DREQ). The selections are made by setting the relevant values in registers EXDMCR0 to EXDMCR2. In compliance with the settings, the BSC internally receives a DREQ signal and outputs the DMA transfer request signal from the BSC to the LBSC-DMAC. If level detection is selected, the BSC continues to output the DMA transfer request signal to the LBSC-DMAC as long as the DREQ signal from the external device is asserted. Conversely, if edge detection of the DREQ signal is selected, the BSC will not output a DMA transfer request signal to the LBSC-DMAC until an edge is detected, even if the DREQ signal from the external device continues to be asserted. In addition, even if more than one edge is detected during the period from the first edge detection to the start of DMA transfer, only one transfer request is issued.



**(3) Role of the BSC between the LBSC-DMAC and an External Device**

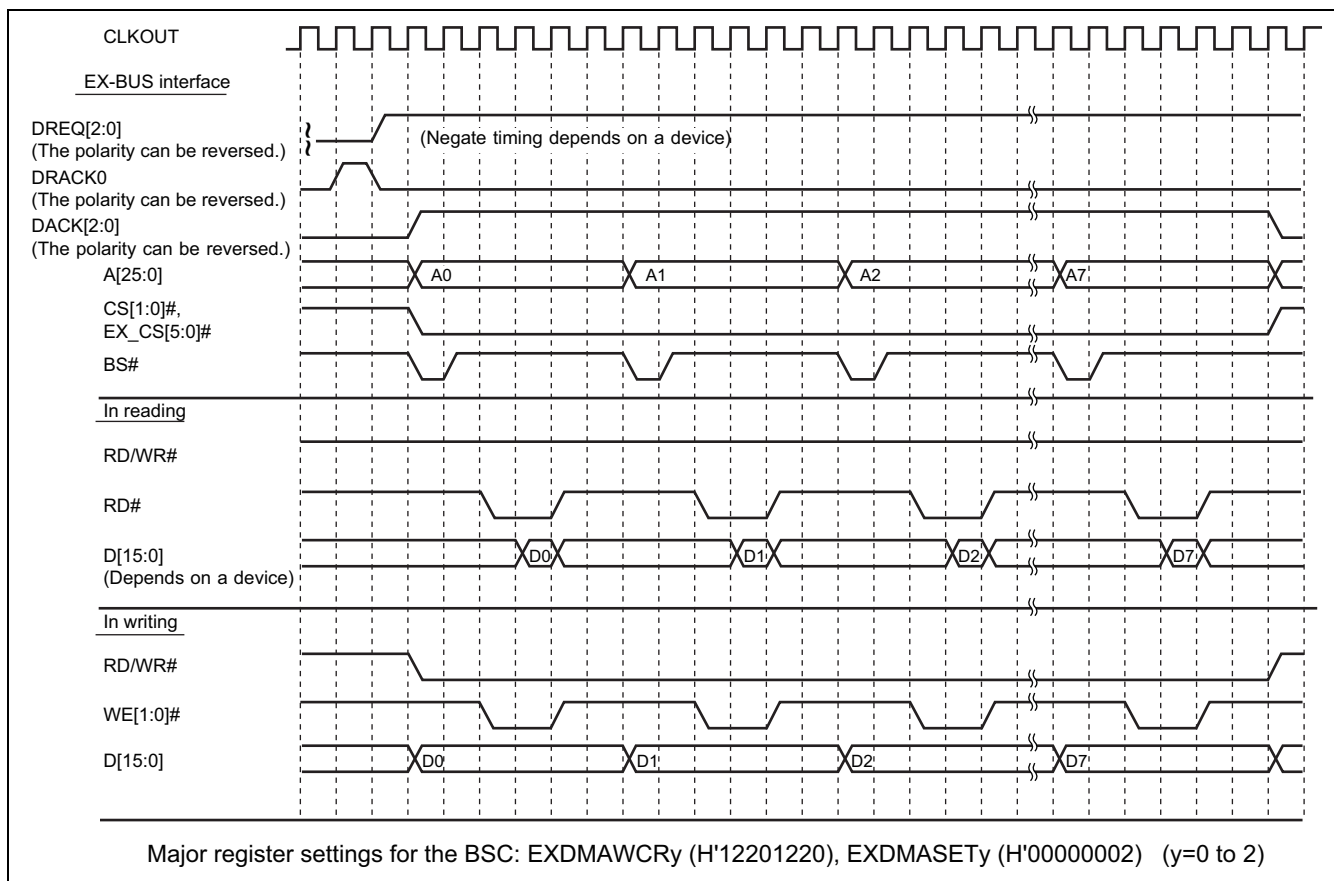
Figure 14.11 shows a basic timing chart for LBSC-DMAC-to-EX-BUS output translation. Upon receipt of an access request from the DMAC, the BSC first performs bus contention arbitration. When the LBSC-DMAC acquires the bus mastership, the BSC controls the pulse width of RD#, WE1# and WE0# that are output on the EX-BUS according to the settings provided in the LBSC-DMAC channel RD/WE pulse control registers (EXDMAWCR0 to EXDMAWCR2) that the BSC possesses, for the LBSC-DMAC access period.



**Figure 14.11 Basic Timing Chart for Access from LBSC-DMAC to EX-BUS**

**(4) LBSC-DMAC → EX-BUS Burst Access**

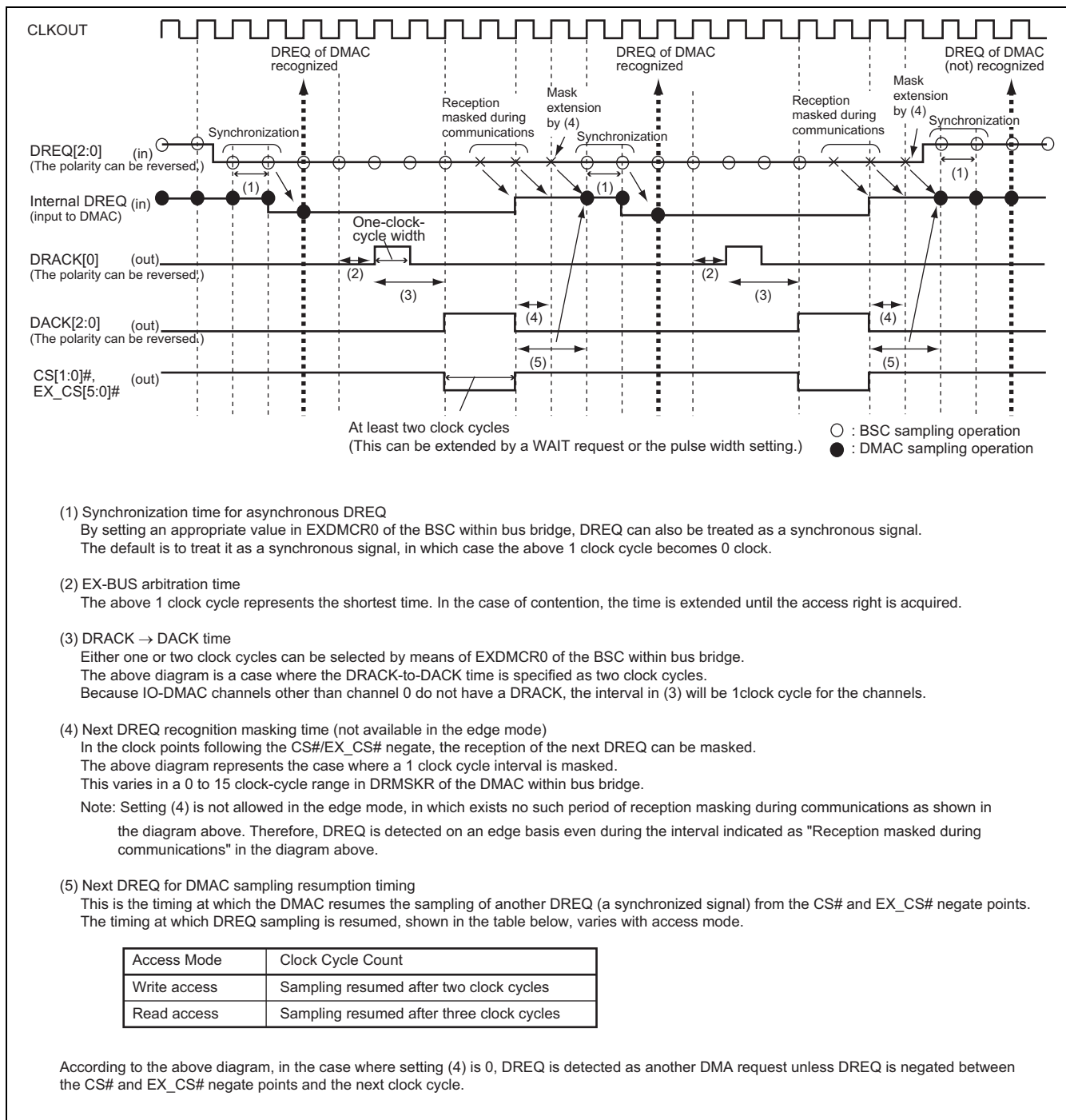
The BSC supports the EX-BUS output function for burst access operations from the LBSC-DMAC (eight consecutive transfers irrespective of the access size). Figure 14.12 shows a timing chart on LBSC-DMAC burst access. The waveform for LBSC-DMAC burst access basically takes the form of repeated single-access waveforms. However, because external DMAC bus access does not release the bus mastership until the burst access is finished, PIO access from the CPU (AXI) does not result in a cycle stealing. In addition, transfer performance is enhanced because the DMAC treats data involving 8 transfer operations as a single packet and performs transfer operations with the destination.



**Figure 14.12 Basic Timing Chart for Burst Access from LBSC- DMAC to EX-BUS**

**(5) DREQ Reception Timing**

Figure 14.13 shows the timing at which a DMA request (DREQ) signal is set in the level reception mode and any continuation of an asserted state is regarded as another DMA request. The figure also shows DREQ negate timing that prevents the above condition from being mistaken as another DREQ request.



**Figure 14.13 Next DREQ Signal Recognition Timing on EX-BUS**

#### 14.6.4 CPU (AXI Bus) → Byte-Control SRAM Interface

With respect to EX-BUS area 1 and expansion areas 0 to 5, the LBSC supports byte-control SRAM interface from the CPU (AXI bus) or LBSC-DMAC (area 0 is excluded). Byte-control SRAM interface is a memory interface in which byte select strobe signal WE# is output in both read and write cycles. Write timing for byte-control SRAM interface is the same as that for SRAM interface. In read access, however, WE# is output at a different timing. In read access, WE# is output for a read byte only. The assertion timing of WE# can be selected with the CS1BRM bit in the CS1CTRL register or the ECSxBRM bit in the ECSxCTRL register to be the same as that of CS# or RD#. In default setting, SRAM operating mode is set for each area. Accordingly, along with the setting of assertion timing, byte-control SRAM mode should be set in the registers corresponding to a given area (CS1CTRL or ECSxCTRL(x = 0 to 5)).

##### (1) Byte-control SRAM Interface

- The WE# assertion period can be selected by the CS1BRM bit or the ECSxBRM bit (x = 0 to 5) to be the same as that of CS# or RD#.
- In read access, WE# is asserted only for a valid access byte. (For example, when a byte is read from a device with the byte-control SRAM interface and a bus width of 16 bits, any one of the WE# bits is asserted.)
- The waveform in write access is the same as that for SRAM interface.

##### (2) Basic Timing Charts

Figure 14.14 shows the basic timing chart for byte-control SRAM interface.

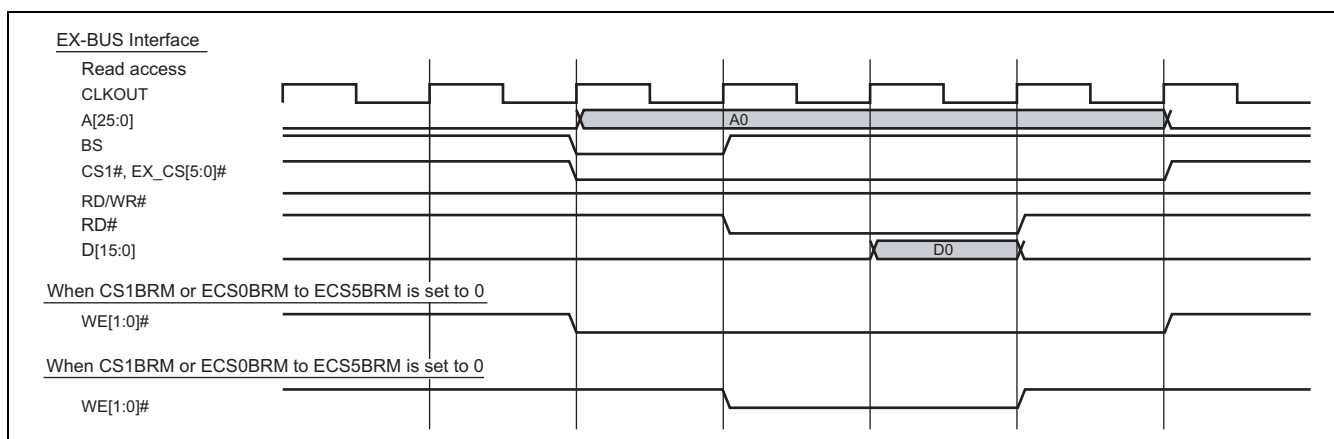


Figure 14.14 Waveforms for Byte-Control SRAM Interface

### 14.6.5 CPU (AXI Bus) → ATA Device Interface

With respect to EX-BUS area 1 and expansion areas 0 to 5, the LBSC supports an ATA device interface from the CPU (AXI bus) or LBSC-DMAC (area 0 is excluded). Since in each space the default is the SRAM operating mode, register settings for a given area from among CS1CTRL and ECS0CTRL to ECS5CTRL should be set for the ATA space. To perform multi-word DMA transfer in the ATA interface, set the DBST bit in the EXDMCRy (y = 0 to 2) register to 1.

ATACS00#, ATACS10#, ATACS01#, or ATACS11# can be asserted in synchronization with the access space CS# signal depending on the ATACS control register (ATACSCTRL) settings.

#### (1) ATACS00, ATACS10, ATACS01, and ATACS11 Signals

If ATACS1\_EN and ATAECSt\_EN (x = 0 to 5) of the ATACS control register are set to 0 or 1, and the ATA mode is selected with the CS1IF bit of the CS1CTRL register and ECSxIF bit of the ECSxCTRL register, ATACS00#, ATACS10#, ATACS01#, or ATACS11# signal is asserted in synchronization with the relevant space CS# signal when the relevant space is accessed (the relevant space CS# signal is also asserted at the same time).

ATACS00#, ATACS10#, ATACS01#, or ATACS11# is asserted in accord with the value being output as address bit 4 on the external bus (i.e., the A4 pin).

If, for example, the CS1 space is ATA interface, the conditions below should apply to ATACS00#, ATACS10#, ATACS01#, and ATACS11# assertion.

ATACS1_EN	A4	CS1#	ATACS00#	ATACS10#	ATACS01#	ATACS11#
0	0	√	—	√	—	—
0	1	√	√	—	—	—
1	0	√	—	—	—	√
1	1	√	—	—	√	—

Note: √: Assert, —: Deassert

**(2) ATA Interface Signals**

Table 14.7 shows the LBSC output signals when the area is set for ATA device interface.

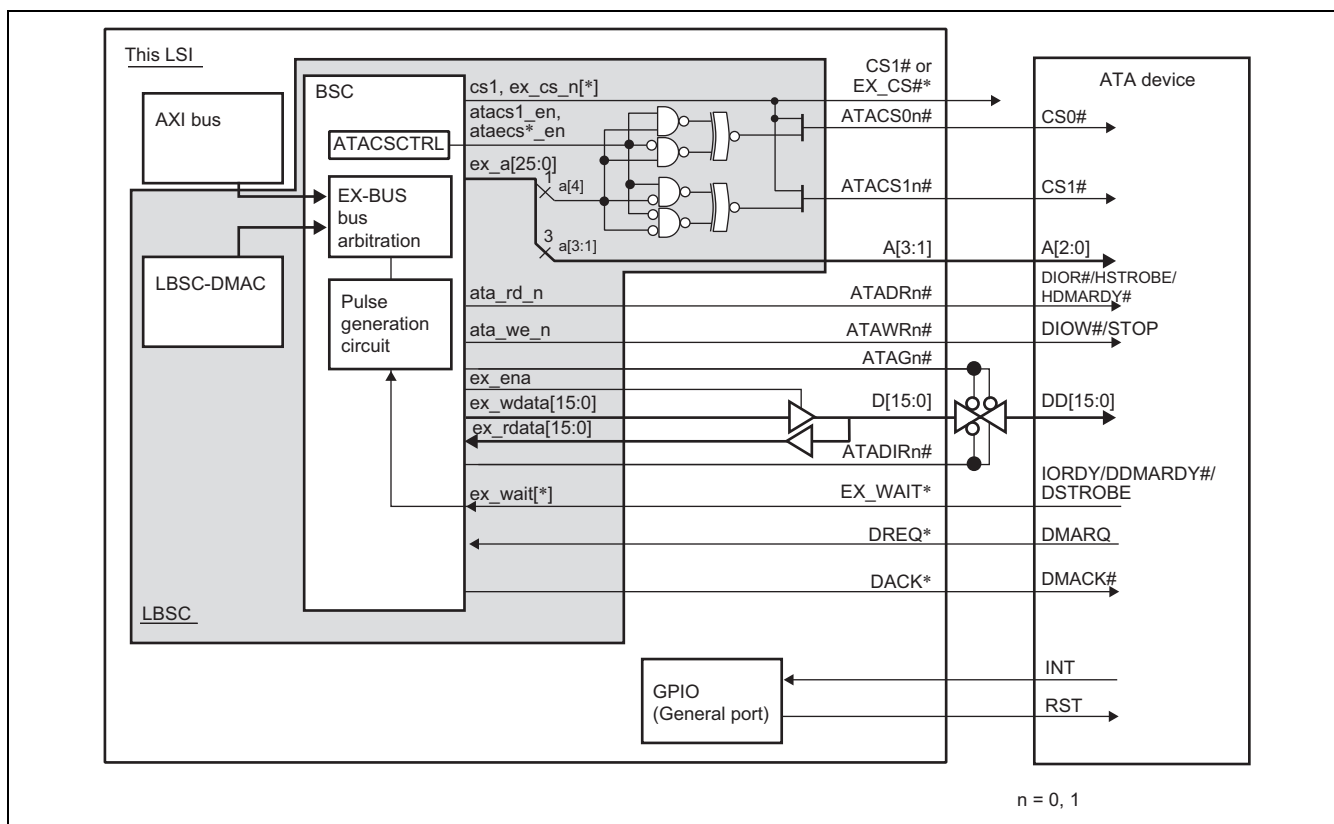
**Table 14.7 List of ATA Interface Signals**

No.	ATA I/F Signals	LBSC I/O Signal	I/O	Function	Remarks
1	CS0#	ATACS00#, ATACS01#	Output	Chip select (command block)	
2	CS1#	ATACS10#, ATACS11#	Output	Chip select (control block)	
3	DMARQ	DREQ[2:0] (the polarity can be reversed)	Input	DMA request	Polarity selectable Only pins DREQ[1:0] are used in Ultra DMA operation.
4	DMACK#	DACK[2:0]# (the polarity can be reversed)	Output	DMA acknowledge	Polarity selectable Only pins DREQ[1:0] are used in Ultra DMA operation.
5	A[2:0]	A[3:1]	Output	Address	
6	DD[15:0]	D[15:0]	I/O	Data	
7	DIOW#/STOP	ATAWR[1:0]#	Output	Write enable/STOP signal (for Ultra DMA operation)	
8	DIOR/HDMARDY#/ HSTROBE	ATARD[1:0]#	Output	Read enable/host DMA ready (for Ultra DMA read)/host data strobe (for Ultra DMA write)	
9	IORDY/DDMARDY#/ DSTROBE	Selected from EX_WAIT[2:0] (the polarity can be reversed)	Input	I/O ready/device DMA ready (for Ultra DMA write)/device data strobe (for Ultra DMA read)	
10	—	ATAG[1:0]#	Output	External buffer enable	
11	—	ATADIR[1:0]#	Output	External buffer direction control	Low output for write accesses

Note: The ATACSCTRL register should be set for use of ATACS00#, ATACS10#, ATACS01#, or ATACS11#.

**(3) ATA Interface Connection Configuration**

Figure 14.15 shows a sample connection between the ATA device and the LBSC when EX-BUS is set for ATA interface.



**Figure 14.15 EX-BUS ATA Device Configuration Example**

**(4) ATA Interface (PIO Mode, Multi-word Mode)**

The BSC provides the following ATA interface support functions:

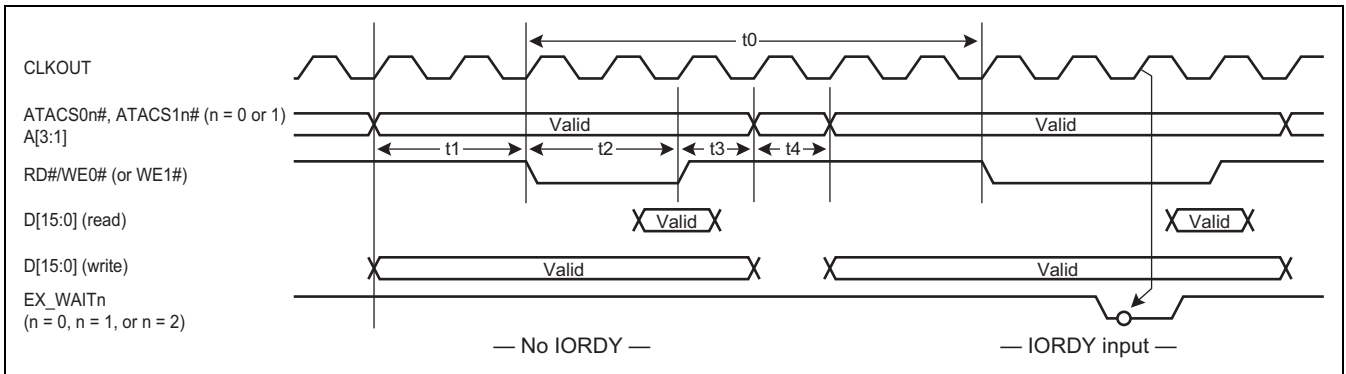
- Based on the IORDY signal received from an ATA device, the BSC performs wait control on the ATA interface.
- With an ATA interface, allocating the LBSC-DMAC makes multi-word DMA transfer possible. However, use the CPU to handle access to the ATA registers and the DMA controller to handle data transfer.
- For the detection of I/O ready timeout, the BSC monitors the state of the IORDY signal from ATA devices, and if an ATA device wait state lasting beyond a certain length of time is detected, the BSC indicates an ATA wait timeout error in a register within the BSC, and forces the termination of access to the ATA interface.

The required detection time depends on the EX-BUS operating frequency as defined in the following formula:

$$\text{Detection time in ns} = \text{period in ns at EX-BUS operating frequency} \times 100 \text{ clock cycles}$$

**(5) Basic Timing Charts (PIO Mode, Multi-word Mode)**

Figure 14.16 shows the basic timing chart for PIO transfer in the ATA interface.



**Figure 14.16 Waveforms for ATA Interface**

Table 14.8 shows sample settings for the RD/WE# pulse control register for PIO transfers in the ATA interface (when the EX-BUS operating frequency is 65 MHz).

**Table 14.8 Sample Settings for RD/WE# Pulse Control Register for PIO Transfers in ATA Interface (EX-BUS Operating Frequency: e.g. 65 MHz)**

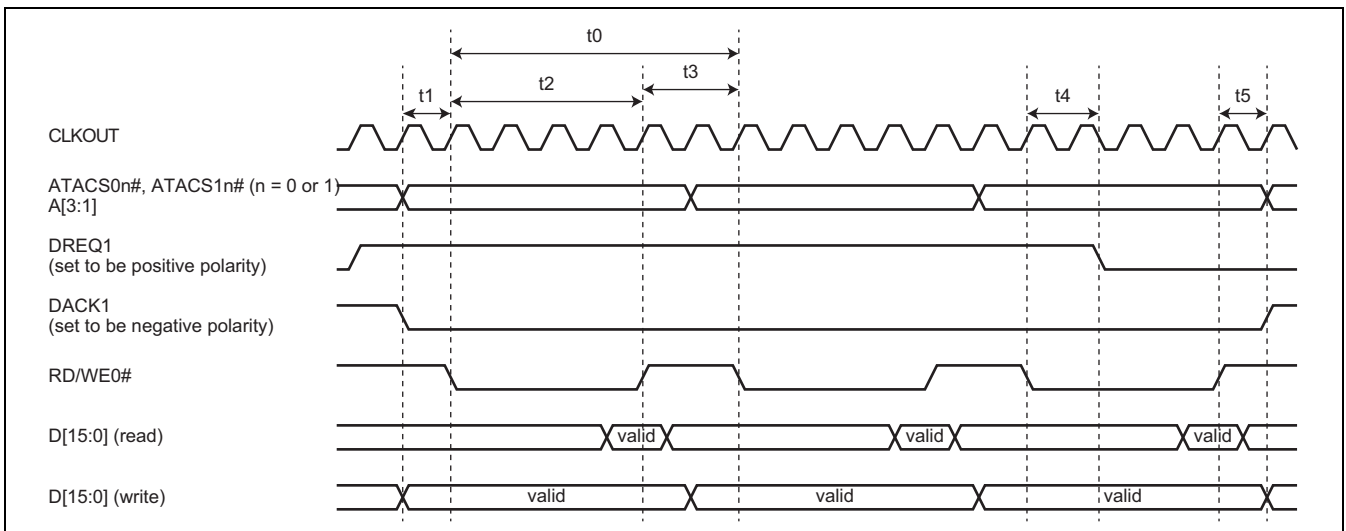
Mode	CSWCR Setting	Cycle Time (t0)	Address Setup (t1)	DIOR#/DIOW# Pulse Width (t2)	Address Hold (t3)	Idle Cycle (t4)
0	H'FF70FF70	691 (600)	107 (70)	477 (290)	107(20)	20 (-)
1	H'AA10AA10	400 (383)	62 (50)	323 (290)	15(15)	20 (-)
2	H'A210A210	347 (330)	31 (30)	301 (290)	15(10)	20 (-)
3	H'52105210	200 (180)	31 (30)	154 (80)	15(10)	20 (-)
4	H'2A102A10	123 (120)	31 (25)	77 (70)	15(10)	20 (-)

Units: ns

Values in parentheses indicate ATA prescribed values.

Note: The CSWCR setting must be such that the following condition is satisfied: ATA prescribed value  $\leq$  CSWCR set value  $\times$  EX-BUS clock (CLKOUT) width

Figure 14.17 shows the basic timing chart for multi-word DMA transfer in the ATA interface.



**Figure 14.17 Multi-Word DMA Waveforms for ATA Interface**



Table 14.9 shows sample settings for the RD/WE# pulse control register for multi-word DMA transfers in the ATA interface (when the EX-BUS operating frequency is 65 MHz).

**Table 14.9 Sample Settings for RD/WE# Pulse Control Register for Multi-Word DMA Transfers in ATA Interface (EX-BUS Operating Frequency: 65 MHz)**

Mode	EXDMAWCR Setting	Cycle Time (t0)	CS[1:0]# Setup (t1)	DIOR#/ DIOW# Pulse Width (t2)	DIOW# Negate Hold/DIOR# Negate Pulse Width (t3)	DIOW#/ DIOR# DREQ Delay Time (t4)	DACK Hold (t5)
0	H'97809780	508 (480)	108 (50)	277 (215)	231 (215/50)	– (120/40)	123 (20)
1	H'32203220	154 (150)	31 (30)	92 (80)	62 (50)	– (40)	31 (5)
2	H'2A202A20	139 (120)	31 (25)	77 (70)	62 (25)	– (35)	31 (5)

Units: ns

Values in parentheses indicate ATA prescribed values.

Note: The EXDMAWCR setting must be such that the following condition is satisfied: ATA prescribed value  $\leq$  EXDMAWCR set value  $\times$  EX-BUS clock (CLKOUT) width

#### (6) Ultra ATA DMA Mode

The Ultra ATA DMA mode differs from the PIO mode or multi-word mode with respect to the function of each signal interfacing with the ATA device. The LBSC operates with changing each interface signal function in Ultra ATA DMA mode as shown in Table 14.7. The connections between the LBSC and an ATA device on a board need not be changed from those shown in Figure 14.15.

For operation in Ultra ATA DMA mode, specify the ATA mode as the operating mode for the external bus area where an ATA device is connected. Specify LBSC-DMAC channel 0 or 1 as the DMAC assigned to the target area. After that, select the Ultra ATA DMA mode through UATMR in the LBSC-DMAC, make the necessary settings in the same way as for normal DMAC activation, and activate the DMA operation.

The following is a list of the features of the Ultra ATA DMA operation.

- Access to the registers in the ATA device such as initial settings, activation, or status read access can be done directly through PIO.
- Up to Ultra DMA mode 4 is supported.
- LBSC-DMAC channel 0 or 1 supports Ultra DMA.
- The A, DD, CS#, DIOR# or DIOW#, and EX\_WAIT signals are used for PIO R/W access to the area set to the ATA mode.
- For DMA write operation, the setup and hold periods of data relative to the HSTROBE (DIOR#) signal edge can be specified in units of output clock cycles.
- For DMA read operation, data is received in synchronization with the DSTROBE (IORDY) signal input. The HDMARDY signal is temporarily negated while reception is busy.
- Cycle-stealing is done for PIO transfer in other areas or transfer in other LBSC-DMAC channels even during Ultra DMA bus operation.
- Cycle-stealing occurs only when an external access request is generated within the LSI. It is executed while HDMARDY or DDMARDY is temporarily negated.
- The DMA transfer size is set to one sector, and a desired sector size can be specified. However, note that the base unit of transfer is 2 bytes  $\times$  16 burst, and this unit should be repeated an integral number of times (n) to obtain the desired transfer size.
- Cycle-stealing for PIO transfer in the current area is not allowed while one-sector DMA transfer is in progress.
- The CRC check function is supported.

- After one-sector DMA transfer, a CRC code (generation polynomial:  $X^{16} + X^{12} + X^5 + 1$ ) is output to the device.
- The output CRC code can be read from an LBSC-DMAC register (for debugging and evaluation use).
- The LBSC-DMAC provides a function for monitoring timeout during DMA transfer. When an overflow occurs, a timeout interrupt notification signal can be issued.

Figure 14.18 shows the Ultra ATA DMA operation timing.

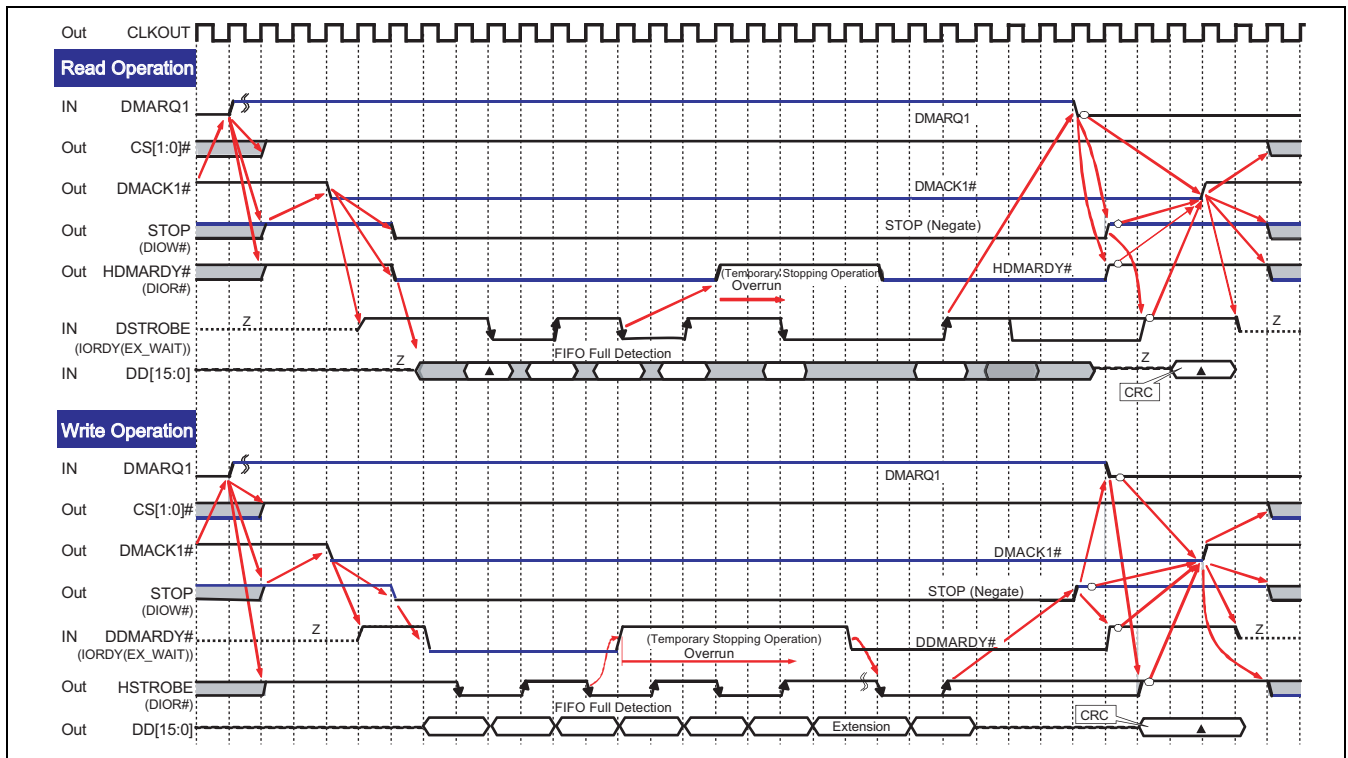
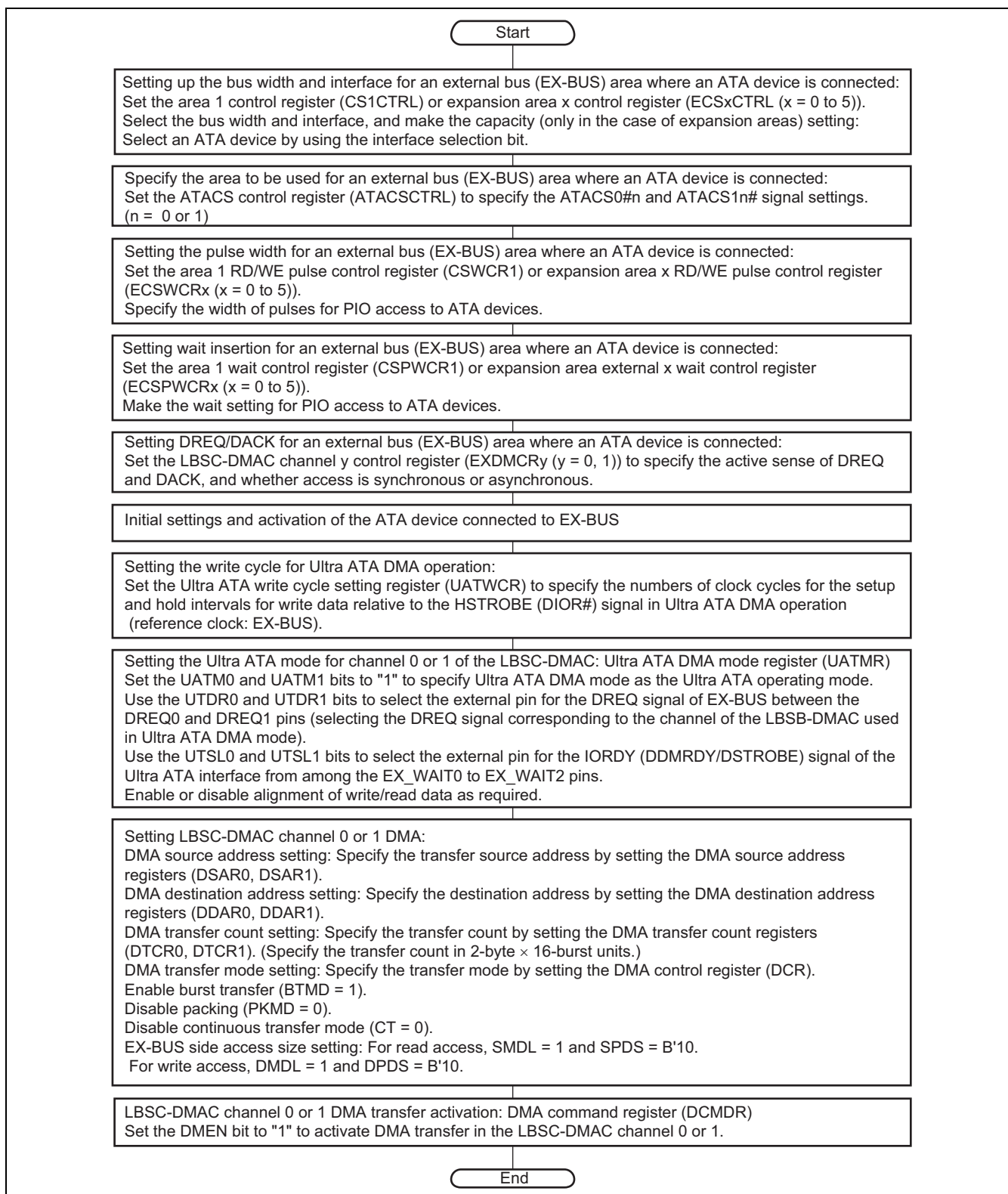


Figure 14.18 Ultra ATA DMA Operating Waveform

Figure 14.19 shows a setting procedure for the Ultra ATA DMA transfer.



**Figure 14.19 Setting Procedure for the Ultra ATA DMA Transfer**

### 14.6.6 Wait Timeout

For the detection of timeout in waiting for access to the EX-BUS, the BSC monitors the states of the EX\_WAIT2, EX\_WAIT1, and EX\_WAIT0 signals from external devices. When an external device is waiting for more than a certain length of time, this is detected as an EX-BUS wait timeout error. The error is reflected in a register within the BSC, and forces the termination of access to the EX-BUS interface.

The value of the timeout counter is specified in a total of 32 bits, consisting of the EXW\_TOBCNT bits in the EX-TIME wait timeout detection base counter register (EXBCT) and the EXW\_TOCNT bits in the EX-BUS wait timeout detection counter register (EXTCT). EXW\_TOBCNT is a 20-bit counter that operates at the EX-BUS operating frequency (CLKOUT). EXW\_TOCNT is a 12-bit counter that counts up by one every time the EXW\_TOBCNT bits overflow.

Writing 0s to all of the bits specifies the maximum time until overflow. The required detection time depends on the EX-BUS operating frequency as defined in the following formula.

$$\text{Detection time in ns} = \text{period in ns at EX-BUS operating frequency} \times \{\text{EXW\_TOCNT}, \text{EXW\_TOBCNT}\}$$

### 14.6.7 EX-BUS Arbitration

To deal with the conflicts between the access requests from the CPU (AXI bus) and LBSC-DMAC channels 0 to 2, the EXBATLV register in the LBSC can set the priority levels for these accesses. Furthermore, to deal with the conflicts among the LBSC-DMAC channels 0 to 2, the three channels are grouped into two groups by the DMA memory access priority level control register (DMLVLR) in the LBSC-DMAC, and the priority levels are determined according to the round-robin scheme in each group.

Figure 14.20 shows a concept diagram for EX-BUS arbitration.

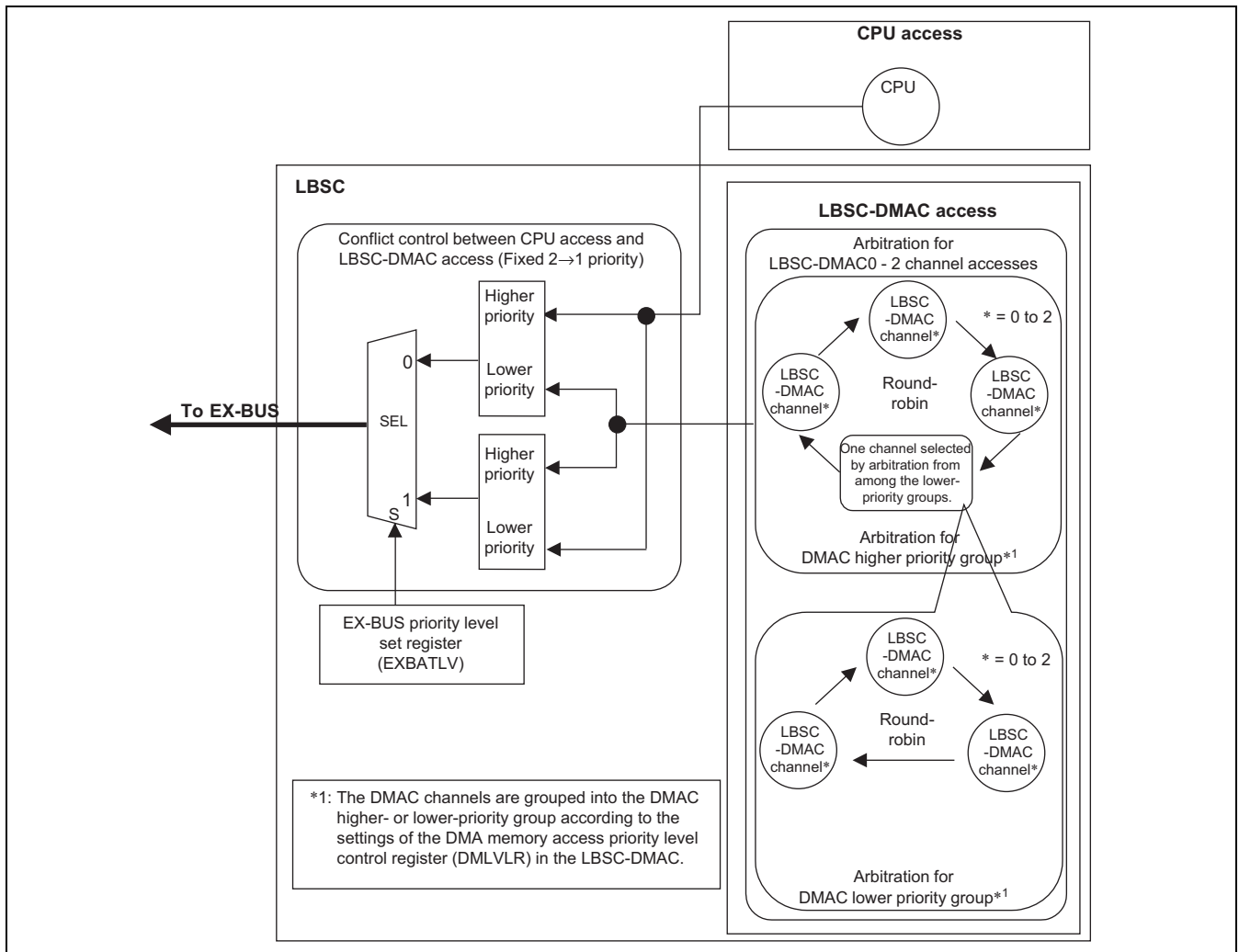


Figure 14.20 Concept Diagram for EX-BUS Arbitration

## 14.7 Usage Notes

<b>RZ/G1H</b>	<b>RZ/G1N</b>
<b>RZ/G1M</b>	<b>RZ/G1E</b>

Keep the following notes in mind when using this LBSC.

### 14.7.1 Pin Multiplexing

When starting this LSI, be sure to set multiplexed pins appropriately using the LSI pin multiplexing set register.

Also, make pull-up resistor settings using the LSI pin pull-up control registers.

For details on the specific set values, refer to section 5, Pin Function Controller (PFC).

### 14.7.2 Operations for Read Access by Ultra DMA

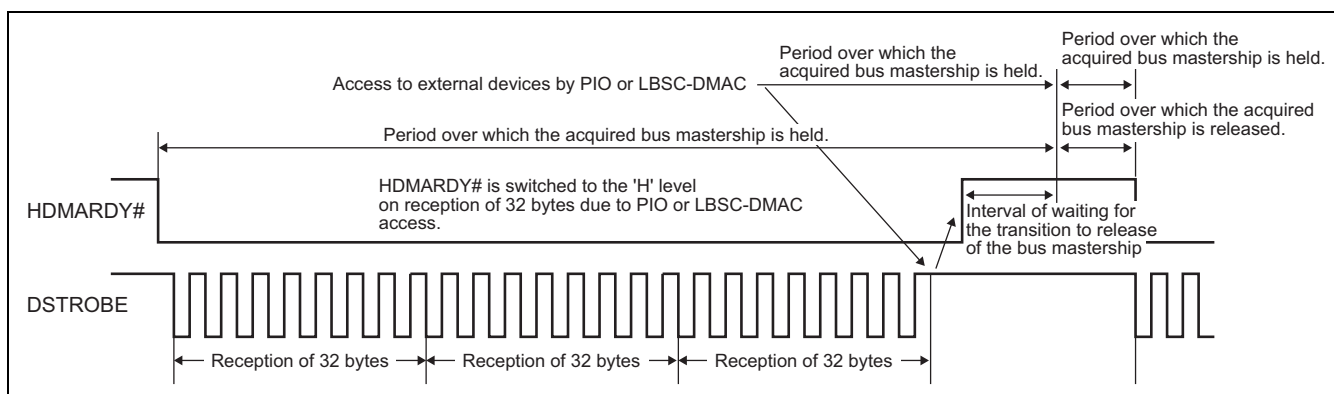
The LBSC and LBSC-DMAC handle Ultra DMA transfer to and from the ATA devices connected to EX-BUS.

Since the EX-BUS is for the connection of multiple external devices, if access to an external device by PIO or the LBSC-DMAC is attempted during Ultra DMA transfer, transfer over the bus is performed while controlling conflict with PIO and LBSC-DMAC access (transfer proceeds through acquisition and release of bus mastership). The operations are thus as described below.

#### (1) Operations for Read Access by Ultra DMA

1. The HDMARDY signal is negated (bus mastership is acquired and released per 32-byte unit of transfer). So that transfer can proceed while controlling conflicts with PIO and LBSC-DMAC access when PIO or LBSC-DMAC access to an external device is attempted, the bus mastership is released (the HDMARDY signal is negated) per 32-byte unit of transfer.

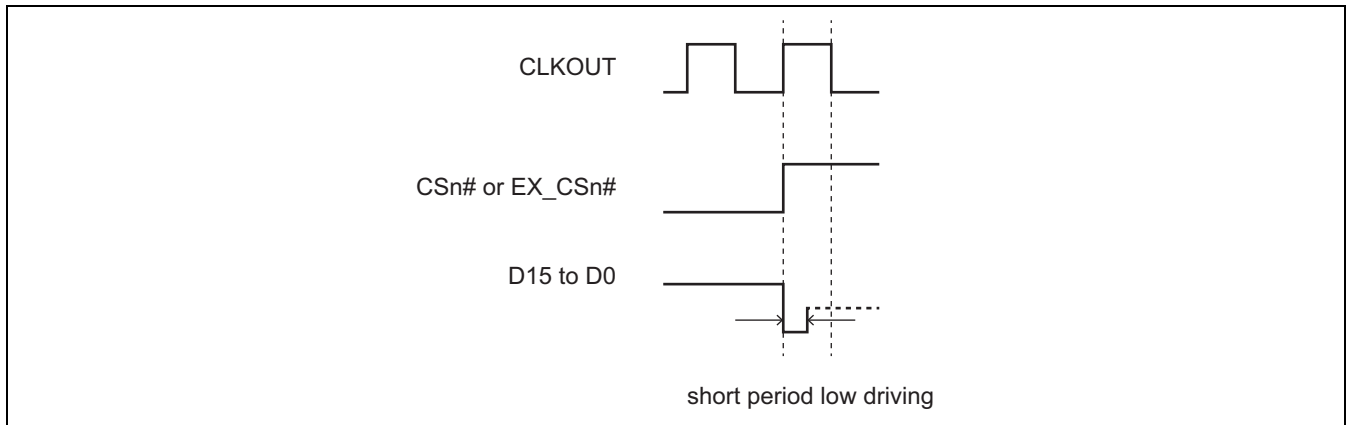
Figure 14.21 shows the operation of the HDMARDY# and DSTROBE signals during operations for read access.



**Figure 14.21 Operation of the HDMARDY# and DSTROBE Signals during Operations for Read Access**

### 14.7.3 Short period low driving at the end of SRAM write access

The external bus is instantaneously driven low at the end of SRAM write access with high write data as shown in Figure 14.22. If the external bus has high load due to system board composition, this short period low driving might cause overshoot on the external bus signals. In designing system board, note that this overshoot might cause voltage level that exceeds the input high voltage.



**Figure 14.22 Short period low driving at the end of SRAM write access**

### 14.7.4 Usage Note

When the QSPI or HSCIF is selected as a boot device by the MD[3:1] settings, the first 256-Kbyte space (H'00 0000 0000 to H'00 0003 FFFF) of the area 0 cannot be accessed from the LBSC even after the LSI is booted up.

## 15. External Bus Controller for DDR3-SDRAM (DBSC3)

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

### 15.1 Overview

The external bus controller for DDR3-SDRAM (DBSC3) supports DDR3-SDRAM and DDR3L-SDRAM\*. The DBSC3 contains bus control, device control, and register control units. The bus control unit receives requests from the bus and issues commands to the device control and register control units. The device control unit reads from and writes to the SDRAM according to the issued commands. Also, the device control unit refreshes the SDRAM. The register control unit reads from and writes to the control registers according to the issued commands.

Note: \* DDR3-SDRAM is supported only for RZ/G1H and RZ/G1E.

DDR3L-SDRAM is supported only for RZ/G1M and RZ/G1N.

#### 15.1.1 Features

The RZ/G1H and RZ/G1M each have two DBSC3 modules (DBSC3\_0 and DBSC3\_1) and determine which to use according to the area being accessed when operating as two independent 32-bit systems. Only DBSC3\_0 is used in operation as a single 64-bit system.

The DBSC3 enables the maximum use of SDRAM bus bandwidth using the following functions:

1. Multibank operation that improves the page hit rate.
2. DDR3-SDRAM operation with burst length 8 that reduces the number of SDRAM command issues.
3. Preceding execution of the bank precharge and activate commands for subsequent requests.

Table 15.1 shows the main functions of the DBSC3.

**Table 15.1 DBSC3 Functions**

Item	Function
Multibank supported	Supports 8-bank multibank operation
Number of banks	Supports eight banks
External bus width	[RZ/G1H and RZ/G1M]: 32 or 64 bits 64-bit bus is supported in 1-ch mode only (can be switched with the mode signal). [RZ/G1N]: 32 bits [RZ/G1E]: 16 or 32 bits
Preceding precharge/activate functions	Determines the content of subsequent requests in a request queue and performs preceding precharge/activate processing for the bank to be accessed during an empty command cycle upon page-miss.
Operating modes	Burst length: 8 (fixed) Burst type: Sequential (fixed) DLL-off mode for the DDR3-SDRAM is not supported.
Power-down mode	Supports self-refresh mode, precharged power-down mode, and active power-down mode. Combined use of the power-down mode and address translation function allows the SDRAM partial array self-refresh function to be effectively implemented.



Item	Function
Address order (address translation function)	<p>The addresses arranged in descending order are: rank address, row address, bank address, and column address.</p> <p>(The 3-bit bank address can be divided into two parts. One can be placed in the upper half of the row address and the other in the lower half. Register settings can be used to determine how to divide the bank address.)</p>
Timing setting	<p>The following timing settings can be specified:</p> <p>CAS latency, CAS write latency, ACT to READ or ACT to WRITE minimum period, PRE period, ACT to ACT or ACT to REF minimum period, ACT to PRE minimum period, ACT(A) to ACT(B) minimum period, four active window minimum period, READ to PRE minimum period, write recovery period, READ to WRITE minimum period, WRITE to READ minimum period, REF to ACT or REF to REF (all banks) minimum period, REF to ACT or REF to REF (per bank) minimum period, minimum period over which CKE is held high, and minimum period over which CKE is held low</p> <p>Only 0 is supported for additive latency (AL).</p>
Refreshes	<p>Average interval and the maximum post count are set by the register. If an empty cycle for request is found, preceding refresh can be performed.</p>
Auto power-down operation	<p>When there is no access for a specified period, power-down mode is automatically entered. The period before power-down mode is entered can be specified through register settings.</p>
ZQ calibration operation	<p>Supports the automatic ZQCS issuing function. After auto-refresh, the ZQCS command is issued to DDR3-SDRAM. The frequency of issuing ZQCS can be specified through register settings in units of the auto-refresh count. The intervals between auto-refresh and ZQCS and between ZQCS and auto-refresh can also be specified through register settings.</p>
PHY interface	<p>[RZ/G1H and RZ/G1M]:</p> <p>1-ch mode: 64-bit bus width 2-ch mode: 32-bit bus width Can be switched with the mode signal.</p> <p>[RZ/G1N]:</p> <p>1-ch mode: 32-bit bus width</p> <p>[RZ/G1E]:</p> <p>1-ch mode: 32-bit bus width 1-ch mode: 16-bit bus width</p>
Memory to be connected	<p>[RZ/G1H and RZ/G1E]:</p> <p>DDR3-SDRAM compliant with JEDEC JESD79-3E. (Supports memory with sizes from 512 Mbits to 8 Gbits. SDRAM with a data bus width of 4 bits is not supported.)</p> <p>[RZ/G1M and RZ/G1N]:</p> <p>DDR3L-SDRAM compliant with JEDEC JESD79-3E. (Supports memory with sizes from 512 Mbits to 8 Gbits. SDRAM with a data bus width of 4 bits is not supported.)</p>
ECC	Not supported.
Parity	Not supported.

### 15.1.2 Definition of Terms and Symbols

The following terms and symbols are used throughout the DBSC3 specifications:

- DDR3-SDRAM and DDR3L-SDRAM are abbreviated as SDRAM in some cases.
- DBSC3\_0 and DBSC3\_1 are collectively called the DBSC3 in some cases.
- "ceil(x)" is the smallest integer which is greater than or equal to real number x.
- "floor(x)" is the greatest integer which is less than or equal to real number x.

Note: DDR3-SDRAM is supported only for RZ/G1H and RZ/G1E.

DDR3L-SDRAM is supported only for RZ/G1M and RZ/G1N.

DBSC3\_1 is supported by RZ/G1H and RZ/G1M only.

15.1.3 Block Diagram

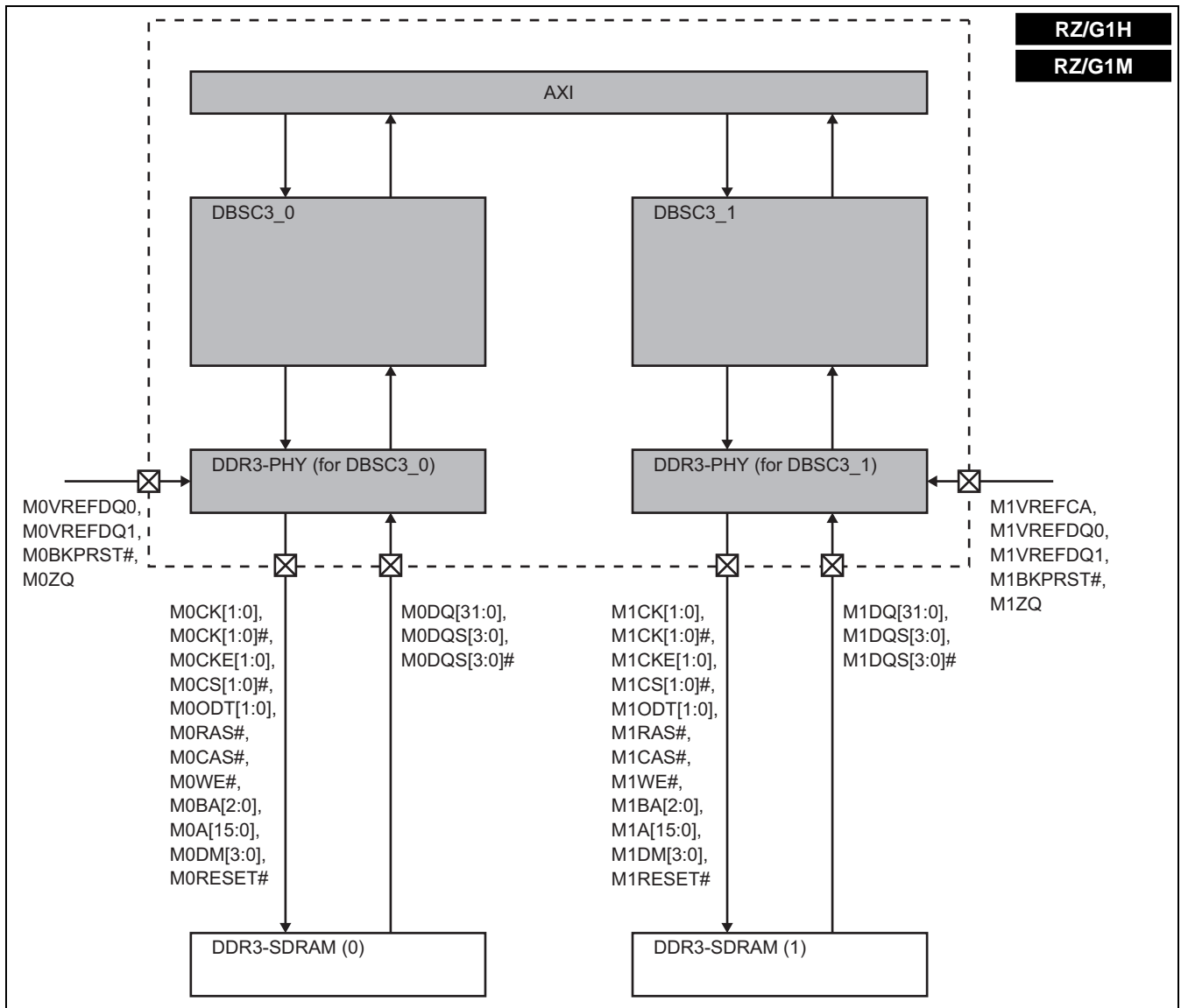


Figure 15.1a Block Diagram of the DBSC3 (for 32-Bit Connection) [RZ/G1H and RZ/G1M]

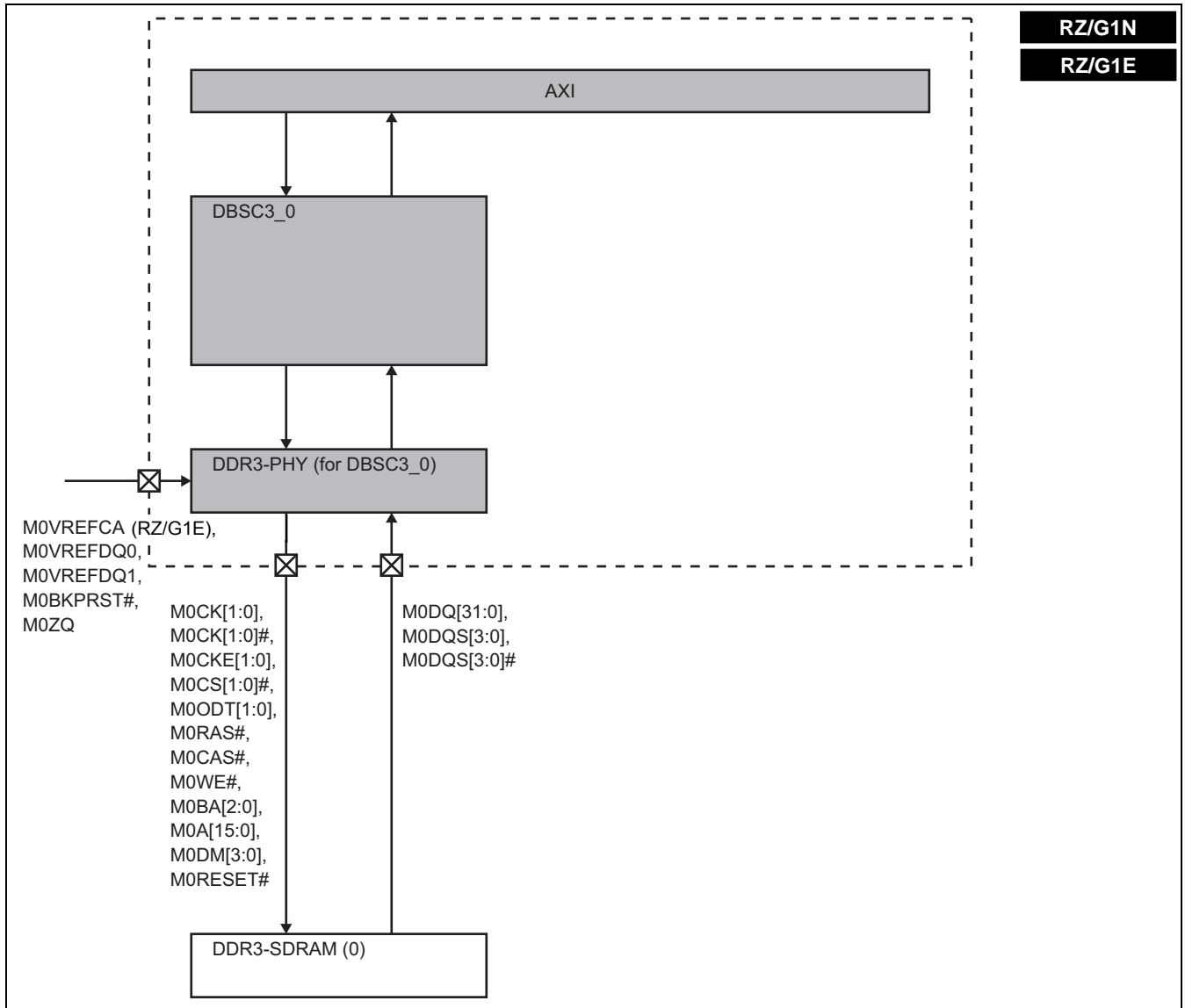


Figure 15.1b Block Diagram of the DBSC3 [RZ/G1N/E]

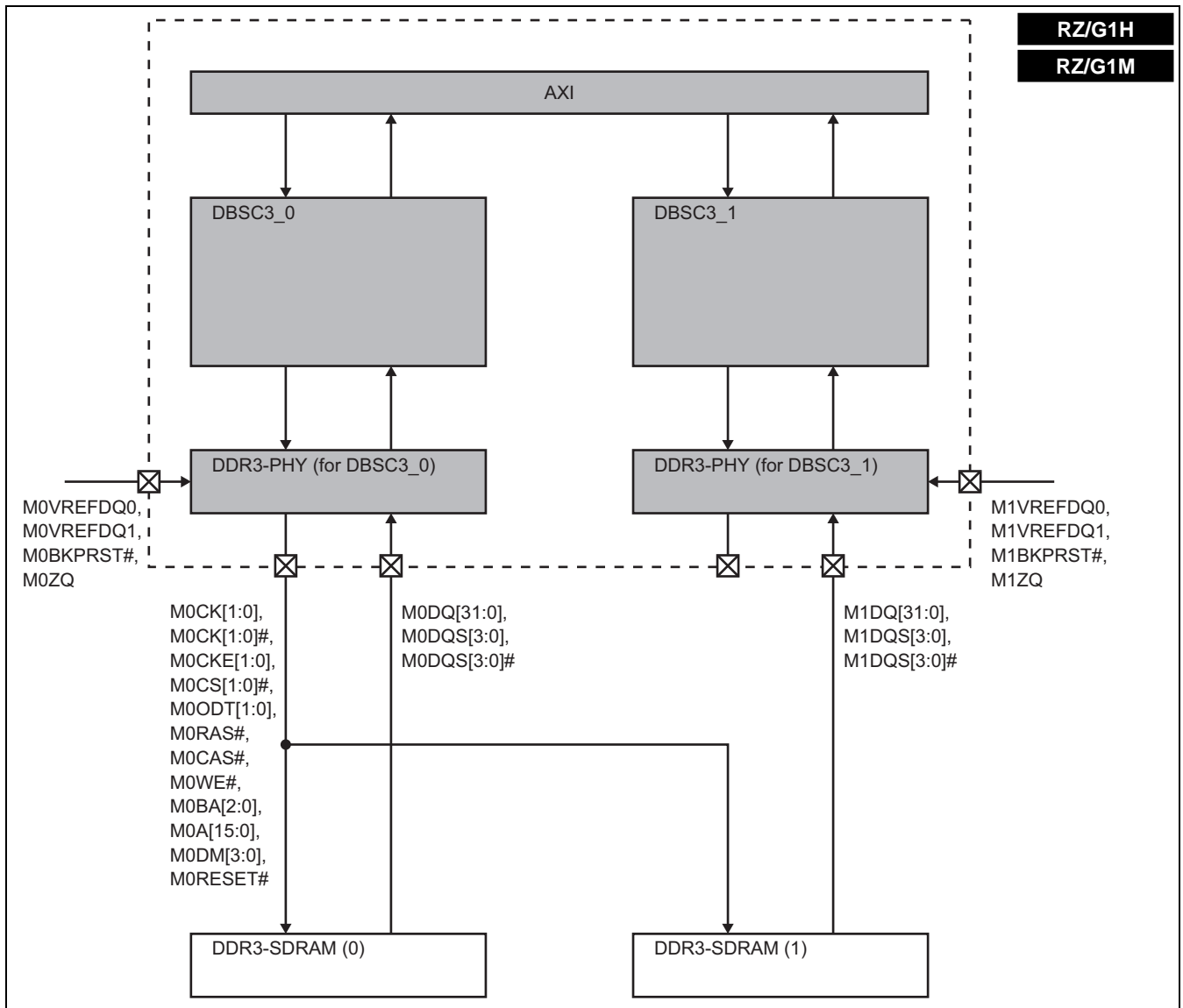


Figure 15.2 Block Diagram of the DBSC3 (for 64-Bit Connection) [RZ/G1H and RZ/G1M]

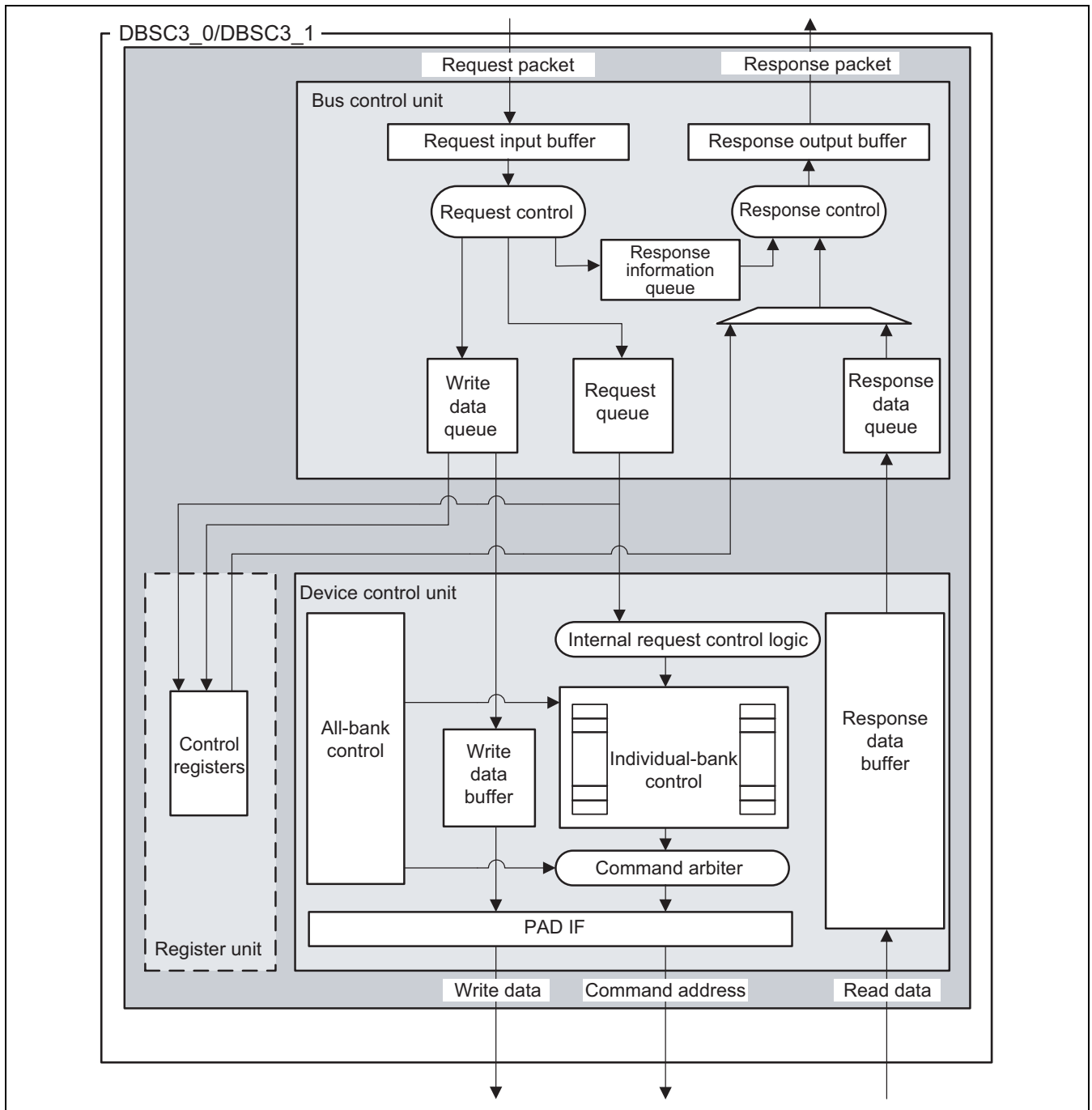


Figure 15.3 Internal Block Diagram of DBSC3\_0/DBSC3\_1

### 15.1.4 Input/Output Pins

Tables 15.2 and 15.3 show the pin configuration of the DBSC3.

**Table 15.2 Pin Configuration of the DBSC3\_0 [RZ/G1H/M/N/E]**

Name	Pin Name	I/O	Function
DDR3-SDRAM clock	M0CK[1:0]	Output	Clock output signals for the DDR3-SDRAM
DDR3-SDRAM clock	M0CK[1:0]#	Output	Clock output signals for the DDR3-SDRAM or M0CK[1:0] inverted clock output signals
Addresses	M0A[15:0]	Output	Address output signals for the DDR3-SDRAM
Bank address	M0BA[2:0]	Output	Bank address output signals
Chip select	M0CS[1:0]#	Output	Chip select output signals
Row address strobe	M0RAS#	Output	Row address strobe output signal
Column address strobe	M0CAS#	Output	Column address strobe output signal
Write enable	M0WE#	Output	Write enable output signal
Clock enable	M0CKE[1:0]	Output	CKE output signals
ODT enable	M0ODT[1:0]	Output	ODT enable output signals in the SDRAM
Power backup reset	M0BKPRST#	Input	Used in power backup mode. When this pin is brought to the low level, M0CKE[1:0] pins are fixed to the low level and M0RESET# pin to the high level.
Reset	M0RESET#	Output	Reset output for the DDR3-SDRAM
Impedance matching	M0ZQ	I/O	Impedance matching Refer to section 15.5.1, Connection of M0ZQ or M1ZQ Pin.
Data mask	M0DM[3:0]	Output	Data mask output signals
I/O data strobe	M0DQS[3:0]	I/O	Data strobe I/O signals
I/O data strobe	M0DQS[3:0]#	I/O	Data strobe I/O signals or M0DQS[3:0] inverted signals
Data	M0DQ[31:0]	I/O	Data I/O signals
Reference voltage input	M0VREFCA	Input	Input reference voltage [RZ/G1E]
Reference voltage input	M0VREFDQ0	Input	Input reference voltage
Reference voltage input	M0VREFDQ1	Input	Input reference voltage

**Table 15.3 Pin Configuration of the DBSC3\_1 [RZ/G1H/M]**

Name	Pin Name	I/O	Function
DDR3-SDRAM clock	M1CK[1:0]	Output	Clock output signals for the DDR3-SDRAM
DDR3-SDRAM clock	M1CK[1:0]#	Output	Clock output signals for the DDR3-SDRAM or M1CK[1:0] inverted clock output signals
Addresses	M1A[15:0]	Output	Address output signals for the DDR3-SDRAM
Bank address	M1BA[2:0]	Output	Bank address output signals
Chip select	M1CS[1:0]#	Output	Chip select output signals
Row address strobe	M1RAS#	Output	Row address strobe output signal
Column address strobe	M1CAS#	Output	Column address strobe output signal
Write enable	M1WE#	Output	Write enable output signal
Clock enable	M1CKE[1:0]	Output	CKE output signals
ODT enable	M1ODT[1:0]	Output	ODT enable output signals in the SDRAM
Power backup reset	M1BKPRST#	Input	Used in power backup mode. When this pin is brought to the low level, M1CKE[1:0] is fixed to the low level and M1RESET# to the high level.
Reset	M1RESET#	Output	Reset output for the DDR3-SDRAM
Impedance matching	M1ZQ	I/O	Impedance matching Refer to section 15.5.1, Connection of M0ZQ or M1ZQ Pin.
Data mask	M1DM[3:0]	Output	Data mask output signals
I/O data strobe	M1DQS[3:0]	I/O	Data strobe I/O signals
I/O data strobe	M1DQS[3:0]#	I/O	Data strobe I/O signals or M1DQS[3:0] inverted signals
Data	M1DQ[31:0]	I/O	Data I/O signals
Reference voltage input	M1VREFCA	Input	Input reference voltage
Reference voltage input	M1VREFDQ0	Input	Input reference voltage
Reference voltage input	M1VREFDQ1	Input	Input reference voltage



## 15.2 Register Configuration

Table 15.4 shows the DBSC3 register mapping, followed by a description of each register. Register addresses are shown in the form of the sum of the DBSC3 register start address (DB\_ADDR for DBSC3\_0 or DBSC3\_1) and an offset (hexadecimal) from that start address.

Registers other than particular ones are initialized by power-on reset.

Access the DBSC3 registers 32 bits at a time. Otherwise, correct operation cannot be guaranteed.

DB\_ADDR (DBSC3\_0) = H'E679 0000 [RZ/G1H/M/N/E]

DB\_ADDR (DBSC3\_1) = H'E67A 0000 [RZ/G1H/M]

**Table 15.4 DBSC3 Register Configuration**

Register Name	Abbreviation	R/W	Address	Initial Value	Access Size (Bits)	RZ/G Series Products			
						RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
DBSC3 status register 1	DBSTATE1	R	DB_ADDR + H'00C	H'000X 0000	32	√	√	√	√
SDRAM access enable register	DBACEN	R/W	DB_ADDR + H'010	H'0000 0000	32	√	√	√	√
Auto-refresh enable register	DBRFEN	R/W	DB_ADDR + H'014	H'0000 0000	32	√	√	√	√
Manual command-issuing register	DBCMD	R/W	DB_ADDR + H'018	H'0000 0000	32	√	√	√	√
Operation completion waiting register	DBWAIT	R	DB_ADDR + H'01C	H'0000 0000	32	√	√	√	√
SDRAM type setting register	DBKIND	R/W	DB_ADDR + H'020	H'0000 0000	32	√	√	√	√
SDRAM configuration setting register 0	DBCONF0	R/W	DB_ADDR + H'024	H'0000 0000	32	√	√	√	√
PHY type setting register	DBPHYTYPE	R/W	DB_ADDR + H'030	H'0000 0000	32	√	√	√	√
SDRAM timing register 0	DBTR0	R/W	DB_ADDR + H'040	H'0000 0000	32	√	√	√	√
SDRAM timing register 1	DBTR1	R/W	DB_ADDR + H'044	H'0000 0000	32	√	√	√	√
SDRAM timing register 2	DBTR2	R/W	DB_ADDR + H'048	H'0000 0000	32	√	√	√	√
SDRAM timing register 3	DBTR3	R/W	DB_ADDR + H'050	H'0000 0000	32	√	√	√	√
SDRAM timing register 4	DBTR4	R/W	DB_ADDR + H'054	H'0000 0000	32	√	√	√	√
SDRAM timing register 5	DBTR5	R/W	DB_ADDR + H'058	H'0000 0000	32	√	√	√	√
SDRAM timing register 6	DBTR6	R/W	DB_ADDR + H'05C	H'0000 0000	32	√	√	√	√
SDRAM timing register 7	DBTR7	R/W	DB_ADDR + H'060	H'0000 0000	32	√	√	√	√
SDRAM timing register 8	DBTR8	R/W	DB_ADDR + H'064	H'0000 0000	32	√	√	√	√
SDRAM timing register 9	DBTR9	R/W	DB_ADDR + H'068	H'0000 0000	32	√	√	√	√
SDRAM timing register 10	DBTR10	R/W	DB_ADDR + H'06C	H'0000 0000	32	√	√	√	√
SDRAM timing register 11	DBTR11	R/W	DB_ADDR + H'070	H'0000 0000	32	√	√	√	√
SDRAM timing register 12	DBTR12	R/W	DB_ADDR + H'074	H'0000 0000	32	√	√	√	√
SDRAM timing register 13	DBTR13	R/W	DB_ADDR + H'078	H'0000 0000	32	√	√	√	√
SDRAM timing register 14	DBTR14	R/W	DB_ADDR + H'07C	H'0000 0000	32	√	√	√	√
SDRAM timing register 15	DBTR15	R/W	DB_ADDR + H'080	H'0000 0000	32	√	√	√	√
SDRAM timing register 16	DBTR16	R/W	DB_ADDR + H'084	H'0000 0000	32	√	√	√	√

Register Name	Abbreviation	R/W	Address	Initial Value	Access Size (Bits)	RZ/G Series Products			
						RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
SDRAM timing register 17	DBTR17	R/W	DB_ADDR + H'088	H'0000 0000	32	√	√	√	√
SDRAM timing register 18	DBTR18	R/W	DB_ADDR + H'08C	H'0000 0000	32	√	√	√	√
SDRAM timing register 19	DBTR19	R/W	DB_ADDR + H'090	H'0000 0000	32	√	√	√	√
SDRAM operation setting register	DBBL	R/W	DB_ADDR + H'0B0	H'0000 0000	32	√	√	√	√
DBSC3 operation adjustment register 0	DBADJ0	R/W	DB_ADDR + H'0C0	H'0000 0000	32	√	√	√	√
DBSC3 operation adjustment register 2	DBADJ2	R/W	DB_ADDR + H'0C8	H'0000 0000	32	√	√	√	√
Refresh configuration register 0	DBRFCNF0	R/W	DB_ADDR + H'0E0	H'0000 0000	32	√	√	√	√
Refresh configuration register 1	DBRFCNF1	R/W	DB_ADDR + H'0E4	H'0000 0000	32	√	√	√	√
Refresh configuration register 2	DBRFCNF2	R/W	DB_ADDR + H'0E8	H'0000 0000	32	√	√	√	√
DDR3-SDRAM calibration configuration register	DBCALCNF	R/W	DB_ADDR + H'0F4	H'0000 0000	32	√	√	√	√
DDR3-SDRAM calibration timing register	DBCALTR	R/W	DB_ADDR + H'0F8	H'0000 0000	32	√	√	√	√
ODT operation setting register	DBRNK0	R/W	DB_ADDR + H'100	H'0000 0000	32	√	√	√	√
Power-down configuration register	DBPDNCNF	R/W	DB_ADDR + H'180	H'0000 0000	32	√	√	√	√
DFI status IF input register	DBDFISTAT	R	DB_ADDR + H'240	H'0000 0000	32	√	√	√	√
DFI status IF output register	DBDFICNT	R/W	DB_ADDR + H'244	H'0000 0000	32	√	√	√	√
PHY unit lock register	DBPDLCK	R/W	DB_ADDR + H'280	H'0000 0000	32	√	√	√	√
PHY unit address register	DBPDRGA	R/W	DB_ADDR + H'290	H'0000 0000	32	√	√	√	√
PHY unit access register	DBPDRGD	R/W	DB_ADDR + H'2A0	H'XXXX XXXX	32	√	√	√	√
Bus control unit 0 control register 1	DBBS0CNT1	R/W	DB_ADDR + H'304	H'0000 0000	32	√	√	√	√
AXI port setting register 0	DBWT0CNF0	R/W	DB_ADDR + H'380	H'0000 0000	32	√	√	√	√
AXI port setting register 4	DBWT0CNF4	R/W	DB_ADDR + H'390	H'0000 0000	32	√	√	√	√
Scheduler setting register 0	DBSCHECNT0	R/W	DB_ADDR + H'500	H'0000 0000	32	√	√	√	√

Note: Do not write to addresses other than the listed above. Otherwise, correct operation is not guaranteed.

### 15.3 Register Descriptions

The legends used in register descriptions have the following meanings.

Initial value: Register value after a reset

—: Undefined value

R/W: Readable/writable. The written value can be read.

R: Read-only. The write value should always be 0.

R/WC0: Readable/writable. Writing 0 initializes the bit. Writing 1 is ignored.

R/WC1: Readable/writable. Writing 1 initializes the bit. Writing 0 is ignored.

W: Write-only. Reading this bit is prohibited. When the bit is reserved, the write value should always be 0.

—/W: Write-only. The read value is undefined.

All access to registers is made in longword units.

Write 0 to the reserved bits.

**15.3.1 DBSC3 Status Register 1 (DBSTATE1)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RFU	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 18	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
17, 16	RFU	Undefined	R	Reserved
15 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.

**15.3.2 SDRAM Access Enable Register (DBACEN)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ACCEN
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
0	ACCEN	0	R/W	SDRAM Access Enable Bit This bit enables data access to the SDRAM. Make data access to the SDRAM after setting this bit to 1. When this bit is 0, do not access the SDRAM area. 0: Disables access to the SDRAM. 1: Enables access to the SDRAM.

Note: When making the setting to disable access (writing 0 to this register), a precharge all or precharge command for the SDRAM may be issued automatically.

**15.3.3 Auto-Refresh Enable Register (DBRFEN)**

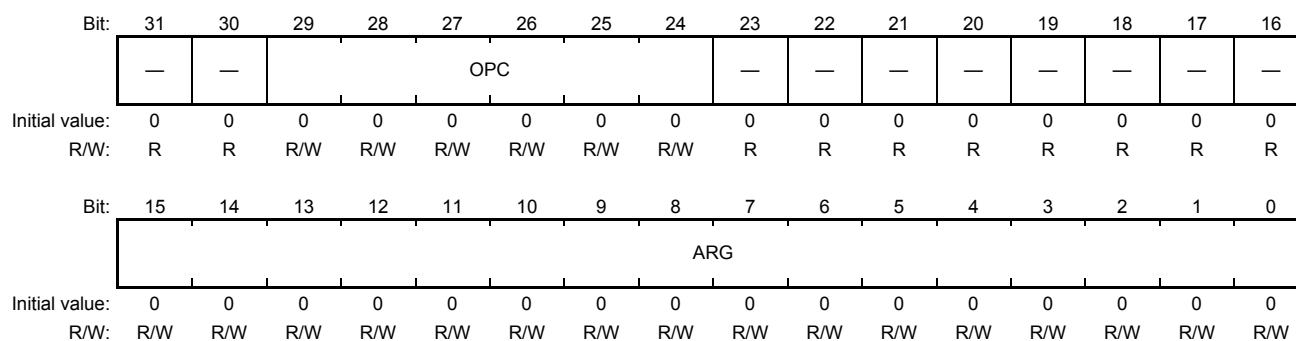
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ARFEN
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
0	ARFEN	0	R/W	Auto-Refresh Enable Bit This bit starts or stops the auto-refresh function. Writing 1 to this bit resets the refresh counter (refresh history) in the DBSC3 and starts the auto-refresh function. While this bit is 1, the DBSC3 issues a refresh command at regular intervals. The refresh cycle time and other settings depend on the values held in the refresh configuration registers 0 to 2 (DBRFCNF0 to DBRFCNF2) when 1 is written to this bit. 0: Stops the auto-refresh function. 1: Starts the auto-refresh function.

### 15.3.4 Manual Command-Issuing Register (DBCMD)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√



Bit	Bit Name	Initial Value	R/W	Description
31, 30	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
29 to 24	OPC	000000	R/W	Operation Code Bits Specify the type of command to be issued. Refer to Table 15.5. If Wait is specified through these bits, valid SDRAM commands are not output and no processing is performed except reserving the time until the next operation. These bits are read as undefined values.
23 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
15 to 0	ARG	H'0000	R/W	Parameter Bits The meaning can differ according to the operation code indicated by the OPC bits. When OPC indicates Mode Register Set (MRS0 to MRS3), the ARG bits specify the value to be issued on the address pins (MA) of SDRAM. When OPC is any other value, the ARG bits specify the minimum interval to issuing of the next command in SDRAM cycles. When ARG = 0, however, the values default to those given in "Interval" column of Table 15.5. These bits are read as undefined values.

The manual command-issuing register (DBCMD) is used to issue the required commands for the sequence of initializing the SDRAM and of transitions to and from the self-refresh mode. The command corresponding to the OPC bits is issued once as a result of writing to this register. For instance, issuing the refresh command twice requires that "001100" be written to the OPC bits twice. Do not write to this register while access to the SDRAM is enabled (ACCEN = 1 in the DBACEN register). The timing with which an operation is complete (i.e. the timing with which the specified SDRAM command is output to the PHY unit from DBSC3) may be later than the response of DBSC3 to writing to this register. If you wish to wait until actual output of the specified SDRAM command to SDRAM; do this by reading the DBWAIT register (described later).

When this register is used to issue a command, the issuing of a subsequent SDRAM command is delayed by a certain period of time from the moment at which each operation is completed (i.e. from the time when the specified SDRAM

command is output to SDRAM). This facilitates securing of the required amounts of time between commands in the issuing of multiple consecutive commands.

These periods are given in the "Interval" column of Table 15.5. They can also be customized by using the ARG bits (except in cases where the OPC bits indicate MRS0 to MRS3).

**Table 15.5 Manual Command Issue Functions**

OPC	Code	Operation	Interval (Number of SDRAM Cycles)	ARG Function	
00 0000	Wait	Issue "Device Deselected" (and insert wait cycles)	4	Customizing the interval (for ARG = 0, the value is that given at left)	
00 0010	ZQCS	Issue "ZQ Calibration Short"	4		
00 0011	ZQCL	Issue "ZQ Calibration Long"	4		
00 1011	PREA	Issue "Precharge All"	TRPA		
00 1100	Ref	Issue "Refresh"	TRFC		
01 0000	PDEn	Power Down Entry	4		
01 0001	PDXt	Power Down Exit	4		
01 1000	SREn	Self-Refresh Entry	4		
01 1001	SRXt	Self-Refresh Exit	TRFC		
10 0000	RstL	Set Reset Pins to Low	4		
10 0001	RstH	Set Reset Pins to High	4		
10 1000	MRS0	Issue "ModeRegisterSet" (for MRS/MR0)"	TMOD		Specifying the setting for SDRAM mode register
10 1001	MRS1	Issue "ModeRegisterSet" (for EMRS1/MR1)	TMOD		
10 1010	MRS2	Issue "ModeRegisterSet" (for EMRS2/MR2)	TMOD		
10 1011	MRS3	Issue "ModeRegisterSet" (for EMRS3/MR3)	TMOD		

- Notes:
1. TRPA, TRFC, and TMOD in the "Interval" column of the above table indicate timing registers. The intervals in these cases are determined by the corresponding register settings.
  2. Only write to this register after having disabled SDRAM access (i.e. the ACCEN bit in the DBACEN register = 0).
  3. Only write to this register after having stopped the auto-refresh function (i.e. the ARFEN bit in the DBRFEN register = 0). However, sequences described in section 15.4, Operation, are not limited to these. If Wait is specified in the OPC bits in this register during auto-refresh operations, the auto-refresh function may issue a refresh command during the time secured for the Wait command.



### 15.3.5 Operation Completion Waiting Register (DBWAIT)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	WAIT
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
0	WAIT	0	R	Operation Completion Waiting Bit This value is meaningless. This bit is always read as 0.

When this register is read, a response is returned after all command issuing that has been specified by using the DBCMD register by that time is completed (i.e., after command output from the DBSC3 to the PHY unit).

This register can be used to guarantee correctness for the relationship between the timing with which SDRAM commands are issued by DBSC3 and timing that is not managed by DBSC3 (e.g. clock control).

### 15.3.6 SDRAM Type Setting Register (DBKIND)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	DDCG		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
2 to 0	DDCG	000	R/W	SDRAM Type Bits These bits can set the type of SDRAM. 111: DDR3-SDRAM Other settings are prohibited.

- Notes:
1. This register must only be written from within the initialization sequence (see section 15.4.3, Initialization Sequence).
  2. Writing to this register should only be performed when the following conditions are met.
    - Access to SDRAM is disabled (i.e. the ACCEN bit in the DBACEN register is 0)
    - Auto-refresh is disabled (i.e. the ARFEN bit in the DBRFEN register is 0)
  3. Set the defined value in each group.
  4. Specify the same SDRAM type as the SDRAM specified at power-on.

### 15.3.7 SDRAM Configuration Setting Register 0 (DBCONF0)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	AWRW0				—	—	—	AWRK0	—	—	AWBK0		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R	R	R	R/W	R	R	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	AWCL0				—	—	—	—	—	—	DW0	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
28 to 24	AWRW0	00000	R/W	Row Address Bit Width Setting Bits These bits specify the width, in bits, of row addresses. 01100: 12 bits : 10000: 16 bits Other settings are prohibited.
23 to 21	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
20	AWRK0	0	R/W	Number of Ranks Setting Bits These bits specify the number of ranks. 0: One rank 1: Setting prohibited
19, 18	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
17, 16	AWBK0	00	R/W	Number of Banks Setting Bits These bits specify the number of banks. 11: Eight banks Other settings are prohibited.
15 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.

Bit	Bit Name	Initial Value	R/W	Description
11 to 8	AWCL0	0000	R/W	Column Address Bit Width Setting Bits These bits specify the width, in bits, of column addresses. 1010: 10 bits 1011: 11 bits Other settings are prohibited.
7 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
1, 0	DW0	00	R/W	External Data Bus Width Setting Bits These bits specify the width of the external bus. 01: 16 bits (for 1-ch mode only) 10: 32 bits (for 1ch, 2ch mode) Other settings are prohibited.

This register sets the memory configuration to be used.

Refer to section 15.4.11, Setting the SDRAM Configuration Setting Register, for details on the memory configurations supported by DBSC3. For details on the relationship between the chip select and address pins of the SDRAM and the logical addresses of this LSI, refer to section 15.4.12, Address Multiplexing.

Notes: 1. Memory Configuration Supported

- 32-bit bus configuration connected with two 16-bit wide SDRAM modules or four 8-bit wide SDRAM modules
2. Although DBSC3 supports the connection of multiple SDRAM modules, the electrical characteristics of some chips may impose a limitation on the number of connectable SDRAM modules.
  3. This register must only be written from within the initialization sequence (see section 15.4.3, Initialization Sequence).
  4. Writing to this register should only be performed when the following conditions are met:
    - Access to SDRAM is disabled (i.e. the ACCEN bit in the DBACEN register is 0)
    - Auto-refresh is disabled (i.e. the ARFEN bit in the DBRFEN register is 0)
  5. Specify predetermined bit values based on the product type.

**15.3.8 PHY Type Setting Register (DBPHYTYPE)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PHYTYPE	PHYTYPE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
1, 0	PHYTYPE	00	R/W	PHY Type Setting Bits 01: DFI Other settings are prohibited.

- Notes:
- This register must only be written from within the initialization sequence (see section 15.4.3, Initialization Sequence).
  - Writing to this register should only be performed when the following conditions are met.
    - Access to SDRAM is disabled (i.e. the ACCEN bit in the DBACEN register is 0)
    - Auto-refresh is disabled (i.e. the ARFEN bit in the DBRFEN register is 0)

**15.3.9 SDRAM Timing Register 0 (DBTR0)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	CL			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
3 to 0	CL	0000	R/W	CAS Latency Setting Bits These bits are for setting the CAS latency of the SDRAM. 0011: 3 cycles : 1110: 14 cycles Other settings are prohibited.

DBTR0 is used to set a timing parameter for the SDRAM.

- Notes:
- The setting is in cycles of the SDRAM operating clock.
  - Writing to this register should only be performed when the following conditions are met.
    - Access to SDRAM is disabled (i.e. the ACCEN bit in the DBACEN register is 0)
    - Auto-refresh is disabled (i.e. the ARFEN bit in the DBRFEN register is 0)

**15.3.10 SDRAM Timing Register 1 (DBTR1)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	CWL			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
3 to 0	CWL	0000	R/W	CAS Write Latency Setting Bits These bits are for setting the CAS-write latency of the SDRAM. 0010: 2 cycle : 1010: 10 cycles Other settings are prohibited.

DBTR1 is used to set a timing parameter for the SDRAM.

- Notes:
- The setting is in cycles of the SDRAM operating clock.
  - Writing to this register should only be performed when the following conditions are met.
    - Access to SDRAM is disabled (i.e. the ACCEN bit in the DBACEN register is 0)
    - Auto-refresh is disabled (i.e. the ARFEN bit in the DBRFEN register is 0)

### 15.3.11 SDRAM Timing Register 2 (DBTR2)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	AL			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
3 to 0	AL	0000	R/W	Additive Latency Setting Bits These bits are for setting the additive latency of the SDRAM. 0000: 0 cycles Other settings are prohibited.

DBTR2 is used to set a timing parameter for the SDRAM.

Notes: 1. The setting is in cycles of the SDRAM operating clock.

2. Writing to this register should only be performed when the following conditions are met.

- Access to SDRAM is disabled (i.e. the ACCEN bit in the DBACEN register is 0)
- Auto-refresh is disabled (i.e. the ARFEN bit in the DBRFEN register is 0)



**15.3.12 SDRAM Timing Register 3 (DBTR3)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	TRCD				
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
4 to 0	TRCD	00000	R/W	ACT to READ/ACT to WRITE Interval Setting Bits These bits set the minimum interval from an ACT command to a READ/WRITE command. 00011: 3 cycles : 11111: 31 cycles Other settings are prohibited.

DBTR3 is used to set a timing parameter for the SDRAM.

- Notes:
- The setting is in cycles of the SDRAM operating clock.
  - Writing to this register should only be performed when the following conditions are met.
    - Access to SDRAM is disabled (i.e. the ACCEN bit in the DBACEN register is 0)
    - Auto-refresh is disabled (i.e. the ARFEN bit in the DBRFEN register is 0)

### 15.3.13 SDRAM Timing Register 4 (DBTR4)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	TRPA				
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	TRP				
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 21	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
20 to 16	TRPA	00000	R/W	PREA Time Setting Bits These bits set the minimum interval from a PREA (precharge all banks) command to an ACT/REF command. The value set in these bits must be greater than or equal to that in the TRP bits. 00011: 3 cycles : 11111: 31 cycles Other settings are prohibited.
15 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
4 to 0	TRP	00000	R/W	PRE Time Setting Bits These bits set the minimum interval from a PRE (precharge) command to an ACT/REF command. 00011: 3 cycles : 11111: 31 cycles Other settings are prohibited.

DBTR4 is used to set timing parameters for the SDRAM.

- Notes:
- The setting is in cycles of the SDRAM operating clock.
  - The following conditions must be satisfied:
    - $TRPA \geq TRP$
    - $TRC - TRP < 32$
  - Writing to this register should only be performed when the following conditions are met.
    - Access to SDRAM is disabled (i.e. the ACCEN bit in the DBACEN register is 0)
    - Auto-refresh is disabled (i.e. the ARFEN bit in the DBRFEN register is 0)

**15.3.14 SDRAM Timing Register 5 (DBTR5)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	TRC					
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
5 to 0	TRC	000000	R/W	ACT to ACT/ACT to REF Interval Setting Bits These bits set the minimum interval from one ACT command to another ACT command (for the same bank) or to a REF command. 000110: 6 cycles : 111111: 63 cycles Other settings are prohibited.

DBTR5 is used to set a timing parameter for the SDRAM.

- Notes:
- The setting is in cycles of the SDRAM operating clock.
  - The following condition must be satisfied: TRC – TRP < 32
  - Writing to this register should only be performed when the following conditions are met.
    - Access to SDRAM is disabled (i.e. the ACCEN bit in the DBACEN register is 0)
    - Auto-refresh is disabled (i.e. the ARFEN bit in the DBRFEN register is 0)

**15.3.15 SDRAM Timing Register 6 (DBTR6)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	TRAS					
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
5 to 0	TRAS	000000	R/W	ACT to PRE Interval Setting Bits These bits set the minimum interval from an ACT command to a PRE command. 000011: 3 cycles : 100010: 34 cycles Other settings are prohibited.

DBTR6 is used to set a timing parameter for the SDRAM.

- Notes:
- The setting is in cycles of the SDRAM operating clock.
  - Writing to this register should only be performed when the following conditions are met.
    - Access to SDRAM is disabled (i.e. the ACCEN bit in the DBACEN register is 0)
    - Auto-refresh is disabled (i.e. the ARFEN bit in the DBRFEN register is 0)

**15.3.16 SDRAM Timing Register 7 (DBTR7)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	TRRD			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
3 to 0	TRRD	0000	R/W	ACT(A) to ACT(B) Interval Setting Bits These bits set the minimum interval between ACT commands issued for different banks. 0010: 2 cycles : 1111: 15 cycles Other settings are prohibited.

DBTR7 is used to set a timing parameter for the SDRAM.

- Notes:
- The setting is in cycles of the SDRAM operating clock.
  - Writing to this register should only be performed when the following conditions are met.
    - Access to SDRAM is disabled (i.e. the ACCEN bit in the DBACEN register is 0)
    - Auto-refresh is disabled (i.e. the ARFEN bit in the DBRFEN register is 0)

**15.3.17 SDRAM Timing Register 8 (DBTR8)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	TFAW							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
7 to 0	TFAW	00000000	R/W	Four Activate Window Length Setting Bits These bits set the length of the four activate window. The value of these bits must be at least four times as large as that of the TRRD bits in DBTR7. 00001000: 8 cycles : 00111111: 63 cycles Other settings are prohibited.

DBTR8 is used to set a timing parameter for the SDRAM.

- Notes:
- The setting is in cycles of the SDRAM operating clock.
  - The following condition must be satisfied:  $TFAW \geq 4 \times TRRD$ .
  - Writing to this register should only be performed when the following conditions are met.
    - Access to SDRAM is disabled (i.e. the ACCEN bit in the DBACEN register is 0)
    - Auto-refresh is disabled (i.e. the ARFEN bit in the DBRFEN register is 0)

**15.3.18 SDRAM Timing Register 9 (DBTR9)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	TRDPR			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
3 to 0	TRDPR	0000	R/W	READ-PRE Interval Setting Bits These bits set the minimum interval from a READ command to a PRE command. 0100: 4 cycles : 1111: 15 cycles Other settings are prohibited.

DBTR9 is used to set a timing parameter for the SDRAM.

- Notes:
- The setting is in cycles of the SDRAM operating clock.
  - The following condition must be satisfied:  $TRDPR \geq BL/2$ .
  - If the SDRAM in use conforms to the JEDEC standard, the value of the bits can be calculated from the following formula.  

$$TRDPR = \max \{4, \text{ceil}(tRTP / tCK)\}$$
  - Writing to this register should only be performed when the following conditions are met.
    - Access to SDRAM is disabled (i.e. the ACCEN bit in the DBACEN register is 0)
    - Auto-refresh is disabled (i.e. the ARFEN bit in the DBRFEN register is 0)

**15.3.19 SDRAM Timing Register 10 (DBTR10)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	TWR			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
3 to 0	TWR	0000	R/W	Write-Recovery Period Setting Bits These bits set the write-recovery period. 0011: 3 cycles 0100: 4 cycles : 1110: 14 cycles Other settings are prohibited.

DBTR10 is used to set a timing parameter for the SDRAM.

- Notes:
- The setting is in cycles of the SDRAM operating clock.
  - Writing to this register should only be performed when the following conditions are met.
    - Access to SDRAM is disabled (i.e. the ACCEN bit in the DBACEN register is 0)
    - Auto-refresh is disabled (i.e. the ARFEN bit in the DBRFEN register is 0)



### 15.3.20 SDRAM Timing Register 11 (DBTR11)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	TRDWR					
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
5 to 0	TRDWR	000000	R/W	READ to WRITE Interval Setting Bits These bits set the minimum interval from a READ command to a WRITE command. 000110: 6 cycles 000111: 7 cycles : 001111: 15 cycles Other settings are prohibited.

DBTR11 is used to set a timing parameter for the SDRAM.

- Notes:
- The setting is in cycles of the SDRAM operating clock.
  - If the SDRAM in use conforms to the JEDEC standard, the value of the bits can be calculated from the following formula.

When the number of  $(CL + (BL/2) + 2 - CWL)$  is even:

$$TRDWR > CL + (BL/2) + 2 - CWL$$

Otherwise:

$$TRDWR \geq CL + (BL/2) + 2 - CWL$$

- Writing to this register should only be performed when the following conditions are met.
  - Access to SDRAM is disabled (i.e. the ACCEN bit in the DBACEN register is 0)
  - Auto-refresh is disabled (i.e. the ARFEN bit in the DBRFEN register is 0)

**15.3.21 SDRAM Timing Register 12 (DBTR12)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	TWRRD					
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
5 to 0	TWRRD	000000	R/W	WRITE to READ Interval Setting Bits These bits set the minimum interval from a WRITE command to a READ command. 000110: 6 cycles : 011111: 31 cycles Other settings are prohibited.

DBTR12 is used to set a timing parameter for the SDRAM.

- Notes:
- The setting is in cycles of the SDRAM operating clock.
  - The following condition must be satisfied:  $TWRRD \geq CWL + BL/2$ .
  - If the SDRAM in use conforms to the JEDEC standard, the value of the bits can be calculated from the following formula.  

$$TWRRD = CWL + 4 + \text{ceil}(tWTR / tCK)$$
  - Writing to this register should only be performed when the following conditions are met.
    - Access to SDRAM is disabled (i.e. the ACCEN bit in the DBACEN register is 0)
    - Auto-refresh is disabled (i.e. the ARFEN bit in the DBRFEN register is 0)

**15.3.22 SDRAM Timing Register 13 (DBTR13)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	TRFC/TRFCAB											
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
11 to 0	TRFC/TRFCAB	H'000	R/W	REF to ACT/REF or All Bank REF to ACT/REF Interval Setting Bits These bits set the minimum interval from a REF (refresh) command for all the banks to an ACT/REF command. H'008 : 8 cycles : H'1FF: 511 cycles Other settings are prohibited.

DBTR13 is used to set a timing parameter for the SDRAM.

- Notes:
- The setting is in cycles of the SDRAM operating clock.
  - Writing to this register should only be performed when the following conditions are met.
    - Access to SDRAM is disabled (i.e. the ACCEN bit in the DBACEN register is 0)
    - Auto-refresh is disabled (i.e. the ARFEN bit in the DBRFEN register is 0)

### 15.3.23 SDRAM Timing Register 14 (DBTR14)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	TCKEHDLL							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	TCKEH							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
23 to 16	TCKEHDLL	H'00	R/W	CKEH (DLL-LOCK) Period Setting Bits These bits set the minimum interval from the time the CKE signal goes high until the issuing of a further valid command that requires the DLL to be locked. H'02: 2 cycles : H'17: 23 cycles Other settings are prohibited.
15 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
7 to 0	TCKEH	H'00	R/W	CKEH Period Setting Bits These bits set the minimum interval from the time the CKE signal goes high until the issuing of a further valid command. H'02: 2 cycles : H'0F: 15 cycles Other settings are prohibited.

DBTR14 is used to set timing parameters for the SDRAM.

- Notes:
- The setting is in cycles of the SDRAM operating clock.
  - The following condition must be satisfied:  $TCKEH \leq TCKEHDLL$ .
  - When the power-down mode is to be used, this register must be set accordingly.  
If the SDRAM in use conforms to the JEDEC standard, the value of the bits can be calculated from the following formula.  

$$TCKEHDLL = \text{ceil}(tXPDLL / tCK)$$

$$TCKEH = \text{ceil}(tXP / tCK)$$

4. Writing to this register should only be performed when the following conditions are met.
  - Access to SDRAM is disabled (i.e. the ACCEN bit in the DBACEN register is 0)
  - Auto-refresh is disabled (i.e. the ARFEN bit in the DBRFEN register is 0)

### 15.3.24 SDRAM Timing Register 15 (DBTR15)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	TCKESR			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	TCKEL			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 20	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
19 to 16	TCKESR	0000	R/W	CKESR Period Setting Bits These bits set the minimum time for self-refresh from the time the CKE signal goes low until it goes high. 0010: 2 cycles 0011: 3 cycles : 1111: 15 cycles Other settings are prohibited.
15 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
3 to 0	TCKEL	0000	R/W	CKEL Period Setting Bits These bits set the minimum time for power down from the time the CKE signal goes low until it goes high. 0010: 2 cycles 0011: 3 cycles : 1111: 15 cycles Other settings are prohibited.

DBTR15 is used to set a timing parameter for the SDRAM.

- Notes:
- The setting is in cycles of the SDRAM operating clock.
  - Writing to this register should only be performed when the following conditions are met.
    - Access to SDRAM is disabled (i.e. the ACCEN bit in the DBACEN register is 0)
    - Auto-refresh is disabled (i.e. the ARFEN bit in the DBRFEN register is 0)

## 15.3.25 SDRAM Timing Register 16 (DBTR16)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DQIENLTNCY				—	—	—	—	—	—	DQL					
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DQENLTNCY				—	—	—	—	—	—	—	—	WDQL			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 28	DQIENLTNCY	0000	R/W	<p>dqientlncy Setting Bits</p> <p>These bits set the latency from issuing of a read command to the PHY unit until the dfi_rddata_en signal is output. Set CL - 4 when CL is odd and CL - 5 when CL is even.</p> <p>0010: 2 cycles</p> <p>:</p> <p>1011: 11 cycles</p> <p>Other settings are prohibited.</p>
27 to 22	—	All 0	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p> <p>If a value other than 0 is written, correct operation cannot be guaranteed.</p>
21 to 16	DQL	000000	R/W	<p>dqltncy Setting Bits</p> <p>These bits set the latency from issuing of a read command to the PHY unit until the read data is returned from the PHY unit. Set DQIENLTNCY + 28.</p> <p>000111: 7 cycles</p> <p>:</p> <p>111111: 63 cycles</p> <p>Other settings are prohibited.</p>
15 to 12	DQENLTNCY	0000	R/W	<p>dqenlncy Setting Bits</p> <p>These bits set the latency from issuing of a write command to the PHY unit until the dfi_wrdata_en signal is output. Set CWL - 4 when CWL is odd and CWL - 5 when CWL is even.</p> <p>0000: 0 cycles</p> <p>:</p> <p>0101: 5 cycles</p> <p>Other settings are prohibited.</p>
11 to 4	—	All 0	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p> <p>If a value other than 0 is written, correct operation cannot be guaranteed.</p>

Bit	Bit Name	Initial Value	R/W	Description
3 to 0	WDQL	0000	R/W	<p>wdqItncy Setting Bits</p> <p>These bits set the latency from issuing of a write command until the write data is output. Set DQENLTNCY + 2.</p> <p>0001: One cycle</p> <p>:</p> <p>1000: 8 cycles</p> <p>Other settings are prohibited.</p>

DBTR16 is used to set a timing parameter for the SDRAM.

- Notes:
- The setting is in cycles of the SDRAM operating clock.
  - Writing to this register should only be performed when the following conditions are met.
    - Access to SDRAM is disabled (i.e. the ACCEN bit in the DBACEN register is 0)
    - Auto-refresh is disabled (i.e. the ARFEN bit in the DBRFEN register is 0)



**15.3.26 SDRAM Timing Register 17 (DBTR17)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	TMOD					
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 22	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
21 to 16	TMOD	000000	R/W	MRS Time Setting Bits These bits indicate the minimum interval from an MRS (mode register set) command to a subsequent command. 000010: 2 cycles : 001111: 15 cycles Other settings are prohibited.
15 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.

DBTR17 is used to set timing parameters for the SDRAM.

- Notes:
- The setting is in cycles of the SDRAM operating clock.
  - Writing to this register should only be performed when the following conditions are met.
    - Access to SDRAM is disabled (i.e. the ACCEN bit in the DBACEN register is 0)
    - Auto-refresh is disabled (i.e. the ARFEN bit in the DBRFEN register is 0)

## 15.3.27 SDRAM Timing Register 18 (DBTR18)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	RODTL			—	—	—	—	—	RODTA		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W	R	R	R	R	R	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	WODTL			—	—	—	—	—	WODTA		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W	R	R	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 27	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
26 to 24	RODTL	000	R/W	Bits for ODT Assert Period Setting at Read These bits set the assert period of the ODT signal that is output when a read command is output. 000: BL/2 cycles 001: BL/2 + 1 cycle : 111: BL/2 + 7 cycles Other settings are prohibited.
23 to 19	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
18 to 16	RODTA	000	R/W	Bits for ODT Assert Start Timing Setting Bits Read These bits set the assert start timing for the ODT signal that is output when a read command is output. 000: Simultaneous with the read command 001: One cycle after the read command 010: Two cycles after the read command 011: Three cycles after the read command Other settings are prohibited.
15 to 11	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.

Bit	Bit Name	Initial Value	R/W	Description
10 to 8	WODTL	000	R/W	<p>Bits for ODT Assert Period Setting at Write</p> <p>These bits set the assert period of the ODT signal that is output when a write command is output.</p> <p>000: BL/2 cycles            001: BL/2 cycles + 1 cycle            :            111: BL/2 cycles + 7 cycles            Other settings are prohibited.</p>
7 to 3	—	All 0	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p> <p>If a value other than 0 is written, correct operation cannot be guaranteed.</p>
2 to 0	WODTA	000	R/W	<p>Bits for ODT Assert Start Timing Setting at Write</p> <p>These bits set the assert start timing for the ODT signal that is output when a write command is output.</p> <p>000: Simultaneous with the write command            001: One cycle after the write command            010: Two cycles after the write command            011: Three cycles after the write command            Other settings are prohibited.</p>

DBTR18 is used to set timing parameters for the SDRAM.

- Notes:
- The setting is in cycles of the SDRAM operating clock.
  - Writing to this register should only be performed when the following conditions are met.
    - Access to SDRAM is disabled (i.e. the ACCEN bit in the DBACEN register is 0)
    - Auto-refresh is disabled (i.e. the ARFEN bit in the DBRFEN register is 0)
  - The following conditions must be satisfied when setting this register:
 
$$\text{RODTL} + \text{RODTA} \leq 7$$

$$\text{WODTL} + \text{WODTA} \leq 7$$

**15.3.28 SDRAM Timing Register 19 (DBTR19)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	TZQCS							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
7 to 0	TZQCS	00000000	R/W	Calibration Period Setting Bits These bits specify the minimum interval from a ZQCS (short calibration) command to the next command. 00000110: 6 cycles 00000111: 7 cycles : 01000000: 64 cycles : 11111111: 255 cycles Other settings are prohibited.

DBTR19 is used to set a timing parameter for the SDRAM.

- Notes:
- The setting is in cycles of the SDRAM operating clock.
  - The following condition must be satisfied:  
TZQCS ≥ T<sub>MOD</sub>
  - Writing to this register should only be performed when the following conditions are met.
    - Access to SDRAM is disabled (i.e. the ACCEN bit in the DBACEN register is 0)
    - Auto-refresh is disabled (i.e. the ARFEN bit in the DBRFEN register is 0)

### 15.3.29 SDRAM Operation Setting Register (DBBL)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	BL	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
1, 0	BL	00	R/W	Burst Length Setting Bits These bits specify the burst length of SDRAM. 00: Fixed to 8 Other settings are prohibited.

DBBL is used to set a burst operation mode of the memory.

- Notes:
- The setting is in cycles of the SDRAM operating clock.
  - Writing to this register should only be performed when the following conditions are met.
    - Access to SDRAM is disabled (i.e. the ACCEN bit in the DBACEN register is 0)
    - Auto-refresh is disabled (i.e. the ARFEN bit in the DBRFEN register is 0)

### 15.3.30 DBSC3 Operation Adjustment Register 0 (DBADJ0)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FREQRATIO	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CAMODE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

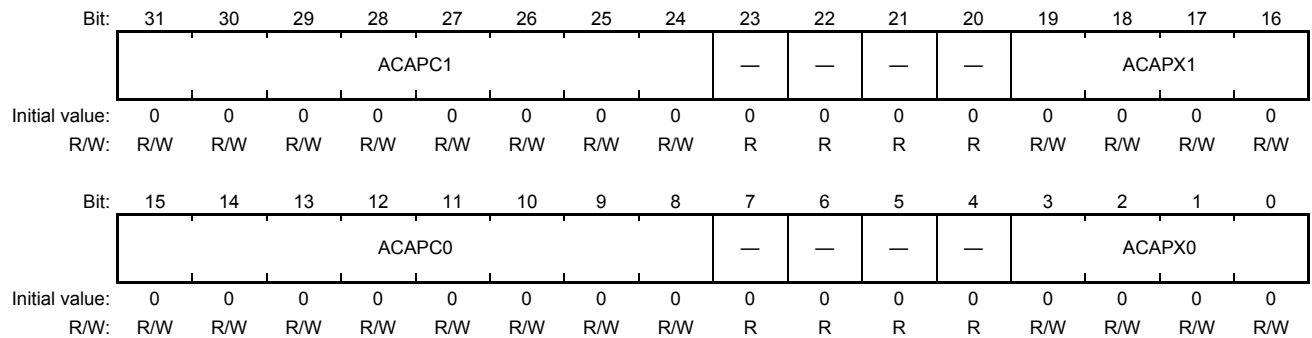
Bit	Bit Name	Initial Value	R/W	Description
31 to 18	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
17, 16	FREQRATIO	00	R/W	PHY Frequency Ratio Setting Bits These bits should be set to 10 (1:4 operating mode). 10: DBSC3: PHY frequency ratio is 1:4. Other settings are prohibited.
15 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
0	CAMODE	0	R/W	Command/Address Output Mode Setting Bit When the CAMODE bit is 1, the DBSC3 outputs a single command per two clock cycles. In this case, command signals and address signals, except for the M0(/1)CS[1:0]# signals of SDRAM, are kept constant for two clock cycles. During this period, the CS# signal becomes low only in the latter one clock cycle. 0: Setting prohibited 1: One command output in two clock cycles

DBADJ0 adjusts the DBSC3 operation.

Note: Writing to this register should only be performed when access to the SDRAM is disabled (i.e. the ACCEN bit in the DBACEN register is 0).

**15.3.31 DBSC3 Operation Adjustment Register 2 (DBADJ2)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	ACAPC1	H'00	R/W	H'20 (fixed value) Other settings are prohibited.
23 to 20	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
19 to 16	ACAPX1	H'0	R/W	Bits for Setting Transaction Count Acceptable by Device Control Unit (for the High priority port) These bits set the number of requests acceptable by the device control unit (for the high priority port) in the DBSC3 in transaction units. H'4: fewer value H'8: default value Other settings are prohibited. If you want to reduce average access latency, please set this bit to H'8. If you want to reduce worst access latency, please set this bit to H'4.
15 to 8	ACAPC0	H'00	R/W	H'20 (fixed value) Other settings are prohibited.
7 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
3 to 0	ACAPX0	H'0	R/W	Bits for Setting Transaction Count Acceptable by Device Control Unit (for the low priority port) These bits set the number of requests acceptable by the device control unit (for the low priority port) in the DBSC3 in transaction units. H'4: fewer value H'8: default value Other settings are prohibited. If you want to reduce average access latency, please set this bit to H'8. If you want to reduce worst access latency, please set this bit to H'4.

DBADJ2 adjusts the DBSC3 operation.

- Notes:
1. Writing to this register should only be performed when access to the SDRAM is disabled (i.e. the ACCEN bit in the DBACEN register is 0).
  2. The display unit module requires to set ACAPX0 and ACAPX1 to H'4.



### 15.3.32 Refresh Configuration Register 0 (DBRFCNF0)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	REFTHF											
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
11 to 0	REFTHF	H'000	R/W	Forcible Auto-Refresh Threshold Setting Bits These bits set the timing for forcible refreshing regardless of bus requests. The value represented by these bits affects the amount of jitter in the refresh interval and performance in access to memory. A smaller value means less jitter in the refresh interval but may reduce performance in access. For details on the amount of jitter in the refresh interval, see section 15.3.33, Refresh Configuration Register 1 (DBRFCNF1). H'080: 128 cycles : H'1FF: 511 cycles Other settings are prohibited.

DBRFCNF0 is used to set the timing for refreshing of the SDRAM.

If you change the value of this register while auto-refresh is active (i.e. the ARFEN bit in the DBRFEN register is 1), the auto-refresh facility must be re-activated to reflect the new value in refreshing. To re-activate the auto-refresh facility, write 1 to the ARFEN bit in the DBRFEN register.

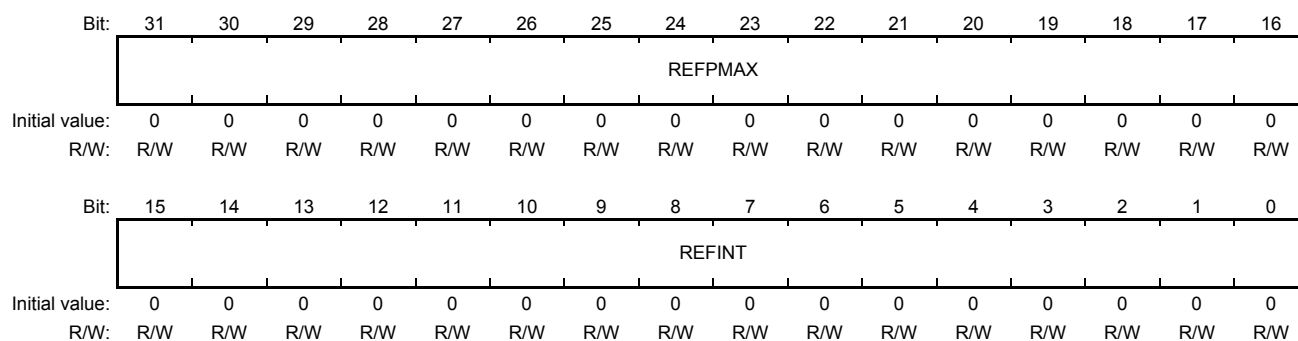
- Notes:
1. If auto-refresh is activated (i.e. the ARFEN bit in the DBRFEN register is set to 1) after a value smaller than the minimum value defined in the above table has been set in this register, correct operation cannot be guaranteed.
  2. The following conditions must be satisfied:  

$$\text{REFTHF} \geq (\text{TCKEL} + \text{TCKEH}) + \text{REFTH0}$$

$$(\text{REFTH0} = \max(\text{TRDPR}, \text{CWL} + (\text{BL}/2) + \text{TWR}, \text{TRAS}, \text{TRC} - \text{TRP}) + \text{TRPA} + 24)$$

### 15.3.33 Refresh Configuration Register 1 (DBRFCNF1)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√



Bit	Bit Name	Initial Value	R/W	Description
31 to 16	REFPMAX	H'0000	R/W	<p>Maximum Post Number of Refresh Commands Setting Bits</p> <p>These bits set the maximum number of refresh commands (post number) accumulated by auto-refresh. As long as the number of refresh commands that has been accumulated is smaller than REFPMAX, refresh commands are issued while there are no bus requests.</p> <p>H'0002: Two (minimum amount of jitter in the refresh interval)</p> <p>:</p> <p>H'0008: Eight cycles (maximum amount of jitter in the refresh interval)</p> <p>Other settings are prohibited.</p>
15 to 0	REFINT	H'0000	R/W	<p>Average Refresh Interval Setting Bits</p> <p>These bits set the average interval for issuing of refresh commands. When the REFINTS bit of the DBRFCNF2 register is 0, the average interval (in cycles) is REFINT. When the REFINTS bit of the DBRFCNF2 register is 1, on the other hand, the average interval (in cycles) is floor (REFINT/2). This average interval is hereafter referred to as REFINT_E. Thus, REFINT_E = REFINT &gt;&gt; REFINTS (&gt;&gt;: logical right-shift operator).</p> <p>H'0080: 128 cycles</p> <p>H'0081: 129 cycles</p> <p>:</p> <p>H'3FFF: 16383 cycles</p> <p>Other settings are prohibited.</p>

DBRFCNF1 is used to set the timing for refreshing of the SDRAM.

If you change the value of this register while auto-refresh is active (i.e. the ARFEN bit in the DBRFEN register is 1), the auto-refresh facility must be re-activated to reflect the new value in refreshing. To re-activate the auto-refresh facility, write 1 to the ARFEN bit in the DBRFEN register.

In the descriptions below, the "number of cycles" unless otherwise specified means the value measured with the SDRAM clock.

**(1) Register Settings and Refresh Generation Timing**

The following is an example of the settings in refresh configuration registers 1 and 2 and the timing of refresh generation.

In the explanations, "a ± b" indicates the range of values from a - b to a + b.

**(a) To make the refresh interval flexible**

Set REFPMAX to a value greater than or equal to 2.

REFINT holds the setting for the average refresh interval (tREFI in the normal range of operating temperatures), which is given in memory-vendor datasheets as an integer number of cycles. Set a value that has been rounded down from this integer. Set REFINTS to 0 or 1 according to the temperature at the time.

In this case, taking n as a positive integer, the time from one round of refresh generation to refresh generation n rounds later is (n × REFINT\_E + REFPMAX × REFINT\_E cycles) or shorter. However, this is on the assumption of no writing to the DBRFEN register during this period.

The following condition must be satisfied:

$$\text{REFINT} \geq (\text{TCALRZ} + \text{TCALZR} + \text{REFTHF} \times 2) \ll \text{REFINTS}$$

- Notes:
1. If auto-refresh is activated (i.e. the ARFEN bit in the DBRFEN register is set to 1) after a value smaller than the minimum value defined in the above table has been set in this register, correct operation cannot be guaranteed.
  2. Other restrictions not mentioned in the above may apply to some types of SDRAM according to the PHY unit specifications.

### 15.3.34 Refresh Configuration Register 2 (DBRFCNF2)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	REFPMIN			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	REF INTS
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

In the descriptions below, the number of cycles means the value measured with the SDRAM clock unless otherwise specified.

Bit	Bit Name	Initial Value	R/W	Description
31 to 20	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
19 to 16	REFPMIN	H'0	R/W	Minimum Post Number of Refresh Commands Setting Bits These bits set the minimum number of refresh commands (post number) accumulated by auto-refresh. As long as the number of refresh commands that has been accumulated is smaller than REFPMIN, refresh commands are issued irrespective of the bus request state. H'1: 1 Other settings are prohibited.
15 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
0	REFINTS	0	R/W	Average Refresh Interval Adjustment Bit When this bit is 0, the average interval (in cycles) is the value set in the REFINT bits. When this bit is 1, on the other hand, the average interval (in cycles) is floor (REFINT/2). 0: Average interval is REFINT 1: Average interval is 1/2 REFINT

DBRFCNF2 is used to set the timing for refreshing of the SDRAM.

If you change the value of this register while auto-refresh is active (i.e. the ARFEN bit in the DBRFEN register is 1), the auto-refresh facility must be re-activated to reflect the new value in refreshing. To re-activate the auto-refresh facility, write 1 to the ARFEN bit in the DBRFEN register.

The following condition must be satisfied:

$$\text{REFPMAX} \geq \text{REFPMIN}$$

### 15.3.35 DDR3-SDRAM Calibration Configuration Register (DBCALCNF)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	CALEN	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CALINT															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 25	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
24	CALEN	0	R/W	DDR3-SDRAM Calibration Enable Bit While this bit is set to 1, calibration of DDR3-SDRAM is executed (ZQCS command is issued) at regular intervals. 0: DDR3-SDRAM calibration is disabled. 1: DDR3-SDRAM calibration is enabled.
23 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
15 to 0	CALINT	H'0000	R/W	DDR3-SDRAM Calibration Frequency Setting Bits These bits adjust the frequency of DDR3-SDRAM calibration. When the CALINT bits are set to n, the ZQCS command is issued once every time the refresh command has been issued for n times by the auto-refresh function. H'0000: Executed only once after auto-refresh executed immediately after the CALEN bit is set to 1. H'0001: Executed at every auto-refresh. H'0002: Executed at every two times of auto-refresh. : H'FFFF: Executed at every 65535 times of auto-refresh.

DBCALCNF controls the function for calibrating DDR3-SDRAM at regular intervals.

- Notes:
- When CALINT = 0, calibration is executed (ZQCS command is issued) only once after auto-refresh executed immediately after 1 is written to the CALEN bit; no calibration is executed after that. To execute calibration again, write 1 to the CALEN bit.
  - Even when the CALEN bit is set to 1, the ZQCS command is not issued when the auto-refresh function is stopped (i.e. the ARFEN bit in the DBRFEN register is 0).

3. Writing a value other than H'0100 0000 to this register should only be performed when the following conditions are met.
  - Access to SDRAM is disabled (i.e. the ACCEN bit in the DBACEN register is 0)
  - Auto-refresh is disabled (i.e. the ARFEN bit in the DBRFEN register is 0)
4. Writing H'0100 0000 to this register should only be performed when the following condition is met.
  - Auto-refresh is enabled (i.e. the ARFEN bit in the DBRFEN register is 1)

### 15.3.36 DDR3-SDRAM Calibration Timing Register (DBCALTR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	TCALRZ											
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	TCALZR											
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 28	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
27 to 16	TCALRZ	H'000	R/W	DDR3-SDRAM Calibration Timing Setting (REF to ZQCS Interval Setting) Bits These bits specify the minimum interval between a REF and ZQCS commands for calibration execution. H'080: 128 cycles : H'FFF: 4095 cycles Other settings are prohibited.
15 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
11 to 0	TCALZR	H'000	R/W	DDR3-SDRAM Calibration Timing Setting (ZQCS to REF Interval Setting) Bits These bits specify the minimum interval between a ZQCS command for calibration and a REF command for the next auto-refresh execution. H'080: 128 cycles : H'FFF: 4095 cycles Other settings are prohibited.

DBCALTR specifies the command interval limitations for DDR3-SDRAM calibration executed at regular intervals.

Notes: 1. This register value has no effect when CALEN = 0.

2. The setting is in cycles of the SDRAM operating clock.

3. The following conditions must be satisfied:

$$TCALRZ \geq \max(128, TRFC + (7 \times TFAW \div 4) + tACTANY + 32)$$

$$TCALZR \geq \max(128, TZQCS + (7 \times TFAW \div 4) + tACTANY + 32)$$

$REFINT \geq (TCALRZ + TCALZR + (REFTHF \times 2)) \ll REFINTS$   
( $tACTANY = \max (TRCD, TRAS, TRC - TRPA, TFAW)$ )

4. Writing to this register should only be performed when the following conditions are met.
  - Access to SDRAM is disabled (i.e. the ACCEN bit in the DBACEN register is 0)
  - Auto-refresh is disabled (i.e. the ARFEN bit in the DBRFEN register is 0)



## 15.3.37 ODT Operation Setting Register (DBRNK0)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RODT OUT0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	WODT OUT0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 17	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
16	RODTOUT0	0	R/W	Bit for ODT Output Level Setting at Read This bit set the ODT output level at read. 0: ODT output level at read is set to 0. 1: ODT output level at read is set to 1.
15 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
0	WODTOUT0	0	R/W	Bit for ODT Output Level Setting at Write This bit set the ODT output level at write. 0: ODT output level at write is set to 0. 1: ODT output level at write is set to 1.

DBRNK0 specifies the ODT output level of SDRAM.

Note: Writing to this register should only be performed when the following conditions are met.

- Access to SDRAM is disabled (i.e. the ACCEN bit in the DBACEN register is 0)
- Auto-refresh is disabled (i.e. the ARFEN bit in the DBRFEN register is 0)

### 15.3.38 Power-Down Configuration Register (DBPDNCNF)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PDWAIT								—	—	—	PDDL	—	—	PDMODE	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R/W	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
15 to 8	PDWAIT	H'00	R/W	Power-Down Wait Bits These bits set the number of cycles it takes to enter power-down mode after memory accesses no longer occur. H'10: 16 cycles : H'FF: 255 cycles Other settings are prohibited.
7 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
4	PDDL	0	R/W	Power-Down DLL Control Bit This bit turns on or off the DLL of SDRAM when entering power-down mode. 0: DLL is turned off at a precharged power-down. DLL is turned on at an active power-down 1: DLL is turned on at a power-down.
3, 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
1, 0	PDMODE	00	R/W	Power-Down/Self-Refresh Mode Bits When these bits are set to "01" and there has been no memory access for a certain period, the power-down entry command is issued to place the SDRAM in power-down mode. When these bits are set to "10" and there has been no memory access for a certain period, the self-refresh entry command is issued to place the SDRAM in self-refresh mode. 00: Auto power-down mode and auto self-refresh mode are off. 01: Auto power-down mode is on. Other settings are prohibited.

DBPDNCNF controls the auto power-down function.

- Notes:
1. The setting is in cycles of the SDRAM operating clock.
  2. Return from a power-down mode incurs a time penalty of  $\max(3, \text{TCKEH}) - 3$  cycles.
  3. Writing to this register should only be performed when the following conditions are met.
    - Access to SDRAM is disabled (i.e. the ACCEN bit in the DBACEN register is 0)
    - Auto-refresh is disabled (i.e. the ARFEN bit in the DBRFEN register is 0)

**15.3.39 DFI Status IF Input Register (DBDFISTAT)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	INITCOMPL
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
0	INITCOMPL	0	R	This bit is only used in the initialization sequence.

**15.3.40 DFI Status IF Output Register (DBDFICNT)**

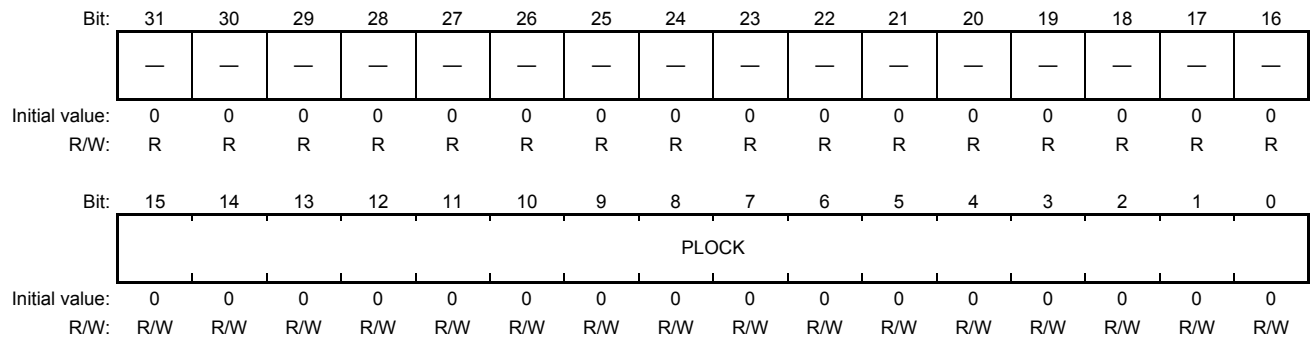
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	FREQRATIO	—	—	—	—	INITSTART
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
5, 4	FREQRATIO	00	R/W	These bits are only used in the initialization sequence. 01: Usual frequency ratio is set as the clock frequency ratio. Other settings are prohibited.
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
0	INITSTART	0	R/W	This bit is only used in the initialization sequence. 0: dfi_init_start is set to 0. 1: dfi_init_start is set to 1.

**15.3.41 PHY Unit Lock Register (DBPDLCK)**

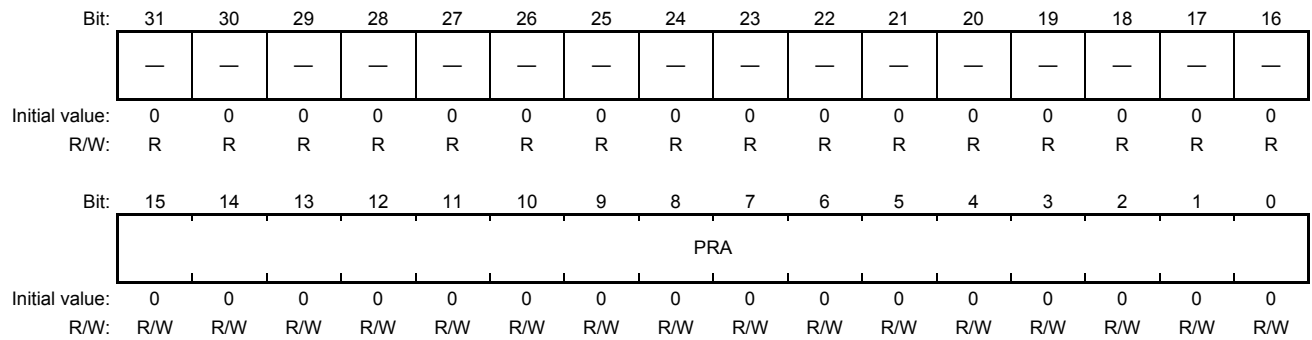
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√



Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
15 to 0	PLOCK	H'0000	R/W	PHY Unit Access Lock Setting Setting this register to H'A55A allows access to the PHY unit registers. H'A55A: Access to the registers of the PHY unit is allowed. Values other than H'A55A: Access to the registers of the PHY unit is prohibited.

**15.3.42 PHY Unit Address Register (DBPDRGA)**

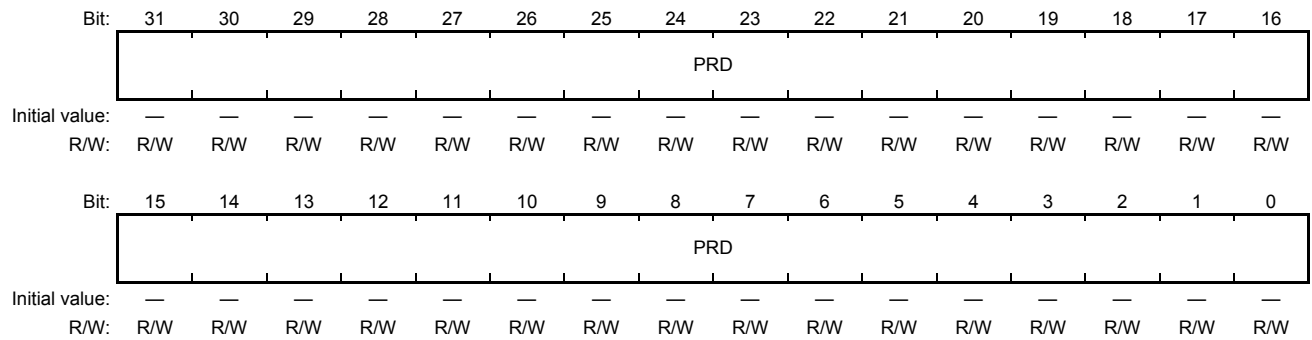
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√



Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
15 to 0	PRA	H'0000	R/W	PHY Unit Address Register This address is used for accessing (setting or referring to values of) the internal registers of the PHY unit (registers built in the PHY unit). For details, see the section 15.3.43, PHY Unit Access Register (DBPDRGD).

**15.3.43 PHY Unit Access Register (DBPDRGD)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	PRD	Undefined	R/W	<p>PHY Unit Access register</p> <p>The values in registers of the PHY unit are readable and writable. Writing to or reading from these bits allows access (setting or referencing values in) the internal registers of the PHY unit. The register to be accessed is determined by the value of the PRA bits in the PHY unit address register (DBPDRGA).</p> <p>To access the registers of the PHY unit, write to or read from these bits after setting the PHY unit lock register (DBPDLCK) and the PHY unit address register (DBPDRGA).</p> <p>Attempted writing to these bits while the setting of the PHY lock register (DBPDLCK) is prohibiting access to registers of the PHY unit is ignored (writing does not proceed but no error occurs).</p>



### 15.3.44 Bus Control Unit 0 Control Register 1 (DBBS0CNT1)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	BKADM
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
1, 0	BKADM	00	R/W	Bank Assignment Setting Bits These bits are used to set the method for assigning the SDRAM banks to the logical address space, i.e. whether and how logical addresses are divided into multiple blocks to which different SDRAM banks are assigned. For details on the relation between the logical addresses and SDRAM addresses, refer to section 15.4.12, Address Multiplexing. 00: The whole logical address space is regarded as one block. 01: The logical address space is divided into the following two blocks: One for banks 0 to 3 and one for banks 4 to 7. 10: The logical address space is divided into the following three blocks: One for banks 0 and 1, one for banks 2 and 3, and one for banks 4 to 7. 11: The logical address space is divided into the following four blocks: One for bank 0, one for bank 1, one for banks 2 and 3, and one for banks 4 to 7.

- Notes:
- This register must only be written from within the initialization sequence (see section 15.4.3, Initialization Sequence).
  - Writing to this register should only be performed when the following conditions are met.
    - Access to SDRAM is disabled (i.e. the ACCEN bit in the DBACEN register is 0)

### 15.3.45 AXI Port Setting Register 0 (DBWT0CNF0)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	WASYN		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	WCN		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 19	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
18 to 16	WASYN	000	R/W	"010" Other settings are prohibited.
15 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
2 to 0	WCN	000	R/W	AXI Clock to Memory Clock Ratio Setting Bits These bits specify the ratio of the memory clock/4 (MCLK) to the AXI clock (AXICLK). When WASYN = 010, 000: 0.5 MCLK < AXICLK < MCLK (default) 001: MCLK < AXICLK < 1.2 MCLK 010: 1.2 MCLK < AXICLK < 1.4 MCLK 011: 1.4 MCLK < AXICLK < 1.6 MCLK 100: 1.6 MCLK < AXICLK < 1.8 MCLK 101: 1.8 MCLK < AXICLK < 2 MCLK Other settings are prohibited.

Note: This register should only be written to only during the initialization sequence (refer to section 15.4.3, Initialization Sequence) or while AXI bus access and external memory access are idle.

**15.3.46 AXI Port Setting Register 4 (DBWT0CNF4)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	RDFIIFONUM				
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
4 to 0	RDFIIFONUM	00000	R/W	Read FIFO Count Bit [RZ/G1H/M] This bit specifies the capacity of the read data FIFO. 01111: 16 (DDR3 DATA 64 bits × 1-ch mode) 11111: 32 (Others) Other settings are prohibited.
				Read FIFO Count Bit [RZ/G1N/E] This bit specifies the capacity of the read data FIFO. 11111: 32 Other settings are prohibited.

Note: This register should only be written to only during the initialization sequence (refer to section 15.4.3, Initialization Sequence).

**15.3.47 Scheduler Setting Register 0 (DBSCHECNT0)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ARBEN
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 2	—	0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
1, 0	ARBEN	00	R/W	Latency Port Enable Bits Fixed to "00"

## 15.4 Operation

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

### 15.4.1 Supported SDRAM Commands

Table 15.6 lists the SDRAM commands issued by the DBSC3. These commands are issued to the SDRAM in synchronously with the M0(1)CK[1:0] and M0(1)CK[1:0]# signals. In the table, "n-1" indicates the state of the signal applied to the SDRAM one cycle before SDRAM command issue; n indicates the state of the signal at the time of command issue.

**Table 15.6 SDRAM Commands Issued by the DBSC3**

Function	Symbol	MCKE[1:0]		MCS [1:0]#	MRAS#	MCAS#	MWE#	MBA [2:0]	MA [15:3]	MA12 /BC	MA10 /AP	MA11, MA[9:0]
		n-1	n									
Device deselected	DES	H	H	H	X	X	X	X	X	X	X	X
Read	READ	H	H	L	H	L	H	V	V	V	L	V
Write	WRITE	H	H	L	H	L	L	V	V	V	L	V
Bank activate	ACT	H	H	L	L	H	H	V	V	V	V	V
Precharge select bank	PRE	H	H	L	L	H	L	V	V	V	L	V
Precharge all banks	PREA	H	H	L	L	H	L	V	V	V	H	V
Auto-refresh	REF	H	H	L	L	L	H	V	V	V	V	V
Self-refresh entry	SRE	H	L	L	L	L	H	V	V	V	V	V
Self-refresh exit	SRX	L	H	H	V	V	V	V	V	V	V	V
Power down entry	PDE	H	L	L	H	H	H	V	V	V	V	V
Power down exit	PDX	L	H	L	H	H	H	V	V	V	V	V
Mode register set	MRS	H	H	L	L	L	L	V	V	V	V	V
ZQ calibration short issue	ZQCS	H	H	L	H	H	L	X	X	X	H	X
ZQ calibration long issue	ZQCL	H	H	L	H	H	L	X	X	X	L	X

[Legend]

H: High level

L: Low level

X: High or low level (don't e)

V: Valid data

In the table, corrective names are used for signals. For example, MCKE and MA indicate M0CKE/M1CKE and M0A/M1A signals, respectively.

The above DES command is issued when the SDRAM is not accessed, and so cannot be explicitly issued by the user.

## 15.4.2 SDRAM Command Issue

### (1) Basic Access

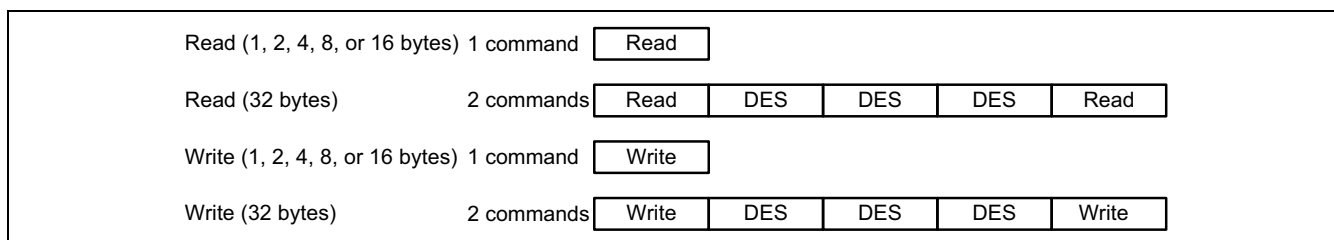
The DBSC3 stores in a queue the requests received via the AXI. The order for the start of request processing changes according to whether or not this is preceded by processing for precharging or activation, but processing is executed in the order allowed in AXI protocol to improve the memory efficiency.

When SDRAM initialization is completed, upon receiving a read/write request, a page miss occurs with all banks in the closed state. Hence the DBSC3 first issues an activate (ACT) command, to open the corresponding bank. After opening the bank, the read/write command of the SDRAM corresponding to the read/write request is issued. At this time, the number of issued read/write commands differs depending on the bus width and the request size (1/2/4/8/16/32 bytes), as indicated in Figure 15.4. For example, when performing 32-byte reading from the AXI bus with an external data bus width of 16 bits, two read commands are issued. When issuing the read command in the first cycle, data is read with a burst length of 8 (four DDR clock cycles), so that it is necessary to wait until the fifth cycle to issue the second read command.

When access ends, the DBSC3 leaves the bank open, without using a precharge (PRE) command. The bank is closed when (1) the following request is for the same bank with a different row address; (2) there is an auto-refresh request; or (3) the user issues a precharge-all (PREA) command using the SDRAM command control register, for self-refresh processing.

Thus in normal access other than self-refresh, the DBSC3 uses hardware for bank management, so that except for the register settings upon initialization, the user need not execute control.

Furthermore, the DBSC3 performs multibank operation of eight banks. Hence the maximum number of banks that can be opened simultaneously is eight. Refer to section 15.4.12, Address Multiplexing, for the correspondence between access addresses from the AXI and SDRAM bank/row addresses.



**Figure 15.4 Read/Write Command Issued to the SDRAM in Response to the Request from the AXI**

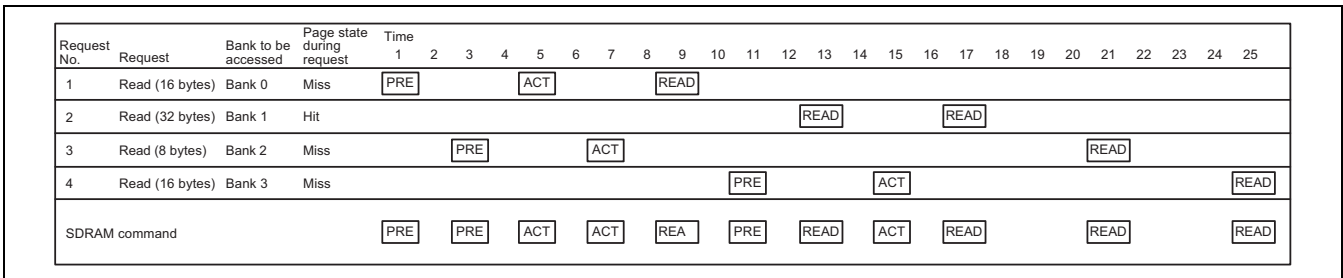
**(2) Preceding Precharge/Activate Processing**

In order to utilize SDRAM multibank functions to reduce SDRAM command vacant cycles insofar as possible and improve the efficiency of bus use, the DBSC3 issues in advance a PRE/ACT command corresponding to the following request queue page miss processing. Only the PRE/ACT command is issued in advance, so there is no change in the read/write order. A PRE/ACT command is issued in advance only when the following request (1) results in a page miss, and moreover (2) entails access of a bank different from that of the request currently being processed. Figure 15.5 shows an example of execution of preceding precharge/activate processing (as an example for operational description). This is an example of a command issued to the SDRAM when the external data bus width is 16 bits, the PRE-ACT minimum time constraint is 4 cycles, the ACT-READ/WRITE minimum time constraint is 4 cycles, and the ACT-ACT minimum time constraint is 2 cycles. In this example, the first through fourth requests are accumulated, and the first request is the request initially provided to the queue.

The DBSC3 issues one command each time it has received two memory clock pulses. Thus, there are always an even number of clock pulses between commands. At time 1, the DBSC3 issues to the SDRAM a PRE command for processing the first read (16-byte) request. Then, when determining the command to be issued at time 3, due to timing constraints it is not possible to issue at time 3 the ACT command necessary as request processing for the first read (16-byte) request, which has higher priority. Hence the DBSC3 searches for a command to be issued at time 3 from the following request queue. From the search results it is seen that preceding precharge processing can be executed for the third read (8-byte) request. Because the DBSC3 gives priority to preceding requests, it decides to perform preceding precharge processing for the third read (8-byte) request, and issues a PRE command to the SDRAM.

At time 5, the DBSC3 can process the first read (16-byte) request and it issues an ACT command to the SDRAM. At time 7, it issues an ACT command to the SDRAM for the first read (8-byte) request processing. After issuing the read command for the first read (16-byte) request processing, it issues a PRE command to the SDRAM for the fourth read (16-byte) request processing at time 11.

Thereafter, the processing described above is repeated.



**Figure 15.5 Example of Preceding Precharge/Activate Processing**

### 15.4.3 Initialization Sequence

The following shows examples of initialization sequence for each memory type. The initialization sequence should be executed to enable SDRAM access after power to the DBSC3 is turned on. Note that the sequence differs depending on the specifications of the target memory.

For detailed information such as the power supply and timing parameters, refer to the datasheet for the SDRAM being used. The procedure for starting the system differs from that for restoring it from the power-supply backup mode.

#### 15.4.3.1 Starting the System

##### (1) 64 Bits × 1-ch Mode [RZ/G1H/M]

##### (a) After power is turned on, apply a power-on reset and wait until the DBSC3 is released from the reset state.

If SDRAM Power-Supply Backup Function is not used, M0/1BKPRST# is driven high before starting Initialization. (Refer to 15.4.14 SDRAM Power-Supply Backup Function)

1. After release from the reset state, set the registers as follows:
  - Write H'0000A55A to the PHY unit lock register (DBPDLCK).  
This allows the access to the PHY unit registers.
  - Write H'0000A55A to DB\_ADDR + H'4000.
  - Write H'00000001 to DB\_ADDR + H'4008.
2. Here, the setting on the M0/1RESET# signals should be executed (The following 3 lines correspond to this setting):
  - Write H'21000000 to the manual command-issuing register (DBCMD).
  - Write H'11000000 to the manual command-issuing register (DBCMD).
  - Write H'10000000 to the manual command-issuing register (DBCMD).
3. Write H'00000001 to the PHY unit address register (DBPDRGA).
4. Write H'80000000 to the PHY unit access register (DBPDRGD).
5. Write H'00000004 to the PHY unit address register (DBPDRGA).
6. Read the PHY unit access register (DBPDRGD) and wait until 1 is read from bit 0.
7. Write H'00000006 to the PHY unit address register (DBPDRGA).
8. Write H'0001C000 to the PHY unit access register (DBPDRGD) (greater than or equal to 1440 MBps, MD19 = 0, refer to Tables 7.6a and 7.6b).  
Write H'0005C000 to the PHY unit access register (DBPDRGD) (less than 1440 MBps, MD19 = 1, refer to Tables 7.6a and 7.6b).
9. Write H'0000000F to the PHY unit address register (DBPDRGA).
10. Write H'00181224 to the PHY unit access register (DBPDRGD).
11. Write H'00000010 to the PHY unit address register (DBPDRGA).
12. Write H'F004649B to the PHY unit access register (DBPDRGD).
13. Write H'00000061 to the PHY unit address register (DBPDRGA).
14. Write H'0000006D to the PHY unit access register (DBPDRGD).
15. Write H'00000001 to the PHY unit address register (DBPDRGA).
16. Write H'00000073 to the PHY unit access register (DBPDRGD).

##### (b) DBSC3 Setting 1

Here, set the DBSC3\_0 side only.

1. SDRAM type setting register (DBKIND)
2. SDRAM configuration setting register 0 (DBCONF0)
3. PHY type setting register (DBPHYTYPE)



4. SDRAM operation setting register (DBBL)
5. SDRAM timing registers 0 to 19 (DBTR0 to DBTR19)
6. ODT operation setting register 0 (DBRNK0)
7. DBSC3 operation adjustment registers 0 and 2 (DBADJ0, DBADJ2)
8. AXI port setting registers 0 and 4 (DBWT0CNF0, DBWT0CNF4)

### (c) PHY Setting 1

#### DBSC3\_0 Setting:

1. Read the DBDFISTAT register and confirm that 1 is read from INITCOMPL (bit 0).  
When 1 is read, the RESET# pin goes low.
2. Write H'00000011 to the DBDFICNT register.  
This sets the clock frequency ratio and dfi\_init\_start.
3. Write H'00000003 to the PHY unit address register (DBPDRGA).
4. Write H'0300C4E1 to the PHY unit access register (DBPDRGD) (For DDR3).  
Write H'0300C561 to the PHY unit access register (DBPDRGD) (For DDR3L).  
Set IOM[2:1] of each buffer IO-Mode to the value for DDR3/DDR3L.
5. Write H'00000023 to the PHY unit address register (DBPDRGA).
6. Write H'00FCDB60 to the PHY unit access register (DBPDRGD).  
PHY Configuration Setting (Modify according to the memory connected to DDR.)  
[17:0]: tREFPRD ( $9 \times tREFI = 9 \times 7.8 \mu\text{s}$ , H'0DB60 at 1600 MHz)  
[18]: NOBUB (fixed to 1)  
[19]: FXDLAT (fixed to 1)  
[27:20]: PUBMODE (fixed to H'0F)  
[31:28]: Reserved (must be H'0 since these bits are not used)
7. Write H'00000011 to the PHY unit address register (DBPDRGA).
8. Write H'1000040B to the PHY unit access register (DBPDRGD).
9. Write H'00000012 to the PHY unit address register (DBPDRGA).
10. Write H'9D5CBB66 to the PHY unit access register (DBPDRGD).  
DRAM Timing Parameters Setting (Modify according to the memory connected to DDR.)  
[3:0]: tRTP (DDR3-1600 = H'6 (number of cycles equal to 7.5 ns or more))  
[7:4]: tWTR (DDR3-1600 = H'6 (number of cycles equal to 7.5 ns or more))  
[11:8]: tRP (DDR3-1600 = H'B (number of cycles equal to 13.75 ns or more (CL = 11)))  
[15:12]: tRCD (DDR3-1600 = H'B (number of cycles equal to 13.75 ns or more (CL = 11)))  
[21:16]: tRAS (DDR3-1600 = H'1C (number of cycles equal to 35 ns or more (CL = 11)))  
[25:22]: tRRD (DDR3-1600 = H'5 (number of cycles equal to 6 ns or more (1-KB page size)))  
[31:26]: tRC (DDR3-1600 = H'27 (number of cycles equal to 48.75 ns or more (CL = 11)))
11. Write H'00000013 to the PHY unit address register (DBPDRGA).
12. Write H'1A868300 to the PHY unit access register (DBPDRGD).  
DRAM Timing Parameters Setting (Modify according to the memory connected to DDR.)  
[1:0]: tMRD (For DDR3, enter the number of cycles to be added to the MIN value, that is 4 cycles.  
The set value is B'00 for using the MIN condition without additional cycles.)  
[4:2]: tMOD (For DDR3-1600, the set value should be 12 cycles equal to 15 ns or more. When the set value is H'0, 12 cycles is specified; as the set value increases by one, the number of cycles increases by one up to 5 cycles.)  
[10:5]: tFAW (DDR3-1600 = H'18 (number of cycles equal to 30 ns or more (1-KB page size)))  
[19:11]: tRFC (The set value is H'0D0 since the cycle is 260 ns for 4 GB.)

- [25:20]: tWLMRD (Minimum delay from when write leveling mode is programmed to the first DQS/DQS# rising edge, Default = H'28.)
- [29:26]: tWLO (Number of clock cycles from when write leveling DQS is driven high by the control block to when the results from the SDRAM on DQ is sampled by the control block, the set value is H'6 since the DDR3-1600 MAX value is 6.)
- [31:30]: tAOND/tAOFD (Default = B'00 since this is only for DDR2.)
13. Write H'00000014 to the PHY unit address register (DBPDRGA).
  14. Write H'300214D8 to the PHY unit access register (DBPDRGD).  
DRAM Timing Parameters Setting (Modify according to the memory connected to DDR.)  
[9:0]: tXS (Self refresh exit delay 5CK to 310 ns: H'005 to H'0F8)  
[14:10]: tXP (Power down exit delay 3CK to 6 ns: H'03 to H'05)  
[18:15]: tCKE (CKE minimum pulse width 3CK to 5 ns: H'3 to H'5)  
[28:19]: tDLLK (DLL locking time 512CK: H'200)  
[29]: tRTODT (Read to ODT delay: 1)  
[30]: Fixed to 0  
[31]: Fixed to 0
  15. Write H'00000015 to the PHY unit address register (DBPDRGA).
  16. Write H'00000D70 to the PHY unit access register (DBPDRGD).  
SDRAM Mode Register 0 Setting (Modify according to the memory connected to DDR.)  
[15:0]: set MR0 values.  
[31:16]: Reserved (must be 0 since these bits are not used)
  17. Write H'00000016 to the PHY unit address register (DBPDRGA).
  18. Write H'00000006 to the PHY unit access register (DBPDRGD).  
SDRAM Mode Register 1 Setting (Modify according to the memory connected to DDR.)  
[15:0]: set MR1 values.  
[31:16]: Reserved (must be 0 since these bits are not used)
  19. Write H'00000017 to the PHY unit address register (DBPDRGA).
  20. Write H'00000018 to the PHY unit access register (DBPDRGD).  
SDRAM Mode Register 2 Setting (Modify according to the memory connected to DDR.)  
[15:0]: set MR2 values.  
[31:16]: Reserved (must be 0 since these bits are not used)
  21. Write H'0000001A to the PHY unit address register (DBPDRGA).
  22. Write H'910035C7 to the PHY unit access register (DBPDRGD).  
Set the above values in DATA Training Configuration setting of DDR-PHY.
  23. Write H'00000004 to the PHY unit address register (DBPDRGA).
  24. Read the PHY unit access register (DBPDRGD) and wait until 1 is read from bit 0.
  25. Write H'00000001 to the PHY unit address register (DBPDRGA).
  26. Write H'00000181 to the PHY unit access register (DBPDRGD).
  27. Write H'11000000 to the manual command-issuing register (DBCMD).
  28. Write H'00000004 to the PHY unit address register (DBPDRGA).
  29. Read the PHY unit access register (DBPDRGD) and wait until 1 is read from bit 0.
  30. Write H'00000001 to the PHY unit address register (DBPDRGA).
  31. Write H'0000FE01 to the PHY unit access register (DBPDRGD).

#### (d) DBSC Setting 2

Here, set the DBSC3\_0 side only.

1. Bus control unit 0 control register 1 (DBBS0CNT1)

2. DDR3-SDRAM calibration configuration register (DBCALCNF)
3. DDR3-SDRAM calibration timing register (DBCALTR)
4. Refresh configuration registers 0 to 2 (DBRFCNF0 to DBRFCNF2)
5. Write H'00000004 to the PHY unit address register (DBPDRGA).  
Read the PHY unit access register (DBPDRGD) and wait until 1 is read from bit 0.
6. Set the ARFEN bit to 1 in the auto-refresh enable register (DBRFEN).
7. Write H'00000010 to the PHY unit address register (DBPDRGA).
8. Write HF00464DB to the PHY unit access register (DBPDRGD).
9. Write H'00000000 to DB\_ADDR + H'4008.
10. Write H'00000000 to DB\_ADDR + H'4000.
11. Set the ACCEN bit to 1 (access enabled) in the SDRAM access enable register (DBACEN).
12. Write H'00000000 to the PHY unit lock register (DBPDLCK).  
This locks the access to the PHY unit registers.

End of initialization sequence

### (2) 32 Bits × 2-ch Mode [RZ/G1H/M]

The initialization sequence for 32 bits × 2-ch mode can be executed by similar way for 64 bits × 1-ch mode. Differences between them are as follows.

In the section "(1) 64 Bits × 1-ch Mode", the DBSC3\_1 setting should also be executed in the flowing each subsection;

- (b) **DBSC3 Setting 1**
- (c) **PHY Setting 1**
- (d) **DBSC Setting 2**

### (3) 32 Bits × 1-ch Mode [RZ/G1N/E]

The initialization sequence for 32 bits × 1-ch mode can be executed by similar way for 64 bits × 1-ch mode.

### (4) 32 Bits × 1-ch Mode [RZ/G1H/M]

The initialization sequence for 32 bits × 1-ch mode can be executed by similar way for 64 bits × 1-ch mode. Differences between them are as follows.

The following sequence should be added below the line No.31 of subsection "(c) PHY Setting 1" in In the section "(1) 64 Bits × 1-ch Mode" to stop the DBSC3\_1 side macro of DDR-PHY;

32. Write H'000000B0 to the PHY unit address register (DBPDRGA).
33. Write H'7C020EB0 to the PHY unit access register (DBPDRGD).
34. Write H'000000C0 to the PHY unit address register (DBPDRGA).
35. Write H'7C020EB0 to the PHY unit access register (DBPDRGD).
36. Write H'000000D0 to the PHY unit address register (DBPDRGA).
37. Write H'7C020EB0 to the PHY unit access register (DBPDRGD).
38. Write H'000000E0 to the PHY unit address register (DBPDRGA).
39. Write H'7C020E80 to the PHY unit access register (DBPDRGD).

#### 15.4.4 Self-Refresh Operation

If it is not necessary to access the SDRAM, the SDRAM can be put in self-refresh mode to reduce power consumption while still retaining data contents.

Since access to the SDRAM is disabled in self-refresh mode, requesting an SDRAM data access to the DBSC3 will cause an error.

The following procedure should be used to enter or release self-refresh mode.

##### (1) Self-Refreshing (When the Clock is Not Stopped)

Use the following procedure to enter self-refresh mode.

1. Set the ACCEN bit to 0 (access disabled) in the SDRAM access enable register (DBACEN).
2. Use the manual command-issuing register (DBCMD) to issue the PREA (precharge all) command. The value written to this register should be OPC = PreA, ARG = 0.
3. Use the manual command-issuing register (DBCMD) to issue the Self-Refresh Entry command. The value written to this register should be OPC = SREn, ARG = 0.
4. Set the ARFEN bit to 0 in the auto-refresh enable register (DBRFEN).

Use the following procedure to release self-refresh mode.

1. Set the ARFEN bit to 1 in the auto-refresh enable register (DBRFEN).
2. Use the manual command-issuing register (DBCMD) to issue the Self-Refresh Exit command. The value written to this register should be OPC = SRXt, ARG = 0.
3. Use the manual command-issuing register (DBCMD) to insert wait cycles until access to the SDRAM is enabled. The value written to this register should be OPC = Wait, ARG = tXSDLL (normally, 512).
4. Set the ACCEN bit to 1 (access enabled) in the SDRAM access enable register (DBACEN).

##### (2) Self-Refreshing (When the Clock is Stopped or Clock Frequency is Changed)

Use the following procedure to enter self-refresh mode.

1. Set the ACCEN bit to 0 (access disabled) in the SDRAM access enable register (DBACEN).
2. Use the manual command-issuing register (DBCMD) to issue the PREA (precharge all) command. The value written to this register should be OPC = PreA, ARG = 0.
3. Use the manual command-issuing register (DBCMD) to issue the Self-Refresh Entry command. The value written to this register should be OPC = SREn, ARG = 0.
4. Set the ARFEN bit to 0 in the auto-refresh enable register (DBRFEN).
5. Use the manual command-issuing register (DBCMD) to insert wait cycles for the clock to stop. The value written to this register should be OPC = Wait, ARG = tCKSRE (normally, max {5, 10 ns}).
6. Read the operation completion waiting register (DBWAIT) and wait for the response.
7. The clock supplied to the DBSC3 can be stopped at this point

Use the following procedure to release self-refresh mode.

1. Restart the clock supply and wait until the clock settles.
2. Reconfigure the PHY unit.
3. Use the manual command-issuing register (DBCMD) to insert wait cycles until self-refresh mode is released. The value written to this register should be OPC = Wait, ARG = tCKSRX (normally, max {5, 10 ns}).
4. Set the ARFEN bit to 1 in the auto-refresh enable register (DBRFEN).
5. Use the manual command-issuing register (DBCMD) to issue the Self-Refresh Exit command. The value written to this register should be OPC = SRXt, ARG = 0.

6. Use the manual command-issuing register (DBCMD) to insert wait cycles until access to the SDRAM is enabled. The value written to this register should be OPC = Wait, ARG = tXSDLL (normally, 512).
7. Set the ACCEN bit to 1 (access enabled) in the SDRAM access enable register (DBACEN).

#### 15.4.5 Power-Down Operation

If there is no need to access SDRAM, entering the power-down mode can place the SDRAM internal clock in inactive state, which can effectively lower the power consumption in the device. Even in a power-down mode, the clock and power need to be supplied.

Use the following procedure to enter the power-down mode.

1. Set the ACCEN bit to 0 (access disabled) in the SDRAM access enable register (DBACEN).
2. Use the manual command-issuing register (DBCMD) to issue the Power Down Entry command. The value written to this register should be OPC = PDEn, ARG = 0.

Use the following procedure to release the power-down mode.

1. Use the manual command-issuing register (DBCMD) to issue the Power Down Exit command. The value written to this register should be OPC = PDXt, ARG = 0.
2. Set the ACCEN bit to 1 (access enabled) in the SDRAM access enable register (DBACEN).

To keep holding the SDRAM data in power-down mode, a refresh command needs to be issued at regular intervals in the same way as in normal operation. In the DBSC3, by entering the power-down mode with the auto-refresh function operating (ARFEN = 1 in the DBRFEN register), refresh is performed regularly and the SDRAM data is held even in the power-down mode.

Since access to the SDRAM is disabled in self-refresh mode, requesting an SDRAM data access to the DBSC3 will cause an error.

#### 15.4.6 Modifying Refresh Settings during Operation

In the DBSC3, refresh settings (such as refresh frequency) can be modified during operation. The following gives the procedure for it. Note that it is assumed that the ACCEN bit in the DBACEN register has been set to 1 (access is enabled) and the ARFEN bit in the DBRFEN register has been set to 1 (auto-refresh is active) in advance.

1. Write to refresh configuration registers 0 to 2 (DBRFCNF0 to DBRFCNF2) to modify settings.
2. Write 1 to the ARFEN bit in the auto-refresh enable register (DBRFEN).

After step 2, the new settings made in step 1 are applied to the refresh operation.

#### 15.4.7 Restrictions on AXI Bus Interface

This section describes the restrictions on the AXI bus interface.

##### (1) Fixed Burst Transfer

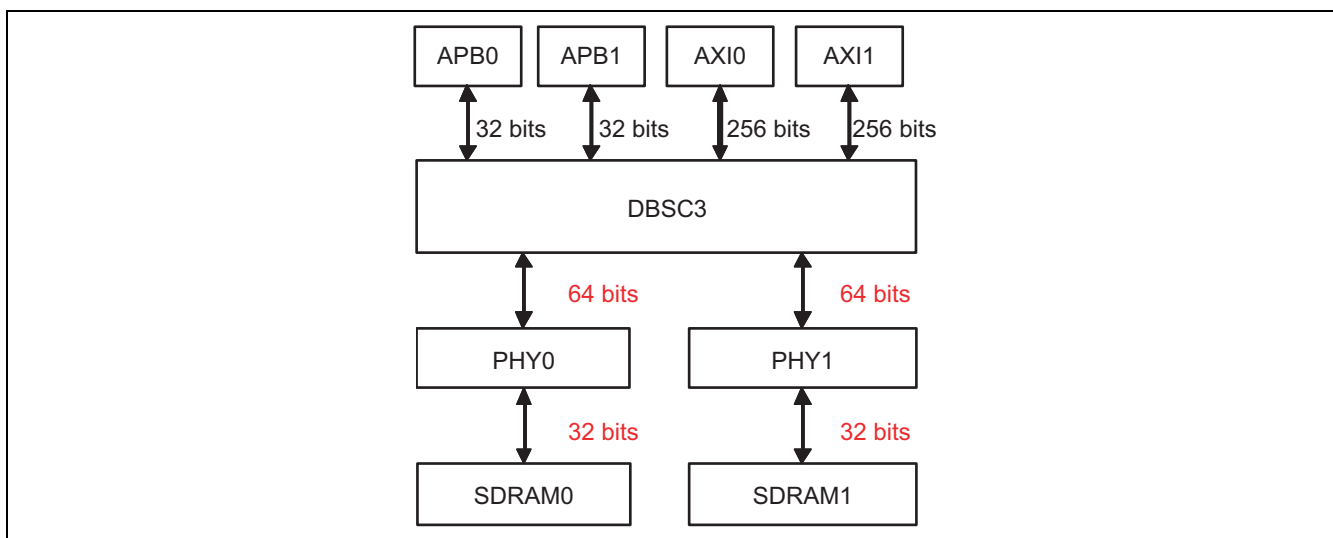
Only a burst length of 1 is supported for the fixed burst length transfer. The DBSC3 returns an error response to the transactions with the other burst length.

**15.4.8 Switching PHY Channel Count (between 32-bit SDRAM and 64-bit SDRAM) [RZ/G1H/M]**

The DBSC3 supports configurations of two 32-bit SDRAMs and one 64-bit SDRAM. By switching the number of PHY channels using the mode signal input to the DBSC3 allows a different SDRAM configuration to be used.

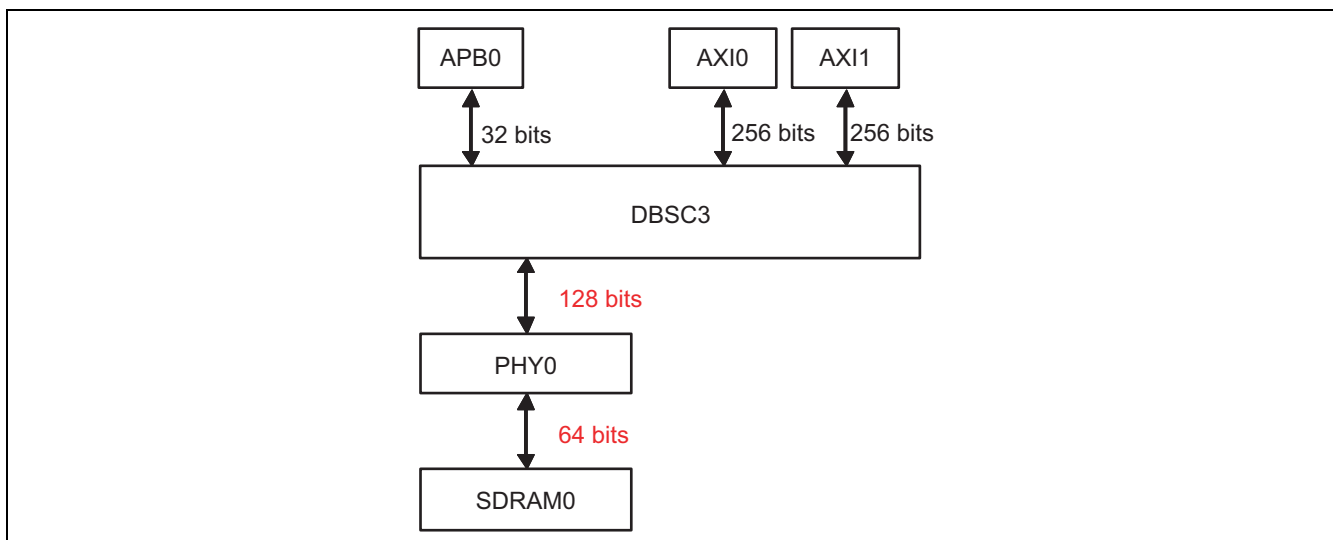
With 2-channel mode selected, PHY 2-channel mode is set to allow the configuration of two 32-bit SDRAMs and with 1-channel mode selected, PHY 1-channel mode is set to allow the configuration of one 64-bit SDRAM. For mode switching method, refer to the mode setting sections.

**15.4.9 PHY 2-Channel Mode (Two 32-Bit SDRAMs) [RZ/G1H/M]**



**Figure 15.6 PHY 2-Channel Mode**

**15.4.10 PHY 1-Channel Mode (One 64-Bit SDRAM) [RZ/G1H/M]**



**Figure 15.7 PHY 1-Channel Mode**

### 15.4.11 Setting the SDRAM Configuration Setting Register

#### (1) DDR3-SDRAM (16-Bit External Bus) [RZ/G1E]

Capacity	Memory Configuration	Rank	Bank [No. of Banks]	Row [No. of Bits]	Column [No. of Bits]	DBCONF0 Setting				
						AWRW0	AWRK0	AWBK0	AWCL0	DW0
64 Mbytes	32 M × 16 bits "512 Mbits" (1 module)	1	8	12	10	01100	0	11	1010	01
128 Mbytes	64 M × 8 bits "512 Mbits" (2 modules)	1	8	13	10	01101	0	11	1010	01
	64 M × 16 bits "1 Gbit" (1 module)	1	8	13	10	01101	0	11	1010	01
256 Mbytes	128 M × 8 bits "1 Gbit" (2 modules)	1	8	14	10	01110	0	11	1010	01
	128 M × 16 bits "2 Gbits" (1 module)	1	8	14	10	01110	0	11	1010	01
512 Mbytes	256 M × 8 bits "2 Gbits" (2 modules)	1	8	15	10	01111	0	11	1010	01
	256 M × 16 bits "4 Gbits" (1 module)	1	8	15	10	01111	0	11	1010	01
1 Gbyte	512 M × 8 bits "4 Gbits" (2 modules)	1	8	16	10	10000	0	11	1010	01
2 Gbytes	1024 M × 8 bits "8 Gbits" (4 modules)	1	8	16	11	10000	0	11	1011	01

Note: Connection between this controller and multiple memory units may or may not be possible depending on the electrical characteristics of the chip.

The above table shows the configuration of memory modules connected to a single DBSC3 channel.

## (2) DDR3-SDRAM (32-Bit External Bus)

Capacity	Memory Configuration	Rank	Bank [No. of Banks]	Row [No. of Bits]	Column [No. of Bits]	DBCONF0 Setting				
						AWRW0	AWRK0	AWBK0	AWCLO	DW0
128 Mbytes	32 M × 16 bits "512 Mbits" (2 modules)	1	8	12	10	01100	0	11	1010	10
256 Mbytes	64 M × 8 bits "512 Mbits" (4 modules)	1	8	13	10	01101	0	11	1010	10
	64 M × 16 bits "1 Gbit" (2 modules)	1	8	13	10	01101	0	11	1010	10
512 Mbytes	128 M × 8 bits "1 Gbit" (4 modules)	1	8	14	10	01110	0	11	1010	10
	128 M × 16 bits "2 Gbits" (2 modules)	1	8	14	10	01110	0	11	1010	10
1 Gbyte	256 M × 8 bits "2 Gbits" (4 modules)	1	8	15	10	01111	0	11	1010	10
	256 M × 16 bits "4 Gbits" (2 modules)	1	8	15	10	01111	0	11	1010	10
2 Gbytes	512 M × 8 bits "4 Gbits" (4 modules)	1	8	16	10	10000	0	11	1010	10
	512 M × 16 bits "8 Gbits" (2 modules)	1	8	16	10	10000	0	11	1010	10
4 Gbytes	1024 M × 8 bits "8 Gbits" (4 modules)	1	8	16	11	10000	0	11	1011	10

Note: Connection between this controller and multiple memory units may or may not be possible depending on the electrical characteristics of the chip.

The above table shows the configuration of memory modules connected to a single DBSC3 channel.



**(3) DDR3-SDRAM (64-Bit External Bus) [RZ/G1H/M]**

Capacity	Memory Configuration	Rank	Bank [No. of Banks]	Row [No. of Bits]	Column [No. of Bits]	DBCONF0 Setting				
						AWRW0	AWRK0	AWBK0	AWCL0	DW0
256 Mbytes	32 M × 16 bits "512 Mbits" (4 modules)	1	8	12	10	01100	0	11	1010	10
512 Mbytes	64 M × 8 bits "512 Mbits" (8 modules)	1	8	13	10	01101	0	11	1010	10
	64 M × 16 bits "1 Gbit" (4 modules)	1	8	13	10	01101	0	11	1010	10
1 Gbyte	128 M × 8 bits "1 Gbit" (8 modules)	1	8	14	10	01110	0	11	1010	10
	128 M × 16 bits "2 Gbits" (4 modules)	1	8	14	10	01110	0	11	1010	10
2 Gbytes	256 M × 8 bits "2 Gbits" (8 modules)	1	8	15	10	01111	0	11	1010	10
	256 M × 16 bits "4 Gbits" (4 modules)	1	8	15	10	01111	0	11	1010	10
4 Gbytes	512 M × 8 bits "4 Gbits" (8 modules)	1	8	16	10	10000	0	11	1010	10
	512 M × 16 bits "8 Gbits" (4 modules)	1	8	16	10	10000	0	11	1010	10
8 Gbytes	1024 M × 8 bits "8 Gbits" (8 modules)	1	8	16	11	10000	0	11	1011	10

Note: Connection between this controller and multiple memory units may or may not be possible depending on the electrical characteristics of the chip.

### 15.4.12 Address Multiplexing

Memory of various sizes can be connected through the settings of the SDRAM configuration setting register 0 (DBCONF0). The DW0 bits are used to set the external data bus width, and the AWRW0 and AWCL0 bits are used to set the size of the memory connected. The AWBK0 bits are used to specify the number of banks; depending on the application the possibility of page hits may be increased.

#### (1) DDR3-SDRAM (16-Bit External Bus) [RZ/G1E]

**Table 15.7 Relation between Address Pins and Logical Addresses (BKADM = B'00)**  
(When One 16-Bit-Width SDRAM Module or Two 8-Bit-Width SDRAM Modules are Connected)

Memory Type		BA2	BA1	BA0	MA15	MA14	MA13	MA12	MA11	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0
32 M × 16 bits	ROW	A13	A12	A11	0	0	0	0	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
	COL	A13	A12	A11	0	0	0	BC#	0	AP	A10	A9	A8	A7	A6	A5	A4	A3	0	0
64 M × 16 bits	ROW	A13	A12	A11	0	0	0	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
	COL	A13	A12	A11	0	0	0	BC#	0	AP	A10	A9	A8	A7	A6	A5	A4	A3	0	0
128 M × 16 bits	ROW	A13	A12	A11	0	0	A27	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
	COL	A13	A12	A11	0	0	0	BC#	0	AP	A10	A9	A8	A7	A6	A5	A4	A3	0	0
256 M × 16 bits	ROW	A13	A12	A11	0	A28	A27	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
	COL	A13	A12	A11	0	0	0	BC#	0	AP	A10	A9	A8	A7	A6	A5	A4	A3	0	0

Notes: 1. A31 to A0 are the logical address bits in byte units. A31 represents the MSB, and A0 the LSB.  
2. AP is an abbreviation of auto precharge option.  
3. BC# is an abbreviation of burst chop option.

**Table 15.8 Relation between Address Pins and Logical Addresses (BKADM = B'01)**  
(When One 16-Bit-Width SDRAM Module or Two 8-Bit-Width SDRAM Modules are Connected)

Memory Type		BA2	BA1	BA0	MA15	MA14	MA13	MA12	MA11	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0
32 M × 16 bits	ROW	A25	A12	A11	0	0	0	0	A13	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
	COL	A25	A12	A11	0	0	0	BC#	0	AP	A10	A9	A8	A7	A6	A5	A4	A3	0	0
64 M × 16 bits	ROW	A26	A12	A11	0	0	0	A13	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
	COL	A26	A12	A11	0	0	0	BC#	0	AP	A10	A9	A8	A7	A6	A5	A4	A3	0	0
128 M × 16 bits	ROW	A27	A12	A11	0	0	A13	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
	COL	A27	A12	A11	0	0	0	BC#	0	AP	A10	A9	A8	A7	A6	A5	A4	A3	0	0
256 M × 16 bits	ROW	A28	A12	A11	0	A13	A27	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
	COL	A28	A12	A11	0	0	0	BC#	0	AP	A10	A9	A8	A7	A6	A5	A4	A3	0	0

**Table 15.9 Relation between Address Pins and Logical Addresses (BKADM = B'10)**  
(When One 16-Bit-Width SDRAM Module or Two 8-Bit-Width SDRAM Modules are Connected)

Memory Type		BA2	BA1	BA0	MA15	MA14	MA13	MA12	MA11	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0
32 M × 16 bits (A25 = 0)	ROW	A25	A24	A11	0	0	0	0	A13	A12	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
	COL	A25	A24	A11	0	0	0	BC#	0	AP	A10	A9	A8	A7	A6	A5	A4	A3	0	0
32 M × 16 bits (A25 = 1)	ROW	A25	A12	A11	0	0	0	0	A13	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
	COL	A25	A12	A11	0	0	0	BC#	0	AP	A10	A9	A8	A7	A6	A5	A4	A3	0	0
64 M × 16 bits (A26 = 0)	ROW	A26	A25	A11	0	0	0	A13	A12	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
	COL	A26	A25	A11	0	0	0	BC#	0	AP	A10	A9	A8	A7	A6	A5	A4	A3	0	0
64 M × 16 bits (A26 = 1)	ROW	A26	A12	A11	0	0	0	A13	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
	COL	A26	A12	A11	0	0	0	BC#	0	AP	A10	A9	A8	A7	A6	A5	A4	A3	0	0
128 M × 16 bits (A27 = 0)	ROW	A27	A26	A11	0	0	A13	A12	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
	COL	A27	A26	A11	0	0	0	BC#	0	AP	A10	A9	A8	A7	A6	A5	A4	A3	0	0
128 M × 16 bits (A27 = 1)	ROW	A27	A12	A11	0	0	A13	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
	COL	A27	A12	A11	0	0	0	BC#	0	AP	A10	A9	A8	A7	A6	A5	A4	A3	0	0
256 M × 16 bits (A28 = 0)	ROW	A28	A27	A11	0	A13	A12	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
	COL	A28	A27	A11	0	0	0	BC#	0	AP	A10	A9	A8	A7	A6	A5	A4	A3	0	0
256 M × 16 bits (A28 = 1)	ROW	A28	A12	A11	0	A13	A27	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
	COL	A28	A12	A11	0	0	0	BC#	0	AP	A10	A9	A8	A7	A6	A5	A4	A3	0	0

**Table 15.10 Relation between Address Pins and Logical Addresses (BKADM = B'11)**  
(When One 16-Bit-Width SDRAM Module or Two 8-Bit-Width SDRAM Modules are Connected)

Memory Type		BA2	BA1	BA0	MA15	MA14	MA13	MA12	MA11	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0
32 M × 16 bits (A[25:24] = 00)	ROW	A25	A24	A23	0	0	0	0	A13	A12	A11	A22	A21	A20	A19	A18	A17	A16	A15	A14
	COL	A25	A24	A23	0	0	0	BC#	0	AP	A10	A9	A8	A7	A6	A5	A4	A3	0	0
32 M × 16 bits (A[25:24] = 01)	ROW	A25	A24	A11	0	0	0	0	A13	A12	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
	COL	A25	A24	A11	0	0	0	BC#	0	AP	A10	A9	A8	A7	A6	A5	A4	A3	0	0
32 M × 16 bits (A25 = 1)	ROW	A25	A12	A11	0	0	0	0	A13	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
	COL	A25	A12	A11	0	0	0	BC#	0	AP	A10	A9	A8	A7	A6	A5	A4	A3	0	0
64 M × 16 bits (A[26:25] = 00)	ROW	A26	A25	A24	0	0	0	A13	A12	A11	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
	COL	A26	A25	A24	0	0	0	BC#	0	AP	A10	A9	A8	A7	A6	A5	A4	A3	0	0
64 M × 16 bits (A[26:25] = 01)	ROW	A26	A25	A11	0	0	0	A13	A12	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
	COL	A26	A25	A11	0	0	0	BC#	0	AP	A10	A9	A8	A7	A6	A5	A4	A3	0	0
64 M × 16 bits (A26 = 1)	ROW	A26	A12	A11	0	0	0	A13	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
	COL	A26	A12	A11	0	0	0	BC#	0	AP	A10	A9	A8	A7	A6	A5	A4	A3	0	0
128 M × 16 bits (A[27:26] = 00)	ROW	A27	A26	A25	0	0	A13	A12	A11	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
	COL	A27	A26	A25	0	0	0	BC#	0	AP	A10	A9	A8	A7	A6	A5	A4	A3	0	0
128 M × 16 bits (A[27:26] = 01)	ROW	A27	A26	A11	0	0	A13	A12	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
	COL	A27	A26	A11	0	0	0	BC#	0	AP	A10	A9	A8	A7	A6	A5	A4	A3	0	0
128 M × 16 bits (A27 = 1)	ROW	A27	A12	A11	0	0	A13	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
	COL	A27	A12	A11	0	0	0	BC#	0	AP	A10	A9	A8	A7	A6	A5	A4	A3	0	0
256 M × 16 bits (A[28:27] = 00)	ROW	A28	A27	A26	0	A13	A12	A11	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
	COL	A28	A27	A26	0	0	0	BC#	0	AP	A10	A9	A8	A7	A6	A5	A4	A3	0	0
256 M × 16 bits (A[28:27] = 01)	ROW	A28	A27	A11	0	A13	A12	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
	COL	A28	A27	A11	0	0	0	BC#	0	AP	A10	A9	A8	A7	A6	A5	A4	A3	0	0
256 M × 16 bits (A28 = 1)	ROW	A28	A12	A11	0	A13	A27	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
	COL	A28	A12	A11	0	0	0	BC#	0	AP	A10	A9	A8	A7	A6	A5	A4	A3	0	0

## (2) DDR3-SDRAM (32-Bit External Bus)

**Table 15.11 Relation between Address Pins and Logical Addresses (BKADM = B'00)  
(When Two 16-Bit-Width SDRAM Modules or Four 8-Bit-Width SDRAM Modules are Connected)**

Memory Type		BA2	BA1	BA0	MA15	MA14	MA13	MA12	MA11	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0
32 M × 32 bits	ROW	A14	A13	A12	0	0	0	0	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15
	COL	A14	A13	A12	0	0	0	BC#	0	AP	A11	A10	A9	A8	A7	A6	A5	A4	0	0
64 M × 32 bits	ROW	A14	A13	A12	0	0	0	A27	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15
	COL	A14	A13	A12	0	0	0	BC#	0	AP	A11	A10	A9	A8	A7	A6	A5	A4	0	0
128 M × 32 bits	ROW	A14	A13	A12	0	0	A28	A27	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15
	COL	A14	A13	A12	0	0	0	BC#	0	AP	A11	A10	A9	A8	A7	A6	A5	A4	0	0
256 M × 32 bits	ROW	A14	A13	A12	0	A29	A28	A27	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15
	COL	A14	A13	A12	0	0	0	BC#	0	AP	A11	A10	A9	A8	A7	A6	A5	A4	0	0
512 M × 32 bits	ROW	A14	A13	A12	A30	A29	A28	A27	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15
	COL	A14	A13	A12	0	0	0	BC#	0	AP	A11	A10	A9	A8	A7	A6	A5	A4	0	0
1024 M × 32 bits	ROW	A15	A14	A13	A31	A30	A29	A28	A27	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16
	COL	A15	A14	A13	0	0	0	BC#	A12	AP	A11	A10	A9	A8	A7	A6	A5	A4	0	0

Notes: 1. A31 to A0 are the logical address bits in byte units. A31 represents the MSB, and A0 the LSB.  
2. AP is an abbreviation of auto precharge option.  
3. BC# is an abbreviation of burst chop option.

**Table 15.12 Relation between Address Pins and Logical Addresses (BKADM = B'01)  
(When Two 16-Bit-Width SDRAM Modules or Four 8-Bit-Width SDRAM Modules are Connected)**

Memory Type		BA2	BA1	BA0	MA15	MA14	MA13	MA12	MA11	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0
32 M × 32 bits	ROW	A26	A13	A12	0	0	0	0	A14	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15
	COL	A26	A13	A12	0	0	0	BC#	0	AP	A11	A10	A9	A8	A7	A6	A5	A4	0	0
64 M × 32 bits	ROW	A27	A13	A12	0	0	0	A14	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15
	COL	A26	A13	A12	0	0	0	BC#	0	AP	A11	A10	A9	A8	A7	A6	A5	A4	0	0
128 M × 32 bits	ROW	A28	A13	A12	0	0	A14	A27	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15
	COL	A28	A13	A12	0	0	0	BC#	0	AP	A11	A10	A9	A8	A7	A6	A5	A4	0	0
256 M × 32 bits	ROW	A29	A13	A12	0	A14	A28	A27	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15
	COL	A29	A13	A12	0	0	0	BC#	0	AP	A11	A10	A9	A8	A7	A6	A5	A4	0	0
512 M × 32 bits	ROW	A30	A13	A12	A14	A29	A28	A27	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15
	COL	A30	A13	A12	0	0	0	BC#	0	AP	A11	A10	A9	A8	A7	A6	A5	A4	0	0
1024 M × 32 bits	ROW	A31	A14	A13	A15	A30	A29	A28	A27	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16
	COL	A31	A14	A13	0	0	0	BC#	A12	AP	A11	A10	A9	A8	A7	A6	A5	A4	0	0

**Table 15.13 Relation between Address Pins and Logical Addresses (BKADM = B'10)  
(When Two 16-Bit-Width SDRAM Modules or Four 8-Bit-Width SDRAM Modules are Connected)**

Memory Type		BA2	BA1	BA0	MA15	MA14	MA13	MA12	MA11	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0
32 M × 32 bits (A26 = 0)	ROW	A26	A25	A12	0	0	0	0	A14	A13	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15
	COL	A26	A25	A12	0	0	0	BC#	0	AP	A11	A10	A9	A8	A7	A6	A5	A4	0	0
32 M × 32 bits (A26 = 1)	ROW	A26	A13	A12	0	0	0	0	A14	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15
	COL	A26	A13	A12	0	0	0	BC#	0	AP	A11	A10	A9	A8	A7	A6	A5	A4	0	0
64 M × 32 bits (A27 = 0)	ROW	A27	A26	A12	0	0	0	A14	A13	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15
	COL	A26	A26	A12	0	0	0	BC#	0	AP	A11	A10	A9	A8	A7	A6	A5	A4	0	0
64 M × 32 bits (A27 = 1)	ROW	A27	A13	A12	0	0	0	A14	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15
	COL	A26	A13	A12	0	0	0	BC#	0	AP	A11	A10	A9	A8	A7	A6	A5	A4	0	0
128 M × 32 bits (A28 = 0)	ROW	A28	A27	A12	0	0	A14	A13	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15
	COL	A28	A27	A12	0	0	0	BC#	0	AP	A11	A10	A9	A8	A7	A6	A5	A4	0	0
128 M × 32 bits (A28 = 1)	ROW	A28	A13	A12	0	0	A14	A27	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15
	COL	A28	A13	A12	0	0	0	BC#	0	AP	A11	A10	A9	A8	A7	A6	A5	A4	0	0
256 M × 32 bits (A29 = 0)	ROW	A29	A28	A12	0	A14	A13	A27	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15
	COL	A29	A28	A12	0	0	0	BC#	0	AP	A11	A10	A9	A8	A7	A6	A5	A4	0	0
256 M × 32 bits (A29 = 1)	ROW	A29	A13	A12	0	A14	A28	A27	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15
	COL	A29	A13	A12	0	0	0	BC#	0	AP	A11	A10	A9	A8	A7	A6	A5	A4	0	0
512 M × 32 bits (A30 = 0)	ROW	A30	A29	A12	A14	A13	A28	A27	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15
	COL	A30	A29	A12	0	0	0	BC#	0	AP	A11	A10	A9	A8	A7	A6	A5	A4	0	0
512 M × 32 bits (A30 = 1)	ROW	A30	A13	A12	A14	A29	A28	A27	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15
	COL	A30	A13	A12	0	0	0	BC#	0	AP	A11	A10	A9	A8	A7	A6	A5	A4	0	0
1024 M × 32 bits (A31 = 0)	ROW	A31	A30	A13	A15	A14	A29	A28	A27	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16
	COL	A31	A30	A13	0	0	0	BC#	A12	AP	A11	A10	A9	A8	A7	A6	A5	A4	0	0
1024 M × 32 bits (A31 = 1)	ROW	A31	A14	A13	A15	A30	A29	A28	A27	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16
	COL	A31	A14	A13	0	0	0	BC#	A12	AP	A11	A10	A9	A8	A7	A6	A5	A4	0	0

**Table 15.14 Relation between Address Pins and Logical Addresses (BKADM = B'11)  
(When Two 16-Bit-Width SDRAM Modules or Four 8-Bit-Width SDRAM Modules are Connected)**

Memory Type		BA2	BA1	BA0	MA15	MA14	MA13	MA12	MA11	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0
32 M × 32 bits (A[26:25] = 00)	ROW	A26	A25	A24	0	0	0	0	A14	A13	A12	A23	A22	A21	A20	A19	A18	A17	A16	A15
	COL	A26	A25	A24	0	0	0	BC#	0	AP	A11	A10	A9	A8	A7	A6	A5	A4	0	0
32 M × 32 bits (A[26:25] = 01)	ROW	A26	A25	A12	0	0	0	0	A14	A13	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15
	COL	A26	A25	A12	0	0	0	BC#	0	AP	A11	A10	A9	A8	A7	A6	A5	A4	0	0
32 M × 32 bits (A26 = 1)	ROW	A26	A13	A12	0	0	0	0	A14	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15
	COL	A26	A13	A12	0	0	0	BC#	0	AP	A11	A10	A9	A8	A7	A6	A5	A4	0	0
64 M × 32 bits (A[27:26] = 00)	ROW	A27	A26	A25	0	0	0	A14	A13	A12	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15
	COL	A26	A26	A25	0	0	0	BC#	0	AP	A11	A10	A9	A8	A7	A6	A5	A4	0	0
64 M × 32 bits (A[27:26] = 01)	ROW	A27	A26	A12	0	0	0	A14	A13	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15
	COL	A26	A26	A12	0	0	0	BC#	0	AP	A11	A10	A9	A8	A7	A6	A5	A4	0	0
64 M × 32 bits (A27 = 1)	ROW	A27	A13	A12	0	0	0	A14	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15
	COL	A26	A13	A12	0	0	0	BC#	0	AP	A11	A10	A9	A8	A7	A6	A5	A4	0	0
128 M × 32 bits (A[28:27] = 00)	ROW	A28	A27	A26	0	0	A14	A13	A12	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15
	COL	A28	A27	A26	0	0	0	BC#	0	AP	A11	A10	A9	A8	A7	A6	A5	A4	0	0
128 M × 32 bits (A[28:27] = 01)	ROW	A28	A27	A12	0	0	A14	A13	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15
	COL	A28	A27	A12	0	0	0	BC#	0	AP	A11	A10	A9	A8	A7	A6	A5	A4	0	0
128 M × 32 bits (A28 = 1)	ROW	A28	A13	A12	0	0	A14	A27	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15
	COL	A28	A13	A12	0	0	0	BC#	0	AP	A11	A10	A9	A8	A7	A6	A5	A4	0	0
256 M × 32 bits (A[29:28] = 00)	ROW	A29	A28	A27	0	A14	A13	A12	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15
	COL	A29	A28	A27	0	0	0	BC#	0	AP	A11	A10	A9	A8	A7	A6	A5	A4	0	0
256 M × 32 bits (A[29:28] = 01)	ROW	A29	A28	A12	0	A14	A13	A27	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15
	COL	A29	A28	A12	0	0	0	BC#	0	AP	A11	A10	A9	A8	A7	A6	A5	A4	0	0
256 M × 32 bits (A29 = 1)	ROW	A29	A13	A12	0	A14	A28	A27	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15
	COL	A29	A13	A12	0	0	0	BC#	0	AP	A11	A10	A9	A8	A7	A6	A5	A4	0	0
512 M × 32 bits (A[30:29] = 00)	ROW	A30	A29	A28	A14	A13	A12	A27	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15
	COL	A30	A29	A28	0	0	0	BC#	0	AP	A11	A10	A9	A8	A7	A6	A5	A4	0	0
512 M × 32 bits (A[30:29] = 01)	ROW	A30	A29	A12	A14	A13	A28	A27	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15
	COL	A30	A29	A12	0	0	0	BC#	0	AP	A11	A10	A9	A8	A7	A6	A5	A4	0	0
512 M × 32 bits (A30 = 1)	ROW	A30	A13	A12	A14	A29	A28	A27	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15
	COL	A30	A13	A12	0	0	0	BC#	0	AP	A11	A10	A9	A8	A7	A6	A5	A4	0	0
1024 M × 32 bits (A[31:30] = 00)	ROW	A31	A30	A29	A15	A14	A13	A28	A27	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16
	COL	A31	A30	A29	0	0	0	BC#	A12	AP	A11	A10	A9	A8	A7	A6	A5	A4	0	0
1024 M × 32 bits (A[31:30] = 01)	ROW	A31	A30	A13	A15	A14	A29	A28	A27	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16
	COL	A31	A30	A13	0	0	0	BC#	A12	AP	A11	A10	A9	A8	A7	A6	A5	A4	0	0
1024 M × 32 bits (A31 = 1)	ROW	A31	A14	A13	A15	A30	A29	A28	A27	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16
	COL	A31	A14	A13	0	0	0	BC#	A12	AP	A11	A10	A9	A8	A7	A6	A5	A4	0	0

**(3) DDR3-SDRAM (64-Bit External Bus) [RZ/G1H/M]****Table 15.15 Relation between Address Pins and Logical Addresses (BKADM = B'00)**

AWBK	AWR	AWCL	DW		BA2	BA1	BA0	MA15	MA14	MA13	MA12	MA11	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0	
11	01100	1010	10	ROW	A27	A14	A13	0	0	0	0	A15	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	
				COL	A27	A14	A13	0	0	0	BC#	0	AP	A12	A11	A10	A9	A8	A7	A6	A5	0	0	
11	01101	1010	10	ROW	A28	A14	A13	0	0	0	A15	A27	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	
				COL	A28	A14	A13	0	0	0	BC#	0	AP	A12	A11	A10	A9	A8	A7	A6	A5	0	0	
11	01110	1010	10	ROW	A29	A14	A13	0	0	0	A15	A28	A27	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16
				COL	A29	A14	A13	0	0	0	BC#	0	AP	A12	A11	A10	A9	A8	A7	A6	A5	0	0	
11	01111	1010	10	ROW	A30	A14	A13	0	A15	A29	A28	A27	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	
				COL	A30	A14	A13	0	0	0	BC#	0	AP	A12	A11	A10	A9	A8	A7	A6	A5	0	0	
11	10000	1010	10	ROW	A31	A14	A13	A15	A30	A29	A28	A27	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	
				COL	A31	A14	A13	0	0	0	BC#	0	AP	A12	A11	A10	A9	A8	A7	A6	A5	0	0	

- Notes: 1. A31 to A0 are the logical address bits in byte units. A31 represents the MSB, and A0 the LSB.  
2. AP is an abbreviation of auto precharge option.  
3. BC# is an abbreviation of burst chop option.

**Table 15.16 Relation between Address Pins and Logical Addresses (BKADM = B'01)**

AWBK	AWR	AWCL	DW		BA2	BA1	BA0	MA15	MA14	MA13	MA12	MA11	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0	
11	01100	1010	10	ROW	A27	A14	A13	0	0	0	0	A15	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	
				COL	A27	A14	A13	0	0	0	BC#	0	AP	A12	A11	A10	A9	A8	A7	A6	A5	0	0	
11	01101	1010	10	ROW	A28	A14	A13	0	0	0	A15	A27	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	
				COL	A28	A14	A13	0	0	0	BC#	0	AP	A12	A11	A10	A9	A8	A7	A6	A5	0	0	
11	01110	1010	10	ROW	A29	A14	A13	0	0	0	A15	A28	A27	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16
				COL	A29	A14	A13	0	0	0	BC#	0	AP	A12	A11	A10	A9	A8	A7	A6	A5	0	0	
11	01111	1010	10	ROW	A30	A14	A13	0	A15	A29	A28	A27	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	
				COL	A30	A14	A13	0	0	0	BC#	0	AP	A12	A11	A10	A9	A8	A7	A6	A5	0	0	
11	10000	1010	10	ROW	A31	A14	A13	A15	A30	A29	A28	A27	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	
				COL	A31	A14	A13	0	0	0	BC#	0	AP	A12	A11	A10	A9	A8	A7	A6	A5	0	0	

**Table 15.17 Relation between Address Pins and Logical Addresses (BKADM = B'10)**

AWBK	AWR	AWCL	DW		BA2	BA1	BA0	MA15	MA14	MA13	MA12	MA11	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0	
11	01100	1010	10	ROW	A27	A26	A13	0	0	0	0	A15	A14	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	
				COL	A27	A26	A13	0	0	0	BC#	0	AP	A12	A11	A10	A9	A8	A7	A6	A5	0	0	
11	01101	1010	10	ROW	A28	A27	A13	0	0	0	A15	A14	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	
				COL	A28	A27	A13	0	0	0	BC#	0	AP	A12	A11	A10	A9	A8	A7	A6	A5	0	0	
11	01110	1010	10	ROW	A29	A28	A13	0	0	0	A15	A14	A27	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16
				COL	A29	A28	A13	0	0	0	BC#	0	AP	A12	A11	A10	A9	A8	A7	A6	A5	0	0	
11	01111	1010	10	ROW	A30	A29	A13	0	A15	A14	A28	A27	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	
				COL	A30	A29	A13	0	0	0	BC#	0	AP	A12	A11	A10	A9	A8	A7	A6	A5	0	0	
11	10000	1010	10	ROW	A31	A30	A13	A15	A14	A29	A28	A27	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	
				COL	A31	A30	A13	0	0	0	BC#	0	AP	A12	A11	A10	A9	A8	A7	A6	A5	0	0	

**Table 15.18 Relation between Address Pins and Logical Addresses (BKADM = B'11)**

AWBK	AWRW	AWCL	DW		BA2	BA1	BA0	MA15	MA14	MA13	MA12	MA11	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0
11	01100	1010	10	ROW	A27	A26	A25	0	0	0	0	A15	A14	A13	A24	A23	A22	A21	A20	A19	A18	A17	A16
				COL	A27	A26	A25	0	0	0	BC#	0	AP	A12	A11	A10	A9	A8	A7	A6	A5	0	0
11	01101	1010	10	ROW	A28	A27	A26	0	0	0	A15	A14	A13	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16
				COL	A28	A27	A26	0	0	0	BC#	0	AP	A12	A11	A10	A9	A8	A7	A6	A5	0	0
11	01110	1010	10	ROW	A29	A28	A27	0	0	A15	A14	A13	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16
				COL	A29	A28	A27	0	0	0	BC#	0	AP	A12	A11	A10	A9	A8	A7	A6	A5	0	0
11	01111	1010	10	ROW	A30	A29	A28	0	A15	A14	A13	A27	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16
				COL	A30	A29	A28	0	0	0	BC#	0	AP	A12	A11	A10	A9	A8	A7	A6	A5	0	0
11	10000	1010	10	ROW	A31	A30	A29	A15	A14	A13	A28	A27	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16
				COL	A31	A30	A29	0	0	0	BC#	0	AP	A12	A11	A10	A9	A8	A7	A6	A5	0	0



### 15.4.13 SDRAM Access and Timing Constraints

In this section, waveforms at the various pins during basic SDRAM access are explained first and then the relation between SDRAM access and the CAS latency (CL, CWL), tRAS, tRFC, tRCD, tRP, tRRD, tWR, tRTP, tRC, READ to WRITE minimum interval, and WRITE to READ minimum interval set using SDRAM timing registers 0 to 19 (DBTR0 to DBTR19) is explained.

#### (1) Basic SDRAM Access

In this section, waveforms at the various pins during basic SDRAM access, including reading, writing, auto-refresh, and self-refresh operations, are explained.

Figure 15.8 shows waveforms for 1-/2-/4-/8-/16-byte reading. In this case, single reading is performed in which the READ command is issued once. In this example, read access processing is executed for bank A after the ACT command is issued, but when there is a page hit, access begins with the issue of the READ command.

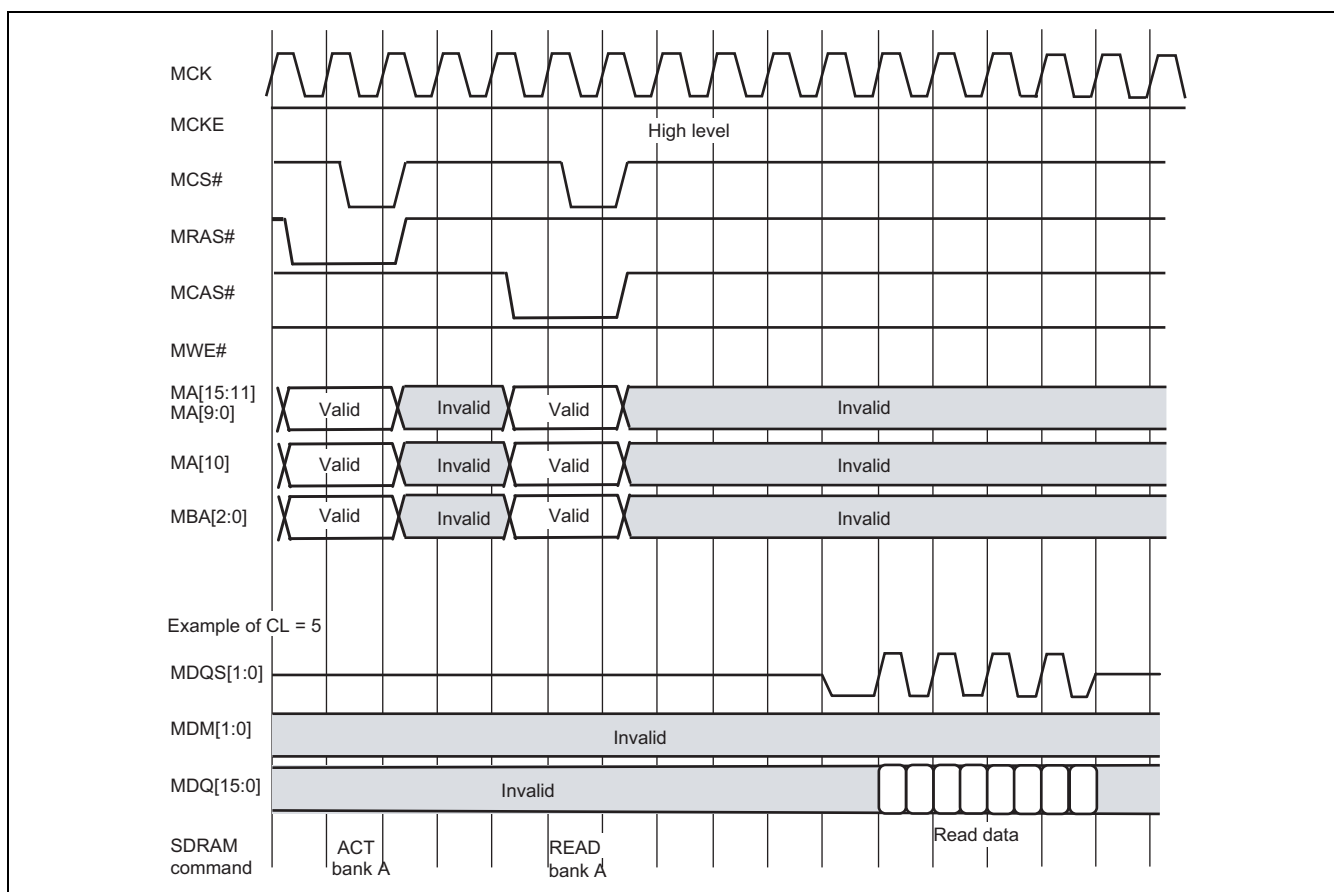
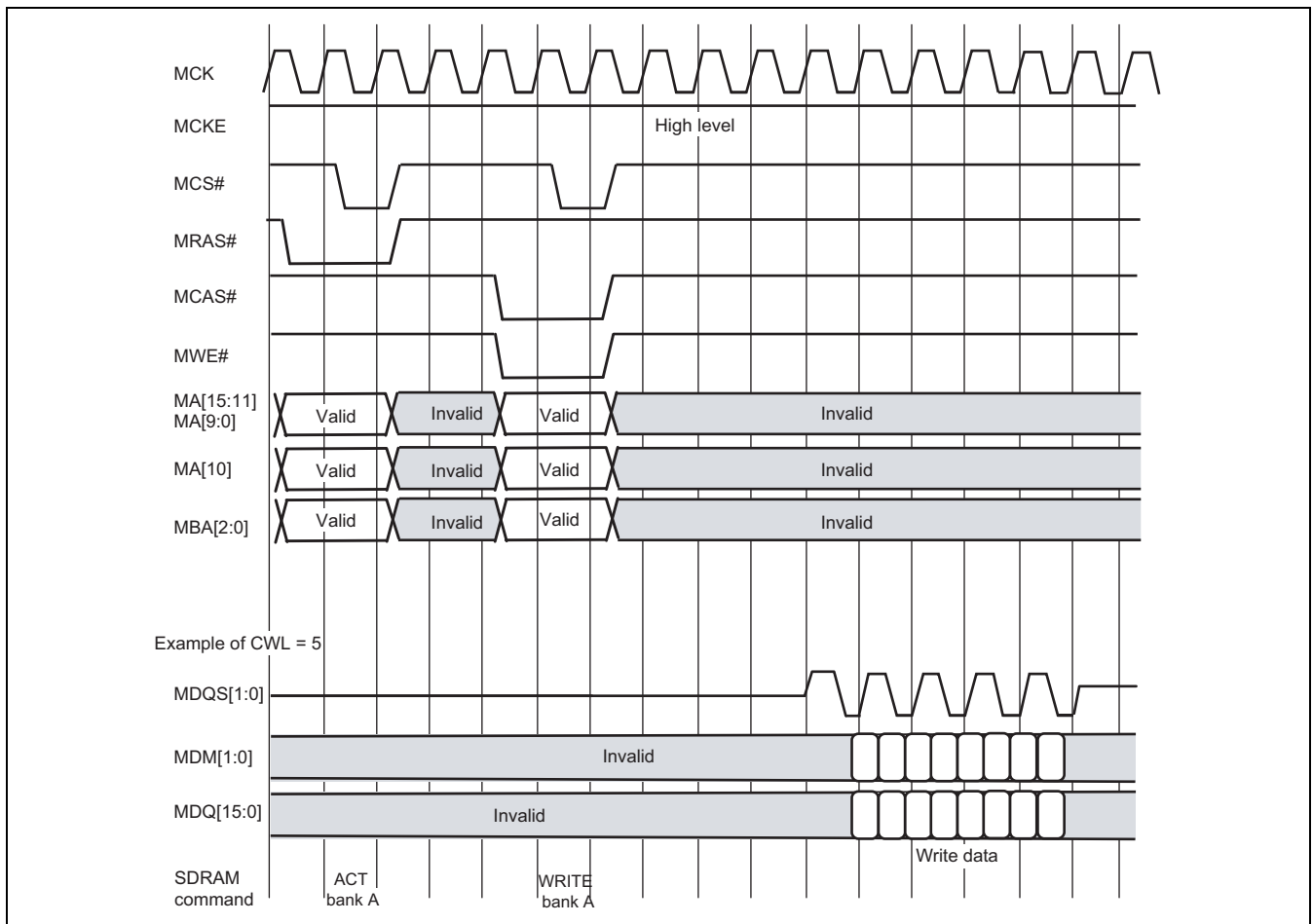


Figure 15.8 Waveforms for 1/2/4/8/16-Byte Reading

Note: In the figure, collective names are used for signals. For example, MCK and MA indicate M0CK/M1CK and M0A/M1A signals, respectively.

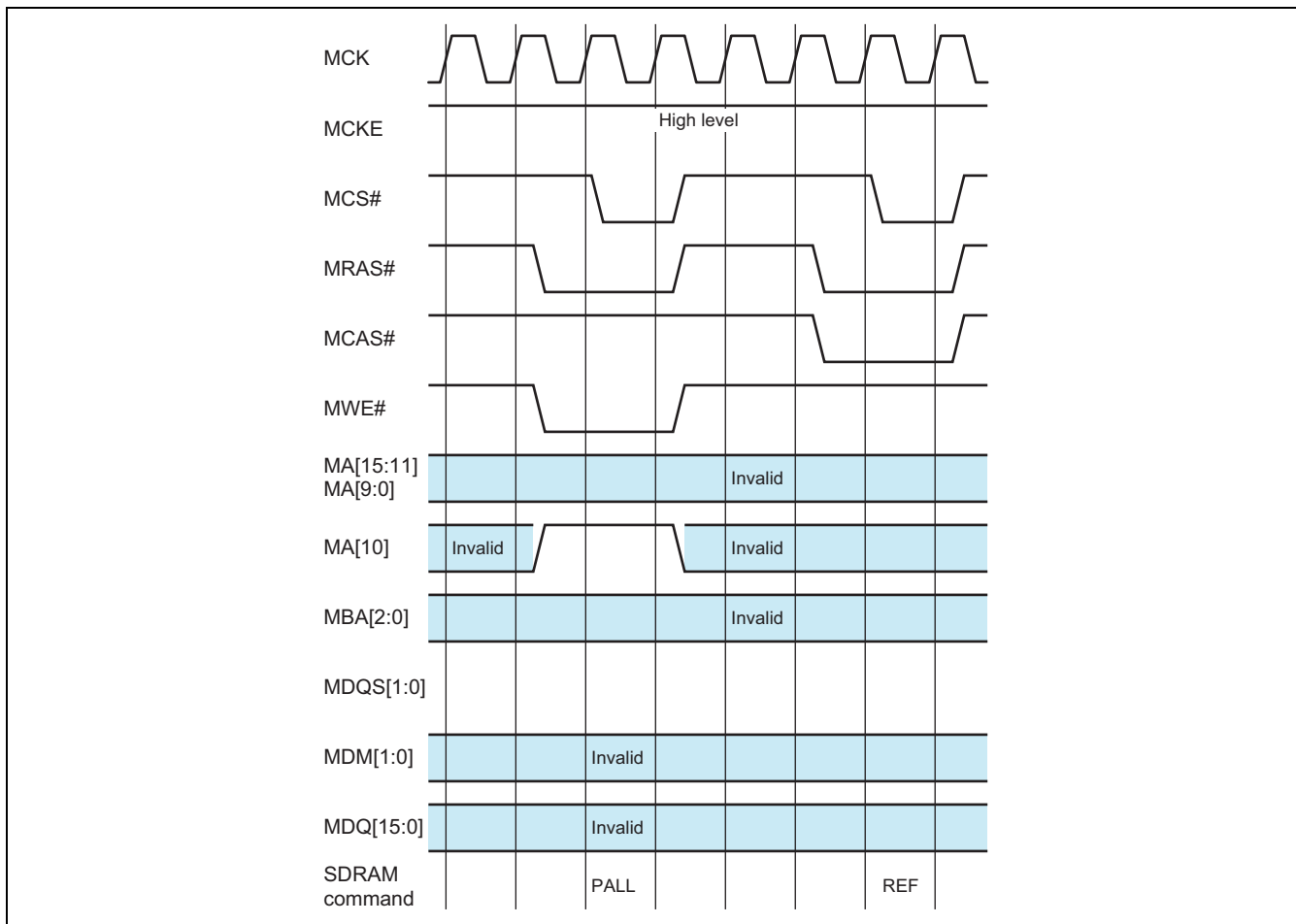
Figure 15.9 shows waveforms for 1-/2-/4-/8-/16-byte writing. In this case, single writing is performed in which the WRITE command is issued once. In this example, write access processing is executed for bank A after the ACT command is issued, but when there is a page hit, access begins with the issue of the WRITE command.



**Figure 15.9 Waveforms for 1/2/4/8/16-Byte Writing**

Note: In the figure, collective names are used for signals. For example, MCK and MA indicate M0CK/M1CK and M0A/M1A signals, respectively.

Figure 15.10 shows waveforms during auto-refresh operation resulting from settings of the refresh configuration registers 0 to 2. The DBSC3 issues a REF command automatically after the PALL command is issued when at least one SDRAM bank is activated before the REF command. Consequently, there is no need to use software to manage precharging of all the banks for the auto-refresh operation.



**Figure 15.10 Auto-Refresh Operation**

Note: In the figure, collective names are used for signals. For example, MCK and MA indicate M0CK/M1CK and M0A/M1A signals, respectively.

Figure 15.11 shows the self-refresh operation. In order to perform self-refresh operation, the specified sequence must be observed. For details, refer to section 15.4.4, Self-Refresh Operation.

When performing processing according to the sequence in section 15.4.4, Self-Refresh Operation, commands to be issued to the SDRAM are those shown in Figure 15.11. Before the transition to self-refresh, the PALL command is issued by software. Then, software is used to issue the REF command and the SRX (self-refresh entry from IDLE) command. The SDRAM is in self-refresh mode until self-refresh is released by software. After issuing the SRX (self-refresh exit) command by software, it is necessary to wait for the time ( $t_{XSNR}$ ) specified in the datasheet for the SDRAM being used until issuing a REF command. A wait example is shown in section 15.4.15, Method for Securing Time Required for Initialization, Self-Refresh Release, etc.

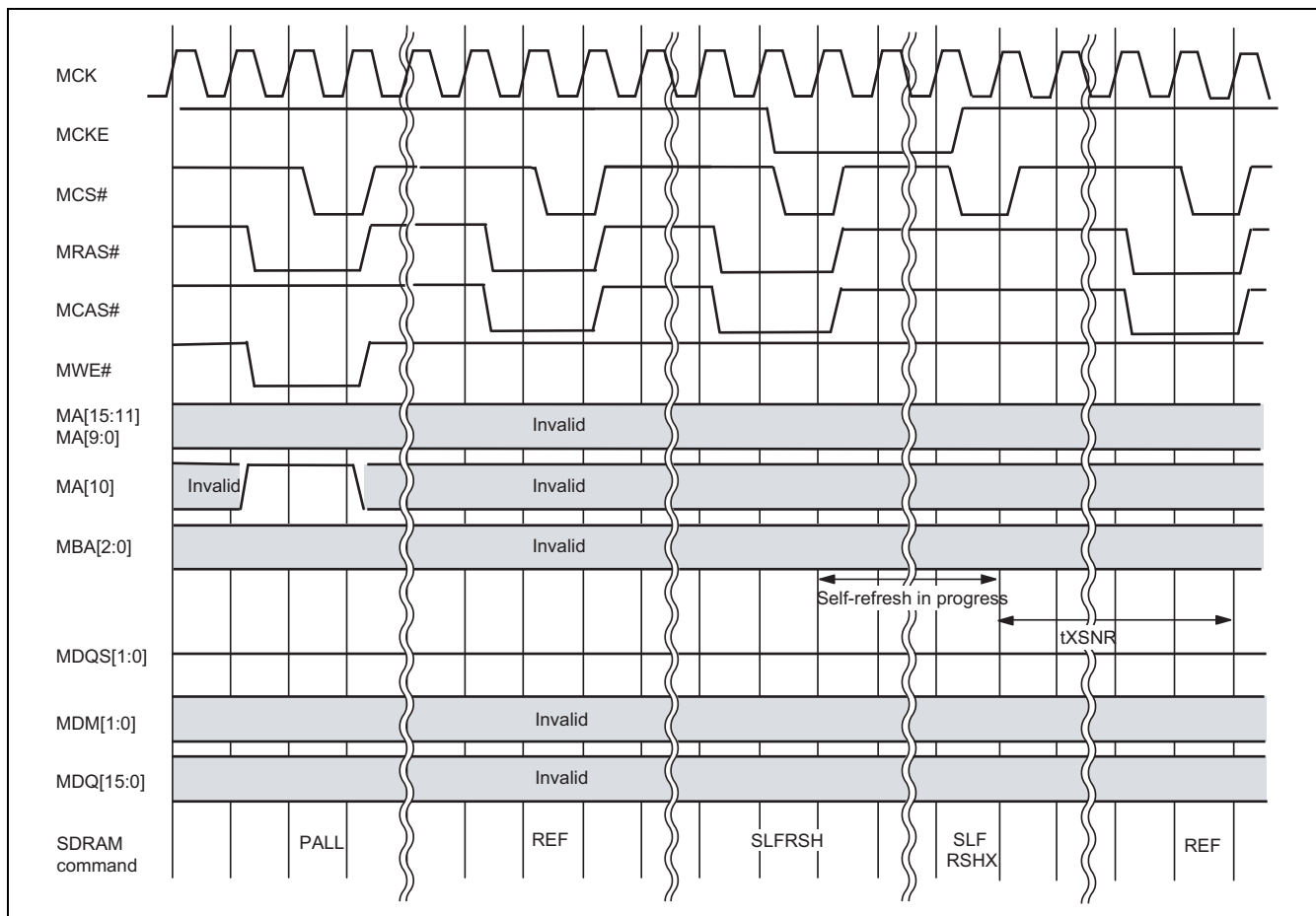


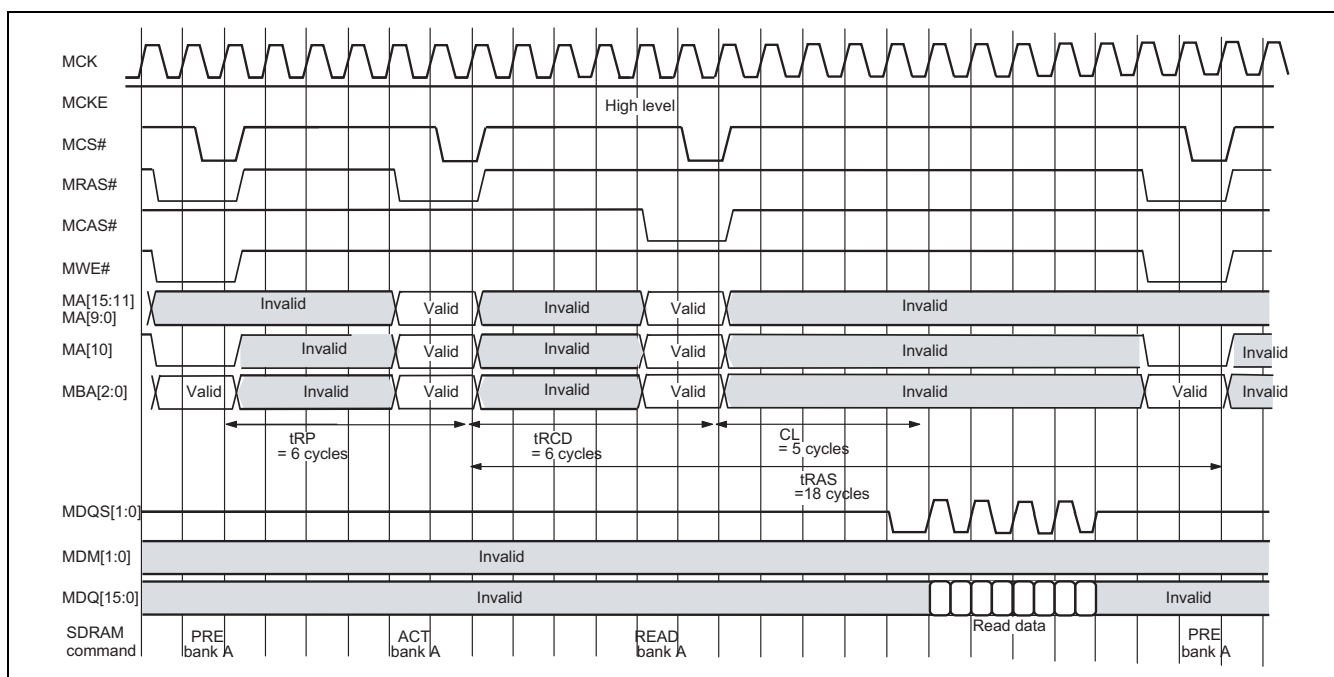
Figure 15.11 Self-Refresh Operation

Note: In the figure, collective names are used for signals. For example, MCK and MA indicate M0CK/M1CK and M0A/M1A signals, respectively.

**(2) Timing Constraints**

Figure 15.12 shows the relation between the settings of CL, tRAS, tRCD, and tRP, and the issuing of commands. Figure 15.13 shows the relation to tRRD and tRTP, Figure 15.14 shows the relation to tWR, Figure 15.15 shows the relation to tRC, Figure 15.16 shows the relation to READ-WRITE, Figure 15.17 shows the relation to WRITE-READ, and Figure 15.18 shows the relation to tRFC.

Figure 15.12 corresponds to operation in a case in which bank A is open, there is read access of bank A, and a page miss occurs. The constraint tRP between the PRE command and ACT command, the constraint tRCD between the ACT command and READ command, and the constraint tRCD between the ACT command and the PRE command are involved. The DBSC3 waits to issue commands until each of the constraints is satisfied.



**Figure 15.12 tRP, tRCD, CL, and tRAS**

Note: In the figure, collective names are used for signals. For example, MCK and MA indicate M0CK/M1CK and M0A/M1A signals, respectively.

Figure 15.13 shows a case in which the pages for both of banks A and B are closed, the page for bank C is open, and a page hit has occurred. When the  $t_{RRD}$  time constraint has been satisfied starting from issue of the ACT command for bank A, the ACT command for bank B is issued. Because time  $t_{RCD}$  has elapsed from the issue of the ACT command for bank A, a READ command can be used. The READ command has a burst length of 8, so after four cycles a READ command for bank B can be issued. A further four cycles later, a READ command for bank C can be issued. However, the next request is access for which bank C must be closed, and so after the elapse of time  $t_{RTP}$ , a PRE command is issued.

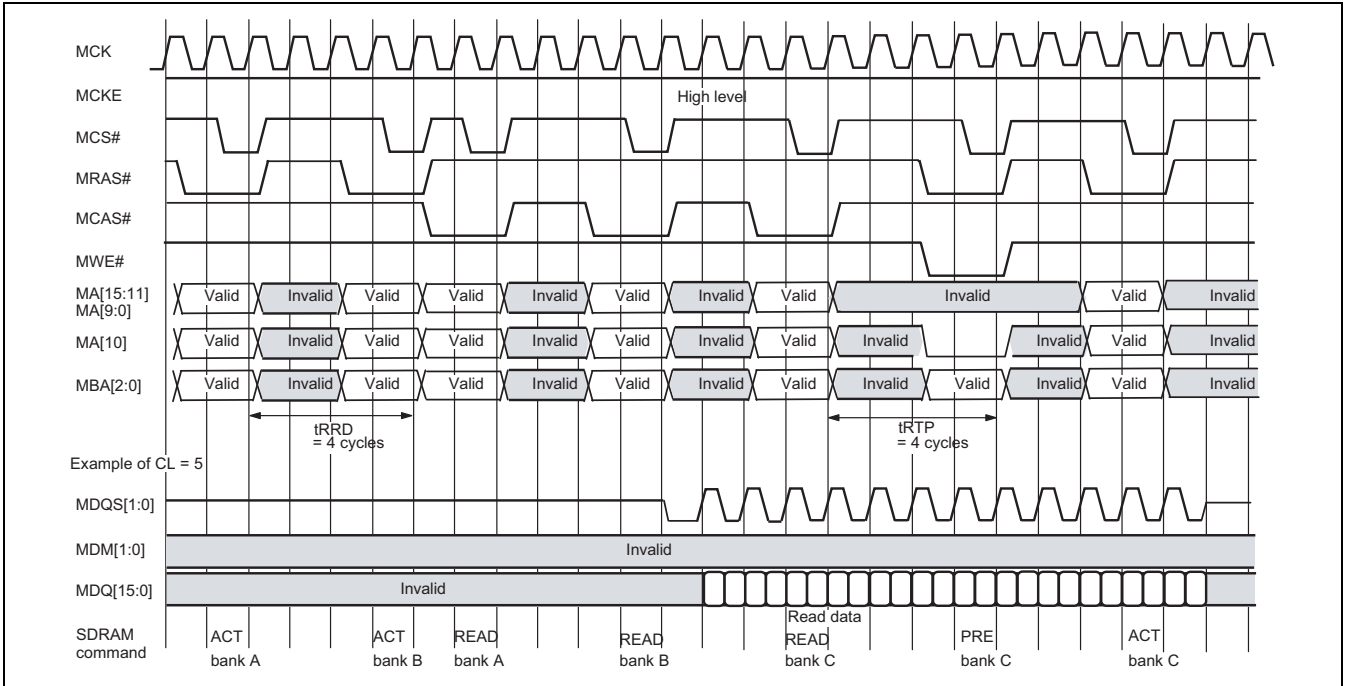


Figure 15.13  $t_{RRD}$  and  $t_{RTP}$

Note: In the figure, collective names are used for signals. For example, MCK and MA indicate M0CK/M1CK and M0A/M1A signals, respectively.

Figure 15.14 shows a case in which, after a write request, access occurs requiring that bank B be closed. After the issue of a WRITE command, it is necessary to wait for time  $t_{WR}$  or longer after output of the write data before issuing a PRE command.

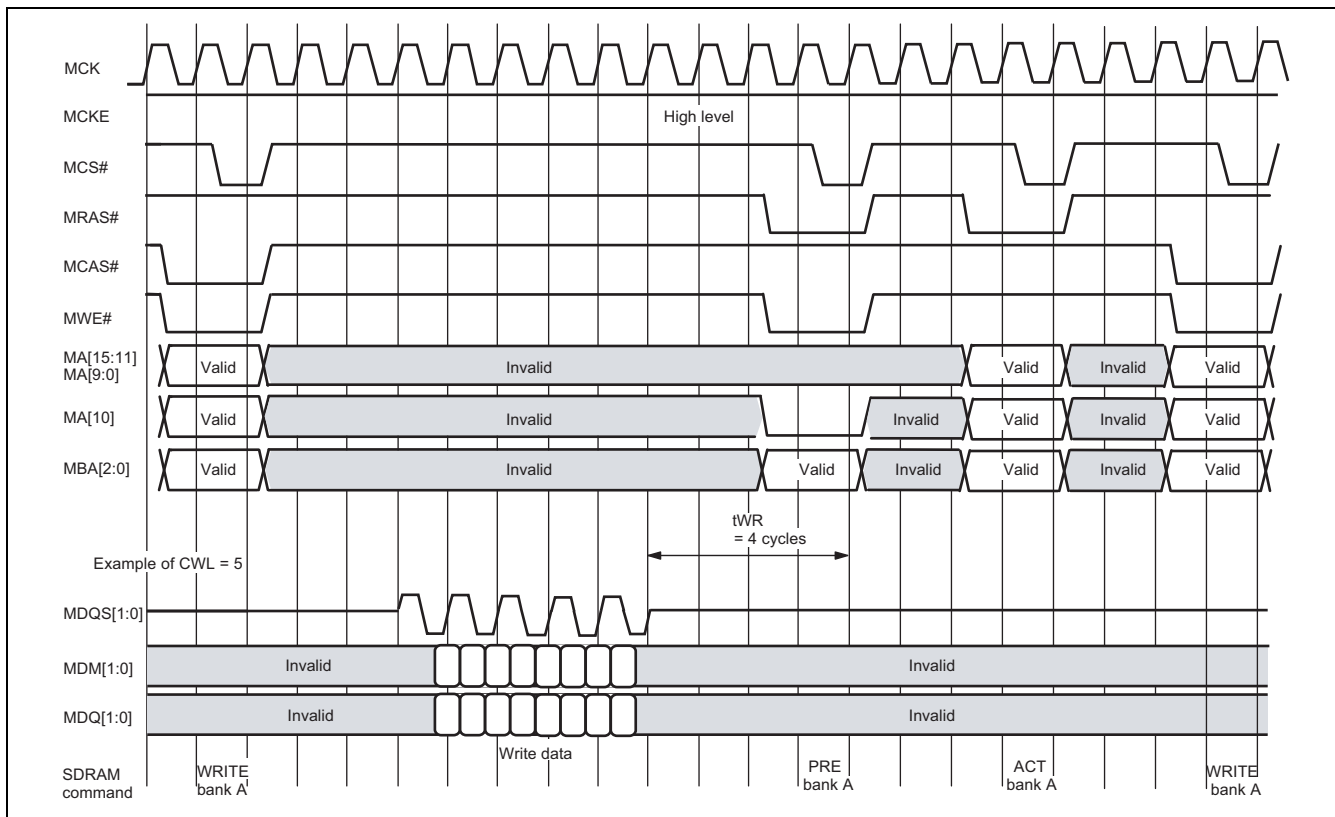


Figure 15.14  $t_{WR}$

Note: In the figure, collective names are used for signals. For example, MCK and MA indicate M0CK/M1CK and M0A/M1A signals, respectively.

Figure 15.15 shows an example of performing auto-refresh after read access of bank A, the page for which had been closed. After issuing an ACT command and READ command for bank A and performing data reading, a PALL command must be used to close all banks in order to perform auto-refresh. In order to issue the PREA command, the tRAS time constraint must be satisfied and issuing of the PREA command is delayed until this time. Then, when issuing the REF command, both of time constraints tRPA and tRC must be satisfied simultaneously. When these constraints are both satisfied, the REF command is issued and auto-refresh is performed.

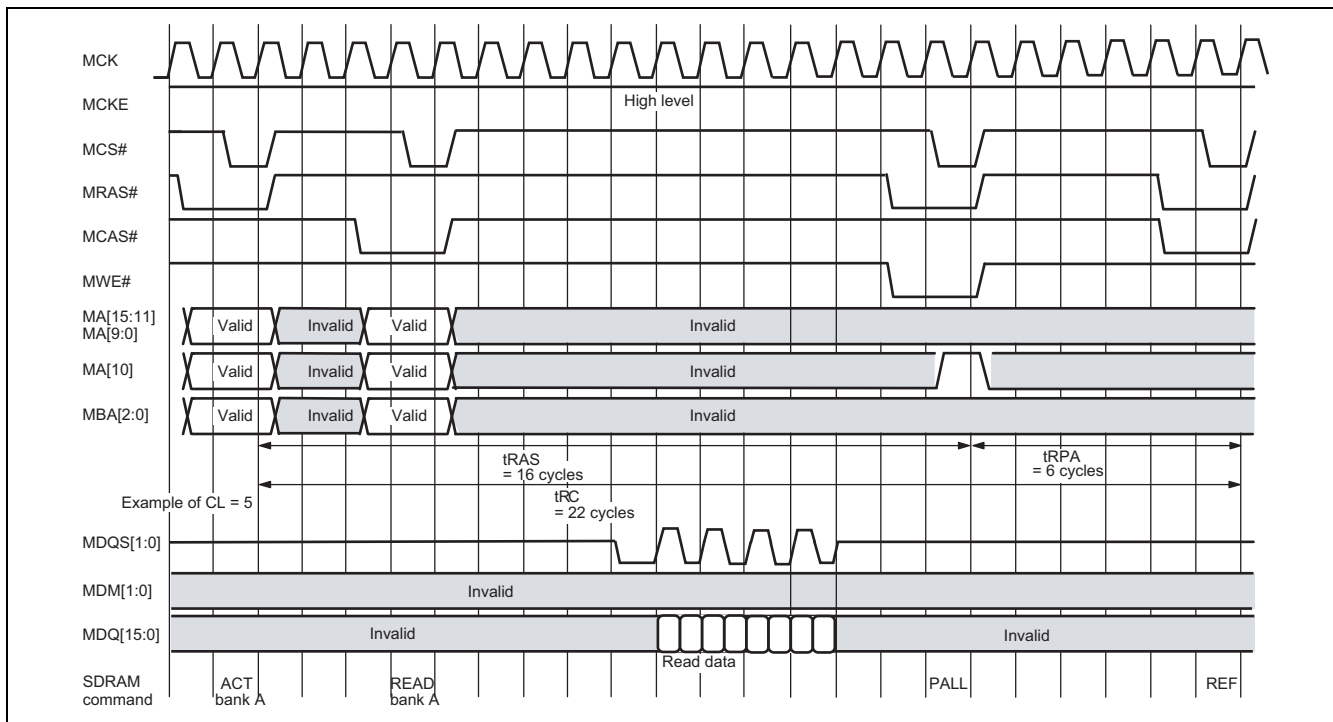
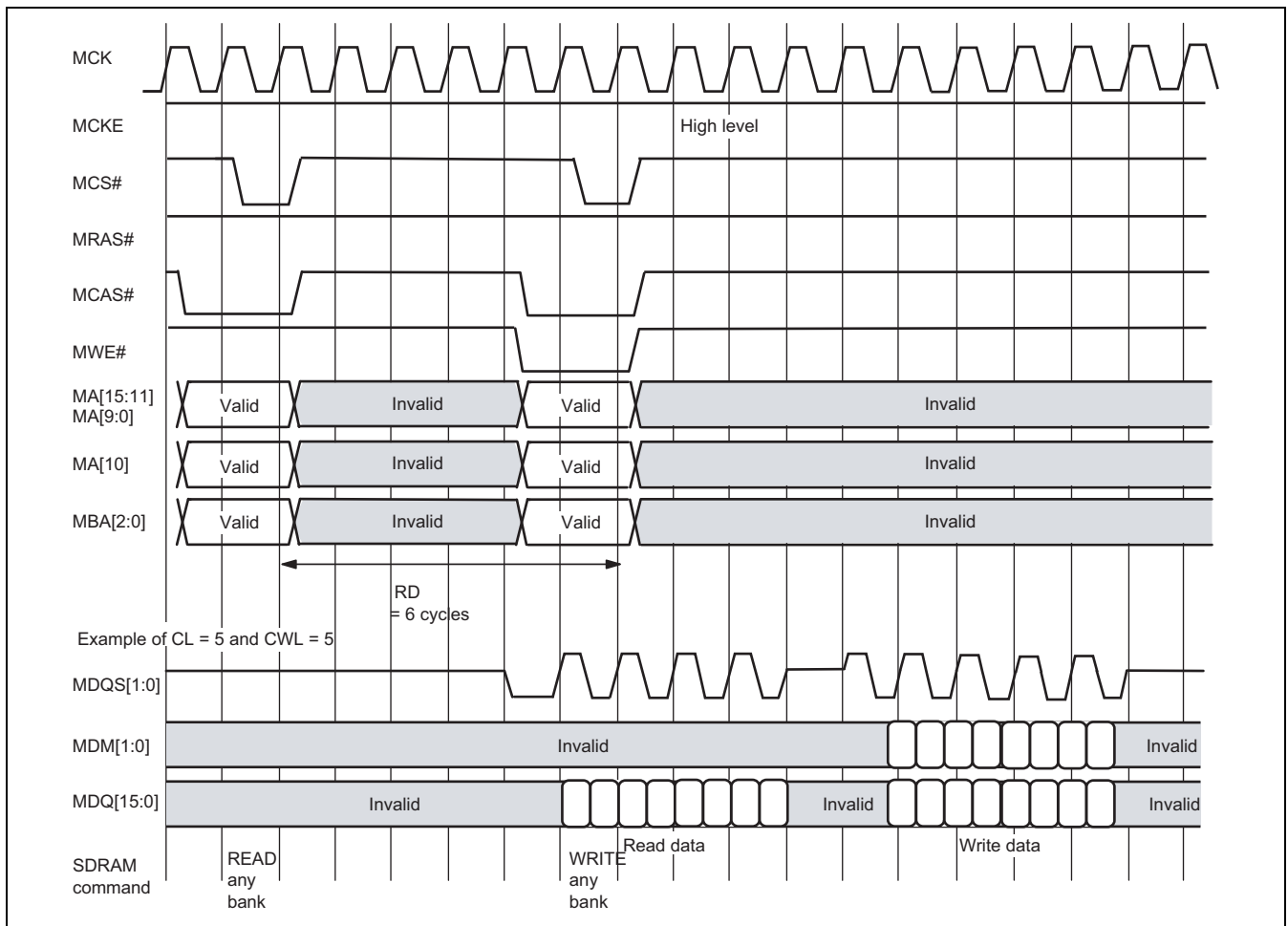


Figure 15.15 tRC

Note: In the figure, collective names are used for signals. For example, MCK and MA indicate M0CK/M1CK and M0A/M1A signals, respectively.



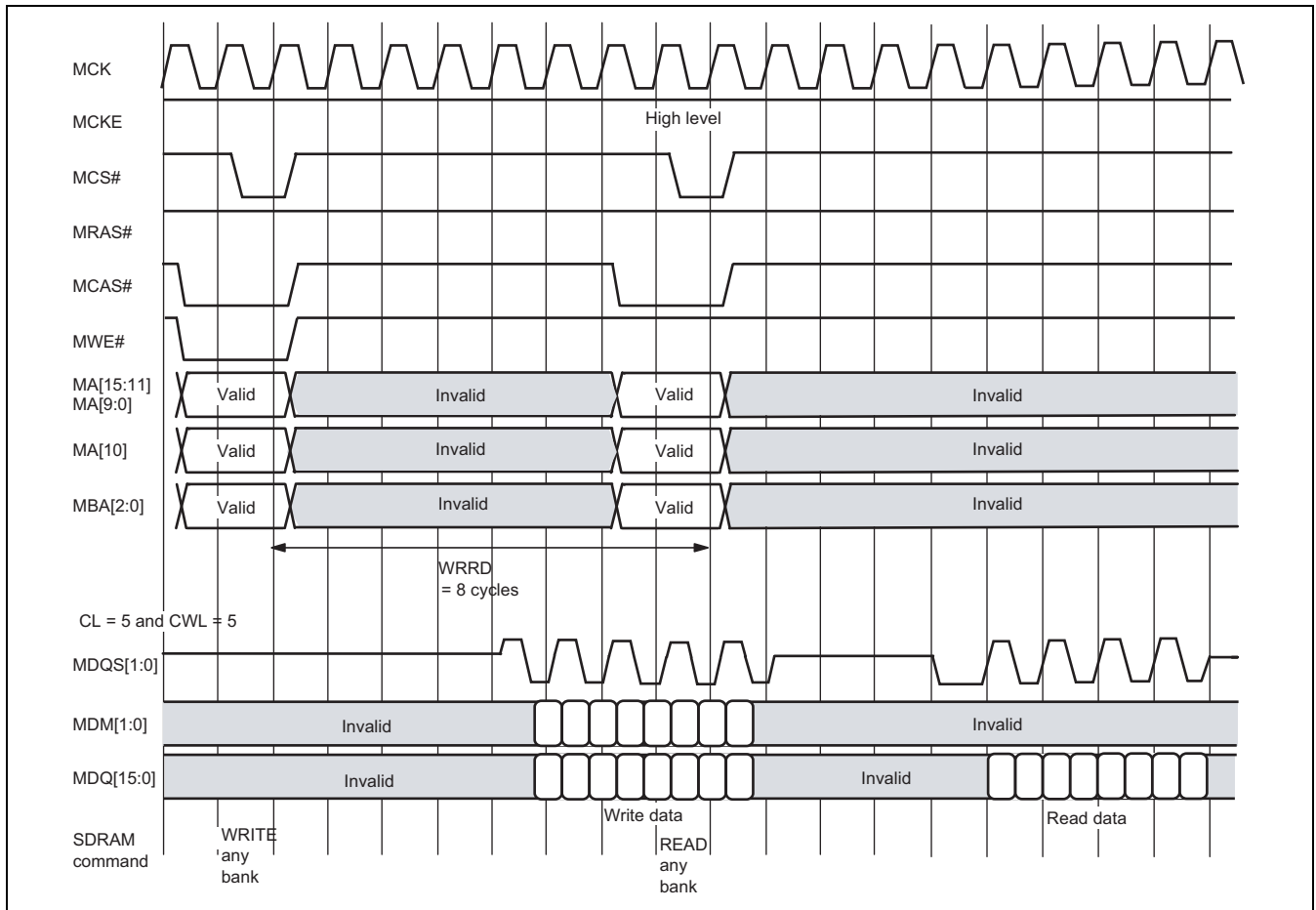
Figure 15.16 shows an example of a case in which, after issuing a READ command, a WRITE command is issued. In order to issue the WRITE command after issuing the READ command, the DBSC3 waits for a minimum time stipulated by the RDWR bits.



**Figure 15.16 READ-WRITE Minimum Time**

Note: In the figure, collective names are used for signals. For example, MCK and MA indicate M0CK/M1CK and M0A/M1A signals, respectively.

Figure 15.17 shows an example of a case in which, after issuing a WRITE command, a READ command is issued. In order to issue the READ command after issuing the WRITE command, the DBSC3 waits for a minimum time stipulated by the WRRD bits.



**Figure 15.17 WRITE-READ Minimum Time**

Note: In the figure, collective names are used for signals. For example, MCK and MA indicate M0CK/M1CK and M0A/M1A signals, respectively.

Figure 15.18 shows an example of a case in which, after issuing a REF command, a READ request is issued. In order to issue the ACT command after issuing the REF command, the DBSC3 waits for a time stipulated by tRFC.

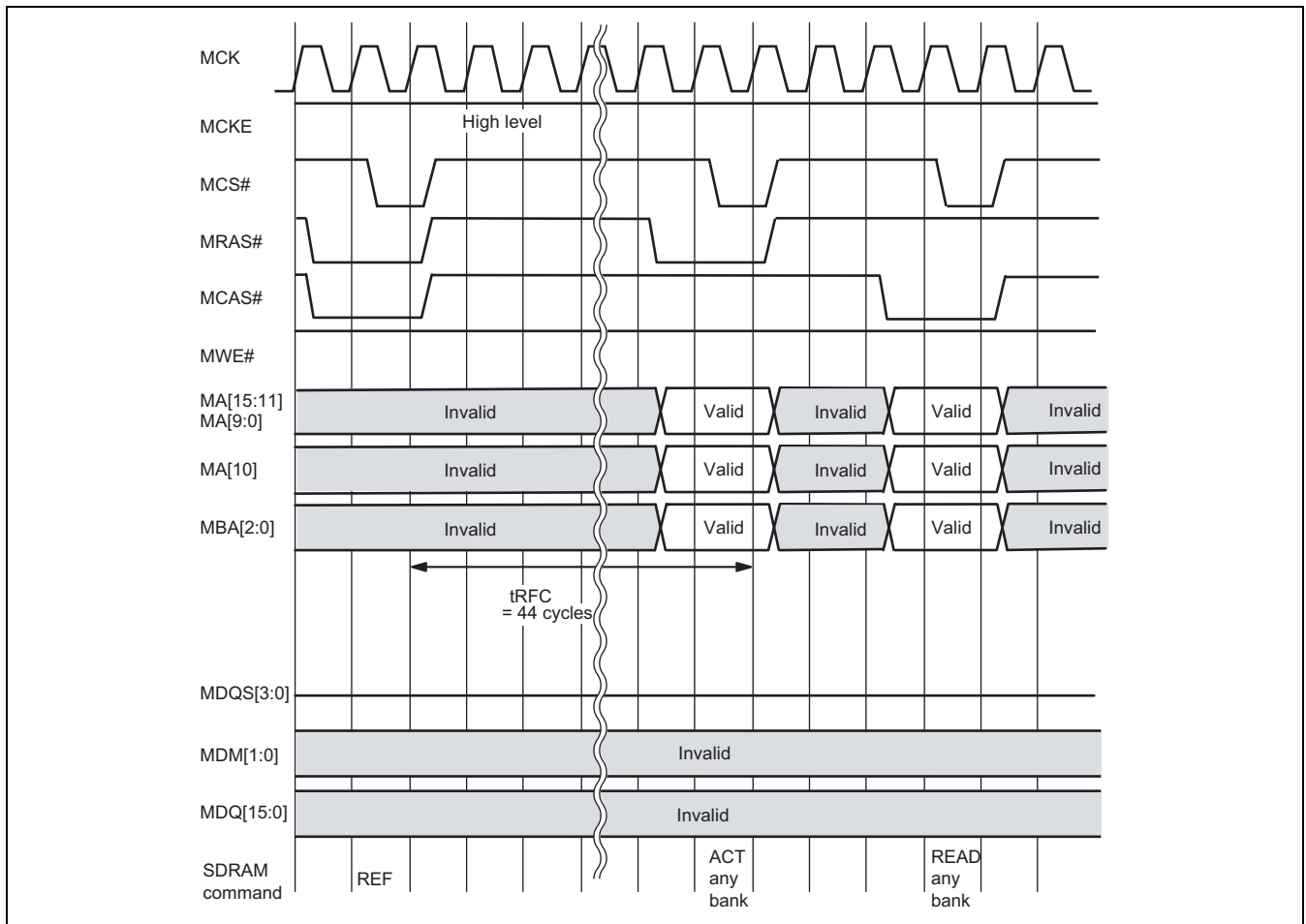
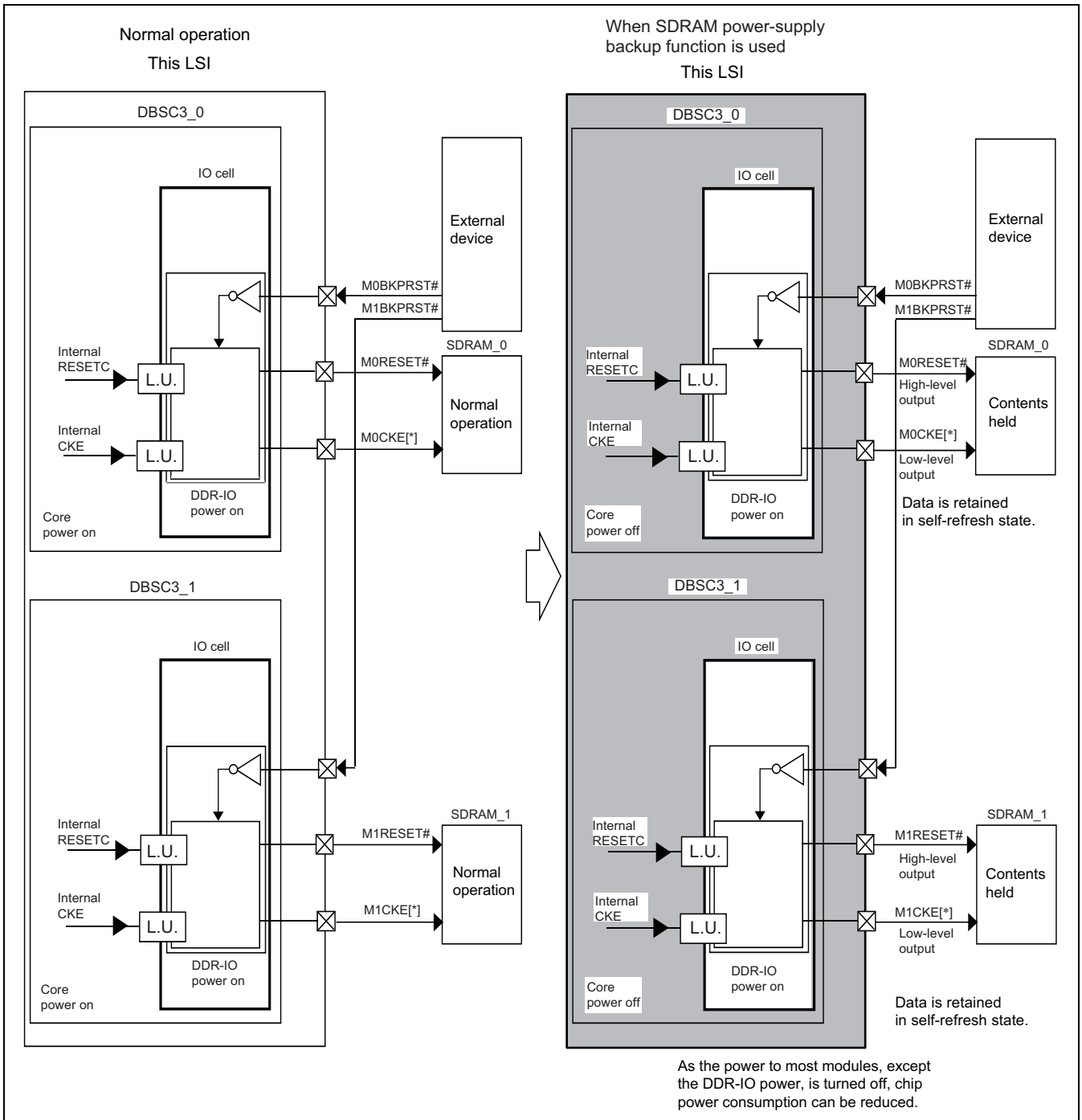


Figure 15.18 tRFC

Note: In the figure, collective names are used for signals. For example, MCK and MA indicate M0CK/M1CK and M0A/M1A signals, respectively.

**15.4.14 SDRAM Power-Supply Backup Function**

The SDRAM power-supply backup function utilizes the SDRAM self-refresh state to turn off the power supply to core power unit of the DBSC3 module, while maintaining the data in the SDRAM. By using this function, not only is it possible to cut power consumption, but the time needed to transfer data once again to the SDRAM can be eliminated, since the valid data is maintained within the SDRAM (see Figure 15.19). In order to realize this function, in addition to the LSI device containing the DBSC3, a separate external control circuit (microcomputer or similar) is needed to monitor the states of this LSI and the memory.



**Figure 15.19 SDRAM Power-Supply Backup Function**

In order to implement the power-supply backup function, a control signal M0(1)BKPRST# is necessary to hold M0(1)CKE[1:0] at low level even when power other than for the DDR-I/O is turned off. When this signal is at low level,

the M0(/1)CKE[1:0] pins can be held at low level even when the power supply within the chip is in the turned-off state. After using DBSC3\_0(/1) to put the SDRAM into the self-refresh state, by using this M0(/1)BKPRST# signal to hold the M0(/1)CKE[1:0] signals at low level, the SDRAM self-refresh state can be maintained even when the power supply in the chip is turned off.

To release the power-supply backup state, perform a power-on reset. As a result, the DBSC3\_0(/1) registers are initialized, and so the self-refresh control circuit is also initialized. In order to put the SDRAM into the self-refresh state before power-on reset and also during power-on reset, when the internal CKE signal is indefinite, the M0(/1)BKPRST# signal must be held at low level. Power-on reset causes the DBSC3\_0(/1) to fix the internal CKE signal at low level, so that after power-on reset is released the M0(/1)BKPRST# signal is raised to high level. (If not in the power-supply backup state, M0(/1)BKPRST# is always at high level and there is no problem).

Thus the power-supply backup state is released through power-on reset, and so the software must decide whether the normal SDRAM initialization sequence is necessary, or whether the LSI was in the power-supply backup state. In order to perform this decision, after power-on reset, the software monitors the external device, and judges whether the state should be the power-supply backup state or whether SDRAM initialization is necessary. Before using register settings to send M0(/1)CKE[1:0] to high level, it is necessary to signify a state other than the power-supply backup state. (After driving the M0(/1)CKE[1:0] pins to high level, upon power-on reset the data within the SDRAM is destroyed. Hence if a state other than power-supply backup state is not set in advance, there is the danger that the destroyed data may be treated as the correct data).

Table 15.19 shows the memory areas in which data cannot be retained in SDRAM power-supply backup mode.

**Table 15.19 Memory Areas in Which Data Cannot Be Retained in SDRAM Power-Supply Backup Mode**

Channel Mode	Memory Area (40-Bit Mode)
64 bits × one channel	H'01_0000_0000 to H'01_0000_00FF
32 bits × two channels	H'01_0000_0000 to H'01_0000_007F H'02_0000_0000 to H'02_0000_007F

In this way, procedures are used to make a transition to and release from the SDRAM power-supply backup mode; if these procedures are not followed, the data in the SDRAM may be destroyed.

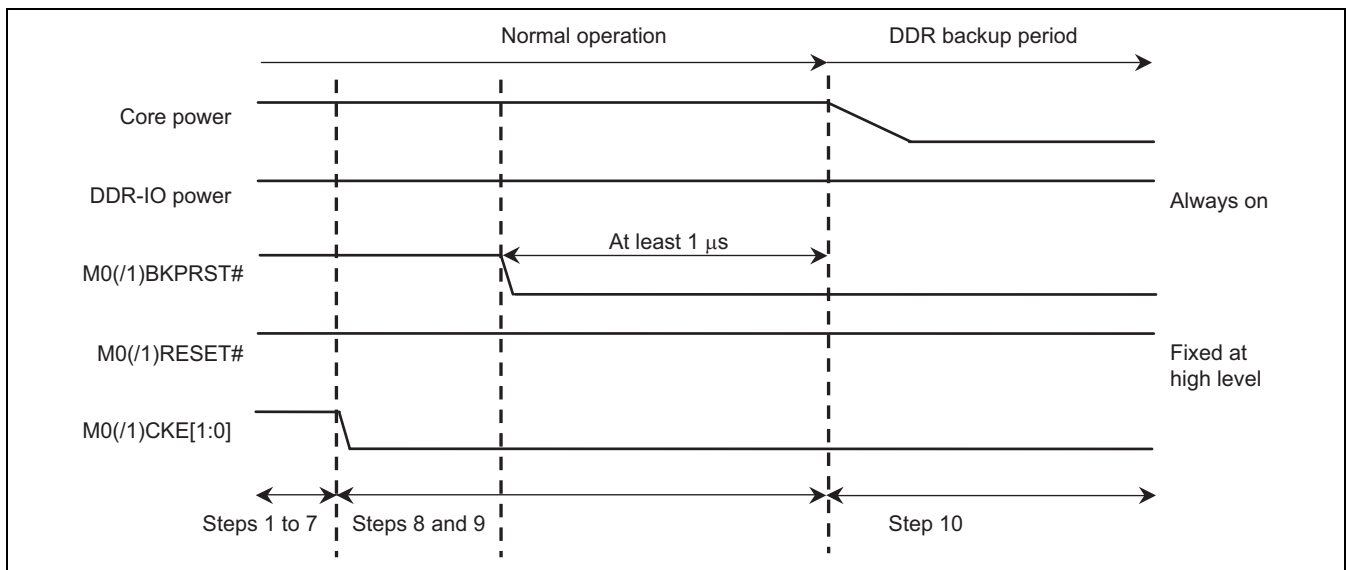
These procedures are explained below.

#### (1) Transition to SDRAM Power-Supply Backup Mode

The following method is used.

1. Confirm that the controller is not being accessed. The time required for transition must not exceed the auto-refresh interval requested by the SDRAM by interrupts or some other causes.
2. Set the ACCEN bit in the SDRAM Access enable register (DBACEN) to 0 (access disabled).
3. Use the manual command-issuing register (DBCMD) to issue a PREA (precharge all banks) command. The value written to this register should be OPC = PreA, ARG = 0.
4. Use the manual command-issuing register (DBCMD) to issue a Self-Refresh Entry command. The value written to this register should be OPC = SREn, ARG = 0.
5. Set the ARFEN bit in the auto-refresh enable register (DBRFEN) to 0.
6. Use the manual command-issuing register (DBCMD) to insert a time to wait for the clock to stop. The value written to this register should be OPC = Wait, ARG = tCKSRE (normally, max {5, 10 ns}).
7. Read the operation completion waiting register (DBWAIT) and wait for the response.
8. Write H'0000A55A to the PHY unit lock register (DBPDLCK).
9. Write H'0000000E to the PHY unit address register (DBPDRGA).
10. Write H'33C03813 to the PHY unit access register (DBPDRGD).

11. Set the M0(/1)BKPRST# signal to low level, wait for at least 1  $\mu$ s, and then turn off the unnecessary power, other than the DBSC3\_0(/1) DDR-IO power.



**Figure 15.20 Transition to SDRAM Power-Supply Backup Mode**

## (2) Recovery from SDRAM Power-Supply Backup Mode

Recover form SDRAM Power-Supply Backup Mode can be executed by similar way for the sequence for "starting the system" explained in the section 15.4.3.1, Starting the System. The following shows difference between them.

Depending on the negate timing M0/1BKPRST#, there are two methods to do this;

### Example:

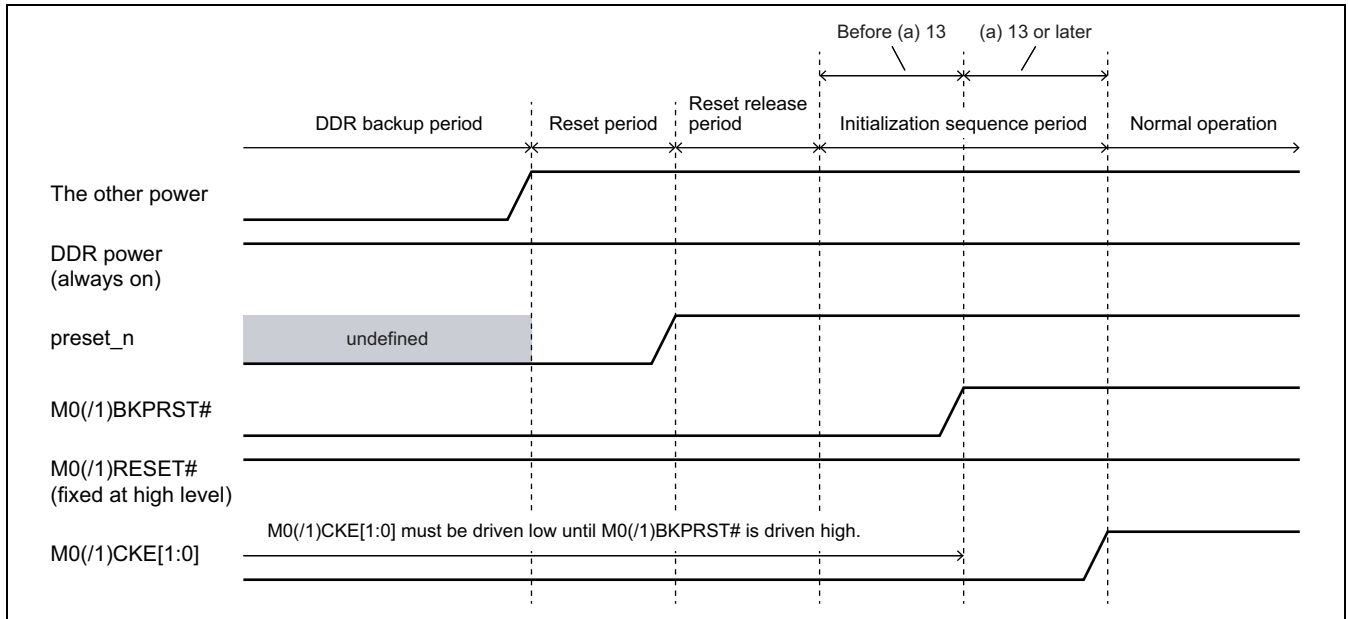
- M0/1BKPRST# is driven high during the initialization sequence.
- There is no timing constraint in this case, however, drive M0/1BKPRST# high after the setting for the M0/1RESET# signals, and before "(a) 13" in "(1) 64 Bits  $\times$  1-ch Mode" in section 15.4.3.1, Starting the System..

In the example above, No.26 in "(a) 13" in "(1) 64 Bits  $\times$  1-ch Mode" in section 15.4.3.1, Starting the System, is modified as follows.

26. Write H'00000101 to the PHY unit access register (DBPDRGD).

In the example above, the following PHY settings are added before "(a) 13" in "(1) 64 Bits  $\times$  1-ch Mode" in section 15.4.3.1, Starting the System.

1. Write H'00000060 to the PHY unit address register (DBPDRGA).
2. Write H'1244DCBD to the PHY unit access register (DBPDRGD). (For DDR3)  
Write H'12651DC1 to the PHY unit access register (DBPDRGD). (For DDR3L)
3. Write H'40000000 to the PHY unit access register (DBPDRGD).
4. Drive M0(/1)BKPRST# high



**Figure 15.21 Recovery from SDRAM Power Supply Backup Mode (Example)**

**(3) A method to stop the return from a power backup state, and to return to a power backup state.**

It can just shift to a power backup state before changing M0(/1)BKPRST# to 'high level' from 'low'.

When M0(/1)BKPRST# signal change to 'high level' from 'low'.

**(a) When processing does not arrive at the section 15.4.3.1 (1)-(c) 27.**

1. Write H'00000004 to the PHY unit address register (DBPDRGA).
2. Read the PHY unit access register (DBPDRGD) and wait until 1 is read from bit 0.
3. Write H'0000000E to the PHY unit address register (DBPDRGA).
4. Write H'33C03813 to the PHY unit access register (DBPDRGD).
5. Set the M0(/1)BKPRST# signal to low level.
6. Return to a power supply backup state.

**(b) When processing goes to section 15.4.3.1 (1)-(c) 27.**

It cannot stop.

**(c) When there is initialization processing from section 15.4.3.1 (1)-(c) 27 to 15.4.3.1 (1)-(c) 30.**

1. Write H'00000001 to the PHY unit address register (DBPDRGA).
2. Write H'80000000 to the PHY unit access register (DBPDRGD).
3. Write H'00000004 to the PHY unit address register (DBPDRGA).
4. Read the PHY unit access register (DBPDRGD) and wait until 1 is read from bit 0.
5. Set DBTR4, DBTR14, and DBTR15 (If do not yet set it).
6. Set the ACCEN bit in the SDRAM Access Enable Register (DBACEN) to 0 (access disabled).
7. Use the manual command-issuing register (DBCMD) to issue a PREA (precharge all banks) command.  
The value written to this register should be OPC = PreA and ARG = 0.
8. Use the manual command-issuing register (DBCMD) to issue a Self-Refresh Entry command.  
The value written to this register should be OPC = SREn and ARG = 0.
9. Set the ARFEN bit in the auto-refresh enable register (DBRFEN) to 0.
10. Write H'0000000E to the PHY unit address register (DBPDRGA).
11. Write H'33C03813 to the PHY unit access register (DBPDRGD).
12. Set the M0(/1)BKPRST# signal to low level.
13. Return to a power supply backup state.

**15.4.15 Method for Securing Time Required for Initialization, Self-Refresh Release, etc.**

When using DBSC3 register settings to set initialization or release the self-refresh state, there is a need to wait for the time defined in the SDRAM specifications. To reserve this waiting time, read from the DBSC3 status register 1 (DBSTATE1). When this is done, at least seven memory clock cycles elapse. For 266-MHz operation, about 26.25 ns elapse upon one DBSTATE1 read. This can be utilized to secure the required time, by repeating read access the necessary number of times.



## 15.5 Notes on Board Design

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

### 15.5.1 Connection of M0ZQ or M1ZQ Pin

A resistor having the following value should be connected to the M0ZQ or M1ZQ pin outside this LSI.

DDR3-SDRAM: 240  $\Omega$  ( $\pm$  1%)

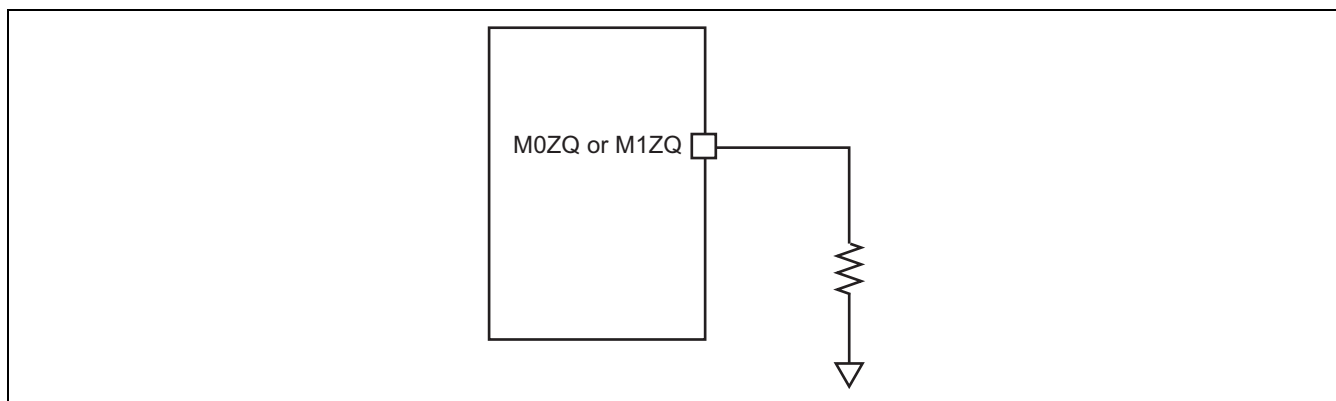


Figure 15.22 Connection of M0ZQ or M1ZQ Pin

### 15.5.2 Connection of PLL Power Supply and GND Pins

A resistor and a capacitor having the following values should be externally connected to the PLL power supply and GND pins as a noise filter.

Resistance: 1  $\Omega$

Capacitance: 2.2  $\mu$ F

PLL power supply pins: VDDQ\_M0(/1)APLL, VDDQ\_M1MPLL, VDDQ\_M(0/1)DPLL0 to VDDQ\_M(0/1)DPLL3

PLL GND pins: VSSQ\_M0(/1)APLL, VSSQ\_M1MPLL, VSSQ\_M(0/1)DPLL0 to VSSQ\_M(0/1)DPLL3

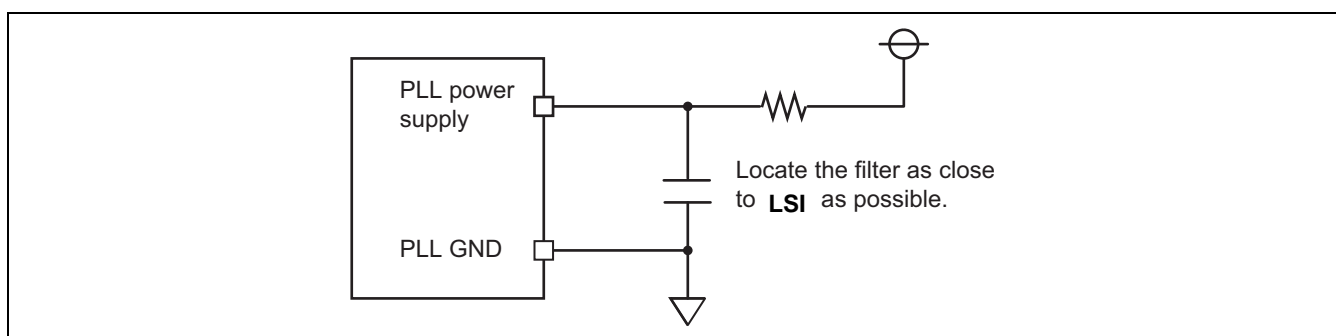


Figure 15.23 Connection of PLL Power Supply and GND Pins

## 15.6 Notes on 16 bit Mode Usage for Initial Settings



### (1) 16 Bits × 1-ch Mode

The initialization sequence for 16 bits × 1-ch mode can be executed by similar way for 64 bits × 1-ch mode. Differences between them are as follows.

The following sequence should be added below the line No.31 of subsection "(c) PHY Setting 1" in In the section "(1) 64 Bits × 1-ch Mode" to stop the DBSC3\_1 side macro and byte lane 2 and 3 of DDR-PHY;

32. Write H'000000B0 to the PHY unit address register (DBPDRGA).
33. Write H'7C020EB0 to the PHY unit access register (DBPDRGD).
34. Write H'000000C0 to the PHY unit address register (DBPDRGA).
35. Write H'7C020EB0 to the PHY unit access register (DBPDRGD).
36. Write H'000000D0 to the PHY unit address register (DBPDRGA).
37. Write H'7C020EB0 to the PHY unit access register (DBPDRGD).
38. Write H'000000E0 to the PHY unit address register (DBPDRGA).
39. Write H'7C020E80 to the PHY unit access register (DBPDRGD).
40. Write H'00000090 to the PHY unit address register (DBPDRGA).
41. Write H'7C020EB0 to the PHY unit access register (DBPDRGD).
42. Write H'000000A0 to the PHY unit address register (DBPDRGA).
43. Write H'7C020EB0 to the PHY unit access register (DBPDRGD).

<b>RZ/G1H</b>	<b>RZ/G1N</b>
<b>RZ/G1M</b>	<b>RZ/G1E</b>

## 15.7 Notes on Address MAP

### 15.7.1 Address Map (Over view)

#### (1) Legacy 2-Gbyte DRAM space

Legacy 2-Gbyte DRAM space (from H'00\_4000\_0000 to H'00\_BFFF\_FFFF) is assigned to the DBSC3\_0 space (from H'01\_0000\_0000) to H'01\_7FFF\_FFFF). If you want to access to other space, access in 40 bits address space.

### 15.7.2 RZ/G1H/M Address Map

#### (1) 32 Bits × 2-ch (DBSC3\_0: 1 Gbyte, DBSC3\_1: 1 Gbyte)

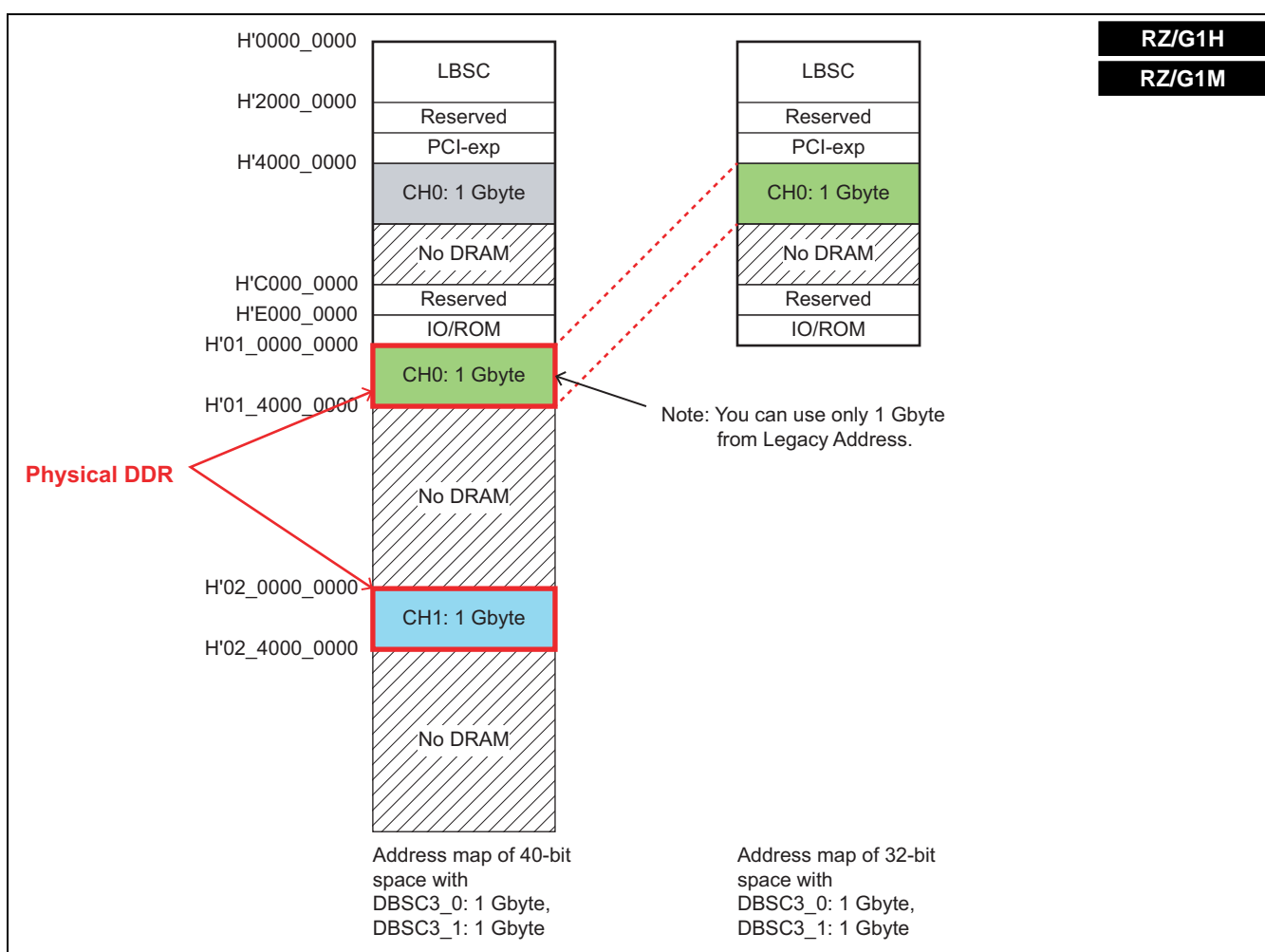


Figure 15.24 RZ/G1H/M Address Map with DBSC3\_0: 1 Gbyte, DBSC3\_1: 1 Gbyte

(2) 32 Bits × 2-ch (DBSC3\_0: 2 Gbytes, DBSC3\_1: 2 Gbytes)

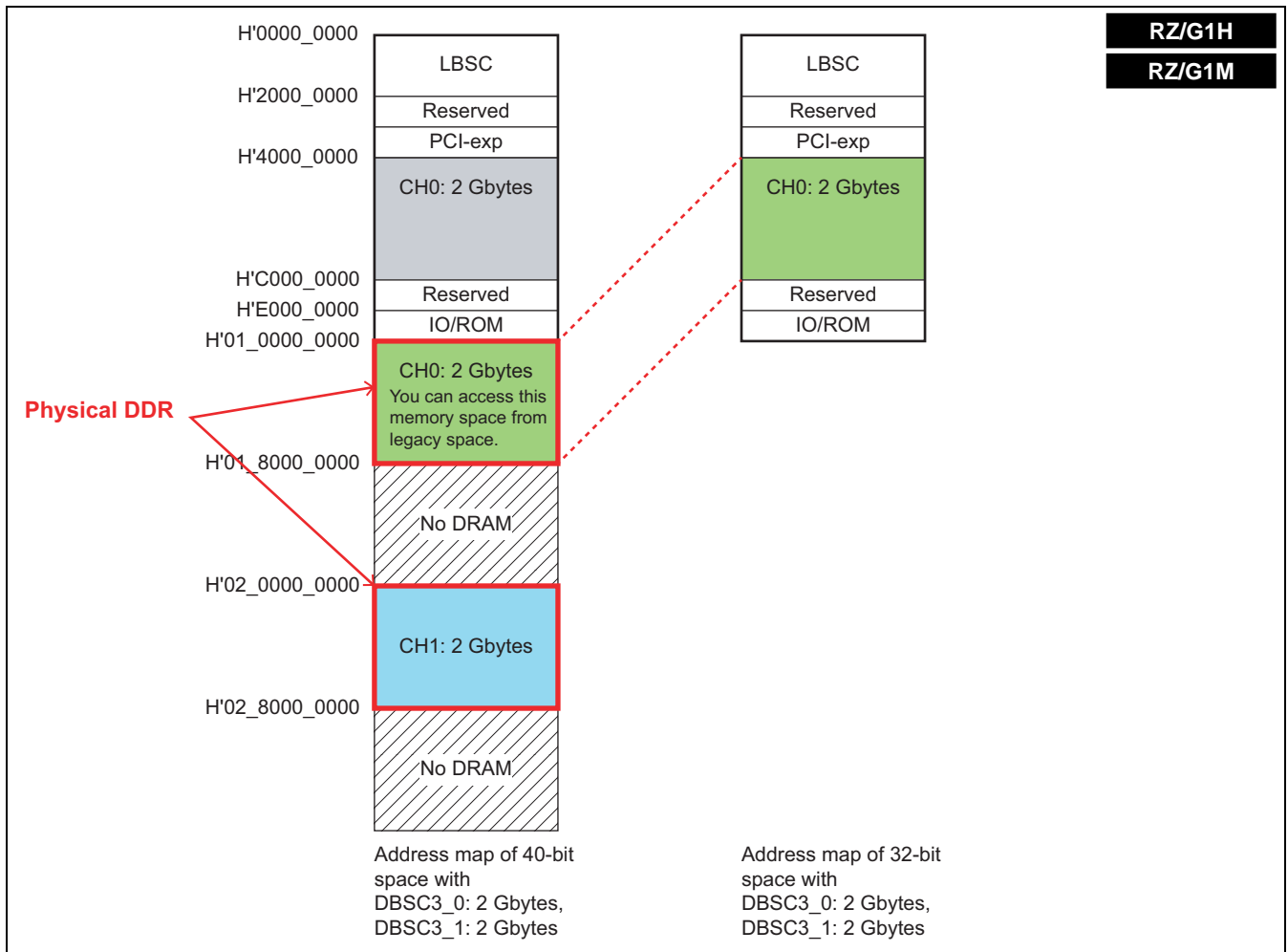


Figure 15.25 RZ/G1H/M Address Map with DBSC3\_0: 2 Gbytes, DBSC3\_1: 2 Gbytes

(3) 64 Bits × 1-ch (DBSC3\_0: 2 Gbytes)

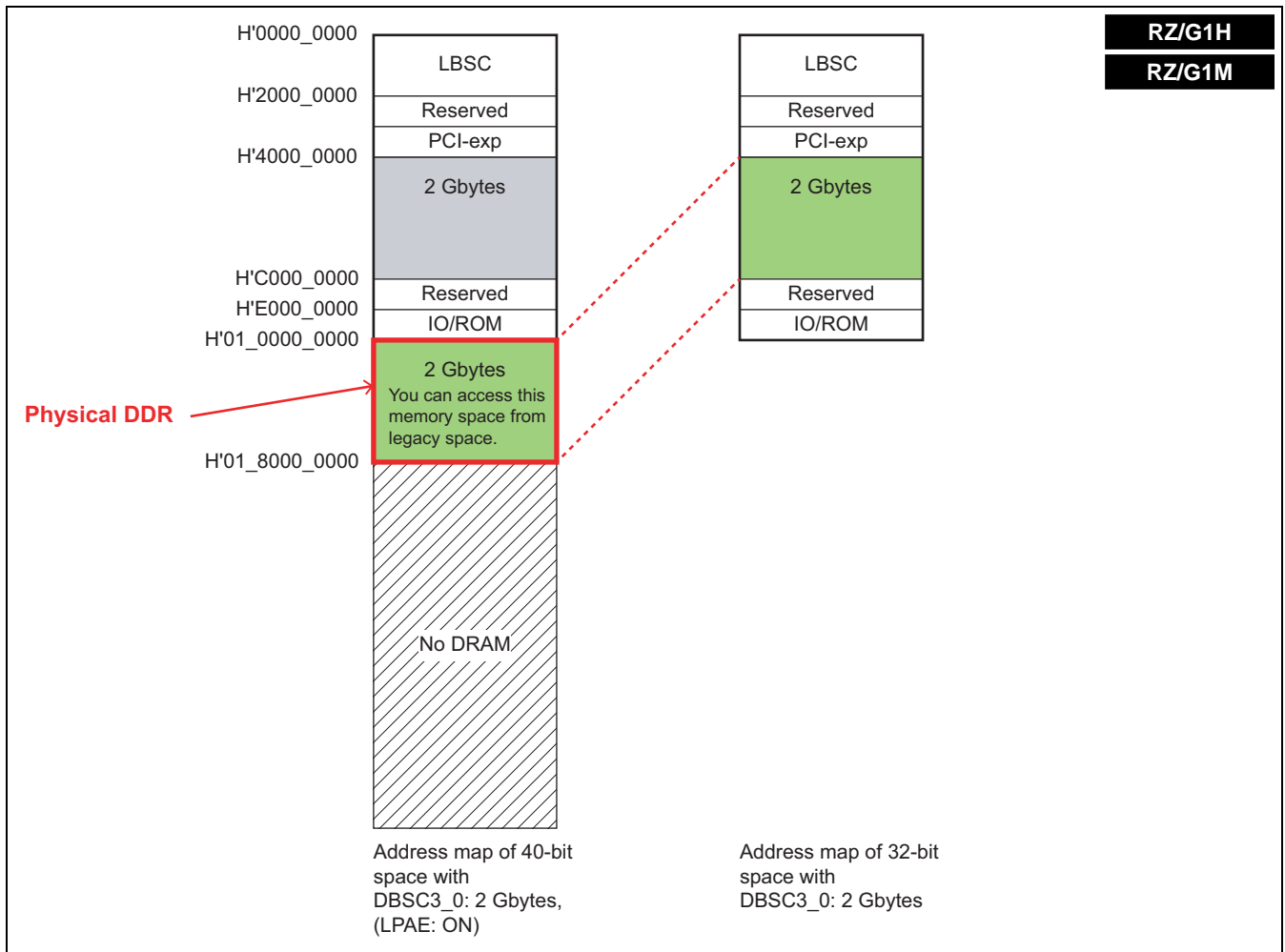


Figure 15.26 RZ/G1H/M Address Map with DBSC3\_0: 2 Gbytes

(4) 64 Bits × 1-ch (DBSC3\_0: 4 Gbytes)

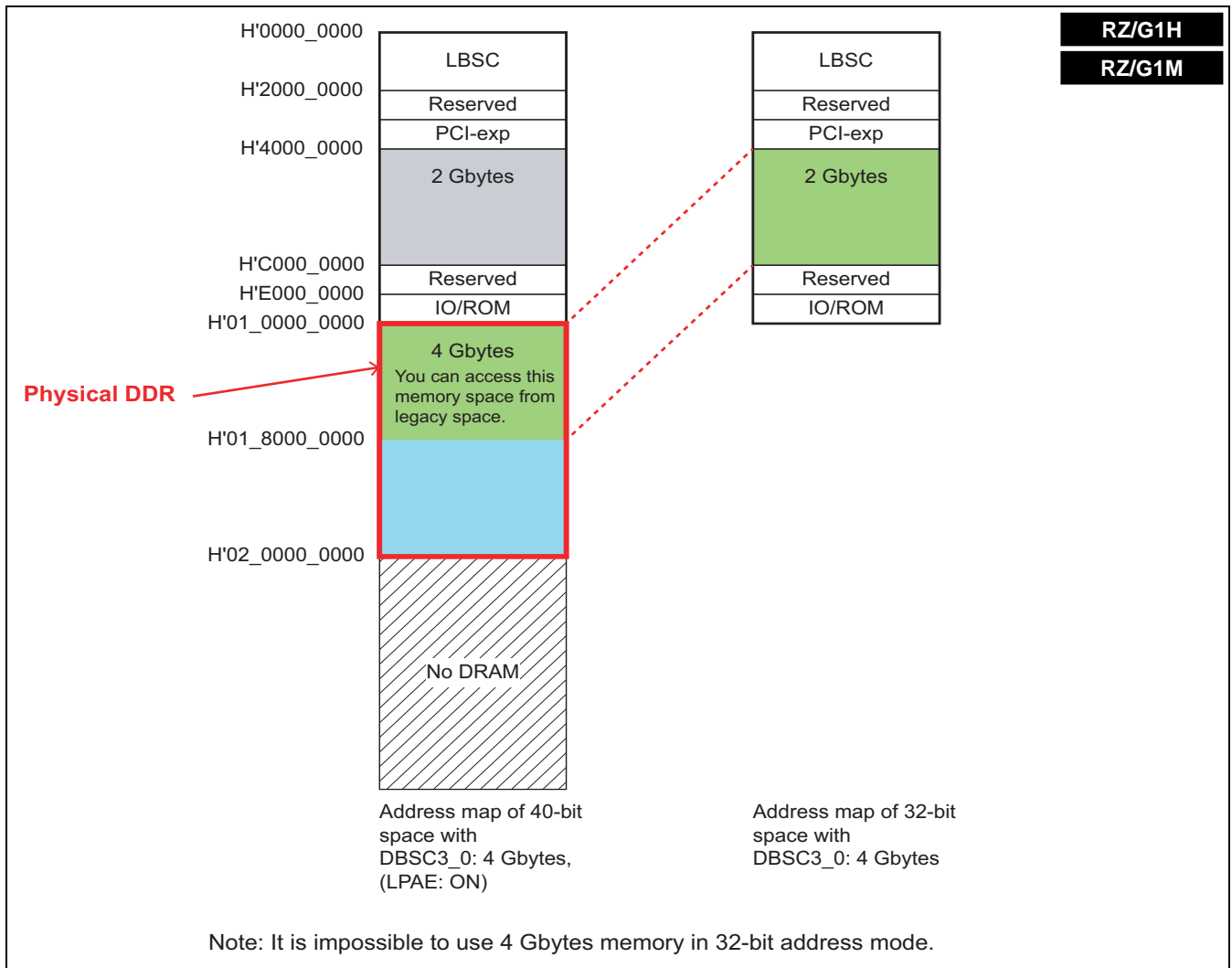


Figure 15.27 RZ/G1H/M Address Map with DBSC3\_0: 4 Gbytes

15.7.3 RZ/G1N/E Address Map

(1) 32 Bits × 1-ch (DBSC3\_0: 4 Gbytes)

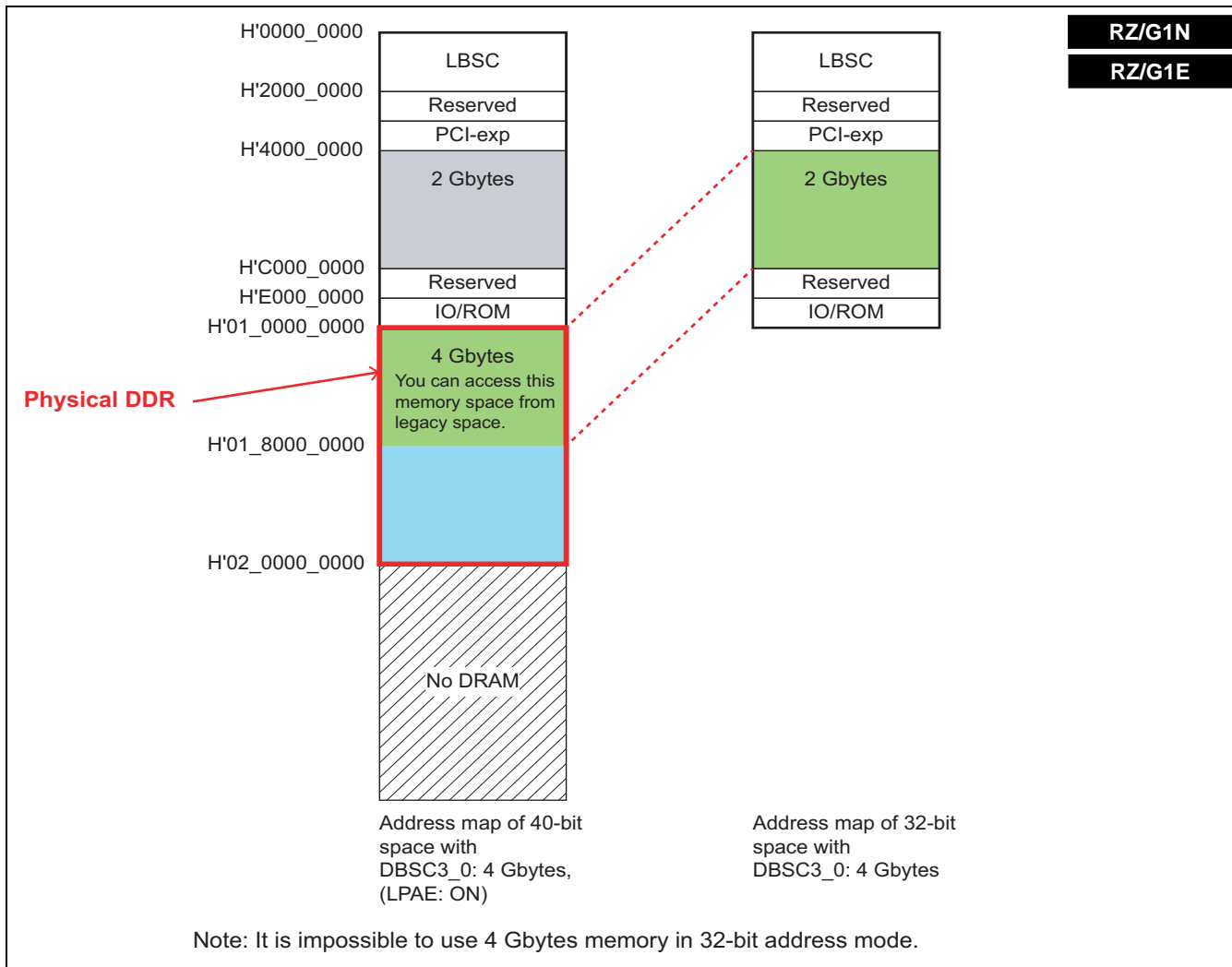


Figure 15.28 RZ/G1N/E Address Map with DBSC3\_0: 4 Gbytes

## 15A. S3 Cache Controller (S3CTRL)

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

### 15A.1 Overview

The S3 cache controller (S3CTRL) includes a local interconnect and L3 system shared cache (s3\$) controller\* placed between AXI-bus interconnects and DBSC memory controller. The S3CTRL improves SDRAM access efficiency with data prefetching and caching. The S3CTRL includes a 2,048-Kbyte RAM which can be used as both cache memory and direct access memory (on-chip RAM)\*.

Note: \* Applicable to the RZ/G1H

#### 15A.1.1 Features

The S3CTRL include the following features.

- Includes the 2,048-Kbyte on-chip RAM shared with cache memory and direct access memory\*<sup>1</sup>
- Cache function\*<sup>1</sup>
  - Physically indexed and physically tagged, 4-bank 8-way set associative 256 line (256 bytes per line)
  - The number of cache way is configurable. The non-used ways can be configured as direct access memory (on-chip RAM)
- Provide flexible SDRAM address mapping. Linear mapping allocates a continuous address space to every single memory controller. Split mapping provides an interleaved address space to two memory controllers at 4 Kbytes granularity.\*<sup>2</sup>
- XY command decoder (media domain only)
- Support 8 entries of system CPU's exclusive access command.
- Interrupt request at the end of cache initialization (all or each banks) is supported\*<sup>1</sup>

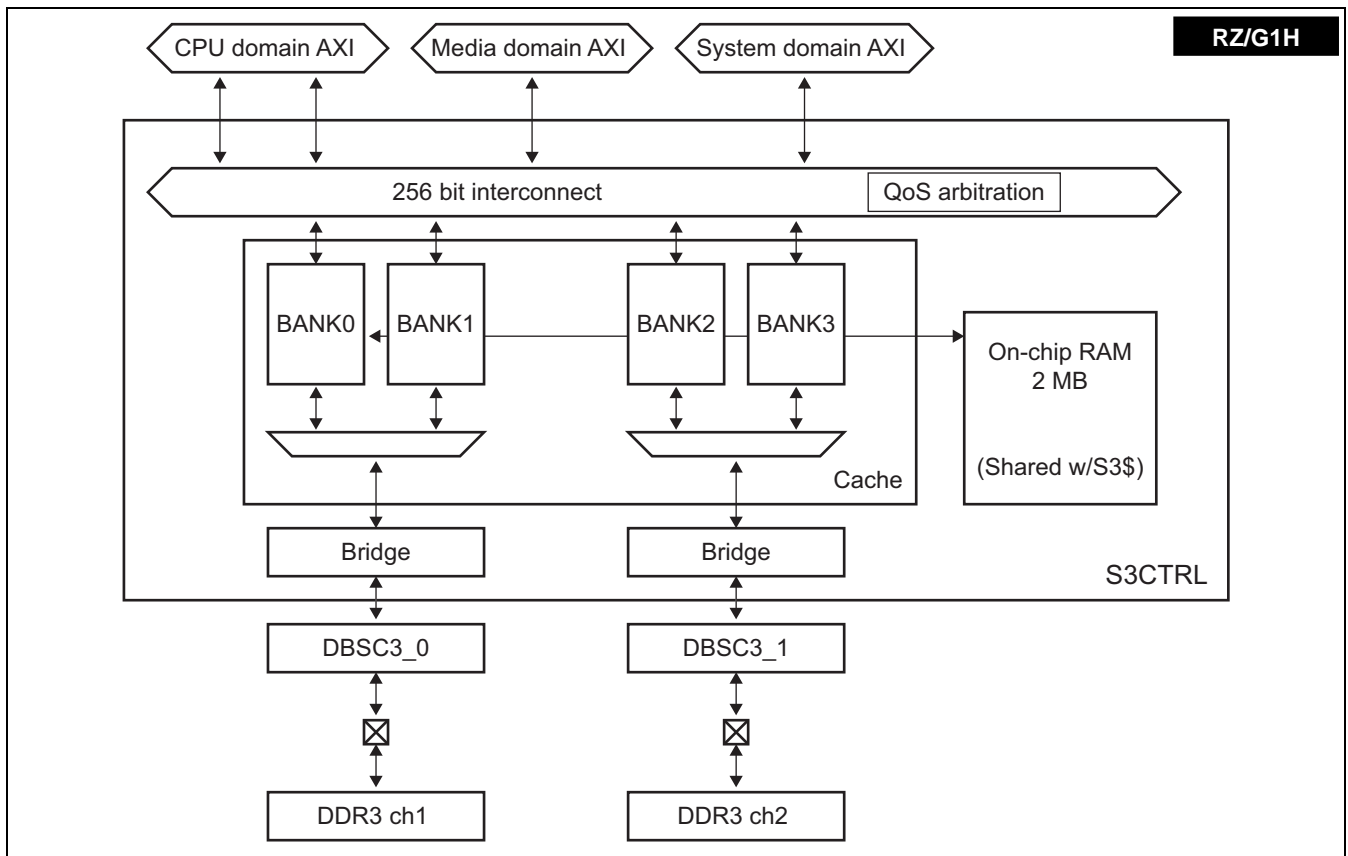
Notes: 1. Applicable to the RZ/G1H

2. Applicable to the RZ/G1H and RZ/G1M



**15A.1.2 Block Diagram**

Figure 15A.1 is a block diagram of the S3CTRL.



**Figure 15A.1a Block Diagram of S3CTRL [RZ/G1H]**

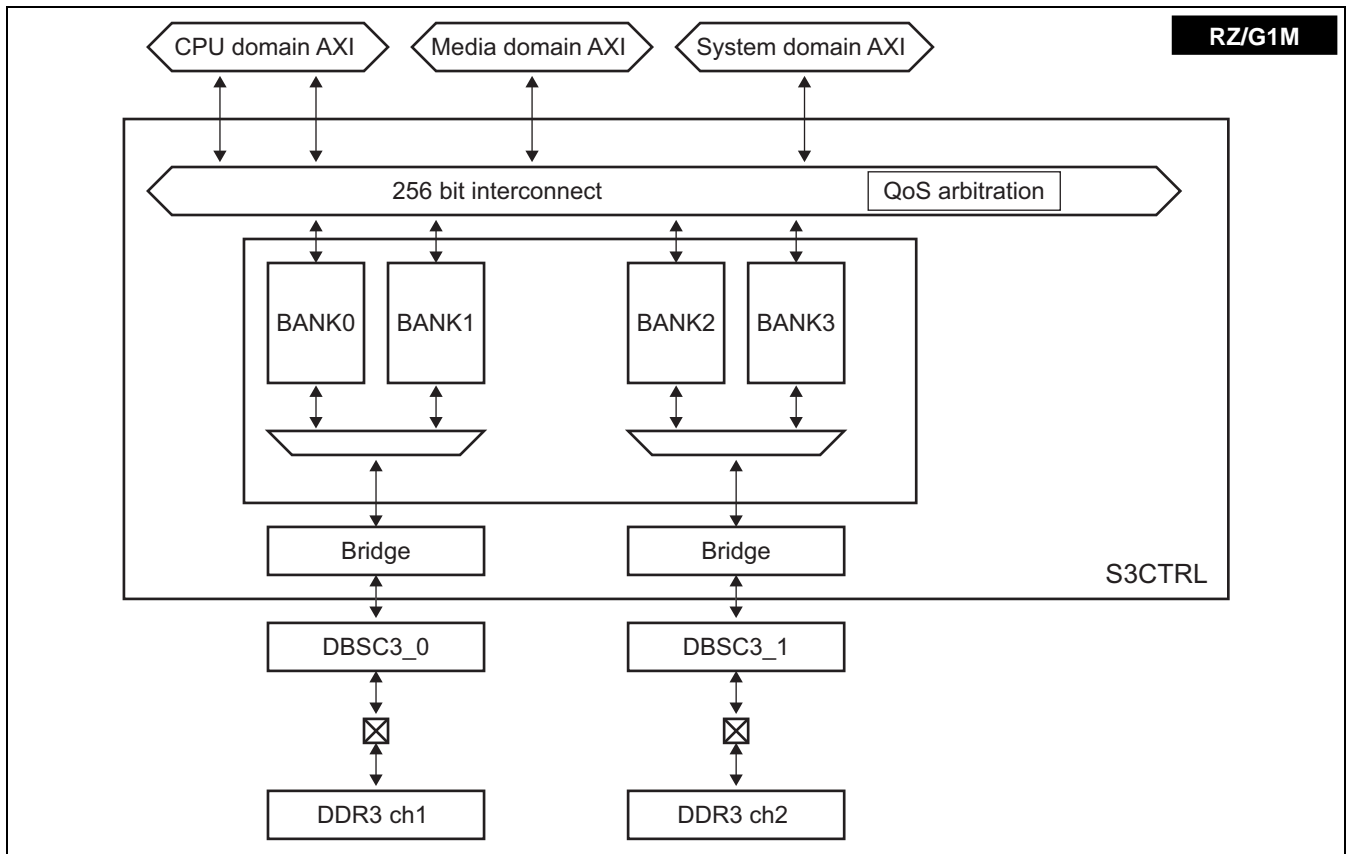


Figure 15A.1b Block Diagram of S3CTRL [RZ/G1M]

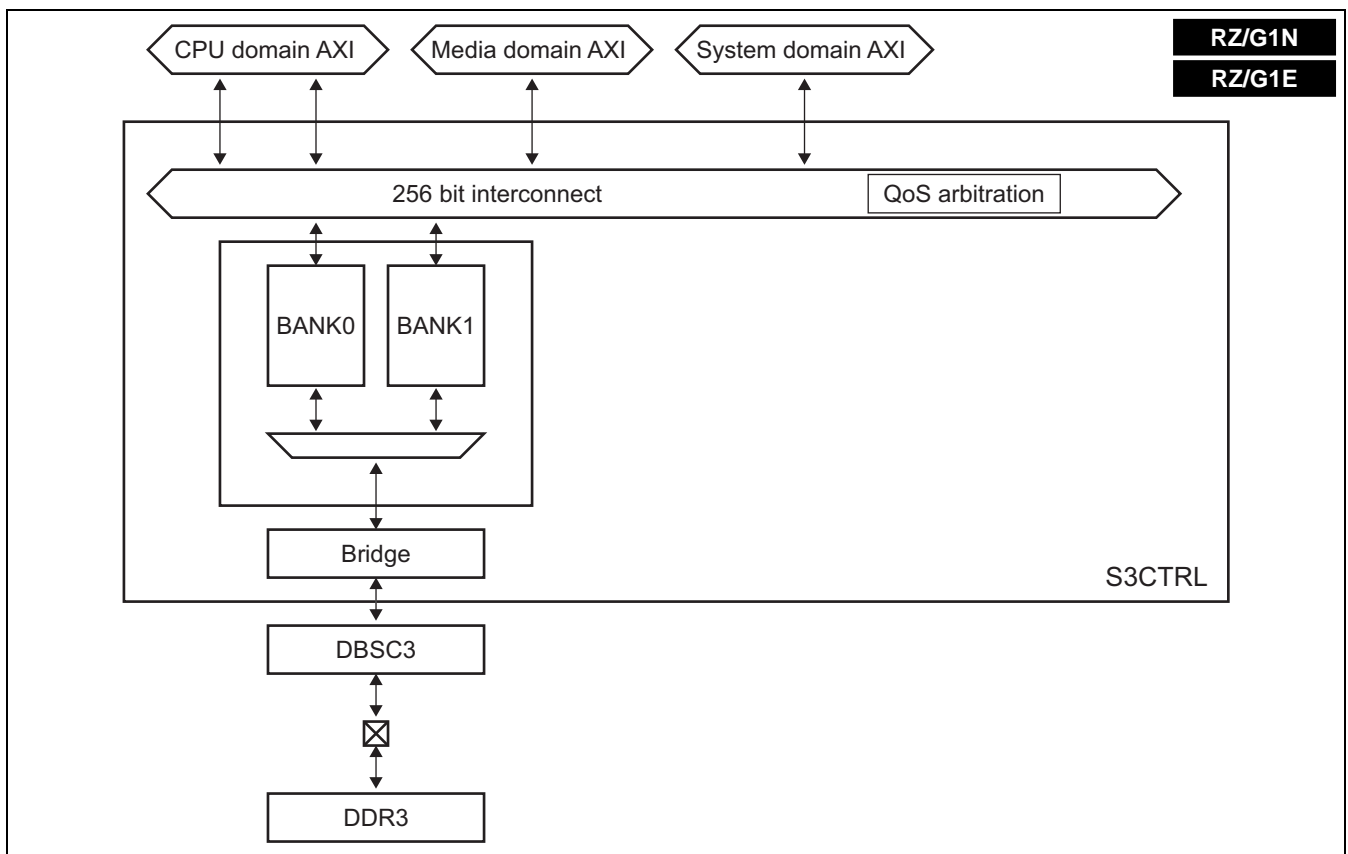


Figure 15A.1c Block Diagram of S3CTRL [RZ/G1N, RZ/G1E]

### 15A.1.3 Input/Output Pins

No external pins are supported.

### 15A.1.4 Register Configuration

Table 15A.1 shows the register configuration. Do not write to any addresses other than listed below. Operations cannot be guaranteed if writing is attempted. Values read from addresses other than those listed below are undefined. Access the register as a longword (32 bits). Operation cannot be guaranteed if the register is not accessed as a longword.

**Table 15A.1 Register Configuration**

Name	Abbreviation	R/W	Address	Initial Value	Access Size	RZ/G Series Products			
						RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Exclusive Address Mask Register	S3CEXCLADDMASK	R/W	H'E678 4000	H'FFFFFFFF	32	√	√	√*1	√*1
Exclusive ID Mask Register	S3CEXCLIDMSK	R/W	H'E678 4004	H'FFFFFFFF	32	√	√	√*1	√*1
S3C Address Split Control Register	S3CADSPLCR	R/W	H'E678 4008	H'00000000	32	√	√	—*2	—*2
Reserved Register	S3CMAAR	R/W	H'E678 400C	H'04080000	32	√*1	√*1	√*1	√*1
S3C Read Outstanding Regulation Register	S3CRORR	R/W	H'E678 4014	H'0F0D0B07	32	√	√	√	√
S3C Write Outstanding Regulation Register	S3CWORR	R/W	H'E678 4018	H'0F0D0B07	32	√	√	√	√
S3C Cache Master Control Register	S3CMCTR	R/W	H'E678 4028	H'00000000	32	√	—	—	—
Cache Configuration Register 0	CCONF0	R/W	H'E678 4030	H'00000000	32	√	—	—	—
Cache Configuration Register 1	CCONF1	R/W	H'E678 4034	H'00000000	32	√	—	—	—
Cache Configuration Register 2	CCONF2	R/W	H'E678 4038	H'00000000	32	√	—	—	—
Cache Configuration Register 3	CCONF3	R/W	H'E678 403C	H'00000000	32	√	—	—	—
Interrupt Control Register	INTCR0	R/W	H'E678 4A00	H'00000000	32	√	—	—	—
Interrupt Clear Register	INTCLR0	R/W	H'E678 4A04	H'00000000	32	√	—	—	—
XY TL Area Control Register A0	XYTLAREAA0	R/W	H'E678 4B00	H'00000000	32	√	√	√	√
XY TL Area Control Register A1	XYTLAREAA1	R/W	H'E678 4B04	H'00000000	32	√	√	√	√
XY TL Area Control Register A2	XYTLAREAA2	R/W	H'E678 4B08	H'00000000	32	√	√	√	√
XY TL Area Control Register A3	XYTLAREAA3	R/W	H'E678 4B0C	H'00000000	32	√	√	√	√
XY TL Area Control Register A4	XYTLAREAA4	R/W	H'E678 4B10	H'00000000	32	√	√	√	√
XY TL Area Control Register A5	XYTLAREAA5	R/W	H'E678 4B14	H'00000000	32	√	√	√	√
XY TL Area Control Register A6	XYTLAREAA6	R/W	H'E678 4B18	H'00000000	32	√	√	√	√

Name	Abbreviation	R/W	Address	Initial Value	Access Size	RZ/G Series Products			
						RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
XY TL Area Control Register A7	XYTLAREAA7	R/W	H'E678 4B1C	H'00000000	32	√	√	√	√
XY TL Area Control Register B0	XYTLAREAB0	R/W	H'E678 4B20	H'00000000	32	√	√	√	√
XY TL Area Control Register B1	XYTLAREAB1	R/W	H'E678 4B24	H'00000000	32	√	√	√	√
XY TL Area Control Register B2	XYTLAREAB2	R/W	H'E678 4B28	H'00000000	32	√	√	√	√
XY TL Area Control Register B3	XYTLAREAB3	R/W	H'E678 4B2C	H'00000000	32	√	√	√	√
XY TL Area Control Register B4	XYTLAREAB4	R/W	H'E678 4B30	H'00000000	32	√	√	√	√
XY TL Area Control Register B5	XYTLAREAB5	R/W	H'E678 4B34	H'00000000	32	√	√	√	√
XY TL Area Control Register B6	XYTLAREAB6	R/W	H'E678 4B38	H'00000000	32	√	√	√	√
XY TL Area Control Register B7	XYTLAREAB7	R/W	H'E678 4B3C	H'00000000	32	√	√	√	√
XY Mode Configuration Register	XYMODECONF	R/W	H'E678 4B40	H'00000000	32	√	√	√	√

Notes: 1. Some restrictions apply.  
2. The operation is not guaranteed when this register is set up.

## 15A.2 Register Description

### Legend for Register Description

Initial value: Register value after a reset. H'xxxx represents a hexadecimal number. Others are represented in binary numbers.

—: Undefined value

R/W: Readable/writable. The written value can be read.

R: Read-only. The write value should always be 0.

R/WC0: Readable/writable. Writing 0 initializes the bit. Writing 1 is ignored.

R/WC1: Readable/writable. Writing 1 initializes the bit. Writing 0 is ignored.

W: Write-only. Reading this bit is prohibited. When the bit is reserved, the write value should always be 0.

—/W: Write-only. The read value is undefined.

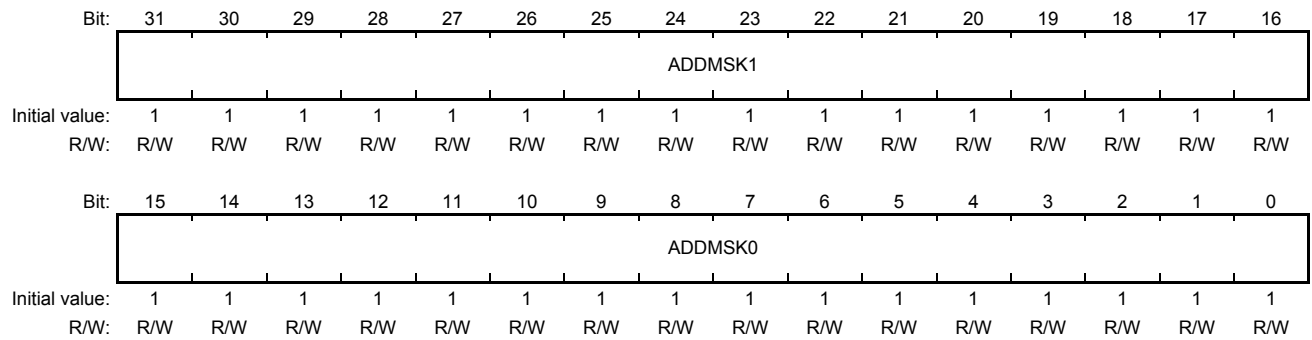
All access to registers is made in longword units.

**15A.2.1 Exclusive Address Mask Register (S3CEXCLADDMSK)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√*	√*

Note: \* Some restrictions apply.

Function: Address bit mask of exclusive access. Lower 16-bit address can be masked.



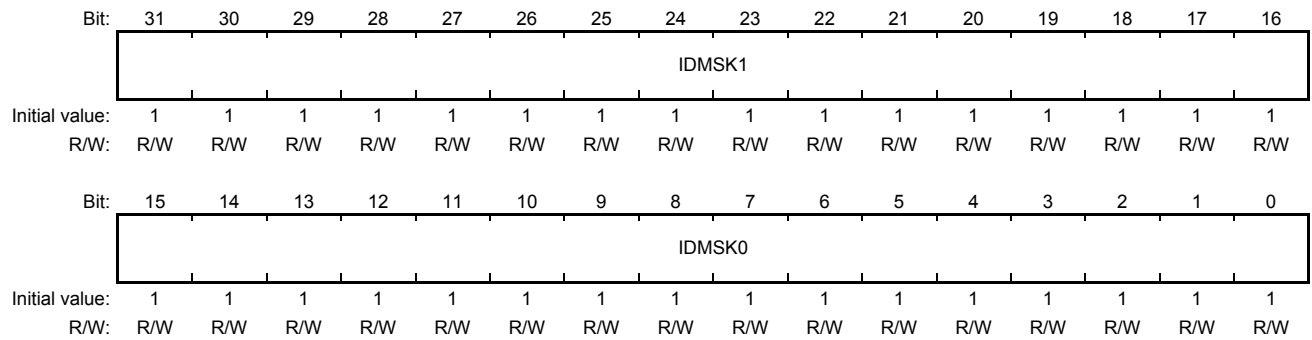
Bit	Bit Name	Initial Value	R/W	Description
31 to 16	ADDMSK1	H'FFFF	R/W	[RZ/G1H, M] Exclusive address mask (Lower 16 bits) enable bit for DBSC channel 1 0: Disable bit 1: Enable bit
				[RZ/G1N, E] Reserved These bits are always read as H'FFFF. The write value should always be H'FFFF.
15 to 0	ADDMSK0	H'FFFF	R/W	Exclusive address mask (Lower 16 bits) enable bit for DBSC channel 0 0: Disable bit 1: Enable bit

**15A.2.2 Exclusive ID Mask Register (S3CEXCLIDMSK)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√*	√*

Note: \* Some restrictions apply.

Function: ID bit mask of exclusive access



Bit	Bit Name	Initial Value	R/W	Description
31 to 16	IDMSK1	H'FFFF	R/W	[RZ/G1H, M] Exclusive ID mask (Lower 16 bits) enable bit for DBSC channel 1 0: Disable bit 1: Enable bit
				[RZ/G1N, E] Reserved These bits are always read as H'FFFF. The write value should always be H'FFFF.
15 to 0	IDMSK0	H'FFFF	R/W	Exclusive ID mask (Lower 16 bits) enable bit for DBSC channel 0 0: Disable bit 1: Enable bit



### 15A.2.3 S3C Address Split Control Register (S3CADSPLCR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	—*	—*

Note: \* The operation is not guaranteed when this register is set up.

Function: This register sets about SDRAM linear/split address mapping.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SWPO E	SWP2SEL			SWP2	—	—	—	SPLITSEL							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	AREA				—	—	—	SWP					
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	SWPOE	0	R/W	Select output address to DBSC. 0: Output address after SWP translation for 2 channels SDRAM mode (32-bit bus mode) 1: Output address before SWP translation for 1 channels SDRAM mode (64-bit bus mode)
30 to 28	SWP2SEL	000	R/W	Specify the address bit replaced with the address bit of SWP. 000: bit 17 001: bit 18 others: Reserved
27	SWP2	0	R/W	0: Disable SWP2SEL translation. 1: Enable SWP2SEL translation.
26 to 24	—	All 0	R/W	Reserved These bits are always read as 0. The write value should always be 0.
23 to 16	SPLITSEL	H'00	R/W	Specify the areas translated through SWP. Each bit of SPLITSEL represents the number of area (0 to 7).
15 to 13	—	All 0	R/W	Reserved These bits are always read as 0. The write value should always be 0.
12 to 8	AREA	H'00	R/W	Indicate the address bit which divides a DBSC address space into 8 areas. H'18 and more must be set. Example: H'1D: 8 Gbytes DRAM H'1C: 4 Gbytes DRAM H'1B: 2 Gbytes DRAM
7 to 5	—	All 0	R/W	Reserved These bits are always read as 0. The write value should always be 0.
4 to 0	SWP	H'00	R/W	Indicate the address bit to interleave two DBSCs. H'C and more must be set.

**15A.2.4 Reserved Register (S3CMAAR)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√*	√*	√*	√*

Note: \* Some restrictions apply.

Function: This register is reserved. The operation is not guaranteed when setting up other than an initial value.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 27	—	All 0	R/W	Reserved These bits are always read as 0. The write value should always be 0.
26	—	1	R/W	Reserved This bit is always read as 1. The write value should always be 1.
25 to 20	—	All 0	R/W	Reserved These bits are always read as 0. The write value should always be 0.
19	—	1	R/W	Reserved This bit is always read as 1. The write value should always be 1.
18 to 0	—	All 0	R/W	Reserved These bits are always read as 0. The write value should always be 0.

### 15A.2.5 S3C Read Outstanding Regulation Register (S3CRORR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: S3CTRL can control the number of read transaction at every QoS level to prevent DBSC's queue with low priority transactions. Transaction number is set by QOSTHn + 1. When QOSTHn = H'1F, its transaction number is not limited.

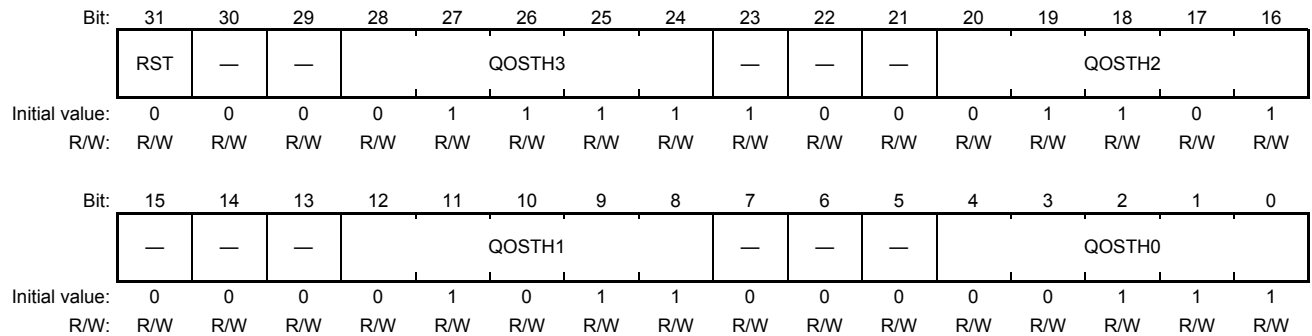
Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	RST	—	—	QOSTH3					—	—	—	QOSTH2				
Initial value:	0	0	0	0	1	1	1	1	1	0	0	0	1	1	0	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	QOSTH1				—	—	—	QOSTH0					
Initial value:	0	0	0	0	1	0	1	1	0	0	0	0	0	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	RST	0	R/W	Reset the read transaction counter.
30, 29	—	All 0	R/W	Reserved These bits are always read as 0. The write value should always be 0.
28 to 24	QOSTH3	H'0F	R/W	The threshold queue length which the read transactions of QOS-Level3 can fill.
23 to 21	—	All 0	R/W	Reserved These bits are always read as 0. The write value should always be 0.
20 to 16	QOSTH2	H'0D	R/W	The threshold queue length which the read transactions of QOS-Level2 can fill.
15 to 13	—	All 0	R/W	Reserved These bits are always read as 0. The write value should always be 0.
12 to 8	QOSTH1	H'0B	R/W	The threshold queue length which the read transactions of QOS-Level1 can fill.
7 to 5	—	All 0	R/W	Reserved These bits are always read as 0. The write value should always be 0.
4 to 0	QOSTH0	H'07	R/W	The threshold queue length which the read transactions of QOS-Level0 can fill.

**15A.2.6 S3C Write Outstanding Regulation Register (S3CWORR)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: S3CTRL can control the number of write transaction at every QoS level to prevent DBSC’s queue with low priority transactions. Transaction number is set by QOSTHn + 1. When QOSTHn = H'1F, its transaction number is not limited.



Bit	Bit Name	Initial Value	R/W	Description
31	RST	0	R/W	Reset the write transaction counter.
30, 29	—	All 0	R/W	Reserved These bits are always read as 0. The write value should always be 0.
28 to 24	QOSTH3	H'0F	R/W	The threshold queue length which the write transactions of QOS-Level3 can fill.
23 to 21	—	All 0	R/W	Reserved These bits are always read as 0. The write value should always be 0.
20 to 16	QOSTH2	H'0D	R/W	The threshold queue length which the write transactions of QOS-Level2 can fill.
15 to 13	—	All 0	R/W	Reserved These bits are always read as 0. The write value should always be 0.
12 to 8	QOSTH1	H'0B	R/W	The threshold queue length which the write transactions of QOS-Level1 can fill.
7 to 5	—	All 0	R/W	Reserved These bits are always read as 0. The write value should always be 0.
4 to 0	QOSTH0	H'07	R/W	The threshold queue length which the write transactions of QOS-Level0 can fill.

**15A.2.7 S3C Cache Master Control Register (S3CMCTR)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	—	—	—

Function: This register sets about cache functions.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ME
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

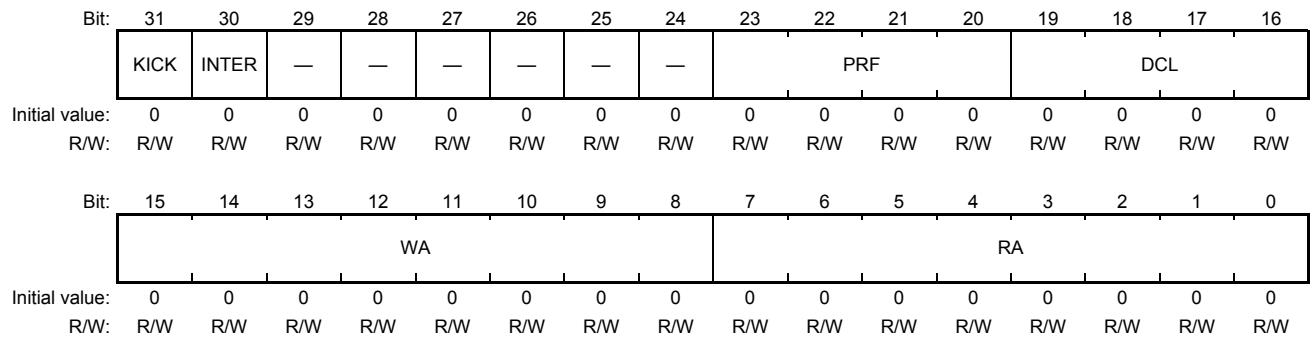
Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R/W	Reserved These bits are always read as 0. The write value should always be 0.
0	ME	0	R/W	Cache Function Enable 0: Disable 1: Enable

### 15A.2.8 Cache Configuration Register n (CCONFn)

Note: n = 0 to 3

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	—	—	—

Function: This register sets about cache functions for each bank n (n = 0 to 3).



Bit	Bit Name	Initial Value	R/W	Description
31	KICK	0	R/W	KICK bit is set to 1 in order to update cache configurations.
30	INTER	0	R/W	In Normal mode, cache bank n is associated with transaction port. In Bank interleave mode, cache line of both banks are interleaved so that all cache line can be used from a single port. 0: Normal mode 1: Bank Interleave mode
29 to 24	—	All 0	R/W	Reserved These bits are always read as 0. The write value should always be 0.
23 to 20	PRF	H'0	R/W	Pre-fetch mode H'0: 64 Bytes H'1: 64 Bytes × 2 H'2: 128 Bytes × 1 H'3: 256 Bytes others: Never Set
19 to 16	DCL	H'0	R/W	The number of remained dirty way for auto cleanup is executed (H'0: None, H'1: if all way is dirty, oldest way is cleaned ... H'8: always cleanup and no dirty way remained.)
15 to 8	WA	H'00	R/W	Write allocate on-chip RAM area WA[7]: Way7 WA[6]: Way6 WA[5]: Way5 WA[4]: Way4 WA[3]: Way3 WA[2]: Way2 WA[1]: Way1 WA[0]: Way0

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Bit	Bit Name	Initial Value	R/W	Description
7 to 0	RA	H'00	R/W	Read allocate on-chip RAM area RA[7]: Way7 RA[6]: Way6 RA[5]: Way5 RA[4]: Way4 RA[3]: Way3 RA[2]: Way2 RA[1]: Way1 RA[0]: Way0

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**15A.2.9 Interrupt Control Register (INTCR0)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	—	—	—

Function: This register sets interrupt request control.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	IE_KICK R_END	IE_KIC KR3	IE_KIC KR2	IE_KIC KR1	IE_KIC KR0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 5	—	All 0	R/W	Reserved These bits are always read as 0. The write value should always be 0.
4	IE_KICKR_END	0	R/W	Interrupt enable when initialization of all banks are end. 0: Disable 1: Enable
3	IE_KICKR3	0	R/W	Interrupt enable when initialization of all bank3 is end. 0: Disable 1: Enable
2	IE_KICKR2	0	R/W	Interrupt enable when initialization of all bank2 is end. 0: Disable 1: Enable
1	IE_KICKR1	0	R/W	Interrupt enable when initialization of all bank1 is end. 0: Disable 1: Enable
0	IE_KICKR0	0	R/W	Interrupt enable when initialization of all bank0 is end. 0: Disable 1: Enable



### 15A.2.10 Interrupt Clear Register (INTCLR0)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	—	—	—

Function: This register shows interrupt request status and sets status clear.

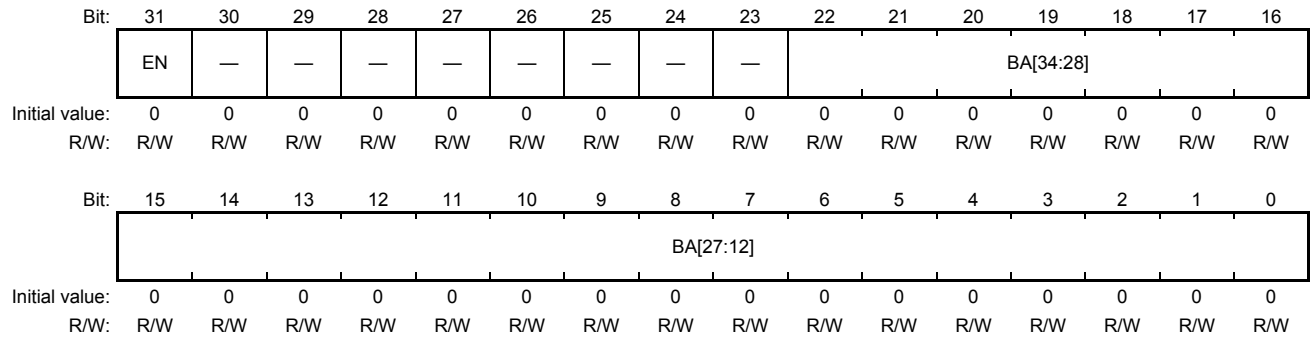
Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	IE_KICK R_END	IE_KIC KR3	IE_KIC KR2	IE_KIC KR1	IE_KIC KR0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1

Bit	Bit Name	Initial Value	R/W	Description
31 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	IE_KICKR_END	0	R/WC1	Interrupt status when initialization of all banks is end. To clear the event writes 1. 0: this event is not occurred 1: this event is occurred
3	IE_KICKR3	0	R/WC1	Interrupt status when initialization of bank3 is end. To clear the event writes 1. 0: this event is not occurred 1: this event is occurred
2	IE_KICKR2	0	R/WC1	Interrupt status when initialization of bank2 is end. To clear the event writes 1. 0: this event is not occurred 1: this event is occurred
1	IE_KICKR1	0	R/WC1	Interrupt status when initialization of bank1 is end. To clear the event writes 1. 0: this event is not occurred 1: this event is occurred
0	IE_KICKR0	0	R/WC1	Interrupt status when initialization of bank0 is end. To clear the event writes 1. 0: this event is not occurred 1: this event is occurred

**15A.2.11 XY TL Area Control Register A0 to A7 (XYTLAREAAn, (n = 0 to 7))**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: This register sets XY TL area. To change the value, set EN bit to 0.



Bit	Bit Name	Initial Value	R/W	Description
31	EN	0	R/W	Enable bit for this Area. 0: Disable 1: Enable
30 to 23	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
22 to 0	BA[34:12]	H'00 0000	R/W	Base address [34:12] The start address of Tile area is specified. Set values by STRIDE × 32 align.

### 15A.2.12 XY TL Area Control Register B0 to B7 (XYTLAREABn, (n = 0 to 7))

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: This register sets XY TL area. To change the value, set XYTLAREAA<sub>n</sub>.EN bit to 0.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	TT	—	—	—	—	SIZE			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R	R	R	R	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	STRIDE[11:4]								—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 25	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
24	TT	0	R/W	Tile Type 0: 128 pix × 32 line 1: 256 pix × 32 line
23 to 20	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
19 to 16	SIZE	0000	R/W	Size of area 0000: 256 Kbytes 0001: 512 Kbytes 0010: 1 Mbyte 0011: 2 Mbytes 0100: 4 Mbytes 0101: 8 Mbytes 0110: 16 Mbytes 0111: 32 Mbytes 1000: 64 Mbytes 1001: 128 Mbytes 1010: 256 Mbytes others: Never Set
15 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11 to 4	STRIDE[11:4]	H'00	R/W	Breadth of Tile Area. The value which can be set has restriction by TT (Tile Type) bit. 128 × 2 <sup>n</sup> (n = 0 to 5) (TT bit is 0) 256 × 2 <sup>n</sup> (n = 0 to 4) (TT bit is 1)
3 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

### 15A.2.13 XY Mode Configuration Register (XYMODECONF)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: This register sets XY mode configuration.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	XRCM	XWCM	YRCM	YWCM	—	—	—	LM	—	—	—	TT
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R	R	R	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11	XRCM	0	R/W	X Read Convert Mode. Convert $16 \times 1$ to $16 \times 2$ . 0: Disable 1: Enable
10	XWCM	0	R/W	X Write Convert Mode. Convert $16 \times 1$ to $16 \times 2$ . 0: Disable 1: Enable
9	YRCM	0	R/W	Y Read Convert Mode. Convert $16 \times 1$ to $16 \times 2$ . 0: Disable 1: Enable
8	YWCM	0	R/W	Y Write Convert Mode. Convert $16 \times 1$ to $16 \times 2$ . 0: Disable 1: Enable
7 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	LM	0	R/W	Line Mode 0: $16 \times 1$ mode 1: $16 \times 2$ mode
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	TT	0	R/W	Tile Type 0: $128 \text{ pix} \times 32 \text{ line}$ 1: $256 \text{ pix} \times 32 \text{ line}$

<b>RZ/G1H</b>	<b>RZ/G1N</b>
<b>RZ/G1M</b>	<b>RZ/G1E</b>

### 15A.3 Operation

#### 15A.3.1 SDRAM Address Space

The S3CTRL supports two\* independent SDRAM memory controllers (DBSC) and 4 Gbytes address space on each controller. The SDRAM address mapping is managed on 40-bit physical address. Legacy address space is mapped to H'01\_00000000 to H'01\_7FFFFFFF.

Note: \* Applicable to the RZ/G1H and RZ/G1M

Figure 15A.2 is shown SDRAM address map related to S3CTRL.

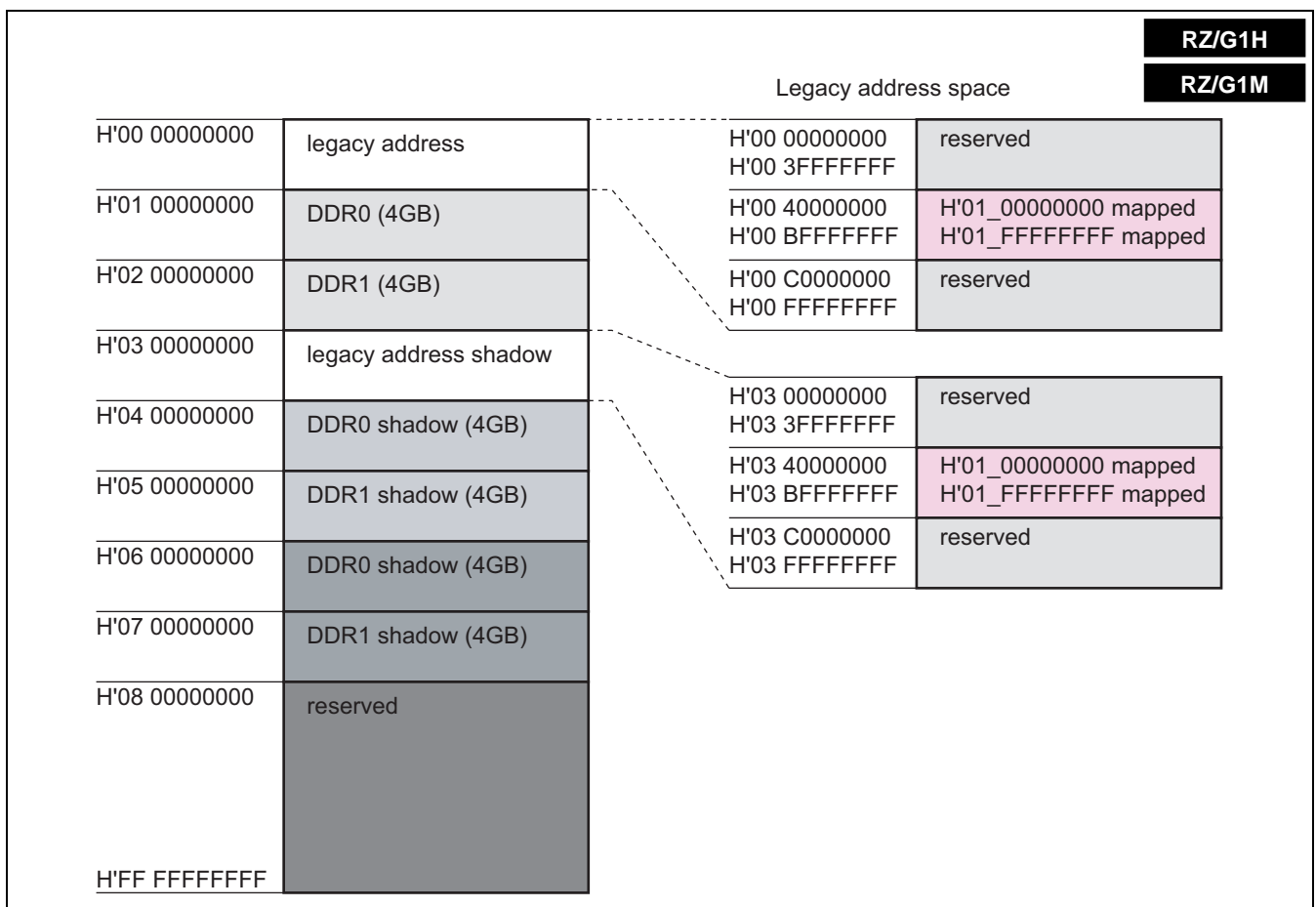
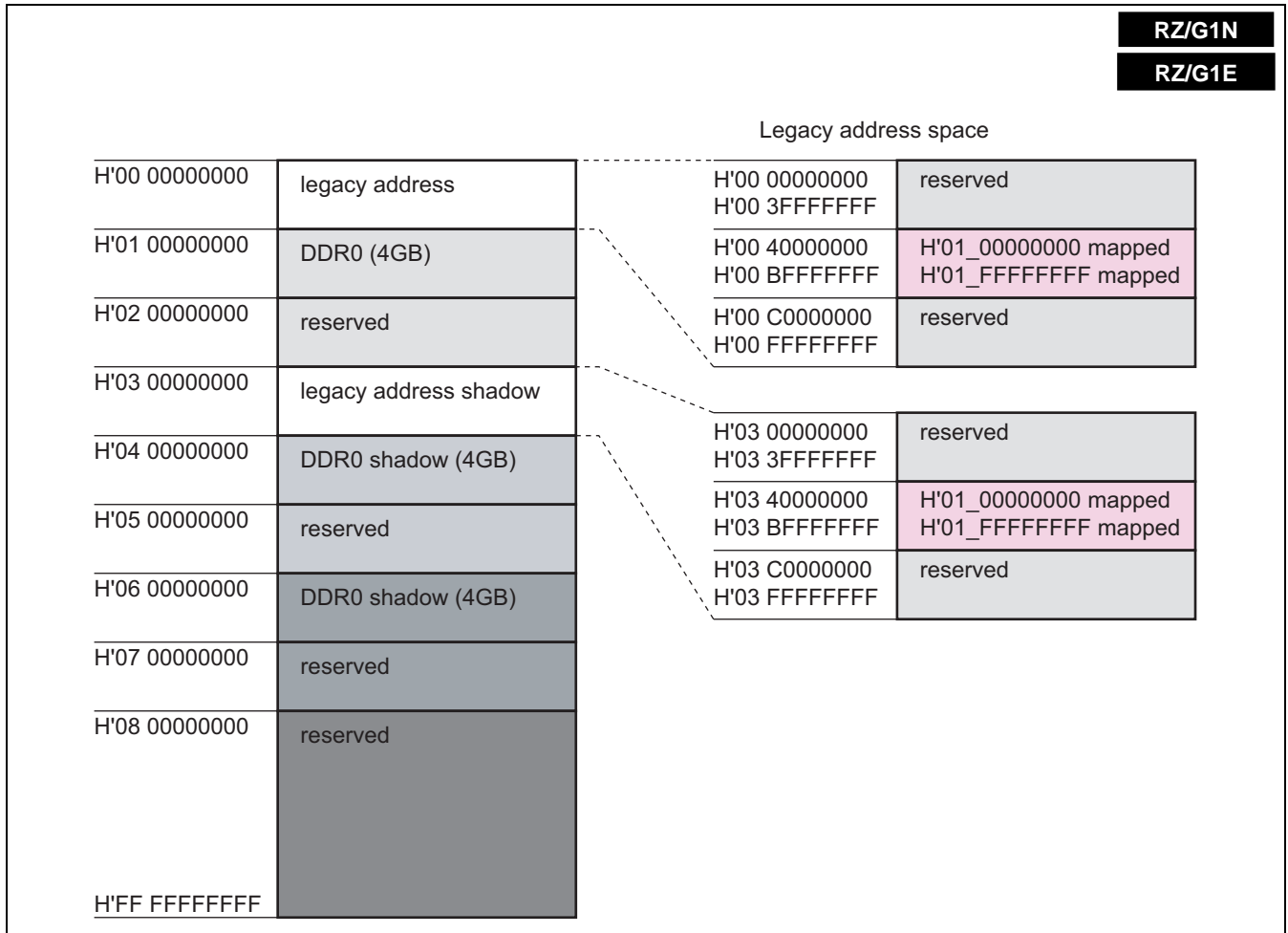


Figure 15A.2a SDRAM Address Map (Concerned with S3CTRL) [RZ/G1H and RZ/G1M]



**Figure 15A.2b SDRAM Address Map (Concerned with S3CTRL)**  
**[RZ/G1N, RZ/G1E]**

### 15A.3.2 SDRAM Split/Linear Address Mapping for RZ/G1H and RZ/G1M

The S3CTRL provides the mixed address space of interleaved address mapping (split mapping) and no-interleaved address mapping (linear mapping) on two memory controllers through S3CADSP\_LCR register. The split mapping mode enhances SDRAM access efficiency and bandwidth via parallel access to two memory controllers. In this mode, the even block is allocated to DBSC0 and the odd block is to DBSC1 at the specified granularity that set by S3CADSP\_LCR.SWP bit. The linear mapping mode allocates a continuous address space to each memory controller. It can be divided into 8 areas through S3CADSP\_LCR.AREA. And also, linear or split mapping can be chosen in each area through S3CADSP\_LCR.SPLITSEL.

Figure 15A.3 is shown split/linear address mapping, and Figure 15A.4 is shown example of split/linear address mapping with 32 bit × 2 ch DRAM mode (ch1: 1 Gbyte/ch2: 1 Gbyte). Figure 15A.5 is shown example of split address mapping with S3CADSP\_LCR.SPLITSEL = H'CF setting.

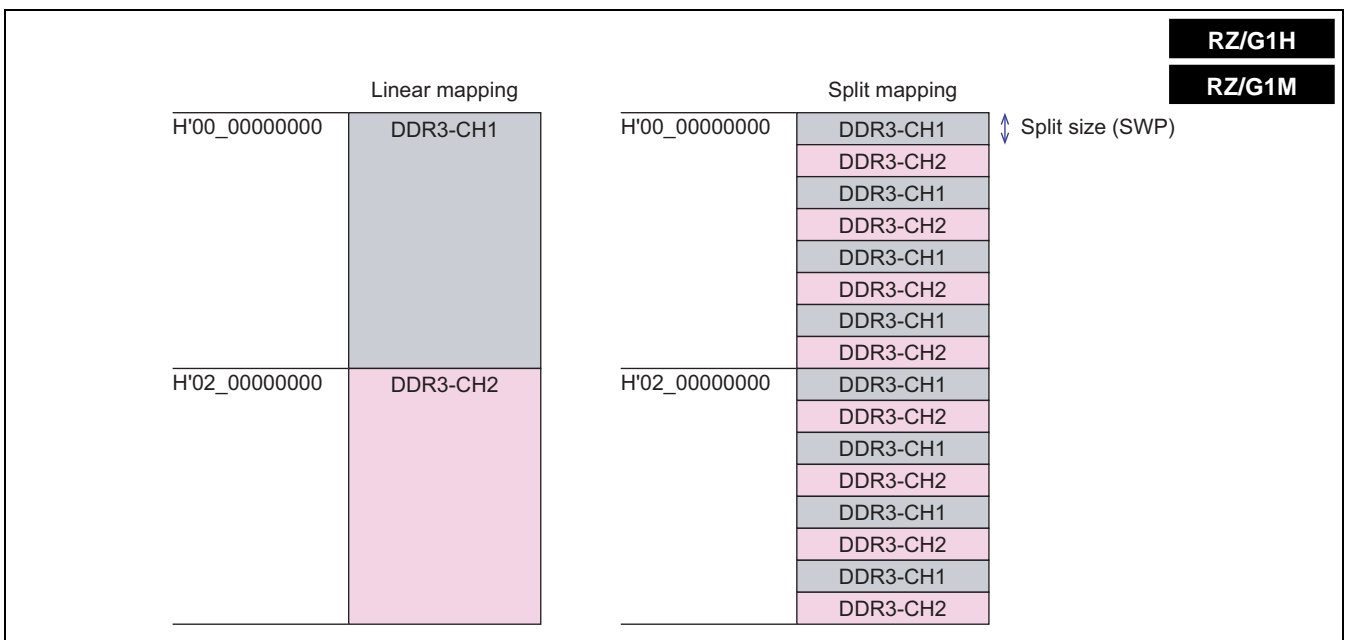
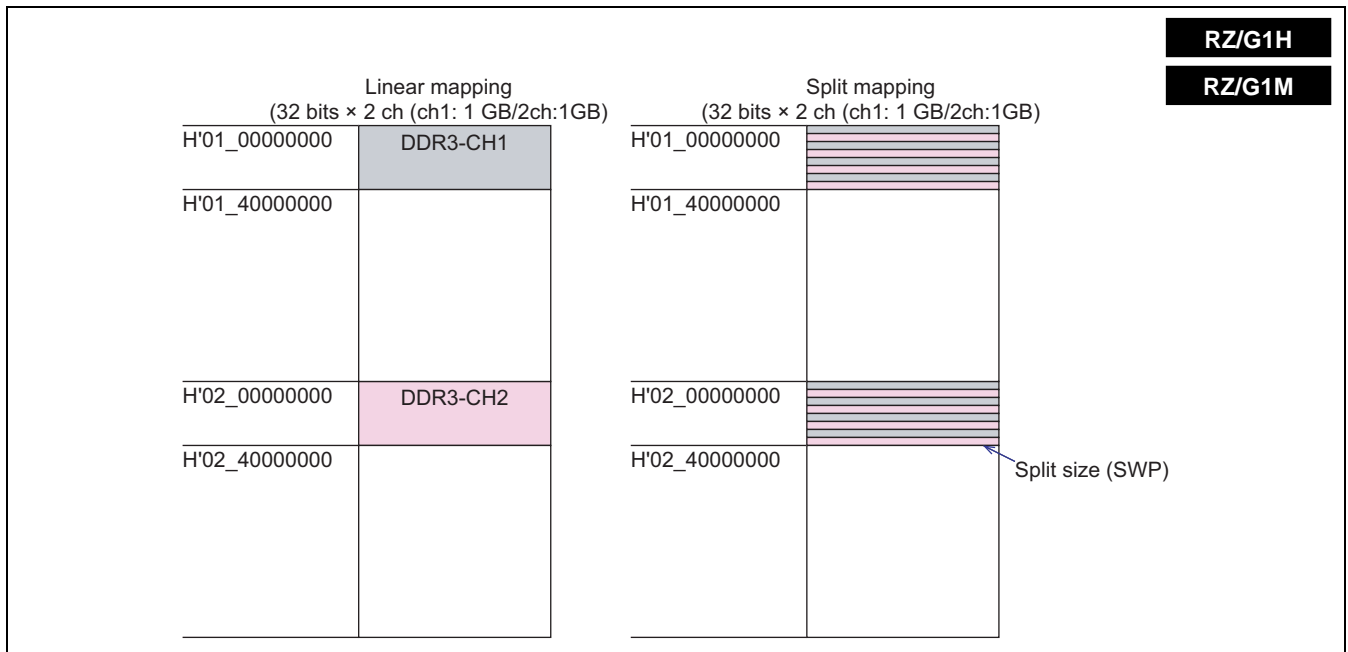
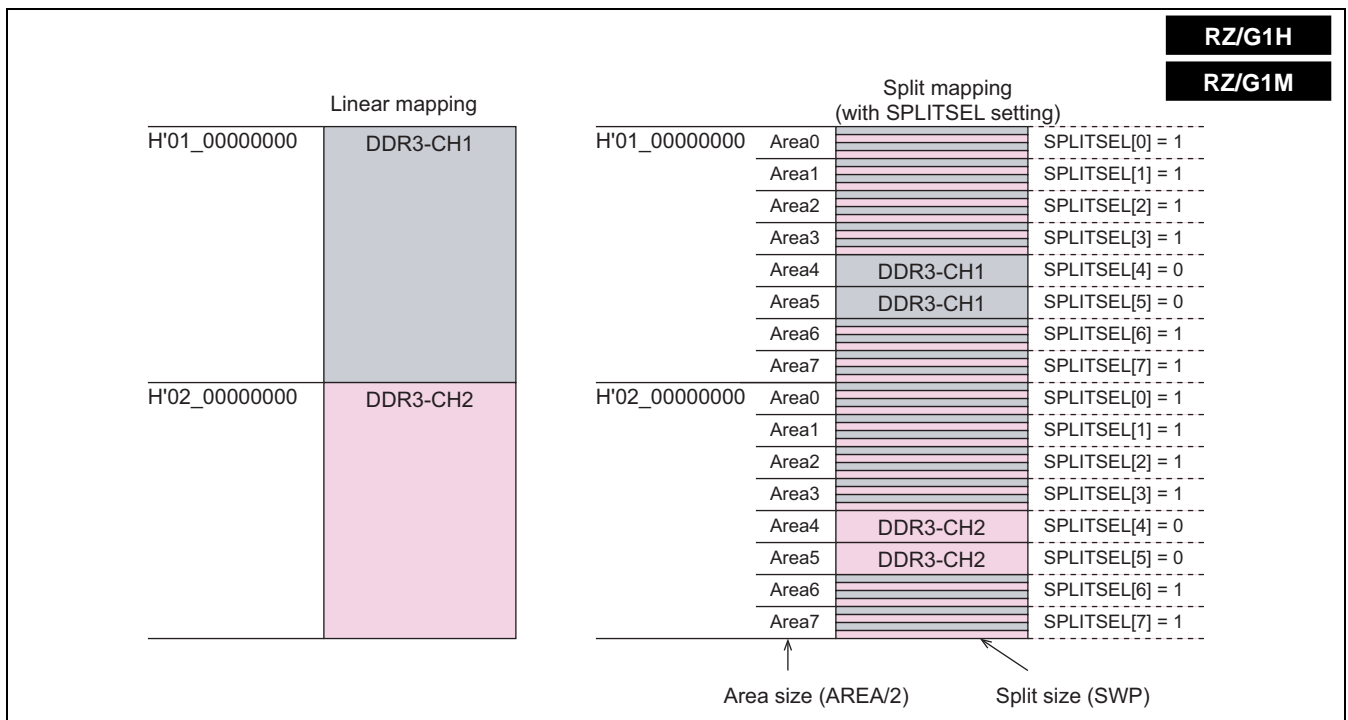


Figure 15A.3 Split/Linear Address Mapping [RZ/G1H and RZ/G1M]



**Figure 15A.4 Example of Split/Linear Address Mapping with 32bit × 2ch DRAM Mode (ch1: 1 Gbyte/ch2: 1 Gbyte) [RZ/G1H and RZ/G1M]**



**Figure 15A.5 Example of Split Address Mapping with S3CADSPLCR.SPLITSEL = H'CF Setting [RZ/G1H and RZ/G1M]**



### 15A.3.3 On-Chip RAM Address Space for RZ/G1H

The on-chip RAM is 2,048-Kbyte RAM shared between S3CTRL, Audio domain and S3\$. Unallocated ways in the S3CTRL can be used as direct access memory.

Figure 15A.6 shows on-chip RAM address space.

S3CTRL	Audio domain	S3\$		<b>RZ/G1H</b>
H'E8080000	H'ED000000	Way 0	256 KB	
H'E80BFFFF	H'ED03FFFF	(Bank0, 1, 2, 3)		
H'E80C0000	H'ED040000	Way 1		
H'E8100000	H'ED080000	Way 2		
H'E8140000	H'ED0C0000	Way 3		
H'E8180000	H'ED100000	Way 4		
H'E81C0000	H'ED140000	Way 5		
H'E8200000	H'ED180000	Way 6		
H'E8240000	H'ED1C0000	Way 7		
H'E827FFFF	H'ED1FFFFF			

**Figure 15A.6 On-Chip RAM Address Space [RZ/G1H]**

### 15A.3.4 XY Command Address Area

S3CTRL supports XY operation from Media domain. The address area accessed by XY operation is defined as Tile-Linear translated area. This area can be defined up to 8 areas. This Tile-Linear translated area also can be accessed by normal (linear) transaction from Media domain.

### 15A.3.5 Cache Operation for RZ/G1H

S3CTRL supports cache function by using on-chip RAM as cache memory. This cache function can be validated in units of 4-bank and 8-way. The validation or invalidation of cache function is set by register. S3CTRL supports interrupt request at the end of each or all cache validation.

### 15A.3.6 QoS Arbitration

Every AXI domain has their own QoS level generator which can change a priority value of transactions dynamically based on its mode. The value is used when choosing the highest priority transaction at arbitration points. Read/Write transaction queues before a memory controller can limit the maximum number of transaction that can be enqueued at every QoS level through S3CRORR/S3CWORR register. That allows low QoS transactions not to fill the queues and reserves space for higher QoS transactions.

### 15A.3.7 About Exclusive Instruction Monitor

The S3CTRL provides 8 exclusive access monitors for each memory controller. In the AXI specification, the AXI IDs and the addresses of the exclusive read and the exclusive write must be identical. However, the S3CTRL can specify the valid range of the IDs and the address through S3CEXCLADMSK and S3CEXCLIDMSK registers.

## 16. Direct Memory Access Controller for System (SYS-DMAC)

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

This LSI includes a direct memory access controller for system (SYS-DMAC). The SYS-DMAC can be used in place of the CPU to handle high-speed data transfer to and from an external memory, the on-chip memory, memory-mapped external devices, or on-chip peripheral modules.

### 16.1 Features

- Up to 30 channels are available (in the RZ/G1H, M, N, and E).
- 4-Gbyte physical address space
- Transfer data length: Byte, word (2 bytes), longword (4 bytes), 8 bytes, 16 bytes, 32 bytes, and 64 bytes
- Maximum number of transfer times: 16,777,216
- Address mode: Dual address mode
- Transfer requests:
 

Requests from on-chip peripheral modules or auto requests can be selected. The following modules can issue on-chip peripheral module requests.

TPU0, MMCIF0/1, IIC0/1/2/3, MSIOF0/1/2/3, HSCIF0/1/2, SCIF0/1/2/3/4/5, SCIFA0/1/2/3/4/5, SCIFB0/1/2, SDHI0/1/2/3, QSPI

Note: The availability of these modules and channels depends on the product. Refer to Table 16.5 for available modules in each product.
- Selectable bus modes:
 

Normal speed mode or slow mode can be selected for each channel.
- Either fixed priority or round-robin arbitration can be selected for use in arbitration among the transfer channels.
- Interrupt request:
 

The SYS-DMAC can be set up to generate an interrupt request for the CPU upon completion of transfer under the control of one stage of the descriptor memory, at the end of the data transfer, in response to an MMU error, and in response to an address error.
- Descriptor memory function:
 

Up to 128 sets of the settings for the source address register, destination address register, and transfer count register are available (if use of the descriptor memory is only enabled for one channel) for use in setting up consecutive DMA transfers (the memory can hold register values for up to 256 stages of transfer when the external memory is selected). An infinite repeat mode is also available.

Figure 16.1 shows the block diagram of the SYS-DMAC.

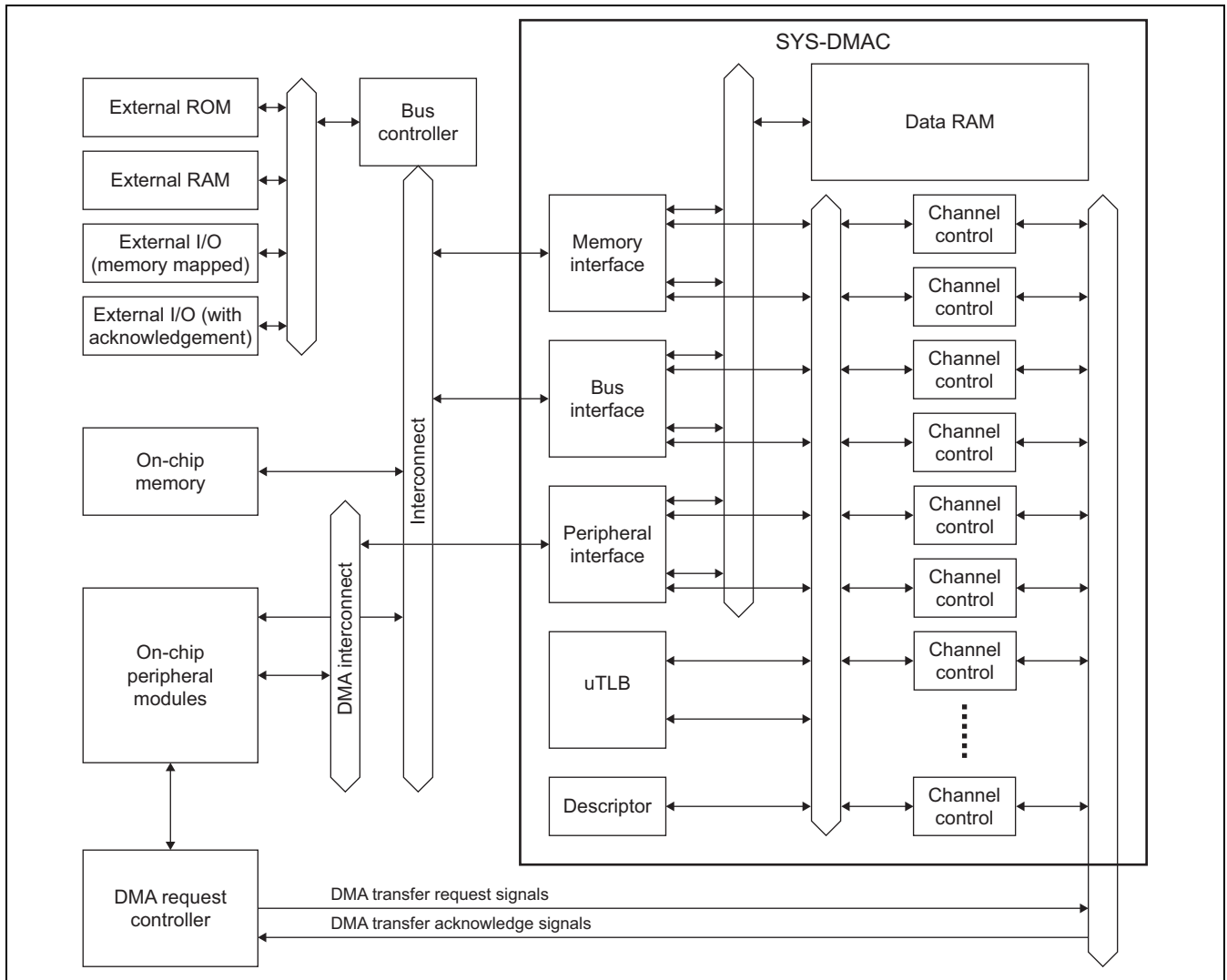


Figure 16.1 Block Diagram of the SYS-DMAC

## 16.2 Input/Output Pins

There are no external pins relevant to the SYS-DMAC.

## 16.3 Register Descriptions

Table 16.1 lists the registers of the SYS-DMAC. Table 16.2 shows the register states of the SYS-DMAC in each operating mode.

Each product of the RZ/G series has the same configuration of registers for the SYS-DMAC.

**Table 16.1 Register Configuration of the SYS-DMAC**

Name	Abbreviation	R/W	Address	Access Size	RZ/G Series Products			
					RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
DMA interrupt status register (for lower-numbered channels)	DMAISTA_L	R	H'E670 0020	32	√	√	√	√
DMA secure control register (for lower-numbered channels)	DMASEC_L	R/W	H'E670 0030	32	√	√	√	√
DMA operation register (for lower-numbered channels)	DMAOR_L	R/W	H'E670 0060	16	√	√	√	√
DMA channel clear register (for lower-numbered channels)	DMACHCLR_L	W	H'E670 0080	32	√	√	√	√
DPRAM secure control register (for lower-numbered channels)	DMADPSEC_L	R/W	H'E670 00A0	32	√	√	√	√
DMA source address register_0	DMASAR_0	R/W	H'E670 8000 H'E670 8020*	32	√	√	√	√
DMA destination address register_0	DMADAR_0	R/W	H'E670 8004 H'E670 8024*	32	√	√	√	√
DMA transfer count register_0	DMATCR_0	R/W	H'E670 8008	32	√	√	√	√
DMA transfer size register_0	DMATSR_0	R/W	H'E670 8028*	32	√	√	√	√
DMA channel control register_0	DMACHCR_0	R/W	H'E670 800C H'E670 802C*	32	√	√	√	√
DMA transfer count register B_0	DMATCRB_0	R/W	H'E670 8018	32	√	√	√	√
DMA transfer size register B_0	DMATSRB_0	R/W	H'E670 8038	32	√	√	√	√
DMA channel control register B_0	DMACHCRB_0	R/W	H'E670 801C	32	√	√	√	√
DMA extended resource selector_0	DMARS_0	R/W	H'E670 8040	16	√	√	√	√
DMA buffer control register_0	DMABUFCR_0	R/W	H'E670 8048	32	√	√	√	√
DMA descriptor base address register_0	DMADPBASE_0	R/W	H'E670 8050	32	√	√	√	√
DMA descriptor control register_0	DMADPCR_0	R/W	H'E670 8054	32	√	√	√	√
DMA fixed source address register_0	DMAFIXSAR_0	R/W	H'E670 8010	32	√	√	√	√
DMA fixed destination address register_0	DMAFIXDAR_0	R/W	H'E670 8014	32	√	√	√	√
DMA fixed descriptor base address register_0	DMAFIXDP BASE_0	R/W	H'E670 8060	32	√	√	√	√
DMA source address register_1	DMASAR_1	R/W	H'E670 8080 H'E670 80A0*	32	√	√	√	√
DMA destination address register_1	DMADAR_1	R/W	H'E670 8084 H'E670 80A4*	32	√	√	√	√
DMA transfer count register_1	DMATCR_1	R/W	H'E670 8088	32	√	√	√	√

Name	Abbreviation	R/W	Address	Access Size	RZ/G Series Products			
					RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
DMA transfer size register_1	DMATSR_1	R/W	H'E670 80A8*	32	√	√	√	√
DMA channel control register_1	DMACHCR_1	R/W	H'E670 808C H'E670 80AC*	32	√	√	√	√
DMA transfer count register B_1	DMATCRB_1	R/W	H'E670 8098	32	√	√	√	√
DMA transfer size register B_1	DMATSRB_1	R/W	H'E670 80B8*	32	√	√	√	√
DMA channel control register B_1	DMACHCRB_1	R/W	H'E670 809C	32	√	√	√	√
DMA extended resource selector_1	DMARS_1	R/W	H'E670 80C0	16	√	√	√	√
DMA buffer control register_1	DMABUFCR_1	R/W	H'E670 80C8	32	√	√	√	√
DMA descriptor base address register_1	DMADPBASE_1	R/W	H'E670 80D0	32	√	√	√	√
DMA descriptor control register_1	DMADPCR_1	R/W	H'E670 80D4	32	√	√	√	√
DMA fixed descriptor base address register_1	DMAFIXDPBASE_1	R/W	H'E670 80E0	32	√	√	√	√
DMA fixed source address register_1	DMAFIXSAR_1	R/W	H'E670 8090	32	√	√	√	√
DMA fixed destination address register_1	DMAFIXDAR_1	R/W	H'E670 8094	32	√	√	√	√
DMA source address register_2	DMASAR_2	R/W	H'E670 8100 H'E670 8120*	32	√	√	√	√
DMA destination address register_2	DMADAR_2	R/W	H'E670 8104 H'E670 8124*	32	√	√	√	√
DMA transfer count register_2	DMATCR_2	R/W	H'E670 8108	32	√	√	√	√
DMA transfer size register_2	DMATSR_2	R/W	H'E670 8128*	32	√	√	√	√
DMA channel control register_2	DMACHCR_2	R/W	H'E670 810C H'E670 812C*	32	√	√	√	√
DMA transfer count register B_2	DMATCRB_2	R/W	H'E670 8118	32	√	√	√	√
DMA transfer size register B_2	DMATSRB_2	R/W	H'E670 8138*	32	√	√	√	√
DMA channel control register B_2	DMACHCRB_2	R/W	H'E670 811C	32	√	√	√	√
DMA extended resource selector_2	DMARS_2	R/W	H'E670 8140	16	√	√	√	√
DMA buffer control register_2	DMABUFCR_2	R/W	H'E670 8148	32	√	√	√	√
DMA descriptor base address register_2	DMADPBASE_2	R/W	H'E670 8150	32	√	√	√	√
DMA descriptor control register_2	DMADPCR_2	R/W	H'E670 8154	32	√	√	√	√
DMA fixed source address register_2	DMAFIXSAR_2	R/W	H'E670 8110	32	√	√	√	√
DMA fixed destination address register_2	DMAFIXDAR_2	R/W	H'E670 8114	32	√	√	√	√
DMA fixed descriptor base address register_2	DMAFIXDPBASE_2	R/W	H'E670 8160	32	√	√	√	√
DMA source address register_3	DMASAR_3	R/W	H'E670 8180 H'E670 81A0*	32	√	√	√	√
DMA destination address register_3	DMADAR_3	R/W	H'E670 8184 H'E670 81A4*	32	√	√	√	√
DMA transfer count register_3	DMATCR_3	R/W	H'E670 8188	32	√	√	√	√
DMA transfer size register_3	DMATSR_3	R/W	H'E670 81A8*	32	√	√	√	√

Name	Abbreviation	R/W	Address	Access Size	RZ/G Series Products			
					RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
DMA channel control register_3	DMACHCR_3	R/W	H'E670 818C H'E670 81AC*	32	√	√	√	√
DMA transfer count register B_3	DMATCRB_3	R/W	H'E670 8198	32	√	√	√	√
DMA transfer size register B_3	DMATSRB_3	R/W	H'E670 81B8*	32	√	√	√	√
DMA channel control register B_3	DMACHCRB_3	R/W	H'E670 819C	32	√	√	√	√
DMA extended resource selector_3	DMARS_3	R/W	H'E670 81C0	16	√	√	√	√
DMA buffer control register_3	DMABUFCR_3	R/W	H'E670 81C8	32	√	√	√	√
DMA descriptor base address register_3	DMADPBASE_3	R/W	H'E670 81D0	32	√	√	√	√
DMA descriptor control register_3	DMADPCR_3	R/W	H'E670 81D4	32	√	√	√	√
DMA fixed source address register_3	DMAFIXSAR_3	R/W	H'E670 8190	32	√	√	√	√
DMA fixed destination address register_3	DMAFIXDAR_3	R/W	H'E670 8194	32	√	√	√	√
DMA fixed descriptor base address register_3	DMAFIXDPBASE_3	R/W	H'E670 81E0	32	√	√	√	√
DMA source address register_4	DMASAR_4	R/W	H'E670 8200 H'E670 8220*	32	√	√	√	√
DMA destination address register_4	DMADAR_4	R/W	H'E670 8204 H'E670 8224*	32	√	√	√	√
DMA transfer count register_4	DMATCR_4	R/W	H'E670 8208	32	√	√	√	√
DMA transfer size register_4	DMATSR_4	R/W	H'E670 8228*	32	√	√	√	√
DMA channel control register_4	DMACHCR_4	R/W	H'E670 820C H'E670 822C*	32	√	√	√	√
DMA transfer count register B_4	DMATCRB_4	R/W	H'E670 8218	32	√	√	√	√
DMA transfer size register B_4	DMATSRB_4	R/W	H'E670 8238*	32	√	√	√	√
DMA channel control register B_4	DMACHCRB_4	R/W	H'E670 821C	32	√	√	√	√
DMA extended resource selector_4	DMARS_4	R/W	H'E670 8240	16	√	√	√	√
DMA buffer control register_4	DMABUFCR_4	R/W	H'E670 8248	32	√	√	√	√
DMA descriptor base address register_4	DMADPBASE_4	R/W	H'E670 8250	32	√	√	√	√
DMA descriptor control register_4	DMADPCR_4	R/W	H'E670 8254	32	√	√	√	√
DMA fixed source address register_4	DMAFIXSAR_4	R/W	H'E670 8210	32	√	√	√	√
DMA fixed destination address register_4	DMAFIXDAR_4	R/W	H'E670 8214	32	√	√	√	√
DMA fixed descriptor base address register_4	DMAFIXDPBASE_4	R/W	H'E670 8260	32	√	√	√	√
DMA source address register_5	DMASAR_5	R/W	H'E670 8280 H'E670 82A0*	32	√	√	√	√
DMA destination address register_5	DMADAR_5	R/W	H'E670 8284 H'E670 82A4*	32	√	√	√	√
DMA transfer count register_5	DMATCR_5	R/W	H'E670 8288	32	√	√	√	√
DMA transfer size register_5	DMATSR_5	R/W	H'E670 82A8*	32	√	√	√	√
DMA channel control register_5	DMACHCR_5	R/W	H'E670 828C H'E670 82AC*	32	√	√	√	√

Name	Abbreviation	R/W	Address	Access Size	RZ/G Series Products			
					RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
DMA transfer count register B_5	DMATCRB_5	R/W	H'E670 8298	32	√	√	√	√
DMA transfer size register B_5	DMATSRB_5	R/W	H'E670 82B8*	32	√	√	√	√
DMA channel control register B_5	DMACHCRB_5	R/W	H'E670 829C	32	√	√	√	√
DMA extended resource selector_5	DMARS_5	R/W	H'E670 82C0	16	√	√	√	√
DMA buffer control register_5	DMABUFCR_5	R/W	H'E670 82C8	32	√	√	√	√
DMA descriptor base address register_5	DMADPBASE_5	R/W	H'E670 82D0	32	√	√	√	√
DMA descriptor control register_5	DMADPCR_5	R/W	H'E670 82D4	32	√	√	√	√
DMA fixed source address register_5	DMAFIXSAR_5	R/W	H'E670 8290	32	√	√	√	√
DMA fixed destination address register_5	DMAFIXDAR_5	R/W	H'E670 8294	32	√	√	√	√
DMA fixed descriptor base address register_5	DMAFIXDPBASE_5	R/W	H'E670 82E0	32	√	√	√	√
DMA source address register_6	DMASAR_6	R/W	H'E670 8300 H'E670 8320*	32	√	√	√	√
DMA destination address register_6	DMADAR_6	R/W	H'E670 8304 H'E670 8324*	32	√	√	√	√
DMA transfer count register_6	DMATCR_6	R/W	H'E670 8308	32	√	√	√	√
DMA transfer size register_6	DMATSR_6	R/W	H'E670 8328*	32	√	√	√	√
DMA channel control register_6	DMACHCR_6	R/W	H'E670 830C H'E670 832C*	32	√	√	√	√
DMA transfer count register B_6	DMATCRB_6	R/W	H'E670 8318	32	√	√	√	√
DMA transfer size register B_6	DMATSRB_6	R/W	H'E670 8338*	32	√	√	√	√
DMA channel control register B_6	DMACHCRB_6	R/W	H'E670 831C	32	√	√	√	√
DMA extended resource selector_6	DMARS_6	R/W	H'E670 8340	16	√	√	√	√
DMA buffer control register_6	DMABUFCR_6	R/W	H'E670 8348	32	√	√	√	√
DMA descriptor base address register_6	DMADPBASE_6	R/W	H'E670 8350	32	√	√	√	√
DMA descriptor control register_6	DMADPCR_6	R/W	H'E670 8354	32	√	√	√	√
DMA fixed source address register_6	DMAFIXSAR_6	R/W	H'E670 8310	32	√	√	√	√
DMA fixed destination address register_6	DMAFIXDAR_6	R/W	H'E670 8314	32	√	√	√	√
DMA fixed descriptor base address register_6	DMAFIXDPBASE_6	R/W	H'E670 8360	32	√	√	√	√
DMA source address register_7	DMASAR_7	R/W	H'E670 8380 H'E670 83A0*	32	√	√	√	√
DMA destination address register_7	DMADAR_7	R/W	H'E670 8384 H'E670 83A4*	32	√	√	√	√
DMA transfer count register_7	DMATCR_7	R/W	H'E670 8388	32	√	√	√	√
DMA transfer size register_7	DMATSR_7	R/W	H'E670 83A8*	32	√	√	√	√
DMA channel control register_7	DMACHCR_7	R/W	H'E670 838C H'E670 83AC*	32	√	√	√	√
DMA transfer count register B_7	DMATCRB_7	R/W	H'E670 8398	32	√	√	√	√
DMA transfer size register B_7	DMATSRB_7	R/W	H'E670 83B8*	32	√	√	√	√



Name	Abbreviation	R/W	Address	Access Size	RZ/G Series Products			
					RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
DMA channel control register B_7	DMACHCRB_7	R/W	H'E670 839C	32	√	√	√	√
DMA extended resource selector_7	DMARS_7	R/W	H'E670 83C0	16	√	√	√	√
DMA buffer control register_7	DMABUFCR_7	R/W	H'E670 83C8	32	√	√	√	√
DMA descriptor base address register_7	DMADPBASE_7	R/W	H'E670 83D0	32	√	√	√	√
DMA descriptor control register_7	DMADPCR_7	R/W	H'E670 83D4	32	√	√	√	√
DMA fixed source address register_7	DMAFIXSAR_7	R/W	H'E670 8390	32	√	√	√	√
DMA fixed destination address register_7	DMAFIXDAR_7	R/W	H'E670 8394	32	√	√	√	√
DMA fixed descriptor base address register_7	DMAFIXDPBASE_7	R/W	H'E670 83E0	32	√	√	√	√
DMA source address register_8	DMASAR_8	R/W	H'E670 8400 H'E670 8420*	32	√	√	√	√
DMA destination address register_8	DMADAR_8	R/W	H'E670 8404 H'E670 8424*	32	√	√	√	√
DMA transfer count register_8	DMATCR_8	R/W	H'E670 8408	32	√	√	√	√
DMA transfer size register_8	DMATSR_8	R/W	H'E670 8428*	32	√	√	√	√
DMA channel control register_8	DMACHCR_8	R/W	H'E670 840C H'E670 842C*	32	√	√	√	√
DMA transfer count register B_8	DMATCRB_8	R/W	H'E670 8418	32	√	√	√	√
DMA transfer size register B_8	DMATSRB_8	R/W	H'E670 8438*	32	√	√	√	√
DMA channel control register B_8	DMACHCRB_8	R/W	H'E670 841C	32	√	√	√	√
DMA extended resource selector_8	DMARS_8	R/W	H'E670 8440	16	√	√	√	√
DMA buffer control register_8	DMABUFCR_8	R/W	H'E670 8448	32	√	√	√	√
DMA descriptor base address register_8	DMADPBASE_8	R/W	H'E670 8450	32	√	√	√	√
DMA descriptor control register_8	DMADPCR_8	R/W	H'E670 8454	32	√	√	√	√
DMA fixed source address register_8	DMAFIXSAR_8	R/W	H'E670 8410	32	√	√	√	√
DMA fixed destination address register_8	DMAFIXDAR_8	R/W	H'E670 8414	32	√	√	√	√
DMA fixed descriptor base address register_8	DMAFIXDPBASE_8	R/W	H'E670 8460	32	√	√	√	√
DMA source address register_9	DMASAR_9	R/W	H'E670 8480 H'E670 84A0*	32	√	√	√	√
DMA destination address register_9	DMADAR_9	R/W	H'E670 8484 H'E670 84A4*	32	√	√	√	√
DMA transfer count register_9	DMATCR_9	R/W	H'E670 8488	32	√	√	√	√
DMA transfer size register_9	DMATSR_9	R/W	H'E670 84A8*	32	√	√	√	√
DMA channel control register_9	DMACHCR_9	R/W	H'E670 848C H'E670 84AC*	32	√	√	√	√
DMA transfer count register B_9	DMATCRB_9	R/W	H'E670 8498	32	√	√	√	√
DMA transfer size register B_9	DMATSRB_9	R/W	H'E670 84B8*	32	√	√	√	√
DMA channel control register B_9	DMACHCRB_9	R/W	H'E670 849C	32	√	√	√	√
DMA extended resource selector_9	DMARS_9	R/W	H'E670 84C0	16	√	√	√	√

Name	Abbreviation	R/W	Address	Access Size	RZ/G Series Products			
					RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
DMA buffer control register_9	DMABUFCR_9	R/W	H'E670 84C8	32	√	√	√	√
DMA descriptor base address register_9	DMADPBASE_9	R/W	H'E670 84D0	32	√	√	√	√
DMA descriptor control register_9	DMADPCR_9	R/W	H'E670 84D4	32	√	√	√	√
DMA fixed source address register_9	DMAFIXSAR_9	R/W	H'E670 8490	32	√	√	√	√
DMA fixed destination address register_9	DMAFIXDAR_9	R/W	H'E670 8494	32	√	√	√	√
DMA fixed descriptor base address register_9	DMAFIXDPBASE_9	R/W	H'E670 84E0	32	√	√	√	√
DMA source address register_10	DMASAR_10	R/W	H'E670 8500 H'E670 8520*	32	√	√	√	√
DMA destination address register_10	DMADAR_10	R/W	H'E670 8504 H'E670 8524*	32	√	√	√	√
DMA transfer count register_10	DMATCR_10	R/W	H'E670 8508	32	√	√	√	√
DMA transfer size register_10	DMATSR_10	R/W	H'E670 8528*	32	√	√	√	√
DMA channel control register_10	DMACHCR_10	R/W	H'E670 850C H'E670 852C*	32	√	√	√	√
DMA transfer count register B_10	DMATCRB_10	R/W	H'E670 8518	32	√	√	√	√
DMA transfer size register B_10	DMATSRB_10	R/W	H'E670 8538*	32	√	√	√	√
DMA channel control register B_10	DMACHCRB_10	R/W	H'E670 851C	32	√	√	√	√
DMA extended resource selector_10	DMARS_10	R/W	H'E670 8540	16	√	√	√	√
DMA buffer control register_10	DMABUFCR_10	R/W	H'E670 8548	32	√	√	√	√
DMA descriptor base address register_10	DMADPBASE_10	R/W	H'E670 8550	32	√	√	√	√
DMA descriptor control register_10	DMADPCR_10	R/W	H'E670 8554	32	√	√	√	√
DMA fixed source address register_10	DMAFIXSAR_10	R/W	H'E670 8510	32	√	√	√	√
DMA fixed destination address register_10	DMAFIXDAR_10	R/W	H'E670 8514	32	√	√	√	√
DMA fixed descriptor base address register_10	DMAFIXDPBASE_10	R/W	H'E670 8560	32	√	√	√	√
DMA source address register_11	DMASAR_11	R/W	H'E670 8580 H'E670 85A0*	32	√	√	√	√
DMA destination address register_11	DMADAR_11	R/W	H'E670 8584 H'E670 85A4*	32	√	√	√	√
DMA transfer count register_11	DMATCR_11	R/W	H'E670 8588	32	√	√	√	√
DMA transfer size register_11	DMATSR_11	R/W	H'E670 85A8*	32	√	√	√	√
DMA channel control register_11	DMACHCR_11	R/W	H'E670 858C H'E670 85AC*	32	√	√	√	√
DMA transfer count register B_11	DMATCRB_11	R/W	H'E670 8598	32	√	√	√	√
DMA transfer size register B_11	DMATSRB_11	R/W	H'E670 85B8*	32	√	√	√	√
DMA channel control register B_11	DMACHCRB_11	R/W	H'E670 859C	32	√	√	√	√
DMA extended resource selector_11	DMARS_11	R/W	H'E670 85C0	16	√	√	√	√
DMA buffer control register_11	DMABUFCR_11	R/W	H'E670 85C8	32	√	√	√	√
DMA descriptor base address register_11	DMADPBASE_11	R/W	H'E670 85D0	32	√	√	√	√

Name	Abbreviation	R/W	Address	Access Size	RZ/G Series Products			
					RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
DMA descriptor control register_11	DMADPCR_11	R/W	H'E670 85D4	32	√	√	√	√
DMA fixed source address register_11	DMAFIXSAR_11	R/W	H'E670 8590	32	√	√	√	√
DMA fixed destination address register_11	DMAFIXDAR_11	R/W	H'E670 8594	32	√	√	√	√
DMA fixed descriptor base address register_11	DMAFIXDPBASE_11	R/W	H'E670 85E0	32	√	√	√	√
DMA source address register_12	DMASAR_12	R/W	H'E670 8600 H'E670 8620*	32	√	√	√	√
DMA destination address register_12	DMADAR_12	R/W	H'E670 8604 H'E670 8624*	32	√	√	√	√
DMA transfer count register_12	DMATCR_12	R/W	H'E670 8608	32	√	√	√	√
DMA transfer size register_12	DMATSR_12	R/W	H'E670 8628*	32	√	√	√	√
DMA channel control register_12	DMACHCR_12	R/W	H'E670 860C H'E670 862C*	32	√	√	√	√
DMA transfer count register B_12	DMATCRB_12	R/W	H'E670 8618	32	√	√	√	√
DMA transfer size register B_12	DMATSRB_12	R/W	H'E670 8638*	32	√	√	√	√
DMA channel control register B_12	DMACHCRB_12	R/W	H'E670 861C	32	√	√	√	√
DMA extended resource selector_12	DMARS_12	R/W	H'E670 8640	16	√	√	√	√
DMA buffer control register_12	DMABUFCR_12	R/W	H'E670 8648	32	√	√	√	√
DMA descriptor base address register_12	DMADPBASE_12	R/W	H'E670 8650	32	√	√	√	√
DMA descriptor control register_12	DMADPCR_12	R/W	H'E670 8654	32	√	√	√	√
DMA fixed source address register_12	DMAFIXSAR_12	R/W	H'E670 8610	32	√	√	√	√
DMA fixed destination address register_12	DMAFIXDAR_12	R/W	H'E670 8614	32	√	√	√	√
DMA fixed descriptor base address register_12	DMAFIXDPBASE_12	R/W	H'E670 8660	32	√	√	√	√
DMA source address register_13	DMASAR_13	R/W	H'E670 8680 H'E670 86A0*	32	√	√	√	√
DMA destination address register_13	DMADAR_13	R/W	H'E670 8684 H'E670 86A4*	32	√	√	√	√
DMA transfer count register_13	DMATCR_13	R/W	H'E670 8688	32	√	√	√	√
DMA transfer size register_13	DMATSR_13	R/W	H'E670 86A8*	32	√	√	√	√
DMA channel control register_13	DMACHCR_13	R/W	H'E670 868C H'E670 86AC*	32	√	√	√	√
DMA transfer count register B_13	DMATCRB_13	R/W	H'E670 8698	32	√	√	√	√
DMA transfer size register B_13	DMATSRB_13	R/W	H'E670 86B8*	32	√	√	√	√
DMA channel control register B_13	DMACHCRB_13	R/W	H'E670 869C	32	√	√	√	√
DMA extended resource selector_13	DMARS_13	R/W	H'E670 86C0	16	√	√	√	√
DMA buffer control register_13	DMABUFCR_13	R/W	H'E670 86C8	32	√	√	√	√
DMA descriptor base address register_13	DMADPBASE_13	R/W	H'E670 86D0	32	√	√	√	√
DMA descriptor control register_13	DMADPCR_13	R/W	H'E670 86D4	32	√	√	√	√
DMA fixed source address register_13	DMAFIXSAR_13	R/W	H'E670 8690	32	√	√	√	√

Name	Abbreviation	R/W	Address	Access Size	RZ/G Series Products			
					RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
DMA fixed destination address register_13	DMAFIXDAR_13	R/W	H'E670 8694	32	√	√	√	√
DMA fixed descriptor base address register_13	DMAFIXDPBASE_13	R/W	H'E670 86E0	32	√	√	√	√
DMA source address register_14	DMASAR_14	R/W	H'E670 8700 H'E670 8720*	32	√	√	√	√
DMA destination address register_14	DMADAR_14	R/W	H'E670 8704 H'E670 8724*	32	√	√	√	√
DMA transfer count register_14	DMATCR_14	R/W	H'E670 8708	32	√	√	√	√
DMA transfer size register_14	DMATSR_14	R/W	H'E670 8728*	32	√	√	√	√
DMA channel control register_14	DMACHCR_14	R/W	H'E670 870C H'E670 872C*	32	√	√	√	√
DMA transfer count register B_14	DMATCRB_14	R/W	H'E670 8718	32	√	√	√	√
DMA transfer size register B_14	DMATSRB_14	R/W	H'E670 8738*	32	√	√	√	√
DMA channel control register B_14	DMACHCRB_14	R/W	H'E670 871C	32	√	√	√	√
DMA extended resource selector_14	DMARS_14	R/W	H'E670 8740	16	√	√	√	√
DMA buffer control register_14	DMABUFCR_14	R/W	H'E670 8748	32	√	√	√	√
DMA descriptor base address register_14	DMADPBASE_14	R/W	H'E670 8750	32	√	√	√	√
DMA descriptor control register_14	DMADPCR_14	R/W	H'E670 8754	32	√	√	√	√
DMA fixed source address register_14	DMAFIXSAR_14	R/W	H'E670 8710	32	√	√	√	√
DMA fixed destination address register_14	DMAFIXDAR_14	R/W	H'E670 8714	32	√	√	√	√
DMA fixed descriptor base address register_14	DMAFIXDPBASE_14	R/W	H'E670 8760	32	√	√	√	√
Descriptor memory (for lower-numbered channels)	DescriptorMEM	R/W	H'E670 A000 to H'E670 A7FC	32	√	√	√	√
DMA interrupt status register (for higher-numbered channels)	DMAISTA_U	R	H'E672 0020	32	√	√	√	√
DMA secure control register (for higher-numbered channels)	DMASEC_U	R/W	H'E672 0030	32	√	√	√	√
DMA operation register (for higher-numbered channels)	DMAOR_U	R/W	H'E672 0060	16	√	√	√	√
DMA channel clear register (for higher-numbered channels)	DMACHCLR_U	W	H'E672 0080	32	√	√	√	√
DPRAM secure control register (for higher-numbered channels)	DMADPSEC_U	R/W	H'E672 00A0	32	√	√	√	√
DMA source address register_15	DMASAR_15	R/W	H'E672 8000 H'E672 8020*	32	√	√	√	√
DMA destination address register_15	DMADAR_15	R/W	H'E672 8004 H'E672 8024*	32	√	√	√	√
DMA transfer count register_15	DMATCR_15	R/W	H'E672 8008	32	√	√	√	√
DMA transfer size register_15	DMATSR_15	R/W	H'E672 8028	32	√	√	√	√
DMA channel control register_15	DMACHCR_15	R/W	H'E672 800C H'E672 802C*	32	√	√	√	√

Name	Abbreviation	R/W	Address	Access Size	RZ/G Series Products			
					RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
DMA transfer count register B_15	DMATCRB_15	R/W	H'E672 8018	32	√	√	√	√
DMA transfer size register B_15	DMATSRB_15	R/W	H'E672 8038	32	√	√	√	√
DMA channel control register B_15	DMACHCRB_15	R/W	H'E672 801C	32	√	√	√	√
DMA extended resource selector_15	DMARS_15	R/W	H'E672 8040	16	√	√	√	√
DMA buffer control register_15	DMABUFCR_15	R/W	H'E672 8048	32	√	√	√	√
DMA descriptor base address register_15	DMADPBASE_15	R/W	H'E672 8050	32	√	√	√	√
DMA descriptor control register_15	DMADPCR_15	R/W	H'E672 8054	32	√	√	√	√
DMA fixed source address register_15	DMAFIXSAR_15	R/W	H'E672 8010	32	√	√	√	√
DMA fixed destination address register_15	DMAFIXDAR_15	R/W	H'E672 8014	32	√	√	√	√
DMA fixed descriptor base address register_15	DMAFIXDPBASE_15	R/W	H'E672 8060	32	√	√	√	√
DMA source address register_16	DMASAR_16	R/W	H'E672 8080 H'E672 80A0*	32	√	√	√	√
DMA destination address register_16	DMADAR_16	R/W	H'E672 8084 H'E672 80A4*	32	√	√	√	√
DMA transfer count register_16	DMATCR_16	R/W	H'E672 8088	32	√	√	√	√
DMA transfer size register_16	DMATSR_16	R/W	H'E672 80A8*	32	√	√	√	√
DMA channel control register_16	DMACHCR_16	R/W	H'E672 808C H'E67280AC*	32	√	√	√	√
DMA transfer count register B_16	DMATCRB_16	R/W	H'E672 8098	32	√	√	√	√
DMA transfer size register B_16	DMATSRB_16	R/W	H'E672 80B8*	32	√	√	√	√
DMA channel control register B_16	DMACHCRB_16	R/W	H'E672 809C	32	√	√	√	√
DMA extended resource selector_16	DMARS_16	R/W	H'E672 80C0	16	√	√	√	√
DMA buffer control register_16	DMABUFCR_16	R/W	H'E672 80C8	32	√	√	√	√
DMA descriptor base address register_16	DMADPBASE_16	R/W	H'E672 80D0	32	√	√	√	√
DMA descriptor control register_16	DMADPCR_16	R/W	H'E672 80D4	32	√	√	√	√
DMA fixed descriptor base address register_16	DMAFIXDPBASE_16	R/W	H'E672 80E0	32	√	√	√	√
DMA fixed source address register_16	DMAFIXSAR_16	R/W	H'E672 8090	32	√	√	√	√
DMA fixed destination address register_16	DMAFIXDAR_16	R/W	H'E672 8094	32	√	√	√	√
DMA source address register_17	DMASAR_17	R/W	H'E672 8100 H'E672 8120*	32	√	√	√	√
DMA destination address register_17	DMADAR_17	R/W	H'E672 8104 H'E672 8124*	32	√	√	√	√
DMA transfer count register_17	DMATCR_17	R/W	H'E672 8108	32	√	√	√	√
DMA transfer size register_17	DMATSR_17	R/W	H'E672 8128*	32	√	√	√	√
DMA channel control register_17	DMACHCR_17	R/W	H'E672 810C H'E672 812C*	32	√	√	√	√
DMA transfer count register B_17	DMATCRB_17	R/W	H'E672 8118	32	√	√	√	√
DMA transfer size register B_17	DMATSRB_17	R/W	H'E672 8138*	32	√	√	√	√

Name	Abbreviation	R/W	Address	Access Size	RZ/G Series Products			
					RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
DMA channel control register B_17	DMACHCRB_17	R/W	H'E672 811C	32	√	√	√	√
DMA extended resource selector_17	DMARS_17	R/W	H'E672 8140	16	√	√	√	√
DMA buffer control register_17	DMABUFCR_17	R/W	H'E672 8148	32	√	√	√	√
DMA descriptor base address register_17	DMADPBASE_17	R/W	H'E672 8150	32	√	√	√	√
DMA descriptor control register_17	DMADPCR_17	R/W	H'E672 8154	32	√	√	√	√
DMA fixed source address register_17	DMAFIXSAR_17	R/W	H'E672 8110	32	√	√	√	√
DMA fixed destination address register_17	DMAFIXDAR_17	R/W	H'E672 8114	32	√	√	√	√
DMA fixed descriptor base address register_17	DMAFIXDPBASE_17	R/W	H'E672 8160	32	√	√	√	√
DMA source address register_18	DMASAR_18	R/W	H'E672 8180 H'E672 81A0*	32	√	√	√	√
DMA destination address register_18	DMADAR_18	R/W	H'E672 8184 H'E672 81A4*	32	√	√	√	√
DMA transfer count register_18	DMATCR_18	R/W	H'E672 8188	32	√	√	√	√
DMA transfer size register_18	DMATSR_18	R/W	H'E672 81A8*	32	√	√	√	√
DMA channel control register_18	DMACHCR_18	R/W	H'E672 818C H'E672 81AC*	32	√	√	√	√
DMA transfer count register B_18	DMATCRB_18	R/W	H'E672 8198	32	√	√	√	√
DMA transfer size register B_18	DMATSRB_18	R/W	H'E672 81B8*	32	√	√	√	√
DMA channel control register B_18	DMACHCRB_18	R/W	H'E672 819C	32	√	√	√	√
DMA extended resource selector_18	DMARS_18	R/W	H'E672 81C0	16	√	√	√	√
DMA buffer control register_18	DMABUFCR_18	R/W	H'E672 81C8	32	√	√	√	√
DMA descriptor base address register_18	DMADPBASE_18	R/W	H'E672 81D0	32	√	√	√	√
DMA descriptor control register_18	DMADPCR_18	R/W	H'E672 81D4	32	√	√	√	√
DMA fixed source address register_18	DMAFIXSAR_18	R/W	H'E672 8190	32	√	√	√	√
DMA fixed destination address register_18	DMAFIXDAR_18	R/W	H'E672 8194	32	√	√	√	√
DMA fixed descriptor base address register_18	DMAFIXDPBASE_18	R/W	H'E672 81E0	32	√	√	√	√
DMA source address register_19	DMASAR_19	R/W	H'E672 8200 H'E672 8220*	32	√	√	√	√
DMA destination address register_19	DMADAR_19	R/W	H'E672 8204 H'E672 8224*	32	√	√	√	√
DMA transfer count register_19	DMATCR_19	R/W	H'E672 8208	32	√	√	√	√
DMA transfer size register_19	DMATSR_19	R/W	H'E672 8228*	32	√	√	√	√
DMA channel control register_19	DMACHCR_19	R/W	H'E672 820C H'E672 822C*	32	√	√	√	√
DMA transfer count register B_19	DMATCRB_19	R/W	H'E672 8218	32	√	√	√	√
DMA transfer size register B_19	DMATSRB_19	R/W	H'E672 8238*	32	√	√	√	√
DMA channel control register B_19	DMACHCRB_19	R/W	H'E672 821C	32	√	√	√	√
DMA extended resource selector_19	DMARS_19	R/W	H'E672 8240	16	√	√	√	√

Name	Abbreviation	R/W	Address	Access Size	RZ/G Series Products			
					RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
DMA buffer control register_19	DMABUFCR_19	R/W	H'E672 8248	32	√	√	√	√
DMA descriptor base address register_19	DMADPBASE_19	R/W	H'E672 8250	32	√	√	√	√
DMA descriptor control register_19	DMADPCR_19	R/W	H'E672 8254	32	√	√	√	√
DMA fixed source address register_19	DMAFIXSAR_19	R/W	H'E672 8210	32	√	√	√	√
DMA fixed destination address register_19	DMAFIXDAR_19	R/W	H'E672 8214	32	√	√	√	√
DMA fixed descriptor base address register_19	DMAFIXDPBASE_19	R/W	H'E672 8260	32	√	√	√	√
DMA source address register_20	DMASAR_20	R/W	H'E672 8280 H'E672 82A0*	32	√	√	√	√
DMA destination address register_20	DMADAR_20	R/W	H'E672 8284 H'E672 82A4*	32	√	√	√	√
DMA transfer count register_20	DMATCR_20	R/W	H'E672 8288	32	√	√	√	√
DMA transfer size register_20	DMATSR_20	R/W	H'E672 82A8*	32	√	√	√	√
DMA channel control register_20	DMACHCR_20	R/W	H'E672 828C H'E672 82AC*	32	√	√	√	√
DMA transfer count register B_20	DMATCRB_20	R/W	H'E672 8298	32	√	√	√	√
DMA transfer size register B_20	DMATSRB_20	R/W	H'E672 82B8*	32	√	√	√	√
DMA channel control register B_20	DMACHCRB_20	R/W	H'E672 829C	32	√	√	√	√
DMA extended resource selector_20	DMARS_20	R/W	H'E672 82C0	16	√	√	√	√
DMA buffer control register_20	DMABUFCR_20	R/W	H'E672 82C8	32	√	√	√	√
DMA descriptor base address register_20	DMADPBASE_20	R/W	H'E672 82D0	32	√	√	√	√
DMA descriptor control register_20	DMADPCR_20	R/W	H'E672 82D4	32	√	√	√	√
DMA fixed source address register_20	DMAFIXSAR_20	R/W	H'E672 8290	32	√	√	√	√
DMA fixed destination address register_20	DMAFIXDAR_20	R/W	H'E672 8294	32	√	√	√	√
DMA fixed descriptor base address register_20	DMAFIXDPBASE_20	R/W	H'E672 82E0	32	√	√	√	√
DMA source address register_21	DMASAR_21	R/W	H'E672 8300 H'E672 8320*	32	√	√	√	√
DMA destination address register_21	DMADAR_21	R/W	H'E672 8304 H'E672 8324*	32	√	√	√	√
DMA transfer count register_21	DMATCR_21	R/W	H'E672 8308	32	√	√	√	√
DMA transfer size register_21	DMATSR_21	R/W	H'E672 8328*	32	√	√	√	√
DMA channel control register_21	DMACHCR_21	R/W	H'E672 830C H'E672 832C*	32	√	√	√	√
DMA transfer count register B_21	DMATCRB_21	R/W	H'E672 8318	32	√	√	√	√
DMA transfer size register B_21	DMATSRB_21	R/W	H'E672 8338*	32	√	√	√	√
DMA channel control register B_21	DMACHCRB_21	R/W	H'E672 831C	32	√	√	√	√
DMA extended resource selector_21	DMARS_21	R/W	H'E672 8340	16	√	√	√	√
DMA buffer control register_21	DMABUFCR_21	R/W	H'E672 8348	32	√	√	√	√
DMA descriptor base address register_21	DMADPBASE_21	R/W	H'E672 8350	32	√	√	√	√

Name	Abbreviation	R/W	Address	Access Size	RZ/G Series Products			
					RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
DMA descriptor control register_21	DMADPCR_21	R/W	H'E672 8354	32	√	√	√	√
DMA fixed source address register_21	DMAFIXSAR_21	R/W	H'E672 8310	32	√	√	√	√
DMA fixed destination address register_21	DMAFIXDAR_21	R/W	H'E672 8314	32	√	√	√	√
DMA fixed descriptor base address register_21	DMAFIXDPBASE_21	R/W	H'E672 8360	32	√	√	√	√
DMA source address register_22	DMASAR_22	R/W	H'E672 8380 H'E672 83A0*	32	√	√	√	√
DMA destination address register_22	DMADAR_22	R/W	H'E672 8384 H'E672 83A4*	32	√	√	√	√
DMA transfer count register_22	DMATCR_22	R/W	H'E672 8388	32	√	√	√	√
DMA transfer size register_22	DMATSR_22	R/W	H'E672 83A8*	32	√	√	√	√
DMA channel control register_22	DMACHCR_22	R/W	H'E672 838C H'E672 83AC*	32	√	√	√	√
DMA transfer count register B_22	DMATCRB_22	R/W	H'E672 8398	32	√	√	√	√
DMA transfer size register B_22	DMATSRB_22	R/W	H'E672 83B8*	32	√	√	√	√
DMA channel control register B_22	DMACHCRB_22	R/W	H'E672 839C	32	√	√	√	√
DMA extended resource selector_22	DMARS_22	R/W	H'E672 83C0	16	√	√	√	√
DMA buffer control register_22	DMABUFCR_22	R/W	H'E672 83C8	32	√	√	√	√
DMA descriptor base address register_22	DMADPBASE_22	R/W	H'E672 83D0	32	√	√	√	√
DMA descriptor control register_22	DMADPCR_22	R/W	H'E672 83D4	32	√	√	√	√
DMA fixed source address register_22	DMAFIXSAR_22	R/W	H'E672 8390	32	√	√	√	√
DMA fixed destination address register_22	DMAFIXDAR_22	R/W	H'E672 8394	32	√	√	√	√
DMA fixed descriptor base address register_22	DMAFIXDPBASE_22	R/W	H'E672 83E0	32	√	√	√	√
DMA source address register_23	DMASAR_23	R/W	H'E672 8400 H'E672 8420*	32	√	√	√	√
DMA destination address register_23	DMADAR_23	R/W	H'E672 8404 H'E672 8424*	32	√	√	√	√
DMA transfer count register_23	DMATCR_23	R/W	H'E672 8408	32	√	√	√	√
DMA transfer size register_23	DMATSR_23	R/W	H'E672 8428*	32	√	√	√	√
DMA channel control register_23	DMACHCR_23	R/W	H'E672 840C H'E672 842C*	32	√	√	√	√
DMA transfer count register B_23	DMATCRB_23	R/W	H'E672 8418	32	√	√	√	√
DMA transfer size register B_23	DMATSRB_23	R/W	H'E672 8438*	32	√	√	√	√
DMA channel control register B_23	DMACHCRB_23	R/W	H'E672 841C	32	√	√	√	√
DMA extended resource selector_23	DMARS_23	R/W	H'E672 8440	16	√	√	√	√
DMA buffer control register_23	DMABUFCR_23	R/W	H'E672 8448	32	√	√	√	√
DMA descriptor base address register_23	DMADPBASE_23	R/W	H'E672 8450	32	√	√	√	√
DMA descriptor control register_23	DMADPCR_23	R/W	H'E672 8454	32	√	√	√	√
DMA fixed source address register_23	DMAFIXSAR_23	R/W	H'E672 8410	32	√	√	√	√



Name	Abbreviation	R/W	Address	Access Size	RZ/G Series Products			
					RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
DMA fixed destination address register_23	DMAFIXDAR_23	R/W	H'E672 8414	32	√	√	√	√
DMA fixed descriptor base address register_23	DMAFIXDPBASE_23	R/W	H'E672 8460	32	√	√	√	√
DMA source address register_24	DMASAR_24	R/W	H'E672 8480 H'E672 84A0*	32	√	√	√	√
DMA destination address register_24	DMADAR_24	R/W	H'E672 8484 H'E672 84A4*	32	√	√	√	√
DMA transfer count register_24	DMATCR_24	R/W	H'E672 8488	32	√	√	√	√
DMA transfer size register_24	DMATSR_24	R/W	H'E672 84A8*	32	√	√	√	√
DMA channel control register_24	DMACHCR_24	R/W	H'E672 848C H'E672 84AC*	32	√	√	√	√
DMA transfer count register B_24	DMATCRB_24	R/W	H'E672 8498	32	√	√	√	√
DMA transfer size register B_24	DMATSRB_24	R/W	H'E672 84B8*	32	√	√	√	√
DMA channel control register B_24	DMACHCRB_24	R/W	H'E672 849C	32	√	√	√	√
DMA extended resource selector_24	DMARS_24	R/W	H'E672 84C0	16	√	√	√	√
DMA buffer control register_24	DMABUFCR_24	R/W	H'E672 84C8	32	√	√	√	√
DMA descriptor base address register_24	DMADPBASE_24	R/W	H'E672 84D0	32	√	√	√	√
DMA descriptor control register_24	DMADPCR_24	R/W	H'E672 84D4	32	√	√	√	√
DMA fixed source address register_24	DMAFIXSAR_24	R/W	H'E672 8490	32	√	√	√	√
DMA fixed destination address register_24	DMAFIXDAR_24	R/W	H'E672 8494	32	√	√	√	√
DMA fixed descriptor base address register_24	DMAFIXDPBASE_24	R/W	H'E672 84E0	32	√	√	√	√
DMA source address register_25	DMASAR_25	R/W	H'E672 8500 H'E672 8520*	32	√	√	√	√
DMA destination address register_25	DMADAR_25	R/W	H'E672 8504 H'E672 8524*	32	√	√	√	√
DMA transfer count register_25	DMATCR_25	R/W	H'E672 8508	32	√	√	√	√
DMA transfer size register_25	DMATSR_25	R/W	H'E672 8528*	32	√	√	√	√
DMA channel control register_25	DMACHCR_25	R/W	H'E672 850C H'E672 852C*	32	√	√	√	√
DMA transfer count register B_25	DMATCRB_25	R/W	H'E672 8518	32	√	√	√	√
DMA transfer size register B_25	DMATSRB_25	R/W	H'E672 8538*	32	√	√	√	√
DMA channel control register B_25	DMACHCRB_25	R/W	H'E672 851C	32	√	√	√	√
DMA extended resource selector_25	DMARS_25	R/W	H'E672 8540	16	√	√	√	√
DMA buffer control register_25	DMABUFCR_25	R/W	H'E672 8548	32	√	√	√	√
DMA descriptor base address register_25	DMADPBASE_25	R/W	H'E672 8550	32	√	√	√	√
DMA descriptor control register_25	DMADPCR_25	R/W	H'E672 8554	32	√	√	√	√
DMA fixed source address register_25	DMAFIXSAR_25	R/W	H'E672 8510	32	√	√	√	√
DMA fixed destination address register_25	DMAFIXDAR_25	R/W	H'E672 8514	32	√	√	√	√
DMA fixed descriptor base address register_25	DMAFIXDPBASE_25	R/W	H'E672 8560	32	√	√	√	√

Name	Abbreviation	R/W	Address	Access Size	RZ/G Series Products			
					RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
DMA source address register_26	DMASAR_26	R/W	H'E672 8580 H'E672 85A0*	32	√	√	√	√
DMA destination address register_26	DMADAR_26	R/W	H'E672 8584 H'E672 85A4*	32	√	√	√	√
DMA transfer count register_26	DMATCR_26	R/W	H'E672 8588	32	√	√	√	√
DMA transfer size register_26	DMATSR_26	R/W	H'E672 85A8*	32	√	√	√	√
DMA channel control register_26	DMACHCR_26	R/W	H'E672 858C H'E672 85AC*	32	√	√	√	√
DMA transfer count register B_26	DMATCRB_26	R/W	H'E672 8598	32	√	√	√	√
DMA transfer size register B_26	DMATSRB_26	R/W	H'E672 85B8*	32	√	√	√	√
DMA channel control register B_26	DMACHCRB_26	R/W	H'E672 859C	32	√	√	√	√
DMA extended resource selector_26	DMARS_26	R/W	H'E672 85C0	16	√	√	√	√
DMA buffer control register_26	DMABUFCR_26	R/W	H'E672 85C8	32	√	√	√	√
DMA descriptor base address register_26	DMADPBASE_26	R/W	H'E672 85D0	32	√	√	√	√
DMA descriptor control register_26	DMADPCR_26	R/W	H'E672 85D4	32	√	√	√	√
DMA fixed source address register_26	DMAFIXSAR_26	R/W	H'E672 8590	32	√	√	√	√
DMA fixed destination address register_26	DMAFIXDAR_26	R/W	H'E672 8594	32	√	√	√	√
DMA fixed descriptor base address register_26	DMAFIXDPBASE_26	R/W	H'E672 85E0	32	√	√	√	√
DMA source address register_27	DMASAR_27	R/W	H'E672 8600 H'E672 8620*	32	√	√	√	√
DMA destination address register_27	DMADAR_27	R/W	H'E672 8604 H'E672 8624*	32	√	√	√	√
DMA transfer count register_27	DMATCR_27	R/W	H'E672 8608	32	√	√	√	√
DMA transfer size register_27	DMATSR_27	R/W	H'E672 8628*	32	√	√	√	√
DMA channel control register_27	DMACHCR_27	R/W	H'E672 860C H'E672 862C*	32	√	√	√	√
DMA transfer count register B_27	DMATCRB_27	R/W	H'E672 8618	32	√	√	√	√
DMA transfer size register B_27	DMATSRB_27	R/W	H'E672 8638*	32	√	√	√	√
DMA channel control register B_27	DMACHCRB_27	R/W	H'E672 861C	32	√	√	√	√
DMA extended resource selector_27	DMARS_27	R/W	H'E672 8640	16	√	√	√	√
DMA buffer control register_27	DMABUFCR_27	R/W	H'E672 8648	32	√	√	√	√
DMA descriptor base address register_27	DMADPBASE_27	R/W	H'E672 8650	32	√	√	√	√
DMA descriptor control register_27	DMADPCR_27	R/W	H'E672 8654	32	√	√	√	√
DMA fixed source address register_27	DMAFIXSAR_27	R/W	H'E672 8610	32	√	√	√	√
DMA fixed destination address register_27	DMAFIXDAR_27	R/W	H'E672 8614	32	√	√	√	√
DMA fixed descriptor base address register_27	DMAFIXDPBASE_27	R/W	H'E672 8660	32	√	√	√	√
DMA source address register_28	DMASAR_28	R/W	H'E672 8680 H'E672 86A0*	32	√	√	√	√

Name	Abbreviation	R/W	Address	Access Size	RZ/G Series Products			
					RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
DMA destination address register_28	DMADAR_28	R/W	H'E672 8684 H'E672 86A4*	32	√	√	√	√
DMA transfer count register_28	DMATCR_28	R/W	H'E672 8688	32	√	√	√	√
DMA transfer size register_28	DMATSR_28	R/W	H'E672 86A8*	32	√	√	√	√
DMA channel control register_28	DMACHCR_28	R/W	H'E672 868C H'E672 86AC*	32	√	√	√	√
DMA transfer count register B_28	DMATCRB_28	R/W	H'E672 8698	32	√	√	√	√
DMA transfer size register B_28	DMATSRB_28	R/W	H'E672 86B8*	32	√	√	√	√
DMA channel control register B_28	DMACHCRB_28	R/W	H'E672 869C	32	√	√	√	√
DMA extended resource selector_28	DMARS_28	R/W	H'E672 86C0	16	√	√	√	√
DMA buffer control register_28	DMABUFCR_28	R/W	H'E672 86C8	32	√	√	√	√
DMA descriptor base address register_28	DMADPBASE_28	R/W	H'E672 86D0	32	√	√	√	√
DMA descriptor control register_28	DMADPCR_28	R/W	H'E672 86D4	32	√	√	√	√
DMA fixed source address register_28	DMAFIXSAR_28	R/W	H'E672 8690	32	√	√	√	√
DMA fixed destination address register_28	DMAFIXDAR_28	R/W	H'E672 8694	32	√	√	√	√
DMA fixed descriptor base address register_28	DMAFIXDPBASE_28	R/W	H'E672 86E0	32	√	√	√	√
DMA source address register_29	DMASAR_29	R/W	H'E672 8700 H'E672 8720*	32	√	√	√	√
DMA destination address register_29	DMADAR_29	R/W	H'E672 8704 H'E672 8724*	32	√	√	√	√
DMA transfer count register_29	DMATCR_29	R/W	H'E672 8708	32	√	√	√	√
DMA transfer size register_29	DMATSR_29	R/W	H'E672 8728*	32	√	√	√	√
DMA channel control register_29	DMACHCR_29	R/W	H'E672 870C H'E672 872C*	32	√	√	√	√
DMA transfer count register B_29	DMATCRB_29	R/W	H'E672 8718	32	√	√	√	√
DMA transfer size register B_29	DMATSRB_29	R/W	H'E672 8738*	32	√	√	√	√
DMA channel control register B_29	DMACHCRB_29	R/W	H'E672 871C	32	√	√	√	√
DMA extended resource selector_29	DMARS_29	R/W	H'E672 8740	16	√	√	√	√
DMA buffer control register_29	DMABUFCR_29	R/W	H'E672 8748	32	√	√	√	√
DMA descriptor base address register_29	DMADPBASE_29	R/W	H'E672 8750	32	√	√	√	√
DMA descriptor control register_29	DMADPCR_29	R/W	H'E672 8754	32	√	√	√	√
DMA fixed source address register_29	DMAFIXSAR_29	R/W	H'E672 8710	32	√	√	√	√
DMA fixed destination address register_29	DMAFIXDAR_29	R/W	H'E672 8714	32	√	√	√	√
DMA fixed descriptor base address register_29	DMAFIXDPBASE_29	R/W	H'E672 8760	32	√	√	√	√
Descriptor memory (for higher-numbered channels)	DescriptorMEM	R/W	H'E672 A000 to H'E672 A7FC	32	√	√	√	√

Notes: The base address of registers for the lower-numbered channels (0 to 14) is H'E670 0000.

The base address of registers for the higher-numbered channels (15 to 29) is H'E672 0000.

\* This address is used in total size transmission (see section 16.4.6, Total Size Transmission).

**Table 16.2 States of SYS-DMAC Registers in each Operating Mode**

<b>Abbreviation</b>	<b>Power-On Reset</b>	<b>Module Standby</b>
DMAISTA_L/DMAISTA_U	Initialized	Retained
DMASEC_L/DMASEC_U	Initialized	Retained
DMAOR_L/DMAOR_U	Initialized	Retained
DMACHCLR_L/DMACHCLR_U	Initialized	Retained
DMADPSEC_L/DMADPSEC_U	Initialized	Retained
DMASAR_0 to DMASAR_29	Initialized	Retained
DMADAR_0 to DMADAR_29	Initialized	Retained
DMATCR_0 to DMATCR_29	Initialized	Retained
DMATSR_0 to DMATSR_29	Initialized	Retained
DMACHCR_0 to DMACHCR_29	Initialized	Retained
DMATCRB_0 DMATCRB_29	Initialized	Retained
DMATSRB_0 to DMATSRB_29	Initialized	Retained
DMACHCRB_0 to DMACHCRB_29	Initialized	Retained
DMABUFCR_0 to DMABUFCR_29	Initialized	Retained
DMARS_0 to DMARS_29	Initialized	Retained
DMADPBASE_0 to DMADPBASE_29	Initialized	Retained
DMADPCR_0 DMADPCR_29	Initialized	Retained
DMAFIXSAR_0 to DMAFIXSAR_29	Initialized	Retained
DMAFIXDAR_0 to DMAFIXDAR_29	Initialized	Retained
DMAFIXDPBASE_0 to DMAFIXDPBASE_29	Initialized	Retained
DescriptorMEM	Undefined	Retained

### 16.3.1 DMA Interrupt Status Register for Lower-Numbered Channels (DMAISTA\_L)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

DMAISTA\_L is a 32-bit readable register that indicates the states of the interrupt signals for each of the lower-numbered channels.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 15	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
14	I14	0	R	Interrupt State in Channel 14 0: An interrupt is not present. 1: An interrupt is present.
13	I13	0	R	Interrupt State in Channel 13 0: An interrupt is not present. 1: An interrupt is present.
12	I12	0	R	Interrupt State in Channel 12 0: An interrupt is not present. 1: An interrupt is present.
11	I11	0	R	Interrupt State in Channel 11 0: An interrupt is not present. 1: An interrupt is present.
10	I10	0	R	Interrupt State in Channel 10 0: An interrupt is not present. 1: An interrupt is present.
9	I9	0	R	Interrupt State in Channel 9 0: An interrupt is not present. 1: An interrupt is present.
8	I8	0	R	Interrupt State in Channel 8 0: An interrupt is not present. 1: An interrupt is present.

Bit	Bit Name	Initial Value	R/W	Descriptions
7	I7	0	R	Interrupt State in Channel 7 0: An interrupt is not present. 1: An interrupt is present.
6	I6	0	R	Interrupt State in Channel 6 0: An interrupt is not present. 1: An interrupt is present.
5	I5	0	R	Interrupt State in Channel 5 0: An interrupt is not present. 1: An interrupt is present.
4	I4	0	R	Interrupt State in Channel 4 0: An interrupt is not present. 1: An interrupt is present.
3	I3	0	R	Interrupt State in Channel 3 0: An interrupt is not present. 1: An interrupt is present.
2	I2	0	R	Interrupt State in Channel 2 0: An interrupt is not present. 1: An interrupt is present.
1	I1	0	R	Interrupt State in Channel 1 0: An interrupt is not present. 1: An interrupt is present.
0	I0	0	R	Interrupt State in Channel 0 0: An interrupt is not present. 1: An interrupt is present.

### 16.3.2 DMA Interrupt Status Register for Higher-Numbered Channels (DMAISTA\_U)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

DMAISTA\_U is a 32-bit readable register that indicates the states of the interrupt signals for each of the higher-numbered channels.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	I29	I28	I27	I26	I25	I24	I23	I22	I21	I20	I19	I18	I17	I16	I15
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 15	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
14	I29	0	R	Interrupt State in Channel 29 0: An interrupt is not present. 1: An interrupt is present.
13	I28	0	R	Interrupt State in Channel 28 0: An interrupt is not present. 1: An interrupt is present.
12	I27	0	R	Interrupt State in Channel 27 0: An interrupt is not present. 1: An interrupt is present.
11	I26	0	R	Interrupt State in Channel 26 0: An interrupt is not present. 1: An interrupt is present.
10	I25	0	R	Interrupt State in Channel 25 0: An interrupt is not present. 1: An interrupt is present.
9	I24	0	R	Interrupt State in Channel 24 0: An interrupt is not present. 1: An interrupt is present.
8	I23	0	R	Interrupt State in Channel 23 0: An interrupt is not present. 1: An interrupt is present.
7	I22	0	R	Interrupt State in Channel 22 0: An interrupt is not present. 1: An interrupt is present.

Bit	Bit Name	Initial Value	R/W	Descriptions
6	I21	0	R	Interrupt State in Channel 21 0: An interrupt is not present. 1: An interrupt is present.
5	I20	0	R	Interrupt State in Channel 20 0: An interrupt is not present. 1: An interrupt is present.
4	I19	0	R	Interrupt State in Channel 19 0: An interrupt is not present. 1: An interrupt is present.
3	I18	0	R	Interrupt State in Channel 18 0: An interrupt is not present. 1: An interrupt is present.
2	I17	0	R	Interrupt State in Channel 17 0: An interrupt is not present. 1: An interrupt is present.
1	I16	0	R	Interrupt State in Channel 16 0: An interrupt is not present. 1: An interrupt is present.
0	I15	0	R	Interrupt State in Channel 15 0: An interrupt is not present. 1: An interrupt is present.



### 16.3.3 DMA Secure Control Register for Lower-Numbered Channels (DMASEC\_L)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

DMASEC\_L is a 32-bit readable/writeable register that controls the security attribute of each of the lower-numbered channels. Only the initiator in the secure mode can change the setting of this register.

Only secure access is allowed to registers of channels with the secure mode setting. The following registers are protected by the secure mode.

DMASAR, DMADAR, DMATCR, DMATSR, DMACHCR, DMATCRB, DMATSRB, DMACHCRB, DMARS, DMABUFCR, DMADPBASE, DMADPCR, DMAFIXSAR, DMAFIXDAR, and DMAFIXDPBASE

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	S14	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	S0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 15	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
14	S14	0	R/W	Secure Mode Setting for Channel 14 0: Non-secure mode 1: Secure mode
13	S13	0	R/W	Secure Mode Setting for Channel 13 0: Non-secure mode 1: Secure mode
12	S12	0	R/W	Secure Mode Setting for Channel 12 0: Non-secure mode 1: Secure mode
11	S11	0	R/W	Secure Mode Setting for Channel 11 0: Non-secure mode 1: Secure mode
10	S10	0	R/W	Secure Mode Setting for Channel 10 0: Non-secure mode 1: Secure mode
9	S9	0	R/W	Secure Mode Setting for Channel 9 0: Non-secure mode 1: Secure mode

Bit	Bit Name	Initial Value	R/W	Descriptions
8	S8	0	R/W	Secure Mode Setting for Channel 8 0: Non-secure mode 1: Secure mode
7	S7	0	R/W	Secure Mode Setting for Channel 7 0: Non-secure mode 1: Secure mode
6	S6	0	R/W	Secure Mode Setting for Channel 6 0: Non-secure mode 1: Secure mode
5	S5	0	R/W	Secure Mode Setting for Channel 5 0: Non-secure mode 1: Secure mode
4	S4	0	R/W	Secure Mode Setting for Channel 4 0: Non-secure mode 1: Secure mode
3	S3	0	R/W	Secure Mode Setting for Channel 3 0: Non-secure mode 1: Secure mode
2	S2	0	R/W	Secure Mode Setting for Channel 2 0: Non-secure mode 1: Secure mode
1	S1	0	R/W	Secure Mode Setting for Channel 1 0: Non-secure mode 1: Secure mode
0	S0	0	R/W	Secure Mode Setting for Channel 0 0: Non-secure mode 1: Secure mode

### 16.3.4 DMA Secure Control Register Higher-Numbered Channels (DMASEC\_U)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

DMASEC\_U is a 32-bit readable/writable register that controls the security attribute of each of the higher-numbered channels. Only the initiator in the secure mode can change the setting of this register.

Only secure access is allowed to registers of channels with the secure mode setting. The following registers are protected by the secure mode.

DMASAR, DMADAR, DMATCR, DMATSR, DMACHCR, DMATCRB, DMATSRB, DMACHCRB, DMARS, DMABUFCR, DMADPBASE, DMADPCR, DMAFIXSAR, DMAFIXDAR, and DMAFIXDPBASE

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	S29	S28	S27	S26	S25	S24	S23	S22	S21	S20	S19	S18	S17	S16	S15
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 15	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
14	S29	0	R/W	Secure Mode Setting for Channel 29 0: Non-secure mode 1: Secure mode
13	S28	0	R/W	Secure Mode Setting for Channel 28 0: Non-secure mode 1: Secure mode
12	S27	0	R/W	Secure Mode Setting for Channel 27 0: Non-secure mode 1: Secure mode
11	S26	0	R/W	Secure Mode Setting for Channel 26 0: Non-secure mode 1: Secure mode
10	S25	0	R/W	Secure Mode Setting for Channel 25 0: Non-secure mode 1: Secure mode
9	S24	0	R/W	Secure Mode Setting for Channel 24 0: Non-secure mode 1: Secure mode

Bit	Bit Name	Initial Value	R/W	Descriptions
8	S23	0	R/W	Secure Mode Setting for Channel 23 0: Non-secure mode 1: Secure mode
7	S22	0	R/W	Secure Mode Setting for Channel 22 0: Non-secure mode 1: Secure mode
6	S21	0	R/W	Secure Mode Setting for Channel 21 0: Non-secure mode 1: Secure mode
5	S20	0	R/W	Secure Mode Setting for Channel 20 0: Non-secure mode 1: Secure mode
4	S19	0	R/W	Secure Mode Setting for Channel 19 0: Non-secure mode 1: Secure mode
3	S18	0	R/W	Secure Mode Setting for Channel 18 0: Non-secure mode 1: Secure mode
2	S17	0	R/W	Secure Mode Setting for Channel 17 0: Non-secure mode 1: Secure mode
1	S16	0	R/W	Secure Mode Setting for Channel 16 0: Non-secure mode 1: Secure mode
0	S15	0	R/W	Secure Mode Setting for Channel 15 0: Non-secure mode 1: Secure mode

### 16.3.5 DMA Operation Register for Lower-Numbered Channels (DMAOR\_L)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

DMAOR\_L is a 16-bit readable/writable register that enables DMA transfer on all lower-numbered channels and specifies the method used to determine the priority levels for all lower-numbered DMA channels. This register also indicates address errors.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	PR[1:0]	—	—	—	—	—	—	AE	—	DME
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R	R	R	R	R	R/(W)*	R	R/W

Bit	Bit Name	Initial Value	R/W	Descriptions
15 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9, 8	PR[1:0]	00	R/W	Priority Mode Select the method for setting the order of priority of channels when transfer requests for multiple channels arrive simultaneously. 00: Fixed CH0 > CH1 > ... > CH13 > CH14 11: Round-robin priority Other than above: Setting prohibited
7 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2	AE	0	R/(W)*	Address Error Flag Indicates that an address error interrupt occurred during DMA transfer. This bit is set under the following conditions: The value set in DMASAR or DMADAR does not fall on a boundary corresponding to the transfer size. The source or destination for transfer is in an invalid space. The source or destination for transfer is in module stop mode. If this bit is set, DMA transfer through the channel is not possible even if the DE bit is set to 1. To clear the AE bit, write 0 to the AE bit after reading 1 from it or clear the CAE bit for each channel for which it is set. Clearing the AE bit clears the channel address error bits for all channels. 0: A SYS-DMAC address error interrupt is not present. [Clearing condition] Writing CAE = 0 after reading CAE = 1 1: A SYS-DMAC address error interrupt being generated during DMA transfer.
1	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

---

Bit	Bit Name	Initial Value	R/W	Descriptions
0	DME	0	R/W	<p>DMA Master Enable</p> <p>Enables or disables DMA transfer on all channels. If the DME bit and the DE bit in DMACHCR are both set to 1, DMA transfer is enabled. At this time all AE bits in DMAOR_L must have the value 0. For DMA transfer on a channel to then proceed, the TE bit in DMACHCR for the channel must also have the value 0. Clearing this bit during transfer aborts transfer on all channels.</p> <p>0: Disables DMA transfers on all channels</p> <p>1: Enables DMA transfers on all channels</p>

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### 16.3.6 DMA Operation Register for Higher-Numbered Channels (DMAOR\_U)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

DMAOR\_U is a 16-bit readable/writable register that enables DMA transfer on all higher-numbered channels and specifies the method used to determine the priority levels for all higher-numbered DMA channels. This register also indicates address errors.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	PR[1:0]	—	—	—	—	—	—	AE	—	DME
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R	R	R	R	R	R/(W)*	R	R/W

Bit	Bit Name	Initial Value	R/W	Descriptions
15 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9, 8	PR[1:0]	00	R/W	Priority Mode Select the method for setting the order of priority of channels when transfer requests for multiple channels arrive simultaneously. 00: Fixed CH15 > CH16 > ... > CH28 > CH29 11: Round-robin priority Other than above: Setting prohibited
7 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2	AE	0	R/(W)*	Address Error Flag Indicates that an address error interrupt occurred during DMA transfer. This bit is set under the following conditions: The value set in DMASAR or DMADAR does not fall on a boundary corresponding to the transfer size. The source or destination for transfer is in an invalid space. The source or destination for transfer is in module stop mode. If this bit is set, DMA transfer through the channel is not possible even if the DE bit is set to 1. To clear the AE bit, write 0 to the AE bit after reading 1 from it or clear the CAE bit for each channel for which it is set. Clearing the AE bit clears the channel address error bits for all channels. 0: A SYS-DMAC address error interrupt is not present. [Clearing condition] Writing CAE = 0 after reading CAE = 1 1: A SYS-DMAC address error interrupt being generated during DMA transfer.
1	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

---

Bit	Bit Name	Initial Value	R/W	Descriptions
0	DME	0	R/W	<p>DMA Master Enable</p> <p>Enables or disables DMA transfer on all channels. If the DME bit and the DE bit in DMACHCR are both set to 1, DMA transfer is enabled. At this time all AE bits in DMAOR_U must have the value 0. For DMA transfer on a channel to then proceed, the TE bit in DMACHCR for the channel must also have the value 0. Clearing this bit during transfer aborts transfer on all channels.</p> <p>0: Disables DMA transfers on all channels</p> <p>1: Enables DMA transfers on all channels</p>

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### 16.3.7 DMA Channel Clear Register for Lower-Numbered Channels (DMACHCLR\_L)

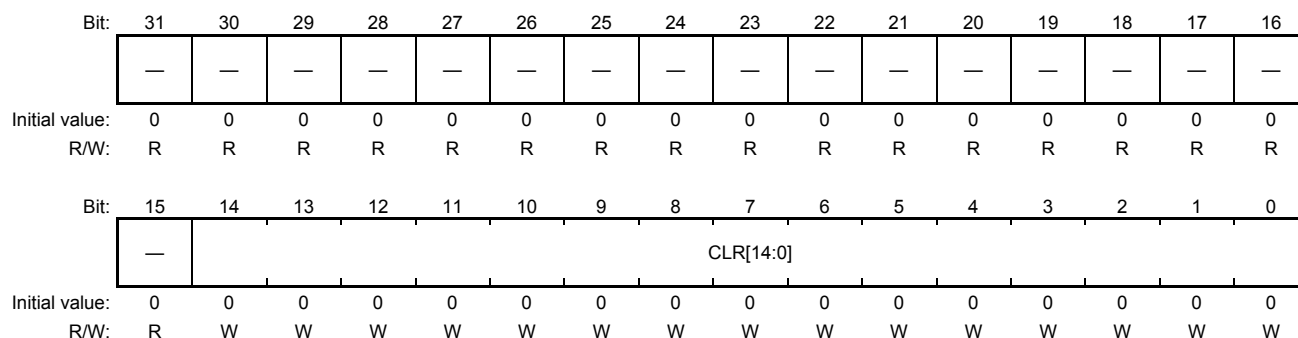
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

DMACHCLR\_L is a 32-bit writable register that initializes each of the lower-numbered channels.

When a bit of this register is set, the state of the corresponding channel is completely initialized.

This includes initialization of the following registers.

DMASAR, DMADAR, DMATCR, DMATSR, DMACHCR, DMATCRB, DMATSRB, DMACHCRB, DMARS, DMABUFCR, DMADPBASE, DMADPCR, DMAFIXSAR, DMAFIXDAR, and DMAFIXDPBASE



Bit	Bit Name	Initial Value	R/W	Description
31 to 15	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
14 to 0	CLR[14:0]	All 0	W	Writing to a bit leads to clearing of all registers for the corresponding channel. CLR[0] 0: Ignored 1: All registers for channel 0 are cleared. CLR[1] 0: Ignored 1: All registers for channel 1 are cleared. CLR[2] 0: Ignored 1: All registers for channel 2 are cleared. ... CLR[14] 0: Ignored 1: All registers for channel 14 are cleared. When writing to this register, confirm that the DE bit is set to 0.

### 16.3.8 DMA Channel Clear Register for Higher-Numbered Channels (DMACHCLR\_U)

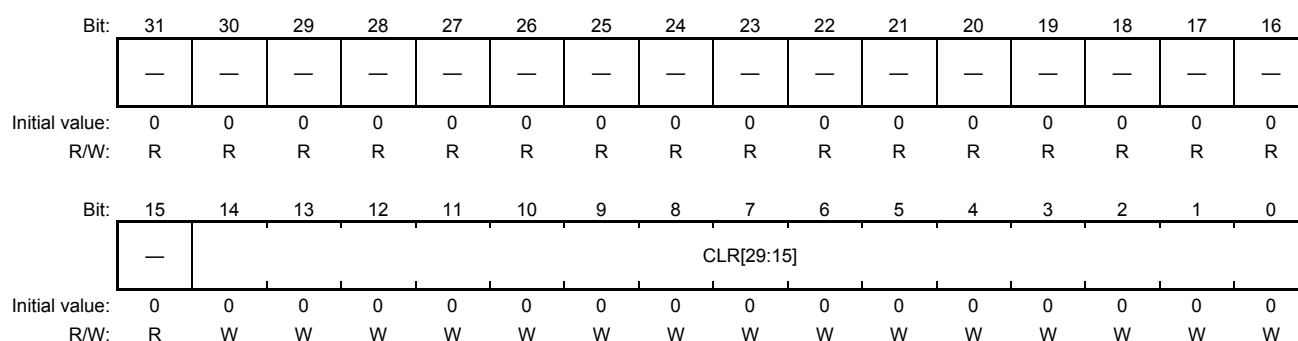
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

DMACHCLR\_U is a 32-bit writable register that initializes each of the higher-numbered channels.

When a bit of this register is set, the state of the corresponding channel is completely initialized.

This includes initialization of the following registers.

DMASAR, DMADAR, DMATCR, DMATSR, DMACHCR, DMATCRB, DMATSRB, DMACHCRB, DMARS, DMABUFGR, DMADPBASE, DMADPCR, DMAFIXSAR, DMAFIXDAR, and DMAFIXDPBASE



Bit	Bit Name	Initial Value	R/W	Description
31 to 15	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
14 to 0	CLR[29:15]	All 0	W	Writing to a bit leads to clearing of all registers for the corresponding channel. CLR[15] 0: Ignored 1: All registers for channel 15 are cleared. CLR[16] 0: Ignored 1: All registers for channel 16 are cleared. ... CLR[29] 0: Ignored 1: All registers for channel 29 are cleared. When writing to this register, confirm that the DE bit is set to 0.

### 16.3.9 DPRAM Secure Control Register for Lower-Numbered Channels (DMADPSEC\_L)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

DMADPSEC\_L is a 32-bit readable/writable register that controls the security attribute of the descriptor memory. Only the initiator in the secure mode can change the setting of this register.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16			
	SEC	—	—	—	—	—	—	SA[8:0]											
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
R/W:	R/W	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
	—	—	—	—	—	—	—	SM[8:0]											
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
R/W:	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			

Bit	Bit Name	Initial Value	R/W	Description
31	SEC	0	R/W	Security Attribute Setting for Descriptor Memory Specifies the security attribute of the address space used for the descriptor memory. 0: Non-secure 1: Secure
30 to 25	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
24 to 16	SA[8:0]	H'000	R/W	Security Attribute Setting for Base Address of Descriptor Memory Specify the base address of the descriptor memory to be assigned the security attribute. H'000: H'A000 H'001: H'A004 ... H'1FF: H'A7FC
15 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8 to 0	SM[8:0]	H'000	R/W	Security Attribute Setting for Base Address Mask of Descriptor Memory Specify the security attribute base address mask of the descriptor memory. The range of memory to be assigned the security attribute is specified by this register. See Figure 16.4.

### 16.3.10 DPRAM Secure Control Register for Higher-Numbered Channels (DMADPSEC\_U)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

DMADPSEC\_U is a 32-bit readable/writeable register that controls the security attribute of the descriptor memory. Only the initiator in the secure mode can change the setting of this register.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16			
	SEC	—	—	—	—	—	—	SA[8:0]											
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
R/W:	R/W	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
	—	—	—	—	—	—	—	SM[8:0]											
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
R/W:	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			

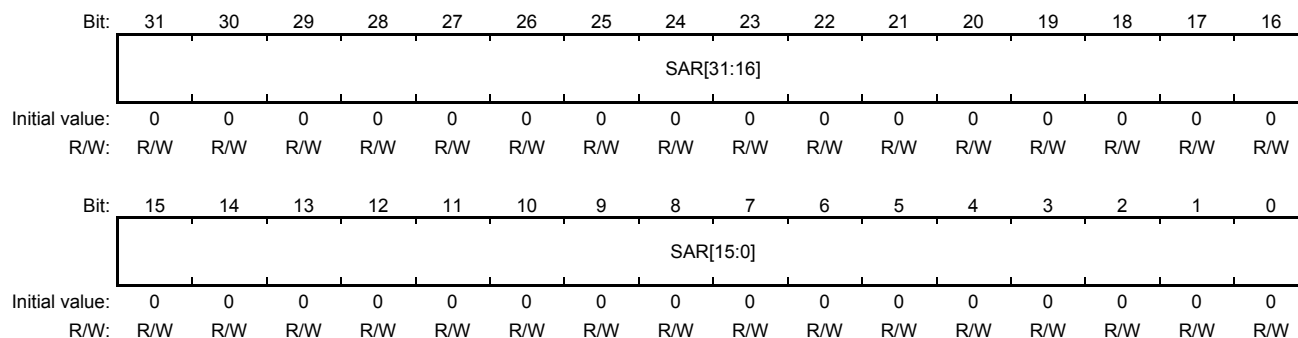
Bit	Bit Name	Initial Value	R/W	Description
31	SEC	0	R/W	Security Attribute Setting for Descriptor Memory Specifies the security attribute of the address space used for the descriptor memory. 0: Non-secure 1: Secure
30 to 25	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
24 to 16	SA[8:0]	H'000	R/W	Security Attribute Setting for Base Address of Descriptor Memory Specify the base address of the descriptor memory to be assigned the security attribute. H'000: H'A000 H'001: H'A004 ... H'1FF: H'A7FC
15 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8 to 0	SM[8:0]	H'000	R/W	Security Attribute Setting for Base Address Mask of Descriptor Memory Specify the security attribute base address mask of the descriptor memory. The range of memory to be assigned the security attribute is specified by this register. See Figure 16.4.

**16.3.11 DMA Source Address Registers 0 to 29 (DMASAR\_0 to DMASAR\_29)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

DMASAR is a 32-bit readable/writable register that specifies the source address of a DMA transfer. While a DMA transfer is in progress, this register indicates the next source address.

When the address mode is incrementation, sources in memory only have byte boundaries. For details, refer to Table 16.3.

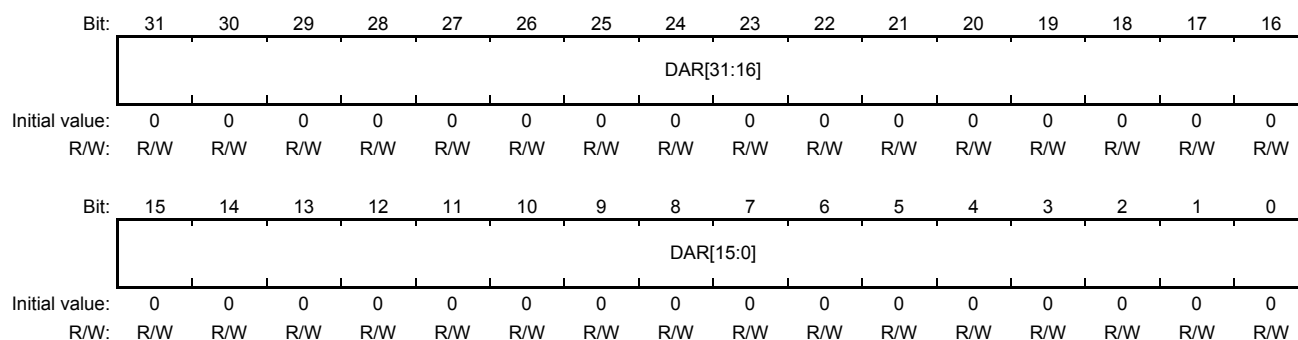


**16.3.12 DMA Destination Address Registers 0 to 29 (DMADAR\_0 to DMADAR\_29)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

DMADAR is 32-bit readable/writable register that specify the destination address of a DMA transfer. While a DMA transfer is in progress, this register indicates the next destination address.

When the address mode is incrementation, destinations in memory only have byte boundaries. For details, refer to Table 16.3.



**Table 16.3 SAR/DAR Address Restriction**

Resource Selection	Address Mode	Restriction
Auto request	Incrementation	No restriction (byte boundaries)
	Others	Boundary corresponding to the DMA transfer size
On-chip peripheral module request Transmission/DAR, Reception/SAR	All	Boundary corresponding to the DMA transfer size
On-chip peripheral module request Transmission/SAR, Reception/DAR	Incrementation	No restriction (byte boundaries)
	Others	Boundary corresponding to the DMA transfer size

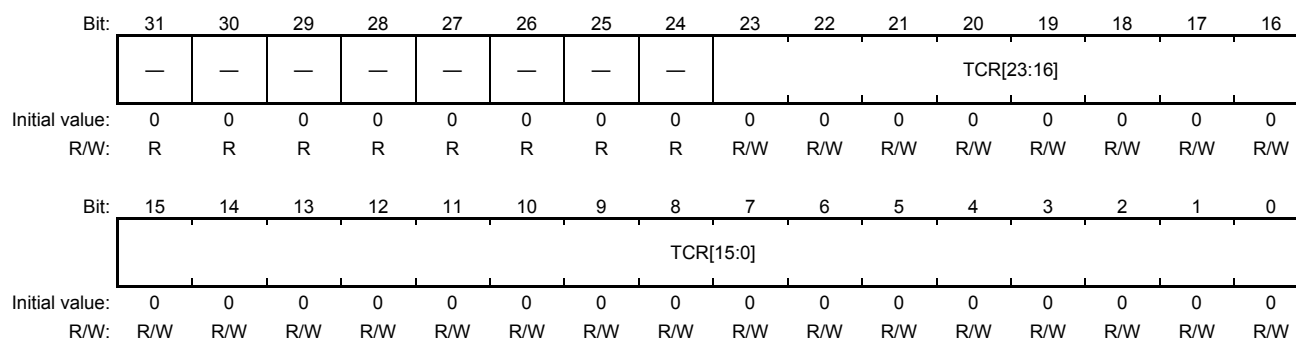
**16.3.13 DMA Transfer Count Registers 0 to 29 (DMATCR\_0 to DMATCR\_29)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

DMATCR is a 32-bit readable/writable register that specifies the number of rounds of DMA transfer. The number of rounds of DMA transfer is 1 when the setting is H'00000001, 16,777,215 when the setting is H'00FFFFFF, and 16,777,216 (the maximum) when the setting is H'00000000. During a DMA transfer, this register indicates the remaining number of rounds of transfer.

The SYS-DMAC includes independent data buffers for reading and writing. Therefore, the read transfer counter and write transfer counter have different values. This register indicates the counter value used in reading.

The eight higher-order bits of DMATCR are always read as 0, and the write value should always be 0.



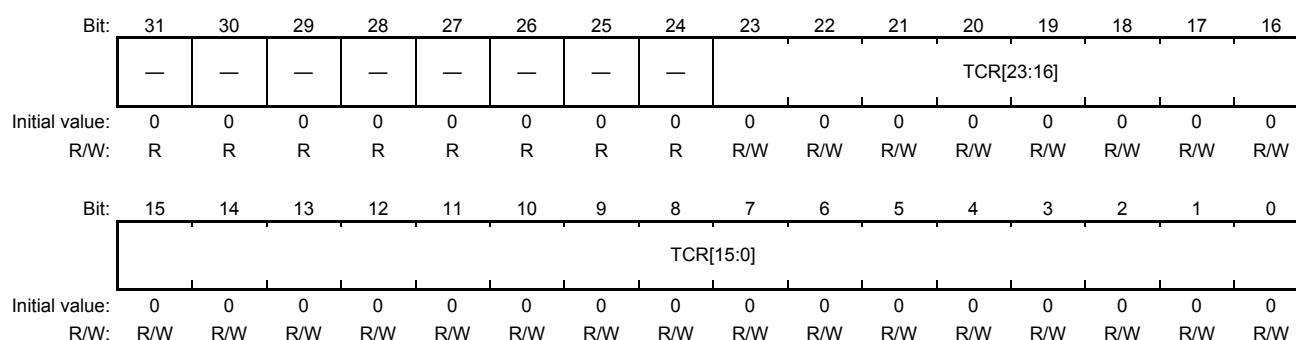
### 16.3.14 DMA Transfer Count Registers B\_0 to 29 (DMATCRB\_0 to DMATCRB\_29)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

DMATCRB is a 32-bit readable/writable register that specifies the number of rounds of DMA transfer. The number of rounds of DMA transfer is 1 when the setting is H'00000001, 16,777,215 when the setting is H'00FFFFFF, and 16,777,216 (the maximum) when the setting is H'00000000. During a DMA transfer, this register indicates the remaining number of rounds of transfer.

The SYS-DMAC includes independent data buffers for reading and writing. Therefore, the read transfer counter and write transfer counter have different values. This register indicates the counter value used in writing.

The eight higher-order bits of DMATCRB are always read as 0, and the write value should always be 0.

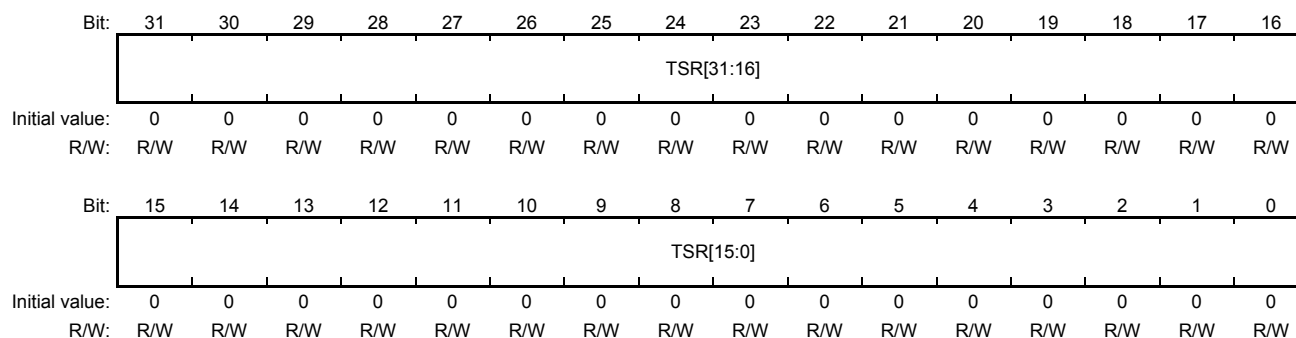


### 16.3.15 DMA Transfer Size Registers 0 to 29 (DMATSR\_0 to DMATSR\_29)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

DMATSR is a 32-bit readable/writable register that specifies a total amount of memory to be transferred. The total size of DMA transfer is 1 byte when the setting is H'00000001, 4,294,967,295 bytes when the setting is H'FFFFFFF, and 4,294,967,296 bytes (the maximum) when the setting is H'00000000. During a DMA transfer, this register indicates the remaining amount of memory to be transferred. This register is used in total size transmission.

The SYS-DMAC includes independent data buffers for reading and writing. Therefore, reading and writing will have different transfer sizes. This register indicates the value of the read transfer size.

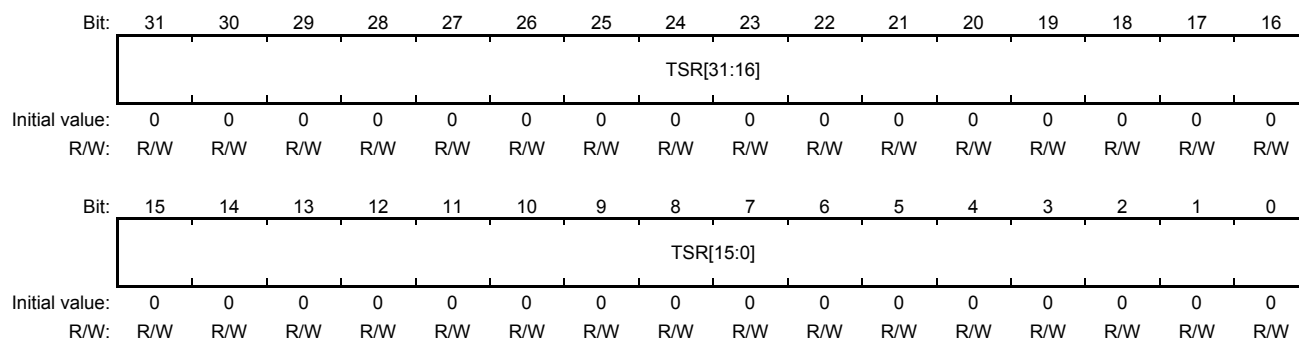


**16.3.16 DMA Transfer Size Registers B\_0 to 29 (DMATSRB\_0 to DMATSRB\_29)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

DMATSRB is a 32-bit readable/writable register that specifies a total amount of memory to be transferred. The total size of DMA transfer is 1 byte when the setting is H'00000001, 4,294,967,295 bytes when the setting is H'FFFFFFFF, and 4,294,967,296 bytes (the maximum) when the setting is H'00000000. During a DMA transfer, this register indicates the remaining amount of memory to be transferred. This register is used in total size transmission.

The SYS-DMAC includes independent data buffers for reading and writing. Therefore, reading and writing will have different transfer sizes. This register indicates the value of the write transfer size.





### 16.3.17 DMA Channel Control Registers 0 to 29 (DMACHCR\_0 to DMACHCR\_29)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

DMACHCR is a 32-bit readable/writable register that controls the DMA transfer mode.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CAE	CAIE	DPM[1:0]		RPT[2:0]		—	—	DPB	TS[3:2]		DSE	DSIE	—	—	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/(W)*	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/(W)*	R/W	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DM[1:0]		SM[1:0]		RS[3:0]			—	—	—	TS[1:0]		IE	TE	DE	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R/W	R/W	R/W	R/(W)*	R/W

Bit	Bit Name	Initial Value	R/W	Descriptions
31	CAE	0	R/(W)*	<p>Channel Address Error Flag</p> <p>Indicates that an address error interrupt occurred during DMA transfer.</p> <p>This bit is set under the following conditions:</p> <ul style="list-style-type: none"> <li>The value set in DMASAR or DMADAR does not fall on a boundary corresponding to the transfer size.</li> <li>The source or destination for transfer is in an invalid space.</li> <li>The source or destination for transfer is in module stop mode.</li> </ul> <p>If this bit is set, DMA transfer through the channel is not possible even if the DE bit is set to 1.</p> <p>To clear the CAE bit, write 0 to the CAE bit after reading 1 from it or clear the AE bit in DMAOR.</p> <p>Clearing the CAE bit clears the channel address error bits for all channels.</p> <p>0: A SYS-DMAC address error interrupt is not present.</p> <p>[Clearing condition]</p> <p>Writing CAE = 0 after reading CAE = 1</p> <p>1: A SYS-DMAC address error interrupt being generated during DMA transfer.</p>
30	CAIE	0	R/W	<p>Channel Address Error Interrupt Enable</p> <p>Enables or disables the generation of interrupt requests for the CPU when address errors occur. When the CAIE bit is set to 1, if the CAE bit is also set, an interrupt (DEI 0 to 29) from the corresponding channel will be generated for the CPU in response to address errors.</p> <p>Note: An address error interrupt (DADERR) is also asserted simultaneously. See section 11, Interrupt Controller for AP-System Core (INTC-SYS) for more details.</p> <p>0: Interrupt requests are disabled.</p> <p>1: Interrupt requests are enabled.</p>

Bit	Bit Name	Initial Value	R/W	Descriptions
29, 28	DPM[1:0]	00	R/W	<p>Operating Mode of Descriptor Memory</p> <p>Enable or disable the descriptor memory and specify its operating mode.</p> <p>00: Disabled (normal use)</p> <p>01: Enabled (normal mode)</p> <p>10: Enabled (repeat mode)</p> <p>11: Enabled (read-out interrupt mode, infinite repeat mode)</p>
27 to 25	RPT[2:0]	000	R/W	<p>Descriptor Setting Update</p> <p>Specify the parameters to be updated from the descriptor memory.</p> <p>RPT[2]: Enables or disables updating of the source address register</p> <p>RPT[1]: Enables or disables updating of the destination address register</p> <p>RPT[0]: Enables or disables updating of the transfer count register</p> <p>0: Disabled</p> <p>1: Enabled</p>
24, 23	—	All 0	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>
22	DPB	0	R/W	<p>Descriptor Start</p> <p>Specifies configuration to be loaded when transfer under control of the descriptor memory begins.</p> <p>This bit is cleared after the descriptor memory is read.</p> <p>0: Processing starts with the values in DMASAR, DMADAR, and DMATCR.</p> <p>1: Processing starts after the first set of descriptors is read out.</p>
21, 20	TS[3:2]	00	R/W	<p>DMA Transfer Size</p> <p>In combination with TS[1:0], these bits specify the DMA transfer size. When the transfer source or transfer destination is a register of an on-chip peripheral module for which a transfer size is specified, be sure to select the specified transfer size. For the transfer source or destination address specified by DMASAR or DMADAR, an appropriate boundary address should be set according to the transfer data size.</p> <p>TS[3:2] + TS[1:0] (“+” here indicates concatenation, not addition)</p> <p>0000: Transfer is in byte units.</p> <p>0001: Transfer is in word (2-byte) units.</p> <p>0010: Transfer is in longword (4-byte) units.</p> <p>0011: Transfer is in 16-byte units.</p> <p>0100: Transfer is in 32-byte units.</p> <p>0101: Transfer is in 64-byte units.</p> <p>0111: Transfer is in 8-byte units.</p> <p>Other than above: Setting prohibited</p> <p>Note: Transfer size must be specified to satisfy both source and destination access sizes.</p>

Bit	Bit Name	Initial Value	R/W	Descriptions
19	DSE	0	R/(W)*	<p>Descriptor Stage End</p> <p>When the DSIE bit is set to 1 and the descriptor memory is enabled, the DSE bit is set to 1 on completion of the DMA transfer. This bit is not set when the DPM bit is set to 0 (descriptors are disabled). To clear the DSE bit, start by reading it as 1, and then write 0 to the bit.</p> <p>0: DMA transfer is still running or has been aborted. 1: Transfer under the control of one stage of the descriptor memory has been completed.</p>
18	DSIE	0	R/W	<p>Descriptor Stage End Interrupt Enable</p> <p>Specifies whether an interrupt request is generated for the CPU on completion of transfer under the control of one stage of the descriptor memory. When this bit is set to 1, an interrupt (DEI) is generated for the CPU whenever the DSE is set to 1.</p> <p>0: Interrupt requests are disabled. 1: Interrupt requests are enabled.</p>
17, 16	—	All 0	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>
15, 14	DM[1:0]	00	R/W	<p>Destination Address Mode</p> <p>Specify whether the DMA destination address is incremented, fixed, or decremented. The unit of transfer (transfer size) determines the size of the increment.</p> <p>00: Destination address is fixed. 01: Destination addresses are incremented.</p> <ul style="list-style-type: none"> <li>+ 1 when transfer is in byte units.</li> <li>+ 2 when transfer is in word units.</li> <li>+ 4 when transfer is in longword units.</li> <li>+ 8 when transfer is in 8-byte units.</li> <li>+ 16 when transfer is in 16-byte units.</li> <li>+ 32 when transfer is in 32-byte units.</li> <li>+ 64 when transfer is in 64-byte units.</li> </ul> <p>10: Destination addresses are decremented.</p> <ul style="list-style-type: none"> <li>– 1 when transfer is in byte units.</li> <li>– 2 when transfer is in word units.</li> <li>– 4 when transfer is in longword units.</li> </ul> <p>Setting prohibited when transfer is in 8-, 16-, 32-, or 64-byte units.</p> <p>11: Setting Prohibited</p>

Bit	Bit Name	Initial Value	R/W	Descriptions
13, 12	SM[1:0]	00	R/W	<p>Source Address Mode</p> <p>Specify whether the DMA source address is incremented, fixed, or decremented. The unit of transfer (transfer size) determines the size of the increment.</p> <p>00: Source address is fixed.</p> <p>01: Source addresses are incremented.</p> <ul style="list-style-type: none"> <li>+ 1 when transfer is in byte units.</li> <li>+ 2 when transfer is in word units.</li> <li>+ 4 when transfer is in longword units.</li> <li>+ 8 when transfer is in 8-byte units.</li> <li>+ 16 when transfer is in 16-byte units.</li> <li>+ 32 when transfer is in 32-byte units.</li> <li>+ 64 when transfer is in 64-byte units.</li> </ul> <p>10: Source addresses are decremented.</p> <ul style="list-style-type: none"> <li>– 1 when transfer is in byte units.</li> <li>– 2 when transfer is in word units.</li> <li>– 4 when transfer is in longword units.</li> </ul> <p>Setting prohibited when transfer is in 8-, 16-, 32-, or 64-byte units.</p> <p>11: Setting Prohibited</p>
11 to 8	RS[3:0]	0000	R/W	<p>Resource Selection</p> <p>Specify the source of transfer requests. Only change the transfer request source while the DMA enable bit (DE) is set to 0.</p> <p>0100: Auto request</p> <p>1000: Source is selected by the DMA extended resource selector.</p> <p>Other than above: Settings prohibited</p>
7 to 5	—	All 0	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>
4, 3	TS[1:0]	00	R/W	<p>DMA Transfer Size</p> <p>See the description of TS[3:2] (bits 21 and 20).</p>
2	IE	0	R/W	<p>Interrupt Enable</p> <p>Specifies whether or not an interrupt request is generated for the CPU on completion of DMA transfer. When this bit is set to 1, an interrupt request (DEI) for the CPU is generated whenever the TE bit is set to 1.</p> <p>0: Interrupt request is disabled.</p> <p>1: Interrupt request is enabled.</p>

Bit	Bit Name	Initial Value	R/W	Descriptions
1	TE	0	R/(W)*	<p>Transfer End Flag</p> <p>When the descriptor memory is not in use, the TE bit is set to 1 when DMATCR becomes 0 on completion of the DMA transfer.</p> <p>When the descriptor memory is in use, the TE bit is set to 1 on completion of all transfers set up in the descriptor memory. The TE bit is not set to 1 in the following cases.</p> <ul style="list-style-type: none"> <li>• DMA transfer ends due to a DMA address error before DMATCR becomes 0.</li> <li>• DMA transfer is aborted by clearing the DE and DME bits in DMAOR.</li> </ul> <p>To clear the TE bit, start by reading it as 1, and then write 0 to it.</p> <p>When the TE bit is set to 1, transfer is not possible even if the DE bit is set to 1.</p> <p>0: DMA transfer is in progress or was aborted [Clearing condition] Writing of 0 after reading of 1</p> <p>1: DMA transfer ended on the specified count (TCR = 0)</p>
0	DE	0	R/W	<p>DMA Enable</p> <p>Enables or disables DMA transfer. In the auto request mode, a DMA transfer is started by setting the DE and DME bits in DMAOR to 1. At this time, the setting of both the AE and TE bits in DMAOR must be 0. In a peripheral module request, a DMA transfer starts if the transfer request is generated by the selected device or on-chip peripheral module after setting the DE and DME bits to 1. In this case too, the settings of both the TE and AE bits must be 0. Clearing the DE bit to 0 aborts all DMA transfer.</p> <p>Note: Ensure that the setting of the DE bit is actually 0 after clearing it.</p> <p>0: DMA transfer is disabled. 1: DMA transfer is enabled.</p>

Note: \* Writing 0 is possible to clear the flag.

**16.3.18 DMA Channel Control Register B\_0 to 29 (DMACHCRB\_0 to DMACHCRB\_29)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

DMACHCRB is a 32-bit readable/writable register that controls the DMA transfer mode.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DCNT[7:0]								DPTR[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DRST	—	—	—	—	—	—	DTS	SLM[3:0]				PRI[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	W	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 24	DCNT[7:0]	H'00	R/W	Number of Stages of Descriptor Memory Specify the number of stages of the descriptor memory as DCNT + 1. When the descriptor memory is enabled, a transfer end (TE) interrupt is only generated for the CPU on completion of transfer under control of the specified number of stages.
23 to 16	DPTR[7:0]	H'00	R	Descriptor Pointer This bit indicates the pointer to the next descriptor to be read. It is cleared to 0 when the last descriptor of the number of stages specified by DCNT[7:0] is read. It is also cleared to 0 when 1 is written to DRST.
15	DRST	0	W	Descriptor Reset Resets the descriptor pointer. Before the descriptor memory is used, the pointer must be reset by writing 1 to this bit. This bit is always read as 0.
14 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	DTS	0	R/W	Total Size Transmission under Descriptor Control This bit is only effective when total size transmission is selected. 0: The TCR fields of the descriptors are used as transfer count settings. 1: The TCR fields of the descriptors are used as total size settings.

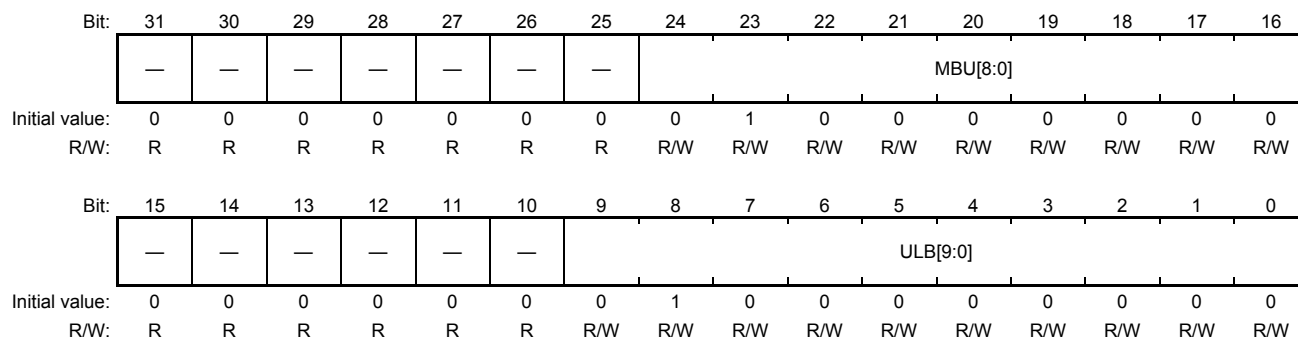
Bit	Bit Name	Initial Value	R/W	Descriptions
7 to 4	SLM[3:0]	0000	R/W	<p>DMA Transfer Low-Speed Mode</p> <p>Specify the number of cycles of the clock (ZS) for the DMA transfer. One round of DMA transfer is executed in the number of cycles of the clock specified by this bit.</p> <p>0000: Normal mode</p> <p>1000: On round in 256 cycles of the clock.</p> <p>1001: On round in 512 cycles of the clock.</p> <p>1010: On round in 1024 cycles of the clock.</p> <p>:</p> <p>1111: On round in 32768 cycles of the clock.</p> <p>Other than above: Setting prohibited</p>
3 to 0	PRI[3:0]	0000	R/W	<p>Channel Request Priority Setting</p> <p>These bits set the priority of requests for transfer on the given channel.</p> <p>1111: Highest priority</p> <p>:</p> <p>0111 to 0000: Lowest priority</p>

**16.3.19 DMA Buffer Control Registers 0 to 29 (DMABUFCR\_0 to DMABUFCR\_29)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

DMABUFCR is a 32-bit readable/writable register that controls the upper limit on buffer size in and burst unit for the SDRAM.

Use this register when the upper limit on buffering requires control.



Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 25	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
24 to 16	MBU[8:0]	H'080	R/W	Maximum Burst Unit for SDRAM This register is only effective for SDRAM access, and everything other than that is under control of the transfer size (unit). Settings bigger than UBL are prohibited. Power-of-two settings are recommended. Maximum value is 256 (bytes).
15 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9 to 0	ULB[9:0]	H'100	R/W	Upper Limit on Buffer Size This register controls the upper limit value for buffering. Power-of-two settings are recommended. Maximum value is 512 (bytes).



**16.3.20 DMA Extended Resource Selectors 0 to 29 (DMARS\_0 to DMARS\_29)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

DMARS is a 16-bit readable/writable register that specifies the on-chip peripheral module to be the source of the DMA transfer request for the given channel. DMARS\_0 specifies the source for channel 0, DMARS\_1 specifies the source for channel 1 and so on.

When bits MID and RID are set to a value other than the values listed in Table 16.4, the operation of this LSI is not guaranteed. Transfer requests from the source selected in DMARS are only valid when the resource selection bits (RS[3:0]) in DMACHCR have been set to B'1000. Otherwise, even if DMARS has been set, requests from the corresponding transfer request source are not accepted.

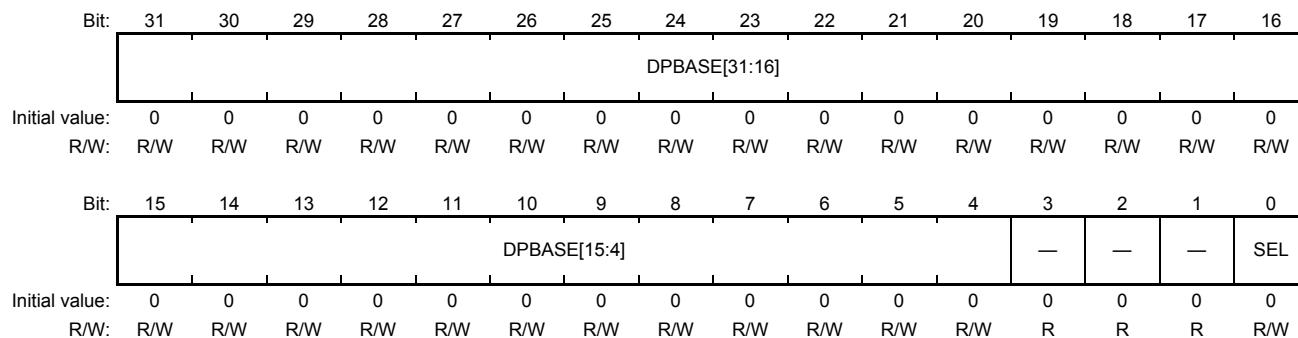
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	MID[5:0]						RID[1:0]	
Initial value:	—	—	—	—	—	—	—	—	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Descriptions
15 to 8	—	—	R	Reserved These bits are always read as an undefined value. The write value should always be 0.
7 to 2	MID[5:0]	000000	R/W	DMA Request Source Adoption ID5 to ID0 (MID) See Table 16.4.
1, 0	RID[1:0]	00	R/W	DMA Request Source Adoption ID1 and ID0 (RID) See Table 16.4.

**16.3.21 DMA Descriptor Base Address Registers 0 to 29 (DMADPBASE\_0 to DMADPBASE\_29)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

DMADPBASE specifies the base address of the descriptor memory. The address range of the descriptor memory is specified by setting this register.

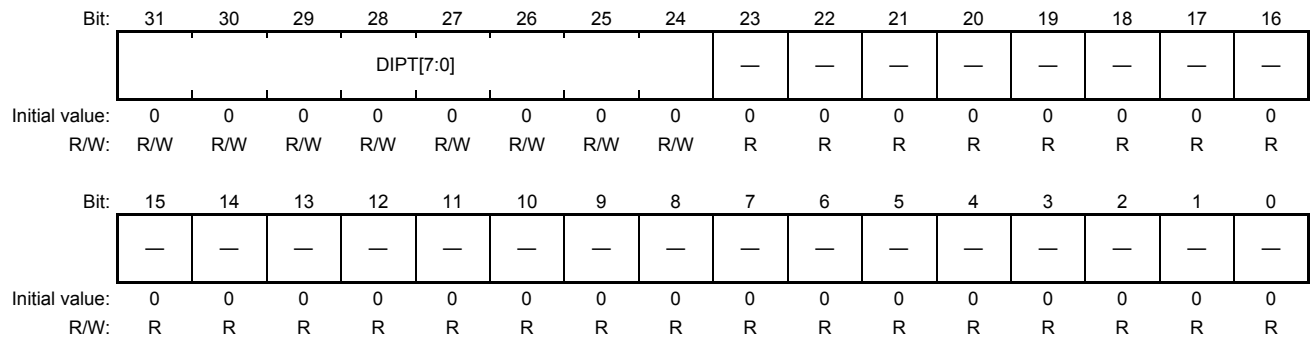


Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 4	DPBASE[31:4]	All 0	R/W	Base Address of Descriptor Memory Place each stage of the descriptor memory on a 16-byte boundary. Setting example When Built-in memory is used, [SYS-DMAC Lower]: H'E670 A000 to H'E670 A7FC [SYS-DMAC Higher]: H'E672 A000 to H'E672 A7FC When External memory is used, Other memory area on a 16-byte boundary
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	SEL	0	R/W	Descriptor Memory Selection Select the memory to be used as descriptor memory. 0: Setting Prohibited 1: Built-in memory or External memory is used.

**16.3.22 DMA Descriptor Control Registers 0 to 29 (DMADPCR\_0 to DMADPCR\_29)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

DMADPCR is a 32-bit readable/writable register that controls the timing with which interrupts are output in read-out interrupt mode (descriptor mode 3).



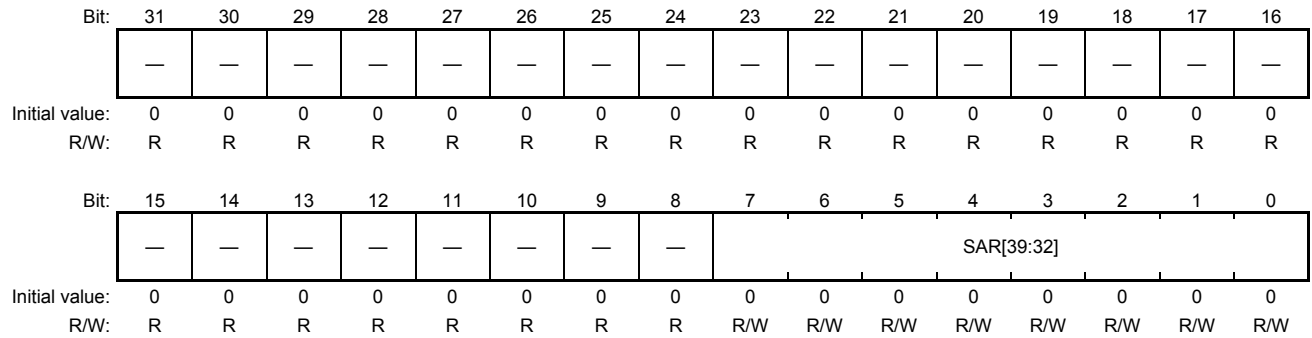
Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 24	DIPT[7:0]	All 0	R/W	Descriptor Read-out Interrupt Pointer The number of stages for which descriptor read-out interrupts are generated in descriptor mode 3. DIPT + 1 specifies the number of descriptor stages.
23 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

**16.3.23 DMA Fixed Source Address Registers 0 to 29 (DMAFIXSAR\_0 to DMAFIXSAR\_29)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

DMAFIXSAR is a 32-bit readable/writable register that specifies the most significant 8 bits of the 40-bit source address for a DMA transfer.

This register is not incremented by carrying when DMASAR overflows.

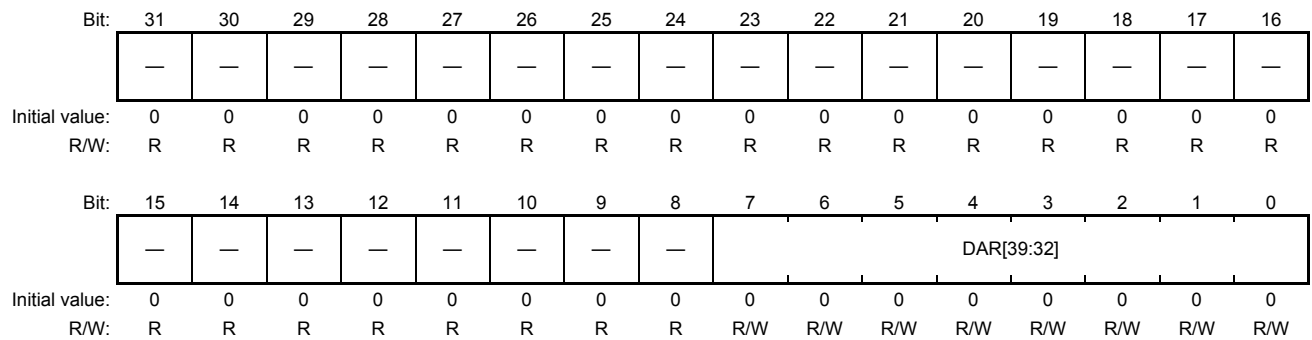


**16.3.24 DMA Fixed Destination Address Registers 0 to 29 (DMAFIXDAR\_0 to DMAFIXDAR\_29)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

DMAFIXDAR is a 32-bit readable/writable register that specifies the most significant 8 bits of the 40-bit destination address for a DMA transfer.

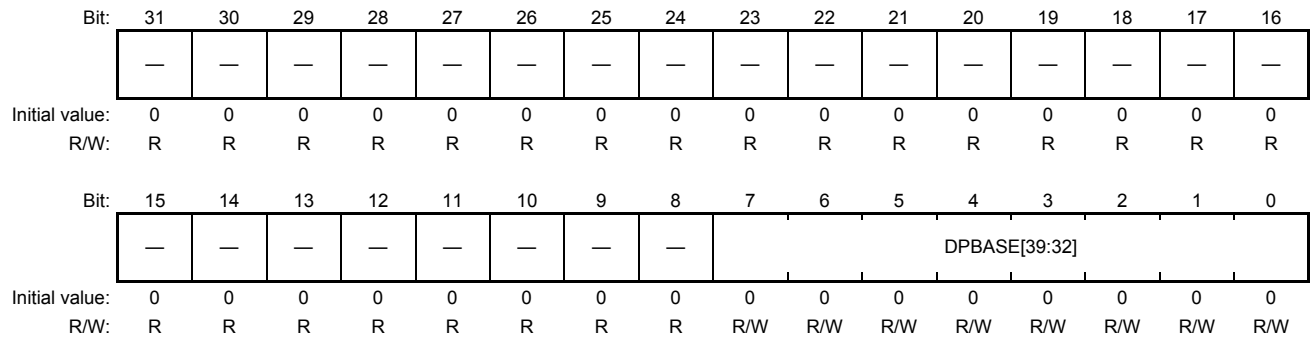
This register is not incremented by carrying when DMASAR overflows.



**16.3.25 DMA Fixed Descriptor Base Address Registers 0 to 29 (DMAFIXDPBASE\_0 to DMAFIXDPBASE\_29)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

DMAFIXDPBASE is a 32-bit readable/writable register that specifies the most significant 8 bits of the 40-bit descriptor base address for a DMA transfer.



**16.3.26 Descriptor Memory (DescriptorMEM)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

See section 16.4.4, Descriptor Memory.

## 16.4 Operation

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

When there is a DMA transfer request, the DMAC starts the transfer according to the predetermined channel priority; when the transfer end conditions are satisfied, it ends the transfer. Transfers can be requested in two modes: auto request and on-chip peripheral module request. The bus mode can be selected from normal speed mode and slow speed mode).

### 16.4.1 DMA Transfer Requests

Most commonly, DMA transfer requests are generated by either the source or destination for transfer, but they can also be generated by on-chip peripheral modules that are neither the source nor the destination. Transfers can be requested in two modes: auto request, and on-chip peripheral module request. The request mode is selected for each channel by DMARS.

#### (1) Auto-Request Mode

When there is no transfer request signal from an external source, as in a memory-to-memory transfer or a transfer between memory and an on-chip peripheral module unable to request a transfer, auto-request mode allows the SYS-DMAC to automatically generate a transfer request signal internally. When the DE bit in DMACHCR and the DME bit in DMAOR are set to 1 for the target channel, the transfer begins so long as the CAE bit in DMACHCR is 0.

#### (2) On-Chip Peripheral Module Request Mode

In this mode, a transfer is performed at the transfer request signal of an on-chip peripheral module. The source (on-chip peripheral module) of the DMA transfer request is specified by DMARS.

When this mode is selected, if the DMA transfer is enabled (DE = 1, DME = 1, TE = 0, CAE = 0), a transfer is performed upon the input of a transfer request signal.

When a transmit data empty transfer request of the SCIF is set as the transfer request, the transfer destination must be the SCIF's transmit data register. Likewise, when receive data full transfer request of the SCIF is set as the transfer request, the transfer source must be the SCIF's receive data register. These conditions also apply to the other on-chip peripheral modules.

The number of the receive FIFO triggers can be set as a transfer request depending on an on-chip peripheral module. Data needs to be read after the DMA transfer is ended, because data may be left in the receive FIFO when the receive FIFO trigger condition is not satisfied.

Table 16.4 Selecting On-Chip Peripheral Module Request Modes

DMARS MID + RID	DMA Transfer Request Source	DMA Transfer Request Signal	Source	Destination	RZ/G Series Products			
					RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
H'21	SCIFA0 transmitter	TXI (Transmit FIFO data empty)	Arbitrary	SCAFTDR0	√	√	√	√
H'22	SCIFA0 receiver	RXI (Receive FIFO data full)	SCAFRDR0	Arbitrary	√	√	√	√
H'25	SCIFA1 transmitter	TXI (Transmit FIFO data empty)	Arbitrary	SCAFTDR1	√	√	√	√
H'26	SCIFA1 receiver	RXI (Receive FIFO data full)	SCAFRDR1	Arbitrary	√	√	√	√
H'27	SCIFA2 transmitter	TXI (Transmit FIFO data empty)	Arbitrary	SCAFTDR2	√	√	√	√
H'28	SCIFA2 receiver	RXI (Receive FIFO data full)	SCAFRDR2	Arbitrary	√	√	√	√
H'1B	SCIFA3 transmitter	TXI (Transmit FIFO data empty)	Arbitrary	SCAFTDR3	—	√	√	√
H'1C	SCIFA3 receiver	RXI (Receive FIFO data full)	SCAFRDR3	Arbitrary	—	√	√	√
H'1F	SCIFA4 transmitter	TXI (Transmit FIFO data empty)	Arbitrary	SCAFTDR4	—	√	√	√
H'20	SCIFA4 receiver	RXI (Receive FIFO data full)	SCAFRDR4	Arbitrary	—	√	√	√
H'23	SCIFA5 transmitter	TXI (Transmit FIFO data empty)	Arbitrary	SCAFTDR5	—	√	√	√
H'24	SCIFA5 receiver	RXI (Receive FIFO data full)	SCAFRDR5	Arbitrary	—	√	√	√
H'3D	SCIFB0 transmitter	TXI (Transmit FIFO data empty)	Arbitrary	SCBFTDR	√	√	√	√
H'3E	SCIFB0 receiver	RXI (Receive FIFO data full)	SCBFRDR	Arbitrary	√	√	√	√
H'19	SCIFB1 transmitter	TXI (Transmit FIFO data empty)	Arbitrary	SCBFTDR	√	√	√	√
H'1A	SCIFB1 receiver	RXI (Receive FIFO data full)	SCBFRDR	Arbitrary	√	√	√	√
H'1D	SCIFB2 transmitter	TXI (Transmit FIFO data empty)	Arbitrary	SCBFTDR	√	√	√	√
H'1E	SCIFB2 receiver	RXI (Receive FIFO data full)	SCBFRDR	Arbitrary	√	√	√	√
H'39	HSCIF0 transmitter	TXI (Transmit FIFO data empty)	Arbitrary	Data register	√	√	√	√
H'3A	HSCIF0 receiver	RXI (Receive FIFO data full)	Data register	Arbitrary	√	√	√	√
H'4D	HSCIF1 transmitter	TXI (Transmit FIFO data empty)	Arbitrary	Data register	√	√	√	√
H'4E	HSCIF1 receiver	RXI (Receive FIFO data full)	Data register	Arbitrary	√	√	√	√
H'3B	HSCIF2 transmitter	TXI (Transmit FIFO data empty)	Arbitrary	Data register	—	√	√	√
H'3C	HSCIF2 receiver	RXI (Receive FIFO data full)	Data register	Arbitrary	—	√	√	√
H'29	SCIF0 transmitter	TXI (Transmit FIFO data empty)	Arbitrary	Data register	√	√	√	√
H'2A	SCIF0 receiver	RXI (Receive FIFO data full)	Data register	Arbitrary	√	√	√	√
H'2D	SCIF1 transmitter	TXI (Transmit FIFO data empty)	Arbitrary	Data register	√	√	√	√
H'2E	SCIF1 receiver	RXI (Receive FIFO data full)	Data register	Arbitrary	√	√	√	√
H'2B	SCIF2 transmitter	TXI (Transmit FIFO data empty)	Arbitrary	Data register	—	√	√	√
H'2C	SCIF2 receiver	RXI (Receive FIFO data full)	Data register	Arbitrary	—	√	√	√
H'2F	SCIF3 transmitter	TXI (Transmit FIFO data empty)	Arbitrary	Data register	—	√	√	√
H'30	SCIF3 receiver	RXI (Receive FIFO data full)	Data register	Arbitrary	—	√	√	√
H'FB	SCIF4 transmitter	TXI (Transmit FIFO data empty)	Arbitrary	Data register	—	√	√	√
H'FC	SCIF4 receiver	RXI (Receive FIFO data full)	Data register	Arbitrary	—	√	√	√
H'FD	SCIF5 transmitter	TXI (Transmit FIFO data empty)	Arbitrary	Data register	—	√	√	√
H'FE	SCIF5 receiver	RXI (Receive FIFO data full)	Data register	Arbitrary	—	√	√	√
H'51	MSIOF0 transmitter	TXI (Transmit FIFO data empty)	Arbitrary	SITDR	√	√	√	√
H'52	MSIOF0 receiver	RXI (Receive FIFO data full)	SIRDR	Arbitrary	√	√	√	√

						RZ/G Series Products			
DMARS MID + RID	DMA Transfer Request Source	DMA Transfer Request Signal	Source	Destination	RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E	
H'55	MSIOF1 transmitter	TXI (Transmit FIFO data empty)	Arbitrary	SITDR	√	√	√	√	
H'56	MSIOF1 receiver	RXI (Receive FIFO data full)	SIRDR	Arbitrary	√	√	√	√	
H'41	MSIOF2 transmitter	TXI (Transmit FIFO data empty)	Arbitrary	SITDR	√	√	√	√	
H'42	MSIOF2 receiver	RXI (Receive FIFO data full)	SIRDR	Arbitrary	√	√	√	√	
H'45	MSIOF3 transmitter	TXI (Transmit FIFO data empty)	Arbitrary	SITDR	√	—	—	—	
H'46	MSIOF3 receiver	RXI (Receive FIFO data full)	SIRDR	Arbitrary	√	—	—	—	
H'17	QSPI	Transmit	Arbitrary	Data register	√	√	√	√	
H'18		Receive	Data register	Arbitrary	√	√	√	√	
H'61	IIC0	Transmit empty transfer request	Arbitrary	Data register	√	√	√	√	
H'62		Receive full transfer request	Data register	Arbitrary	√	√	√	√	
H'65	IIC1	Transmit empty transfer request	Arbitrary	Data register	√	√	√	√	
H'66		Receive full transfer request	Data register	Arbitrary	√	√	√	√	
H'69	IIC2	Transmit empty transfer request	Arbitrary	Data register	√	—	—	—	
H'6A		Receive full transfer request	Data register	Arbitrary	√	—	—	—	
H'77	IIC3	Transmit empty transfer request	Arbitrary	Data register	√	√	√	—	
H'78		Receive full transfer request	Data register	Arbitrary	√	√	√	—	
H'CD	SDHI0 channel 0	Transmit empty transfer request	Arbitrary	Data register	√	√	√	√	
H'CE	SDHI0 channel 1	Receive full transfer request	Data register	Arbitrary	√	√	√	√	
H'C9	SDHI1 channel 0	Transmit empty transfer request	Arbitrary	Data register	√	—	—	—	
H'CA	SDHI1 channel 1	Receive full transfer request	Data register	Arbitrary	√	—	—	—	
H'C1	SDHI2 channel 0	Transmit empty transfer request	Arbitrary	Data register	√	√	√	√	
H'C2	SDHI2 channel 1	Receive full transfer request	Data register	Arbitrary	√	√	√	√	
H'C5	SDHI2 C2 channel 0	Transmit empty transfer request	Arbitrary	Data register	√	√	√	√	
H'C6	SDHI2 C2 channel 1	Receive full transfer request	Data register	Arbitrary	√	√	√	√	
H'D3	SDHI3 channel 0	Transmit empty transfer request	Arbitrary	Data register	√	√	√	√	
H'D4	SDHI3 channel 1	Receive full transfer request	Data register	Arbitrary	√	√	√	√	
H'DF	SDHI3 C2 channel 0	Transmit empty transfer request	Arbitrary	Data register	√	√	√	√	
H'DE	SDHI3 C2 channel 1	Receive full transfer request	Data register	Arbitrary	√	√	√	√	
H'F1	TPU0	Transmit empty transfer request	Arbitrary	Data register	√	√	√	√	
H'D1	MMCIF0 transmitter	TXI (Transmit data request)	Arbitrary	Data register	√	√	√	√	
H'D2	MMCIF0 receiver	RXI (Receive data request)	Data register	Arbitrary	√	√	√	√	
H'E1	MMCIF1 transmitter	TXI (Transmit data request)	Arbitrary	Data register	√	—	—	—	
H'E2	MMCIF1 receiver	RXI (Receive data request)	Data register	Arbitrary	√	—	—	—	
H'AE	AXSTM	Receive transfer request	Data register	Arbitrary	√	√	√	—	



**Table 16.5 Data Length of DMA Transfer for Each of the On-Chip Peripheral Modules**

Module*	1 Byte	2 Bytes	4 Bytes	8 Bytes	16 Bytes	32 Bytes	RZ/G Series Products			
							RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
SCIFA0/1/2/3/4/5	√						√	√	√	√
SCIFB0/1/2	√						√	√	√	√
HSCIF0/1/2	√						√	√	√	√
SCIF0/1/2/3/4/5	√						√	√	√	√
MSIOF0/1/2/3			√				√	√	√	√
QSPI	√	√	√				√	√	√	√
IIC0/1/2	√						√	√	√	√
IIC3	√						√	√	√	—
SDHI0		√	√		√	√	√	√	√	√
SDHI1		√	√		√	√	√	—	—	—
SDHI2		√	√		√	√	√	√	√	√
SDHI3		√	√		√	√	√	√	√	√
TPU0		√					√	√	√	√
AXISTR			√				√	√	√	√
MMCIF0/1			√				√	√	√	√
AXSTM			√				√	√	√	—

Note: \* For the availability of module channels of each product, refer to Table 16.4.

### 16.4.2 Channel Priority

When the SYS-DMAC receives simultaneous transfer requests on two or more channels, it transfers data according to a predetermined priority. Two modes (fixed mode and round-robin mode) are selected by the PR[1:0] bits in DMAOR.

#### (a) Fixed Mode

In this mode, the priority levels among the channels remain fixed.

CH0 > CH1 > ... > CH13 > CH14, CH15 > CH16 > ... > CH28 > CH29

#### (b) Round-Robin Mode

In round-robin mode, each time data of one transfer unit (byte, word, longword, 8-byte, or 16-byte units) is transferred on one channel, the priority is rotated. The channel on which the transfer was just finished rotates to the bottom of the priority. The priority of round-robin mode is CH0 > CH1 > ... > CH13 > CH14 and CH15 > CH16 > ... > CH28 > CH29 immediately after reset.

### 16.4.3 Slow Speed Mode

In the low-speed mode, a single round of DMA transfer is performed every time the number of clock cycles specified by the SLM bits in DMACHCRB elapse. This mode can be selected per DMA channel. Transfer on other channels can proceed after each round of transfer for a channel in the low-speed mode is completed.

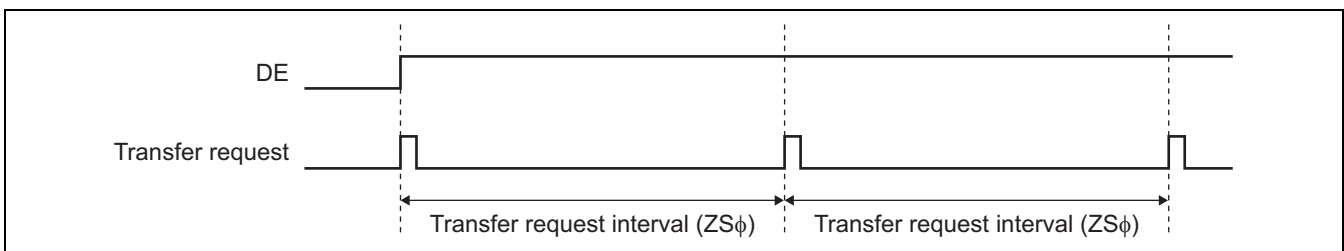


Figure 16.2 Slow Speed Mode

### 16.4.4 Descriptor Memory

The descriptor memory function is selected by setting the DPM[1:0] bits in DMACHCR to B'01, B'10, or B'11. When DMATCR is set to 0 and the DMA transfer is completed, the next set of settings is read, and if only a single channel is enabled, the contents defined by up to 128 stages of descriptor memory can be consecutively transferred when the built-in descriptor memory is used. External memory can also be used as the descriptor memory. In that case, the contents defined by up to 256 stages of descriptor memory can be transferred.

The following initial settings are required to use the descriptor memory.

- Set the base address of the descriptor memory for the DMA transfer in DMADPBASE.
- Set the DRST bit in DMACHCRB to reset the descriptor memory.
- Set the number of stages of the descriptor memory in the DCNT bits of DMACHCRB.

The descriptor memory is shared between all channels. Ensure that the areas of descriptor memory for use by each of the channels do not overlap. It is necessary to arrange each stage of the descriptor memory on a 16-byte boundary.

There are two methods to activate the descriptor memory as follows.

- Specify the first DMA transfer settings in DMASAR, DMADAR, and DMATCR, and specify the subsequent settings in the descriptor memory. Then, set the DPB bit in DMACHCR to 0 to activate the descriptor memory. In this case, after completion of the transfer specified in DMASAR, DMADAR, and DMATCR, transfer continues after new settings are read from the descriptor memory. Note, however, that when the operating mode of the descriptor memory is set to the repeat mode, the values specified in DMASAR, DMADAR, and DMATCR are not read, and the transfer starts and is repeated from the head of the descriptor memory.
- Write the DMA transfer settings to the descriptor memory, and write 1 to the DPB bit in DMACHCR to activate the descriptor memory. In this case, the DMA transfer starts from the first settings in the descriptor memory.

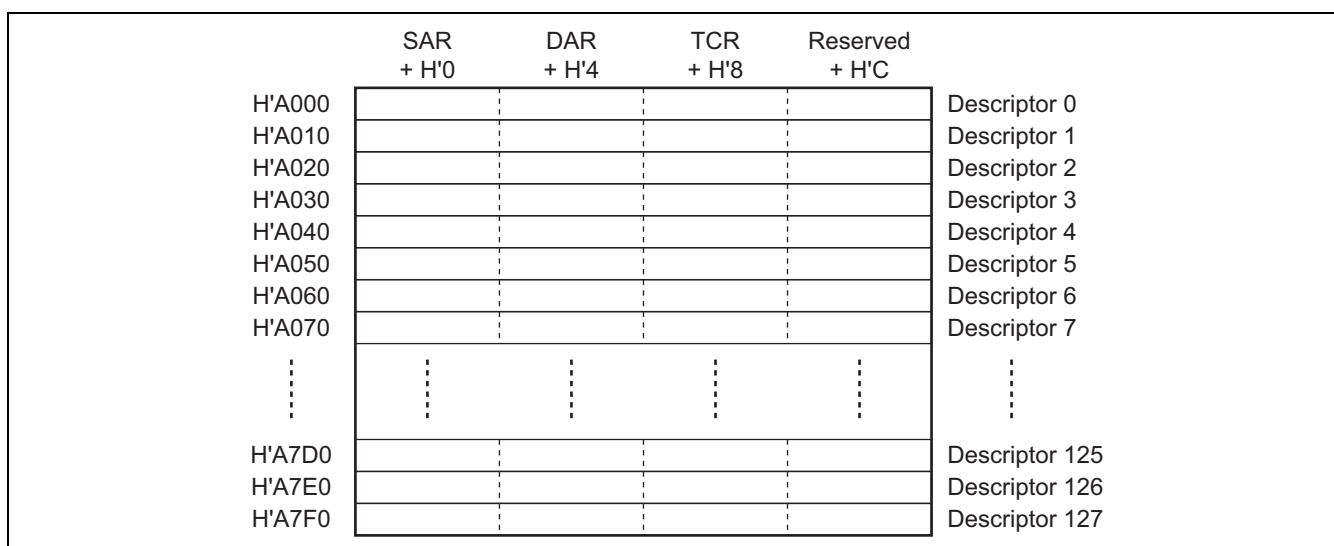
There are three operating modes of the descriptor memory, which can be selected by setting the DPM bits in DMACHCR.

For details on these operating modes, see the descriptions of each operating mode in this section.

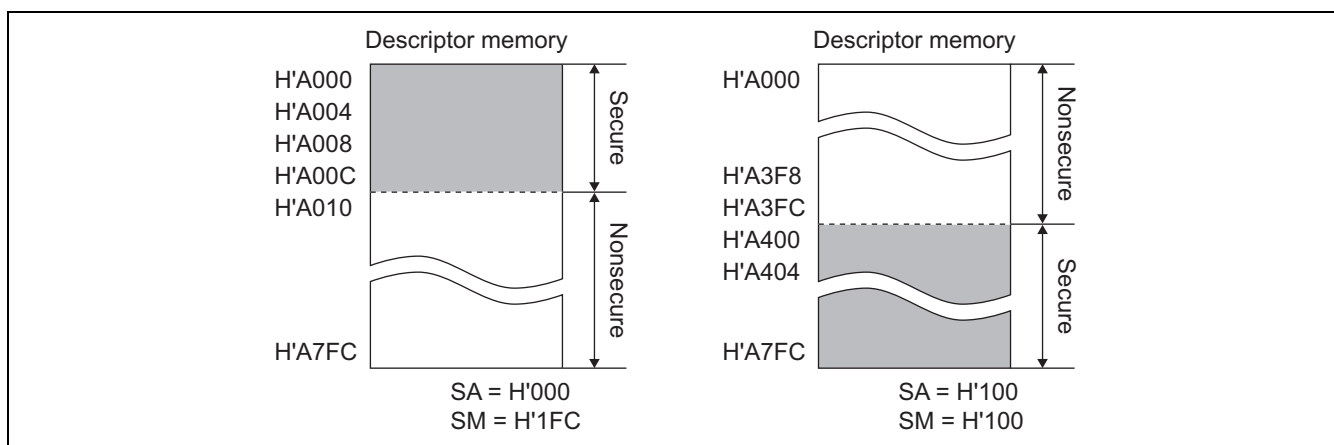
**(1) Configuration of Descriptor Memory**

Figure 16.3 shows the configuration of the built-in descriptor memory.

The capacity of the built-in descriptor memory is 16 bytes per stage × 128 stages.



**Figure 16.3 Configuration of Built-in Descriptor Memory**



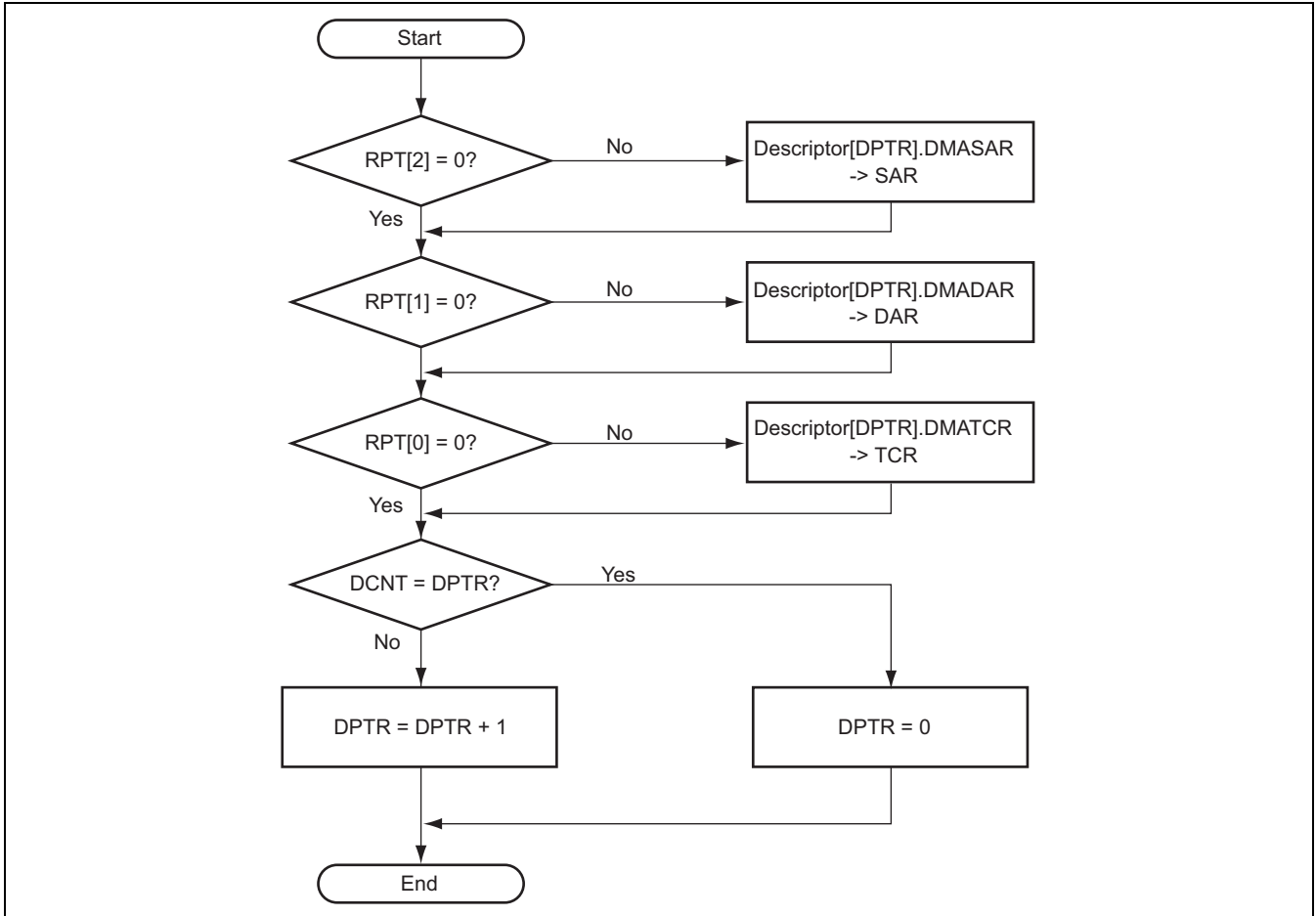
**Figure 16.4 Example of DMADPSEC Setting**

**(2) Flow of Updating from Descriptor Memory**

The RPT bits in DMACHCR can be used to specify which registers are to be updated from the descriptor memory.

The DPTR bits in DMACHCRB are incremented when updating from the descriptor memory is completed. If the DPTR value matches the DCNT value, the DPTR value is reset to 0.

This flow is automatically processed by hardware.



**Figure 16.5 Flow of Updating from Descriptor Memory**

**(3) Operating Mode 1 of Descriptor Memory**

Set the DPM bits in DMACHCR to B'01 to select operating mode 1 (normal mode). This mode allows consecutive transfer under control of the descriptor memory.

In this mode, the DMA transfer is complete when the TE bit in DMACHCR is set to 1 after transfer under control of the number of stages of the descriptor memory specified in the DCNT bits in DMACHCRB.

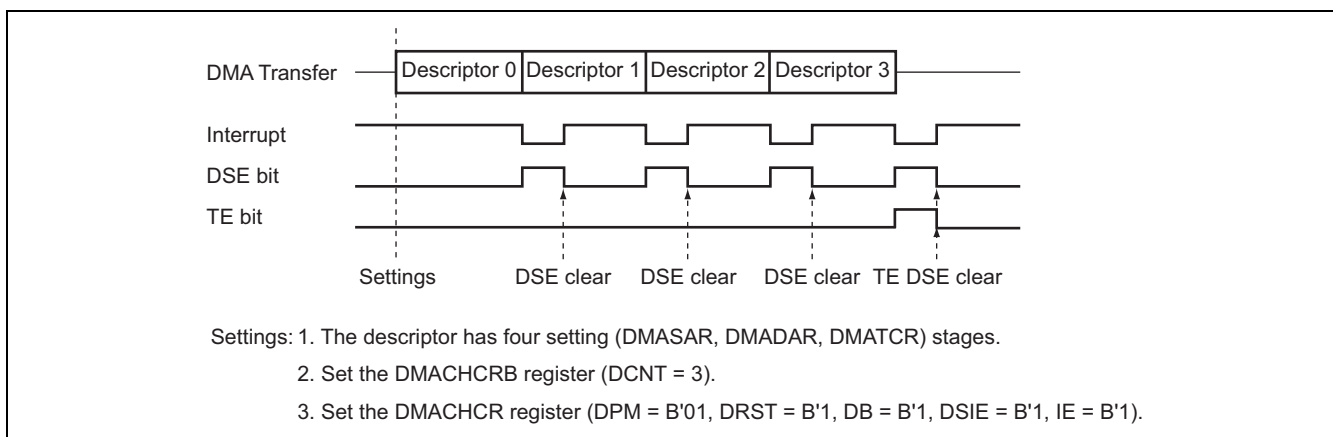
When the DSIE bit in DMACHCR is set to 1, a DSE interrupt is generated every time transfer under the control of one stage of descriptor memory is complete. If a first DSE interrupt has not been processed when a further DSE interrupt is generated, the contents of the next stage of the descriptor memory are not read and the DMA transfer is aborted. Clearing the DSE bit only causes clearing of the first interrupt and reading of the next stage of the descriptor memory.

Figure 16.6 is an example of transfer when operating mode 1 is selected and the TE and DSE bits are set to 1.

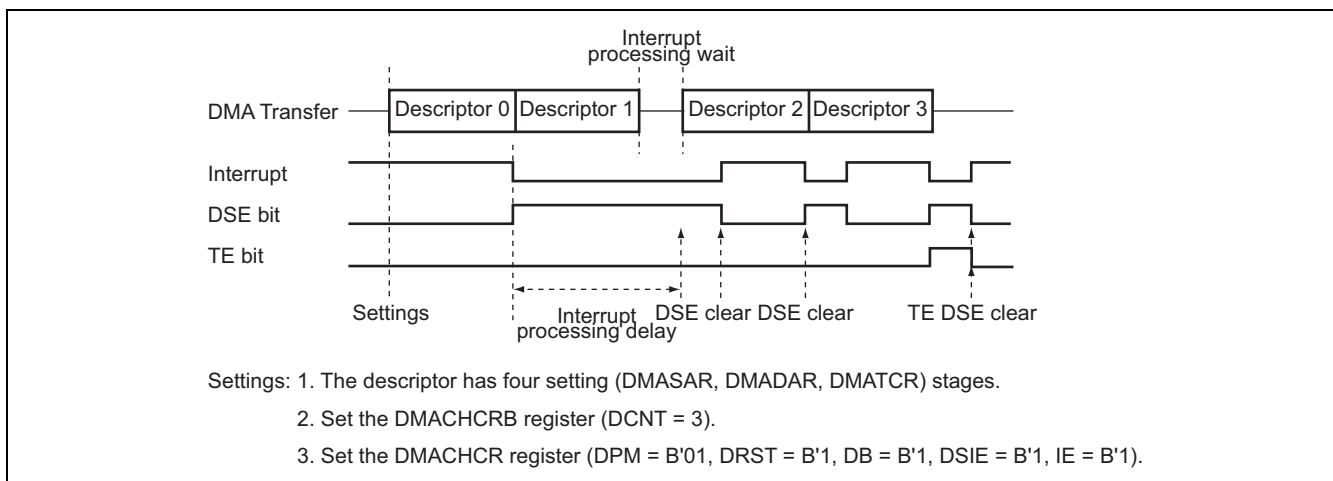
Figure 16.7 is an example of transfer when there is a delay in processing of the DSE interrupt when operating mode 1 is selected and the TE and DSE bits are set to 1.

Figure 16.8 is an example of transfer when operating mode 1 is selected and the TE bit is set to 1.

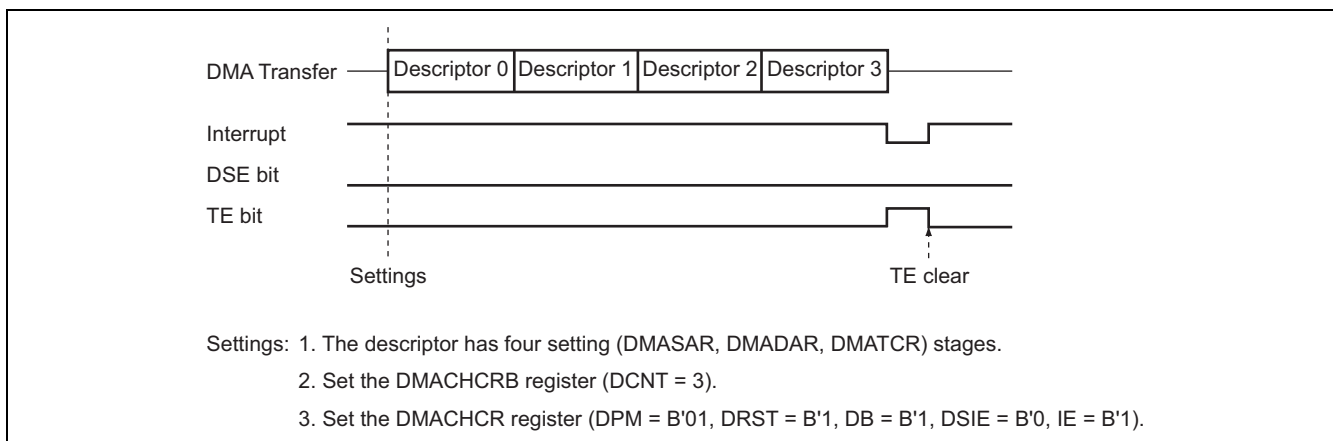
In each example, there are four descriptor stages.



**Figure 16.6 Operating Mode 1 (Example 1)**



**Figure 16.7 Operating Mode 1 (Example 2)**



**Figure 16.8 Operating Mode 1 (Example 3)**

#### (4) Operating Mode 2 of Descriptor Memory

Set the DPM bits in DMACHCR to B'10 to select operating mode 2 (repeat mode). This mode allows consecutive transfer under control of the descriptor memory.

In this mode, after transfer under control of the number of stages of descriptor memory specified in the DCNT bits in DMACHCRB, the TE bit in DMACHCR is set to 1. This operation is then repeated from the head of the descriptor memory.

When the DSIE bit in DMACHCR is set to 1, a DSE interrupt is generated every time transfer under the control of one stage of descriptor memory is complete. If a first DSE interrupt has not been processed when a further DSE interrupt is generated, the contents of the next stage of the descriptor memory are not read and the DMA transfer is aborted. Clearing the DSE bit only causes clearing of the first interrupt and reading of the next stage of the descriptor memory.

When the DSIE bit in DMACHCR is set to 0, after transfer under control of all stages of the descriptor memory is complete, the TE bit in DMACHCR is set to 1 and a TE interrupt is generated. If a TE interrupt has not been processed when a further DSE interrupt is generated, the contents of the next stage of the descriptor memory are not read and the DMA transfer is aborted. Clearing the TE bit only causes clearing of the first interrupt and reading of the next stage of the descriptor memory.

To end operation in mode 2, change the mode to mode 1 by using the TE interrupt processing. When the mode is changed to mode 1, the DMA transfer is completed when the next TE interrupt is generated.

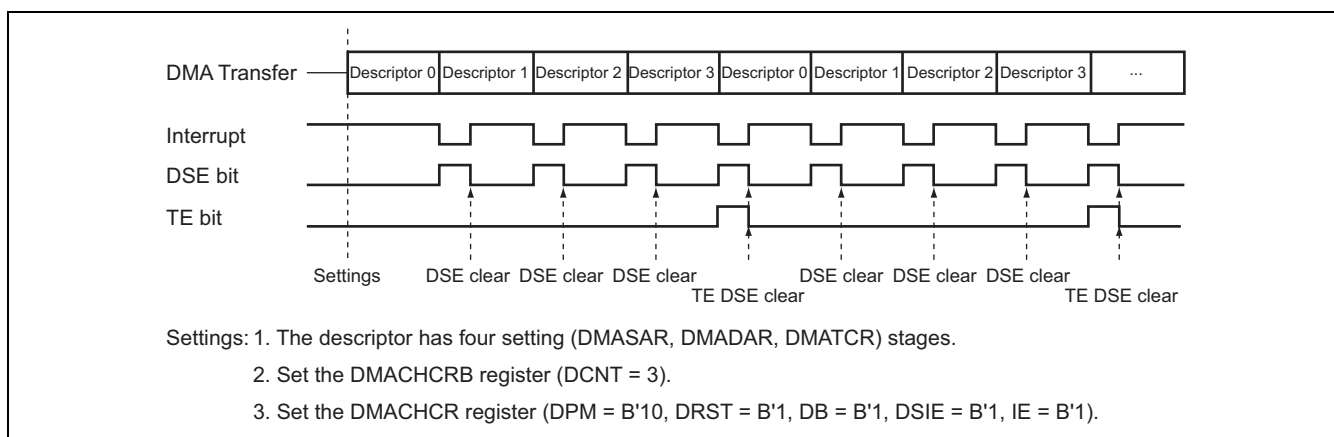
Figure 16.9 is an example of transfer when operating mode 2 is selected and the TE and DSE bits are set to 1.

Figure 16.10 is an example of transfer when there is a delay in processing of the DSE interrupt when operating mode 2 is selected and the TE and DSE bits are set to 1.

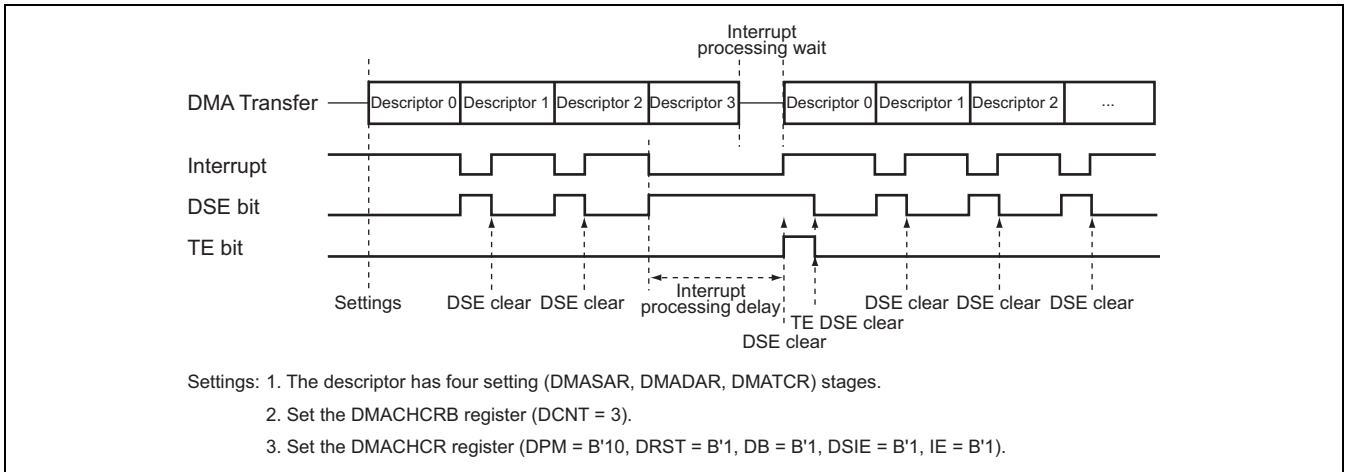
Figure 16.11 is an example of transfer when operating mode 2 is selected and the TE bit is set to 1.

Figure 16.12 is an example of transfer when there is a delay in processing of the DSE interrupt when operating mode 2 is selected and the TE is set to 1.

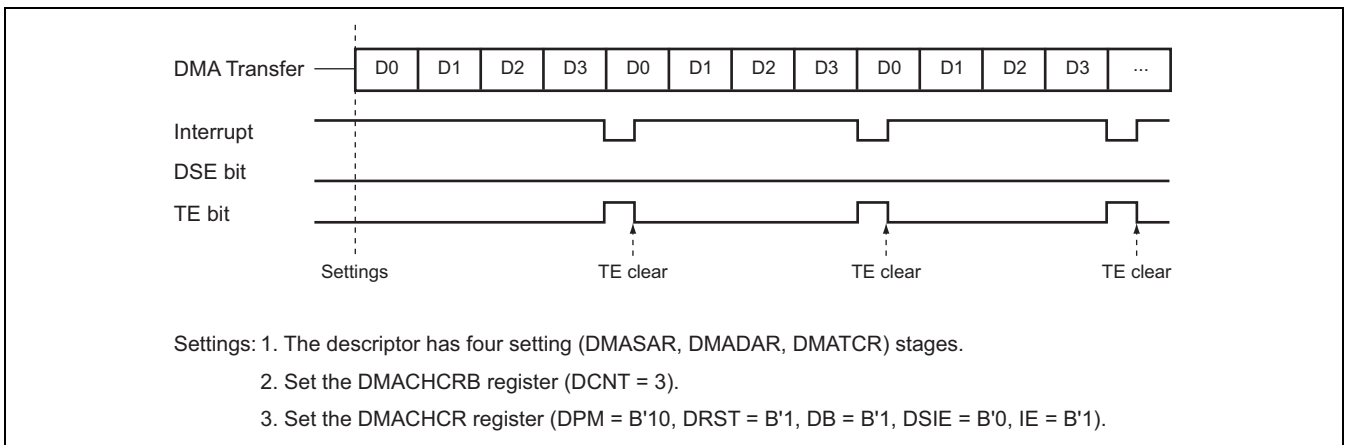
In each example, there are four descriptor stages.



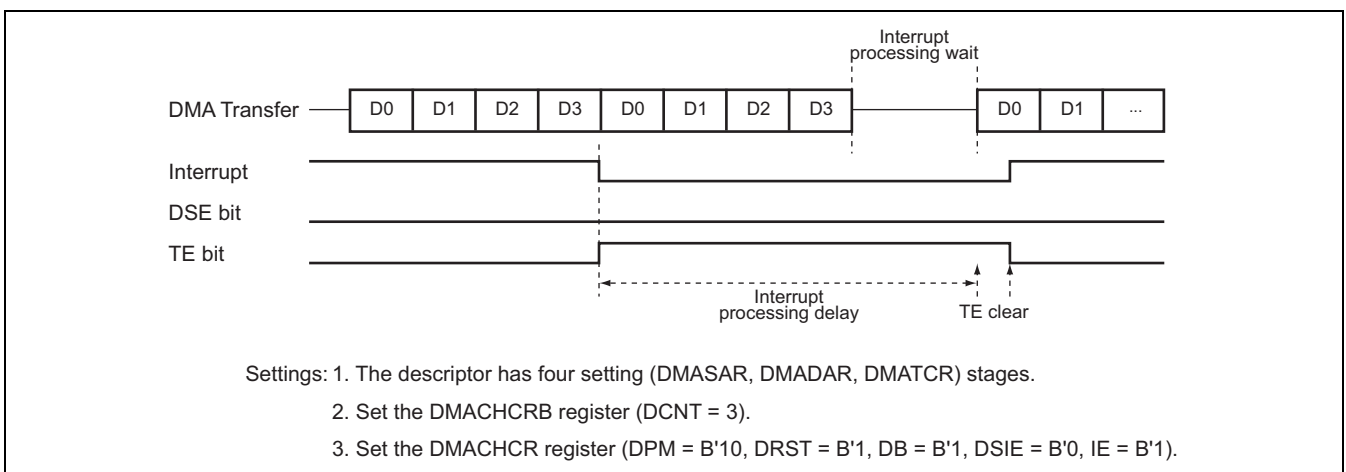
**Figure 16.9 Operating Mode 2 (Example 1)**



**Figure 16.10 Operating Mode 2 (Example 2)**



**Figure 16.11 Operating Mode 2 (Example 3)**



**Figure 16.12 Operating Mode 2 (Example 4)**

### (5) Operating Mode 3 of Descriptor Memory

Set the DPM bits in DMACHCR to B'11 to select operating mode 3 (infinite repeat mode). This mode allows consecutive transfer under control of the descriptor memory.

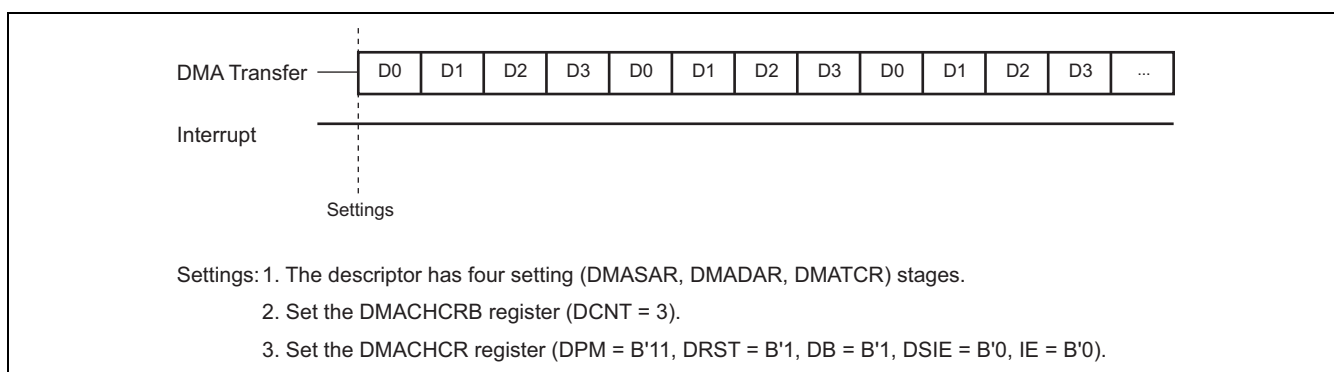
In this mode, after transfer under control of the number of stages of descriptor memory specified in the DCNT bits in DMACHCRB, the TE bit in DMACHCR is set to 1. This operation is then repeated from the head of the descriptor memory.

When the DSIE bit in DMACHCR is set to 1, a DSE interrupt is generated every time transfer under the control of one stage of descriptor memory is complete. Even if a first DSE interrupt has not been processed when a further DSE interrupt is generated, the DMA transfer is not aborted. Regardless of the number of DSE interrupts that have been generated, the TE bit can be cleared by writing to it once. Similarly, even if a first TE interrupt has not been processed when a further TE interrupt is generated, the DMA transfer is not aborted. Regardless of the number of TE interrupts that have been generated, the TE bit can be cleared by writing to it once.

Figure 16.13 is an example of transfer when infinite repeat mode is selected.

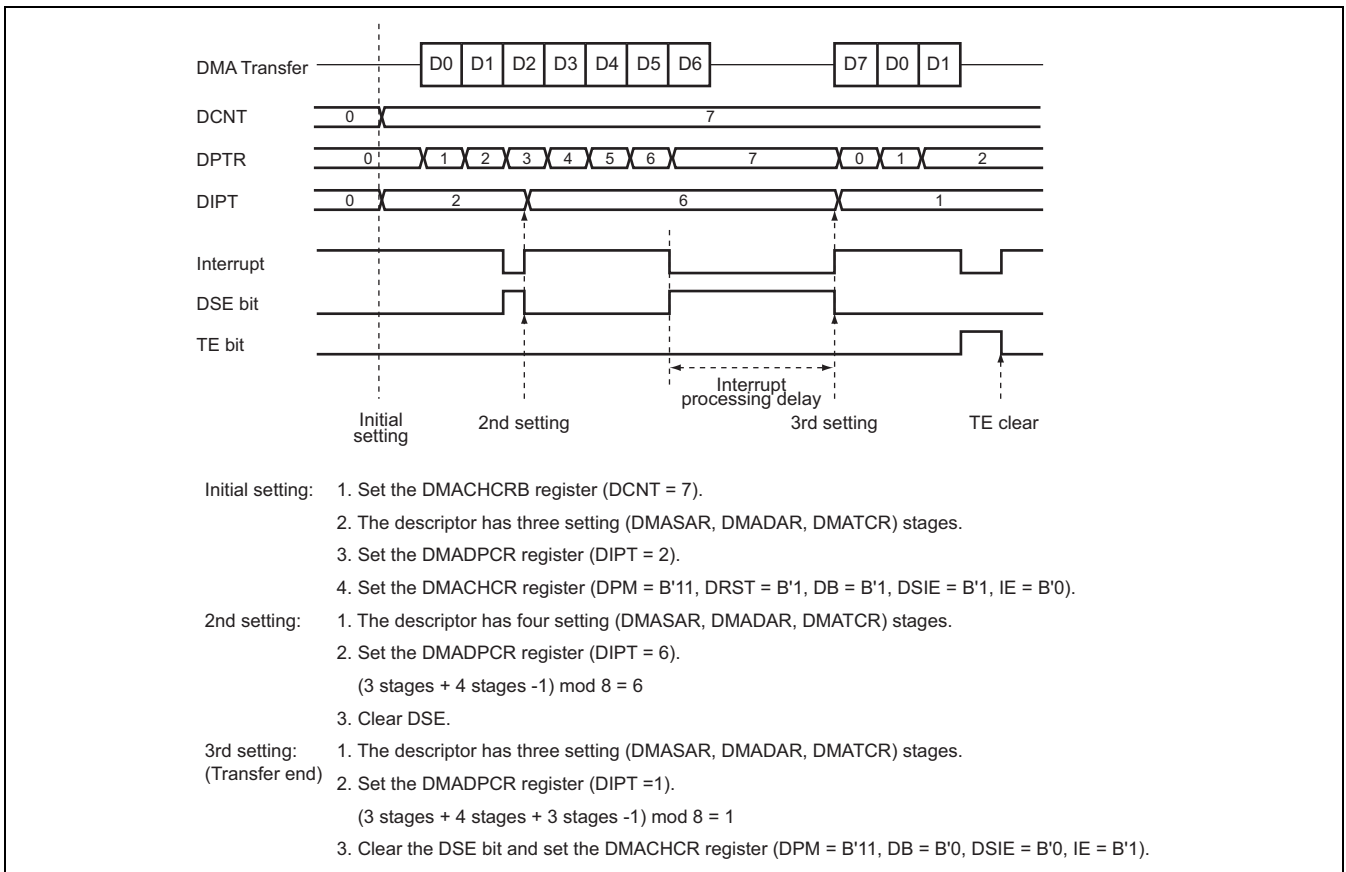
Figure 16.14 is an example of transfer when read-out interrupt mode is selected.

In each example, there are four descriptor stages.



**Figure 16.13 Operating Mode 3 (Infinite Repeat Mode)**

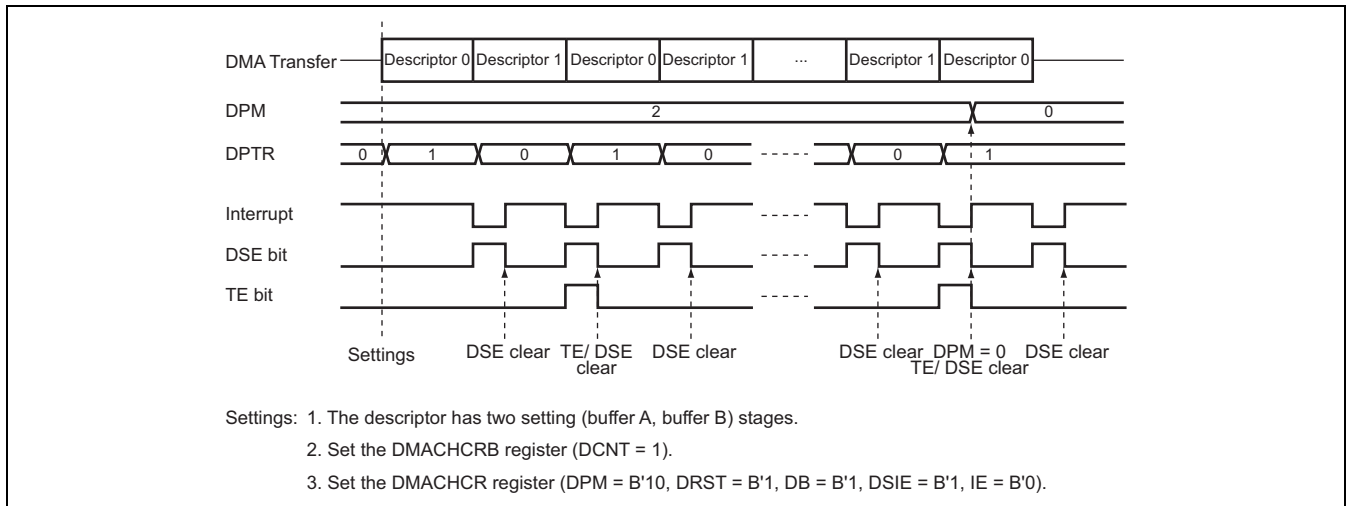




**Figure 16.14 Operating Mode 3 (Read-Out Interrupt Mode)**

### (6) Using the Descriptor Memory for Double Buffering

To use the descriptor memory for double buffering, set the number of stages of descriptor memory to 2, set the buffer configuration to the descriptor memory, and activate the memory in operating mode 2. The DSE interrupt is used in double buffering. To end the use of double buffering, disable the descriptor operating mode, which stops the transfer on completion of the transfer currently in progress.



**Figure 16.15 Using the Descriptor Memory for Double Buffering**

#### 16.4.5 Transmission Flow

Set the transfer conditions as required in the following registers:

DMA source address register (DMASAR), DMA destination address register (DMADAR), DMA transfer count register (DMATCR), DMA Channel control register (DMACHCR), DMA operation register (DMAOR) and DMA extended resource selector (DMARS)

The DMAC then transmits data in the following order.

- A transfer request is generated and the controller checks whether the transfer is allowed (DE = 1, DME = 1, TE = 0, DSE = 0, CAE = 0). When a channel is in the auto request mode, the transfer starts automatically.
- The controller checks whether updating from the descriptor memory is required.  
 Updating from the descriptor memory proceeds when the DPB bit in DMACHCR is set to 1 or the descriptor memory is enabled, if DMATCR is set to 0.  
 For updating by using the descriptor memory, see section 16.4.4, Descriptor Memory.
- Check whether address translation by the IPMMU is required.  
 Address translation by the IPMMU proceeds if the address exceeds the effective size for address translation when the DE bit in DMACHCR is enabled and updating of transfer settings from the descriptor memory is executed.
- Each time a transfer request is generated, the amount of data for a single round of transfer (specified by the TS[3:0] bits) is transmitted. The value in DMATCR is decremented by 1 every time the DMA transfer is completed.
- When the specified number of rounds of transfer are completed (the value in DMATCR is set to 0), the transfer ends normally. A TE interrupt is generated for the CPU upon the end of the transfer if the IE bit in DMACHCR is set to 1. If the descriptor memory is enabled, the processing differs with the mode of the descriptor memory. For more details, see section 16.4.4, Descriptor Memory.
- Transfer is aborted when the DMAC encounters an address error. Transfer is also aborted when the DE bit in DMACHCR or the DME bit in DMAOR is set to 0.

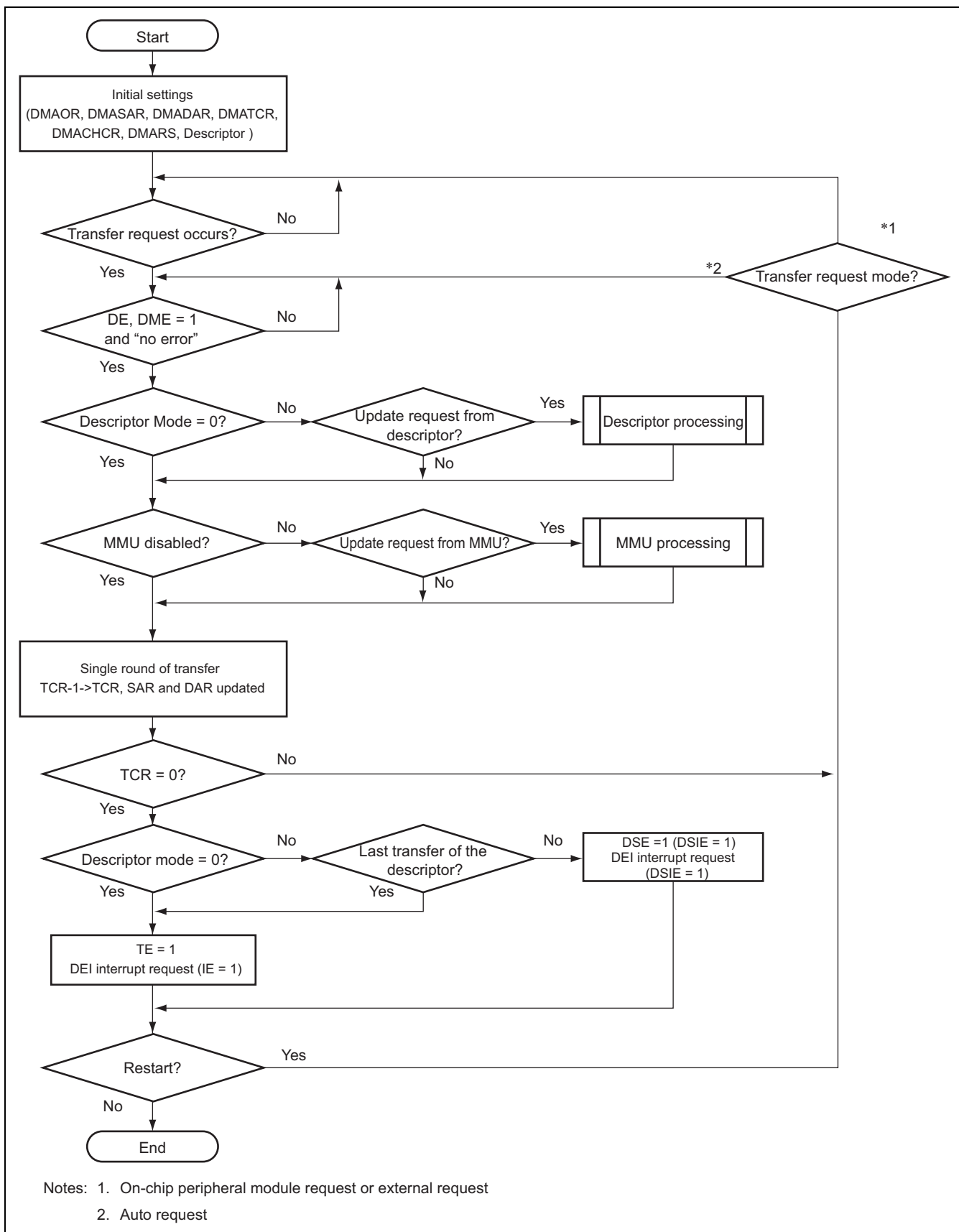


Figure 16.16 Transmission Flow

#### 16.4.6 Total Size Transmission

The amount of data for total size transmission can be set in DMATSR (in bytes), and this setting is effective regardless of the size specified in the TS bits in DMACHCR. Thereby, the desired size can be transmitted in a single round of DMA transfer.

To use this function, make the settings for total size transmission in DMASAR, DMADAR, DMATSR, DMATSRB and DMACHCR.

Total size is set in the TCR (TSR) field of descriptors and 1 is set in DMACHCRB.DTS when total size transmission and descriptors are in use.

## 16.5 Usage Notes

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

Pay attention to the following notes when using the SYS-DMAC.

### (1) DMA Transfer for Peripheral Modules

When executing DMA transfer for an on-chip peripheral module, set addresses on the appropriate boundary (in terms of the amount of data for each round of transfer) for the transfer source and destination addresses. Otherwise, an address error may occur.

### (2) Module Stop

While the SYS-DMAC is operating, the module stop register (MSTPCR2) should not be set to stop the SYS-DMAC. If the SYS-DMAC is stopped in this way, results of the transfer that was in progress cannot be guaranteed.

### (3) Address Error

When a DMA address error is generated, reset the registers of the channel on which the error has occurred and then start transfer anew.

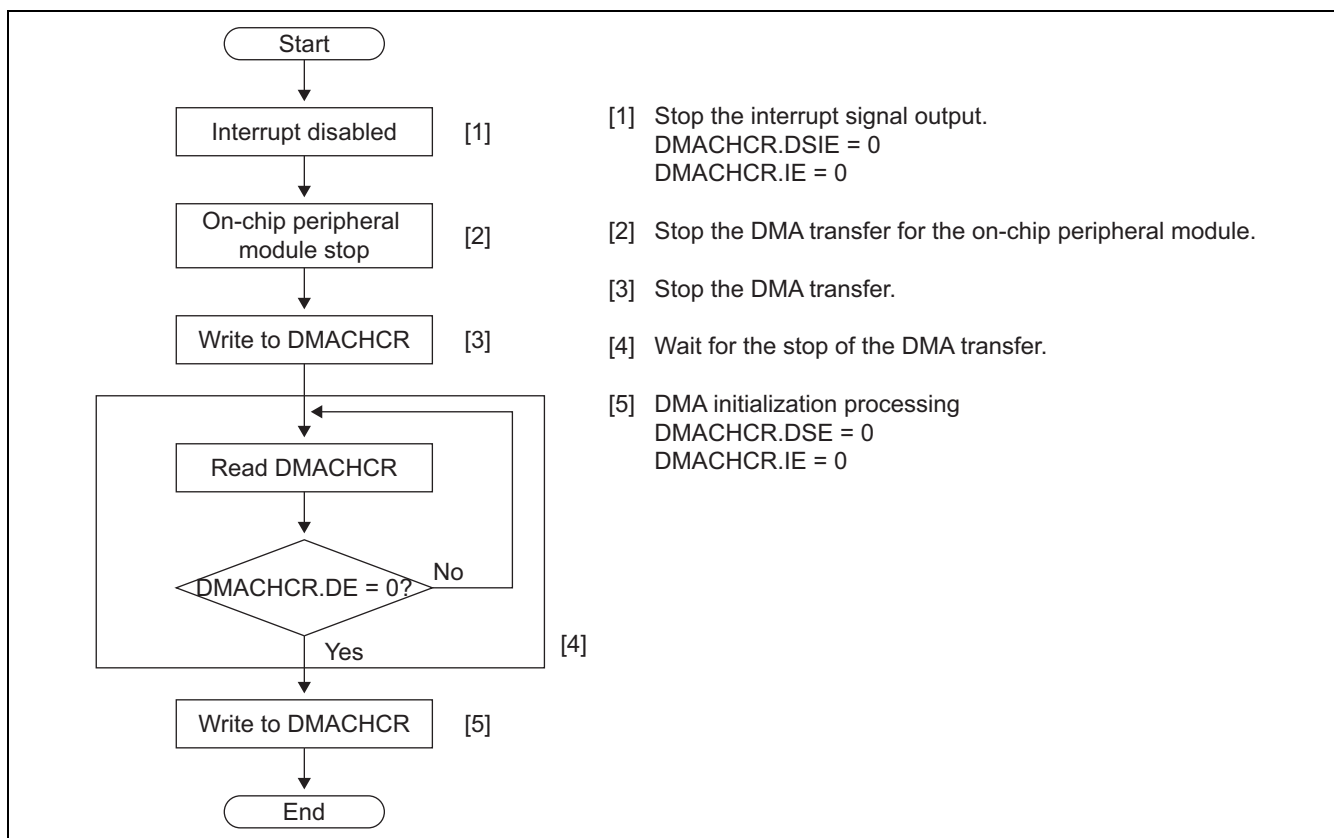
### (4) Aborting DMA Transfer

To abort a DMA transfer, disable the interrupt signal and set the DE bit in the DMA channel control register (DMACHCR) to 0 to disable the DMA transfer. If the TE and DSE bits are set when DMA transfer is aborted, these bits should be initialized. There is a possibility that TE and DSE will not be set with synchronized timing after transmission, so it's necessary to recognize the following three possibilities and take measures accordingly.

1. The DSE and TE bits are set to 1 before initialization of DMACHCR, but after the interrupt was disabled.  
The TE and DSE bits are initialized within the DMA transfer initialization sequence.
2. The DSE and TE bits are set to 1 and the controller fails to abort the transfer, after the interrupt was disabled.  
When the DE bit has become 0 after DMA transfer initialization, check the TE and DSE bits. If the TE or DSE bit is 1, go through the DMA transfer initialization process.
3. The TE and DSE bits are not cleared to 0 but the transfer is aborted, after the interrupt is disabled.  
The TE or DSE bits are not set because data for transfer still remain after transfer is aborted.

Note: Initialization of DMA transfer during execution of the last transfer leads to a delay in setting of the TE and DSE bits, so include a dummy read.

Figure 16.17 shows an example of processing to abort DMA transfer.



**Figure 16.17 Example of Processing to Abort DMA Transfer**

### (5) Descriptor Transfer

When using the descriptor transfer in cases where both conditions 1) and 2) apply, an incorrect DMA transfer proceeds before the correct transfer starts.

- Conditions

- 1) The timing of the start of transfer is specified as being after the descriptor information is loaded, i.e. DPB = 1.  
SYS-DMAC: DMACHCR\_n.DPB = 1 (refer to the description of bit 22 in section 16.3.17)
- 2) Address translation by the uTLB is enabled.

- Problem

When both conditions 1) and 2) apply, an incorrect DMA read transfer to the address formerly stored in DAR proceeds after DMA is enabled (DE = 1). Furthermore, if the address is undefined in the IPMMU, the DMA transfer may stop and operation of the DMAC may hang up without any indication of the error.

[Workarounds]

1. Use the descriptor transfer with DPB = 0.
2. Use the descriptor transfer with DPB = 1 and address translation by the uTLB disabled.
3. When using the descriptor transfer with DBP = 1 and address translation by the uTLB enabled, write the same destination address as the first address in the descriptor to the corresponding DAR before enabling DMA (DE = 1). While the incorrect DMA read transfer still proceeds, the descriptor transfer is executed correctly as long as the address written to the corresponding DAR is a defined address.

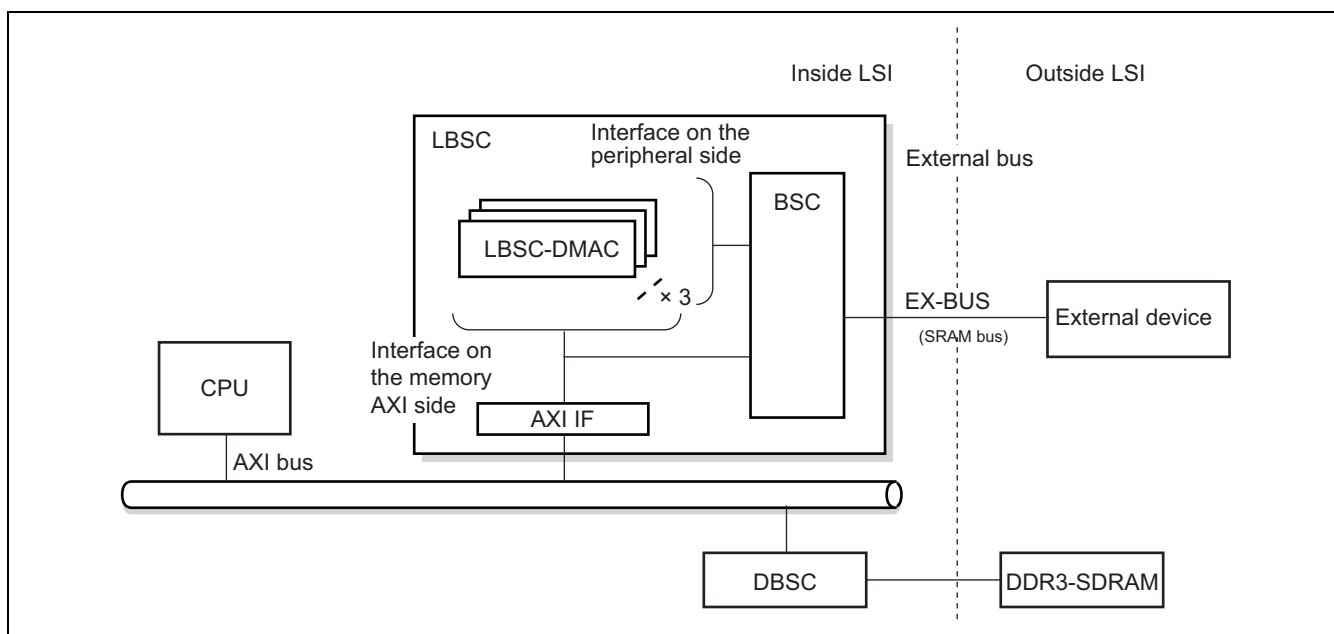
# 17. LBSC-DMAC

RZ/G1H	RZ/G1N
RZ/G1M	RZ/G1E

## 17.1 Overview

The LBSC-DMAC performs DMA transfer between the external bus (EX-BUS) and DDR3-SDRAM. The LBSC-DMAC is assigned channel numbers 0 to 2. These DMA channels are capable of independent parallel operation and a different transfer destination can be selected for each.

Different data transfer modes are selectable for each channel. In this section, the character "n" refers to one of the 43 DMA channels of the DMACs.



**Figure 17.1 Context of LBSC-DMAC**

Figure 17.1 shows the context of the LBSC-DMAC. The DMACs are connected to DDR3-SDRAM outside the chip via the DBSC, connected via a memory-side (AXI-bus) interface, and to peripherals connected to the external bus via the peripheral-side interface. Register settings within each of the DMACs select the connected (source and destination) peripheral module or memory. Of these, the LBSC-DMAC supports DMA transfers with general-purpose external devices on the EX-BUS (SRAM bus), and transfer can be performed under handshaking control by the DMA request and DMA acknowledge signals (these channels also support an auto-request mode with no handshaking).

## 17.2 Features

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

The LBSC-DMAC has the following features.

- Number of channels: Three channels (channels 0 to 2)
- Address space: Physical address space
- Transfer direction: Capable of transfer from a peripheral module to a memory (AXI bus), or from a memory (AXI bus) to a peripheral module
- Transfer data length:
  - For peripherals: Selectable from 1, 2, or 4 bytes.
  - For memory (AXI bus):
    - When the SWMD bit in the DCR register is cleared to 0: Access size specified for a memory (AXI bus) (For details on each channel access size, see section 17.4.8, DMA Control Register (DCR).)
    - When the SWMD bit in the DCR register is set to 1: Selectable from 1, 2, or 4 bytes
    - When final packing processing is performed while the PKMD bit in the DCR register is set to 1: 1 byte or the access size specified for a memory (AXI bus)
- Transfer burst length: 1 or 8 (Transfer with a burst length of 8 is supported only for channels 0 and 1.)
- Transfer count:
  - Maximum: 16 M (16,777,216) or 64 M (67,108,864) times (64 M is supported only for channel 0 of LBSC-DMAC.)
  - Minimum: One time
- Address mode: Dual address mode
  - Dual address mode
    - Both the transfer source and transfer destination are accessed by using addresses.
    - Values set in the DMAC's internal registers indicate the addresses for both the transfer source and the transfer destination. (Registers: DMA source address register (DSAR0 or DSAR1), DMA destination address register (DDAR0 or DDAR1), and DMA control register (DCR; bits SPDAM and DPDAM))
- Transfer requests: The external requests, peripheral requests, auto-requests, and timer requests are supported.
  - External requests (LBSC-DMAC channel 2)
    - Requests from three external DREQ pins. Low or high level detection or edge detection can be specified for the request signals (DREQ) in the LBSC register. Either the active high or active low logic can be specified by LBSC for the request acknowledge level signal (DRACK) and the acknowledge level signal (DACK). (DRACK is supported for only channel 0 of the LBSC-DMAC.)
  - Peripheral request
    - Transfer requests from on-chip peripheral modules.
  - Auto-request
    - Initiates DMA transfer according to the DMAC internal timing.
  - Timer request
    - A transfer request is generated at an interval specified by a timer in the DMAC.
- Transfer modes: Single transfer and continuous transfer modes are supported.
  - Single transfer mode
    - DMA transfer ends when transfer is completed for the transfer count specified by the DMA transfer count register.



— Continuous transfer mode

Available in all channels. If there is a next DMA transfer request (DNXT) when transfer is completed for the transfer count specified by the DMA transfer count register, the next DMA transfer information is fetched and the next DMA transfer is continued. If no next DMA transfer request (DNXT) is found, the DMAC waits until a next DMA transfer request is specified. The continuous transfer mode is terminated by the DQEND bit in the DMA command register (DCMDR).

- DMA information can be specified in two modes: one mode uses one of two sets of DMA information registers (registers in which the offset of the address is in the range from H'0000\_0000 to H'0000\_0014) repeatedly, and the other uses the two sets alternately.
- The DMAC also provides the automatic continuous transfer mode. The automatic continuous transfer mode is enabled by setting the ACMD bit in the DMA control register (DCR) to 1 while the continuous transfer mode is enabled (the CT bit in DCR is set to 1). In this mode, when transfer is completed for the transfer count specified by the DMA transfer count register, the DMAC fetches the next DMA transfer information and continues DMA transfer regardless of whether there is a next DMA transfer request (DNXT). This mode is terminated by the DQEND bit in the DMA command register (DCMDR).
- Transfer end interrupt: An interrupt request can be sent to the CPU on completion of the number of transfers specified for each DMA information unit.
- Supports DMA operation for Ultra ATA (LBSC-DMAC channels 0 and 1 only)
  - Timer monitoring function for temporarily queued requests, write-data setup/hold setting function, and CRC indicating function in DMA operations for Ultra ATA.

### 17.3 DMA Transfer Method in LBSC-DMAC

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

The relation of each DMA channel to peripherals is shown below. Transfers can be performed with between various functional blocks over different channels, but if destination is on the memory (AXI) side, DDR3-SDRAM via the DBSC and so on becomes the destination for transfer according to the address setting.

Channel	Application	Communication Type	Selection of Transfer Destination (On-Chip Peripheral Function)
LBSC-DMA00	Communication with general-purpose device via EX-BUS	Dual address transfer, single transfer or 8-burst transfer,	DREQ/DACK number and DMA channel number correspond.
LBSC-DMA01		DREQ/DACK handshake (Channel 0 can select DRACK) Channels 0 and 1 can select Ultra ATA DMA function. (Only RZ/G1H, M, N, and E)	External bus spaces allocated to each DMAC are specified in the LBSC internal register.
LBSC-DMA02		Dual address transfer single transfer, DREQ/DACK handshake (Only RZ/G1H, M, N, and E)	

## 17.4 Register Descriptions

Registers shown below can be accessed from ARM CPU. The DMAC has forty-three channels; some registers are prepared for each individual channel and some are used by all channels in common.

### 17.4.1 LBSC-DMAC Register Map

**Table 17.1 List of LBSC-DMAC Registers**

Register Name		Abbr.	Access Type	Address	Access Size	RZ/G Series Products			
						RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
DMA source address register 0	DMA information register set 0	DSAR0	R/W	H'FEC0 1000 + H'40 × [n]	32	√	√	√	√
DMA destination address register 0		DDAR0	R/W	H'FEC0 1004 + H'40 × [n]	32	√	√	√	√
DMA transfer count register 0		DTCR0	R/W	H'FEC0 1008 + H'40 × [n]	32	√	√	√	√
DMA source address register 1	DMA information register set 1	DSAR1	R/W	H'FEC0 100C + H'40 × [n]	32	√	√	√	√
DMA destination address register 1		DDAR1	R/W	H'FEC0 1010 + H'40 × [n]	32	√	√	√	√
DMA transfer count register 1		DTCR1	R/W	H'FEC0 1014 + H'40 × [n]	32	√	√	√	√
DMA source address status register		DSASR	R	H'FEC0 1018 + H'40 × [n]	32	√	√	√	√
DMA destination address status register		DDASR	R	H'FEC0 101C + H'40 × [n]	32	√	√	√	√
DMA transfer count status register		DTCSR	R	H'FEC0 1020 + H'40 × [n]	32	√	√	√	√
DMA control register		DCR	R/W	H'FEC0 1028 + H'40 × [n]	32	√	√	√	√
DMA command register		DCMDR	—/W	H'FEC0 102C + H'40 × [n]	32	√	√	√	√
DMA forced stop register		DSTPR	—/W	H'FEC0 1030 + H'40 × [n]	32	√	√	√	√
DMA status register		DSTSR	R	H'FEC0 1034 + H'40 × [n]	32	√	√	√	√
DMA channel debugging register		DDBG	R/W	H'FEC0 1038 + H'40 × [n]	32	√	√	√	√
DMA channel debugging register 2		DDBG2	R/W	H'FEC0 103C + H'40 × [n]	32	√	√	√	√
DMA timer control register		DTIMR	R/W	H'FEC0 1400	32	√	√	√	√
DMA request mask control register		DRMSKR	R/W	H'FEC0 1404	32	√	√	√	√
DMA memory access priority level control register		DMLVLR	R/W	H'FEC0 140C	32	√	√	√	√
DMA transfer end interrupt status register		DINTSR	R	H'FEC0 1410	32	√	√	√	√
DMA transfer end interrupt status clear register		DINTCR	—/W	H'FEC0 1414	32	√	√	√	√
DMA transfer end interrupt enable register		DINTMR	R/W	H'FEC0 1418	32	√	√	√	√
DMA activation status register		DACTSR	R	H'FEC0 1420	32	√	√	√	√

Register Name	Abbr.	Access Type	Address	Access Size	RZ/G Series Products			
					RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
DMA00 to DMA02 channel software-reset register	LSRSTR0 to LSRSTR2	R/WC1	H'FEC0 1424 to H'FEC0 142C	32	√	√	√	√
External-DMA data alignment control register	DMALGR	R/W	H'FEC0 1480	32	√	√	√	√
LBSC-DMA AXI priority control register	LBSC-DMASPR	R/W	H'FEC0 1490	32	√	√	√	√
Ultra ATA DMA mode register	UATMR	R/W	H'FEC0 14C0	32	√	√	√	√
Ultra ATA write cycle setting register	UATWCR	R/W	H'FEC0 14C4	32	√	√	√	√
Ultra ATA timeout period setting registers 0 and 1	UATTSR0/ UATTSR1	R/W	H'FEC0 14C8 to H'FEC0 14E8	32	√	√	√	√
Ultra ATA error indication register	UATTER	R/W	H'FEC0 14CC	32	√	√	√	√
Ultra ATA error interrupt enable register	UATIER	R/W	H'FEC0 14D0	32	√	√	√	√
Ultra ATA CRC code indication register	UATCRCR	R	H'FEC0 14D4	32	√	√	√	√
Ultra ATA transfer mode register	UATTMR	R/W	H'FEC0 0030	32	√	√	√	√

Notes: 1. n: LBSC-DMAC channel number

2. The CPU should access the above register in longword units (32 bits). The CPU should not access the above register in byte or word units.
3. Do not write to any addresses other than listed above. Operations cannot be guaranteed if writing is attempted. Values read from addresses other than listed above are undefined.

#### [Legend]

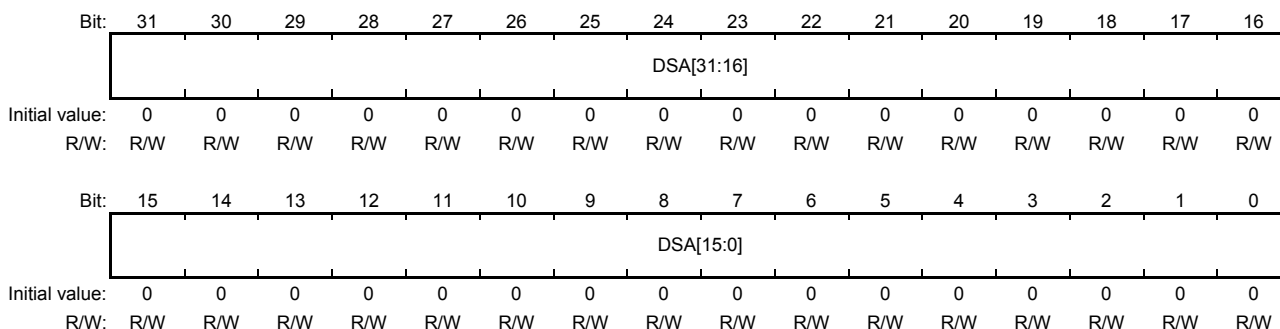
Initial value:	Register value after a reset
—:	Undefined value
R/W:	Readable/writable. The written value can be read.
R/WC1:	Readable/writable. Writing 1 initializes the bit. Writing 0 is ignored.
R:	Read-only. The write value should always be 0.
—/W:	Write-only. The read value is undefined.

All signals for the control registers and status registers are active-high.

### 17.4.2 DMA Source Address Registers 0, 1 (DSAR0, DSAR1)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

**Function:** Each register specifies the DMA start address of the transfer source.



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	DSA	All 0	R/W	<p>DMA Transfer Source Start Address</p> <p>The transfer source start address indicates a memory address, a peripheral module address, or an external module address according to the SMDL bit value in the DMA control register (DCR).</p> <p>When SMDL = 0: Transfer source address = Memory (AXI bus) address</p> <p>When SMDL = 1: Transfer source address = Peripheral address or external module address</p>

Notes: 1. When the address setting is a memory address, the following address boundary should be used.

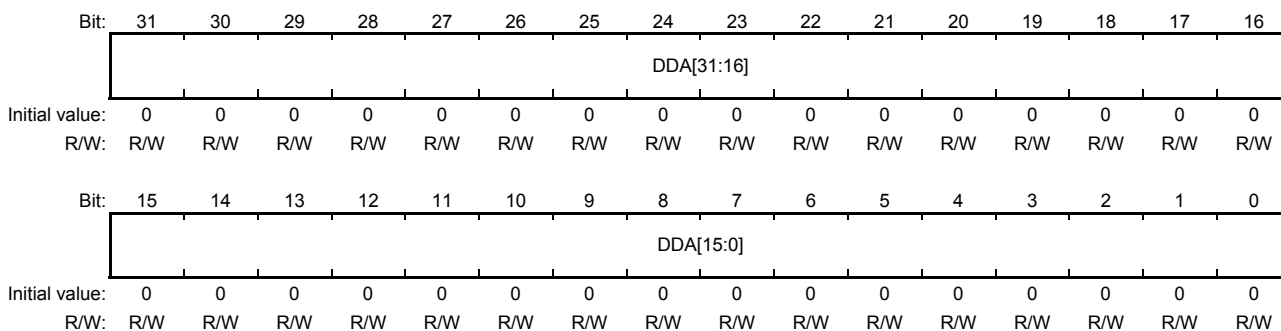
SWMD Bit in the DCR Register	LBSC-DMAC Channel Number	
	Channels 0 and 1	Channel 2
0	32-byte boundary	16-byte boundary
1	4-byte boundary	

- When the address set is an external module address, and in addition the SPDS or DPDS bit in DCR selects an 8-bit access size, up to an 8-bit boundary can be set.
- In the case of note 2, when the DMAC external module data access size is smaller than the external bus width setting in LBSC, the DMALGR register in the DMAC can be used to specify whether there is a change in data alignment (data access byte lane according to the address value). See section 17.4.22, External DMA Data Alignment Control Register (DMALGR) and specifications of section 14, LBSC within Bus Bridge.
- When an address setting is an external module address, the upper address bits 31 to 26 are not connected to the external bus. These are provided for ease in understanding the contents of software settings. Also, CS1 and EX\_CS0 to EX\_CS5 space identification using these upper bits is not performed. DMAC access destination space is identified through the LBSC external DMAC channel area allocation register.
- When an address setting is for a peripheral device, the upper address is provided for ease of understanding of the contents of software settings, and is not used for identification of access destination space specific to the peripheral.

### 17.4.3 DMA Destination Address Registers 0, 1 (DDAR0, DDAR1)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

**Function:** Each register specifies the DMA start address of the transfer destination.



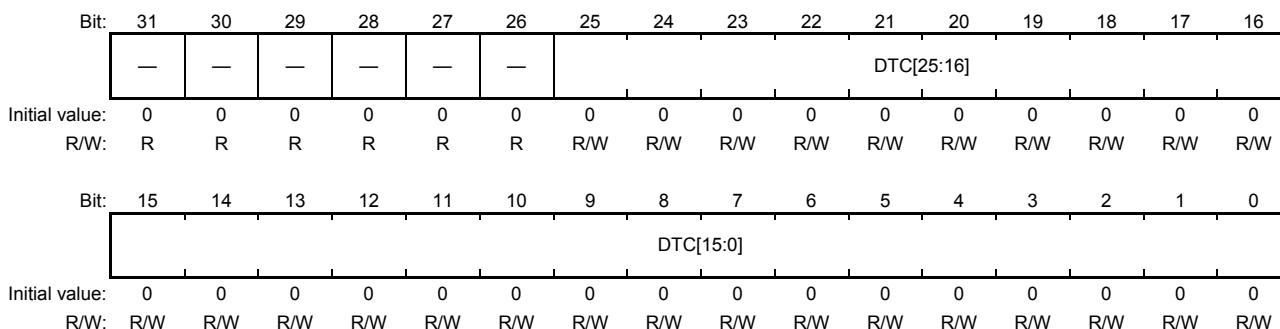
Bit	Bit Name	Initial Value	R/W	Description
31 to 0	DDA	All 0	R/W	<p>DMA Transfer Destination Start Address</p> <p>The transfer destination start address indicates a memory address, a peripheral module address, or an external module address according to the DMDL bit value in the DMA control register (DCR).</p> <p>When DMDL = 0: Transfer destination address = Memory (AXI bus) address</p> <p>When DMDL = 1: Transfer destination address = Peripheral module or external module address</p>

**Note:** See the notes 1 to 5 in section 17.4.2, DMA Source Address Registers 0, 1 (DSAR0, DSAR1). Those notes also apply to this register.

### 17.4.4 DMA Transfer Count Registers 0, 1 (DTCR0, DTCR1)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

**Function:** Each register specifies the DMA transfer count.



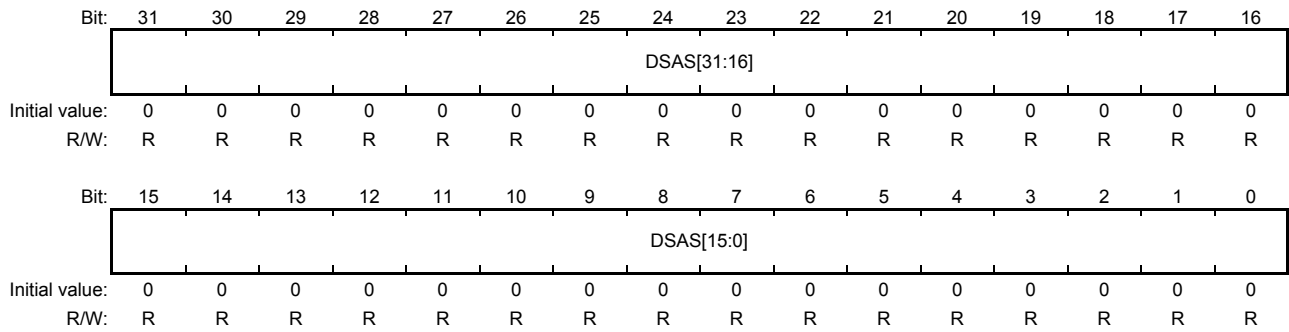
Bit	Bit Name	Initial Value	R/W	Description
31 to 26	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
25 to 0	DTC	All 0	R/W	DMA Transfer Count These bits specify the DMA transfer count (number of bytes, words, or longwords). LBSC-DMAC channel 0: The maximum count is DTC = H'0, which indicates 64 M (67,108,864) times. Other than LBSC-DMAC channel 0: The maximum count is DTC = H'0, which indicates 16 M (16,777,216) times.

**Note:** This register specifies the transfer count on the peripheral side for transfer from a peripheral to a memory (AXI bus) or from a memory (AXI bus) to a peripheral. For 8-burst DMA operation, one count for each 8-burst operation.

### 17.4.5 DMA Source Address Status Register (DSASR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

**Function:** DSASR indicates the transfer source address.

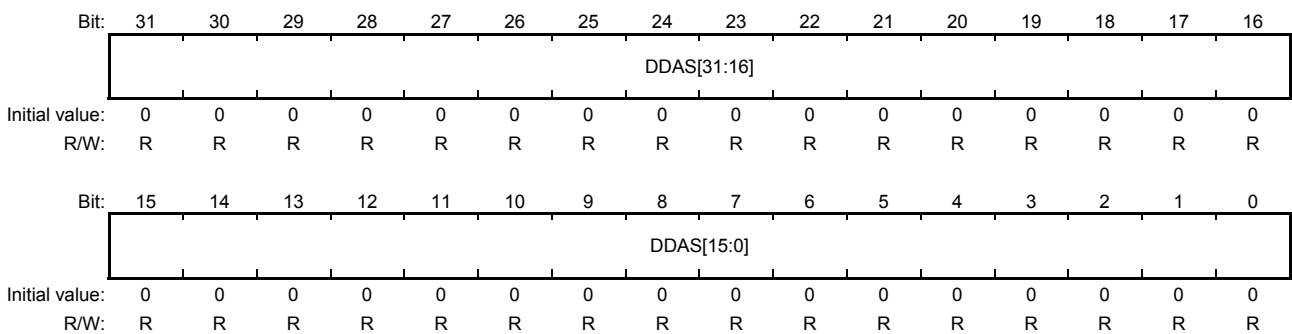


Bit	Bit Name	Initial Value	R/W	Description
31 to 0	DSAS	All 0	R	These bits indicate the latest source address for which DMA transfer has been completed.

### 17.4.6 DMA Destination Address Status Register (DDASR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

**Function:** DDASR indicates the transfer destination address.



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	DDAS	All 0	R	These bits indicate the latest destination address for which DMA transfer has been completed.



### 17.4.7 DMA Transfer Count Status Register (DTCSR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

**Function:** DTCSR indicates the remaining count of the current transfer.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
	—	—	—	—	—	—	DTCS[25:16]											
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R		
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
	DTCS[15:0]																	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R		

Bit	Bit Name	Initial Value	R/W	Description
31 to 26	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
25 to 0	DTCS	All 0	R	Remaining DMA Transfer Count These bits indicate the remaining count of the current DMA transfer (number of bytes, words, or longwords). Note that bits 25 to 0 are used only for the LBSC-DMAC channel 0 and bits 23 to 0 are used for the other channels. The number of transferred bytes depends on the peripheral's data bus width.

**Note:** This register indicates the remaining transfer count on the peripheral side for transfer from a peripheral to a memory (AXI bus) or from a memory (AXI bus) to a peripheral.

### 17.4.8 DMA Control Register (DCR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

**Function:** DCR specifies the transfer mode.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	DTAMD	DTAC	DTAU	DTAU1	SWMD	BTMD	PKMD	—	CT	ACMD	DIP
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	SMDL	SPDAM	SDRMD	SPDS	—	—	DMDL	DPDAM	DDRMD	DPDS	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 27	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
26	DTAMD	0	R/W	Specifies the data alignment conversion mode when a memory is accessed in DMA transfer (see section 17.5.7, Data Alignment in AXI Bus Interface). 0: Conversion according to the combination of the input pin (little: endian mode) and the AXI width. 1: Conversion according to the combination of DTAC (DMA data alignment conversion), DTAU (DMA data alignment unit), and DTAU1 (8-byte conversion in 4-byte units).
25	DTAC	0	R/W	Enables or disables data alignment conversion when a memory is accessed in DMA transfer (see section 17.5.7, Data Alignment in AXI Bus Interface). This setting is valid when DTAMD = 1. 0: Disables data alignment conversion. 1: Enables data alignment conversion.
24	DTAU	0	R/W	Specifies the unit for data alignment conversion (see section 17.5.7, Data Alignment in AXI Bus Interface). This setting is valid when DTAMD = 1. 0: Byte units 1: Word units
23	DTAU1	0	R/W	Specifies whether 8-byte data alignment is performed in 4 bytes unit (see section 17.5.7, Data Alignment in AXI Bus Interface). The setting value is valid when DTAMD = 1. 0: Not performed. 1: Performed.
22	SWMD	0	R/W	Specifies memory (AXI bus) access size. 0: * (Clearing this bit to 0 is recommended when DDR3-SDRAM is specified.) 1: 4 bytes

Bit	Bit Name	Initial Value	R/W	Description
21	BTMD	0	R/W	Specifies the burst DMA transfer (only for LBSC-DMAC channels 0 and 1). Burst DMA transfer is performed for peripherals. 0: Does not transfer in burst mode. 1: Transfers in burst mode (burst length is fixed to eight).
20	PKMD	0	R/W	Enables or disables packing of data read from a peripheral for DMA transfer from the peripheral to the AXI bus. 0: Disables packing. 1: Enables packing.
19	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
18	CT	0	R/W	Specifies continuous DMA transfer. 0: Does not transfer in continuous mode. 1: Transfers in continuous mode.
17	ACMD	0	R/W	Specifies automatic continuous DMA transfer (valid only when CT = 1). 0: Does not transfer in automatic continuous mode (checks DNXT = 1 in DCMDR). 1: Transfers in automatic continuous mode (regardless of the DNXT bit in DCMDR).
16	DIP	0	R/W	Specifies the valid DMA information set(s). 0: Uses one DMA information set repeatedly. 1: Uses two DMA information sets alternately.
15, 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13	SMDL	0	R/W	Selects the transfer source module. 0: Memory (AXI bus) 1: Peripheral
12	SPDAM	0	R/W	Specifies whether to fix or increment the transfer source peripheral address. 0: Fixes the peripheral address at the value specified in DSAR0 or DSAR1. 1: Increments the peripheral address (increments by one for 8-bit transfer, by two for 16-bit transfer, or by 4 for 32-bit transfer). When SMDL = 0, the address for memory access (via the AXI bus) is incremented regardless of the setting of this bit.
11, 10	SDRMD	00	R/W	These bits specify the DMA request mode for the transfer source. 00: Module request (external request or peripheral module request) 01: Auto-request 10: Timer request 11: Setting prohibited When SMDL = 0, clear the SDRMD bits to B'00 or set them to the same value as that of the DDRMD bits.
9, 8	SPDS	00	R/W	These bits specify the data bus width for the transfer source peripheral. 00: 8 bits 01: 16 bits 10: 32 bits 11: Setting prohibited When SMDL = 0, clear the SPDS bits to B'00 or set them to the same value as that of the DPDS bits.

Bit	Bit Name	Initial Value	R/W	Description
7, 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5	DMDL	0	R/W	Selects the transfer destination module. 0: Memory (AXI bus) 1: Peripheral
4	DPDAM	0	R/W	Specifies whether to fix or increment the transfer destination peripheral address. 0: Fixes the peripheral address at the value specified in DDAR0 or DDAR1. 1: Increments the peripheral address (increments by one for 8-bit transfer, by two for 16-bit transfer, or by 4 for 32-bit transfer). When DMDL = 0, the address for memory access (via the AXI bus) is incremented regardless of the setting of this bit.
3, 2	DDRMD	00	R/W	These bits specify the DMA request mode for the transfer destination. 00: Module request (external request or peripheral module request) 01: Auto-request 10: Timer request 11: Setting prohibited When DMDL = 0, clear the DDRMD bits to B'00 or set them to the same value as that of the SDRMD bits.
1, 0	DPDS	00	R/W	These bits specify the data bus width for the transfer destination peripheral. 00: 8 bits 01: 16 bits 10: 32 bits 11: Setting prohibited When DMDL = 0, clear the DPDS bits to B'00 or set them to the same value as that of the SPDS bits.

- Notes:
- When SMDL and DMDL = 1 and 0, data is transferred from a peripheral to a memory.  
When SMDL and DMDL = 0 and 1, data is transferred from a memory to a peripheral.  
Setting SMDL and DMDL = "1 and 1" or "0 and 0" is prohibited.
  - Not all DMAC functions can be applied to every peripheral. DMAC functions must be specified appropriately according to the functions and restrictions of each peripheral.
  - Since the width of the EX-BUS is 16 bits, setting of the SPDS or DPDS bits for the LBSC-DMAC to B'10 (selecting a transfer source or destination width of 32 bits, respectively) is prohibited.
- \* The following table summarizes the memory (AXI) access size in each DMAC channel when SWMD bit is cleared to 0.

SWMD Bit in DCR Register	LBSC-DMAC Channel Number	
	Channels 0 and 1	Channel 2
0	32 bytes	16 bytes

### 17.4.9 DMA Command Register (DCMDR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

**Function:** DCMDR activates or stops DMA transfer.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	BDOUT	DQSPD	DQSPC	DMSPD	DMSP C	DQEND	DNXT	DMEN
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7	BDOUT	0	—/W	1: Forcibly writes the data read from a peripheral to the AXI bus side (Transfer direction: from a peripheral to the AXI bus). Writing 1 to this bit forcibly writes to the AXI bus side, and then terminates DMA transfer.
6	DQSPD	0	—/W	1: Temporarily stops transfer in DMA information units.
5	DQSPC	0	—/W	1: Cancels temporary transfer stop in DMA information units.
4	DMSPD	0	—/W	1: Temporarily stops transfer in bus cycle units.
3	DMSPC	0	—/W	1: Cancels temporary transfer stop in bus cycle units.
2	DQEND	0	—/W	1: Terminates continuous DMA transfer mode. Only the DMA information specified before is transferred, and then continuous transfer mode is terminated.
1	DNXT	0	—/W	1: Requests the next DMA transfer. In continuous transfer mode, after the current DMA information is transferred, the next DMA information is transferred.
0	DMEN	0	—/W	1: Activates DMA transfer.

**Note:** For use of BDOUT, see sections 17.5.3, Packing Data Read from Peripheral or External Module and 17.5.4, Limitations on Packing of Data Read from Peripheral or External Module.

**17.4.10 DMA Forced Stop Register (DSTPR)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

**Function:** DSTPR forcibly terminates DMA transfer.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DMSTP
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	—/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	DMSTP	0	—/W	1: Forcibly terminates DMA transfer. After the current bus cycle is completed, DMA transfer is terminated. (Values set for the DMA transfer status registers (DSASR, DDASR, and DTCSR) are retained.)

### 17.4.11 DMA Status Register (DSTSR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

**Function:** DSTSR indicates the DMA transfer status.

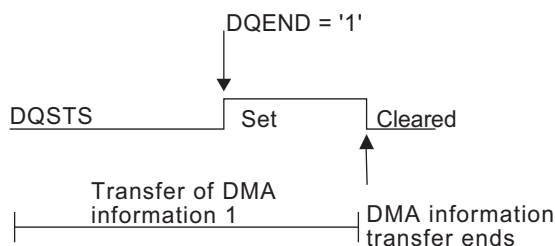
Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	NDP1	NDP0	DQSPS	DMSPS	DQSTS	DRSTS	DMSTS
Initial value:	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 7	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
6	NDP1	0	R	Next DMA Transfer Information Register Status 1 0: Does not transfer DMA information in DMA information register set 1 in the next DMA information transfer. 1: Transfers DMA information in DMA information register set 1 in the next DMA information transfer.
5	NDP0	1	R	Next DMA Transfer Information Register Status 0 0: Does not transfer DMA information in DMA information register set 0 in the next DMA information transfer. 1: Transfers DMA information in DMA information register set 0 in the next DMA information transfer.
4	DQSPS	0	R	Temporary Stop Status of DMA Information Updating 0: Normal operation 1: DMA information updating is temporarily stopped.
3	DMSPS	0	R	Temporary Stop Status of DMA Transfer 0: Normal operation 1: DMA transfer is temporarily stopped.
2	DQSTS	0	R	DMA Acceptance End Status 0: DMA information can be accepted. 1: DMA information acceptance is stopped.
1	DRSTS	0	R	DMA Transfer Request Status 0: Next DMA transfer has not been requested. 1: Next DMA transfer has been requested.
0	DMSTS	0	R	DMA Status 0: DMA transfer has been completed. 1: DMA transfer is active.

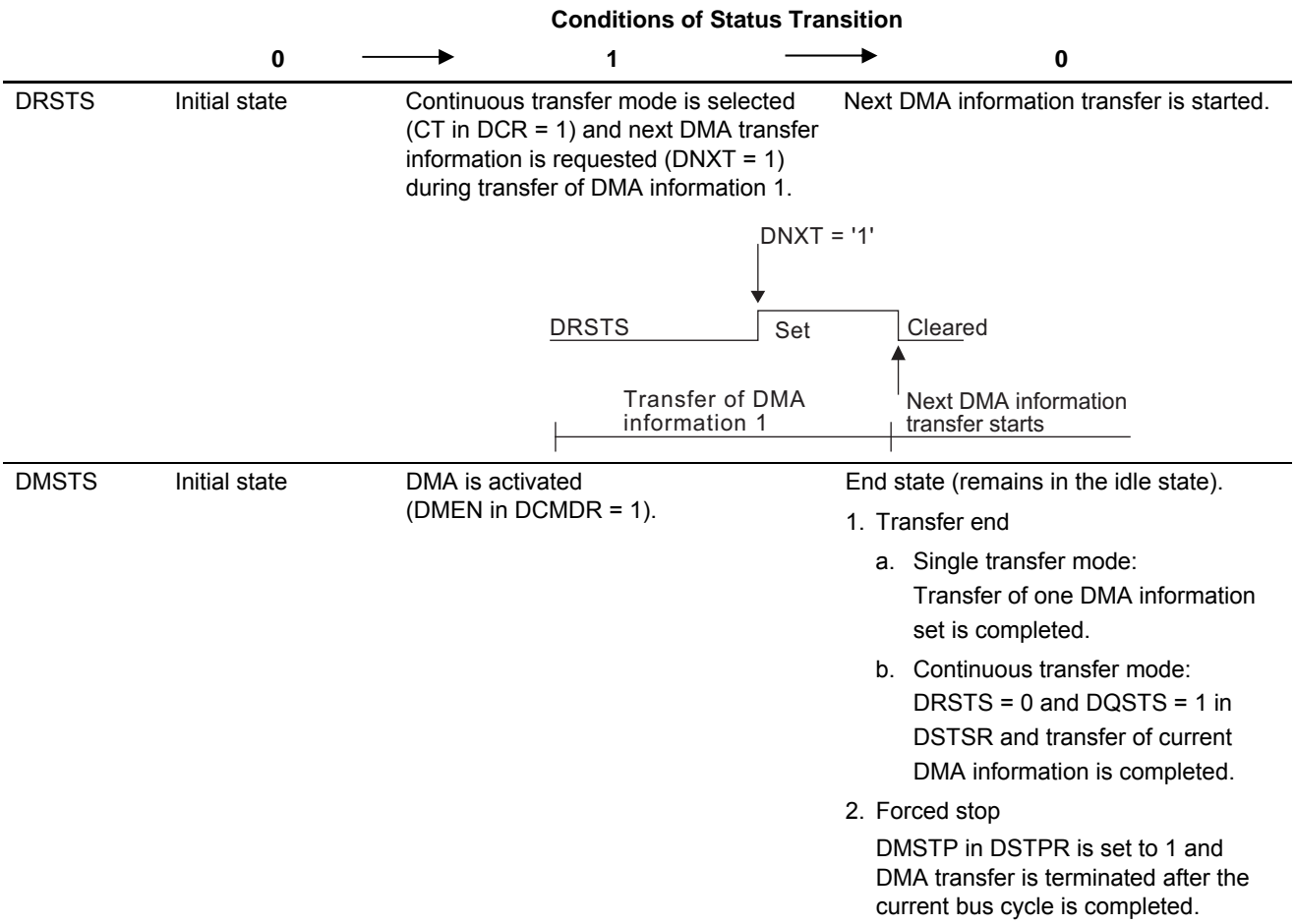
Note: Either NDP0 or NDP1 (next DMA transfer information register status 0 or 1) is always set to 1.

The following shows the transition of each bit status in DSTSR.

		<b>Conditions of Status Transition</b>	
		0	1
		→	→
		0	0
NDP1	Initial state	Continuous transfer mode is selected and information register sets 0 and 1 are used alternately (DIP in DCR = 1): DMA transfer for information register set 0 is in progress.	Continuous transfer mode is selected and information register sets 0 and 1 are used alternately (DIP in DCR = 1): DMA transfer for information register set 1 is in progress.
NDP0	—	1. Initial state 2. Single transfer mode: Always 3. Continuous transfer mode is selected and information register set 0 is used repeatedly (DIP in DCR = 0): Always 4. Continuous transfer mode is selected and information register sets 0 and 1 are used alternately (DIP in DCR = 1): DMA transfer for information register set 1 is in progress.	Continuous transfer mode is selected and information register sets 0 and 1 are used alternately (DIP in DCR = 1): DMA transfer for information register set 0 is in progress.
DQSPS	Initial state	DMA transfer is temporarily stopped in DMA information units (DQSPD in DCMDR = 1) and the current information transfer is completed.	Temporary stop of DMA transfer in DMA information units is canceled (DQSPC in DCMDR = 1).
DMSPS	Initial state	DMA transfer is temporarily stopped in bus cycle units (DMSPD in DCMDR = 1) and the current bus cycle is completed.	Temporary stop of DMA transfer in bus cycle units is canceled (DMSPC in DCMDR = 1).
DQSTS	Initial state	Continuous transfer mode is selected (CT in DCR = 1) and DMA continuous transfer is terminated (DQEND = 1) during transfer of DMA information 1.	Transfer of DMA transfer information ends.







### 17.4.12 DMA Channel Debugging Register (DDBGR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

**Function:** DDBGR is used for debugging.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DBG02	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	DBG01		—	DBG00			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31	DBG02	0	R/W	Test Bit This bit is a test bit and cannot be written to. If this bit is written to, correct operation cannot be guaranteed.
30 to 7	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
6 to 4	DBG01	All 0	R	Test Bits
3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
2 to 0	DBG00	All 0	R	Test Bits

### 17.4.13 DMA Channel Debugging Register 2 (DDBGR2)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

**Function:** DDBGR2 is used to for debugging.

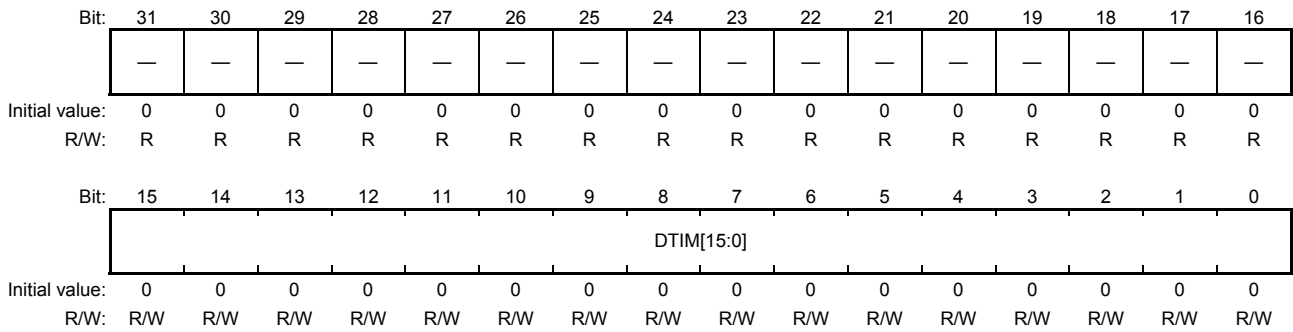
Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	DBG12	DBG11		—	—	DBG10									
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DBG10															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
30	DBG12	0	R/W	Test Bit This bit is a test bit and cannot be written to. If this bit is written to, correct operation cannot be guaranteed.
29, 28	DBG11	All 0	R/W	Test Bits These bits are test bits and cannot be written to. If these bits are written to, correct operation cannot be guaranteed.
27, 26	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
25 to 0	DBG10	All 0	R	Test Bits

**17.4.14 DMA Timer Control Register (DTIMR)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: DTIMR specifies the timer cycle in the DMAC.



Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 0	DTIM	All 0	R/W	DMAC Internal Timer Cycle Set Request mode: Specify the DMA request interval in timer request mode. Request interval: DTIM × peripheral-side bus clock cycle (ns) Peripheral-side bus clock cycle (ns) for LBSC-DMAC: Approximately 15 ns (EX-BUS frequency 65.00 MHz) Approximately 23 ns (EX-BUS frequency 43.33 MHz) Note: Even in timer request mode, operation is the same as that in auto-request mode when the value of DTIM is 0.

### 17.4.15 DMA Request Mask Control Register (DRMSKR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

**Function:** DRMSKR0 specifies the timing for detecting DMA requests in the external-bus DMAC.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	DRMSK2[3:0]			DRMSK1[3:0]			DRMSK0[3:0]			—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11 to 8	DRMSK2	All 0	R/W	These bits specify the number of clock cycles from the completion of a DMA transfer (at the time of CS# signal negation) until the next DMA request is detected, for each DMAC channel corresponding to each field. Request detection cycle: DRMSK × external bus clock cycle (ns)
7 to 4	DRMSK1	All 0	R/W	
3 to 0	DRMSK0	All 0	R/W	

**Note:** Settings for DRMSK2 to DRMSK0 are only valid when level-detection is specified for the external DREQ signal (specified by EXDMCRy in the LBSC) for the channel. In edge-detection mode, set the bits to 0.

### 17.4.16 DMA Memory Access Priority Level Control Register (DMLVLR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

**Function:** DMLVLR specifies the access priority level (1 or 2).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	DMLV2	DMLV1	DMLV0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2	DMLV2	0	R/W	These bits specify the external bus arbitration priority group for each DMAC channel which corresponds to each bit. 0: Level 2 (Low: Group 2) 1: Level 1 (High: Group 1)
1	DMLV1	0	R/W	
0	DMLV0	0	R/W	

### 17.4.17 DMA Transfer End Interrupt Status Register (DINTSR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

**Function:** DINTSR indicates the DMA transfer end interrupt status.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	DTE2	DTE1	DTE0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2	DTE2	0	R	DMA Transfer End Interrupt Status
1	DTE1	0	R	Each bit indicates the DMA transfer status (n: DMA channel number).
0	DTE0	0	R	0: Initial state or data is being transferred before the count specified by DTCR is reached. 1: Transfer has been completed for the count specified by DTCR.

### 17.4.18 DMA Transfer End Interrupt Status Clear Register (DINTCR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

**Function:** DINTCR clears the DMA transfer end interrupt status.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	DTEC2	DTEC1	DTEC0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	—/W	—/W	—/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2	DTEC2	0	—/W	DMA Transfer End Interrupt Status Clear
1	DTEC1	0	—/W	Writing 1 to each bit clears the corresponding DMA transfer end interrupt status (n: DMAC channel number)
0	DTEC0	0	—/W	Writing 0 to these bits is ignored. Each bit is always read as 0.



**17.4.19 DMA Transfer End Interrupt Enable Register (DINTMR)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

**Function:** DINTMR controls output of DMA transfer end interrupts.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	DTEM2	DTEM1	DTEM0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2	DTEM2	0	R/W	DMA Transfer End Interrupt Output Control
1	DTEM1	0	R/W	An interrupt signal is output as a level signal (n: DMA channel number).
0	DTEM0	0	R/W	0: Does not output an interrupt on completion of a DMA transfer. 1: Outputs an interrupt on completion of a DMA transfer.

### 17.4.20 DMA Activation Status Register (DACTSR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

**Function:** DACTSR indicates the activation status of each channel.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	DS2	DS1	DS0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2	DS2	0	R	DMA Channel n Status (n: DMA channel number)
1	DS1	0	R	0: Idle state
0	DS0	0	R	1: Active state

### 17.4.21 Software-Reset Registers (LSRSTR0 to LSRSTR2)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

**Function:** Each register resets DMA channel n.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SRST
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/WC1

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	SRST	0	R/WC1	Software Reset Resets DMA channel n. 0: Writing 0 is ignored. 1: Resets DMA channel n. This register is always read as 0.

**Note:** Writing 1 resets the DMAC regardless of the DMA transfer status. The same registers are reset as when a power-on reset is performed. Accordingly, a software reset should be used only while DMA transfer is not in progress (e.g., during system debugging). To stop operation, forced termination or temporary stop should be specified instead of software reset. In the registers used by all channels in common (DMA transfer end interrupt status register (DINTSR) and DMA transfer end interrupt enable register (DINTMR)), only the bits corresponding to the software-reset channel are initialized.

### 17.4.22 External DMA Data Alignment Control Register (DMALGR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

**Function:** DMALGR specifies whether there is a data alignment conversion in external bus access by the external bus DMAC.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	DMLG2			DMLG1			DMLG0					
					exbwe	exac	exbw	exbwe	exac	exbw	exbwe	exac	exbw			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11 to 0	DMLGn exbwe	0	R/W	Specifies whether there is an EX-BUS data alignment conversion for each DMAC channel (n: DMAC channel number). When the DMAC/DCR setting DMA access bus width is smaller than the external bus width for the relevant DMA area set in LBSC. 0: Access byte lanes fixed 1: Access byte lanes variable
	DMLGn exac	0	R/W	Specifies endian setting when there is alignment conversion with the exbwe bit set to 1 (n: DMAC channel number). 0: Big endian 1: Little endian
	DMLGn exbw	00	R/W	Specifies the unit for data alignment conversion with the exbwe bit set to 1 (n: DMAC channel number). 00: 8 bits 01: 16 bits 10: Setting prohibited 11: Invalid

**Note:** Does not need to be set when the bus width set in LBSC and the DMA access size set in DMAC/DCR are the same. For details, see section 14.6.3 (1), Data Alignment during LBSC-DMAC Access in specifications for LBSC within Bus Bridge.

### 17.4.23 LBSC-DMA AXI Priority Control Register (LBSC-DMASPR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

**Function:** LBSC-DMASPR specifies the AXI bus access priority level for external DMAC.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	SPRR2				SPRR1				SPRR0			
Initial value:	0	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11 to 0	SPRRn	H'8	R/W	Specify the AXI bus access priority level for each DMAC channel (n: DMAC channel number). Priority: H'0 (lowest) to H'F (highest)

**Note:** Since AXI bus access priority level settings relate to priority control for the AXI bus overall, priority levels with other access modules must be confirmed when making settings.

### 17.4.24 Ultra ATA DMA Mode Register (UATMR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

**Function:** UATMR enables the Ultra ATA mode and specifies data alignment in Ultra ATA mode.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	UTDR1		—	—	UTWE1	UTRE1	—	UTSL1		UATM1
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R	R	R/W	R/W	R	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	UTDR0		—	—	UTWE0	UTRE0	—	UTSL0		UATM0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R	R	R/W	R/W	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 26	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
25, 24	UTDR1	00	R/W	[For Ultra ATA port 1] These bits select the external pin for the DREQ signal in the Ultra ATA interface. 00: No external pin is used. 01: The DREQ0 pin in the EX-BUS is used as the DREQ (DMARQ) pin. 10: The DREQ1 pin in the EX-BUS is used as the DREQ (DMARQ) pin. 11: No external pin is used.
23, 22	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
21	UTWE1	0	R/W	[For Ultra ATA port 1] Enables or disables data alignment conversion for write operation in Ultra ATA mode. 0: Disables data alignment conversion for DMA write operation. 1: Enables data alignment conversion for DMA write operation. (Data alignment is in 2-byte units for every 4 bytes of data.)
20	UTRE1	0	R/W	[For Ultra ATA port 1] Enables or disables data alignment conversion for read operation in Ultra ATA mode. 0: Disables data alignment conversion for DMA read operation. 1: Enables data alignment conversion for DMA read operation. (Data alignment is in 2-byte units for every 4 bytes of data.)
19	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
18, 17	UTSL1	00	R/W	[For Ultra ATA port 1] These bits select the external pin for the IORDY (DDMARDY#/DSTROBE) signal in the Ultra ATA interface. 00: No external pin is used. 01: The EX_WAIT0 pin in the EX-BUS is used as the IORDY (DDMARDY#/DSTROBE) pin. 10: The EX_WAIT1 pin in the EX-BUS is used as the IORDY (DDMARDY#/DSTROBE) pin. 11: The EX_WAIT2 pin in the EX-BUS is used as the IORDY (DDMARDY#/DSTROBE) pin.
16	UATM1	0	R/W	[For Ultra ATA port 1] Specifies the Ultra ATA operating mode. 0: Normal DMA mode 1: Ultra ATA DMA mode
15 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9, 8	UTDR0	00	R/W	[For Ultra ATA port 0] These bits select the external pin for the DREQ signal in the Ultra ATA interface. 00: No external pin is used. 01: The DREQ0 pin in the EX-BUS is used as the DREQ (DMARQ) pin. 10: The DREQ1 pin in the EX-BUS is used as the DREQ (DMARQ) pin. 11: No external pin is used.
7, 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5	UTWE0	0	R/W	[For Ultra ATA port 0] Enables or disables data alignment conversion for write operation in Ultra ATA mode. 0: Disables data alignment conversion for DMA write operation. 1: Enables data alignment conversion for DMA write operation. (Data alignment is in 2-byte units for every 4 bytes of data.)
4	UTRE0	0	R/W	[For Ultra ATA port 0] Enables or disables data alignment conversion for read operation in Ultra ATA mode. 0: Disables data alignment conversion for DMA read operation. 1: Enables data alignment conversion for DMA read operation. (Data alignment is in 2-byte units for every 4 bytes of data.)
3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
2, 1	UTSL0	00	R/W	<p>[For Ultra ATA port 0]</p> <p>These bits select the external pin for the IORDY (DDMARDY#/DSTROBE) signal in the Ultra ATA interface.</p> <p>00: No external pin is used.</p> <p>01: The EX_WAIT0 pin in the EX-BUS is used as the IORDY (DDMARDY#/DSTROBE) pin.</p> <p>10: The EX_WAIT1 pin in the EX-BUS is used as the IORDY (DDMARDY#/DSTROBE) pin.</p> <p>11: The EX_WAIT2 pin in the EX-BUS is used as the IORDY (DDMARDY#/DSTROBE) pin.</p>
0	UATM0	0	R/W	<p>[For Ultra ATA port 0]</p> <p>Specifies the Ultra ATA operating mode.</p> <p>0: Normal DMA mode</p> <p>1: Ultra ATA DMA mode</p>

- Notes:
1. For the Ultra ATA DMA operation, refer to section 14, LBSC within Bus Bridge.
  2. When the UTSL bits (external pin selection for the IORDY (DDMARDY#/DSTROBE) signal in the Ultra ATA interface) are set to B'00 (initial value: no external pin is used), the IORDY (DDMARDY#/DSTROBE) signal in the Ultra ATA interface is set to an internally-fixed value and does not work correctly; be sure to select one of EX\_WAIT0 to EX\_WAIT2 in the EX-BUS.
  3. When the UTDR bits (external pin selection for the DREQ signal in the Ultra ATA interface) are set to B'00 or B'11 (no external pin is used), the DREQ signal in the Ultra ATA interface is set to an internally-fixed value and does not work correctly; be sure to select DREQ0 or DREQ1 in the EX-BUS.



**17.4.25 Ultra ATA Write Cycle Setting Register (UATWCR)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

**Function:** UARWCR (a dedicated register of the LBSC-DMAC) specifies the setup and hold clock cycles of the write data relative to the HSTROBE signal in Ultra ATA DMA operation.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	UATWCYC1		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	UATWCYC0		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W

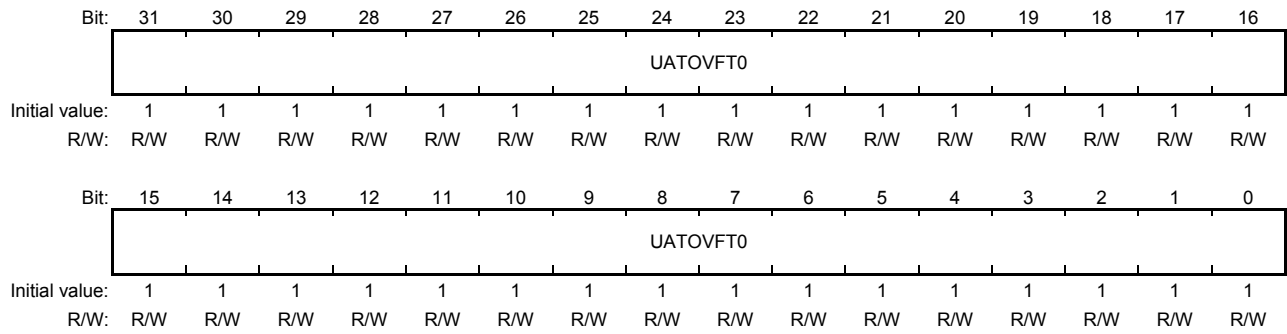
Bit	Bit Name	Initial Value	R/W	Description
31 to 19	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
18 to 16	UATWCYC1	H'0	R/W	[For Ultra ATA port 1] These bits specify the setup and hold clock cycles of the write data relative to the HSTROBE (DIOR#) signal in Ultra ATA DMA operation. H'0: Setup = 1 bus clock cycle, Hold = 1 bus clock cycle H'1: Setup = 2 bus clock cycles, Hold = 1 bus clock cycle H'2: Setup = 2 bus clock cycles, Hold = 2 bus clock cycles H'3: Setup = 3 bus clock cycles, Hold = 2 bus clock cycles H'4: Setup = 3 bus clock cycles, Hold = 3 bus clock cycles H'5: Setup = 4 bus clock cycles, Hold = 3 bus clock cycles H'6: Setup = 4 bus clock cycles, Hold = 4 bus clock cycles H'7: Setup = 5 bus clock cycles, Hold = 4 bus clock cycles
15 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2 to 0	UATWCYC0	H'0	R/W	[For Ultra ATA port 0] These bits specify the setup and hold clock cycles of the write data relative to the HSTROBE (DIOR#) signal in Ultra ATA DMA operation. H'0: Setup = 1 bus clock cycle, Hold = 1 bus clock cycle H'1: Setup = 2 bus clock cycles, Hold = 1 bus clock cycle H'2: Setup = 2 bus clock cycles, Hold = 2 bus clock cycles H'3: Setup = 3 bus clock cycles, Hold = 2 bus clock cycles H'4: Setup = 3 bus clock cycles, Hold = 3 bus clock cycles H'5: Setup = 4 bus clock cycles, Hold = 3 bus clock cycles H'6: Setup = 4 bus clock cycles, Hold = 4 bus clock cycles H'7: Setup = 5 bus clock cycles, Hold = 4 bus clock cycles

Note: For the Ultra ATA DMA operation, refer to section 14, LBSC within Bus Bridge.

**17.4.26 Ultra ATA Timeout Period Setting Register 0 (UATTSR0)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

**Function:** UATTSR0 specifies the period until timeout when communication temporarily stops in Ultra ATA DMA read operation.



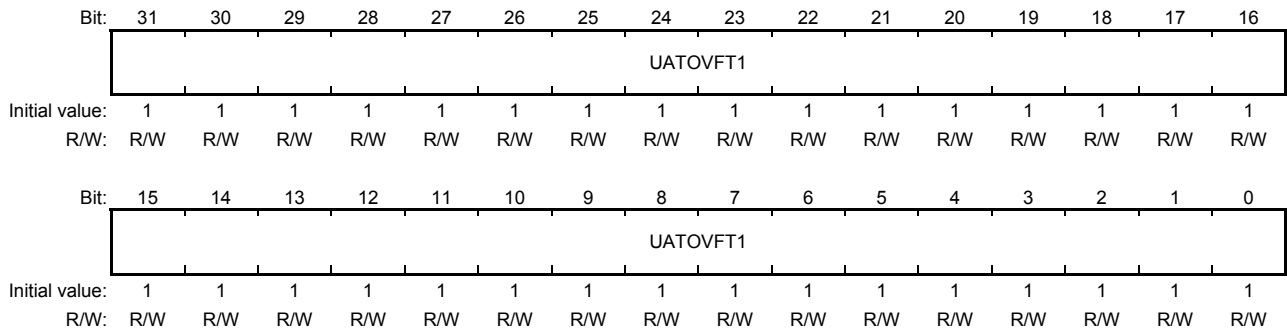
Bit	Bit Name	Initial Value	R/W	Description
31 to 0	UATOVFT0	All 1	R/W	<p>[For Ultra ATA port 0]</p> <p>These bits specify the period until HOST timeout when communication temporarily stops (no change in DSTROBE) in Ultra ATA DMA read operation.</p> <p>Timeout period (ns) = Set value converted to decimal × EX-BUS clock period (ns).</p>

**Note:** For the Ultra ATA DMA operation, refer to section 14, LBSC within Bus Bridge.

**17.4.27 Ultra ATA Timeout Period Setting Register 1 (UATTSR1)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: UATTSR1 specifies the period until timeout when communication temporarily stops in Ultra ATA DMA read operation.



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	UATOVFT1	All 1	R/W	<p>[For Ultra ATA port 1]</p> <p>These bits specify the period until HOST timeout when communication temporarily stops (no change in DSTROBE) in Ultra ATA DMA read operation.</p> <p>Timeout period (ns) = Set value converted to decimal × EX-BUS clock period (ns).</p>

Note: For the Ultra ATA DMA operation, refer to section 14, LBSC within Bus Bridge.

### 17.4.28 Ultra ATA Error Indication Register (UATTER)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

**Function:** UATTER indicates the error status in Ultra ATA DMA operation.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DER1
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PER	DER0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 17	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
16	DER1	0	R/W	[For Ultra ATA port 1] Indicates whether timeout occurs due to a temporary communication stop (no change in DSTROBE) during Ultra ATA DMA read operation. The timeout period is specified through UATTSR1. (When reading) 0: No timeout error has occurred. 1: A timeout error has occurred (interrupt is generated when enabled through UATIER). (When writing) No timeout detection.
15 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	PER	0	R/W	Indicates whether PIO access is executed for the area allocated to the ATA space during Ultra ATA DMA operation. (The PIO access attempted for the area allocated to the ATA space during Ultra ATA DMA operation is ignored.) 0: No PIO access has been executed for the area allocated to the ATA space during Ultra ATA DMA operation. 1: PIO access has been executed for the area allocated to the ATA space during Ultra ATA DMA operation.
0	DER0	0	R/W	[For Ultra ATA port 0] Indicates whether timeout occurs due to a temporary communication stop (no change in DSTROBE) during Ultra ATA DMA read operation. The timeout period is specified through UATTSR0. (When reading) 0: No timeout error has occurred. 1: A timeout error has occurred (interrupt is generated when enabled through UATIER). (When writing) No timeout detection.

**Note:** For the Ultra ATA DMA operation, refer to section 14, LBSC within Bus Bridge.

### 17.4.29 Ultra ATA Error Interrupt Enable Register (UATIER)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

**Function:** UATIER enables interrupts when errors occur in Ultra ATA DMA operation.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DERE1
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PERE	DERE0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

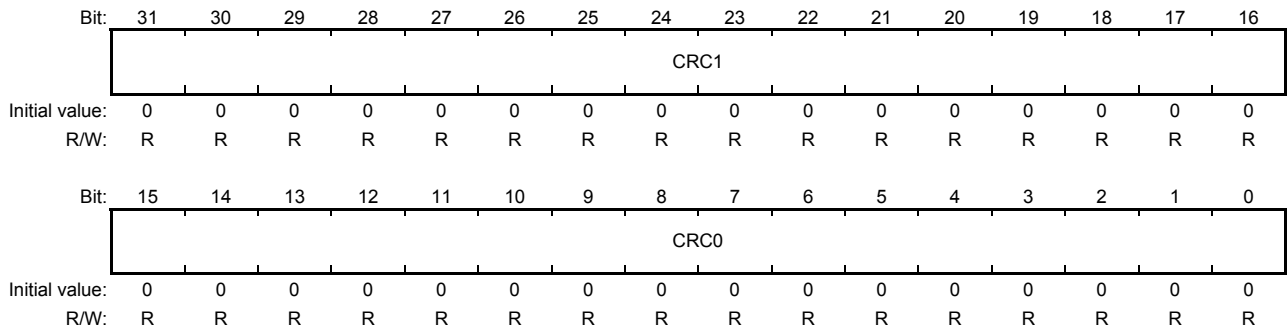
Bit	Bit Name	Initial Value	R/W	Description
31 to 17	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
16	DERE1	0	R/W	[For Ultra ATA port 1] Specifies whether to output an interrupt notification signal while the DER1 bit in UATTER is set to 1. 0: The interrupt notification signal is not output. 1: The interrupt notification signal is output.
15 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	PERE	0	R/W	Specifies whether to output the interrupt notification signal while the PER bit in UATTER is set to 1. 0: The interrupt notification signal is not output. 1: The interrupt notification signal is output.
0	DERE0	0	R/W	[For Ultra ATA port 0] Specifies whether to output an interrupt notification signal while the DER0 bit in UATTER is set to 1. 0: The interrupt notification signal is not output. 1: The interrupt notification signal is output.

**Note:** For the Ultra ATA DMA operation, refer to section 14, LBSC within Bus Bridge.

**17.4.30 Ultra ATA CRC Code Indication Register (UATCRCR)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: UATCRCR indicates the CRC code of the communication data in Ultra ATA DMA operation.



Bit	Bit Name	Initial Value	R/W	Description
31 to 16	CRC1	All 0	R	[For Ultra ATA port 1] These bits indicate the CRC code created from the transfer data in Ultra ATA DMA operation.
15 to 0	CRC0	All 0	R	[For Ultra ATA port 0] These bits indicate the CRC code created from the transfer data in Ultra ATA DMA operation.

Note: For the Ultra ATA DMA operation, refer to section 14, LBSC within Bus Bridge.

## 17.4.31 Ultra ATA Transfer Mode Register (UATTMR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	DTCD1	DTCD0	—	—	—	—	—	—	—	DBG0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 10	—	All 0	R/W	Reserved These bits are always read as 0. The write value should always be 0.
9	DTCD1	0	R/W	[For Ultra ATA port 1] Controls the operating mode for continuation in case of transfer termination operations during DMA operations for Ultra ATA. This bit is used to enable or disable the transfer termination continuation mode. Some existing ATA devices handle the termination of transfer in the same way as a pause. If the DMA transfer count has not been reached, such devices should not abnormally end the transfer even if they acknowledge the termination request, but should restart the transfer upon reception of the next DREQ (DMARQ) signal from the device. This operation is called “transfer termination continuation mode”. 1: Transfer termination continuation mode is disabled. 0: Transfer termination continuation mode is enabled.
8	DTCD0	0	R/W	[For Ultra ATA port 0] Controls the operating mode for continuation in case of transfer termination operations during DMA operations for Ultra ATA. This bit is used to enable or disable the transfer termination continuation mode. Some existing ATA devices handle the termination of transfer in the same way as a pause. If the DMA transfer count has not been reached, such devices should not abnormally end the transfer even if they acknowledge the termination request, but should restart the transfer upon reception of the next DREQ (DMARQ) signal from the device. This operation is called “transfer termination continuation mode”. 1: Transfer termination continuation mode is disabled. 0: Transfer termination continuation mode is enabled.
7 to 1	—	All 0	R/W	Reserved These bits are always read as 0. The write value should always be 0.

---

<b>Bit</b>	<b>Bit Name</b>	<b>Initial Value</b>	<b>R/W</b>	<b>Description</b>
0	DBG0	0	R/W	Test Bit

---

Writing 1 to this bit is prohibited since this is a test bit. This bit is always read as 0. The write value should always be 0.

---

Note: For the Ultra ATA DMA operation, refer to section 14, LBSC within Bus Bridge.



## 17.5 Operation

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

### 17.5.1 DMA Transfer Procedure

The following describes the DMA transfer procedure.

1. Making the initial setting for the DMAC
  - Specify transfer conditions in the DMA control register (DCR).
2. Specifying DMA transfer information
  - Make appropriate settings in the following registers according to the DIP bit setting (input mode: using one information set repeatedly or two information sets alternately) in DCR:
    - DMA source address register (DSAR)
    - DMA destination address register (DDAR)
    - DMA transfer count register (DTCR)
 When the DIP bit specifies that one information set is used repeatedly, make the appropriate settings in DSAR0, DDAR0, and DTCR0.
3. Activating the DMAC
  - Activate the DMAC by setting the DMEN bit in the DMA command register (DCMDR).
4. Reading the specified DMA transfer information
  - The specified DMA transfer information is read from DMA information registers 0 and 1 in that order.
5. Clearing the DMA transfer request
  - The DMA transfer request status signal is cleared.
6. Starting DMA transfer
  - When the auto-request mode is selected as the transfer request mode, transfer automatically starts at the DMAC transfer timing after the transfer information is obtained.
  - When the external request or peripheral request mode is selected, DMA transfer is performed for one bus access cycle when a transfer request is accepted.
  - When the timer request is selected, transfer automatically starts at the intervals specified in the DMAC internal timer after the transfer information is obtained.
7. Issuing an interrupt for the end of a specified number of transfers
  - In single transfer mode, DMA transfer stops when transfer is completed for the specified number of times, and the CPU is notified of the end of transfer through an interrupt.
  - In continuous transfer mode, the CPU is notified of the end of transfer in DMA transfer information units through an interrupt.
  - The interrupt signal is controlled according to the setting in the DMA transfer end interrupt enable register (DINTMR).
  - RZ/G1H and RZ/G1M have a possibility that the DMA transfer end interrupt reaches to CPU in advance of completion of the last write access if the destination address is in the DDR3 area. In order to prevent from reading the value before the last write access is completed, a dummy DMA transfer with SYS-DMAC is required.
  - The source address of the dummy SYS-DMAC transfer can be any address.
  - The destination address of the dummy SYS-DMAC transfer can be any DDR3 area address in DDR3 64-bit mode.
  - In case of DDR3 32-bit dual channel mode, the destination address of the dummy SYS-DMAC transfer must be an address in the same DDR3 channel as the destination address of last transfer of LBSC-DMAC transfer.
  - The transfer count and transfer data size of the dummy SYS-DMAC transfer can be the minimum value.
  - RZ/G1N, and RZ/G1E don't have this problem.
8. Reading the next DMA transfer information (continuous transfer mode)

If the next DMA transfer request is specified, the information of the transfer is read and data is transferred in the same way as described in step 6.

If no additional DMA transfer request is specified (DRSTS = 0), the continuous DMA transfer mode is terminated when DQSTS = 1, or the next DMA transfer request is waited for when DQSTS = 0.

9. Adding DMA transfer information (continuous transfer mode)

If new DMA transfer information should be added, specify the information in the DMA transfer information set that will be used for the next transfer (the next DMA transfer information set can be checked with the NDP1 and NDP0 bits in the DMA status register (DSTSR)).

If no DMA transfer information should be added, write 1 to the DQEND bit in the DMA command register (DCMDR) to terminate the continuous transfer mode.

Note: Actually, the source bus and destination bus operate independently.

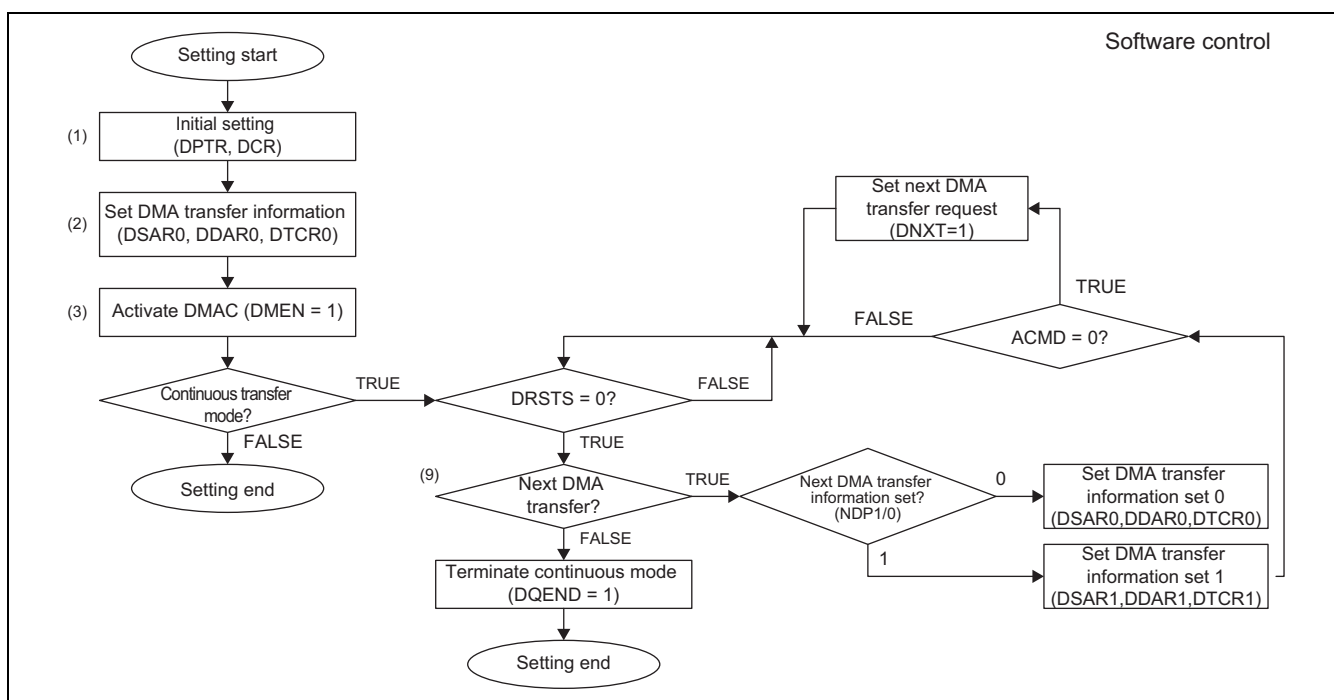


Figure 17.2 DMA Transfer Flowchart (1)

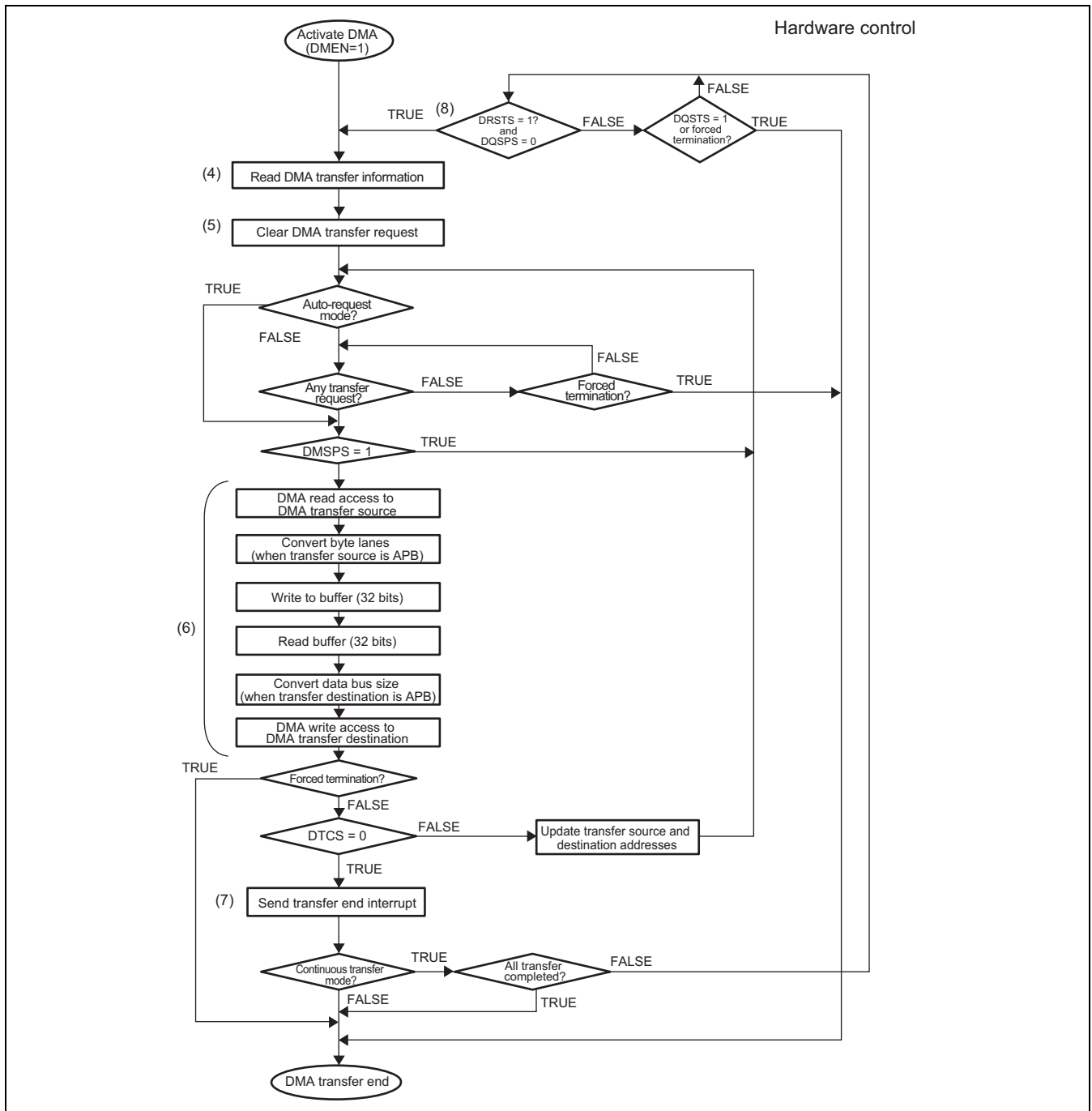


Figure 17.3 DMA Transfer Flowchart (2)

### 17.5.2 Continuous DMA Transfer Operation

The following shows the relationship between addition of DMA transfer information by software and DMA transfer information read and data transfer operation by hardware, which are described in step 9 in section 17.5.1, DMA Transfer Procedure. Figures 17.4 and 17.5 show transfer using DMA information set 0 repeatedly, and Figures 17.6 and 17.7 show transfer using DMA information sets 0 and 1 alternately.

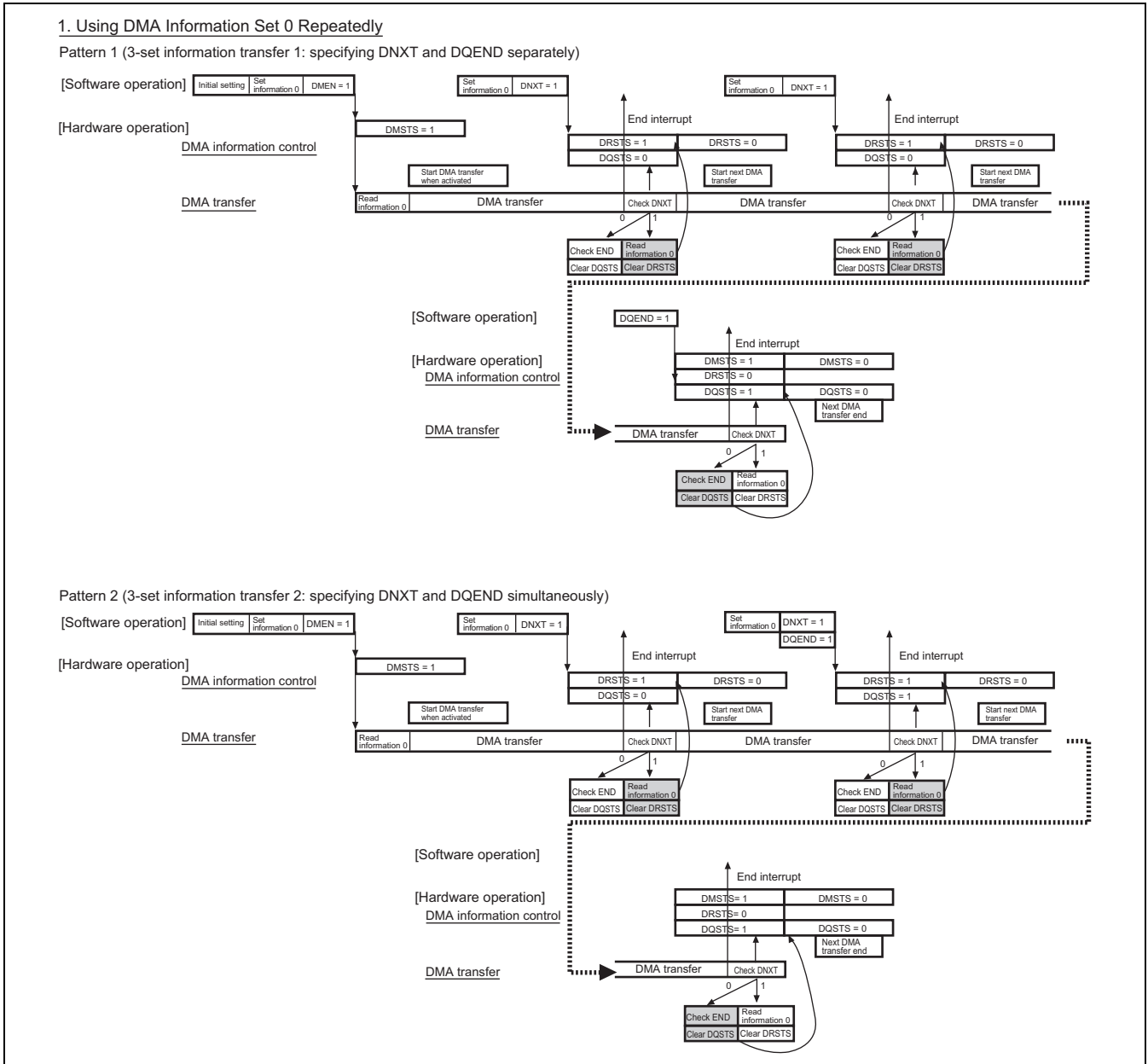


Figure 17.4 Transfer Using DMA Information Set 0 Repeatedly (1)

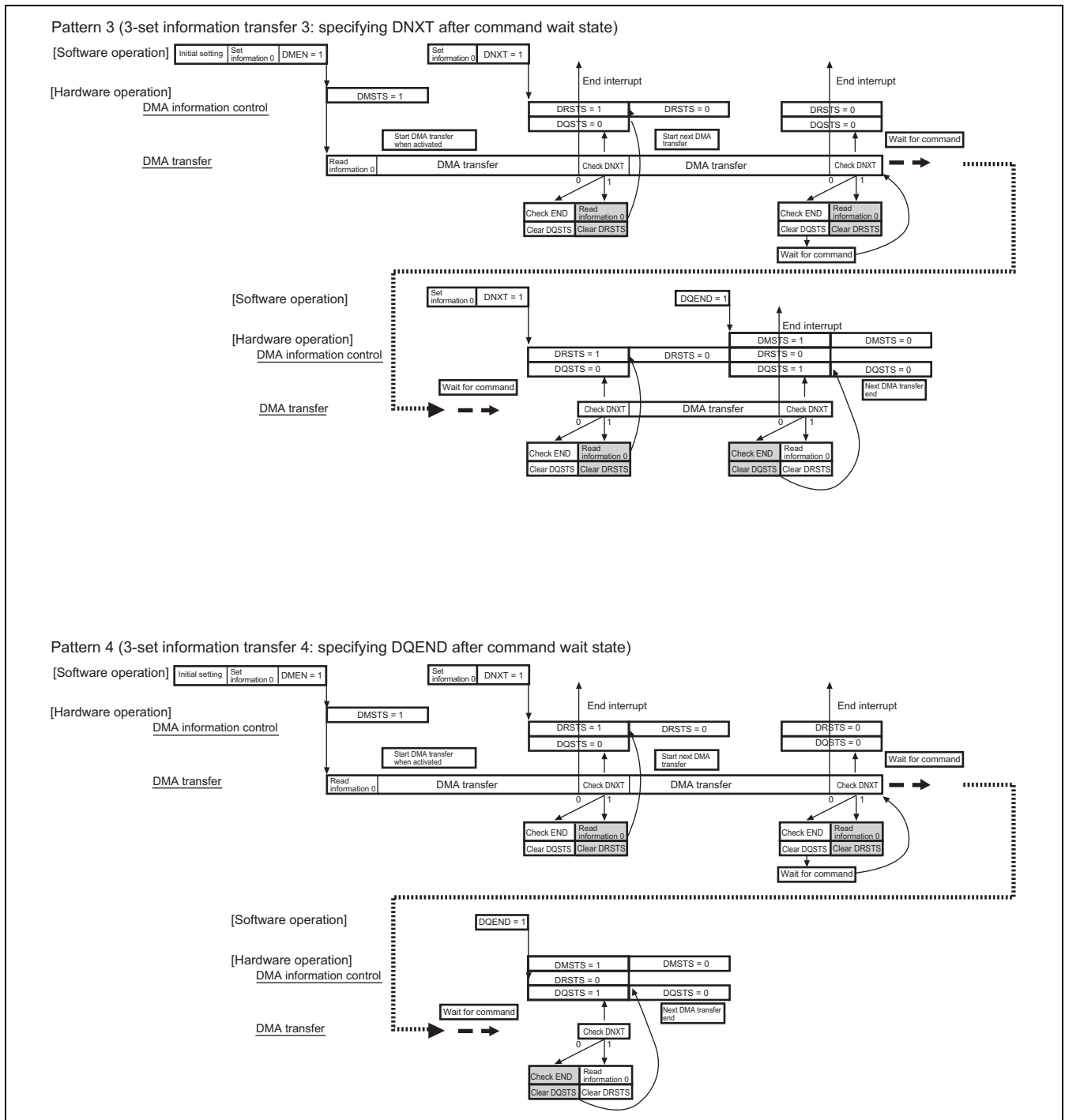
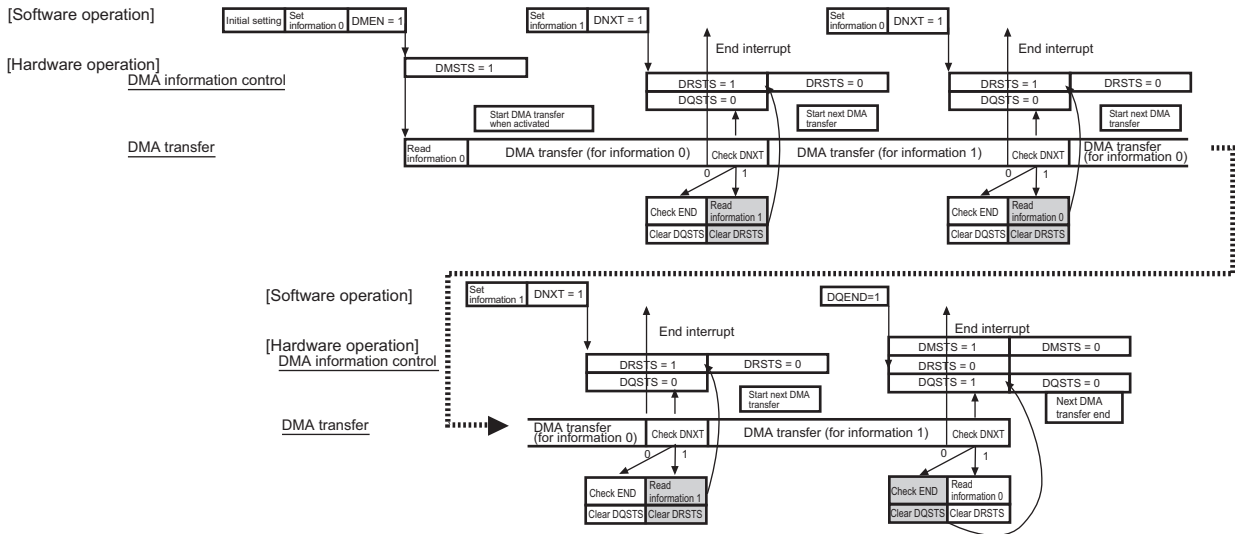


Figure 17.5 Using DMA Information Set 0 Repeatedly (2)

2. Using DMA Information Sets 0 and 1 Alternately

Pattern 1 (4-set information transfer 1: specifying DMEN, DNXT, and DQEND separately)



Pattern 2 (4-set information transfer 2: specifying DNXT and DQEND simultaneously)

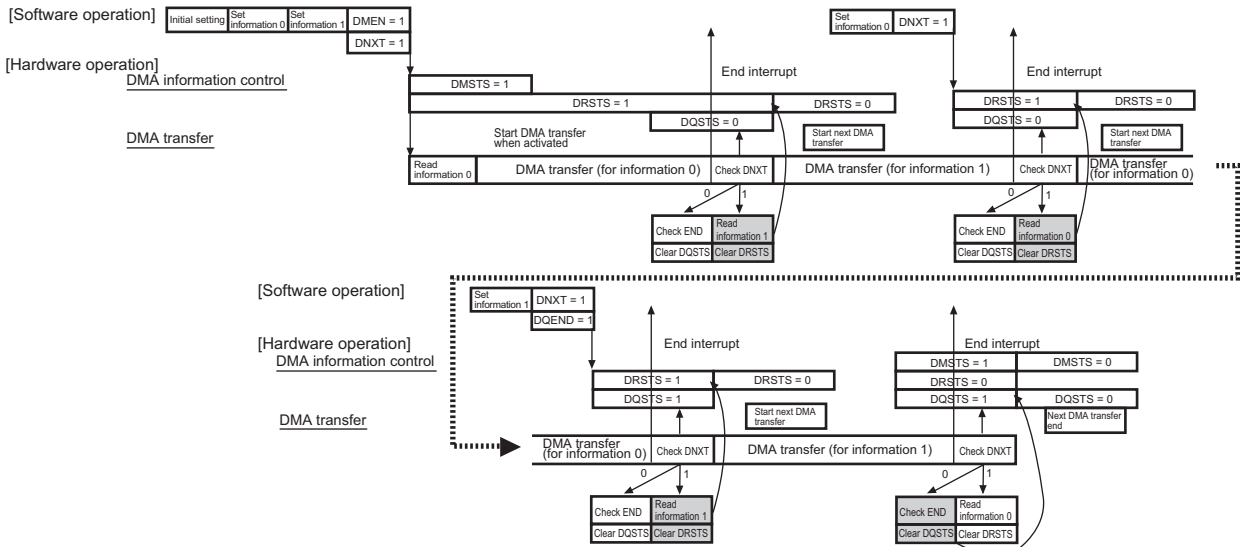


Figure 17.6 Using DMA Information Sets 0 and 1 Alternately (1)

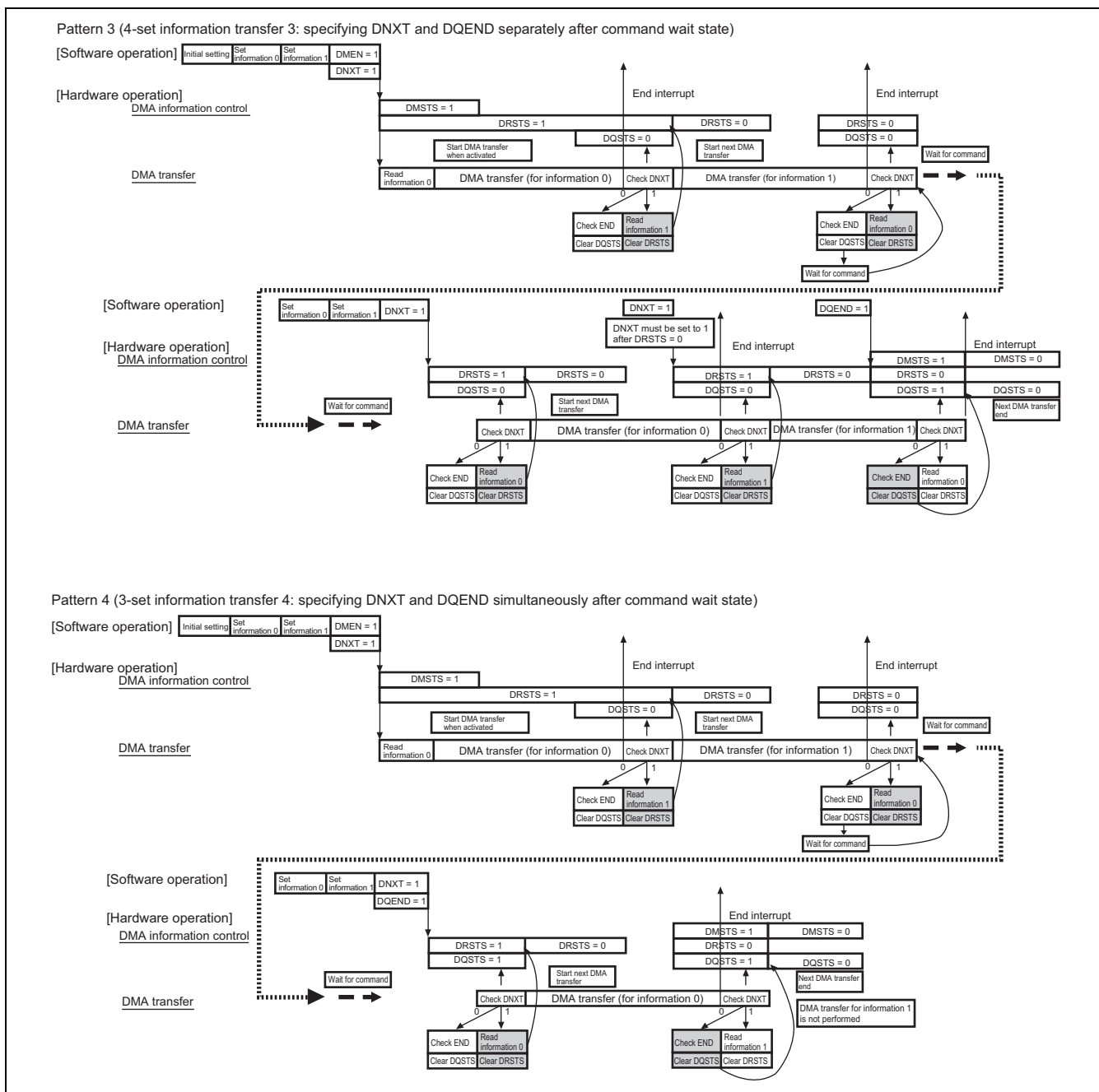


Figure 17.7 Using DMA Information Sets 0 and 1 Alternately (2)

### 17.5.3 Packing Data Read from Peripheral or External Module

Writing 1 to the PKMD bit when making necessary settings in the DMA control register (DCR) in the usual DMA activation procedure enables packing of data read from a peripheral or external module and then writing the data to memory (the AXI bus). Packing size can be specified to either 4 bytes or byte units shown in \* in the DCR register description by the SWMD bit in DCR. However, when the transfer destination on the AXI side is memory (DDR-DRAM), packing size in a byte unit shown in \* in the DCR register description is recommended in order to use memory and the AXI efficiently. The data packing of an access size when SWMD in DCR = 0 cannot be specified for the LBSC-DMAC (for details on access size in each channel, see \* in the DCR register description), because size of data written from peripheral modules connected to the APB to registers is equal to or less than 4 bytes when the transfer destination on the AXI side is one of the units connected to the APB.

During the packing operation, even if the DMAC holds data less than the specified packing size when the DMAC completes the specified count of transfer, the DMAC writes fetched data to memory and indicates the end of DMA transfer by setting the DTEn bit in the DMA transfer end interrupt status register (DINTSR). If the peripheral or external module completes a DMA request before the specified transfer count is reached, DMA transfer can be terminated by writing 1 to the BDOUT bit in the DMA command register (DCMDR). In this case, if data which is being packed remains in the DMAC, the DMAC writes the data to memory (AXI). The DTE[n] bit in the DMA transfer end interrupt status register (DINTSR) is set and a transfer end interrupt is generated. Note that zero padding does not occur during write to memory. If no data remains in the DMAC, the DMAC terminates DMA transfer without accessing memory and generates a transfer end interrupt in the same way as when data remains in the DMAC.

When transfer is terminated by the BDOUT bit setting in continuous transfer mode, the DMAC transfers the next DMA information if the next DMA information transfer is requested through the DNXT bit in DCMDR, and then terminates DMA transfer in the continuous transfer mode termination procedure. In this mode, DMA requests (DREQ) from peripheral or external modules are masked (not accepted) before a transfer end interrupt occurs after the BDOUT bit is set to 1.

### 17.5.4 Limitations on Packing of Data Read from Peripheral or External Module

The transfer count is specified in DMA transfer count registers 0 and 1 (DTCR0 and DTCR1) in the DMAC.

If DMA transfer from a peripheral or external module is completed before the specified transfer count is reached, the DMAC cannot distinguish whether data is being transferred or the transfer has been completed, and data of less than packing size may remain in the DMAC internal buffer. When the size of remaining data is the same as the specified packing size, the data is transferred to memory.

Data remaining in the DMAC internal buffer is written to memory through a forced write executed by setting the BDOUT bit in the DMA command register (DCMDR). (Zero padding does not occur because the transfer destination is memory. For example, if 3-byte data remains in the DMAC un-transferred to memory, the 3-byte data is written to the memory as is.)

A forced write can be triggered by a communication completion interrupt from a peripheral or external module. Note that whether DMA transfer from the peripheral or external module is completed when the communication end interrupt occurs depends on the specifications of the peripheral or external module. Accordingly, check the specifications of the module before executing a forced write.



### 17.5.5 Notification of the End of DMA Transfer

The DMAC notifies the CPU of the end of transfer by outputting transfer end interrupt signal (a level signal) through INTC (SYS) when transfer is completed for the transfer count specified in DMA transfer information in single transfer mode. In continuous transfer mode, the DMAC outputs transfer end interrupt signal every time transfer is completed for the transfer count specified in one DMA transfer information set.

The transfer end interrupt signal is controlled according to the setting in the DMA transfer end interrupt enable register (DINTMR). Writing 1 to the DMA transfer end interrupt status clear register (DINTCR) clears the transfer end interrupt signal.

### 17.5.6 DMA Transfer Stop, and Resume Procedures

This section describes the procedures for stopping, and resuming DMA transfer.

- To stop (cancel) DMA transfer during operation

Step	Overview	Register Operation	Operation after Register Write
1 ↓	Specify forced termination for DMAC.	Write 1 to DMSTP of DSTPR in DMAC.	The DMAC stops DMA transfer as soon as the current DMA bus cycle is completed, and then enters the idle state. Unfinished transfer data remaining in the buffer is discarded. The registers retain the values. No end interrupt is issued.
2 ↓	Check that the DMAC has entered the idle state.	If DMSTS of DSTSR in DMAC is 0, the DMAC is in the idle state.	—
3	Specify forced termination for external devices.	(Depends on the external devices.)	The external devices stop sending DMA requests.

Note: Step 2 can be done after step 3.

- To temporarily stop (pause) DMA transfer during operation and then resume it

Step	Overview	Register Operation	Operation after Register Write
1 ↓	Specify temporary stop for DMAC.	Write 1 to DMSPD of DCMDR in DMAC.	The DMAC temporarily stops DMA transfer as soon as the current DMA bus cycle is completed. The DMAC retains its internal status, including unfinished transfer data remaining in the buffer, without change.
2 ↓	Check that the DMAC has entered the temporary stop state.	If DMSPS of DSTSR in DMAC is 1, the DMAC is in the suspended state.	—
3 ↓	A certain period of time has elapsed (the LBSC may detect a DREQ signal from an external device during this period, but the DMAC keeps the temporary stop and the external devices continue to wait for DMA transfer).		
4	Specify cancel of temporary stop (resume transfer).	Write 1 to DMSPC of DCMDR in DMAC.	The paused state is canceled, and the DMAC resumes its operation with the DMA transfer for the DREQ detected by the LBSC.

Note: Step 2 can be done between steps 3 and 4.

- To temporarily stop (pause) DMA transfer during operation and then terminate (cancel) operation

Step	Overview	Register Operation	Operation after Register Write
1 ↓	Specify temporary stop for DMAC.	Write 1 to DMSPD of DCMDR in DMAC.	The DMAC temporarily stops DMA transfer as soon as the current DMA bus cycle is completed.  The DMAC retains its internal status, including unfinished transfer data remaining in the buffer, without change.
2 ↓	Check that the DMAC has entered the temporary stop state.	If DMSPS of DSTSR in DMAC is 1, the DMAC is in the suspended state.	—
3 ↓	A certain period of time has elapsed (the LBSC may detect a DREQ signal from an external device during this period, but the DMAC keeps the temporary stop and the external devices continue to wait for DMA transfer).		
4 ↓	Specify forced termination for DMAC.	Write 1 to DMSTP of DSTPR in DMAC.	The DMAC exits the temporary stop state and enters the idle state.  Unfinished transfer data remaining in the buffer is discarded.  The registers retain the values. No end interrupt is issued.
5 ↓	Check that the DMAC has entered the idle state.	If DMSTS of DSTSR in DMAC is 0, the DMAC is in the idle state.	—
6	Specify forced termination for external devices.	(Depends on the external devices.)	The external devices stop sending DMA requests.

- Notes:
- Step 2 can be done between steps 3 and 4.
  - Step 5 can be done after step 6.

### 17.5.7 Data Alignment in AXI Bus Interface

The AXI bus is always accessed through a handshake using an access request and a request acknowledge. Alignment of data read or written during the access to memory through the AXI bus is always converted.

When the DTAMD bit in the DMA control register (DCR) is 0, the AXI bus data alignment is converted according to the endian mode signal (DMAC input signal: little) and the peripheral data bus width (the SPDS1 and SPDS0 bits or DPDS1 and DPDS0 bits in DCR). When the DTAMD bit in DCR is 1, data alignment is converted according to the DTAC, DTAU, and DTAU1 bit settings in DCR.

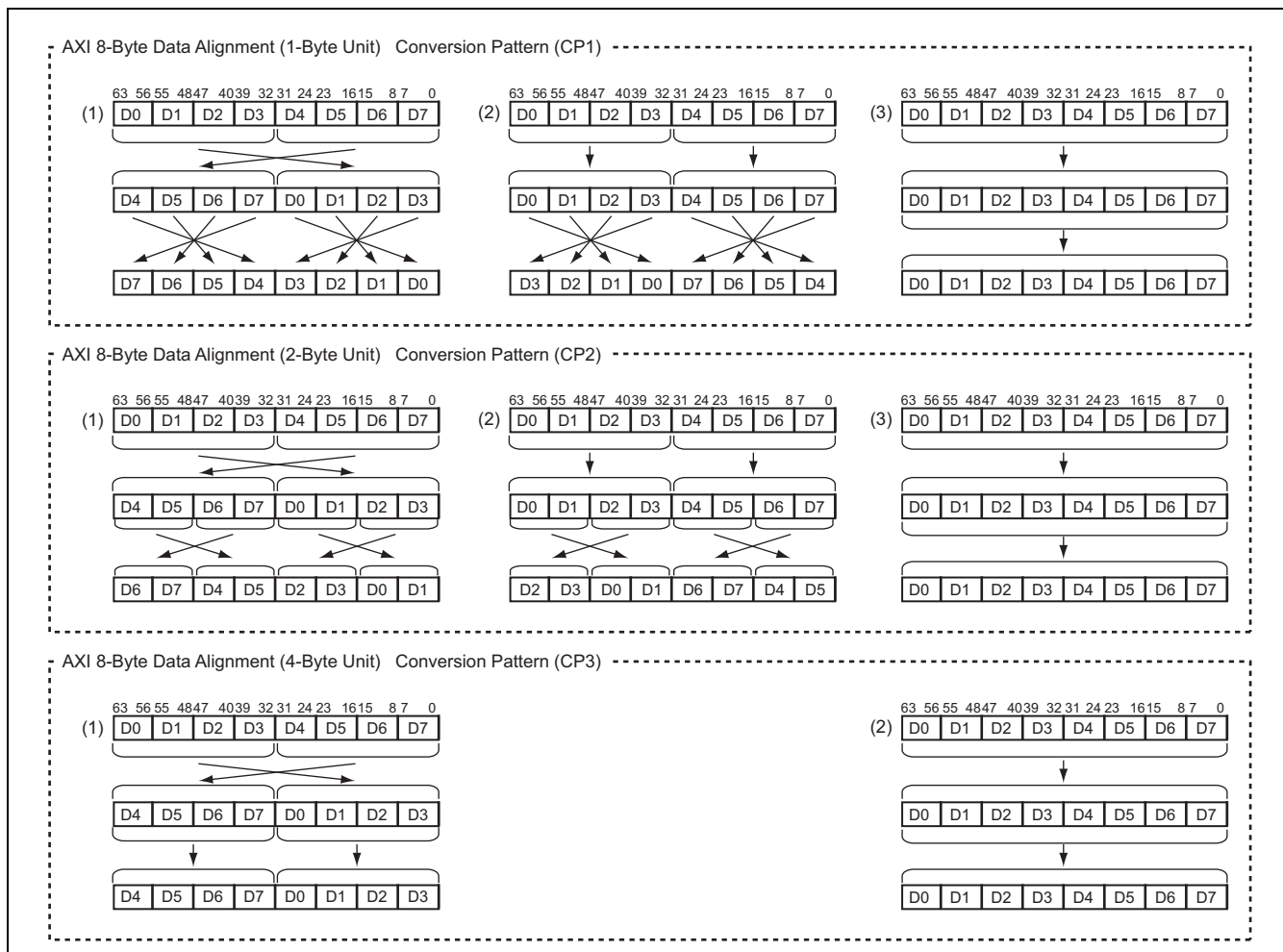
The following table shows the AXI bus data alignment control according to the DTAMD bit in DCR, endian mode signal (DMAC input signal: little), peripheral data bus width (the SPDS1 and SPDS0 bits or DPDS1 and DPDS0 bits in DCR), and DTAC, DTAU, and DTAU1 bits in DCR.

**Table 17.2 Data Alignment Control According to Bit and Signal Settings**

No.	DTAMD	little (MD[8])	PDS [1:0]	DTAC	DTAU	DTAU1	Data Alignment of 4 Bytes	Unit for 4-Byte Data Alignment	8-Byte Data Alignment in 4-Byte Unit	Conversion Pattern	Remarks
1	0	0	00 (8 bits)	*	*	*	Not controlled	8 bits	Not controlled	CP1 (3)	Standard conversion (Software must specify only PDS[1:0])
2	0	0	01 (16 bits)	*	*	*	Not controlled	16 bits	Not controlled	CP2 (3)	
3	0	0	10 (32 bits)	*	*	*	Not controlled	8 bits	Not controlled	CP3 (2)	
4	0	1	00 (8 bits)	*	*	*	Controlled	8 bits	Controlled	CP1 (1)	
5	0	1	01 (16 bits)	*	*	*	Controlled	16 bits	Controlled	CP2 (1)	
6	0	1	10 (32 bits)	*	*	*	Not controlled	8 bits	Controlled	CP3 (1)	
7	1	*	*	0	0	0	Not controlled	8 bits	Not controlled	CP1 (3)	Special conversion (Software must specify the alignment mode)
8	1	*	*	0	0	1	Not controlled	8 bits	Controlled	CP3 (1)	
9	1	*	*	0	1	0	Not controlled	16 bits	Not controlled	CP2 (3)	
10	1	*	*	0	1	1	Not controlled	16 bits	Controlled	CP3 (1)	
11	1	*	*	1	0	0	Controlled	8 bits	Not controlled	CP1 (2)	
12	1	*	*	1	0	1	Controlled	8 bits	Controlled	CP1 (1)	
13	1	*	*	1	1	0	Controlled	16 bits	Not controlled	CP2 (2)	
14	1	*	*	1	1	1	Controlled	16 bits	Controlled	CP2 (1)	

\*: Don't care

The following shows data alignment conversion in the DMAC. Conversion pattern numbers in the table above correspond to the conversion numbers below.



**Figure 17.8 Data Alignment Conversion in the DMAC**

**17.5.8 Data Alignment in EX-BUS Interface**

Setting the DMALGR register in the DMAC allows variable alignment mode for the external bus access as the mode of alignment conversion. For the CPU operation in a variable alignment mode, see section 14.6.3 (1), Data Alignment during LBSC-DMAC Access, in section 14, LBSC within Bus Bridge.

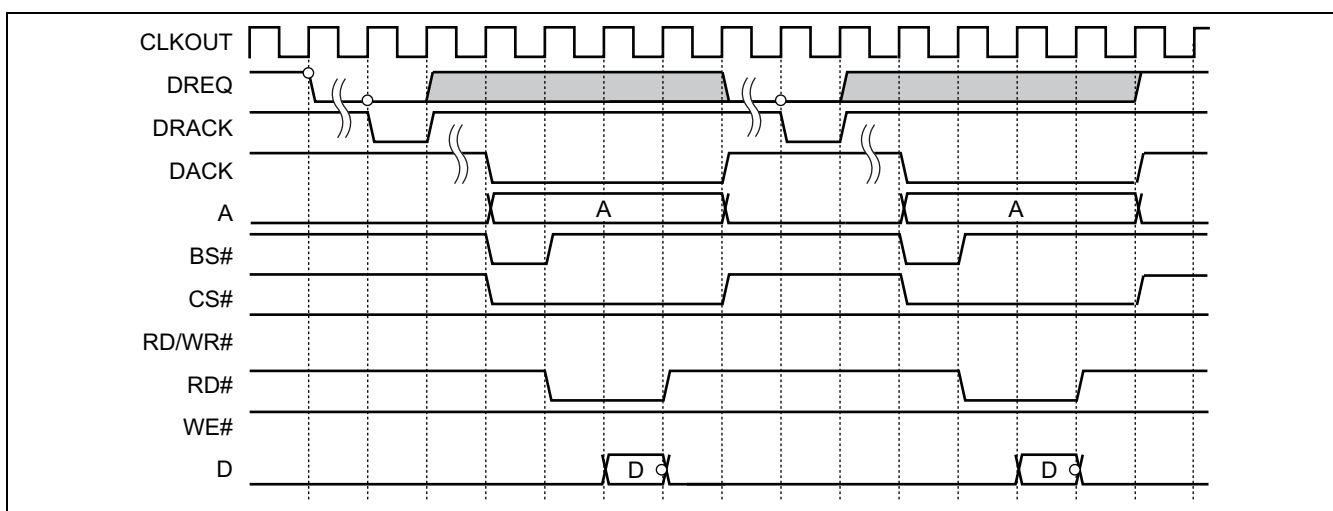
**17.5.9 Timing Charts**

Timing charts are given for DMA operation during the external SRAM bus operation. In the timing charts, the DREQ, DRACK, and DACK signal polarity is indicated as negative; however, these polarity settings, assertion of either the CS# or DACK signal, and switching DREQ to a level signal or to edge detection mode, can be set. In all cases these settings should be made using LBSC internal registers.

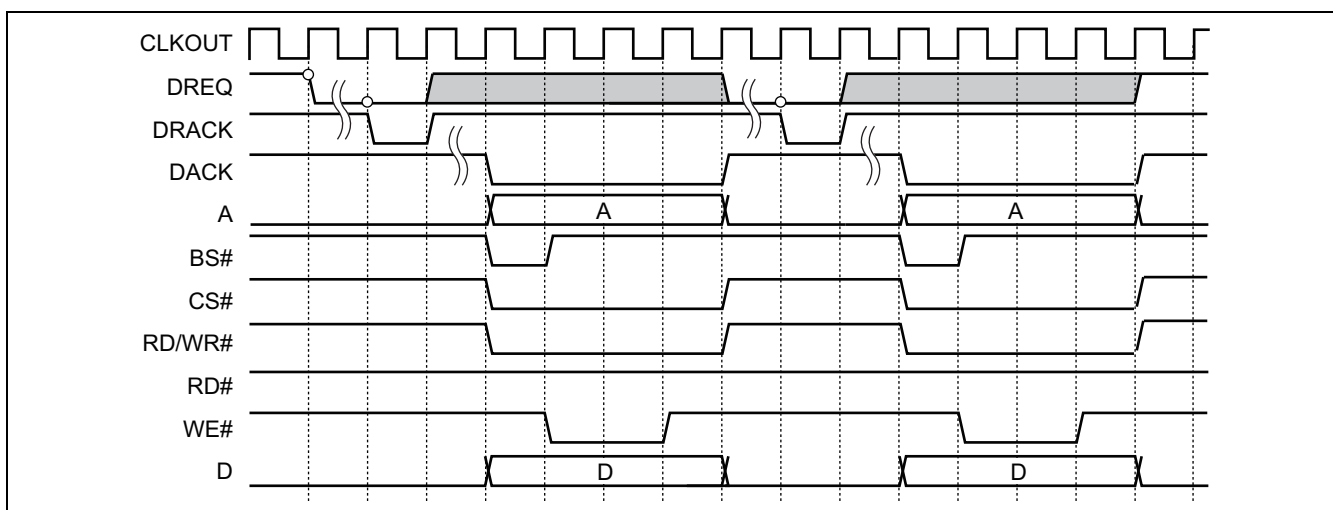
**(1) EX-BUS DMA single-read/write operation**

In SRAM bus operation, upon receiving a DREQ signal a DRACK is asserted to send notification of detection of a DMA request. There are no DRACK signals for other than LBSC-DMAC channel 0. In these cases, the device which is the DMA request source must negate the DREQ signal until the end of the bus operation through the DACK signal indicating that the DMA transfer has actually started. The DMAC starts the next DREQ sampling from the next clock cycle after the end of the DMA bus transfer (LBSC-DMAC DMA request mask control register (DRMSKR) settings can be used to delay the start of the next sampling), and upon detection, starts the next DMA transfer bus operation.

In DMA single read and write operations, the number of clock cycles from CS# assertion to RD# (or WE#) signal assertion, the number of RD# (or WE#) pulse clock cycles, and the number of clock cycles from RD# (or WE#) negation to CS# negation, can be set through the LBSC internal register. During the period of RD# (or WE#) assertion, if a WAIT signal from the DMA request source is detected, then during the WAIT assertion period, the RD# (or WE#) pulse width is extended. With respect to specification of WAIT signal sampling also, the internal LBSC register should be used.



**Figure 17.9 External Bus DMA Read Operation (SRAM Bus Single Read)**

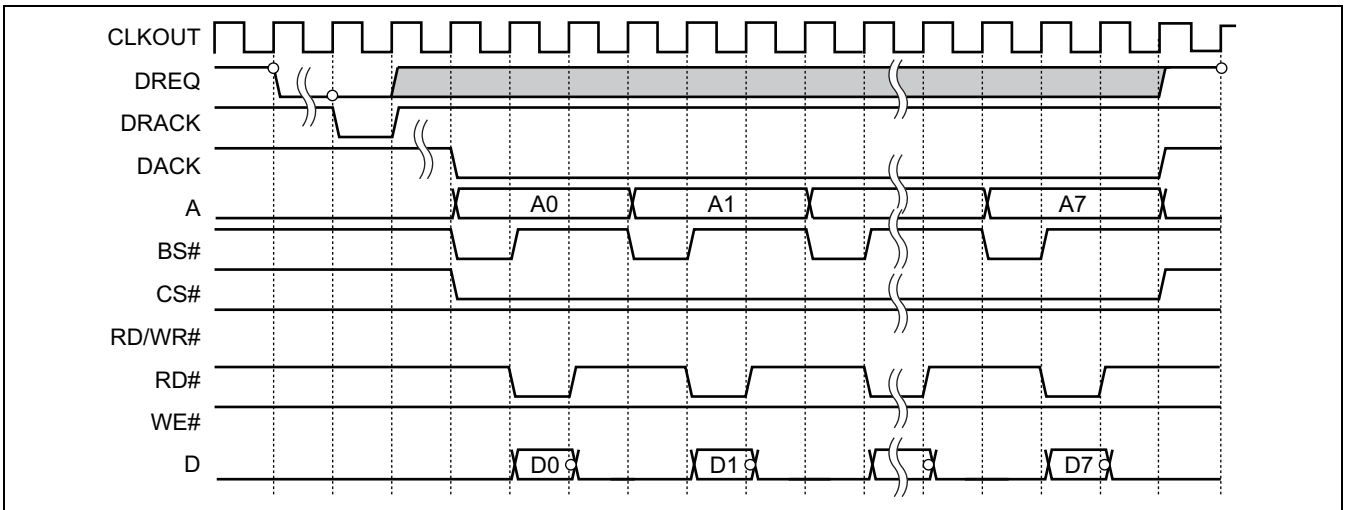


**Figure 17.10 External Bus DMA Write Operation (SRAM Bus Single Write)**

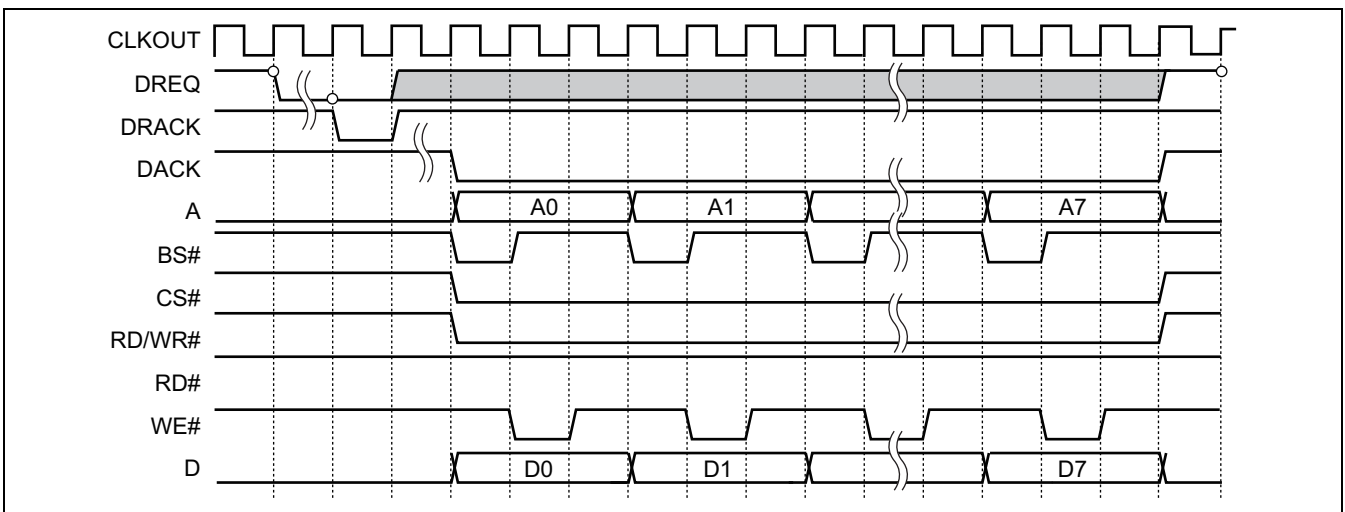
**(2) EX-BUS DMA 8-burst read/write operation**

In DMA 8-burst operation, 8-burst bus transfer operation is performed upon detection of a single DREQ signal. In SRAM bus operation, upon receiving a DREQ signal a DRACK is asserted to send notification of detection of a DMA request. There are no DRACK signals for other than LBSC-DMAC channel 0, so that in these cases the device which is the DMA request source must negate the DREQ signal until the end of the 8-burst bus operation through the DACK signal indicating that the DMA transfer has actually started. The DMAC starts the next DREQ sampling from the next clock cycle after the end of the DMA bus operation (LBSC-DMAC DMA request mask control register (DRMSKR) settings can be used to delay the start of the next sampling), and upon detection, starts 8-burst bus operation for the next DMA transfer.

Also in DMA 8-burst operations, the number of clock cycles from CS# assertion to RD# (or WE#) signal assertion, the number of RD# (or WE#) pulse clock cycles, and the number of clock cycles from RD# (or WE#) negation to CS# negation, can be set through the LBSC internal register. During the period of RD# (or WE#) assertion, if a WAIT signal from the DMA request source is detected, then during the WAIT assertion period, the RD# (or WE#) pulse width can be extended. With respect to WAIT signal control also, the internal LBSC register should be used.



**Figure 17.11 External Bus DMA Read Operation (SRAM Bus Burst Read)**



**Figure 17.12 External Bus DMA Write Operation (SRAM Bus Burst Write)**

## 18. Booting

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

### 18.1 Overview

In this product, the levels on the MD7 and MD6 pins can be set to select the master boot processor. When the Cortex-A7 or Cortex-A15 is selected as the master boot processor, the levels on the MD[3:1] pins can select booting up from the serial flash ROM connected to the QSPI.

### 18.2 Features

- The levels on the MD7 and MD6 pins can select the Cortex-A7\*<sup>1</sup>, or Cortex-A15\*<sup>1</sup> as the master boot processor.
- The external boot device can be selected as either external ROM (area 0) or on-chip ROM by the levels on the MD3 to MD1 pins.
- Booting from the serial flash ROM connected to the QSPI is supported.
  - The master boot processor (if this is the Cortex-A15\*<sup>1</sup> or Cortex-A7\*<sup>1</sup>) executes the instructions in the on-chip ROM, and the specified amount of data are transferred from the serial flash ROM to the on-chip RAM at the specified QSPI clock frequency. After transfer, execution jumps to the top address of the on-chip RAM.
  - After 16 or 4 Kbytes of code are transferred to the on-chip RAM at 39 MHz, execution jumps to the top address of the on-chip RAM.
  - After 16 Kbytes of code are transferred to the on-chip RAM at 48.75 MHz, execution jumps to the top address of the on-chip RAM.

Notes: 1. The presence of CPU cores depends on the product. For details, see the notes under Table 18.1.

### 18.3 Input/Output Pins

**Table 18.1 Mode Pin Configuration**

Name	Pin Name	I/O	Function	RZ/G Series Products							
				RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E				
Mode pin	MD7 and MD6	Input	Select a master boot processor.	<b>MD7</b>	<b>MD6</b>	<b>Description</b>					
				0	0	Booted through CPU0 in Cortex-A15* <sup>1</sup> .	√	√	√	—	
				0	1	Booted through CPU0 in Cortex-A7* <sup>1</sup> .	√	—	—	√	
				1	0	Reserved	√	√	√	√	
				1	1	Setting prohibited	√	√	√	√	
Mode pin	MD3 to MD1	Input	Select a boot device.	<b>MD3</b>	<b>MD2</b>	<b>MD1</b>	<b>Description</b>				
				0	0	0	External ROM boot (area 0)	√	√	√	√
				0	0	1	Reserved	√	√	√	√
				0	1	0	Serial flash ROM boot via QSPI; 16 Kbytes transferred at 48.75 MHz	√	√	√	√
				0	1	1	Reserved	√	√	√	√
				1	0	0	Serial flash ROM boot via QSPI; 16 Kbytes transferred at 39 MHz	√	√	√	√
				1	0	1	Serial flash ROM boot via QSPI; 16 Kbytes transferred at 78 MHz	—	—	—	√
				1	1	0	Serial flash ROM boot via QSPI; 4 Kbytes transferred at 39 MHz	√	√	√	√
				1	1	1	Reserved	√	√	√	√

Notes: 1. The RZ/G1H, RZ/G1M, and RZ/G1N include a Cortex-A15. The RZ/G1H and RZ/G1E include a Cortex-A7.



## 18.4 Operation

RZ/G1H	RZ/G1N
RZ/G1M	RZ/G1E

### 18.4.1 Booting Up of RZ/G1H

Figures 18.1 illustrate the flow of booting up.

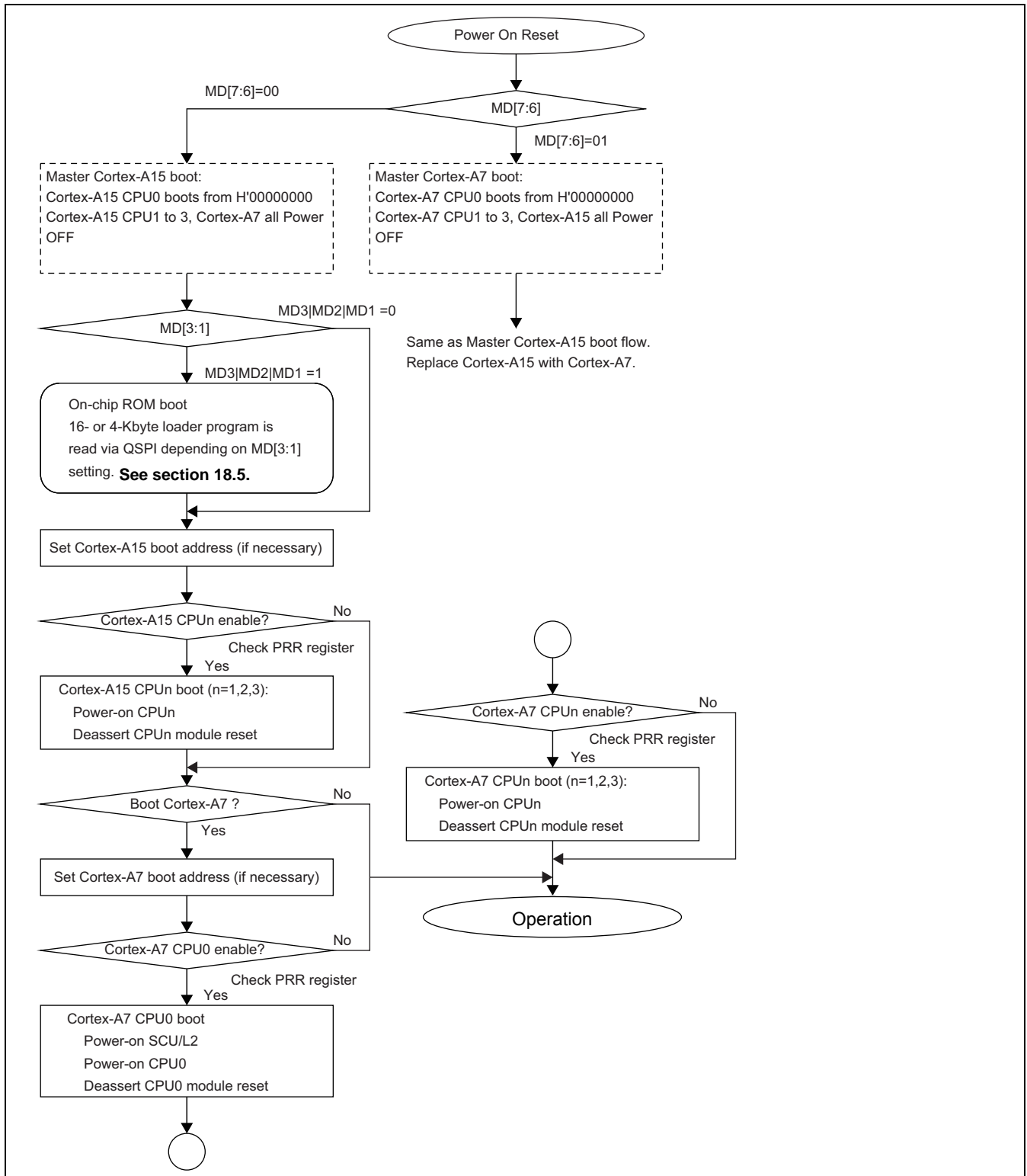


Figure 18.1 Flow of Booting Up

### 18.4.2 Booting Up of RZ/G1M and RZ/G1N

Figure 18.2 illustrate the flow of booting up.

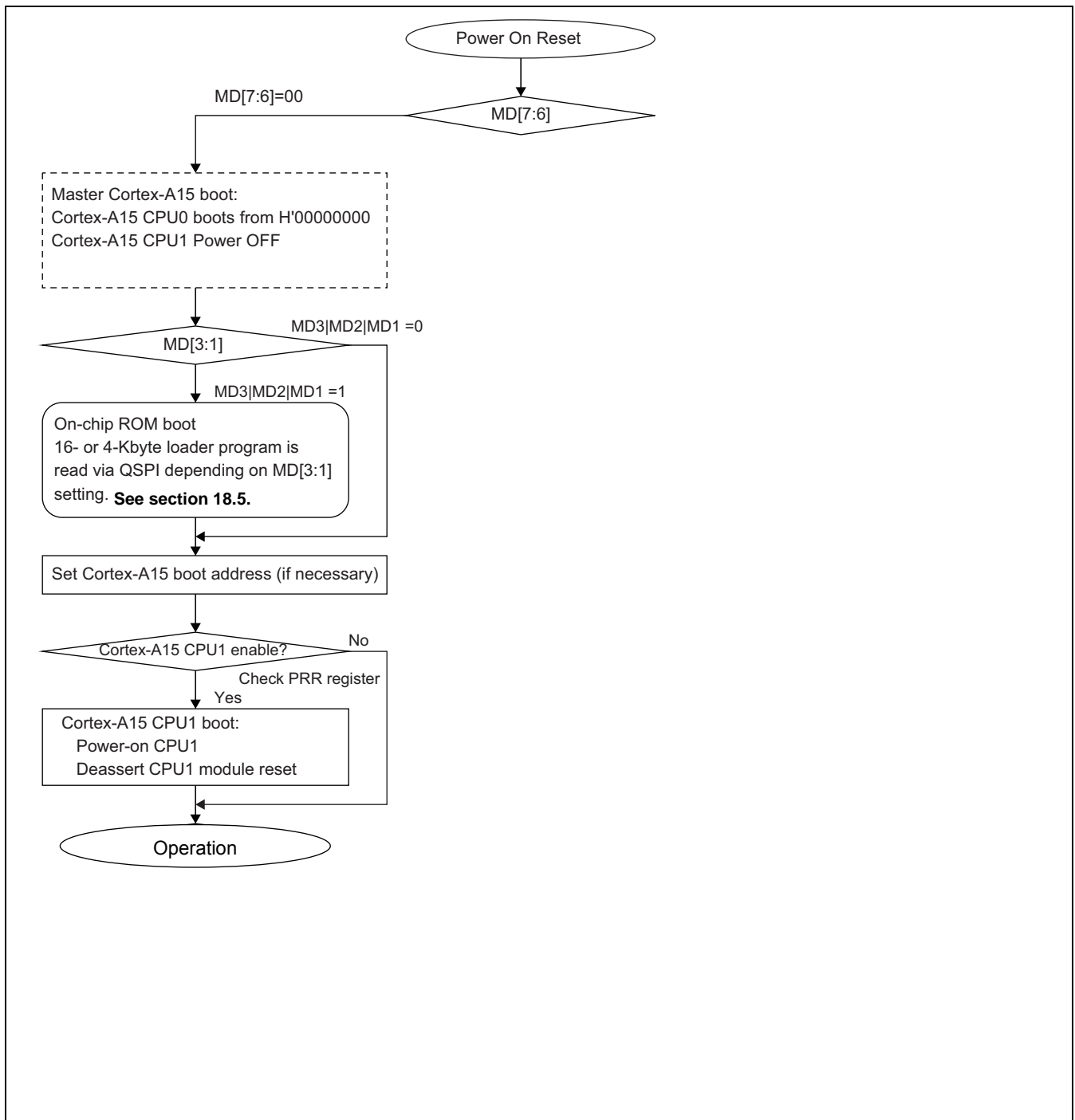


Figure 18.2 Flow of Booting Up

### 18.4.3 Booting Up of RZ/G1E

Figure 18.3 illustrate the flow of booting up.

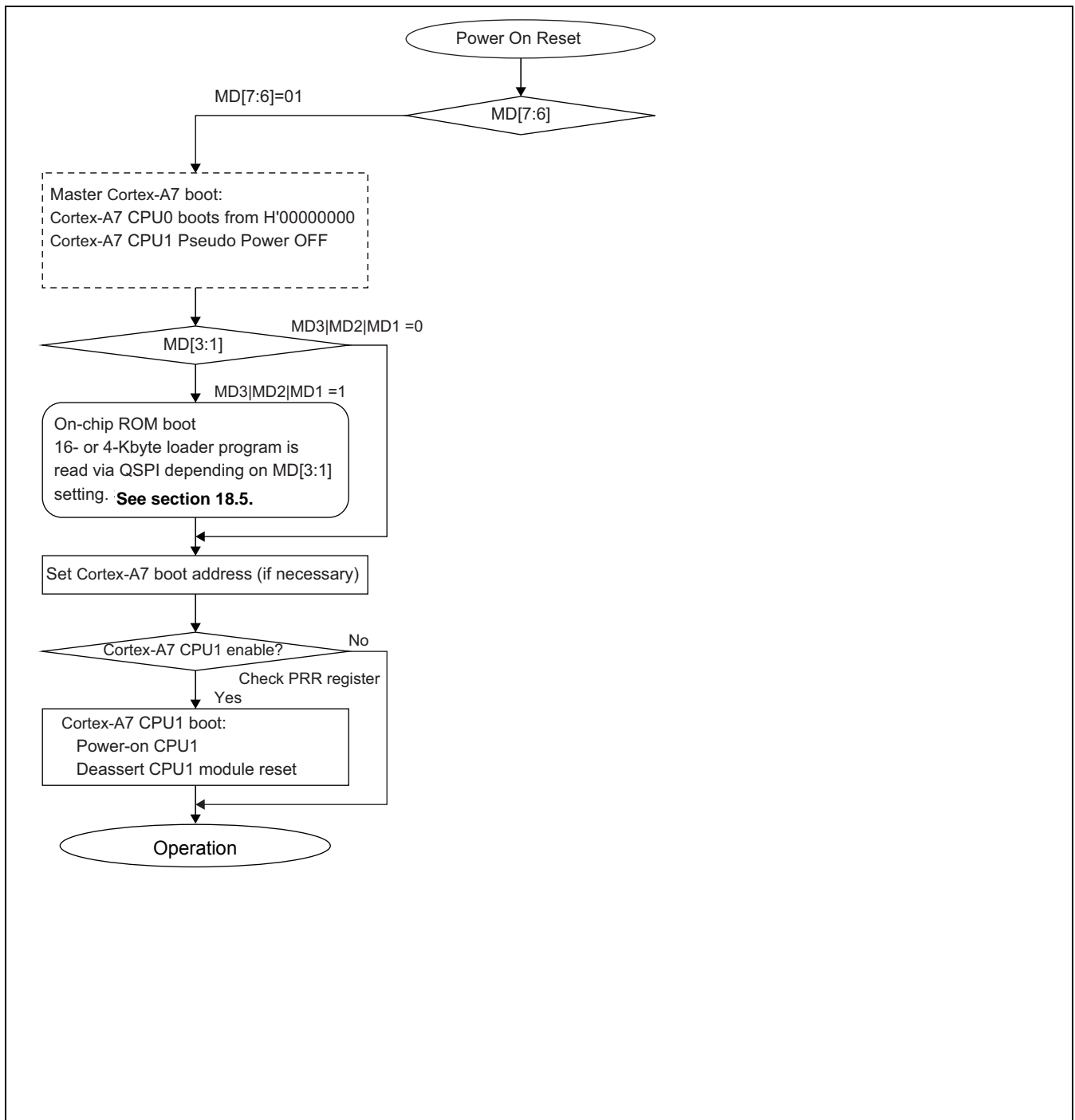


Figure 18.3 Flow of Booting Up

## 18.5 Serial Flash ROM Boot

RZ/G1H	RZ/G1N
RZ/G1M	RZ/G1E

### 18.5.1 Serial Flash ROM Boot

In QSPI boot, the boot program in the on-chip ROM starts up the QSPI and SYS-DMAC channel 1, and transfers the loader program previously stored in the serial flash ROM to the on-chip RAM via the QSPI module. Here, the QSPI module reads the serial flash ROM with the fast read mode. After loader program is transferred, the program automatically jumps to the top address of the loader program. The amount of data to be transferred and QSPI IF frequency depend on the MD[3:1] pin setting. Controlling the device-specific quad serial flash ROM through the loader program enables reduction of program load time after loader program transfer.

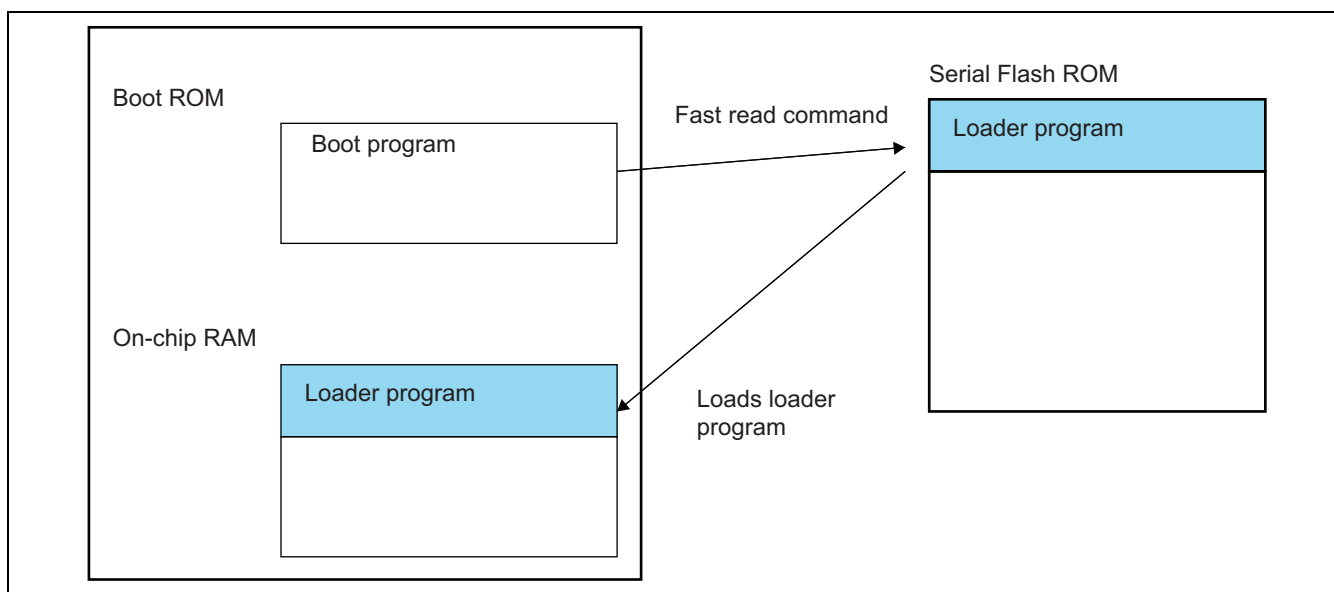


Figure 18.4 Address Space in Serial Flash Memory Boot Mode

## 18.5.2 Usage of QSPI Pins

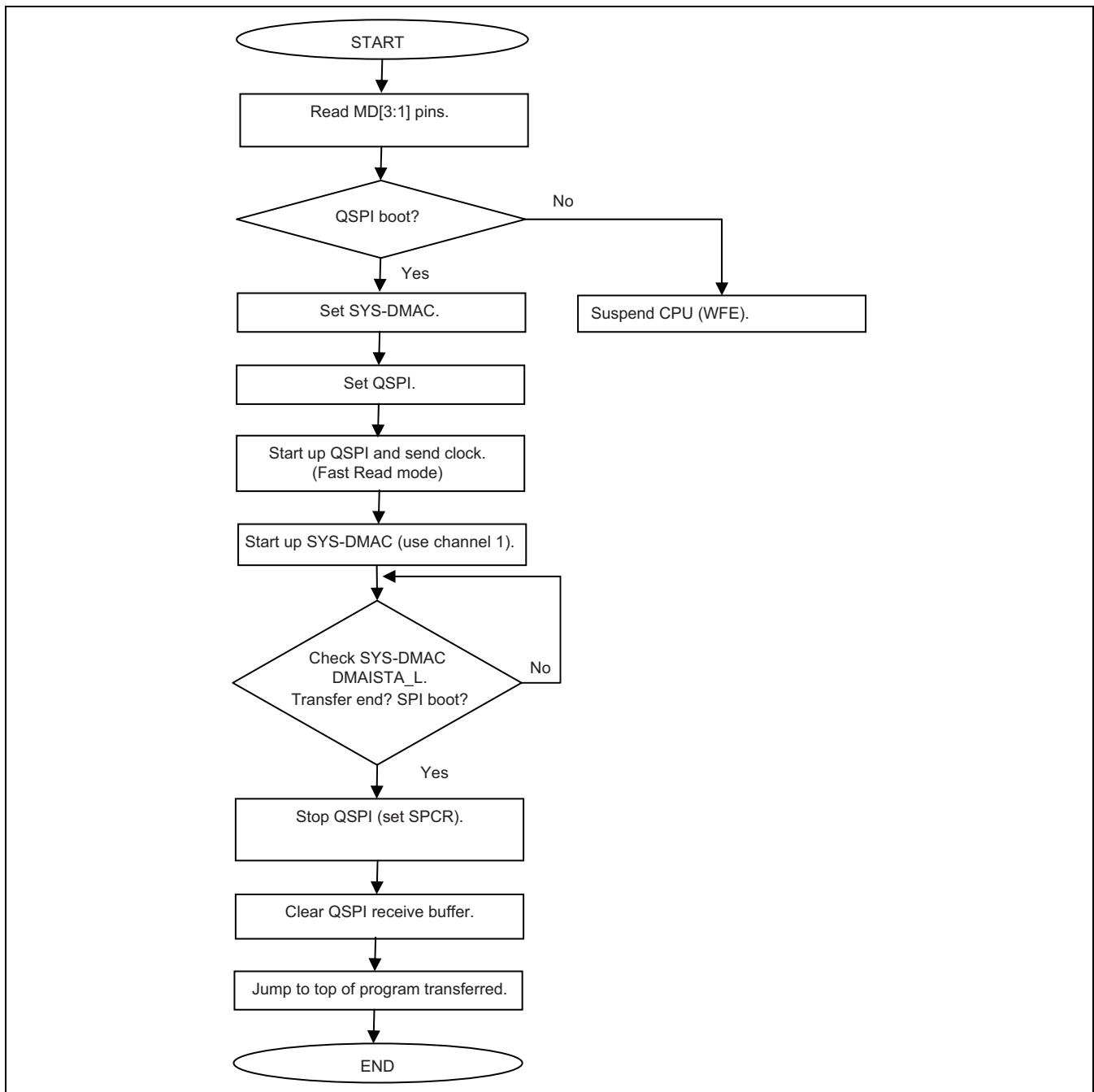
**Table 18.2 QSPI Pin Configuration**

Name	Pin Name	Function Name	I/O	Function
Serial clock	A20	SPCLK	Output	Outputs serial clock.
Transmit data	A21	MOSI	Output	Outputs transmit data.
Receive data	A22	MISO	Input	Inputs receive data.
Chip select	A25	SSL	Output	Outputs chip select signal. To be set to active low using boot ROM code

Note: IO2 (A23) and IO3 (A24) pins are set in High level by the boot program in the on-chip ROM.

### 18.5.3 Serial Flash ROM Boot Flow

Figure 18.5 show the serial flash ROM boot flow by the on-chip ROM boot program.



**Figure 18.5 Serial Flash ROM Boot Flow by the On-chip ROM Boot Program**

**18.5.4 Notes**

- Upon error occurrence, the CPU issues the WFE command and enters in the suspended state.
- The boot ROM program allows no interrupts.
- The boot ROM program does not issue a reset command or mode bit reset command to the serial flash ROM; using a serial flash ROM with a reset pin is recommended.
- All register settings regarding PFC, QSPI and SYS-DMA channel 1 (except the DMA enable) are not initialized after Serial Flash data transfer is end.

## 18.6 Boot Program in On-Chip ROM

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

The on-chip ROM contains the program to control QSPI as the standard boot ROM program. Modifying the ROM code enables booting through another peripheral module.



## 19. R-GP2D



### 19.1 Overview

The R-GP2D is a module that provides a 2D graphics rendering function.

#### 19.1.1 Features

1. Drawing functions
  - 4-vertex screen drawing, polygonal drawing, line drawing, high-functional bold line drawing, anti-aliasing, and BITBLT-type commands with raster operation/alpha blending, line alpha blending.
2. Coordinate transformation
  - Coordinate transformation ( $4 \times 4$  matrix operation + perspective W division)
3. Color mode
  - Source: 1, 8, 16, or 32 bits/pixel
  - Drawing: 8, 16, or 32 bits/pixel
  - Work: 1 bit/pixel
  - $\alpha$  map: 8 bits/pixel
4. Screen coordinates
  - X direction: 0 to 4,095
  - Y direction: 0 to 4,095
5. Register settings
  - Current pointer setting (MOVE/RMOVE), local offset setting (LCOFS/RLCOFS), specific address mapped register setting (WPR), local coordinate transformation offset setting (RGTOFS).
6. Sequence control
  - Waiting for Vsync (VBKEM), jump (JUMP), subroutine (GOSUB) (nesting levels: 1 or 8)
7. Antialias font
  - 8-bit/pixel color format – antialias font drawing
8. Multi-valued source blend referencing  $\alpha$  map
  - $\alpha$  map in the 8-bit/pixel color format
9. Customized bold line
  - Setting of thickness direction switching boundary (BDS), jaggy reduction (WLM)
10. New anti-aliasing
  - Anti-aliasing process to the horizontal, vertical, and 45-degree diagonal line segment is enabled. [NAA]
11. Loop function
  - Creates a closed figure of which starting and final points are linked [LOOP]
12. Anti-aliasing coverage drawing function
  - The function to draw anti-aliasing coverage. [ACDE]

## 19.1.2 List of Commands and Rendering Attributes

Table 19.1 List of Commands and Rendering Attributes (1)

Command	OP CODE								Rendering Attribute							
									b15	b14	b13	b12	b11	b10	b9	b8
	M TRE	LOOP	CLIP	RCLIP	STRANS	DTRANS	WORK	SS								
POLYGON4A	1	0	0	0	0	0	1	0	MTRE		CLIP	RCLIP	STRANS		WORK	SS
POLYGON4B					0	0	0	1	MTRE		CLIP	RCLIP	STRANS		WORK	SS
POLYGON4C					0	0	0	0	MTRE		CLIP	RCLIP			WORK	
LINEA	1	0	1	1	0	0	1	0	MTRE	LOOP	CLIP	RCLIP	STRANS			SS (0)
LINEB					0	0	0	1	MTRE	LOOP	CLIP	RCLIP	STRANS			SS (0)
LINEC					0	0	0	0	MTRE	LOOP	CLIP	RCLIP		LINKE	LREL	
LINED					0	0	1	1	MTRE	LOOP	CLIP	RCLIP		LINKE	LREL	
RLINEA					0	1	1	0	MTRE	LOOP	CLIP	RCLIP	STRANS			SS (0)
RLINEB					0	1	0	1	MTRE	LOOP	CLIP	RCLIP	STRANS			SS (0)
RLINEC					0	1	0	0	MTRE	LOOP	CLIP	RCLIP		LINKE	LREL	
RLINED					0	1	1	1	MTRE	LOOP	CLIP	RCLIP		LINKE	LREL	
FTRAPC	1	1	0	1	0	0	0	0	MTRE	LOOP	CLIP	RCLIP		LINKE	LREL	
RFTRAPC					0	1	0	0	MTRE	LOOP	CLIP	RCLIP		LINKE	LREL	
CLRWC	1	1	1	0	0	0	0	0	MTRE		CLIP	RCLIP				
LINEWC	1	1	1	1	0	0	0	0	MTRE	LOOP	CLIP	RCLIP				
RLINEWC					0	1	0	0	MTRE	LOOP	CLIP	RCLIP				
BITBLTA	1	0	1	0	0	0	1	0	MTRE		CLIP	RCLIP	STRANS	DTRANS	WORK	SS
BITBLTB					0	0	0	1	MTRE		CLIP	RCLIP	STRANS	DTRANS	WORK	SS
BITBLTC					0	0	0	0	MTRE		CLIP	RCLIP		DTRANS	WORK	
AAFA	1	0	1	0	1	0	1	0	MTRE		CLIP	RCLIP	STRANS	DTRANS	WORK	SS (1)
AAFC					1	0	0	0	MTRE		CLIP	RCLIP		DTRANS		SS (0)
Reserved					1	0	1	1	Only for internal verification. This setting should not be specified. If specified, the command error (CER) flag is not set.							

Table 19.1 List of Commands and Rendering Attributes (1) (cont.)

Command	OP CODE								Rendering Attribute							
									b7	b6	b5	b4	b3	b2	b1	b0
	REL	STYLE	BLKE	NET/EDG	EOS	COOF	AA	CLKW								
POLYGON4A	1	0	0	0	0	0	1	0	REL	STYLE	BLKE	NET	EOS	COOF	αE	SαE
POLYGON4B					0	0	0	1	REL	STYLE	BLKE	NET	EOS	COOF	αE	
POLYGON4C					0	0	0	0			BLKE	NET	EOS	COOF	αE	
LINEA	1	0	1	1	0	0	1	0	REL	STYLE (1)		NET	EOS	COOF	AA	
LINEB					0	0	0	1	REL	STYLE (1)		NET	EOS	COOF	AA	
LINEC					0	0	0	0				NET	EOS	COOF	AA	
LINED					0	0	1	1							AA (1)	CLKW
RLINEA					0	1	1	0	REL	STYLE (1)		NET	EOS	COOF	AA	
RLINEB					0	1	0	1	REL	STYLE (1)		NET	EOS	COOF	AA	
RLINEC					0	1	0	0				NET	EOS	COOF	AA	
RLINED					0	1	1	1							AA (1)	CLKW
FTRAPC	1	1	0	1	0	0	0	0			BLKE (1)	EDG	EOS			
RFTRAPC					0	1	0	0			BLKE (1)	EDG	EOS			
CLRWC	1	1	1	0	0	0	0	0			BLKE (1)					
LINEWC	1	1	1	1	0	0	0	0					EOS			
RLINEWC					0	1	0	0					EOS			
BITBLTA	1	0	1	0	0	0	1	0	REL	SRCDIRX	SRCDIRY	DSTDIRX	DSTDIRY	COOF	αE	SαE
BITBLTB					0	0	0	1	REL	SRCDIRX	SRCDIRY	DSTDIRX	DSTDIRY	COOF	αE	
BITBLTC					0	0	0	0				DSTDIRX	DSTDIRY	COOF	αE	
AAFA	1	0	1	0	1	0	1	0						COOF	αE (1)	SαE
AAFC					1	0	0	0	REL							
Reserved					1	0	1	1	Only for internal verification. This setting should not be specified. If specified, the command error (CER) flag is not set.							

- REL: Valid only when SS = 0. Clear this bit to 0 when SS = 1.
- COOF: Clear this bit to 0 in 8-bit/pixel mode (GBM = 0).
- S $\alpha$ E: Valid only for the ARGB format (SPF = DPF = 1). Clear this bit to 0 for the RGB format (SPF = DPF = 0) and 8-bit/pixel mode (GBM = 0).  
Clear this bit to 0 when  $\alpha$ E = 0.
- $\alpha$ E: Clear this bit to 0 in 8-bit/pixel mode (GBM = 0).  
In the POLYGON4A, POLYGON4B, or POLYGON4C command, valid only when BLKE = 1. Clear this bit to 0 when BLKE = 0.  
In the BITBLTA, BITBLTB, or BITBLTC command, valid only when the ROP code = H'CC. Clear this bit to 0 for other codes.  
In the AAFA command, set this bit to 1.
- LREL: Valid only when LINKE = 1. The LREL bit should be cleared to 0 when LINKE = 0.
- STYLE: Set this bit to 1 when BLKE = 1. In the LINEA, LINEB, RLINEA, or RLINEB command, set this bit to 1.
- AA: Clear this bit to 0 when NET = 1. Clear this bit to 0 in 8-bit/pixel mode (GBM = 0).  
In the LINED or RLINED command, set this bit to 1.
- SS: In the LINEA, LINEB, RLINEA, RLINEB, or AAFC command, clear this bit to 0. In the AAFA command, set this bit to 1.
- BLKE: In the FTRAPC, RFTRAPC, or CLRWC command, set this bit to 1.
- Shaded bit: Cannot be used (clear this bit to 0).

**Table 19.2 List of Commands and Rendering Attributes (2)**

Command	OP CODE								Rendering Attribute						
	b31	b30	b29	b28	b27	b26	b25	b24	b15	b14	b13	b12	b11	b10	b9
TRAP	0	0	0	0	0	0	0	0							
NOP/INT	0	0	0	0	1	0	0	0	INT						
VBKEM	0	0	0	1	0	0	0	0							
WPR	0	0	0	1	1	0	0	0						LINKE	LREL
JUMP	0	0	1	0	1	0	0	0							
GOSUB	0	0	1	1	0	0	0	0							
RET	0	0	1	1	1	0	0	0							
LCOFS	0	1	0	0	0	0	0	0							
RLCOFS	0	1	0	0	0	1	0	0							
MOVE	0	1	0	0	1	0	0	0							
RMOVE	0	1	0	0	1	1	0	0							
SYNC	0	0	0	1	0	0	1	0						WCLR	WFLSH
RGTOFS	0	1	1	0	0	1	0	0	Bits 23 to 12: RXOFS		Bits 11 to 0: RYOFS				
Reserved	0	1	0	1	0	0	0	0	Only for internal verification. This setting should not be specified. If specified, the command error (CER) flag is not set.						

**Table 19.2 List of Commands and Rendering Attributes (2) (cont.)**

Command	OP CODE								Rendering Attribute							
	b31	b30	b29	b28	b27	b26	b25	b24	b7	b6	b5	b4	b3	b2	b1	b0
TRAP	0	0	0	0	0	0	0	0	Flip7	Flip6	Flip5	Flip4	Flip3	Flip2	Flip1	Flip0
NOP/INT	0	0	0	0	1	0	0	0	INT No							
VBKEM	0	0	0	1	0	0	0	0								
WPR	0	0	0	1	1	0	0	0				ByteM3	ByteM2	ByteM1	ByteM0	
JUMP	0	0	1	0	1	0	0	0	REL							
GOSUB	0	0	1	1	0	0	0	0	REL						No	No
RET	0	0	1	1	1	0	0	0							No	No
LCOFS	0	1	0	0	0	0	0	0								
RLCOFS	0	1	0	0	0	1	0	0								
MOVE	0	1	0	0	1	0	0	0								
RMOVE	0	1	0	0	1	1	0	0								
SYNC	0	0	0	1	0	0	1	0	ACLR	TCLR		DCLR				DFLSH
RGTOFS	0	1	1	0	0	1	0	0	Bits 23 to 12: RXOFS		Bits 11 to 0: RYOFS					
Reserved	0	1	0	1	0	0	0	0	Only for internal verification. This setting should not be specified. If specified, the command error (CER) flag is not set.							

### 19.1.3 Block Diagram

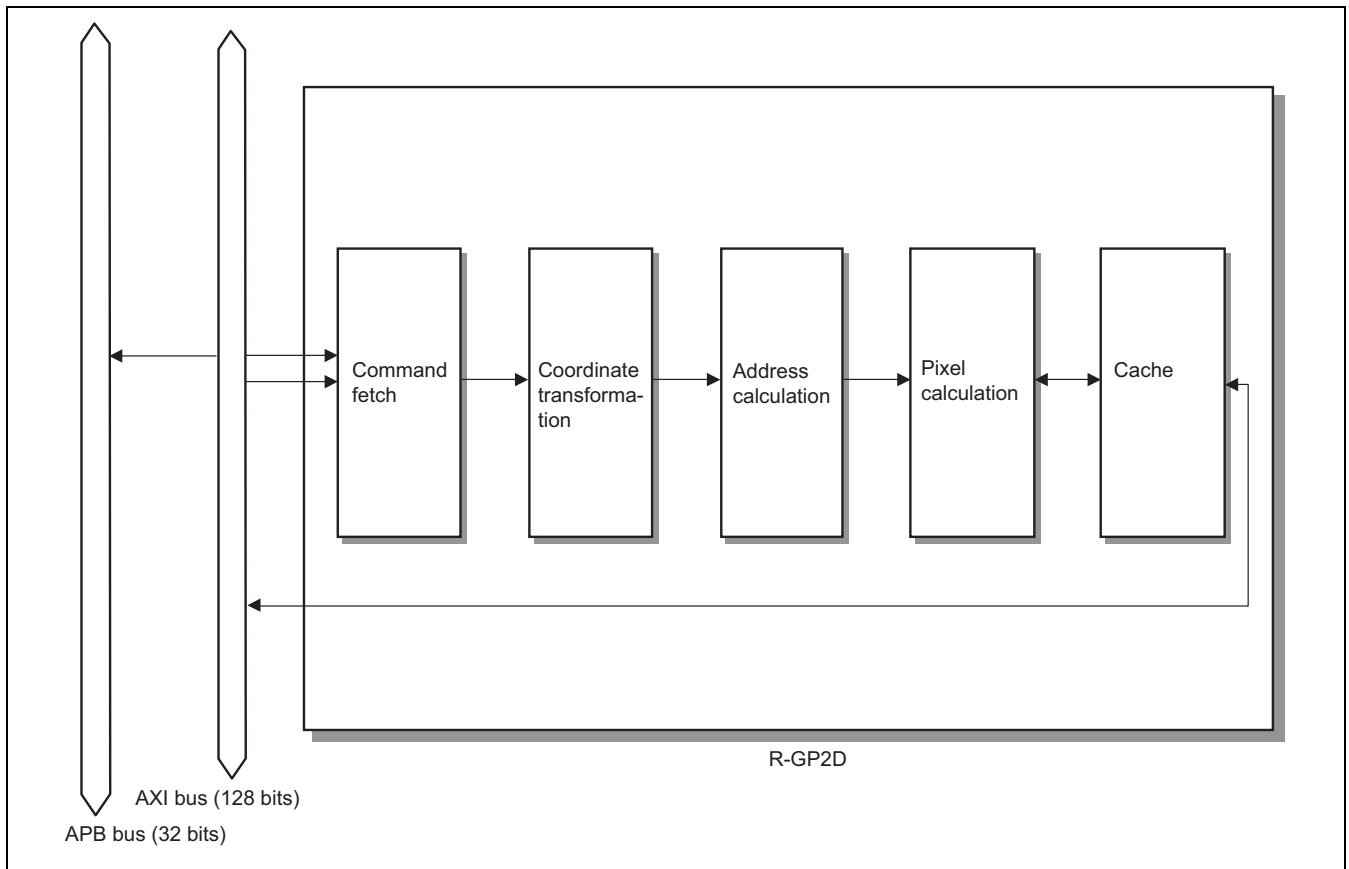


Figure 19.1 R-GP2D Block Diagram

### 19.1.4 Register Configuration

Tables 19.3 through 19.7 show the configuration of the R-GP2D registers.

These registers are 32-bit wide and should be accessed in longword (32-bit) units. If accessed in other sizes, operation is not guaranteed. The R-GP2D register address area is allocated in the range from H'E6EC 0000 to H'E6EE FFFC. Even in this range, however, if an address other than those shown in the following tables is accessed, operation is not guaranteed.

The CPU writing to registers, excluding the system control registers (SCLR), is prohibited during the time from the start of rendering to the TRAP command execution, except for the drawing halted period specified by the INT command. The CPU reading from registers, excluding the status registers, is prohibited.

Note: When writing to the registers to which ByteM control at the WPR command cannot be applied, set B'0000 to the ByteM bits at the WPR command.

#### (1) System Control Registers

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	—	—	—

**Table 19.3 Register Configuration (System Control Registers)**

Name	Abbr.	R/W	Value after Reset	Address	Access Size	Setting in WPR Command	WPR Command ByteM Control
System control register	SCLR	R/W	H'XXXX XXXX	H'E6EC 0000	32	Unsettable	—
Status register	SR	R	H'EXXX XXX0	H'E6EC 0004	32	Unsettable	—
Status register clear register	SRCR	W	H'XXXX XXX0	H'E6EC0008	32	Unsettable	—
Interrupt enable register	IER	R/W	H'XXXX XXX0	H'E6EC000C	32	Settable	Possible
Interrupt command id register	ICIDR	R	H'XXXX XXXX	H'E6EC0010	32	Unsettable	—

**(2) Memory Control Registers**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	—	—	—

**Table 19.4 Register Configuration (Memory Control Registers)**

Name	Abbr.	R/W	Value after Reset	Address	Access Size	Setting in WPR Command	WPR Command ByteM Control
Return address register 0	RTN0R	R/W	H'XXXX XXXX	H'E6EC0040	32	Settable	Impossible
Return address register 1	RTN1R	R/W	H'XXXX XXXX	H'E6EC0044	32	Settable	Impossible
Display list start address register	DLSAR	R/W	H'XXXX XXXX	H'E6EC0048	32	Unsettable	—
2-dimensional source area start address register	SSAR	R/W	H'XXXX XXXX	H'E6EC004C	32	Settable	Impossible
Rendering start address register	RSAR	R/W	H'XXXX XXXX	H'E6EC0050	32	Settable	Impossible
Work area start address register	WSAR	R/W	H'XXXX XXXX	H'E6EC0054	32	Settable	Impossible
Source stride register	SSTRR	R/W	H'XXXX XXXX	H'E6EC0058	32	Settable	Impossible
Destination stride register	DSTRR	R/W	H'XXXX XXXX	H'E6EC005C	32	Settable	Impossible
Endian conversion control register	ENDCVR	R/W	H'XX00 0XX0	H'E6EC0060	32	Unsettable	—
$\alpha$ -Map area start address register	ASAR	R/W	H'XXXX XXXX	H'E6EC0064	32	Settable	Impossible
$\alpha$ -Map stride register	ASTRR	R/W	H'XXXX XXXX	H'E6EC0068	32	Settable	Impossible
Address extension register	ADREXTR	R/W	H'XXXX XXXX	H'E6EC006C	32	Unsettable	—
Return address STK register	RTNSTKR	R	H'X000 000X	H'E6EC0074	32	Unsettable	—

**(3) Color Control Registers**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	—	—	—

**Table 19.5 Register Configuration (Color Control Registers)**

Name	Abbr.	R/W	Value after Reset	Address	Access Size	Setting in WPR Command	WPR Command ByteM Control
Source transparent color register	STCR	R/W	H'XXXX XXXX	H'E6EC0080	32	Settable	Impossible
Destination transparent color register	DTCR	R/W	H'XXXX XXXX	H'E6EC0084	32	Settable	Impossible
Alpha value register	ALPHR	R/W	H'XXXX XXXX	H'E6EC0088	32	Settable	Impossible
Color offset register	COFSR	R/W	H'XXXX XXXX	H'E6EC008C	32	Settable	Impossible
A value 8 register	AVALUE8R	R/W	H'XXXX XX00	H'E6EC0098	32	Settable	Impossible
Alpha test control register	ATCLR	R/W	H'XX00 XX00	H'E6EC009C	32	Settable	Impossible

**(4) Rendering Control Registers**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	—	—	—

**Table 19.6 Register Configuration (Rendering Control Registers)**

Name	Abbr.	R/W	Value after Reset	Address	Access Size	Setting in WPR Command	WPR Command ByteM Control
Rendering control register	RCLR	R/W	H'00X0 0004	H'E6EC00C0	32	Settable	Possible
Command status register	CSTR	R	H'XXXX XXXX	H'E6EC00C4	32	Unsettable	—
Current pointer register	CURR	R	H'XXXX XXXX	H'E6EC00C8	32	Unsettable	—
Local offset register	LCOR	R	H'XXXX XXXX	H'E6EC00CC	32	Unsettable	—
System clipping area MAX register	SCLMAR	R	H'XXXX XXXX	H'E6EC00D0	32	Settable	Impossible
User clipping area MIN register	UCLMIR	R	H'XXXX XXXX	H'E6EC00D4	32	Settable	Impossible
User clipping area MAX register	UCLMAR	R	H'XXXX XXXX	H'E6EC00D8	32	Settable	Impossible
Relative user clipping area MIN register	RUCLMIR	R	H'XXXX XXXX	H'E6EC00DC	32	Settable	Impossible
Relative user clipping area MAX register	RUCLMAR	R	H'XXXX XXXX	H'E6EC00E0	32	Settable	Impossible
Rendering control 2 register	RCL2R	R/W	H'0X00 4X0X	H'E6EC00F0	32	Settable	Possible
Pattern offset register	POFSR	R/W	H'X000 X000	H'E6EC00F8	32	Settable	Impossible



**(5) Coordinate Transformation Control Registers**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	—	—	—

**Table 19.7 Register Configuration (Coordinate Transformation Control Registers)**

Name	Abbr.	R/W	Value after Reset	Address	Access Size	Setting in WPR Command	WPR Command ByteM Control
Coordinate transformation control register	GTRCR	R/W	H'XXXX XXXX	H'E6EC0100	32	Settable	Impossible
Matrix parameter A register	MTRAR	R/W	H'3F80 0000	H'E6EC0104	32	Settable	Impossible
Matrix parameter B register	MTRBR	R/W	H'0000 0000	H'E6EC0108	32	Settable	Impossible
Matrix parameter C register	MTRCR	R/W	H'0000 0000	H'E6EC010C	32	Settable	Impossible
Matrix parameter D register	MTRDR	R/W	H'0000 0000	H'E6EC0110	32	Settable	Impossible
Matrix parameter E register	MTRER	R/W	H'3F80 0000	H'E6EC0114	32	Settable	Impossible
Matrix parameter F register	MTRFR	R/W	H'0000 0000	H'E6EC0118	32	Settable	Impossible
Matrix parameter G register	MTRGR	R/W	H'0000 0000	H'E6EC011C	32	Settable	Impossible
Matrix parameter H register	MTRHR	R/W	H'0000 0000	H'E6EC0120	32	Settable	Impossible
Matrix parameter I register	MTRIR	R/W	H'3F80 0000	H'E6EC0124	32	Settable	Impossible
Coordinate transformation offset X register	GTROFSXR	R/W	H'XXXX 0000	H'E6EC0128	32	Settable	Impossible
Coordinate transformation offset Y register	GTROFSYR	R/W	H'XXXX 0000	H'E6EC012C	32	Settable	Impossible
Z clipping area MIN register	ZCLPMINR	R/W	H'3F00 0000	H'E6EC0130	32	Settable	Impossible
Z clipping area MAX register	ZCLPMAXR	R/W	H'477F FF00	H'E6EC0134	32	Settable	Impossible
Z saturation value MIN register	ZSATVMINR	R/W	H'3F00 0000	H'E6EC0138	32	Settable	Impossible
2-dimensional vertex clip extension width register	2DVCEXTR	R/W	H'XXXX XXX5	H'E6EC0160	32	Settable	Impossible

**(6) Mode Control Register**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	—	—	—

**Table 19.8 Register Configuration (Mode Control Register)**

Name	Abbr.	R/W	Value after Reset	Address	Access Size	Setting in WPR Command	WPR Command ByteM Control
Mode 0 register	MD0R	R/W	H'XXXX XXXX	H'E6EC01FC	32	Settable	Possible

**19.1.5 Register States in Each Operating Mode****Table 19.9 Register States in Each Operating Mode**

Register	Abbr.	Power-On Reset	Module Standby
All registers of R-GP2D	—	See the register description in each section.	Retained

## 19.2 Register Description



- Legend for Register Description:

Initial value: Register value after a reset

—: Undefined value

R/W: Readable/writable. The written value can be read.

R/WC0: Readable/writable. Writing 0 initializes the bit. Writing 1 is ignored.

R: Read-only. If a bit has a defined initial value (0 or 1), read out the value of the bit and write it back without alteration. (Writing should not change such bits from their initial values, i.e. only the target bits should be modified (read-modify-write).) If a bit has an undefined initial value, write 0.

—/W: Write-only. The read value is undefined.

Set range: [a, b] indicates that the values are included. (a, b) indicates that the values are excluded.

Hereafter, "reset" refers to both a hardware reset and software reset unless specified otherwise.

### Point for Caution

Note that when the R-GP2D registers are read under any of the following conditions, the first value to be read out may be incorrect.

#### Conditions:

- 1) After a power-on reset (PRESET# = L to H)
- 2) After leaving the module stop state (MSTPSR8.MSTPST807 = 1 to 0)
- 3) After certain drawing states; specifically, any of the following states (which involve interrupts)
  - Rendering break (SR.BRK = 1)
  - Command error (SR.CER = 1)
  - Interrupt (SR.INT = 1)
  - Trap (SR.TRA = 1)

#### Workaround:

One dummy read of the R-GP2D registers should be executed after a power-on reset, the R-GP2D leaving the module stop state, and at the beginning of the interrupt handling routines for the R-GP2D.

#### Note:

When using polling of the flags of SR, this usage note and workaround are not necessary because the polling can replace a dummy-read as the read operation.

## 19.2.1 System Control Registers

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	—	—	—

### 19.2.1.1 System Control Register (SCLR)

Address: H'E6EC0000

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SRES	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	1	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	RBRK	—	—	RS
Initial value:	—	—	—	—	—	—	—	0	—	—	—	—	0	—	—	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	SRES	1	R/W	<p>Software Resets the R-GP2D.</p> <p>0: Command processing execution is enabled. 1: Reset state</p> <p>This bit is set to 1 when a hardware reset is performed. Clear this bit to 0 in initialization.</p> <p>When this bit is set to 1 by software, a reset is performed for drawing operations only. The R-GP2D registers are also initialized. While this bit is set to 1, this is the only register that can be written to.</p> <p>Note: To issue a software-reset during the drawing period (the interval from the start of rendering to execution of a TRAP command), follow the procedure below.</p> <ol style="list-style-type: none"> <li>1. Set SRES to 1.</li> <li>2. Wait for 1 vsync period.</li> <li>3. Specify module reset as 1 (for at least four cycles of P<math>\phi</math>).</li> <li>4. Specify module reset as 0.</li> <li>5. Set SRES to 0.</li> </ol> <p>For details on the module reset, refer to section 7A, Module Standby, Software Reset.</p>
30	—	0	R	Reserved
29 to 9	—	—	R	Reserved
8	—	0	R	Reserved
7 to 4	—	—	R	Reserved

Bit	Bit Name	Initial Value	R/W	Description
3	RBRK	0	R/W	<p>Rendering Break</p> <p>This bit can be used to stop rendering. Set this bit while the value of the BRK bit in the status register (SR) is 0.</p> <p>0: Drawing is not stopped.</p> <p>1: If the R-GP2D module is in the midst of drawing, the command that is currently being executed is completed, the value of the BRK bit in the status register (SR) becomes 1 at the time the next command is fetched, and drawing is stopped. If drawing by the R-GP2D module is not in progress when the bit is set to 1, the value of the BRK bit is not changed. Furthermore, the address where the next command to be executed after suspension is placed in the command status register.</p> <p>This bit is only cleared to 0 when drawing has been suspended.</p>
2, 1	—	—	R	Reserved
0	RS	0	R/W	<p>Rendering Start</p> <p>Specifies the start of rendering. During the drawing period (from rendering start to TRAP command execution), writing 1 to this bit is prohibited.</p> <p>0: Rendering is not started.</p> <p>1: Rendering is started. This bit is cleared to 0 after rendering starts.</p> <p>Note: Setting the SRES and RS bits to 1 simultaneously is prohibited.</p>

### 19.2.1.2 Status Register (SR)

Address: H'E6EC0004

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	VER				—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	1	1	1	0	—	0	0	0	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	BRK	CER	INT	TRA
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 28	VER	1110	R	Version Flag This flag is read as B'1110.
27	—	—	R	Reserved
26 to 24	—	All 0	R	Reserved
23 to 4	—	—	R	Reserved
3	BRK	0	R	Rendering Break Flag 0: The values of the SRES bit in SCLR and the BRCL bit in SRCR determine the time from clearing of the BRK flag to the next time drawing is suspended. 1: When suspension of drawing has been specified, this value indicates that the current command is no longer being executed. The BRK flag retains its value until it is cleared by a reset or by the SRCR setting.
2	CER	0	R	Command Error Flag Indicates that an illegal command has been fetched. 0: Normal state. An illegal command has not been fetched since the CER flag has been cleared by the SRES bit in SCLR or the CECL bit in SRCR. An illegal command is one in which the upper eight bits of the command code are undefined. The R-GP2D does not check the legality of the rendering attributes in the lower 16 bits. 1: Drawing operation halt state. Drawing operation remains halted because an illegal command was fetched after the CER flag has been cleared by the SRES bit in SCLR or the CECL bit in SRCR. To resume drawing operation, after executing a software reset, make the bit setting for rendering start. The CER flag retains its state until it is cleared by a reset or by SRCR. A command error occurs if n is 0 or 1 in LINE-type commands and n is 0 in RLINE-type commands.

Bit	Bit Name	Initial Value	R/W	Description
1	INT	0	R	<p>Interrupt Flag</p> <p>Indicates that the NOP/INT command has been fetched (only when the rendering attribute INT bit is 1).</p> <p>0: The NOP/INT command has not been fetched since the INT flag has been cleared by the SRES bit in SCLR or the INCL bit in SRCR.</p> <p>1: Drawing operation halt state. Drawing operation remains halted because the NOP/INT command was fetched after the INT flag has been cleared by the SRES bit in SCLR or the INCL bit in SRCR (only when the rendering attribute INT bit is 1).</p> <p>Clearing the INT flag by the INCL bit in SRCR resumes drawing operation from the next command. The CPU writing to registers, excluding the system control registers (SCLR), is prohibited during the time from the start of drawing to the TRAP command execution.</p> <p>The INT flag retains its state until it is cleared by a reset or by SRCR.</p> <p>Note: Do not rewrite the display list when drawing operation is halted by the INT command.</p>
0	TRA	0	R	<p>Trap Flag</p> <p>Indicates the end of command execution.</p> <p>0: The TRAP command has not been fetched since the TRA flag has been cleared by the SRES bit in SCLR or the TRCL bit in SRCR.</p> <p>1: Command execution has ended, or the current command is not being executed.</p> <p>The TRA flag retains its state until it is cleared by a reset or by SRCR.</p>

### 19.2.1.3 Status Register Clear Register (SRCR)

Address: H'E6EC0008

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	BRCL	CECL	INCL	TRCL
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	0	0	0	0
R/W:	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

Bit	Bit Name	Initial Value	R/W	Description
31 to 4	—	—	W	Reserved
3	BRCL	0	W	Rendering Break Flag Clear Selects whether the BRK flag in SR is cleared or not. 0: The BRK flag in SR is not cleared to 0. 1: The BRK flag in SR is cleared to 0. All of the values in SRCR are cleared to 0 internally after SR clearing is completed.
2	CECL	0	W	Command Error Flag Clear Selects whether the CER flag in SR is cleared or not. 0: The CER flag in SR is not cleared to 0. 1: The CER flag in SR is cleared to 0. All of the values in SRCR are cleared to 0 internally after SR clearing is completed.
1	INCL	0	W	Interrupt Flag Clear Selects whether the INT flag in SR is cleared or not. 0: The INT flag in SR is not cleared to 0. 1: The INT flag in SR is cleared to 0. All of the values in SRCR are cleared to 0 internally after SR clearing is completed.
0	TRCL	0	W	Trap Flag Clear Selects whether the TRA flag in SR is cleared or not. 0: The TRA flag in SR is not cleared to 0. 1: The TRA flag in SR is cleared to 0. All of the values in SRCR are cleared to 0 internally after SR clearing is completed.



### 19.2.1.4 Interrupt Enable Register (IER)

Address: H'E6EC000C

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	BRE	CEE	INE	TRE
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 4	—	—	R	Reserved
3	BRE	0	R/W	Rendering Break Flag Enable Enables or disables interrupts initiated by the BRK flag in SR. 0: Interrupts initiated by the BRK flag in SR are disabled. 1: Interrupts initiated by the BRK flag in SR are enabled.
2	CEE	0	R/W	Command Error Flag Enable Enables or disables interrupts initiated by the CER flag in SR. 0: Interrupts initiated by the CER flag in SR are disabled. 1: Interrupts initiated by the CER flag in SR are enabled.
1	INE	0	R/W	Interrupt Flag Enable Enables or disables interrupts initiated by the INT flag in SR. 0: Interrupts initiated by the INT flag in SR are disabled. 1: Interrupts initiated by the INT flag in SR are enabled.
0	TRE	0	R/W	Trap Flag Enable Enables or disables interrupts initiated by the TRA flag in SR. 0: Interrupts initiated by the TRA flag in SR are disabled. 1: Interrupts initiated by the TRA flag in SR are enabled.

### 19.2.1.5 Interrupt Command ID Register (ICIDR)

Address: H'E6EC0010

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—		
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—		
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R		
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
	—	—	—	—	—	—	—	—	ICID								—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—		
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R		

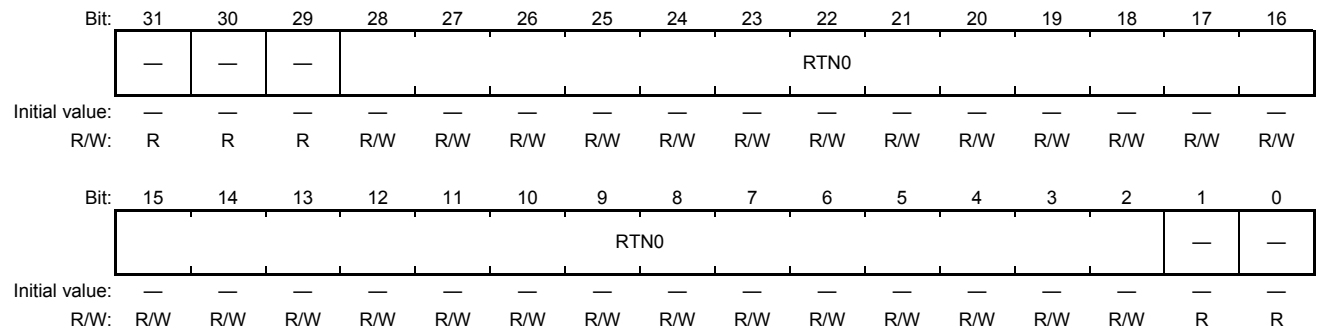
Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	—	R	Reserved
7 to 0	ICID	Un-defined	R	Interrupt Command ID Stores the ID specified by the rendering attribute if the rendering attribute INT bit is set to 1 when the NOP/INT command is fetched.

### 19.2.2 Memory Control Registers

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	—	—	—

#### 19.2.2.1 Return Address Register 0 (RTN0R)

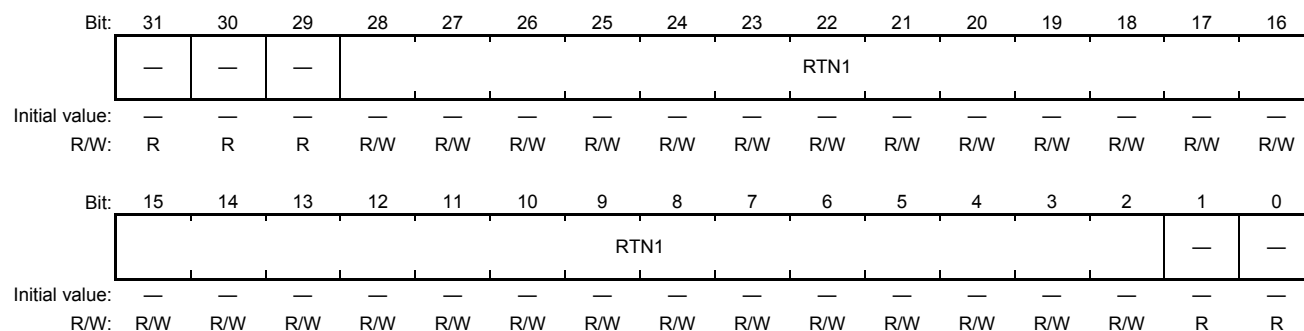
Address: H'E6EC0040



Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	—	R	Reserved
28 to 2	RTN0	Un-defined	R/W	Return Address 0 (A28 to A2) Stores the return address when the rendering attribute No bit is 0 in the GOSUB command. The address indicated by RTN0R is a longword address (bits A28 to A2).
1, 0	—	—	R	Reserved

### 19.2.2.2 Return Address Register 1 (RTN1R)

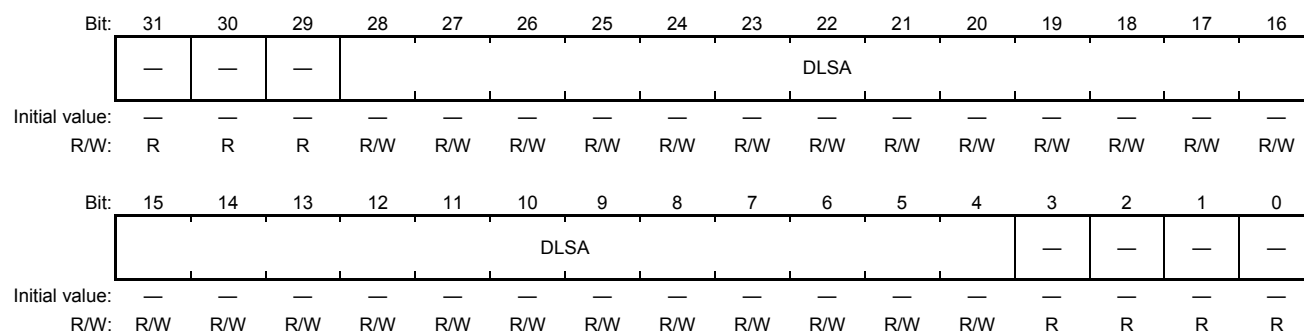
Address: H'E6EC0044



Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	—	R	Reserved
28 to 2	RTN1	Un-defined	R/W	Return Address 1 (A28 to A2) Stores the return address when the rendering attribute No bit is 1 in the GOSUB command. The address indicated by RTN1R is a longword address (bits A28 to A2).
1, 0	—	—	R	Reserved

### 19.2.2.3 Display List Start Address Register (DLSAR)

Address: H'E6EC0048



Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	—	R	Reserved
28 to 4	DLSA	Un-defined	R/W	Display List Start Address (A28 to A4) Specifies the memory area to be used as the display list. The start physical address (bits A28 to A4) of the display list is set in 16-byte units. Even in 32-bit addressing mode, write the lower 29 bits of the specified 32-bit address to bits 28 to 4.
3 to 0	—	—	R	Reserved

### 19.2.2.4 2-Dimensional Source Area Start Address Register (SSAR)

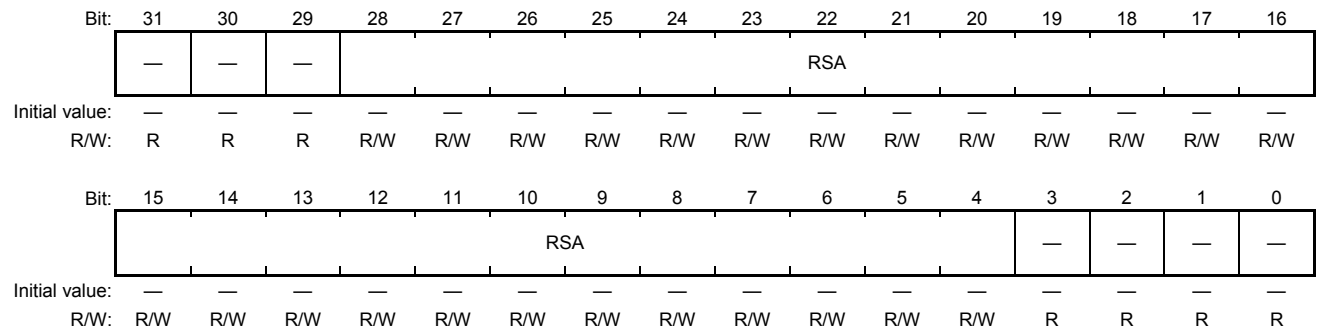
Address: H'E6EC004C

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—			SSA												
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SSA												—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	—	R	Reserved
28 to 4	SSA	Un-defined	R/W	2-Dimensional Source Area Start Address (A28 to A4) Specifies the memory area to be used as the 2-dimensional source area. The physical address set in this register becomes the physical address for the origin of the 2-dimensional source coordinates. The start physical address (bits A28 to A4) of the 2-dimensional source area is set in 16-byte units. Even in 32-bit addressing mode, write the lower 29 bits of the specified 32-bit address to bits 28 to 4.
3 to 0	—	—	R	Reserved

### 19.2.2.5 Rendering Start Address Register (RSAR)

Address: H'E6EC0050



Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	—	R	Reserved
28 to 4	RSA	Un-defined	R/W	<p>Rendering Start Address (A28 to A4)</p> <p>Specifies the memory area to be used as the rendering area. The physical address set in this register becomes the physical address for the rendering coordinate origin. The start physical address (bits A28 to A4) of the rendering area is set in 16-byte units. Even in 32-bit addressing mode, write the lower 29 bits of the specified 32-bit address to bits 28 to 4.</p> <p>Set the rendering start address so that the rendering area does not overlap with the work area.</p>
3 to 0	—	—	R	Reserved

### 19.2.2.6 Work Area Start Address Register (WSAR)

Address: H'E6EC0054

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—			WSA												
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	WSA												—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	—	R	Reserved
28 to 4	WSA	Un-defined	R/W	<p>Work Area Start Address (A28 to A4)</p> <p>Specifies the memory area to be used as the work area. The physical address set in this register becomes the physical address for the work coordinate origin. The start physical address (bits A28 to A4) of the work area is set in 16-byte units. Even in 32-bit addressing mode, write the lower 29 bits of the specified 32-bit address to bits 28 to 4.</p> <p>Use only the work drawing commands for drawing in the work area. When writing to the work area by the CPU, avoid the drawing period (from rendering start to TRAP command execution (including the drawing halt period specified by the NOP/INT command)).</p> <p>Do not use a figure drawn by a work drawing command as the source figure.</p>
3 to 0	—	—	R	Reserved

**19.2.2.7 Source Stride Register (SSTR)**

Address: H'E6EC0058

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	SSTR										—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 13	—	—	R	Reserved
12 to 3	SSTR	Un-defined	R/W	Source Stride (b12 to b3) Specifies the stride of the 2-dimensional source area in pixel units. Set the value in the range of $8 \leq SSTRIDE \leq 4096$ in 8-pixel units.
2 to 0	—	—	R	Reserved

**19.2.2.8 Destination Stride Register (DSTR)**

Address: H'E6EC005C

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	DSTR										—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 13	—	—	R	Reserved
12 to 4	DSTR	Un-defined	R/W	Destination Stride (b12 to b4) Specifies the stride of the destination area in pixel units. Set the value in the range of $256 \leq DSTRIDE \leq 4096$ in 16-pixel units.
3 to 0	—	—	R	Reserved



### 19.2.2.9 Endian Conversion Control Register (ENDCVR)

Address: H'E6EC0060

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	—	—	—	0	0	—	—	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	LW SWAP	W SWAP	BYTE SWAP	BIT SWAP
Initial value:	0	0	0	0	0	0	0	—	0	0	0	—	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	—	0	R	Reserved
30 to 28	—	—	R	Reserved
27, 26	—	00	R	Reserved
25, 24	—	—	R	Reserved
23 to 9	—	All 0	R	Reserved
8	—	—	R	Reserved
7 to 5	—	All 0	R	Reserved
4	—	—	R	Reserved
3	LWSWAP	0	R/W	Longword Swap Swaps data in longword (32-bit) units. 0: Data is not swapped. 1: Data is swapped in longword (32-bit) units.
2	WSWAP	0	R/W	Word Swap Swaps data in word (16-bit) units. 0: Data is not swapped. 1: Data is swapped in word (16-bit) units.
1	BYTESWAP	0	R/W	Byte Swap Swaps data in byte (8-bit) units. 0: Data is not swapped. 1: Data is swapped in byte (8-bit) units.
0	BITSWAP	0	R/W	Bit Swap Swaps data in bit units. 0: Data is not swapped. 1: Data is swapped in 1-bit units.

### 19.2.2.10 $\alpha$ -Map Area Start Address Register (ASAR)

Address: H'E6EC0064

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
	—	—	—	ASA													
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	ASA													—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	

Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	—	R	Reserved
28 to 4	ASA	Un-defined	R/W	$\alpha$ -Map Area Start Address (A28 to A4) Specifies the memory area to be used as the $\alpha$ -map work area. The physical address set in this register becomes the physical address for the $\alpha$ -map coordinate origin. The start physical address (bits A28 to A4) of the $\alpha$ -map area is set in 16-byte units. Even in 32-bit addressing mode, write the lower 29 bits of the specified 32-bit address to bits 28 to 4.
3 to 0	—	—	R	Reserved

### 19.2.2.11 $\alpha$ -Map Stride Register (ASTRR)

Address: H'E6EC0068

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	—	—	—	ASTR											—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	

Bit	Bit Name	Initial Value	R/W	Description
31 to 13	—	—	R	Reserved
12 to 3	ASTR	Un-defined	R/W	$\alpha$ -Map Stride (b12 to b3) Specifies the stride of the $\alpha$ -map area in pixel units. Set the value in the range of $8 \leq \text{ASTRIDE} \leq 4096$ in 8-pixel units.
2 to 0	—	—	R	Reserved

**19.2.2.12 Address Extension Register (ADREXTR)**

Address: H'E6EC006C

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	ADREXT			—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 29	ADREXT	000	R/W	Address Extension (A31 to A29) Specifies the upper three bits (A31 to A29) of the address to be output to the AXI bus.
28 to 0	—	—	R	Reserved

**19.2.2.13 Return Address STK Register (RTNSTKR)**

Address: H'E6EC0074

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
	—	—	—	RTNSTK													
Initial value:	—	—	—	0	0	0	0	0	0	0	0	0	0	0	0	0	
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	RTNSTK														—	—	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

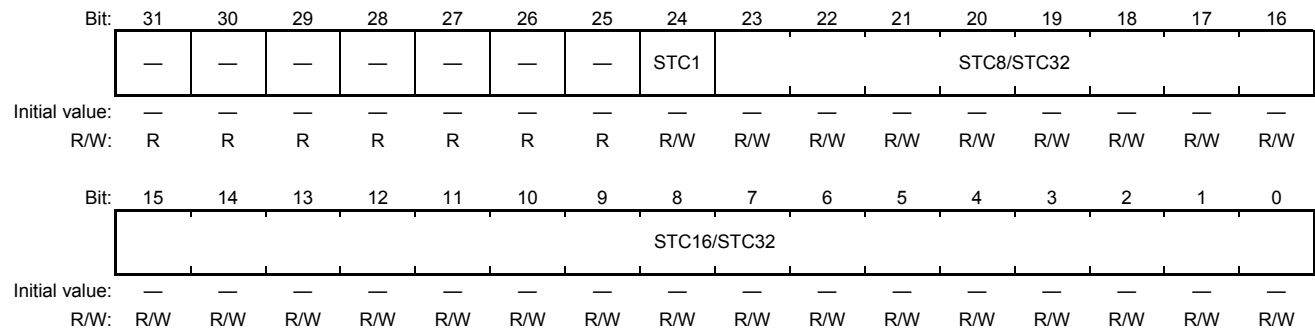
Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	—	R	Reserved
28 to 2	RTNSTK	H'0000000	R	Return Address STK (A28 to A2) Stores the return address when the rendering attribute No bit is 2 in the GOSUB command. The address indicated by RTNSTKR is a longword address (bits A28 to A2).
1, 0	—	—	R	Reserved

### 19.2.3 Color Control Registers

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	—	—	—

#### 19.2.3.1 Source Transparent Color Register (STCR)

Address: H'E6EC0080

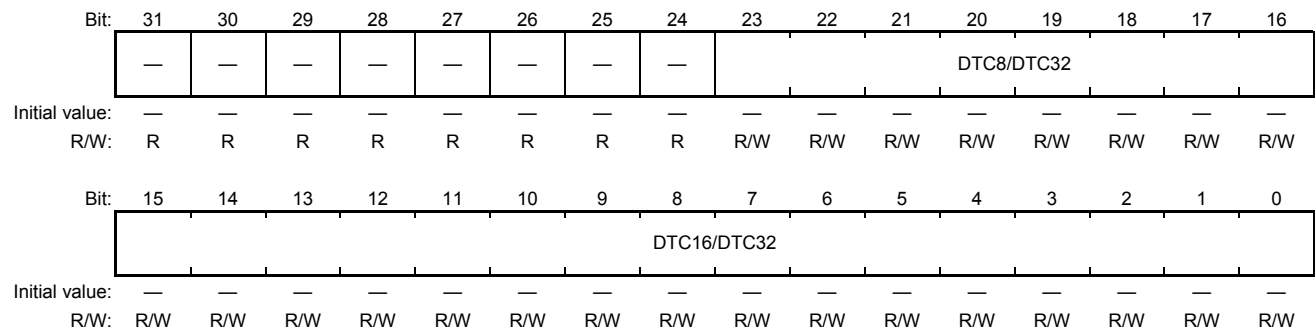


Bit	Bit Name	Initial Value	R/W	Description
31 to 25	—	—	R	Reserved
24	STC1	Un-defined	R/W	Source Transparent Color 1 Transparent color for 1-bit/pixel source
23 to 16	STC8/ STC32	Un-defined	R/W	Source Transparent Color 8 Transparent color for 8-bit/pixel source Transparent color for 32-bit/pixel source R
15 to 0	STC16/ STC32	Un-defined	R/W	Source Transparent Color 16 Transparent color for 16-bit/pixel source Transparent color for 32-bit/pixel source G and B

- Notes:
- For 16-bit/pixel source data, use the same format specified by the SPF bit in the rendering control register (RCLR).
  - When SPF = 1 (ARGB = 1555), the A value is not compared.
  - If the source data are 32-bit/pixel, specify the R, G, and B components in bits 23 to 0, in that order.

### 19.2.3.2 Destination Transparent Color Register (DTCR)

Address: H'E6EC0084

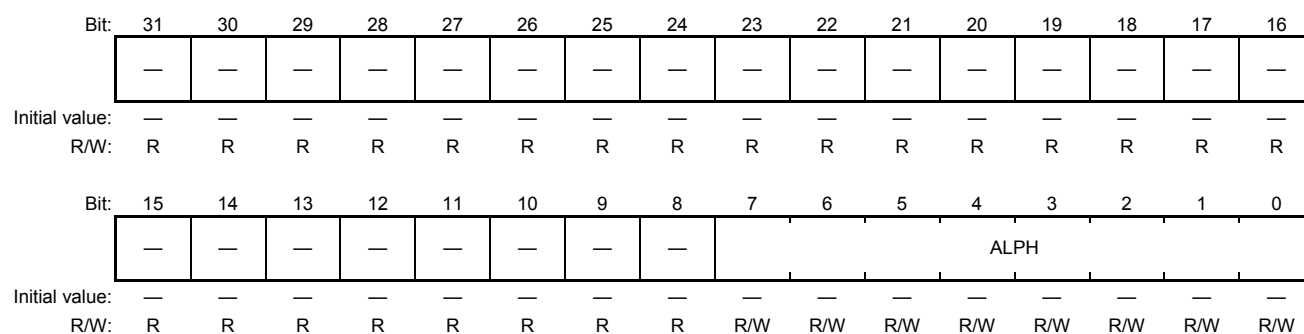


Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	—	R	Reserved
23 to 16	DTC8/ DTC32	Un-defined	R/W	Destination Transparent Color 8 Transparent color for 8-bit/pixel destination Transparent color for 32-bit/pixel destination (R components)
15 to 0	DTC16/ DTC32	Un-defined	R/W	Destination Transparent Color 16 Transparent color for 16-bit/pixel destination Transparent color for 32-bit/pixel destination (G or B components)

- Notes:
1. For 16-bit/pixel destination data, use the same format specified by the DPF bit in the rendering control register (RCLR).
  2. When DPF = 1 (ARGB = 1555), the A value is not compared.
  3. If the destination data are 32-bit/pixel, specify the R, G, and B components in bits 23 to 0, in that order.

### 19.2.3.3 Alpha Value Register (ALPHR)

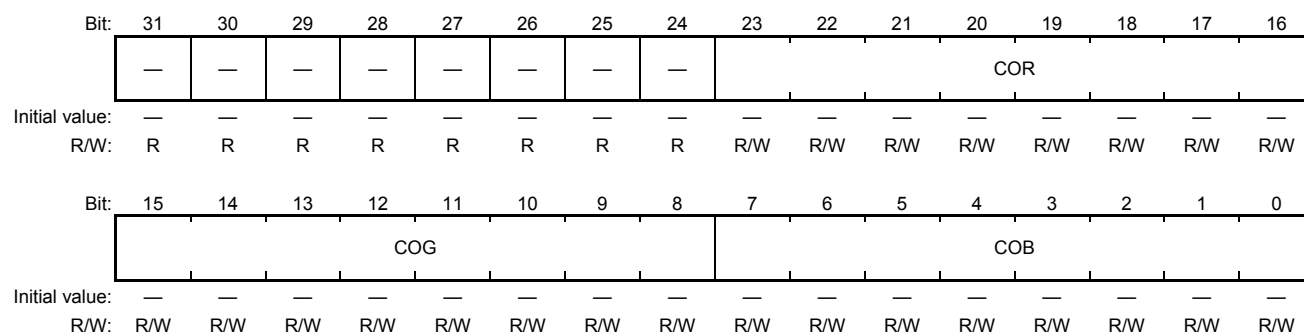
Address: H'E6EC0088



Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	—	R	Reserved
7 to 0	ALPH	Un-defined	R/W	Alpha Value (b7 to b0) Specifies the alpha blending value when the rendering attribute $\alpha E$ bit is set to 1. $Destination \approx source \times ALPH/255 + destination \times (1 - ALPH/255)$ (approximate expression when ALPH is an 8-bit value).

### 19.2.3.4 Color Offset Register (COFSR)

Address: H'E6EC008C



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	—	R	Reserved
23 to 16	COR	Un-defined	R/W	Color offset R component (b23 to b16) The offset components are treated as signed integers. Negative numbers are expressed as two's complements.
15 to 8	COG	Un-defined	R/W	Color offset G component (b15 to b8) The offset components are treated as signed integers. Negative numbers are expressed as two's complements.
7 to 0	COB	Un-defined	R/W	Color offset B component (b7 to b0) The offset components are treated as signed integers. Negative numbers are expressed as two's complements.

**19.2.3.5 A Value 8 Register (AVALUE8R)**

Address: H'E6EC0098

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	AVALUE8							
Initial value:	—	—	—	—	—	—	—	—	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	—	R	Reserved
7 to 0	AVALUE8	H'00	R/W	A value 8 The A value is for drawing when GBM2 = 1 and SAU = 0.

### 19.2.3.6 Alpha Test Control Register (ATCLR)

Address: H'E6EC009C

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	SATSEL				—	—	—	—	SATRV						
Initial value:	—	0	0	0	—	—	—	—	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	DATSEL				—	—	—	—	DATRV						
Initial value:	—	0	0	0	—	—	—	—	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	—	—	R	Reserved
30 to 28	SATSEL	000	R/W	Source Alpha Test Mode Select This setting is enabled when GBM2 = 1 and the rendering attribute SαE is set to 1. 000: ALWAYS 001: NEVER 010: LESS 011: LEQUAL 100: EQUAL 101: GEQUAL 110: GREATER 111: NEQUAL
27 to 24	—	—	R	Reserved
23 to 16	SATRV	H'00	R/W	Source Alpha Test Reference Value Reference value of the source alpha test
15	—	—	R	Reserved
14 to 12	DATSEL	000	R/W	Destination Alpha Test Mode Select Enabled when GBM2 = 1 and RCL2R/DAE = 1 000: ALWAYS 001: NEVER 010: LESS 011: LEQUAL 100: EQUAL 101: GEQUAL 110: GREATER 111: NEQUAL
11 to 8	—	—	R	Reserved
7 to 0	DATRV	H'00	R/W	Destination Alpha Test Reference Value Reference value of the destination alpha test



## 19.2.4 Rendering Control Registers

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	—	—	—

### 19.2.4.1 Rendering Control Register (RCLR)

Address: H'E6EC00C0

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	SAEP	—	STP	DTP	—	—	SPF	DPF	—	GBM	SAU	A VALUE
Initial value:	0	0	0	0	0	0	0	0	—	—	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R	R/W	R/W	R	R	R/W	R/W	R	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	BDS	—	—	—	LaE	2DV CLPE	—	—	—	NAA	WLM	LPCE	COM	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
R/W:	R	R	R/W	R/W	R	R	R/W	R/W	R/W	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 28	—	All 0	R	Reserved
27	SAEP	0	R/W	Source Alpha Enable Polarity When source alpha is set to be enabled in the rendering attributes, this bit selects whether alpha blending is performed when the A value of the source data is 1 or 0. 0: Alpha blending is performed when the source data A value is 1. The source data is drawn back as is when the A value is 0. 1: Alpha blending is performed when the source data A value is 0. The source data is drawn back as is when the A value is 1. Note: This setting is ignored when GBM2 = 1.
26	—	0	R	Reserved
25	STP	0	R/W	Source Transparent Color Polarity Selects whether source transparency occurs when the source data and the value set in the source transparent color register match or do not match. 0: Source transparency at a match 1: Source transparency at an unmatched
24	DTP	0	R/W	Destination Transparent Color Polarity Selects whether destination transparency occurs when the destination data and the value set in the destination transparent color register match or do not match. 0: Destination transparency at a match 1: Destination transparency at an unmatched
23, 22	—	—	R	Reserved

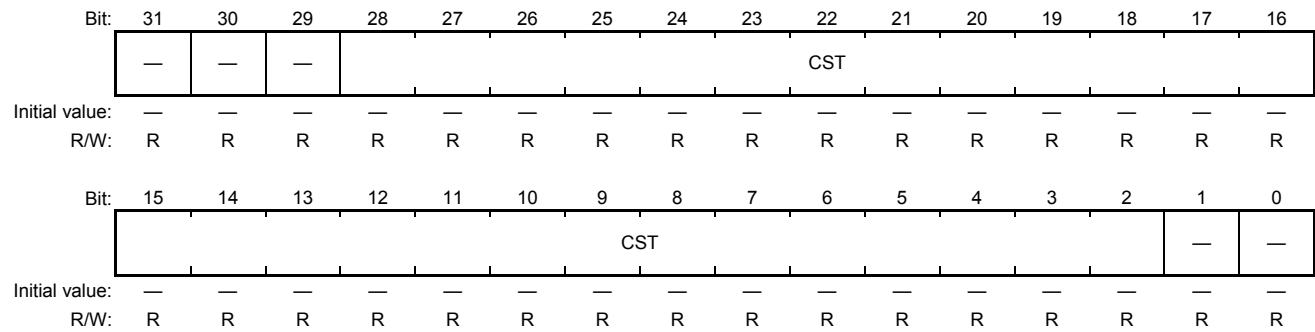
Bit	Bit Name	Initial Value	R/W	Description
21	SPF	0	R/W	<p>Source Pixel Format</p> <p>Specifies the pixel format for the multi-valued source. This setting is valid only for a multi-valued 16-bit/pixel source. This bit should be cleared to 0 for an 8-bit/pixel destination. Set this bit to match the destination pixel format.</p> <p>0: RGB = 565 format 1: ARGB = 1555 format</p>
20	DPF	0	R/W	<p>Destination Pixel Format</p> <p>Specifies the pixel format for the destination. This setting is valid only for a 16-bit/pixel destination. This bit should be cleared to 0 for an 8-bit/pixel destination. Set this bit to match the multi-valued source pixel format.</p> <p>0: RGB = 565 format 1: ARGB = 1555 format</p>
19	—	0	R	Reserved
18	GBM	0	R/W	<p>Graphics Bit Mode</p> <p>Specifies the graphics bit mode for the multi-valued source and destination.</p> <p>0: 8-bit/pixel 1: 16-bit/pixel</p>
17	SAU	0	R/W	<p>Source Value A Use</p> <p>When the pixel format of the source and destination is the ARGB format, drawing is performed while referencing the source value A as the destination value A.</p> <p>GBM2 = 0:</p> <p>0: The destination value A is drawn as AVALUE. 1: The destination value A is drawn referencing the source value A.</p> <p>Note: When SAU = 1, the value A of the command parameter Color0 or Color1 is referenced in a binary source reference command and the value A of the command parameter Color is referenced in a monochrome specification command.</p> <p>In the LINED command, the value A of the destination is written back, regardless of the settings of the SAU and AVALUE bits.</p> <p>GBM2 = 1:</p> <p>0: The destination value A is drawn as AVALUE8R. 1: The destination A values are drawn as the A value of command parameters Color0 or Color1 in the case of a command that refers to a binary source, the A value of the Color parameter in the case of a command that refers to a monochromatic source, and by reference to the A values (8-bit) of the source in the case of a command that refers to a multi-color source.</p>
16	AVALUE	0	R/W	<p>Value A</p> <p>When the pixel format of the source and destination is the ARGB format, drawing is performed with the destination value A as 0 or 1.</p> <p>0: The destination value A is drawn as 0. 1: The destination value A is drawn as 1.</p> <p>Note: This setting is ignored when GBM2 = 1.</p>
15, 14	—	00	R	Reserved

Bit	Bit Name	Initial Value	R/W	Description
13, 12	BDS	00	R/W	<p>Thickness Direction Boundary Select</p> <p>When the LINEA, LINEB, LINEC, RLINEA, RLINEB, or RLINEC command is executed and a bold line has been specified, these bits select the boundary at which the thickness direction changes.</p> <p>00: The thickness direction changes at the boundary A.</p> <p>01: The thickness direction changes at the boundary B.</p> <p>10: The thickness direction changes at the boundary C.</p> <p>11: The thickness direction changes at the boundary D.</p>
11, 10	—	00	R	Reserved
9, 8	LαE	00	R/W	<p>Line Alpha Enable</p> <p>The source data (color expanded data for a binary source and the specified color for the monochrome specification) and ground data are alpha blended and drawn in the LINEA, LINEB, LINEC, RLINEA, RLINEB, or RLINEC command. The alpha value is set in the alpha value register (ALPHR).</p> <p>A thick line is drawn by the 4-point drawing method, so some pixels that have been alpha blended twice appear, and in some cases the result of the drawing is unsatisfactory. Accordingly, to prevent the same pixel from being written over twice, it is recommended that the DAE bit in RCL2R be used at the same time.</p> <p>00: Alpha blending is not performed.</p> <p>01: Reserved</p> <p>10: Alpha blending is performed.</p> <p>11: Only the value A of ARGB = 1555 is rewritten. RGB data are not rewritten. The value A is rewritten in accordance with the SAU and AVALUE settings.</p> <p>Only the value A (8 bit) of ARGB = 8888 is rewritten. RGB data are not rewritten. The value A is rewritten in accordance with the SAU and A VALUE 8 register settings.</p> <p>Notes: 1. When the RGB = 565 format and 8 bits/pixel have been set, specify LαE = 00.</p> <p>2. For commands other than the LINEA, LINEB, LINEC, RLINEA, RLINEB, and RLINEC, specify LαE = 00.</p> <p>3. These bits are not decoded with a command, so these bits must be set or cleared in each relevant command.</p>

Bit	Bit Name	Initial Value	R/W	Description
7	2DVCLPE	0	R/W	<p>2-Dimensional Vertex Clipping Enable</p> <p>Generates intersection points with the 2-dimensional vertex clipping area (ANDed area of the system clipping area, user clipping area, and relative user clipping area) and performs drawing using the generated points in the LINEA/B/C/D, RLINEA/B/C/D, LINEWC, RLINEWC, FTRAPC, RFTRAPC (circumscribed quadrangle and trapezoid vertices), CLRWC, and POLYGON4A/B/C (BLKE = 1) commands.</p> <p>0: Intersection points with the 2-dimensional vertex clipping area are not generated.</p> <p>1: Intersection points with the 2-dimensional vertex clipping area are generated and drawing is performed using the generated points.</p> <p>Notes: 1. This specification is invalid for commands other than above.</p> <p>2. Drawing tracks may not match between 2DVCLPE = 0 and 2DVCLPE = 1.</p> <p>3. Patterns do not match.</p> <p>4. For the intersection edge between the (R)FTRAPC screen and 2-dimensional clipping area screen, (R)LINE and (R)LINEWC commands do not perform drawing.</p>
6 to 4	—	All 0	R	Reserved
3	NAA	0	R/W	<p>New Antialias Mode</p> <p>Performs antialiasing for horizontal, vertical, and 45-degree diagonal line segments.</p> <p>0: Antialiasing is not performed for horizontal, vertical, and 45-degree diagonal line segments.</p> <p>1: Antialiasing is performed for horizontal, vertical, and 45-degree diagonal line segments.</p>
2	WLM	1	R/W	<p>Bold Line Mode</p> <p>Selects thickness mode.</p> <p>0: Jaggy reduction is disabled.</p> <p>1: Jaggy reduction is enabled. (initial value)</p>
1	LPCE	0	R/W	<p>Line Pre-Clipping Enable</p> <p>This bit is valid for the (R)LINE and (R)LINEW type commands. When this bit is set to 1, pre-clipping is performed in line-segment units in the 2-dimensional clipping areas (system clipping, user clipping, and relative user clipping areas). If a line segment in the middle is pre-clipped, the pattern continuity is broken (the pattern starts from the final point of the line segment previously drawn).</p> <p>0: Pre-clipping is not performed.</p> <p>1: Pre-clipping is performed in line-segment units in the 2-dimensional clipping areas.</p>
0	COM	0	R/W	<p>Connection Drawing Mask</p> <p>Selects whether the linkage parts of bold lines are drawn or not.</p> <p>0: Linkage parts of bold lines are drawn.</p> <p>1: Linkage parts of bold lines are not drawn.</p>

### 19.2.4.2 Command Status Register (CSTR)

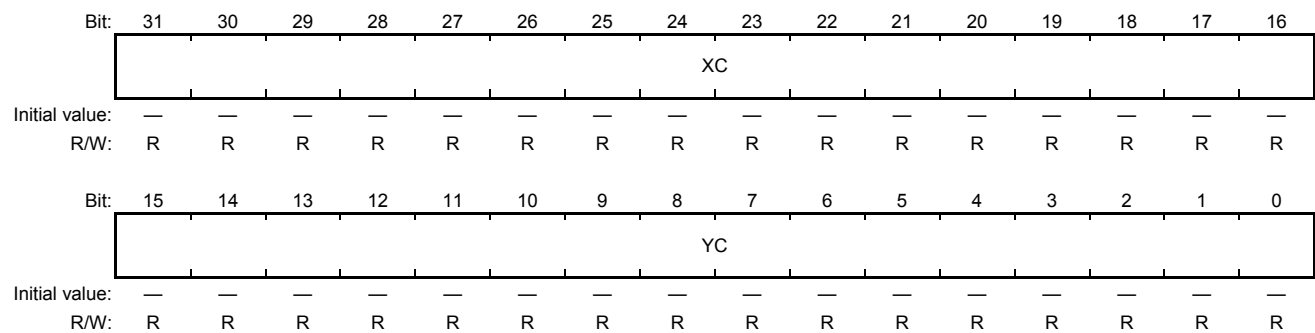
Address: H'E6EC00C4



Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	—	R	Reserved
28 to 2	CST	Un-defined	R	Command Status (A28 to A2) Stores the address of the fetched command word (op code word). The address indicated by CSTR is a longword address (bits A28 to A2).
1, 0	—	—	R	Reserved

### 19.2.4.3 Current Pointer Register (CURR)

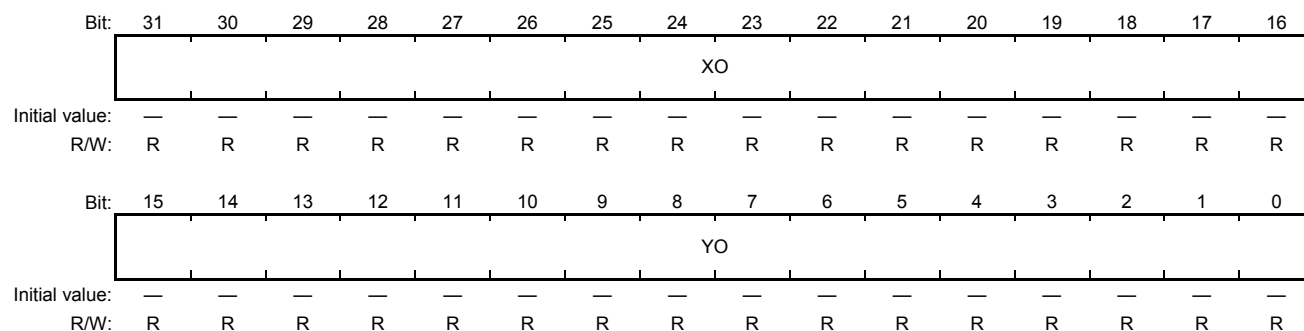
Address: H'E6EC00C8



Bit	Bit Name	Initial Value	R/W	Description
31 to 16	XC	Un-defined	R	Current Pointer X The X coordinate of the current pointer
15 to 0	YC	Un-defined	R	Current Pointer Y The Y coordinate of the current pointer

### 19.2.4.4 Local Offset Register (LCOR)

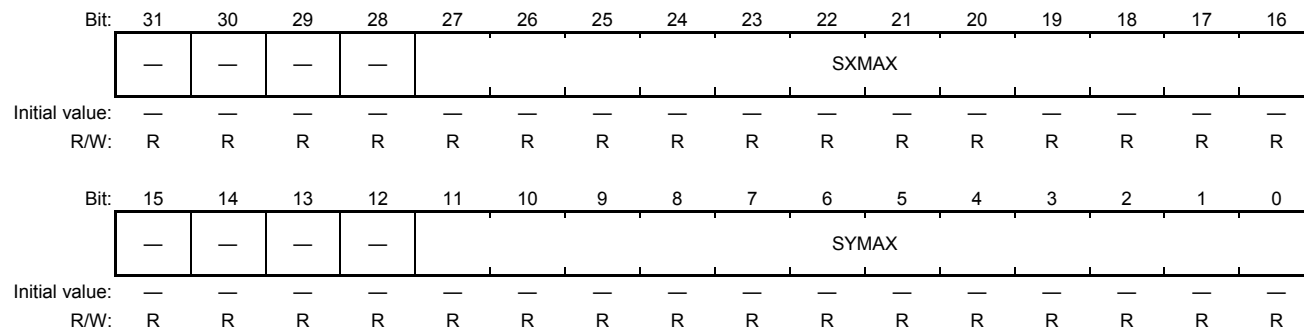
Address: H'E6EC00CC



Bit	Bit Name	Initial Value	R/W	Description
31 to 16	XO	Un-defined	R	Local Offset X The X coordinate of the local offset
15 to 0	YO	Un-defined	R	Local Offset Y The Y coordinate of the local offset

### 19.2.4.5 System Clipping Area MAX Register (SCLMAR)

Address: H'E6EC00D0



Bit	Bit Name	Initial Value	R/W	Description
31 to 28	—	—	R	Reserved
27 to 16	SXMAX	Un-defined	R	System Clipping XMAX The XMAX of the system clipping coordinates.
15 to 12	—	—	R	Reserved
11 to 0	SYMAX	Un-defined	R	System Clipping YMAX The YMAX of the system clipping coordinates.

Note: When setting this register by the WPR command, set the maximum values of the drawing range (max. 4,095. SXMAX < DSTRR).

### 19.2.4.6 User Clipping Area MIN Register (UCLMIR)

Address: H'E6EC00D4

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—				UXMIN											
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—				UYMIN											
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 28	—	—	R	Reserved
27 to 16	UXMIN	Un-defined	R	User Clipping XMIN The XMIN of the user clipping coordinates.
15 to 12	—	—	R	Reserved
11 to 0	UYMIN	Un-defined	R	User Clipping YMIN The YMIN of the user clipping coordinates.

Note: When setting this register by the WPR command, set UXMIN and UYMIN in the following ranges:  
 $0 \leq UXMIN \leq UXMAX \leq SXMAX \leq 4,095$ ,  $0 \leq UYMIN \leq UYMAX \leq SYMAX \leq 4,095$ .

### 19.2.4.7 User Clipping Area MAX Register (UCLMAR)

Address: H'E6EC00D8

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—				UXMAX											
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—				UYMAX											
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 28	—	—	R	Reserved
27 to 16	UXMAX	Un-defined	R	User Clipping XMAX The XMAX of the user clipping coordinates.
15 to 12	—	—	R	Reserved
11 to 0	UYMAX	Un-defined	R	User Clipping YMAX The YMAX of the user clipping coordinates.

Note: When setting this register by the WPR command, set UXMAX and UYMAX in the following ranges:  
 $0 \leq UXMIN \leq UXMAX \leq SXMAX \leq 4,095$ ,  $0 \leq UYMIN \leq UYMAX \leq SYMAX \leq 4,095$ .

### 19.2.4.8 Relative User Clipping Area MIN Register (RUCLMIR)

Address: H'E6EC00DC

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	RUXMIN											
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	RUYMIN											
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 28	—	—	R	Reserved
27 to 16	RUXMIN	Un-defined	R	Relative User Clipping XMIN The XMIN of the relative user clipping coordinates (offset values added to the local offset).
15 to 12	—	—	R	Reserved
11 to 0	RUYMIN	Un-defined	R	Relative User Clipping YMIN The YMIN of the relative user clipping coordinates (offset values added to the local offset).

Note: When setting this register by the WPR command, set RUXMIN and RUYMIN in the following ranges:  
 $0 \leq \text{RUXMIN} \leq \text{RUXMAX} \leq \text{SXMAX} \leq 4,095 - \text{XO}$ ,  $0 \leq \text{RUYMIN} \leq \text{RUYMAX} \leq \text{SYMAX} \leq 4,095 - \text{YO}$ .  
 For details on the setting ranges, see section 19.3.5 (5), Relative Clipping Specification (RCLIP).



**19.2.4.9 Relative User Clipping Area MAX Register (RUCLMAR)**

Address: H'E6EC00E0

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	RUXMAX											
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	RUYMAX											
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 28	—	—	R	Reserved
27 to 16	RUXMAX	Un-defined	R	Relative User Clipping XMAX The XMAX of the relative user clipping coordinates (offset values added to the local offset).
15 to 12	—	—	R	Reserved
11 to 0	RUYMAX	Un-defined	R	Relative User Clipping YMAX The YMAX of the relative user clipping coordinates (offset values added to the local offset).

Note: When setting this register by the WPR command, set RUXMAX and RUYMAX in the following ranges:  
 $0 \leq \text{RUXMIN} \leq \text{RUXMAX} \leq \text{SXMAX} \leq 4,095 - \text{XO}$ ,  $0 \leq \text{RUYMIN} \leq \text{RUYMAX} \leq \text{SYMAX} \leq 4,095 - \text{YO}$ .  
 For details on the setting ranges, see section 19.3.5 (5), Relative Clipping Specification (RCLIP).

### 19.2.4.10 Rendering Control 2 Register (RCL2R)

Address: H'E6EC00F0

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	DAE	PSTYL E	PXSIZ		PYSIZ	
Initial value:	0	0	0	0	0	0	—	—	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	1	0	0	—	0	0	0	0	0	0	0	0	1	0	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 26	—	All 0	R	Reserved
25, 24	—	—	R	Reserved
23, 22	—	All 0	R	Reserved
21	DAE	0	R/W	<p>Destination Alpha Enable</p> <p>This bit is used in combination with the alpha blend enable (<math>\alpha</math>E) bit and line alpha enable (L<math>\alpha</math>E) bit. In the ARGB = 1555 format, only the pixels whose destination value A is 1 are alpha blended. Pixels whose destination value A is 0 are not drawn.</p> <p>When GBM2 = 0:</p> <p>0: Alpha blending is performed regardless of the destination value A.</p> <p>1: Only the pixels whose destination value A is 1 are alpha blended.</p> <p>When GBM2 = 1:</p> <p>0: Alpha blending is performed regardless of the destination value A.</p> <p>1: Only when the destination value A has passed the destination alpha test is alpha blended.</p> <p>Notes: 1. Clear this bit to 0 for the RGB = 565 format or at 8-bit/pixel drawing.</p> <p>2. Clear this bit to 0 for commands other than POLYGON4A, POLYGON4B, POLYGON4C, LINEA, LINEB, LINEC, RLINEA, RLINEB, and RLINEC.</p> <p>3. Clear this bit to 0 when the alpha blend enable bit (<math>\alpha</math>E) is 0 or the line alpha enable (L<math>\alpha</math>E) bit is 0.</p> <p>4. This bit is not decoded by a command so it must be set or cleared in each relevant command.</p>

Bit	Bit Name	Initial Value	R/W	Description
20	PSTYLE	0	R/W	<p>Pattern Style Enable</p> <p>This bit is used in combination with the source style specification (STYLE). The source pattern is created repeatedly in the pattern size based on the destination coordinates.</p> <p>0: Pattern style disabled</p> <p>1: The source pattern is created based on the destination coordinates.</p> <p>Notes: 1. Set the source offset TXOFS and TYOFS to 0.            2. Clear this bit to 0 when the source style specification bit (STYLE) is 0.            3. Clear the source address specification bit (SS) to 0.            4. Clear this bit to 0 for commands other than POLYGON4A and POLYGON4B.            5. This bit is not decoded by a command so it must be set or cleared in each relevant command.</p>
19, 18	PXSIZE	00	R/W	<p>Pattern X Size</p> <p>These bits specify the pattern X size when the pattern style enable (PSTYLE) bit is 1.</p> <p>00: Pattern X size = 8 pixels            01: Pattern X size = 16 pixels            10: Pattern X size = 32 pixels            11: Pattern X size = 64 pixels</p> <p>Note: Set the specified pattern X size (8, 16, 32, or 64) in the source size TDX.</p>
17, 16	PYSIZE	00	R/W	<p>Pattern Y Size</p> <p>These bits specify the pattern Y size when the pattern style enable (PSTYLE) bit is 1.</p> <p>00: Pattern Y size = 8 pixels            01: Pattern Y size = 16 pixels            10: Pattern Y size = 32 pixels            11: Pattern Y size = 64 pixels</p> <p>Note: Set the specified pattern Y size (8, 16, 32, or 64) in the source size TDY.</p>
15	—	0	R	Reserved
14	—	1	R	Reserved
13, 12	—	00	R	Reserved
11	—	—	R	Reserved
10 to 3	—	All 0	R	Reserved
2	—	1	R	Reserved
1	—	0	R	Reserved
0	—	—	R	Reserved

**19.2.4.11 Pattern Offset Register (POFSR)**

Address: H'E6EC00F8

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	POFSX											
Initial value:	—	—	—	—	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	POFSY											
Initial value:	—	—	—	—	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 28	—	—	R	Reserved
27 to 16	POFSX	H'000	R/W	Pattern Offset X These bits specify the pattern offset value in the X direction as a 16-bit integer when the pattern style enable bit (PSTYLE) is set to 1. Negative numbers are expressed as two's complements.
15 to 12	—	—	R	Reserved
11 to 0	POFSY	H'000	R/W	Pattern Offset Y These bits specify the pattern offset value in the Y direction as a 16-bit integer when the pattern style enable bit (PSTYLE) is set to 1. Negative numbers are expressed as two's complements.

## 19.2.5 Coordinate Transformation Control Registers

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	—	—	—

### 19.2.5.1 Coordinate Transformation Control Register (GTRCR)

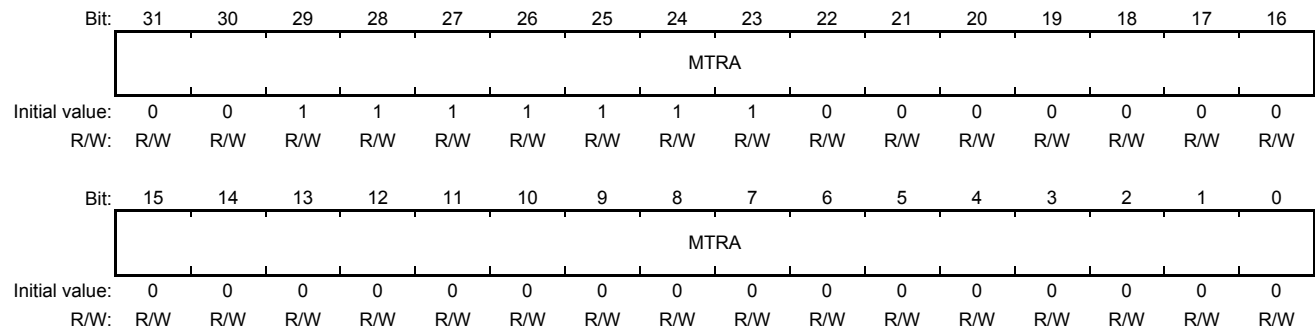
Address: H'E6EC0100

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	GTE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	AFE
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	GTE	0	R/W	<p>Coordinate Transformation Enable</p> <p>Performs coordinate transformation.</p> <p>0: Coordinate transformation is not performed. The rendering attribute MTRE bit is disabled.</p> <p>1: The rendering attribute MTRE bit is enabled.</p>
30 to 1	—	—	R	Reserved
0	AFE	0	R/W	<p>Affine Transformation Enable</p> <p>Does not perform W division and offset addition at coordinate transformation. This bit is enabled when both the rendering attribute MTRE bit and GTE bit are set to 1.</p> <p>0: The vertex coordinates X' and Y' are obtained by dividing the matrix operation result coordinates TX and TY by WC, and then adding the offset values.</p> $X' = TX/WC + GTROFSX$ $Y' = TY/WC + GTROFSY$ <p>GTROFSX and GTROFSY are set in the coordinate transformation offset X register (GTROFSXR) and coordinate transformation offset Y register (GTROFSYR), respectively.</p> <p>1: The vertex coordinates X' and Y' are the matrix operation result coordinates TX and TY.</p> $X' = TX$ $Y' = TY$

### 19.2.5.2 Matrix Parameter A Register (MTRAR)

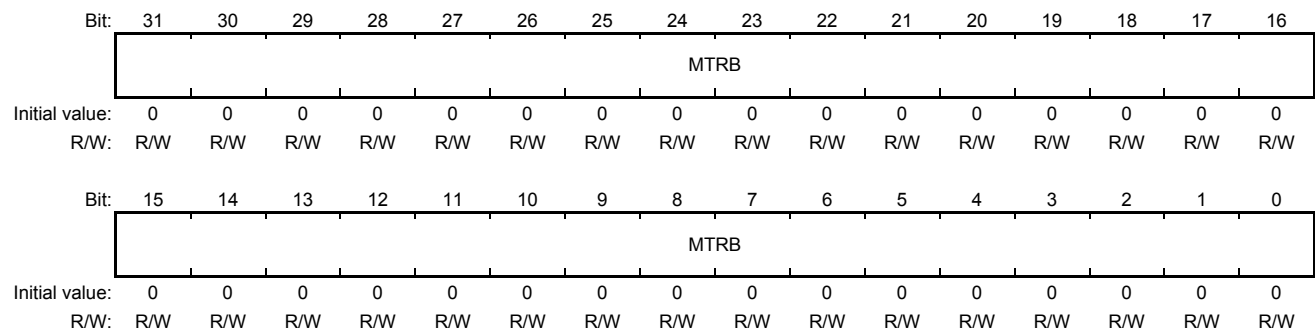
Address: H'E6EC0104



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	MTRA	H'3F800000	R/W	Matrix Parameter A Matrix parameter A at coordinate transformation. Specify in the single-precision floating-point format defined by the IEEE754 standard.

### 19.2.5.3 Matrix Parameter B Register (MTRBR)

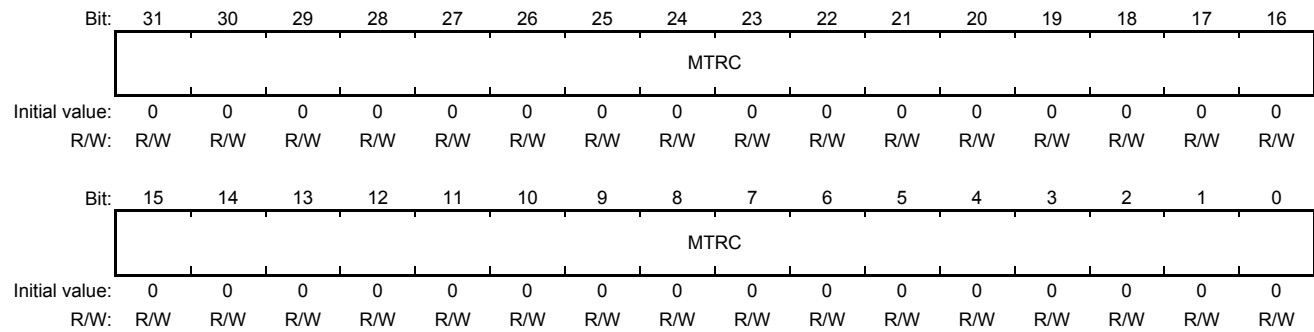
Address: H'E6EC0108



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	MTRB	H'00000000	R/W	Matrix Parameter B Matrix parameter B at coordinate transformation. Specify in the single-precision floating-point format defined by the IEEE754 standard.

### 19.2.5.4 Matrix Parameter C Register (MTRCR)

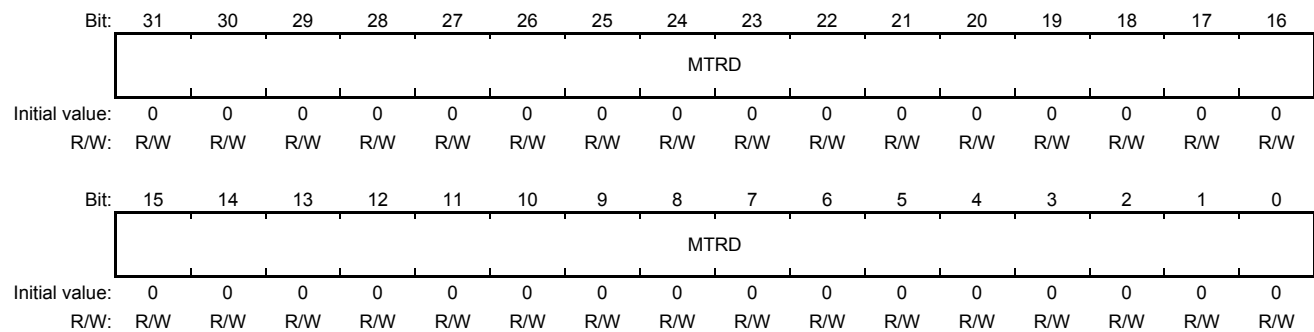
Address: H'E6EC010C



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	MTRC	H'00000000	R/W	Matrix Parameter C Matrix parameter C at coordinate transformation. Specify in the single-precision floating-point format defined by the IEEE754 standard.

### 19.2.5.5 Matrix Parameter D Register (MTRDR)

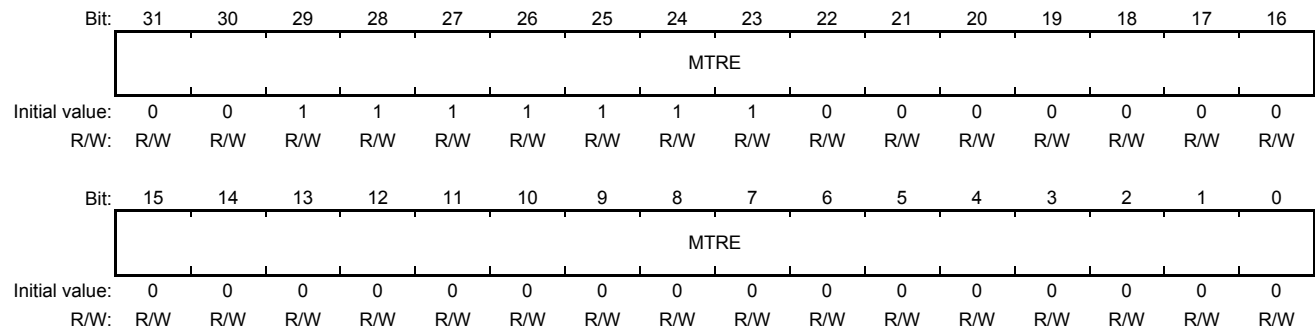
Address: H'E6EC0110



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	MTRD	H'00000000	R/W	Matrix Parameter D Matrix parameter D at coordinate transformation. Specify in the single-precision floating-point format defined by the IEEE754 standard.

**19.2.5.6 Matrix Parameter E Register (MTRER)**

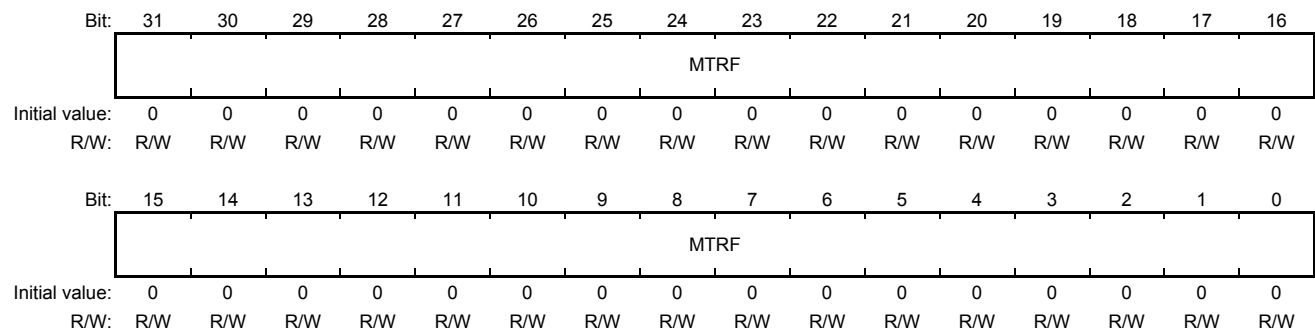
Address: H'E6EC0114



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	MTRER	H'3F800000	R/W	Matrix Parameter E Matrix parameter E at coordinate transformation. Specify in the single-precision floating-point format defined by the IEEE754 standard.

**19.2.5.7 Matrix Parameter F Register (MTRFR)**

Address: H'E6EC0118

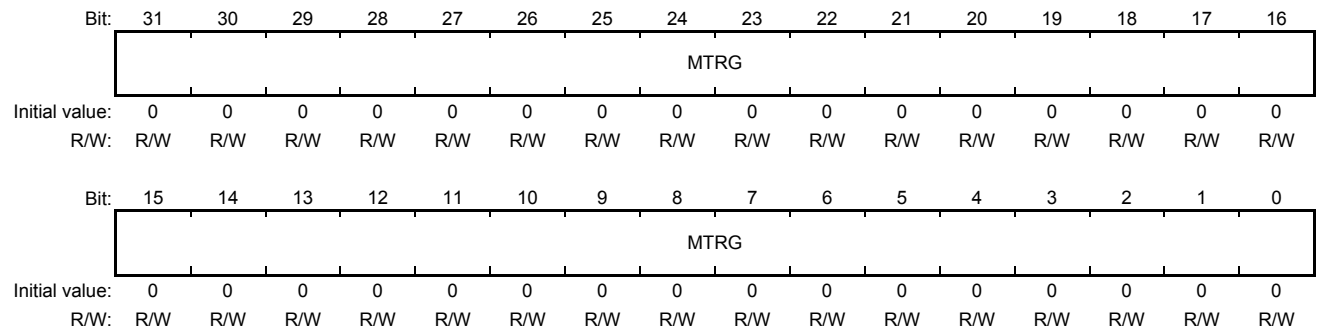


Bit	Bit Name	Initial Value	R/W	Description
31 to 0	MTRFR	H'00000000	R/W	Matrix Parameter F Matrix parameter F at coordinate transformation. Specify in the single-precision floating-point format defined by the IEEE754 standard.



**19.2.5.8 Matrix Parameter G Register (MTRGR)**

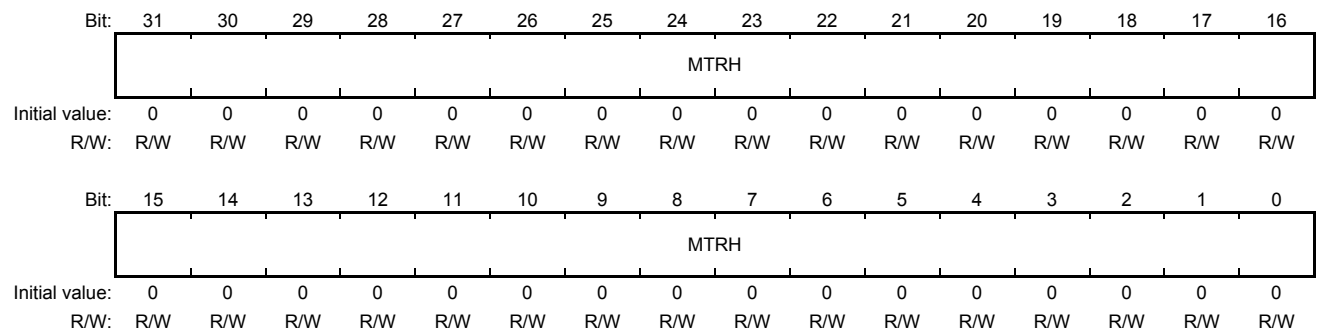
Address: H'E6EC011C



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	MTRG	H'00000000	R/W	Matrix Parameter G Matrix parameter G at coordinate transformation. Specify in the single-precision floating-point format defined by the IEEE754 standard.

**19.2.5.9 Matrix Parameter H Register (MTRHR)**

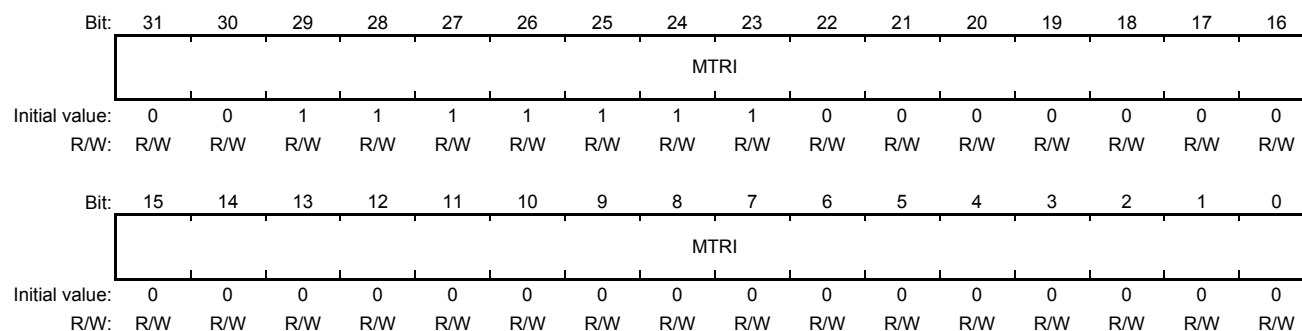
Address: H'E6EC0120



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	MTRH	H'00000000	R/W	Matrix Parameter H Matrix parameter H at coordinate transformation. Specify in the single-precision floating-point format defined by the IEEE754 standard.

### 19.2.5.10 Matrix Parameter I Register (MTRIR)

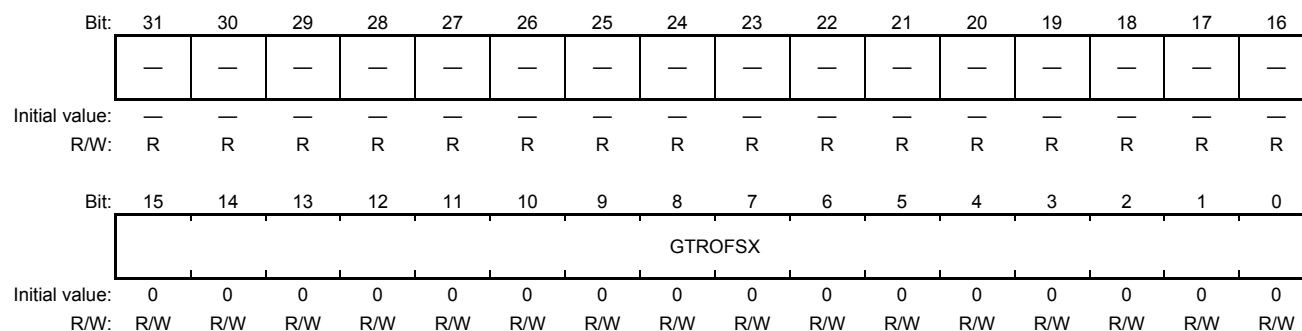
Address: H'E6EC0124



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	MTRI	H'3F800000	R/W	Matrix Parameter I Matrix parameter I at coordinate transformation. Specify in the single-precision floating-point format defined by the IEEE754 standard.

### 19.2.5.11 Coordinate Transformation Offset X Register (GTROFSXR)

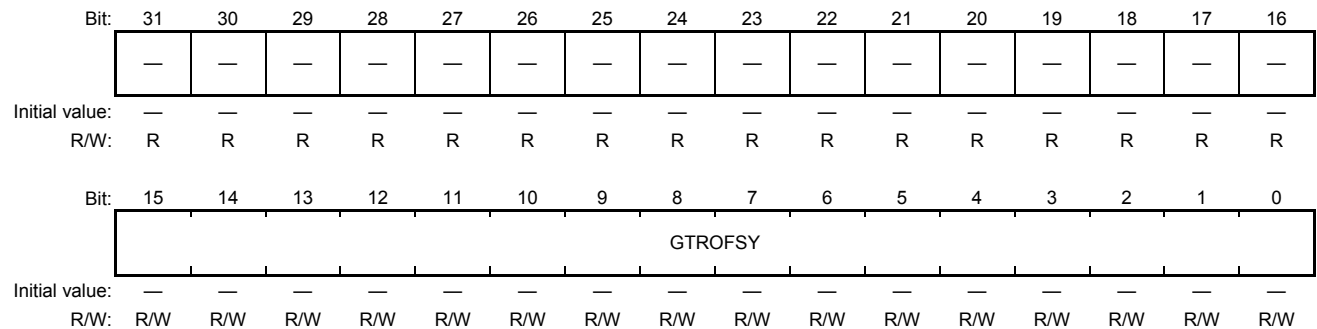
Address: H'E6EC0128



Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	—	R	Reserved
15 to 0	GTROFSX	H'0000	R/W	Coordinate Transformation Offset X Specifies the X offset value for a coordinate transformation as a 16-bit integer. Negative numbers are expressed as two's complements. GTROFSXR is initialized to H'0000 at a reset. This register is read as a value added by the RGTOFS command.

**19.2.5.12 Coordinate Transformation Offset Y Register (GTROFSYR)**

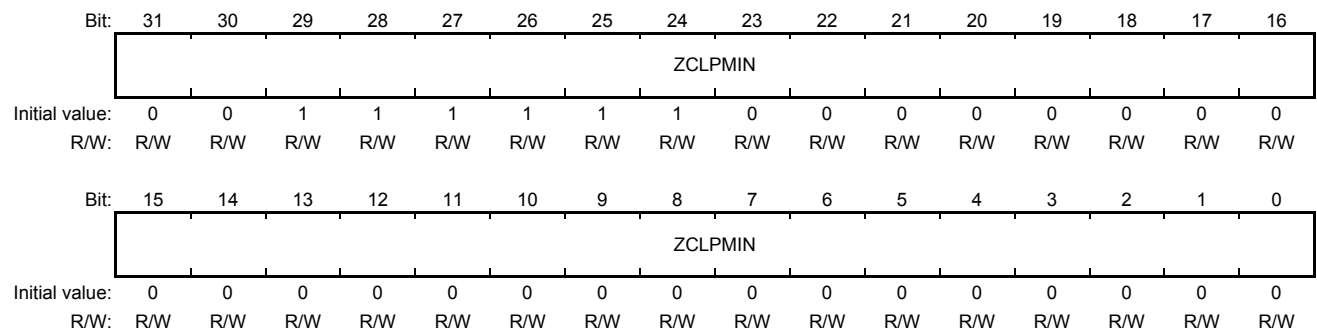
Address: H'E6EC012C



Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	—	R	Reserved
15 to 0	GTROFSY	Un-defined	R/W	Coordinate Transformation Offset Y Specifies the Y offset value at coordinate transformation as a 16-bit integer. Negative numbers are expressed as two's complements. GTROFSYR is initialized to H'0000 at a reset. This register is read as a value added by the RGTOFS command.

**19.2.5.13 Z Clipping Area MIN Register (ZCLPMINR)**

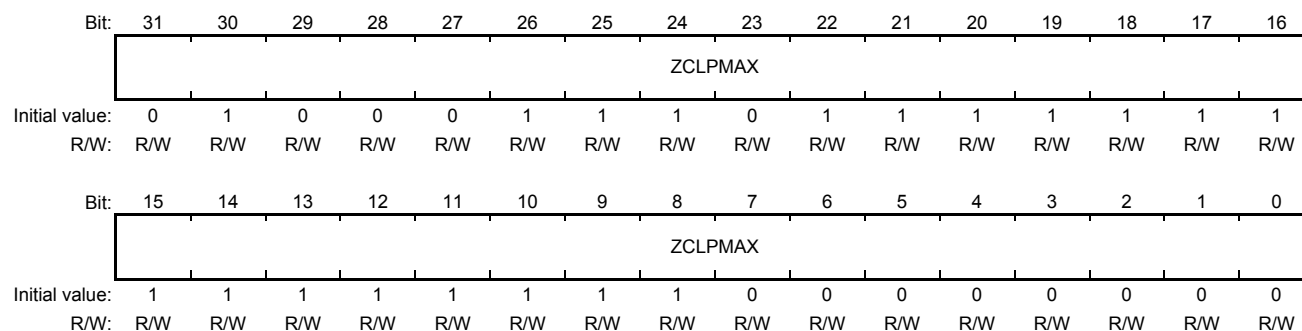
Address: H'E6EC0130



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	ZCLPMIN	H'3F000000	R/W	Z Clipping Area MIN Specifies the minimum value of the Z clipping area in the single-precision floating-point format defined by the IEEE754 standard. Since the setting is compared with the W value, set a value corresponding to W in ZCLPMINR. The value must be set within the ranges of $0 < ZCLPMIN \leq ZCLPMAX$ . (Only positive normalized values are allowed. Setting negative values, 0s, infinity, denormalized values, and NaN is prohibited.)

### 19.2.5.14 Z Clipping Area MAX Register (ZCLPMAXR)

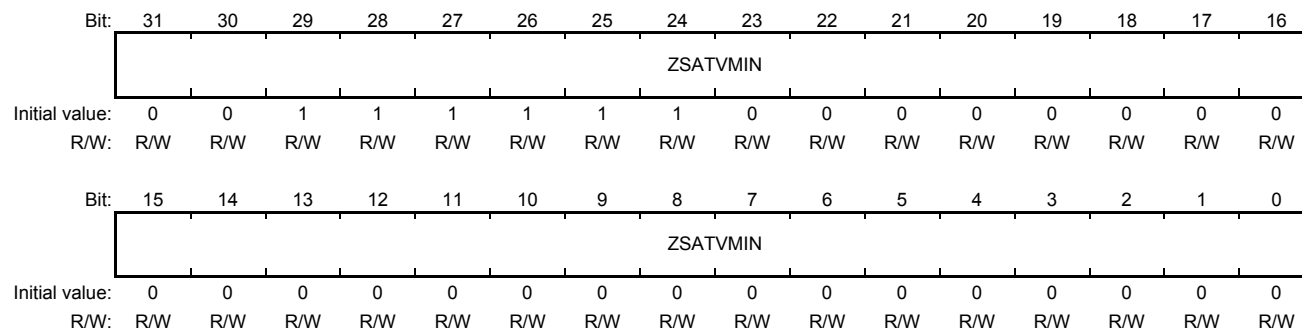
Address: H'E6EC0134



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	ZCLPMAX	H'477FFF00	R/W	<p>Z Clipping Area MAX</p> <p>Specifies the maximum value of the Z clipping area in the single-precision floating-point format defined by the IEEE754 standard. Since the setting is compared with the W value, set a value corresponding to W in ZCLPMAXR.</p> <p>The value must be set within the ranges of <math>0 &lt; ZCLPMIN \leq ZCLPMAX</math>. (Only positive normalized values are allowed. Setting negative values, 0s, infinity, denormalized values, and NaN is prohibited.)</p>

### 19.2.5.15 Z Saturation Value MIN Register (ZSATVMINR)

Address: H'E6EC0138



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	ZSATVMIN	H'3F000000	R/W	<p>Z Saturation Value MIN</p> <p>Specifies the minimum Z saturation value in the single-precision floating-point format defined by the IEEE754 standard. Since the setting is compared with the W value, set a value corresponding to W in ZSATVMINR. The value must be set within the ranges of <math>0 &lt; ZSATVMIN \leq ZCLPMIN \leq ZCLPMAX</math>. (Only positive normalized values are allowed. Setting negative values, 0s, infinity, denormalized values, and NaN is prohibited.)</p>

**19.2.5.16 2-Dimensional Vertex Clip Extension Width Register (2DVCEXTR)**

Address: H'E6EC0160

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	2DVCEXT					
Initial value:	—	—	—	—	—	—	—	—	—	—	0	0	0	1	0	1
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 6	—	—	R	Reserved
5 to 0	2DVCEXT	000101	R/W	<p>2-Dimensional Vertex Clip Extension Width</p> <p>When the 2-dimensional vertex clipping is enabled with the 2DVCLPE bit in RCLR, a 2-dimensional clipping area (ANDed area of the system clipping area, user clipping area, and relative user clipping area) is extended by the amount of the value set by this register, and the extended area is handled as a 2-dimensional vertex clipping area. Usually, a half the maximum value of the line width for bold line drawing is set for this register. The initial value is set as line width of 10.</p> <p>Note: If different values are set for the 2-dimensional clipping area and this register in each command, intersection point coordinates will differ according to the setting and drawn tracks will not match. (Care should be taken when drawing an edge line of a polygon.)</p>

## 19.2.6 Mode Control Register

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	—	—	—

### 19.2.6.1 Mode 0 Register (MD0R)

Address: H'E6EC01FC

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	GBM2	—	—	—	—	—	—	—	—
Initial value:	0	—	—	—	—	—	—	0	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R/W	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	ACDE	—	—	—	—	—	—	—	DITHE RENB
Initial value:	—	—	—	—	—	—	—	0	—	—	—	—	—	—	—	0
R/W:	R	R	R	R	R	R	R	R/W	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	—	0	R	Reserved
30 to 25	—	—	R	Reserved
24	GBM2	0	R/W	Graphic Bit Mode 0: In accord with GBM 1: ARGB8888 format
23 to 9	—	—	R	Reserved
8	ACDE	0	R/W	Anti-aliasing Coverage Drawing Enable 0: Anti-aliasing Coverage Drawing is not performed (initial value) 1: Anti-aliasing Coverage Drawing is performed When drawing the anti-aliasing line, anti-aliasing coverage is drawn to A value. And, anti-aliasing of RGB is not performed. Use this function in ARGB8888 format. In addition, do not use this function except the LINE type and RLINE type commands because it is not decoded by the commands. When the line of different colors overlap, draw on the different plane for each color.
7 to 1	—	—	R	Reserved
0	DITHERENB	0	R/W	Dither enable 0: Dithering is not performed (initial value) 1: Dithering is performed



### 19.3 Operation

#### 19.3.1 Basic Functions

##### (1) 4 × 4 Matrix Operation

A 4 × 4 matrix is used to transform the input vertex. Setting the coordinate transformation enable bit (GTE) in the coordinate transformation control register (GTRCR) to 1 and then setting the rendering attribute MTRE bit of each command to 1 executes matrix operation for the input vertex.

The following matrix equation is used for transforming the coordinates of the input vertex for 2D commands.

$$\begin{pmatrix} TX \\ TY \\ TZ \\ w \end{pmatrix} = \begin{matrix} \text{Parse transformation matrix} & \text{Affine transformation matrix} \end{matrix} \begin{pmatrix} X \\ Y \\ Z \\ 1 \end{pmatrix}$$

$$\begin{pmatrix} TX \\ TY \\ TZ \\ w \end{pmatrix} = \begin{pmatrix} 1 & 0 & P02 & P03 \\ 0 & 1 & P12 & P13 \\ 0 & 0 & P22 & P23 \\ 0 & 0 & P32 & P33 \end{pmatrix} \begin{pmatrix} m00 & m01 & m02 & m03 \\ m10 & m11 & m12 & m13 \\ m20 & m21 & m22 & m23 \\ 0 & 0 & 0 & 1 \end{pmatrix} \begin{pmatrix} X \\ Y \\ Z \\ 1 \end{pmatrix}$$

$$= \begin{pmatrix} m00+P02m20 & m01+P02m21 & m02+P02m22 & m03+P02m23 \\ m10+P12m20 & m11+P12m21 & m12+P12m22 & m13+P12m23 \\ P22m20 & P22m21 & P22m22 & P22m23 \\ P32m20 & P32m21 & P32m22 & P32m23+P33 \end{pmatrix} \begin{pmatrix} X \\ Y \\ Z \\ 1 \end{pmatrix}$$

Here the input vertex Z is 0 and the TZ output is not used, so the synthesized matrix becomes as follows:

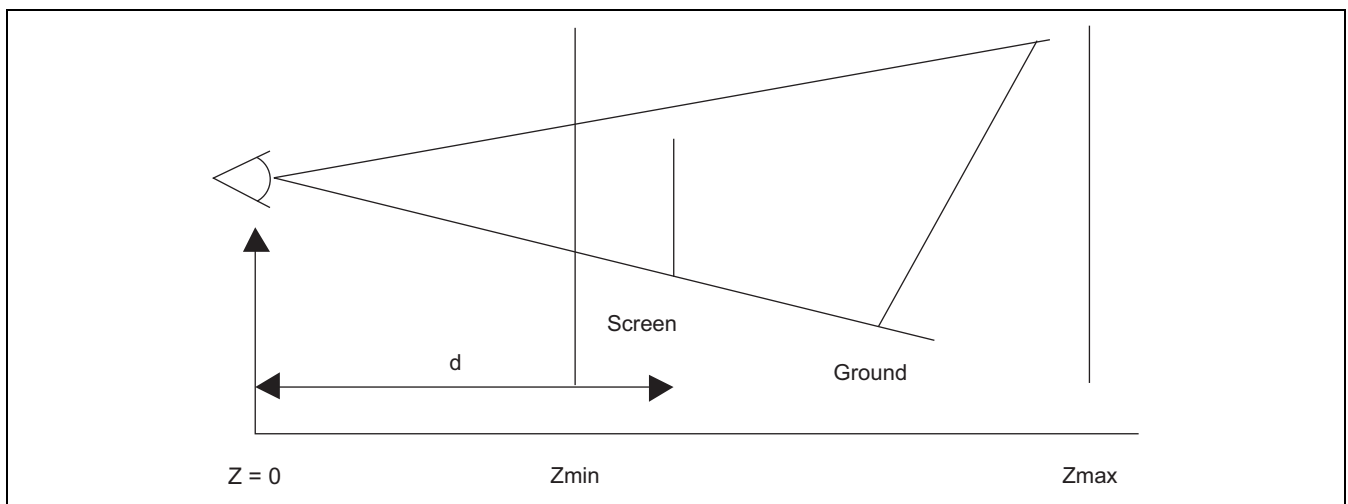
$$\begin{pmatrix} m00+P02m20 & m01+P02m21 & 0 & m03+P02m23 \\ m10+P12m20 & m11+P12m21 & 0 & m13+P12m23 \\ 0 & 0 & 0 & 0 \\ P32m20 & P32m21 & 0 & P32m20+P33 \end{pmatrix}$$

The remaining nine parameters are set to the matrix parameter A to I registers (MTRAR to MTRIR), which are coordinate transformation control registers.

The relationship between the matrix parameter registers and matrix parameters is shown below.

$$\begin{pmatrix} A & B & 0 & C \\ D & E & 0 & F \\ 0 & 0 & 0 & 0 \\ G & H & 0 & I \end{pmatrix}$$

For example, when the view point is  $Z = 0$  as in the figure below, the parse transformation matrix becomes (1). Therefore, the synthesized matrix obtained by combining the parse transformation matrix with the affine transformation matrix becomes (2).



**Figure 19.2 Example of  $4 \times 4$  Matrix Operation**



$$\begin{pmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 1/d & 0 \end{pmatrix} \quad (1)$$

$$\begin{pmatrix} m00 & m01 & 0 & m03 \\ m10 & m11 & 0 & m13 \\ 0 & 0 & 0 & 0 \\ m20/d & m21/d & 0 & m23/d \end{pmatrix} \quad (2)$$

The above nine parameters are set to the matrix parameter A to I registers (MTRAR to MTRIR), which are coordinate transformation control registers.

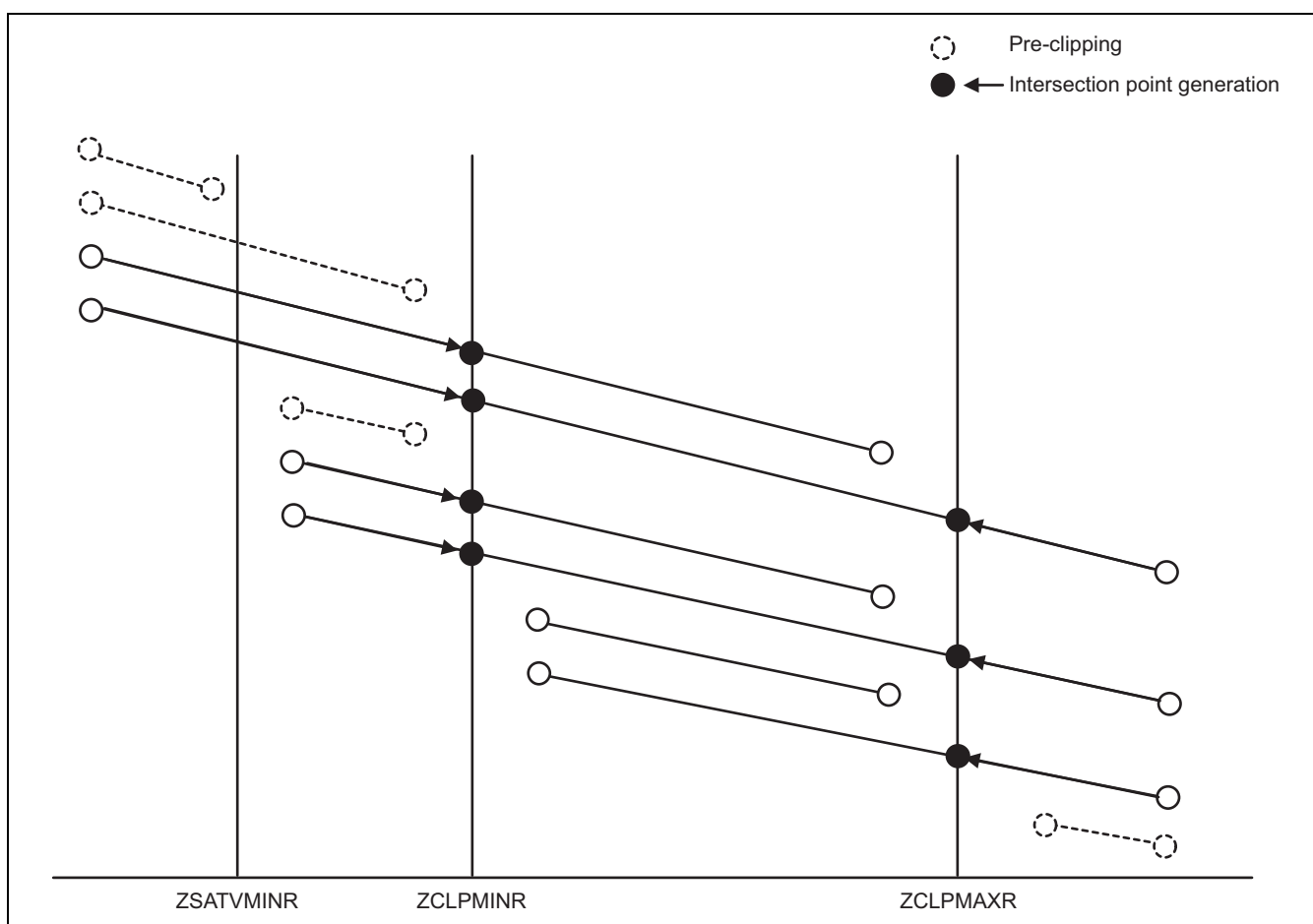
MTRAR to MTRIR are set in the single-precision floating-point format defined by the IEEE754 standard.

- Notes:
1. Before matrix operation, internally add the local offset to the input coordinates X and Y in the R-GP2D.
  2. For a command with a relative coordinate specification, the coordinates are internally modified to the absolute coordinates in the R-GP2D before matrix operation.
  3. Matrix operation is performed for only the center coordinates (BXC, BYC) in a BITBLTA, BITBLTB, BITBLTC, AAFA, or AAFC command and for only the starting and final coordinate points in bold line drawing.
  4. For internal matrix operation, rounding off and exceptional processing conforming to IEEE754 are not performed to increase the operational speed. If an overflow occurs in the mantissa, truncation is performed.
  5. If NaN (non-numeric data) is input or if NaN or infinity appears in the course of operation, the result is undefined.
  6. If denormalized data is input or if denormalized data appears in the course of operation, the result is regarded as 0.

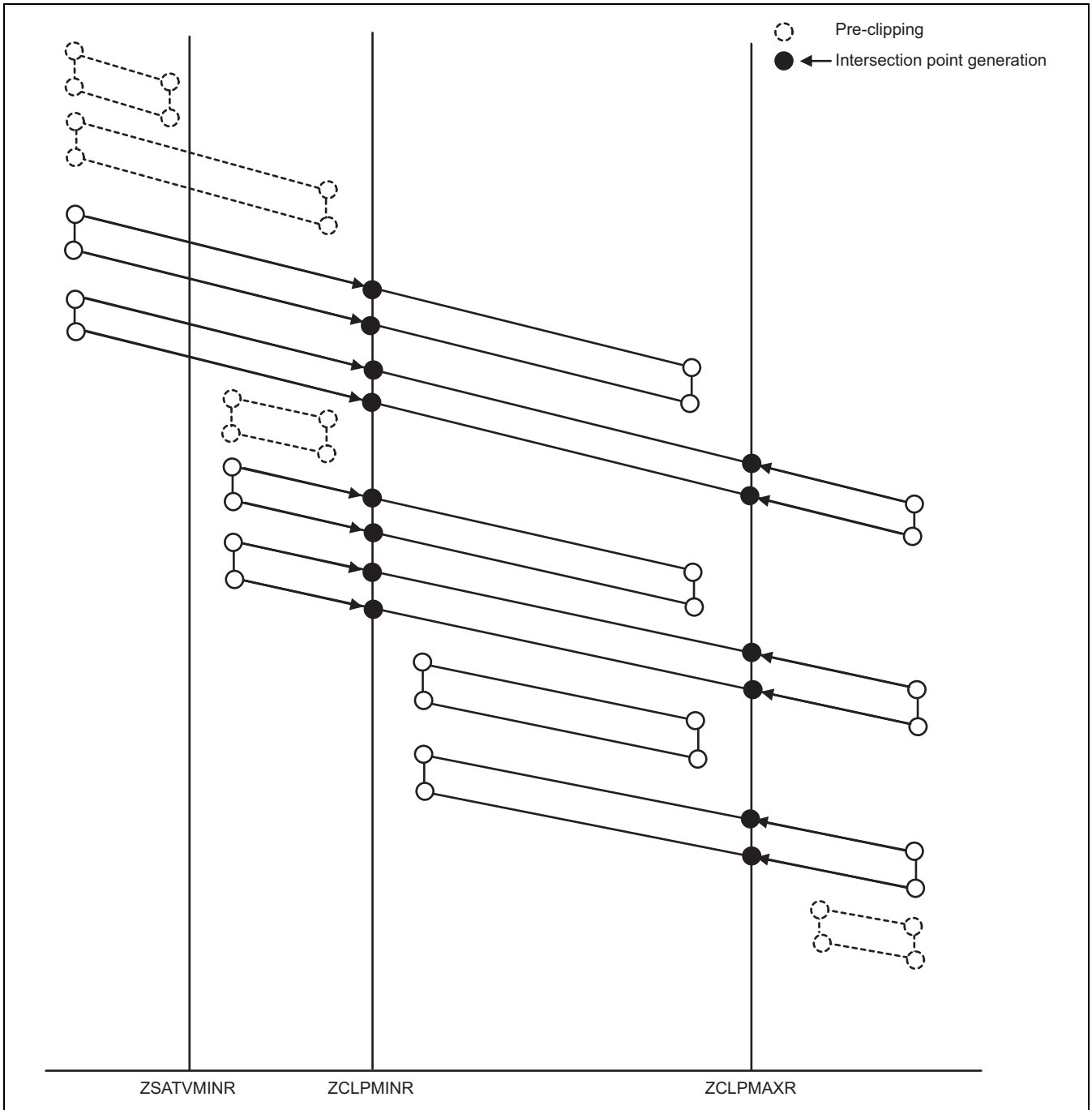
## (2) 2DZ Clipping

Pre-clipping is performed when all vertices of the drawn figure (see the notes below) are smaller than the value in the Z clipping area MIN register (ZCLPMINR) or greater than the value in the Z clipping area MAX register (ZCLPMAXR). Since the W value is used for comparison in Z clipping, set values corresponding to W in ZCLPMINR, ZCLPMAXR and ZSATVMINR (Zmin/d and Zmax/d in the above example). If pre-clipping is not performed, intersection points with the ZCLPMIN and ZCLPMAX areas are searched for in the LINE, RLINE, FTRAPC, RFTRAPC (trapezoid vertices), LINEWC, and RLINEWC commands. In the POLYGON4 commands with BLKE = 1, FTRAPC or RFTRAPC command circumscribed quadrangle drawing (when BLKE = 1), and CLRWC command (when BLKE = 1), BLKE processing is performed after intersection points with the ZCLPMIN and ZCLPMAX area are searched for in the same way as the LINE, RLINE, FTRAPC, RFTRAPC (trapezoid vertices), LINEWC, and RLINEWC commands. In the POLYGON4 command with BLKE = 0, intersection points with ZCLIPMIN and ZCLPMAX are not searched for, and if the W value is equal to or less than the value set in ZSATVMIN after the matrix operation, saturation processing is performed to become the ZSATVMIN value. ZCLPMINR, ZCLPMAXR, and ZSATVMINR must be set in the single-precision floating-point format defined by the IEEE 754 standard. 2DZ clipping is performed only when GTE = 1 and MTRE = 1 simultaneously. It is not performed when GTE = 0 or MTRE = 0.

- Notes:
1. If Z pre-clipping is performed or intersection points are searched for in a LINE, RLINE, command, the continuity of the pattern is not maintained.
  2. If X pre-clipping is performed in bold-line drawing, the linkage parts may not be drawn.
  3. Drawing is not performed on the edge line between the FTRAPC or RFTRAPC screen and ZCLPMIN and ZCLPMAX screens in LINE, RLINE, LINEWC and RLINEWC commands.
  4. In FTRAPC and RFTRAPC commands, drawing may not be performed on the edge line with the ZCLPMIN and ZCLPMAX screens.
  5. In map drawing with coordinate transformation, such as birds-eye view, a POLYGON4 command used for drawing a polygon is assumed to be used with BLKE = 1 and PSTYLE = 1 (for POLYGON4A or POLYGON4B). If a POLYGON4 command is used with BLKE = 0 or PSTYLE = 0, the drawn figure may be broken.
  6. Meaning of "all vertices":  
 POLYGON4 and CLRWC: Four vertices after coordinate transformation  
 BITBLT, AAFA, and AAFC: The center coordinate vertex after coordinate transformation  
 FTRAPC and RFTRAPC: Four vertices of circumscribed quadrangle after coordinate transformation  
 LINE, RLINE, LINEW, and RLINEW: Two vertices of the line



**Figure 19.3 Example of Z Clipping for LINE, RLINE, FTRAPC, RFTRAPC (Trapezoid Vertices), LINEW, and RLINEW Commands**



**Figure 19.4 Example of Z Clipping for POLYGON4 Commands (BLKE = 1), FTRAPC or RFTRAPC Command (Circumscribed Quadrangle), and CLRWC Command**

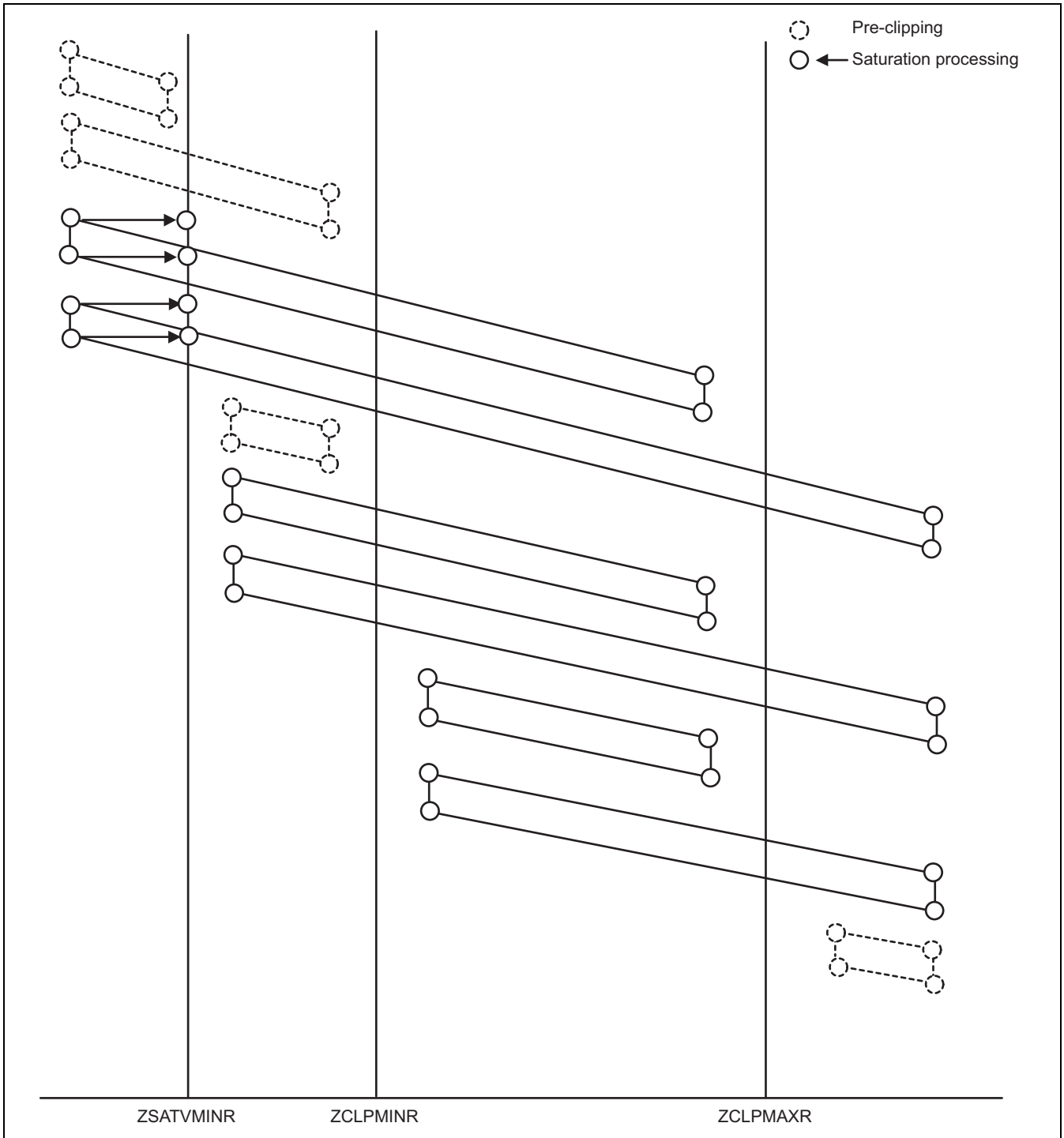


Figure 19.5 Example of Z Clipping for POLYGON4 Commands (BLKE = 0)

### (3) Perspective W Division

TX and TY after matrix operation are processed as follows, according to the affine transformation enable bit (AFE) in the coordinate transformation control register (GTRCR).

- AFE = 0

The output X coordinate X' and output Y coordinate Y' become:  $X' = TX/WC + GTROFSX$ ,  $Y' = TY/WC + GTROFSY$ .

GTROFSX and GTROFSY are set in the coordinate transformation offset X register (GTROFSXR) and coordinate transformation offset Y register (GTROFSYR), respectively. GTROFSX and GTROFSY are set as 16-bit integers (two's complements).

- AFE = 1

The output X coordinate X' and output Y coordinate Y' become:  $X' = TX$ ,  $Y' = TY$ . Z clipping, perspective W division, and offset addition are not performed.

Z clipping, perspective W division, and offset addition are not performed.

When AFE = 0, if  $TX/WC + GTROFSX$  or  $TY/WC + GTROFSY$  (offset GTROFSX and GTROFSY added to TX/WC and TY/WC after W division) is smaller than  $-H'7FFF$  or greater than  $H'7FFF$ , respectively, saturation processing is performed. Even if saturation processing has been performed, the command is continuously executed at the vertex coordinates which have been saturated.

An offset (from -2048 to 2047) can be added to GTROFSX and GTROFSY using the RGTOFS command.

Note: In a BITBLT type, AAFA, or AAFC command, the four vertices are obtained by adding the width (LW, RW) and height (TH, BH) to the center coordinate values after they have been transformed.

In bold line drawing, the four vertices are obtained from the final and starting points of the transformed coordinates and the line width (W). Therefore, be careful the rendering coordinates are not exceeded in these two commands because saturation processing is not performed for vertices obtained from the reference points (center coordinates in a BITBLT type command, and starting and final coordinate points in bold line drawing).

### (4) 2-Dimensional Vertex Clipping

When the 2-dimensional vertex clipping enable specification is set to enable with the 2DVCLPE bit in RCLR, generates intersection points with the 2-dimensional vertex clipping area (ANDed area of the system clipping area, user clipping area, and relative user clipping area) and performs drawing using the generated points in the LINEA/B/C/D, RLINEA/B/C/D, LINEWC, RLINWC, FTRAPC, RFTRAPC (circumscribed quadrangle and trapezoid vertices), CLRWC, and POLYGON4A/B/C (BLK = 1) commands.

In addition, setting a value other than 0 in 2DVCEXTR extends the 2-dimensional clipping area to be used for intersection generation by the amount of the set value. This function is effective to prevent end points of a bold line from being cut off since bold-line coordinates are generated from the intersection points generated by 2-dimensional vertex clipping in bold-line drawing. Usually, a half the maximum value of the line width for bold line drawing is set for 2DVCEXTR. The initial value is set as line width of 10.

- Notes:
1. This function is invalid for commands other than above.
  2. Drawing tracks may not match between 2DVCLPE = 0 and 2DVCLPE = 1.
  3. Patterns do not match.
  4. For the intersection edge between the FTRAPC or RFTRAPC screen and 2-dimensional clipping area screen, LINE, RLINE, LINEWC, or RLINWC commands do not perform drawing.
  5. If different values are set for the 2-dimensional clipping area and 2DVCEXTR in each command, intersection point coordinates will differ according to the setting and drawn tracks will not match. (Care should be taken when drawing an edge line of a polygon.)

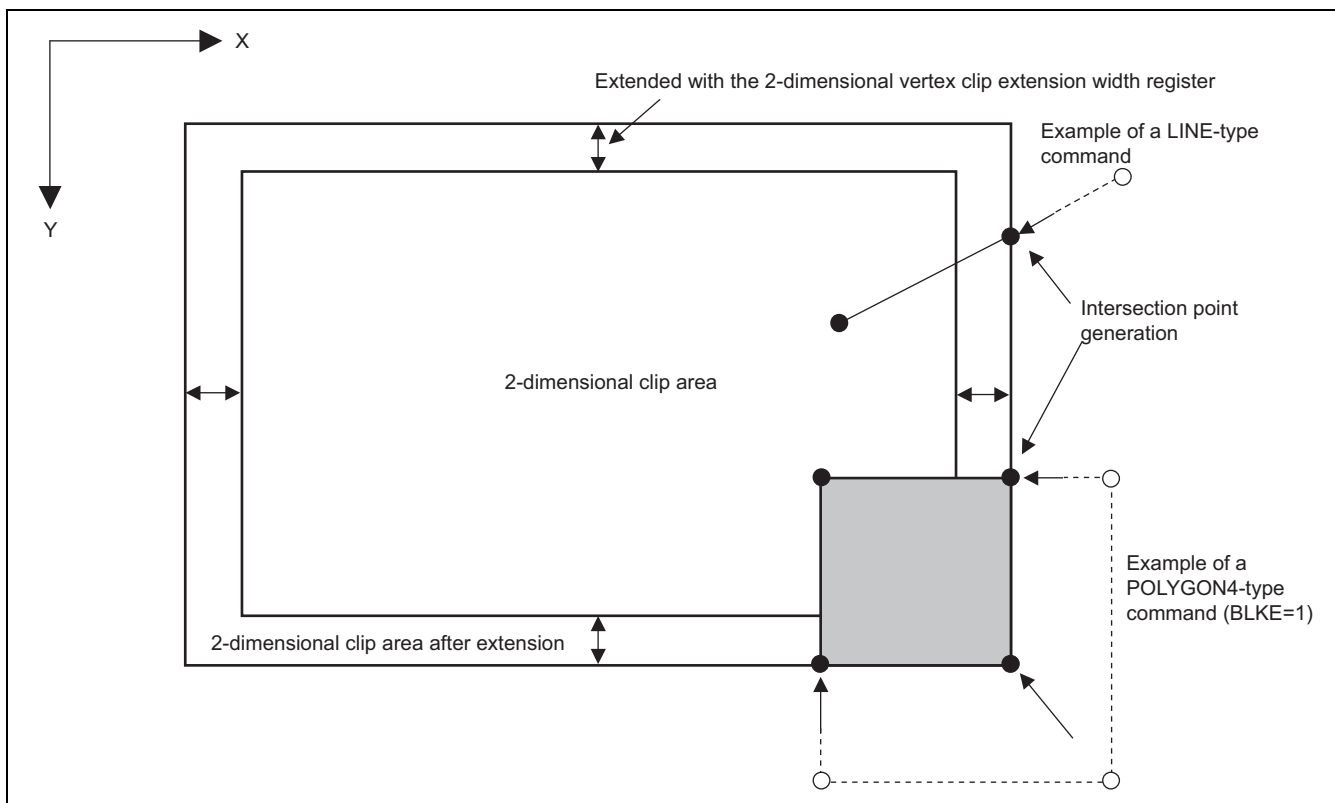


Figure 19.6 2-Dimensional Vertex Clipping

(5) Coordinate Transformation Flow and Saturation Processing

Coordinate transformation is performed in the following sequence.

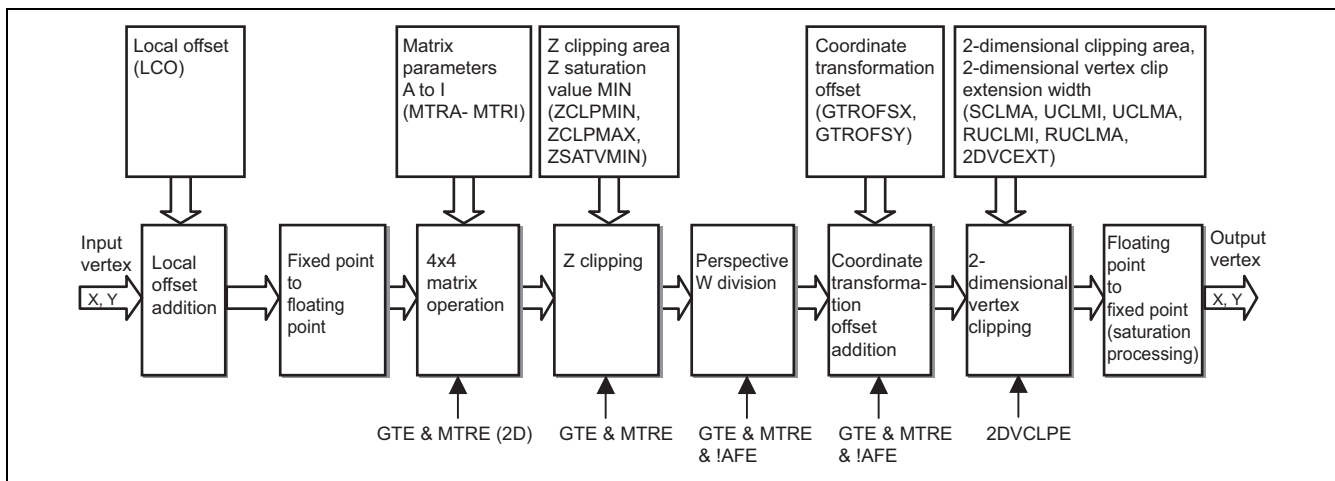
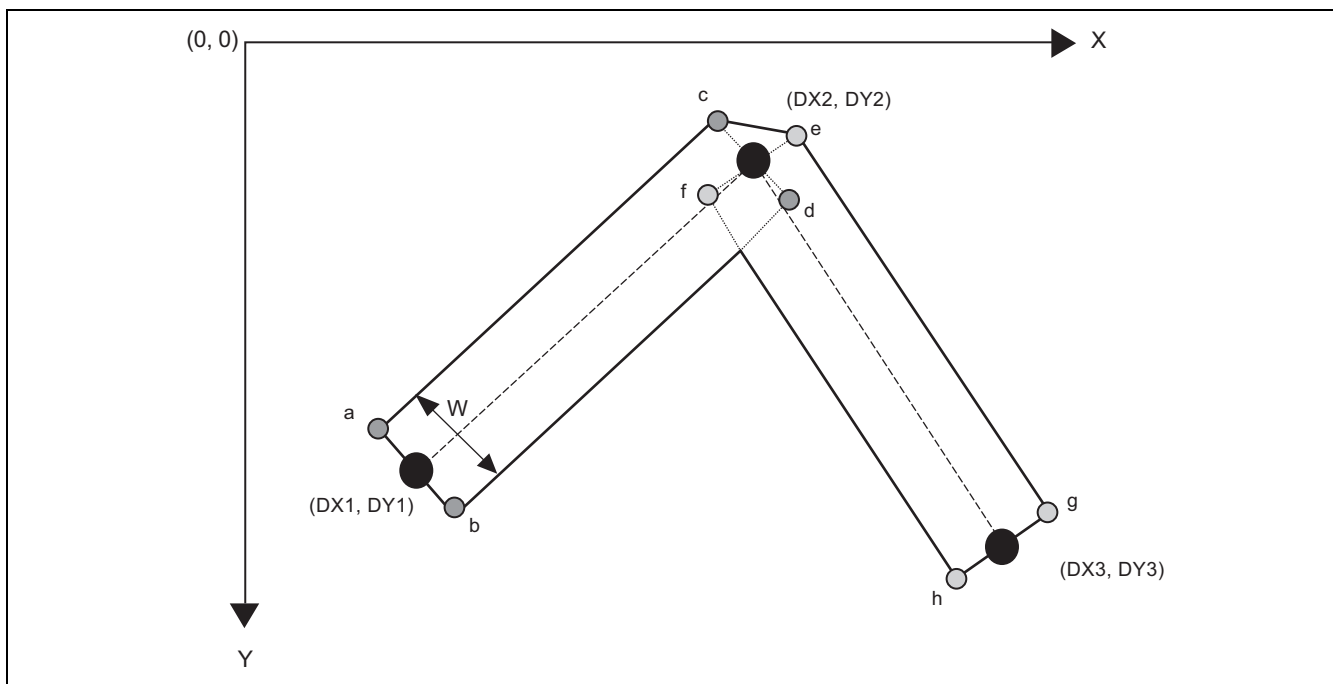


Figure 19.7 Coordinate Transformation Flow Image

**(6) Bold Line Drawing**

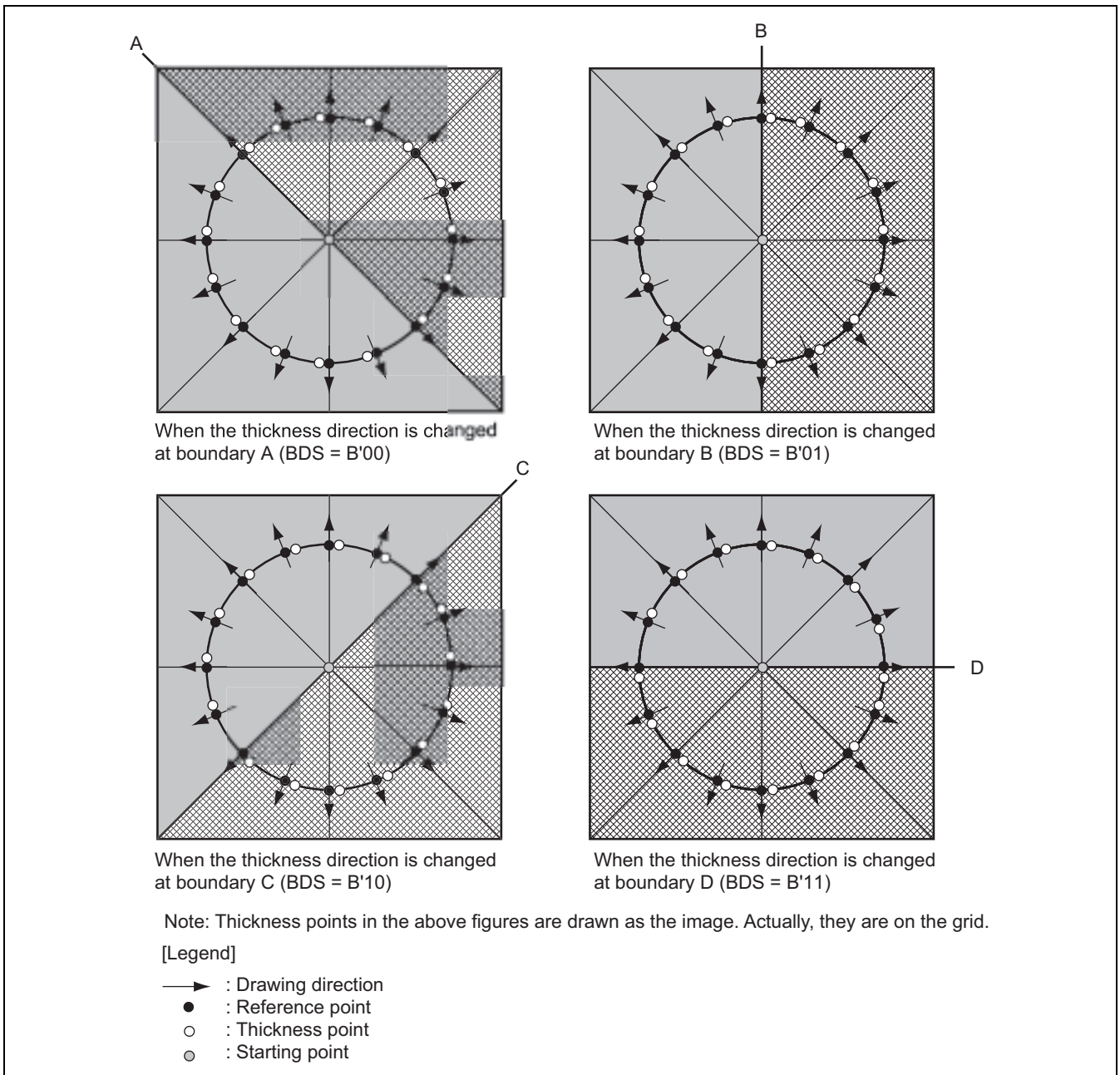
A bold line can be drawn by setting a value greater than 0 as line width  $W$  in a LINEA, LINEB, LINEC type or RLINEA, RLINEB, RLINEC type command. The bold line coordinates  $a$ ,  $b$ ,  $c$ , and  $d$  are obtained from the starting and final coordinate points and line width  $W$ , and the bold line drawn.  $W$  is set in the 6-bit integer part. When 0 is set in  $W$ , a line of line width 1 is drawn. The connection drawing mask bit (COM) in the rendering control register (RCLR) is used to select whether the linkage parts of bold lines are drawn or not. When the starting and final coordinate points of a line segment match in bold line drawing, nothing is drawn.

When the WLM (bold line mode) bit in RCLR is set to 1, jaggy is reduced in bold line drawing.



**Figure 19.8 Bold Line Drawing**

A boundary for switching thickness directions can be set according to the BDS (thickness direction boundary select) bit in RCLR.



**Figure 19.9 Thickness Direction Boundary Select Bit**



## (7) Antialiasing

Antialiasing which reduces alias can be used in a (R)LINEA/B/C/D or 3DLINE command.

For (R)LINEA/B/C/D commands, antialiasing is performed by setting the rendering attribute AA (antialias enable) bit to 1. There are two antialiasing modes. When the NAA (new antialiasing mode) bit in RCLR is set to 0, antialiasing is not performed for horizontal, vertical, and 45-degree diagonal line segments. When the NAA bit is 1, antialiasing is performed for horizontal, vertical, and 45-degree diagonal line segments.

- For a dashed line in LINEA/B or RLINEA/B command, antialiasing is not performed for the gaps in the dashed line.
- When the starting and final coordinate points of a line segment match in the LINEA, LINEB, LINEC, RLINEA, RLINEB, or RLINEC command, a single dot is drawn for a 1-bit-wide line ( $W = 0$ ) without antialiasing and nothing is drawn for bold line drawing.
- When the starting and final coordinate points of a line segment match in the LINED or RLINED command, nothing is drawn.
- Antialiasing is not performed for horizontal, vertical, and 45-degree diagonal line segments in the LINEA, LINEB, LINEC, RLINEA, RLINEB, or RLINEC command. In new antialias mode (when NAA is set to 1), antialiasing is performed for horizontal, vertical, and 45-degree diagonal line segments.
- Antialiasing is not performed for horizontal and vertical line segments in the LINED or RLINED command.



**Figure 19.10 Example of Antialias Specification**

### 19.3.2 Coordinate Systems

The R-GP2D has five 2-dimensional coordinate systems (screen coordinates, rendering coordinates, 2-dimensional source coordinates, work coordinates, and  $\alpha$ -map coordinates), and one 1-dimensional coordinate system (1-dimensional source coordinates).

Screen coordinates are the display control coordinates. Screen coordinate X corresponds to the horizontal dimension of the display screen and Y to the vertical dimension. The origin is the top-left corner in the display screen. The screen coordinate positive directions are right for the X-axis and down for the Y-axis. 32 bits (32 bits/pixel), 16 bits (16 bits/pixel), or 8 bits (8 bits/pixel) can be selected as the data width of one screen coordinate. The maximum values of the screen coordinates are  $X = 4,095$ ,  $Y = 4,095$ .

Rendering coordinates are drawing control coordinates. Rendering coordinates are shifted horizontally and vertically with respect to screen coordinates by the offset amounts specified in drawing commands. According to the drawing commands, the R-GP2D performs drawing operations using these coordinates. 32 bits (32 bits/pixel), 16 bits (16 bits/pixel), or 8 bits (8 bits/pixel) can be selected as the data width of one rendering coordinate.

2-dimensional source coordinates are drawing control coordinates. When a drawing command is executed with  $SS = 1$ , these are the source data (rectangle) coordinates specified by the drawing command. 32 bits (32 bits/pixel), 16 bits (16 bits/pixel), or 8 bits (8 bits/pixel) can be selected as the data width of one 2-dimensional source coordinate.

1-dimensional source coordinates are drawing control coordinates. When a drawing command is executed with  $SS = 0$ , these are the source data (1-dimensional) coordinates specified by the drawing command. 32 bits (32 bits/pixel), 1 bit (1 bit/pixel), 16 bits (16 bits/pixel), or 8 bits (8 bits/pixel) can be selected as the data width of one 1-dimensional source coordinate. For one 1-dimensional source, one physical address (top-left) and the horizontal width and vertical height of the 1-dimensional source are specified.

Work coordinates are drawing control coordinates that correspond one-to-one with the rendering coordinates. When a drawing command is executed, these are the work coordinates specified by the drawing command. The data width of one work coordinate is 1 bit (1 bit/pixel).

$\alpha$ -map coordinates are drawing control coordinates that are specified by the AAFA command. The data width of one  $\alpha$ -map coordinate is 8 bits (8 bits/pixel).

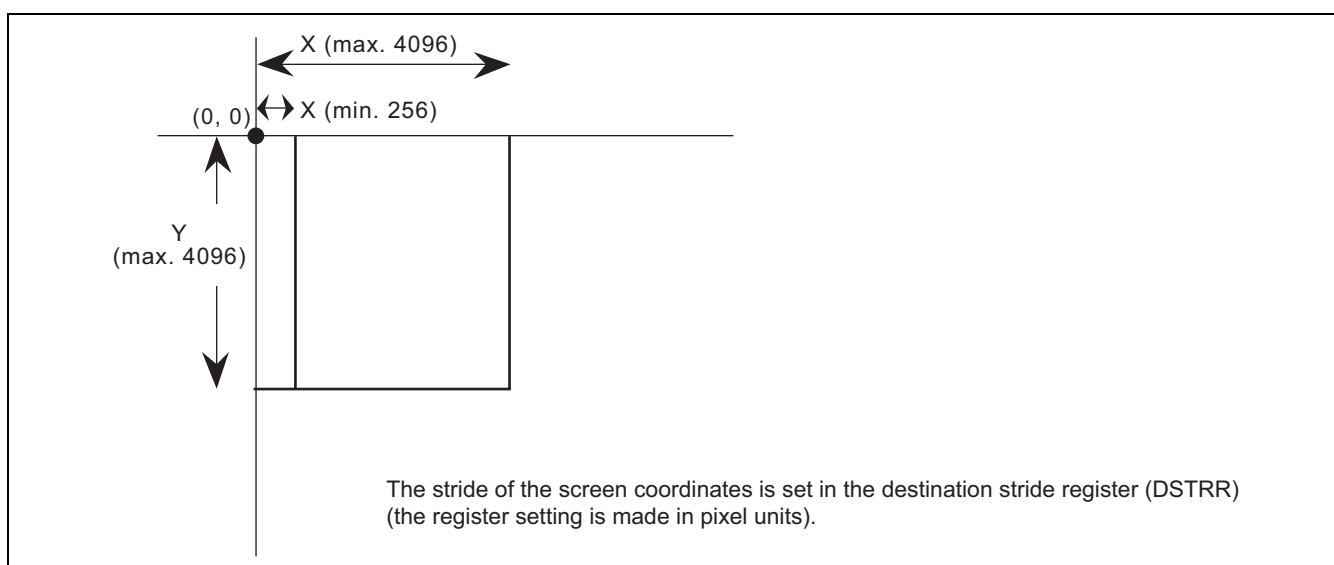


Figure 19.11 Screen Coordinates

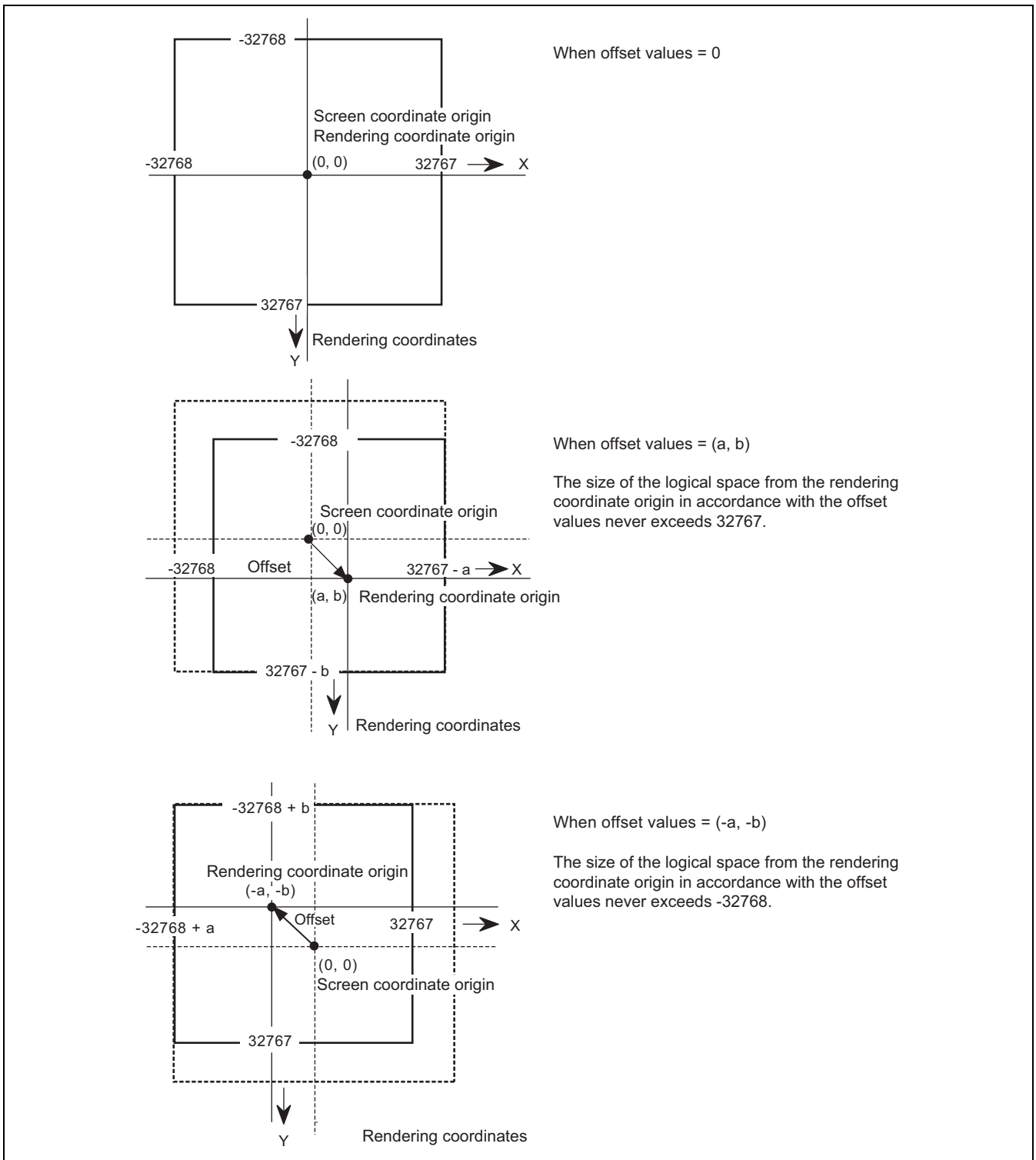


Figure 19.12 Rendering Coordinates

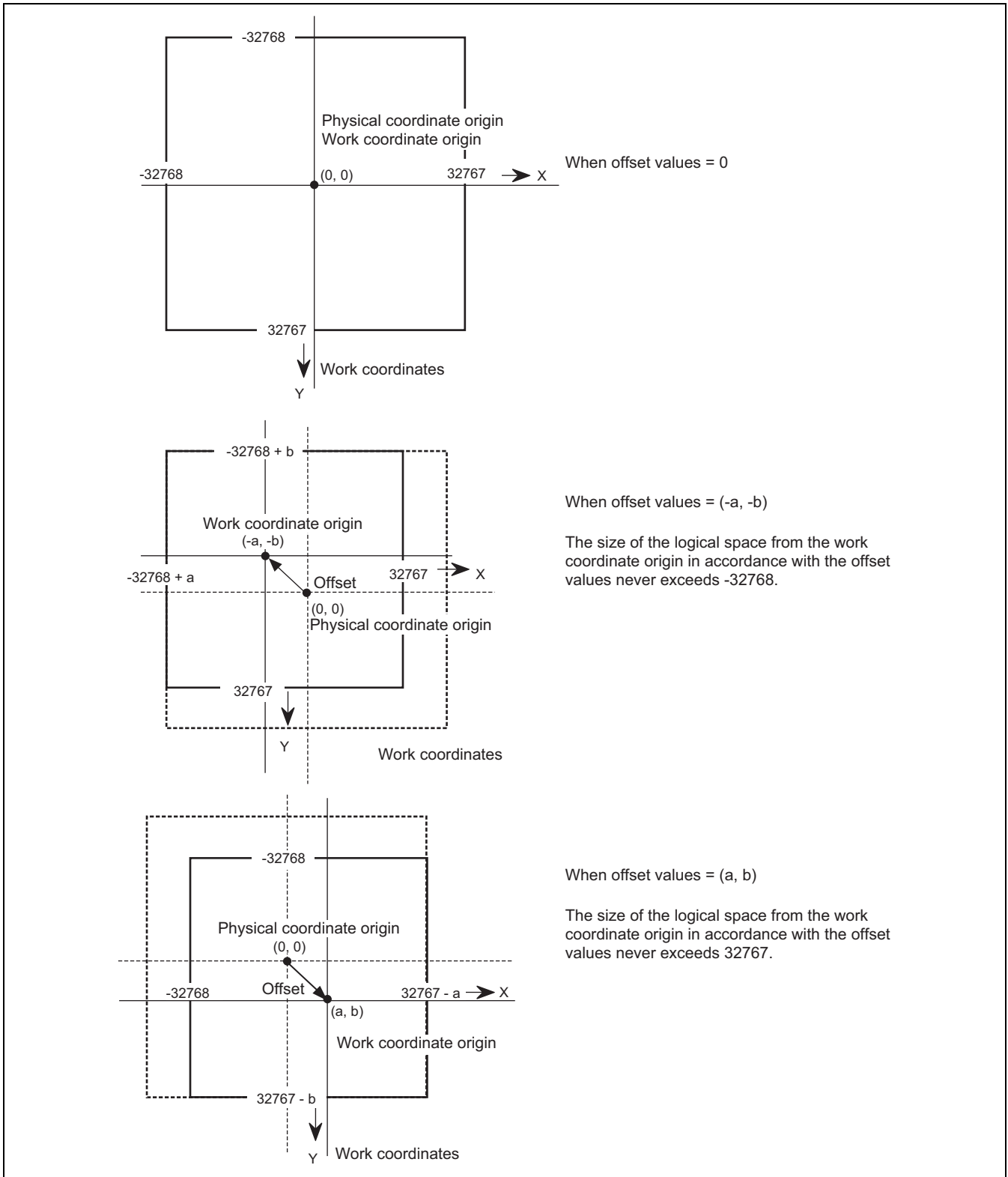
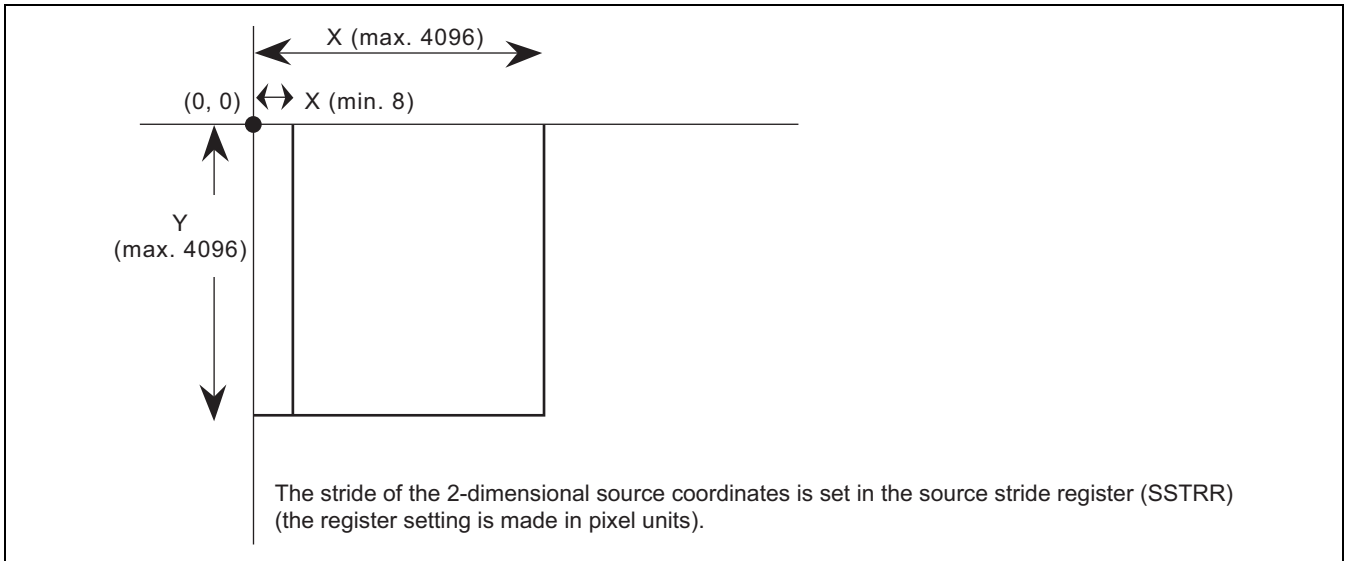
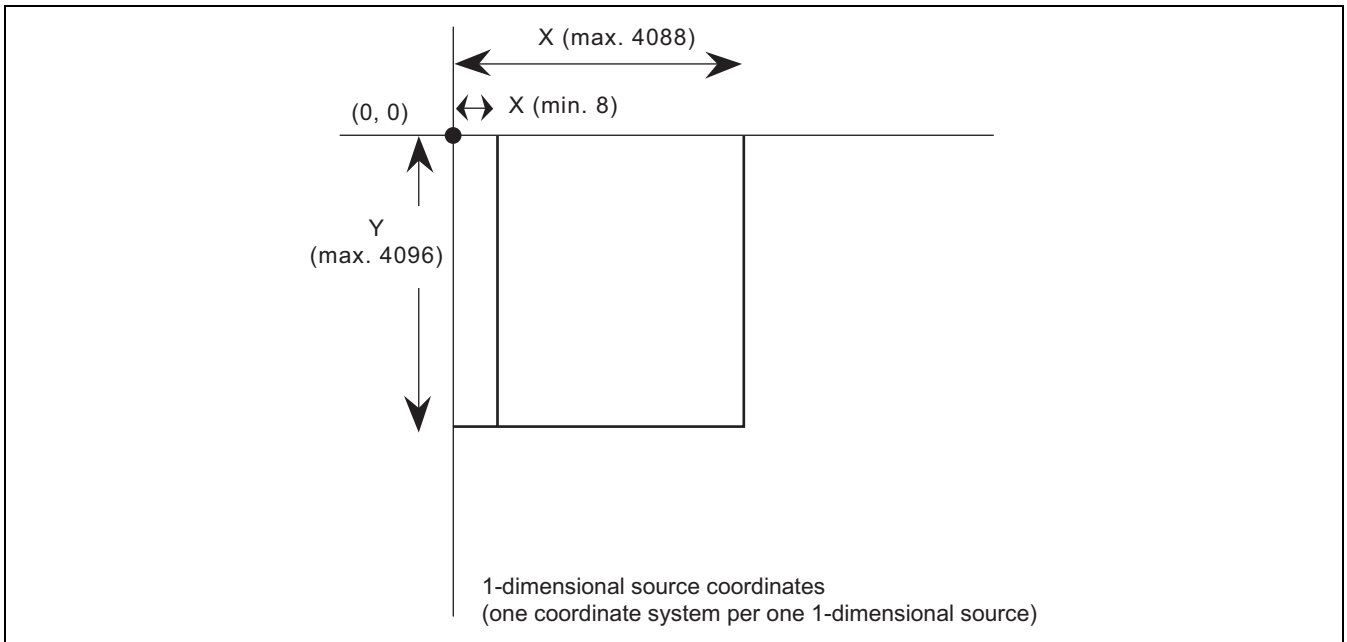


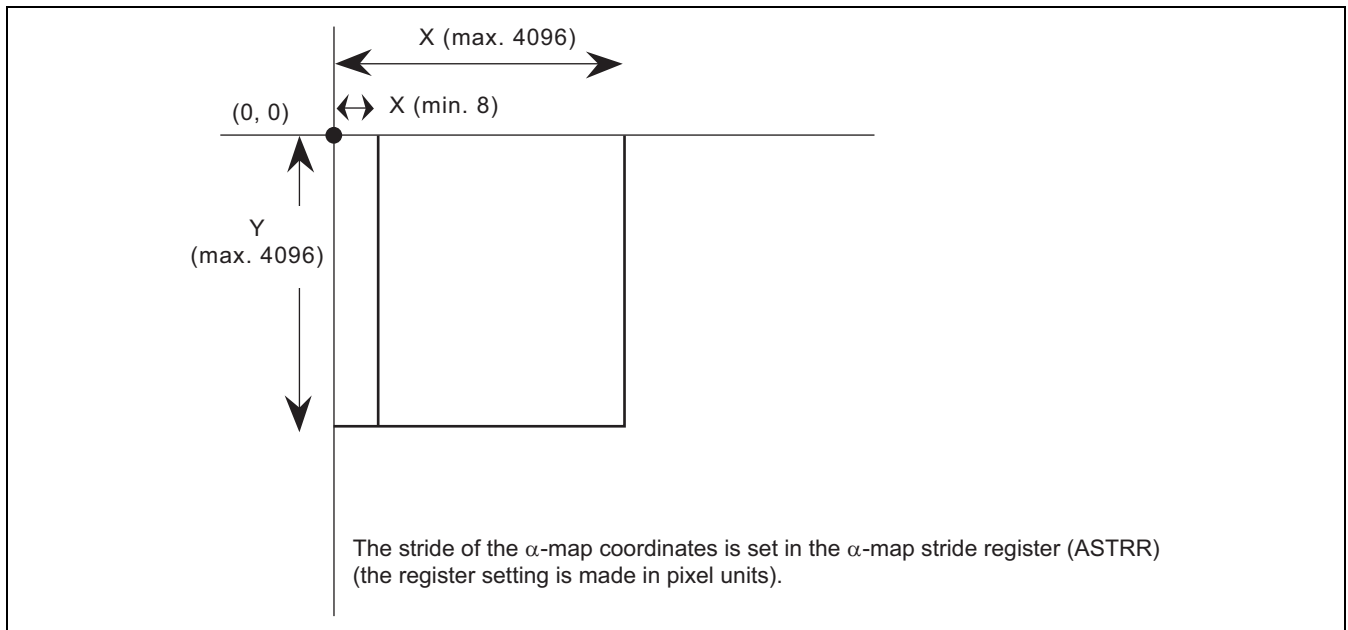
Figure 19.13 Work Coordinates



**Figure 19.14 2-Dimensional Source Coordinates (SS = 1)**



**Figure 19.15 1-Dimensional Source Coordinates (SS = 0)**



**Figure 19.16  $\alpha$ -Map Coordinates**

### 19.3.3 Data Formats

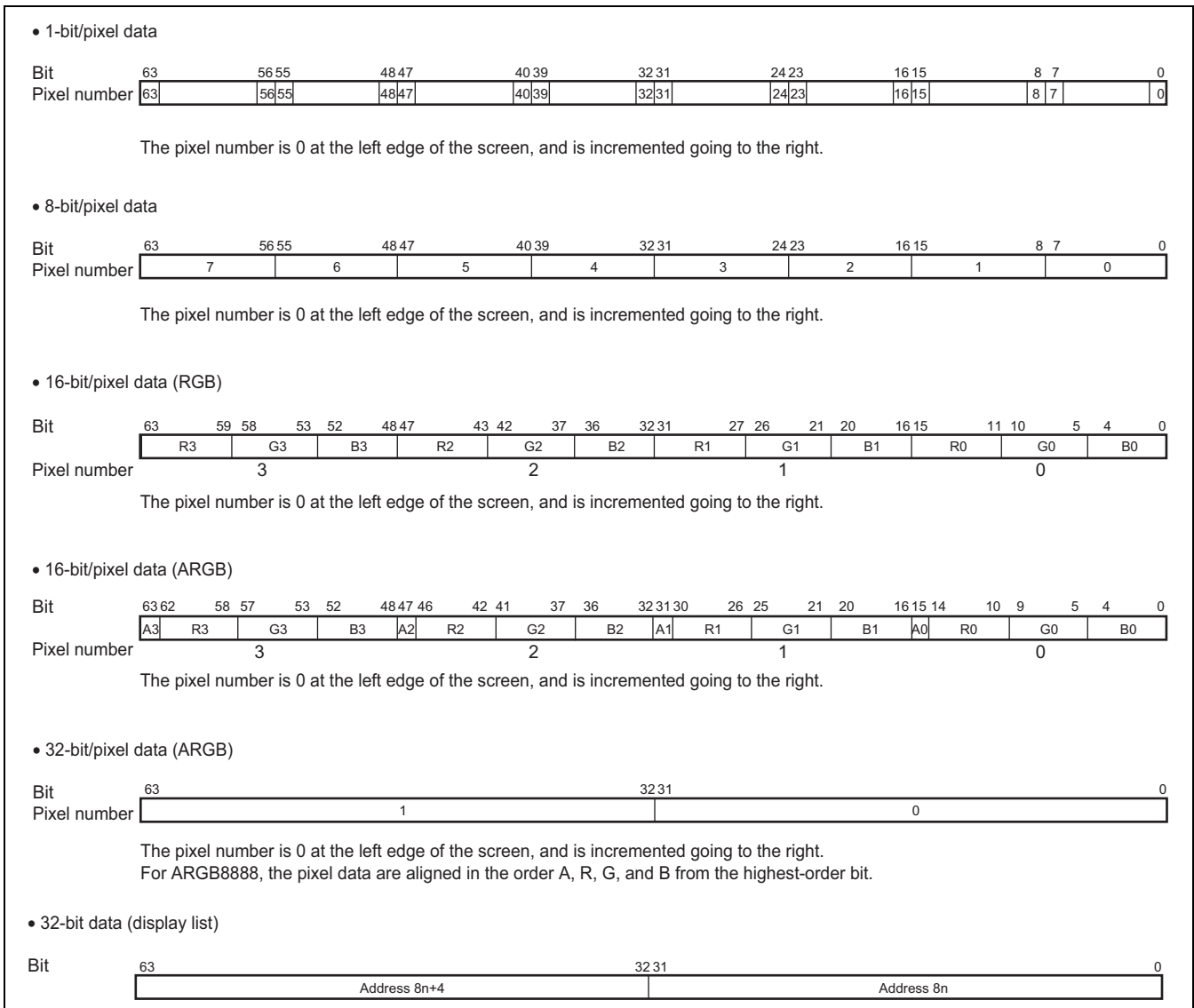


Figure 19.17 Data Formats

### 19.3.4 Endian Conversion

Endian conversion mode can be specified in ENDCVR.

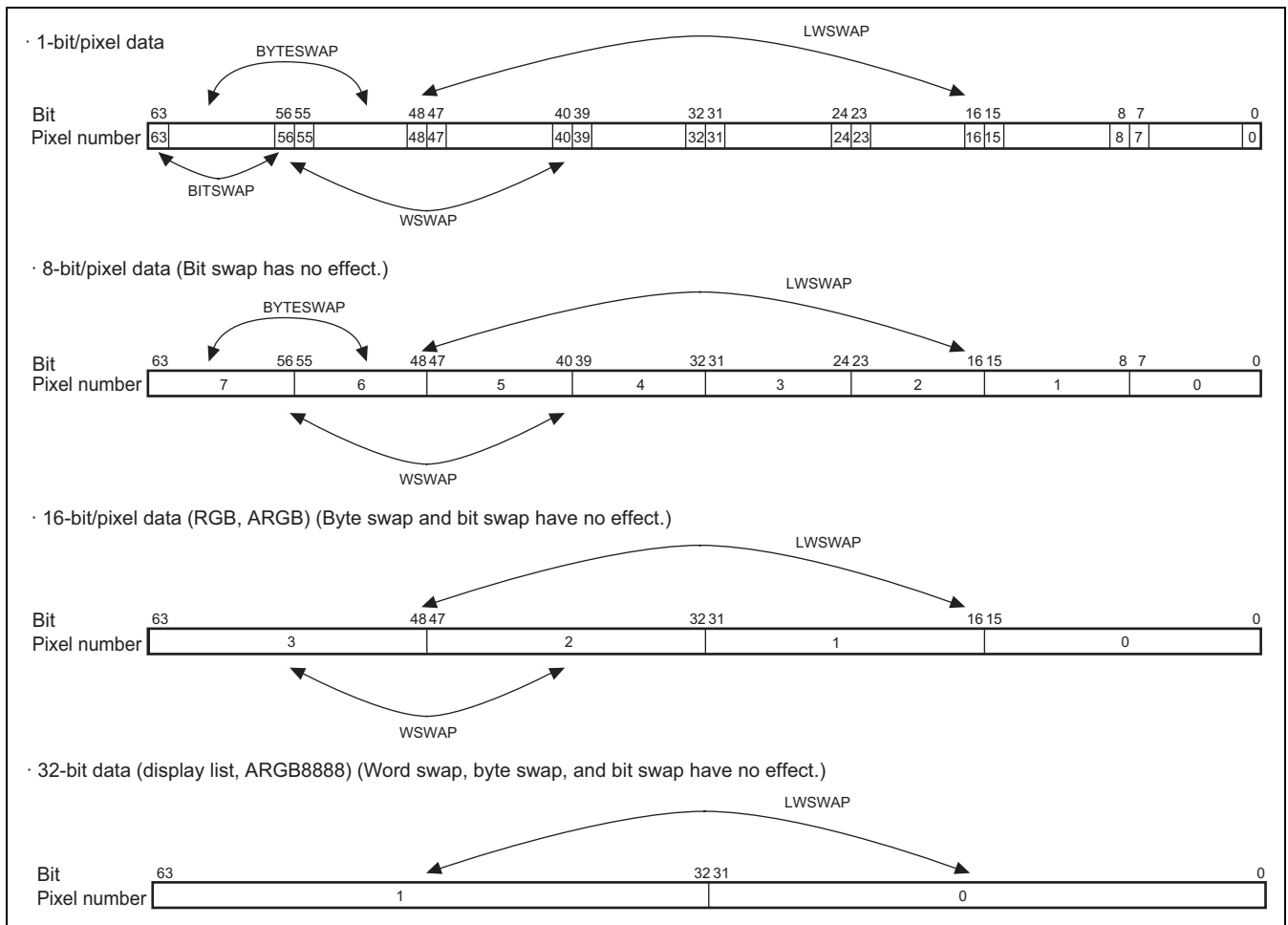


Figure 19.18 Endian Conversion



### 19.3.5 Rendering Attributes

#### (1) Source Transparency Specification (STRANS)

When referencing source data, the STRANS bit can be used to select transparency or non-transparency on an individual drawing command basis. If transparency is selected, the source color becomes transparent at register value = source color when the source transparent color polarity bit (STP) in the rendering control register (RCLR) is 0, and the source color becomes transparent at register value  $\neq$  source color when the STP bit is 1, and the pixels are not drawn in either case. The source transparency specification can be used with the POLYGON4A, POLYGON4B, LINEA, LINEB, RLINEA, RLINEB, BITBLTA, BITBLTB, and AAFA commands. The STRANS bit should be cleared to 0 in other commands. When the source pixel format is ARGB, the A value is not compared. Note that when the STRANS bit is set to 1, the source data is always read in the BITBLTA or BITBLTB command, regardless of the ROP code.

#### (2) Destination Transparency Specification (DTRANS)

When referencing destination data, the DTRANS bit can be used to select transparency or non-transparency on an individual drawing command basis. If transparency is selected, the destination color becomes transparent at register value = source color when the destination transparent color polarity bit (DTP) in the rendering control register (RCLR) is 0, and the destination color becomes transparent at register value  $\neq$  destination color when the DTP bit is 1, and the pixels are not drawn in either case. The destination transparency specification can be used with the BITBLTA, BITBLTB, BITBLTC, AAFA, and AAFC commands. The DTRANS bit should be cleared to 0 in other commands. When the destination pixel format is ARGB, the A value is not compared. Note that when the DTRANS bit is set to 1, the destination data is always read, regardless of the ROP code.

#### (3) Source Style Specification (STYLE)

The STYLE bit can be used to select, on an individual drawing command basis, whether to enlarge or reduce the source data or repeatedly reference it. If no style specification is made, the source data is enlarged or reduced in proportion to the size of the rendering area. When a style specification is made, the source data is referenced repeatedly in proportion to the size of the rendering area. This attribute is therefore used when drawing repeated patterns such as hatch patterns. The source style specification can be used with the POLYGON4A, POLYGON4B, LINEA, LINEB, RLINEA, and RLINEB commands. The STYLE bit should be cleared to 0 in other commands. The STYLE bit must be set to 1 when BLKE = 1 in the POLYGON4A, POLYGON4B, LINEA, LINEB, RLINEA, or RLINEB command.

In the LINEA, LINEB, RLINEA, and RLINEB commands, the source data is repeatedly referenced in only the X direction of the source data. The source data is enlarged or reduced in proportion to the line width in the Y direction of the source data.

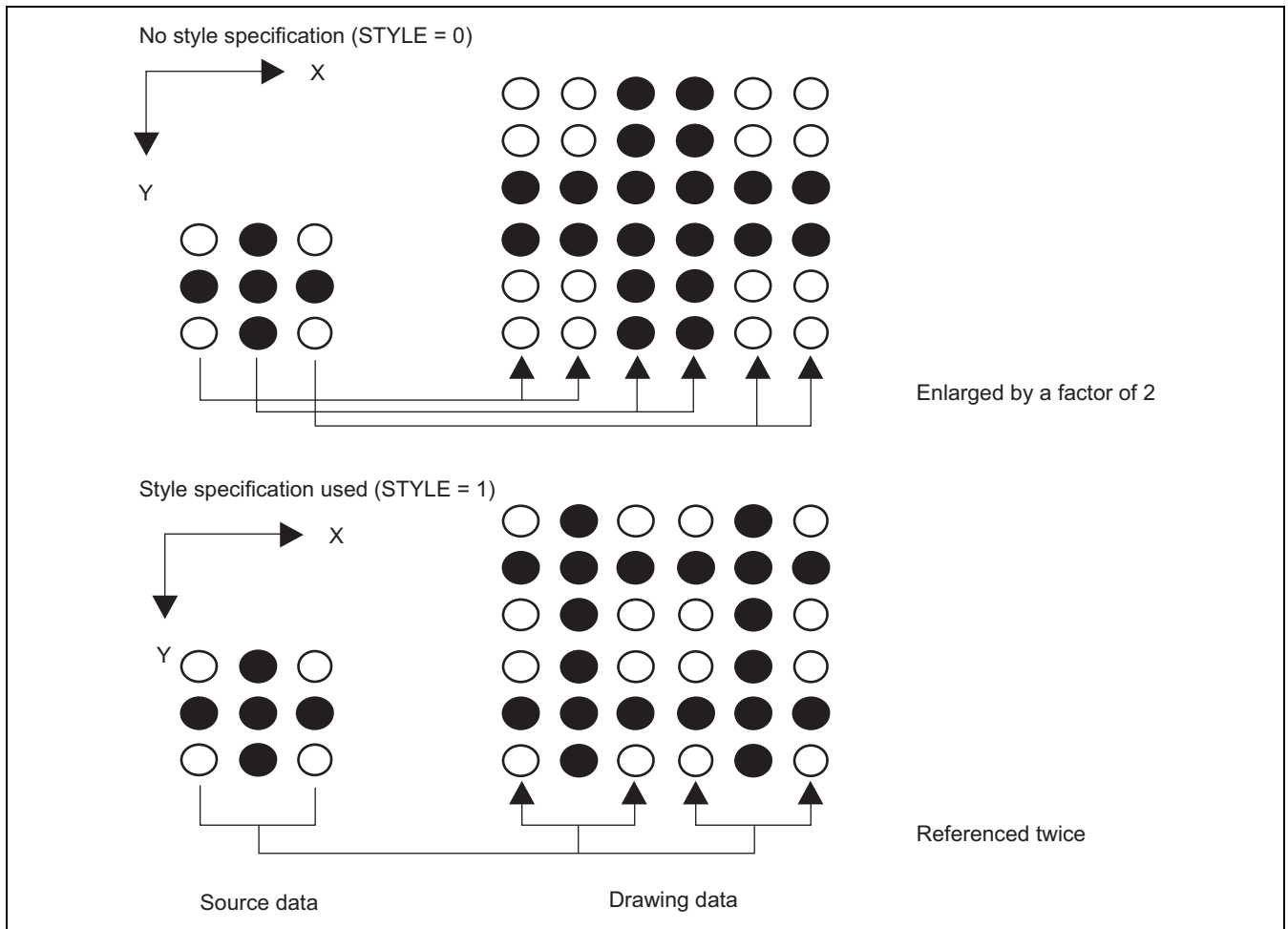


Figure 19.19 Example of Source Style Specification

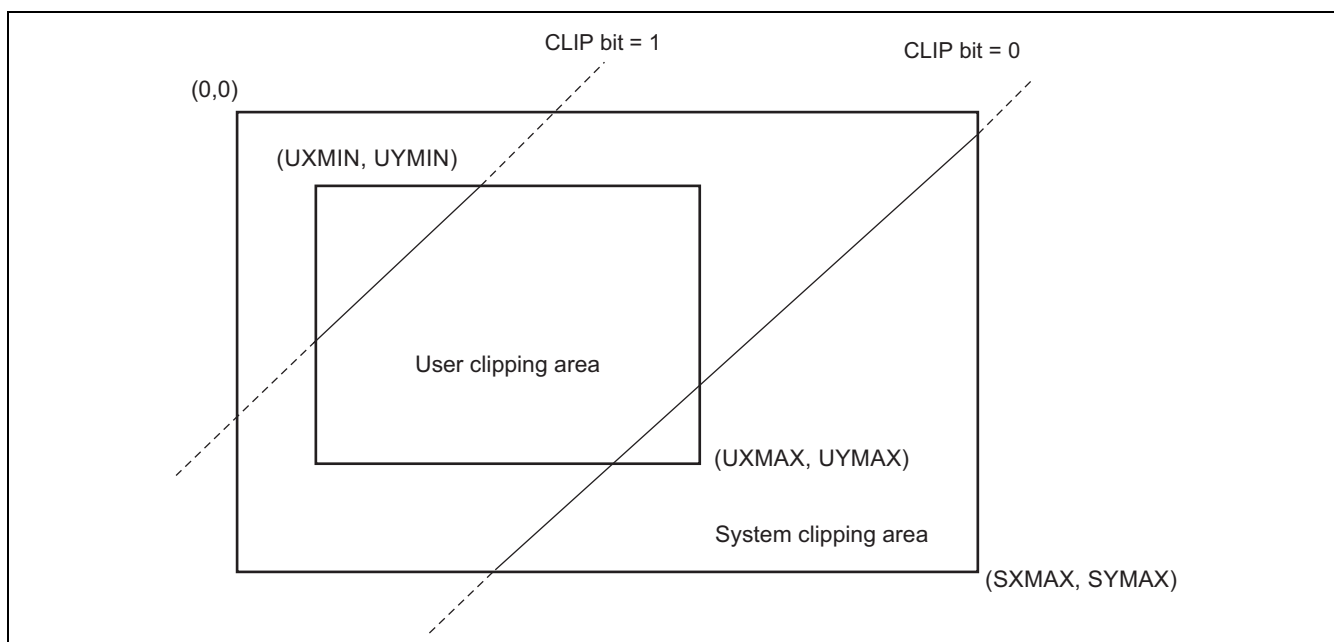
#### (4) Clipping Specification (CLIP)

The R-GP2D can perform clipping area management. There are three kinds of clipping areas: system clipping area, user clipping area, and relative user clipping area.

The system clipping area has a fixed drawing range. The system clipping area is always valid, regardless of attribute specifications.

A user clipping area can be designated as desired within the system clipping area. Whether or not clipping is performed in that area can be selected on an individual command basis with the rendering attribute CLIP bit. The boundary is drawn. The local offset values specified by the LCOFS or RLCOFS command are not added. When setting a user clipping area, the following ranges must be satisfied:  $XMIN < XMAX$ ,  $YMIN < YMAX$ .

Clipping is set with screen coordinates. Since the clipping area is undefined after the power is turned on, set the clipping area by the WPR command at the top of the display list that is executed first. XMAX must be set to a value less than the value set in the destination stride register (DSTRR).



**Figure 19.20 Example of Clipping Specification**

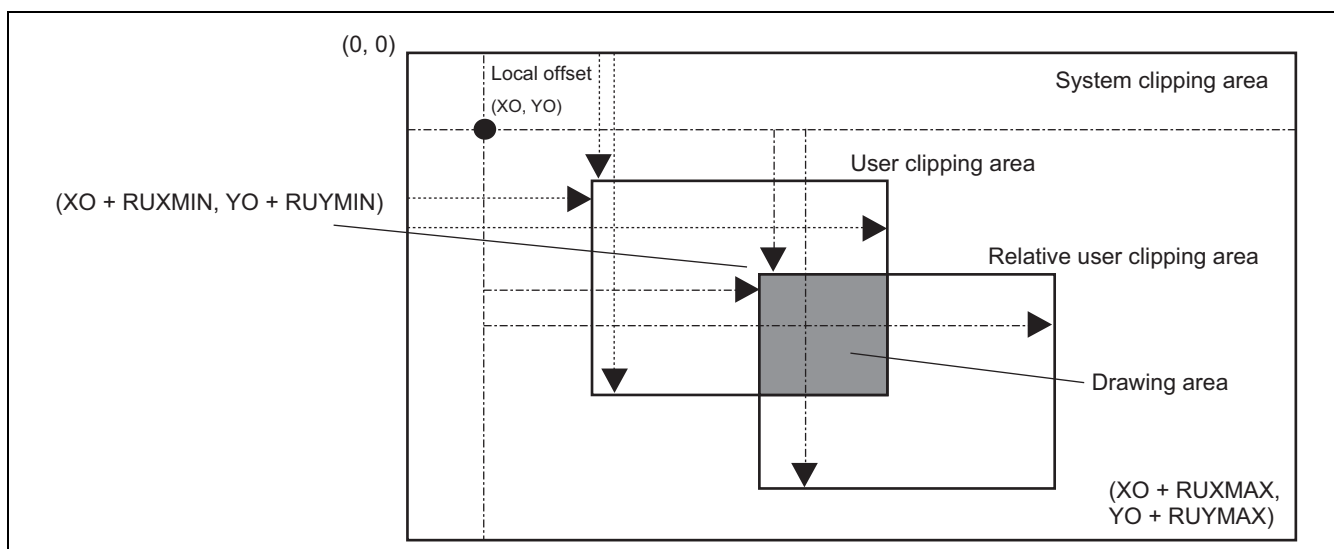
**(5) Relative Clipping Specification (RCLIP)**

The R-GP2D can perform clipping area management. There are three kinds of clipping areas: system clipping area, user clipping area, and relative user clipping area.

The system clipping area has a fixed drawing range. The system clipping area is always valid, regardless of attribute specifications.

A relative user clipping area can be designated as desired within the system clipping area at a relative setting with respect to the local offset. Whether or not clipping is performed in that area can be selected on an individual command basis with the rendering attribute RCLIP bit. The boundary is drawn. The local offset values specified by the LCOFS or RLCOFS command are added.

When setting a relative user clipping area, the following ranges must be satisfied:  $XMIN < XMAX$ ,  $YMIN < YMAX$ . Clipping is set with screen coordinates. Since the clipping area is undefined after the power is turned on, set the clipping area by the WPR command at the top of the display list that is executed first. XMAX must be set to a value less than the value set in the destination stride register (DSTRR). If both the RCLIP and CLIP bits are set to 1 simultaneously, the region where the two clipping areas overlap is drawn.



**Figure 19.21 Example of Relative User Clipping Specification**

When a relative user clipping area  $((XO + RUXMIN, YO + RUYMIN) - (XO + RUXMAX, YO + RUYMAX))$  intersects with the system clipping area, saturation processing is performed as follows:

$$XO + RUXMIN < 0 \rightarrow XO + RUXMIN = 0$$

$$XO + RUXMAX > SXMAX \rightarrow XO + RUXMAX = SXMAX$$

$$YO + RUYMIN < 0 \rightarrow YO + RUYMIN = 0$$

$$YO + RUYMAX > SYMAX \rightarrow YO + RUYMAX = SYMAX$$

Note: Set the local offset values and relative user clipping area without exceeding the following ranges:

$$-4,096 \leq XO + RUXMIN \leq 4,095$$

$$-4,096 \leq YO + RUYMIN \leq 4,095$$

$$0 \leq XO + RUXMAX \leq 8,191$$

$$0 \leq YO + RUYMAX \leq 8,191$$

When  $RCLIP = 1$  and the relative user clipping area satisfies one of the following conditions, the relative user clipping area is disabled internally by the R-GP2D (same operation as  $RCLIP = 0$ ).

$$4,095 < XO + RUXMIN$$

$$4,095 < YO + RUYMIN$$

$$XO + RUXMAX < 0$$

$$YO + RUYMAX < 0$$

### (6) Net Drawing Specification (NET)

The NET bit can be used to select, on an individual drawing command basis, whether or not net drawing is to be performed. Net drawing is a function for drawing only pixels at coordinates for which the condition "rendering coordinates  $X + Y = EOS$  (0: even number, 1: odd number)" is true. For example, if  $EOS = 0$ , drawing is only performed on the pixels at coordinates  $Y = 0, X = 0, 2, 4, 6, 8, \dots$  and  $Y = 1, X = 1, 3, 5, 7, 9, \dots$

This function enables the drawn figure and ground to be mutually semi-composed.

The net drawing specification can be used with the POLYGON4 type, LINEA, LINEB, LINEC, RLINEA, RLINEB, and RLINEC commands. The NET bit should be cleared to 0 in other commands. The NET bit cannot be used together with the antialias enable bit (AA).

### (7) Even/Odd Select Specification (EOS)

Even pixels are selected when  $EOS = 0$ , and odd pixels when  $EOS = 1$ .

The even/odd select specification is used together with the net drawing specification (NET). With the LINEWC and RLINEWC commands, drawing is performed at the work coordinates with 0 when  $EOS = 0$ , and with 1 when  $EOS = 1$ .

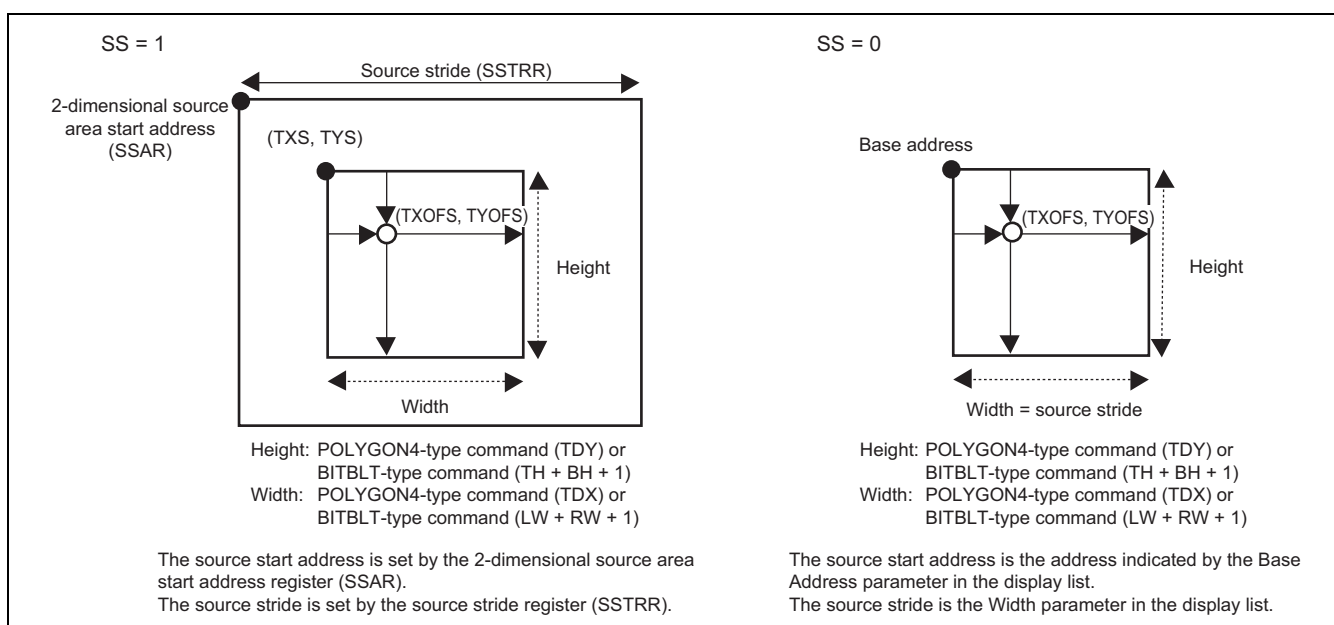
### (8) Work Specification (WORK)

When drawing is performed at rendering coordinates with the POLYGON4 type or BITBLT type command, the WORK bit can be used to select, on an individual drawing command basis, whether or not binary work data is to be referenced.

When binary work data referencing is selected, drawing is performed if the work data for the pixel corresponding to the rendering coordinates is 1, but not if the work data is 0. The same shape as that drawn at work coordinates can thus be drawn at rendering coordinates. Drawing at work coordinates can be performed either by means of the FTRAPC, RFTRAPC, LINEWC, RLINEWC, or CLRWC command. The work specification can be used with the POLYGON4 type, BITBLT type, and AAFA commands. The WORK bit should be cleared to 0 in the other commands.

### (9) Source Address Specification (SS)

The SS bit is used to select whether the source is to be referenced at a 2-dimensional source area address or at the address indicated by the base address parameter in the display list. The source address specification can be used with the POLYGON4A, POLYGON4B, BITBLTA, BITBLTB, and AAFA commands. Set the SS bit to 1 in the AAFA command, and clear to 0 in the commands for which the SS bit cannot be used. If the offset values are set, the source is referenced from (TXOFS, TYOFS).



**Figure 19.22 Example of Source Address Specification**

Note: When SS = 1, settings must be made within the ranges of  $0 \leq \text{TXS} \leq \text{SSTRR} - \text{Width}$  (TDX, LW + RW + 1),  $0 \leq \text{TYS} \leq 4,096 - \text{Height}$  (TDY, TH + BH + 1).

### (10) Source Coordinate Relative Address Specification (REL)

Setting the REL bit to 1 in the POLYGON4A, POLYGON4B, BITBLTA, BITBLTB, AAFC, LINEA, LINEB, RLINEA, RLINEB, JUMP, and GOSUB commands enables source referencing and branching to be performed at an address relative to (before or after) the command code. Clear the SS bit to 0 in the POLYGON4A or BITBLTA command; correct operation is not guaranteed when the SS bit is set to 1.

The command code address is the origin of the relative address (longword address).

Note: With the POLYGON4A, POLYGON4B, BITBLTA, BITBLTB, AAFC, LINEA, LINEB, RLINEA, and RLINEB commands, adding the address (longword: 32-bit units) where the command code is located to the source start relative address (longword: 32-bit units) must result in a quad word address (64-bit units).

**(11) Edge Drawing (EDG)**

With the FTRAPC and RFTRAPC commands, setting the EDG bit to 1 enables edge lines to be drawn after completion of trapezoid painting to the work area. Whether edge line drawing is performed with 0 or with 1 is specified by the EOS bit.

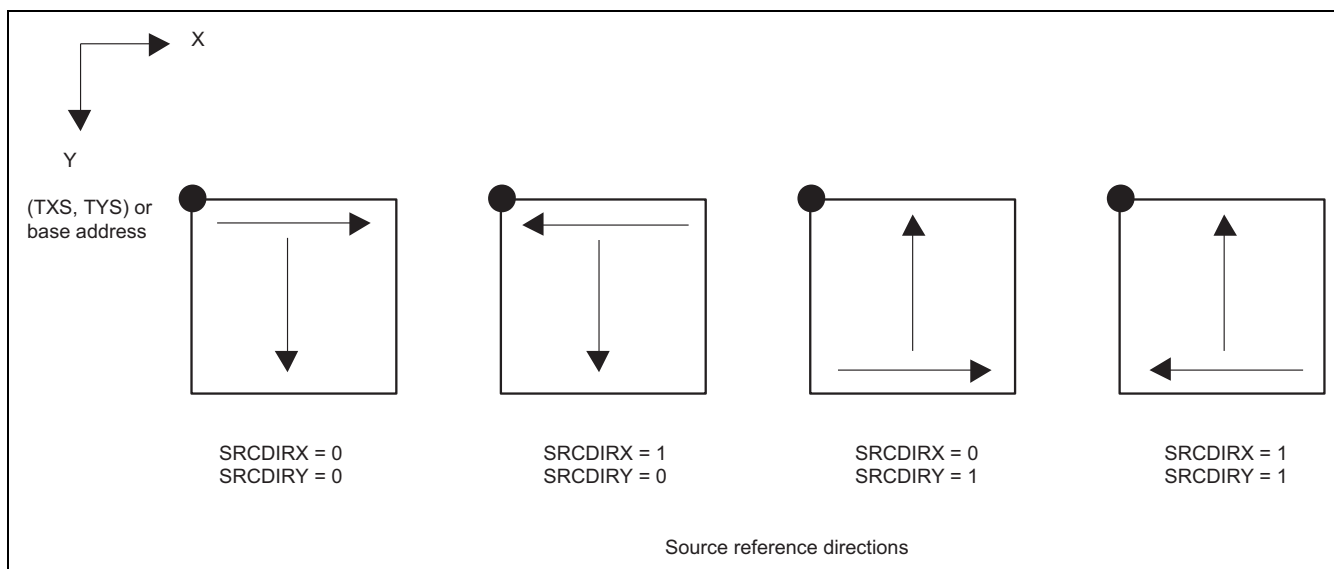
**(12) Color Offset (COOF)**

The color offset specification can be used with the POLYGON4 type, LINEA, LINEB, LINEC, RLINEA, RLINEB, RLINEC, BITBLT type, and AAFA commands. If the rendering attribute COOF bit is set to 1, the result of adding the value in COFSR to the value of the source data (color expanded data for a binary source and the specified color for the monochrome specification) is drawn. In 8-bit/pixel drawing, the COOF bit should be cleared to 0. When the source pixel format is ARGB, the A value is not used in operation.

**(13) Source Direction X, Y (SRCDIRX, SRCDIRY)**

The source direction X, Y specification can be used with the BITBLTA and BITBLTB commands. The directions in which to scan the source data are selected.

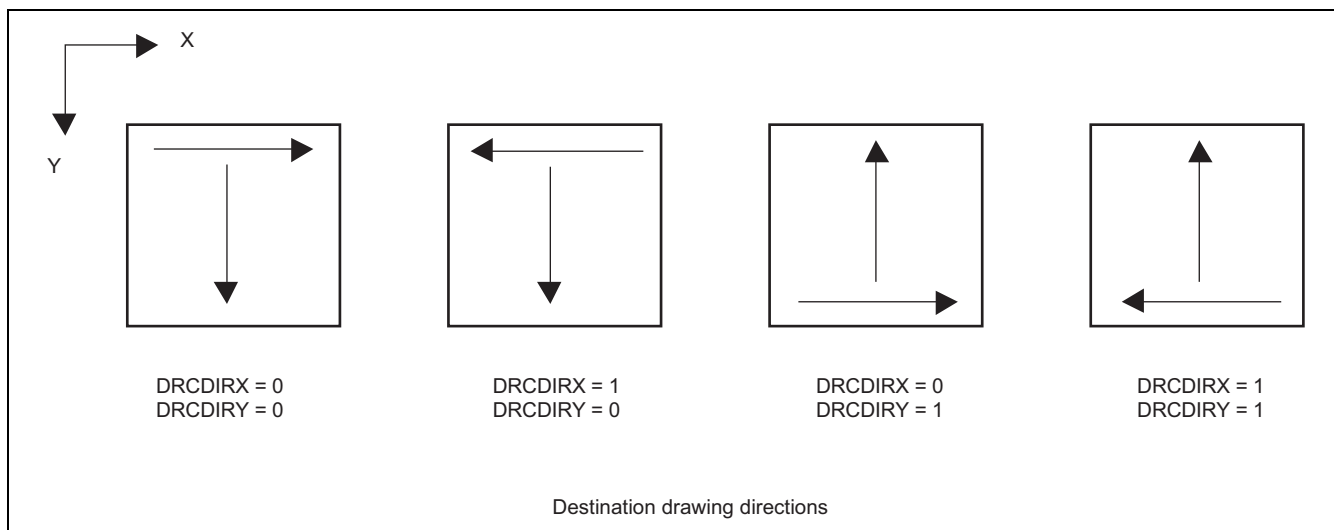
(TXS, TYS) or the base address specifies the top-left corner of the rectangle source, regardless of the source scan directions.



**Figure 19.23 Example of Source Direction Specification**

**(14) Destination Direction X, Y (DSTDIRX, DSTDIRY)**

The destination direction X, Y specification can be used with the BITBLTA, BITBLTB, and BITBLTC commands. The directions in which to draw the destination data are selected.



**Figure 19.24 Example of Destination Direction Specification**

**(15) Antialias Enable (AA)**

The antialias enable specification can be used with the LINE type and RLINE type commands to reduce alias. When the destination is set to 8-bits/pixel drawing, the AA bit should be cleared to 0. The AA bit should be set to 1 with the LINED and RLINED commands. The antialias enable specification cannot be used together with the net drawing specification (NET).

**(16) Alpha Blend Enable ( $\alpha E$ )**

The alpha blend enable specification can be used with the POLYGON4 type and BITBLT type commands. The source data (color expanded data for a binary source and the specified color for the monochrome specification) and ground data are alpha blended and drawn. The alpha value is set in the alpha value register (ALPHR). When the destination is set to 8-bit/pixel drawing, the  $\alpha E$  bit should be cleared to 0. In the POLYGON4 type commands, the alpha blend enable specification is enabled only when BLKE = 1. The  $\alpha E$  bit should be cleared to 0 when BLKE = 0. In the BITBLT type commands, the alpha blend enable specification is enabled only when the ROP code is H'CC (source copy). For other ROP codes, the  $\alpha E$  bit should be cleared to 0. The A value in the ARGB format is not alpha blended. The A value is drawn according to the source A value use (SAU) and A value (AVALUE) bits in the rendering control register (RCLR) and A Value 8 Register (AVALUE8R). In the AAFA command, set this bit to 1.

**(17) Source Alpha Enable (S $\alpha E$ )**

The source alpha enable specification can be used with the POLYGON4A, BITBLTA, and AAFA commands. The S $\alpha E$  bit is used together with the alpha blend enable bit ( $\alpha E$ ). When  $\alpha E = 0$ , the S $\alpha E$  bit should be cleared to 0.

In the ARGB1555 format (when the source pixel format bit (SPF) is 1), when the source alpha enable polarity (SAEP) is 0, only the pixels whose source A value is 1 are alpha blended. At this time, pixels whose source A value is 0 are not alpha blended and the source data is drawn back as is. When SAEP is 1, only the pixels whose source A value is 0 are alpha blended. At this time, pixels whose source A value is 1 are not alpha blended and the source data is drawn back as is.

The source alpha enable specification is enabled only when SPF = 1. The S $\alpha E$  bit should be cleared to 0 when SPF = 0.



### (18) Block Enable (BLKE)

The block enable specification can be used with POLYGON4 type commands. When  $BLKE = 1$ , the input vertex coordinates ( $DX_n, DY_n$ ) are internally transformed to circumscribed rectangular coordinates ( $DX'_n, DY'_n$ ) and four-vertex drawing is performed. When coordinate transformation is to be performed, the transformed vertices are internally converted into a rectangle and drawn. This is effective for vertically pasting a pattern even after coordinate transformation. When  $BLKE = 1$ , the direction of drawing is fixed: drawing proceeds from the upper-left corner to the lower-right corner (up-and-down and right-and-left directions cannot be reversed).

When coordinate transformation is performed by the CLRWC command, the four vertices are internally obtained from the input left and right X coordinate values and upper and lower Y coordinate values, and the coordinates for these four vertices are transformed. A circumscribed rectangle around the four vertices is then internally generated and drawn.

When coordinate transformation is performed by the FTRAPC or RFTRAPC command, the four vertices are internally obtained from the coordinate values for the circumscribed rectangle of the input polygon, and the coordinates for these four vertices are transformed. A circumscribed rectangle around the four vertices is then internally generated and drawing proceeds once the left edge is obtained. The BLKE bit should be set to 1 with the CLRWC, FTRAPC, and RFTRAPC commands.

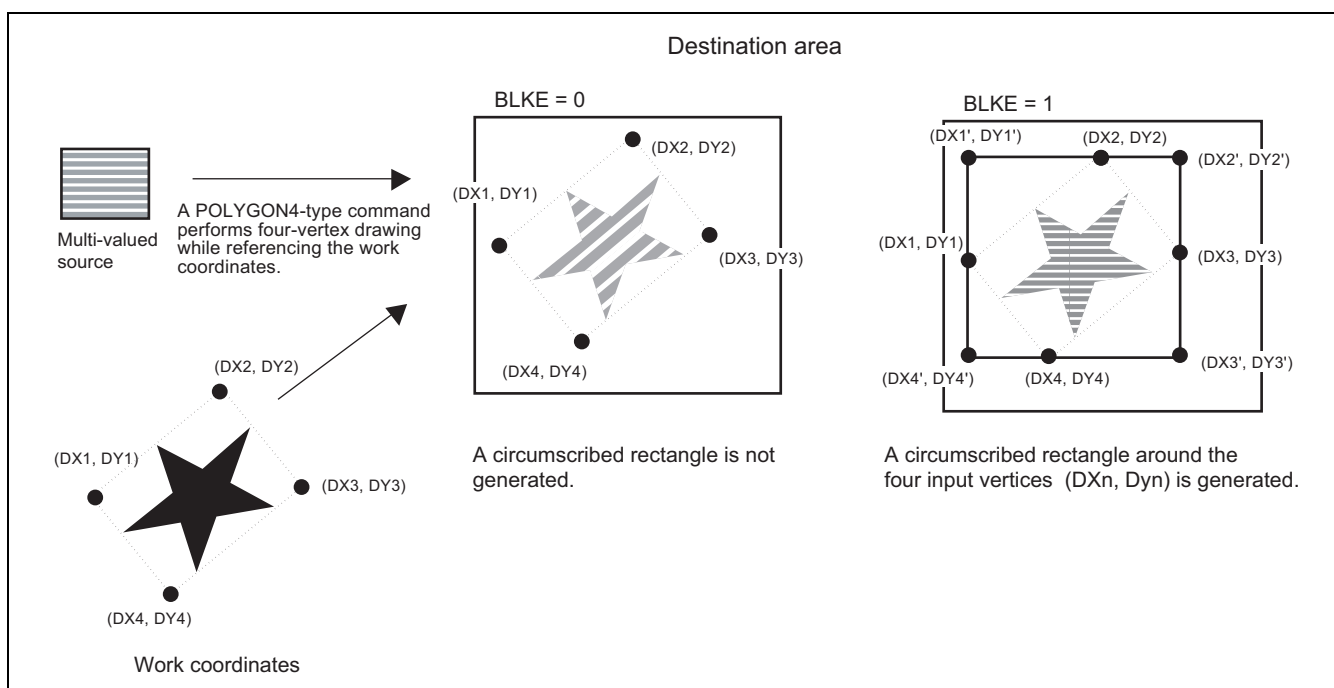


Figure 19.25 Example of Block Enable Specification

### (19) Coordinate Transformation Enable (MTRE)

Setting the MTRE bit to 1 when the coordinate transformation enable bit (GTE) in the coordinate transformation control register (GTRCR) is 1 performs coordinate transformation for the input vertex.

### (20) Link Specification Enable (LINKE)

The link specification enable specification can be used with the LINEC, LINED, RLINEC, RLINED, FTRAPC, RFTRAPC, and WPR commands. From the memory address specified by the LINK Address, the vertex coordinates are read with the LINEC, LINED, RLINEC, RLINED, FTRAPC, and RFTRAPC commands, and the register write data is read with the WPR command.

The longword address following the LINK Address is handled as the next command code. Therefore, do not specify the longword address following the address where the LINK Address is to be assigned as the link destination address specified by the LINK Address.

**(21) Link Address Relative Specification (LREL)**

The link address relative specification can be used with the LINEC, LINED, RLINEC, RLINED, FTRAPC, RFTRAPC, and WPR commands. The LREL bit is used together with the link specification enable bit (LINKE). The LREL bit should be cleared to 0 when LINKE = 0. The link destination address is specified as a relative address. The command code address is the origin of the relative address.

The longword address following the LINK Address is handled as the next command code. Therefore, do not specify the longword address following the address where the LINK Address is to be assigned as the link destination address specified by the LINK Address.

**(22) Clockwise (CLKW)**

The clockwise specification can be used with the LINED and RLINED commands. The CLKW bit is used to specify whether the order in giving the n vertices is clockwise or counterclockwise. The order is clockwise when CLKW = 1 and counterclockwise when CLKW = 0.

**(23) Raster Operation (ROP)**

The raster operation specification can be used with the BITBLT type commands. The ROP code is specified in the ROP field, which is a BITBLT command parameter.

**Table 19.10 ROP Codes**

ROP Code	Operation
H'00	0
H'11	$\sim(S \mid D)$
H'22	$\sim S \ \& \ D$
H'33	$\sim S$
H'44	$S \ \& \ \sim D$
H'55	$\sim D$
H'66	$S \ \wedge \ D$
H'77	$\sim(S \ \& \ D)$
H'88	$S \ \& \ D$
H'99	$\sim(S \ \wedge \ D)$
H'AA	D
H'BB	$\sim S \mid D$
H'CC	S
H'DD	$S \mid \sim D$
H'EE	$S \mid D$
H'FF	1

Set the ROP code to H'CC when alpha blending is enabled ( $\alpha E = 1$ ). Neither alpha blending nor raster operation is performed for the A value in the ARGB format. The A value is drawn according to the source A value use (SAU) and A value (AVALUE) bits in the rendering control register (RCLR) and A value 8 register (AVALUE8R).

## (24) Loop (LOOP)

The loop specification can be used with the LINE type, RLINE type, FTRAPC, RFTRAPC, LINEWC, and RLINEWC commands. When the loop specification is set, a closed figure, of which starting and final points are linked, is created.

- Notes:
1. Linkage section of a bold line may not be drawn with the Z clipping or 2-dimensional vertex clipping by 2DVCLPE.
  2. "n" should be 3 or greater. (2 or greater for relative specification commands)

### 19.3.6 R-GP2D Internal Cache Structure

The R-GP2D incorporates five caches: a command cache, a source (texture) cache, an  $\alpha$  map cache, a work cache, and a destination cache. The R-GP2D uses these caches for temporal storing of DDR memory data and performs drawing using the stored cached data. The following describes functions of these caches:

1. Command Cache (64 bytes)  
The command cache is used for storing of display lists in the DDR memory. This cache is cleared when rendering is started. However, it is not cleared at a restart from a suspended state with the NOP command (INT = 1).
2. Source (Texture) Cache (16 Kbytes)  
The source (texture) cache is used for storing source (texture) data in the DDR memory. This cache is cleared by TRAP, NOP (INT = 1), and VBKEM commands.
3.  $\alpha$  Map Cache (8 Kbytes)  
The  $\alpha$  map cache is used for storing  $\alpha$  map data in the DDR memory. This cache is cleared by TRAP, NOP (INT = 1), and VBKEM commands.
4. Work Cache (2 Kbytes)  
The work cache is used for drawing a figure on work coordinates and referencing work data in the DDR memory. This cache is flushed by TRAP, NOP (INT = 1), and VBKEM commands.
5. Destination Cache (2 Kbytes)  
The destination cache is used for drawing a figure on rendering coordinates in the DDR memory. This cache is flushed by TRAP, NOP (INT = 1), and VBKEM commands.

If the R-GP2D internal cache contents are not updated (the same address is referenced with data smaller than the cache size or referencing is started from the previous reference start position and ended before a position of data of the cache size is reached), the previous cache content will be used even if the DDR memory data is rewritten. This results that data coherency may not be maintained in the section where cache areas overlap.

To prevent this, contents of the caches should be updated intentionally as follows:

Reference should be made so that an address which exceeds the cache size is accessed. Contents of caches other than the command cache can be updated using the SYNC command.

## 19.4 Display List

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

### 19.4.1 4-Vertex Screen Drawing Commands

#### (1) POLYGON4A

##### (a) Function

Performs any four-vertex drawing in the destination area while referencing a multi-valued (8-, 16-, or 32-bit/pixel) source.

##### (b) Command Format

- SS = 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OP CODE = 1000_0010								Reserved (all 0)								Draw mode															
0	0	0	0	TXS ( $0 \leq \text{TXS} \leq 4,088$ )								0	0	0	0	TYS ( $0 \leq \text{TYS} \leq 4,095$ )															
0	0	0	0	TDX ( $8 \leq \text{TDX} \leq 4,095$ )								0	0	0	0	TDY ( $1 \leq \text{TDY} \leq 4,095$ )															
0	0	0	0	TXOFS ( $0 \leq \text{TXOFS} \leq \text{TDX} - 1$ )								0	0	0	0	TYOFS ( $0 \leq \text{TYOFS} \leq \text{TDY} - 1$ )															
Sign				DX1 ( $-32,768 \leq \text{DX1} \leq 32,767$ )								Sign				DY1 ( $-32,768 \leq \text{DY1} \leq 32,767$ )															
Sign				DX2 ( $-32,768 \leq \text{DX2} \leq 32,767$ )								Sign				DY2 ( $-32,768 \leq \text{DY2} \leq 32,767$ )															
Sign				DX3 ( $-32,768 \leq \text{DX3} \leq 32,767$ )								Sign				DY3 ( $-32,768 \leq \text{DY3} \leq 32,767$ )															
Sign				DX4 ( $-32,768 \leq \text{DX4} \leq 32,767$ )								Sign				DY4 ( $-32,768 \leq \text{DY4} \leq 32,767$ )															

Note:  $0 \leq \text{TXS} \leq \text{SSTRR} - \text{TDX}$ ,  $0 \leq \text{TYS} \leq 4,096 - \text{TDY}$  (SSTRR: source stride register setting)

- SS = 0 and REL = 0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OP CODE = 1000_0010								Reserved (all 0)								Draw mode															
0	0	0	Base address (quad word address)																0	0	0										
0	0	0	0	TDX ( $8 \leq \text{TDX} \leq 4,088$ )								0	0	0	0	0	0	0	0	TDY ( $1 \leq \text{TDY} \leq 4,095$ )											
0	0	0	0	TXOFS ( $0 \leq \text{TXOFS} \leq \text{TDX} - 1$ )								0	0	0	0	TYOFS ( $0 \leq \text{TYOFS} \leq \text{TDY} - 1$ )															
Sign				DX1 ( $-32,768 \leq \text{DX1} \leq 32,767$ )								Sign				DY1 ( $-32,768 \leq \text{DY1} \leq 32,767$ )															
Sign				DX2 ( $-32,768 \leq \text{DX2} \leq 32,767$ )								Sign				DY2 ( $-32,768 \leq \text{DY2} \leq 32,767$ )															
Sign				DX3 ( $-32,768 \leq \text{DX3} \leq 32,767$ )								Sign				DY3 ( $-32,768 \leq \text{DY3} \leq 32,767$ )															
Sign				DX4 ( $-32,768 \leq \text{DX4} \leq 32,767$ )								Sign				DY4 ( $-32,768 \leq \text{DY4} \leq 32,767$ )															

- SS = 0 and REL = 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
OP CODE = 1000_0010								Reserved (all 0)								Draw mode																	
Sign extended		Sign		Base Address (longword address)																								0		0			
0		0		TDX (8 ≤ TDX ≤ 4,088)								0		0		0		0		0		0		0		TDY (1 ≤ TDY ≤ 4,095)							
0		0		TXOFS (0 ≤ TXOFS ≤ TDX - 1)								0		0		0		0		TYOFS (0 ≤ TYOFS ≤ TDY - 1)													
Sign		DX1 (-32,768 ≤ DX1 ≤ 32,767)								Sign		DY1 (-32,768 ≤ DY1 ≤ 32,767)																					
Sign		DX2 (-32,768 ≤ DX2 ≤ 32,767)								Sign		DY2 (-32,768 ≤ DY2 ≤ 32,767)																					
Sign		DX3 (-32,768 ≤ DX3 ≤ 32,767)								Sign		DY3 (-32,768 ≤ DY3 ≤ 32,767)																					
Sign		DX4 (-32,768 ≤ DX4 ≤ 32,767)								Sign		DY4 (-32,768 ≤ DY4 ≤ 32,767)																					

Note: Adding the address (longword: 32-bit units) where the command code is located to the base address (longword: 32-bit units) must result in a quad word address (64-bit units).

(c) Code

B'10000010

(d) Rendering Attributes

Reference Data							Drawing Destination				
Multi-Valued Source	Binary Source	Binary Work	Specified Color	Rendering	Work						
√		√ (only WORK = 1)		√							

Draw Mode															
b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
MTRE	Fixed to 0	CLIP	RCLIP	STRANS	Fixed to 0	WORK	SS	REL	STYLE	BLKE	NET	EOS	COOF	αE	SgE

(e) Command Parameters

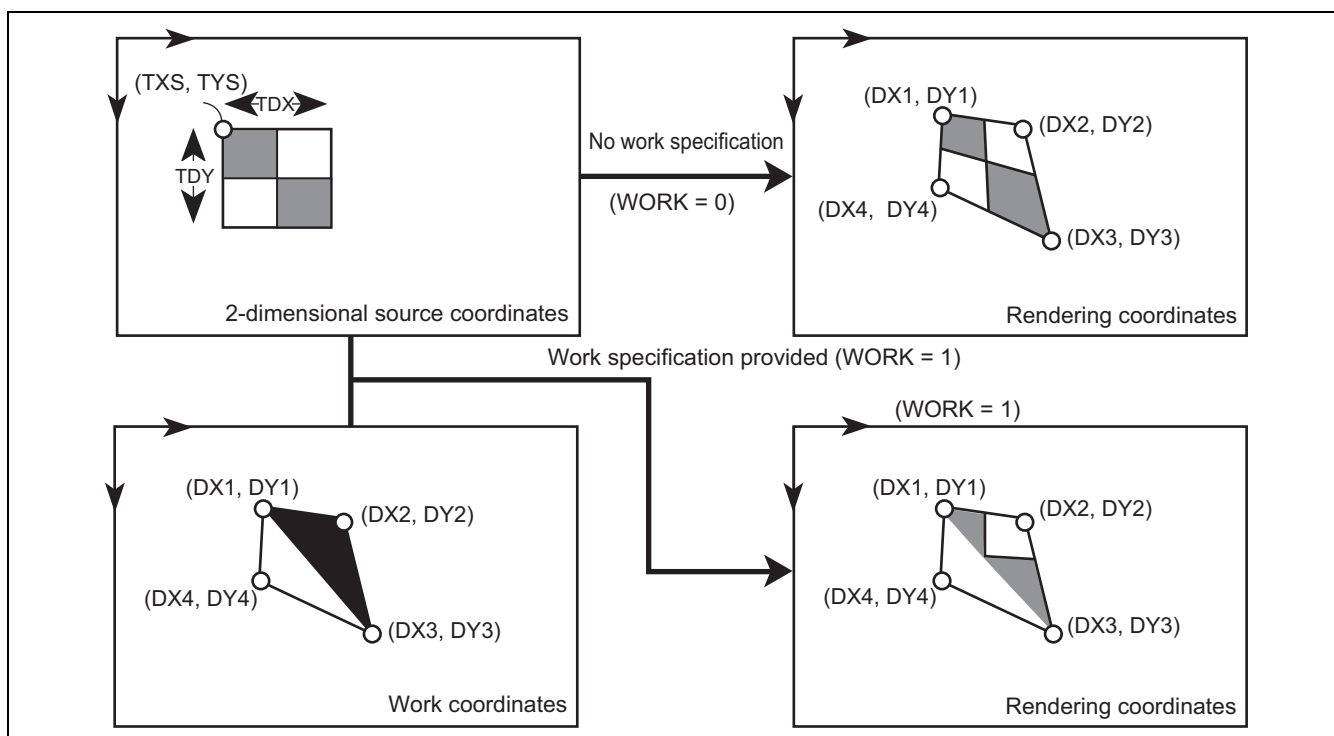
- TXS, TYS: Source starting point. Write 0 to the unused bits.
- Base address: Source start absolute address (Quad word address. Write 0 to bits A31 to A29 and A2 to A0.)  
 Source start relative address (Longword address. Negative numbers are expressed as two's complements. Bits A31 to A29 are used to extend the sign in bit A28. Write 0 to bits A1 and A0.)  
 Note: Even in 32-bit addressing mode, write the values in bits 28 to 3 of the specified 32-bit address to bits A28 to A3.
- TDX, TDY: Source size. Write 0 to the unused bits.
- DXn, DYn (n = 1 to 4): Rendering coordinates (absolute coordinates). Negative numbers are expressed as two's complements.
- TXOFS, TYOFS: Source offset. Write 0 to the unused bits.

**(f) Description**

Transfers multi-valued (8-, 16-, or 32-bit/pixel) source data to any quadrilateral rendering coordinates. The source data is always scanned horizontally, but diagonal scanning may be used in the drawing, depending on the shape. In diagonally-scanned drawing, double-writing occurs to fill in gaps.

When  $SS = 0$ , set a multiple of 8 pixels as the TDX value. When  $SS = 1$ , set 8 or more pixels as the TDX value. If the TDX setting is less than 8 pixels, multi-valued source references will not be performed normally. If TXOFS or TYOFS is set, the source at a location shifted by the offset amount is referenced. Make the TXOFS and TYOFS settings in pixel units.

1. When source style specification is selected as a rendering attribute ( $STYLE = 1$ ), the source data is not enlarged or reduced, but is referenced repeatedly.
2. When work specification is selected as a rendering attribute ( $WORK = 1$ ), only places where the work coordinate pixel is 1 are drawn at rendering coordinates while referencing work coordinates for the same coordinates as the rendering coordinates.
3. When  $SS = 1$ , the source data is referenced from the 2-dimensional source area. When  $SS = 0$ , the source data is referenced from the base address in the display list. When  $REL = 0$ , the source address can be specified as an absolute address. When  $REL = 1$ , the source address can be specified as a relative address with respect to the memory address at which the POLYGON4A command code is located.
4. If the rendering attribute COOF bit is set to 1, the result of adding the value in COFSR to the value of the multi-valued source data is drawn. The operation is performed by saturation processing. In 8-bit/pixel drawing, the COOF bit should be cleared to 0.

**(g) Example**

**Figure 19.26 Example of POLYGON4A Command Operation**

**(2) POLYGON4B****(a) Function**

Performs any four-vertex drawing in the destination area while referencing a binary (1-bit/pixel) source.

**(b) Command Format**

(i) GBM2 = 0

- SS = 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OP CODE = 1000_0001				Reserved (all 0)												Draw mode															
Color1																Color0															
0	0	0	0	TXS ( $0 \leq \text{TXS} \leq 4,088$ )												0	0	0	0	TYS ( $0 \leq \text{TYS} \leq 4,095$ )											
0	0	0	0	TDX ( $8 \leq \text{TDX} \leq 4,088$ )								0	0	0	0	0	0	0	0	TDY ( $1 \leq \text{TDY} \leq 4,095$ )											
0	0	0	0	TXOFS ( $0 \leq \text{TXOFS} \leq \text{TDX} - 1$ )												0	0	0	0	TYOFS ( $0 \leq \text{TYOFS} \leq \text{TDY} - 1$ )											
Sign				DX1 ( $-32,768 \leq \text{DX1} \leq 32,767$ )												Sign				DY1 ( $-32,768 \leq \text{DY1} \leq 32,767$ )											
Sign				DX2 ( $-32,768 \leq \text{DX2} \leq 32,767$ )												Sign				DY2 ( $-32,768 \leq \text{DY2} \leq 32,767$ )											
Sign				DX3 ( $-32,768 \leq \text{DX3} \leq 32,767$ )												Sign				DY3 ( $-32,768 \leq \text{DY3} \leq 32,767$ )											
Sign				DX4 ( $-32,768 \leq \text{DX4} \leq 32,767$ )												Sign				DY4 ( $-32,768 \leq \text{DY4} \leq 32,767$ )											

Note:  $0 \leq \text{TXS} \leq \text{SSTRR} - \text{TDX}$ ,  $0 \leq \text{TYS} \leq 4,096 - \text{TDY}$  (SSTRR: Source stride register setting)

- SS = 0 and REL = 0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OP CODE = 1000_0001				Reserved (all 0)												Draw mode															
Color1																Color0															
0	0	0	Base address (quad word address)																								0	0	0		
0	0	0	0	TDX ( $8 \leq \text{TDX} \leq 4,088$ )								0	0	0	0	0	0	0	0	TDY ( $1 \leq \text{TDY} \leq 4,095$ )											
0	0	0	0	TXOFS ( $0 \leq \text{TXOFS} \leq \text{TDX} - 1$ )												0	0	0	0	TYOFS ( $0 \leq \text{TYOFS} \leq \text{TDY} - 1$ )											
Sign				DX1 ( $-32,768 \leq \text{DX1} \leq 32,767$ )												Sign				DY1 ( $-32,768 \leq \text{DY1} \leq 32,767$ )											
Sign				DX2 ( $-32,768 \leq \text{DX2} \leq 32,767$ )												Sign				DY2 ( $-32,768 \leq \text{DY2} \leq 32,767$ )											
Sign				DX3 ( $-32,768 \leq \text{DX3} \leq 32,767$ )												Sign				DY3 ( $-32,768 \leq \text{DY3} \leq 32,767$ )											
Sign				DX4 ( $-32,768 \leq \text{DX4} \leq 32,767$ )												Sign				DY4 ( $-32,768 \leq \text{DY4} \leq 32,767$ )											

- SS = 0 and REL = 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OP CODE = 1000_0001								Reserved (all 0)								Draw mode															
Color1																Color0															
Sign extended				Sign				Base address (longword address)																0		0					
0				0				TDX ( $8 \leq TDX \leq 4,088$ )								0				0				TDY ( $1 \leq TDY \leq 4,095$ )							
0				0				TXOFS ( $0 \leq TXOFS \leq TDX - 1$ )								0				0				TYOFS ( $0 \leq TYOFS \leq TDY - 1$ )							
Sign								DX1 ( $-32,768 \leq DX1 \leq 32,767$ )								Sign								DY1 ( $-32,768 \leq DY1 \leq 32,767$ )							
Sign								DX2 ( $-32,768 \leq DX2 \leq 32,767$ )								Sign								DY2 ( $-32,768 \leq DY2 \leq 32,767$ )							
Sign								DX3 ( $-32,768 \leq DX3 \leq 32,767$ )								Sign								DY3 ( $-32,768 \leq DY3 \leq 32,767$ )							
Sign								DX4 ( $-32,768 \leq DX4 \leq 32,767$ )								Sign								DY4 ( $-32,768 \leq DY4 \leq 32,767$ )							

Note: Adding the address (longword: 32-bit units) where the command code is located to the base address (longword: 32-bit units) must result in a quad word address (64-bit units).

- (ii) GBM2 = 1

- SS = 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OP CODE=1000_0001								Reserve (all 0)								Draw Mode															
Color0																															
Color1																															
0				0				TXS ( $0 \leq TXS \leq 4,088$ )								0				0				TYS ( $0 \leq TYS \leq 4,095$ )							
0				0				TDX ( $8 \leq TDX \leq 4,088$ )								0				0				TDY ( $1 \leq TDY \leq 4,095$ )							
0				0				TXOFS ( $0 \leq TXOFS \leq TDX - 1$ )								0				0				TYOFS ( $0 \leq TYOFS \leq TDY - 1$ )							
Sign								TYOFS ( $0 \leq TYOFS \leq TDY - 1$ )								Sign								DY1( $-32,768 \leq DY1 \leq 32,767$ )							
Sign								DX2( $-32,768 \leq DX2 \leq 32,767$ )								Sign								DY2( $-32,768 \leq DY2 \leq 32,767$ )							
Sign								DX3( $-32,768 \leq DX3 \leq 32,767$ )								Sign								DY3( $-32,768 \leq DY3 \leq 32,767$ )							
Sign								DX4( $-32,768 \leq DX4 \leq 32,767$ )								Sign								DY4( $-32,768 \leq DY4 \leq 32,767$ )							

Note:  $0 \leq TXS \leq SSTRR-TDX \leq 0 \leq TYS \leq 4,096-TDY$  (SSTRR: Source stride register setting)

- SS = 0 and REL = 0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OP CODE = 1000_0001								Reserved (all 0)								Draw mode															
Color0																															
Color1																															
0				0				Base address (quad word address)																0		0		0			
0				0				TDX ( $8 \leq TDX \leq 4,088$ )								0				0				TDY ( $1 \leq TDY \leq 4,095$ )							
0				0				TXOFS ( $0 \leq TXOFS \leq TDX - 1$ )								0				0				TYOFS ( $0 \leq TYOFS \leq TDY - 1$ )							
Sign								DX1 ( $-32,768 \leq DX1 \leq 32,767$ )								Sign								DY1 ( $-32,768 \leq DY1 \leq 32,767$ )							
Sign								DX2 ( $-32,768 \leq DX2 \leq 32,767$ )								Sign								DY2 ( $-32,768 \leq DY2 \leq 32,767$ )							
Sign								DX3 ( $-32,768 \leq DX3 \leq 32,767$ )								Sign								DY3 ( $-32,768 \leq DY3 \leq 32,767$ )							
Sign								DX4 ( $-32,768 \leq DX4 \leq 32,767$ )								Sign								DY4 ( $-32,768 \leq DY4 \leq 32,767$ )							



- SS = 0 and REL = 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OP CODE = 1000_0001								Reserved (all 0)								Draw mode															
Color0																															
Color1																															
Sign extended		Sign		Base address (longword address)																								0		0	
0 0 0 0				TDX ( $8 \leq TDX \leq 4,088$ )																0 0 0 0				TDY ( $1 \leq TDY \leq 4,095$ )							
0 0 0 0				TXOFS ( $0 \leq TXOFS \leq TDX - 1$ )																0 0 0 0				TYOFS ( $0 \leq TYOFS \leq TDY - 1$ )							
Sign		DX1 ( $-32,768 \leq DX1 \leq 32,767$ )																Sign		DY1 ( $-32,768 \leq DY1 \leq 32,767$ )											
Sign		DX2 ( $-32,768 \leq DX2 \leq 32,767$ )																Sign		DY2 ( $-32,768 \leq DY2 \leq 32,767$ )											
Sign		DX3 ( $-32,768 \leq DX3 \leq 32,767$ )																Sign		DY3 ( $-32,768 \leq DY3 \leq 32,767$ )											
Sign		DX4 ( $-32,768 \leq DX4 \leq 32,767$ )																Sign		DY4 ( $-32,768 \leq DY4 \leq 32,767$ )											

Note: Adding the address (longword: 32-bit units) where the command code is located to the base address (longword: 32-bit units) must result in a quad word address (64-bit units).

### (c) Code

B'10000001

### (d) Rendering Attributes

Reference Data							Drawing Destination									
Multi-Valued Source	Binary Source	Binary Work	Specified Color	Rendering	Work											
	√	√		√												
		(only WORK = 1)														

Draw Mode															
b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
MTRE	Fixed to 0	CLIP	RCLIP	STRANS	Fixed to 0	WORK	SS	REL	STYLE	BLKE	NET	EOS	COOF	αE	Fixed to 0

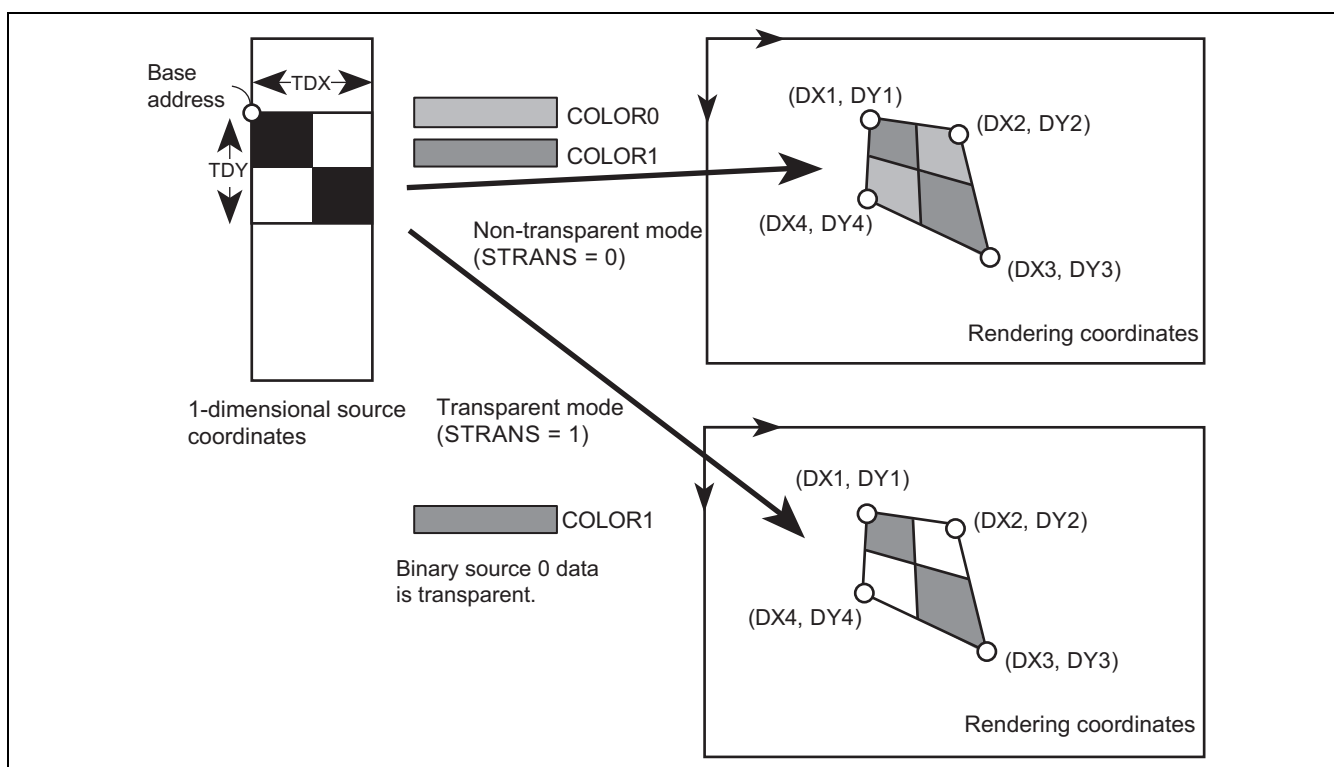
### (e) Command Parameters

- TXS, TYS: Source starting point. Write 0 to the unused bits.
- Base address: Source start absolute address (Quad word address. Write 0 to bits A31 to A29 and A2 to A0.)  
 Source start relative address (Longword address. Negative numbers are expressed as two's complements. Bits A31 to A29 are used to extend the sign in bit A28. Write 0 to bits A1 and A0.)  
 Note: Even in 32-bit addressing mode, write the values in bits 28 to 3 of the specified 32-bit address to bits A28 to A3.
- TDX, TDY: Source size. Write 0 to the unused bits.
- DXn, DYn (n = 1 to 4): Rendering coordinates (absolute coordinates). Negative numbers are expressed as two's complements.
- TXOFS, TYOFS: Source offset. Write 0 to the unused bits.
- Color0, Color1: 8-, 16-, or 32-bit/pixel color specification. For 16-bit/pixel drawing, the color specification should match the destination pixel format.  
 For 8-bit/pixel drawing, the same value should be set in the upper and lower bytes.

**(f) Description**

Draws binary (1-bit/pixel) source data in any quadrilateral rendering area, using the colors specified by parameters Color0 and Color1. For the color specifications (Color0 and Color1) in 8-bit/pixel drawing, set the same 8-bit data in the upper and lower bytes. The source data is always scanned horizontally, but diagonal scanning may be used in the drawing, depending on the shape. In diagonally-scanned drawing, double-writing occurs to fill in gaps. A multiple of 8 pixels must be set as the TDX value, regardless of the SS bit value. If TXOFS or TYOFS is set, the source at a location shifted by the offset amount is referenced. Make the TXOFS and TYOFS settings in pixel units.

1. When source style specification is selected as a rendering attribute (STYLE = 1), the source data is not enlarged or reduced, but is referenced repeatedly.
2. When work specification is selected as a rendering attribute (WORK = 1), only places where the work coordinate pixel is 1 are drawn at rendering coordinates while referencing work coordinates for the same coordinates as the rendering coordinates.
3. When REL = 0, the source address can be specified as an absolute address. When REL = 1, the source address can be specified as a relative address with respect to the memory address at which the POLYGON4B command code is located.

**(g) Example**

**Figure 19.27 Example of POLYGON4B Command Operation**

**(3) POLYGON4C****(a) Function**

Performs any four-vertex drawing at rendering coordinates with a monochrome specification.

**(b) Command Format**

- GBM2 = 0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OP CODE = 1000_0000								Reserved (all 0)								Draw mode															
All 0																Color															
Sign		DX1 ( $-32,768 \leq DX1 \leq 32,767$ )										Sign		DY1 ( $-32,768 \leq DY1 \leq 32,767$ )																	
Sign		DX2 ( $-32,768 \leq DX2 \leq 32,767$ )										Sign		DY2 ( $-32,768 \leq DY2 \leq 32,767$ )																	
Sign		DX3 ( $-32,768 \leq DX3 \leq 32,767$ )										Sign		DY3 ( $-32,768 \leq DY3 \leq 32,767$ )																	
Sign		DX4 ( $-32,768 \leq DX4 \leq 32,767$ )										Sign		DY4 ( $-32,768 \leq DY4 \leq 32,767$ )																	

- GBM2 = 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OP CODE = 1000_0000								Reserved (all 0)								Draw mode															
																Color															
Sign		DX1 ( $-32,768 \leq DX1 \leq 32,767$ )										Sign		DY1 ( $-32,768 \leq DY1 \leq 32,767$ )																	
Sign		DX2 ( $-32,768 \leq DX2 \leq 32,767$ )										Sign		DY2 ( $-32,768 \leq DY2 \leq 32,767$ )																	
Sign		DX3 ( $-32,768 \leq DX3 \leq 32,767$ )										Sign		DY3 ( $-32,768 \leq DY3 \leq 32,767$ )																	
Sign		DX4 ( $-32,768 \leq DX4 \leq 32,767$ )										Sign		DY4 ( $-32,768 \leq DY4 \leq 32,767$ )																	

**(c) Code**

B'10000000

**(d) Rendering Attributes**

Multi-Valued Source	Reference Data				Drawing Destination	
	Binary Source	Binary Work	Specified Color	Rendering	Work	
		√ (only WORK = 1)	√	√		

Draw Mode															
b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
MTRE	Fixed to 0	CLIP	RCLIP	Fixed to 0	Fixed to 0	WORK	Fixed to 0	Fixed to 0	Fixed to 0	BLKE	NET	EOS	COOF	αE	Fixed to 0

**(e) Command Parameters**

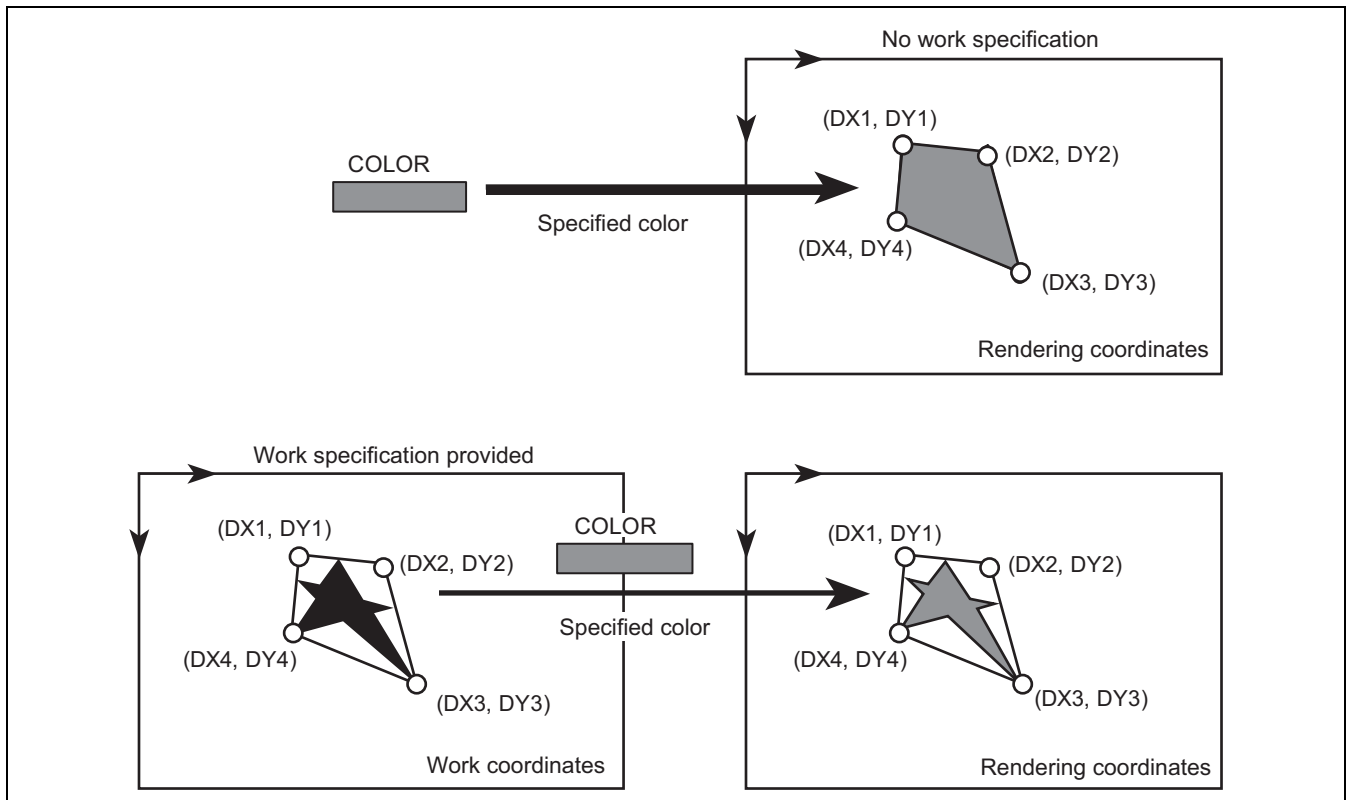
DX<sub>n</sub>, DY<sub>n</sub> (n = 1 to 4): Rendering coordinates (absolute coordinates). Negative numbers are expressed as two's complements.

Color: 8-, 16-, or 32-bit/pixel color specification. For 16-bit/pixel drawing, the color specification should match the destination pixel format.

For 8-bit/pixel drawing, the same value should be set in the upper and lower bytes.

**(f) Description**

Draws any quadrilateral in the rendering area in the single color specified by the Color parameter. When work specification is selected as a rendering attribute ( $WORK = 1$ ), only places where the work coordinate pixel is 1 are drawn at rendering coordinates while referencing work coordinates for the same coordinates as the rendering coordinates.

**(g) Example**

**Figure 19.28 Example of POLYGON4C Command Operation**

## 19.4.2 Line Drawing Commands

### (1) LINEA

#### (a) Function

Draws a polygonal line with any width in the destination area while referencing a multi-valued (8-, 16-, or 32-bit/pixel) source.

#### (b) Command Format

- REL = 0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OP CODE = 1011_0010								Reserved (all 0)								Draw mode															
0 0 0			Base address (quad word address)																								0 0 0				
0 0 0 0				TDX ( $8 \leq TDX \leq 4,088$ )												0 0 0 0 0 0 0 0				TDY ( $1 \leq TDY \leq 4,095$ )											
0 0 0 0				TXOFS ( $0 \leq TXOFS \leq TDX - 1$ )												n ( $2 \leq n \leq 65535$ )															
Reserved (all 0)															0 0 0 0 0 0 0 0				W ( $0, 2 \leq W \leq 63$ )												
Sign		DX1 ( $-32,768 \leq DX1 \leq 32,767$ )												Sign		DY1 ( $-32,768 \leq DY1 \leq 32,767$ )															
Sign		:												Sign		:															
Sign		:												Sign		:															
Sign		DXn ( $-32,768 \leq DXn \leq 32,767$ )												Sign		DYn ( $-32,768 \leq DYn \leq 32,767$ )															

- Notes:
- When W = 0, set TDY to 1.
  - When n = 0 or 1, correct operation is not guaranteed.

- REL = 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OP CODE = 1011_0010								Reserved (all 0)								Draw mode															
Sign extended		Sign		Base address (longword address)																								0 0			
0 0 0 0				TDX ( $8 \leq TDX \leq 4,088$ )												0 0 0 0 0 0 0 0				TDY ( $1 \leq TDY \leq 4,095$ )											
0 0 0 0				TXOFS ( $0 \leq TXOFS \leq TDX - 1$ )												n ( $2 \leq n \leq 65,535$ )															
Reserved (all 0)															0 0 0 0 0 0 0 0				W ( $0, 2 \leq W \leq 63$ )												
Sign		DX1 ( $-32,768 \leq DX1 \leq 32,767$ )												Sign		DY1 ( $-32,768 \leq DY1 \leq 32,767$ )															
Sign		:												Sign		:															
Sign		:												Sign		:															
Sign		DXn ( $-32,768 \leq DXn \leq 32,767$ )												Sign		DYn ( $-32,768 \leq DYn \leq 32,767$ )															

- Notes:
- Adding the address (longword: 32-bit units) where the command code is located to the base address (longword: 32-bit units) must result in a quad word address (64-bit units).
  - When W = 0, set TDY to 1.
  - When n = 0 or 1, correct operation is not guaranteed.

#### (c) Code

B'10110010

**(d) Rendering Attributes**

Reference Data										Drawing Destination						
Multi-Valued Source	Binary Source					Binary Work		Specified Color			Rendering	Work				
√											√					
Draw Mode																
b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0	
MTRE	LOOP	CLIP	RCLIP	STRANS	Fixed to 0	Fixed to 0	SS (0)	REL	STYLE (1)	Fixed to 0	NET	EOS	COOF	AA	Fixed to 0	

- Notes: 1. Clear the SS bit to 0.  
2. Set the STYLE bit to 1.

**(e) Command Parameters**

- Base address: Source start absolute address (Quad word address. Write 0 to bits A31 to A29 and A2 to A0.)  
Source start relative address (Longword address. Negative numbers are expressed as two's complements. Bits A31 to A29 are used to extend the sign in bit A28. Write 0 to bits A1 and A0.)  
Note: Even in 32-bit addressing mode, write the values in bits 28 to 3 of the specified 32-bit address to bits A28 to A3.
- TDX, TDY: Source size. Write 0 to the unused bits.
- TXOFS: Source offset. Write 0 to the unused bits.
- n (n = 2 to 65,535): Number of vertices
- W: Line width. Set a 6-bit integer. Write 0 to the unused bits.  
When 0 is set in W, a polygonal line of line width 1 is drawn. Setting 1 in W is prohibited.
- DX<sub>i</sub> (i = 1 to 65,535): Rendering coordinate (absolute coordinate). Negative numbers are expressed as two's complements.
- DY<sub>i</sub> (i = 1 to 65,535): Rendering coordinate (absolute coordinate). Negative numbers are expressed as two's complements.

**(f) Description**

Draws a polygonal line from vertex 1 (DX<sub>1</sub>, DY<sub>1</sub>), through vertex 2 (DX<sub>2</sub>, DY<sub>2</sub>), ..., vertex n – 1 (DX<sub>n – 1</sub>, DY<sub>n – 1</sub>), to vertex n (DX<sub>n</sub>, DY<sub>n</sub>). Set a multiple of 8 pixels as the TDX value. If TXOFS is set, the source at a location shifted by the offset amount is referenced. Make the TXOFS setting in pixel units. Pattern repetition selected when the STYLE bit = 1 is only performed in the X direction of the source data. The source data is enlarged or reduced in proportion to the line width in the Y direction.

When a value greater than 1 is set in W, a bold line can be drawn.

- Notes: 1. 8-point drawing is used for a line width of 1. 4-point drawing is used for bold line drawing.
2. The final point of each line segment is drawn. When the starting and final coordinate points of a line segment match, a single dot is drawn for a line width of 1 and nothing is drawn for bold line drawing
3. When AA = 1, note the following:
- For a dashed line, antialiasing is not performed for the gaps in the dashed line.
  - When the starting and final coordinate points of a line segment match, antialiasing is not performed.
  - When the NAA (new antialias mode) bit is 0, antialiasing is not performed for horizontal, vertical, and 45-degree diagonal line segments. When the NAA bit is 1, antialiasing is performed for horizontal, vertical, and 45-degree diagonal line segments.

**(2) LINEB****(a) Function**

Draws a polygonal line with any width in the destination area while referencing a binary (1-bit/pixel) source.

**(b) Command Format**

(i) GBM2 = 0

- REL = 0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
OP CODE = 1011_0001								Reserved (all 0)								Draw mode																			
Color1																Color0																			
0	0	0	Base address (quad word address)																0	0	0														
0	0	0	0	TDX ( $8 \leq TDX \leq 4,088$ )								0	0	0	0	0	0	0	0	TDY ( $1 \leq TDY \leq 4,095$ )															
0	0	0	0	TXOFS ( $0 \leq TXOFS \leq TDX - 1$ )												n ( $2 \leq n \leq 65,535$ )																			
Reserved (all 0)												0	0	0	0	0	0	0	0	0	0	0	0	W ( $0,2 \leq W \leq 63$ )											
Sign		DX1 ( $-32,768 \leq DX1 \leq 32,767$ )												Sign		DY1 ( $-32,768 \leq DY1 \leq 32,767$ )																			
Sign		:																Sign		:															
Sign		:																Sign		:															
Sign		DXn ( $-32,768 \leq DXn \leq 32,767$ )												Sign		DYn ( $-32,768 \leq DYn \leq 32,767$ )																			

- Notes:
1. When W = 0, set TDY to 1.
  2. When n = 0 or 1, correct operation is not guaranteed.

- REL = 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
OP CODE = 1011_0001								Reserved (all 0)								Draw mode																			
Color1																Color0																			
Sign extended		Sign		Base address (longword address)																0		0													
0	0	0	0	TDX ( $8 \leq TDX \leq 4,088$ )								0	0	0	0	0	0	0	0	TDY ( $1 \leq TDY \leq 4,095$ )															
0	0	0	0	TXOFS ( $0 \leq TXOFS \leq TDX - 1$ )												n ( $2 \leq n \leq 65,535$ )																			
Reserved (all 0)												0	0	0	0	0	0	0	0	0	0	0	0	W ( $0,2 \leq W \leq 63$ )											
Sign		DX1 ( $-32,768 \leq DX1 \leq 32,767$ )												Sign		DY1 ( $-32,768 \leq DY1 \leq 32,767$ )																			
Sign		:																Sign		:															
Sign		:																Sign		:															
Sign		DXn ( $-32,768 \leq DXn \leq 32,767$ )												Sign		DYn ( $-32,768 \leq DYn \leq 32,767$ )																			

- Notes:
1. Adding the address (longword: 32-bit units) where the command code is located to the base address (longword: 32-bit units) must result in a quad word address (64-bit units).
  2. When W = 0, set TDY to 1.
  3. When n = 0 or 1, correct operation is not guaranteed.

(ii) GBM2 = 1

- REL = 0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0								
OP CODE = 1011_0001								Reserved (all 0)								Draw mode																							
Color0																																							
Color1																																							
0 0 0			Base address (quad word address)																								0 0 0												
0 0 0 0				TDX ( $8 \leq TDX \leq 4,088$ )								0 0 0 0 0 0 0 0								TDY ( $1 \leq TDY \leq 4,095$ )																			
0 0 0 0				TXOFS ( $0 \leq TXOFS \leq TDX - 1$ )																n ( $2 \leq n \leq 65,535$ )																			
Reserved (all 0)																0 0 0 0 0 0 0 0 0 0 0 0								W ( $0,2 \leq W \leq 63$ )															
Sign								DX1 ( $-32,768 \leq DX1 \leq 32,767$ )																Sign								DY1 ( $-32,768 \leq DY1 \leq 32,767$ )							
Sign								:																Sign								:							
Sign								:																Sign								:							
Sign								DXn ( $-32,768 \leq DXn \leq 32,767$ )																Sign								DYn ( $-32,768 \leq DYn \leq 32,767$ )							

- Notes: 1. When W = 0, set TDY to 1.  
2. When n = 0 or 1, correct operation is not guaranteed.

- REL = 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0								
OP CODE = 1011_0001								Reserved (all 0)								Draw mode																							
Color0																																							
Color1																																							
Sign extended		Sign	Base address (longword address)																								0 0												
0 0 0 0				TDX ( $8 \leq TDX \leq 4,088$ )								0 0 0 0 0 0 0 0								TDY ( $1 \leq TDY \leq 4,095$ )																			
0 0 0 0				TXOFS ( $0 \leq TXOFS \leq TDX - 1$ )																n ( $2 \leq n \leq 65,535$ )																			
Reserved (all 0)																0 0 0 0 0 0 0 0 0 0 0 0								W ( $0,2 \leq W \leq 63$ )															
Sign								DX1 ( $-32,768 \leq DX1 \leq 32,767$ )																Sign								DY1 ( $-32,768 \leq DY1 \leq 32,767$ )							
Sign								:																Sign								:							
Sign								:																Sign								:							
Sign								DXn ( $-32,768 \leq DXn \leq 32,767$ )																Sign								DYn ( $-32,768 \leq DYn \leq 32,767$ )							

- Notes: 1. Adding the address (longword: 32-bit units) where the command code is located to the base address (longword: 32-bit units) must result in a quad word address (64-bit units).  
2. When W = 0, set TDY to 1.  
3. When n = 0 or 1, correct operation is not guaranteed.

(c) Code

B'10110001



**(d) Rendering Attributes**

Reference Data								Drawing Destination							
Multi-Valued Source	Binary Source				Binary Work		Specified Color		Rendering				Work		
	√								√						
Draw Mode															
b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
MTRE	LOOP	CLIP	RCLIP	STRANS	Fixed to 0	Fixed to 0	SS (0)	REL	STYLE (1)	Fixed to 0	NET	EOS	COOF	AA	Fixed to 0

- Notes: 1. Clear the SS bit to 0.  
2. Set the STYLE bit to 1.

**(e) Command Parameters**

- Color0, Color1: 8-, 16-, or 32-bit/pixel color specification. For 16-bit/pixel drawing, the color specification should match the destination pixel format.  
For 8-bit/pixel drawing, the same value should be set in the upper and lower bytes.
- Base address: Source start absolute address (Quad word address. Write 0 to bits A31 to A29 and A2 to A0.)  
Source start relative address (Longword address. Negative numbers are expressed as two's complements. Bits A31 to A29 are used to extend the sign in bit A28. Write 0 to bits A1 and A0.)  
Note: Even in 32-bit addressing mode, write the values in bits 28 to 3 of the specified 32-bit address to bits A28 to A3.
- TDX, TDY: Source size. Write 0 to the unused bits.
- TXOFS: Source offset. Write 0 to the unused bits.
- n (n = 2 to 65,535): Number of vertices
- W: Line width. Set a 6-bit integer. Write 0 to the unused bits.  
When 0 is set in W, a polygonal line of line width 1 is drawn. Setting 1 in W is prohibited.
- DX<sub>i</sub> (i = 1 to 65,535): Rendering coordinate (absolute coordinate). Negative numbers are expressed as two's complements.
- DY<sub>i</sub> (i = 1 to 65,535): Rendering coordinate (absolute coordinate). Negative numbers are expressed as two's complements.

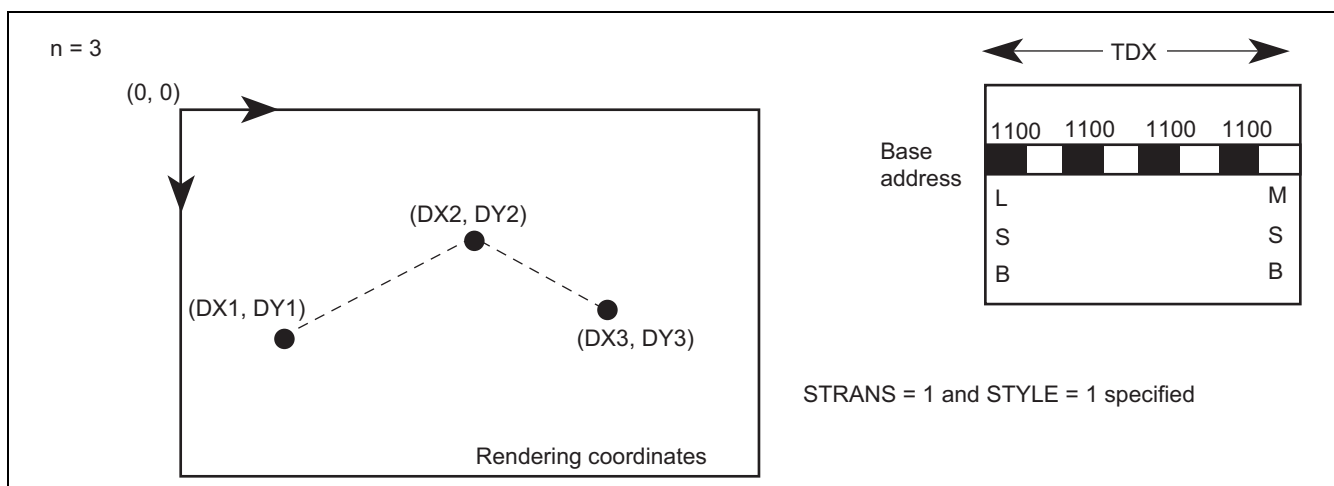
**(f) Description**

Draws a polygonal line from vertex 1 (DX1, DY1), through vertex 2 (DX2, DY2), ..., vertex n - 1 (DXn - 1, DYn - 1), to vertex n (DXn, DYn). Set a multiple of 8 pixels as the TDX value. If TXOFS is set, the source at a location shifted by the offset amount is referenced. Make the TXOFS setting in pixel units. Pattern repetition selected when the STYLE bit = 1 is only performed in the X direction of the source data. The source data is enlarged or reduced in proportion to the line width in the Y direction.

When a value greater than 1 is set in W, a bold line can be drawn.

- Notes:
1. 8-point drawing is used for a line width of 1. 4-point drawing is used for bold line drawing.
  2. The final point of each line segment is drawn. When the starting and final coordinate points of a line segment match, a single dot is drawn for a line width of 1 and nothing is drawn for bold line drawing.
  3. When AA = 1, note the following:
    - For a dashed line, antialiasing is not performed for the gaps in the dashed line.
    - When the starting and final coordinate points of a line segment match, antialiasing is not performed.
    - When the NAA (new antialias mode) bit is 0, antialiasing is not performed for horizontal, vertical, and 45-degree diagonal line segments. When the NAA bit is 1, antialiasing is performed for horizontal, vertical, and 45-degree diagonal line segments.

**(g) Example**



**Figure 19.29 Example of LINEB Command Operation**

**(3) LINEC****(a) Function**

Draws a polygonal line with any width in the destination area with a monochrome specification.

**(b) Command Format**

(i) GBM2 = 0

- LINKE = 0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
OP CODE = 1011_0000								Reserved (all 0)								Draw mode																			
Color																n (2 ≤ n ≤ 65,535)																			
Reserved (all 0)																0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	W (0,2 ≤ W ≤ 63)			
Sign								DX1 (-32,768 ≤ DX1 ≤ 32,767)								Sign								DY1 (-32,768 ≤ DY1 ≤ 32,767)											
Sign								:								Sign								:											
Sign								:								Sign								:											
Sign								DXn (-32,768 ≤ DXn ≤ 32,767)								Sign								DYn (-32,768 ≤ DYn ≤ 32,767)											

Note: When n = 0 or 1, correct operation is not guaranteed.

- LINKE = 1 and LREL = 0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
OP CODE = 1011_0000								Reserved (all 0)								Draw mode																			
Color																n (2 ≤ n ≤ 65,535)																			
Reserved (all 0)																0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	W (0,2 ≤ W ≤ 63)			
0	0	0	LINK address (longword address)														0	0																	

Notes: 1. When n = 0 or 1, correct operation is not guaranteed.

2. The longword address following the LINK address is handled as the next command code. Therefore, do not specify the longword address following the address where the LINK address is to be assigned as the link destination address specified by the LINK address.

- LINKE = 1 and LREL = 1

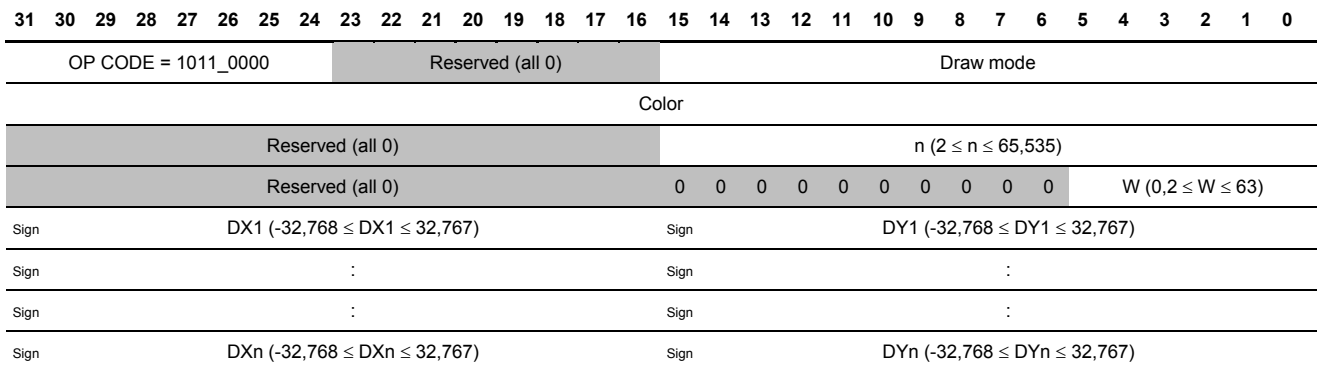
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
OP CODE = 1011_0000								Reserved (all 0)								Draw mode																			
Color																n (2 ≤ n ≤ 65,535)																			
Reserved (all 0)																0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	W (0,2 ≤ W ≤ 63)			
Sign extended		Sign		LINK address (longword address)														0		0															

Notes: 1. When n = 0 or 1, correct operation is not guaranteed.

2. The longword address following the LINK address is handled as the next command code. Therefore, do not specify the longword address following the address where the LINK address is to be assigned as the link destination address specified by adding the address where the command code is located to the LINK address.

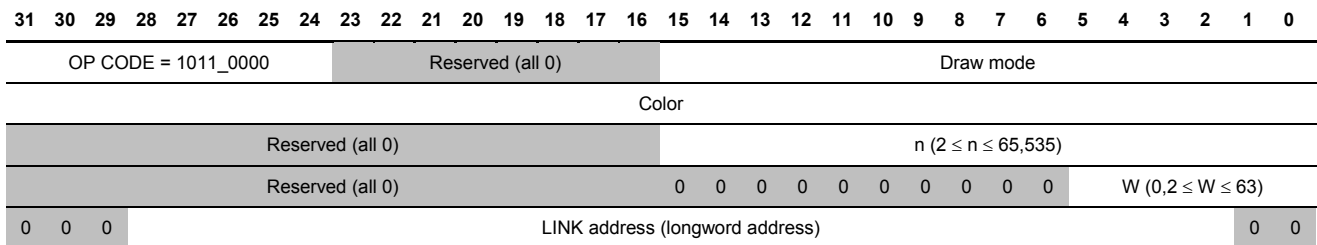
(ii) GBM2 = 1

- LINKE = 0



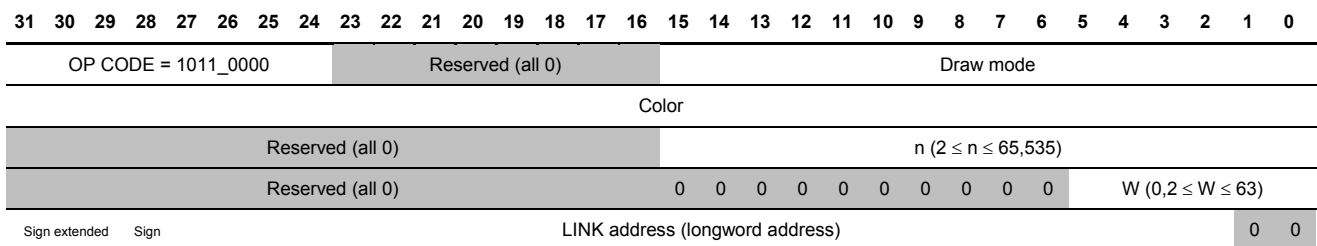
Note: When n = 0 or 1, correct operation is not guaranteed.

- LINKE = 1 and LREL = 0



Notes: 1. When n = 0 or 1, correct operation is not guaranteed.  
 2. The longword address following the LINK address is handled as the next command code. Therefore, do not specify the longword address following the address where the LINK address is to be assigned as the link destination address specified by the LINK address.

- LINKE = 1 and LREL = 1



Notes: 1. When n = 0 or 1, correct operation is not guaranteed.  
 2. The longword address following the LINK address is handled as the next command code. Therefore, do not specify the longword address following the address where the LINK address is to be assigned as the link destination address specified by adding the address where the command code is located to the LINK address.

(c) Code

B'10110000

**(d) Rendering Attributes**

		Reference Data				Drawing Destination									
Multi-Valued Source	Binary Source	Binary Work	Specified Color	Rendering	Work										
			√	√											
Draw Mode															
b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
MTRE	LOOP	CLIP	RCLIP	Fixed to 0	LINKE	LREL	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	NET	EOS	COOF	AA	Fixed to 0

**(e) Command Parameters**

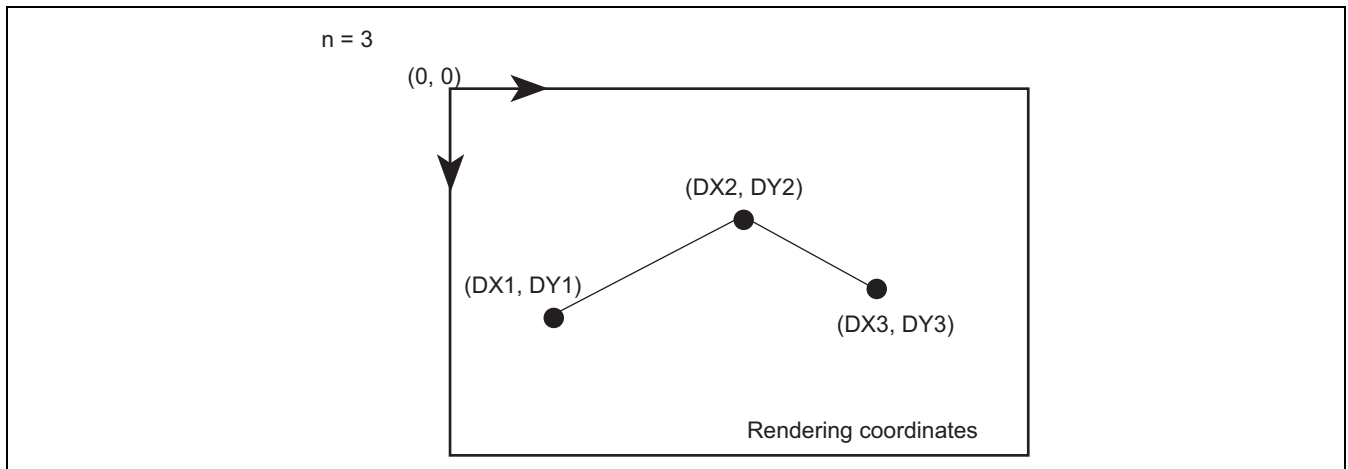
- Color: 8-, 16-, or 32-bit/pixel color specification. For 16-bit/pixel drawing, the color specification should match the destination pixel format.  
For 8-bit/pixel drawing, the same value should be set in the upper and lower bytes.
- n (n = 2 to 65,535): Number of vertices
- W: Line width. Set a 6-bit integer. Write 0 to the unused bits.  
When 0 is set in W, a polygonal line of line width 1 is drawn. Setting 1 in W is prohibited.
- DX<sub>i</sub> (i = 1 to 65,535): Rendering coordinate (absolute coordinate). Negative numbers are expressed as two's complements.
- DY<sub>i</sub> (i = 1 to 65,535): Rendering coordinate (absolute coordinate). Negative numbers are expressed as two's complements.
- LINK address: LINK absolute address (Longword address. Write 0 to bits A31 to A29, A1, and A0.)  
LINK relative address (Longword address. Negative numbers are expressed as two's complements. Bits A31 to A29 are used to extend the sign in bit A28. Write 0 to bits A1 and A0.)

Note: Even in 32-bit addressing mode, write the values in bits 28 to 3 of the specified 32-bit address to bits A28 to A3.

**(f) Description**

Draws a polygonal line from vertex 1 (DX<sub>1</sub>, DY<sub>1</sub>), through vertex 2 (DX<sub>2</sub>, DY<sub>2</sub>), ..., vertex n – 1 (DX<sub>n – 1</sub>, DY<sub>n – 1</sub>), to vertex n (DX<sub>n</sub>, DY<sub>n</sub>). When a value greater than 1 is set in W, a bold line can be drawn. When LINKE = 1, the vertex coordinates are read from the memory address specified by the LINK address. The LINK address can be specified through the LREL bit as an absolute address or a relative address with respect to the memory address at which the LINEC command code is located.

- Notes:
- 8-point drawing is used for a line width of 1. 4-point drawing is used for bold line drawing.
  - The final point of each line segment is drawn. When the starting and final coordinate points of a line segment match, a single dot is drawn for a line width of 1 and nothing is drawn for bold line drawing.
  - When AA = 1, note the following:
    - When the starting and final coordinate points of a line segment match, antialiasing is not performed.
    - When the NAA (new antialias mode) bit is 0, antialiasing is not performed for horizontal, vertical, and 45-degree diagonal line segments. When the NAA bit is 1, antialiasing is performed for horizontal, vertical, and 45-degree diagonal line segments.

**(g) Example****Figure 19.30 Example of LINEC Command Operation**

**(4) LINED****(a) Function**

Performs antialiasing for the exterior frame of a polygon. This command can only be executed for a 16- or 32-bit/pixel destination.

**(b) Command Format**

- LINKE = 0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OP CODE = 1011_0011								Reserved (all 0)								Draw mode															
Reserved (all 0)																n (2 ≤ n ≤ 65,535)															
Sign								DX1 (-32,768 ≤ DX1 ≤ 32,767)								Sign								DY1 (-32,768 ≤ DY1 ≤ 32,767)							
Sign								:								Sign								:							
Sign								:								Sign								:							
Sign								DXn (-32,768 ≤ DXn ≤ 32,767)								Sign								DYn (-32,768 ≤ DYn ≤ 32,767)							

Note: When n = 0 or 1, correct operation is not guaranteed.

- LINKE = 1 and LREL = 0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OP CODE = 1011_0011								Reserved (all 0)								Draw mode															
Reserved (all 0)																n (2 ≤ n ≤ 65,535)															
0 0 0			LINK address (longword address)																								0 0				

- Notes:
1. When n = 0 or 1, correct operation is not guaranteed.
  2. The longword address following the LINK address is handled as the next command code. Therefore, do not specify the longword address following the address where the LINK address is to be assigned as the link destination address specified by the LINK address.

- LINKE = 1 and LREL = 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OP CODE = 1011_0011								Reserved (all 0)								Draw mode															
Reserved (all 0)																n (2 ≤ n ≤ 65,535)															
Sign extended		Sign		LINK address (longword address)																								0 0			

- Notes:
1. When n = 0 or 1, correct operation is not guaranteed.
  2. The longword address following the LINK address is handled as the next command code. Therefore, do not specify the longword address following the address where the LINK address is to be assigned as the link destination address specified by adding the address where the command code is located to the LINK address.

**(c) Code**

B'10110011

**(d) Rendering Attributes**

		Reference Data				Drawing Destination									
Multi-Valued Source	Binary Source	Binary Work	Specified Color	Rendering	Work										
				√											
Draw Mode															
b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
MTRE	LOOP	CLIP	RCLIP	Fixed to 0	LINKE	LREL	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	AA (1)	CLKW

**(e) Command Parameters**

- n (n = 2 to 65,535): Number of vertices
- DX<sub>i</sub> (i = 1 to 65,535): Rendering coordinate (absolute coordinate). Negative numbers are expressed as two's complements.
- DY<sub>i</sub> (i = 1 to 65,535): Rendering coordinate (absolute coordinate). Negative numbers are expressed as two's complements.
- LINK address: LINK absolute address (Longword address. Write 0 to bits A31 to A29, A1, and A0).  
LINK relative address (Longword address. Negative numbers are expressed as two's complements. Bits A31 to A29 are used to extend the sign in bit A28. Write 0 to bits A1 and A0.)

Note: Even in 32-bit addressing mode, write the values in bits 28 to 3 of the specified 32-bit address to bits A28 to A3.

**(f) Description**

Performs antialiasing for the exterior frame of a polygon drawn using work reference.

The CLKW bit specifies whether the order to give the n vertices is clockwise or counterclockwise: CLKW = 1 selects clockwise and CLKW = 0 selects counterclockwise. When clockwise is specified, the left image with respect to the drawing direction is referenced by antialiasing. On the other hand, the right image is referenced when counterclockwise is selected. When LINKE = 1, the vertex coordinates are read from the memory address specified by the LINK address. The LINK address can be specified through the LREL bit as an absolute address or a relative address with respect to the memory address at which the LINED command code is located.

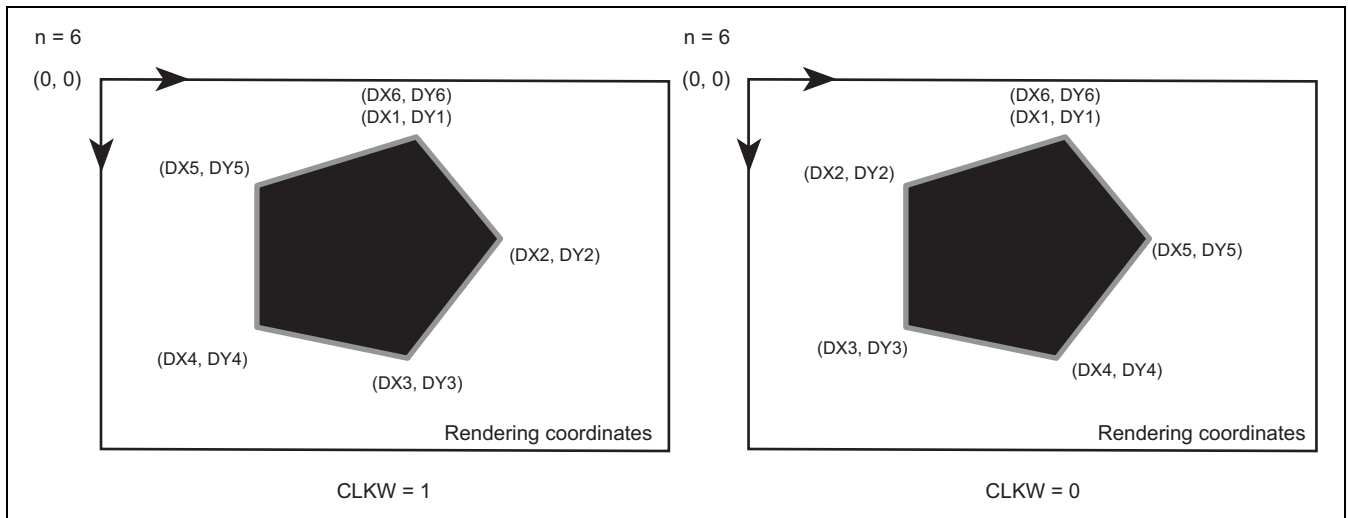
This command can only be executed for a 16- or 32-bit/pixel destination.

When a polygon used in work reference is drawn by the FTRAPC (RFTRAPC) command, perform drawing with both the EDG and EOS bits set to 1.

- Notes:
- 8-point drawing is used.
  - The final point of each line segment is not drawn. When antialiasing is performed for the exterior frame of a polygon drawn by a POLYGON4 type command, the paths may not match.
  - When the starting and final coordinate points of a line segment match, nothing is drawn.
  - Antialiasing is not performed for horizontal, vertical, and 45-degree diagonal line segments, which are pre-clipped inside the R-GP2D.
  - Clipping is performed on a pixel basis when either the referenced pixel or the pixel to be drawn is outside the clipping area, and antialiasing is not performed in such a case.



**(g) Example**



**Figure 19.31 Example of LINED Command Operation**

**(5) RLINEA****(a) Function**

Draws a polygonal line with any width in the destination area with a relative coordinate specification from the current pointer value while referencing a multi-valued (8-, 16-, or 32-bit/pixel) source.

**(b) Command Format**

- REL = 0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OP CODE = 1011_0110								Reserved (all 0)								Draw mode															
0 0 0			Base address (quad word address)														0 0 0														
0 0 0 0				TDX ( $8 \leq TDX \leq 4,088$ )								0 0 0 0 0 0 0 0				TDY ( $1 \leq TDY \leq 4,095$ )															
0 0 0 0				TXOFS ( $0 \leq TXOFS \leq TDX - 1$ )												n ( $1 \leq n \leq 65,535$ )															
Reserved (all 0)												0 0 0 0 0 0 0 0				W ( $0,2 \leq W \leq 63$ )															
Sign	DX2 ( $-128 \leq DX2 \leq 127$ )				Sign	DY2 ( $-128 \leq DY2 \leq 127$ )				Sign	DX1 ( $-128 \leq DX1 \leq 127$ )				Sign	DY1 ( $-128 \leq DY1 \leq 127$ )															
Sign	:				Sign	:				Sign	:				Sign	:															
Sign	:				Sign	:				Sign	:				Sign	:															
Sign	DXn ( $-128 \leq DXn \leq 127$ )				Sign	DYn ( $-128 \leq DYn \leq 127$ )				Sign	DXn-1 ( $-128 \leq DXn-1 \leq 127$ )				Sign	DYn-1 ( $-128 \leq DYn-1 \leq 127$ )															

- Notes:
- When  $W = 0$ , set TDY to 1.
  - When  $n = 0$ , correct operation is not guaranteed.
  - When  $n$  is an odd number, insert a dummy word of 0 at the end.

- REL = 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OP CODE = 1011_0110								Reserved (all 0)								Draw mode															
Sign extended		Sign		Base address (longword address)														0 0													
0 0 0 0				TDX ( $8 \leq TDX \leq 4,088$ )								0 0 0 0 0 0 0 0				TDY ( $1 \leq TDY \leq 4,095$ )															
0 0 0 0				TXOFS ( $0 \leq TXOFS \leq TDX - 1$ )												n ( $1 \leq n \leq 65,535$ )															
Reserved (all 0)												0 0 0 0 0 0 0 0				W ( $0,2 \leq W \leq 63$ )															
Sign	DX2 ( $-128 \leq DX2 \leq 127$ )				Sign	DY2 ( $-128 \leq DY2 \leq 127$ )				Sign	DX1 ( $-128 \leq DX1 \leq 127$ )				Sign	DY1 ( $-128 \leq DY1 \leq 127$ )															
Sign	:				Sign	:				Sign	:				Sign	:															
Sign	:				Sign	:				Sign	:				Sign	:															
Sign	DXn ( $-128 \leq DXn \leq 127$ )				Sign	DYn ( $-128 \leq DYn \leq 127$ )				Sign	DXn-1 ( $-128 \leq DXn-1 \leq 127$ )				Sign	DYn-1 ( $-128 \leq DYn-1 \leq 127$ )															

- Notes:
- Adding the address (longword: 32-bit units) where the command code is located to the base address (longword: 32-bit units) must result in a quad word address (64-bit units).
  - When  $W = 0$ , set TDY to 1.
  - When  $n = 0$ , correct operation is not guaranteed.
  - When  $n$  is an odd number, insert a dummy word of 0 at the end.

**(c) Code**

B'10110110

**(d) Rendering Attributes**

Reference Data		Drawing Destination				
Multi-Valued Source	Binary Source	Binary Work	Specified Color	Rendering	Work	
√				√		

Draw Mode															
b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
MTRE	LOOP	CLIP	RCLIP	STRANS	Fixed to 0	Fixed to 0	SS (0)	REL	STYLE (1)	Fixed to 0	NET	EOS	COOF	AA	Fixed to 0

- Notes: 1. Clear the SS bit to 0.  
2. Set the STYLE bit to 1.

**(e) Command Parameters**

- Base address: Source start absolute address (Quad word address. Write 0 to bits A31 to A29 and A2 to A0.)  
Source start relative address (Longword address. Negative numbers are expressed as two's complements. Bits A31 to A29 are used to extend the sign in bit A28. Write 0 to bits A1 and A0.)  
Note: Even in 32-bit addressing mode, write the values in bits 28 to 3 of the specified 32-bit address to bits A28 to A3.
- TDX, TDY: Source size. Write 0 to the unused bits.
- TXOFS: Source offset. Write 0 to the unused bits.
- n (n = 1 to 65,535): Number of vertices
- W: Line width. Set a 6-bit integer. Write 0 to the unused bits.  
When 0 is set in W, a polygonal line of line width 1 is drawn. Setting 1 in W is prohibited.
- DX<sub>i</sub> (i = 1 to 65,535): Rendering coordinate (relative coordinate). Negative numbers are expressed as two's complements.
- DY<sub>i</sub> (i = 1 to 65,535): Rendering coordinate (relative coordinate). Negative numbers are expressed as two's complements.

**(f) Description**

Draws a polygonal line comprising line segments  $(XC, YC) - (XC + DX1, YC + DY1)$ ,  $(XC + DX1, YC + DY1) - (XC + DX1 + DX2, YC + DY1 + DY2)$ , ...,  $(XC + \dots + DX_{n-1}, YC + \dots + DY_{n-1}) - (XC + \dots + DX_n, YC + \dots + DY_n)$  to the coordinates specified by the relative shift (DX, DY) from the current pointer values (XC, YC).

The final coordinate point is stored as the current pointer values (XC, YC). Set a multiple of 8 pixels as the TDX value. If TXOFS is set, the source at a location shifted by the offset amount is referenced. Make the TXOFS setting in pixel units.

Pattern repetition selected when the STYLE bit = 1 is only performed in the X direction of the source data. The source data is enlarged or reduced in proportion to the line width in the Y direction.

When a value greater than 0 is set in W, a bold line can be drawn.

- Notes: 1. 8-point drawing is used for a line width of 1. 4-point drawing is used for bold line drawing.  
2. The final point of each line segment is drawn. When the starting and final coordinate points of a line segment match, a single dot is drawn for a line width of 1 and nothing is drawn for bold line drawing.  
3. When AA = 1, note the following:
- For a dashed line, antialiasing is not performed for the gaps in the dashed line.
  - When the starting and final coordinate points of a line segment match, antialiasing is not performed.

- When the NAA (new antialias mode) bit is 0, antialiasing is not performed for horizontal, vertical, and 45-degree diagonal line segments. When the NAA bit is 1, antialiasing is performed for horizontal, vertical, and 45-degree diagonal line segments.
4. The final coordinate point before coordinate transformation is stored as the current pointer values (XC, YC).

**(6) RLINEB****(a) Function**

Draws a polygonal line with any width in the destination area with a relative coordinate specification from the current pointer value while referencing a binary (1-bit/pixel) source.

**(b) Command Format**

(i) GBM2 = 0

- REL = 0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OP CODE = 1011_0101								Reserved (all 0)								Draw mode															
Color1																Color0															
0	0	0	Base address (quad word address)																								0	0	0		
0	0	0	0	TDX ( $8 \leq TDX \leq 4,088$ )								0	0	0	0	0	0	0	0	TDY ( $1 \leq TDY \leq 4,095$ )											
0	0	0	0	TXOFS ( $0 \leq TXOFS \leq TDX - 1$ )												n ( $1 \leq n \leq 65,535$ )															
Reserved (all 0)																0	0	0	0	0	0	0	0	0	0	0	0	W ( $0,2 \leq W \leq 63$ )			
Sign	DX2 ( $-128 \leq DX2 \leq 127$ )				Sign	DY2 ( $-128 \leq DY2 \leq 127$ )				Sign	DX1 ( $-128 \leq DX1 \leq 127$ )				Sign	DY1 ( $-128 \leq DY1 \leq 127$ )															
Sign	:				Sign	:				Sign	:				Sign	:															
Sign	:				Sign	:				Sign	:				Sign	:															
Sign	DXn ( $-128 \leq DXn \leq 127$ )				Sign	DYn ( $-128 \leq DYn \leq 127$ )				Sign	DXn-1 ( $-128 \leq DXn-1 \leq 127$ )				Sign	DYn-1 ( $-128 \leq DYn-1 \leq 127$ )															

- Notes:
1. When W = 0, set TDY to 1.
  2. When n = 0, correct operation is not guaranteed.
  3. When n is an odd number, insert a dummy word of 0 at the end.

- REL = 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OP CODE = 1011_0101								Reserved (all 0)								Draw mode															
Color1																Color0															
Sign extended	Sign	Base address (longword address)																								0	0				
0	0	0	0	TDX ( $8 \leq TDX \leq 4,088$ )								0	0	0	0	0	0	0	0	TDY ( $1 \leq TDY \leq 4,095$ )											
0	0	0	0	TXOFS ( $0 \leq TXOFS \leq TDX - 1$ )												n ( $1 \leq n \leq 65,535$ )															
Reserved (all 0)																0	0	0	0	0	0	0	0	0	0	0	0	W ( $0,2 \leq W \leq 63$ )			
Sign	DX2 ( $-128 \leq DX2 \leq 127$ )				Sign	DY2 ( $-128 \leq DY2 \leq 127$ )				Sign	DX1 ( $-128 \leq DX1 \leq 127$ )				Sign	DY1 ( $-128 \leq DY1 \leq 127$ )															
Sign	:				Sign	:				Sign	:				Sign	:															
Sign	:				Sign	:				Sign	:				Sign	:															
Sign	DXn ( $-128 \leq DXn \leq 127$ )				Sign	DYn ( $-128 \leq DYn \leq 127$ )				Sign	DXn-1 ( $-128 \leq DXn-1 \leq 127$ )				Sign	DYn-1 ( $-128 \leq DYn-1 \leq 127$ )															

- Notes:
1. Adding the address (longword: 32-bit units) where the command code is located to the base address (longword: 32-bit units) must result in a quad word address (64-bit units).
  2. When W = 0, set TDY to 1.
  3. When n = 0, correct operation is not guaranteed.
  4. When n is an odd number, insert a dummy word of 0 at the end.

## (ii) GBM2 = 1

- REL = 0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
OP CODE = 1011_0101								Reserved (all 0)								Draw mode																			
Color0																																			
Color1																																			
0	0	0	Base address (quad word address)																								0	0	0						
0	0	0	0	TDX ( $8 \leq TDX \leq 4,088$ )								0	0	0	0	0	0	0	0	TDY ( $1 \leq TDY \leq 4,095$ )															
0	0	0	0	TXOFS ( $0 \leq TXOFS \leq TDX - 1$ )																n ( $1 \leq n \leq 65,535$ )															
Reserved (all 0)																0	0	0	0	0	0	0	0	0	0	0	0	W ( $0,2 \leq W \leq 63$ )							
Sign	DX2 ( $-128 \leq DX2 \leq 127$ )								Sign	DY2 ( $-128 \leq DY2 \leq 127$ )								Sign	DX1 ( $-128 \leq DX1 \leq 127$ )								Sign	DY1 ( $-128 \leq DY1 \leq 127$ )							
Sign	:								Sign	:								Sign	:								Sign	:							
Sign	:								Sign	:								Sign	:								Sign	:							
Sign	DXn ( $-128 \leq DXn \leq 127$ )								Sign	DYn ( $-128 \leq DYn \leq 127$ )								Sign	DXn-1 ( $-128 \leq DXn-1 \leq 127$ )								Sign	DYn-1 ( $-128 \leq DYn-1 \leq 127$ )							

- Notes:
- When W = 0, set TDY to 1.
  - When n = 0, correct operation is not guaranteed.
  - When n is an odd number, insert a dummy word of 0 at the end.

- REL = 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
OP CODE = 1011_0101								Reserved (all 0)								Draw mode																			
Color0																																			
Color1																																			
Sign extended	Sign	Base address (longword address)																								0	0								
0	0	0	0	TDX ( $8 \leq TDX \leq 4,088$ )								0	0	0	0	0	0	0	0	TDY ( $1 \leq TDY \leq 4,095$ )															
0	0	0	0	TXOFS ( $0 \leq TXOFS \leq TDX - 1$ )																n ( $1 \leq n \leq 65,535$ )															
Reserved (all 0)																0	0	0	0	0	0	0	0	0	0	0	0	W ( $0,2 \leq W \leq 63$ )							
Sign	DX2 ( $-128 \leq DX2 \leq 127$ )								Sign	DY2 ( $-128 \leq DY2 \leq 127$ )								Sign	DX1 ( $-128 \leq DX1 \leq 127$ )								Sign	DY1 ( $-128 \leq DY1 \leq 127$ )							
Sign	:								Sign	:								Sign	:								Sign	:							
Sign	:								Sign	:								Sign	:								Sign	:							
Sign	DXn ( $-128 \leq DXn \leq 127$ )								Sign	DYn ( $-128 \leq DYn \leq 127$ )								Sign	DXn-1 ( $-128 \leq DXn-1 \leq 127$ )								Sign	DYn-1 ( $-128 \leq DYn-1 \leq 127$ )							

- Notes:
- Adding the address (longword: 32-bit units) where the command code is located to the base address (longword: 32-bit units) must result in a quad word address (64-bit units).
  - When W = 0, set TDY to 1.
  - When n = 0, correct operation is not guaranteed.
  - When n is an odd number, insert a dummy word of 0 at the end.

## (c) Code

B'10110101

**(d) Rendering Attributes**

Reference Data										Drawing Destination					
Multi-Valued Source	Binary Source					Binary Work		Specified Color			Rendering	Work			
	√										√				
Draw Mode															
b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
MTRE	LOOP	CLIP	RCLIP	STRANS	Fixed to 0	Fixed to 0	SS (0)	REL	STYLE (1)	Fixed to 0	NET	EOS	COOF	AA	Fixed to 0

- Notes: 1. Clear the SS bit to 0.  
2. Set the STYLE bit to 1.

**(e) Command Parameters**

- Color0, Color1: 8-, 16-, or 32-bit/pixel color specification. For 16-bit/pixel drawing, the color specification should match the destination pixel format.  
For 8-bit/pixel drawing, the same value should be set in the upper and lower bytes.
- Base address: Source start absolute address (Quad word address. Write 0 to bits A31 to A29 and A2 to A0.)  
Source start relative address (Longword address. Negative numbers are expressed as two's complements. Bits A31 to A29 are used to extend the sign in bit A28. Write 0 to bits A1 and A0.)  
Note: Even in 32-bit addressing mode, write the values in bits 28 to 3 of the specified 32-bit address to bits A28 to A3.
- TDX, TDY: Source size. Write 0 to the unused bits.
- TXOFS: Source offset. Write 0 to the unused bits.
- n (n = 1 to 65,535): Number of vertices
- W: Line width. Set a 6-bit integer. Write 0 to the unused bits.  
When 0 is set in W, a polygonal line of line width 1 is drawn. Setting 1 in W is prohibited.
- DX<sub>i</sub> (i = 1 to 65,535): Rendering coordinate (relative coordinate). Negative numbers are expressed as two's complements.
- DY<sub>i</sub> (i = 1 to 65,535): Rendering coordinate (relative coordinate). Negative numbers are expressed as two's complements.

**(f) Description**

Draws a polygonal line comprising line segments  $(XC, YC) - (XC + DX1, YC + DY1)$ ,  $(XC + DX1, YC + DY1) - (XC + DX1 + DX2, YC + DY1 + DY2)$ , ...,  $(XC + \dots + DX_{n-1}, YC + \dots + DY_{n-1}) - (XC + \dots + DX_n, YC + \dots + DY_n)$  to the coordinates specified by the relative shift  $(DX, DY)$  from the current pointer values  $(XC, YC)$ .

The final coordinate point is stored as the current pointer values  $(XC, YC)$ .

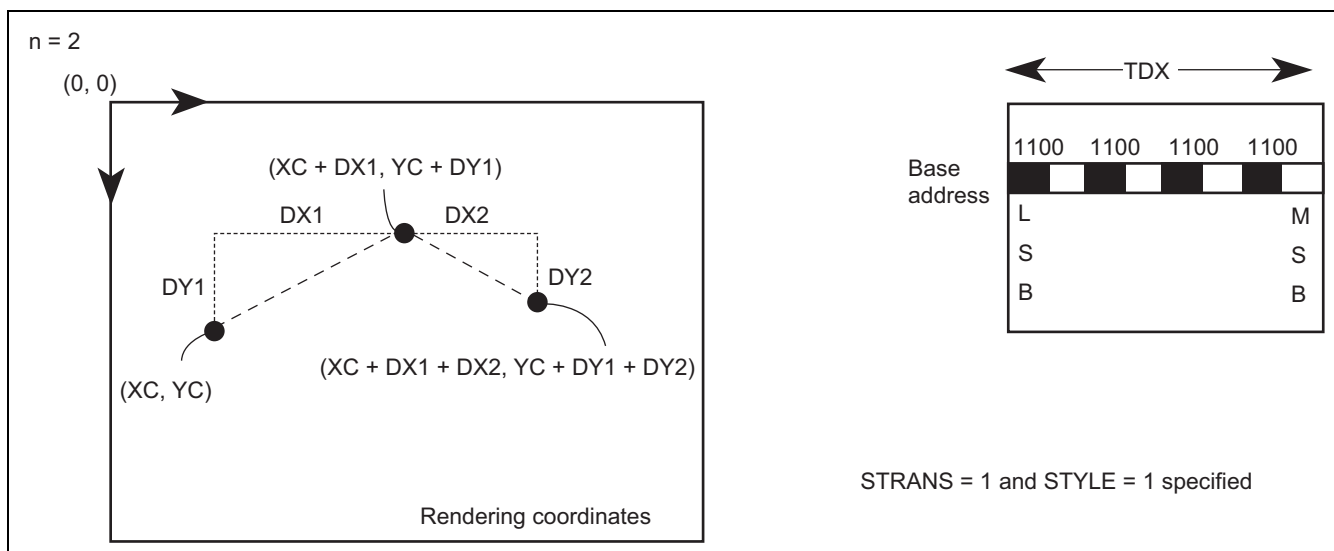
Set a multiple of 8 pixels as the TDX value. If TXOFS is set, the source at a location shifted by the offset amount is referenced. Make the TXOFS setting in pixel units.

Pattern repetition selected when the STYLE bit = 1 is only performed in the X direction of the source data. The source data is enlarged or reduced in proportion to the line width in the Y direction.

When a value greater than 1 is set in W, a bold line can be drawn.

- Notes:
1. 8-point drawing is used for a line width of 1. 4-point drawing is used for bold line drawing.
  2. The final point of each line segment is drawn. When the starting and final coordinate points of a line segment match, a single dot is drawn for a line width of 1 and nothing is drawn for bold line drawing.
  3. When AA = 1, note the following:
    - For a dashed line, antialiasing is not performed for the gaps in the dashed line.
    - When the starting and final coordinate points of a line segment match, antialiasing is not performed.
    - When the NAA (new antialias mode) bit is 0, antialiasing is not performed for horizontal, vertical, and 45-degree diagonal line segments. When the NAA bit is 1, antialiasing is performed for horizontal, vertical, and 45-degree diagonal line segments.
  4. The final coordinate point before coordinate transformation is stored as the current pointer values  $(XC, YC)$ .

**(g) Example**



**Figure 19.32 Example of RLINEB Command Operation**



**(7) RLINEC****(a) Function**

Draws a polygonal line with any width in the destination area with a monochrome specification and with a relative coordinate specification from the current pointer value.

**(b) Command Format**

(i) GBM2 = 0

- LINKE = 0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
OP CODE = 1011_0100								Reserved (all 0)								Draw mode																			
Color																n (1 ≤ n ≤ 65,535)																			
Reserved (all 0)																0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	W (0,2 ≤ W ≤ 63)			
Sign	DX2 (-128 ≤ DX2 ≤ 127)							Sign	DY2 (-128 ≤ DY2 ≤ 127)							Sign	DX1 (-128 ≤ DX1 ≤ 127)							Sign	DY1 (-128 ≤ DY1 ≤ 127)										
Sign	:							Sign	:							Sign	:							Sign	:										
Sign	:							Sign	:							Sign	:							Sign	:										
Sign	DXn (-128 ≤ DXn ≤ 127)							Sign	DYn (-128 ≤ DYn ≤ 127)							Sign	DXn-1 (-128 ≤ DXn-1 ≤ 127)							Sign	DYn-1 (-128 ≤ DYn-1 ≤ 127)										

Notes: 1. When n = 0, correct operation is not guaranteed.  
2. When n is an odd number, insert a dummy word of 0 at the end.

- LINKE = 1 and LREL = 0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
OP CODE = 1011_0100								Reserved (all 0)								Draw mode																			
Color																n (1 ≤ n ≤ 65,535)																			
Reserved (all 0)																0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	W (0,2 ≤ W ≤ 63)			
0	0	0	LINK address (longword address)													0	0																		

Notes: 1. When n = 0, correct operation is not guaranteed.  
2. When n is an odd number, insert a dummy word of 0 at the end.  
3. The longword address following the LINK address is handled as the next command code. Therefore, do not specify the longword address following the address where the LINK address is to be assigned as the link destination address specified by the LINK address.

- LINKE = 1 and LREL = 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0					
OP CODE = 1011_0100								Reserved (all 0)								Draw mode																				
Color																n (1 ≤ n ≤ 65,535)																				
Reserved (all 0)																0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	W (0,2 ≤ W ≤ 63)			
Sign extended		Sign		LINK address (longword address)														0		0																

- Notes:
1. When n = 0, correct operation is not guaranteed.
  2. When n is an odd number, insert a dummy word of 0 at the end.
  3. The longword address following the LINK address is handled as the next command code. Therefore, do not specify the longword address following the address where the LINK address is to be assigned as the link destination address specified by adding the address where the command code is located to the LINK address.

## (ii) GBM2 = 1

- LINKE = 0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0					
OP CODE = 1011_0100								Reserved (all 0)								Draw mode																				
Color																n (1 ≤ n ≤ 65,535)																				
Reserved (all 0)																0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	W (0,2 ≤ W ≤ 63)			
Sign	DX2 (-128 ≤ DX2 ≤ 127)				Sign	DY2 (-128 ≤ DY2 ≤ 127)				Sign	DX1 (-128 ≤ DX1 ≤ 127)				Sign	DY1 (-128 ≤ DY1 ≤ 127)																				
Sign	:				Sign	:				Sign	:				Sign	:																				
Sign	:				Sign	:				Sign	:				Sign	:																				
Sign	DXn (-128 ≤ DXn ≤ 127)				Sign	DYn (-128 ≤ DYn ≤ 127)				Sign	DXn-1 (-128 ≤ DXn-1 ≤ 127)				Sign	DYn-1 (-128 ≤ DYn-1 ≤ 127)																				

- Notes:
1. When n = 0, correct operation is not guaranteed.
  2. When n is an odd number, insert a dummy word of 0 at the end.

- LINKE = 1 and LREL = 0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0					
OP CODE = 1011_0100								Reserved (all 0)								Draw mode																				
Color																n (1 ≤ n ≤ 65,535)																				
Reserved (all 0)																0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	W (0,2 ≤ W ≤ 63)			
0		0		0		LINK address (longword address)														0		0														

- Notes:
1. When n = 0, correct operation is not guaranteed.
  2. When n is an odd number, insert a dummy word of 0 at the end.
  3. The longword address following the LINK address is handled as the next command code. Therefore, do not specify the longword address following the address where the LINK address is to be assigned as the link destination address specified by the LINK address.

- LINKE = 1 and LREL = 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																		
OP CODE = 1011_0100								Reserved (all 0)								Draw mode																																	
Color																																																	
Reserved (all 0)																n (1 ≤ n ≤ 65,535)																																	
Reserved (all 0)																0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
Sign extended																Sign																LINK address (longword address)																0	0

- Notes:
1. When n = 0, correct operation is not guaranteed.
  2. When n is an odd number, insert a dummy word of 0 at the end.
  3. The longword address following the LINK address is handled as the next command code. Therefore, do not specify the longword address following the address where the LINK address is to be assigned as the link destination address specified by adding the address where the command code is located to the LINK address.

### (c) Code

B'10110100

### (d) Rendering Attributes

Reference Data								Drawing Destination							
Multi-Valued Source	Binary Source	Binary Work	Specified Color	Rendering	Work										
			√	√											
Draw Mode															
b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
MTRE	LOOP	CLIP	RCLIP	Fixed to 0	LINKE	LREL	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	NET	EOS	COOF	AA	Fixed to 0

### (e) Command Parameters

- Color: 8-, 16-, or 32-bit/pixel color specification. For 16-bit/pixel drawing, the color specification should match the destination pixel format.  
For 8-bit/pixel drawing, the same value should be set in the upper and lower bytes.
- n (n = 1 to 65,535): Number of vertices
- W: Line width. Set a 6-bit integer. Write 0 to the unused bits.  
When 0 is set in W, a polygonal line of line width 1 is drawn. Setting 1 in W is prohibited.
- DX<sub>i</sub> (i = 1 to 65,535): Rendering coordinate (relative coordinate). Negative numbers are expressed as two's complements.
- DY<sub>i</sub> (i = 1 to 65,535): Rendering coordinate (relative coordinate). Negative numbers are expressed as two's complements.
- LINK address: LINK absolute address (Longword address. Write 0 to bits A31 to A29, A1, and A0.)  
LINK relative address (Longword address. Negative numbers are expressed as two's complements. Bits A31 to A29 are used to extend the sign in bit A28. Write 0 to bits A1 and A0.)

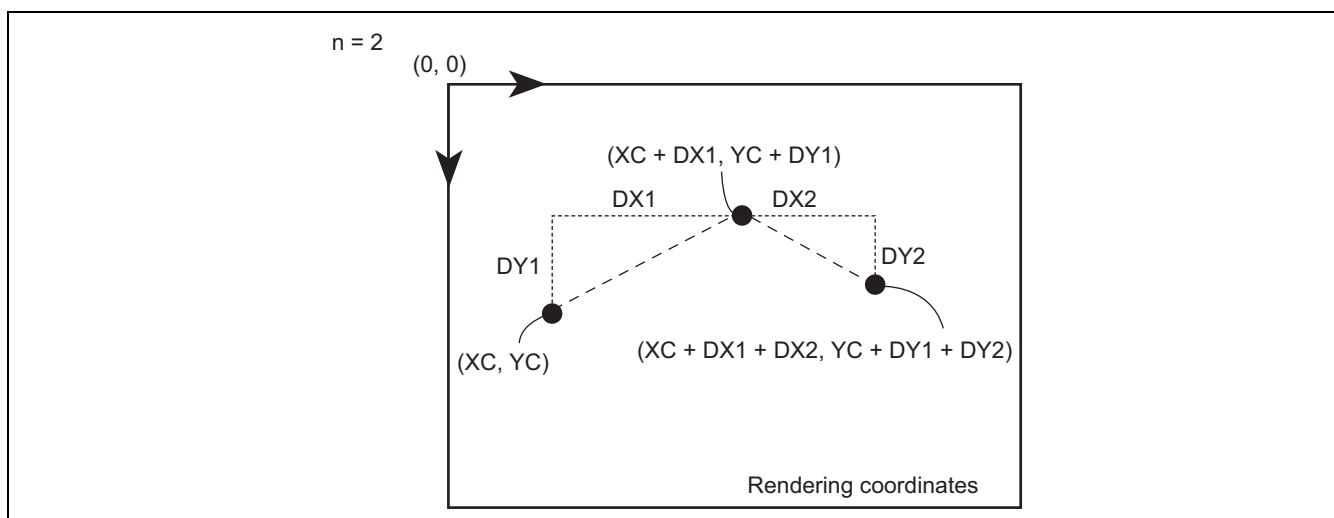
Note: Even in 32-bit addressing mode, write the values in bits 28 to 3 of the specified 32-bit address to bits A28 to A3.

**(f) Description**

Draws a polygonal line comprising line segments  $(XC, YC) - (XC + DX1, YC + DY1)$ ,  $(XC + DX1, YC + DY1) - (XC + DX1 + DX2, YC + DY1 + DY2)$ , ...,  $(XC + \dots + DX_{n-1}, YC + \dots + DY_{n-1}) - (XC + \dots + DX_n, YC + \dots + DY_n)$  to the coordinates specified by the relative shift  $(DX, DY)$  from the current pointer values  $(XC, YC)$ . When a value greater than 1 is set in  $W$ , a bold line can be drawn. When  $LINKE = 1$ , the vertex coordinates are read from the memory address specified by the LINK address. The LINK address can be specified through the LREL bit as an absolute address or a relative address with respect to the memory address at which the RLINEC command code is located.

The final coordinate point is stored as the current pointer values  $(XC, YC)$ .

- Notes:
1. 8-point drawing is used for a line width of 1. 4-point drawing is used for bold line drawing.
  2. The final point of each line segment is drawn. When the starting and final coordinate points of a line segment match, a single dot is drawn for a line width of 1 and nothing is drawn for bold line drawing.
  3. When  $AA = 1$ , note the following:
    - When the starting and final coordinate points of a line segment match, antialiasing is not performed.
    - When the NAA (new antialias mode) bit is 0, antialiasing is not performed for horizontal, vertical, and 45-degree diagonal line segments. When the NAA bit is 1, antialiasing is performed for horizontal, vertical, and 45-degree diagonal line segments.
  4. The final coordinate point before coordinate transformation is stored as the current pointer values  $(XC, YC)$ .

**(g) Example**

**Figure 19.33 Example of RLINEC Command Operation**

**(8) RLINED****(a) Function**

Performs antialiasing for the exterior frame of a polygon with a relative coordinate specification from the current pointer value. This command can only be executed for a 16- or 32-bit/pixel destination.

**(b) Command Format**

- LINKE = 0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OP CODE = 1011_0111								Reserved (all 0)								Draw mode															
Reserved (all 0)																n (1 ≤ n ≤ 65,535)															
Sign DX2 (-128 ≤ DX2 ≤ 127)				Sign DY2 (-128 ≤ DY2 ≤ 127)				Sign DX1 (-128 ≤ DX1 ≤ 127)				Sign DY1 (-128 ≤ DY1 ≤ 127)																			
Sign :				Sign :				Sign :				Sign :																			
Sign :				Sign :				Sign :				Sign :																			
Sign DXn (-128 ≤ DXn ≤ 127)				Sign DYn (-128 ≤ DYn ≤ 127)				Sign DXn-1 (-128 ≤ DXn-1 ≤ 127)				Sign DYn-1 (-128 ≤ DYn-1 ≤ 127)																			

- Notes:
1. When n = 0, correct operation is not guaranteed.
  2. When n is an odd number, insert a dummy word of 0 at the end.

- LINKE = 1 and LREL = 0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OP CODE = 1011_0111								Reserved (all 0)								Draw mode															
Reserved (all 0)																n (1 ≤ n ≤ 65,535)															
0 0 0			LINK address (longword address)																								0 0				

- Notes:
1. When n = 0, correct operation is not guaranteed.
  2. When n is an odd number, insert a dummy word of 0 at the end.
  3. The longword address following the LINK address is handled as the next command code. Therefore, do not specify the longword address following the address where the LINK address is to be assigned as the link destination address specified by the LINK address.

- LINKE = 1 and LREL = 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OP CODE = 1011_0111								Reserved (all 0)								Draw mode															
Reserved (all 0)																n (1 ≤ n ≤ 65,535)															
Sign extended		Sign		LINK address (longword address)																								0 0			

- Notes:
1. When n = 0, correct operation is not guaranteed.
  2. When n is an odd number, insert a dummy word of 0 at the end.
  3. The longword address following the LINK address is handled as the next command code. Therefore, do not specify the longword address following the address where the LINK address is to be assigned as the link destination address specified by adding the address where the command code is located to the LINK address.

**(c) Code**

B'10110111

**(d) Rendering Attributes**

Reference Data										Drawing Destination					
Multi-Valued Source	Binary Source			Binary Work		Specified Color			Rendering	Work					
										√					
Draw Mode															
b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
MTRE	LOOP	CLIP	RCLIP	Fixed to 0	LINKE	LREL	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	AA (1)	CLKW

Note: Set the AA bit to 1.

**(e) Command Parameters**

- n (n = 1 to 65,535): Number of vertices
- DX<sub>i</sub> (i = 1 to 65,535): Rendering coordinate (relative coordinate). Negative numbers are expressed as two's complements.
- DY<sub>i</sub> (i = 1 to 65,535): Rendering coordinate (relative coordinate). Negative numbers are expressed as two's complements.
- LINK address: LINK absolute address (Longword address. Write 0 to bits A31 to A29, A1, and A0.)  
LINK relative address (Longword address. Negative numbers are expressed as two's complements. Bits A31 to A29 are used to extend the sign in bit A28. Write 0 to bits A1 and A0.)

Note: Even in 32-bit addressing mode, write the values in bits 28 to 3 of the specified 32-bit address to bits A28 to A3.

**(f) Description**

Performs antialiasing for the exterior frame of a polygon drawn using work reference, with a relative coordinate specification from the current pointer value.

The CLKW bit specifies whether the order to give the n vertices is clockwise or counterclockwise: CLKW = 1 selects clockwise and CLKW = 0 selects counterclockwise. When clockwise is specified, the left image with respect to the drawing direction is referenced by antialiasing. On the other hand, the right image is referenced when counterclockwise is selected. When LINKE = 1, the vertex coordinates are read from the memory address specified by the LINK address. The LINK address can be specified through the LREL bit as an absolute address or a relative address with respect to the memory address at which the RLINED command code is located.

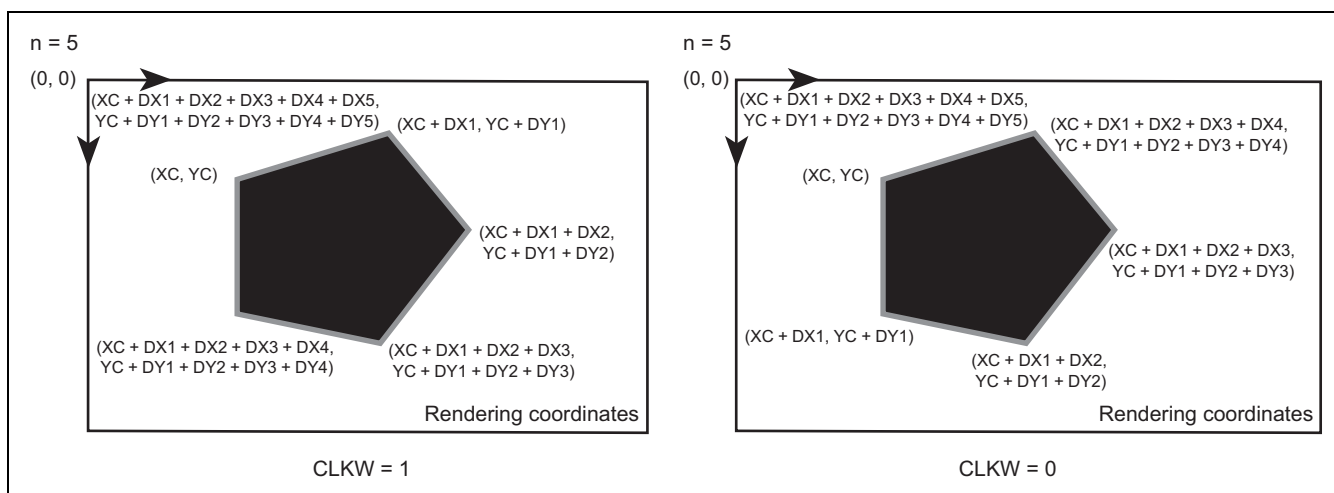
This command can only be executed for a 16- or 32-bit/pixel destination.

When a polygon used in work reference is drawn by the FTRAPC (RFTRAPC) command, perform drawing with both the EDG and EOS bits set to 1.

The final coordinate point is stored as the current pointer values (XC, YC).

Notes: 1. 8-point drawing is used.

2. The final point of each line segment is not drawn. When antialiasing is performed for the exterior frame of a polygon drawn by a POLYGON4 type command, the paths may not match.
3. When the starting and final coordinate points of a line segment match, nothing is drawn.
4. Antialiasing is not performed for horizontal, vertical, and 45-degree diagonal line segments, which are pre-clipped inside the R-GP2D.
5. Clipping is performed on a pixel basis when either the referenced pixel or the pixel to be drawn is outside the clipping area, and antialiasing is not performed in such a case.
6. The final coordinate point before coordinate transformation is stored as the current pointer values (XC, YC).

**(g) Example**

**Figure 19.34 Example of RLINED Command Operation**

### 19.4.3 Work Screen Drawing Commands

#### (1) FTRAPC

##### (a) Function

Draws a polygon at work coordinates.

##### (b) Command Format

- LINKE = 0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OP CODE = 1101_0000								Reserved (all 0)								Draw mode															
Reserved (all 0)								Reserved (all 0)								n ( $2 \leq n \leq 65,535$ )															
Sign				Xmin ( $-32,768 \leq Xmin \leq 32,767$ )								Sign				Ymin ( $-32,768 \leq Ymin \leq 32,767$ )															
Sign				Xmax ( $-32,768 \leq Xmax \leq 32,767$ )								Sign				Ymax ( $-32,768 \leq Ymax \leq 32,767$ )															
Sign				DX1 ( $-32,768 \leq DX1 \leq 32,767$ )								Sign				DY1 ( $-32,768 \leq DY1 \leq 32,767$ )															
Sign				:								Sign				:															
Sign				:								Sign				:															
Sign				DXn ( $-32,768 \leq DXn \leq 32,767$ )								Sign				DYn ( $-32,768 \leq DYn \leq 32,767$ )															

Note: When  $n = 0$  or  $1$ , correct operation is not guaranteed.

- LINKE = 1 and LREL = 0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OP CODE = 1101_0000								Reserved (all 0)								Draw mode															
Reserved (all 0)								Reserved (all 0)								n ( $2 \leq n \leq 65,535$ )															
Sign				Xmin ( $-32,768 \leq Xmin \leq 32,767$ )								Sign				Ymin ( $-32,768 \leq Ymin \leq 32,767$ )															
Sign				Xmax ( $-32,768 \leq Xmax \leq 32,767$ )								Sign				Ymax ( $-32,768 \leq Ymax \leq 32,767$ )															
0	0	0	LINK address (longword address)													0	0														

Notes: 1. When  $n = 0$  or  $1$ , correct operation is not guaranteed.

2. The longword address following the LINK address is handled as the next command code. Therefore, do not specify the longword address following the address where the LINK address is to be assigned as the link destination address specified by the LINK address.



- LINKE = 1 and LREL = 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OP CODE = 1101_0000								Reserved (all 0)								Draw mode															
Reserved (all 0)																n (2 ≤ n ≤ 65,535)															
Sign								Xmin (-32,768 ≤ Xmin ≤ 32,767)								Sign								Ymin (-32,768 ≤ Ymin ≤ 32,767)							
Sign								Xmax (-32,768 ≤ Xmax ≤ 32,767)								Sign								Ymax (-32,768 ≤ Ymax ≤ 32,767)							
Sign extended		Sign		LINK address (longword address)														0		0											

- Notes:
1. When n = 0 or 1, correct operation is not guaranteed.
  2. The longword address following the LINK address is handled as the next command code. Therefore, do not specify the longword address following the address where the LINK address is to be assigned as the link destination address specified by adding the address where the command code is located to the LINK address.

### (c) Code

B'11010000

### (d) Rendering Attributes

Reference Data				Drawing Destination			
Multi-Valued Source	Binary Source	Binary Work	Specified Color	Rendering	Work		
							√

Draw Mode															
b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
MTRE	LOOP	CLIP	RCLIP	Fixed to 0	LINKE	LREL	Fixed to 0	Fixed to 0	Fixed to 0	BLKE (1)	EDG	EOS	Fixed to 0	Fixed to 0	Fixed to 0

Note: Set the BLKE bit to 1.

### (e) Command Parameters

- n (n = 2 to 65,535): Number of vertices
- Xmin: Xmin value in the circumscribed quadrangle of the polygon. Work coordinate (absolute coordinate). Negative numbers are expressed as two's complements.
- Ymin: Ymin value in the circumscribed quadrangle of the polygon. Work coordinate (absolute coordinate). Negative numbers are expressed as two's complements.
- Xmax: Xmax value in the circumscribed quadrangle of the polygon. Work coordinate (absolute coordinate). Negative numbers are expressed as two's complements.
- Ymax: Ymax value in the circumscribed quadrangle of the polygon. Work coordinate (absolute coordinate). Negative numbers are expressed as two's complements.
- DXi (i = 1 to 65,535): Work coordinate (absolute coordinate). Negative number expressed as two's complement.
- DYi (i = 1 to 65,535): Work coordinate (absolute coordinate). Negative number expressed as two's complement.
- LINK address: LINK absolute address (Longword address. Write 0 to bits A31 to A29, A1, and A0.)  
LINK relative address (Longword address. Negative numbers are expressed as two's complements. Bits A31 to A29 are used to extend the sign in bit A28. Write 0 to bits A1 and A0.)

Note: Even in 32-bit addressing mode, write the values in bits 28 to 3 of the specified 32-bit address to bits A28 to A3.

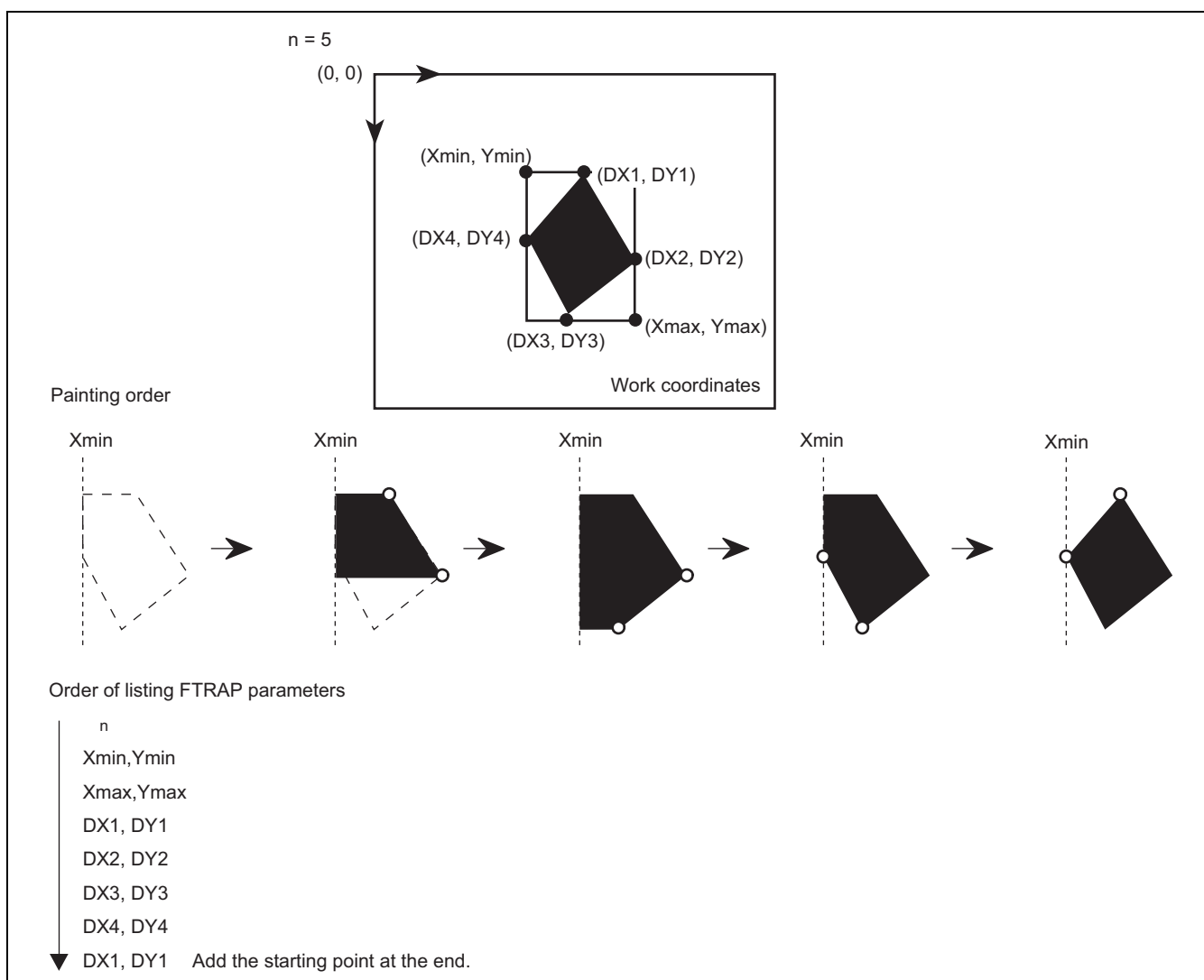
**(f) Description**

Draws a polygon with  $n - 1$  vertices at work coordinates. Paints  $n - 1$  trapezoids at work coordinates using binary EOR, with  $X = X_{min}$  as the left-hand side, and line segments  $(DX1, DY1) - (DX2, DY2), (DX2, DY2) - (DX3, DY3), \dots, (DX_{n-1}, DY_{n-1}) - (DX_n, DY_n)$  as the right-hand sides, and with the top and bottom bases parallel to the X-axis. Bottom base drawing is not performed. Set  $(DX_n, DY_n) = (DX_1, DY_1)$  to give a closed figure. If the rendering attribute EDG bit is set to 1, an edge line is drawn after the paint operation. The line drawing data is selected with the EOS bit.

The FTRAPC command performs coordinate transformation by internally obtaining the four vertices from the coordinates for the circumscribed quadrangle of the input polygon and then transforming the coordinates for these four vertices. The transformed four vertices are then internally converted into a circumscribed rectangle, the left edge obtained, and the polygon drawn.

Note: When enabling edge drawing ( $EDG = 1$ ), Z pre-clipping is not performed on the edge line.

**(g) Example**



**Figure 19.35 Example of FTRAPC Command Operation**

**(2) RFTRAPC****(a) Function**

Draws a polygon at work coordinates with a relative coordinate specification from the current pointer value.

**(b) Command Format**

- LINKE = 0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																																
OP CODE = 1101_0100								Reserved (all 0)								Draw mode																																															
Reserved (all 0)																n (1 ≤ n ≤ 65,535)																																															
Sign								Xmin (-32,768 ≤ Xmin ≤ 32,767)								Sign								Ymin (-32,768 ≤ Ymin ≤ 32,767)																																							
Sign								Xmax (-32,768 ≤ Xmax ≤ 32,767)								Sign								Ymax (-32,768 ≤ Ymax ≤ 32,767)																																							
Sign				DX2 (-128 ≤ DX2 ≤ 127)				Sign				DY2 (-128 ≤ DY2 ≤ 127)				Sign				DX1 (-128 ≤ DX1 ≤ 127)				Sign				DY1 (-128 ≤ DY1 ≤ 127)																																			
Sign				:				Sign				:				Sign				:				Sign				:																																			
Sign				:				Sign				:				Sign				:				Sign				:																																			
Sign								DXn (-128 ≤ DXn ≤ 127)								Sign								DYn (-128 ≤ DYn ≤ 127)								Sign								DXn-1 (-128 ≤ DXn-1 ≤ 127)								Sign								DYn-1 (-128 ≤ DYn-1 ≤ 127)							

- Notes:
1. When n = 0, correct operation is not guaranteed.
  2. When n is an odd number, insert a dummy word of 0 at the end.

- LINKE = 1 and LREL = 0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0							
OP CODE = 1101_0100								Reserved (all 0)								Draw mode																						
Reserved (all 0)																n (1 ≤ n ≤ 65,535)																						
Sign								Xmin (-32,768 ≤ Xmin ≤ 32,767)								Sign								Ymin (-32,768 ≤ Ymin ≤ 32,767)														
Sign								Xmax (-32,768 ≤ Xmax ≤ 32,767)								Sign								Ymax (-32,768 ≤ Ymax ≤ 32,767)														
0			0			0			LINK address (longword address)																								0			0		

- Notes:
1. When n = 0, correct operation is not guaranteed.
  2. When n is an odd number, insert a dummy word of 0 at the end.
  3. The longword address following the LINK address is handled as the next command code. Therefore, do not specify the longword address following the address where the LINK address is to be assigned as the link destination address specified by the LINK address.

- LINKE = 1 and LREL = 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OP CODE = 1101_0100								Reserved (all 0)								Draw mode															
Reserved (all 0)																n (1 ≤ n ≤ 65,535)															
Sign								Xmin (-32,768 ≤ Xmin ≤ 32,767)								Sign				Ymin (-32,768 ≤ Ymin ≤ 32,767)											
Sign								Xmax (-32,768 ≤ Xmax ≤ 32,767)								Sign				Ymax (-32,768 ≤ Ymax ≤ 32,767)											
Sign extended		Sign		LINK address (longword address)																								0		0	

- Notes:
1. When n = 0, correct operation is not guaranteed.
  2. When n is an odd number, insert a dummy word of 0 at the end.
  3. The longword address following the LINK address is handled as the next command code. Therefore, do not specify the longword address following the address where the LINK address is to be assigned as the link destination address specified by the address where the command code is located plus the LINK address.

(c) Code

B'11010100

(d) Rendering Attributes

Multi-Valued Source	Reference Data				Drawing Destination			
	Binary Source	Binary Work	Specified Color	Rendering	Work			
								√

Draw Mode															
b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
MTRE	LOOP	CLIP	RCLIP	Fixed to 0	LINKE	LREL	Fixed to 0	Fixed to 0	Fixed to 0	BLKE (1)	EDG	EOS	Fixed to 0	Fixed to 0	Fixed to 0

Note: Set the BLKE bit to 1.

(e) Command Parameters

- n (n = 1 to 65,535): Number of vertices
- Xmin: Xmin value in the circumscribed quadrangle of the polygon. Work coordinate (absolute coordinate). Negative numbers are expressed as two's complements.
- Ymin: Ymin value in the circumscribed quadrangle of the polygon. Work coordinate (absolute coordinate). Negative numbers are expressed as two's complements.
- Xmax: Xmax value in the circumscribed quadrangle of the polygon. Work coordinate (absolute coordinate). Negative numbers are expressed as two's complements.
- Ymax: Ymax value in the circumscribed quadrangle of the polygon. Work coordinate (absolute coordinate). Negative numbers are expressed as two's complements.
- DXi (i = 1 to 65,535): Work coordinate (relative coordinate). Negative numbers are expressed as two's complements.
- DYi (i = 1 to 65,535): Work coordinate (relative coordinate). Negative numbers are expressed as two's complements.
- LINK address: LINK absolute address (Longword address. Write 0 to bits A31 to A29, A1, and A0.)  
LINK relative address (Longword address. Negative numbers are expressed as two's complements. Bits A31 to A29 are used to extend the sign in bit A28. Write 0 to bits A1 and A0.)

Note: Even in 32-bit addressing mode, write the values in bits 28 to 3 of the specified 32-bit address to bits A28 to A3.

**(f) Description**

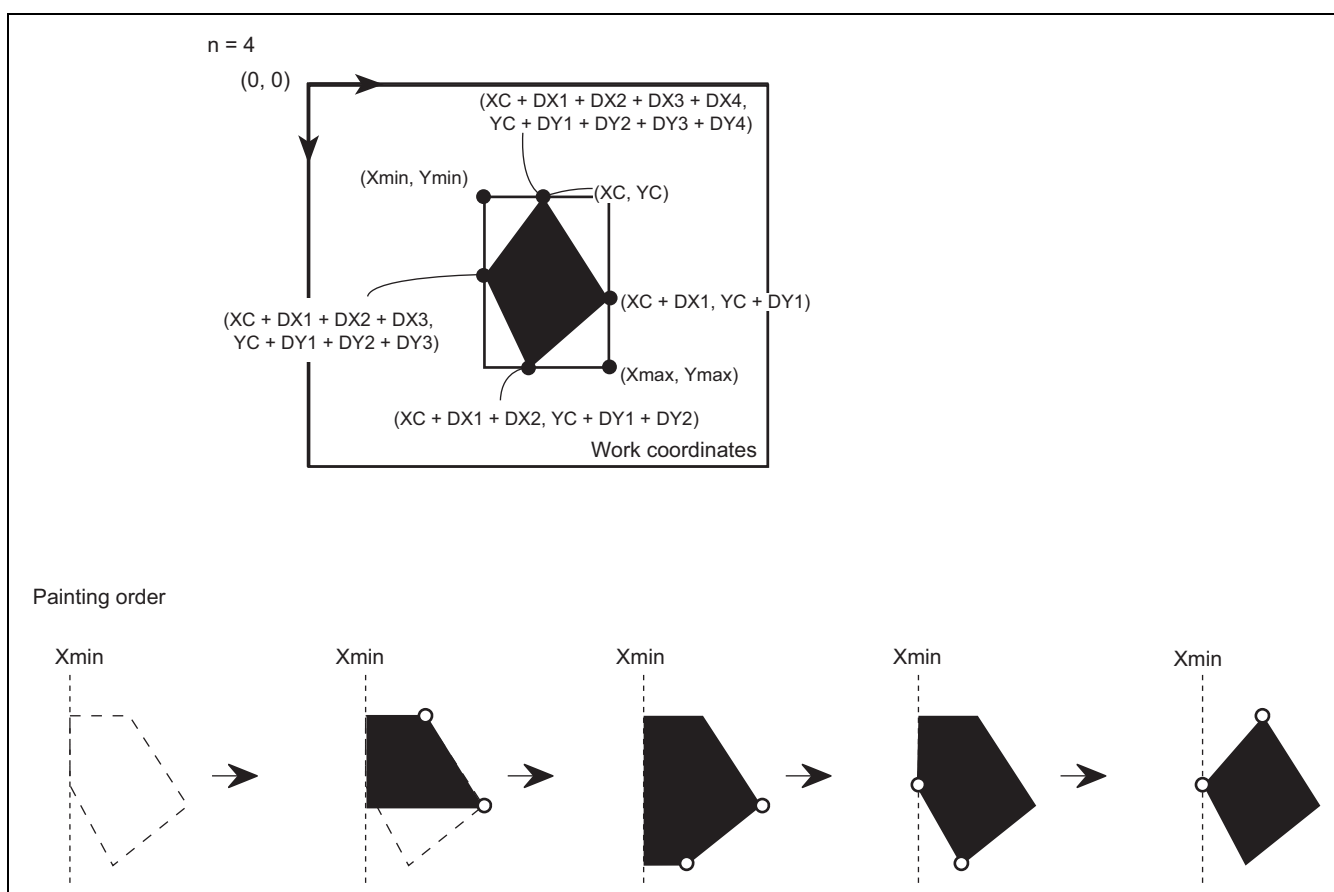
Paints  $n$  trapezoids at work coordinates using binary EOR, with  $X = X_{min}$  as the left-hand side, and line segments specified by the relative shift  $(DX, DY)$  from the current pointer values  $(XC, YC)$   $((XC, YC) - (XC + DX1, YC + DY1), (XC + DX1, YC + DY1) - (XC + DX1 + DX2, YC + DY1 + DY2), \dots, (XC + \dots + DX_{n-1}, YC + \dots + DY_{n-1}) - (XC + \dots + DX_n - 1 + DX_n, YC + \dots + DY_n - 1 + DY_n))$  as the right-hand sides, and with the top and bottom bases parallel to the X-axis. Bottom base drawing is not performed.

The final coordinate point is stored as the current pointer values  $(XC, YC)$ . Set  $(DX1 + DX2 + \dots + DX_n = 0, DY1 + DY2 + \dots + DY_n = 0)$  to give a closed figure. If the rendering attribute EDG bit is set to 1, an edge line is drawn after the paint operation. The line drawing data is selected with the EOS bit.

The RFTRAPC command performs coordinate transformation by internally obtaining the four vertices from the coordinates for the circumscribed quadrangle of the input polygon and then transforming the coordinates for these four vertices. The transformed four vertices are then internally converted into a circumscribed rectangle, the left edge obtained, and the polygon drawn.

- Notes: 1. The final coordinate point before coordinate transformation is stored as the current pointer values  $(XC, YC)$ .  
 2. When enabling edge drawing  $(EDG = 1)$ , Z pre-clipping is not performed on the edge line.

**(g) Example**



**Figure 19.36 Example of RFTRAPC Command Operation**

**(3) CLRWC**

**(a) Function**

Clears the specified work area to 0.

**(b) Command Format**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OP CODE = 1110_0000								Reserved (all 0)								Draw mode															
Sign								Xmin (-32,768 ≤ Xmin ≤ 32,767)								Sign								Ymin (-32,768 ≤ Ymin ≤ 32,767)							
Sign								Xmax (-32,768 ≤ Xmax ≤ 32,767)								Sign								Ymax (-32,768 ≤ Ymax ≤ 32,767)							

**(c) Code**

B'11100000

**(d) Rendering Attributes**

Reference Data				Drawing Destination		
Multi-Valued Source	Binary Source	Binary Work	Specified Color	Rendering	Work	
						√

Draw Mode															
b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
MTRE	Fixed to 0	CLIP	RCLIP	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	BLKE (1)	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0

Note: Set the BLKE bit to 1.

**(e) Command Parameters**

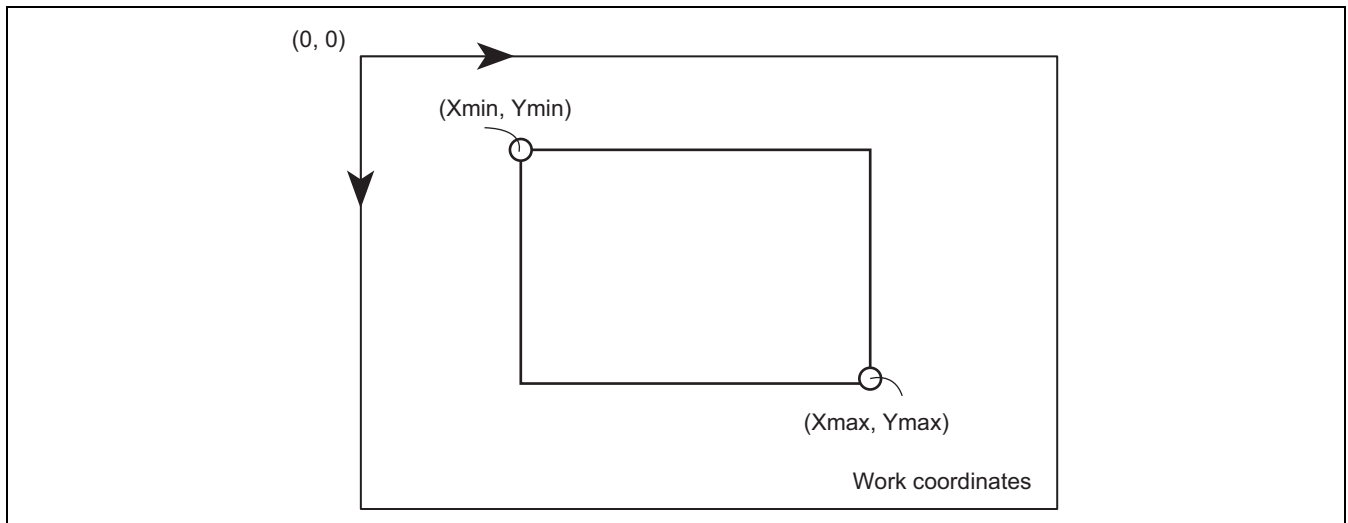
Xmin, Xmax: Left and right X coordinate values. Work coordinates (absolute coordinates). Negative numbers are expressed as two's complements.

Ymin, Ymax: Upper and lower Y coordinate values. Work coordinates (absolute coordinates). Negative numbers are expressed as two's complements.

**(f) Description**

Zero-clears the area specified by upper-left coordinates (Xmin, Ymin) and lower-right coordinates (Xmax, Ymax) at work coordinates.

The CLRWC command performs coordinate transformation by internally obtaining the four vertices from the left and right X coordinate values and upper and lower Y coordinate values, and then transforming the coordinates for these four vertices. The transformed four vertices are then internally converted into a circumscribed rectangle and the polygon drawn.

**(g) Example****Figure 19.37 Example of CLRWC Command Operation**

### 19.4.4 Work Line Drawing Commands

#### (1) LINEWC

##### (a) Function

Draws a 1-dot-wide solid line at work coordinates.

##### (b) Command Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OP CODE = 1111_0000								Reserved (all 0)								Draw mode															
Reserved (all 0)																n (2 ≤ n ≤ 65,535)															
Sign								DX1 (-32,768 ≤ DX1 ≤ 32,767)								Sign								DY1 (-32,768 ≤ DY1 ≤ 32,767)							
Sign								:								Sign								:							
Sign								:								Sign								:							
Sign								DXn (-32,768 ≤ DXn ≤ 32,767)								Sign								DYn (-32,768 ≤ DYn ≤ 32,767)							

Note: When n = 0 or 1, correct operation is not guaranteed.

##### (c) Code

B'11110000

##### (d) Rendering Attributes

Reference Data				Drawing Destination			
Multi-Valued Source	Binary Source	Binary Work	Specified Color	Rendering	Work		
			√ (EOS of binary work)		√		

Draw Mode															
b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
MTRE	LOOP	CLIP	RCLIP	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	EOS	Fixed to 0	Fixed to 0	Fixed to 0

##### (e) Command Parameters

n (n = 2 to 65,535): Number of vertices

DX<sub>i</sub> (i = 1 to 65,535): Work coordinate (absolute coordinate). Negative numbers are expressed as two's complements.

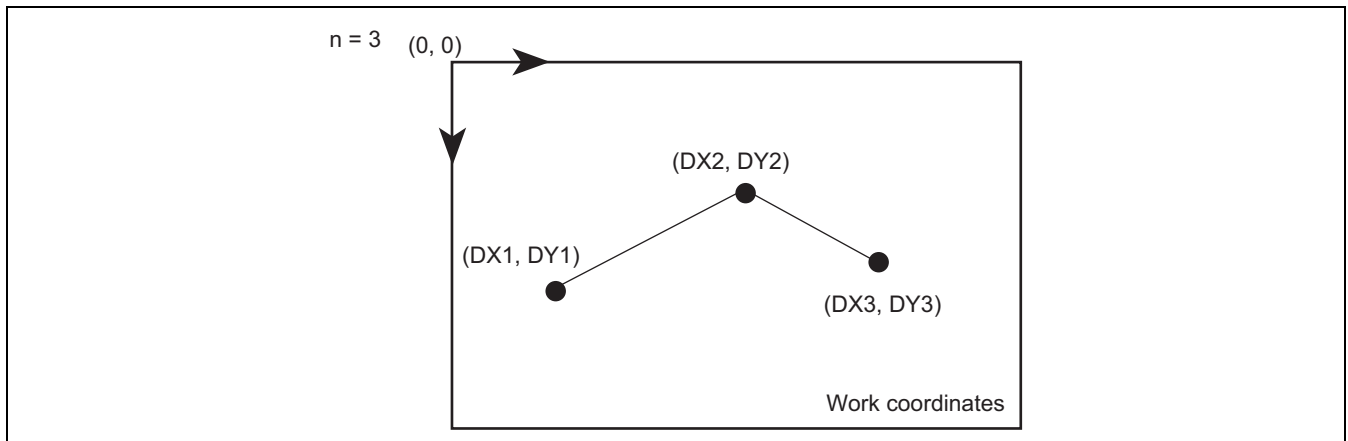
DY<sub>i</sub> (i = 1 to 65,535): Work coordinate (absolute coordinate). Negative numbers are expressed as two's complements.

##### (f) Description

Performs binary drawing at work coordinates of a polygonal line from vertex 1 (DX1, DY1), through vertex 2 (DX2, DY2), ..., vertex n - 1 (DX<sub>n-1</sub>, DY<sub>n-1</sub>), to vertex n (DX<sub>n</sub>, DY<sub>n</sub>). 0 drawing or 1 drawing is selected with the rendering attribute EOS bit. Drawing is performed at work coordinates with 0 when EOS = 0, and at work coordinates with 1 when EOS = 1. (Used for edge drawing at work coordinates for a polygonal painted figure.)

Note: 8-point drawing is used. The final point of each line segment is drawn.



**(g) Example****Figure 19.38 Example of LINEWC Command Operation**

**(2) RLINEWC****(a) Function**

Draws a 1-dot-wide solid line at work coordinates with a relative coordinate specification from the current pointer value.

**(b) Command Format**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
OP CODE = 1111_0100								Reserved (all 0)								Draw mode																			
Reserved (all 0)																n (1 ≤ n ≤ 65,535)																			
Sign	DX2 (-128 ≤ DX2 ≤ 127)								Sign	DY2 (-128 ≤ DY2 ≤ 127)								Sign	DX1 (-128 ≤ DX1 ≤ 127)								Sign	DY1 (-128 ≤ DY1 ≤ 127)							
Sign	:								Sign	:								Sign	:								Sign	:							
Sign	:								Sign	:								Sign	:								Sign	:							
Sign	DXn (-128 ≤ DXn ≤ 127)								Sign	DYn (-128 ≤ DYn ≤ 127)								Sign	DXn-1 (-128 ≤ DXn-1 ≤ 127)								Sign	DYn-1 (-128 ≤ DYn-1 ≤ 127)							

Notes: 1. When n = 0, correct operation is not guaranteed.

2. When n is an odd number, insert a dummy word of 0 at the end.

**(c) Code**

B'11110100

**(d) Rendering Attributes**

Reference Data								Drawing Destination							
Multi-Valued Source	Binary Source	Binary Work	Specified Color	Rendering	Work										
			√ (EOS of binary work)		√										
Draw Mode															
b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
MTRE	LOOP	CLIP	RCLIP	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	EOS	Fixed to 0	Fixed to 0	Fixed to 0

**(e) Command Parameters**

n (n = 1 to 65,535): Number of vertices

DX<sub>i</sub> (i = 1 to 65,535): Work coordinate (relative coordinate). Negative numbers are expressed as two's complements.

DY<sub>i</sub> (i = 1 to 65,535): Work coordinate (relative coordinate). Negative numbers are expressed as two's complements.

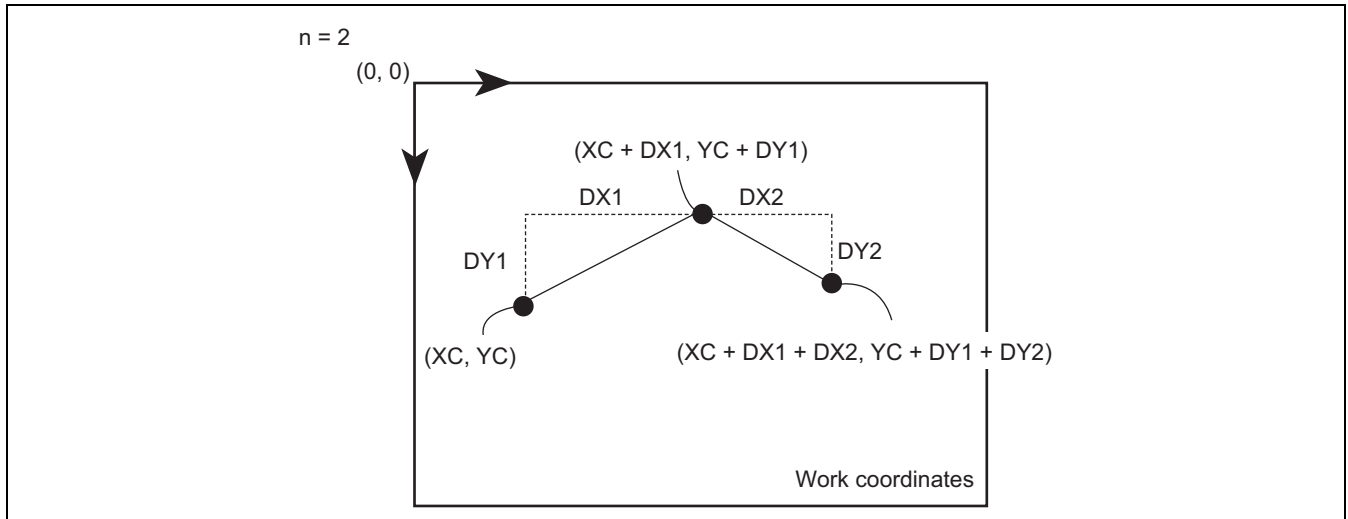
**(f) Description**

Performs binary drawing at work coordinates of a polygonal line comprising line segments (XC, YC) – (XC + DX1, YC + DY1), (XC + DX1, YC + DY1) – (XC + DX1 + DX2, YC + DY1 + DY2), ..., (XC + ... + DX<sub>n-1</sub>, YC + ... + DY<sub>n-1</sub>) – (XC + ... + DX<sub>n-1</sub> + DX<sub>n</sub>, YC + ... + DY<sub>n-1</sub> + DY<sub>n</sub>) to the coordinates specified by the relative shift (DX, DY) from the current pointer values (XC, YC). 0 drawing or 1 drawing is selected with the drawing mode EOS bit. Drawing is performed at work coordinates with 0 when EOS = 0, and at work coordinates with 1 when EOS = 1. (Used for edge drawing at work coordinates for a polygonal painted figure.)

The final coordinate point is stored as the current pointer values (XC, YC).

- Notes: 1. 8-point drawing is used. The end of a line is drawn.  
2. The final coordinate point before coordinate transformation is stored as the current pointer values (XC, YC).

**(g) Example**



**Figure 19.39 Example of RLINEWC Command Operation**

### 19.4.5 Rectangle Drawing Commands

#### (1) BITBLTA

##### (a) Function

Transfers multi-valued (8-, 16-, or 32-bit/pixel) rectangle source data to the destination area.

##### (b) Command Format

- SS = 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OP CODE = 1010_0010								Reserved (all 0)								Draw mode															
Reserved (all 0)								0 0 0 0 0 0 0 0								ROP															
0 0 0 0				TXS ( $0 \leq \text{TXS} \leq 4,088$ )								0 0 0 0				TYS ( $0 \leq \text{TYS} \leq 4,095$ )															
0 0 0 0				LW ( $0 \leq \text{LW} \leq 4,094$ )								0 0 0 0				RW ( $0 \leq \text{RW} \leq 4,094$ )															
0 0 0 0				TH ( $0 \leq \text{TH} \leq 4,094$ )								0 0 0 0				BH ( $0 \leq \text{BH} \leq 4,094$ )															
Sign								BXC ( $-32,768 \leq \text{BXC} \leq 32,767$ )								Sign								BYC ( $-32,768 \leq \text{BYC} \leq 32,767$ )							

- Notes:
1.  $0 \leq \text{TXS} \leq \text{SSTRR} - (\text{LW} + \text{RW} + 1)$ ,  $0 \leq \text{TYS} \leq 4,096 - (\text{TH} + \text{BH} + 1)$  (SSTRR: source stride register setting)
  2.  $8 \leq \text{LW} + \text{RW} + 1 \leq 4,095$ ,  $1 \leq \text{TH} + \text{BH} + 1 \leq 4,095$
  3.  $-32,768 \leq \text{BXC} - \text{LW} \leq 32,767$ ,  $-32,768 \leq \text{BYC} - \text{TH} \leq 32,767$ ,  $-32,768 \leq \text{BXC} + \text{RW} \leq 32,767$ ,  $-32,768 \leq \text{BYC} + \text{BH} \leq 32,767$

- SS = 0 and REL = 0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OP CODE = 1010_0010								Reserved (all 0)								Draw mode															
Reserved (all 0)								0 0 0 0 0 0 0 0								ROP															
0 0 0			Base address (quad word address)																								0 0 0				
0 0 0 0				LW ( $0 \leq \text{LW} \leq 4,087$ )								0 0 0 0				RW ( $0 \leq \text{RW} \leq 4,087$ )															
0 0 0 0				TH ( $0 \leq \text{TH} \leq 4,094$ )								0 0 0 0				BH ( $0 \leq \text{BH} \leq 4,094$ )															
Sign								BXC ( $-32,768 \leq \text{BXC} \leq 32,767$ )								Sign								BYC ( $-32,768 \leq \text{BYC} \leq 32,767$ )							

- Notes:
1.  $8 \leq \text{LW} + \text{RW} + 1 \leq 4,088$  (multiple of 8),  $1 \leq \text{TH} + \text{BH} + 1 \leq 4,095$
  2.  $-32,768 \leq \text{BXC} - \text{LW} \leq 32,767$ ,  $-32,768 \leq \text{BYC} - \text{TH} \leq 32,767$ ,  $-32,768 \leq \text{BXC} + \text{RW} \leq 32,767$ ,  $-32,768 \leq \text{BYC} + \text{BH} \leq 32,767$

- SS = 0 and REL = 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
OP CODE = 1010_0010								Reserved (all 0)								Draw mode																
Reserved (all 0)																0	0	0	0	0	0	0	0	0	ROP							
Sign extended		Sign		Base address (longword address)																								0		0		
0	0	0	0	LW (0 ≤ LW ≤ 4,087)												0	0	0	0	RW (0 ≤ RW ≤ 4,087)												
0	0	0	0	TH (0 ≤ TH ≤ 4,094)												0	0	0	0	BH (0 ≤ BH ≤ 4,094)												
Sign		BXC (-32,768 ≤ BXC ≤ 32,767)												Sign		BYC (-32,768 ≤ BYC ≤ 32,767)																

- Notes:
1.  $8 \leq LW + RW + 1 \leq 4,088$  (multiple of 8),  $1 \leq TH + BH + 1 \leq 4,095$
  2.  $-32,768 \leq BXC - LW \leq 32,767$ ,  $-32,768 \leq BYC - TH \leq 32,767$ ,  $-32,768 \leq BXC + RW \leq 32,767$ ,  $-32,768 \leq BYC + BH \leq 32,767$
  3. Adding the address (longword: 32-bit units) where the command code is located to the base address (longword: 32-bit units) must result in a quad word address (64-bit units).

(c) Code

B'10100010

(d) Rendering Attributes

Reference Data				Drawing Destination		
Multi-Valued Source	Binary Source	Binary Work	Specified Color	Rendering	Work	
√		√ (only WORK = 1)		√		

Draw Mode															
b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
MTRE	Fixed to 0	CLIP	RCLIP	STRANS	DTRANS	WORK	SS	REL	SRCDIRX	SRCDIRY	DSTDIRX	DSTDIRY	COOF	αE	ScE

(e) Command Parameters

- TXS, TYS: Source starting point. Write 0 to the unused bits.
- Base address: Source start absolute address (Quad word address. Write 0 to bits A31 to A29 and A2 to A0.)  
 Source start relative address (Longword address. Negative numbers are expressed as two's complements. Bits A31 to A29 are used to extend the sign in bit A28. Write 0 to bits A1 and A0.)  
 Note: Even in 32-bit addressing mode, write the values in bits 28 to 3 of the specified 32-bit address to bits A28 to A3.
- BXC, BYC: Center X and Y coordinate values. Rendering coordinates (absolute coordinates). Negative numbers are expressed as two's complements.
- LW, RW: Left and right widths. Relative value from (BXC, BYC). Rendering coordinates. Make the setting in pixel units. Write 0 to the unused bits.
- TH, BH: Top and bottom heights. Relative value from (BXC, BYC). Rendering coordinates. Make the setting in pixel units. Write 0 to the unused bits.
- ROP: Raster operation code

**(f) Description**

Transfers multi-valued (8-, 16-, or 32-bit/pixel) rectangle source data to rendering coordinates.

When  $SS = 0$ , set the  $(LW + RW + 1)$  value to be a multiple of 8 pixels. When  $SS = 1$ , set the  $(LW + RW + 1)$  value to be 8 or more pixels.

1. When work specification is selected as a rendering attribute ( $WORK = 1$ ), only places where the work coordinate pixel is 1 are drawn at rendering coordinates while referencing work coordinates for the same coordinates as the rendering coordinates.
2. When  $SS = 1$ , the source data is referenced from the 2-dimensional source area. When  $SS = 0$ , the source data is referenced from the base address in the display list. When  $REL = 0$ , the source address can be specified as an absolute address. When  $REL = 1$ , the source address can be specified as a relative address with respect to the memory address at which the BITBLTA command code is located.
3. In 16-bit/pixel drawing, if the rendering attribute COOF bit is set to 1, the result of adding the value in COFSR to the value of the multi-valued source data is drawn. The operation is performed by saturation processing. In 8-bit/pixel drawing, the COOF bit should be cleared to 0.
4. The direction to reference the source data can be selected by the SRCDIRX and SRCDIRY bits.
5. The drawing direction can be selected by the DSTDIRX and DSTDIRY bits.
6. When  $\alpha E = 1$ , the source data and ground data are alpha blended before drawing. When setting  $\alpha E = 1$ , also set the ROP code = H'CC (source copy). The A value in the ARGB format is not alpha blended. The A value is drawn according to the source A value use (SAU) and A value (AVALUE) bits in the rendering control register (RCLR) and A value 8 register (AVALUE8R). Alpha blending is valid only in 16- or 32-bit/pixel drawing.
7. 16 raster operations are possible. The A value in the ARGB format is not subject to raster operations. The A value is drawn according to the source A value use (SAU) and A value (AVALUE) bits in the rendering control register (RCLR) and A value 8 register (AVALUE8R).

Note: System clipping or (relative) user clipping is performed when drawing a rectangle. Z clipping is performed only at the center coordinates.

(g) Example

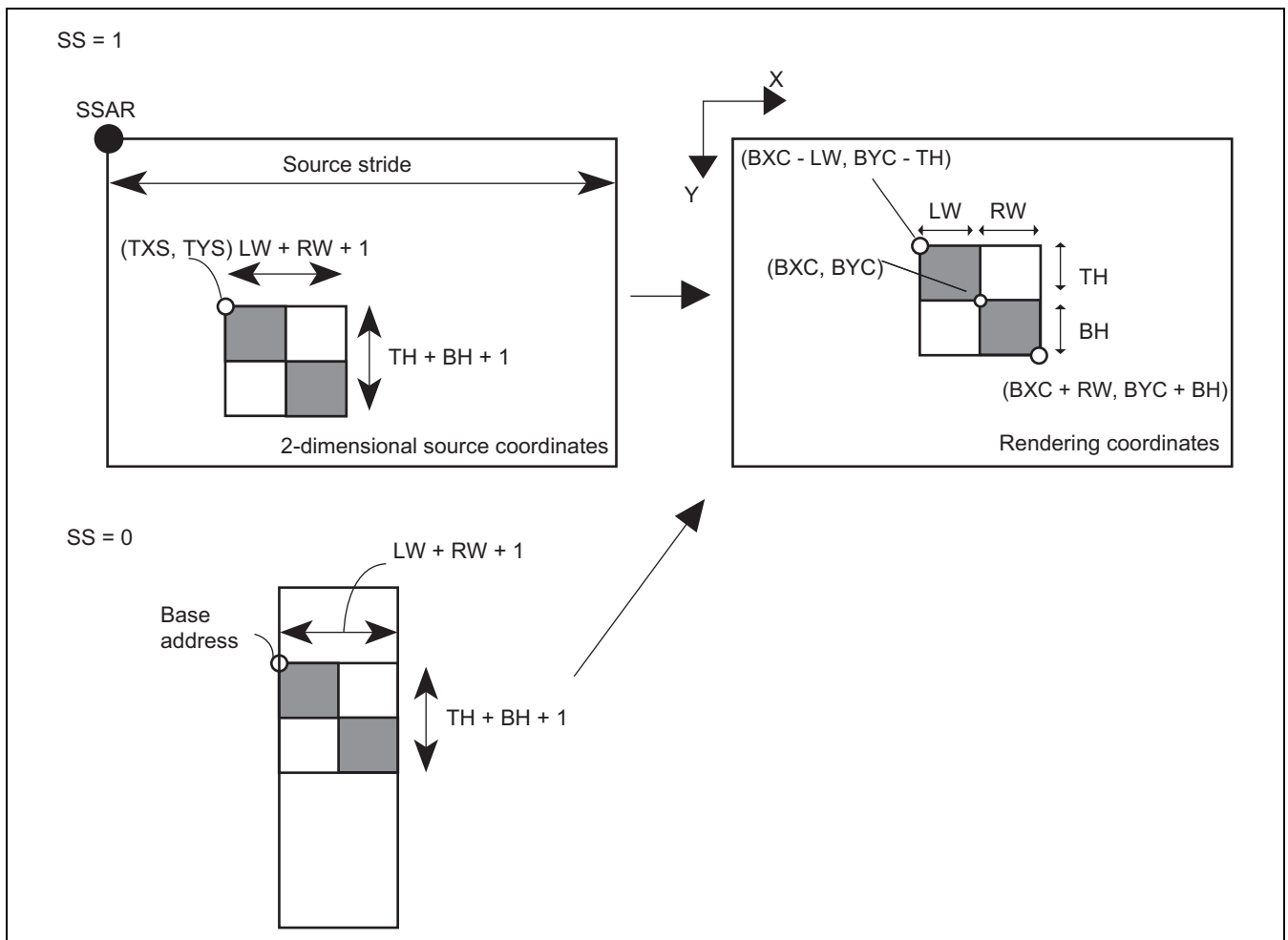


Figure 19.40 Example of BITBLTA Command Operation

**(2) BITBLTB****(a) Function**

Transfers binary (1-bit/pixel) rectangle source data that has been color expanded to the destination area.

**(b) Command Format**

(i) GBM2 = 0

- SS = 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																
OP CODE = 1010_0001				Reserved (all 0)												Draw mode																															
Reserved (all 0)												0 0 0 0				0 0 0 0				0 0 0 0				ROP																							
Color1												Color0																																			
0 0 0 0				TXS ( $0 \leq \text{TXS} \leq 4,088$ )												0 0 0 0				TYS ( $0 \leq \text{TYS} \leq 4,095$ )																											
0 0 0 0				LW ( $0 \leq \text{LW} \leq 4,087$ )												0 0 0 0				RW ( $0 \leq \text{RW} \leq 4,087$ )																											
0 0 0 0				TH ( $0 \leq \text{TH} \leq 4,094$ )												0 0 0 0				BH ( $0 \leq \text{BH} \leq 4,094$ )																											
Sign												BXC ( $-32,768 \leq \text{BXC} \leq 32,767$ )												Sign												BYC ( $-32,768 \leq \text{BYC} \leq 32,767$ )											

- Notes:
- $0 \leq \text{TXS} \leq \text{SSTRR} - (\text{LW} + \text{RW} + 1)$ ,  $0 \leq \text{TYS} \leq 4,096 - (\text{TH} + \text{BH} + 1)$  (SSTRR: source stride register setting)
  - $8 \leq \text{LW} + \text{RW} + 1 \leq 4,088$  (multiple of 8),  $1 \leq \text{TH} + \text{BH} + 1 \leq 4,095$
  - $-32,768 \leq \text{BXC} - \text{LW} \leq 32,767$ ,  $-32,768 \leq \text{BYC} - \text{TH} \leq 32,767$ ,  $-32,768 \leq \text{BXC} + \text{RW} \leq 32,767$ ,  $-32,768 \leq \text{BYC} + \text{BH} \leq 32,767$

- SS = 0 and REL = 0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																
OP CODE = 1010_0001				Reserved (all 0)												Draw mode																															
Reserved (all 0)												0 0 0 0				0 0 0 0				0 0 0 0				ROP																							
Color1												Color0																																			
0 0 0				Base address (quad word address)												0 0 0																															
0 0 0 0				LW ( $0 \leq \text{LW} \leq 4,087$ )												0 0 0 0				RW ( $0 \leq \text{RW} \leq 4,087$ )																											
0 0 0 0				TH ( $0 \leq \text{TH} \leq 4,094$ )												0 0 0 0				BH ( $0 \leq \text{BH} \leq 4,094$ )																											
Sign												BXC ( $-32,768 \leq \text{BXC} \leq 32,767$ )												Sign												BYC ( $-32,768 \leq \text{BYC} \leq 32,767$ )											

- Notes:
- $8 \leq \text{LW} + \text{RW} + 1 \leq 4,088$  (multiple of 8),  $1 \leq \text{TH} + \text{BH} + 1 \leq 4,095$
  - $-32,768 \leq \text{BXC} - \text{LW} \leq 32,767$ ,  $-32,768 \leq \text{BYC} - \text{TH} \leq 32,767$ ,  $-32,768 \leq \text{BXC} + \text{RW} \leq 32,767$ ,  $-32,768 \leq \text{BYC} + \text{BH} \leq 32,767$



- SS = 0 and REL = 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
OP CODE = 1010_0001								Reserved (all 0)								Draw mode																	
Reserved (all 0)																0	0	0	0	0	0	0	0	0	0	ROP							
Color1																Color0																	
Sign extended		Sign		Base address (longword address)																0		0											
0	0	0	0	LW ( $0 \leq LW \leq 4,087$ )												0	0	0	0	RW ( $0 \leq RW \leq 4,087$ )													
0	0	0	0	TH ( $0 \leq TH \leq 4,094$ )												0	0	0	0	BH ( $0 \leq BH \leq 4,094$ )													
Sign		BXC ( $-32,768 \leq BXC \leq 32,767$ )												Sign		BYC ( $-32,768 \leq BYC \leq 32,767$ )																	

- Notes:
1.  $8 \leq LW + RW + 1 \leq 4,088$  (multiple of 8),  $1 \leq TH + BH + 1 \leq 4,095$
  2.  $-32,768 \leq BXC - LW \leq 32,767$ ,  $-32,768 \leq BYC - TH \leq 32,767$ ,  $-32,768 \leq BXC + RW \leq 32,767$ ,  $-32,768 \leq BYC + BH \leq 32,767$
  3. Adding the address (longword: 32-bit units) where the command code is located to the base address (longword: 32-bit units) must result in a quad word address (64-bit units).

## (ii) GBM2 = 1

- SS = 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
OP CODE = 1010_0001								Reserved (all 0)								Draw mode																	
Reserved (all 0)																0	0	0	0	0	0	0	0	0	0	ROP							
Color0																Color1																	
0	0	0	0	TXS ( $0 \leq TXS \leq 4,088$ )												0	0	0	0	TYS ( $0 \leq TYS \leq 4,095$ )													
0	0	0	0	LW ( $0 \leq LW \leq 4,087$ )												0	0	0	0	RW ( $0 \leq RW \leq 4,087$ )													
0	0	0	0	TH ( $0 \leq TH \leq 4,094$ )												0	0	0	0	BH ( $0 \leq BH \leq 4,094$ )													
Sign		BXC ( $-32,768 \leq BXC \leq 32,767$ )												Sign		BYC ( $-32,768 \leq BYC \leq 32,767$ )																	

- Notes:
1.  $0 \leq TXS \leq SSTRR - (LW + RW + 1)$ ,  $0 \leq TYS \leq 4,096 - (TH + BH + 1)$  (SSTRR: Source stride register setting)
  2.  $8 \leq LW + RW + 1 \leq 4,088$  (multiple of 8),  $1 \leq TH + BH + 1 \leq 4,095$
  3.  $-32,768 \leq BXC - LW \leq 32,767$ ,  $-32,768 \leq BYC - TH \leq 32,767$ ,  $-32,768 \leq BXC + RW \leq 32,767$ ,  $-32,768 \leq BYC + BH \leq 32,767$

- SS = 0 and REL = 0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
OP CODE = 1010_0001								Reserved (all 0)								Draw mode																	
Reserved (all 0)																0	0	0	0	0	0	0	0	0	0	ROP							
Color0																Color1																	
0	0	0	Base address (quad word address)																0	0	0												
0	0	0	0	LW ( $0 \leq LW \leq 4,087$ )												0	0	0	0	RW ( $0 \leq RW \leq 4,087$ )													
0	0	0	0	TH ( $0 \leq TH \leq 4,094$ )												0	0	0	0	BH ( $0 \leq BH \leq 4,094$ )													
Sign		BXC ( $-32,768 \leq BXC \leq 32,767$ )												Sign		BYC ( $-32,768 \leq BYC \leq 32,767$ )																	

- Notes:
1.  $8 \leq LW + RW + 1 \leq 4,088$  (multiple of 8),  $1 \leq TH + BH + 1 \leq 4,095$
  2.  $-32,768 \leq BXC - LW \leq 32,767$ ,  $-32,768 \leq BYC - TH \leq 32,767$ ,  $-32,768 \leq BXC + RW \leq 32,767$ ,  $-32,768 \leq BYC + BH \leq 32,767$

- SS = 0 and REL = 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0								
OP CODE = 1010_0001								Reserved (all 0)								Draw mode																							
Reserved (all 0)																0	0	0	0	0	0	0	0	0	ROP														
Color0																																							
Color1																																							
Sign extended		Sign		Base address (longword address)																								0		0									
0	0	0	0	LW ( $0 \leq LW \leq 4,087$ )																0	0	0	0	RW ( $0 \leq RW \leq 4,087$ )															
0	0	0	0	TH ( $0 \leq TH \leq 4,094$ )																0	0	0	0	BH ( $0 \leq BH \leq 4,094$ )															
Sign		BXC ( $-32,768 \leq BXC \leq 32,767$ )																Sign		BYC ( $-32,768 \leq BYC \leq 32,767$ )																			

- Notes:
- $8 \leq LW + RW + 1 \leq 4,088$  (multiple of 8),  $1 \leq TH + BH + 1 \leq 4,095$
  - $-32,768 \leq BXC - LW \leq 32,767$ ,  $-32,768 \leq BYC - TH \leq 32,767$ ,  $-32,768 \leq BXC + RW \leq 32,767$ ,  $-32,768 \leq BYC + BH \leq 32,767$
  - Adding the address (longword: 32-bit units) where the command code is located to the base address (longword: 32-bit units) must result in a quad word address (64-bit units).

(c) Code

B'10100001

(d) Rendering Attributes

Reference Data										Drawing Destination					
Multi-Valued Source	Binary Source	Binary Work	Specified Color	Rendering	Work										
	√	√		√		(only WORK = 1)									

Draw Mode															
b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
MTRE	Fixed to 0	CLIP	RCLIP	STRANS	DTRANS	WORK	SS	REL	SRCDIRX	SRCDIRY	DSTDIRX	DSTDIRY	COOF	αE	Fixed to 0

**(e) Command Parameters**

TXS, TYS:	Source starting point. Write 0 to the unused bits.
Base Address:	Source start absolute address (Quad word address. Write 0 to bits A31 to A29 and A2 to A0.) Source start relative address (Longword address. Negative numbers are expressed as two's complements. Bits A31 to A29 are used to extend the sign in bit A28. Write 0 to bits A1 and A0.) Note: Even in 32-bit addressing mode, write the values in bits 28 to 3 of the specified 32-bit address to bits A28 to A3.
BXC, BYC:	Center X and Y coordinate values. Rendering coordinates (absolute coordinates). Negative numbers are expressed as two's complements.
LW, RW:	Left and right widths. Relative value from (BXC, BYC). Rendering coordinates. Make the setting in pixel units. Write 0 to the unused bits.
TH, BH:	Top and bottom heights. Relative value from (BXC, BYC). Rendering coordinates. Make the setting in pixel units. Write 0 to the unused bits.
ROP:	Raster operation code
Color0, Color1:	8-, 16-, or 32-bit/pixel color specification. For 16-bit/pixel drawing, the color specification should match the destination pixel format. For 8-bit/pixel drawing, the same value should be set in the upper and lower bytes.

**(f) Description**

Transfers binary (1-bit/pixel) rectangle source data to rendering coordinates.

A multiple of 8 pixels must be set as the  $(LW + RW + 1)$  value, regardless of the SS bit value.

1. When work specification is selected as a rendering attribute ( $WORK = 1$ ), only places where the work coordinate pixel is 1 are drawn at rendering coordinates while referencing work coordinates for the same coordinates as the rendering coordinates.
2. The binary source data is arranged in memory in a linear fashion. When  $REL = 0$ , the source address can be specified as an absolute address. When  $REL = 1$ , the source address can be specified as a relative address with respect to the memory address at which the BITBLTB command code is located.
3. If the rendering attribute COOF bit is set to 1, the result of adding the value in COFSR to the value of the binary source data that has been color expanded is drawn. The operation is performed by saturation processing. In 8-bit/pixel drawing, the COOF bit should be cleared to 0.
4. The direction to reference the source data can be selected by the SRCDIRX and SRCDIRY bits.
5. The drawing direction can be selected by the DSTDIRX and DSTDIRY bits.
6. When  $\alpha E = 1$ , the data obtained by color expanding the binary source data and the ground data are alpha blended before drawing. When setting  $\alpha E = 1$ , also set the ROP code = H'CC (source copy). The A value in the ARGB format is not alpha blended. The A value is drawn according to the source A value use (SAU) and A value (AVALUE) bits in the rendering control register (RCLR) and A value 8 register (AVALUE8R). Alpha blending is valid only in 16- or 32-bit/pixel drawing.
7. 16 raster operations are possible. The A value in the ARGB format is not subject to raster operations. The A value is drawn according to the source A value use (SAU) and A value (AVALUE) bits in the rendering control register (RCLR) and A value 8 register (AVALUE8R).

Note: System clipping or (relative) user clipping is performed when drawing a rectangle. Z clipping is performed only at the center coordinates.

(g) Example

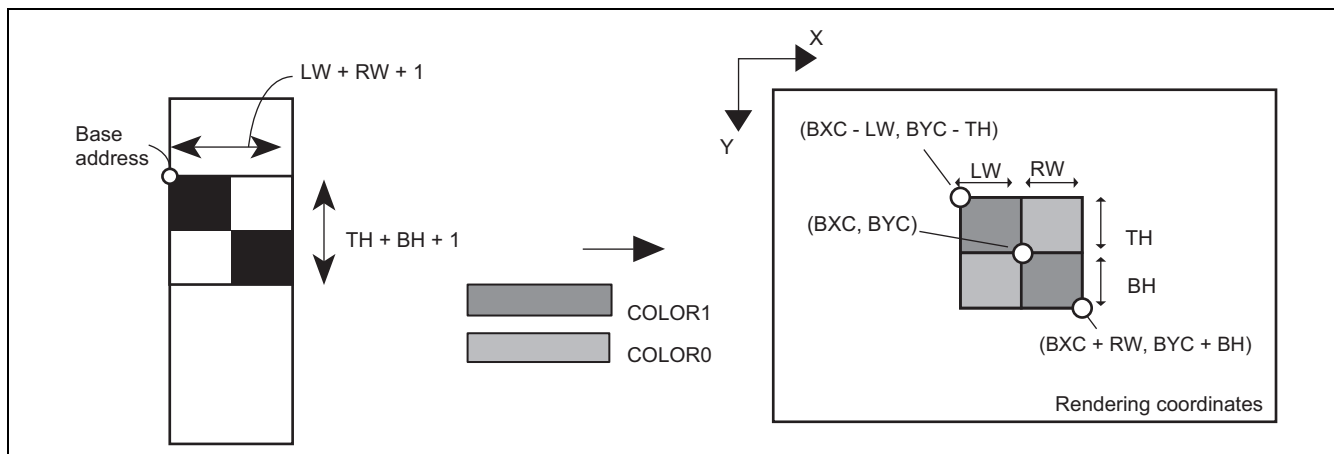


Figure 19.41 Example of BITBLTB Command Operation

**(3) BITBLTC**

**(a) Function**

Draws a rectangle with a monochrome specification to the destination area.

**(b) Command Format**

- GBM2 = 0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OP CODE = 1010_0000								Reserved (all 0)								Draw mode															
Reserved (all 0)								0 0 0 0 0 0 0 0								ROP															
Reserved (all 0)								Color																							
0 0 0 0				LW (0 ≤ LW ≤ 4,094)								0 0 0 0				RW (0 ≤ RW ≤ 4,094)															
0 0 0 0				TH (0 ≤ TH ≤ 4,094)								0 0 0 0				BH (0 ≤ BH ≤ 4,094)															
Sign BXC (-32,768 ≤ BXC ≤ 32,767)								Sign BYC (-32,768 ≤ BYC ≤ 32,767)																							

Notes: 1.  $1 \leq LW + RW + 1 \leq 4,095$ ,  $1 \leq TH + BH + 1 \leq 4,095$   
 2.  $-32,768 \leq BXC - LW \leq 32,767$ ,  $-32,768 \leq BYC - TH \leq 32,767$ ,  $-32,768 \leq BXC + RW \leq 32,767$ ,  
 $-32,768 \leq BYC + BH \leq 32,767$

- GBM2 = 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OP CODE = 1010_0000								Reserved (all 0)								Draw mode															
Reserved (all 0)								0 0 0 0 0 0 0 0								ROP															
								Color																							
0 0 0 0				LW (0 ≤ LW ≤ 4,094)								0 0 0 0				RW (0 ≤ RW ≤ 4,094)															
0 0 0 0				TH (0 ≤ TH ≤ 4,094)								0 0 0 0				BH (0 ≤ BH ≤ 4,094)															
Sign BXC (-32,768 ≤ BXC ≤ 32,767)								Sign BYC (-32,768 ≤ BYC ≤ 32,767)																							

Notes: 1.  $1 \leq LW + RW + 1 \leq 4,095$ ,  $1 \leq TH + BH + 1 \leq 4,095$   
 2.  $-32,768 \leq BXC - LW \leq 32,767$ ,  $-32,768 \leq BYC - TH \leq 32,767$ ,  $-32,768 \leq BXC + RW \leq 32,767$ ,  
 $-32,768 \leq BYC + BH \leq 32,767$

**(c) Code**

B'10100000

**(d) Rendering Attributes**

Reference Data										Drawing Destination					
Multi-Valued Source										Work					
Binary Source					Binary Work					Specified Color			Rendering		
					√					√			√		
					(only WORK = 1)										

Draw Mode															
b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
MTRE	Fixed to 0	CLIP	RCLIP	Fixed to 0	DTRANS	WORK	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	DSTDIRX	DSTDIRY	COOF	αE	Fixed to 0

**(e) Command Parameters**

BXC, BYC:	Center X and Y coordinate values. Rendering coordinates (absolute coordinates). Negative numbers are expressed as two's complements.
LW, RW:	Left and right widths. Relative value from (BXC, BYC). Rendering coordinates. Make the setting in pixel units. Write 0 to the unused bits.
TH, BH:	Top and bottom heights. Relative value from (BXC, BYC). Rendering coordinates. Make the setting in pixel units. Write 0 to the unused bits.
Color:	8-, 16-, or 32-bit/pixel color specification. For 16-bit/pixel drawing, the color specification should match the destination pixel format. For 8-bit/pixel drawing, the same value should be set in the upper and lower bytes.
ROP:	Raster operation code

**(f) Description**

Draws a rectangle in the destination area in the single color specified by the Color parameter.

1. When work specification is selected as a rendering attribute ( $WORK = 1$ ), only places where the work coordinate pixel is 1 are drawn at rendering coordinates while referencing work coordinates for the same coordinates as the rendering coordinates.
2. If the rendering attribute COOF bit is set to 1, the result of adding the value in COFSR to the value of the specified color is drawn. The operation is performed by saturation processing. In 8-bit/pixel drawing, the COOF bit should be cleared to 0.
3. The drawing direction can be selected by the DSTDIRX and DSTDIRY bits.
4. When  $\alpha E = 1$ , the specified color data and ground data are alpha blended before drawing. When setting  $\alpha E = 1$ , also set the ROP code = H'CC (source copy). The A value in the ARGB format is not alpha blended. The A value is drawn according to the source A value use (SAU) and A value (AVALUE) bits in the rendering control register (RCLR) and A value 8 register (AVALUE8R). Alpha blending is valid only in 16- or 32-bit/pixel drawing.
5. 16 raster operations are possible. The A value in the ARGB format is not subject to raster operations. The A value is drawn according to the source A value use (SAU) and A value (AVALUE) bits in the rendering control register (RCLR) and A value 8 register (AVALUE8R).

Note: System clipping or (relative) user clipping is performed when drawing a rectangle. Z clipping is performed only at the center coordinates.

(g) Example

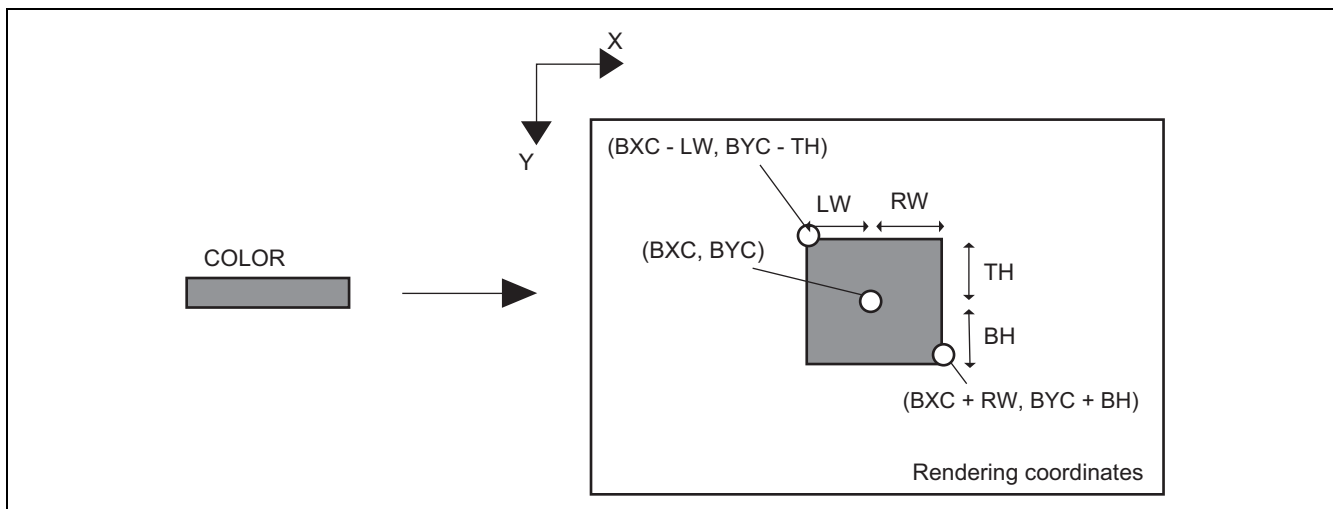


Figure 19.42 Example of BITBLTC Command Operation

**(4) AAFA****(a) Function**

AAFA commands perform alpha blending of the multi-valued source (S) and ground data (D) with reference to the  $\alpha$  map for drawing (8 bits/pixel) and draw the result in the destination area (D'). This command can only be executed for a 16-bit/pixel destination.

**(b) Command Format**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OP CODE = 1010_1010				Reserved (all 0)												Draw mode															
0	0	0	0	RAXS ( $0 \leq \text{RAXS} \leq 4,088$ )												0	0	0	0	RAYS ( $0 \leq \text{RAYS} \leq 4,095$ )											
0	0	0	0	TXS ( $0 \leq \text{TXS} \leq 4,088$ )												0	0	0	0	TYS ( $0 \leq \text{TYS} \leq 4,095$ )											
0	0	0	0	LW ( $0 \leq \text{LW} \leq 4,094$ )												0	0	0	0	RW ( $0 \leq \text{RW} \leq 4,094$ )											
0	0	0	0	TH ( $0 \leq \text{TH} \leq 4,094$ )												0	0	0	0	BH ( $0 \leq \text{BH} \leq 4,094$ )											
Sign				BXC ( $-32,768 \leq \text{BXC} \leq 32,767$ )												Sign				BYC ( $-32,768 \leq \text{BYC} \leq 32,767$ )											

- Notes:
- $0 \leq \text{TXS} \leq \text{SSTRR} - (\text{LW} + \text{RW} + 1)$ ,  $0 \leq \text{TYS} \leq 4,096 - (\text{TH} + \text{BH} + 1)$  (SSTRR: source stride register setting)
  - $0 \leq \text{RAXS} \leq \text{ASTRR} - (\text{LW} + \text{RW} + 1)$ ,  $0 \leq \text{RAYS} \leq 4,096 - (\text{TH} + \text{BH} + 1)$  (ASTRR:  $\alpha$  map stride register setting)
  - $8 \leq \text{LW} + \text{RW} + 1 \leq 4,095$ ,  $1 \leq \text{TH} + \text{BH} + 1 \leq 4,095$
  - $-32,768 \leq \text{BXC} - \text{LW} \leq 32,767$ ,  $-32,768 \leq \text{BYC} - \text{TH} \leq 32,767$ ,  $-32,768 \leq \text{BXC} + \text{RW} \leq 32,767$ ,  $-32,768 \leq \text{BYC} + \text{BH} \leq 32,767$

**(c) Code**

B'10101010

**(d) Rendering Attributes**

Reference Data				Drawing Destination		
Multi-Valued Source	Binary Source	Binary Work	Specified Color	Rendering	Work	
√	√	√ (only WORK = 1)		√		

Draw Mode															
b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
MTRE	Fixed to 0	CLIP	RCLIP	STRANS	DTRANS	WORK	SS (1)	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	COOF	$\alpha$ E (1)	ScE

- Notes:
- Set the SS bit to 1.
  - Set the  $\alpha$ E bit to 1.

**(e) Command Parameters**

- RAXS, RAYS: Starting point of  $\alpha$  map for drawing. Write 0 to the unused bits.
- TXS, TYS: Source starting point. Write 0 to the unused bits.
- BXC, BYC: Center X and Y coordinate values. Rendering coordinates (absolute coordinates). Negative numbers are expressed as two's complements.
- LW, RW: Left and right widths. Relative value from (BXC, BYC). Rendering coordinates. Make the setting in pixel units. Write 0 to the unused bits.
- TH, BH: Top and bottom heights. Relative value from (BXC, BYC). Rendering coordinates. Make the setting in pixel units. Write 0 to the unused bits.

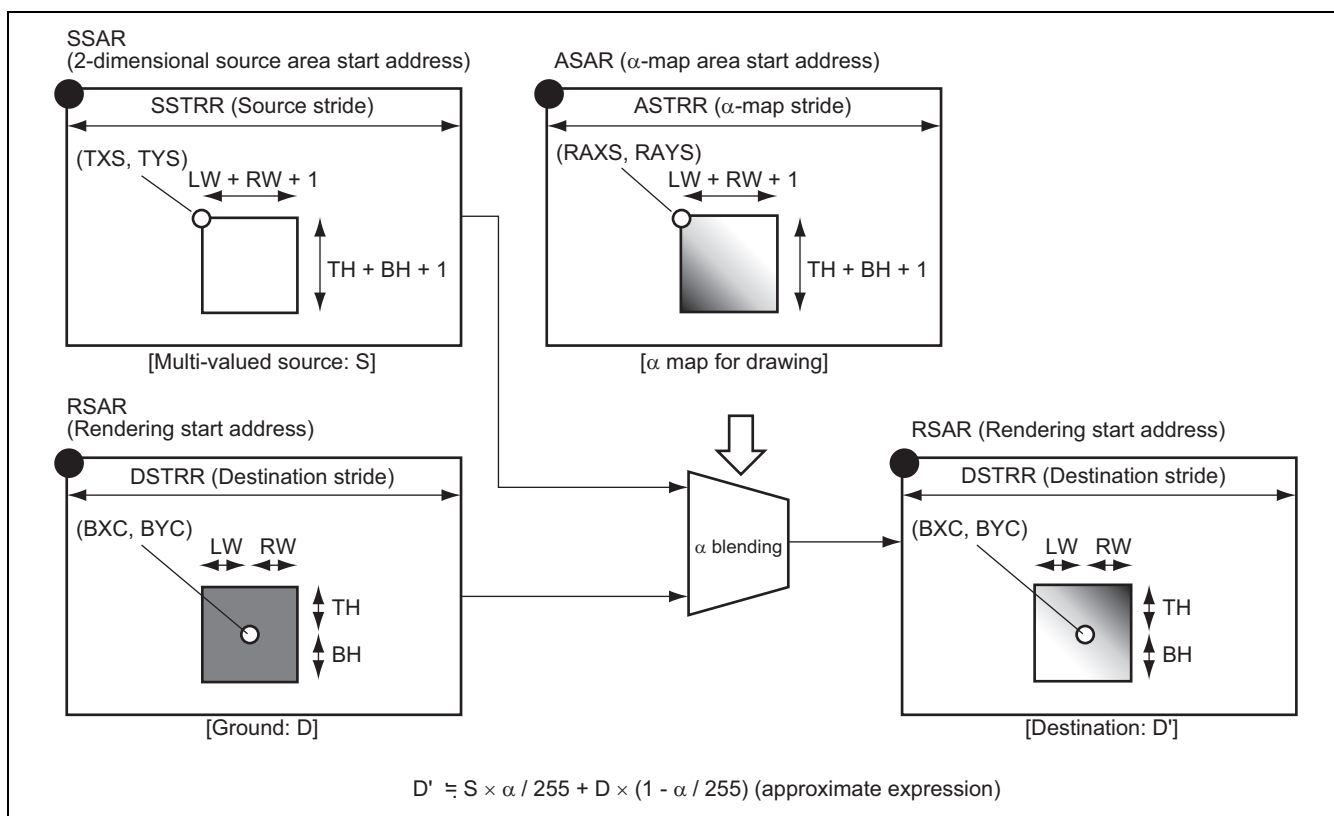


**(f) Description**

AAFA commands perform alpha blending of the multi-valued source (S) and ground data (D) with reference to the  $\alpha$  map for drawing (8 bits/pixel) and draw the result in the destination area (D'). The multi-valued source and the  $\alpha$  map for drawing can only be used for 2-dimensional positioning, so set SS to 1. If it is desired to use the multi-valued source and  $\alpha$  map for drawing in 1 dimension, set the stride of the multi-valued source and the  $\alpha$  map for drawing to LW + RW + 1. The stride of the multi-valued source and the  $\alpha$  map for drawing is set in 8-pixel units, so in the case of use in 1 dimension, LW + RW + 1 is also set in 8-pixel units.

- Notes:
1. System clipping or (relative) user clipping is performed when drawing a rectangle. Z clipping is performed only at the center coordinates.
  2. The scan direction for the multi-valued source and the  $\alpha$  map for drawing and the direction of drawing to the destination are fixed to upper left to lower right.
  3. If the  $\alpha$  map for drawing are all 0, the pixel is not drawn (the value A also is not changed).

**(g) Example**



**Figure 19.43 Example of AAFA Command Operation**

**(5) AAFC****(a) Function**

AAFC commands perform alpha blending of the specified color and the ground data with reference to the  $\alpha$  map for drawing (8 bits/pixel) as the alpha value and draw the result in the destination area. This command can only be executed for a 16- or 32-bit/pixel destination.

**(b) Command Format**

(i) GBM2 = 0

- REL = 0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OP CODE = 1010_1000								Reserved (all 0)								Draw mode															
Reserved (all 0)																Color															
0 0 0			Base address (quad word address)																								0 0 0				
0 0 0 0				LW ( $0 \leq LW \leq 4,087$ )												0 0 0 0				RW ( $0 \leq RW \leq 4,087$ )											
0 0 0 0				TH ( $0 \leq TH \leq 4,094$ )												0 0 0 0				BH ( $0 \leq BH \leq 4,094$ )											
Sign		BXC ( $-32,768 \leq BXC \leq 32,767$ )												Sign		BYC ( $-32,768 \leq BYC \leq 32,767$ )															

- Notes:
- $8 \leq LW + RW + 1 \leq 4,088$  (multiple of 8),  $1 \leq TH + BH + 1 \leq 4,095$
  - $-32,768 \leq BXC - LW \leq 32,767$ ,  $-32,768 \leq BYC - TH \leq 32,767$ ,  $-32,768 \leq BXC + RW \leq 32,767$ ,  $-32,768 \leq BYC + BH \leq 32,767$

- REL = 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OP CODE = 1010_1000								Reserved (all 0)								Draw mode															
Reserved (all 0)																Color															
Sign extended		Sign		Base address (longword address)																								0 0			
0 0 0 0				LW ( $0 \leq LW \leq 4,087$ )												0 0 0 0				RW ( $0 \leq RW \leq 4,087$ )											
0 0 0 0				TH ( $0 \leq TH \leq 4,094$ )												0 0 0 0				BH ( $0 \leq BH \leq 4,094$ )											
Sign		BXC ( $-32,768 \leq BXC \leq 32,767$ )												Sign		BYC ( $-32,768 \leq BYC \leq 32,767$ )															

- Notes:
- $8 \leq LW + RW + 1 \leq 4,088$  (multiple of 8),  $1 \leq TH + BH + 1 \leq 4,095$
  - $-32,768 \leq BXC - LW \leq 32,767$ ,  $-32,768 \leq BYC - TH \leq 32,767$ ,  $-32,768 \leq BXC + RW \leq 32,767$ ,  $-32,768 \leq BYC + BH \leq 32,767$
  - Adding the address (longword: 32-bit units) where the command code is located to the base address (longword: 32-bit units) must result in a quad word address (64-bit units).

(ii) GBM2 = 1

- REL = 0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OP CODE = 1010_1000								Reserved (all 0)								Draw mode															
Color																															
0 0 0			Base address (quad word address)																								0 0 0				
0 0 0 0				LW (0 ≤ LW ≤ 4,087)												0 0 0 0				RW (0 ≤ RW ≤ 4,087)											
0 0 0 0				TH (0 ≤ TH ≤ 4,094)												0 0 0 0				BH (0 ≤ BH ≤ 4,094)											
Sign BXC (-32,768 ≤ BXC ≤ 32,767)																Sign BYC (-32,768 ≤ BYC ≤ 32,767)															

- Notes:
- $8 \leq LW + RW + 1 \leq 4,088$  (multiple of 8),  $1 \leq TH + BH + 1 \leq 4,095$
  - $-32,768 \leq BXC - LW \leq 32,767$ ,  $-32,768 \leq BYC - TH \leq 32,767$ ,  $-32,768 \leq BXC + RW \leq 32,767$ ,  $-32,768 \leq BYC + BH \leq 32,767$

- REL = 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OP CODE = 1010_1000								Reserved (all 0)								Draw mode															
Color																															
Sign extended		Sign		Base address (longword address)																								0 0			
0 0 0 0				LW (0 ≤ LW ≤ 4,087)												0 0 0 0				RW (0 ≤ RW ≤ 4,087)											
0 0 0 0				TH (0 ≤ TH ≤ 4,094)												0 0 0 0				BH (0 ≤ BH ≤ 4,094)											
Sign BXC (-32,768 ≤ BXC ≤ 32,767)																Sign BYC (-32,768 ≤ BYC ≤ 32,767)															

- Notes:
- $8 \leq LW + RW + 1 \leq 4,088$  (multiple of 8),  $1 \leq TH + BH + 1 \leq 4,095$
  - $-32,768 \leq BXC - LW \leq 32,767$ ,  $-32,768 \leq BYC - TH \leq 32,767$ ,  $-32,768 \leq BXC + RW \leq 32,767$ ,  $-32,768 \leq BYC + BH \leq 32,767$
  - Adding the address (longword: 32-bit units) where the command code is located to the base address (longword: 32-bit units) must result in a quad word address (64-bit units).

(c) Code

B'10101000

(d) Rendering Attributes

Reference Data				Drawing Destination			
a_value	Source	Binary Source	Binary Work	Specified Color	Rendering	Work	
√				√	√		

Draw Mode															
b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
MTRE	Fixed to 0	CLIP	RCLIP	Fixed to 0	DTRANS	Fixed to 0	SS (0)	REL	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0

Note: Clear the SS bit to 0.

**(e) Command Parameters**

Base address:	<p><math>\alpha</math>-map address for drawing start absolute address (Quad word address. Write 0 to bits A31 to A29 and A2 to A0.)</p> <p><math>\alpha</math>-map address for drawing start relative address (Longword address. Negative numbers are expressed as two's complements. Bits A31 to A29 are used to extend the sign in bit A28. Write 0 to bits A1 and A0.)</p> <p>Note: Even in 32-bit addressing mode, write the values in bits 28 to 3 of the specified 32-bit address to bits A28 to A3.</p>
BXC, BYC:	Center X and Y coordinate values. Rendering coordinates (absolute coordinates). Negative numbers are expressed as two's complements.
LW, RW:	Left and right widths. Relative value from (BXC, BYC). Rendering coordinates. Make the setting in pixel units. Write 0 to the unused bits.
TH, BH:	Top and bottom heights. Relative value from (BXC, BYC). Rendering coordinates. Make the setting in pixel units. Write 0 to the unused bits.
Color:	16- or 32-bit/pixel color specification. The color specification should match the destination pixel format.

**(f) Description**

AAFC commands perform alpha blending of the specified color and the ground data with reference to the  $\alpha$  map for drawing use (8 bits/pixel) as the alpha value and draw the result in the destination area. A multiple of 8 pixels must be set as the  $(LW + RW + 1)$  value.

The 8-bit  $\alpha$  map for drawing is arranged linearly in memory. When  $REL = 0$ , the source address can be specified as an absolute address.

When  $REL = 1$ , the address of  $\alpha$  map for drawing can be specified as a relative address with respect to the memory address at which the AAFC command code is located.

- Notes:
1. System clipping or (relative) user clipping is performed when drawing a rectangle. Z clipping is performed only at the center coordinates.
  2. The scan direction for the  $\alpha$  map for drawing and the direction of drawing to the destination are fixed to upper left to lower right.
  3. If the  $\alpha$  map for drawing are all 0, the pixel is not drawn (the value A also is not changed).

(g) Example

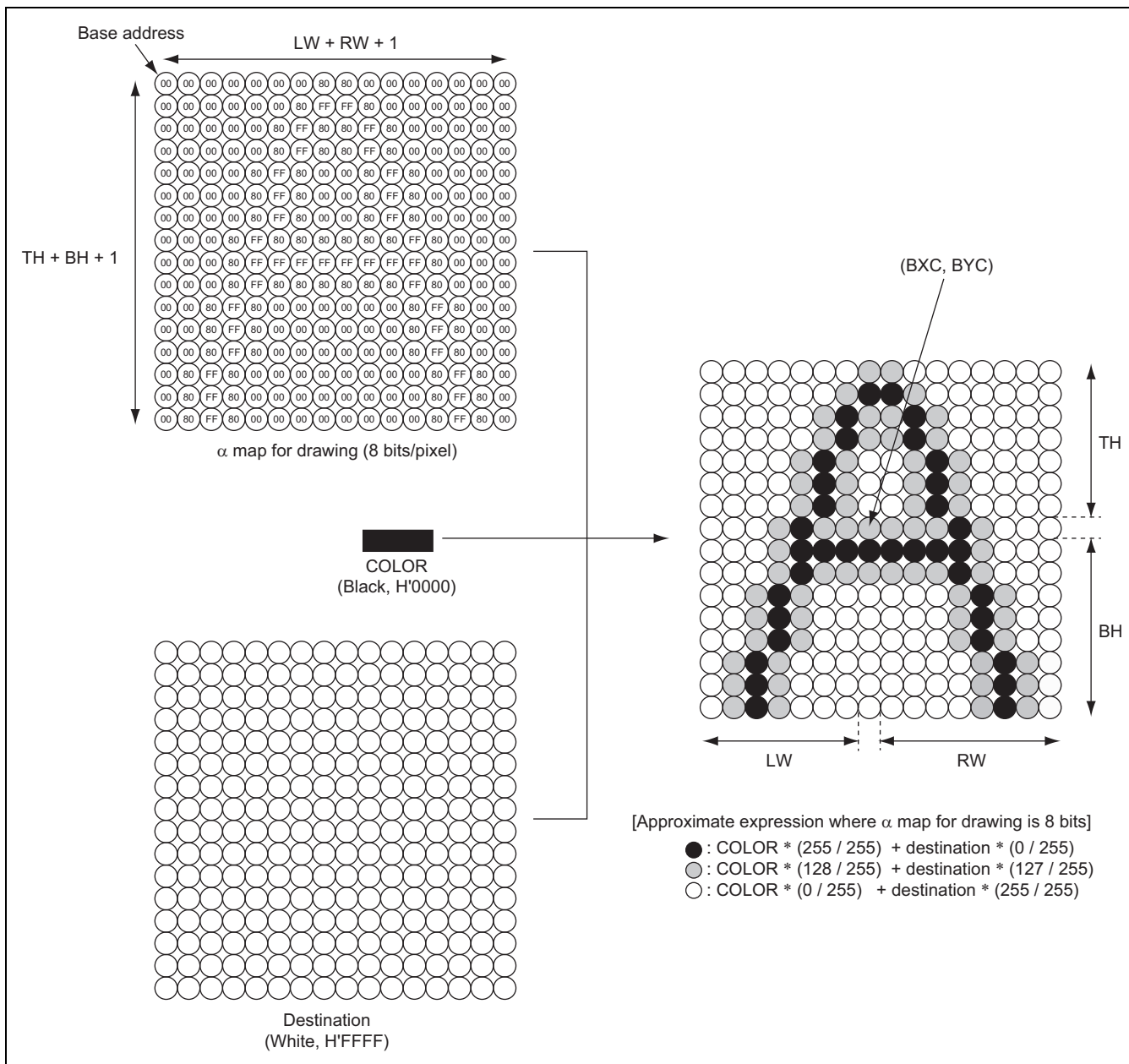


Figure 19.44 Example of AAFC Command Operation

## 19.4.6 Control Commands

### (1) MOVE

#### (a) Function

Sets the current pointer.

#### (b) Command Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OP CODE = 0100_1000								Reserved (all 0)								Draw mode															
XC ( $-32,768 \leq XC \leq 32,767$ )																YC ( $-32,768 \leq YC \leq 32,767$ )															

#### (c) Code

B'01001000

#### (d) Rendering Attributes

Draw Mode															
b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0

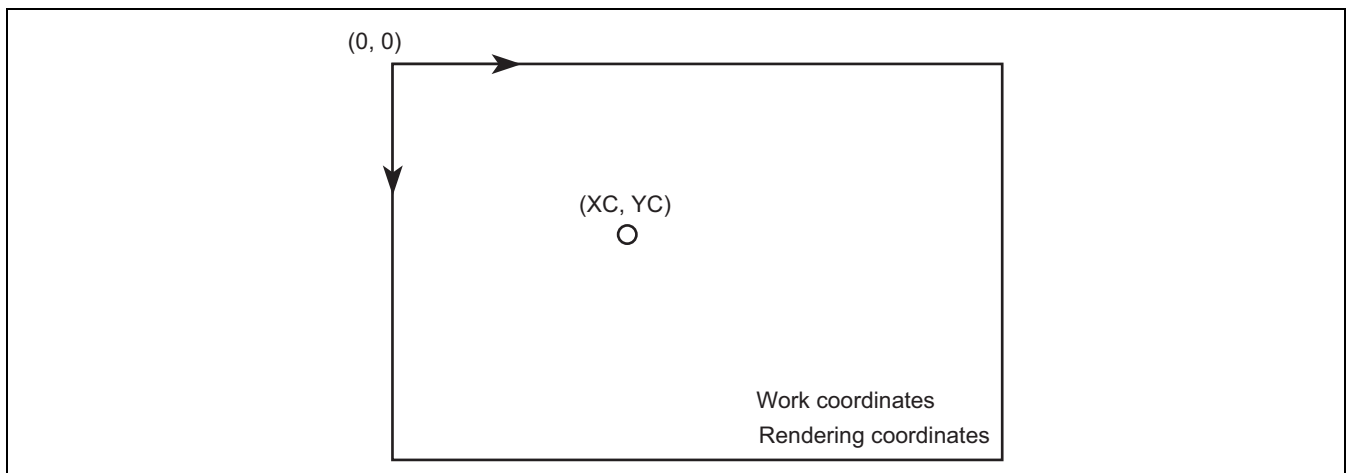
#### (e) Command Parameters

XC: Rendering coordinate (absolute coordinate) or work coordinate (absolute coordinate).  
Negative numbers are expressed as two's complements.

YC: Rendering coordinate (absolute coordinate) or work coordinate (absolute coordinate).  
Negative numbers are expressed as two's complements.

#### (f) Description

Sets the values obtained by adding the local offset values to XC and YC in the current pointers. XC and YC are set as absolute coordinates. The current pointers are used by relative drawing commands only. After issuing a MOVE command, use relative drawing commands in succession. If an absolute drawing command is used during this sequence, the current pointers will be used as registers for internal computation, and the current pointer values will be lost. A MOVE command must therefore be issued before using relative drawing commands again.

**(g) Example****Figure 19.45 Example of MOVE Command Operation**

**(2) RMOVE**

**(a) Function**

Adds XC and YC to the current pointers.

**(b) Command Format**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OP CODE = 0100_1100								Reserved (all 0)								Draw mode															
XC (-32,768 ≤ XC ≤ 32,767)																YC (-32,768 ≤ YC ≤ 32,767)															

**(c) Code**

B'01001100

**(d) Rendering Attributes**

Draw Mode															
b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0

**(e) Command Parameters**

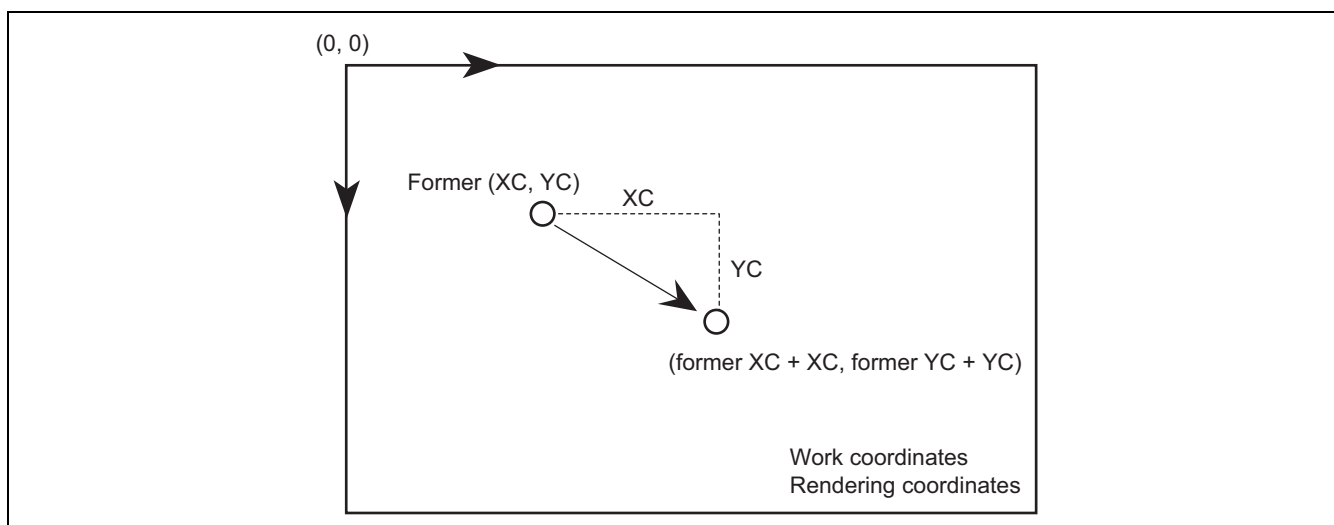
XC: Rendering coordinate (relative coordinate) or work coordinate (relative coordinate). Negative numbers are expressed as two's complements.

YC: Rendering coordinate (relative coordinate) or work coordinate (relative coordinate). Negative numbers are expressed as two's complements.

**(f) Description**

Adds XC and YC to the current pointers.

**(g) Example**



**Figure 19.46 Example of RMOVE Command Operation**



**(3) LCOFS****(a) Function**

Sets the offset values (local offset) of the destination area and work area.

**(b) Command Format**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OP CODE = 0100_0000								Reserved (all 0)								Draw mode															
XO (-32,768 ≤ XO ≤ 32,767)																YO (-32,768 ≤ YO ≤ 32,767)															

**(c) Code**

B'01000000

**(d) Rendering Attributes**

Draw Mode															
b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0

**(e) Command Parameters**

- XO: Local offset value. Rendering coordinate (absolute coordinate) or work coordinate (absolute coordinate). Negative numbers are expressed as two's complements.
- YO: Local offset value. Rendering coordinate (absolute coordinate) or work coordinate (absolute coordinate). Negative numbers are expressed as two's complements.

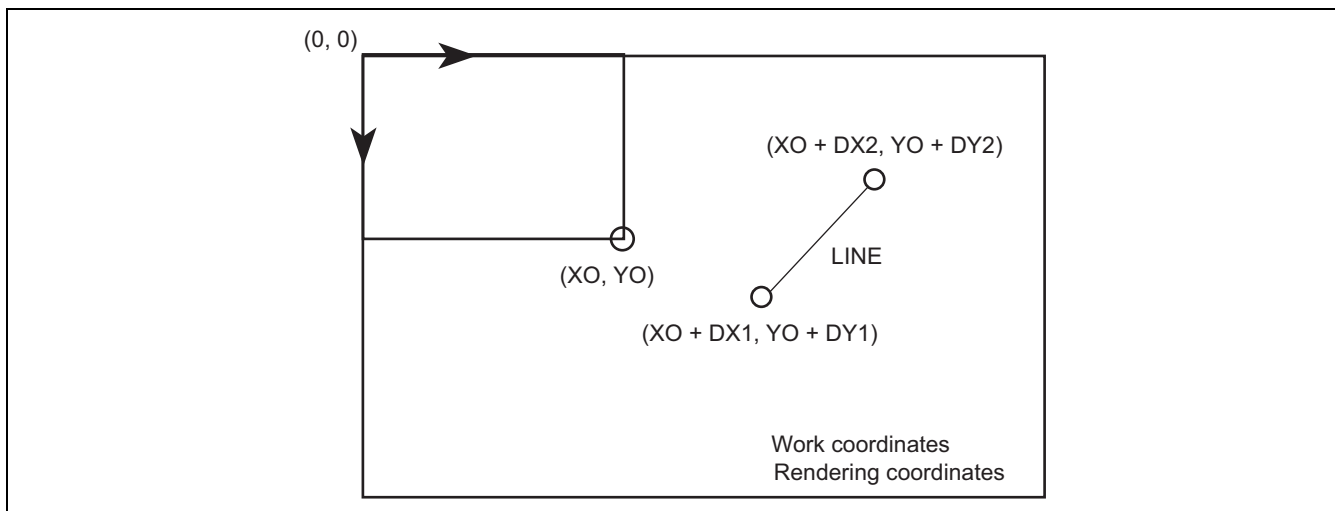
**(f) Description**

After the local offset values are set, these offset values are added in all subsequent coordinate specifications made in drawing commands.

These settings must be made at the start of the display list (the initial values are undefined).

To reflect the local offset values in the current pointers, issue a MOVE command after the LCOFS command.

**(g) Example**



**Figure 19.47 Example of LCOFS Command Operation**

**(4) RLCOFS****(a) Function**

Adds XO and YO to the local offset.

**(b) Command Format**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OP CODE = 0100_0100								Reserved (all 0)								Draw mode															
XO (-32,768 ≤ XO ≤ 32,767)																YO (-32,768 ≤ YO ≤ 32,767)															

**(c) Code**

B'01000100

**(d) Rendering Attributes**

Draw Mode															
b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0

**(e) Command Parameters**

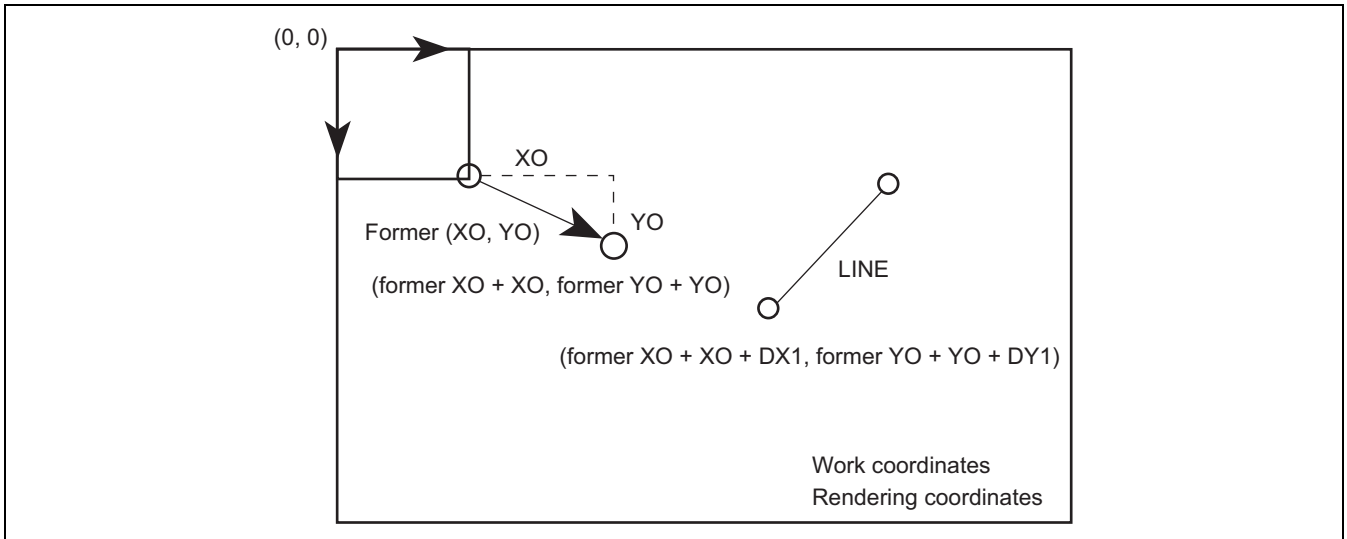
- XO: Local offset value. Rendering coordinate (relative coordinate) or work coordinate (relative coordinate). Negative numbers are expressed as two's complements.
- YO: Local offset value. Rendering coordinate (relative coordinate) or work coordinate (relative coordinate). Negative numbers are expressed as two's complements.

**(f) Description**

Adding XO and YO to the local offset makes the local offset values. After the local offset values are set, these offset values are added in all subsequent coordinate specifications made in drawing commands.

To reflect the local offset values in the current pointers, issue a MOVE command after setting the local offset with the LCOFS or RLCOFS command.

**(g) Example**



**Figure 19.48 Example of RLCOFS Command Operation**

**(5) WPR**

**(a) Function**

Sets a value in a specific address-mapped register.

**(b) Command Format**

- LINKE = 0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OP CODE = 0001_1000								Reserved (all 0)								Draw mode															
Reserved (all 0)								n - 1 (0 ≤ n - 1 ≤ 255)								0 0 0 0				W reg No											
Data0																															
:																															
:																															
Data n-1																															

- LINKE = 1 and LREL = 0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OP CODE = 0001_1000								Reserved (all 0)								Draw mode															
Reserved (all 0)								n - 1 (0 ≤ n - 1 ≤ 255)								0 0 0 0				W reg No											
0 0 0			LINK address (longword address)													0 0															

Note: The longword address following the LINK address is handled as the next command code. Therefore, do not specify the longword address following the address where the LINK address is to be assigned as the link destination address specified by the LINK address.

- LINKE = 1 and LREL = 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OP CODE = 0001_1000								Reserved (all 0)								Draw mode															
Reserved (all 0)								n - 1 (0 ≤ n - 1 ≤ 255)								0 0 0 0				W reg No											
Sign extended		Sign		LINK address (longword address)													0 0														

Note: The longword address following the LINK address is handled as the next command code. Therefore, do not specify the longword address following the address where the LINK address is to be assigned as the link destination address specified by the address where the command code is located plus the LINK address.

**(c) Code**

B'00011000

**(d) Rendering Attributes**

Draw Mode															
b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	LINKE	LREL	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	ByteM3	ByteM2	ByteM1	ByteM0

**(e) Command Parameters**

W reg No:	Register number
Data i (i = 0 to n – 1):	Write data
n – 1:	The number of write data
LINK Address:	LINK absolute address (Longword address. Write 0 to bits A31 to A29, A1, and A0.) LINK relative address (Longword address. Negative numbers are expressed as two's complements. Bits A31 to A29 are used to extend the sign in bit A28. Write 0 to bits A1 and A0.)

Note: Even in 32-bit addressing mode, write the values in bits 28 to 3 of the specified 32-bit address to bits A28 to A3.

**(f) Description**

Writes data to the address-mapped registers. The register number is set in W reg No, and the write data in Data n.

Also ensure that there is no conflict with access by the CPU.

1. When the LINKE bit is set to 1, data is read from the memory address specified by the LINK address and written to a register.
2. The LINK address can be specified through the LREL bit as an absolute address or a relative address with respect to the memory address at which the WPR command code is located.
3. Setting the ByteM3 to ByteM0 bits to 1 allows writing to a register to be masked in byte units.

Note: When writing to the registers to which ByteM control at the WPR command cannot be applied, set 0000 to the ByteM bits at the WPR command.

**(6) JUMP**

**(a) Function**

Changes the display list fetch destination.

**(b) Command Format**

- REL = 0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OP CODE = 0010_1000								Reserved (all 0)								Draw mode															
0	0	0	JUMP address (longword address)														0	0													

- REL = 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OP CODE = 0010_1000								Reserved (all 0)								Draw mode															
Sign extended		Sign		JUMP address (longword address)														0		0											

**(c) Code**

B'00101000

**(d) Rendering Attributes**

Draw Mode															
b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	REL	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0

**(e) Command Parameter**

JUMP address:            Jump destination absolute address (Longword address. Write 0 to bits A31 to A29, A1, and A0.)  
                                  Jump destination relative address (Longword address. Negative numbers are expressed as two's complements. Bits A31 to A29 are used to extend the sign in bit A28. Write 0 to bits A1 and A0.)

Note: Even in 32-bit addressing mode, write the values in bits 28 to 3 of the specified 32-bit address to bits A28 to A3.

**(f) Description**

Changes the display list fetch destination to the specified address.

When REL = 0, the jump destination address can be specified as an absolute address. When REL = 1, the jump destination address can be specified as a relative address with respect to the memory address at which the command code is located.

(g) Example

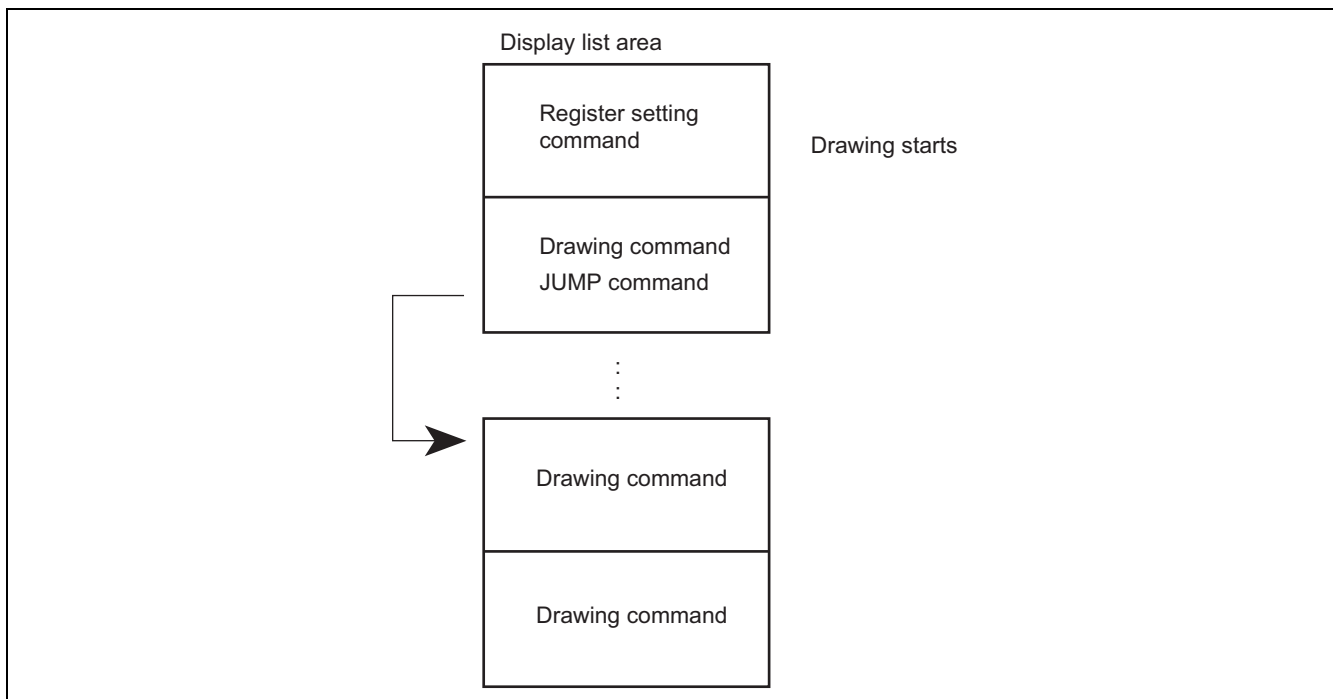


Figure 19.49 Example of JUMP Command Operation



**(7) GOSUB****(a) Function**

Makes a subroutine call for the display list.

**(b) Command Format**

- REL = 0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OP CODE = 0011_0000								Reserved (all 0)								Draw mode															
0	0	0	GOSUB address (longword address)														0	0													

- REL = 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OP CODE = 0011_0000								Reserved (all 0)								Draw mode															
Sign extended	Sign	GOSUB address (longword address)														0	0														

**(c) Code**

B'00110000

**(d) Rendering Attributes****Draw Mode**

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	REL	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	No	No

**(e) Command Parameter**

GOSUB address: Subroutine absolute address (Longword address. Write 0 to bits A31 to A29, A1, and A0.)  
 Subroutine relative address (Longword address. Negative numbers are expressed as two's complements. Bits A31 to A29 are used to extend the sign in bit A28. Write 0 to bits A1 and A0.)

Note: Even in 32-bit addressing mode, write the values in bits 28 to 3 of the specified 32-bit address to bits A28 to A3.

**(f) Description**

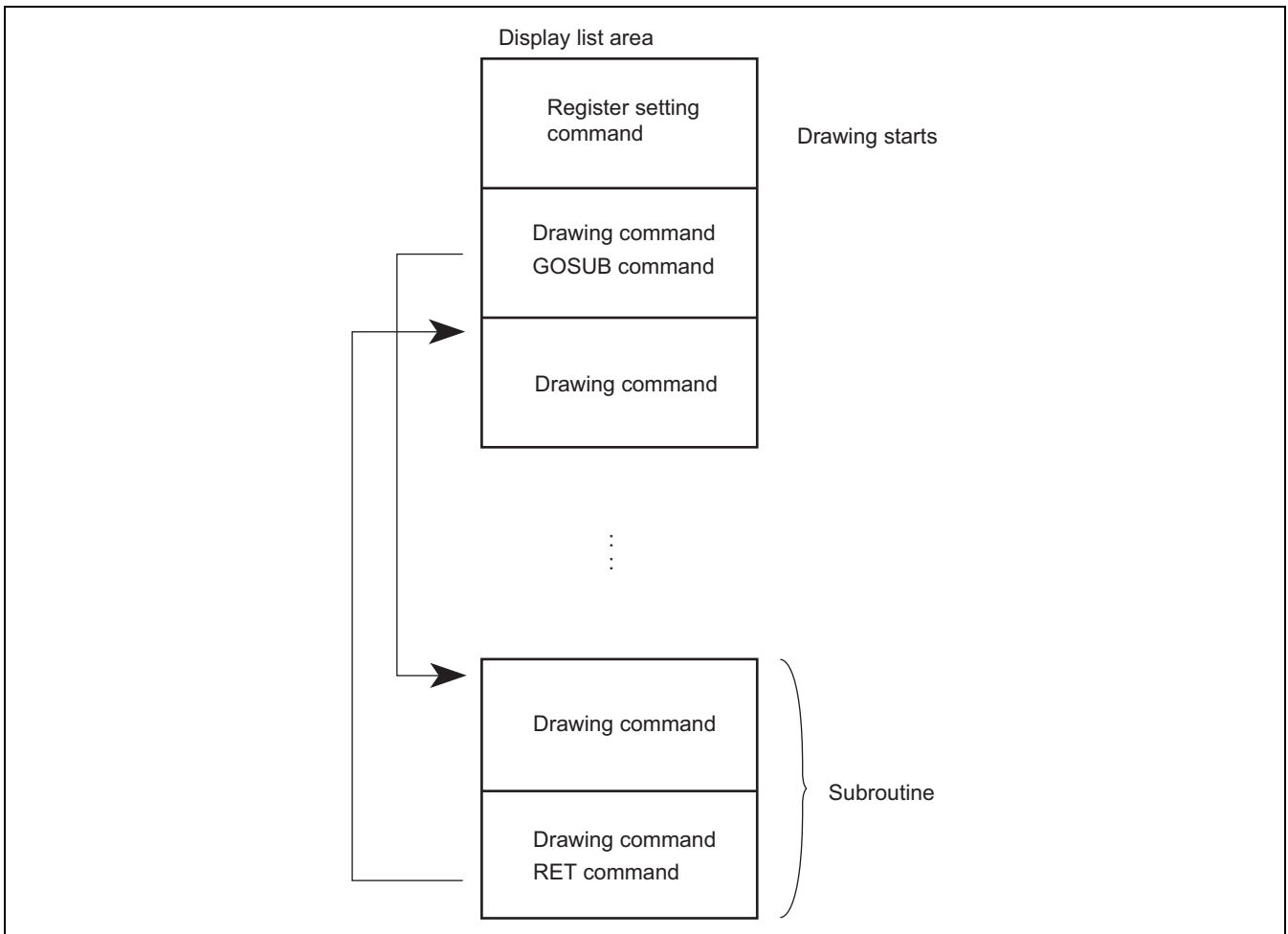
Changes the display list fetch destination to the specified subroutine address. The fetch address is restored by an RET instruction. As only one level of nesting is permitted, it will not be possible to return if a subroutine call is issued within the subroutine.

When REL = 0, the subroutine address can be specified as an absolute address. When REL = 1, the jump destination address can be specified as a relative address with respect to the memory address at which the command code is located.

When the No bit is 0, the return address is set in the return address 0 register (RTN0R). When the No bit is 1, the return address is set in the return address 1 register (RTN1R). When the No bit is 2, the return address is set in the return address STK register (RTNSTKR). When the No bit is 2, a maximum of eight levels of nesting are permitted.

Note: The GOSUB and RET commands should be appropriately allocated to prevent overflows or underflows in consideration that the maximum nesting level is eight. If an overflow or an underflow occurs, a hang up may be caused.

**(g) Example**



**Figure 19.50 Example of GOSUB Command Operation**

**(8) RET****(a) Function**

Returns from a subroutine call made by the GOSUB command.

**(b) Command Format**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OP CODE = 0011_1000								Reserved (all 0)								Draw mode															

**(c) Code**

B'00111000

**(d) Rendering Attributes**

Draw Mode															
b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	No	No

**(e) Description**

Restores the display list fetch destination to the address following the source of the subroutine call.

When the No bit is 0, the return address is set in the return address 0 register (RTN0R). When the No bit is 1, the return address is set in the return address 1 register (RTN1R). When the No bit is 2, the return address is set in the return address STK register (RTNSTKR).

**(9) NOP/INT****(a) Function**

Executes no operation.

**(b) Command Format**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OP CODE = 0000_1000								Reserved (all 0)								Draw mode															

**(c) Code**

B'00001000

**(d) Rendering Attributes**

Draw Mode																
b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0	
INT	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0								INT No	

**(e) Description**

This command does not perform any operation. This command simply fetches the next instruction. However when the INT bit is set to 1 in this command, after this command has been fetched, the INT bit in the status register (SR) is set to 1, INT No is saved in the interrupt command ID register (ICIDR), and the drawing operation is halted. Clearing the INT bit in the status register (SR) restarts the drawing operation from the next command.

**(10) VBKEM****(a) Function**

Performs synchronization with the frame change timing.

**(b) Command Format**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OP CODE = 0001_0000								Reserved (all 0)								Draw mode															

**(c) Code**

B'00010000

**(d) Rendering Attributes**

Draw Mode															
b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0

**(e) Description**

When this command is executed, the drawing operation is kept waiting until the timing for a frame change. As soon as the frame change timing has elapsed, control passes to the next command. The frame change timing is the next VSYNC in non-interlace mode display or interlace sync & video mode display, and the starting point of the next frame in interlace sync mode display.

Note: This command can only be used in manual display change mode or auto-rendering mode.

**(11) TRAP****(a) Function**

Informs the end of the display list.

**(b) Command Format**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OP CODE = 0000_0000								Reserved (all 0)								Draw mode															

**(c) Code**

B'00000000

**(d) Rendering Attributes**

Draw Mode															
b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Flip7	Flip6	Flip5	Flip4	Flip3	Flip2	Flip1	Flip0

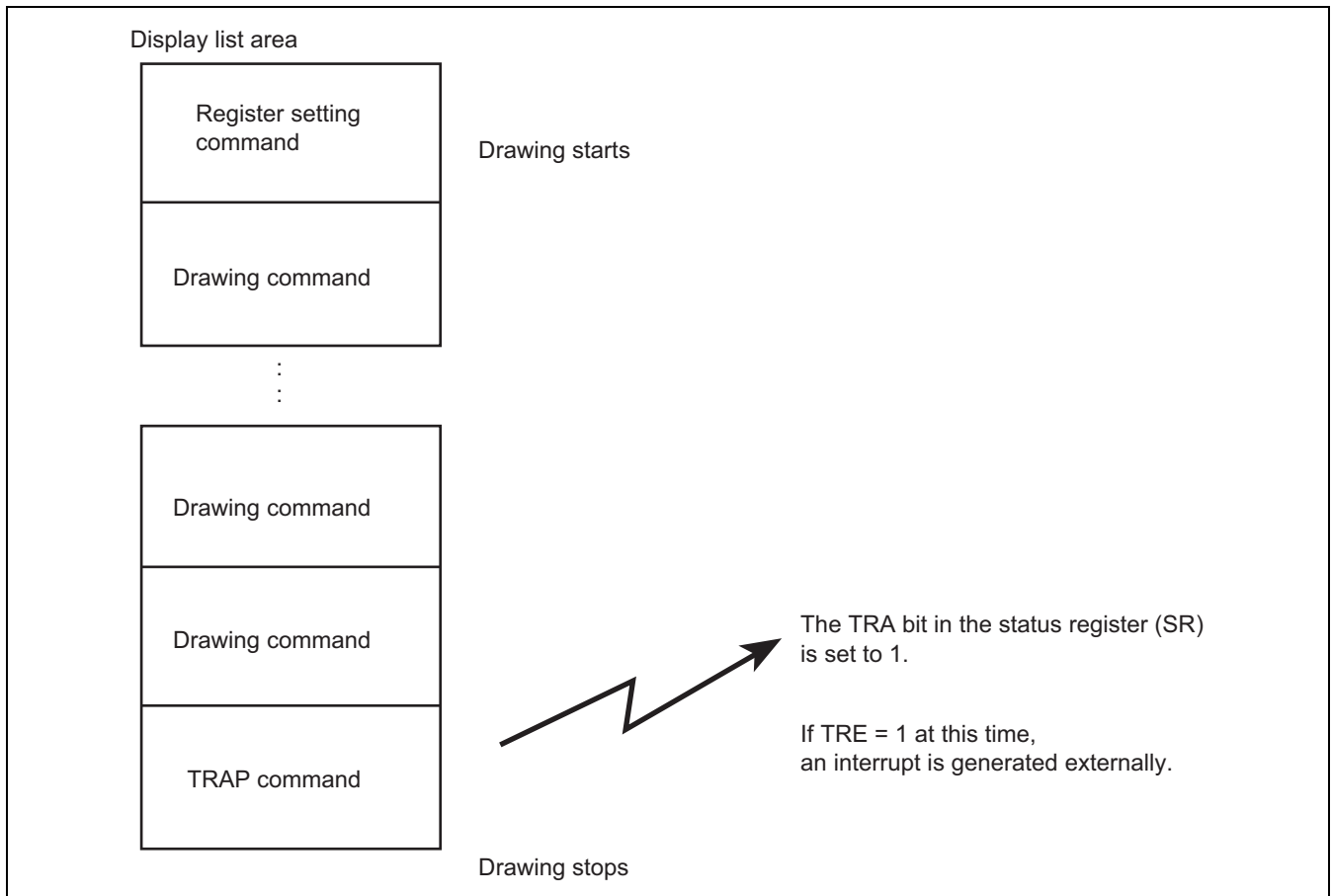
**(e) Description**

Halts the drawing operation and sets the TRA bit in the status register (SR) to 1. If the TRE bit in the interrupt enable register (IER) is set to 1, an interrupt is sent to the CPU.

This command must be placed at the end of the display list.

If the Flip7 to Flip0 bits are set, the corresponding plane is flipped (only valid in auto-rendering mode). The flip timing is the next VSYNC in non-interlace mode display or interlace sync & video mode display, and the starting point of the next frame in interlace sync mode display.

**(f) Example**



**Figure 19.51 Example of TRAP Command Operation**

**(12) SYNC****(a) Function**

Controls cache clearing/flushing.

**(b) Command Format**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OP CODE = 0001_0010								Reserved (all 0)								Draw mode															

**(c) Code**

B'00010010

**(d) Rendering Attributes**

Draw Mode															
b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0	WCLR	WFLSH	ACLR	Fixed to 0	Fixed to 0	TCLR	Fixed to 0	Fixed to 0	DCLR	DFLSH

**(e) Description**

SYNC is used to flush or clear cache data intentionally. When all of the rendering attributes are 0, NOP operation is performed.

1. When TCLR = 1, the source (texture) cache is cleared.
2. When DCLR = 1, the destination cache is cleared.
3. When DFLSH = 1, the destination cache is flushed.
4. When WCLR = 1, the work cache is cleared.
5. When WFLSH = 1, the work cache is flushed.
6. When ACLR = 1, the  $\alpha$  map cache is cleared.

- Notes:
1. All caches are cleared when rendering starts.
  2. When a TRAP, NOP (INT = 1), or VBKEM command is issued and a command error occurs, the destination cache and working cache are flushed, and the texture cache and  $\alpha$  map cache are cleared.
  3. For the destination cache and working cache, do not set both the cache clearing and flushing bits to 1 at the same time.



**(13) RGTOFS****(a) Function**

Adds RXOFS or RYOFS to a coordinate transformation offset.

**(b) Command Format**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OP CODE = 0110_0100										RXOFS ( $-2048 \leq \text{RXOFS} \leq 2047$ )										RYOFS ( $-2048 \leq \text{RYOFS} \leq 2047$ )											

**(c) Code**

B'01100100

**(d) Description**

This command is used to obtain a coordinate transformation offset value by adding RXOFS and RYOFS to the coordinate transformation offset (GTROFSX, GTROFSY).

- $\text{GTROFSX} = \text{GTROFSX} + \text{RXOFS}$
- $\text{GTROFSY} = \text{GTROFSY} + \text{RYOFS}$

After this command is set, the coordinate transformation offset value is added to the coordinates after the perspective W division for a drawing command which allows a coordinate transformation offset.

- Notes:
1. The results of this command addition are read from GTROFSXR and GTROFSYR.
  2. The addition results must satisfy the following condition because saturation processing is not performed:  
 $-32,768 \leq \text{GTROFSX}$  and  $\text{GTROFSY} \leq 32,767$ .

## 20. 3D Graphics Engine

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

### 20.1 Overview

The table below lists the graphics engine supported by each of RZ/G series products. See the relevant section for each product.

	GPU Core	Section
RZ/G1H	PowerVR Series6 G6400	20.2
RZ/G1M/N	PowerVR Series5-XT SGX544-MP2	20.3
RZ/G1E	PowerVR Series5 SGX540	20.4

This section only introduces the features of each 3D graphics engine. The graphics processing performed by each graphics engine is provided as the graphics driver software.

### 20.2 PowerVR Series6 G6400

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

The description of this section is quoted from the press release ‘Imagination announces first PowerVR Series6 GPU cores’ on January 10, 2012.

(<http://www.imgtec.com/news/Release/index.asp?NewsID=666>)

#### 20.2.1 Features of PowerVR Series6

PowerVR Series6 sets a new benchmark for high performance, ultra-low power GPU cores, scalable for markets from mobile and tablet to high end gaming and computing.

The innovative PowerVR Rogue architecture, on which Series6 is based, builds on the maturity and unrivalled success of the previous generations of PowerVR GPUs. It enables Imagination’s partners to deliver amazing user experiences in devices from innovative ‘natural’ user interfaces to ultra-realistic gaming, as well as enabling new applications never before thought of from advanced content creation and image processing to sophisticated augmented reality and environment-aware solutions.

Based on a scalable number of compute clusters the PowerVR Rogue architecture is designed to target the requirements of a growing range of demanding markets from mobile to the highest performance embedded graphics including smartphones, tablets, PC, console, DTV and other Rich Graphics Applications. Compute clusters are arrays of programmable computing elements that are designed to offer high performance and efficiency while minimizing power and bandwidth requirements. The PowerVR G6400 has four compute clusters.

#### 20.2.2 Register Base Address

Base address of registers is allocated to H'00\_FD00\_0000.

## 20.3 PowerVR Series5-XT SGX544MP2

RZ/G1H	RZ/G1N
RZ/G1M	RZ/G1E

The description of this section is quoted from 'POWERVR SGX Series5XT Factsheet'.

([http://www.imgtec.com/factsheets/powervr/PowerVR\\_SGX\\_Series5XT\\_IP\\_Core\\_Family\\_\[3.2\].pdf](http://www.imgtec.com/factsheets/powervr/PowerVR_SGX_Series5XT_IP_Core_Family_[3.2].pdf))

### 20.3.1 Features of POWERVR SGX Series5XT

The POWERVR SGX Series5XT GPU IP core family is a series of highly efficient graphics acceleration IP cores that meet the multimedia requirements of the next generation of consumer, communications and computing applications.

POWERVR SGX Series5XT architecture is fully scalable for a wide range of area and performance requirements, enabling it to target markets from low cost feature-rich mobile multimedia products to very high performance consoles and computing devices.

The family incorporates the second-generation Universal Scalable Shader Engine (USSE2), with a feature set that exceeds the requirements of OpenGL 2.0 and Microsoft Shader Model 3, enabling 2D, 3D and general purpose (GP-GPU) processing in a single core.

- Most comprehensive IP core family and roadmap in the industry
- USSE2 delivers twice the peak floating point and instruction throughput of Series5 USSE
- YUV and color space accelerators for improved performance
- Upgraded POWERVR Series5XT shader-driven tile-based deferred rendering (TBDR) architecture
- Multi-processor options enable scalability to higher performance
- Support for all industry standard mobile and desktop graphics APIs and operating systems
- Fully backwards compatible with POWERVR MBX and SGX Series5

### 20.3.2 Register Base Address

Base address of registers is allocated to H'FD80\_0000.

## 20.4 PowerVR Series5 SGX540

RZ/G1H	RZ/G1N
RZ/G1M	<b>RZ/G1E</b>

The description of this section is quoted from 'POWERVR SGX Series5 Factsheet'.

(PowerVR\_SGX\_Series5\_IP\_Core\_Family\_[3.4].pdf, available at [www.imgtec.com](http://www.imgtec.com)).

### 20.4.1 Features of POWERVR SGX Series5

The POWERVR SGX Series5 GPU IP core family is a series of highly efficient graphics acceleration IP cores that meet the multimedia requirements of the next generation of consumer, communications and computing applications.

POWERVR SGX Series5 architecture is fully scalable for a wide range of area and performance requirements, enabling it to target markets from low cost feature-rich mobile multimedia products to very high performance consoles and computing devices.

The family incorporates the revolutionary Universal Scalable Shader Engine (USSE), with a feature set that exceeds the requirements of OpenGL 2.0 and Microsoft Shader Model 3, enabling 2D, 3D and general purpose (GP-GPU) processing in a single core.

- Most comprehensive IP core family and roadmap in the industry
- Series5 shader-driven tile-based deferred rendering (TBDR) architecture
- Fully programmable GPU using unique USSE architecture
- Support for all industry standard mobile and desktop graphics APIs and operating systems
- Fully backwards compatible with PowerVR MBX

### 20.4.2 Register Base Address

See section 20.3.2, Register Base Address.

## 21. Display Unit (DU)

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

### 21.1 Overview

#### 21.1.1 Features

##### (1) Display Channel

Three\*<sup>1</sup>/Two\*<sup>2</sup> independently controllable channels are provided. Using the DU0 and DU1, different images or the same image can be displayed on two monitors.

Notes: 1. Only for RZ/G1H  
2. For RZ/G1M/N/E

##### (2) Plane

The display surfaces normally called the foreground, background, and cursor, are called planes in this section. Parameters for each plane can be set independently through the settings of an internal register. The internal register settings can also be used to set the display priority order.

- Display size
- Display position
- Display data format (8-bit/pixel, 16-bit/pixel, 32-bit/pixel, ARGB, or YC)
- Plane superpositioning
- Scrolling
- Wrapping-around
- Blinking
- Buffering control

The internal register settings can be used to select four different control modes.

- Auto rendering mode (double buffering)
- Manual display change mode (double buffering)
- Auto display change mode (double buffering)
- Video capture mode (triple buffering)

##### (3) Type and Number of Planes

In the DU0 or DU1 and the DU2\*<sup>1</sup>, there are eight planes (display planes) available, each using both image data and an alpha ratio. Also, there are two special planes (alpha-ratio planes) available, each using only an alpha ratio.

Up to eight display planes can be superposed on each other. Correspondences between the DU0 and DU1 planes are not fixed but can be selected as desired through register settings.

For the number of planes which can be used at the same time, refer to the description in section 1, Overview.

Notes: 1. Only for RZ/G1H

#### (4) Synchronization Method

Internal register settings can be used to select any of three synchronization modes for the display output timing.

- Master mode (internal sync mode)
- TV sync mode (external sync mode)
- Sync method switching mode

#### (5) CRT Scan Mode (CRT Scan Method)

Internal register settings can be used to select from among three scan modes.

- Non-interlaced mode
- Interlaced sync mode
- Interlaced sync & video mode

#### (6) YC → RGB Color Space Conversion Functions

Image data stored in YC format can be converted into the RGB color space and displayed in a window. The conversion coefficients can be set in a register.

However, data for two or more pixels cannot be converted into the RGB color space at the same time.

Data in YUV422 and YUV420 format are convertible into the RGB color space.

#### (7) RBG → YC Color Space Conversion Functions [RZ/G1M/N/E]

Display data superposed in RGB format can be converted into the YC color space and output from the DU0 pin as the YC data.

#### (8) Color Palette

Eight\*<sup>1</sup> /Four\*<sup>2</sup> internal color palette planes are provided, capable of simultaneously displaying 256 colors out of 262 thousand colors

Eight-bit blending ratios are provided for every 256 colors. The color palettes are only accessible by superposition processors 0 and 2\*<sup>1</sup>.

Notes: 1. Only for RZ/G1H  
2. For RZ/G1M/N/E

#### (9) Display Capture

The RGB-888 or RGB-666 data for output on the three\*<sup>1</sup>/two\*<sup>2</sup> display channels is convertible into ARGB-888 or RGB-565 or ARGB-1555 data for separate storage in external memory.

Notes: 1. Only for RZ/G1H  
2. For RZ/G1M/N/E

#### (10) Register Access Control

The module has internal control registers; these are writable/readable by the APB protocol over the APB. The unit of access is fixed to 32 bits.

#### (11) DRC Connection [RZ/G1H]

Connection with the DRC allows the contrast correction of image data, superimposed data, or display data. To apply the correction, select the DU0, DU1 or DU2.

Connection with the DRC allows contrast correction of the image data, superposed data, or display data separately for each channel.

**(12) VSP1 Connection**

Connection with the VSP1 allows the image data processed by the VSP1 to be output directly to the display unit without an external memory. VSP1-ch0 has been connected with plane 1 for the DU0 or DU1, VSP1-ch1 has been connected with either plane 2 for DU0 or DU1 or plane 1 for the DU2\*<sup>1</sup>. VSP1-ch0 has been connected with plane 1 for the DU0 or DU1, VSP1-ch1 has been connected with plane 2 for the DU0 or DU1\*<sup>2</sup>. VSP1-ch0 has been connected with plane 1 for the DU0 or DU1\*<sup>3</sup>.

Notes: 1. Only for RZ/G1H  
2. For RZ/G1M/N  
3. Only for RZ/G1E

**(13) LVDS Connection [RZ/G1H/M/N]**

Connection with the LVDS allows the output of image data from the LVDS. The DU0 has been connected with the LVDS, for the DU1 and DU2, either one should be selected for connection\*<sup>1</sup>. The DU0 has been connected with the LVDS\*<sup>2</sup>.

Notes: 1. Only for RZ/G1H  
2. For RZ/G1M/N

**(14) DPAD Connection**

Connection with the DPAD allows the output of the digital RGB data from a pin.

To output the RGB data, select the DU0, DU1 or DU2\*<sup>1</sup>. Either DU0 or DU1 is chosen and outputted\*<sup>2</sup>.

Connection with the DPAD allows the output of the digital RGB data from a pin separately for each channel\*<sup>3</sup>.

Notes: 1. Only for RZ/G1H  
2. For RZ/G1M/N  
3. Only for RZ/G1E

21.1.2 Block Diagram

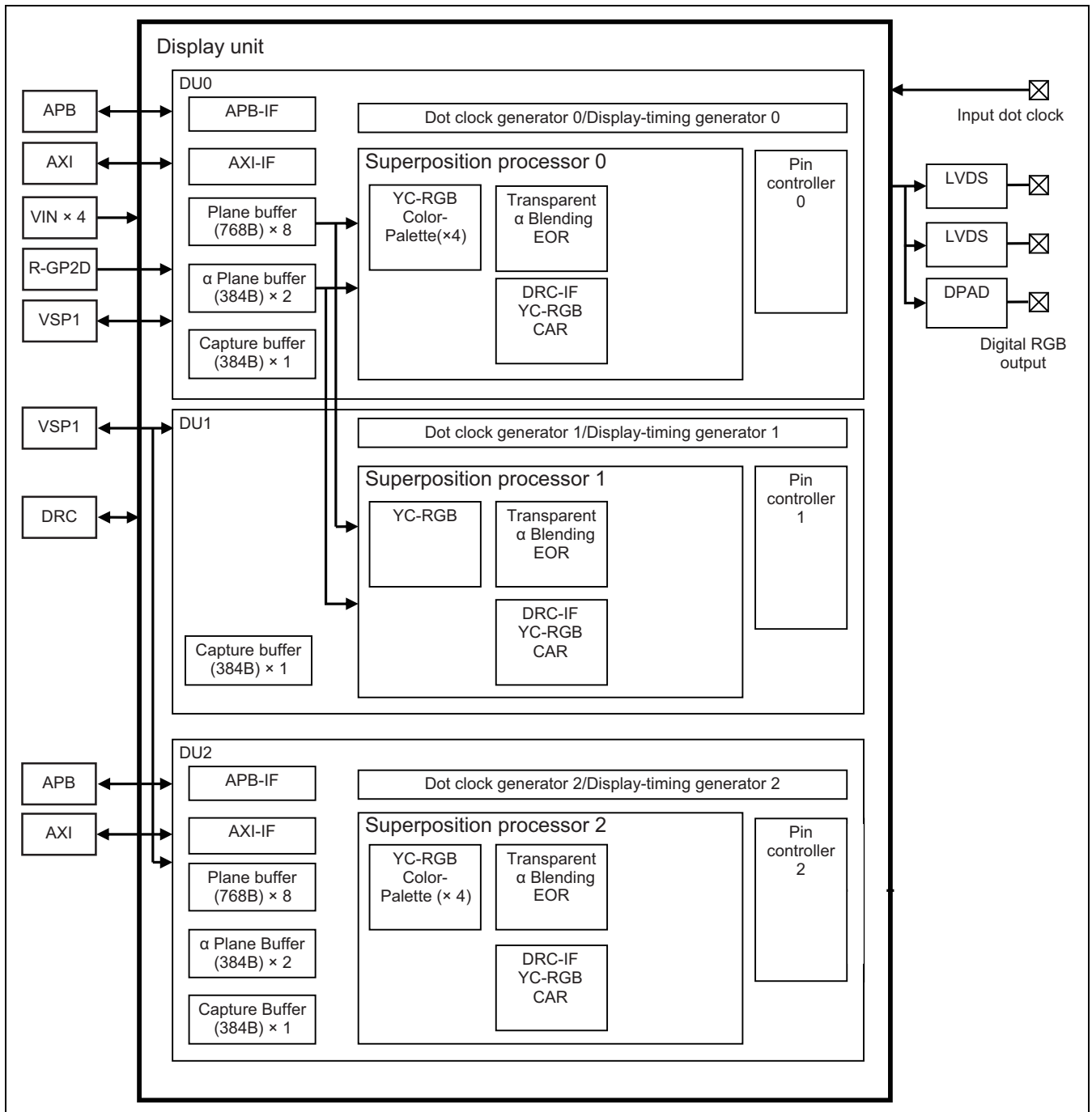


Figure 21.1a Block Diagram of the Display Unit (DU) [RZ/G1H]



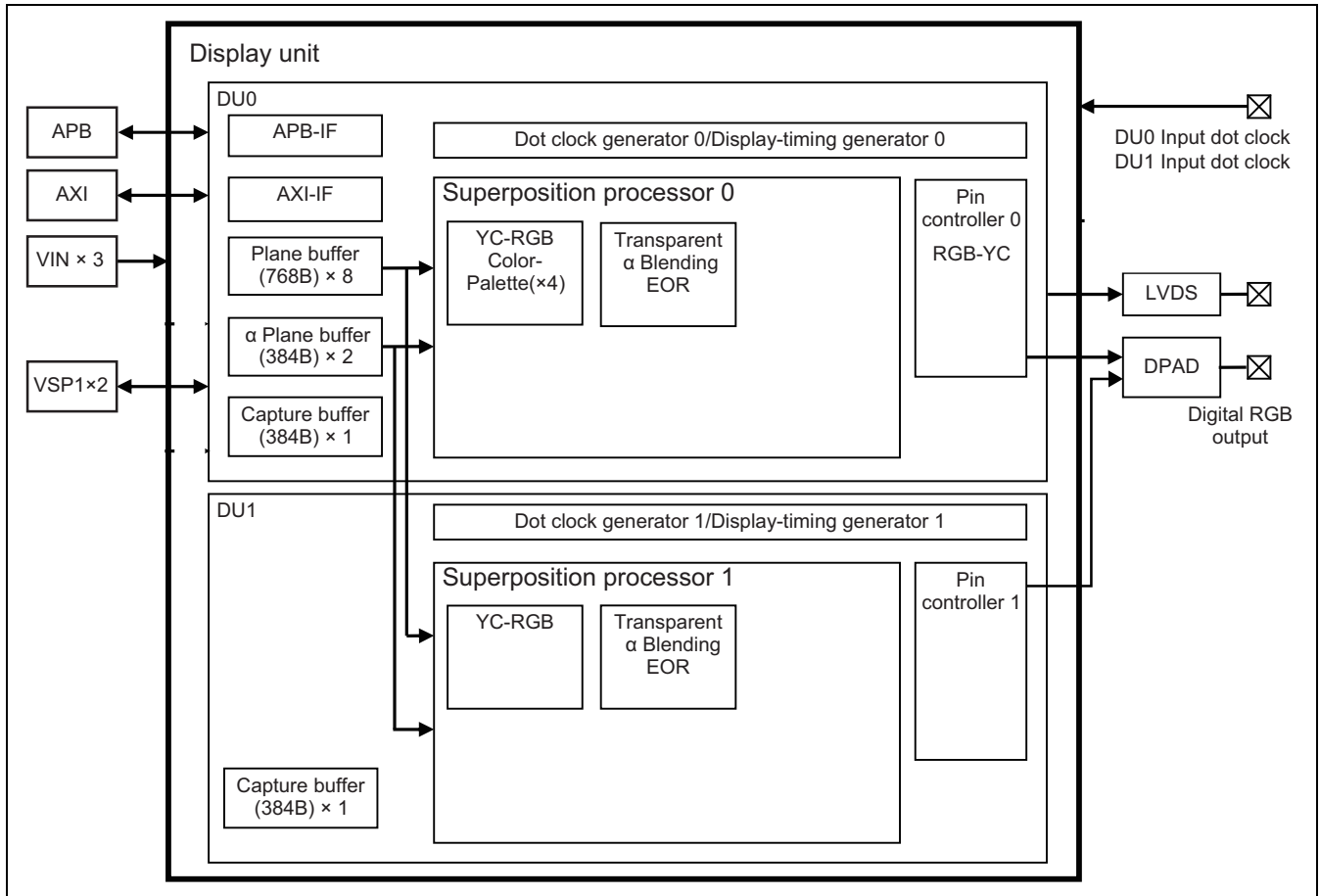


Figure 21.1b Block Diagram of the Display Unit (DU) [RZ/G1M/N]

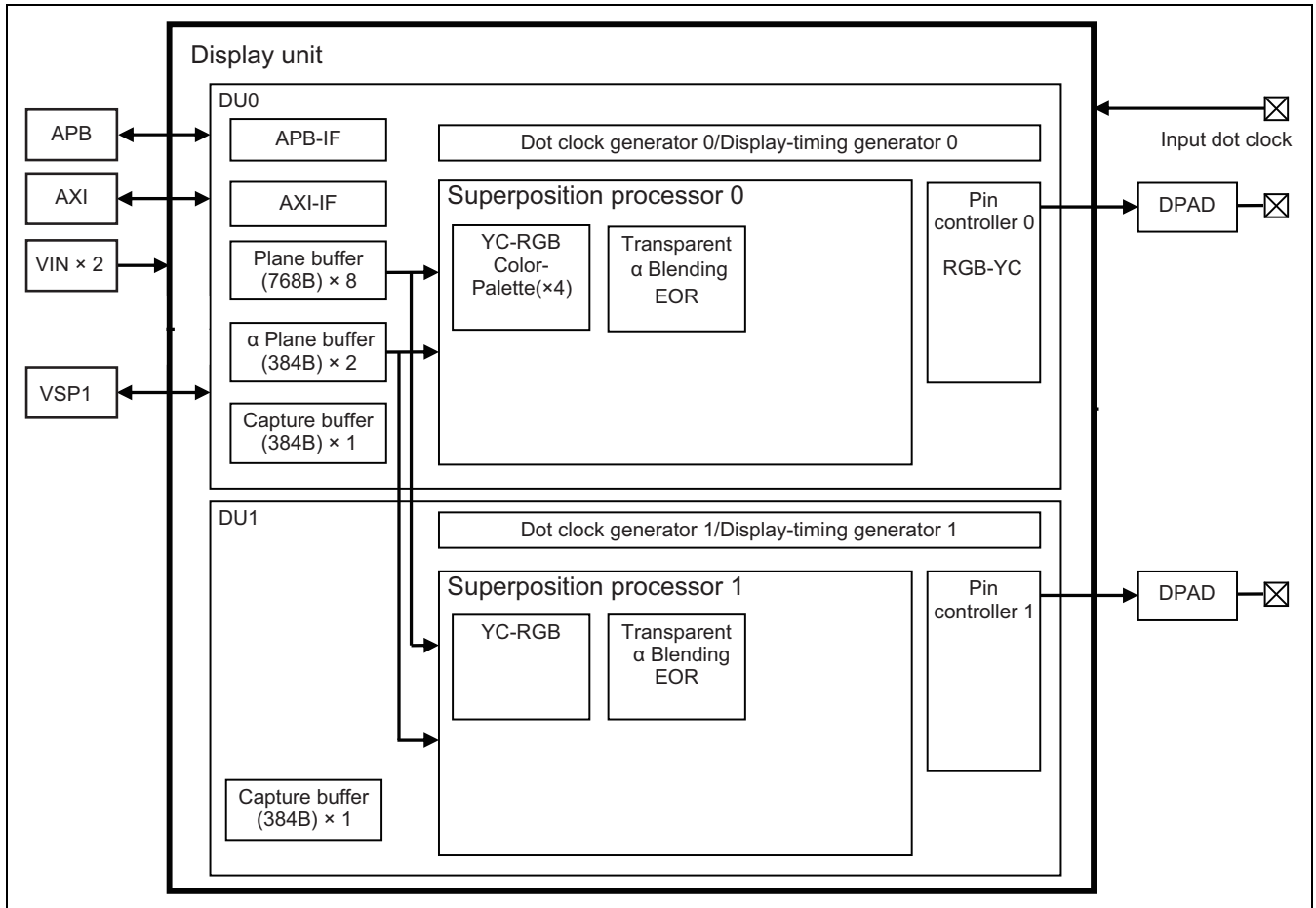


Figure 21.1c Block Diagram of the Display Unit (DU) [RZ/G1E]

### 21.1.3 Input/Output Pins

**Table 21.1a Pin Functions (DU0/DU1/DU2 [RZ/G1H], DU0/DU1 [RZ/G1M/N])**

Name	Pin Name	I/O	Function	Signal Name Used in This Section
DU0 input dot clock	DU_DOTCLKIN0 [ RZ/G1H ]	Input	DU0 input dot clock (Initial value) DU1 input dot clock DU2 input dot clock	DCLKIN
	DU0_DOTCLKIN [ RZ/G1M/N ]		DU0 input dot clock (Initial value) DU1 input dot clock	
DU1 input dot clock	DU_DOTCLKIN1 [ RZ/G1H ]	Input	DU0 input dot clock DU1 input dot clock (Initial value) DU2 input dot clock	DCLKIN
	DU1_DOTCLKIN [ RZ/G1M/N ]		DU0 input dot clock DU1 input dot clock (Initial value)	
DU2 input dot clock [ RZ/G1H ]	DU_DOTCLKIN2	Input	DU0 input dot clock DU1 input dot clock DU2 input dot clock (Initial value)	DCLKIN
DU output dot clock 0	DU_DOTCLKOUT0 [ RZ/G1H ]	Output	DU0 output dot clock (normal phase) (Initial value) DU1 output dot clock (normal phase) DU2 output dot clock (normal phase)	DCLKOUT
	DU1_DOTCLKOUT0 [ RZ/G1M/N ]		DU0 output dot clock (normal phase) (Initial value) DU1 output dot clock (normal phase)	
DU output dot clock 1	DU_DOTCLKOUT1 [ RZ/G1H ]	Output	DU0 output dot clock (counter phase) (Initial value) DU1 output dot clock (counter phase) DU2 output dot clock (counter phase)	DCLKOUTB
	DU1_DOTCLKOUT1 [ RZ/G1M/N ]		DU0 output dot clock (counter phase) (Initial value) DU1 output dot clock (counter phase)	

Name	Pin Name	I/O	Function	Signal Name Used in This Section
DU external horizontal synchronous output/DU horizontal synchronous input	DU_EXHSYNC/ DU_HSYNC	I/O	DU0 composite synchronous output signal (Initial value)	CSYNC
	[ RZ/G1H ]		DU1 composite synchronous output signal	
	DU1_EXHSYNC/ DU1_HSYNC		DU2 composite synchronous output signal [ RZ/G1H ]	
	[ RZ/G1M/N ]		DU0 horizontal synchronous output/DU0 external horizontal synchronous input	
DU external vertical synchronous output/DU vertical synchronous output	DU_EXVSYNC/ DU_VSYNC	I/O	DU0 vertical synchronous output/ DU0 external vertical synchronous input (Initial value)	VSYNC or EXVSYNC*1
	[ RZ/G1H ]		DU1 vertical synchronous output/ DU1 external vertical synchronous input	
	DU1_EXVSYNC/ DU1_VSYNC		DU2 vertical synchronous output/ DU2 external vertical synchronous input [ RZ/G1H ]	
	[ RZ/G1M/N ]		DU0 composite synchronous output signal	
DU odd/even field	DU_EXODDF/ DU_ODDF/ DISP/ CDE	I/O	DU0 odd/even field (Initial value)	ODDF or EXODDF*1
	[ RZ/G1H ]		DU1 odd/even field	
	DU1_EXODDF/ DU1_ODDF/ DISP/ CDE		DU2 odd/even field [ RZ/G1H ]	
	[ RZ/G1M/N ]		DU0 CLAMP output signal	
DU odd/even field	DU1_EXODDF/ DU1_ODDF/ DISP/ CDE	I/O	DU1 CLAMP output signal	CLAMP
	[ RZ/G1M/N ]		DU2 CLAMP output signal [ RZ/G1H ]	
	DU0 display interval		DISP	
	DU1 display interval		DISP	
DU odd/even field	DU1_EXODDF/ DU1_ODDF/ DISP/ CDE	I/O	DU2 display interval [ RZ/G1H ]	DISP
	[ RZ/G1M/N ]		DU0 color detection	
	DU0 color detection		CDE	
	DU1 color detection		CDE	
DU odd/even field	DU1_EXODDF/ DU1_ODDF/ DISP/ CDE	I/O	DU2 color detection [ RZ/G1H ]	CDE
	[ RZ/G1M/N ]		DU0 color detection	
	DU0 color detection		CDE	
	DU1 color detection		CDE	

Name	Pin Name	I/O	Function	Signal Name Used in This Section
DU display interval	DU_DISP [ RZ/G1H ]	Output	DU0 display interval (Initial value)	DISP
			DU1 display interval	
			DU2 display interval [ RZ/G1H ]	
DU color detection	DU1_DISP [ RZ/G1M/N ]	Output	DU0 composite synchronous output signal	CSYNC
			DU1 composite synchronous output signal	
			DU2 composite synchronous output signal [ RZ/G1H ]	
			DU0 DE output signal	
DU1 DE output signal				
DU2 DE output signal [ RZ/G1H ]				
DU color detection	DU_CDE [ RZ/G1H ]	Output	DU0 color detection (Initial value)	CDE
			DU1 color detection	
			DU2 color detection [ RZ/G1H ]	
	DU1_CDE [ RZ/G1M/, N ]			

Name	Pin Name	I/O	Function	Signal Name Used in This Section
DU display data	DU_DR0 [ RZ/G1H ]	Output	DU0 digital red 0/green 4	Digital RGB [RZ/G1H ] Digital RGB or YC [ RZ/G1M/N ]*5
	DU1_DR0 [ RZ/G1M/N ]		DU1 digital red 0 DU2 digital red 0/green 4	
	DU_DR1 [ RZ/G1H ]	Output	DU0 digital red 0/green 4	
	DU1_DR1 [ RZ/G1M/N ]		DU1 digital red 0/green 4	
	DU_DR2 [ RZ/G1H ]	Output	DU0 digital red 1/green 5	
	DU1_DR2 [ RZ/G1M/N ]		DU1 digital red 1 DU2 digital red 1/green 5	
	DU_DR3 [ RZ/G1H ]	Output	DU0 digital red 1/green 5	
	DU1_DR3 [ RZ/G1M/N ]		DU1 digital red 1/green 5	
	DU_DR4 [ RZ/G1H ]	Output	DU0 digital red 2/green 6	
	DU1_DR4 [ RZ/G1M/N ]		DU1 digital red 2 DU2 digital red 2/green 6	
	DU_DR5 [ RZ/G1H ]	Output	DU0 digital red 2/green 6	
	DU1_DR5 [ RZ/G1M/N ]		DU1 digital red 2/green 6	
	DU_DR6 [ RZ/G1H ]	Output	DU0 digital red 3/green 7	
	DU1_DR6 [ RZ/G1M/N ]		DU1 digital red 3 DU2 digital red 3/green 7	
	DU_DR7 [ RZ/G1H ]	Output	DU0 digital red 3/green 7	
	DU1_DR7 [ RZ/G1M/N ]		DU1 digital red 3/green 7	
	DU_DR8 [ RZ/G1H ]	Output	DU0 digital red 4/blue 0	
	DU1_DR8 [ RZ/G1M/N ]		DU1 digital red 4 DU2 digital red 4/blue 0	
	DU_DR9 [ RZ/G1H ]	Output	DU0 digital red 4/blue 0	
	DU1_DR9 [ RZ/G1M/N ]		DU1 digital red 4/blue 0	
	DU_DR10 [ RZ/G1H ]	Output	DU0 digital red 5/blue 1	
	DU1_DR10 [ RZ/G1M/N ]		DU1 digital red 5 DU2 digital red 5/blue 1	
	DU_DR11 [ RZ/G1H ]	Output	DU0 digital red 5/blue 1	
	DU1_DR11 [ RZ/G1M/N ]		DU1 digital red 5/blue 1	
	DU_DR12 [ RZ/G1H ]	Output	DU0 digital red 6/blue 2	
	DU1_DR12 [ RZ/G1M/N ]		DU1 digital red 6 DU2 digital red 6/blue 2	
	DU_DR13 [ RZ/G1H ]	Output	DU0 digital red 6/blue 2	
	DU1_DR13 [ RZ/G1M/N ]		DU1 digital red 6/blue 2	
	DU_DR14 [ RZ/G1H ]	Output	DU0 digital red 7/blue 3	
	DU1_DR14 [ RZ/G1M/N ]		DU1 digital red 7 DU2 digital red 7/blue 3	
	DU_DR15 [ RZ/G1H ]	Output	DU0 digital red 7/blue 3	
	DU1_DR15 [ RZ/G1M/N ]		DU1 digital red 7/blue 3	

Name	Pin Name	I/O	Function	Signal Name Used in This Section
DU display data	DU_DG0	Output	DU0 digital green 0/blue 4	Digital RGB [RZ/G1H ]
	[ RZ/G1H ]		DU1 digital green 0	Digital RGB or YC [ RZ/G1M/N ]*5
	DU1_DG0		DU0 digital green 0/blue 4	
	[ RZ/G1M/N ]		DU1 digital green 0/blue 4	
	DU_DG1	Output	DU0 digital green 1/blue 5	
	[ RZ/G1H ]		DU1 digital green 1	
	DU1_DG1		DU0 digital green 1/blue 5	
	[ RZ/G1M/N ]		DU1 digital green 1/blue 5	
	DU_DG2	Output	DU0 digital green 2/blue 6	
	[ RZ/G1H ]		DU1 digital green 2	
	DU1_DG2		DU0 digital green 2/blue 6	
	[ RZ/G1M/N ]		DU1 digital green 2/blue 6	
	DU_DG3	Output	DU0 digital green 3/blue 7	
	[ RZ/G1H ]		DU1 digital green 3	
	DU1_DG3		DU0 digital green 3/blue 7	
	[ RZ/G1M/N ]		DU1 digital green 3/blue 7	
	DU_DG4	Output	DU0 digital green 4	
	[ RZ/G1H ]		DU1 digital green 4	
	DU1_DG4		DU0 digital green 4	
	[ RZ/G1M/N ]		DU1 digital green 4	
	DU_DG5	Output	DU0 digital green 5	
	[ RZ/G1H ]		DU1 digital green 5	
	DU1_DG5		DU0 digital green 5	
	[ RZ/G1M/N ]		DU1 digital green 5	
	DU_DG6	Output	DU0 digital green 6	
	[ RZ/G1H ]		DU1 digital green 6	
	DU1_DG6		DU0 digital green 6	
	[ RZ/G1M/N ]		DU1 digital green 6	
	DU_DG7	Output	DU0 digital green 7	
	[ RZ/G1H ]		DU1 digital green 7	
	DU1_DG7		DU0 digital green 7	
	[ RZ/G1M/N ]		DU1 digital green 7	

Name	Pin Name	I/O	Function	Signal Name Used in This Section
DU display data	DU_DB0	Output	DU0 digital blue 0	Digital RGB [RZ/G1H ]
	[ RZ/G1H ]		DU1 digital blue 0	Digital RGB or YC [ RZ/G1M/N ]*5
	DU1_DB0		DU0 digital blue 0	
	[ RZ/G1M/N ]		DU1 digital blue 0	
	DU_DB1	Output	DU0 digital blue 1	
	[ RZ/G1H ]		DU1 digital blue 1	
	DU1_DB1		DU0 digital blue 1	
	[ RZ/G1M/N ]		DU1 digital blue 1	
	DU_DB2	Output	DU0 digital blue 2	
	[ RZ/G1H ]		DU1 digital blue 2	
	DU1_DB2		DU0 digital blue 2	
	[ RZ/G1M/N ]		DU1 digital blue 2	
	DU_DB3	Output	DU0 digital blue 3	
	[ RZ/G1H ]		DU1 digital blue 3	
	DU1_DB3		DU0 digital blue 3	
	[ RZ/G1M/N ]		DU1 digital blue 3	
	DU_DB4	Output	DU0 digital blue 4	
	[ RZ/G1H ]		DU1 digital blue 4	
	DU1_DB4		DU0 digital blue 4	
	[ RZ/G1M/N ]		DU1 digital blue 4	
	DU_DB5	Output	DU0 digital blue 5	
	[ RZ/G1H ]		DU1 digital blue 5	
	DU1_DB5		DU0 digital blue 5	
	[ RZ/G1M/N ]		DU1 digital blue 5	
	DU_DB6	Output	DU0 digital blue 6	
	[ RZ/G1H ]		DU1 digital blue 6	
	DU1_DB6		DU0 digital blue 6	
	[ RZ/G1M/N ]		DU1 digital blue 6	
	DU_DB7	Output	DU0 digital blue 7	
	[ RZ/G1H ]		DU1 digital blue 7	
	DU1_DB7		DU0 digital blue 7	
	[ RZ/G1M/N ]		DU1 digital blue 7	

Notes: 1. These are expressed as EXHSYNC, EXVSYNC, and EXODDF in explanations of the functions as input signals and as HSYNC, VSYNC and ODDF otherwise.

2. When DU0 and DU1 are output at the same time, DU0 and DU1 are output in synchronization with rising and falling edges of the dot clock, respectively.



3. Synchronization for the output of digital 0 only is in accord with the setting of the output signal timing adjustment register m (OTARm). m = 0 to 2 for RZ/G1H, m = 0 and 1 for RZ/G1M/N.
4. In this section, unless otherwise noted, "dot clock" refers to the output dot clock.
5. In YC format display, please refer to Table 21.39a. [RZ/G1M/N]

**Table 21.1b Pin Functions (DU0 [RZ/G1E])**

Name	Pin Name	I/O	Function	Signal Name Used in This Section
DU0 input dot clock	DU0_DOTCLKIN	Input	DU0 input dot clock (Initial value) DU1 input dot clock	DCLKIN
DU0 output dot clock 0	DU0_DOTCLKOUT0	Output	DU0 output dot clock (normal phase)	DCLKOUT
DU0 output dot clock 1	DU0_DOTCLKOUT1	Output	DU0 output dot clock (counter phase)	DCLKOUTB
DU0 external horizontal synchronous output/DU0 horizontal synchronous input	DU0_EXHSYNC/ DU0_HSYNC	I/O	DU0 composite synchronous output signal DU0 horizontal synchronous output/DU0 external horizontal synchronous input	CSYNC HSYNC or EXHSYNC* <sup>1</sup>
DU0 external vertical synchronous output/DU0 vertical synchronous output	DU0_EXVSYNC/ DU0_VSYNC	I/O	DU0 vertical synchronous output/ DU0 external vertical synchronous input DU0 composite synchronous output signal	VSYNC or EXVSYNC* <sup>1</sup> CSYNC
DU0 odd/even field	DU0_EXODDF/ DU0_ODDF/ DISP/ CDE	I/O	DU0 odd/even field DU0 CLAMP output signal DU0 display interval DU0 color detection	ODDF or EXODDF* <sup>1</sup> CLAMP DISP CDE
DU0 display interval	DU0_DISP	Output	DU0 display interval DU0 composite synchronous output signal DU0 DE output signal	DISP CSYNC DE
DU0 color detection	DU0_CDE	Output	DU0 color detection	CDE

Name	Pin Name	I/O	Function	Signal Name Used in This Section
DU0 display data	DU0_DR0	Output	DU0 digital red 0/green 4 DU1 digital red 0	Digital RGB or YC* <sup>5</sup>
	DU0_DR1	Output	DU0 digital red 1/green 5 DU1 digital red 1	
	DU0_DR2	Output	DU0 digital red 2/green 6 DU1 digital red 2	
	DU0_DR3	Output	DU0 digital red 3/green 7 DU1 digital red 3	
	DU0_DR4	Output	DU0 digital red 4/blue 0 DU1 digital red 4	
	DU0_DR5	Output	DU0 digital red 5/blue 1 DU1 digital red 5	
	DU0_DR6	Output	DU0 digital red 6/blue 2 DU1 digital red 6	
	DU0_DR7	Output	DU0 digital red 7/blue 3 DU1 digital red 7	
	DU0_DG0	Output	DU0 digital green 0/blue 4 DU1 digital green 0	
	DU0_DG1	Output	DU0 digital green 1/blue 5 DU1 digital green 1	
	DU0_DG2	Output	DU0 digital green 2/blue 6 DU1 digital green 2	
	DU0_DG3	Output	DU0 digital green 3/blue 7 DU1 digital green 3	
	DU0_DG4	Output	DU0 digital green 4 DU1 digital green 4	

Name	Pin Name	I/O	Function	Signal Name Used in This Section
DU0 display data	DU0_DG5	Output	DU0 digital green 5 DU1 digital green 5	Digital RGB or YC*5
	DU0_DG6	Output	DU0 digital green 6 DU1 digital green 6	
	DU0_DG7	Output	DU0 digital green 7 DU1 digital green 7	
	DU0_DB0	Output	DU0 digital blue 0 DU1 digital blue 0	
	DU0_DB1	Output	DU0 digital blue 1 DU1 digital blue 1	
	DU0_DB2	Output	DU0 digital blue 2 DU1 digital blue 2	
	DU0_DB3	Output	DU0 digital blue 3 DU1 digital blue 3	
	DU0_DB4	Output	DU0 digital blue 4 DU1 digital blue 4	
	DU0_DB5	Output	DU0 digital blue 5 DU1 digital blue 5	
	DU0_DB6	Output	DU0 digital blue 6 DU1 digital blue 6	
DU0_DB7	Output	DU0 digital blue 7 DU1 digital blue 7		

- Notes:
1. These are expressed as EXHSYNC, EXVSYNC, and EXODDF in explanations of the functions as input signals and as HSYNC, VSYNC and ODDF otherwise.
  2. When DU0 and DU1 are output at the same time, DU0 and DU1 are output in synchronization with rising and falling edges of the dot clock, respectively.
  3. Synchronization for the output of digital 0 only is in accord with the setting of the output signal timing adjustment register 0 (OTAR0).
  4. In this section, unless otherwise noted, "dot clock" refers to the output dot clock.
  5. In YC format display, please refer to Table 21.39b.

**Table 21.1c Pin Functions (DU1 [RZ/G1E])**

<b>Name</b>	<b>Pin Name</b>	<b>I/O</b>	<b>Function</b>	<b>Signal Name Used in This Section</b>
DU1 input dot clock	DU1_DOTCLKIN	Input	DU0 input dot clock DU1 input dot clock (Initial value)	DCLKIN
DU1 output dot clock 0	DU1_DOTCLKOUT0	Output	DU1 output dot clock (normal phase)	DCLKOUT
DU1 output dot clock 1	DU1_DOTCLKOUT1	Output	DU1 output dot clock (counter phase)	DCLKOUTB
DU1 external horizontal synchronous output/DU1 horizontal synchronous input	DU1_EXHSYNC/ DU1_HSYNC	I/O	DU1 composite synchronous output signal DU1 horizontal synchronous output/DU1 external horizontal synchronous input	CSYNC HSYNC or EXHSYNC*1
DU1 external vertical synchronous output/DU1 vertical synchronous output	DU1_EXVSYNC/ DU1_VSYNC	I/O	DU1 vertical synchronous output/ DU1 external vertical synchronous input DU1 composite synchronous output signal	VSYNC or EXVSYNC*1 CSYNC
DU1 odd/even field	DU1_EXODDF/ DU1_ODDF/ DISP/ CDE	I/O	DU1 odd/even field DU1 CLAMP output signal DU1 display interval DU1 color detection	ODDF or EXODDF*1 CLAMP DISP CDE
DU1 display interval	DU1_DISP	Output	DU1 display interval DU1 composite synchronous output signal DU1 DE output signal	DISP CSYNC DE
DU1 color detection	DU1_CDE	Output	DU1 color detection	CDE

Name	Pin Name	I/O	Function	Signal Name Used in This Section
DU1 display data	DU1_DR0	Output	DU1 digital red 0/green 4	Digital RGB or YC *4
	DU1_DR1	Output	DU1 digital red 1/green 5	
	DU1_DR2	Output	DU1 digital red 2/green 6	
	DU1_DR3	Output	DU1 digital red 3/green 7	
	DU1_DR4	Output	DU1 digital red 4/blue 0	
	DU1_DR5	Output	DU1 digital red 5/blue 1	
	DU1_DR6	Output	DU1 digital red 6/blue 2	
	DU1_DR7	Output	DU1 digital red 7/blue 3	
	DU1_DG0	Output	DU1 digital green 0/blue 4	
	DU1_DG1	Output	DU1 digital green 1/blue 5	
	DU1_DG2	Output	DU1 digital green 2/blue 6	
	DU1_DG3	Output	DU1 digital green 3/blue 7	
	DU1_DG4	Output	DU1 digital green 4	
	DU1_DG5	Output	DU1 digital green 5	
	DU1_DG6	Output	DU1 digital green 6	

<b>Name</b>	<b>Pin Name</b>	<b>I/O</b>	<b>Function</b>	<b>Signal Name Used in This Section</b>
DU1 display data	DU1_DG7	Output	DU1 digital green 7	Digital RGB or YC *4
	DU1_DB0	Output	DU1 digital blue 0	
	DU1_DB1	Output	DU1 digital blue 1	
	DU1_DB2	Output	DU1 digital blue 2	
	DU1_DB3	Output	DU1 digital blue 3	
	DU1_DB4	Output	DU1 digital blue 4	
	DU1_DB5	Output	DU1 digital blue 5	
	DU1_DB6	Output	DU1 digital blue 6	
	DU1_DB7	Output	DU1 digital blue 7	

- Notes:
1. These are expressed as EXHSYNC, EXVSYNC, and EXODDF in explanations of the functions as input signals and as HSYNC, VSYNC and ODDF otherwise.
  2. Synchronization for the output of digital 1 only is in accord with the setting of the output signal timing adjustment register 1 (OTAR1).
  3. In this section, unless otherwise noted, "dot clock" refers to the output dot clock.
  4. In YC format display, please refer to Table 21.39b.

## 21.2 Register Configuration

In the display unit (DU), register update methods include external update and internal update.

### (1) External Update

An "external update" is an update which reflects the address-mapped register settings made by the CPU after the end of CPU access. Registers related to display control (for example, the display unit system control register) and the settings of which are updated through external updates can be overwritten without display flicker by using bits 11 and 14 in the display unit status register n (DSSRn) \*4 indicating the start position of the vertical blanking interval.

### (2) Internal Update

An "internal update" is an update that reflects the address-mapped register settings with the internal update timing of the display unit (DU). Hence in the case of a register with an internal update function, even when the CPU overwrites address-mapped registers related to display operation without being aware of the display timing, display flicker can be prevented.

An internal update is performed during the interval in which the display reset (DRES) bit in the display unit system control register (m (DSYSRm)\*1/ (0 (DSYSR0))\*2 is 1 and at the beginning of each frame. The internal update performed at the beginning of each frame is disabled using the internal update disable (IUPD) bit in the display unit system control register (m (DSYSRm))\*1/ (0 (DSYSR0))\*2.

Bits which are internally updated in response to setting of the display reset (DRES) bit in the display unit system control register (m (DSYSRm))\*1/ (0 (DSYSR0))\*2 are listed in the column headed "Bit with Internal Update Function" in tables on the following pages.

The registers for the X and Y start positions for plane n in the interlaced sync & video mode (PnSPXRm\*3, PnSPYRm\*3) are also internally updated at the beginning of a field.

Updates are performed at the falling edge of VSYNC output when the sync method of the display unit system control register n (DSYSRn)\*4 is master mode (bit 7 = 0, bit 6 = 0), or at the falling edge of EXVSYNC detected in TV sync mode (bit 7 = 1, bit 6 = 0). In sync transition mode (bit 7 = 0, bit 6 = 1), internal updates are not performed.

However, plane n display area start address 0 register (PnDSA0Rm\*3), plane n display area start address 1 register (PnDSA1Rm\*3), and plane n display area start address 2 register (PnDSA2Rm\*3) are internally updated in display operation and externally updated when the video data and rendering data are written to addresses specified for these registers.

The address-mapped registers with an internal update function are shown in Tables 21.2 to 21.23. The initial settings for these registers should be made during the interval in which the DRES bit in (DSYSRm)\*1/ (DSYSR0)\*2 is 1.

- Notes:
1. m = 0 and 2 only for RZ/G1H
  2. For RZ/G1M/N/E
  3. m = 0 and 2, suffix "m" is only for RZ/G1H.  
n = 1 to 8.
  4. n = 0 to 2 only for RZ/G1H  
n = 0 and 1 for RZ/G1M/N/E

**(3) Register Configuration**

The suffixes m and n which are added to the register names and their abbreviations represent the DU channel numbers ( $m = 0$  and  $2^{*1}$ ;  $n = 0$  to  $2^{*2}$ ).

- Notes: 1. Only for RZ/G1H.  
 2. "n=0 and 1" For RZ/G1M/N/E.  
 "n=0 to 2" Only for RZ/G1H.

**(a) Display Unit System Control Register Configuration****Table 21.2 Display Unit System Control Register Configuration (1)**

Base address: DU0: H'FEB0 0000 (suffix 0)  
 DU1: H'FEB3 0000 (suffix 1)  
 DU2: H'FEB4 0000 (suffix 2) [Only for RZ/G1H]

Register Name	Abbr.	R/W	Offset Address	Access Size	Bit with Internal Update Function*	RZ/G Series Products			
						RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Display unit system control register m	DSYSRm	R/W	H'0000	32 bits	DSEC (bit 20) DEN (bit 8)	√	—	—	—
Display unit system control register 0	DSYSR0					—	√	√	√
Display unit system control register 1	DSYSR1	R/W	H'0000	32 bits	DSEC2 (bit 20)	√	√	√	√
Display unit mode register n	DSMRn	R/W	H'0004	32 bits	All bits However, the following bits are updated with DRES: VSPM (bit 28) ODPM (bit 27) DIPM (bits 26, 25) CSPM (bit 24) DIL (bit 19) VSL (bit 18) HSL (bit 17)	√	√	√	√
Display unit status register n	DSSRn	R	H'0008	32 bits	None	√	√	√	√
Display unit status register clear register n	DSRCRn	W	H'000C	32 bits	None	√	√	√	√
Display unit interrupt enable register n	DIERN	R/W	H'0010	32 bits	None	√	√	√	√
Color palette control register m	CPCRm	R/W	H'0014	32 bits	All bits	√	—	—	—
Color palette control register	CPCR					—	√	√	√
Display plane priority register m	DPPRm	R/W	H'0018	32 bits	All bits	√	—	—	—
Display plane priority register	DPPR					—	√	√	√



						<b>RZ/G Series Products</b>			
Register Name	Abbr.	R/W	Offset Address	Access Size	Bit with Internal Update Function*	RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Display unit extensional function control register m	DEFRm	R/W	H'0020	32 bits	The following bits are updated with DRES: EXSL (bit 12) EXUP (bit 5) VCUP (bit 4) DEFE (bit 0)	√	—	—	—
Display unit extensional function control register 0	DEFR0	R/W	H'0020	32 bits	The following bits are updated with DRES: EXSL (bit 12) EXUP (bit 5) VCUP (bit 4) DEFE (bit 0)	—	√	√	√
Display unit extensional function control register 1	DEFR1	R/W	H'0020	32 bits	The following bits are updated with DRES: EXSL1 (bit 12) DODF1 (bits 9, 8) [RZ/G1M/N/E] VCUP1 (bit 4)	√	√	√	√
Display alpha ratio plane control register m	DAPCRm	R/W	H'0024	32 bits	All bits	√	—	—	—
Display alpha ratio plane control register	DAPCR					—	√	√	√
Display capture control register m	DCPCRm	R/W	H'0028	32 bits	All bits	√	—	—	—
Display capture control register	DCPCR					—	√	√	√
Display unit extensional function control 2 register m	DEF2Rm	R/W	H'0034	32 bits	All bits Updated with DRES	√	—	—	—
Display unit extensional function control 2 register	DEF2R					—	√	√	√
Display unit extensional function control 3 register m	DEF3Rm	R/W	H'0038	32 bits	All bits Updated with DRES	√	—	—	—
Display unit extensional function control 3 register	DEF3R					—	√	√	√
Display unit extensional function control 4 register m	DEF4Rm	R/W	H'003C	32 bits	All bits Updated with DRES	√	—	—	—
Display unit extensional function control 4 register	DEF4R					—	√	√	√
Display unit video capture status register m	DVCSRm	R	H'00D0	32 bits	None	√	—	—	—
Display unit video capture status register	DVCSR					—	√	√	√
Display unit extensional function control 5 register m	DEF5Rm	R/W	H'00E0	32 bits	All bits	√	—	—	—
Display unit extensional function control 5 register	DEF5R				However, the following bit is updated with DRES: DEFE5 (bit 0)	—	√	√	√

						RZ/G Series Products			
Register Name	Abbr.	R/W	Offset Address	Access Size	Bit with Internal Update Function*	RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Display unit data latency adjustment register	DDLTR	R/W	H'00E4	32 bits	All bits Updated with DRES	√	√	√	√
Display unit extensional function control 6 register m	DEF6Rm	R/W	H'00E8	32 bits	All bits Updated with DRES	√	—	—	—
Display unit extensional function control 6 register	DEF6R					—	√	√	√
Display unit extensional function control 7 register	DEF7R	R/W	H'00EC	32 bits	All bits Updated with DRES	—	√	√	—

Base address: DU0: H'FEB2 0000 (suffix 0)  
 DU1: H'FEB2 0000 (suffix 1)  
 DU2: H'FEB6 0000 (suffix 2) [Only for RZ/G1H]

						RZ/G Series Products			
Register Name	Abbr.	R/W	Offset Address	Access Size	Bit with Internal Update Function*	RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Display unit domain 1 status register m	DD1SSRm	R	H'0008	32 bits	None	√	—	—	—
Display unit domain 1 status register 0	DD1SSR0					—	√	√	√
Display unit domain 1 status register 1	DD1SSR1	R	H'8008	32 bits	None	√	√	√	√
Display unit domain 1 status register clear register m	DD1SRCRm	W	H'000C	32 bits	None	√	—	—	—
Display unit domain 1 status register clear register 0	DD1SRCR0					—	√	√	√
Display unit domain 1 status register clear register 1	DD1SRCR1	W	H'800C	32 bits	None	√	√	√	√
Display unit domain 1 interrupt enable register m	DD1IERm	R/W	H'0010	32 bits	None	√	—	—	—
Display unit domain 1 interrupt enable register 0	DD1IER0					—	√	√	√
Display unit domain 1 interrupt enable register 1	DD1IER1	R/W	H'8010	32 bits	None	√	√	√	√
Display unit extensional function control 8 register m	DEF8Rm	R/W	H'0020	32 bits	All bits Updated with DRES	√	—	—	—
Display unit extensional function control 8 register	DEF8R					—	√	√	√
Display unit output signal fix register m	DOFLRm	R/W	H'0024	32 bits	None	√	—	—	—
Display unit output signal fix register	DOFLR					—	√	√	√

Register Name	Abbr.	R/W	Offset Address	Access Size	Bit with Internal Update Function*	RZ/G Series Products			
						RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Display unit input dot clock select register	DIDSR	R/W	H'0028	32 bits	All bits Updated with DRES	√	√	√	√

Notes: 1. m = 0 and 2, n = 0 to 2 [RZ/G1H]  
n = 0 and 1 [RZ/G1M/N/E]

2. The register available code is excluded. There is no internal update function for the register available code.

Table 21.3 Display Unit System Control Register Configuration (2)

Register Name	Abbr.	Power-on Reset	RZ/G Series Products			
			RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Display unit system control register m	DSYSRm	H'*****8*	√	—	—	—
Display unit system control register 0	DSYSR0		—	√	√	√
Display unit system control register 1	DSYSR1	H'*****8*	√	√	√	√
Display unit mode register n	DSMRn	H'*0*0*0**	√	√	√	√
Display unit status register 0	DSSR0	H'3000**00	√	√	√	√
Display unit status register 1	DSSR1	H'*****	√	√	√	√
Display unit status register 2	DSSR2	H'3000****	√	—	—	—
Display unit status register clear register n	DSRCRn	H'*****	√	√	√	√
Display unit interrupt enable register m	DIERm	H'*****00	√	—	—	—
Display unit interrupt enable register 0	DIER0		—	√	√	√
Display unit interrupt enable register 1	DIER1	H'*****	√	√	√	√
Color palette control register m	CPCRm	H'***0****	√	—	—	—
Color palette control register	CPCR		—	√	√	√
Display plane priority register m	DPPRm	H'76543210	√	—	—	—
Display plane priority register	DPPR		—	√	√	√
Display unit extensional function control register m	DEFRm	H'*****	√	—	—	—
Display unit extensional function control register 0	DEFR0		—	√	√	√
Display unit extensional function control register 1	DEFR1	H'*****	√	√	√	√
Display alpha ratio plane control register m	DAPCRm	H'*****	√	—	—	—
Display alpha ratio plane control register	DAPCR		—	√	√	√
Display capture control register m	DCPCRm	H'*****	√	—	—	—
Display capture control register	DCPCR		—	√	√	√
Display unit extensional function control 2 register m	DEF2Rm	H'*****	√	—	—	—
Display unit extensional function control 2 register	DEF2R		—	√	√	√
Display unit extensional function control 3 register m	DEF3Rm	H'*****	√	—	—	—
Display unit extensional function control 3 register	DEF3R		—	√	√	√
Display unit extensional function control 4 register m	DEF4Rm	H'*****	√	—	—	—
Display unit extensional function control 4 register	DEF4R		—	√	√	√
Display unit video capture status register m	DVCSRm	H'**00**00	√	—	—	—
Display unit video capture status register	DVCSR		—	√	√	√
Display unit extensional function control 5 register m	DEF5Rm	H'*****0**	√	—	—	—
Display unit extensional function control 5 register	DEF5R		—	√	√	√
Display unit data latency adjustment register	DDLTR	H'*****	√	√	√	√
Display unit extensional function control 6 register m	DEF6Rm	H'*****0**	√	—	—	—
Display unit extensional function control 6 register	DEF6R		—	√	√	√
Display unit extensional function control 7 register	DEF7R	H'*****	—	√	√	—
Display unit domain 1 status register 0	DD1SSR0	H'*****00	√	√	√	√
Display unit domain 1 status register 1	DD1SSR1	H'*****	√	√	√	√

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Register Name	Abbr.	Power-on Reset	RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Display unit domain 1 status register 2	DD1SSR2	H'*****	√	—	—	—
Display unit domain 1 status register clear register m	DD1SRCRm	H'*****	√	—	—	—
Display unit domain 1 status register clear register 0	DD1SRCR0		—	√	√	√
Display unit domain 1 status register clear register 1	DD1SRCR1	H'*****	√	√	√	√
Display unit domain 1 interrupt enable register m	DD1IERm	H'*****00	√	—	—	—
Display unit domain 1 interrupt enable register 0	DD1IER0		—	√	√	√
Display unit domain 1 interrupt enable register 1	DD1IER1	H'*****	√	√	√	√
Display unit extensional function control 8 register m	DEF8Rm	H'****00**	√	—	—	—
Display unit extensional function control 8 register	DEF8R		—	√	√	√
Display unit output signal fix register m	DOFLRm	H'*****0*0	√	—	—	—
Display unit output signal fix register	DOFLR		—	√	√	√
Display unit input dot clock select register	DIDSR	H'*****0*0	√	√	√	√

Note: m = 0 and 2, n = 0 to 2 [RZ/G1H]  
n = 0 and 1 [RZ/G1M/N/E]

**(b) Display Timing Generation Register Configuration****Table 21.4 Display Timing Generation Register Configuration (1)**

Base address: DU0: H'FEB0 0000 (suffix 0)  
 DU1: H'FEB3 0000 (suffix 1)  
 DU2: H'FEB4 0000 (suffix 2) [Only for RZ/G1H]

Register Name	Abbr.	R/W	Offset Address	Access Size	Bit with Internal Update Function	RZ/G Series Products			
						RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Horizontal display start register n	HDSR0	R/W	H'0040	32 bits	All bits	√	√	√	√
	HDSR1					√	√	√	√
	HDSR2					√	—	—	—
Horizontal display end register n	HDER0	R/W	H'0044	32 bits	All bits	√	√	√	√
	HDER1					√	√	√	√
	HDER2					√	—	—	—
Vertical display start register n	VDSR0	R/W	H'0048	32 bits	All bits	√	√	√	√
	VDSR1					√	√	√	√
	VDSR2					√	—	—	—
Vertical display end register n	VDER0	R/W	H'004C	32 bits	All bits	√	√	√	√
	VDER1					√	√	√	√
	VDER2					√	—	—	—
Horizontal cycle register n	HCR0	R/W	H'0050	32 bits	All bits	√	√	√	√
	HCR1					√	√	√	√
	HCR2					√	—	—	—
Horizontal sync width register n	HSWR0	R/W	H'0054	32 bits	All bits	√	√	√	√
	HSWR1					√	√	√	√
	HSWR2					√	—	—	—
Vertical cycle register n	VCR0	R/W	H'0058	32 bits	All bits	√	√	√	√
	VCR1					√	√	√	√
	VCR2					√	—	—	—
Vertical sync point register n	VSPR0	R/W	H'005C	32 bits	All bits	√	√	√	√
	VSPR1					√	√	√	√
	VSPR2					√	—	—	—
Equal pulse width register n	EQWR0	R/W	H'0060	32 bits	All bits	√	√	√	√
	EQWR1					√	√	√	√
	EQWR2					√	—	—	—
Serration width register n	SPWR0	R/W	H'0064	32 bits	All bits	√	√	√	√
	SPWR1					√	√	√	√
	SPWR2					√	—	—	—

Register Name	Abbr.	R/W	Offset Address	Access Size	Bit with Internal Update Function	RZ/G Series Products			
						RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
CLAMP signal start register n	CLAMPSR0	R/W	H'0070	32 bits	All bits	√	√	√	√
	CLAMPSR1					√	√	√	√
	CLAMPSR2					√	—	—	—
CLAMP signal width register n	CLAMPWR0	R/W	H'0074	32 bits	All bits	√	√	√	√
	CLAMPWR1					√	√	√	√
	CLAMPWR2					√	—	—	—
DE signal start register n	DESR0	R/W	H'0078	32 bits	All bits	√	√	√	√
	DESR1					√	√	√	√
	DESR2					√	—	—	—
DE signal width register n	DEWR0	R/W	H'007C	32 bits	All bits	√	√	√	√
	DEWR1					√	√	√	√
	DEWR2					√	—	—	—

Note: n = 0 to 2 [RZ/G1H]

n = 0 and 1 [RZ/G1M/N/E]

Table 21.5 Display Timing Generation Register Configuration (2)

Register Name	Abbr.	Power-on Reset	RZ/G Series Products			
			RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Horizontal display start register n	HDSR0	H'*****	√	√	√	√
	HDSR1		√	√	√	√
	HDSR2		√	—	—	—
Horizontal display end register n	HDER0	H'*****	√	√	√	√
	HDER1		√	√	√	√
	HDER2		√	—	—	—
Vertical display start register n	VDSR0	H'*****	√	√	√	√
	VDSR1		√	√	√	√
	VDSR2		√	—	—	—
Vertical display end register n	VDER0	H'*****	√	√	√	√
	VDER1		√	√	√	√
	VDER2		√	—	—	—
Horizontal cycle register n	HCR0	H'*****	√	√	√	√
	HCR1		√	√	√	√
	HCR2		√	—	—	—
Horizontal sync width register n	HSWR0	H'*****	√	√	√	√
	HSWR1		√	√	√	√
	HSWR2		√	—	—	—
Vertical cycle register n	VCR0	H'*****	√	√	√	√
	VCR1		√	√	√	√
	VCR2		√	—	—	—
Vertical sync point register n	VSPR0	H'*****	√	√	√	√
	VSPR1		√	√	√	√
	VSPR2		√	—	—	—
Equal pulse width register n	EQWR0	H'*****	√	√	√	√
	EQWR1		√	√	√	√
	EQWR2		√	—	—	—
Serration width register n	SPWR0	H'*****	√	√	√	√
	SPWR1		√	√	√	√
	SPWR2		√	—	—	—
CLAMP signal start register n	CLAMPSR0	H'*****	√	√	√	√
	CLAMPSR1		√	√	√	√
	CLAMPSR2		√	—	—	—
CLAMP signal width register n	CLAMPWR0	H'*****	√	√	√	√
	CLAMPWR1		√	√	√	√
	CLAMPWR2		√	—	—	—



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Register Name	Abbr.	Power-on Reset	RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
DE signal start register n	DESR0	H'*****	√	√	√	√
	DESR1		√	√	√	√
	DESR2		√	—	—	—
DE signal width register n	DEWR0	H'*****	√	√	√	√
	DEWR1		√	√	√	√
	DEWR2		√	—	—	—

Note: n = 0 to 2 [RZ/G1H]  
n = 0 and 1 [RZ/G1M/N/E]

## (c) Display Attribute Register Configuration

**Table 21.6 Display Attribute Register Configuration (1)**

Base address: DU0: H'FEB0 0000 (suffix 0)  
 DU1: H'FEB3 0000 (suffix 1)  
 DU2: H'FEB4 0000 (suffix 2) [Only for RZ/G1H]

Register Name	Abbr.	R/W	Address in P4	Access Size	Bit with Internal Update Function*	RZ/G Series Products			
						RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Color palette 1 transparent color register m	CP1TRm	R/W	H'0080	32 bits	All bits	√	—	—	—
Color palette 1 transparent color register	CP1TR					—	√	√	√
Color palette 2 transparent color register m	CP2TRm	R/W	H'0084	32 bits	All bits	√	—	—	—
Color palette 2 transparent color register	CP2TR					—	√	√	√
Color palette 3 transparent color register m	CP3TRm	R/W	H'0088	32 bits	All bits	√	—	—	—
Color palette 3 transparent color register	CP3TR					—	√	√	√
Color palette 4 transparent color register m	CP4TRm	R/W	H'008C	32 bits	All bits	√	—	—	—
Color palette 4 transparent color register	CP4TR					—	√	√	√
Display off mode output register n	DOOR0	R/W	H'0090	32 bits	All bits	√	√	√	√
	DOOR1					√	√	√	√
	DOOR2					√	—	—	—
Color detection register n	CDER0	R/W	H'0094	32 bits	All bits	√	√	√	√
	CDER1					√	√	√	√
	CDER2					√	—	—	—
Background plane output register n	BPOR0	R/W	H'0098	32 bits	All bits	√	√	√	√
	BPOR1					√	√	√	√
	BPOR2					√	—	—	—
Raster interrupt offset register n	RINTOFSR0	R/W	H'009C	32 bits	All bits	√	√	√	√
	RINTOFSR1					√	√	√	√
	RINTOFSR2					√	—	—	—

Notes: 1. m = 0 and 2, n = 0 to 2 [RZ/G1H]  
 n = 0 and 1 [RZ/G1M/N/E]

2. The register available code is excluded. There is no internal update function for the register available code.

**Table 21.7 Display Attribute Register Configuration (2)**

Register Name	Abbr.	Power-on Reset	RZ/G Series Products			
			RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Color palette 1 transparent color register m	CP1TRm	H'****0000	√	—	—	—
Color palette 1 transparent color register	CP1TR		—	√	√	√
Color palette 2 transparent color register m	CP2TRm	H'****0000	√	—	—	—
Color palette 2 transparent color register	CP2TR		—	√	√	√
Color palette 3 transparent color register m	CP3TRm	H'****0000	√	—	—	—
Color palette 3 transparent color register	CP3TR		—	√	√	√
Color palette 4 transparent color register m	CP4TRm	H'****0000	√	—	—	—
Color palette 4 transparent color register	CP4TR		—	√	√	√
Display off mode output register n	DOOR0	H'*****	√	√	√	√
	DOOR1		√	√	√	√
	DOOR2		√	—	—	—
Color detection register n	CDER0	H'*****	√	√	√	√
	CDER1		√	√	√	√
	CDER2		√	—	—	—
Background plane output register n	BPOR0	H'*****	√	√	√	√
	BPOR1		√	√	√	√
	BPOR2		√	—	—	—
Raster interrupt offset register n	RINTOFSR0	H'*****	√	√	√	√
	RINTOFSR1		√	√	√	√
	RINTOFSR2		√	—	—	—

Note: m = 0 and 2, n = 0 to 2 [RZ/G1H]  
n = 0 and 1 [RZ/G1M/N/E]

**(d) Display Plane Register Configuration****Table 21.8 Display Plane Register Configuration (1)**

Base address: DU0: H'FEB0 0000 (suffix 0)

DU2: H'FEB4 0000 (suffix 2) [Only for RZ/G1H]

Register Name	Abbr.	R/W	Offset Address	Access Size	Bit with Internal Update Function*	RZ/G Series Products			
						RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Plane 1 mode register m	P1MRm	R/W	H'0100	32 bits	All bits	√	—	—	—
Plane 1 mode register	P1MR					—	√	√	√
Plane 1 memory width register m	P1MWRm	R/W	H'0104	32 bits	All bits	√	—	—	—
Plane 1 memory width register	P1MWR					—	√	√	√
Plane 1 blending ratio register m	P1ALPHARm	R/W	H'0108	32 bits	All bits	√	—	—	—
Plane 1 blending ratio register	P1ALPHAR					—	√	√	√
Plane 1 display size X register m	P1DSXRm	R/W	H'0110	32 bits	All bits	√	—	—	—
Plane 1 display size X register	P1DSXR					—	√	√	√
Plane 1 display size Y register m	P1DSYRm	R/W	H'0114	32 bits	All bits	√	—	—	—
Plane 1 display size Y register	P1DSYR					—	√	√	√
Plane 1 display position X register m	P1DPXRm	R/W	H'0118	32 bits	All bits	√	—	—	—
Plane 1 display position X register	P1DPXR					—	√	√	√
Plane 1 display position Y register m	P1DPYRm	R/W	H'011C	32 bits	All bits	√	—	—	—
Plane 1 display position Y register	P1DPYR					—	√	√	√
Plane 1 display area start address 0 register m	P1DSA0Rm	R/W	H'0120	32 bits	All bits	√	—	—	—
Plane 1 display area start address 0 register	P1DSA0R					—	√	√	√
Plane 1 display area start address 1 register m	P1DSA1Rm	R/W	H'0124	32 bits	All bits	√	—	—	—
Plane 1 display area start address 1 register	P1DSA1R					—	√	√	√
Plane 1 display area start address 2 register m	P1DSA2Rm	R/W	H'0128	32 bits	All bits	√	—	—	—
Plane 1 display area start address 2 register	P1DSA2R					—	√	√	√
Plane 1 start position X register m	P1SPXRm	R/W	H'0130	32 bits	All bits	√	—	—	—
Plane 1 start position X register	P1SPXR					—	√	√	√
Plane 1 start position Y register m	P1SPYRm	R/W	H'0134	32 bits	All bits	√	—	—	—
Plane 1 start position Y register	P1SPYR					—	√	√	√
Plane 1 wrap-around start position register m	P1WASPRm	R/W	H'0138	32 bits	All bits	√	—	—	—
Plane 1 wrap-around start position register	P1WASPR					—	√	√	√
Plane 1 wrap-around memory width register m	P1WAMWRm	R/W	H'013C	32 bits	All bits	√	—	—	—
Plane 1 wrap-around memory width register	P1WAMWR					—	√	√	√
Plane 1 blinking time register m	P1BTRm	R/W	H'0140	32 bits	All bits	√	—	—	—
Plane 1 blinking time register	P1BTR					—	√	√	√
Plane 1 transparent color 1 register m	P1TC1Rm	R/W	H'0144	32 bits	All bits	√	—	—	—
Plane 1 transparent color 1 register	P1TC1R					—	√	√	√

Register Name	Abbr.	R/W	Offset Address	Access Size	Bit with Internal Update Function*	RZ/G Series Products			
						RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Plane 1 transparent color 2 register m	P1TC2Rm	R/W	H'0148	32 bits	All bits	√	—	—	—
Plane 1 transparent color 2 register	P1TC2R					—	√	√	√
Plane 1 transparent color 3 register m	P1TC3Rm	R/W	H'014C	32 bits	All bits	√	—	—	—
Plane 1 transparent color 3 register	P1TC3R					—	√	√	√
Plane 1 memory length register m	P1MLRm	R/W	H'0150	32 bits	All bits	√	—	—	—
Plane 1 memory length register	P1MLR					—	√	√	√
Plane 1 swap control register m	P1SWAPRm	R/W	H'0180	32 bits	All bits	√	—	—	—
Plane 1 swap control register	P1SWAPR					—	√	√	√
Plane 1 display data control register m	P1DDCRm	R/W	H'0184	32 bits	All bits	√	—	—	—
Plane 1 display data control register	P1DDCR					—	√	√	√
Plane 1 display data control 2 register m	P1DDC2Rm	R/W	H'0188	32 bits	All bits	√	—	—	—
Plane 1 display data control 2 register	P1DDC2R					—	√	√	√
Plane 1 display data control 4 register m	P1DDC4Rm	R/W	H'0190	32 bits	All bits	√	—	—	—
Plane 1 display data control 4 register	P1DDC4R					—	√	√	√
Plane 2 mode register m	P2MRm	R/W	H'0200	32 bits	All bits	√	—	—	—
Plane 2 mode register	P2MR					—	√	√	√
Plane 2 memory width register m	P2MWRm	R/W	H'0204	32 bits	All bits	√	—	—	—
Plane 2 memory width register	P2MWR					—	√	√	√
Plane 2 blending ratio register m	P2ALPHARm	R/W	H'0208	32 bits	All bits	√	—	—	—
Plane 2 blending ratio register	P2ALPHAR					—	√	√	√
Plane 2 display size X register m	P2DSXRm	R/W	H'0210	32 bits	All bits	√	—	—	—
Plane 2 display size X register	P2DSXR					—	√	√	√
Plane 2 display size Y register m	P2DSYRm	R/W	H'0214	32 bits	All bits	√	—	—	—
Plane 2 display size Y register	P2DSYR					—	√	√	√
Plane 2 display position X register m	P2DPXRm	R/W	H'0218	32 bits	All bits	√	—	—	—
Plane 2 display position X register	P2DPXR					—	√	√	√
Plane 2 display position Y register m	P2DPYRm	R/W	H'021C	32 bits	All bits	√	—	—	—
Plane 2 display position Y register	P2DPYR					—	√	√	√
Plane 2 display area start address 0 register m	P2DSA0Rm	R/W	H'0220	32 bits	All bits	√	—	—	—
Plane 2 display area start address 0 register	P2DSA0R					—	√	√	√
Plane 2 display area start address 1 register m	P2DSA1Rm	R/W	H'0224	32 bits	All bits	√	—	—	—
Plane 2 display area start address 1 register	P2DSA1R					—	√	√	√
Plane 2 display area start address 2 register m	P2DSA2Rm	R/W	H'0228	32 bits	All bits	√	—	—	—
Plane 2 display area start address 2 register	P2DSA2R					—	√	√	√
Plane 2 start position X register m	P2SPXRm	R/W	H'0230	32 bits	All bits	√	—	—	—
Plane 2 start position X register	P2SPXR					—	√	√	√
Plane 2 start position Y register m	P2SPYRm	R/W	H'0234	32 bits	All bits	√	—	—	—
Plane 2 start position Y register	P2SPYR					—	√	√	√

Register Name	Abbr.	R/W	Offset Address	Access Size	Bit with Internal Update Function*	RZ/G Series Products			
						RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Plane 2 wrap-around start position register m	P2WASPRm	R/W	H'0238	32 bits	All bits	√	—	—	—
Plane 2 wrap-around start position register	P2WASPR					—	√	√	√
Plane 2 wrap-around memory width register m	P2WAMWRm	R/W	H'023C	32 bits	All bits	√	—	—	—
Plane 2 wrap-around memory width register	P2WAMWR					—	√	√	√
Plane 2 blinking time register m	P2BTRm	R/W	H'0240	32 bits	All bits	√	—	—	—
Plane 2 blinking time register	P2BTR					—	√	√	√
Plane 2 transparent color 1 register m	P2TC1Rm	R/W	H'0244	32 bits	All bits	√	—	—	—
Plane 2 transparent color 1 register	P2TC1R					—	√	√	√
Plane 2 transparent color 2 register m	P2TC2Rm	R/W	H'0248	32 bits	All bits	√	—	—	—
Plane 2 transparent color 2 register	P2TC2R					—	√	√	√
Plane 2 transparent color 3 register m	P2TC3Rm	R/W	H'024C	32 bits	All bits	√	—	—	—
Plane 2 transparent color 3 register	P2TC3R					—	√	√	√
Plane 2 memory length register m	P2MLRm	R/W	H'0250	32 bits	All bits	√	—	—	—
Plane 2 memory length register	P2MLR					—	√	√	√
Plane 2 swap control register m	P2SWAPRm	R/W	H'0280	32 bits	All bits	√	—	—	—
Plane 2 swap control register	P2SWAPR					—	√	√	√
Plane 2 display data control register m	P2DDCRm	R/W	H'0284	32 bits	All bits	√	—	—	—
Plane 2 display data control register	P2DDCR					—	√	√	√
Plane 2 display data control 2 register m	P2DDC2Rm	R/W	H'0288	32 bits	All bits	√	—	—	—
Plane 2 display data control 2 register	P2DDC2R					—	√	√	√
Plane 2 display data control 4 register m	P2DDC4Rm	R/W	H'0290	32 bits	All bits	√	—	—	—
Plane 2 display data control 4 register	P2DDC4R					—	√	√	√
Plane 3 mode register m	P3MRm	R/W	H'0300	32 bits	All bits	√	—	—	—
Plane 3 mode register	P3MR					—	√	√	√
Plane 3 memory width register m	P3MWRm	R/W	H'0304	32 bits	All bits	√	—	—	—
Plane 3 memory width register	P3MWR					—	√	√	√
Plane 3 blending ratio register m	P3ALPHARm	R/W	H'0308	32 bits	All bits	√	—	—	—
Plane 3 blending ratio register	P3ALPHAR					—	√	√	√
Plane 3 display size X register m	P3DSXRm	R/W	H'0310	32 bits	All bits	√	—	—	—
Plane 3 display size X register	P3DSXR					—	√	√	√
Plane 3 display size Y register m	P3DSYRm	R/W	H'0314	32 bits	All bits	√	—	—	—
Plane 3 display size Y register	P3DSYR					—	√	√	√
Plane 3 display position X register m	P3DPXRm	R/W	H'0318	32 bits	All bits	√	—	—	—
Plane 3 display position X register	P3DPXR					—	√	√	√
Plane 3 display position Y register m	P3DPYRm	R/W	H'031C	32 bits	All bits	√	—	—	—
Plane 3 display position Y register	P3DPYR					—	√	√	√
Plane 3 display area start address 0 register m	P3DSA0Rm	R/W	H'0320	32 bits	All bits	√	—	—	—
Plane 3 display area start address 0 register	P3DSA0R					—	√	√	√

Register Name	Abbr.	R/W	Offset Address	Access Size	Bit with Internal Update Function*	RZ/G Series Products			
						RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Plane 3 display area start address 1 register m	P3DSA1Rm	R/W	H'0324	32 bits	All bits	√	—	—	—
Plane 3 display area start address 1 register	P3DSA1R					—	√	√	√
Plane 3 display area start address 2 register m	P3DSA2Rm	R/W	H'0328	32 bits	All bits	√	—	—	—
Plane 3 display area start address 2 register	P3DSA2R					—	√	√	√
Plane 3 start position X register m	P3SPXRm	R/W	H'0330	32 bits	All bits	√	—	—	—
Plane 3 start position X register	P3SPXR					—	√	√	√
Plane 3 start position Y register m	P3SPYRm	R/W	H'0334	32 bits	All bits	√	—	—	—
Plane 3 start position Y register	P3SPYR					—	√	√	√
Plane 3 wrap-around start position register m	P3WASPRm	R/W	H'0338	32 bits	All bits	√	—	—	—
Plane 3 wrap-around start position register	P3WASPR					—	√	√	√
Plane 3 wrap-around memory width register m	P3WAMWRm	R/W	H'033C	32 bits	All bits	√	—	—	—
Plane 3 wrap-around memory width register	P3WAMWR					—	√	√	√
Plane 3 blinking time register m	P3BTRm	R/W	H'0340	32 bits	All bits	√	—	—	—
Plane 3 blinking time register	P3BTR					—	√	√	√
Plane 3 transparent color 1 register m	P3TC1Rm	R/W	H'0344	32 bits	All bits	√	—	—	—
Plane 3 transparent color 1 register	P3TC1R					—	√	√	√
Plane 3 transparent color 2 register m	P3TC2Rm	R/W	H'0348	32 bits	All bits	√	—	—	—
Plane 3 transparent color 2 register	P3TC2R					—	√	√	√
Plane 3 transparent color 3 register m	P3TC3Rm	R/W	H'034C	32 bits	All bits	√	—	—	—
Plane 3 transparent color 3 register	P3TC3R					—	√	√	√
Plane 3 memory length register m	P3MLRm	R/W	H'0350	32 bits	All bits	√	—	—	—
Plane 3 memory length register	P3MLR					—	√	√	√
Plane 3 swap control register m	P3SWAPRm	R/W	H'0380	32 bits	All bits	√	—	—	—
Plane 3 swap control register	P3SWAPR					—	√	√	√
Plane 3 display data control register m	P3DDCRm	R/W	H'0384	32 bits	All bits	√	—	—	—
Plane 3 display data control register	P3DDCR					—	√	√	√
Plane 3 display data control 2 register m	P3DDC2Rm	R/W	H'0388	32 bits	All bits	√	—	—	—
Plane 3 display data control 2 register	P3DDC2R					—	√	√	√
Plane 3 display data control 4 register m	P3DDC4Rm	R/W	H'0390	32 bits	All bits	√	—	—	—
Plane 3 display data control 4 register	P3DDC4R					—	√	√	√
Plane 4 mode register m	P4MRm	R/W	H'0400	32 bits	All bits	√	—	—	—
Plane 4 mode register	P4MR					—	√	√	√
Plane 4 memory width register m	P4MWRm	R/W	H'0404	32 bits	All bits	√	—	—	—
Plane 4 memory width register	P4MWR					—	√	√	√
Plane 4 blending ratio register m	P4ALPHARm	R/W	H'0408	32 bits	All bits	√	—	—	—
Plane 4 blending ratio register	P4ALPHAR					—	√	√	√
Plane 4 display size X register m	P4DSXRm	R/W	H'0410	32 bits	All bits	√	—	—	—
Plane 4 display size X register	P4DSXR					—	√	√	√

Register Name	Abbr.	R/W	Offset Address	Access Size	Bit with Internal Update Function*	RZ/G Series Products			
						RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Plane 4 display size Y register m	P4DSYRm	R/W	H'0414	32 bits	All bits	√	—	—	—
Plane 4 display size Y register	P4DSYR					—	√	√	√
Plane 4 display position X register m	P4DPXRm	R/W	H'0418	32 bits	All bits	√	—	—	—
Plane 4 display position X register	P4DPXR					—	√	√	√
Plane 4 display position Y register m	P4DPYRm	R/W	H'041C	32 bits	All bits	√	—	—	—
Plane 4 display position Y register	P4DPYR					—	√	√	√
Plane 4 display area start address 0 register m	P4DSA0Rm	R/W	H'0420	32 bits	All bits	√	—	—	—
Plane 4 display area start address 0 register	P4DSA0R					—	√	√	√
Plane 4 display area start address 1 register m	P4DSA1Rm	R/W	H'0424	32 bits	All bits	√	—	—	—
Plane 4 display area start address 1 register	P4DSA1R					—	√	√	√
Plane 4 display area start address 2 register m	P4DSA2Rm	R/W	H'0428	32 bits	All bits	√	—	—	—
Plane 4 display area start address 2 register	P4DSA2R					—	√	√	√
Plane 4 start position X register m	P4SPXRm	R/W	H'0430	32 bits	All bits	√	—	—	—
Plane 4 start position X register	P4SPXR					—	√	√	√
Plane 4 start position Y register m	P4SPYRm	R/W	H'0434	32 bits	All bits	√	—	—	—
Plane 4 start position Y register	P4SPYR					—	√	√	√
Plane 4 wrap-around start position register m	P4WASPRm	R/W	H'0438	32 bits	All bits	√	—	—	—
Plane 4 wrap-around start position register	P4WASPR					—	√	√	√
Plane 4 wrap-around memory width register m	P4WAMWRm	R/W	H'043C	32 bits	All bits	√	—	—	—
Plane 4 wrap-around memory width register	P4WAMWR					—	√	√	√
Plane 4 blinking time register m	P4BTRm	R/W	H'0440	32 bits	All bits	√	—	—	—
Plane 4 blinking time register	P4BTR					—	√	√	√
Plane 4 transparent color 1 register m	P4TC1Rm	R/W	H'0444	32 bits	All bits	√	—	—	—
Plane 4 transparent color 1 register	P4TC1R					—	√	√	√
Plane 4 transparent color 2 register m	P4TC2Rm	R/W	H'0448	32 bits	All bits	√	—	—	—
Plane 4 transparent color 2 register	P4TC2R					—	√	√	√
Plane 4 transparent color 3 register m	P4TC3Rm	R/W	H'044C	32 bits	All bits	√	—	—	—
Plane 4 transparent color 3 register	P4TC3R					—	√	√	√
Plane 4 memory length register m	P4MLRm	R/W	H'0450	32 bits	All bits	√	—	—	—
Plane 4 memory length register	P4MLR					—	√	√	√
Plane 4 swap control register m	P4SWAPRm	R/W	H'0480	32 bits	All bits	√	—	—	—
Plane 4 swap control register	P4SWAPR					—	√	√	√
Plane 4 display data control register m	P4DDCRm	R/W	H'0484	32 bits	All bits	√	—	—	—
Plane 4 display data control register	P4DDCR					—	√	√	√
Plane 4 display data control 2 register m	P4DDC2Rm	R/W	H'0488	32 bits	All bits	√	—	—	—
Plane 4 display data control 2 register	P4DDC2R					—	√	√	√
Plane 4 display data control 4 register m	P4DDC4Rm	R/W	H'0490	32 bits	All bits	√	—	—	—
Plane 4 display data control 4 register	P4DDC4R					—	√	√	√



Register Name	Abbr.	R/W	Offset Address	Access Size	Bit with Internal Update Function*	RZ/G Series Products			
						RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Plane 5 mode register m	P5MRm	R/W	H'0500	32 bits	All bits	√	—	—	—
Plane 5 mode register	P5MR					—	√	√	√
Plane 5 memory width register m	P5MWRm	R/W	H'0504	32 bits	All bits	√	—	—	—
Plane 5 memory width register	P5MWR					—	√	√	√
Plane 5 blending ratio register m	P5ALPHARm	R/W	H'0508	32 bits	All bits	√	—	—	—
Plane 5 blending ratio register	P5ALPHAR					—	√	√	√
Plane 5 display size X register m	P5DSXRm	R/W	H'0510	32 bits	All bits	√	—	—	—
Plane 5 display size X register	P5DSXR					—	√	√	√
Plane 5 display size Y register m	P5DSYRm	R/W	H'0514	32 bits	All bits	√	—	—	—
Plane 5 display size Y register	P5DSYR					—	√	√	√
Plane 5 display position X register m	P5DPXRm	R/W	H'0518	32 bits	All bits	√	—	—	—
Plane 5 display position X register	P5DPXR					—	√	√	√
Plane 5 display position Y register m	P5DPYRm	R/W	H'051C	32 bits	All bits	√	—	—	—
Plane 5 display position Y register	P5DPYR					—	√	√	√
Plane 5 display area start address 0 register m	P5DSA0Rm	R/W	H'0520	32 bits	All bits	√	—	—	—
Plane 5 display area start address 0 register	P5DSA0R					—	√	√	√
Plane 5 display area start address 1 register m	P5DSA1Rm	R/W	H'0524	32 bits	All bits	√	—	—	—
Plane 5 display area start address 1 register	P5DSA1R					—	√	√	√
Plane 5 display area start address 2 register m	P5DSA2Rm	R/W	H'0528	32 bits	All bits	√	—	—	—
Plane 5 display area start address 2 register	P5DSA2R					—	√	√	√
Plane 5 start position X register m	P5SPXRm	R/W	H'0530	32 bits	All bits	√	—	—	—
Plane 5 start position X register	P5SPXR					—	√	√	√
Plane 5 start position Y register m	P5SPYRm	R/W	H'0534	32 bits	All bits	√	—	—	—
Plane 5 start position Y register	P5SPYR					—	√	√	√
Plane 5 wrap-around start position register m	P5WASPRm	R/W	H'0538	32 bits	All bits	√	—	—	—
Plane 5 wrap-around start position register	P5WASPR					—	√	√	√
Plane 5 wrap-around memory width register m	P5WAMWRm	R/W	H'053C	32 bits	All bits	√	—	—	—
Plane 5 wrap-around memory width register	P5WAMWR					—	√	√	√
Plane 5 blinking time register m	P5BTRm	R/W	H'0540	32 bits	All bits	√	—	—	—
Plane 5 blinking time register	P5BTR					—	√	√	√
Plane 5 transparent color 1 register m	P5TC1Rm	R/W	H'0544	32 bits	All bits	√	—	—	—
Plane 5 transparent color 1 register	P5TC1R					—	√	√	√
Plane 5 transparent color 2 register m	P5TC2Rm	R/W	H'0548	32 bits	All bits	√	—	—	—
Plane 5 transparent color 2 register	P5TC2R					—	√	√	√
Plane 5 transparent color 3 register m	P5TC3Rm	R/W	H'054C	32 bits	All bits	√	—	—	—
Plane 5 transparent color 3 register	P5TC3R					—	√	√	√
Plane 5 memory length register m	P5MLRm	R/W	H'0550	32 bits	All bits	√	—	—	—
Plane 5 memory length register	P5MLR					—	√	√	√

Register Name	Abbr.	R/W	Offset Address	Access Size	Bit with Internal Update Function*	RZ/G Series Products			
						RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Plane 5 swap control register m	P5SWAPRm	R/W	H'0580	32 bits	All bits	√	—	—	—
Plane 5 swap control register	P5SWAPR					—	√	√	√
Plane 5 display data control register m	P5DDCRm	R/W	H'0584	32 bits	All bits	√	—	—	—
Plane 5 display data control register	P5DDCR					—	√	√	√
Plane 5 display data control 2 register m	P5DDC2Rm	R/W	H'0588	32 bits	All bits	√	—	—	—
Plane 5 display data control 2 register	P5DDC2R					—	√	√	√
Plane 5 display data control 4 register m	P5DDC4Rm	R/W	H'0590	32 bits	All bits	√	—	—	—
Plane 5 display data control 4 register	P5DDC4R					—	√	√	√
Plane 6 mode register m	P6MRm	R/W	H'0600	32 bits	All bits	√	—	—	—
Plane 6 mode register	P6MR					—	√	√	√
Plane 6 memory width register m	P6MWRm	R/W	H'0604	32 bits	All bits	√	—	—	—
Plane 6 memory width register	P6MWR					—	√	√	√
Plane 6 blending ratio register m	P6ALPHARm	R/W	H'0608	32 bits	All bits	√	—	—	—
Plane 6 blending ratio register	P6ALPHAR					—	√	√	√
Plane 6 display size X register m	P6DSXRm	R/W	H'0610	32 bits	All bits	√	—	—	—
Plane 6 display size X register	P6DSXR					—	√	√	√
Plane 6 display size Y register m	P6DSYRm	R/W	H'0614	32 bits	All bits	√	—	—	—
Plane 6 display size Y register	P6DSYR					—	√	√	√
Plane 6 display position X register m	P6DPXRm	R/W	H'0618	32 bits	All bits	√	—	—	—
Plane 6 display position X register	P6DPXR					—	√	√	√
Plane 6 display position Y register m	P6DPYRm	R/W	H'061C	32 bits	All bits	√	—	—	—
Plane 6 display position Y register	P6DPYR					—	√	√	√
Plane 6 display area start address 0 register m	P6DSA0Rm	R/W	H'0620	32 bits	All bits	√	—	—	—
Plane 6 display area start address 0 register	P6DSA0R					—	√	√	√
Plane 6 display area start address 1 register m	P6DSA1Rm	R/W	H'0624	32 bits	All bits	√	—	—	—
Plane 6 display area start address 1 register	P6DSA1R					—	√	√	√
Plane 6 display area start address 2 register m	P6DSA2Rm	R/W	H'0628	32 bits	All bits	√	—	—	—
Plane 6 display area start address 2 register	P6DSA2R					—	√	√	√
Plane 6 start position X register m	P6SPXRm	R/W	H'0630	32 bits	All bits	√	—	—	—
Plane 6 start position X register	P6SPXR					—	√	√	√
Plane 6 start position Y register m	P6SPYRm	R/W	H'0634	32 bits	All bits	√	—	—	—
Plane 6 start position Y register	P6SPYR					—	√	√	√
Plane 6 wrap-around start position register m	P6WASPRm	R/W	H'0638	32 bits	All bits	√	—	—	—
Plane 6 wrap-around start position register	P6WASPR					—	√	√	√
Plane 6 wrap-around memory width register m	P6WAMWRm	R/W	H'063C	32 bits	All bits	√	—	—	—
Plane 6 wrap-around memory width register	P6WAMWR					—	√	√	√
Plane 6 blinking time register m	P6BTRm	R/W	H'0640	32 bits	All bits	√	—	—	—
Plane 6 blinking time register	P6BTR					—	√	√	√

Register Name	Abbr.	R/W	Offset Address	Access Size	Bit with Internal Update Function*	RZ/G Series Products			
						RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Plane 6 transparent color 1 register m	P6TC1Rm	R/W	H'0644	32 bits	All bits	√	—	—	—
Plane 6 transparent color 1 register	P6TC1R					—	√	√	√
Plane 6 transparent color 2 register m	P6TC2Rm	R/W	H'0648	32 bits	All bits	√	—	—	—
Plane 6 transparent color 2 register	P6TC2R					—	√	√	√
Plane 6 transparent color 3 register m	P6TC3Rm	R/W	H'064C	32 bits	All bits	√	—	—	—
Plane 6 transparent color 3 register	P6TC3R					—	√	√	√
Plane 6 memory length register m	P6MLRm	R/W	H'0650	32 bits	All bits	√	—	—	—
Plane 6 memory length register	P6MLR					—	√	√	√
Plane 6 swap control register m	P6SWAPRm	R/W	H'0680	32 bits	All bits	√	—	—	—
Plane 6 swap control register	P6SWAPR					—	√	√	√
Plane 6 display data control register m	P6DDCRm	R/W	H'0684	32 bits	All bits	√	—	—	—
Plane 6 display data control register	P6DDCR					—	√	√	√
Plane 6 display data control 2 register m	P6DDC2Rm	R/W	H'0688	32 bits	All bits	√	—	—	—
Plane 6 display data control 2 register	P6DDC2R					—	√	√	√
Plane 6 display data control 4 register m	P6DDC4Rm	R/W	H'0690	32 bits	All bits	√	—	—	—
Plane 6 display data control 4 register	P6DDC4R					—	√	√	√
Plane 7 mode register m	P7MRm	R/W	H'0700	32 bits	All bits	√	—	—	—
Plane 7 mode register	P7MR					—	√	√	√
Plane 7 memory width register m	P7MWRm	R/W	H'0704	32 bits	All bits	√	—	—	—
Plane 7 memory width register	P7MWR					—	√	√	√
Plane 7 blending ratio register m	P7ALPHARm	R/W	H'0708	32 bits	All bits	√	—	—	—
Plane 7 blending ratio register	P7ALPHAR					—	√	√	√
Plane 7 display size X register m	P7DSXRm	R/W	H'0710	32 bits	All bits	√	—	—	—
Plane 7 display size X register	P7DSXR					—	√	√	√
Plane 7 display size Y register m	P7DSYRm	R/W	H'0714	32 bits	All bits	√	—	—	—
Plane 7 display size Y register	P7DSYR					—	√	√	√
Plane 7 display position X register m	P7DPXRm	R/W	H'0718	32 bits	All bits	√	—	—	—
Plane 7 display position X register	P7DPXR					—	√	√	√
Plane 7 display position Y register m	P7DPYRm	R/W	H'071C	32 bits	All bits	√	—	—	—
Plane 7 display position Y register	P7DPYR					—	√	√	√
Plane 7 display area start address 0 register m	P7DSA0Rm	R/W	H'0720	32 bits	All bits	√	—	—	—
Plane 7 display area start address 0 register	P7DSA0R					—	√	√	√
Plane 7 display area start address 1 register m	P7DSA1Rm	R/W	H'0724	32 bits	All bits	√	—	—	—
Plane 7 display area start address 1 register	P7DSA1R					—	√	√	√
Plane 7 display area start address 2 register m	P7DSA2Rm	R/W	H'0728	32 bits	All bits	√	—	—	—
Plane 7 display area start address 2 register	P7DSA2R					—	√	√	√
Plane 7 start position X register m	P7SPXRm	R/W	H'0730	32 bits	All bits	√	—	—	—
Plane 7 start position X register	P7SPXR					—	√	√	√

Register Name	Abbr.	R/W	Offset Address	Access Size	Bit with Internal Update Function*	RZ/G Series Products			
						RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Plane 7 start position Y register m	P7SPYRm	R/W	H'0734	32 bits	All bits	√	—	—	—
Plane 7 start position Y register	P7SPYR					—	√	√	√
Plane 7 wrap-around start position register m	P7WASPRm	R/W	H'0738	32 bits	All bits	√	—	—	—
Plane 7 wrap-around start position register	P7WASPR					—	√	√	√
Plane 7 wrap-around memory width register m	P7WAMWRm	R/W	H'073C	32 bits	All bits	√	—	—	—
Plane 7 wrap-around memory width register	P7WAMWR					—	√	√	√
Plane 7 blinking time register m	P7BTRm	R/W	H'0740	32 bits	All bits	√	—	—	—
Plane 7 blinking time register	P7BTR					—	√	√	√
Plane 7 transparent color 1 register m	P7TC1Rm	R/W	H'0744	32 bits	All bits	√	—	—	—
Plane 7 transparent color 1 register	P7TC1R					—	√	√	√
Plane 7 transparent color 2 register m	P7TC2Rm	R/W	H'0748	32 bits	All bits	√	—	—	—
Plane 7 transparent color 2 register	P7TC2R					—	√	√	√
Plane 7 transparent color 3 register m	P7TC3Rm	R/W	H'074C	32 bits	All bits	√	—	—	—
Plane 7 transparent color 3 register	P7TC3R					—	√	√	√
Plane 7 memory length register m	P7MLRm	R/W	H'0750	32 bits	All bits	√	—	—	—
Plane 7 memory length register	P7MLR					—	√	√	√
Plane 7 swap control register m	P7SWAPRm	R/W	H'0780	32 bits	All bits	√	—	—	—
Plane 7 swap control register	P7SWAPR					—	√	√	√
Plane 7 display data control register m	P7DDCRm	R/W	H'0784	32 bits	All bits	√	—	—	—
Plane 7 display data control register	P7DDCR					—	√	√	√
Plane 7 display data control 2 register m	P7DDC2Rm	R/W	H'0788	32 bits	All bits	√	—	—	—
Plane 7 display data control 2 register	P7DDC2R					—	√	√	√
Plane 7 display data control 4 register m	P7DDC4Rm	R/W	H'0790	32 bits	All bits	√	—	—	—
Plane 7 display data control 4 register	P7DDC4R					—	√	√	√
Plane 8 mode register m	P8MRm	R/W	H'0800	32 bits	All bits	√	—	—	—
Plane 8 mode register	P8MR					—	√	√	√
Plane 8 memory width register m	P8MWRm	R/W	H'0804	32 bits	All bits	√	—	—	—
Plane 8 memory width register	P8MWR					—	√	√	√
Plane 8 blending ratio register m	P8ALPHARm	R/W	H'0808	32 bits	All bits	√	—	—	—
Plane 8 blending ratio register	P8ALPHAR					—	√	√	√
Plane 8 display size X register m	P8DSXRm	R/W	H'0810	32 bits	All bits	√	—	—	—
Plane 8 display size X register	P8DSXR					—	√	√	√
Plane 8 display size Y register m	P8DSYRm	R/W	H'0814	32 bits	All bits	√	—	—	—
Plane 8 display size Y register	P8DSYR					—	√	√	√
Plane 8 start position X register m	P8DPXRm	R/W	H'0818	32 bits	All bits	√	—	—	—
Plane 8 start position X register	P8DPXR					—	√	√	√
Plane 8 display position Y register m	P8DPYRm	R/W	H'081C	32 bits	All bits	√	—	—	—
Plane 8 display position Y register	P8DPYR					—	√	√	√

Register Name	Abbr.	R/W	Offset Address	Access Size	Bit with Internal Update Function*	RZ/G Series Products			
						RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Plane 8 display area start address 0 register m	P8DSA0Rm	R/W	H'0820	32 bits	All bits	√	—	—	—
Plane 8 display area start address 0 register	P8DSA0R					—	√	√	√
Plane 8 display area start address 1 register m	P8DSA1Rm	R/W	H'0824	32 bits	All bits	√	—	—	—
Plane 8 display area start address 1 register	P8DSA1R					—	√	√	√
Plane 8 display area start address 2 register m	P8DSA2Rm	R/W	H'0828	32 bits	All bits	√	—	—	—
Plane 8 display area start address 2 register	P8DSA2R					—	√	√	√
Plane 8 start position X register m	P8SPXRm	R/W	H'0830	32 bits	All bits	√	—	—	—
Plane 8 start position X register	P8SPXR					—	√	√	√
Plane 8 start position Y register m	P8SPYRm	R/W	H'0834	32 bits	All bits	√	—	—	—
Plane 8 start position Y register	P8SPYR					—	√	√	√
Plane 8 wrap-around start position register m	P8WASPRm	R/W	H'0838	32 bits	All bits	√	—	—	—
Plane 8 wrap-around start position register	P8WASPR					—	√	√	√
Plane 8 wrap-around memory width register m	P8WAMWRm	R/W	H'083C	32 bits	All bits	√	—	—	—
Plane 8 wrap-around memory width register	P8WAMWR					—	√	√	√
Plane 8 blinking time register m	P8BTRm	R/W	H'0840	32 bits	All bits	√	—	—	—
Plane 8 blinking time register	P8BTR					—	√	√	√
Plane 8 transparent color 1 register m	P8TC1Rm	R/W	H'0844	32 bits	All bits	√	—	—	—
Plane 8 transparent color 1 register	P8TC1R					—	√	√	√
Plane 8 transparent color 2 register m	P8TC2Rm	R/W	H'0848	32 bits	All bits	√	—	—	—
Plane 8 transparent color 2 register	P8TC2R					—	√	√	√
Plane 8 transparent color 3 register m	P8TC3Rm	R/W	H'084C	32 bits	All bits	√	—	—	—
Plane 8 transparent color 3 register	P8TC3R					—	√	√	√
Plane 8 memory length register m	P8MLRm	R/W	H'0850	32 bits	All bits	√	—	—	—
Plane 8 memory length register	P8MLR					—	√	√	√
Plane 8 swap control register m	P8SWAPRm	R/W	H'0880	32 bits	All bits	√	—	—	—
Plane 8 swap control register	P8SWAPR					—	√	√	√
Plane 8 display data control register m	P8DDCRm	R/W	H'0884	32 bits	All bits	√	—	—	—
Plane 8 display data control register	P8DDCR					—	√	√	√
Plane 8 display data control 2 register m	P8DDC2Rm	R/W	H'0888	32 bits	All bits	√	—	—	—
Plane 8 display data control 2 register	P8DDC2R					—	√	√	√
Plane 8 display data control 4 register m	P8DDC4Rm	R/W	H'0890	32 bits	All bits	√	—	—	—
Plane 8 display data control 4 register	P8DDC4R					—	√	√	√

Notes: 1. m = 0 and 2 [Only for RZ/G1H]

2. The register available code is excluded. There is no internal update function for the register available code.

Table 21.9 Display Plane Register Configuration (2)

Register Name	Abbr.	Power-on Reset	RZ/G Series Products			
			RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Plane 1 mode register m	P1MRm	H'*****	√	—	—	—
Plane 1 mode register	P1MR		—	√	√	√
Plane 1 memory width register m	P1MWRm	H'*****	√	—	—	—
Plane 1 memory width register	P1MWR		—	√	√	√
Plane 1 blending ratio register m	P1ALPHARm	H'*****	√	—	—	—
Plane 1 blending ratio register	P1ALPHAR		—	√	√	√
Plane 1 display size X register m	P1DSXRm	H'*****	√	—	—	—
Plane 1 display size X register	P1DSXR		—	√	√	√
Plane 1 display size Y register m	P1DSYRm	H'*****	√	—	—	—
Plane 1 display size Y register	P1DSYR		—	√	√	√
Plane 1 display position X register m	P1DPXRm	H'*****	√	—	—	—
Plane 1 display position X register	P1DPXR		—	√	√	√
Plane 1 display position Y register m	P1DPYRm	H'*****	√	—	—	—
Plane 1 display position Y register	P1DPYR		—	√	√	√
Plane 1 display area start address 0 register m	P1DSA0Rm	H'*****	√	—	—	—
Plane 1 display area start address 0 register	P1DSA0R		—	√	√	√
Plane 1 display area start address 1 register m	P1DSA1Rm	H'*****	√	—	—	—
Plane 1 display area start address 1 register	P1DSA1R		—	√	√	√
Plane 1 display area start address 2 register m	P1DSA2Rm	H'*****	√	—	—	—
Plane 1 display area start address 2 register	P1DSA2R		—	√	√	√
Plane 1 start position X register m	P1SPXRm	H'*****	√	—	—	—
Plane 1 start position X register	P1SPXR		—	√	√	√
Plane 1 start position Y register m	P1SPYRm	H'*****	√	—	—	—
Plane 1 start position Y register	P1SPYR		—	√	√	√
Plane 1 wrap-around start position register m	P1WASPRm	H'*****	√	—	—	—
Plane 1 wrap-around start position register	P1WASPR		—	√	√	√
Plane 1 wrap-around memory width register m	P1WAMWRm	H'*****	√	—	—	—
Plane 1 wrap-around memory width register	P1WAMWR		—	√	√	√
Plane 1 blinking time register m	P1BTRm	H'****0101	√	—	—	—
Plane 1 blinking time register	P1BTR		—	√	√	√
Plane 1 transparent color 1 register m	P1TC1Rm	H'*****	√	—	—	—
Plane 1 transparent color 1 register	P1TC1R		—	√	√	√
Plane 1 transparent color 2 register m	P1TC2Rm	H'*****	√	—	—	—
Plane 1 transparent color 2 register	P1TC2R		—	√	√	√
Plane 1 transparent color 3 register m	P1TC3Rm	H'*****	√	—	—	—
Plane 1 transparent color 3 register	P1TC3R		—	√	√	√
Plane 1 memory length register m	P1MLRm	H'****0000	√	—	—	—
Plane 1 memory length register	P1MLR		—	√	√	√

			RZ/G Series Products			
Register Name	Abbr.	Power-on Reset	RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Plane 1 swap control register m	P1SWAPRm	H'*****0	√	—	—	—
Plane 1 swap control register	P1SWAPR		—	√	√	√
Plane 1 display data control register m	P1DDCRm	H'*****	√	—	—	—
Plane 1 display data control register	P1DDCR		—	√	√	√
Plane 1 display data control 2 register m	P1DDC2Rm	H'*****	√	—	—	—
Plane 1 display data control 2 register	P1DDC2R		—	√	√	√
Plane 1 display data control 4 register m	P1DDC4Rm	H'*****	√	—	—	—
Plane 1 display data control 4 register	P1DDC4R		—	√	√	√
Plane 2 mode register m	P2MRm	H'*****	√	—	—	—
Plane 2 mode register	P2MR		—	√	√	√
Plane 2 memory width register m	P2MWRm	H'*****	√	—	—	—
Plane 2 memory width register	P2MWR		—	√	√	√
Plane 2 blending ratio register m	P2ALPHARm	H'*****	√	—	—	—
Plane 2 blending ratio register	P2ALPHAR		—	√	√	√
Plane 2 display size X register m	P2DSXRm	H'*****	√	—	—	—
Plane 2 display size X register	P2DSXR		—	√	√	√
Plane 2 display size Y register m	P2DSYRm	H'*****	√	—	—	—
Plane 2 display size Y register	P2DSYR		—	√	√	√
Plane 2 display position X register m	P2DPXRm	H'*****	√	—	—	—
Plane 2 display position X register	P2DPXR		—	√	√	√
Plane 2 display position Y register m	P2DPYRm	H'*****	√	—	—	—
Plane 2 display position Y register	P2DPYR		—	√	√	√
Plane 2 display area start address 0 register m	P2DSA0Rm	H'*****	√	—	—	—
Plane 2 display area start address 0 register	P2DSA0R		—	√	√	√
Plane 2 display area start address 1 register m	P2DSA1Rm	H'*****	√	—	—	—
Plane 2 display area start address 1 register	P2DSA1R		—	√	√	√
Plane 2 display area start address 2 register m	P2DSA2Rm	H'*****	√	—	—	—
Plane 2 display area start address 2 register	P2DSA2R		—	√	√	√
Plane 2 start position X register m	P2SPXRm	H'*****	√	—	—	—
Plane 2 start position X register	P2SPXR		—	√	√	√
Plane 2 start position Y register m	P2SPYRm	H'*****	√	—	—	—
Plane 2 start position Y register	P2SPYR		—	√	√	√
Plane 2 wrap-around start position register m	P2WASPRm	H'*****	√	—	—	—
Plane 2 wrap-around start position register	P2WASPR		—	√	√	√
Plane 2 wrap-around memory width register m	P2WAMWRm	H'*****	√	—	—	—
Plane 2 wrap-around memory width register	P2WAMWR		—	√	√	√
Plane 2 blinking time register m	P2BTRm	H'****0101	√	—	—	—
Plane 2 blinking time register	P2BTR		—	√	√	√

Register Name	Abbr.	Power-on Reset	RZ/G Series Products			
			RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Plane 2 transparent color 1 register m	P2TC1Rm	H'*****	√	—	—	—
Plane 2 transparent color 1 register	P2TC1R		—	√	√	√
Plane 2 transparent color 2 register m	P2TC2Rm	H'*****	√	—	—	—
Plane 2 transparent color 2 register	P2TC2R		—	√	√	√
Plane 2 transparent color 3 register m	P2TC3Rm	H'*****	√	—	—	—
Plane 2 transparent color 3 register	P2TC3R		—	√	√	√
Plane 2 memory length register m	P2MLRm	H'****0000	√	—	—	—
Plane 2 memory length register	P2MLR		—	√	√	√
Plane 2 swap control register m	P2SWAPRm	H'*****0	√	—	—	—
Plane 2 swap control register	P2SWAPR		—	√	√	√
Plane 2 display data control register m	P2DDCRm	H'*****	√	—	—	—
Plane 2 display data control register	P2DDCR		—	√	√	√
Plane 2 display data control 2 register m	P2DDC2Rm	H'*****	√	—	—	—
Plane 2 display data control 2 register	P2DDC2R		—	√	√	√
Plane 2 display data control 4 register m	P2DDC4Rm	H'*****	√	—	—	—
Plane 2 display data control 4 register	P2DDC4R		—	√	√	√
Plane 3 mode register m	P3MRm	H'*****	√	—	—	—
Plane 3 mode register	P3MR		—	√	√	√
Plane 3 memory width register m	P3MWRm	H'*****	√	—	—	—
Plane 3 memory width register	P3MWR		—	√	√	√
Plane 3 blending ratio register m	P3ALPHARm	H'*****	√	—	—	—
Plane 3 blending ratio register	P3ALPHAR		—	√	√	√
Plane 3 display size X register m	P3DSXRm	H'*****	√	—	—	—
Plane 3 display size X register	P3DSXR		—	√	√	√
Plane 3 display size Y register m	P3DSYRm	H'*****	√	—	—	—
Plane 3 display size Y register	P3DSYR		—	√	√	√
Plane 3 display position X register m	P3DPXRm	H'*****	√	—	—	—
Plane 3 display position X register	P3DPXR		—	√	√	√
Plane 3 display position Y register m	P3DPYRm	H'*****	√	—	—	—
Plane 3 display position Y register	P3DPYR		—	√	√	√
Plane 3 display area start address 0 register m	P3DSA0Rm	H'*****	√	—	—	—
Plane 3 display area start address 0 register	P3DSA0R		—	√	√	√
Plane 3 display area start address 1 register m	P3DSA1Rm	H'*****	√	—	—	—
Plane 3 display area start address 1 register	P3DSA1R		—	√	√	√
Plane 3 display area start address 2 register m	P3DSA2Rm	H'*****	√	—	—	—
Plane 3 display area start address 2 register	P3DSA2R		—	√	√	√
Plane 3 start position X register m	P3SPXRm	H'*****	√	—	—	—
Plane 3 start position X register	P3SPXR		—	√	√	√



Register Name	Abbr.	Power-on Reset	RZ/G Series Products			
			RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Plane 3 start position Y register m	P3SPYRm	H'*****	√	—	—	—
Plane 3 start position Y register	P3SPYR		—	√	√	√
Plane 3 wrap-around start position register m	P3WASPRm	H'*****	√	—	—	—
Plane 3 wrap-around start position register	P3WASPR		—	√	√	√
Plane 3 wrap-around memory width register m	P3WAMWRm	H'*****	√	—	—	—
Plane 3 wrap-around memory width register	P3WAMWR		—	√	√	√
Plane 3 blinking time register m	P3BTRm	H'****0101	√	—	—	—
Plane 3 blinking time register	P3BTR		—	√	√	√
Plane 3 transparent color 1 register m	P3TC1Rm	H'*****	√	—	—	—
Plane 3 transparent color 1 register	P3TC1R		—	√	√	√
Plane 3 transparent color 2 register m	P3TC2Rm	H'*****	√	—	—	—
Plane 3 transparent color 2 register	P3TC2R		—	√	√	√
Plane 3 transparent color 3 register m	P3TC3Rm	H'*****	√	—	—	—
Plane 3 transparent color 3 register	P3TC3R		—	√	√	√
Plane 3 memory length register m	P3MLRm	H'****0000	√	—	—	—
Plane 3 memory length register	P3MLR		—	√	√	√
Plane 3 swap control register m	P3SWAPRm	H'*****0	√	—	—	—
Plane 3 swap control register	P3SWAPR		—	√	√	√
Plane 3 display data control register m	P3DDCRm	H'*****	√	—	—	—
Plane 3 display data control register	P3DDCR		—	√	√	√
Plane 3 display data control 2 register m	P3DDC2Rm	H'*****	√	—	—	—
Plane 3 display data control 2 register	P3DDC2R		—	√	√	√
Plane 3 display data control 4 register m	P3DDC4Rm	H'*****	√	—	—	—
Plane 3 display data control 4 register	P3DDC4R		—	√	√	√
Plane 4 mode register m	P4MRm	H'*****	√	—	—	—
Plane 4 mode register	P4MR		—	√	√	√
Plane 4 memory width register m	P4MWRm	H'*****	√	—	—	—
Plane 4 memory width register	P4MWR		—	√	√	√
Plane 4 blending ratio register m	P4ALPHARm	H'*****	√	—	—	—
Plane 4 blending ratio register	P4ALPHAR		—	√	√	√
Plane 4 display size X register m	P4DSXRm	H'*****	√	—	—	—
Plane 4 display size X register	P4DSXR		—	√	√	√
Plane 4 display size Y register m	P4DSYRm	H'*****	√	—	—	—
Plane 4 display size Y register	P4DSYR		—	√	√	√
Plane 4 display position X register m	P4DPXRm	H'*****	√	—	—	—
Plane 4 display position X register	P4DPXR		—	√	√	√
Plane 4 display position Y register m	P4DPYRm	H'*****	√	—	—	—
Plane 4 display position Y register	P4DPYR		—	√	√	√

Register Name	Abbr.	Power-on Reset	RZ/G Series Products			
			RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Plane 4 display area start address 0 register m	P4DSA0Rm	H'*****	√	—	—	—
Plane 4 display area start address 0 register	P4DSA0R		—	√	√	√
Plane 4 display area start address 1 register m	P4DSA1Rm	H'*****	√	—	—	—
Plane 4 display area start address 1 register	P4DSA1R		—	√	√	√
Plane 4 display area start address 2 register m	P4DSA2Rm	H'*****	√	—	—	—
Plane 4 display area start address 2 register	P4DSA2R		—	√	√	√
Plane 4 start position X register m	P4SPXRm	H'*****	√	—	—	—
Plane 4 start position X register	P4SPXR		—	√	√	√
Plane 4 start position Y register m	P4SPYRm	H'*****	√	—	—	—
Plane 4 start position Y register	P4SPYR		—	√	√	√
Plane 4 wrap-around start position register m	P4WASPRm	H'*****	√	—	—	—
Plane 4 wrap-around start position register	P4WASPR		—	√	√	√
Plane 4 wrap-around memory width register m	P4WAMWRm	H'*****	√	—	—	—
Plane 4 wrap-around memory width register	P4WAMWR		—	√	√	√
Plane 4 blinking time register m	P4BTRm	H'****0101	√	—	—	—
Plane 4 blinking time register	P4BTR		—	√	√	√
Plane 4 transparent color 1 register m	P4TC1Rm	H'*****	√	—	—	—
Plane 4 transparent color 1 register	P4TC1R		—	√	√	√
Plane 4 transparent color 2 register m	P4TC2Rm	H'*****	√	—	—	—
Plane 4 transparent color 2 register	P4TC2R		—	√	√	√
Plane 4 transparent color 3 register m	P4TC3Rm	H'*****	√	—	—	—
Plane 4 transparent color 3 register	P4TC3R		—	√	√	√
Plane 4 memory length register m	P4MLRm	H'****0000	√	—	—	—
Plane 4 memory length register	P4MLR		—	√	√	√
Plane 4 swap control register m	P4SWAPRm	H'*****0	√	—	—	—
Plane 4 swap control register	P4SWAPR		—	√	√	√
Plane 4 display data control register m	P4DDCRm	H'*****	√	—	—	—
Plane 4 display data control register	P4DDCR		—	√	√	√
Plane 4 display data control 2 register m	P4DDC2Rm	H'*****	√	—	—	—
Plane 4 display data control 2 register	P4DDC2R		—	√	√	√
Plane 4 display data control 4 register m	P4DDC4Rm	H'*****	√	—	—	—
Plane 4 display data control 4 register	P4DDC4R		—	√	√	√
Plane 5 mode register m	P5MRm	H'*****	√	—	—	—
Plane 5 mode register	P5MR		—	√	√	√
Plane 5 memory width register m	P5MWRm	H'*****	√	—	—	—
Plane 5 memory width register	P5MWR		—	√	√	√
Plane 5 blending ratio register m	P5ALPHARm	H'*****	√	—	—	—
Plane 5 blending ratio register	P5ALPHAR		—	√	√	√

Register Name	Abbr.	Power-on Reset	RZ/G Series Products			
			RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Plane 5 display size X register m	P5DSXRm	H'*****	√	—	—	—
Plane 5 display size X register	P5DSXR		—	√	√	√
Plane 5 display size Y register m	P5DSYRm	H'*****	√	—	—	—
Plane 5 display size Y register	P5DSYR		—	√	√	√
Plane 5 display position X register m	P5DPXRm	H'*****	√	—	—	—
Plane 5 display position X register	P5DPXR		—	√	√	√
Plane 5 display position Y register m	P5DPYRm	H'*****	√	—	—	—
Plane 5 display position Y register	P5DPYR		—	√	√	√
Plane 5 display area start address 0 register m	P5DSA0Rm	H'*****	√	—	—	—
Plane 5 display area start address 0 register	P5DSA0R		—	√	√	√
Plane 5 display area start address 1 register m	P5DSA1Rm	H'*****	√	—	—	—
Plane 5 display area start address 1 register	P5DSA1R		—	√	√	√
Plane 5 display area start address 2 register m	P5DSA2Rm	H'*****	√	—	—	—
Plane 5 display area start address 2 register	P5DSA2R		—	√	√	√
Plane 5 start position X register m	P5SPXRm	H'*****	√	—	—	—
Plane 5 start position X register	P5SPXR		—	√	√	√
Plane 5 start position Y register m	P5SPYRm	H'*****	√	—	—	—
Plane 5 start position Y register	P5SPYR		—	√	√	√
Plane 5 wrap-around start position register m	P5WASPRm	H'*****	√	—	—	—
Plane 5 wrap-around start position register	P5WASPR		—	√	√	√
Plane 5 wrap-around memory width register m	P5WAMWRm	H'*****	√	—	—	—
Plane 5 wrap-around memory width register	P5WAMWR		—	√	√	√
Plane 5 blinking time register m	P5BTRm	H'****0101	√	—	—	—
Plane 5 blinking time register	P5BTR		—	√	√	√
Plane 5 transparent color 1 register m	P5TC1Rm	H'*****	√	—	—	—
Plane 5 transparent color 1 register	P5TC1R		—	√	√	√
Plane 5 transparent color 2 register m	P5TC2Rm	H'*****	√	—	—	—
Plane 5 transparent color 2 register	P5TC2R		—	√	√	√
Plane 5 transparent color 3 register m	P5TC3Rm	H'*****	√	—	—	—
Plane 5 transparent color 3 register	P5TC3R		—	√	√	√
Plane 5 memory length register m	P5MLRm	H'****0000	√	—	—	—
Plane 5 memory length register	P5MLR		—	√	√	√
Plane 5 swap control register m	P5SWAPRm	H'*****0	√	—	—	—
Plane 5 swap control register	P5SWAPR		—	√	√	√
Plane 5 display data control register m	P5DDCRm	H'*****	√	—	—	—
Plane 5 display data control register	P5DDCR		—	√	√	√
Plane 5 display data control 2 register m	P5DDC2Rm	H'*****	√	—	—	—
Plane 5 display data control 2 register	P5DDC2R		—	√	√	√

			RZ/G Series Products			
Register Name	Abbr.	Power-on Reset	RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Plane 5 display data control 4 register m	P5DDC4Rm	H'*****	√	—	—	—
Plane 5 display data control 4 register	P5DDC4R		—	√	√	√
Plane 6 mode register m	P6MRm	H'*****	√	—	—	—
Plane 6 mode register	P6MR		—	√	√	√
Plane 6 memory width register m	P6MWRm	H'*****	√	—	—	—
Plane 6 memory width register	P6MWR		—	√	√	√
Plane 6 blending ratio register m	P6ALPHARm	H'*****	√	—	—	—
Plane 6 blending ratio register	P6ALPHAR		—	√	√	√
Plane 6 display size X register m	P6DSXRm	H'*****	√	—	—	—
Plane 6 display size X register	P6DSXR		—	√	√	√
Plane 6 display size Y register m	P6DSYRm	H'*****	√	—	—	—
Plane 6 display size Y register	P6DSYR		—	√	√	√
Plane 6 display position X register m	P6DPXRm	H'*****	√	—	—	—
Plane 6 display position X register	P6DPXR		—	√	√	√
Plane 6 display position Y register m	P6DPYRm	H'*****	√	—	—	—
Plane 6 display position Y register	P6DPYR		—	√	√	√
Plane 6 display area start address 0 register m	P6DSA0Rm	H'*****	√	—	—	—
Plane 6 display area start address 0 register	P6DSA0R		—	√	√	√
Plane 6 display area start address 1 register m	P6DSA1Rm	H'*****	√	—	—	—
Plane 6 display area start address 1 register	P6DSA1R		—	√	√	√
Plane 6 display area start address 2 register m	P6DSA2Rm	H'*****	√	—	—	—
Plane 6 display area start address 2 register	P6DSA2R		—	√	√	√
Plane 6 start position X register m	P6SPXRm	H'*****	√	—	—	—
Plane 6 start position X register	P6SPXR		—	√	√	√
Plane 6 start position Y register m	P6SPYRm	H'*****	√	—	—	—
Plane 6 start position Y register	P6SPYR		—	√	√	√
Plane 6 wrap-around start position register m	P6WASPRm	H'*****	√	—	—	—
Plane 6 wrap-around start position register	P6WASPR		—	√	√	√
Plane 6 wrap-around memory width register m	P6WAMWRm	H'*****	√	—	—	—
Plane 6 wrap-around memory width register	P6WAMWR		—	√	√	√
Plane 6 blinking time register m	P6BTRm	H'****0101	√	—	—	—
Plane 6 blinking time register	P6BTR		—	√	√	√
Plane 6 transparent color 1 register m	P6TC1Rm	H'*****	√	—	—	—
Plane 6 transparent color 1 register	P6TC1R		—	√	√	√
Plane 6 transparent color 2 register m	P6TC2Rm	H'*****	√	—	—	—
Plane 6 transparent color 2 register	P6TC2R		—	√	√	√
Plane 6 transparent color 3 register m	P6TC3Rm	H'*****	√	—	—	—
Plane 6 transparent color 3 register	P6TC3R		—	√	√	√

Register Name	Abbr.	Power-on Reset	RZ/G Series Products			
			RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Plane 6 memory length register m	P6MLRm	H'****0000	√	—	—	—
Plane 6 memory length register	P6MLR		—	√	√	√
Plane 6 swap control register m	P6SWAPRm	H'*****0	√	—	—	—
Plane 6 swap control register	P6SWAPR		—	√	√	√
Plane 6 display data control register m	P6DDCRm	H'*****	√	—	—	—
Plane 6 display data control register	P6DDCR		—	√	√	√
Plane 6 display data control 2 register m	P6DDC2Rm	H'*****	√	—	—	—
Plane 6 display data control 2 register	P6DDC2R		—	√	√	√
Plane 6 display data control 4 register m	P6DDC4Rm	H'*****	√	—	—	—
Plane 6 display data control 4 register	P6DDC4R		—	√	√	√
Plane 7 mode register m	P7MRm	H'*****	√	—	—	—
Plane 7 mode register	P7MR		—	√	√	√
Plane 7 memory width register m	P7MWRm	H'*****	√	—	—	—
Plane 7 memory width register	P7MWR		—	√	√	√
Plane 7 blending ratio register m	P7ALPHARm	H'*****	√	—	—	—
Plane 7 blending ratio register	P7ALPHAR		—	√	√	√
Plane 7 display size X register m	P7DSXRm	H'*****	√	—	—	—
Plane 7 display size X register	P7DSXR		—	√	√	√
Plane 7 display size Y register m	P7DSYRm	H'*****	√	—	—	—
Plane 7 display size Y register	P7DSYR		—	√	√	√
Plane 7 display position X register m	P7DPXRm	H'*****	√	—	—	—
Plane 7 display position X register	P7DPXR		—	√	√	√
Plane 7 display position Y register m	P7DPYRm	H'*****	√	—	—	—
Plane 7 display position Y register	P7DPYR		—	√	√	√
Plane 7 display area start address 0 register m	P7DSA0Rm	H'*****	√	—	—	—
Plane 7 display area start address 0 register	P7DSA0R		—	√	√	√
Plane 7 display area start address 1 register m	P7DSA1Rm	H'*****	√	—	—	—
Plane 7 display area start address 1 register	P7DSA1R		—	√	√	√
Plane 7 display area start address 2 register m	P7DSA2Rm	H'*****	√	—	—	—
Plane 7 display area start address 2 register	P7DSA2R		—	√	√	√
Plane 7 start position X register m	P7SPXRm	H'*****	√	—	—	—
Plane 7 start position X register	P7SPXR		—	√	√	√
Plane 7 start position Y register m	P7SPYRm	H'*****	√	—	—	—
Plane 7 start position Y register	P7SPYR		—	√	√	√
Plane 7 wrap-around start position register m	P7WASPRm	H'*****	√	—	—	—
Plane 7 wrap-around start position register	P7WASPR		—	√	√	√
Plane 7 wrap-around memory width register m	P7WAMWRm	H'*****	√	—	—	—
Plane 7 wrap-around memory width register	P7WAMWR		—	√	√	√

			RZ/G Series Products			
Register Name	Abbr.	Power-on Reset	RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Plane 7 blinking time register m	P7BTRm	H'****0101	√	—	—	—
Plane 7 blinking time register	P7BTR		—	√	√	√
Plane 7 transparent color 1 register m	P7TC1Rm	H'*****	√	—	—	—
Plane 7 transparent color 1 register	P7TC1R		—	√	√	√
Plane 7 transparent color 2 register m	P7TC2Rm	H'*****	√	—	—	—
Plane 7 transparent color 2 register	P7TC2R		—	√	√	√
Plane 7 transparent color 3 register m	P7TC3Rm	H'*****	√	—	—	—
Plane 7 transparent color 3 register	P7TC3R		—	√	√	√
Plane 7 memory length register m	P7MLRm	H'****0000	√	—	—	—
Plane 7 memory length register	P7MLR		—	√	√	√
Plane 7 swap control register m	P7SWAPRm	H'*****0	√	—	—	—
Plane 7 swap control register	P7SWAPR		—	√	√	√
Plane 7 display data control register m	P7DDCRm	H'*****	√	—	—	—
Plane 7 display data control register	P7DDCR		—	√	√	√
Plane 7 display data control 2 register m	P7DDC2Rm	H'*****	√	—	—	—
Plane 7 display data control 2 register	P7DDC2R		—	√	√	√
Plane 7 display data control 4 register m	P7DDC4Rm	H'*****	√	—	—	—
Plane 7 display data control 4 register	P7DDC4R		—	√	√	√
Plane 8 mode register m	P8MRm	H'*****	√	—	—	—
Plane 8 mode register	P8MR		—	√	√	√
Plane 8 memory width register m	P8MWRm	H'*****	√	—	—	—
Plane 8 memory width register	P8MWR		—	√	√	√
Plane 8 blending ratio register m	P8ALPHARm	H'*****	√	—	—	—
Plane 8 blending ratio register	P8ALPHAR		—	√	√	√
Plane 8 display size X register m	P8DSXRm	H'*****	√	—	—	—
Plane 8 display size X register	P8DSXR		—	√	√	√
Plane 8 display size Y register m	P8DSYRm	H'*****	√	—	—	—
Plane 8 display size Y register	P8DSYR		—	√	√	√
Plane 8 display position X register m	P8DPXRm	H'*****	√	—	—	—
Plane 8 display position X register	P8DPXR		—	√	√	√
Plane 8 display position Y register m	P8DPYRm	H'*****	√	—	—	—
Plane 8 display position Y register	P8DPYR		—	√	√	√
Plane 8 display area start address 0 register m	P8DSA0Rm	H'*****	√	—	—	—
Plane 8 display area start address 0 register	P8DSA0R		—	√	√	√
Plane 8 display area start address 1 register m	P8DSA1Rm	H'*****	√	—	—	—
Plane 8 display area start address 1 register	P8DSA1R		—	√	√	√
Plane 8 display area start address 2 register m	P8DSA2Rm	H'*****	√	—	—	—
Plane 8 display area start address 2 register	P8DSA2R		—	√	√	√

Register Name	Abbr.	Power-on Reset	RZ/G Series Products			
			RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Plane 8 start position X register m	P8SPXRm	H'*****	√	—	—	—
Plane 8 start position X register	P8SPXR		—	√	√	√
Plane 8 start position Y register m	P8SPYRm	H'*****	√	—	—	—
Plane 8 start position Y register	P8SPYR		—	√	√	√
Plane 8 wrap-around start position register m	P8WASPRm	H'*****	√	—	—	—
Plane 8 wrap-around start position register	P8WASPR		—	√	√	√
Plane 8 wrap-around memory width register m	P8WAMWRm	H'*****	√	—	—	—
Plane 8 wrap-around memory width register	P8WAMWR		—	√	√	√
Plane 8 blinking time register m	P8BTRm	H'****0101	√	—	—	—
Plane 8 blinking time register	P8BTR		—	√	√	√
Plane 8 transparent color 1 register m	P8TC1Rm	H'*****	√	—	—	—
Plane 8 transparent color 1 register	P8TC1R		—	√	√	√
Plane 8 transparent color 2 register m	P8TC2Rm	H'*****	√	—	—	—
Plane 8 transparent color 2 register	P8TC2R		—	√	√	√
Plane 8 transparent color 3 register m	P8TC3Rm	H'*****	√	—	—	—
Plane 8 transparent color 3 register	P8TC3R		—	√	√	√
Plane 8 memory length register m	P8MLRm	H'****0000	√	—	—	—
Plane 8 memory length register	P8MLR		—	√	√	√
Plane 8 swap control register m	P8SWAPRm	H'*****0	√	—	—	—
Plane 8 swap control register	P8SWAPR		—	√	√	√
Plane 8 display data control register m	P8DDCRm	H'*****	√	—	—	—
Plane 8 display data control register	P8DDCR		—	√	√	√
Plane 8 display data control 2 register m	P8DDC2Rm	H'*****	√	—	—	—
Plane 8 display data control 2 register	P8DDC2R		—	√	√	√
Plane 8 display data control 4 register m	P8DDC4Rm	H'*****	√	—	—	—
Plane 8 display data control 4 register	P8DDC4R		—	√	√	√

Note: m = 0 and 2 [Only for RZ/G1H]

**(e) Alpha Plane Register Configuration****Table 21.10 Alpha Plane Register Configuration (1)**

Base address: DU0: H'FEB0 0000 (suffix 0)  
DU2: H'FEB4 0000 (suffix 2) [Only for RZ/G1H]

Register Name	Abbr.	R/W	Offset Address	Access Size	Bit with Internal Update Function	RZ/G Series Products			
						RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Alpha-ratio plane 1 mode register m	AP1MRm	R/W	H'A100	32 bits	All bits	√	—	—	—
Alpha-ratio plane 1 mode register	AP1MR					—	√	√	√
Alpha-ratio plane 1 memory width register m	AP1MWRm	R/W	H'A104	32 bits	All bits	√	—	—	—
Alpha-ratio plane 1 memory width register	AP1MWR					—	√	√	√
Alpha-ratio plane 1 display size X register m	AP1DSXRm	R/W	H'A110	32 bits	All bits	√	—	—	—
Alpha-ratio plane 1 display size X register	AP1DSXR					—	√	√	√
Alpha-ratio plane 1 display size Y register m	AP1DSYRm	R/W	H'A114	32 bits	All bits	√	—	—	—
Alpha-ratio plane 1 display size Y register	AP1DSYR					—	√	√	√
Alpha-ratio plane 1 display position X register m	AP1DPXRm	R/W	H'A118	32 bits	All bits	√	—	—	—
Alpha-ratio plane 1 display position X register	AP1DPXR					—	√	√	√
Alpha-ratio plane 1 display position Y register m	AP1DPYRm	R/W	H'A11C	32 bits	All bits	√	—	—	—
Alpha-ratio plane 1 display position Y register	AP1DPYR					—	√	√	√
Alpha-ratio plane 1 display area start address 0 register m	AP1DSA0Rm	R/W	H'A120	32 bits	All bits	√	—	—	—
Alpha-ratio plane 1 display area start address 0 register	AP1DSA0R					—	√	√	√
Alpha-ratio plane 1 display area start address 1 register m	AP1DSA1Rm	R/W	H'A124	32 bits	All bits	√	—	—	—
Alpha-ratio plane 1 display area start address 1 register	AP1DSA1R					—	√	√	√
Alpha-ratio plane 1 start position X register m	AP1SPXRm	R/W	H'A130	32 bits	All bits	√	—	—	—
Alpha-ratio plane 1 start position X register	AP1SPXR					—	√	√	√
Alpha-ratio plane 1 start position Y register m	AP1SPYRm	R/W	H'A134	32 bits	All bits	√	—	—	—
Alpha-ratio plane 1 start position Y register	AP1SPYR					—	√	√	√
Alpha-ratio plane 1 wrap-around start position register m	AP1WASPRm	R/W	H'A138	32 bits	All bits	√	—	—	—
Alpha-ratio plane 1 wrap-around start position register	AP1WASPR					—	√	√	√
Alpha-ratio plane 1 wrap-around memory width register m	AP1WAMWRm	R/W	H'A13C	32 bits	All bits	√	—	—	—
Alpha-ratio plane 1 wrap-around memory width register	AP1WAMWR					—	√	√	√
Alpha-ratio plane 1 blinking time register m	AP1BTRm	R/W	H'A140	32 bits	All bits	√	—	—	—
Alpha-ratio plane 1 blinking time register	AP1BTR					—	√	√	√
Alpha-ratio plane 1 memory length register m	AP1MLRm	R/W	H'A150	32 bits	All bits	√	—	—	—
Alpha-ratio plane 1 memory length register	AP1MLR					—	√	√	√



							<b>RZ/G Series Products</b>			
<b>Register Name</b>	<b>Abbr.</b>	<b>R/W</b>	<b>Offset Address</b>	<b>Access Size</b>	<b>Bit with Internal Update Function</b>	<b>RZ/G1H</b>	<b>RZ/G1M</b>	<b>RZ/G1N</b>	<b>RZ/G1E</b>	
Alpha-ratio plane 1 swap control register m	AP1SWAPRm	R/W	H'A180	32 bits	All bits	√	—	—	—	
Alpha-ratio plane 1 swap control register	AP1SWAPR					—	√	√	√	
Alpha-ratio plane 1 display data control 4 register m	AP1DDC4Rm	R/W	H'A190	32 bits	All bits	√	—	—	—	
Alpha-ratio plane 1 display data control 4 register	AP1DDC4R					—	√	√	√	
Alpha-ratio plane 2 mode register m	AP2MRm	R/W	H'A200	32 bits	All bits	√	—	—	—	
Alpha-ratio plane 2 mode register	AP2MR					—	√	√	√	
Alpha-ratio plane 2 memory width register m	AP2MWRm	R/W	H'A204	32 bits	All bits	√	—	—	—	
Alpha-ratio plane 2 memory width register	AP2MWR					—	√	√	√	
Alpha-ratio plane 2 display size X register m	AP2DSXRm	R/W	H'A210	32 bits	All bits	√	—	—	—	
Alpha-ratio plane 2 display size X register	AP2DSXR					—	√	√	√	
Alpha-ratio plane 2 display size Y register m	AP2DSYRm	R/W	H'A214	32 bits	All bits	√	—	—	—	
Alpha-ratio plane 2 display size Y register	AP2DSYR					—	√	√	√	
Alpha-ratio plane 2 display position X register m	AP2DPXRm	R/W	H'A218	32 bits	All bits	√	—	—	—	
Alpha-ratio plane 2 display position X register	AP2DPXR					—	√	√	√	
Alpha-ratio plane 2 display position Y register m	AP2DPYRm	R/W	H'A21C	32 bits	All bits	√	—	—	—	
Alpha-ratio plane 2 display position Y register	AP2DPYR					—	√	√	√	
Alpha-ratio plane 2 display area start address 0 register m	AP2DSA0Rm	R/W	H'A220	32 bits	All bits	√	—	—	—	
Alpha-ratio plane 2 display area start address 0 register	AP2DSA0R					—	√	√	√	
Alpha-ratio plane 2 display area start address 1 register m	AP2DSA1Rm	R/W	H'A224	32 bits	All bits	√	—	—	—	
Alpha-ratio plane 2 display area start address 1 register	AP2DSA1R					—	√	√	√	
Alpha-ratio plane 2 start position X register m	AP2SPXRm	R/W	H'A230	32 bits	All bits	√	—	—	—	
Alpha-ratio plane 2 start position X register	AP2SPXR					—	√	√	√	
Alpha-ratio plane 2 start position Y register m	AP2SPYRm	R/W	H'A234	32 bits	All bits	√	—	—	—	
Alpha-ratio plane 2 start position Y register	AP2SPYR					—	√	√	√	
Alpha-ratio plane 2 wrap-around start position register m	AP2WASPRm	R/W	H'A238	32 bits	All bits	√	—	—	—	
Alpha-ratio plane 2 wrap-around start position register	AP2WASPR					—	√	√	√	
Alpha-ratio plane 2 wrap-around memory width register m	AP2WAMWRm	R/W	H'A23C	32 bits	All bits	√	—	—	—	
Alpha-ratio plane 2 wrap-around memory width register	AP2WAMWR					—	√	√	√	
Alpha-ratio plane 2 blinking time register m	AP2BTRm	R/W	H'A240	32 bits	All bits	√	—	—	—	
Alpha-ratio plane 2 blinking time register	AP2BTR					—	√	√	√	
Alpha-ratio plane 2 memory length register m	AP2MLRm	R/W	H'A250	32 bits	All bits	√	—	—	—	
Alpha-ratio plane 2 memory length register	AP2MLR					—	√	√	√	

Register Name	Abbr.	R/W	Offset Address	Access Size	Bit with Internal Update Function	RZ/G Series Products			
						RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Alpha-ratio plane 2 swap control register m	AP2SWAPRm	R/W	H'A280	32 bits	All bits	√	—	—	—
Alpha-ratio plane 2 swap control register	AP2SWAPR					—	√	√	√
Alpha-ratio plane 2 display data control 4 register m	AP2DDC4Rm	R/W	H'A290	32 bits	All bits	√	—	—	—
Alpha-ratio plane 2 display data control 4 register	AP2DDC4R					—	√	√	√

Note: m = 0 and 2 [Only for RZ/G1H]

Table 21.11 Alpha Plane Register Configuration (2)

Register Name	Abbr.	Power-on Reset	RZ/G Series Products			
			RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Alpha-ratio plane 1 mode register m	AP1MRm	H'*****	√	—	—	—
Alpha-ratio plane 1 mode register	AP1MR		—	√	√	√
Alpha-ratio plane 1 memory width register m	AP1MWRm	H'*****	√	—	—	—
Alpha-ratio plane 1 memory width register	AP1MWR		—	√	√	√
Alpha-ratio plane 1 display size X register m	AP1DSXRm	H'*****	√	—	—	—
Alpha-ratio plane 1 display size X register	AP1DSXR		—	√	√	√
Alpha-ratio plane 1 display size Y register m	AP1DSYRm	H'*****	√	—	—	—
Alpha-ratio plane 1 display size Y register	AP1DSYR		—	√	√	√
Alpha-ratio plane 1 display position X register m	AP1DPXRm	H'*****	√	—	—	—
Alpha-ratio plane 1 display position X register	AP1DPXR		—	√	√	√
Alpha-ratio plane 1 display position Y register m	AP1DPYRm	H'*****	√	—	—	—
Alpha-ratio plane 1 display position Y register	AP1DPYR		—	√	√	√
Alpha-ratio plane 1 display area start address 0 register m	AP1DSA0Rm	H'*****	√	—	—	—
Alpha-ratio plane 1 display area start address 0 register	AP1DSA0R		—	√	√	√
Alpha-ratio plane 1 display area start address 1 register m	AP1DSA1Rm	H'*****	√	—	—	—
Alpha-ratio plane 1 display area start address 1 register	AP1DSA1R		—	√	√	√
Alpha-ratio plane 1 start position X register m	AP1SPXRm	H'*****	√	—	—	—
Alpha-ratio plane 1 start position X register	AP1SPXR		—	√	√	√
Alpha-ratio plane 1 start position Y register m	AP1SPYRm	H'*****	√	—	—	—
Alpha-ratio plane 1 start position Y register	AP1SPYR		—	√	√	√
Alpha-ratio plane 1 wrap-around start position register m	AP1WASPRm	H'*****	√	—	—	—
Alpha-ratio plane 1 wrap-around start position register	AP1WASPR		—	√	√	√
Alpha-ratio plane 1 wrap-around memory width register m	AP1WAMWRm	H'*****	√	—	—	—
Alpha-ratio plane 1 wrap-around memory width register	AP1WAMWR		—	√	√	√
Alpha-ratio plane 1 blinking time register m	AP1BTRm	H'****0101	√	—	—	—
Alpha-ratio plane 1 blinking time register	AP1BTR		—	√	√	√
Alpha-ratio plane 1 memory length register m	AP1MLRm	H'****0000	√	—	—	—
Alpha-ratio plane 1 memory length register	AP1MLR		—	√	√	√
Alpha-ratio plane 1 swap control register m	AP1SWAPRm	H'*****0	√	—	—	—
Alpha-ratio plane 1 swap control register	AP1SWAPR		—	√	√	√
Alpha-ratio plane 1 display data control 4 register m	AP1DDC4Rm	H'*****	√	—	—	—
Alpha-ratio plane 1 display data control 4 register	AP1DDC4R		—	√	√	√
Alpha-ratio plane 2 mode register m	AP2MRm	H'*****	√	—	—	—
Alpha-ratio plane 2 mode register	AP2MR		—	√	√	√
Alpha-ratio plane 2 memory width register m	AP2MWRm	H'*****	√	—	—	—
Alpha-ratio plane 2 memory width register	AP2MWR		—	√	√	√
Alpha-ratio plane 2 display size X register m	AP2DSXRm	H'*****	√	—	—	—
Alpha-ratio plane 2 display size X register	AP2DSXR		—	√	√	√

			RZ/G Series Products			
Register Name	Abbr.	Power-on Reset	RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Alpha-ratio plane 2 display size Y register m	AP2DSYRm	H'*****	√	—	—	—
Alpha-ratio plane 2 display size Y register	AP2DSYR		—	√	√	√
Alpha-ratio plane 2 display position X register m	AP2DPXRm	H'*****	√	—	—	—
Alpha-ratio plane 2 display position X register	AP2DPXR		—	√	√	√
Alpha-ratio plane 2 display position Y register m	AP2DPYRm	H'*****	√	—	—	—
Alpha-ratio plane 2 display position Y register	AP2DPYR		—	√	√	√
Alpha-ratio plane 2 display area start address 0 register m	AP2DSA0Rm	H'*****	√	—	—	—
Alpha-ratio plane 2 display area start address 0 register	AP2DSA0R		—	√	√	√
Alpha-ratio plane 2 display area start address 1 register m	AP2DSA1Rm	H'*****	√	—	—	—
Alpha-ratio plane 2 display area start address 1 register	AP2DSA1R		—	√	√	√
Alpha-ratio plane 2 start position X register m	AP2SPXRm	H'*****	√	—	—	—
Alpha-ratio plane 2 start position X register	AP2SPXR		—	√	√	√
Alpha-ratio plane 2 start position Y register m	AP2SPYRm	H'*****	√	—	—	—
Alpha-ratio plane 2 start position Y register	AP2SPYR		—	√	√	√
Alpha-ratio plane 2 wrap-around start position register m	AP2WASPRm	H'*****	√	—	—	—
Alpha-ratio plane 2 wrap-around start position register	AP2WASPR		—	√	√	√
Alpha-ratio plane 2 wrap-around memory width register m	AP2WAMWRm	H'*****	√	—	—	—
Alpha-ratio plane 2 wrap-around memory width register	AP2WAMWR		—	√	√	√
Alpha-ratio plane 2 blinking time register m	AP2BTRm	H'***0101	√	—	—	—
Alpha-ratio plane 2 blinking time register	AP2BTR		—	√	√	√
Alpha-ratio plane 2 memory length register m	AP2MLRm	H'***0000	√	—	—	—
Alpha-ratio plane 2 memory length register	AP2MLR		—	√	√	√
Alpha-ratio plane 2 swap control register m	AP2SWAPRm	H'*****0	√	—	—	—
Alpha-ratio plane 2 swap control register	AP2SWAPR		—	√	√	√
Alpha-ratio plane 2 display data control 4 register m	AP2DDC4Rm	H'*****	√	—	—	—
Alpha-ratio plane 2 display data control 4 register	AP2DDC4R		—	√	√	√

Note: m = 0 and 2 [Only for RZ/G1H]

**(f) Display Capture Register Configuration****Table 21.12 Display Capture Register Configuration (1)**

Base address: DU0: H'FEB0 0000 (suffix 0)  
 DU2: H'FEB4 0000 (suffix 2) [Only for RZ/G1H]

Register Name	Abbr.	R/W	Offset Address	Access Size	Bit with Internal Update Function	RZ/G Series Products			
						RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Display capture mode register m	DCMRm	R/W	H'C100	32 bits	All bits	√	—	—	—
Display capture mode register	DCMR					—	√	√	√
Display capture memory width register m	DCMWRm	R/W	H'C104	32 bits	All bits	√	—	—	—
Display capture memory width register	DCMWR					—	√	√	√
Display capture area start address register m	DCSARm	R/W	H'C120	32 bits	All bits	√	—	—	—
Display capture area start address register	DCSAR					—	√	√	√
Display capture memory length register m	DCMLRm	R/W	H'C150	32 bits	All bits	√	—	—	—
Display capture memory length register	DCMLR					—	√	√	√
Display capture 2 mode register m	DC2MRm	R/W	H'C200	32 bits	All bits	√	—	—	—
Display capture 2 mode register	DC2MR					—	√	√	√
Display capture 2 memory width register 0	DC2MWR0	R/W	H'C204	32 bits	All bits	√	—	—	—
Display capture 2 memory width register	DC2MWR					—	√	√	√
Display capture 2 area start address register 0	DC2SAR0	R/W	H'C220	32 bits	All bits	√	—	—	—
Display capture 2 area start address register	DC2SAR					—	√	√	√
Display capture 2 memory length register 0	DC2MLR0	R/W	H'C250	32 bits	All bits	√	—	—	—
Display capture 2 memory length register	DC2MLR					—	√	√	√

Note: m = 0 and 2 [Only for RZ/G1H]

**Table 21.13 Display Capture Register Configuration (2)**

Register Name	Abbr.	Power-on Reset	RZ/G Series Products			
			RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Display capture mode register m	DCMRm	H'****00**	√	—	—	—
Display capture mode register	DCMR		—	√	√	√
Display capture memory width register m	DCMWRm	H'*****	√	—	—	—
Display capture memory width register	DCMWR		—	√	√	√
Display capture area start address register m	DCSARm	H'*****	√	—	—	—
Display capture area start address register	DCSAR		—	√	√	√
Display capture memory length register m	DCMLRm	H'****0000	√	—	—	—
Display capture memory length register	DCMLR		—	√	√	√
Display capture 2 mode register 0	DC2MR0	H'****00**	√	—	—	—
Display capture 2 mode register	DC2MR		—	√	√	√
Display capture 2 memory width register 0	DC2MWR0	H'*****	√	—	—	—
Display capture 2 memory width register	DC2MWR		—	√	√	√
Display capture 2 area start address register 0	DC2SAR0	H'*****	√	—	—	—
Display capture 2 area start address register	DC2SAR		—	√	√	√
Display capture 2 memory length register 0	DC2MLR0	H'****0000	√	—	—	—
Display capture 2 memory length register	DC2MLR		—	√	√	√

Note: m = 0 and 2 [Only for RZ/G1H]

**(g) Color Palette Register Configuration****Table 21.14 Color Palette Register Configuration (1)**

Base address: DU0: H'FEB0 0000 (suffix 0)  
 DU2: H'FEB4 0000 (suffix 2) [Only for RZ/G1H]

Register Name	Abbr.	R/W	Offset Address	Access Size	Bit with Internal Update Function	RZ/G Series Products				
						RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E	
Color palette 1_000 register m	CP1_000Rm	R/W	H'1000	32 bits	All bits	√	—	—	—	
Color palette 1_000 register	CP1_000R					—	√	√	√	
to										
Color palette 1_255 register m	CP1_255Rm	R/W	H'13FC	32 bits	All bits	√	—	—	—	
Color palette 1_255 register	CP1_255R					—	√	√	√	
Color palette 2_000 register m	CP2_000Rm	R/W	H'2000	32 bits	All bits	√	—	—	—	
Color palette 2_000 register	CP2_000R					—	√	√	√	
to										
Color palette 2_255 register m	CP2_255Rm	R/W	H'23FC	32 bits	All bits	√	—	—	—	
Color palette 2_255 register	CP2_255R					—	√	√	√	
Color palette 3_000 register m	CP3_000Rm	R/W	H'3000	32 bits	All bits	√	—	—	—	
Color palette 3_000 register	CP3_000R					—	√	√	√	
to										
Color palette 3_255 register m	CP3_255Rm	R/W	H'33FC	32 bits	All bits	√	—	—	—	
Color palette 3_255 register	CP3_255R					—	√	√	√	
Color palette 4_000 register m	CP4_000Rm	R/W	H'4000	32 bits	All bits	√	—	—	—	
Color palette 4_000 register	CP4_000R					—	√	√	√	
to										
Color palette 4_255 register m	CP4_255Rm	R/W	H'43FC	32 bits	All bits	√	—	—	—	
Color palette 4_255 register	CP4_255R					—	√	√	√	

Note: m = 0 and 2 [Only for RZ/G1H]

Table 21.15 Color Palette Register Configuration (2)

Register Name	Abbr.	Power-on Reset	RZ/G Series Products			
			RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Color palette 1_000 register m	CP1_000Rm	H'*****	√	—	—	—
Color palette 1_000 register	CP1_000R		—	√	√	√
to						
Color palette 1_255 register m	CP1_255Rm	H'*****	√	—	—	—
Color palette 1_255 register	CP1_255R		—	√	√	√
Color palette 2_000 register m	CP2_000Rm	H'*****	√	—	—	—
Color palette 2_000 register	CP2_000R		—	√	√	√
to						
Color palette 2_255 register m	CP2_255Rm	H'*****	√	—	—	—
Color palette 2_255 register	CP2_255R		—	√	√	√
Color palette 3_000 register m	CP3_000Rm	H'*****	√	—	—	—
Color palette 3_000 register	CP3_000R		—	√	√	√
to						
Color palette 3_255 register m	CP3_255Rm	H'*****	√	—	—	—
Color palette 3_255 register	CP3_255R		—	√	√	√
Color palette 4_000 register m	CP4_000Rm	H'*****	√	—	—	—
Color palette 4_000 register	CP4_000R		—	√	√	√
to						
Color palette 4_255 register m	CP4_255Rm	H'*****	√	—	—	—
Color palette 4_255 register	CP4_255R		—	√	√	√

Note: m = 0 and 2 [Only for RZ/G1H]



**(h) External Synchronization Control Register Configuration****Table 21.16 External Synchronization Control Register Configuration (1)**

Base address: DU0: H'FEB1 0000 (suffix 0)  
 DU1: H'FEB3 0000 (suffix 1)  
 DU2: H'FEB5 0000 (suffix 2) [Only for RZ/G1H]

Register Name	Abbr.	R/W	Offset Address	Access Size	Bit with Internal Update Function*	RZ/G Series Products			
						RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
External synchronization control register n	ESCR0	R/W	H'0000	32 bits	None	√	√	√	√
	ESCR1					√	√	√	√
	ESCR2					√	—	—	—
Output signal timing adjustment register n	OTAR0	R/W	H'0004	32 bits	All bits updated with DRES	√	√	√	√
	OTAR1					√	√	√	√
	OTAR2					√	—	—	—

Note: n = 0 to 2 [RZ/G1H]  
 n = 0 and 1 [RZ/G1M/N/E]

**Table 21.17 External Synchronization Control Register Configuration (2)**

Register Name	Abbr.	Power-on Reset	RZ/G Series Products			
			RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
External synchronization control register n	ESCR0	H'*****0	√	√	√	√
	ESCR1		√	√	√	√
	ESCR2		√	—	—	—
Output signal timing adjustment register n	OTAR0	H'*****	√	√	√	√
	OTAR1		√	√	√	√
	OTAR2		√	—	—	—

Note: n = 0 to 2 [RZ/G1H]  
 n = 0 and 1 [RZ/G1M /N /E]

**(i) Dual Display Output Control Register Configuration****Table 21.18 Dual Display Output Control Register Configuration (1)**

Base address: DU0: H'FEB1 0000 (suffix 0)  
 DU2: H'FEB5 0000 (suffix 2) [Only for RZ/G1H]

Register Name	Abbr.	R/W	Offset Address	Access Size	Bit with Internal Update Function	RZ/G Series Products			
						RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Display unit output route control register m	DORCRm	R/W	H'1000	32 bits	All bits updated with DRES	√	—	—	—
Display unit output route control register	DORCR					—	√	√	√
Display plane timing select register	DPTSR	R/W	H'1004	32 bits	All bits updated with DRES	√	√	√	√
Display alpha plane timing select register	DAPTSR	R/W	H'1008	32 bits	All bits updated with DRES	√	√	√	√
Display superimpose 0 priority register m	DS0PRm	R/W	H'1020	32 bits	All bits	√	—	—	—
Display superimpose 0 priority register	DS0PR					—	√	√	√
Display superimpose 1 priority register	DS1PR	R/W	H'1024	32 bits	All bits	√	√	√	√

Note: m = 0 and 2 [Only for RZ/G1H]

**Table 21.19 Dual Display Output Control Register Configuration (2)**

Register Name	Abbr.	Power-on Reset	RZ/G Series Products			
			RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Display unit output route control register 0	DORCR0	H'*****0**	√	—	—	—
Display unit output route control register	DORCR		—	√	√	√
Display unit output route control register 2	DORCR2	H'*****	√	—	—	—
Display plane timing select register	DPTSR	H'**00**00	√	√	√	√
Display alpha plane timing select register	DAPTSR	H'*****	√	√	√	√
Display superimpose 0 priority register m	DS0PRm	H'00000000	√	—	—	—
Display superimpose 0 priority register	DS0PR		—	√	√	√
Display superimpose 1 priority register	DS1PR	H'00000000	√	√	√	√

Note: m = 0 and 2 [Only for RZ/G1H]

**(j) YC-RGB Conversion Coefficient Register Configuration****Table 21.20 YC-RGB Conversion Coefficient Register Configuration (1)**

Base address: DU0: H'FEB1 1000(suffix 0)

DU0: H'FEB1 4000 (suffix 0) [Only for RZ/G1H]

DU2: H'FEB5 1000, H'FEB5 4000 (suffix 2) [Only for RZ/G1H]

Register Name	Abbr.	R/W	Address in P4	Access Size	Bit with Internal Update Function	RZ/G Series Products			
						RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Y normalization coefficient register m	YNCRm	R/W	H'80	32 bits	All bits	√	—	—	—
Y normalization coefficient register	YNCR					—	√	√	√
Y normalization offset register m	YNORM	R/W	H'84	32 bits	All bits	√	—	—	—
Y normalization offset register	YNOR					—	√	√	√
Cr normalization offset register m	CRNORM	R/W	H'88	32 bits	All bits	√	—	—	—
Cr normalization offset register	CRNOR					—	√	√	√
Cb normalization offset register m	CBNORM	R/W	H'8C	32 bits	All bits	√	—	—	—
Cb normalization offset register	CBNOR					—	√	√	√
Red Cr coefficient register m	RCRCRm	R/W	H'90	32 bits	All bits	√	—	—	—
Red Cr coefficient register	RCRCR					—	√	√	√
Green Cr coefficient register m	GRCRCRm	R/W	H'94	32 bits	All bits	√	—	—	—
Green Cr coefficient register	GRCRCR					—	√	√	√
Green Cb coefficient register m	GCBCRm	R/W	H'98	32 bits	All bits	√	—	—	—
Green Cb coefficient register	GCBCR					—	√	√	√
Blue Cb coefficient register m	BCBCRm	R/W	H'9C	32 bits	All bits	√	—	—	—
Blue Cb coefficient register	BCBCR					—	√	√	√

Note: m = 0 and 2 [Only for RZ/G1H]

**Table 21.21 YC-RGB Conversion Coefficient Register Configuration (2)**

Register Name	Abbr.	Power-on Reset	RZ/G Series Products			
			RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Y normalization coefficient register m	YNCRm	H'*800*800	√	—	—	—
Y normalization coefficient register	YNCR		—	√	√	√
Y normalization offset register m	YNORM	H'**00**00	√	—	—	—
Y normalization offset register	YNOR		—	√	√	√
Cr normalization offset register m	CRNORM	H'**80**80	√	—	—	—
Cr normalization offset register	CRNOR		—	√	√	√
Cb normalization offset register m	CBNORM	H'**80**80	√	—	—	—
Cb normalization offset register	CBNOR		—	√	√	√
Red Cr coefficient register m	RCRCRm	H'*AF0*AF0	√	—	—	—
Red Cr coefficient register	RCRCR		—	√	√	√
Green Cr coefficient register m	GRCRCRm	H'*590*590	√	—	—	—
Green Cr coefficient register	GRCRCR		—	√	√	√
Green Cb coefficient register m	GCBCRm	H'*2B0*2B0	√	—	—	—
Green Cb coefficient register	GCBCR		—	√	√	√
Blue Cb coefficient register m	BCBCRm	H'*DE0*DE0	√	—	—	—
Blue Cb coefficient register	BCBCR		—	√	√	√

Note: m = 0 and 2 [Only for RZ/G1H]

**(k) RGB-YC Conversion Coefficient Register Configuration****Table 21.22 RGB-YC Conversion Coefficient Register Configuration (1)**

Base address: DU0: H'FEB1 0000

Register Name	Abbr.	R/W	Offset Address	Access Size	Bit with Internal Update Function	RZ/G Series Products			
						RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Y calculation R coefficient register	YCLRP	R/W	H'4000	32 bits	All bits	—	√	√	√
Y calculation G coefficient register	YCLGP	R/W	H'4004	32 bits	All bits	—	√	√	√
Y calculation B coefficient register	YCLBP	R/W	H'4008	32 bits	All bits	—	√	√	√
Y calculation addition constant register	YCLAP	R/W	H'400C	32 bits	All bits	—	√	√	√
Cb calculation R coefficient register	CBCLRP	R/W	H'4010	32 bits	All bits	—	√	√	√
Cb calculation G coefficient register	CBCLGP	R/W	H'4014	32 bits	All bits	—	√	√	√
Cb calculation B coefficient register	CBCLBP	R/W	H'4018	32 bits	All bits	—	√	√	√
Cb calculation addition constant register	CBCLAP	R/W	H'401C	32 bits	All bits	—	√	√	√
Cr calculation R coefficient register	CRCLRP	R/W	H'4020	32 bits	All bits	—	√	√	√
Cr calculation G coefficient register	CRCLGP	R/W	H'4024	32 bits	All bits	—	√	√	√
Cr calculation B coefficient register	CRCLBP	R/W	H'4028	32 bits	All bits	—	√	√	√
Cr calculation addition constant register	CRCLAP	R/W	H'402C	32 bits	All bits	—	√	√	√

**Table 21.23 RGB-YC Conversion Coefficient Register Configuration (2)**

Register Name	Abbr.	Power-on Reset	RZ/G Series Products			
			RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Y calculation R coefficient register	YCLRP	H'*****264	—	√	√	√
Y calculation G coefficient register	YCLGP	H'*****4B2	—	√	√	√
Y calculation B coefficient register	YCLBP	H'*****0E9	—	√	√	√
Y calculation addition constant register	YCLAP	H'*****10	—	√	√	√
Cb calculation R coefficient register	CBCLRP	H'*****15A	—	√	√	√
Cb calculation G coefficient register	CBCLGP	H'*****2A5	—	√	√	√
Cb calculation B coefficient register	CBCLBP	H'*****400	—	√	√	√
Cb calculation addition constant register	CBCLAP	H'*****80	—	√	√	√
Cr calculation R coefficient register	CRCLRP	H'*****400	—	√	√	√
Cr calculation G coefficient register	CRCLGP	H'*****35A	—	√	√	√
Cr calculation B coefficient register	CRCLBP	H'*****0A5	—	√	√	√
Cr calculation addition constant register	CRCLAP	H'*****80	—	√	√	√

## 21.3 Register Description

### Legend for Register Description

Initial value: Register value after a reset.

—: Undefined value

R/W: Readable/writable. The written value can be read.

R/WC0: Readable/writable. Writing 0 initializes the bit. Writing 1 is ignored.

R: Read-only. The write value should always be 0.

—/W: Write-only. The read value is undefined.

Plane n: Indicates plane 1 to plane 8

Note: Do not access locations that appear empty in the address map. Operation is not guaranteed in case of access to change the value at any location other than those of the registers listed in Tables 21.2 to 21.23.

### 21.3.1 Display Unit System Control Registers

#### 21.3.1.1 Display Unit System Control Register m (DSYSRm, m = 0 and 2 / m = 0)

Note. m = 0 and 2 for RZ/G1H, DU2 is only for RZ/G1H.  
m = 0 for RZ/G1M/N/E.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address: DU0: H'FEB0 0000, DU2: H'FEB4 0000

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	ILTS	—	—	—	—	—	—	—	—	DSEC	—	—	—	IUPD
Initial value:	—	—	0	—	—	—	—	—	—	—	—	0	—	—	—	0
R/W:	R	R	R/W	R	R	R	R	R	R	R	R	R/W	R	R	R	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	DRES	DEN	TVM		SCM		—	—	—	—
Initial value:	—	—	—	—	—	—	1	0	1	0	0	0	—	—	—	—
R/W:	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31, 30	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
29	ILTS	0	R/W	Not available	Input Pad Latch Timing Select To enable this bit, the DEFE bit in the display unit extensional function control register m (DEFERm) should be set to 1. In the initial state, this bit is fixed to 0. 0: A signal of the input pad is latched at the DCLKIN rising edge. 1: A signal of the input pad is latched at the DCLKIN falling edge. Electrical characteristics do not apply.
28 to 21	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
20	DSEC	0	R/W	Available	Display Data Endian Change For details on data swapping, see section 21.4.7, Endian Conversion. 0: Display data on memory is not swapped in byte or word units. 1: Display data on memory is swapped in byte or word units.
19 to 17	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
16	IUPD	0	R/W	Not available	<p>Internal Updating Disable</p> <p>When DRES = 1, internal register updating occurs regardless of this bit setting.</p> <p>For details on internal updating, see section 21.2 (2), Internal Update.</p> <p>0: Internal register updating occurs for each vertical synchronous signal (VSYNC) assertion.</p> <p>1: If this bit is set to 1, internal register updating does not occur.</p> <ul style="list-style-type: none"> <li>If this bit is set to 0, register updating occurs according to the next vertical synchronous signal (VSYNC).</li> <li>This bit is shared by DU0 and DU1.</li> </ul>
15 to 10	—	—	R	—	<p>Reserved</p> <p>The read value is undefined. The write value should always be 0.</p>
9	DRES	1	R/W	Not available	Display Reset
8	DEN	0	R/W	Available	<p>Display Enable</p> <p>00: Display synchronous operation starts.</p> <p>If any register has not been set yet, the display unit may perform unexpected operation, thus set DRES to 0 after setting all registers in the display unit.</p> <p>For DEN = 0, the display data becomes values set with the display off mode output register n (DOORn).</p> <p>01: Display synchronous operation starts.</p> <p>If any register has not been set yet, the display unit may perform unexpected operation, thus set DRES = 0, DEN = 1 after setting all registers in the display unit.</p> <p>To re-set DRES to 1 following the start of operations for synchronization of the display with this setting, proceed with steps 1 and 2 in section 21.6.2, Transition to Module Standby Mode before doing so.</p> <p>For DEN = 1, the display data becomes values stored on the unified memory from the next frame.</p> <p>10: Display operation stops.</p> <p>Display operation and synchronization operation stop. The set values except for the following bits in the display unit status register n (DSSRn) are retained. In this setting, the following operations occur:</p> <ol style="list-style-type: none"> <li>All 0s are output as display data.</li> <li>The following bits of the display unit status register n (DSSRn) are cleared to 0: <ul style="list-style-type: none"> <li>TV synchronization signal error flag (TVR and TVR1)</li> <li>Frame flag (FRM and FRM1)</li> <li>Vertical blanking flag (VBK and VBK1)</li> <li>Raster interrupt flag (RINT and RINT1)</li> <li>Horizontal blanking flag (HBK and HBK1)</li> </ul> </li> <li>HSYNC, VSYNC, and ODDF pins function as inputs.</li> </ol> <p>However, the ODDF pin functions as a CLAMP output when the ODPM bit in the display unit mode register m (DSMRm) is 1.</p> <p>11: Setting prohibited</p> <ul style="list-style-type: none"> <li>This bit is shared by DU0 and DU1.</li> </ul>



Bit	Bit Name	Initial Value	R/W	Internal Update	Description
7, 6	TVM	10	R/W	Not available	<p>TV Synchronized Mode</p> <p>00: Master Mode HSYNC, VSYNC, and CSYNC are output.</p> <p>01: The switching mode of synchronous mode is set. Use this mode if necessary when switching from TV synchronized mode to master mode or vice versa is performed. In this mode, display operation forcibly stops and the DISP pin outputs the low level. Moreover, clock supply to DCLKIN can be stopped (input invalid) (the inside of the LSI is fixed to the high level). The EXHSYNC, EXVSYNC, and EXODDF pins are used as input pins.</p> <p>10: TV synchronized mode EXHSYNC, EXVSYNC, and EXODDF are input. When the ODPM bit in the display unit mode register m (DSMRm) is set to 1, the ODDF pin functions as an output pin.</p> <p>11: Setting prohibited</p>
5, 4	SCM	00	R/W	Not available	<p>Scan Mode</p> <p>00: Non-interlaced mode</p> <p>01: Setting prohibited</p> <p>10: Interlace sync mode</p> <p>11: Interlace sync &amp; video mode</p>
3 to 0	—	—	R	—	<p>Reserved</p> <p>The read value is undefined. The write value should always be 0.</p>

Note: m = 0 and 2, n = 0 to 2 for RZ/G1H.  
m = 0, n = 0 and 1 for RZ/G1M/N/E.

**21.3.1.2 Display Unit System Control Register 1 (DSYSR1)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address: DU1: H'FEB3 0000

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	ILTS1	—	—	—	—	—	—	—	—	DSEC1	—	—	—	—
Initial value:	—	—	0	—	—	—	—	—	—	—	—	0	—	—	—	—
R/W:	R	R	R/W	R	R	R	R	R	R	R	R	R/W	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	TVM1	—	SCM1	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	1	0	0	0	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R	R	R

- Bits 16, 9, and 8 of display unit system control register 0 (DSYSR0) are shared by DU0 and DU1. Thus, the bits in this register do not have a function.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31, 30	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
29	ILTS1	0	R/W	Not available	Input Pad Latch Timing Select 1 To enable this bit, the DEFE bit in the display unit extensional function control register 0 (DEFR0) should be set to 1. In the initial state, this bit is fixed to 0. 0: A signal of the input pad is latched at the DCLKIN rising edge. 1: A signal of the input pad is latched at the DCLKIN falling edge. Electrical characteristics do not apply.
28 to 21	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
20	DSEC1	0	R/W	Available	Display Data Endian Change 1 For details on data swapping, see section 21.4.7, Endian Conversion. 0: Display data on memory is not swapped in byte or word units. 1: Display data on memory is swapped in byte or word units.
19 to 8	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
7, 6	TVM1	10	R/W	Not available	<p>TV Synchronized Mode 1</p> <p>00: Master Mode</p> <p>HSYNC, VSYNC, and CSYNC are output.</p> <p>01: The switching mode of synchronous mode is set. Use this mode if necessary when switching from TV synchronized mode to master mode or vice versa is performed.</p> <p>In this mode, display operation forcibly stops and the DISP pin outputs the low level. Moreover, clock supply to DCLKIN can be stopped (input invalid) (the inside of the LSI is fixed to the high level). The EXHSYNC, EXVSYNC, and EXODDF pins are used as input pins.</p> <p>10: TV synchronized mode</p> <p>EXHSYNC, EXVSYNC, and EXODDF are input. When the ODPM bit in the display unit mode register 1 (DSMR1) is set to 1, the ODDF pin functions as an output pin.</p> <p>11: Setting prohibited</p>
5, 4	SCM1	00	R/W	Not available	<p>Scan Mode 1</p> <p>00: Non-interlaced mode</p> <p>01: Setting prohibited</p> <p>10: Interlace sync mode</p> <p>11: Interlace sync &amp; video mode</p>
3 to 0	—	—	R	—	<p>Reserved</p> <p>The read value is undefined. The write value should always be 0.</p>

### 21.3.1.3 Display Unit Mode Register n (DSMRn)

Note: n = 0 to 2 for RZ/G1H ; n = 0 and 1 for RZ/G1M/N/E.  
DU2 is only for RZ/G1H.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address: DU0: H'FEB0 0004, DU1: H'FEB3 0004, DU2: H'FEB4 0004

For the RZ/G1H, M, and N, all bit in this register setting is also available for the display data output via the LVDS.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	VSPM	ODPM	DIPM		CSPM	—	—	—	—	DIL	VSL	HSL	DDIS
Initial value:	—	—	—	0	0	0	0	0	—	—	—	—	0	0	0	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CDEL	CDEM		CDED	—	—	—	ODEV	CSY		—	—	—	—	—	—
Initial value:	0	0	0	0	—	—	—	0	0	0	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R	R	R	R/W	R/W	R/W	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 29	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
28	VSPM	0	R/W	DRES	VSYNC Pin Mode 0: The VSYNC signal is output to the VSYNC pin. 1: The CSYNC signal is output to the VSYNC pin. "VSYNC pin" refers to the DU_VSYNC/DU_EXVSYNC pin indicated in Table 21.1a* <sup>1</sup> . "VSYNC pin" refers to the DU1_VSYNC/DU1_EXVSYNC pin indicated in Table 21.1a* <sup>3</sup> . "VSYNC pin" refers to the DU0_VSYNC/DU0_EXVSYNC pin indicated in Table 21.1b or the DU1_VSYNC/DU1_EXVSYNC pin indicated in Table 21.1c* <sup>2</sup> .
27	ODPM	0	R/W	DRES	ODDF Pin Mode 0: The ODDF signal is output to the ODDF pin. 1: The CLAMP signal is output to the ODDF pin. Even if bits 7 and 6 in the display unit system control register n (DSYSRn) indicate TV synchronized mode, the ODDF pin becomes an output. "ODDF pin" refers to the DU_ODDF/DU_EXODDF pin indicated in Table 21.1a* <sup>1</sup> . "ODDF pin" refers to the DU1_ODDF/DU1_EXODDF pin indicated in Table 21.1a* <sup>3</sup> . "ODDF pin" refers to the DU0_ODDF/DU0_EXODDF pin indicated in Table 21.1b or the DU1_ODDF/DU1_EXODDF pin indicated in Table 21.1c* <sup>2</sup> .

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
26, 25	DIPM	All 0	R/W	DRES	<p>DISP Pin Mode</p> <p>00: The DISP signal is output to the DISP pin.            01: The CSYNC signal is output to the DISP pin.            10: Setting prohibited. (Fixed to 0.)            11: The DE signal is output to the DISP pin.</p> <p>"DISP pin" refers to the DU_DISP pin indicated in Table 21.1a*<sup>1</sup>.            "DISP pin" refers to the DU1_DISP pin indicated in Table 21.1a*<sup>3</sup>.            "DISP pin" refers to the DU0_DISP pin indicated in Table 21.1b or the DU1_DISP pin indicated in Table 21.1c*<sup>2</sup>.</p>
24	CSPM	0	R/W	DRES	<p>CSYNC Pin Mode</p> <p>0: The CSYNC signal is output to the CSYNC pin.            1: The HSYNC signal is output to the CSYNC pin.</p> <p>"CSYNC pin" refers to the DU_HSYNC/DU_EXHSYNC pin indicated in Table 21.1a*<sup>1</sup>.            "CSYNC pin" refers to the DU1_HSYNC/DU1_EXHSYNC pin indicated in Table 21.1a*<sup>3</sup>.            "CSYNC pin" refers to the DU0_HSYNC/DU0_EXHSYNC pin indicated in Table 21.1b or the DU1_HSYNC/DU1_EXHSYNC pin indicated in Table 21.1c*<sup>2</sup>.</p>
23 to 20	—	—	R	—	<p>Reserved</p> <p>The read value is undefined. The write value should always be 0.</p>
19	DIL	0	R/W	DRES	<p>DISP Polarity Select</p> <p>0: The DISP signal becomes a high level during display period.            1: The polarity of the DISP signal is inverted.</p>
18	VSL	0	R/W	DRES	<p>VSYNC Polarity Select</p> <p>0: The VSYNC signal becomes active low.            1: The polarity of VSYNC is inverted.</p>
17	HSL	0	R/W	DRES	<p>HSYNC Polarity Select</p> <p>0: The HSYNC signal becomes active low.            1: The polarity of the HSYNC signal is inverted.</p>
16	DDIS	0	R/W	Available	<p>DISP Disable</p> <p>0: The DISP signal is output.            1: The DISP signal is not output.</p>
15	CDEL	0	R/W	Available	<p>CDE Polarity Select</p> <p>0: The CDE signal becomes high when the output display data and color detection register n (CDERn) match.            1: The polarity of the CDE signal is inverted.</p>
14, 13	CDEM	00	R/W	Available	<p>CDE Output Mode</p> <p>00: The CDE signal is output as is.            01: The CDE signal is output as is.            10: The low level is output outside the display period.            11: The high level is output outside the display period.</p>

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
12	CDED	0	R/W	Available	CDE Disable 0: The CDE signal is output. 1: The CDE signal output is prohibited.
11 to 9	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
8	ODEV	0	R/W	Available	Odd Even Location for ODDF Signal 0: The odd field (ODDF = low) is located in the first half of the same frame of the interlace display. 1: The odd field (ODDF = low) is located in the second half of the same frame of the interlace display.
7, 6	CSY	00	R/W	Available	CSYNC Mode 00: A waveform obtained by performing exclusive logical OR for VSYNC and HSYNC is output as CSYNC. 01: Setting prohibited 10: During intervals of 3 rasters from the VSYNC falling edge, the equalizing pulse is output. After that, during intervals of 3 rasters, the serration pulse is output. After that, during intervals of 3 rasters, the equalizing pulse is output. During other intervals, the HSYNC waveform is output as CSYNC. 11: After 1/2 rasters from the VSYNC falling edge, the equalizing pulse is output during intervals of 2.5 rasters. After that, during intervals of 2.5 rasters, the serration pulse is output. After that, during intervals of 2.5 rasters, the equalizing pulse is output. During other intervals, the HSYNC waveform is output as CSYNC.
5 to 0	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

- Notes
1. For RZ/G1H
  2. For RZ/G1E
  3. For RZ/G1M/N

### 21.3.1.4 Display Unit Status Register 0 (DSSR0)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address: DU0: H'FEB0 0008

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	VC1FB		VC0FB		VC2FB/—*		DFB10	DFB9	DFB8	DFB7	DFB6	DFB5	DFB4	DFB3	DFB2	DFB1
Initial value:	0	0	1	1	0—*	0/—*	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R*	R*	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TVR	FRM	—	BUF	VBK	—	RINT	HBK	ADC8	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1
Initial value:	0	0	—	0	0	—	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Note: \* For reserved bit (bit name: —), initial value is undefined. For details, refer to following table.

- Video capture is the same as video input.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31, 30	VC1FB	00	R	Not available	<p>Video Capture 1 Frame Buffer Flag</p> <p>Set the DEFE bit in the display unit extensional function control register 0 (DEFR0) to 1 to enable bits 31 and 30. In the initial state, bits 31 and 30 are fixed to 0.</p> <p>00: In the plane set for video capture 1, the address indicated with PnDSA0Rm* is in use as the display area start address.</p> <p>01: In the plane set for video capture 1, the address indicated with PnDSA1Rm* is in use as the display area start address.</p> <p>10: In the plane set for video capture 1, the address indicated with PnDSA2Rm* is in use as the display area start address.</p> <p>11: The video capture 1 module is in the initial state.</p>
29, 28	VC0FB	11	R	Not available	<p>Video Capture 0 Frame Buffer Flag</p> <p>00: In the plane set for video capture 0, the address indicated with PnDSA0Rm* is in use as the display area start address.</p> <p>01: In the plane set for video capture 0, the address indicated with PnDSA1Rm* is in use as the display area start address.</p> <p>10: In the plane set for video capture 0, the address indicated with PnDSA2Rm* is in use as the display area start address.</p> <p>11: The video capture 0 module is in the initial state.</p>
27, 26	VC2FB	00	R	Not available	<p>Video Capture 2 Frame Buffer Flag [RZ/G1H/M/N]</p> <p>Set the DEFE bit in the display unit extensional function control register 0 (DEFR0) to 1 to enable bits 27 and 26. In the initial state, bits 27 and 26 are fixed to 0.</p> <p>00: In the plane set for video capture 2, the address indicated with PnDSA0Rm* is in use as the display area start address.</p> <p>01: In the plane set for video capture 2, the address indicated with PnDSA1Rm* is in use as the display area start address.</p> <p>10: In the plane set for video capture 2, the address indicated with PnDSA2Rm* is in use as the display area start address.</p> <p>11: The video capture 1 module is in the initial state.</p>

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
—	—	—	—	—	Reserved [RZ/G1E] The read value is undefined. The write value should always be 0.
25	DFB10	0	R	Not available	Display Frame Buffer 10 Flag 0: In $\alpha$ plane 2, the address indicated with AP2DSA0Rm* is in use as the display area start address. 1: In $\alpha$ plane 2, the address indicated with AP2DSA1Rm* is in use as the display area start address.
24	DFB9	0	R	Not available	Display Frame Buffer 9 Flag 0: In $\alpha$ plane 1, the address indicated with AP1DSA0Rm* is in use as the display area start address. 1: In $\alpha$ plane 1, the address indicated with AP1DSA1Rm* is in use as the display area start address.
23	DFB8	0	R	Not available	Display Frame Buffer 8 Flag 0: In plane 8, the address indicated with P8DSA0Rm* is in use as the display area start address. 1: In plane 8, the address indicated with P8DSA1Rm* is in use as the display area start address.
22	DFB7	0	R	Not available	Display Frame Buffer 7 Flag 0: In plane 7, the address indicated with P7DSA0Rm* is in use as the display area start address. 1: In plane 7, the address indicated with P7DSA1Rm* is in use as the display area start address.
21	DFB6	0	R	Not available	Display Frame Buffer 6 Flag 0: In plane 6, the address indicated with P6DSA0Rm* is in use as the display area start address. 1: In plane 6, the address indicated with P6DSA1Rm* is in use as the display area start address.
20	DFB5	0	R	Not available	Display Frame Buffer 5 Flag 0: In plane 5, the address indicated with P5DSA0Rm* is in use as the display area start address. 1: In plane 5, the address indicated with P5DSA1Rm* is in use as the display area start address.
19	DFB4	0	R	Not available	Display Frame Buffer 4 Flag 0: In plane 4, the address indicated with P4DSA0Rm* is in use as the display area start address. 1: In plane 4, the address indicated with P4DSA1Rm* is in use as the display area start address.
18	DFB3	0	R	Not available	Display Frame Buffer 3 Flag 0: In plane 3, the address indicated with P3DSA0Rm* is in use as the display area start address. 1: In plane 3, the address indicated with P3DSA1Rm* is in use as the display area start address.
17	DFB2	0	R	Not available	Display Frame Buffer 2 Flag 0: In plane 2, the address indicated with P2DSA0Rm* is in use as the display area start address. 1: In plane 2, the address indicated with P2DSA1Rm* is in use as the display area start address.



Bit	Bit Name	Initial Value	R/W	Internal Update	Description
16	DFB1	0	R	Not available	<p>Display Frame Buffer 1 Flag</p> <p>0: In plane 1, the address indicated with P1DSA0Rm* is in use as the display area start address.</p> <p>1: In plane 1, the address indicated with P1DSA1Rm* is in use as the display area start address.</p>
15	TVR	0	R	Not available	<p>TV Synchronization Error Flag</p> <p>0: Indicates that, after the TVR bit is cleared with the DRES bit of the display unit system control register 0 (DSYSR0) or the TVCL bit of the display unit status register clear register 0 (DSRCR0), the EXVSYNC rising edge is detected every time within the vertical cycle determined with the setting of the vertical cycle register 0 (VCR0).</p> <p>1: Indicates that, in TV synchronized mode, the EXVSYNC rising edge was not detected within the vertical cycle determined with the setting of the vertical cycle register 0 (VCR0).</p> <p>The TVR bit retains its status until it is cleared with the DRES or TVCL bit.</p>
14	FRM	0	R	Not available	<p>Frame Flag</p> <p>0: Indicates the period from the time when the FRM bit is cleared by the DRES bit of the display unit system control register 0 (DSYSR0) or by the FRCL bit of the display unit status register clear register 0 (DSRCR0) to the time when display of the next field is completed in the non-interlaced mode, or when display of the next even field is completed in interlace sync mode or interlace sync &amp; video mode.</p> <p>1: Indicates the period (in units of frames) from the start of the vertical blanking period of the first even field after the FRM bit is cleared by the DRES or FRCL bit, to the time when the FRM bit is cleared again.</p>
13	—	—	R	—	<p>Reserved</p> <p>The read value is undefined. The write value should always be 0.</p>
12	BUF	0	R	Not available	<p>Buffer Underflow Flag</p> <p>Set the DEFE8 bit in the display unit extensional function control register m (DEF8Rm*) to 1 to enable bit 12. In the initial state, bit 12 is fixed to 0.</p> <p>0: The buffer underflow has not occurred.</p> <p>1: The buffer underflow has occurred.</p>
11	VBK	0	R	Not available	<p>Vertical Blanking Flag</p> <p>0: Indicates the period from the time when the VBK bit is cleared by the DRES bit of the display unit system control register 0 (DSYSR0) or by the VBCL bit of the display unit status register clear register 0 (DSRCR0) to the time when display of the next field is completed.</p> <p>1: Indicates the period (in units of fields) from the start of the first vertical blanking period after the VBK bit is cleared by the DRES or VBCL bit, to the time when the VBK bit is cleared again.</p>
10	—	—	R	—	<p>Reserved</p> <p>The read value is undefined. The write value should always be 0.</p>

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
9	RINT	0	R	Not available	<p>Raster Interrupt Flag</p> <p>0: Indicates the period from the time when the RINT bit is cleared by the DRES bit of the display unit system control register 0 (DSYSR0) or by the RICL bit of the display unit status register clear register 0 (DSRCR0) to the time when the period of the rasters set in the raster interrupt offset register 0 (RINTOFSR0) has elapsed after the beginning of the next field display.</p> <p>1: Indicates the period from the time when the period of the rasters set in the raster interrupt offset register 0 (RINTOFSR0) has elapsed after the beginning of the next field display after the RINT bit is cleared by the DRES or RICL bit, to the time when the RINT bit is cleared again.</p>
8	HBK	0	R	Not available	<p>Horizontal Blanking Flag</p> <p>0: Indicates the period from the time when the HBK bit is cleared by the DRES bit of the display unit system control register 0 (DSYSR0) or by the HBCL bit of the display unit status register clear register 0 (DSRCR0) to the time of the next HSYNC assertion.</p> <p>1: Indicates the period from the start of the first horizontal blanking period after the HBK bit is cleared by the DRES or HBCL bit, to the time when the HBK bit is cleared again.</p>
7	ADC8	0	R	Not available	<p>Auto Rendering Display Change Flag 8</p> <p>0: Indicates that the frame buffer for plane 8 has not been switched.</p> <p>1: Indicates that the frame buffer for plane 8 has been switched. The ADC8 bit state is held until it is cleared.</p>
6	ADC7	0	R	Not available	<p>Auto Rendering Display Change Flag 7</p> <p>0: Indicates that the frame buffer for plane 7 has not been switched.</p> <p>1: Indicates that the frame buffer for plane 7 has been switched. The ADC7 bit state is held until it is cleared.</p>
5	ADC6	0	R	Not available	<p>Auto Rendering Display Change Flag 6</p> <p>0: Indicates that the frame buffer for plane 6 has not been switched.</p> <p>1: Indicates that the frame buffer for plane 6 has been switched. The ADC6 bit state is held until it is cleared.</p>
4	ADC5	0	R	Not available	<p>Auto Rendering Display Change Flag 5</p> <p>0: Indicates that the frame buffer for plane 5 has not been switched.</p> <p>1: Indicates that the frame buffer for plane 5 has been switched. The ADC5 bit state is held until it is cleared.</p>
3	ADC4	0	R	Not available	<p>Auto Rendering Display Change Flag 4</p> <p>0: Indicates that the frame buffer for plane 4 has not been switched.</p> <p>1: Indicates that the frame buffer for plane 4 has been switched. The ADC4 bit state is held until it is cleared.</p>
2	ADC3	0	R	Not available	<p>Auto Rendering Display Change Flag 3</p> <p>0: Indicates that the frame buffer for plane 3 has not been switched.</p> <p>1: Indicates that the frame buffer for plane 3 has been switched. The ADC3 bit state is held until it is cleared.</p>
1	ADC2	0	R	Not available	<p>Auto Rendering Display Change Flag 2</p> <p>0: Indicates that the frame buffer for plane 2 has not been switched.</p> <p>1: Indicates that the frame buffer for plane 2 has been switched. The ADC2 bit state is held until it is cleared.</p>

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
0	ADC1	0	R	Not available	Auto Rendering Display Change Flag 1 0: Indicates that the frame buffer for plane 1 has not been switched. 1: Indicates that the frame buffer for plane 1 has been switched. The ADC1 bit state is held until it is cleared.

Note: m = 0. suffix "m" as register name is only for RZ/G1H.  
n = 1 to 8.

- Description of the ADC bits

For animation, although the display of moving images can be performed in auto rendering mode, at this time

1. A check for a TRAP interrupt proceeds,
2. A check for a VBK interrupt proceeds, and
3. Rendering starts after a VBK interrupt has occurred, so two rounds of flag checking are required before this.

With these flag bits (ADC), an ADC interrupt is generated after a single flag check, and rendering can then start.

### 21.3.1.5 Display Unit Status Register 1 (DSSR1)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address: DU1: H'FEB3 0008

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TVR1	FRM1	—	—	VBK1	—	RINT1	HBK1	—	—	—	—	—	—	—	—
Initial value:	0	0	—	—	0	—	0	0	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 16	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
15	TVR1	0	R	Not available	<p>TV Synchronization Error Flag 1</p> <p>0: Indicates that, after the TVR1 bit is cleared with the DRES bit of the display unit system control register 0 (DSYSR0) or the TVCL1 bit of the display unit status register clear register 1 (DSRCR1), the EXVSYNC rising edge is detected every time within the vertical cycle determined with the setting of the vertical cycle register 1 (VCR1).</p> <p>1: Indicates that, in TV synchronized mode, the EXVSYNC rising edge was not detected within the vertical cycle determined with the setting of the vertical cycle register 1 (VCR1).</p> <p>The TVR1 bit retains its status until it is cleared with the DRES or TVCL1 bit.</p>
14	FRM1	0	R	Not available	<p>Frame Flag 1</p> <p>0: Indicates the period from the time when the FRM1 bit is cleared by the DRES bit of the display unit system control register 0 (DSYSR0) or by the FRCL1 bit of the display unit status register clear register 1 (DSRCR1) to the time when display of the next field is completed in the non-interlaced mode, or when display of the next even field is completed in interlace sync mode or interlace sync &amp; video mode.</p> <p>1: Indicates the period (in units of frames) from the start of the vertical blanking period of the first even field after the FRM1 bit is cleared by the DRES or FRCL1 bit, to the time when the FRM1 bit is cleared again.</p>
13, 12	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
11	VBK1	0	R	Not available	<p>Vertical Blanking Flag 1</p> <p>0: Indicates the period from the time when the VBK1 bit is cleared by the DRES bit of the display unit system control register 0 (DSYSR0) or by the VBCL1 bit of the display unit status register clear register 1 (DSRCR1) to the time when display of the next field is completed.</p> <p>1: Indicates the period (in units of fields) from the start of the first vertical blanking period after the VBK1 bit is cleared by the DRES or VBCL1 bit, to the time when the VBK1 bit is cleared again.</p>
10	—	—	R	—	<p>Reserved</p> <p>The read value is undefined. The write value should always be 0.</p>
9	RINT1	0	R	Not available	<p>Raster Interrupt Flag 1</p> <p>0: Indicates the period from the time when the RINT1 bit is cleared by the DRES bit of the display unit system control register 0 (DSYSR0) or by the RICL1 bit of the display unit status register clear register 1 (DSRCR1) to the time when the period of the rasters set in the raster interrupt offset register 1 (RINTOFSR1) has elapsed after the beginning of the next field display.</p> <p>1: Indicates the period from the time when the period of the rasters set in the raster interrupt offset register 1 (RINTOFS1) has elapsed after the beginning of the next field display after the RINT1 bit is cleared by the DRES or RICL1 bit, to the time when the RINT1 bit is cleared again.</p>
8	HBK1	0	R	Not available	<p>Horizontal Blanking Flag 1</p> <p>0: Indicates the period from the time when the HBK1 bit is cleared by the DRES bit of the display unit system control register 0 (DSYSR0) or by the HBCL1 bit of the display unit status register clear register 1 (DSRCR1) to the time of the next HSYNC assertion.</p> <p>1: Indicates the period from the start of the first horizontal blanking period after the HBK1 bit is cleared by the DRES or HBCL1 bit, to the time when the HBK1 bit is cleared again.</p>
7 to 0	—	—	R	—	<p>Reserved</p> <p>The read value is undefined. The write value should always be 0.</p>

### 21.3.1.6 Display Unit Status Register 2 (DSSR2)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	—	—	—

Address: DU2: H'FEB4 0008

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	VC1FB		VC0FB		VC2FB		DFB10	DFB9	DFB8	DFB7	DFB6	DFB5	DFB4	DFB3	DFB2	DFB1
Initial value:	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TVR	FRM	—	BUF	VBK	—	RINT	HBK	—	—	—	—	—	—	—	—
Initial value:	0	0	—	0	0	—	0	0	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

- Video capture is the same as video input.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31, 30	VC1FB	00	R	Not available	<p>Video Capture 1 Frame Buffer Flag</p> <p>Set the DEFE bit in the display unit extensional function control register 2 (DEFR2) to 1 to enable bits 31 and 30. In the initial state, bits 31 and 30 are fixed to 0.</p> <p>00: In the plane set for video capture 1, the address indicated with PnDSA0R2 is in use as the display area start address.</p> <p>01: In the plane set for video capture 1, the address indicated with PnDSA1R2 is in use as the display area start address.</p> <p>10: In the plane set for video capture 1, the address indicated with PnDSA2R2 is in use as the display area start address.</p> <p>11: The video capture 1 module is in the initial state.</p>
29, 28	VC0FB	11	R	Not available	<p>Video Capture 0 Frame Buffer Flag</p> <p>00: In the plane set for video capture 0, the address indicated with PnDSA0R2 is in use as the display area start address.</p> <p>01: In the plane set for video capture 0, the address indicated with PnDSA1R2 is in use as the display area start address.</p> <p>10: In the plane set for video capture 0, the address indicated with PnDSA2R2 is in use as the display area start address.</p> <p>11: The video capture 0 module is in the initial state.</p>
27, 26	VC2FB	00	R	Not available	<p>Video Capture 2 Frame Buffer Flag</p> <p>Set the DEFE bit in the display unit extensional function control register 2(DEFR2) to 1 to enable bits 27 and 26. In the initial state, bits 27 and 26 are fixed to 0.</p> <p>00: In the plane set for video capture 1, the address indicated with PnDSA0R2 is in use as the display area start address.</p> <p>01: In the plane set for video capture 1, the address indicated with PnDSA1R2 is in use as the display area start address.</p> <p>10: In the plane set for video capture 1, the address indicated with PnDSA2R2 is in use as the display area start address.</p> <p>11: The video capture 1 module is in the initial state.</p>

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
25	DFB10	0	R	Not available	Display Frame Buffer 10 Flag 0: In $\alpha$ plane 2, the address indicated with AP2DSA0R2 is in use as the display area start address. 1: In $\alpha$ plane 2, the address indicated with AP2DSA1R2 is in use as the display area start address.
24	DFB9	0	R	Not available	Display Frame Buffer 9 Flag 0: In $\alpha$ plane 1, the address indicated with AP1DSA0R2 is in use as the display area start address. 1: In $\alpha$ plane 1, the address indicated with AP1DSA1R2 is in use as the display area start address.
23	DFB8	0	R	Not available	Display Frame Buffer 8 Flag 0: In plane 8, the address indicated with P8DSA0R2 is in use as the display area start address. 1: In plane 8, the address indicated with P8DSA1R2 is in use as the display area start address.
22	DFB7	0	R	Not available	Display Frame Buffer 7 Flag 0: In plane 7, the address indicated with P7DSA0R2 is in use as the display area start address. 1: In plane 7, the address indicated with P7DSA1R2 is in use as the display area start address.
21	DFB6	0	R	Not available	Display Frame Buffer 6 Flag 0: In plane 6, the address indicated with P6DSA0R2 is in use as the display area start address. 1: In plane 6, the address indicated with P6DSA1R2 is in use as the display area start address.
20	DFB5	0	R	Not available	Display Frame Buffer 5 Flag 0: In plane 5, the address indicated with P5DSA0R2 is in use as the display area start address. 1: In plane 5, the address indicated with P5DSA1R2 is in use as the display area start address.
19	DFB4	0	R	Not available	Display Frame Buffer 4 Flag 0: In plane 4, the address indicated with P4DSA0R2 is in use as the display area start address. 1: In plane 4, the address indicated with P4DSA1R2 is in use as the display area start address.
18	DFB3	0	R	Not available	Display Frame Buffer 3 Flag 0: In plane 3, the address indicated with P3DSA0R2 is in use as the display area start address. 1: In plane 3, the address indicated with P3DSA1R2 is in use as the display area start address.
17	DFB2	0	R	Not available	Display Frame Buffer 2 Flag 0: In plane 2, the address indicated with P2DSA0R2 is in use as the display area start address. 1: In plane 2, the address indicated with P2DSA1R2 is in use as the display area start address.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
16	DFB1	0	R	Not available	<p>Display Frame Buffer 1 Flag</p> <p>0: In plane 1, the address indicated with P1DSA0R2 is in use as the display area start address.</p> <p>1: In plane 1, the address indicated with P1DSA1R2 is in use as the display area start address.</p>
15	TVR	0	R	Not available	<p>TV Synchronization Error Flag</p> <p>0: Indicates that, after the TVR bit is cleared with the DRES bit of the display unit system control register 2 (DSYSR2) or the TVCL bit of the display unit status register clear register 2 (DSRCR2), the EXVSYNC rising edge is detected every time within the vertical cycle determined with the setting of the vertical cycle register 2 (VCR2).</p> <p>1: Indicates that, in TV synchronized mode, the EXVSYNC rising edge was not detected within the vertical cycle determined with the setting of the vertical cycle register 2 (VCR2).</p> <p>The TVR bit retains its status until it is cleared with the DRES or TVCL bit.</p>
14	FRM	0	R	Not available	<p>Frame Flag</p> <p>0: Indicates the period from the time when the FRM bit is cleared by the DRES bit of the display unit system control register 2 (DSYSR2) or by the FRCL bit of the display unit status register clear register 2 (DSRCR2) to the time when display of the next field is completed in the non-interlaced mode, or when display of the next even field is completed in interlace sync mode or interlace sync &amp; video mode.</p> <p>1: Indicates the period (in units of frames) from the start of the vertical blanking period of the first even field after the FRM bit is cleared by the DRES or FRCL bit, to the time when the FRM bit is cleared again.</p>
13	—	—	R	—	<p>Reserved</p> <p>The read value is undefined. The write value should always be 0.</p>
12	BUF	0	R	Not available	<p>Buffer Underflow Flag</p> <p>Set the DEFE8 bit in the display unit extensional function control 8 register 2 (DEF8R2) to 1 to enable bit 12. In the initial state, bit 12 is fixed to 0.</p> <p>0: The buffer underflow has not occurred.</p> <p>1: The buffer underflow has occurred.</p>
11	VBK	0	R	Not available	<p>Vertical Blanking Flag</p> <p>0: Indicates the period from the time when the VBK bit is cleared by the DRES bit of the display unit system control register 2 (DSYSR2) or by the VBCL bit of the display unit status register clear register 2 (DSRCR2) to the time when display of the next field is completed.</p> <p>1: Indicates the period (in units of fields) from the start of the first vertical blanking period after the VBK bit is cleared by the DRES or VBCL bit, to the time when the VBK bit is cleared again.</p>
10	—	—	R	—	<p>Reserved</p> <p>The read value is undefined. The write value should always be 0.</p>



Bit	Bit Name	Initial Value	R/W	Internal Update	Description
9	RINT	0	R	Not available	<p>Raster Interrupt Flag</p> <p>0: Indicates the period from the time when the RINT bit is cleared by the DRES bit of the display unit system control register 2 (DSYSR2) or by the RICL bit of the display unit status register clear register 2 (DSRCR2) to the time when the period of the rasters set in the raster interrupt offset register 2 (RINTOFSR2) has elapsed after the beginning of the next field display.</p> <p>1: Indicates the period from the time when the period of the rasters set in the raster interrupt offset register 2 (RINTOFSR2) has elapsed after the beginning of the next field display after the RINT bit is cleared by the DRES or RICL bit, to the time when the RINT bit is cleared again.</p>
8	HBK	0	R	Not available	<p>Horizontal Blanking Flag</p> <p>0: Indicates the period from the time when the HBK bit is cleared by the DRES bit of the display unit system control register 2 (DSYSR2) or by the HBCL bit of the display unit status register clear register 2 (DSRCR2) to the time of the next HSYNC assertion.</p> <p>1: Indicates the period from the start of the first horizontal blanking period after the HBK bit is cleared by the DRES or HBCL bit, to the time when the HBK bit is cleared again.</p>
7 to 0	—	—	R	—	<p>Reserved</p> <p>The read value is undefined. The write value should always be 0.</p>

## 21.3.1.7 Display Unit Status Register Clear Register 0 (DSRCR0)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address: DU0: H'FEB0 000C

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TVCL	FRCL	—	BUFL	VBCL	—	RICL	HBCL	ADCL8	ADCL7	ADCL6	ADCL5	ADCL4	ADCL3	ADCL2	ADCL1
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	-/W	-/W	R	-/W	-/W	R	-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 16	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
15	TVCL	—	-/W	Not available	TV Synchronization Signal Error Flag Clear 0: Does not change the TVR flag in the display unit status register 0 (DSSR0). 1: Clears the TVR flag in the display unit status register 0 (DSSR0).
14	FRCL	—	-/W	Not available	Frame Flag Clear 0: Does not change the FRM flag in the display unit status register 0 (DSSR0). 1: Clears the FRM flag in the display unit status register 0 (DSSR0).
13	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
12	BUFL	—	-/W	Not available	Buffer Underflow Flag Clear Set the DEFE8 bit in the display unit extensional function control 8 register m (DEF8Rm*) to 1 to enable bit 12. In the initial state, bit 12 is fixed to 0. 0: Does not change the BUF flag in the display unit status register 0 (DSSR0). 1: Clear the BUF flag in the display unit status register 0 (DSSR0).
11	VBCL	—	-/W	Not available	Vertical Blanking Flag Clear 0: Does not change the VBK flag in the display unit status register 0 (DSSR0). 1: Clears the VBK flag in the display unit status register 0 (DSSR0).
10	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
9	RICL	—	—/W	Not available	Raster Interrupt flag clear 0: Does not change the RINT flag in the display unit status register 0 (DSSR0). 1: Clears the RINT flag in the display unit status register 0 (DSSR0).
8	HBCL	—	—/W	Not available	HBK flag clear 0: Does not change the HBK flag in the display unit status register 0 (DSSR0). 1: Clears the HBK flag in the display unit status register 0 (DSSR0).
7	ADCL8	—	—/W	Not available	Auto Rendering Display Change Flag Clear 8 0: Does not change the ADC flag 8 in the display unit status register 0 (DSSR0). 1: Clears the ADC flag 8 in the display unit status register 0 (DSSR0).
6	ADCL7	—	—/W	Not available	Auto Rendering Display Change Flag Clear 7 0: Does not change the ADC flag 7 in the display unit status register 0 (DSSR0). 1: Clears the ADC flag 7 in the display unit status register 0 (DSSR0).
5	ADCL6	—	—/W	Not available	Auto Rendering Display Change Flag Clear 6 0: Does not change the ADC flag 6 in the display unit status register 0 (DSSR0). 1: Clears the ADC flag 6 in the display unit status register 0 (DSSR0).
4	ADCL5	—	—/W	Not available	Auto Rendering Display Change Flag Clear 5 0: Does not change the ADC flag 5 in the display unit status register 0 (DSSR0). 1: Clears the ADC flag 5 in the display unit status register 0 (DSSR0).
3	ADCL4	—	—/W	Not available	Auto Rendering Display Change Flag Clear 4 0: Does not change the ADC flag 4 in the display unit status register 0 (DSSR0). 1: Clears the ADC flag 4 in the display unit status register 0 (DSSR0).
2	ADCL3	—	—/W	Not available	Auto Rendering Display Change Flag Clear 3 0: Does not change the ADC flag 3 in the display unit status register 0 (DSSR0). 1: Clears the ADC flag 3 in the display unit status register 0 (DSSR0).
1	ADCL2	—	—/W	Not available	Auto Rendering Display Change Flag Clear 2 0: Does not change the ADC flag 2 in the display unit status register 0 (DSSR0). 1: Clears the ADC flag 2 in the display unit status register 0 (DSSR0).
0	ADCL1	—	—/W	Not available	Auto Rendering Display Change Flag Clear 1 0: Does not change the ADC flag 1 in the display unit status register 0 (DSSR0). 1: Clears the ADC flag 1 in the display unit status register 0 (DSSR0).

Note: m = 0. suffix "m" as register name is only for RZ/G1H.

### 21.3.1.8 Display Unit Status Register Clear Register 1 (DSRCR1)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address: DU1: H'FEB3 000C

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TVCL1	FRCL1	—	—	VBCL1	—	RICL1	HBCL1	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	-/W	-/W	R	R	-/W	R	-/W	-/W	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 16	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
15	TVCL1	—	—/W	Not available	TV Synchronization Signal Error Flag 1 Clear 0: Does not change the TVR flag 1 in the display unit status register 1 (DSSR1). 1: Clears the TVR flag 1 in the display unit status register 1 (DSSR1).
14	FRCL1	—	—/W	Not available	Frame Flag 1 Clear 0: Does not change the FRM flag 1 in the display unit status register 1 (DSSR1). 1: Clears the FRM flag 1 in the display unit status register 1 (DSSR1).
13, 12	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
11	VBCL1	—	—/W	Not available	Vertical Blanking Flag 1 Clear 0: Does not change the VBK flag 1 in the display unit status register 1 (DSSR1). 1: Clears the VBK flag 1 in the display unit status register 1 (DSSR1).
10	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
9	RICL1	—	—/W	Not available	Raster Interrupt Flag 1 Clear 0: Does not change the RINT flag 1 in the display unit status register 1 (DSSR1). 1: Clears the RINT flag 1 in the display unit status register 1 (DSSR1).

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
8	HBCL1	—	—/W	Not available	HBK1 Flag Clear 0: Does not change the HBK flag 1 in the display unit status register 1 (DSSR1). 1: Clears the HBK flag 1 in the display unit status register 1 (DSSR1).
7 to 0	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

## 21.3.1.9 Display Unit Status Register Clear Register 2 (DSRCR2)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	—	—	—

Address: DU2: H'FEB4 000C

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TVCL	FRCL	—	BUFL	VBCL	—	RICL	HBCL	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	-/W	-/W	R	-/W	-/W	R	-/W	-/W	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 16	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
15	TVCL	—	-/W	Not available	TV Synchronization Signal Error Flag Clear 0: Does not change the TVR flag in the display unit status register 2 (DSSR2). 1: Clears the TVR flag in the display unit status register 2 (DSSR2).
14	FRCL	—	-/W	Not available	Frame Flag Clear 0: Does not change the FRM flag in the display unit status register 2 (DSSR2). 1: Clears the FRM flag in the display unit status register 2 (DSSR2).
13	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
12	BUFL	—	-/W	Not available	Buffer Underflow Flag Clear Set the DEFE8 bit in the display unit extensional function control 8 register 2 (DEF8R2) to 1 to enable bit 12. In the initial state, bit 12 is fixed to 0. 0: Does not change the BUF flag in the display unit status register 2 (DSSR2). 1: Clear the BUF flag in the display unit status register 2 (DSSR2).
11	VBCL	—	-/W	Not available	Vertical Blanking Flag Clear 0: Does not change the VBK flag in the display unit status register 2 (DSSR2). 1: Clears the VBK flag in the display unit status register 2 (DSSR2).
10	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
9	RICL	—	—/W	Not available	Raster Interrupt Flag Clear 0: Does not change the RINT flag in the display unit status register 2 (DSSR2). 1: Clears the RINT flag in the display unit status register 2 (DSSR2).
8	HBCL	—	—/W	Not available	HBK Flag Clear 0: Does not change the HBK flag in the display unit status register 2 (DSSR2). 1: Clears the HBK flag in the display unit status register 2 (DSSR2).
7 to 0	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

### 21.3.1.10 Display Unit Interrupt Enable Register 0 (DIER0)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address: DU0: H'FEB0 0010

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TVE	FRE	—	BUE	VBE	—	RIE	HBE	ADCE8	ADCE7	ADCE6	ADCE5	ADCE4	ADCE3	ADCE2	ADCE1
Initial value:	0	0	—	0	0	—	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The display unit interrupt enable register 0 (DIER0) allows the generation of interrupts for the CPU by aspects of the internal state of the display unit as reflected in bits of the display unit status register 0 (DSSR0) as the sources. When a bit of this register is set, setting of the bit in the same position within DSSR 0 will lead to the generation of an interrupt for the CPU.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 16	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
15	TVE	0	R/W	Not available	TV Synchronization Signal Error Interrupt Enable 0: Disables the TVR flag interrupt of the display unit status register 0 (DSSR0). 1: Enables the TVR flag interrupt of the display unit status register 0 (DSSR0).
14	FRE	0	R/W	Not available	Frame Flag Interrupt Enable 0: Disables the FRM flag interrupt of the display unit status register 0 (DSSR0). 1: Enables the FRM flag interrupt of the display unit status register 0 (DSSR0).
13	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
12	BUE	0	R/W	Not available	Buffer Underflow Flag Interrupt Enable Set the DEFE8 bit in the display unit extensional function control 8 register m (DEF8Rm*) to 1 to enable bit 12. In the initial state, bit 12 is fixed to 0. 0: Disables the BUF flag interrupt of the display unit status register 0 (DSSR0). 1: Enables the BUF flag interrupt of the display unit status register 0 (DSSR0).



Bit	Bit Name	Initial Value	R/W	Internal Update	Description
11	VBE	0	R/W	Not available	Vertical Blanking Flag Interrupt Enable 0: Disables the VBK flag interrupt of the display unit status register 0 (DSSR0). 1: Enables the VBK flag interrupt of the display unit status register 0 (DSSR0).
10	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
9	RIE	0	R/W	Not available	Raster Interrupt Flag Interrupt Enable 0: Disables the RINT flag interrupt of the display unit status register 0 (DSSR0). 1: Enables the RINT flag interrupt of the display unit status register 0 (DSSR0).
8	HBE	0	R/W	Not available	HBK Flag Interrupt Enable 0: Disables the HBK flag interrupt of the display unit status register 0 (DSSR0). 1: Enables the HBK flag interrupt of the display unit status register 0 (DSSR0).
7	ADCE8	0	R/W	Not available	Auto Rendering Display Change Flag 8 Interrupt Enable 0: Disables the ADC flag 8 interrupt of the display unit status register 0 (DSSR0). 1: Enables the ADC flag 8 interrupt of the display unit status register 0 (DSSR0).
6	ADCE7	0	R/W	Not available	Auto Rendering Display Change Flag 7 Interrupt Enable 0: Disables the ADC flag 7 interrupt of the display unit status register 0 (DSSR0). 1: Enables the ADC flag 7 interrupt of the display unit status register 0 (DSSR0).
5	ADCE6	0	R/W	Not available	Auto Rendering Display Change Flag 6 Interrupt Enable 0: Disables the ADC flag 6 interrupt of the display unit status register 0 (DSSR0). 1: Enables the ADC flag 6 interrupt of the display unit status register 0 (DSSR0).
4	ADCE5	0	R/W	Not available	Auto Rendering Display Change Flag 5 Interrupt Enable 0: Disables the ADC flag 5 interrupt of the display unit status register 0 (DSSR0). 1: Enables the ADC flag 5 interrupt of the display unit status register 0 (DSSR0).
3	ADCE4	0	R/W	Not available	Auto Rendering Display Change Flag 4 Interrupt Enable 0: Enables the ADC flag 4 interrupt of the display unit status register 0 (DSSR0). 1: Enables the ADC flag 4 interrupt of the display unit status register 0 (DSSR0).
2	ADCE3	0	R/W	Not available	Auto Rendering Display Change Flag 3 Interrupt Enable 0: Disables the ADC flag 3 interrupt of the display unit status register 0 (DSSR0). 1: Enables the ADC flag 3 interrupt of the display unit status register 0 (DSSR0).

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
1	ADCE2	0	R/W	Not available	Auto Rendering Display Change Flag 2 Interrupt Enable 0: Disables the ADC flag 2 interrupt of the display unit status register 0 (DSSR0). 1: Enables the ADC flag 2 interrupt of the display unit status register 0 (DSSR0).
0	ADCE1	0	R/W	Not available	Auto Rendering Display Change Flag 1 Interrupt Enable 0: Enables the ADC flag 1 interrupt of the display unit status register 0 (DSSR0). 1: Enables the ADC flag 1 interrupt of the display unit status register 0 (DSSR0).

Note: \* m = 0. suffix "m" as register name is only for RZ/G1H.

The following are conditions, based on DSSR0, DIER0, DSSR1, and DIER1, for issuing an interrupt to the CPU from the DU0/DU1.

The following are conditions, based on DSSR2 and DIER2, for issuing an interrupt to the CPU from the DU2. [RZ/G1H]

Conditions for issuing an interrupt from the DU0/DU1 = a + b + c + d + e + f + g + h + i + j + k + l + m + n + o + p + q + r + s + t

Conditions for issuing an interrupt from the DU2 = a + b + c + d + e + s [RZ/G1H]

- a = TVR & TVE
- b = FRM & FRE
- c = VBK & VBE
- d = RINT & RIE
- e = HBK & HBE
- f = ADC6 & ADCE6
- g = ADC5 & ADCE5
- h = ADC4 & ADCE4
- i = ADC3 & ADCE3
- j = ADC2 & ADCE2
- k = ADC1 & ADCE1
- l = ADC8 & ADCE8
- m = ADC7 & ADCE7
- n = TVR1 & TVE1
- o = FRM1 & FRE1
- p = VBK1 & VBE1
- q = RINT1 & RIE1
- r = HBK1 & HIBE1
- s = BUF & BUE
- t = BUK1 & BUE1

### 21.3.1.11 Display Unit Interrupt Enable Register 1 (DIER1)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address: DU1: H'FEB3 0010

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TVE1	FRE1	—	—	VBE1	—	RIE1	HBE1	—	—	—	—	—	—	—	—
Initial value:	0	0	—	—	0	—	0	0	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R	R	R/W	R	R/W	R/W	R	R	R	R	R	R	R	R

The display unit interrupt enable register 1 (DIER1) allows the generation of interrupts for the CPU by aspects of the internal state of the display unit as reflected in bits of the display unit status register 1 (DSSR1) as the sources. When a bit of this register is set, setting of the bit in the same position within DSSR1 will lead to the generation of an interrupt for the CPU.

For conditions for issuing an interrupt to the CPU from the display unit, see section 21.3.1.10, Display Unit Interrupt Enable Register 0 (DIER0).

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 16	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
15	TVE1	0	R/W	Not available	TV Synchronization Signal Error Flag 1 Interrupt Enable 0: Disables the TVR flag 1 interrupt of the display unit status register 1 (DSSR1). 1: Enables the TVR flag 1 interrupt of the display unit status register 1 (DSSR1).
14	FRE1	0	R/W	Not available	Frame Flag 1 Interrupt Enable 0: Disables the FRM flag 1 interrupt of the display unit status register 1 (DSSR1). 1: Enables the FRM flag 1 interrupt of the display unit status register 1 (DSSR1).
13, 12	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
11	VBE1	0	R/W	Not available	Vertical Blanking Flag 1 Interrupt Enable 0: Disables the VBK flag 1 interrupt of the display unit status register 1 (DSSR1). 1: Enables the VBK flag 1 interrupt of the display unit status register 1 (DSSR1).
10	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
9	RIE1	0	R/W	Not available	Raster Interrupt Flag 1 Interrupt Enable 0: Disables the RINT flag 1 interrupt of the display unit status register 1 (DSSR1). 1: Enables the RINT flag 1 interrupt of the display unit status register 1 (DSSR1).
8	HBE1	0	R/W	Not available	HBK Flag 1 Interrupt Enable 0: Disables the HBK flag 1 interrupt of the display unit status register 1 (DSSR1). 1: Enables the HBK flag 1 interrupt of the display unit status register 1 (DSSR1).
7 to 0	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

### 21.3.1.12 Display Unit Interrupt Enable Register 2 (DIER2)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	—	—	—

Address: DU2: H'FEB4 0010

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TVE	FRE	—	BUE	VBE	—	RIE	HBE	—	—	—	—	—	—	—	—
Initial value:	0	0	—	0	0	—	0	0	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R	R/W	R/W	R	R/W	R/W	R	R	R	R	R	R	R	R

The display unit interrupt enable register 2 (DIER2) allows the generation of interrupts for the CPU by aspects of the internal state of the display unit as reflected in bits of the display unit status register 2 (DSSR2) as the sources. When a bit of this register is set, setting of the bit in the same position within the DSSR2 will lead to the generation of an interrupt for the CPU.

For conditions for issuing an interrupt to the CPU from the display unit, see section 21.3.1.10, Display Unit Interrupt Enable Register 0 (DIER0).

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 16	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
15	TVE	0	R/W	Not available	TV Synchronization Signal Error Flag Interrupt Enable 0: Disables the TVR flag interrupt of the display unit status register 2 (DSSR2). 1: Enables the TVR flag interrupt of the display unit status register 2 (DSSR2).
14	FRE	0	R/W	Not available	Frame Flag Interrupt Enable 0: Disables the FRM flag interrupt of the display unit status register 2 (DSSR2). 1: Enables the FRM flag interrupt of the display unit status register 2 (DSSR2).
13	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
12	BUE	0	R/W	Not available	Buffer Underflow Flag Interrupt Enable Set the DEFE8 bit in the display unit extensional function control 8 register 2 (DEF8R2) to 1 to enable bit 12. In the initial state, bit 12 is fixed to 0. 0: Disables the BUF flag interrupt of the display unit status register 2 (DSSR2). 1: Enables the BUF flag interrupt of the display unit status register 2 (DSSR2).

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
11	VBE	0	R/W	Not available	Vertical Blanking Flag Interrupt Enable 0: Disables the VBK flag interrupt of the display unit status register 2 (DSSR2). 1: Enables the VBK flag interrupt of the display unit status register 2 (DSSR2).
10	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
9	RIE	0	R/W	Not available	Raster Interrupt Flag Interrupt Enable 0: Disables the RINT flag interrupt of the display unit status register 2 (DSSR2). 1: Enables the RINT flag interrupt of the display unit status register 2 (DSSR2).
8	HBE	0	R/W	Not available	HBK Flag Interrupt Enable 0: Disables the HBK flag interrupt of the display unit status register 2 (DSSR2). 1: Enables the HBK flag interrupt of the display unit status register 2 (DSSR2).
7 to 0	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

### 21.3.1.13 Display Unit Domain 1 Status Register 0 (DD1SSR0)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address: DU0: H'FEB2 0008

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TVR	FRM	—	BUF	VBK	—	RINT	HBK	ADC8	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1
Initial value:	0	0	—	0	0	—	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 16	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
15	TVR	0	R	Not available	TV Synchronization Error Flag 0: Indicates that, after the TVR bit is cleared with the DRES bit of the display unit system control register 0 (DSYSR0) or the TVCL bit of the display unit domain 1 status register clear register 0 (DD1SRCR0), the EXVSYNC rising edge is detected every time within the vertical cycle determined with the setting of the vertical cycle register 0 (VCR0). 1: Indicates that, in TV synchronized mode, the EXVSYNC rising edge was not detected within the vertical cycle determined with the setting of the vertical cycle register 0 (VCR0). The TVR bit retains its status until it is cleared with the DRES or TVCL bit.
14	FRM	0	R	Not available	Frame Flag 0: Indicates the period from the time when the FRM bit is cleared by the DRES bit of the display unit system control register 0 (DSYSR0) or by the FRCL bit of the display unit domain 1 status register clear register 0 (DD1SRCR0) to the time when display of the next field is completed in the non-interlaced mode, or when display of the next even field is completed in interlace sync mode or interlace sync & video mode. 1: Indicates the period (in units of frames) from the start of the vertical blanking period of the first even field after the FRM bit is cleared by the DRES or FRCL bit, to the time when the FRM bit is cleared again.
13	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
12	BUF	0	R	Not available	Buffer Underflow Flag Set the DEFE8 bit in the display unit extensional function control 8 register m (DEF8Rm*) to 1 to enable bit 12. In the initial state, bit 12 is fixed to 0. 0: The buffer underflow has not occurred. 1: The buffer underflow has occurred.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
11	VBK	0	R	Not available	<p>Vertical Blanking Flag</p> <p>0: Indicates the period from the time when the VBK bit is cleared by the DRES bit of the display unit system control register 0 (DSYSR0) or by the VBCL bit of the display unit domain 1 status register clear register 0 (DD1SRCR0) to the time when display of the next field is completed.</p> <p>1: Indicates the period (in units of fields) from the start of the first vertical blanking period after the VBK bit is cleared by the DRES or VBCL bit, to the time when the VBK bit is cleared again.</p>
10	—	—	R	—	<p>Reserved</p> <p>The read value is undefined. The write value should always be 0.</p>
9	RINT	0	R	Not available	<p>Raster Interrupt Flag</p> <p>0: Indicates the period from the time when the RINT bit is cleared by the DRES bit of the display unit system control register 0 (DSYSR0) or by the RICL bit of the display unit domain 1 status register clear register 0 (DD1SRCR0) to the time when the period of the rasters set in the raster interrupt offset register 0 (RINTOFSR0) has elapsed after the beginning of the next field display.</p> <p>1: Indicates the period from the time when the period of the rasters set in the raster interrupt offset register 0 (RINTOFSR0) has elapsed after the beginning of the next field display after the RINT bit is cleared by the DRES or RICL bit, to the time when the RINT bit is cleared again.</p>
8	HBK	0	R	Not available	<p>Horizontal Blanking Flag</p> <p>0: Indicates the period from the time when the HBK bit is cleared by the DRES bit of the display unit system control register 0 (DSYSR0) or by the HBCL bit of the display unit domain 1 status register clear register 0 (DD1SRCR0) to the time of the next HSYNC assertion.</p> <p>1: Indicates the period from the start of the first horizontal blanking period after the HBK bit is cleared by the DRES or HBCL bit, to the time when the HBK bit is cleared again.</p>
7	ADC8	0	R	Not available	<p>Auto Rendering Display Change Flag 8</p> <p>0: Indicates that the frame buffer for plane 8 has not been switched.</p> <p>1: Indicates that the frame buffer for plane 8 has been switched. The ADC8 bit state is held until it is cleared.</p>
6	ADC7	0	R	Not available	<p>Auto Rendering Display Change Flag 7</p> <p>0: Indicates that the frame buffer for plane 7 has not been switched.</p> <p>1: Indicates that the frame buffer for plane 7 has been switched. The ADC7 bit state is held until it is cleared.</p>
5	ADC6	0	R	Not available	<p>Auto Rendering Display Change Flag 6</p> <p>0: Indicates that the frame buffer for plane 6 has not been switched.</p> <p>1: Indicates that the frame buffer for plane 6 has been switched. The ADC6 bit state is held until it is cleared.</p>
4	ADC5	0	R	Not available	<p>Auto Rendering Display Change Flag 5</p> <p>0: Indicates that the frame buffer for plane 5 has not been switched.</p> <p>1: Indicates that the frame buffer for plane 5 has been switched. The ADC5 bit state is held until it is cleared.</p>



Bit	Bit Name	Initial Value	R/W	Internal Update	Description
3	ADC4	0	R	Not available	Auto Rendering Display Change Flag 4 0: Indicates that the frame buffer for plane 4 has not been switched. 1: Indicates that the frame buffer for plane 4 has been switched. The ADC4 bit state is held until it is cleared.
2	ADC3	0	R	Not available	Auto Rendering Display Change Flag 3 0: Indicates that the frame buffer for plane 3 has not been switched. 1: Indicates that the frame buffer for plane 3 has been switched. The ADC3 bit state is held until it is cleared.
1	ADC2	0	R	Not available	Auto Rendering Display Change Flag 2 0: Indicates that the frame buffer for plane 2 has not been switched. 1: Indicates that the frame buffer for plane 2 has been switched. The ADC2 bit state is held until it is cleared.
0	ADC1	0	R	Not available	Auto Rendering Display Change Flag 1 0: Indicates that the frame buffer for plane 1 has not been switched. 1: Indicates that the frame buffer for plane 1 has been switched. The ADC1 bit state is held until it is cleared.

Note: \* m = 0. suffix "m" as register name is only for RZ/G1H.

### 21.3.1.14 Display Unit Domain 1 Status Register 1 (DD1SSR1)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address: DU1: H'FEB2 8008

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TVR1	FRM1	—	—	VBK1	—	RINT1	HBK1	—	—	—	—	—	—	—	—
Initial value:	0	0	—	—	0	—	0	0	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 16	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
15	TVR1	0	R	Not available	<p>TV Synchronization Error Flag 1</p> <p>0: Indicates that, after the TVR1 bit is cleared with the DRES bit of the display unit system control register 0 (DSYSR0) or the TVCL1 bit of the display unit status register clear register 1 (DD1SRCLR1), the EXVSYNC rising edge is detected every time within the vertical cycle determined with the setting of the vertical cycle register 1 (VCR1).</p> <p>1: Indicates that, in TV synchronized mode, the EXVSYNC rising edge was not detected within the vertical cycle determined with the setting of the vertical cycle register 1 (VCR1).</p> <p>The TVR1 bit retains its status until it is cleared with the DRES or TVCL1 bit.</p>
14	FRM1	0	R	Not available	<p>Frame Flag 1</p> <p>0: Indicates the period from the time when the FRM1 bit is cleared by the DRES bit of the display unit system control register 0 (DSYSR0) or by the FRCL1 bit of the display unit status register clear register 1 (DD1SRCLR1) to the time when display of the next field is completed in the non-interlaced mode, or when display of the next even field is completed in interlace sync mode or interlace sync &amp; video mode.</p> <p>1: Indicates the period (in units of frames) from the start of the vertical blanking period of the first even field after the FRM1 bit is cleared by the DRES or FRCL1 bit, to the time when the FRM1 bit is cleared again.</p>
13, 12	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
11	VBK1	0	R	Not available	<p>Vertical Blanking Flag 1</p> <p>0: Indicates the period from the time when the VBK1 bit is cleared by the DRES bit of the display unit system control register 0 (DSYSR0) or by the VBCL1 bit of the display unit status register clear register 1 (DD1SRCR1) to the time when display of the next field is completed.</p> <p>1: Indicates the period (in units of fields) from the start of the first vertical blanking period after the VBK1 bit is cleared by the DRES or VBCL1 bit, to the time when the VBK1 bit is cleared again.</p>
10	—	—	R	—	<p>Reserved</p> <p>The read value is undefined. The write value should always be 0.</p>
9	RINT1	0	R	Not available	<p>Raster Interrupt Flag 1</p> <p>0: Indicates the period from the time when the RINT1 bit is cleared by the DRES bit of the display unit system control register 0 (DSYSR0) or by the RICL1 bit of the display unit status register clear register 1 (DD1SRCR1) to the time when the period of the rasters set in the raster interrupt offset register 1 (RINTOFSR1) has elapsed after the beginning of the next field display.</p> <p>1: Indicates the period from the time when the period of the rasters set in the raster interrupt offset register 1 (RINTOFS1) has elapsed after the beginning of the next field display after the RINT1 bit is cleared by the DRES or RICL1 bit, to the time when the RINT1 bit is cleared again.</p>
8	HBK1	0	R	Not available	<p>Horizontal Blanking Flag 1</p> <p>0: Indicates the period from the time when the HBK1 bit is cleared by the DRES bit of the display unit system control register 0 (DSYSR0) or by the HBCL1 bit of the display unit status register clear register 1 (DD1SRCR1) to the time of the next HSYNC assertion.</p> <p>1: Indicates the period from the start of the first horizontal blanking period after the HBK1 bit is cleared by the DRES or HBCL1 bit, to the time when the HBK1 bit is cleared again.</p>
7 to 0	—	—	R	—	<p>Reserved</p> <p>The read value is undefined. The write value should always be 0.</p>

## 21.3.1.15 Display Unit Domain 1 Status Register 2 (DD1SSR2)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	—	—	—

Address: DU2: H'FEB6 0008

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TVR	FRM	—	BUF	VBK	—	RINT	HBK	—	—	—	—	—	—	—	—
Initial value:	0	0	—	0	0	—	0	0	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 16	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
15	TVR	0	R	Not available	TV Synchronization Error Flag 0: Indicates that, after the TVR bit is cleared with the DRES bit of the display unit system control register 2 (DSYSR2) or the TVCL bit of the display unit domain 1 status register clear register 2 (DD1SRCR2), the EXVSYNC rising edge is detected every time within the vertical cycle determined with the setting of the vertical cycle register 2 (VCR2). 1: Indicates that, in TV synchronized mode, the EXVSYNC rising edge was not detected within the vertical cycle determined with the setting of the vertical cycle register 2 (VCR2). The TVR bit retains its status until it is cleared with the DRES or TVCL bit.
14	FRM	0	R	Not available	Frame Flag 0: Indicates the period from the time when the FRM bit is cleared by the DRES bit of the display unit system control register 2 (DSYSR2) or by the FRCL bit of the display unit domain 1 status register clear register 2 (DD1SRCR2) to the time when display of the next field is completed in the non-interlaced mode, or when display of the next even field is completed in interlace sync mode or interlace sync & video mode. 1: Indicates the period (in units of frames) from the start of the vertical blanking period of the first even field after the FRM bit is cleared by the DRES or FRCL bit, to the time when the FRM bit is cleared again.
13	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
12	BUF	0	R	Not available	Buffer Underflow Flag Set the DEFE8 bit in the display unit extensional function control 8 register 2 (DEF8R2) to 1 to enable bit 12. In the initial state, bit 12 is fixed to 0. 0: The buffer underflow has not occurred. 1: The buffer underflow has occurred.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
11	VBK	0	R	Not available	<p>Vertical Blanking Flag</p> <p>0: Indicates the period from the time when the VBK bit is cleared by the DRES bit of the display unit system control register 2 (DSYSR2) or by the VBCL bit of the display unit domain 1 status register clear register 2 (DD1SRCR2) to the time when display of the next field is completed.</p> <p>1: Indicates the period (in units of fields) from the start of the first vertical blanking period after the VBK bit is cleared by the DRES or VBCL bit, to the time when the VBK bit is cleared again.</p>
10	—	—	R	—	<p>Reserved</p> <p>The read value is undefined. The write value should always be 0.</p>
9	RINT	0	R	Not available	<p>Raster Interrupt Flag</p> <p>0: Indicates the period from the time when the RINT bit is cleared by the DRES bit of the display unit system control register 2 (DSYSR2) or by the RICL bit of the display unit domain 1 status register clear register 2 (DD1SRCR2) to the time when the period of the rasters set in the raster interrupt offset register 2 (RINTOFSR2) has elapsed after the beginning of the next field display.</p> <p>1: Indicates the period from the time when the period of the rasters set in the raster interrupt offset register 2 (RINTOFSR2) has elapsed after the beginning of the next field display after the RINT bit is cleared by the DRES or RICL bit, to the time when the RINT bit is cleared again.</p>
8	HBK	0	R	Not available	<p>Horizontal Blanking Flag</p> <p>0: Indicates the period from the time when the HBK bit is cleared by the DRES bit of the display unit system control register 2 (DSYSR2) or by the HBCL bit of the display unit domain 1 status register clear register 2 (DD1SRCR2) to the time of the next HSYNC assertion.</p> <p>1: Indicates the period from the start of the first horizontal blanking period after the HBK bit is cleared by the DRES or HBCL bit, to the time when the HBK bit is cleared again.</p>
7 to 0	—	—	R	—	<p>Reserved</p> <p>The read value is undefined. The write value should always be 0.</p>

### 21.3.1.16 Display Unit Domain 1 Status Register Clear Register 0 (DD1SRCR0)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address: DU0: H'FEB2 000C

The specifications shown in section 21.3.1 (7), Display Unit Status Register Clear Register 0 (DSRCR0), are also applied to this register.

**21.3.1.17 Display Unit Domain 1 Status Register Clear Register 1 (DD1SRCR1)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address: DU1: H'FEB2 800C

The specifications shown in section 21.3.1 (8), Display Unit Status Register Clear Register 1 (DSRCR1), are also applied to this register.

**21.3.1.18 Display Unit Domain 1 Status Register Clear Register 2 (DD1SRCR2)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	—	—	—

Address: DU2: H'FEB6 000C

The specifications shown in section 21.3.1 (9), Display Unit Status Register Clear Register 2 (DSRCR2), are also applied to this register.

**21.3.1.19 Display Unit Domain 1 Interrupt Enable Register 0 (DD1IER0)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address: DU0: H'FEB2 0010

The specifications shown in section 21.3.1 (10), Display Unit Interrupt Enable Register 0 (DIER0), are also applied to this register.

**21.3.1.20 Display Unit Domain 1 Interrupt Enable Register 1 (DD1IER1)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address: DU1: H'FEB2 8010

The specifications shown in section 21.3.1 (11), Display Unit Interrupt Enable Register 1 (DIER1), are also applied to this register.

**21.3.1.21 Display Unit Domain 1 Interrupt Enable Register 2 (DD1IER2)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	—	—	—

Address: DU2: H'FEB6 0010

The specifications shown in section 21.3.1 (12), Display Unit Interrupt Enable Register 2 (DIER2), are also applied to this register.

### 21.3.1.22 Color Palette Control Register m (CPCRM, m = 0 and 2)

Note: Suffix "m" as register name and DU2 are only for RZ/G1H.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address: DU0: H'FEB0 0014, DU2: H'FEB4 0014

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	CP4CE	CP3CE	CP2CE	CP1CE
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 20	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
19	CP4CE	0	R/W	Available	Color Palette 4 Change Enable 0: The color palette 4 is not switched. 1: The color palette 4 is switched. Switching occurs when the DRES bit of the display unit system control register m (DSYSRm*) is set to 0 from 1 or when internal updating is performed. This bit is valid only when it is set to 1. Setting this bit to 0 is invalid. This bit is cleared to 0 after the color palette 4 is switched. If setting of 1 and clearing to 0 occur at the same time, clearing to 0 is given priority.
18	CP3CE	0	R/W	Available	Color Palette 3 Change Enable 0: The color palette 3 is not switched. 1: The color palette 3 is switched. Switching occurs when the DRES bit of the display unit system control register m (DSYSRm*) is set to 0 from 1 or when internal updating is performed. This bit is valid only when it is set to 1. Setting this bit to 0 is invalid. This bit is cleared to 0 after the color palette 3 is switched. If setting of 1 and clearing to 0 occur at the same time, clearing to 0 is given priority.
17	CP2CE	0	R/W	Available	Color Palette 2 Change Enable 0: The color palette 2 is not switched. 1: The color palette 2 is switched. Switching occurs when the DRES bit of the display unit system control register m (DSYSRm*) is set to 0 from 1 or when internal updating is performed. This bit is valid only when it is set to 1. Setting this bit to 0 is invalid. This bit is cleared to 0 after the color palette 2 is switched. If setting of 1 and clearing to 0 occur at the same time, clearing to 0 is given priority.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
16	CP1CE	0	R/W	Available	Color Palette 1 Change Enable 0: The color palette 1 is not switched. 1: The color palette 1 is switched. Switching occurs when the DRES bit of the display unit system control register m (DSYSRm*) is set to 0 from 1 or when internal updating is performed. This bit is valid only when set to 1. Setting this bit to 0 is invalid. This bit is cleared to 0 after the color palette 1 is switched. If setting of 1 and clearing to 0 occur at the same time, clearing to 0 is given priority.
15 to 0	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

Note: \* m = 0 and 2 only for RZ/G1H, m = 0 for RZ/G1M/N/E.



### 21.3.1.23 Display Plane Priority Register m (DPPRm, m = 0 and 2)

Note: Suffix "m" as register name and DU2 are only for RZ/G1H.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address: DU0: H'FEB0 0018, DU2: H'FEB4 0018

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DPE8	DPS8			DPE7	DPS7			DPE6	DPS6			DPE5	DPS5		
Initial value:	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DPE4	DPS4			DPE3	DPS3			DPE2	DPS2			DPE1	DPS1		
Initial value:	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Defines the order of planes in image composition and turns the display of planes on or off
- When the DPRS bit in the display unit output route control register m (DORCRm\*) is 0, the display of planes from among planes 1 to 8 for which display is enabled is switched on.
- This register can only be used to set the priority order for superposition processor m. To use superposition processor 1, set the DPRS bit in the display unit output route control register m (DORCRm\*) to 1 and make other settings as required in the display superimpose 1 priority register.
- After setting a desired value in a register listed in section 21.3.4, Display Plane Registers (Alpha Plane Registers), set the corresponding bit in the DPPRm (bit 31, 27, 23, 19, 15, 11, 7, or 3) to 1.

Note: \* m = 0 and 2, suffix "m" is only for RZ/G1H.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31	DPE8	0	R/W	Available	Display Plane Priority 8 Enable
30 to 28	DPS8	111	R/W	Available	Display Plane Priority 8 Select 1000: Assigns priority 8 to plane 1 and displays plane 1. 1001: Assigns priority 8 to plane 2 and displays plane 2. 1010: Assigns priority 8 to plane 3 and displays plane 3. 1011: Assigns priority 8 to plane 4 and displays plane 4. 1100: Assigns priority 8 to plane 5 and displays plane 5. 1101: Assigns priority 8 to plane 6 and displays plane 6. 1110: Assigns priority 8 to plane 7 and displays plane 7. 1111: Assigns priority 8 to plane 8 and displays plane 8. 0---: Priority 8 is not displayed.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
27	DPE7	0	R/W	Available	Display Plane Priority 7 Enable
26 to 24	DPS7	110	R/W	Available	Display Plane Priority 7 Select 1000: Assigns priority 7 to plane 1 and displays plane 1. 1001: Assigns priority 7 to plane 2 and displays plane 2. 1010: Assigns priority 7 to plane 3 and displays plane 3. 1011: Assigns priority 7 to plane 4 and displays plane 4. 1100: Assigns priority 7 to plane 5 and displays plane 5. 1101: Assigns priority 7 to plane 6 and displays plane 6. 1110: Assigns priority 7 to plane 7 and displays plane 7. 1111: Assigns priority 7 to plane 8 and displays plane 8. 0---: Priority 7 is not displayed.
23	DPE6	0	R/W	Available	Display Plane Priority 6 Enable
22 to 20	DPS6	101	R/W	Available	Display Plane Priority 6 Select 1000: Assigns priority 6 to plane 1 and displays plane 1. 1001: Assigns priority 6 to plane 2 and displays plane 2. 1010: Assigns priority 6 to plane 3 and displays plane 3. 1011: Assigns priority 6 to plane 4 and displays plane 4. 1100: Assigns priority 6 to plane 5 and displays plane 5. 1101: Assigns priority 6 to plane 6 and displays plane 6. 1110: Assigns priority 6 to plane 7 and displays plane 7. 1111: Assigns priority 6 to plane 8 and displays plane 8. 0---: Priority 6 is not displayed.
19	DPE5	0	R/W	Available	Display Plane Priority 5 Enable
18 to 16	DPS5	100	R/W	Available	Display Plane Priority 5 Select 1000: Assigns priority 5 to plane 1 and displays plane 1. 1001: Assigns priority 5 to plane 2 and displays plane 2. 1010: Assigns priority 5 to plane 3 and displays plane 3. 1011: Assigns priority 5 to plane 4 and displays plane 4. 1100: Assigns priority 5 to plane 5 and displays plane 5. 1101: Assigns priority 5 to plane 6 and displays plane 6. 1110: Assigns priority 5 to plane 7 and displays plane 7. 1111: Assigns priority 5 to plane 8 and displays plane 8. 0---: Priority 5 is not displayed.
15	DPE4	0	R/W	Available	Display Plane Priority 4 Enable
14 to 12	DPS4	011	R/W	Available	Display Plane Priority 4 Select 1000: Assigns priority 4 to plane 1 and displays plane 1. 1001: Assigns priority 4 to plane 2 and displays plane 2. 1010: Assigns priority 4 to plane 3 and displays plane 3. 1011: Assigns priority 4 to plane 4 and displays plane 4. 1100: Assigns priority 4 to plane 5 and displays plane 5. 1101: Assigns priority 4 to plane 6 and displays plane 6. 1110: Assigns priority 4 to plane 7 and displays plane 7. 1111: Assigns priority 4 to plane 8 and displays plane 8. 0---: Priority 4 is not displayed.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
11	DPE3	0	R/W	Available	Display Plane Priority 3 Enable
10 to 8	DPS3	010	R/W	Available	Display Plane Priority 3 Select 1000: Assigns priority 3 to plane 1 and displays plane 1. 1001: Assigns priority 3 to plane 2 and displays plane 2. 1010: Assigns priority 3 to plane 3 and displays plane 3. 1011: Assigns priority 3 to plane 4 and displays plane 4. 1100: Assigns priority 3 to plane 5 and displays plane 5. 1101: Assigns priority 3 to plane 6 and displays plane 6. 1110: Assigns priority 3 to plane 7 and displays plane 7. 1111: Assigns priority 3 to plane 8 and displays plane 8. 0---: Priority 3 is not displayed.
7	DPE2	0	R/W	Available	Display Plane Priority 2 Enable
6 to 4	DPS2	001	R/W	Available	Display Plane Priority 2 Select 1000: Assigns priority 2 to plane 1 and displays plane 1. 1001: Assigns priority 2 to plane 2 and displays plane 2. 1010: Assigns priority 2 to plane 3 and displays plane 3. 1011: Assigns priority 2 to plane 4 and displays plane 4. 1100: Assigns priority 2 to plane 5 and displays plane 5. 1101: Assigns priority 2 to plane 6 and displays plane 6. 1110: Assigns priority 2 to plane 7 and displays plane 7. 1111: Assigns priority 2 to plane 8 and displays plane 8. 0---: Priority 2 is not displayed.
3	DPE1	0	R/W	Available	Display Plane Priority 1 Enable
2 to 0	DPS1	000	R/W	Available	Display Plane Priority 1 Select 1000: Assigns priority 1 to plane 1 and displays plane 1. 1001: Assigns priority 1 to plane 2 and displays plane 2. 1010: Assigns priority 1 to plane 3 and displays plane 3. 1011: Assigns priority 1 to plane 4 and displays plane 4. 1100: Assigns priority 1 to plane 5 and displays plane 5. 1101: Assigns priority 1 to plane 6 and displays plane 6. 1110: Assigns priority 1 to plane 7 and displays plane 7. 1111: Assigns priority 1 to plane 8 and displays plane 8. 0---: Priority 1 is not displayed.

### 21.3.1.24 Display Unit Extensional Function Control Register m (DEFRm/n, m/n = 0 and 2 or m/n = 0)

Note: For DEFRm and DEFRn, m/n = 0 and 2 for RZ/G1H, DU2 is only for RZ/G1H.  
m/n = 0 for RZ/G1M/N/E.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address: DU0: H'FEB0 0020, DU2: H'FEB4 0020

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CODE															
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	EXSL	EXVL	—	—	—	—	—	EXUP	VCUP	—	—	—	DEFE
Initial value:	—	—	—	0	0	—	—	—	—	—	0	0	—	—	—	0
R/W:	R	R	R	R/W	R/W	R	R	R	R	R	R/W	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 16	CODE	—	-/W	Not available	DEFRm*1 Enabling Code (register available code) For a value written to DEFRm*1 to be effective, the value must include H'7773 in these bits.
15 to 13	—	—	R	—	Reserved. The read value is undefined. The write value should always be 0.
12	EXSL	0	R/W	DRES	External Sync Signal Select 0: External SYNC signals (EXVSYNC, EXHSYNC) allow signals from the pins to be directly read in terms of post-division clocks. 1: External SYNC signals (EXVSYNC, EXHSYNC) allow the signals that were read in terms of pre-division clock to be read again as post-division clocks.
11	EXVL	0	R/W	Not available	External Vsync Latch Select 0: External VSYNC signal (EXVSYNC) allows the signal from the pin to be latched every clock cycle. 1: External VSYNC signal (EXVSYNC) allows the signal from the pin to be latched at the rising edge of the external HSYNC signal.
10 to 6	—	—	R	—	Reserved. The read value is undefined. The write value should always be 0.
5	EXUP	0	R/W	DRES	External Updating Mode 0: Internally updates the internal update function bit. 1: Externally updates the internal update function bit without updating it internally. This bit takes precedence over the display unit system control register m (DSYSRm*1)/IUPD.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
4	VCUP	0	R/W	DRES	Vertical Cycle Register Update Timing Select 0: The internal updating is based on the falling VSYNC. 1: The internal updating is based on the rising VSYNC. By setting the internal updating of the vertical scanning cycle register as a VSYNC rise, any disturbance of VSYNC signals during vertical scanning cycle register switching can be prevented.
3 to 1	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
0	DEFE	0	R/W	DRES	Display Unit Extensional Function Enable 0: Disables the extensional functions 1: Enables the following extensional functions: Enables bits 27 and 26 in the plane n mode register m (PnMRm* <sup>2</sup> ). Enables bits 31 to 29 of plane n display area start address 0-2 register m (PnDSA0-2Rm* <sup>2</sup> ) and display capture n area start address register m (DCnSARm* <sup>3</sup> ). Enables bits 25 and 5 in the external synchronization control register m (ESCRm* <sup>4</sup> ). Enables bit 10 in the plane n blending ratio register m* <sup>2</sup> (PnALPHAR m* <sup>2</sup> ). Enables bit 29 in the display unit system control register m (DSYSRm* <sup>4</sup> ).

- Notes:
1. m = 0 and 2 for RZ/G1H, m = 0 for RZ/G1M/N/E.
  2. m = 0 and 2, suffix "m" is only for RZ/G1H.  
n = 1 to 8.
  3. m = 0 and 2, suffix "m" is only for RZ/G1H.  
n = no number or 2.
  4. m = 0 to 2 for RZ/G1H, m = 0 and 1 for RZ/G1M/N/E.

### 21.3.1.25 Display Unit Extensional Function Control Register 1 (DEFR1)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address: DU1: H'FEB3 0020

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CODE															
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	EXSL1	EXV1L	—	—/DODF1*	—	—	—	VCUP1	—	—	—	—	—
Initial value:	—	—	—	0	0	—	—/0*	—/0*	—	—	—	0	—	—	—	—
R/W:	R	R	R	R/W	R/W	R	R/W*	R/W*	R	R	R	R/W	R	R	R	R

Note: \* For reserved bit (bit name: —), initial value is undefined, writing is not available and writing value should be specified. For details of bit description, refer to following table.

- Since the bits 5 and 0 of the display expanded-function control register 0 (DEFR0) are made to serve a double purpose by DU0 and DU1, this register does not have a function.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 16	CODE	—	—/W	Not available	DEFR1 Enabling Code (register available code) For a value written to DEFR1 to be effective, the value must include H'7773 in these bits.
15 to 13	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
12	EXSL1	0	R/W	DRES	External Sync Signal Select 1 0: External SYNC signals (EXVSYNC, EXHSYNC) allow signals from the pins to be directly read in terms of post-division clocks. 1: External SYNC signals (EXVSYNC, EXHSYNC) allow the signals that were read in terms of pre-division clock to be read again as post-division clocks.
11	EXV1L	0	R/W	Not available	External Vsync Latch Select 1 0: External VSYNC signal (EXVSYNC) allows the signal from the pin to be latched every clock cycle. 1: External VSYNC signal (EXVSYNC) allows the signal from the pin to be latched at the rising edge of the external HSYNC signal.
10	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
9, 8	—	—	R	—	Reserved [Only for RZ/G1H] The read value is undefined. The write value should always be 0.
	DODF1	00	R/W	DRES	Display Output Data Format. [RZ/G1M/N/E] 00: Sets the DU1 display output to RGB data format. 01: Setting prohibited 10: Sets the DU1 display output to non-multiplexed YC data format. Y (luminance) and C (chrominance) are output in parallel. 11: Sets the DU1 display output to multiplexed YC data format. Y (luminance) and C (chrominance) are output in multiplexed format.  When YC format is displayed by the timing as shown in Figure 21.22 and Figure 21.23, set 1 bits to DCKOSEL and FRQSEL (division by 2) in the External Synchronization Control Register 1 (ESCR1). Non-multiplexed YC format can be displayed in Figure 21.22a and Figure 21.22b, this setting is not required. External Vsync Latch Select 1
7 to 5	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
4	VCUP1	0	R/W	DRES	Vertical cycle register update timing select 0: The internal updating is based on the falling VSYNC. 1: The internal updating is based on the rising VSYNC. By setting the internal updating of the vertical scanning cycle register as a VSYNC rise, any disturbance of VSYNC signals during vertical scanning cycle register switching can be prevented.
3 to 0	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

### 21.3.1.26 Display Alpha Ratio Plane Control Register m (DAPCRm, m = 0 and 2)

Note: Suffix "m" as register name and DU2 are only for RZ/G1H.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address: DU0: H'FEB0 0024, DU2: H'FEB4 0024

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CODE															
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	AP2E	—	—	—	AP1E
Initial value:	—	—	—	—	—	—	—	—	—	—	—	0	—	—	—	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R	R/W

After setting a desired value in a register listed in section 21.3.4, Display Plane Registers (Alpha Plane Registers), set the corresponding bit in the DAPCRm (bit 4, or 0) to 1.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 16	CODE	—	—/W	Not available	DAPCRm Enabling Code (register available code) For a value written to DAPCRm* to be effective, the value must include H'7773 in these bits.
15 to 5	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
4	AP2E	0	R/W	Available	Alpha Ratio Plane 2 Enable 0: $\alpha$ plane 2 cannot be used. 1: $\alpha$ plane 2 can be used.
3 to 1	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
0	AP1E	0	R/W	Available	Alpha Ratio Plane 1 Enable 0: $\alpha$ plane 1 cannot be used. 1: $\alpha$ plane 1 can be used.

Note: \* m = 0 and 2, suffix "m" is only for RZ/G1H.



### 21.3.1.27 Display Capture Control Register m (DCPCRm, m = 0 and 2)

Note: Suffix "m" as register name and DU2 are only for RZ/G1H.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address DU0: H'FEB0 0028, DU2: H'FEB4 0028

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CODE															
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
			CA2B	CD2F	—	—	—	DC2E	—		CAB	CDF	—	—	—	DCE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R	R	R	R/W	R	R	R/W	R/W	R	R	R	R/W

After setting a desired value in a register listed in section 21.3.5, Display Capture Registers, set the corresponding bit in the DCPCRm\*<sup>1</sup> (bit 8 or 0) to 1.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 16	CODE	—	—/W	Not available	DCPCRm* <sup>1</sup> Enabling Code (register available code) For a value written to DCPCRm to be effective, the value must include H'7773 in these bits.
15, 14	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
13	CA2B	0	R/W	Available	Display Capture A Bit 2 Function Select To enable this bit, DEFE3 bit in the display unit extensional function control 3 register m (DEF3Rm* <sup>1</sup> ) should be set to 1. In the initial state, this bit is fixed to 0. 0: When the display capture data 2 format is ARGB1555, the A value is 0. 1: When the display capture data 2 format is ARGB1555, the A value is 1.
12	CD2F	0	R/W	Available	Display Capture Data 2 Format To enable this bit, the DEFE3 bit in the display unit extensional function control 3 register m (DEF3Rm* <sup>1</sup> ) should be set to 1. In the initial state, this bit is fixed to 0. 0: Display capture data format in the superposition processor 1 is RGB565. 1: Display capture data format in the superposition processor 1 is ARGB1555. The A value is determined by bit 13 in this register.
11 to 9	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
8	DC2E	0	R/W	Available	<p>Display Capture 2 Enable</p> <p>To enable this bit, DEFE3 bit in the display unit extensional function control register 3 m (DEF3Rm*<sup>1</sup>) should be set to 1. In the initial state, this bit is fixed to 0.</p> <p>0: Display data in the superposition processor 1 is not captured.</p> <p>1: Display data in the superposition processor 1 is captured when the DRES and DEN bits in the display unit system control register m (DSYSRm*<sup>2</sup>) are B'01. After this bit is set to 1, data capture is started in the subsequent frame.</p>
7, 6	—	—	R	—	<p>Reserved</p> <p>The read value is undefined. The write value should always be 0.</p>
5	CAB	0	R/W	Available	<p>Display Capture A Bit Function Select</p> <p>To enable this bit, the DEFE2G bit in the display unit extensional function control 2 register m (DEF2Rm*<sup>1</sup>) should be set to 1. In the initial state, this bit is fixed to 0.</p> <p>0: When the display capture data format is ARGB1555, the A value is 0.</p> <p>1: When the display capture data format is ARGB1555, the A value is 1.</p>
4	CDF	0	R/W	Available	<p>Display Capture Data Format</p> <p>To enable this bit, the DEFE2G bit in the display unit extensional function control 2 register m (DEF2Rm*<sup>1</sup>) should be set to 1. In the initial state, this bit is fixed to 0.</p> <p>0: Display capture data format in the superposition processor m is RGB565.</p> <p>1: Display capture data format in the superposition processor m is ARGB1555. The A value is determined by bit 5 in this register.</p>
3 to 1	—	—	R	—	<p>Reserved</p> <p>The read value is undefined. The write value should always be 0.</p>
0	DCE	0	R/W	Available	<p>Display Capture Enable</p> <p>0: Display data in the superposition processor m*<sup>2</sup> is not captured.</p> <p>1: Display data in the superposition processor m*<sup>2</sup> is captured when the DRES and DEN bits in the display unit system control register m (DSYSRm*<sup>2</sup>) are B'01. After this bit is set to 1, data capture is started in the subsequent frame.</p>

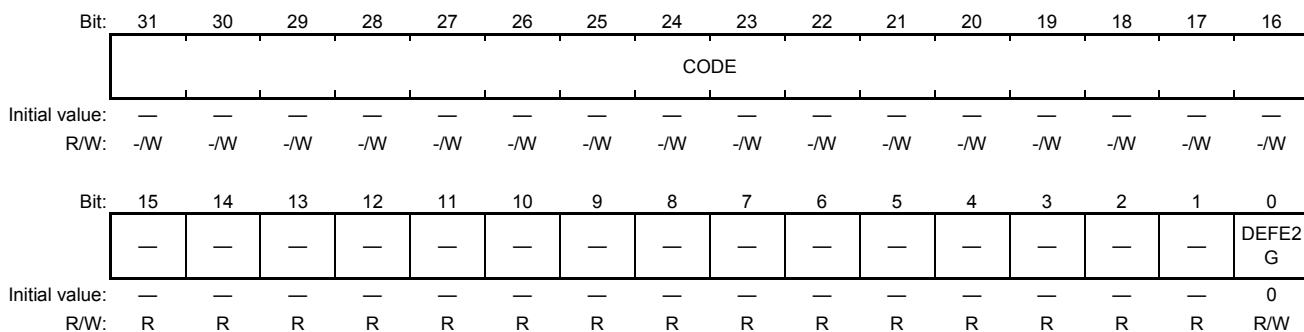
Notes: 1. m = 0 and 2, suffix "m" is only for RZ/G1H.  
2. m = 0 and 2 for RZ/G1H, m = 0 for RZ/G1M/N/E.

**21.3.1.28 Display Unit Extensional Function Control 2 Register m (DEF2Rm, m = 0 and 2)**

Note: Suffix "m" as register name and DU2 are only for RZ/G1H.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address: DU0: H'FEB0 0034, DU2: H'FEB4 0034



Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 16	CODE	—	—/W	Not available	DEF2Rm Enabling Code (register available code) For a value written to DEF2Rm to be effective, the value must include H'7775 in these bits.
15 to 1	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
0	DEFE2G	0	R/W	DRES	Display Unit Extensional Function Enable 2G 0: Extensional functions are disabled. 1: Extensional functions are enabled. The following extensional functions are enabled. Bits 13 and 12 in the plane n blending ratio register m (PnALPHARm) Bits 5 and 4 in the display capture control register m (DCPCRm)

Note: m = 0 and 2, suffix "m" is only for RZ/G1H.  
n = 1 to 8.

### 21.3.1.29 Display Unit Extensional Function Control 3 Register m (DEF3Rm, m = 0 and 2)

Note: Suffix "m" as register name and DU2 are only for RZ/G1H.

Address: DU0: H'FEB0 0038, DU2: H'FEB4 0038

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CODE															
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DEFE3
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 16	CODE	—	—/W	Not available	DEF3Rm Enabling Code (register available code) For a value written to DEF3Rm to be effective, the value must include H'7776 in these bits.
15 to 1	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
0	DEFE3	0	R/W	DRES	Display Unit Extensional Function Enable 3 0: Extensional functions are disabled. 1: Extensional functions are enabled. The following extensional functions are enabled. Bits 13, 12 and 8 in the display capture control register m (DCPCRm) Display video capture status register m (DVCSRm)

Note: m = 0 and 2, suffix "m" is only for RZ/G1H.

### 21.3.1.30 Display Unit Extensional Function Control 4 Register m (DEF4Rm, m = 0 and 2)

Note: Suffix "m" as register name and DU2 are only for RZ/G1H.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address: DU0: H'FEB0 003C, DU2: H'FEB4 003C

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CODE															
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	LRUO	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	0	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 16	CODE	—	-/W	Not available	DEF4Rm Enabling Code (register available code) For a value written to DEF4Rm to be effective, the value must include H'7777 in these bits.
15 to 6	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
5	LRUO	0	R/W	DRES	LRU Function Off 0: Requests for the AXI from the individual planes are arbitrated by the LRU system. 1: Requests for the AXI from the individual planes are arbitrated according to the following decreasing order of priority: plane 1, plane 2, plane 3, plane 4, plane 5, plane 6, plane 7, plane 8, α plane 1, α plane 2, display capture1, and display capture 2. When the display is 32-bit/pixel, set this bit to 1.
4 to 0	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

Note: m = 0 and 2, suffix "m" is only for RZ/G1H.

### 21.3.1.31 Display Unit Video Capture Status Register m (DVCSRm, m = 0 and 2)

Note: Suffix "m" as register name and DU2 are only for RZ/G1H.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address: DU0: H'FEB0 00D0, DU2: H'FEB4 00D0

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	VC3FB1/—*	VC2FB1/—*	VC1FB1	VC0FB1				
Initial value:	—	—	—	—	—	—	—	—	0/—*	0/—*	0/—*	0/—*	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	VC3FB/—*	VC2FB/—*	VC1FB	VC0FB				
Initial value:	—	—	—	—	—	—	—	—	0/—*	0/—*	0/—*	0/—*	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Note: \* For reserved bit (bit name: —), initial value is undefined. For details, refer to following table.

- To enable this register, set the DEFE3 bit in the display unit extensional function control 3 register m (DEF3Rm, m = 0 and 2) to 1. The value read from this register in its initial state is fixed to 0. Suffix "m" as register name is only for RZ/G1H.
- Video Capture is the same as Video Input.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 24	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
23, 22	VC3FB1	00	R	Not available	<p>Video Capture 3 Frame Buffer Flag 1 [RZ/G1H]</p> <p>These bits are updated with the same timing as internal updating of timing generator 1.</p> <p>00: In the plane set for video capture 3, the display area starts at the address indicated by PnDSA0Rm.</p> <p>01: In the plane set for video capture 3, the display area starts at the address indicated by PnDSA1Rm.</p> <p>10: In the plane set for video capture 3, the display area starts at the address indicated by PnDSA2Rm.</p> <p>11: The video capture 3 module is in its initial state.</p> <hr/> <p>Reserved [RZ/G1M/N/E]</p> <p>The read value is undefined. The write value should always be 0.</p>
21, 20	VC2FB1	00	R	Not available	<p>Video Capture 2 Frame Buffer Flag 1 [RZ/G1H/M/N]</p> <p>These bits are updated with the same timing as internal updating of timing generator 1.</p> <p>00: In the plane set for video capture 2, the display area starts at the address indicated by PnDSA0Rm.</p> <p>01: In the plane set for video capture 2, the display area starts at the address indicated by PnDSA1Rm.</p> <p>10: In the plane set for video capture 2, the display area starts at the address indicated by PnDSA2Rm.</p> <p>11: The video capture 2 module is in its initial state.</p> <hr/> <p>Reserved [RZ/G1E]</p> <p>The read value is undefined. The write value should always be 0.</p>
19, 18	VC1FB1	00	R	Not available	<p>Video Capture 1 Frame Buffer Flag 1</p> <p>These bits are updated with the same timing as internal updating of timing generator 1.</p> <p>00: In the plane set for video capture 1, the display area starts at the address indicated by PnDSA0Rm.</p> <p>01: In the plane set for video capture 1, the display area starts at the address indicated by PnDSA1Rm.</p> <p>10: In the plane set for video capture 1, the display area starts at the address indicated by PnDSA2Rm.</p> <p>11: The video capture 1 module is in its initial state.</p>
17, 16	VC0FB1	00	R	Not available	<p>Video Capture 0 Frame Buffer Flag 1</p> <p>These bits are updated with the same timing as internal updating of timing generator 1.</p> <p>00: In the plane set for video capture 0, the display area starts at the address indicated by PnDSA0Rm.</p> <p>01: In the plane set for video capture 0, the display area starts at the address indicated by PnDSA1Rm.</p> <p>10: In the plane set for video capture 0, the display area starts at the address indicated by PnDSA2Rm.</p> <p>11: The video capture 0 module is in its initial state.</p>
15 to 8	—	—	R	—	<p>Reserved</p> <p>The read value is undefined. The write value should always be 0.</p>

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
7, 6	VC3FB	00	R	Not available	<p>Video Capture 3 Frame Buffer Flag [RZ/G1H]</p> <p>These bits are updated with the same timing as internal updating of timing generator m*<sup>1</sup>.</p> <p>00: In the plane set for video capture 3, the display area starts at the address indicated by PnDSA0Rm*<sup>2</sup>.</p> <p>01: In the plane set for video capture 3, the display area starts at the address indicated by PnDSA1Rm*<sup>2</sup>.</p> <p>10: In the plane set for video capture 3, the display area starts at the address indicated by PnDSA2Rm*<sup>2</sup>.</p> <p>11: The video capture 3 module is in its initial state.</p>
	—	—		—	<p>Reserved [RZ/G1M/N/E]</p> <p>The read value is undefined. The write value should always be 0.</p>
5, 4	VC2FB	00	R	Not available	<p>Video Capture 2 Frame Buffer Flag [RZ/G1H/M/N]</p> <p>These bits are updated with the same timing as internal updating of timing generator m*<sup>1</sup>.</p> <p>00: In the plane set for video capture 2, the display area starts at the address indicated by PnDSA0Rm*<sup>2</sup>.</p> <p>01: In the plane set for video capture 2, the display area starts at the address indicated by PnDSA1Rm*<sup>2</sup>.</p> <p>10: In the plane set for video capture 2, the display area starts at the address indicated by PnDSA2Rm*<sup>2</sup>.</p> <p>11: The video capture 2 module is in its initial state.</p>
	—	—		—	<p>Reserved [RZ/G1E]</p> <p>The read value is undefined. The write value should always be 0.</p>
3, 2	VC1FB	00	R	Not available	<p>Video Capture 1 Frame Buffer Flag</p> <p>These bits are updated with the same timing as internal updating of timing generator m*<sup>1</sup>.</p> <p>00: In the plane set for video capture 1, the display area starts at the address indicated by PnDSA0Rm*<sup>2</sup>.</p> <p>01: In the plane set for video capture 1, the display area starts at the address indicated by PnDSA1Rm*<sup>2</sup>.</p> <p>10: In the plane set for video capture 1, the display area starts at the address indicated by PnDSA2Rm*<sup>2</sup>.</p> <p>11: The video capture 1 module is in its initial state.</p>
1, 0	VC0FB	00	R	Not available	<p>Video Capture 0 Frame Buffer Flag</p> <p>These bits are updated with the same timing as internal updating of timing generator m*<sup>1</sup>.</p> <p>00: In the plane set for video capture 0, the display area starts at the address indicated by PnDSA0Rm*<sup>2</sup>.</p> <p>01: In the plane set for video capture 0, the display area starts at the address indicated by PnDSA1Rm*<sup>2</sup>.</p> <p>10: In the plane set for video capture 0, the display area starts at the address indicated by PnDSA2Rm*<sup>2</sup>.</p> <p>11: The video capture 0 module is in its initial state.</p>

Notes: 1. m = 0 and 2 for RZ/G1H, m = 0 for RZ/G1M/N/E  
2. m = 0 and 2 for RZ/G1H, suffix m is only for RZ/G1H.



### 21.3.1.32 Display Unit Extensional Function Control 5 Register m (DEF5Rm, m = 0 and 2)

Note: Suffix "m" as register name and DU2 are only for RZ/G1H.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address: DU0: H'FEB0 00E0, DU2: H'FEB4 00E0

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CODE								—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	YCRGB1/—*	YCRGB0/—	DRC1/—*	DRC0/—*	—	—	—/RGBYC0*	—	—	—	—	—	—	—	—	DEFE5
Initial value:	0/—*	0/—*	0/—*	0/—*	0/—*	0/—*	0/—*	0/—*	—	—	—/0*	—/0*	—	—	—	0
R/W:	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R	R	R/W*	R/W*	R	R	R	R/W

Note: \* For reserved bit (bit name: —), initial value is undefined, writing is not available and writing value should be specified. For details, refer to following table.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 24	CODE	—	—/W	Not available	DEF5Rm*1 Enabling Code (register available code) For a value written to DEF5Rm*1 to be effective, the value must include H'66 in these bits.
23 to 16	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
15, 14	YCRGB1	00	R/W	Available	YC-RGB Select 1 [RZ/G1H] 00: YC-RGB conversion is not performed after superpositioning in superposition processor 1. 01: YC-RGB conversion is performed for the superposed result of priority levels 1 and 2 in superposition processor 1. 10: YC-RGB conversion is performed for the superposed result of priority levels 2 and 3 in superposition processor 1. 11: YC-RGB conversion is performed for the superposed result of priority levels 3 and 4 in superposition processor 1. DRC should have a priority equal to or lower than that of YC-RGB conversion. When YC-RGB conversion is performed, the functions of display capture in section 21.4.18, Display Capture and color detection in section 21.5.4, Color Detection cannot be used. For RZ/G1H, these bits are not provided in the display unit extensional function control 5 register 2 (DEF5R2).
—	—	—	R	—	Reserved [RZ/G1M/N/E] The read value is undefined. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
13, 12	YCRGB0	00	R/W	Available	<p>YC-RGB Select 1 [RZ/G1H]</p> <p>00: YC-RGB conversion is not performed after superpositioning in superposition processor m.</p> <p>01: YC-RGB conversion is performed for the superposed result of priority levels 1 and 2 in superposition processor m.</p> <p>10: YC-RGB conversion is performed for the superposed result of priority levels 2 and 3 in superposition processor m.</p> <p>11: YC-RGB conversion is performed for the superposed result of priority levels 3 and 4 in superposition processor m.</p> <p>DRC should have a priority equal to or lower than that of YC-RGB conversion.</p> <p>When YC-RGB conversion is performed, the functions of display capture in section 21.4.18, Display Capture and color detection in section 21.5.4, Color Detection cannot be used.</p>
—	—	—	R	—	<p>Reserved [RZ/G1M/N/E]</p> <p>The read value is undefined. The write value should always be 0.</p>
11, 10	DRC1	00	R/W	Available	<p>DRC Select 1 [RZ/G1H]</p> <p>00: DRC processing is not performed after superpositioning in superposition processor 1.</p> <p>01: DRC processing is performed for the superposed result of priority levels 1 and 2 in superposition processor 1.</p> <p>10: DRC processing is performed for the superposed result of priority levels 2 and 3 in superposition processor 1.</p> <p>11: DRC processing is performed for the superposed result of priority levels 3 and 4 in superposition processor 1.</p> <p>DRC should have a priority equal to or lower than that of YC-RGB conversion.</p> <p>For RZ/G1H, the superposition processors 0, 1 and 2 cannot use DRC simultaneously. Select either superposition processor 0, 1 or 2 by DU select register in DRC.</p> <p>When DRC processing is performed, the functions of display capture in section 21.4.18, Display Capture and color detection in section 21.5.4, Color Detection cannot be used.</p> <p>For RZ/G1H, these bits are not provided in the display unit extensional function control 5 register 2 (DEF5R2).</p>
—	—	—	R	—	<p>Reserved [RZ/G1M/N/E]</p> <p>The read value is undefined. The write value should always be 0.</p>

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
9, 8	DRC0	00	R/W	Available	<p>DRC Select 0 [RZ/G1H]</p> <p>00: DRC processing is not performed after superpositioning in superposition processor m*4.</p> <p>01: DRC processing is performed for the superposed result of priority levels 1 and 2 in superposition processor m*4.</p> <p>10: DRC processing is performed for the superposed result of priority levels 2 and 3 in superposition processor m*4.</p> <p>11: DRC processing is performed for the superposed result of priority levels 3 and 4 in superposition processor m*4.</p> <p>DRC should have a priority equal to or lower than that of YC- RGB conversion.</p> <p>For RZ/G1H, the superposition processors 0, 1 and 2 cannot use DRC simultaneously. Select either superposition processor 0, 1 or 2 by DU select register in DRC.</p> <p>When DRC processing is performed, the functions of display capture in section 21.4.18, Display Capture and color detection in section 21.5.4, Color Detection cannot be used.</p>
—	—	—	R	—	<p>Reserved [RZ/G1M/N/E]</p> <p>The read value is undefined. The write value should always be 0.</p>
7, 6	—	—	R	—	<p>Reserved</p> <p>The read value is undefined. The write value should always be 0.</p>

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
5, 4	—	—	R	—	Reserved [RZ/G1H] The read value is undefined. The write value should always be 0.
	RGBYC0	00	R/W	DRES	RGB-YC Converted Output 0 [RZ/G1M/N/E] 00: DU0 display output is RGB data format. 01: DU0 display output is RGB-YC converted multiplexed YC data format. 10: DU0 display output is RGB-YC converted non-multiplexed YC data format. 11: Setting prohibited For YC data format, set to 1 bits DCKOSEL and FRQSEL (division by 2) in the External Synchronization Control Register 0 (ESCR0). For performing RGB-YC conversion, the display capture function (section 21.4.18) or the color detection function (section 21.5.4) cannot be used.
3 to 1	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
0	DEFE5	0	R/W	DRES	Display Unit Extensional Function Enable 5 0: Extensional functions are disabled. 1: Extensional functions are enabled. The following extensional function is enabled. The number of bits is increased by one for the following registers: Display timing generation registers HDSRn*2, HDERn*2, VDERn*2, HCRn*2, VCRn*2, VSPrn*2, CLAMPsRn*2, CLAMPwRn*2, DESRn*2, and DEWRn*2 Display attribute registers RINTOFsRn*2 Display plane registers (alpha plane registers) PnDSXRm*3, PnDSYRm*3, PnDPXRm*3, and PnDPYRm*3

- Notes:
1. m = 0 and 2. suffix "m" is only for RZ/G1H.
  2. n = 0 to 2 for RZ/G1H ;0 and 1 for RZ/G1M/N/E.
  3. m = 0 and 2. suffix "m" is only for RZ/G1H.  
n = 1 to 8.
  4. m = 0 and 2 for RZ/G1H.

### 21.3.1.33 Display Unit Data Latency Adjustment Register (DDLTR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address: DU0: H'FEb0 00E4

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CODE															
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—/DLAR1	DLAY1 /—*	DLAD1 /—*	—	—	DLAY0 /—*	DLAD0 /—*
Initial value:	—	—	—	—	—	—	—	—	—	—/0*	0/—*	0/—*	—	—	0/—*	0/—*
R/W:	R	R	R	R	R	R	R	R	R	R/W	R/W*	R/W*	R	R	R/W*	R/W*

Note: \* For reserved bit (bit name: —), initial value is undefined, writing is not available and writing value should be specified. For details, refer to following table.

This register is used to adjust the latency of two display data items output from the DU0 and DU1 when two image data items are output from the DU pins on both edges (rising and falling edges) of the output dot clock. This register should not be changed from its initial value when the DR0D bit in the display unit output route control register m (DORCRm, m = 0) is 0. When the DR0D bit is set to 1 (when two image data items are output from the DU pins on both edges of the output dot clock), set the necessary bits in this register to 1. Suffix "m" as register name is only for RZ/G1H.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 16	CODE	—	—/W	Not available	DDLTRm Enabling Code (register available code) For a value written to DDLTRm to be effective, the value must include H'7766 in these bits.
15 to 7	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
6	—	—	R	—	Reserved [RZ/G1H] The read value is undefined. The write value should always be 0.
	DLAR1	0	R/W	DRES	Display Data Latency Adjustment RGBYC1 [RZ/G1M/N/E] Set this bit to 1 in order to adjust the latency on the DU1 side when the RGBYC0 bit in the display unit extensional function control 5 register (DEF5R) is set to B'10 (RGB-YC conversion is performed). 0: DU1 display data is output without delay. 1: DU1 display data is output with a delay corresponding to the latency of RGB-YC conversion on the DU0 side.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
5	DLAY1	0	R/W	DRES	<p>Display Data Latency Adjustment YCRGB1 [RZ/G1H]</p> <p>Set this bit to 1 in order to adjust the latency on the DU1 side when the values of the YCRGB0 and YCRGB1 bits in the display unit extensional function control 5 register m (DEF5Rm) are set to B'01 or B'10 (RGB-YC conversion is performed) and B'00 (YC- RGB conversion is not performed), respectively.</p> <p>0: DU1 display data is output without delay.</p> <p>1: DU1 display data is output with a delay corresponding to the latency of YC- RGB conversion after DRC on the DU0 side.</p>
—	—	—	R	—	<p>Reserved [RZ/G1M/N/E]</p> <p>The read value is undefined. The write value should always be 0.</p>
4	DLAD1	0	R/W	DRES	<p>Display Data Latency Adjustment DRC1 [RZ/G1H]</p> <p>Set this bit to 1 in order to adjust the latency on the DU1 side when the value of the DRC0 bit in the display unit extensional function control 5 register m (DEF5Rm) is B'01, B'10, or B'11 (DRC is performed).</p> <p>0: DU1 display data is output without delay.</p> <p>1: DU1 display data is output with a delay corresponding to the latency of DRC on the DU0 side.</p>
—	—	—	R	—	<p>Reserved [RZ/G1M/N/E]</p> <p>The read value is undefined. The write value should always be 0.</p>
3, 2	—	—	R	—	<p>Reserved</p> <p>The read value is undefined. The write value should always be 0.</p>
1	DLAY0	0	R/W	DRES	<p>Display Data Latency Adjustment YCRGB0 [RZ/G1H]</p> <p>Set this bit to 1 in order to adjust the latency on the DU0 side when the values of the YCRGB1 and YCRGB0 bits in the display unit extensional function control 5 register m (DEF5Rm) are B'01, B'10, or B'11 (YC- RGB conversion is performed) and 00 (YC- RGB conversion is not performed), respectively.</p> <p>0: DU0 display data is output without delay.</p> <p>1: DU0 display data is output with a delay corresponding to the latency of YC- RGB conversion after DRC on the DU1 side.</p>
—	—	—	R	—	<p>Reserved [RZ/G1M/N/E]</p> <p>The read value is undefined. The write value should always be 0.</p>
0	DLAD0	0	R/W	DRES	<p>Display Data Latency Adjustment DRC0 [RZ/G1H]</p> <p>Set this bit to 1 in order to adjust the latency on the DU0 side when the value of the DRC1 bit in the display unit extensional function control 5 register m (DEF5Rm) is B'01, B'10, or B'11 (DRC is performed).</p> <p>0: DU0 display data is output without delay.</p> <p>1: DU0 display data is output with a delay corresponding to the latency of DRC on the DU1 side.</p>
—	—	—	R	—	<p>Reserved [RZ/G1M/N/E]</p> <p>The read value is undefined. The write value should always be 0.</p>

Note: m = 0. suffix "m" is only for RZ/G1H

### 21.3.1.34 Display Unit Extensional Function Control 6 Register m (DEF6Rm, m = 0 and 2)

Note: Suffix "m" as register name and DU2 are only for RZ/G1H.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address: DU0: H'FEB0 00E8, DU2: H'FEB4 00E8

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CODE															
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	ODPM12	ODPM02	—	—	—	—	—	—/MLOS1*	MLOS0	—	—	
Initial value:	—	—	—	—	0	0	0	0	—	—	—	—	—/0*	0	—	—
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R	R	R	R	R/W*	R/W	R	R

Note: \* For reserved bit (bit name: —), initial value is undefined, writing is not available and writing value should be specified. For details, refer to following table.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 16	CODE	—	—/W	Not available	DEF6Rm* <sup>5</sup> Enabling Code (register available code) For a value written to DEF6Rm* <sup>5</sup> to be effective, the value must include H'7778 in these bits.
15 to 12	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
11, 10	ODPM12	00	R/W	DRES	ODDF Pin Mode 12 00: The ODDF pin function is determined by the ODPM bit in the display unit mode register 1 (DSMR1). 01: Setting prohibited. 10: The DISP signal is output to the ODDF pin, which is a DU1 pin. Even if the TVM1 bits in the display unit system control register 1 (DSYSR1) indicate TV synchronized mode, the ODDF pin becomes an output. 11: The CDE signal is output to the ODDF pin, which is a DU1 pin. Even if the TVM1 bits in the display unit system control register 1 (DSYSR1) indicate TV synchronized mode, the ODDF pin becomes an output. "ODDF pin" refers to the DU_EXODDF/DU_ODDF pin indicated in Table 21.1a* <sup>3</sup> . "ODDF pin" refers to the DU1_ODDF/DU1_EXODDF pin indicated in Table 21.1a* <sup>7</sup> . "ODDF pin" refers to the DU1_ODDF/DU1_EXODDF pin indicated in Table 21.1c* <sup>2</sup> . For RZ/G1H, these bits are not provided in the display unit extensional function control 6 register 2 (DEF6R2).

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
9, 8	ODPM02	00	R/W	DRES	<p>ODDF Pin Mode 02</p> <p>00: The ODDF pin function is determined by the ODPM bit in the display unit mode register m (DSMRm*<sup>6</sup>).</p> <p>01: Setting prohibited.</p> <p>10: The DISP signal is output to the ODDF pin, which are DU0 and DU2*3 pins. Even if the TVM bits in display unit system control register m (DSYSRm*<sup>6</sup>) indicate TV synchronized mode, the ODDF pin becomes an output.</p> <p>11: The CDE signal is output to the ODDF pin, which are DU0 and DU2*3 pins. Even if the TVM bits in display unit system control register m (DSYSRm*<sup>6</sup>) indicate TV synchronized mode, the ODDF pin becomes an output.</p> <p>"ODDF pin" refers to the DU_EXODDF/DU_ODDF pin indicated in Table 21.1a*<sup>3</sup>.</p> <p>"ODDF pin" refers to the DU1_ODDF/DU1_EXODDF pin indicated in Table 21.1a*<sup>7</sup>.</p> <p>"ODDF pin" refers to the DU0_ODDF/DU0_EXODDF pin indicated in Table 21.1b*<sup>2</sup>.</p>
7 to 4	—	—	R	—	<p>Reserved</p> <p>The read value is undefined. The write value should always be 0.</p>
3	—	—	R	—	<p>Reserved [RZ/G1H]</p> <p>The read value is undefined. The write value should always be 0.</p>
	MLOS1	0	R/W	DRES	<p>Multiple Output Select 1 [RZ/G1M/N/E]</p> <p>0: DU1 pins function as a 24-bit non-multiple output.</p> <p>1: DU1 pins output 12-bit data generated by multiplexing 24-bit data. When this bit is set to 1, set the DCKOINV bit in the external synchronization control register 1 (ESCR1) to 1.</p>



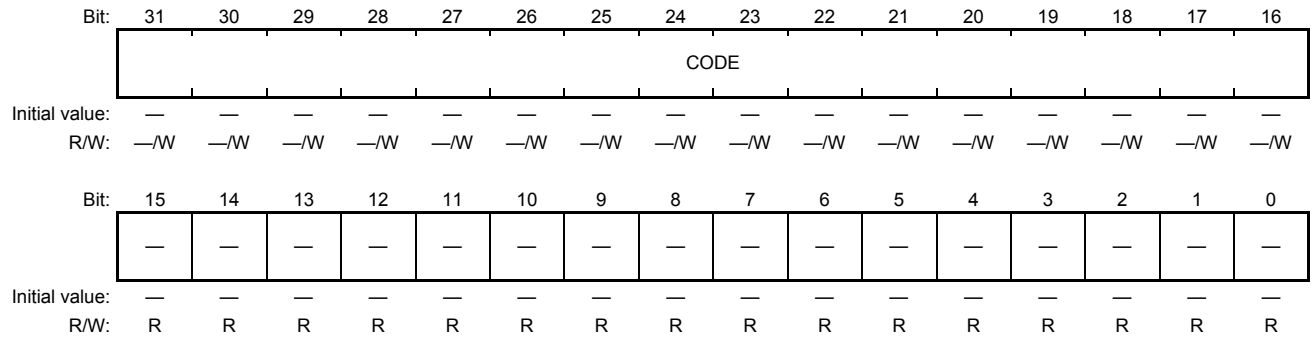
Bit	Bit Name	Initial Value	R/W	Internal Update	Description
2	MLOS0	0	R/W	DRES	Multiple Output Select 0 0: DU0 and DU2* <sup>3</sup> pins function as a 24-bit non-multiple output. 1: DU0 and DU2* <sup>3</sup> pins output 12-bit data generated by multiplexing 24-bit data. When this bit is set to 1, set the DCKOINV bit in the external synchronization control register m (ESCRm* <sup>6</sup> ) to 1.
1, 0	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

- Notes:
1. For RZ/G1H/M/N
  2. For RZ/G1E
  3. For RZ/G1H
  4. For RZ/G1M/N/E
  5. m = 0 and 2. suffix "m" is only for RZ/G1H.
  6. m = 0 and 2 for RZ/G1H, m = 0 for RZ/G1M/N/E.
  7. For RZ/G1M/N

**21.3.1.35 Display Unit Extensional Function Control 7 Register (DEF7R)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
—	√	√	—

Address: DU0: H'FEB0 00EC



Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 16	CODE	—	—/W	Not available	DEF7R Enabling Code (register available code) For a value written to DEF7R to be effective, the value must include H'7779 in these bits.
15 to 0	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

### 21.3.1.36 Display Unit Extensional Function Control 8 Register m (DEF8Rm, m = 0 and 2)

Note: Suffix "m" as register name and DU2 are only for RZ/G1H.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address: DU0: H'FEB2 0020, DU2: H'FEB6 0020

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CODE															
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	VSCS /—*	DRGBS/—*	—	—	—/— YCOD*	DEFEB8	
Initial value:	—	—	—	—	—	—	—	—	—	0/—*	0/—*	0/—*	—	—	—/0*	0
R/W:	R	R	R	R	R	R	R	R	R	R/W*	R/W*	R/W*	R	R	R/W*	R/W

Note: \* For reserved bit (bit name: —), initial value is undefined, writing is not available and writing value should be specified. For details, refer to following table.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 16	CODE	—	—/W	Not available	DEF8Rm* <sup>1</sup> Enabling Code (register available code) For a value written to DEF8Rm* <sup>1</sup> to be effective, the value must include H'7790 in these bits.
15 to 7	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
6	VSCS	0	R/W	DRES	VSP1 Channel Select [RZ/G1H] 0: VSP1-ch1 is connected with the DU0/DU1 plane 2. 1: VSP1-ch1 is connected with the DU2 plane 1. To display the VSP1 image data, make the setting in the plane n display data control 4 register m (PnDDC4Rm* <sup>2</sup> ). VSP1-ch0 is always connected with the DU1/DU0 plane 1. VSP1-ch1 cannot be used at the same time in the DU0/DU1 and DU2. This bit is not provided in the display unit extensional function control 8 register 2 (DEF8R2).
—	—	—	R	—	Reserved [RZ/G1M/N/E] The read value is undefined. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
5, 4	DRGBS	00	R/W	DRES	<p>Digital RGB Output Select [RZ/G1H/M/N]</p> <p>These bits are used to select the digital RGB signal output from the DPAD (shown in Figure 21.1, Block Diagram of the Display Unit).</p> <p>00: Digital RGB signal from the DU0 is selected.            01: Digital RGB signal from the DU1 is selected.            10: Digital RGB signal from the DU2 is selected. [RZ/G1H] Setting prohibited. [RZ/G1M/N]            11: Setting prohibited.</p> <ul style="list-style-type: none"> <li>For RZ/G1H, these bits are not provided in the display unit extensional function control 8 register 2 (DEF8R2).</li> <li>For selection of signals output from the LVDS, refer to the target specifications of the LVDS.</li> </ul>
	—	—	R	—	<p>Reserved [RZ/G1E]</p> <p>The read value is undefined. The write value should always be 0.</p>
3, 2	—	—	R	—	<p>Reserved</p> <p>The read value is undefined. The write value should always be 0.</p>
1	—	—	R	—	<p>Reserved [RZ/G1H]</p> <p>The read value is undefined. The write value should always be 0.</p>
	YCOD	0	R/W	DRES	<p>YC Off mode Output Data [RZ/G1M/N/E]</p> <p>0: When data is displayed in YC format, UV data in YC off mode is H'00.            1: When data is displayed in YC format, UV data in YC off mode is H'80.</p>
0	DEFE8	0	R/W	DRES	<p>Display Unit Extensional Function Enable 8</p> <p>0: Extensional functions are disabled.            1: Extensional functions are enabled.</p> <p>The following extensional functions are enabled.</p> <p>Bit 12 in the display unit status register m (DSSRm*3)            Bit 13 in the plane n display data control 4 register m (PnDDC4Rm*2)</p>

- Notes:
- m = 0 and 2. suffix "m" is only for RZ/G1H.
  - m = 0 and 2. suffix "m" is only for RZ/G1H.  
n = 1 to 8.
  - m = 0 and 2 for RZ/G1H, m = 0 for RZ/G1M/N/E.

### 21.3.1.37 Display Unit Output Signal Fixed Level Register m (DOFLRm, m = 0 and 2)

Note: Suffix "m" as register name and DU2 are only for RZ/G1H.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address: DU0: H'FEB2 0024, DU2: H'FEB6 0024

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CODE															
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	HSYCF L1	VSYCF L1	ODDFL 1	DISP FL1	CDEFL 1	RGB FL1	—	—	HSYCF L0	VSYCF L0	ODDFL 0	DISPFL 0	CDEFL 0	RGBFL 0
Initial value:	—	—	0	0	0	0	0	0	—	—	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 16	CODE	—	—/W	Not available	DOFLRm Enabling Code (register available code) For a value written to DOFLRm to be effective, the value must include H'7790 in these bits.
15, 14	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
13	HSYCF L1	0	R/W	Not available	HSYNC (DU1) Signal Fixed Low Level 0: HSYNC (DU1) output is normal. 1: HSYNC (DU1) output is fixed low. This bit setting is effective only in master mode. For RZ/G1H, this bit is not provided in the display unit output signal fixed level register 2 (DOFLR2).
12	VSYCF L1	0	R/W	Not available	VSYNC (DU1) Signal Fixed Low Level 0: VSYNC (DU1) output is normal. 1: VSYNC (DU1) output is fixed low. This bit setting is effective only in master mode. For RZ/G1H, this bit is not provided in the display unit output signal fixed level register 2 (DOFLR2).
11	ODDFL 1	0	R/W	Not available	ODDF (DU1) Signal Fixed Low Level 0: ODDF (DU1) output is normal. 1: ODDF (DU1) output is fixed low. This bit setting is effective only in master mode. For RZ/G1H, this bit is not provided in the display unit output signal fixed level register 2 (DOFLR2).
10	DISPFL 1	0	R/W	Not available	DISP (DU1) Signal Fixed Low Level 0: DISP (DU1) output is normal. 1: DISP (DU1) output is fixed low. For RZ/G1H, this bit is not provided in the display unit output signal fixed level register 2 (DOFLR2).

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
9	CDEFL1	0	R/W	Not available	CDE (DU1) Signal Fixed Low Level 0: CDE (DU1) output is normal. 1: CDE (DU1) output is fixed low. For RZ/G1H, this bit is not provided in the display unit output signal fixed level register 2 (DOFLR2).
8	RGBFL1	0	R/W	Not available	RGB (DU1) Signal Fixed Low Level 0: RGB (DU1) output is normal. 1: RGB (DU1) output is fixed low. For RZ/G1H, this bit is not provided in the display unit output signal fixed level register 2 (DOFLR2).
7, 6	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
5	HSYCFL0	0	R/W	Not available	HSYNC (DU0 and DU2) Signal Fixed Low Level 0: HSYNC (DU0 and DU2) output is normal. 1: HSYNC (DU0 and DU2) output is fixed low. This bit setting is effective only in master mode. Note: DU2 is only for RZ/G1H.
4	VSYCFL0	0	R/W	Not available	VSYNC (DU0 and DU2) Signal Fixed Low Level 0: VSYNC (DU0 and DU2) output is normal. 1: VSYNC (DU0 and DU2) output is fixed low. This bit setting is effective only in master mode. Note: DU2 is only for RZ/G1H.
3	ODDFL0	0	R/W	Not available	ODDF (DU0 and DU2) Signal Fixed Low Level 0: ODDF (DU0 and DU2) output is normal. 1: ODDF (DU0 and DU2) signal at fixed low level. This bit setting is effective only in master mode. Note: DU2 is only for RZ/G1H.
2	DISPFL0	0	R/W	Not available	DISP (DU0 and DU2) Signal Fixed Low Level 0: DISP (DU0 and DU2) output is normal. 1: DISP (DU0 and DU2) output is fixed low. Note: DU2 is only for RZ/G1H.
1	CDEFL0	0	R/W	Not available	CDE (DU0 and DU2) Signal Fixed Low Level 0: CDE (DU0 and DU2) output is normal. 1: CDE (DU0 and DU2) output is fixed low. Note: DU2 is only for RZ/G1H.
0	RGBFL0	0	R/W	Not available	RGB (DU0 and DU2) Signal Fixed Low Level 0: RGB (DU0 and DU2) output is normal. 1: RGB (DU0 and DU2) output is fixed low. Note: DU2 is only for RZ/G1H.

Note: m = 0 and 2. suffix "m" is only for RZ/G1H

### 21.3.1.38 Display Unit Input Dot Clock Select Register (DIDSR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address: H'FEB2 0028

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CODE															
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	LDCS2/—*	LDCS1/—*	LDCS0/—*	—	—	PDCS2/—*	PDCS1	PDCS0						
Initial value:	—	—	0/—*	0/—*	0/—*	0/—*	0/—*	0/—*	—	—	0/—*	0/—*	0	0	0	0
R/W:	R	R	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R	R	R/W*	R/W*	R/W	R/W	R/W	R/W

Note: \* For reserved bit (bit name: —), initial value is undefined, writing is not available and writing value should be specified. For details of bit description, refer to following table.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 16	CODE	—	—/W	Not available	DIDSR Enabling Code (register available code) For a value written to DIDSR to be effective, the value must include H'7790 in these bits.
15, 14	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
13, 12	LDCS2	00	R/W	DRES	DU2 LVDS Dot Clock Select [RZ/G1H] 0-: The DU2 input dot clock source is the DCLKIN pin. 10: The DU2 input dot clock source is the LVDS0 pin* <sup>3</sup> . 11: The DU2 input dot clock source is the LVDS1 pin* <sup>3</sup> .
	—	—	R	—	Reserved [RZ/G1M/N/E] The read value is undefined. The write value should always be 0.
11, 10	LDCS1	00	R/W	DRES	DU1 LVDS Dot Clock Select [RZ/G1H] 0-: The DU1 input dot clock source is the DCLKIN pin. 10: The DU1 input dot clock source is the LVDS0 pin* <sup>3</sup> . 11: The DU1 input dot clock source is the LVDS1 pin* <sup>3</sup> .
	—	—	R	—	Reserved [RZ/G1M/N/E] The read value is undefined. The write value should always be 0.
9, 8	LDCS0	00	R/W	DRES	DU0 LVDS Dot Clock Select [RZ/G1H/M/N] 0-: The DU0 input dot clock source is the DCLKIN pin. 10: The DU0 input dot clock source is the LVDS0 pin* <sup>3</sup> . 11: The DU0 input dot clock source is the LVDS1 pin* <sup>3</sup> . [RZ/G1H] Setting prohibited. [RZ/G1M/N]
	—	—	R	—	Reserved [RZ/G1E] The read value is undefined. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
7, 6	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
5, 4	PDCS2	00	R/W	DRES	DU2 Pad Dot Clock Select [RZ/G1H] -0: The DU2 input dot clock source is the DU_DOTCLKIN2 pin. 01: The DU2 input dot clock source is the DU_DOTCLKIN0 pin. 11: The DU2 input dot clock source is the DU_DOTCLKIN1 pin.
	—	—	R	—	Reserved [RZ/G1M/N/E] The read value is undefined. The write value should always be 0.
3, 2	PDCS1	00	R/W	DRES	DU1 Pad Dot Clock Select -0: The DU1 input dot clock source is the DU_DOTCLKIN1*2 pin. 01: The DU1 input dot clock source is the DU_DOTCLKIN0*1 pin. 11: The DU1 input dot clock source is the DU_DOTCLKIN2 pin. [RZ/G1H] Setting prohibited. [RZ/G1M/N/E]
1, 0	PDCS0	00	R/W	DRES	DU0 Pad Dot Clock Select -0: The DU0 input dot clock source is the DU_DOTCLKIN0*1 pin. 01: The DU0 input dot clock source is the DU_DOTCLKIN1*2 pin. 11: The DU0 input dot clock source is the DU_DOTCLKIN2 pin. [RZ/G1H] Setting prohibited. [RZ/G1M/N/E]

- Notes:
1. DU\_DOTCLKIN0 for RZ/G1H, DU0\_DOTCLKIN for RZ/G1M/N/E.
  2. DU\_DOTCLKIN1 for RZ/G1H, DU1\_DOTCLKIN for RZ/G1M/N/E.
  3. LVDS0 pin and LVDS1 pin mean the equivalent clock of the internal CLK clock from the LVDS0 PLL and LVDS1 PLL respectively. When setting B'10 or B'11 to LDCSx, the LVDS must be enabled.



### 21.3.2 Display Timing Generation Registers

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Note: All registers in section 21.3.2 are common to RZ/G1H, M, N and E.

The sets of display timing generation registers are for the respective channels and have the same functions; they are described as one here.

In section 21.3.2, n = 0 to 2 for RZ/G1H, 0 and 1 for RZ/G1M/N/E. m = 0 and 2, suffix "m" as register name and DU2 are only for RZ/G1H.

#### 21.3.2.1 Horizontal Display Start Register n (HDSRn)

Address: DU0: H'FEB0 0040, DU1: H'FEB30 040, DU2: H'FEB4 0040

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	HDS									
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 10	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
9 to 0	HDS	—	R/W	Available	Horizontal Display Start To enable bit 9, set the DEFE5 bit in the display unit extensional function control 5 register m (DEF5Rm) to 1. In the initial state, bit 9 cannot be written to. These bits are used to set the horizontal display start position in dot clock units. The set value is retained at a reset.

### 21.3.2.2 Horizontal Display End Register n (HDERn)

Address: DU0: H'FEB0 0044, DU1: H'FEB3 0044 DU2: H'FEB4 0044

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	HDE											
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 12	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
11 to 0	HDE	—	R/W	Available	Horizontal Display End To enable bit 11, set the DEFE5 bit in the display unit extensional function control 5 register m (DEF5Rm) to 1. In the initial state, bit 11 cannot be written to. These bits are used to set the horizontal display end position in dot clock units. The set value is retained at a reset.

### 21.3.2.3 Vertical Display Start Register n (VDSRn)

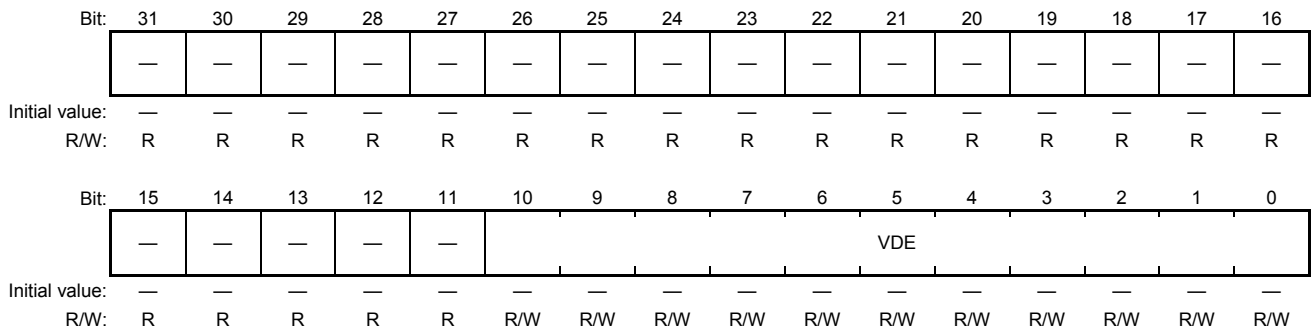
Address: DU0: H'FEB0 0048, DU1: H'FEB3 0048, DU2: H'FEB4 0048

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	VDS								
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 9	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
8 to 0	VDS	—	R/W	Available	Vertical Display Start These bits are used to set the vertical display start position in raster line units. The set value is retained at a reset.

**21.3.2.4 Vertical Display End Register n (VDERn)**

Address: DU0: H'FEB0 004C, DU1: H'FEB3 004C, DU2: H'FEB4 004C



Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 11	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
10 to 0	VDE	—	R/W	Available	Vertical Display End To enable bit 10, set the DEFE5 bit in the display unit extensional function control 5 register m (DEF5Rm) to 1. In the initial state, bit 10 cannot be written to. These bits are used to set the vertical display end position in raster line units. The set value is retained at a reset.

### 21.3.2.5 Horizontal Cycle Register n (HCRn)

Address: DU0: H'FEB0 0050, DU1: H'FEB3 0050, DU2: H'FEB4 0050

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	HC											
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 12	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
11 to 0	HC	—	R/W	Available	Horizontal Cycle To enable bit 11, set the DEFE5 bit in the display unit extensional function control 5 register m (DEF5Rm) to 1. In the initial state, bit 11 cannot be written to. These bits are used to set one horizontal scan cycle including the horizontal blanking period in dot clock units. In TV synchronized mode, set this register so that the HSYNC cycle set with this register is equal to or greater than the EXHSYNC cycle. The set value is retained at a reset.

### 21.3.2.6 Horizontal Sync Width Register n (HSWRn)

Address: DU0: H'FEB0 0054, DU1: H'FEB3 0054, DU2: H'FEB4 0054

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	HSW								
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 9	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
8 to 0	HSW	—	R/W	Available	Horizontal Sync Width These bits are used to set the low-level pulse width of the horizontal synchronous signal in dot clock units. The set value is retained at a reset.

### 21.3.2.7 Vertical Cycle Register n (VCRn)

Address: DU0: H'FEB0 0058, DU1: H'FEB3 0058, DU2: H'FEB4 0058

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	VC										
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 11	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
10 to 0	VC	—	R/W	Available	Vertical Cycle To enable bit 10, set the DEFE5 bit in the display unit extensional function control 5 register m (DEF5Rm) to 1. In the initial state, bit 10 cannot be written to. These bits are used to set the vertical scan cycle including the vertical blanking period in raster line units. In TV synchronized mode, set the time limit of the EXVSYNC rising edge detection. If the EXVSYNC rising edge is not detected within the time limit, the result is reflected in bit 15 of the display unit status register n (DSSRn). The set value is retained at a reset.

### 21.3.2.8 Vertical Sync Point Register n (VSPRn)

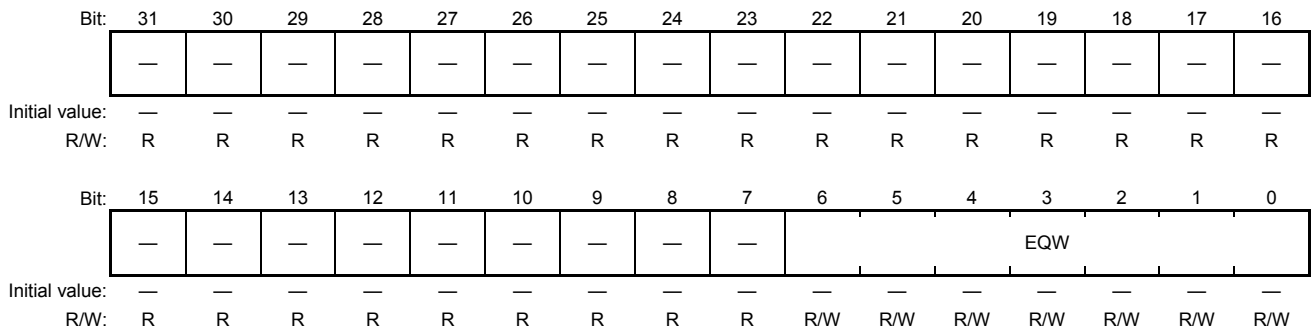
Address: DU0: H'FEB0 005C, DU1: H'FEB3 005C, DU2: H'FEB4 005C

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	VSP										
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 11	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
10 to 0	VSP	—	R/W	Available	Vertical Sync Point To enable bit 10, set the DEFE5 bit in the display unit extensional function control 5 register m (DEF5Rm) to 1. In the initial state, bit 10 cannot be written to. These bits are used to set the vertical synchronous signal start position in raster line units. In TV synchronized mode, set this register so that the VSYNC falling edge setting position set with this register is the same as or comes after that of the EXVSYNC falling edge. The set value is retained at a reset.

**21.3.2.9 Equal Pulse Width Register n (EQWRn)**

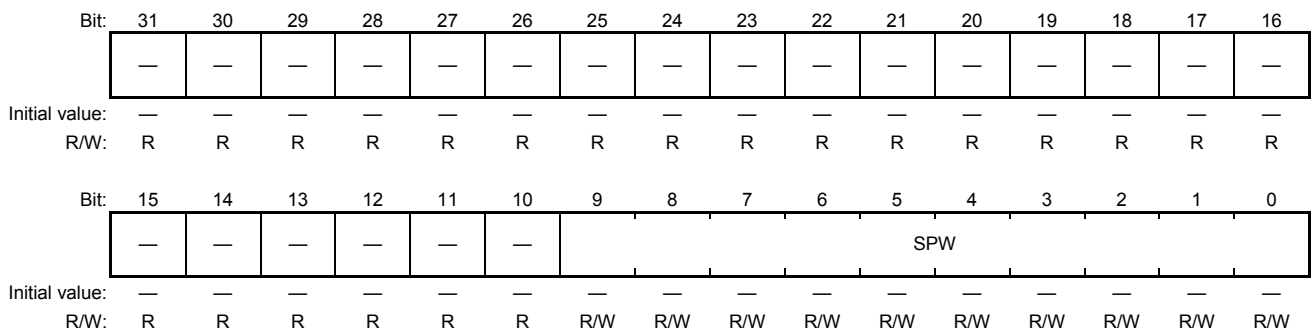
Address: DU0: H'FEB0 0060, DU1: H'FEB3 0060, DU2: H'FEB4 0060



Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 7	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
6 to 0	EQW	—	R/W	Available	Equal Pulse Width These bits are used to set the low-level equalizing pulse width of the CSYNC signal in dot clock units. To validate this setting, set bit 7 in the display unit mode register n (DSMRn)/CSYNC mode (CSY) to 1. The set value is retained at a reset.

**21.3.2.10 Serration Width Register n (SPWRn)**

Address: DU0: H'FEB0 0064, DU1: H'FEB3 0064, DU2: H'FEB4 0064



Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 10	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
9 to 0	SPW	—	R/W	Available	Serration Width These bits are used to set the low-level serration pulse width of the CSYNC signal in dot clock units. Set a value smaller than 1/2 of HC. To validate this setting, set bit 7 in the display unit mode register n (DSMRn)/CSYNC mode (CSY) to 1. The set value is retained at a reset.

**21.3.2.11 CLAMP Signal Start Register n (CLAMPSRn)**

Address: DU0: H'FEB0 0070, DU1: H'FEB3 0070, DU2: H'FEB4 0070

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	CLAMPS											
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 12	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
11 to 0	CLAMPS	—	R/W	Available	<p>CLAMP Signal Start</p> <p>To enable bit 11, set the DEFE5 bit in the display unit extensional function control 5 register m (DEF5Rm) to 1. In the initial state, bit 11 cannot be written to.</p> <p>These bits are used to set the CLAMP signal rising edge position in dot clock units, using as the reference the HSYNC signal falling edge.</p> <p>The CLAMP signal rises (setting value + 1) cycle after the HSYNC signal falls. Therefore, the CLAMP signal cannot rise in the same cycle as the HSYNC signal falling edge.</p> <p>The set value is retained at a reset.</p>



**21.3.2.12 CLAMP Signal Width Register n (CLAMPWRn)**

Address: DU0: H'FEB0 0074, DU1: H'FEB3 0074, DU2: H'FEB4 0074

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	—	—	—	—	CLAMPW												—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 12	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
11 to 0	CLAMPW	—	R/W	Available	<p>CLAMP Signal Width</p> <p>To enable bit 11, set the DEFE5 bit in the display unit extensional function control 5 register m (DEF5Rm) to 1. In the initial state, bit 11 cannot be written to.</p> <p>These bits are used to set the high-level width of the CLAMP signal in dot clock units.</p> <p>When the CLAMP signal is high, if the HSYNC signal falls, the CLAMP signal falls.</p> <p>The set value is retained at a reset.</p>

**21.3.2.13 DE Signal Start Register n (DESRn)**

Address: DU0: H'FEB0 0078, DU1: H'FEB3 0078, DU2: H'FEB4 0078

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	DES											
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 12	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
11 to 0	DES	—	R/W	Available	<p>DE Signal Start</p> <p>To enable bit 11, set the DEFE5 bit in the display unit extensional function control 5 register m (DEF5Rm) to 1. In the initial state, bit 11 cannot be written to.</p> <p>These bits are used to set the DE signal rising edge position in dot clock units, using as the reference the HSYNC signal falling edge.</p> <p>The DE signal rises (setting value + 1) cycle after the HSYNC signal falls. Therefore, the DE signal cannot rise in the same cycle as the HSYNC signal falling edge.</p> <p>During a vertical blanking period, the DE signal is fixed to the low level.</p> <p>The set value is retained at a reset.</p>

**21.3.2.14 DE Signal Width Register n (DEWRn)**

Address: DU0: H'FEB0 007C, DU1: H'FEB3 007C, DU2: H'FEB4 007C

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	DEW											
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 12	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
11 to 0	DEW	—	R/W	Available	DE Signal Width To enable bit 11, set the DEFE5 bit in the display unit extensional function control 5 register m (DEF5Rm) to 1. In the initial state, bit 11 cannot be written to. These bits are used to set the high-level width of the DE signal in dot clock units. When the DE signal is high, if the HSYNC signal falls, the DE signal falls. The set value is retained at a reset.

### 21.3.3 Display Attribute Registers

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Note: All registers in section 21.3.3 are common to RZ/G1H, M, N and E.

In section 21.3.3, n = 0 to 2 for RZ/G1H, 0 and 1 for RZ/G1M/N/E. Without instructions in particular, m = 0 and 2, suffix "m" as register name and DU2 are only for RZ/G1H.

#### 21.3.3.1 Color Palette 1 Transparent Color Register m (CP1TRm, m = 0 and 2)

Address: DU0: H'FEB0 0080, DU2: H'FEB4 0080

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CP1IF	CP1IE	CP1ID	CP1IC	CP1IB	CP1IA	CP1I9	CP1I8	CP1I7	CP1I6	CP1I5	CP1I4	CP1I3	CP1I2	CP1I1	CP1I0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 16	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
15	CP1IF	0	R/W	Available	Color Palette 1 Index F This bit is used to specify the color palette 1 transparent color. 0: Does not set the color of the color palette 1 index F to the transparent color. 1: Sets the color of the color palette 1 index F to the transparent color.
14	CP1IE	0	R/W	Available	Color Palette 1 Index E This bit is used to specify the color palette 1 transparent color. 0: Does not set the color of the color palette 1 index E to the transparent color. 1: Sets the color of the color palette 1 index E to the transparent color.
13	CP1ID	0	R/W	Available	Color Palette 1 Index D This bit is used to specify the color palette 1 transparent color. 0: Does not set the color of the color palette 1 index D to the transparent color. 1: Sets the color of the color palette 1 index D to the transparent color.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
12	CP1IC	0	R/W	Available	<p>Color Palette 1 Index C</p> <p>This bit is used to specify the color palette 1 transparent color.</p> <p>0: Does not set the color of the color palette 1 index C to the transparent color.</p> <p>1: Sets the color of the color palette 1 index C to the transparent color.</p>
11	CP1IB	0	R/W	Available	<p>Color Palette 1 Index B</p> <p>This bit is used to specify the color palette 1 transparent color.</p> <p>0: Does not set the color of the color palette 1 index B to the transparent color.</p> <p>1: Sets the color of the color palette 1 index B to the transparent color.</p>
10	CP1IA	0	R/W	Available	<p>Color Palette 1 Index A</p> <p>This bit is used to specify the color palette 1 transparent color.</p> <p>0: Does not set the color of the color palette 1 index A to the transparent color.</p> <p>1: Sets the color of the color palette 1 index A to the transparent color.</p>
9	CP1I9	0	R/W	Available	<p>Color Palette 1 Index 9</p> <p>This bit is used to specify the color palette 1 transparent color.</p> <p>0: Does not set the color of the color palette 1 index 9 to the transparent color.</p> <p>1: Sets the color of the color palette 1 index 9 to the transparent color.</p>
8	CP1I8	0	R/W	Available	<p>Color Palette 1 Index 8</p> <p>This bit is used to specify the color palette 1 transparent color.</p> <p>0: Does not set the color of the color palette 1 index 8 to the transparent color.</p> <p>1: Sets the color of the color palette 1 index 8 to the transparent color.</p>
7	CP1I7	0	R/W	Available	<p>Color Palette 1 Index 7</p> <p>This bit is used to specify the color palette 1 transparent color.</p> <p>0: Does not set the color of the color palette 1 index 7 to the transparent color.</p> <p>1: Sets the color of the color palette 1 index 7 to the transparent color.</p>
6	CP1I6	0	R/W	Available	<p>Color Palette 1 Index 6</p> <p>This bit is used to specify the color palette 1 transparent color.</p> <p>0: Does not set the color of the color palette 1 index 6 to the transparent color.</p> <p>1: Sets the color of the color palette 1 index 6 to the transparent color.</p>

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
5	CP1I5	0	R/W	Available	<p>Color Palette 1 Index 5</p> <p>This bit is used to specify the color palette 1 transparent color.</p> <p>0: Does not set the color of the color palette 1 index 5 to the transparent color.</p> <p>1: Sets the color of the color palette 1 index 5 to the transparent color.</p>
4	CP1I4	0	R/W	Available	<p>Color Palette 1 Index 4</p> <p>This bit is used to specify the color palette 1 transparent color.</p> <p>0: Does not set the color of the color palette 1 index 4 to the transparent color.</p> <p>1: Sets the color of the color palette 1 index 4 to the transparent color.</p>
3	CP1I3	0	R/W	Available	<p>Color Palette 1 Index 3</p> <p>This bit is used to specify the color palette 1 transparent color.</p> <p>0: Does not set the color of the color palette 1 index 3 to the transparent color.</p> <p>1: Sets the color of the color palette 1 index 3 to the transparent color.</p>
2	CP1I2	0	R/W	Available	<p>Color Palette 1 Index 2</p> <p>This bit is used to specify the color palette 1 transparent color.</p> <p>0: Does not set the color of the color palette 1 index 2 to the transparent color.</p> <p>1: Sets the color of the color palette 1 index 2 to the transparent color.</p>
1	CP1I1	0	R/W	Available	<p>Color Palette 1 Index F</p> <p>This bit is used to specify the color palette 1 transparent color.</p> <p>0: Does not set the color of the color palette 1 index 1 to the transparent color.</p> <p>1: Sets the color of the color palette 1 index 1 to the transparent color.</p>
0	CP1I0	0	R/W	Available	<p>Color Palette 1 Index 0</p> <p>This bit is used to specify the color palette 1 transparent color.</p> <p>0: Does not set the color of the color palette 1 index 0 to the transparent color.</p> <p>1: Sets the color of the color palette 1 index 0 to the transparent color.</p>

**21.3.3.2 Color Palette 2 Transparent Color Register m (CP2TRm, m = 0 and 2)**

Address: DU0: H'FEB0 0084, DU2: H'FEB4 0084

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CP2IF	CP2IE	CP2ID	CP2IC	CP2IB	CP2IA	CP2I9	CP2I8	CP2I7	CP2I6	CP2I5	CP2I4	CP2I3	CP2I2	CP2I1	CP2I0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 16	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
15	CP2IF	0	R/W	Available	Color Palette 2 Index F This bit is used to specify the color palette 2 transparent color. 0: Does not set the color of the color palette 2 index F to the transparent color. 1: Sets the color of the color palette 2 index F to the transparent color.
14	CP2IE	0	R/W	Available	Color Palette 2 Index E This bit is used to specify the color palette 2 transparent color. 0: Does not set the color of the color palette 2 index E to the transparent color. 1: Sets the color of the color palette 2 index E to the transparent color.
13	CP2ID	0	R/W	Available	Color Palette 2 Index D This bit is used to specify the color palette 2 transparent color. 0: Does not set the color of the color palette 2 index D to the transparent color. 1: Sets the color of the color palette 2 index D to the transparent color.
12	CP2IC	0	R/W	Available	Color Palette 2 Index C This bit is used to specify the color palette 2 transparent color. 0: Does not set the color of the color palette 2 index C to the transparent color. 1: Sets the color of the color palette 2 index C to the transparent color.
11	CP2IB	0	R/W	Available	Color Palette 2 Index B This bit is used to specify the color palette 2 transparent color. 0: Does not set the color of the color palette 2 index B to the transparent color. 1: Sets the color of the color palette 2 index B to the transparent color.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
10	CP21A	0	R/W	Available	Color Palette 2 Index A This bit is used to specify the color palette 2 transparent color. 0: Does not set the color of the color palette 2 index A to the transparent color. 1: Sets the color of the color palette 2 index A to the transparent color.
9	CP219	0	R/W	Available	Color Palette 2 Index 9 This bit is used to specify the color palette 2 transparent color. 0: Does not set the color of the color palette 2 index 9 to the transparent color. 1: Sets the color of the color palette 2 index 9 to the transparent color.
8	CP218	0	R/W	Available	Color Palette 2 Index 8 This bit is used to specify the color palette 2 transparent color. 0: Does not set the color of the color palette 2 index 8 to the transparent color. 1: Sets the color of the color palette 2 index 8 to the transparent color.
7	CP217	0	R/W	Available	Color Palette 2 Index 7 This bit is used to specify the color palette 2 transparent color. 0: Does not set the color of the color palette 2 index 7 to the transparent color. 1: Sets the color of the color palette 2 index 7 to the transparent color.
6	CP216	0	R/W	Available	Color Palette 2 Index 6 This bit is used to specify the color palette 2 transparent color. 0: Does not set the color of the color palette 2 index 6 to the transparent color. 1: Sets the color of the color palette 2 index 6 to the transparent color.
5	CP215	0	R/W	Available	Color Palette 2 Index 5 This bit is used to specify the color palette 2 transparent color. 0: Does not set the color of the color palette 2 index 5 to the transparent color. 1: Sets the color of the color palette 2 index 5 to the transparent color.
4	CP214	0	R/W	Available	Color Palette 2 Index 4 This bit is used to specify the color palette 2 transparent color. 0: Does not set the color of the color palette 2 index 4 to the transparent color. 1: Sets the color of the color palette 2 index 4 to the transparent color.
3	CP213	0	R/W	Available	Color Palette 2 Index 3 This bit is used to specify the color palette 2 transparent color. 0: Does not set the color of the color palette 2 index 3 to the transparent color. 1: Sets the color of the color palette 2 index 3 to the transparent color.



Bit	Bit Name	Initial Value	R/W	Internal Update	Description
2	CP2I2	0	R/W	Available	<p>Color Palette 2 Index 2</p> <p>This bit is used to specify the color palette 2 transparent color.</p> <p>0: Does not set the color of the color palette 2 index 2 to the transparent color.</p> <p>1: Sets the color of the color palette 2 index 2 to the transparent color.</p>
1	CP2I1	0	R/W	Available	<p>Color Palette 2 Index 1</p> <p>This bit is used to specify the color palette 2 transparent color.</p> <p>0: Does not set the color of the color palette 2 index 1 to the transparent color.</p> <p>1: Sets the color of the color palette 2 index 1 to the transparent color.</p>
0	CP2I0	0	R/W	Available	<p>Color Palette 2 Index 0</p> <p>This bit is used to specify the color palette 2 transparent color.</p> <p>0: Does not set the color of the color palette 2 index 0 to the transparent color.</p> <p>1: Sets the color of the color palette 2 index 0 to the transparent color.</p>

### 21.3.3.3 Color Palette 3 Transparent Color Register m (CP3TRm, m = 0 and 2)

Address: DU0: H'FEB0 0088, DU2: H'FEB4 0088

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CP3IF	CP3IE	CP3ID	CP3IC	CP3IB	CP3IA	CP3I9	CP3I8	CP3I7	CP3I6	CP3I5	CP3I4	CP3I3	CP3I2	CP3I1	CP3I0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 16	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
15	CP3IF	0	R/W	Available	Color Palette 3 Index F This bit is used to specify the color palette 3 transparent color. 0: Does not set the color of the color palette 3 index F to the transparent color. 1: Sets the color of the color palette 3 index F to the transparent color.
14	CP3IE	0	R/W	Available	Color Palette 3 Index E This bit is used to specify the color palette 3 transparent color. 0: Does not set the color of the color palette 3 index E to the transparent color. 1: Sets the color of the color palette 3 index E to the transparent color.
13	CP3ID	0	R/W	Available	Color Palette 3 Index D This bit is used to specify the color palette 3 transparent color. 0: Does not set the color of the color palette 3 index D to the transparent color. 1: Sets the color of the color palette 3 index D to the transparent color.
12	CP3IC	0	R/W	Available	Color Palette 3 Index C This bit is used to specify the color palette 3 transparent color. 0: Does not set the color of the color palette 3 index C to the transparent color. 1: Sets the color of the color palette 3 index C to the transparent color.
11	CP3IB	0	R/W	Available	Color Palette 3 Index B This bit is used to specify the color palette 3 transparent color. 0: Does not set the color of the color palette 3 index B to the transparent color. 1: Sets the color of the color palette 3 index B to the transparent color.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
10	CP3IA	0	R/W	Available	Color Palette 3 Index A This bit is used to specify the color palette 3 transparent color. 0: Does not set the color of the color palette 3 index A to the transparent color. 1: Sets the color of the color palette 3 index A to the transparent color.
9	CP3I9	0	R/W	Available	Color Palette 3 Index 9 This bit is used to specify the color palette 3 transparent color. 0: Does not set the color of the color palette 3 index 9 to the transparent color. 1: Sets the color of the color palette 3 index 9 to the transparent color.
8	CP3I8	0	R/W	Available	Color Palette 3 Index 8 This bit is used to specify the color palette 3 transparent color. 0: Does not set the color of the color palette 3 index 8 to the transparent color. 1: Sets the color of the color palette 3 index 8 to the transparent color.
7	CP3I7	0	R/W	Available	Color Palette 3 Index 7 This bit is used to specify the color palette 3 transparent color. 0: Does not set the color of the color palette 3 index 7 to the transparent color. 1: Sets the color of the color palette 3 index 7 to the transparent color.
6	CP3I6	0	R/W	Available	Color Palette 3 Index 6 This bit is used to specify the color palette 3 transparent color. 0: Does not set the color of the color palette 3 index 6 to the transparent color. 1: Sets the color of the color palette 3 index 6 to the transparent color.
5	CP3I5	0	R/W	Available	Color Palette 3 Index 5 This bit is used to specify the color palette 3 transparent color. 0: Does not set the color of the color palette 3 index 5 to the transparent color. 1: Sets the color of the color palette 3 index 5 to the transparent color.
4	CP3I4	0	R/W	Available	Color Palette 3 Index 4 This bit is used to specify the color palette 3 transparent color. 0: Does not set the color of the color palette 3 index 4 to the transparent color. 1: Sets the color of the color palette 3 index 4 to the transparent color.
3	CP3I3	0	R/W	Available	Color Palette 3 Index 3 This bit is used to specify the color palette 3 transparent color. 0: Does not set the color of the color palette 3 index 3 to the transparent color. 1: Sets the color of the color palette 3 index 3 to the transparent color.
2	CP3I2	0	R/W	Available	Color Palette 3 Index 2 This bit is used to specify the color palette 3 transparent color. 0: Does not set the color of the color palette 3 index 2 to the transparent color. 1: Sets the color of the color palette 3 index 2 to the transparent color.

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<b>Bit</b>	<b>Bit Name</b>	<b>Initial Value</b>	<b>R/W</b>	<b>Internal Update</b>	<b>Description</b>
1	CP3I1	0	R/W	Available	Color Palette 3 Index 1 This bit is used to specify the color palette 3 transparent color. 0: Does not set the color of the color palette 3 index 1 to the transparent color. 1: Sets the color of the color palette 3 index 1 to the transparent color.
0	CP3I0	0	R/W	Available	Color Palette 3 Index 0 This bit is used to specify the color palette 3 transparent color. 0: Does not set the color of the color palette 3 index 0 to the transparent color. 1: Sets the color of the color palette 3 index 0 to the transparent color.

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### 21.3.3.4 Color Palette 4 Transparent Color Register m (CP4TRm, m = 0 and 2)

Address: DU0: H'FEB0 008C, DU2: H'FEB4 008C

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CP4IF	CP4IE	CP4ID	CP4IC	CP4IB	CP4IA	CP4I9	CP4I8	CP4I7	CP4I6	CP4I5	CP4I4	CP4I3	CP4I2	CP4I1	CP4I0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 16	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
15	CP4IF	0	R/W	Available	Color Palette 4 Index F This bit is used to specify the color palette 4 transparent color. 0: Does not set the color of the color palette 4 index F to the transparent color. 1: Sets the color of the color palette 4 index F to the transparent color.
14	CP4IE	0	R/W	Available	Color Palette 4 Index E This bit is used to specify the color palette 4 transparent color. 0: Does not set the color of the color palette 4 index E to the transparent color. 1: Sets the color of the color palette 4 index E to the transparent color.
13	CP4ID	0	R/W	Available	Color Palette 4 Index D This bit is used to specify the color palette 4 transparent color. 0: Does not set the color of the color palette 4 index D to the transparent color. 1: Sets the color of the color palette 4 index D to the transparent color.
12	CP4IC	0	R/W	Available	Color Palette 4 Index C This bit is used to specify the color palette 4 transparent color. 0: Does not set the color of the color palette 4 index C to the transparent color. 1: Sets the color of the color palette 4 index C to the transparent color.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
11	CP4IB	0	R/W	Available	<p>Color Palette 4 Index B</p> <p>This bit is used to specify the color palette 4 transparent color.</p> <p>0: Does not set the color of the color palette 4 index B to the transparent color.</p> <p>1: Sets the color of the color palette 4 index B to the transparent color.</p>
10	CP4IA	0	R/W	Available	<p>Color Palette 4 Index A</p> <p>This bit is used to specify the color palette 4 transparent color.</p> <p>0: Does not set the color of the color palette 4 index A to the transparent color.</p> <p>1: Sets the color of the color palette 4 index A to the transparent color.</p>
9	CP4I9	0	R/W	Available	<p>Color Palette 4 Index 9</p> <p>This bit is used to specify the color palette 4 transparent color.</p> <p>0: Does not set the color of the color palette 4 index 9 to the transparent color.</p> <p>1: Sets the color of the color palette 4 index 9 to the transparent color.</p>
8	CP4I8	0	R/W	Available	<p>Color Palette 4 Index 8</p> <p>This bit is used to specify the color palette 4 transparent color.</p> <p>0: Does not set the color of the color palette 4 index 8 to the transparent color.</p> <p>1: Sets the color of the color palette 4 index 8 to the transparent color.</p>
7	CP4I7	0	R/W	Available	<p>Color Palette 4 Index 7</p> <p>This bit is used to specify the color palette 4 transparent color.</p> <p>0: Does not set the color of the color palette 4 index 7 to the transparent color.</p> <p>1: Sets the color of the color palette 4 index 7 to the transparent color.</p>
6	CP4I6	0	R/W	Available	<p>Color Palette 4 Index 6</p> <p>This bit is used to specify the color palette 4 transparent color.</p> <p>0: Does not set the color of the color palette 4 index 6 to the transparent color.</p> <p>1: Sets the color of the color palette 4 index 6 to the transparent color.</p>
5	CP4I5	0	R/W	Available	<p>Color Palette 4 Index 5</p> <p>This bit is used to specify the color palette 4 transparent color.</p> <p>0: Does not set the color of the color palette 4 index 5 to the transparent color.</p> <p>1: Sets the color of the color palette 4 index 5 to the transparent color.</p>

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
4	CP4I4	0	R/W	Available	<p>Color Palette 4 Index 4</p> <p>This bit is used to specify the color palette 4 transparent color.</p> <p>0: Does not set the color of the color palette 4 index 4 to the transparent color.</p> <p>1: Sets the color of the color palette 4 index 4 to the transparent color.</p>
3	CP4I3	0	R/W	Available	<p>Color Palette 4 Index 3</p> <p>This bit is used to specify the color palette 4 transparent color.</p> <p>0: Does not set the color of the color palette 4 index 3 to the transparent color.</p> <p>1: Sets the color of the color palette 4 index 3 to the transparent color.</p>
2	CP4I2	0	R/W	Available	<p>Color Palette 4 Index 2</p> <p>This bit is used to specify the color palette 4 transparent color.</p> <p>0: Does not set the color of the color palette 4 index 2 to the transparent color.</p> <p>1: Sets the color of the color palette 4 index 2 to the transparent color.</p>
1	CP4I1	0	R/W	Available	<p>Color Palette 4 Index 1</p> <p>This bit is used to specify the color palette 4 transparent color.</p> <p>0: Does not set the color of the color palette 4 index 1 to the transparent color.</p> <p>1: Sets the color of the color palette 4 index 1 to the transparent color.</p>
0	CP4I0	0	R/W	Available	<p>Color Palette 4 Index 0</p> <p>This bit is used to specify the color palette 4 transparent color.</p> <p>0: Does not set the color of the color palette 4 index 0 to the transparent color.</p> <p>1: Sets the color of the color palette 4 index 0 to the transparent color.</p>

### 21.3.3.5 Display Off Mode Output Register n (DOORn)

Address: DU0: H'FEB0 0090, DU1: H'FEB3 0090, DU2: H'FEB4 0090

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	DOR						—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DOG						—	—	DOB						—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R

The three registers are for the respective channels and have the same functions.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 24	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
23 to 18	DOR	—	R/W	Available	Display Off Mode Output Red These bits are used to set the red display data to be output when the display is off (DRES and DEN bits in the display unit system control register m (DSYSRm *) are B'00). The set value is retained at a reset.
17, 16	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
15 to 10	DOG	—	R/W	Available	Display Off Mode Output Green These bits are used to set the green display data to be output when the display is off (DRES and DEN bits in the display unit system control register m (DSYSRm *) are B'00). The set value is retained at a reset.
9, 8	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
7 to 2	DOB	—	R/W	Available	Display Off Mode Output Blue These bits are used to set the blue display data to be output when the display is off (DRES and DEN bits in the display unit system control register m (DSYSRm *) are B'00). The set value is retained at a reset.
1, 0	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

Note: m = 0 and 2 for RZ/G1H, m = 0 for RZ/G1M/N/E.



### 21.3.3.6 Color Detection Register n (CDERn)

Address: DU0: H'FEB0 0094, DU1: H'FEB3 0094, DU2: H'FEB4 0094

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	CDR						—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CDG						—	—	CDB						—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R

The three registers are for the respective channels and have the same functions.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 24	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
23 to 18	CDR	—	R/W	Available	Color Detection Red These bits are used to set the red data for color detection. The set value is retained at a reset.
17, 16	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
15 to 10	CDG	—	R/W	Available	Color Detection Green These bits are used to set the green data for color detection. The set value is retained at a reset.
9, 8	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
7 to 2	CDB	—	R/W	Available	Color Detection Blue These bits are used to set the blue data for color detection. The set value is retained at a reset.
1, 0	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

Note: When output data matches the setting value of this register, the high level is output from the CDE pin. For details about the output color data format, see section 21.4.6, Data Formats for Output and Display Capture.

### 21.3.3.7 Background Plane Output Register n (BPORn)

Address: DU0: H'FEB0 0098, DU1: H'FEB3 0098, DU2: H'FEB4 0098

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	BPOR						—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BPOG						—	—	BPOB						—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R

The three registers are for the respective channels and have the same functions.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 24	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
23 to 18	BPOR	—	R/W	Available	Background Plane Output Red These bits are used to set the red color to be displayed if no plane to be displayed exists due to a display size, transparent color, and so on. The set value is retained at a reset.
17, 16	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
15 to 10	BPOG	—	R/W	Available	Background Plane Output Green These bits are used to set the green color to be displayed if no plane to be displayed exists due to a display size, transparent color, and so on. The set value is retained at a reset.
9, 8	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
7 to 2	BPOB	—	R/W	Available	Background Plane Output Blue These bits are used to set the blue color to be displayed if no plane to be displayed exists due to a display size, transparent color, and so on. The set value is retained at a reset.
1, 0	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

### 21.3.3.8 Raster Interrupt Offset Register n (RINTOFSRn)

Address: DU0: H'FEB0 009C, DU1: H'FEB3 009C, DU2: H'FEB4 009C

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	—	—	—	—	—	RINTOFS											—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
R/W:	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

The three registers are for the respective channels and have the same functions.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 11	—	—	R	—	Reserved
10 to 0	RINTOFS	—	R/W	Available	<p>Raster Interrupt Offset</p> <p>To enable bit 10, set the DEFE5 bit in the display unit extensional function control 5 register m (DEF5Rm) to 1. In the initial state, bit 10 cannot be written to.</p> <p>These bits are used to set the raster offset value (number of Hs) that is based on the number of rasters set with the vertical display start register n (VD5SRn).</p> <p>If the offset value is assumed to be n, bit 9 in the display unit status register n (D5SSRn) is set to 1 at the HSYNC falling edge after the horizontal display period of (VDS + n-th raster).</p> <p>The set value is retained at a reset.</p>

Note: n = 0 to 2 for RZ/G1H, n = 0 and 1 for RZ/G1M/N/E.

### 21.3.4 Display Plane Registers (Alpha Plane Registers)

In descriptions of registers that are common to planes 1 to 8, the planes are generically referred to as plane n. The meanings of characters m, n, and # are given below.

m: Indicates the display unit channel number (0 or 2). (RZ/G1H only)

n: 1 to 8

#: Replaces n (in hexadecimal) in addresses. For example, address H'FEB00#00 for the plane 3 mode register corresponds to H'FEB00300.

Descriptions of the registers for the alpha-ratio planes are also given in this section, because a given register for the alpha-ratio planes has almost the same functionality as the corresponding register for the display planes.

#### Register names:

The names of corresponding registers for the alpha-ratio planes start with the string "Alpha".

#### Abbreviation:

Abbreviations of the names of corresponding registers for the alpha-ratio planes start with "A".

For alpha plane registers, n is given as follows;

n: 1, 2

#### Address:

The addresses of registers for the alpha-ratio planes are given to the right of the address information for the corresponding display-plane registers (# = 1, 2).

The plane n memory width register (PnMWR) for the alpha-ratio planes, for example, is the alpha plane n memory width register (APnMWR).

The alpha plane n mode register (APnMR) is described separately because its functionality differs from that of a plane n mode register (PnMR).

### 21.3.4.1 Plane n Mode Register m (PnMRm, m = 0 and 2)

Note: Suffix "m" as register name and DU2 are only for RZ/G1H.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address: DU0: H'FEB00#00, DU2: H'FEB40#00 (for alpha-ratio planes; refer to section 21.3.4.24, Alpha Plane n Mode Register m (APnMRm, m = 0 and 2))

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	PnVISL		—	—	—	—	—	PnYCDF	—	—	PnTC	PnWAE
Initial value:	—	—	—	—	0	0	—	—	—	—	—	0	—	—	0	0
R/W:	R	R	R	R	R/W	R/W	R	R	R	R	R	R/W	R	R	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	PnSPIIM			—	PnCPSL			PnDC	—	PnBM		—	—	PnDDF	
Initial value:	—	0	0	0	—	0	0	0	0	—	0	0	—	—	0	0
R/W:	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R	R/W	R/W	R	R	R/W	R/W

Note: \* For reserved bit (bit name: —), initial value is undefined, writing is not available and writing value should be specified. For details of bit description, refer to following table.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 28	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
27, 26	PnVISL	00	R/W	Available	Plane n Video Input Select To enable these bits, set the DEFE bit in the display unit extensional function control register m/0 (DEFRm/DEFR0*) to 1. In the initial state, these bits cannot be set to 1. 00: Video input 0 (VIN0) is selected. 01: Video input 1 (VIN1) is selected. 10: Video input 2 (VIN2) is selected. [RZ/G1H/M/N] Setting prohibited [RZ/G1E] 11: Video input 3 (VIN3) is selected. [RZ/G1H] Setting prohibited [RZ/G1M/N/E] Note: * DEFR0 is for RZ/G1M/N/E
25 to 21	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
20	PnYCDF	0	R/W	Available	Plane n YC Data Format 0: Sets the alignment of YC data to UYVY format. 1: Sets the alignment of YC data to YUYV format.
19, 18	—	—	R	—	Reserved The setting is invalid when an 8-bit/pixel display has not been selected.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
17	PnTC	0	R/W	Available	<p>Plane n Transparent Color</p> <p>0: When an 8-bit/pixel display has been selected, the transparent color is that indicated by the value of PnTC1Rm</p> <p>1: When an 8-bit/pixel display has been selected, the transparent color is that indicated by the value of CPT1Rm to CPT4Rm</p> <p>The setting is invalid when an 8-bit/pixel display has not been selected. For details, refer to section 21.4.9 (2), Transparent Colors.</p>
16	PnWAE	0	R/W	Available	<p>Plane n Wrap-Around Enable</p> <p>0: Wrapping-around for plane n is disabled.</p> <p>1: Wrapping-around for plane n is enabled.</p>
15	—	—	R	—	<p>Reserved</p> <p>The read value is undefined. The write value should always be 0.</p>
14 to 12	PnSPIM	000	R/W	Available	<p>Plane n Super Impose Mode</p> <p>000: Transparent color processing is performed for plane n. When plane n is in the transparent color, the lower plane is displayed.</p> <p>001: <math>\alpha</math> blending of plane n and the lower plane is performed. When plane n is the transparent color, <math>\alpha</math> blending is not performed, and the lower plane is displayed.</p> <p>010: An EOR operation is performed on plane n and the lower plane. When plane n is the transparent color the EOR operation is not performed, and the lower plane is displayed.</p> <p>011: Setting prohibited</p> <p>100: Transparent color processing is not performed for plane n. Plane n is displayed.</p> <p>101: <math>\alpha</math> blending of plane n and the lower plane is performed. The transparent color specification for plane n is ignored, and <math>\alpha</math> blending is performed between all the pixels of plane n and the lower plane.</p> <p>110: An EOR operation is performed on plane n and the lower plane. The transparent color specification for plane n is ignored, and EOR operation is performed on all the pixels of plane n and the lower plane.</p> <p>111: Setting prohibited</p> <p>Transparent color processing for YC data is not possible.</p> <p>Transparent color processing is not possible when the PnLRGB1 bit or PnLRGB0 bit in the plane n display data control register m (PnDDCRm) specifies 32-bit/pixel data. Transparent color processing is possible when 32-bit/pixel data is specified by plane n display data control 4 register m (PnDDC4Rm).</p>
11	—	—	R	—	<p>Reserved</p> <p>The read value is undefined. The write value should always be 0.</p>

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
10 to 8	PnCPSL	000	R/W	Available	<p>Plane n Color Palette Select</p> <p>These bits indicate whether the color palette is to be used when the value of the PnDDF bits is B'00 (i.e. the plane n display data format is 8-bit/pixel).</p> <p>000: Use color palette 1  001: Use color palette 2  010: Use color palette 3  011: Use color palette 4  100: Setting prohibited  101: Setting prohibited  110: Setting prohibited  111: Setting prohibited</p>
7	PnDC	0	R/W	Available	<p>Plane n Display Area Change</p> <p>0: In manual display change mode, switching of the frame buffer is not performed.  1: In manual display change mode, switching of the frame buffer is performed.  When the PnDC bit is 0, bit setting is possible.  Switching is performed in frame units.  After frame buffer switching (after vertical blanking detection), this bit is cleared to 0.</p>
6	—	—	R	—	<p>Reserved</p> <p>The read value is undefined. The write value should always be 0.</p>
5, 4	PnBM	00	R/W	Available	<p>Plane n Buffer Mode</p> <p>00: Manual display change mode  01: Auto rendering mode  10: Auto display change mode (blinking mode)  11: Video capture mode</p> <p>In manual display change mode, auto rendering mode, or auto display change mode (blinking mode), double-buffering control is performed using addresses 0 and 1, respectively indicated by the PnDSA0 and PnDSA1 bits in PnDSA0Rm and PnDSA1Rm. In video capture mode, triple-buffering control is performed using addresses 0 to 2 indicated by bits 31 to 26 of the display unit status register m/0 (DSSRm/DSSR0*) or the display unit video capture status register m (DVCSRm).</p> <p>Note: * DSSR0 is for RZ/G1M/N/E</p>
3, 2	—	—	R	—	<p>Reserved</p> <p>The read value is undefined. The write value should always be 0.</p>
1, 0	PnDDF	00	R/W	Available	<p>Plane n Display Data Format</p> <p>00: 8-bit/pixel  01: 16-bit/pixel  10: ARGB (ARGB1555)  11: YC (YUV422 is converted to RGB888). For RZ/G1M, N and E, when bits 9 and 8 in the Display Unit Extensional Function Control Register n (DEFRn) are set to B'10 or B'11, conversion to RGB888 is not performed. (n = 1)</p> <p>In the case of 32-bit/pixel data, set these bits to B'01.</p>

**21.3.4.2 Plane n Memory Width Register m (PnMWRm, m = 0 and 2)**

Note: Suffix "m" as register name and DU2 are only for RZ/G1H.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address: DU0: H'FEB00#04, DU2: H'FEB40#04 (Alpha ratio plane address: DU0: H'FEB0A#04, DU2: H'FEB4A#04)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value:	—	—	—	PnMWX								—	—	—	—	
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 13	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
12 to 4	PnMWX	—	R/W	Available	Plane n Memory Width X The plane n memory width should be set in the range 16 pixels to 4096 pixels, in 16-pixel units. If the image data are in 32-bit/pixel format, and the scan mode is set as the interlaced sync & video mode, specify a value corresponding to double the desired size in the PnMWX bits. The value is retained during a reset.
3 to 0	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.



### 21.3.4.3 Plane n Blending Ratio Register m (PnALPHARm, m = 0 and 2)

Note: Suffix "m" as register name and DU2 are only for RZ/G1H.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address: DU0: H'FEB00#08, DU2: H'FEB40#08 (unused for the alpha-ratio planes)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 14	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
13, 12	PnABIT	—	R/W	Available	Plane n A Bit Function Select This facility is not available for 32-bit/pixel data. In the initial state, these bits are fixed to 0. To enable these bits, set the DEFE2G bit in DEF2Rm to 1. 00: In ARGB mode (i.e. when the value of the PnDDF bits in PnMRm is B'10), $\alpha$ blending is performed when the value of A is 1. 01: In ARGB mode (i.e. when the value of the PnDDF bits in PnMRm is B'10), $\alpha$ blending is performed when the value of A is 0. 1-: In ARGB mode (i.e. when the value of the PnDDF bits in PnMRm is B'10), $\alpha$ blending is performed regardless of the value of A. The value is retained during a reset.
11	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
10 to 8	PnBRSL	—	R/W	Available	<p>Plane n Blending Ratio Select</p> <p>This bit is valid when the value of the PnSPIM bits in PnMRm allows <math>\alpha</math> blending.</p> <p>In the initial state, bit 10 is fixed to 0. To enable bit 10, set the DEFE bit in DEFRm/DEFRO* to 1.</p> <p>-00: The value of bits 7 to 0 in this register is taken to be the alpha ratio.</p> <p>-01: Setting prohibited</p> <p>-10: Bits 31 to 24 of the color palette register specified by the PnCPSL bits in PnMRm are taken to be the alpha ratio.</p> <p>*: DEFRO is for RZ/G1M, N, E</p> <p>Note: This setting is only effective when the display data format specified by the PnDDF bits in PnMRm is 8-bit/pixel. For formats other than 8-bit/pixel, the value of bits 7 to 0 in this register is taken to be the alpha ratio.</p> <p>011: The display data for the plane specified by bits 2 to 0 in this register is taken to be the alpha ratio.</p> <p>Bits 2 to 0 = 000: Display data for plane 1 is the alpha ratio</p> <p>Bits 2 to 0 = 001: Display data for plane 2 is the alpha ratio</p> <p>Bits 2 to 0 = 010: Display data for plane 3 is the alpha ratio</p> <p>Bits 2 to 0 = 011: Display data for plane 4 is the alpha ratio</p> <p>Bits 2 to 0 = 100: Display data for plane 5 is the alpha ratio</p> <p>Bits 2 to 0 = 101: Display data for plane 6 is the alpha ratio</p> <p>Bits 2 to 0 = 110: Display data for plane 7 is the alpha ratio</p> <p>Bits 2 to 0 = 111: Display data for plane 8 is the alpha ratio</p> <p>Notes: 1. When the register's own plane is specified, the value of bits 7 to 0 in this register is taken to be the alpha ratio.</p> <p>2. The specified plane should satisfy the following conditions. If the conditions are not satisfied, the alpha ratio is undefined.</p> <ul style="list-style-type: none"> <li>- The display should be turned on by using DPPRm.</li> <li>- The display data format should be set to 8-bit/pixel.</li> <li>- The display size should be greater than or equal to the size of the plane for this register.</li> <li>- Ensure that display positions (X and Y) are the same as those in the plane for this register.</li> </ul>

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
10 to 8	PnBRSL	—	R/W	Available	<p>111: The display data for the alpha-ratio plane specified by bits 2 to 0 in this register is taken to be the alpha ratio.</p> <p>Bits 2 to 0 = 000: Display data for <math>\alpha</math> plane 1 is the alpha ratio</p> <p>Bits 2 to 0 = 001: Display data for <math>\alpha</math> plane 2 is the alpha ratio</p> <p>Take the following steps before setting PnBRSL = 111.</p> <ol style="list-style-type: none"> <li>1. Set the desired value in a register listed in section 21.3.4, Display Plane Registers (Alpha Plane Registers)</li> <li>2. Set the AP1E or AP2E bit in DAPCRm to 1.</li> <li>3. Make the timing and dot clock settings in DPTSR and DAPTSR. The settings in DPTSR and DAPTSR should be the same.</li> </ol> <p>The value is retained during a reset.</p>
7 to 0	PnALPHA	—	R/W	Available	<p>Plane n Blending Ratio</p> <p>These bits indicate the alpha ratio (<math>\alpha</math>), which determines the blending ratio for plane n.</p> <p>This facility is not available for 32-bit/pixel data.</p> <p>Blending result <math>\approx</math> (plane n <math>\times</math> <math>\alpha/255</math>) + lower plane <math>\times</math> (1 - <math>\alpha/255</math>) (Approximation)</p> <p>Note: Blending result, <math>\alpha</math>, plane n, and lower plane in the above formula are all 8-bit data.</p> <p>The value is retained during a reset.</p>

**21.3.4.4 Plane n Display Size X Register m (PnDSXRm, m = 0 and 2)**

Note: Suffix "m" as register name and DU2 are only for RZ/G1H.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address: DU0: H'FEB00#10, DU2: H'FEB40#10 (Alpha ratio plane address: DU0: H'FEB0A#10, DU2: H'FEB4A#10)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	—	—	—	—	PnDSX												—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 12	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
11 to 0	PnDSX	—	R/W	Available	Plane n Display Size X To enable bit 11, set the DEFE5 bit in the display unit extensional function control 5 register m (DEF5Rm) to 1. In the initial state, bit 11 cannot be written to. The horizontal-direction display size of plane n should be set in dot clock units. Note: When YC has been selected by the PnDDF bits in PnMRm, this value should be set to an even number. The value is retained during a reset.

### 21.3.4.5 Plane n Display Size Y Register m (PnDSYm, m = 0 and 2)

Note: Suffix "m" as register name and DU2 are only for RZ/G1H.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address: DU0: H'FEB00#14, DU2: H'FEB40#14 (Alpha ratio plane address: DU0: H'FEB0A#14, DU2: H'FEB0A#14)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 11	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
10 to 0	PnDSY	—	R/W	Available	Plane n Display Size Y To enable bit 10, set the DEFE5 bit in the display unit extensional function control 5 register m (DEF5Rm) to 1. In the initial state, bit 10 cannot be written to. The vertical-direction display size of plane n should be set in raster line units. The value is retained during a reset.

### 21.3.4.6 Plane n Display Position X Register m (PnDPXRm, m = 0 and 2)

Note: Suffix "m" as register name and DU2 are only for RZ/G1H.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address: DU0: H'FEB00#18, DU2: H'FEB40#18 (Alpha ratio plane address: DU0: H'FEB0A#18, DU2: H'FEB4A#18)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 12	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
11 to 0	PnDPX	—	R/W	Available	Plane n Display Position X To enable bit 11, set the DEFE5 bit in the display unit extensional function control 5 register m (DEF5Rm) to 1. In the initial state, bit 11 cannot be written to. The horizontal start position on the display monitor of plane n should be set in dot clock units, taking as the origin the upper-left corner of the display monitor. Notes: 1. For RZ/G1M, N and E, when YC has been selected by the RGBYC0 bit in the Display Extensional Function Control 5 Register (DEF5R) during display output from DU0, this value should be set to an even number. when YC has been selected by the DODF1 bit in the display unit extensional function control register 1 (DEFR1) / DODF1 during display output from DU1, this value should be set to an even number. The value is retained during a reset.

**21.3.4.7 Plane n Display Position Y Register m (PnDPYRm, m = 0 and 2)**

Note: Suffix "m" as register name and DU2 are only for RZ/G1H.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address: DU0: H'FEB00#1C, DU2: H'FEB40#1C (Alpha ratio plane address: DU0: H'FEB0A#1C, DU2: H'FEB4A#1C)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	—	—	—	—	—	PnDPY											—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
R/W:	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 11	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description												
10 to 0	PnDPY	—	R/W	Available	<p>Plane n Display Position Y</p> <p>To enable bit 10, set the DEFE5 bit in the display unit extensional function control 5 register m (DEF5Rm) to 1. In the initial state, bit 10 cannot be written to.</p> <p>The vertical start position on the display monitor of plane n should be set in raster line units, taking as the origin the upper-left corner of the display monitor.</p> <p>For interlaced sync &amp; video display, the display starts at the position one bit shifted from the PnDPY bit setting value.</p> <table border="1"> <tr> <td>PnDPY</td> <td>Vertical start position</td> </tr> <tr> <td>0</td> <td>0</td> </tr> <tr> <td>1</td> <td>0</td> </tr> <tr> <td>2</td> <td>1</td> </tr> <tr> <td>3</td> <td>1</td> </tr> <tr> <td>4</td> <td>2</td> </tr> </table> <p>For non-interlaced and interlaced sync display, the display starts at the position specified by the PnDPY bit.</p> <ul style="list-style-type: none"> <li>When you set one or more values to this register at the time of interlace sync &amp; video, please add one half of the preset values of this register to the VDE bits of the vertical display end register n (VDERn) (n = 0 to 2 for RZ/G1H ;0 and 1 for RZ/G1M/N/E).</li> </ul> <p>Add further 1, when the number of preset values is odd -- when you have set up by two or more planes, please add the maximum.</p> <p>Adding to the value of VDERn can lead to the effects described against (1) and (2) below. Depending on the monitor, these may make display impossible. Use of this register when such cases arise in interlace sync &amp; video mode is prohibited.</p> <p>(1) Although the DISP signal was originally at the low level in the vertical blanking interval, the DISP signal will be at the high level until the next falling edges of the VSYNC and HSYNC signals.</p> <p>(2) Although all bits of the data for display were 0 in the vertical blanking interval, values become non-zero in the same interval as effect (1). This becomes the value of the DDR for the display data if settings of the PnDSY and PnDPY bit fields cause the display to jut out in the vertical direction and the value of the BPORn field if the display does not jut out (n is 0, 1, or 2 for the RZ/G1H and 0 or 1 for the RZ/G1M, RZ/G1N, and RZ/G1E).</p> <p>In the case of a non-interlace and an interlace sync, the necessity for addition is not.</p> <p>The value is retained during a reset.</p>	PnDPY	Vertical start position	0	0	1	0	2	1	3	1	4	2
PnDPY	Vertical start position																
0	0																
1	0																
2	1																
3	1																
4	2																

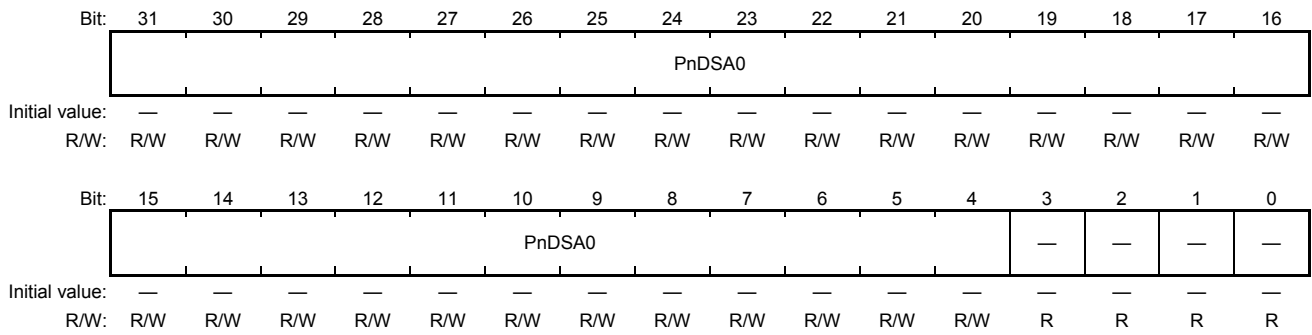


**21.3.4.8 Plane n Display Area Start Address 0 Register m (PnDSA0Rm, m = 0 and 2)**

Note: Suffix "m" as register name and DU2 are only for RZ/G1H.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address: DU0: H'FEB00#20, DU2: H'FEB40#20 (Alpha ratio plane address: DU0: H'FEB0A#20, DU2: H'FEB4A#20)



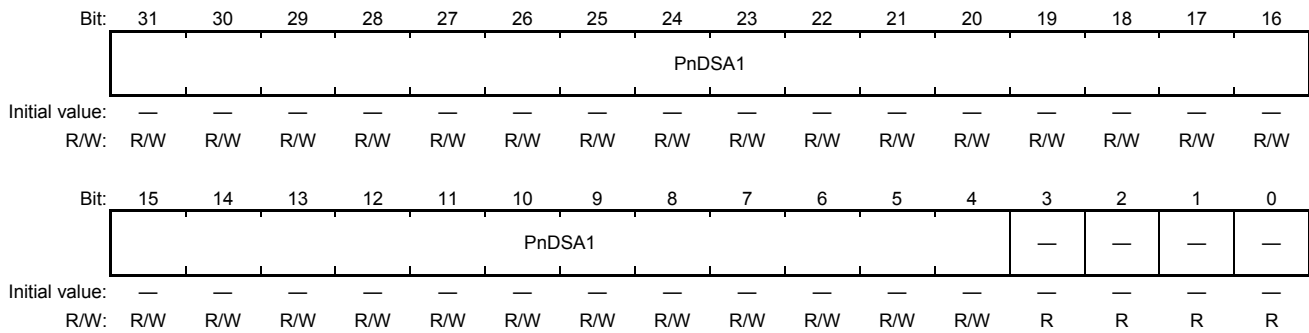
Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 4	PnDSA0	—	R/W	Available	<p>Plane n Display Area Start Address 0</p> <p>To enable bits 31 to 29, the DEFE bit in DEFRm/DEFR0* must be set to 1.</p> <p>In the initial state, these bits are not enabled.</p> <p>When the buffer mode for plane n is manual display, auto rendering, auto display change, or video capture, the area indicated by this register is used as frame buffer 0.</p> <p>The value is retained during a reset.</p> <p>Note: * DEFR0 is for RZ/G1M/N/E</p>
3 to 0	—	—	R	—	<p>Reserved</p> <p>The read value is undefined. The write value should always be 0.</p>

### 21.3.4.9 Plane n Display Area Start Address 1 Register m (PnDSA1Rm, m = 0 and 2)

Note: Suffix "m" as register name and DU2 are only for RZ/G1H.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address: DU0: H'FEB00#24, DU2: H'FEB40#24 (Alpha ratio plane address: DU0: H'FEB0A#24, DU2: H'FEB4A#24)



Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 4	PnDSA1	—	R/W	Available	<p>Plane n Display Area Start Address 1</p> <p>To enable bits 31 to 29, the DEFE bit in DEFRm/DEFR0* must be set to 1.</p> <p>In the initial state, these bits are not enabled.</p> <p>When the buffer mode for plane n is manual display, auto rendering, auto display change, or video capture, the area indicated by this register is used as frame buffer 1.</p> <p>The value is retained during a reset.</p> <p>Note: * DEFR0 is for RZ/G1M/N/E</p>
3 to 0	—	—	R	—	<p>Reserved</p> <p>The read value is undefined. The write value should always be 0.</p>

### 21.3.4.10 Plane n Display Area Start Address 2 Register m (PnDSA2Rm, m = 0 and 2)

Note: Suffix "m" as register name and DU2 are only for RZ/G1H.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address: DU0: H'FEB00#28, DU2: H'FEB40#28 (unused for the alpha-ratio planes)



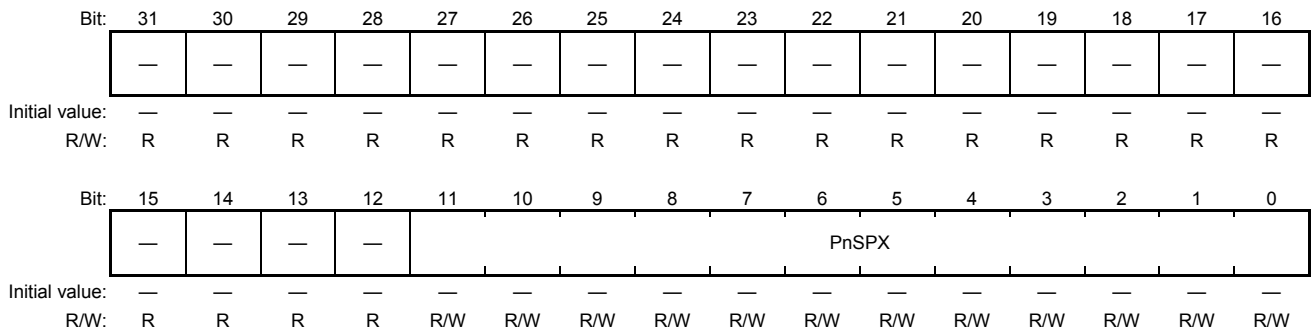
Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 4	PnDSA2	—	R/W	Available	<p>Plane n Display Area Start Address 2</p> <p>To enable bits 31 to 29, the DEFE bit in DEFm/DEF0* must be set to 1.</p> <p>In the initial state, these bits are not enabled.</p> <p>When the buffer mode for plane n is video capture, the area indicated by this register is used as frame buffer 2.</p> <p>The value is retained during a reset.</p> <p>Note: * DEF0 is for RZ/G1M/N/E</p>
3 to 0	—	—	R	—	<p>Reserved</p> <p>The read value is undefined. The write value should always be 0.</p>

**21.3.4.11 Plane n Start Position X Register m (PnSPXRm, m = 0 and 2)**

Note: Suffix "m" as register name and DU2 are only for RZ/G1H.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address: DU0: H'FEB00#30, DU2: H'FEB40#30 (Alpha ratio plane address: DU0: H'FEB0A#30, DU2: H'FEB4A#30)



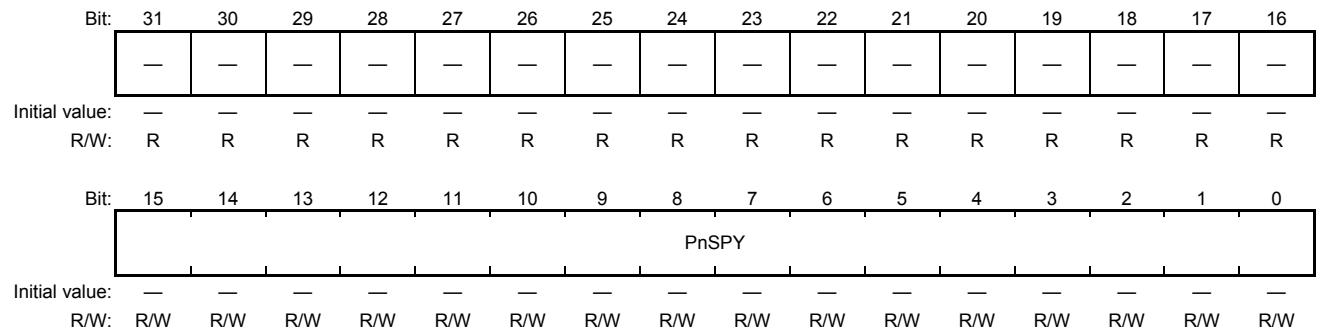
Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 12	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
11 to 0	PnSPX	—	R/W	Available	Plane n Start Position X Specify the distance in the X direction to the position where plane n starts in memory. Notes: 1. When YC has been selected by the PnDDF bits in PnMRm, the value should be even. 2. Setting of a value greater than twice the value of the PnMWX bits is prohibited. The value is retained during a reset.

**21.3.4.12 Plane n Start Position Y Register m (PnSPYm, m = 0 and 2)**

Note: Suffix "m" as register name and DU2 are only for RZ/G1H.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address: DU0: H'FEB00#34, DU2: H'FEB40#34 (Alpha ratio plane address: DU0: H'FEB0A#34, DU2: H'FEB4A#34)



Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 16	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
15 to 0	PnSPY	—	R/W	Available	Plane n Start Position Y Specify the distance in the Y direction to the position where plane n starts in memory. If an image data is in 32-bit/pixel data format, specify a value that is twice a desired value to the PnSPY bit. If memory length has been specified in PnMLRm, add a desired value for the start position to the PnMLY bit setting value. Note: Setting of a value greater than twice {the value of the PnWASPY bits + the value of the PnWAMWY bits} is prohibited. The value is retained during a reset.

**21.3.4.13 Plane n Wrap-Around Start Position Register m (PnWASPRm, m = 0 and 2)**

Note: Suffix "m" as register name and DU2 are only for RZ/G1H.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address: DU0: H'FEB00#38, DU2: H'FEB40#38 (Alpha ratio plane address: DU0: H'FEB0A#38, DU2: H'FEB4A#38)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	PnWASPY										—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 14	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
13 to 4	PnWASPY	—	R/W	Available	Plane n Wrap-Around Start Position Y The Y direction start position of one wrap-around area should be set with reference to the address specified in PnDSA0Rm, PnDSA1Rm and PnDSA2Rm. The position where wrapping-around is to start can be set in 16-pixel units (bits 3 to 0: Fixed to 0). If an image data is in 32-bit/pixel data format, specify a value that is twice a desired value to the PnWASPY bit. The value is retained during a reset.
3 to 0	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

**21.3.4.14 Plane n Wrap-Around Memory Width Register m (PnWAMWRm, m = 0 and 2)**

Note: Suffix "m" as register name and DU2 are only for RZ/G1H.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address: DU0: H'FEB00#3C, DU2: H'FEB40#3C (Alpha ratio plane address: DU0: H'FEB0A#3C, DU2: H'FEB4A#3C)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	PnWAMWY											
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

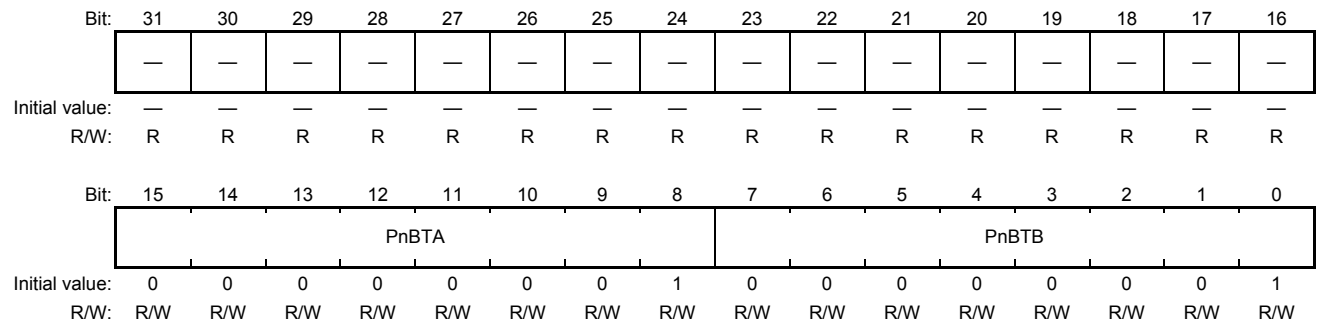
Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 12	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
11 to 0	PnWAMWY	—	R/W	Available	Plane n Wrap-Around Memory Width Y The memory width for wrap-around in the Y-direction should be set to a number corresponding to a value in the range from 240 to 4095 raster lines. If an image data is in 32-bit/pixel data format, specify a value that is twice a desired value to the PnWAMYY bit. The value is retained during a reset.

**21.3.4.15 Plane n Blinking Time Register m (PnBTRm, m = 0 and 2)**

Note: Suffix "m" as register name and DU2 are only for RZ/G1H.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address: DU0: H'FEB00#40, DU2: H'FEB40#40 (Alpha ratio plane address: DU0: H'FEB0A#40, DU2: H'FEB4A#40)



Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 16	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
15 to 8	PnBTA	0000 0001	R/W	Available	Plane n Blinking Time A
7 to 0	PnBTB	0000 0001	R/W	Available	Plane n Blinking Time B

Note: When the PnBM bits in PnMRm are set to select the auto display change mode (blinking mode), specify, as numbers of fields, the times over which plane n display area start address registers 0 and 1 (PnDSA0 and PnDSA1) are to be displayed. Blinking operation employs the settings in PnDSA0 and PnDSA1. Setting this register to 1 (the value should be other than 0) leads to switching between the buffers at the addresses indicated by the plane n display area start address registers 0 and 1 (PnDSA0 and PnDSA1) on each field unit.

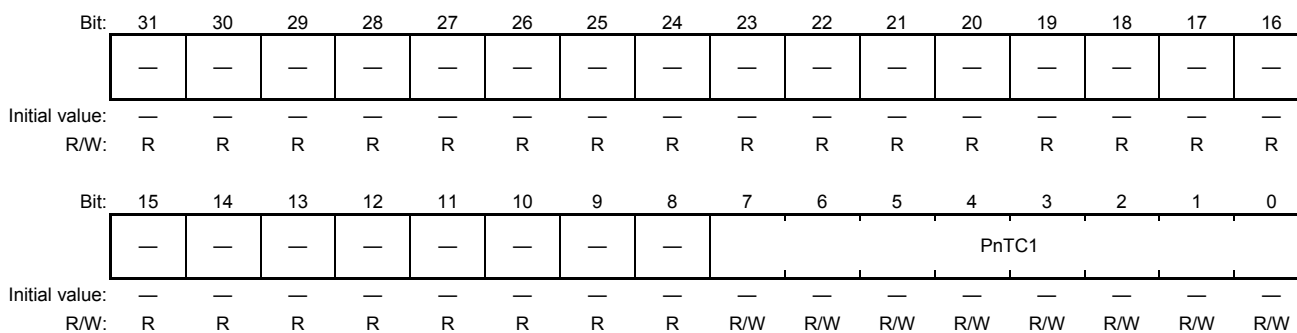


**21.3.4.16 Plane n Transparent Color 1 Register m (PnTC1Rm, m = 0 and 2)**

Note: Suffix "m" as register name and DU2 are only for RZ/G1H.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address: DU0: H'FEB00#44, DU2: H'FEB40#44 (unused for the alpha-ratio planes)



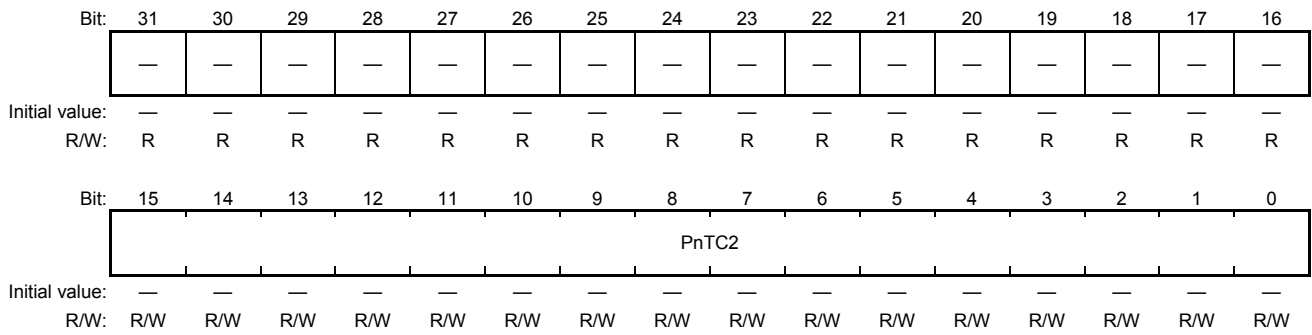
Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 8	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
7 to 0	PnTC1	—	R/W	Available	Plane n Transparent Color 1 for 8-bit/pixel This setting is for a transparent color for plane n in the 8-bit/pixel data format. To enable the transparent color setting in this register, the PnTC bit in PnMRm must be set to 0. The value is retained during a reset.

**21.3.4.17 Plane n Transparent Color 2 Register m (PnTC2Rm, m = 0 and 2)**

Note: Suffix "m" as register name and DU2 are only for RZ/G1H.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address: DU0: H'FEB00#48, DU2: H'FEB40#48 (unused for the alpha-ratio planes)



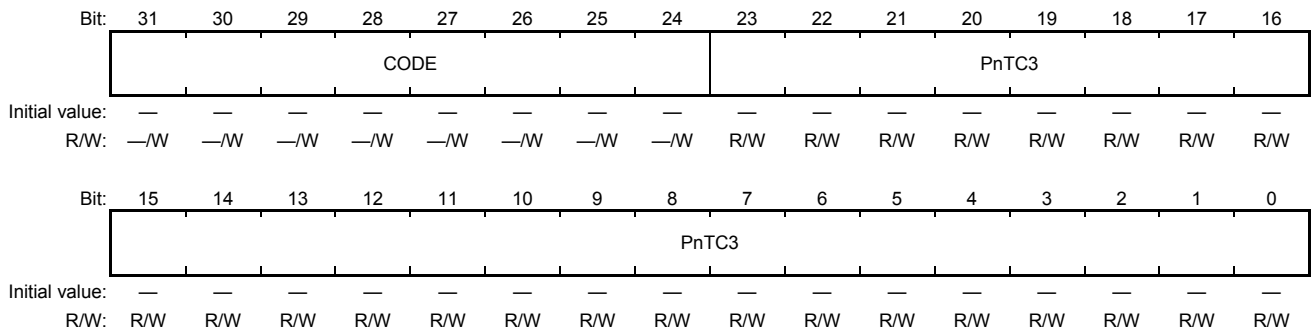
Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 16	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
15 to 0	PnTC2	—	R/W	Available	Plane n Transparent Color 2 for 16-bit/pixel This setting is for a transparent color for plane n in the 16-bit/pixel or ARGB data format. In the case of ARGB, comparison is with bits 14 to 0 of this register, i.e. bit 15 is ignored. The value is retained during a reset.

**21.3.4.18 Plane n Transparent Color 3 Register m (PnTC3Rm, m = 0 and 2)**

Note: Suffix "m" as register name and DU2 are only for RZ/G1H.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address: DU0: H'FEB00#4C, DU2: H'FEB40#4C (unused for the alpha-ratio planes)



Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 24	CODE	—	—/W	Not available	PnTC3Rm Enabling Code (register available code) For a value written to PnTC3Rm to be effective, the value must include H'66 in these bits.
23 to 0	PnTC3	—	R/W	Available	Plane n Transparent Color 3 These bits are used to specify the transparent color for the ARGB8888, RGB888, or RGB666 data format. See Table 21.24 for the bits to be compared.

**Table 21.24 Data Comparison by Plane n Transparent Color 3 Register m (PnTC3Rm)**

Bits in PnTC3R	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ARGB8888 or RGB888	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
RGB666	R5	R4	R3	R2	R1	R0	X	X	G5	G4	G3	G2	G1	G0	X	X	B5	B4	B3	B2	B1	B0	X	X

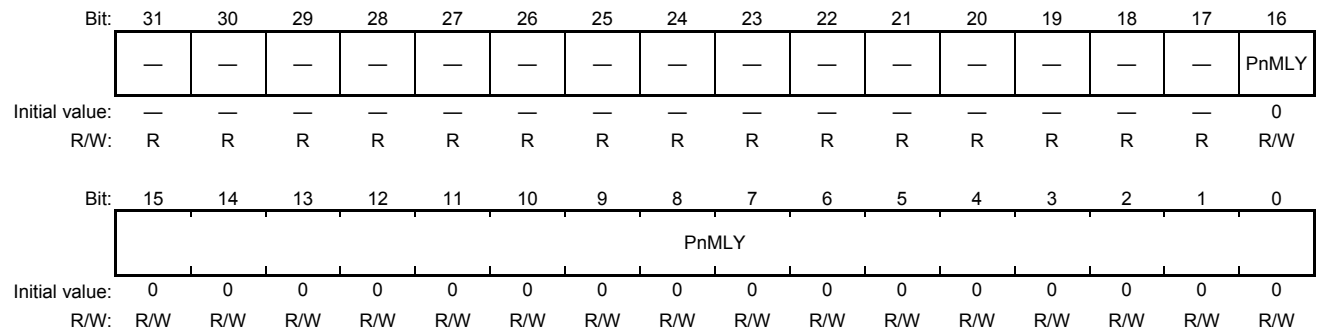
Note: "X" is not compared.

**21.3.4.19 Plane n Memory Length Register m (PnMLRm, m = 0 and 2)**

Note: Suffix "m" as register name and DU2 are only for RZ/G1H.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address: DU0: H'FEB00#50, DU2: H'FEB40#50 (Alpha ratio plane address: DU0: H'FEB 0A#50, DU2: H'FEB4A#50)



Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 17	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
16 to 0	PnMLY	H'00000	R/W	Available	Plane n Memory Length Y These bits indicate the length in memory (memory area in the Y-direction) of plane n. When the actual display is beyond this area, the data selected in BPORn will be displayed. When the value is 0 (initial value), the area is handled as an infinite area. Thus the data selected in BPORn will never be displayed. (n = 0 to 2 for RZ/G1H ;0 and 1 for RZ/G1M/N/E) If an image data is in 32-bit/pixel data format and a value other than 0 is specified in PnSPYRm, add a value that is half the PnSPYR bit setting value to this bit value.

### 21.3.4.20 Plane n SWAP Control Register m (PnSWAPRm, m = 0 and 2)

Note: Suffix "m" as register name and DU2 are only for RZ/G1H.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address: DU0: H'FEB00#80, DU2: H'FEB40#80 (Alpha ratio plane address: DU0: H'FEB0A#80, DU2: H'FEB4A#80)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CODE															
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	Pn DIGN	Pn SPQW	Pn SPLW	Pn SPWD	Pn SPBY
Initial value:	—	—	—	—	—	—	—	—	—	—	—	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 16	CODE	—	—/W	Not available	PnSWAPRm Enabling Code (register available code) For a value written to PnSWAPRm to be effective, the value must include H'7775 in these bits.
15 to 5	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
4	PnDIGN	0	R/W	Available	Plane n Display Data Format Invalid This bit is used in combination with bit 0 to control swapping of data in byte (8-bit) units. Also see the description of bit 0. The setting of this bit does not affect the values of bits 3 to 1.
3	PnSPQW	0	R/W	Available	Plane n Quadword Swap Enable 0: Data are not swapped. 1: Data are swapped in quadword (64-bit) units if bit 20 of DSYSRn is 0. (n = 0 to 2 for RZ/G1H ;0 and 1 for RZ/G1M/N/E)
2	PnSPLW	0	R/W	Available	Plane n Longword Swap Enable 0: Data are not swapped. 1: Data are swapped in longword (32-bit) units if bit 20 of DSYSRn is 0. (n = 0 to 2 for RZ/G1H ;0 and 1 for RZ/G1M/N/E)
1	PnSPWD	0	R/W	Available	Plane n Word Swap Enable 0: Data are not swapped. 1: Data are swapped in word (16-bit) units if bit 20 of DSYSRn is 0. (n = 0 to 2 for RZ/G1H ;0 and 1 for RZ/G1M/N/E)

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
0	PnSPBY	0	R/W	Available	Plane n Byte Swap Enable  This bit is used in combination with bit 4 to control swapping of data in byte (8-bit) units.  The following combinations of values are possible when bit 20 of DSYSRn is 0. (n = 0 to 2 for RZ/G1H ;0 and 1 for RZ/G1M/N/E) 00: Data are not swapped. 01: Data are not swapped. 10: Data are swapped in byte (8-bit) units if the value of the PnDDF bits in PnMRm is 00 or 11. In other cases, data are not swapped. 11: Data are swapped in byte (8-bit) units.

Note: The settings of bit 20 (DSEC) of the display unit system control register n (DSYSRn), the PnDDF bit of the plane n mode register m(PnMRm), and this register are listed with their results below (n = 0 to 2 for RZ/G1H ;0 and 1 for RZ/G1M/N/E).

All combinations of the values of the bits in PnSWAPRm, the DSEC bit in DSYSRn, and the PnDDF bits in PnMRm are shown below.

**Table 21.25 Summary of Endian Conversion**

DSEC	PnSPQW	PnSPLW	PnSPWD	PnSPBY	PnDIGN	PnDDF	Data Format	Swap Unit	
1	—	—	—	—	—	00	8-bit/pixel	128 bits in byte units	
						01	16-bit/pixel (RGB data)	128 bits in word units	
						10	ARGB	128 bits in word units	
						11	YC	128 bits in byte units	
0	0	0	0	0	—	—	—	No conversion	
						1	—	64 bits units	
	—	1	—	—	—	—	—	—	32 bits units
							—	1	—
	—	—	—	1	0	—	00	8-bit/pixel	8 bits units
							01	16-bit/pixel (RGB data)	No conversion
							10	ARGB	No conversion
							11	YC	8 bits units
	1	—	—	—	—	—	—	8 bits units	

### 21.3.4.21 Plane n Display Data Control Register m (PnDDCRm, m = 0 and 2)

Note: Suffix "m" as register name and DU2 are only for RZ/G1H.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address: DU0: H'FEB00#84, DU2: H'FEB40#84 (unused for the alpha-ratio planes)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CODE															
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	Pn LRGB1	Pn LRGB0	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	0	0	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R/W	R/W	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 16	CODE	—	—/W	Not available	PnDDCRm Enabling Code (register available code) For a value written to PnDDCRm to be effective, the value must include H'7775 in these bits.
15 to 12	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
11	PnLRGB1	0	R/W	Available	Plane n 32-bit/pixel display control 1 (Plane n Long (32 bits) RGB1) 0: Data are not handled as 32-bit/pixel (ARGB8888). 1: Data in the plane are used as the lower-order bits (G: 8 bits and B: 8 bits) of 32-bit/pixel data (ARGB8888). When a 32-bit/pixel display is specified with this bit, the following restrictions apply. When specifying a 32-bit/pixel display with the PnEDF bits in plane n display data control 4 register m (PnDDC4Rm), refer to the description of the PnEDF bits. Only ARGB8888 can be specified for 32-bit/pixel data. This bit must be set for plane n after setting of bit 10 for plane n-1 to 1. For example, if bit 10 of P1DDCRm is set to 1, bit 11 of P2DDCRm must be set to 1. The value of the PnDDF bits in PnMRm must be 01. Do not set bits 11 and 10 to 1 at the same time. When bit 10 is set to 1, data are handled as 32-bit/pixel even if bit 11 is set to 0, and thus the function that bit 10 is set to 1 is realized. Since transparent color processing is not possible with 32-bit/pixel data, set the PnSPIM bit in PnMRm to 1. $\alpha$ blending or EOR operations for 32-bit/pixel data and a lower plane must be performed in an area where the lower plane exists. If there is no lower plane, display of 32-bit/pixel data will not be possible after $\alpha$ blending or an EOR operation.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
10	PnLRGB0	0	R/W	Available	<p>Plane n Long (32 Bits) RGB 0</p> <p>0: Data are not handled as 32-bit/pixel (ARGB8888).</p> <p>1: Data in the plane are used as the higher-order bits (A: 8 bits and R: 8 bits) of 32-bit/pixel data (ARGB8888).</p> <p>When a 32-bit/pixel display is specified with this bit, the following restrictions apply. When specifying a 32-bit/pixel display with the PnEDF bits in plane n display data control 4 register m (PnDDC4Rm), refer to the description of the PnEDF bits.</p> <p>Only ARGB8888 can be specified for 32-bit/pixel data.</p> <p>The value of A (8 bits) will be used as the alpha ratio. This means that the alpha ratio selected in the plane n blending ratio register m (PnALPHARm) is invalid.</p> <p>Also, the value of the PnDDF bits in PnMRm must be B'01. Use planes 1 and 2 for a 32-bit/pixel display. Do not set bits 11 and 10 to 1 at the same time.</p> <p>When bit 11 is set to 1, data are handled as 32-bit/pixel even if bit 10 is set to 0, and thus the function that bit 11 is set to 1 is realized.</p> <p>Since transparent color processing is not possible with 32-bit/pixel data, set the PnSPIM bit in PnMRm to 1.</p> <p><math>\alpha</math> blending or EOR operations for 32-bit/pixel data and a lower plane must be performed in an area where the lower plane exists. If there is no lower plane, display of 32-bit/pixel data will not be possible after <math>\alpha</math> blending or an EOR operation.</p>
9 to 0	—	—	R	—	<p>Reserved</p> <p>The read value is undefined. The write value should always be 0.</p>

Use planes 1 and 2 if the display is to have 32-bit/pixel. In this display unit, a 32-bit/pixel display by a single plane is possible. For a 32-bit/pixel display using a single plane, refer to the description of the PnEDF bits in plane n display data control 4 register m (PnDDC4Rm). Register settings for using planes 1 and 2 in a 32-bit/pixel display are given below. Note that the setting of (d) shown below must be made at the last. All other settings can be made in any order.

- (a) Set the LRUO bit in display unit extensional function control 4 register m (DEF4Rm) to 1.  
 (b) The settings for this register are shown below.

Bit:	15	14	13	12	11	10	9	8
					PnLRGB1 PnLRGB0			
Plane 1 (A, R)	—	—	—	—	0	1	—	—
Plane 2 (G, B)	—	—	—	—	1	0	—	—

- (c) The same settings should be made in the plane 1 and plane 2 registers of display plane registers other than this register.
- (d) Turn on the display of planes 1 and 2, and give plane 2 the next order of priority for processing after plane 1. For details on turning on the display, see section 21.4.2, Display On/Off.
- (e) A 32-bit/pixel display should always be specified in lower-numbered planes. For example, when the 32- and 16-bit/pixel display planes are to be superimposed, the 32-bit/pixel display should be specified in planes 1 and 2, and the 16-bit/pixel display should be specified in plane 3 or in higher-numbered planes.
- (f) When the video input module is to be used, refer to the specifications for the video input module.
- (g) If the DU operates in big-endian, set bits 3 and 2 in the plane n swap control register m (PnSWAPRm) to 1 and bits 1 and 0 to 0. Bit 4 may be set to either 1 or 0. Set bit 20 in the display system control register n (DSYSRn) to 0 (n = 0 to 2 for RZ/G1H ;0 and 1 for RZ/G1M/N/E).



### 21.3.4.22 Plane n Display Data Control 2 Register m (PnDDC2Rm, m = 0 and 2)

Note: Suffix "m" as register name and DU2 are only for RZ/G1H.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address: DU0: H'FEB00#88, DU2: H'FEB40#88 (unused for the alpha-ratio planes)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CODE															
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	Pn NV21	Pn Y420	—	—	Pn DIVU	Pn DIVY
Initial value:	—	—	—	—	—	—	—	—	—	—	0	0	—	—	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 16	CODE	—	—/W	Not available	PnDDC2Rm Enabling Code (register available code) For a value written to PnDDC2Rm to be effective, the value must include H'7776 in these bits.
15 to 6	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
5	PnNV21	0	R/W	Available	Plane n NV21 Data Format This bit is only effective when bits 1 and 4 have been set to 1. 0: When YUV420 data are divided up for storage in memory, the order of the UV portion is NV12. 1: When YUV420 data are divided up for storage in memory, the order of the UV portion is NV21.
4	PnY420	0	R/W	Available	Plane n YUV420 Data Format This bit is only effective if bit 1 has been set to 1. When bit 1 is 0, the data format will be YUV422. 0: The YUV data to be divided up for storage in memory is YUV422. 1: The YUV data to be divided up for storage in memory is YUV420. For divided YUV display, see section 21.4.20, Divided YUV Display.
3, 2	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

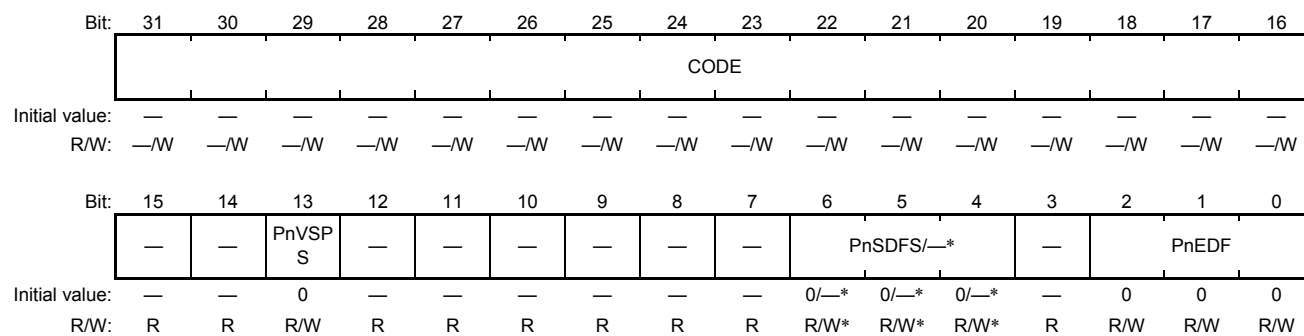
Bit	Bit Name	Initial Value	R/W	Internal Update	Description
1	PnDIVU	0	R/W	Available	<p>Plane n UV Data from Divided YUV</p> <p>0: The data format will be determined by the setting of the PnDDF bits in PnMRm.</p> <p>1: The setting of the PnDDF bits in PnMRm is ineffective and the plane contains the UV data from YUV data that have been divided up for storage in memory. To validate the YC→RGB color space functions, set the PnDDF bits in PnMRm to B'11 (YC format).</p> <p>Do not set bits 1 and 0 in this register at the same time.</p> <p>When bit 0 is set to 1, the data format will not be determined by the setting of the PnDDF bits in PnMRm even if this bit is set to 0. The data format will be determined by bit 0 in this register being set to 1.</p> <p>For divided YUV display, see section 21.4.20, Divided YUV Display.</p>
0	PnDIVY	0	R/W	Available	<p>Plane n Y Data from Divided YUV</p> <p>0: The data format will be determined by the setting of the PnDDF bits in PnMRm.</p> <p>1: The setting of the PnDDF bits in PnMRm is ineffective and the data format is the Y data from YUV data that have been divided up for storage in memory. To validate the YC→RGB color space functions, set the PnDDF bits in PnMRm to B'11 (YC format).</p> <p>Do not set bits 1 and 0 in this register at the same time.</p> <p>When bit 1 is set to 1, the data format will not be determined by the setting of the PnDDF bits in PnMRm even if this bit is set to 0. The data format will be determined by bit 1 in this register being set to 1.</p> <p>For divided YUV display, see section 21.4.20, Divided YUV Display.</p>

### 21.3.4.23 Plane n Display Data Control 4 Register m (PnDDC4Rm, m = 0 and 2)

Note: Suffix "m" as register name and DU2 are only for RZ/G1H.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address: DU0: H'FEB00#90, DU2: H'FEB40#90 (Alpha ratio plane address: DU0: H'FEB0A#90, DU2: H'FEB4A#90)



Note: \* For reserved bit (bit name: —), initial value is undefined, writing is not available and writing value should be specified. For details of bit description, refer to following table.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 16	CODE	—	—/W	Not available	PnDDC4Rm Enabling Code (register available code) For a value written to PnDDC4Rm to be effective, the value must include H'7766 in these bits.
15, 14	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
13	PnVSPS	0	R/W	Available	Plane n VSP1 Select To enable bit 13, set the DEFE8 bit in the display unit extensional function control 8 register m (DEF8Rm) to 1. Bit 13 is fixed to 0 in its initial state. 0: Uses image data in memory. 1: Uses image data in VSP1. This data can be used only in plane 1 and plane 2. For RZ/G1H, the DU2 can only use plane 1. RZ/G1E can only use plane 1. Transparent color processing for VSP1 data is not possible. The format of the pixel data is either ARGB8888 or RGB888. Only the value A for VSP1 is applied as the alpha value in ARGB8888.
12 to 7	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
6 to 4	PnSDFS	000	R/W	Available	<p>Plane n Superimpose Data Format Select [RZ/G1H]</p> <p>0--: RGB composite. For YC data, composition is performed after YC-RGB conversion.</p> <p>100: Setting prohibited.</p> <p>101: YC composite. DRC processing is not performed after YC composite. YC-RGB conversion is performed.</p> <p>110: Setting prohibited.</p> <p>111: YC composite. After YC composite, DRC processing and YC-RGB conversion are performed.</p> <p>When performing DRC processing or YC-RGB conversion, set desired values in the YCRGB1, YCRGB0, DRC1, and DRC0 bits in DEF5Rm. DRC processing or YC-RGB conversion cannot be performed with only the settings of this register.</p> <p>If DRC processing is specified for multiple planes, the same values should be specified to PnDSYRm and PnDPYRm.</p> <p>A plane with DRC processing cannot be superimposed on a plane without DRC processing.</p> <p>When YC composite has been set, YC composite should also be set for the superposed lower plane.</p> <p>When YC composite is set, the PnDDF bits in PnMRm should be set to B'11 (YC).</p>
	—	—	R	—	<p>Reserved [RZ/G1M/N/E]</p> <p>The read value is undefined. The write value should always be 0.</p>
3	—	—	R	—	<p>Reserved</p> <p>The read value is undefined. The write value should always be 0.</p>
2 to 0	PnEDF	000	R/W	Available	<p>Plane n Extensional Data Format</p> <p>000: The data format will be determined by the PnDDF bits in PnMRm, the PnLRGB1 or PnLRGB0 bit in PnDDCRm, or the PnDIVU or PnDIVY bit in PnDDC2Rm.</p> <p>001: ARGB8888</p> <p>010: RGB888</p> <p>011: RGB666</p> <p>100: Setting prohibited</p> <p>101: Setting prohibited</p> <p>110: Setting prohibited</p> <p>111: Setting prohibited</p> <p>This data format cannot be used for alpha-ratio planes.</p> <p>If the DU operates in big-endian, set bits 3 and 2 in PnSWAPRm to 1 and bits 1 and 0 to 0. Bit 4 may be set to either 1 or 0. Set bit 20 in DSYSRn to 0 (n = 0 to 2 for RZ/G1H; 0 and 1 for RZ/G1M/N/E).</p>

### 21.3.4.24 Alpha-ratio Plane n Mode Register m (APnMRm, m = 0 and 2)

Note: Suffix "m" as register name and DU2 are only for RZ/G1H.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address: DU0: H'FEB0A#00, DU2: H'FEB4A#00

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PnWAE
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	PnDC	—	PnBM	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	0	—	0	0	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R/W	R	R/W	R/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 17	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
16	PnWAE	0	R/W	Available	Plane n Wrap-Around Enable 0: Wrapping-around for plane n is disabled. 1: Wrapping-around for plane n is enabled.
15 to 8	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
7	PnDC	0	R/W	Available	Plane n Display Area Change 0: In manual display change mode, switching of the frame buffer is not performed. 1: In manual display change mode, switching of the frame buffer is performed. When the PnDC bit is 0, bit setting is possible. Switching is performed in frame units. After frame buffer switching (after vertical blanking detection), this bit is cleared to 0.
6	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
5, 4	PnBM	00	R/W	Available	Plane n Buffer Mode 00: Manual display change mode 01: Setting prohibited 10: Auto display change mode (blinking mode) 11: Setting prohibited In manual display change mode or auto display change mode (blinking mode), double-buffering control is performed using addresses 0 and 1, respectively indicated by the PnDSA0 and PnDSA1 bits in PnDSA0Rm and PnDSA1Rm.
3 to 0	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

The functions of the plane n mode register m(PnMRm) are partially unavailable in the alpha-ratio plane n mode register m(APnMRm) because the functions of the planes dedicated to the  $\alpha$  value are limited more than those of the display planes. The following bits are unavailable, and thus absent.

Bit 20 (PnYCDF) is absent because the display data format is fixed to 8-bit/pixel.

Bit 17 (PnTC) is absent because the alpha ratios cannot be treated as a transparent color.

Bits 14 to 12 (PnSPIM) are absent because superpositioning is not available.

Bits 10 to 8 (PnCPSL) are absent because the use of a color palette is not possible.

Bits 1 and 0 (PnDDF) are absent because the display data format is fixed to 8-bit/pixel.

### 21.3.5 Display Capture Registers

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Note: All registers in section 21.3.5 are common to RZ/G1H, M, N and E. Suffix "m" as register name and DU2 are only for RZ/G1H.

In descriptions that are common to display capture units 1 and 2, the display capture units are generically referred to as display capture n. This meaning of character n and the meaning of # are given below.

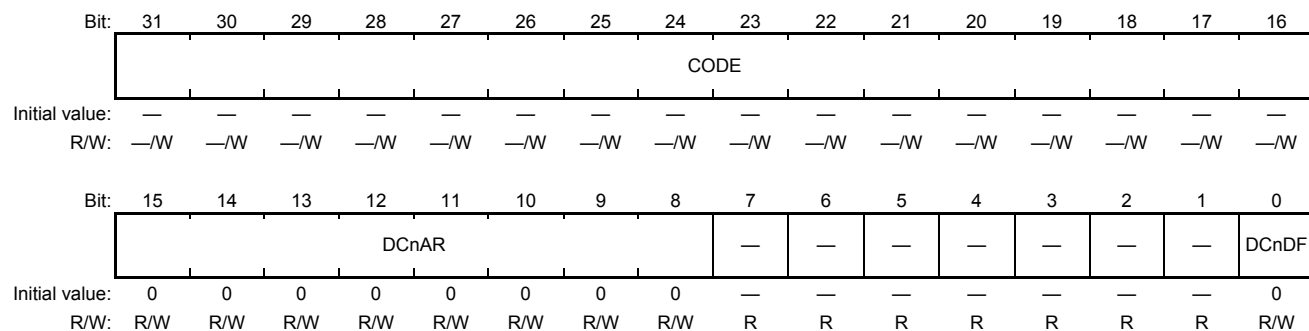
m: Indicates the display unit channel number (0 and 2). (RZ/G1H only)

n: no number or 2 (m = 2 and n = 2 as register name not exist)

#: Corresponds to n but represents a hexadecimal digit in an address. For example, address H'FEBC#04 for the capture 1 memory width register corresponds to H'FEBC104.

#### 21.3.5.1 Display Capture n Mode Register m (DCnMRm, m = 0 and 2)

Address: DU0: H'FEBC#00, DU2: H'FEBC#00



Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 16	CODE	—	—/W	Not available	DCnMRm Enabling Code (register available code) For a value written to DCnMRm to be effective, the value must include H'7790 in these bits.
15 to 8	DCnAR	0	R/W	Available	Display Capture n Alpha Ratio This bit is effective when bit 0 in this register is set to 1.
7 to 1	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
0	DCnDF	0	R/W	Available	Display Capture n Data Format 0: The data format is determined by bits 5 and 4 in DCPCRm. 1: The data format is ARGB8888. The "A" value is specified by bits 15 to 8 in this register.

### 21.3.5.2 Display Capture n Memory Width Register m (DCnMWRm, m = 0 and 2)

Address: DU0: H'FEB0C#04, DU2: H'FEB4C#04

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	DCnMWX								—	—	—	—	
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 13	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
12 to 4	DCnMWX	—	R/W	Available	Display Capture n Memory Width X Select the memory width for display capture n to a value between 16 and 4096 pixels, in 16-pixel units. When the width of captured data exceeds this size, the excess data will not be captured. The value is retained during a reset.
3 to 0	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

### 21.3.5.3 Display Capture n Area Start Address Register m (DCnSARm, m = 0 and 2)

Address: DU0: H'FEB0C#20, DU2: H'FEB4C#20

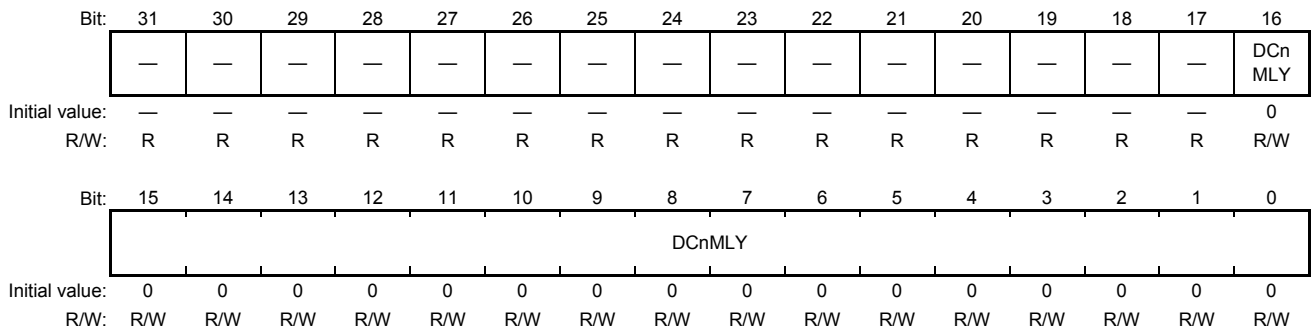
Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DCnSA															
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DCnSA												—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 4	DCnSA	—	R/W	Available	Display Capture n Area Start Address To enable bits 31 to 29, the DEFE bit in DEFRm/DEFRO* must be set to 1. In the initial state, these bits are not enabled. The value is retained during a reset. Note: * DEFRO is for RZ/G1M/N/E
3 to 0	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.



**21.3.5.4 Display Capture n Memory Length Register m (DCnMLRm, m = 0 and 2)**

Address: DU0: H'FEB0C#50, DU2: H'FEB4C#50



Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 17	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
16 to 0	DCnMLY	H'0 0000	R/W	Available	Display Capture n Memory Length Y Select the memory length (Y-direction memory area) for display capture n. When the value of these bits is 0 (default), the size is unlimited.

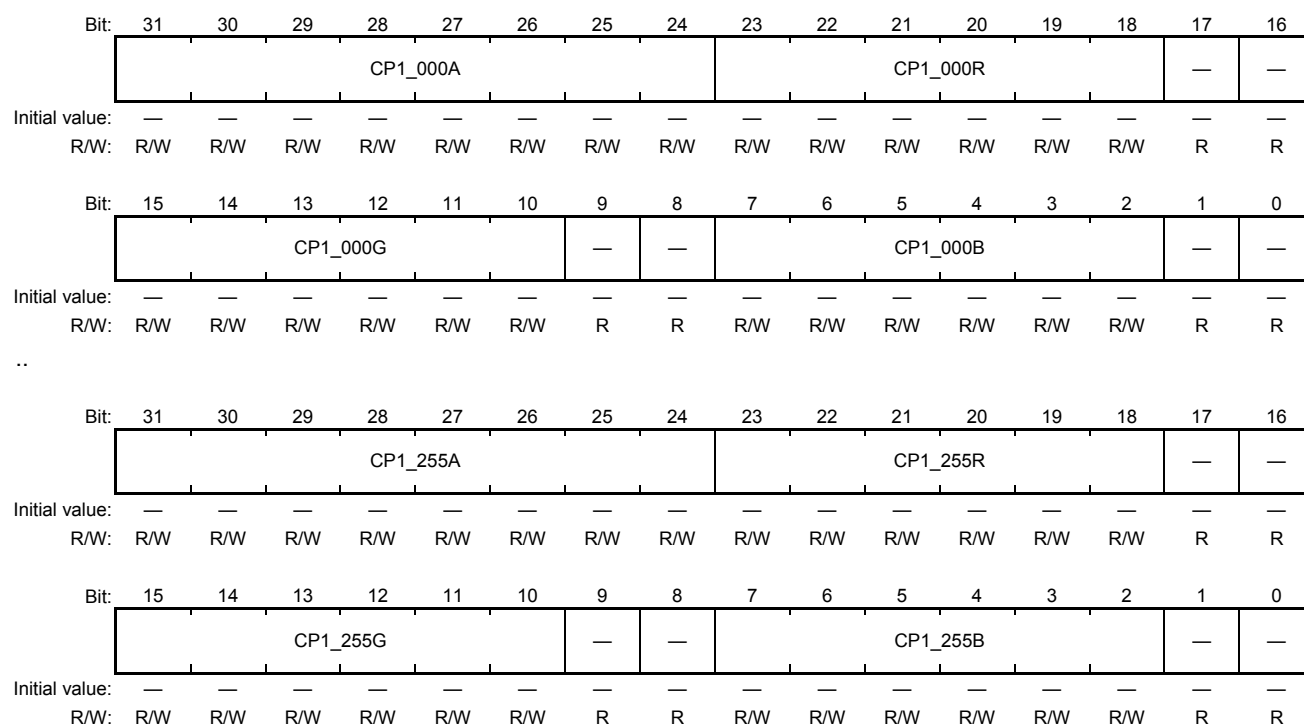
### 21.3.6 Color Palette Registers

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Note: All registers in section 21.3.6 are common to RZ/G1H, M, N and E. Suffix "m" as register name and DU2 are only for RZ/G1H.

#### 21.3.6.1 Color Palette 1 (000 to 255) Register m (CP1\_000Rm to CP1\_255Rm, m = 0 and 2)

Address: DU0: H'FEB01000 to H'FEB013FC, DU2: H'FEB41000 to H'FEB413FC



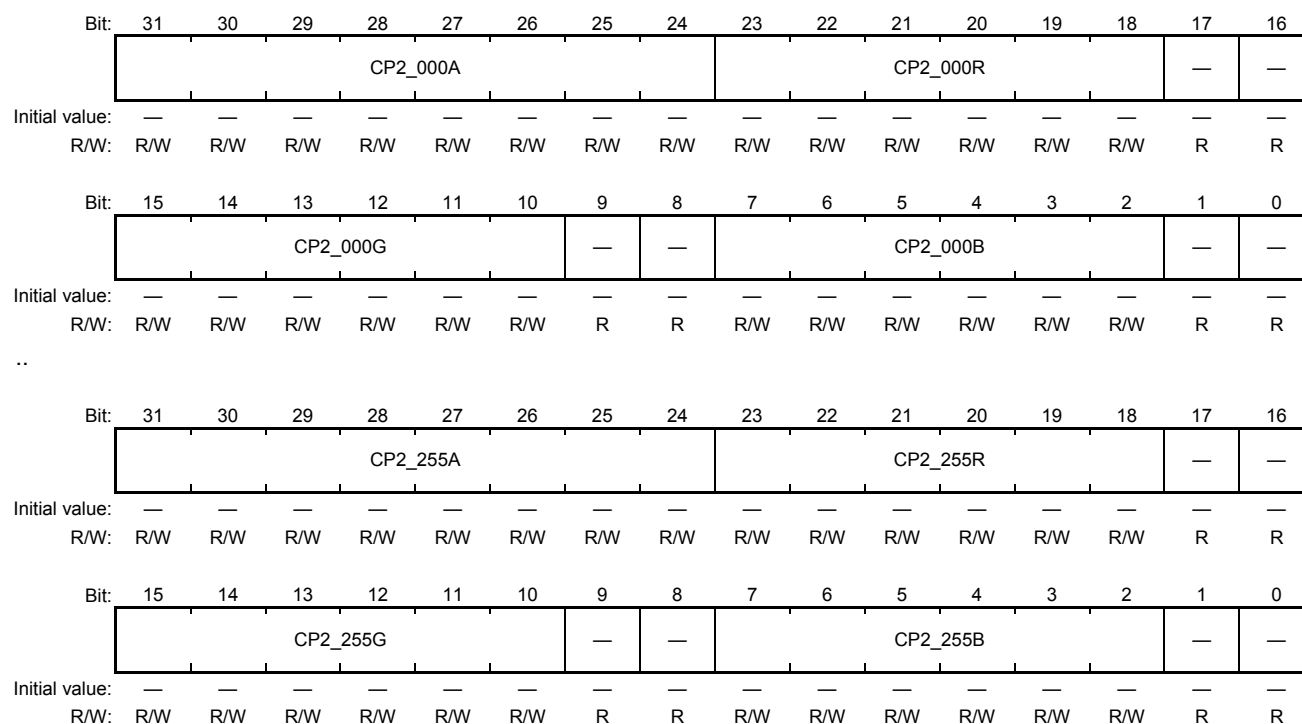
Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 24	CP1_000A to CP1_255A	—	R/W	Available	Color Palette 1_000 to 255 Blending Ratio When the PnBRSLS bits in PnALPHARm are B'10, the value is the alpha ratio, which is the $\alpha$ blending ratio. The value is retained during a reset.
23 to 18	CP1_000R to CP1_255R	—	R/W	Available	Color Palette 1_000 to 255 Red Red-color data of color palette 1. The value is retained during a reset.
17, 16	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
15 to 10	CP1_000G to CP1_255G	—	R/W	Available	Color Palette 1_000 to 255 Green Green-color data of color palette 1. The value is retained during a reset.
9, 8	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
7 to 2	CP1_000B to CP1_255B	—	R/W	Available	Color Palette 1_000 to 255 Blue Blue-color data of color palette 1. The value is retained during a reset.
1, 0	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

- Notes:
1. CP1\_000R to CP1\_255R form a group of 256 registers in which six bits are set for each of the R, G, and B components of a color, setting up the color palette of 256 colors from among the 262 thousand colors for display. The values are valid for 8-bit/pixel data display.  
After the CP1CE bit in CPCRm has been set to 1, settings for CP1\_000R to CP1\_255R become effective on the next falling edge of VSYNC (timing of an internal update) or when the display is reset. When you update the color palette, rewrite the entire palette. Reading of the color palette by the CPU must proceed before the CP1CE bit has been set to 1. The color palette is accessible in longword units.
  2. m = 0 and 2, suffix "m" is only for RZ/G1H.

### 21.3.6.2 Color Palette 2 (000 to 255) Register m (CP2\_000Rm to CP2\_255Rm, m = 0 and 2)

Address: DU0: H'FEB02000 to H'FEB023FC, DU2: H'FEB42000 to H'FEB423FC

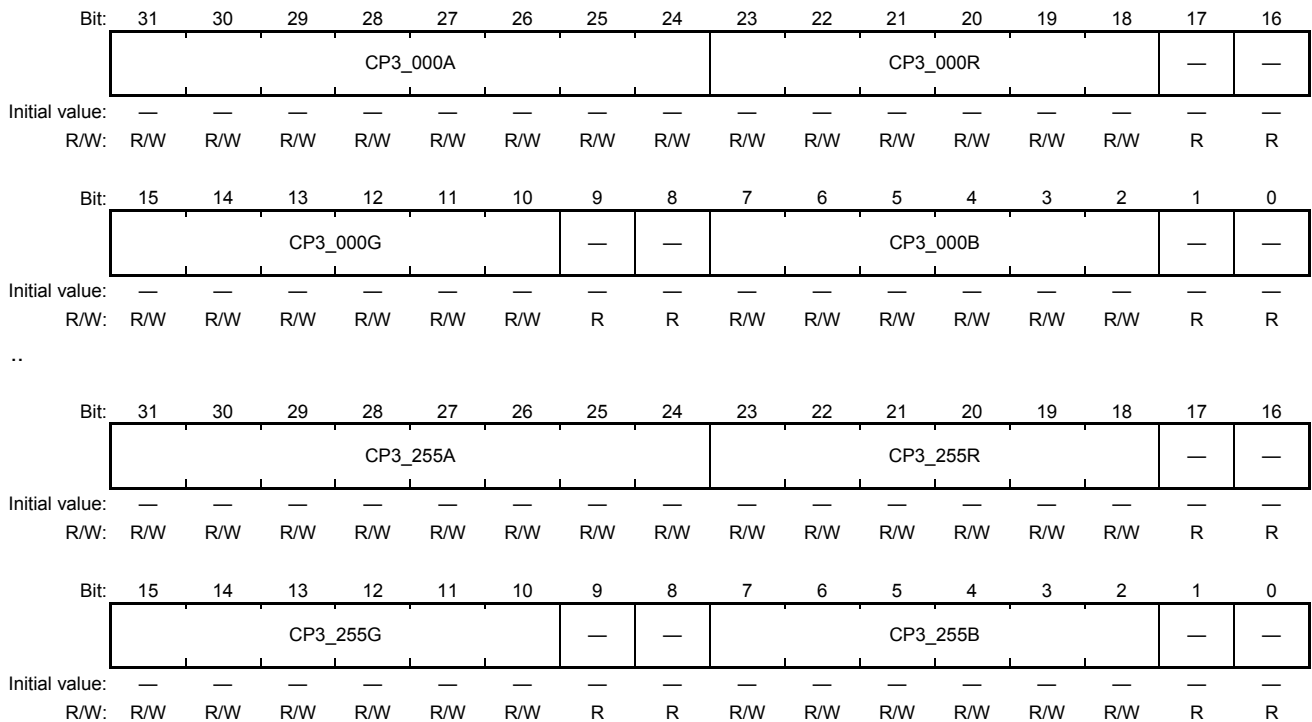


Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 24	CP2_000A to CP2_255A	—	R/W	Available	Color Palette 2_000 to 255 Blending Ratio When the PnBRSL bits in PnALPHARm are B'10, the value is the alpha ratio, which is the $\alpha$ blending ratio. The value is retained during a reset.
23 to 18	CP2_000R to CP2_255R	—	R/W	Available	Color Palette 2_000 to 255 Red Red-color data of color palette 2. The value is retained during a reset.
17, 16	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
15 to 10	CP2_000G to CP2_255G	—	R/W	Available	Color Palette 2_000 to 255 Green Green-color data of color palette 2. The value is retained during a reset.
9, 8	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
7 to 2	CP2_000B to CP2_255B	—	R/W	Available	Color Palette 2_000 to 255 Blue Blue-color data of color palette 2. The value is retained during a reset.
1, 0	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

- Notes: 1. CP2\_000R to CP2\_255R form a group of 256 registers in which six bits are set for each of the R, G, and B components of a color, setting up the color palette of 256 colors from among the 262 thousand colors for display. The values are valid for 8-bit/pixel data display.  
After the CP2CE bit in CPCRM has been set to 1, settings for CP2\_000R to CP2\_255R become effective on the next falling edge of VSYNC (timing of an internal update) or when the display is reset. When you update the color palette, rewrite the entire palette. Reading of the color palette by the CPU must proceed before the CP2CE bit has been set to 1. The color palette is accessible in longword units.
2. m = 0 and 2, suffix "m" is only for RZ/G1H.

**21.3.6.3 Color Palette 3 (000 to 255) Register m (CP3\_000Rm to CP3\_255Rm, m = 0 and 2)**

Address: DU0: H'FEB03000 to H'FEB033FC, DU2: H'FEB43000 to H'FEB433FC

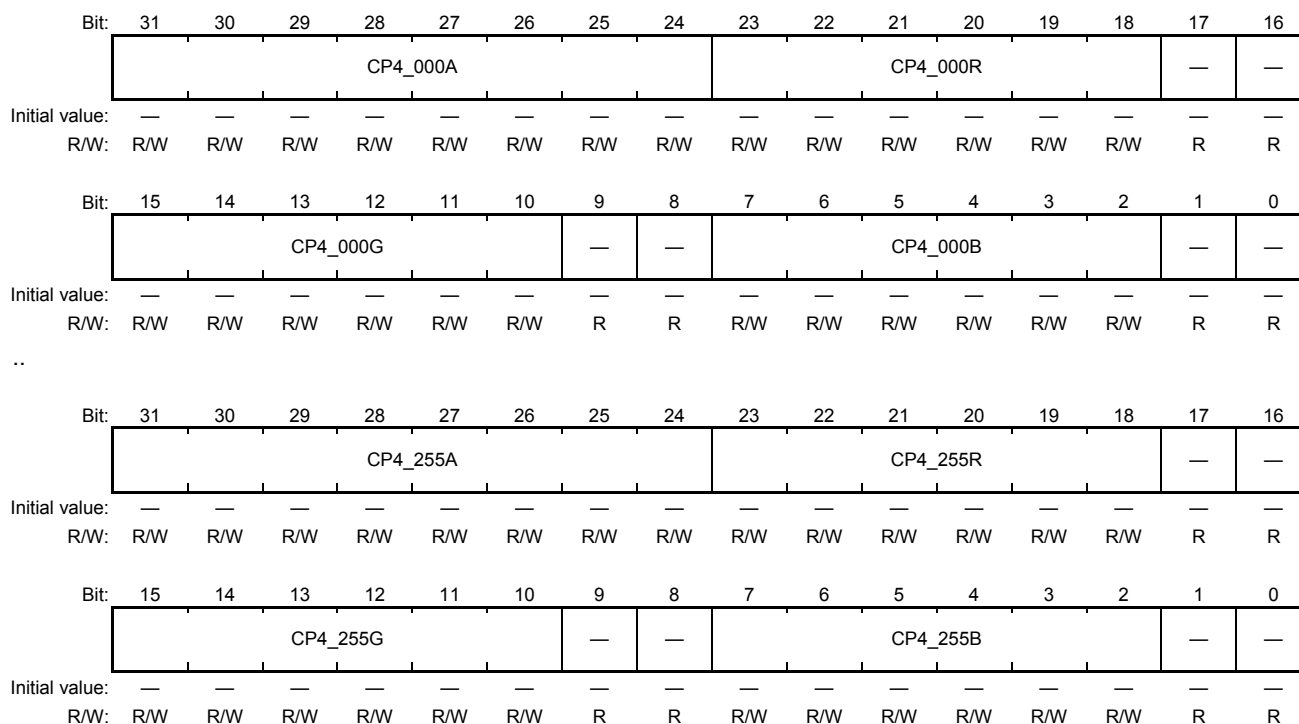


Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 24	CP3_000A to CP3_255A	—	R/W	Available	Color Palette 3_000 to 255 Blending Ratio When the PnBRSL bits in PnALPHARm are B'10, the value is the alpha ratio, which is the α blending ratio. The value is retained during a reset.
23 to 18	CP3_000R to CP3_255R	—	R/W	Available	Color Palette 3_000 to 255 Red Red-color data of color palette 3. The value is retained during a reset.
17, 16	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
15 to 10	CP3_000G to CP3_255G	—	R/W	Available	Color Palette 3_000 to 255 Green Green-color data of color palette 3. The value is retained during a reset.
9, 8	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
7 to 2	CP3_000B to CP3_255B	—	R/W	Available	Color Palette 3_000 to 255 Blue Blue-color data of color palette 3. The value is retained during a reset.
1, 0	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

- Notes:
- CP3\_000R to CP3\_255R form a group of 256 registers in which six bits are set for each of the R, G, and B components of a color, setting up the color palette of 256 colors from among the 262 thousand colors for display. The values are valid for 8-bit/pixel data display.  
After the CP3CE bit in CPCRm has been set to 1, settings for CP3\_000R to CP3\_255R become effective on the next falling edge of VSYNC (timing of an internal update) or when the display is reset. When you update the color palette, rewrite the entire palette. Reading of the color palette by the CPU must proceed before the CP3CE bit has been set to 1. The color palette is accessible in longword units.
  - m = 0 and 2, suffix "m" is only for RZ/G1H.

### 21.3.6.4 Color Palette 4 (000 to 255) Register m (CP4\_000Rm to CP4\_255Rm, m = 0 and 2)

Address: DU0: H'FEB04000 to H'FEB043FC, DU2: H'FEB44000 to H'FEB443FC



Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 24	CP4_000A to CP4_255A	—	R/W	Available	Color Palette 4_000 to 255 Blending Ratio When the PnBRSL bits in PnALPHARm are B'10, the value is the alpha ratio, which is the $\alpha$ blending ratio. The value is retained during a reset.
23 to 18	CP4_000R to CP4_255R	—	R/W	Available	Color Palette 4_000 to 255 Red Red-color data of color palette 4. The value is retained during a reset.
17, 16	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
15 to 10	CP4_000G to CP4_255G	—	R/W	Available	Color Palette 4_000 to 255 Green Green-color data of color palette 4. The value is retained during a reset.
9, 8	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
7 to 2	CP4_000B to CP4_255B	—	R/W	Available	Color Palette 4_000 to 255 Blue Blue-color data of color palette 4. The value is retained during a reset.
1, 0	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

- Notes:
- CP4\_000R to CP4\_255R form a group of 256 registers in which six bits are set for each of the R, G, and B components of a color, setting up the color palette of 256 colors from among the 262 thousand colors for display. The values are valid for 8-bit/pixel data display.  
After the CP4CE bit in CPCRm has been set to 1, settings for CP4\_000R to CP4\_255R become effective on the next falling edge of VSYNC (timing of an internal update) or when the display is reset. When you update the color palette, rewrite the entire palette. Reading of the color palette by the CPU must proceed before the CP4CE bit has been set to 1. The color palette is accessible in longword units.
  - m = 0 and 2, suffix "m" is only for RZ/G1H.

### 21.3.7 External Synchronization Control Registers

The three sets of external synchronization control registers are for the respective channels and have the same functions; they are described as one here.

In section 21.3.7, n = 0 to 2 for RZ/G1H, 0 and 1 for RZ/G1M/N/E. DU2 is only for RZ/G1H.

#### 21.3.7.1 External Synchronization Control Register n (ESCRn)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address: DU0: H'FEB10000, DU1: H'FEB31000, DU2: H'FEB50000[Only RZ/G1H]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	DCKOINV	—/DCKOSEL*	—	—	—	DCLKSEL	—	—	—	DCLKDIS
Initial value:	—	—	—	—	—	—	0	—/0*	—	—	—	0	—	—	—	0
R/W:	R	R	R	R	R	R	R/W	R/W*	R	R	R	R/W	R	R	R	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	SYNCSEL		—	—	FRQSEL					
Initial value:	—	—	—	—	—	—	0	0	—	—	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Note: \* Value of reserved bit (bit name: —) is undefined. For details of bit description, refer to following table.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 26	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
25	DCKOINV	0	R/W	Not available	DCLKOUT Invert To enable this bit, set the DEFE bit in the display unit extensional function control register m*1 (DEFRm*1) to 1. In the initial state, this bit is fixed to 0. 0: DCLKOUT is output in normal phase. 1: DCLKOUT is output in counter phase.
24	—	—	R	—	Reserved [RZ/G1H] The read value is undefined. The write value should always be 0.
	DCKOSEL	0	R/W	Not available	Output Dot Clock Select (DCLKOUT Select) [RZ/G1M/N/E] To enable this bit, set DEFE to 1 in the display unit extensional function control register 0 (DEFR0). In the initial state, this bit is fixed at 0. Set this bit to 1 to specify display output in YC data format. 0: The DCLKOUT division ratio is determined by bits 5 to 0 in this register. 1: DCLKIN is used as DCLKOUT, regardless of the division ratio.
23 to 21	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
20	DCLKSEL	0	R/W	Not available	DCLKIN Select 0: The input dot clock source is the DCLKIN pin 1: The input dot clock source is the ZX $\phi$ clock. If this setting is made, ensure that the frequency of the input dot clock is divided by two or a greater value (so that the result of dividing the frequency is more than or equal to half the ZX $\phi$ frequency).
19 to 17	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
16	DCLKDIS	0	R/W	Not available	DCLKOUT Disable 0: DCLKOUT is output. 1: DCLKOUT is not output. DCLKOUT is fixed to low level.
15 to 10	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
9, 8	SYNCSEL	00	R/W	Not available	SYNC Select 00: Phases are not synchronized 01: Phases are not synchronized 10: Phases are synchronized by using the EXVSYNC signal 11: Phases are synchronized by using the EXHSYNC signal
7, 6	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.



Bit	Bit Name	Initial Value	R/W	Internal Update	Description
5 to 0	FRQSEL	000000	R/W	Not available	<p>Frequency Select</p> <p>To enable bit 5, the DEFE bit in DEFRm*1 must be set to 1. In the initial state, bit 5 is fixed to 0.</p> <p>If frequency division is by an odd number, the duty cycle of the frequency divided dot clock will be below 50%.</p> <p>000000: Frequency division of the input dot clock (clock for division) is not performed.</p> <p>000001: Division by 2 of the input dot clock (clock for division)</p> <p>000010: Division by 3 of the input dot clock (clock for division)</p> <p>000011: Division by 4 of the input dot clock (clock for division)</p> <p>000100: Division by 5 of the input dot clock (clock for division)</p> <p>000101: Division by 6 of the input dot clock (clock for division)</p> <p>000110: Division by 7 of the input dot clock (clock for division)</p> <p>000111: Division by 8 of the input dot clock (clock for division)</p> <p>001000: Division by 9 of the input dot clock (clock for division)</p> <p>001001: Division by 10 of the input dot clock (clock for division)</p> <p>001010: Division by 11 of the input dot clock (clock for division)</p> <p>001011: Division by 12 of the input dot clock (clock for division)</p> <p>001100: Division by 13 of the input dot clock (clock for division)</p> <p>001101: Division by 14 of the input dot clock (clock for division)</p> <p>001110: Division by 15 of the input dot clock (clock for division)</p> <p>001111: Division by 16 of the input dot clock (clock for division)</p> <p>010000: Division by 17 of the input dot clock (clock for division)</p> <p>010001: Division by 18 of the input dot clock (clock for division)</p> <p>010010: Division by 19 of the input dot clock (clock for division)</p> <p>010011: Division by 20 of the input dot clock (clock for division)</p> <p>010100: Division by 21 of the input dot clock (clock for division)</p> <p>010101: Division by 22 of the input dot clock (clock for division)</p> <p>010110: Division by 23 of the input dot clock (clock for division)</p> <p>010111: Division by 24 of the input dot clock (clock for division)</p> <p>011000: Division by 25 of the input dot clock (clock for division)</p> <p>011001: Division by 26 of the input dot clock (clock for division)</p> <p>011010: Division by 27 of the input dot clock (clock for division)</p> <p>011011: Division by 28 of the input dot clock (clock for division)</p> <p>011100: Division by 29 of the input dot clock (clock for division)</p>

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
5 to 0	FRQSEL	000000	R/W	Not available	011101: Division by 30 of the input dot clock (clock for division) 011110: Division by 31 of the input dot clock (clock for division) 011111: Division by 32 of the input dot clock (clock for division) 100000: Division by 33 of the input dot clock (clock for division) 100001: Division by 34 of the input dot clock (clock for division) 100010: Division by 35 of the input dot clock (clock for division) 100011: Division by 36 of the input dot clock (clock for division) 100100: Division by 37 of the input dot clock (clock for division) 100101: Division by 38 of the input dot clock (clock for division) 100110: Division by 39 of the input dot clock (clock for division) 100111: Division by 40 of the input dot clock (clock for division) 101000: Division by 41 of the input dot clock (clock for division) 101001: Division by 42 of the input dot clock (clock for division) 101010: Division by 43 of the input dot clock (clock for division) 101011: Division by 44 of the input dot clock (clock for division) 101100: Division by 45 of the input dot clock (clock for division) 101101: Division by 46 of the input dot clock (clock for division) 101110: Division by 47 of the input dot clock (clock for division) 101111: Division by 48 of the input dot clock (clock for division) 110000: Division by 49 of the input dot clock (clock for division) 110001: Division by 50 of the input dot clock (clock for division) 110010: Division by 51 of the input dot clock (clock for division) 110011: Division by 52 of the input dot clock (clock for division) 110100: Division by 53 of the input dot clock (clock for division) 110101: Division by 54 of the input dot clock (clock for division) 110110: Division by 55 of the input dot clock (clock for division) 110111: Division by 56 of the input dot clock (clock for division) 111000: Division by 57 of the input dot clock (clock for division) 111001: Division by 58 of the input dot clock (clock for division) 111010: Division by 59 of the input dot clock (clock for division) 111011: Division by 60 of the input dot clock (clock for division) 111100: Division by 61 of the input dot clock (clock for division) 111101: Division by 62 of the input dot clock (clock for division) 111110: Division by 63 of the input dot clock (clock for division) 111111: Division by 64 of the input dot clock (clock for division)

Notes: 1. m = 0 and 2 for RZ/G1H, m = 0 for RZ/G1M/N/E.

### 21.3.7.2 Output Signal Timing Adjustment Register n (OTARn)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address: DU0: H'FEB10004, DU1: H'FEB31004, DU2: H'FEB50004 [Only RZ/G1H]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	DEA			—	CLAMPA			—	DRGBA			—	—	—	—
Initial value:	—	0	0	0	—	0	0	0	—	0	0	0	—	—	—	—
R/W:	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	CDEA			—	DISPA			—	SYNCA		
Initial value:	—	—	—	—	—	0	0	0	—	0	0	0	—	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
30 to 28	DEA	000	R/W	DRES	DE Output Timing Adjustment 000: Adjustment of output timing is not performed. The DE signal is output on the rising edge of the dot clock, with the reference timing. 001: The DE signal is output on the rising edge, delayed one dot clock cycle relative to the reference timing. 010: The DE signal is output on the rising edge, delayed two dot clock cycles relative to the reference timing. 011: The DE signal is output on the rising edge, delayed three dot clock cycles relative to the reference timing. 100: The DE signal is output on the falling edge, preceding the reference timing by 1/2 dot clock cycle. 101: The DE signal is output on the falling edge, delayed 1/2 dot clock cycle relative to the reference timing. 110: The DE signal is output on the falling edge, delayed (1+1/2) dot clock cycles relative to the reference timing. 111: The DE signal is output on the falling edge, delayed (2+1/2) dot clock cycles relative to the reference timing.
27	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
26 to 24	CLAMPA	000	R/W	DRES	<p>CLAMP Output Timing Adjustment</p> <p>000: Adjustment of output timing is not performed. The CLAMP signal is output on the rising edge of the dot clock, with the reference timing.</p> <p>001: The CLAMP signal is output on the rising edge, delayed one dot clock cycle relative to the reference timing.</p> <p>010: The CLAMP signal is output on the rising edge, delayed two dot clock cycles relative to the reference timing.</p> <p>011: The CLAMP signal is output on the rising edge, delayed three dot clock cycles relative to the reference timing.</p> <p>100: The CLAMP signal is output on the falling edge, preceding the reference timing by 1/2 dot clock cycle.</p> <p>101: The CLAMP signal is output on the falling edge, delayed 1/2 dot clock cycle relative to the reference timing.</p> <p>110: The CLAMP signal is output on the falling edge, delayed (1+1/2) dot clock cycles relative to the reference timing.</p> <p>111: The CLAMP signal is output on the falling edge, delayed (2+1/2) dot clock cycles relative to the reference timing.</p>
23	—	—	R	—	<p>Reserved</p> <p>The read value is undefined. The write value should always be 0.</p>
22 to 20	DRGBA	000	R/W	DRES	<p>Digital RGB Output Timing Adjustment</p> <p>000: Adjustment of output timing is not performed. The digital RGB signal is output on the rising edge of the dot clock, with the reference timing.</p> <p>001: The digital RGB signal is output on the rising edge, delayed one dot clock cycle relative to the reference timing.</p> <p>010: The digital RGB signal is output on the rising edge, delayed two dot clock cycles relative to the reference timing.</p> <p>011: The digital RGB signal is output on the rising edge, delayed three dot clock cycles relative to the reference timing.</p> <p>100: The digital RGB signal is output on the falling edge, preceding the reference timing by 1/2 dot clock cycle.</p> <p>101: The digital RGB signal is output on the falling edge, delayed 1/2 dot clock cycle relative to the reference timing.</p> <p>110: The digital RGB signal is output on the falling edge, delayed (1+1/2) dot clock cycles relative to the reference timing.</p> <p>111: The digital RGB signal is output on the falling edge, delayed (2+1/2) dot clock cycles relative to the reference timing.</p> <p>If you intend to use the output dot clock to control the timing of the switching of data for display, do not select the falling edge (i.e. do not set bit 22 to 1).</p> <p><u>The value of bits 22 to 20 of output signal timing adjustment register 0 (OTAR0) must be the same as that of bits 22 to 20 in output signal timing adjustment register 1 (OTAR1).</u></p>
19 to 11	—	—	R	—	<p>Reserved</p> <p>The read value is undefined. The write value should always be 0.</p>

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
10 to 8	CDEA	000	R/W	DRES	<p>CDE Output Timing Adjustment</p> <p>000: Adjustment of output timing is not performed. The CDE signal is output on the rising edge of the dot clock, with the reference timing.</p> <p>001: The CDE signal is output on the rising edge, delayed one dot clock cycle relative to the reference timing.</p> <p>010: The CDE signal is output on the rising edge, delayed two dot clock cycles relative to the reference timing.</p> <p>011: The CDE signal is output on the rising edge, delayed three dot clock cycles relative to the reference timing.</p> <p>100: The CDE signal is output on the falling edge, preceding the reference timing by 1/2 dot clock cycle.</p> <p>101: The CDE signal is output on the falling edge, delayed 1/2 dot clock cycle relative to the reference timing.</p> <p>110: The CDE signal is output on the falling edge, delayed (1+1/2) dot clock cycles relative to the reference timing.</p> <p>111: The CDE signal is output on the falling edge, delayed (2+1/2) dot clock cycles relative to the reference timing.</p>
7	—	—	R	—	<p>Reserved</p> <p>The read value is undefined. The write value should always be 0.</p>
6 to 4	DISPA	000	R/W	DRES	<p>DISP Output Timing Adjustment</p> <p>000: Adjustment of output timing is not performed. The DISP signal is output on the rising edge of the dot clock, with the reference timing.</p> <p>001: The DISP signal is output on the rising edge, delayed one dot clock cycle relative to the reference timing.</p> <p>010: The DISP signal is output on the rising edge, delayed two dot clock cycles relative to the reference timing.</p> <p>011: The DISP signal is output on the rising edge, delayed three dot clock cycles relative to the reference timing.</p> <p>100: The DISP signal is output on the falling edge, preceding the reference timing by 1/2 dot clock cycle.</p> <p>101: The DISP signal is output on the falling edge, delayed 1/2 dot clock cycle relative to the reference timing.</p> <p>110: The DISP signal is output on the falling edge, delayed (1+1/2) dot clock cycles relative to the reference timing.</p> <p>111: The DISP signal is output on the falling edge, delayed (2+1/2) dot clock cycles relative to the reference timing.</p>
3	—	—	R	—	<p>Reserved</p> <p>The read value is undefined. The write value should always be 0.</p>

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
2 to 0	SYNCA	000	R/W	DRES	<p>SYNC* Output Timing Adjustment</p> <p>000: Adjustment of output timing is not performed. The SYNC* signal is output on the rising edge of the dot clock, with the reference timing.</p> <p>001: The SYNC* signal is output on the rising edge, delayed one dot clock cycle relative to the reference timing.</p> <p>010: The SYNC* signal is output on the rising edge, delayed two dot clock cycles relative to the reference timing.</p> <p>011: The SYNC* signal is output on the rising edge, delayed three dot clock cycles relative to the reference timing.</p> <p>100: The SYNC* signal is output on the falling edge, preceding the reference timing by 1/2 dot clock cycle.</p> <p>101: The SYNC* signal is output on the falling edge, delayed 1/2 dot clock cycle relative to the reference timing.</p> <p>110: The SYNC* signal is output on the falling edge, delayed (1+1/2) dot clock cycles relative to the reference timing.</p> <p>111: The SYNC* signal is output on the falling edge, delayed (2+1/2) dot clock cycles relative to the reference timing.</p> <p>Note: * HSYNC, VSYNC, CSYNC, and ODDF signals</p>

Note: When signals are to be output on the falling edge, the electrical characteristics do not apply.

## 21.3.8 Dual Display Output Control Registers

### 21.3.8.1 Display Unit Output Route Control Register m (DORCRm, m = 0)

Note: Suffix "m" as register name is only for RZ/G1H.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address: DU0: H'FEB1 1000

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	PG1T	—	DK1S	—	—	PG1D	—	—	DR0D	—	—	—	—	PG0D	0
Initial value:	—	1	—	1	—	—	0	1	—	—	0	—	—	—	0	0
R/W:	R	R/W	R	R/W	R	R	R/W	R/W	R	R	R/W	R	R	R	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	RGPV/ —*	—	—	—	DPRS
Initial value:	—	—	—	—	—	—	—	—	—	—	—	0/—*	—	—	—	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W*	R	R	R	R/W

Note: \* For reserved bit (bit name: —), initial value is undefined. For details, refer to following table.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
30	PG1T	1	R/W	DRES	Pin Generate 1 Timing Select Selects the source of timing for pin controller 1. 0: Display-timing generator 0 1: Display-timing generator 1
29	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
28	DK1S	1	R/W	DRES	Dot Clock Select 1 0: Dot-clock generator 0 supplies the dot clock for display-timing generator 1 and pin controller 1. 1: Dot-clock generator 1 supplies the dot clock for display-timing generator 1 and pin controller 1. When the TVM1 bits in the display unit system control register 1 (DSYSR1) are set to TV synchronized mode, do not set this bit to 0.
27, 26	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
25, 24	PG1D	01	R/W	DRES	<p>Pin Generate 1 Input Data Select</p> <p>Selects the source of input data for pin controller 1.</p> <p>00: Data from superposition processor 0 are input to pin controller 1. For the timing of superposition processor 1, refer to section 21.4.19 (4), Combinations of Blocks for Dual Display Output.</p> <p>01: Data from superposition processor 1 are input to pin controller 1. For the timing of superposition processor 1, refer to section 21.4.19 (4), Combinations of Blocks for Dual Display Output.</p> <p>10: Input to pin controller 1 is fixed to 0. The value of the CDE pin is fixed to 0.</p> <p>11: The value of DOOR1 is input to pin controller 1. The value of the CDE pin is fixed to 0.</p> <p>The combination of the DRES and DEN bits of DSYSR0 determines the data to be superposed.</p> <p>DRES/DEN = 00: The value of DOOR1</p> <p>DRES/DEN = 01: The data in unified memory</p> <p>DRES/DEN = 10: 0</p> <p>DRES/DEN = 11: Setting prohibited (data: 0)</p>
23, 22	—	—	R	—	<p>Reserved</p> <p>The read value is undefined. The write value should always be 0.</p>
21	DR0D	0	R/W	DRES	<p>Display Output Route 0 Data Select</p> <p>0: Data from pin controller 0 are output from the DU0 pins.</p> <p>1: On the DU0 pins, data from pin controller 0 are output on rising edges of the output dot clock and data from pin controller 1 are output on falling edges of the output dot clock. If this setting is made, the frequency of the output dot clock has to be at least half of the frequency of the input dot clock.</p>
20 to 18	—	—	R	—	<p>Reserved</p> <p>The read value is undefined. The write value should always be 0.</p>
17, 16	PG0D	00	R/W	DRES	<p>Pin Generate 0 Input Data Select</p> <p>Selects the source of input data for pin controller 0.</p> <p>00: Data from superposition processor 0 are input to pin controller 0. For the timing of superposition processor 0, refer to section 21.4.19 (4), Combinations of Blocks for Dual Display Output.</p> <p>01: Data from superposition processor 1 are input to pin controller 0. For the timing of superposition processor 1, refer to section 21.4.19 (4), Combinations of Blocks for Dual Display Output.</p> <p>10: Input to pin controller 0 is fixed to 0. The value of the CDE pin is fixed to 0.</p> <p>11: The value of DOOR0 is input to pin controller 0. The value of the CDE pin is fixed to 0.</p> <p>The combination of the DRES and DEN bits of DSYSR0 determines the data to be superposed.</p> <p>DRES/DEN = 00: The value of DOOR0</p> <p>DRES/DEN = 01: The data in unified memory</p> <p>DRES/DEN = 10: 0</p> <p>DRES/DEN = 11: Setting prohibited (data: 0)</p>



Bit	Bit Name	Initial Value	R/W	Internal Update	Description
15 to 5	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
4	RGPV	0	R/W	DRES	R-GP2D V Blank Timing Select [RZ/G1H] 0: The V blank for the R-GP2D is by display-timing generator 0. 1: The V blank for the R-GP2D is by display-timing generator 1.
	—	—		—	Reserved [RZ/G1M/N/E] The read value is undefined. The write value should always be 0.
3 to 1	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
0	DPRS	0	R/W	DRES	Display Priority Register Select 0: The order of priority for the planes is set in DPPR0* <sup>1</sup> /DPPR* <sup>2</sup> . Superposition processor 0 can be used to superpose planes 1 to 8. Superposition processor 1 is not available. 1: The order of priority for the planes is set in DS0PR0* <sup>1</sup> /DS0PR* <sup>2</sup> or DS1PR. Superposition processors 0 and 1 can be used to superpose planes 1 to 8.

Notes: 1. For RZ/G1H.  
2. For RZ/G1M/N/E

**21.3.8.2 Display Unit Output Route Control Register 2 (DORCR2)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	—	—	—

Address: DU2: H'FEB5 1000

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DPRS
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 1	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
0	DPRS	0	R/W	DRES	Display Priority Register Select 0: The order of priority for the planes is set in DPPR2. Superposition processor 2 can be used to superpose planes 1 to 8. Superposition processor 1 is not available. 1: The order of priority for the planes is set in DS0PR2. Superposition processors 2 can be used to superpose planes 1 to 8.

### 21.3.8.3 Display Unit Plane Timing Select Register (DPTSR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address: DU0: H'FEB11004

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	P8DK	P7DK	P6DK	P5DK	P4DK	P3DK	P2DK	P1DK
Initial value:	—	—	—	—	—	—	—	—	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	P8TS	P7TS	P6TS	P5TS	P4TS	P3TS	P2TS	P1TS
Initial value:	—	—	—	—	—	—	—	—	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 24	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
23	P8DK	0	R/W	DRES	Plane 8 Dot Clock Select 0: Dot-clock generator 0 1: Dot-clock generator 1
22	P7DK	0	R/W	DRES	Plane 7 Dot Clock Select 0: Dot-clock generator 0 1: Dot-clock generator 1
21	P6DK	0	R/W	DRES	Plane 6 Dot Clock Select 0: Dot-clock generator 0 1: Dot-clock generator 1
20	P5DK	0	R/W	DRES	Plane 5 Dot Clock Select 0: Dot-clock generator 0 1: Dot-clock generator 1
19	P4DK	0	R/W	DRES	Plane 4 Dot Clock Select 0: Dot-clock generator 0 1: Dot-clock generator 1
18	P3DK	0	R/W	DRES	Plane 3 Dot Clock Select 0: Dot-clock generator 0 1: Dot-clock generator 1
17	P2DK	0	R/W	DRES	Plane 2 Dot Clock Select 0: Dot-clock generator 0 1: Dot-clock generator 1
16	P1DK	0	R/W	DRES	Plane 1 Dot Clock Select 0: Dot-clock generator 0 1: Dot-clock generator 1
15 to 8	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
7	P8TS	0	R/W	DRES	Plane 8 Timing Select 0: Display-timing generator 0 1: Display-timing generator 1
6	P7TS	0	R/W	DRES	Plane 7 Timing Select 0: Display-timing generator 0 1: Display-timing generator 1
5	P6TS	0	R/W	DRES	Plane 6 Timing Select 0: Display-timing generator 0 1: Display-timing generator 1
4	P5TS	0	R/W	DRES	Plane 5 Timing Select 0: Display-timing generator 0 1: Display-timing generator 1
3	P4TS	0	R/W	DRES	Plane 4 Timing Select 0: Display-timing generator 0 1: Display-timing generator 1
2	P3TS	0	R/W	DRES	Plane 3 Timing Select 0: Display-timing generator 0 1: Display-timing generator 1
1	P2TS	0	R/W	DRES	Plane 2 Timing Select 0: Display-timing generator 0 1: Display-timing generator 1
0	P1TS	0	R/W	DRES	Plane 1 Timing Select 0: Display-timing generator 0 1: Display-timing generator 1

**21.3.8.4 Display Unit Alpha Plane Timing Select Register (DAPTSR)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address: DU0: H'FEB11008

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	AP2DK	AP1DK
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	AP2TS	AP1TS
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

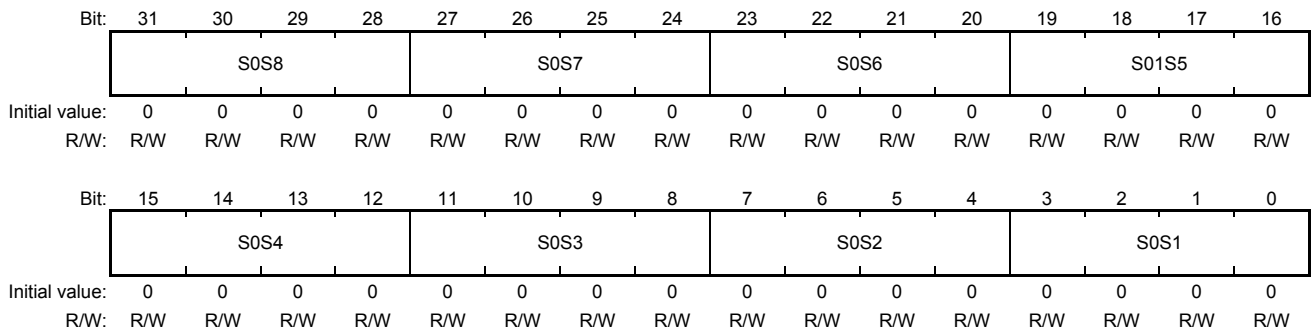
Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 18	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
17	AP2DK	0	R/W	DRES	α Plane 2 Dot Clock Select 0: Dot-clock generator 0 1: Dot-clock generator 1
16	AP1DK	0	R/W	DRES	α Plane 1 Dot Clock Select 0: Dot-clock generator 0 1: Dot-clock generator 1
15 to 2	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
1	AP2TS	0	R/W	DRES	α Plane 2 Timing Select 0: Display-timing generator 0 1: Display-timing generator 1
0	AP1TS	0	R/W	DRES	α Plane 1 Timing Select 0: Display-timing generator 0 1: Display-timing generator 1

**21.3.8.5 Display Superimpose 0 Priority Register m (DS0PRm, m = 0 and 2)**

Note: Suffix "m" as register name and DU2 are only for RZ/G1H.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address: DU0: H'FEB11020, DU2: H'FEB51020 [Only RZ/G1H]



- The setting of this register is valid when the DPRS bit in the display unit output route control register m (DORCRm\*1) is 1.
- After setting a desired value in a register listed in section 21.3.4, Display Plane Registers (Alpha Plane Registers), set DS0PRm to the value indicating the plane number (0001 to 1000).

Notes: 1. m = 0 and 2, suffix "m" as register name is only for RZ/G1H.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 28	S0S8	0000	R/W	Available	<p>Display Superimposition 0 Priority 8 Select</p> <p>0000: Priority level 8 is not used in display generation by superposition processor m.</p> <p>0001: Plane 1 has priority level 8 in display generation by superposition processor m.</p> <p>0010: Plane 2 has priority level 8 in display generation by superposition processor m.</p> <p>0011: Plane 3 has priority level 8 in display generation by superposition processor m.</p> <p>0100: Plane 4 has priority level 8 in display generation by superposition processor m.</p> <p>0101: Plane 5 has priority level 8 in display generation by superposition processor m.</p> <p>0110: Plane 6 has priority level 8 in display generation by superposition processor m.</p> <p>0111: Plane 7 has priority level 8 in display generation by superposition processor m.</p> <p>1000: Plane 8 has priority level 8 in display generation by superposition processor m.</p> <p>Others: Setting prohibited</p>
27 to 24	S0S7	0000	R/W	Available	<p>Display Superimposition 0 Priority 7 Select</p> <p>0000: Priority level 7 is not used in display generation by superposition processor m.</p> <p>0001: Plane 1 has priority level 7 in display generation by superposition processor m.</p> <p>0010: Plane 2 has priority level 7 in display generation by superposition processor m.</p> <p>0011: Plane 3 has priority level 7 in display generation by superposition processor m.</p> <p>0100: Plane 4 has priority level 7 in display generation by superposition processor m.</p> <p>0101: Plane 5 has priority level 7 in display generation by superposition processor m.</p> <p>0110: Plane 6 has priority level 7 in display generation by superposition processor m.</p> <p>0111: Plane 7 has priority level 7 in display generation by superposition processor m.</p> <p>1000: Plane 8 has priority level 7 in display generation by superposition processor m.</p> <p>Others: Setting prohibited</p>

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
23 to 20	S0S6	0000	R/W	Available	<p>Display Superimposition 0 Priority 6 Select</p> <p>0000: Priority level 6 is not used in display generation by superposition processor m.</p> <p>0001: Plane 1 has priority level 6 in display generation by superposition processor m.</p> <p>0010: Plane 2 has priority level 6 in display generation by superposition processor m.</p> <p>0011: Plane 3 has priority level 6 in display generation by superposition processor m.</p> <p>0100: Plane 4 has priority level 6 in display generation by superposition processor m.</p> <p>0101: Plane 5 has priority level 6 in display generation by superposition processor m.</p> <p>0110: Plane 6 has priority level 6 in display generation by superposition processor m.</p> <p>0111: Plane 7 has priority level 6 in display generation by superposition processor m.</p> <p>1000: Plane 8 has priority level 6 in display generation by superposition processor m.</p> <p>Others: Setting prohibited</p>
19 to 16	S0S5	0000	R/W	Available	<p>Display Superimposition 0 Priority 5 Select</p> <p>0000: Priority level 5 is not used in display generation by superposition processor m.</p> <p>0001: Plane 1 has priority level 5 in display generation by superposition processor m.</p> <p>0010: Plane 2 has priority level 5 in display generation by superposition processor m.</p> <p>0011: Plane 3 has priority level 5 in display generation by superposition processor m.</p> <p>0100: Plane 4 has priority level 5 in display generation by superposition processor m.</p> <p>0101: Plane 5 has priority level 5 in display generation by superposition processor m.</p> <p>0110: Plane 6 has priority level 5 in display generation by superposition processor m.</p> <p>0111: Plane 7 has priority level 5 in display generation by superposition processor m.</p> <p>1000: Plane 8 has priority level 5 in display generation by superposition processor m.</p> <p>Others: Setting prohibited</p>



Bit	Bit Name	Initial Value	R/W	Internal Update	Description
15 to 12	S0S4	0000	R/W	Available	<p>Display Superimposition 0 Priority 4 Select</p> <p>0000: Priority level 4 is not used in display generation by superposition processor m.</p> <p>0001: Plane 1 has priority level 4 in display generation by superposition processor m.</p> <p>0010: Plane 2 has priority level 4 in display generation by superposition processor m.</p> <p>0011: Plane 3 has priority level 4 in display generation by superposition processor m.</p> <p>0100: Plane 4 has priority level 4 in display generation by superposition processor m.</p> <p>0101: Plane 5 has priority level 4 in display generation by superposition processor m.</p> <p>0110: Plane 6 has priority level 4 in display generation by superposition processor m.</p> <p>0111: Plane 7 has priority level 4 in display generation by superposition processor m.</p> <p>1000: Plane 8 has priority level 4 in display generation by superposition processor m.</p> <p>Others: Setting prohibited</p>
11 to 8	S0S3	0000	R/W	Available	<p>Display Superimposition 0 Priority 3 Select</p> <p>0000: Priority level 3 is not used in display generation by superposition processor m.</p> <p>0001: Plane 1 has priority level 3 in display generation by superposition processor m.</p> <p>0010: Plane 2 has priority level 3 in display generation by superposition processor m.</p> <p>0011: Plane 3 has priority level 3 in display generation by superposition processor m.</p> <p>0100: Plane 4 has priority level 3 in display generation by superposition processor m.</p> <p>0101: Plane 5 has priority level 3 in display generation by superposition processor m.</p> <p>0110: Plane 6 has priority level 3 in display generation by superposition processor m.</p> <p>0111: Plane 7 has priority level 3 in display generation by superposition processor m.</p> <p>1000: Plane 8 has priority level 3 in display generation by superposition processor m.</p> <p>Others: Setting prohibited</p>

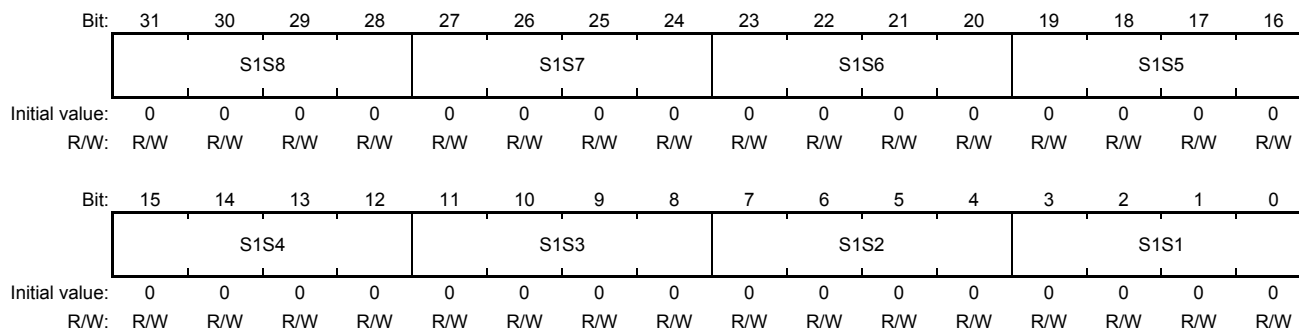
Bit	Bit Name	Initial Value	R/W	Internal Update	Description
7 to 4	S0S2	0000	R/W	Available	<p>Display Superimposition 0 Priority 2 Select</p> <p>0000: Priority level 2 is not used in display generation by superposition processor m.</p> <p>0001: Plane 1 has priority level 2 in display generation by superposition processor m.</p> <p>0010: Plane 2 has priority level 2 in display generation by superposition processor m.</p> <p>0011: Plane 3 has priority level 2 in display generation by superposition processor m.</p> <p>0100: Plane 4 has priority level 2 in display generation by superposition processor m.</p> <p>0101: Plane 5 has priority level 2 in display generation by superposition processor m.</p> <p>0110: Plane 6 has priority level 2 in display generation by superposition processor m.</p> <p>0111: Plane 7 has priority level 2 in display generation by superposition processor m.</p> <p>1000: Plane 8 has priority level 2 in display generation by superposition processor m.</p> <p>Others: Setting prohibited</p>
3 to 0	S0S1	0000	R/W	Available	<p>Display Superimposition 0 Priority 1 Select</p> <p>0000: Priority level 1 is not used in display generation by superposition processor m.</p> <p>0001: Plane 1 has priority level 1 in display generation by superposition processor m.</p> <p>0010: Plane 2 has priority level 1 in display generation by superposition processor m.</p> <p>0011: Plane 3 has priority level 1 in display generation by superposition processor m.</p> <p>0100: Plane 4 has priority level 1 in display generation by superposition processor m.</p> <p>0101: Plane 5 has priority level 1 in display generation by superposition processor m.</p> <p>0110: Plane 6 has priority level 1 in display generation by superposition processor m.</p> <p>0111: Plane 7 has priority level 1 in display generation by superposition processor m.</p> <p>1000: Plane 8 has priority level 1 in display generation by superposition processor m.</p> <p>Others: Setting prohibited</p>

Note: m = 0 and 2 only for RZ/G1H, m = 0 for RZ/G1M/N/E.

### 21.3.8.6 Display Superimpose 1 Priority Register (DS1PR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address: DU1: H'FEB11024



- The setting of this register is valid when the DPRS bit in the display unit output route control register m (DORCRm \*1) is 1.
- After setting a desired value in a register listed in section 21.3.54, Display Plane Registers (Alpha Plane Registers), set DS1PR to the value indicating the plane number (0001 to 1000).

Notes: 1. m = 0 and 2, suffix "m" as register name is only for RZ/G1H.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 28	S1S8	0000	R/W	Available	Display Superimposition 1 Priority 8 Select 0000: Priority level 8 is not used in display generation by superposition processor 1. 0001: Plane 1 has priority level 8 in display generation by superposition processor 1. 0010: Plane 2 has priority level 8 in display generation by superposition processor 1. 0011: Plane 3 has priority level 8 in display generation by superposition processor 1. 0100: Plane 4 has priority level 8 in display generation by superposition processor 1. 0101: Plane 5 has priority level 8 in display generation by superposition processor 1. 0110: Plane 6 has priority level 8 in display generation by superposition processor 1. 0111: Plane 7 has priority level 8 in display generation by superposition processor 1. 1000: Plane 8 has priority level 8 in display generation by superposition processor 1. Others: Setting prohibited

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
27 to 24	S1S7	0000	R/W	Available	<p>Display Superimposition 1 Priority 7 Select</p> <p>0000: Priority level 7 is not used in display generation by superposition processor 1.</p> <p>0001: Plane 1 has priority level 7 in display generation by superposition processor 1.</p> <p>0010: Plane 2 has priority level 7 in display generation by superposition processor 1.</p> <p>0011: Plane 3 has priority level 7 in display generation by superposition processor 1.</p> <p>0100: Plane 4 has priority level 7 in display generation by superposition processor 1.</p> <p>0101: Plane 5 has priority level 7 in display generation by superposition processor 1.</p> <p>0110: Plane 6 has priority level 7 in display generation by superposition processor 1.</p> <p>0111: Plane 7 has priority level 7 in display generation by superposition processor 1.</p> <p>1000: Plane 8 has priority level 7 in display generation by superposition processor 1.</p> <p>Others: Setting prohibited</p>
23 to 20	S1S6	0000	R/W	Available	<p>Display Superimposition 1 Priority 6 Select</p> <p>0000: Priority level 6 is not used in display generation by superposition processor 1.</p> <p>0001: Plane 1 has priority level 6 in display generation by superposition processor 1.</p> <p>0010: Plane 2 has priority level 6 in display generation by superposition processor 1.</p> <p>0011: Plane 3 has priority level 6 in display generation by superposition processor 1.</p> <p>0100: Plane 4 has priority level 6 in display generation by superposition processor 1.</p> <p>0101: Plane 5 has priority level 6 in display generation by superposition processor 1.</p> <p>0110: Plane 6 has priority level 6 in display generation by superposition processor 1.</p> <p>0111: Plane 7 has priority level 6 in display generation by superposition processor 1.</p> <p>1000: Plane 8 has priority level 6 in display generation by superposition processor 1.</p> <p>Others: Setting prohibited</p>

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
19 to 16	S1S5	0000	R/W	Available	<p>Display Superimposition 1 Priority 5 Select</p> <p>0000: Priority level 5 is not used in display generation by superposition processor 1.</p> <p>0001: Plane 1 has priority level 5 in display generation by superposition processor 1.</p> <p>0010: Plane 2 has priority level 5 in display generation by superposition processor 1.</p> <p>0011: Plane 3 has priority level 5 in display generation by superposition processor 1.</p> <p>0100: Plane 4 has priority level 5 in display generation by superposition processor 1.</p> <p>0101: Plane 5 has priority level 5 in display generation by superposition processor 1.</p> <p>0110: Plane 6 has priority level 5 in display generation by superposition processor 1.</p> <p>0111: Plane 7 has priority level 5 in display generation by superposition processor 1.</p> <p>1000: Plane 8 has priority level 5 in display generation by superposition processor 1.</p> <p>Others: Setting prohibited</p>
15 to 12	S1S4	0000	R/W	Available	<p>Display Superimposition 1 Priority 4 Select</p> <p>0000: Priority level 4 is not used in display generation by superposition processor 1.</p> <p>0001: Plane 1 has priority level 4 in display generation by superposition processor 1.</p> <p>0010: Plane 2 has priority level 4 in display generation by superposition processor 1.</p> <p>0011: Plane 3 has priority level 4 in display generation by superposition processor 1.</p> <p>0100: Plane 4 has priority level 4 in display generation by superposition processor 1.</p> <p>0101: Plane 5 has priority level 4 in display generation by superposition processor 1.</p> <p>0110: Plane 6 has priority level 4 in display generation by superposition processor 1.</p> <p>0111: Plane 7 has priority level 4 in display generation by superposition processor 1.</p> <p>1000: Plane 8 has priority level 4 in display generation by superposition processor 1.</p> <p>Others: Setting prohibited</p>

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
11 to 8	S1S3	0000	R/W	Available	<p>Display Superimposition 1 Priority 3 Select</p> <p>0000: Priority level 3 is not used in display generation by superposition processor 1.</p> <p>0001: Plane 1 has priority level 3 in display generation by superposition processor 1.</p> <p>0010: Plane 2 has priority level 3 in display generation by superposition processor 1.</p> <p>0011: Plane 3 has priority level 3 in display generation by superposition processor 1.</p> <p>0100: Plane 4 has priority level 3 in display generation by superposition processor 1.</p> <p>0101: Plane 5 has priority level 3 in display generation by superposition processor 1.</p> <p>0110: Plane 6 has priority level 3 in display generation by superposition processor 1.</p> <p>0111: Plane 7 has priority level 3 in display generation by superposition processor 1.</p> <p>1000: Plane 8 has priority level 3 in display generation by superposition processor 1.</p> <p>Others: Setting prohibited</p>
7 to 4	S1S2	0000	R/W	Available	<p>Display Superimposition 1 Priority 2 Select</p> <p>0000: Priority level 2 is not used in display generation by superposition processor 1.</p> <p>0001: Plane 1 has priority level 2 in display generation by superposition processor 1.</p> <p>0010: Plane 2 has priority level 2 in display generation by superposition processor 1.</p> <p>0011: Plane 3 has priority level 2 in display generation by superposition processor 1.</p> <p>0100: Plane 4 has priority level 2 in display generation by superposition processor 1.</p> <p>0101: Plane 5 has priority level 2 in display generation by superposition processor 1.</p> <p>0110: Plane 6 has priority level 2 in display generation by superposition processor 1.</p> <p>0111: Plane 7 has priority level 2 in display generation by superposition processor 1.</p> <p>1000: Plane 8 has priority level 2 in display generation by superposition processor 1.</p> <p>Others: Setting prohibited</p>

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
3 to 0	S1S1	0000	R/W	Available	<p>Display Superimposition 1 Priority 1 Select</p> <p>0000: Priority level 1 is not used in display generation by superposition processor 1.</p> <p>0001: Plane 1 has priority level 1 in display generation by superposition processor 1.</p> <p>0010: Plane 2 has priority level 1 in display generation by superposition processor 1.</p> <p>0011: Plane 3 has priority level 1 in display generation by superposition processor 1.</p> <p>0100: Plane 4 has priority level 1 in display generation by superposition processor 1.</p> <p>0101: Plane 5 has priority level 1 in display generation by superposition processor 1.</p> <p>0110: Plane 6 has priority level 1 in display generation by superposition processor 1.</p> <p>0111: Plane 7 has priority level 1 in display generation by superposition processor 1.</p> <p>1000: Plane 8 has priority level 1 in display generation by superposition processor 1.</p> <p>Others: Setting prohibited</p>

### 21.3.9 YC-RGB Conversion Coefficient Registers

Registers at addresses H'FEB11080 to H'FEB1109C and H'FEB51080\*<sup>1</sup> to H'FEB5109C\*<sup>1</sup> are for the YC→RGB conversion circuit located in the initial stage of the superposition processor in Figure 21.1.

Registers at addresses FEB14080\*<sup>1</sup> to FEB1409C\*<sup>1</sup> and FEB54080\*<sup>1</sup> to FEB5409C\*<sup>1</sup> are for the YC→RGB conversion circuit located in the latter stage of the superposition processor in Figure 21.1

Notes: 1. For RZ/G1H.

#### 21.3.9.1 Y Normalization Coefficient Register m (YNCRm, m = 0 and 2)

Note: Suffix "m" as register name and DU2 are only for RZ/G1H.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address: DU0: H'FEB11080, H'FEB14080[RZ/G1H], DU2: H'FEB51080 and H'FEB54080

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	YNC1											
Initial value:	—	—	—	—	1	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	YNC0											
Initial value:	—	—	—	—	1	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 28	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
27 to 16	YNC1	H'800	R/W	Available	Y Normalization Coefficient 1 This coefficient is for normalization of Y values in YC-RGB conversion by the YC-RGB conversion generation by superposition processor 1. The coefficient is a fixed-point 12-bit value. The 11th bit represents the integer one or zero and the 10th to 0th bits represent the value below the fixed point. The default value is 1.
15 to 12	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
11 to 0	YNC0	H'800	R/W	Available	Y Normalization Coefficient 0 This coefficient is for normalization of Y values in YC-RGB conversion by the YC-RGB conversion generation by superposition processors 0 and 2*. The coefficient is a fixed-point 12-bit value. The 11th bit represents the integer one or zero and the 10th to 0th bits represent the value below the fixed point. The default value is 1.

Note: \* For RZ/G1H.



### 21.3.9.2 Y Normalization Offset Register m (YNORM, m = 0 and 2)

Note: Suffix "m" as register name and DU2 are only for RZ/G1H.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address: DU0: H'FEB11084, H'FEB14084[RZ/G1H], DU2: H'FEB51084 and H'FEB54084

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	YNO1							
Initial value:	—	—	—	—	—	—	—	—	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	YNO0							
Initial value:	—	—	—	—	—	—	—	—	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 24	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
23 to 16	YNO1	H'00	R/W	Available	Y Normalization Offset 1 This offset is to be subtracted from Y values before they are normalized in YC-RGB conversion by the YC-RGB conversion generation by superposition processor 1. The offset is an unsigned 8-bit integer. Its default value is 0.
15 to 8	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
7 to 0	YNO0	H'00	R/W	Available	Y Normalization Offset 0 This offset is to be subtracted from Y values before they are normalized in YC-RGB conversion by the YC-RGB conversion generation by superposition processors 0 and 2*. The offset is an unsigned 8-bit integer. Its default value is 0.

Note: \* For RZ/G1H.

### 21.3.9.3 Cr Normalization Offset Register m (CRNOR<sub>m</sub>, m = 0 and 2)

Note: Suffix "m" as register name and DU2 are only for RZ/G1H.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address: DU0: H'FEB11088, H'FEB14088[RZ/G1H], DU2: H'FEB51088 and H'FEB54088

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	CRNO1							
Initial value:	—	—	—	—	—	—	—	—	1	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	CRNO0							
Initial value:	—	—	—	—	—	—	—	—	1	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 24	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
23 to 16	CRNO1	H'80	R/W	Available	Cr Normalization Offset 1 This offset is to be subtracted from Cr values before they are normalized in YC-RGB conversion by the YC-RGB conversion generation by superposition processor 1. The offset is an unsigned 8-bit integer. Its default value is 128.
15 to 8	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
7 to 0	CRNO0	H'80	R/W	Available	Cr Normalization Offset 0 This offset is to be subtracted from Cr values before they are normalized in YC-RGB conversion by the YC-RGB conversion generation by superposition processors 0 and 2*. The offset is an unsigned 8-bit integer. Its default value is 128.

Note: \* For RZ/G1H

### 21.3.9.4 Cb Normalization Offset Register m (CBNORM, m = 0 and 2)

Note: Suffix "m" as register name and DU2 are only for RZ/G1H.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address: DU0: H'FEB1108C, H'FEB1408C[RZ/G1H], DU2: H'FEB5108C and H'FEB5408C

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	CBNO1							
Initial value:	—	—	—	—	—	—	—	—	1	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	CBNO0							
Initial value:	—	—	—	—	—	—	—	—	1	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 24	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
23 to 16	CBNO1	H'80	R/W	Available	Cb Normalization Offset 1 This offset is to be subtracted from Cb values before they are normalized in YC-RGB conversion by the YC-RGB conversion generation by superposition processor 1. The offset is an unsigned 8-bit integer. Its default value is 128.
15 to 8	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
7 to 0	CBNO0	H'80	R/W	Available	Cb Normalization Offset 0 This offset is to be subtracted from Cb values before they are normalized in YC-RGB conversion by the YC-RGB conversion generation by superposition processors 0 and 2*. The offset is an unsigned 8-bit integer. Its default value is 128.

Note: \* For RZ/G1H.

### 21.3.9.5 Red Cr Coefficient Register m (RCRCRm, m = 0 and 2)

Note: Suffix "m" as register name and DU2 are only for RZ/G1H.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address: DU0: H'FEB11090, H'FEB14090[RZ/G1H], DU2: H'FEB51090 and H'FEB54090

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	RCRC1											
Initial value:	—	—	—	—	1	0	1	0	1	1	1	1	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	RCRC0											
Initial value:	—	—	—	—	1	0	1	0	1	1	1	1	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 28	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
27 to 16	RCRC1	H'AF0	R/W	Available	Red Cr Coefficient 1 Cr is multiplied by this coefficient to create the red component in YC-RGB conversion by the YC-RGB conversion generation by superposition processor 1. The coefficient is a fixed-point 12-bit value. The 11th bit represents the integer one or zero and the 10th to 0th bits represent the value below the fixed point. The default value is 1.37.
15 to 12	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
11 to 0	RCRC0	H'AF0	R/W	Available	Red Cr Coefficient 0 Cr is multiplied by this coefficient to create the red component in YC-RGB conversion by the YC-RGB conversion generation by superposition processors 0 and 2*. The coefficient is a fixed-point 12-bit value. The 11th bit represents the integer one or zero and the 10th to 0th bits represent the value below the fixed point. The default value is 1.37.

Note: \* For RZ/G1H.

### 21.3.9.6 Green Cr Coefficient Register m (GCRCRm, m = 0 and 2)

Note: Suffix "m" as register name and DU2 are only for RZ/G1H.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address: DU0: H'FEB11094, H'FEB14094[RZ/G1H], DU2: H'FEB51094 and H'FEB54094

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	GCRC1											
Initial value:	—	—	—	—	0	1	0	1	1	0	0	1	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	GCRC0											
Initial value:	—	—	—	—	0	1	0	1	1	0	0	1	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 28	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
27 to 16	GCRC1	H'590	R/W	Available	Green Cr Coefficient 1 Cr is multiplied by this coefficient to create the green component in YC-RGB conversion by the YC-RGB conversion generation by superposition processor 1. The coefficient is a fixed-point 12-bit value. The 11th bit represents the integer one or zero and the 10th to 0th bits represent the value below the fixed point. The default value is 0.698.
15 to 12	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
11 to 0	GCRC0	H'590	R/W	Available	Green Cr Coefficient 0 Cr is multiplied by this coefficient to create the green component in YC-RGB conversion by the YC-RGB conversion generation by superposition processors 0 and 2*. The coefficient is a fixed-point 12-bit value. The 11th bit represents the integer one or zero and the 10th to 0th bits represent the value below the fixed point. The default value is 0.698.

Note: \* For RZ/G1H.

### 21.3.9.7 Green Cb Coefficient Register m (GCBCRm, m = 0 and 2)

Note: Suffix "m" as register name and DU2 are only for RZ/G1H.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address: DU0: H'FEB11098, H'FEB14098[RZ/G1H], DU2: H'FEB51098 and H'FEB54098

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	GCBC1											
Initial value:	—	—	—	—	0	0	1	0	1	0	1	1	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	GCBC0											
Initial value:	—	—	—	—	0	0	1	0	1	0	1	1	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 28	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
27 to 16	GCBC1	H'2B0	R/W	Available	Green Cb Coefficient 1 Cb is multiplied by this coefficient to create the green component in YC-RGB conversion by the YC-RGB conversion generation by superposition processor 1. The coefficient is a fixed-point 12-bit value. The 11th bit represents the integer one or zero and the 10th to 0th bits represent the value below the fixed point. The default value is 0.336.
15 to 12	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
11 to 0	GCBC0	H'2B0	R/W	Available	Green Cb Coefficient 0 Cb is multiplied by this coefficient to create the green component in YC-RGB conversion by the YC-RGB conversion generation by superposition processors 0 and 2*. The coefficient is a fixed-point 12-bit value. The 11th bit represents the integer one or zero and the 10th to 0th bits represent the value below the fixed point. The default value is 0.336.

Note: \* For RZ/G1H.

### 21.3.9.8 Blue Cb Coefficient Register m (BCBCRm, m = 0 and 2)

Note: Suffix "m" as register name and DU2 are only for RZ/G1H.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address: DU0: H'FEB1109C, H'FEB1409C[RZ/G1H], DU2: H'FEB5109C and H'FEB5409C

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	BCBC1											
Initial value:	—	—	—	—	1	1	0	1	1	1	1	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	BCBC0											
Initial value:	—	—	—	—	1	1	0	1	1	1	1	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 28	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
27 to 16	BCBC1	H'DE0	R/W	Available	Blue Cb Coefficient 1 Cb is multiplied by this coefficient to create the blue component in YC-RGB conversion by the YC-RGB conversion generation by superposition processor 1. The coefficient is a fixed-point 12-bit value. The 11th bit represents the integer one or zero and the 10th to 0th bits represent the value below the fixed point. The default value is 1.73.
15 to 12	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
11 to 0	BCBC0	H'DE0	R/W	Available	Blue Cb Coefficient 0 Cb is multiplied by this coefficient to create the blue component in YC-RGB conversion by the YC-RGB conversion generation by superposition processors 0 and 2*. The coefficient is a fixed-point 12-bit value. The 11th bit represents the integer one or zero and the 10th to 0th bits represent the value below the fixed point. The default value is 1.73.

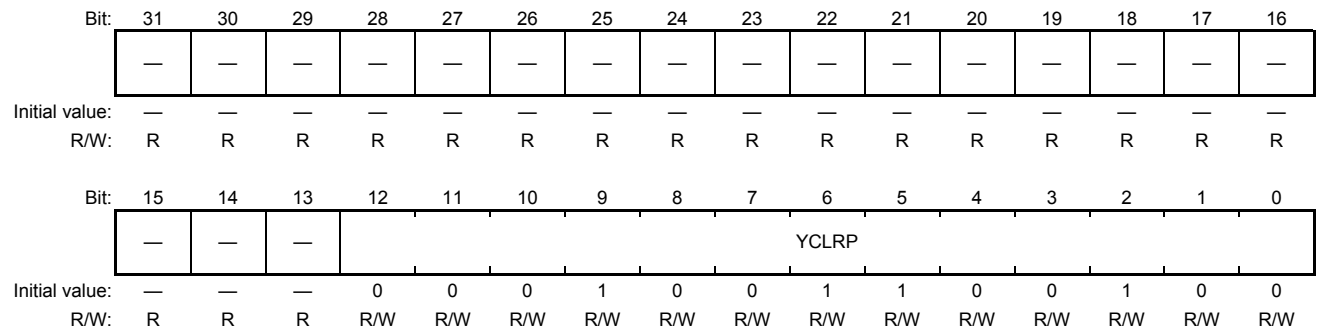
Note: \* For RZ/G1H.

**21.3.10 RGB-YC Conversion Coefficient Registers**

**21.3.10.1 Y Calculation R Coefficient Register (YCLRP)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
—	√	√	√

Address: DU0: H'FEB14000



Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 13	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
12 to 0	YCLRP	H'0264	R/W	Available	Y Calculation R Coefficient This coefficient is for R to generate the Y values in RGB-YC conversion by the RGB-YC conversion circuit. The default value is H'264. The coefficient is a 13-bit value of 1 sign bit + 12 fixed-point bits. The 12th bit represents the sign, the 11th bit represents the integer, and the 10th to 0th bits represent the value below the fixed point. 12th sign bit 0: + 1: - 11th to 0th bits A fixed-point absolute value should be set.



**21.3.10.2 Y Calculation G Coefficient Register (YCLGP)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
—	√	√	√

Address: DU0: H'FEB14004

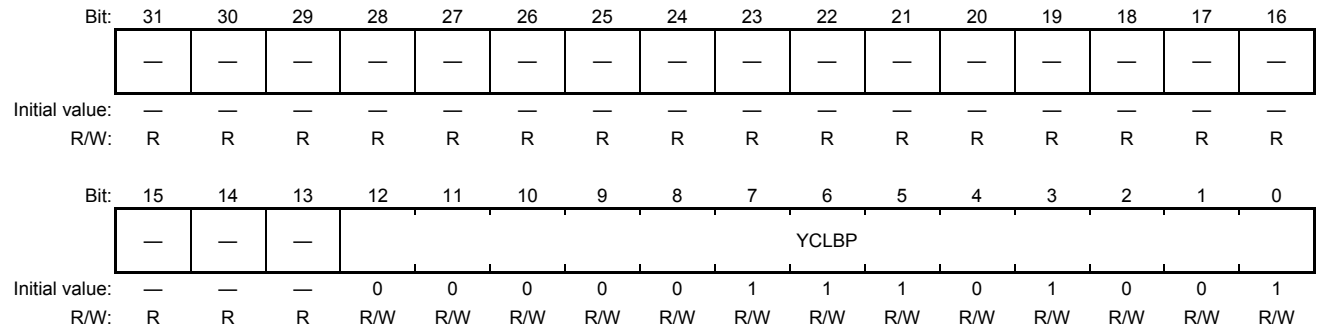
Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	YCLGP												
Initial value:	—	—	—	0	0	1	0	0	1	0	1	1	0	0	1	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 13	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
12 to 0	YCLGP	H'04B2	R/W	Available	<p>Y Calculation G Coefficient</p> <p>This coefficient is for G to generate the Y values in RGB-YC conversion by the RGB-YC conversion circuit. The default value is H'4B2.</p> <p>The coefficient is a 13-bit value of 1 sign bit + 12 fixed-point bits. The 12th bit represents the sign, the 11th bit represents the integer, and the 10th to 0th bits represent the value below the fixed point.</p> <p>12th sign bit</p> <p>0: +</p> <p>1: -</p> <p>11th to 0th bits</p> <p>A fixed-point absolute value should be set.</p>

**21.3.10.3 Y Calculation B Coefficient Register (YCLBP)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
—	√	√	√

Address: DU0: H'FEB14008



Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 13	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
12 to 0	YCLBP	H'00E9	R/W	Available	<p>Y Calculation B Coefficient</p> <p>This coefficient is for B to generate the Y values in RGB-YC conversion by the RGB-YC conversion circuit. The default value is H'E9.</p> <p>The coefficient is a 13-bit value of 1 sign bit + 12 fixed-point bits. The 12th bit represents the sign, the 11th bit represents the integer, and the 10th to 0th bits represent the value below the fixed point.</p> <p>12th sign bit</p> <p>0: +</p> <p>1: -</p> <p>11th to 0th bits</p> <p>A fixed-point absolute value should be set.</p>

**21.3.10.4 Y Calculation Addition Constant Register (YCLAP)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
—	√	√	√

Address: DU0: H'FEB1400C

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	YCLAP							
Initial value:	—	—	—	—	—	—	—	—	0	0	0	1	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 8	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
7 to 0	YCLAP	H'10	R/W	Available	Y Calculation Addition Constant This addition constant is used to generate the Y values in RGB-YC conversion by the RGB-YC conversion circuit. This addition constant is an unsigned 8-bit integer. The default value is H'10.

### 21.3.10.5 Cb Calculation R Coefficient Register (CBCLRP)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
—	√	√	√

Address: DU0: H'FEB14010

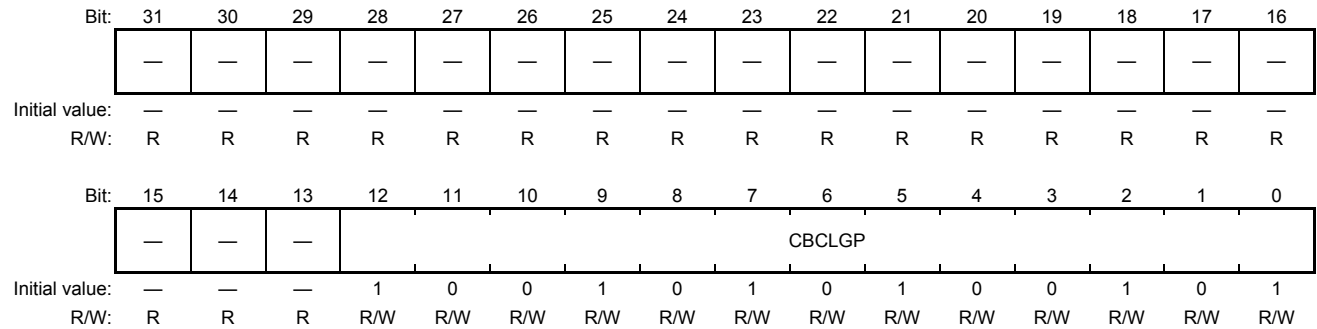
Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	CBCLRP												
Initial value:	—	—	—	1	0	0	0	1	0	1	0	1	1	0	1	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 13	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
12 to 0	CBCLR P	H'115A	R/W	Available	<p>Cb Calculation R Coefficient</p> <p>This coefficient is for R to generate the Cb values in RGB-YC conversion by the RGB-YC conversion circuit. The default value is H'115A.</p> <p>The coefficient is a 13-bit value of 1 sign bit + 12 fixed-point bits. The 12th bit represents the sign, the 11th bit represents the integer, and the 10th to 0th bits represent the value below the fixed point.</p> <p>12th sign bit</p> <p>0: +</p> <p>1: -</p> <p>11th to 0th bits</p> <p>A fixed-point absolute value should be set.</p>

**21.3.10.6 Cb Calculation G Coefficient Register (CBCLGP)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
—	√	√	√

Address: DU0: H'FEB14014



Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 13	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
12 to 0	CBCLGP	H'12A5	R/W	Available	<p>Cb Calculation G Coefficient</p> <p>This coefficient is for G to generate the Cb values in RGB-YC conversion by the RGB-YC conversion circuit. The default value is H'12A5.</p> <p>The coefficient is a 13-bit value of 1 sign bit + 12 fixed-point bits. The 12th bit represents the sign, the 11th bit represents the integer, and the 10th to 0th bits represent the value below the fixed point.</p> <p>12th sign bit</p> <p>0: +</p> <p>1: -</p> <p>11th to 0th bits</p> <p>A fixed-point absolute value should be set.</p>

### 21.3.10.7 Cb Calculation B Coefficient Register (CBCLBP)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
—	√	√	√

Address: DU0: H'FEB14018

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	CBCLBP												
Initial value:	—	—	—	0	0	1	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 13	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
12 to 0	CBCLBP	H'0400	R/W	Available	<p>Cb Calculation B Coefficient</p> <p>This coefficient is for B to generate the Cb values in RGB-YC conversion by the RGB-YC conversion circuit. The default value is H'400.</p> <p>The coefficient is a 13-bit value of 1 sign bit + 12 fixed-point bits. The 12th bit represents the sign, the 11th bit represents the integer, and the 10th to 0th bits represent the value below the fixed point.</p> <p>12th sign bit</p> <p>0: +</p> <p>1: -</p> <p>11th to 0th bits</p> <p>A fixed-point absolute value should be set.</p>

**21.3.10.8 Cb Calculation Addition Constant Register (CBCLAP)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
—	√	√	√

Address: DU0: H'FEB1401C

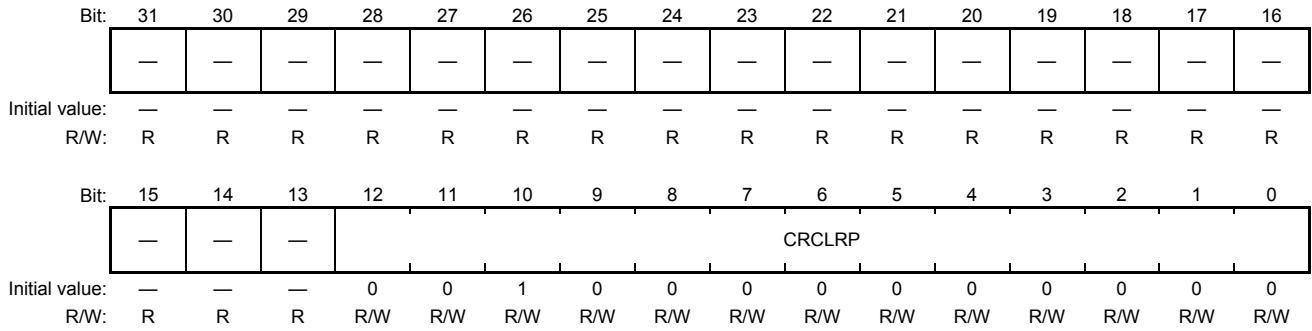
Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	CBCLAP							
Initial value:	—	—	—	—	—	—	—	—	1	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 8	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
7 to 0	CBCLAP	H'80	R/W	Available	Cb Calculation Addition Constant This addition constant is used to generate the Cb values in RGB-YC conversion by the RGB-YC conversion circuit. This addition constant is an unsigned 8-bit integer. The default value is H'80.

**21.3.10.9 Cr Calculation R Coefficient Register (CRCLRP)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
—	√	√	√

**Address: DU0: H'FEB14020**



Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 13	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
12 to 0	CRCLR P	H'0400	R/W	Available	Cr Calculation R Coefficient This coefficient is for R to generate the Cr values in RGB-YC conversion by the RGB-YC conversion circuit. The default value is H'400. The coefficient is a 13-bit value of 1 sign bit + 12 fixed-point bits. The 12th bit represents the sign, the 11th bit represents the integer, and the 10th to 0th bits represent the value below the fixed point. 12th sign bit 0: + 1: - 11th to 0th bits A fixed-point absolute value should be set.



**21.3.10.10 Cr Calculation G Coefficient Register (CRCLGP)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
—	√	√	√

Address: DU0: H'FEB14024

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	CRCLGP												
Initial value:	—	—	—	1	0	0	1	1	0	1	0	1	1	0	1	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 13	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
12 to 0	CRCLGP	H'135A	R/W	Available	Cr Calculation G Coefficient This coefficient is for G to generate the Cr values in RGB-YC conversion by the RGB-YC conversion circuit. The default value is H'135A. The coefficient is a 13-bit value of 1 sign bit + 12 fixed-point bits. The 12th bit represents the sign, the 11th bit represents the integer, and the 10th to 0th bits represent the value below the fixed point. 12th sign bit 0: + 1: - 11th to 0th bits A fixed-point absolute value should be set.

### 21.3.10.11 Cr Calculation B Coefficient Register (CRCLBP)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
—	√	√	√

Address: DU0: H'FEB14028

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	CRCLBP												
Initial value:	—	—	—	1	0	0	0	0	1	0	1	0	0	1	0	1
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 13	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
12 to 0	CRCLBP	H'10A5	R/W	Available	<p>Cr Calculation B Coefficient</p> <p>This coefficient is for B to generate the Cr values in RGB-YC conversion by the RGB-YC conversion circuit. The default value is H'10A5.</p> <p>The coefficient is a 13-bit value of 1 sign bit + 12 fixed-point bits. The 12th bit represents the sign, the 11th bit represents the integer, and the 10th to 0th bits represent the value below the fixed point.</p> <p>12th sign bit</p> <p>0: +</p> <p>1: -</p> <p>11th to 0th bits</p> <p>A fixed-point absolute value should be set.</p>

**21.3.10.12 Cr Calculation Addition Constant Register (CRCLAP)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
—	√	√	√

Address: DU0: H'FEB1402C

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	CRCLAP							
Initial value:	—	—	—	—	—	—	—	—	1	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 8	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
7 to 0	CRCLAP	H'80	R/W	Available	Cr Calculation Addition Constant This addition constant is used to generate the Cr values in RGB-YC conversion by the RGB-YC conversion circuit. This addition constant is an unsigned 8-bit integer. The default value is H'80.

## 21.4 Display Function

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

Note: From section 21.4 on, descriptions of suffixes n and m are provided as the last paragraph or a note for the last table in each subsection.

### 21.4.1 Configuration of Output Screen

The display unit (DU) executes window displays with up to a maximum of eight window layers. Each of these windows is called a "plane", and the order of stacking of the planes can be set arbitrarily. For each plane, display can be turned on and off, and the display data format (8-bit/pixel, 16-bit/pixel, 32-bit/pixel, ARGB, YC), blending functions, and other settings can be changed independently. In addition to the window display plane, a plane that is dedicated to the  $\alpha$  value can be synthesized (a maximum of one layer).

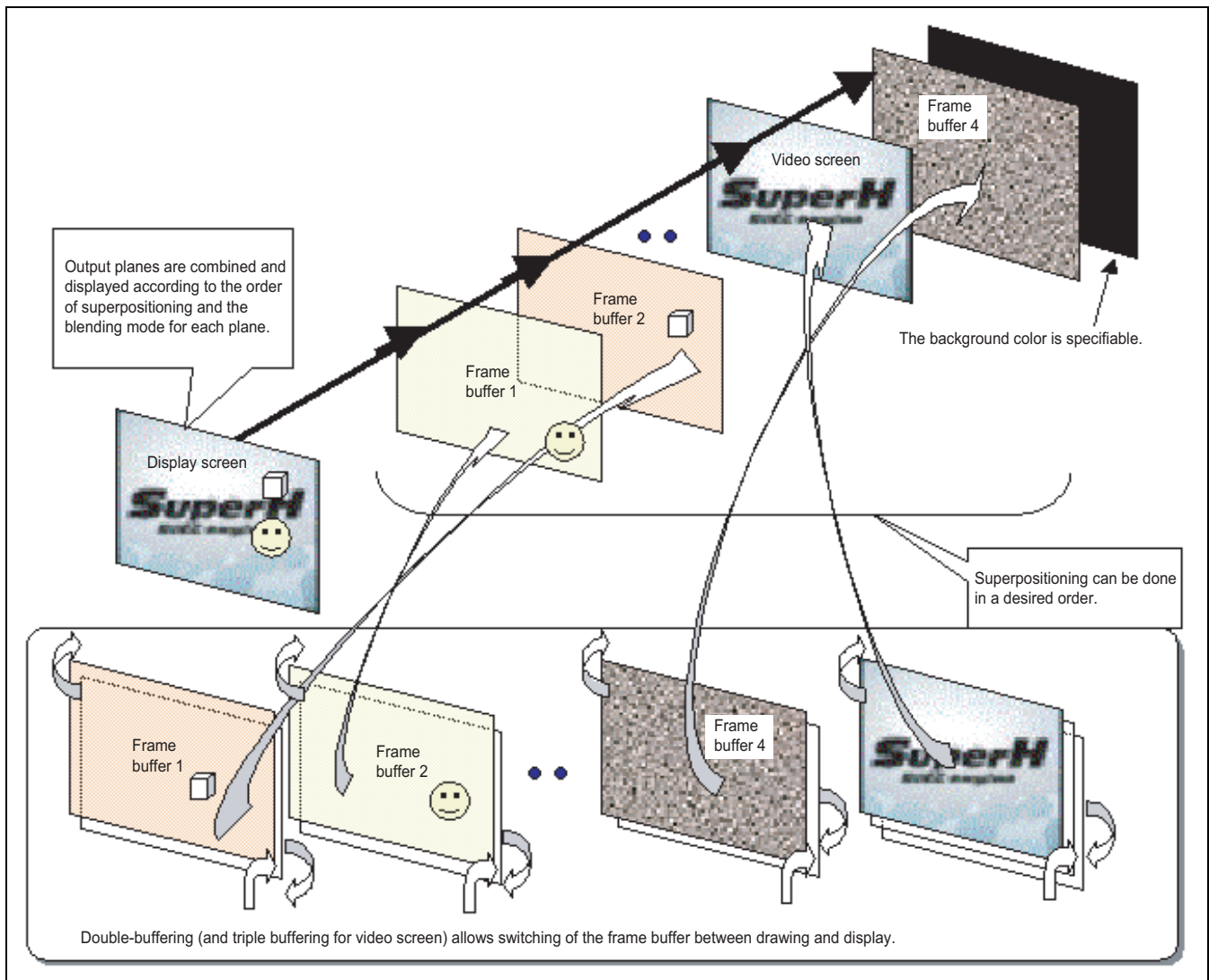
Each plane has a double-buffer configuration (triple buffer only for a video capture plane), so that smooth display is possible.

Note: In cases of high-resolution display, the unified memory traffic volume may be considerable depending on the number of combined planes and display size, and constraints may arise owing to the traffic volume; but there are no constraints on display functions.

**Table 21.26 Display Functions of Planes**

	Display On/Off	Display Data Format					Super-positioning	Blinking	Size	Scroll-ing	Wrap-around	$\alpha$ -Ratio Plane
		8-bit/pixel	16-bit/pixel	ARGB	YC	32-bit/pixel						
Plane 1	✓	✓*1	✓	✓	✓*2	✓*4	$\alpha$ blending/ transparent color*4/ EOR operation	✓	X, Y (as desired)	✓	✓	✓
Plane 2	✓	✓*1	✓	✓	✓*2	✓*4	Same as above	✓	Same as above	✓	✓	✓
Plane 3	✓	✓*1	✓	✓	✓*2	✓*4	Same as above	✓	Same as above	✓	✓	✓
Plane 4	✓	✓*1	✓	✓	✓*2	✓*4	Same as above	✓	Same as above	✓	✓	✓
Plane 5	✓	✓*1	✓	✓	✓	✓*4	Same as above	✓	Same as above	✓	✓	✓
Plane 6	✓	✓*1	✓	✓	✓	✓*4	Same as above	✓	Same as above	✓	✓	✓
Plane 7	✓	✓*1	✓	✓	✓	✓*4	Same as above	✓	Same as above	✓	✓	✓
Plane 8	✓	✓*1	✓	✓	✓	✓*4	Same as above	✓	Same as above	✓	✓	✓
$\alpha$ plane 1	✓	✓	—	—	—	—	—	✓	Same as above	✓	✓	✓
$\alpha$ plane 2	✓	✓	—	—	—	—	—	✓	Same as above	✓	✓	✓
Back-ground color*3	—	—	—	—	—	—	—	—	—	—	—	—

- Notes:
1. Any among color palettes 1, 2, 3, and 4 is selected.
  2. YC→RGB conversion can be performed only for the YUV data of the uppermost plane.
  3. The data format for background color is RGB666.
  4. Transparent color processing is not possible for a 32-bit/pixel display specified with the PnLRGB1 or PnLRGB0 bit in PnDDCRm. Transparent color processing is possible when the PnEDF bits in PnDDC4Rm are used to specify a 32-bit/pixel display.
  5.  $m = 0$  and 2, suffix "m" is only for RZ/G1H.  
 $n = 1$  to 8.



**Figure 21.2 Block Diagram of Plane Configuration and Superpositioning**

### 21.4.2 Display On/Off

All plane display can be turned on and off using the DEN bit in DSYSRm\*<sup>1</sup>. When the DEN bit is 0, the display data set in DOORn\*<sup>2</sup> is displayed.

When the value of the DPRS bit in DORCRm\*<sup>3</sup> is 0, DPPRm\*<sup>3</sup> is used to turn the display of planes 1 to 8 on and off. When the value of the DPRS bit in DORCRm\*<sup>3</sup> is 1, on the other hand, DS0PRm\*<sup>3</sup> and DS1PR are used to turn the display of planes 1 to 8 on and off. Under the following display conditions, display data set in BPORn\*<sup>2</sup> is displayed.

1. When display of all planes 1 to 8 is turned off
2. In an area with no plane for display, due to the display size and display position
3. When the pixels in a plane for display are all a transparent color

**Table 21.27 Turning On and Off the Display of Planes 1 to 8 (when the DPRS Bit of DORCRm\*<sup>3</sup> is 0)**

Display Plane	Display Plane Priority Register m (DPPRm* <sup>3</sup> )
Plane 1	Plane 1 is selected in one among priority positions 1 to 8, and the corresponding enable bit is set to 1
Plane 2	Plane 2 is selected in one among priority positions 1 to 8, and the corresponding enable bit is set to 1
Plane 3	Plane 3 is selected in one among priority positions 1 to 8, and the corresponding enable bit is set to 1
Plane 4	Plane 4 is selected in one among priority positions 1 to 8, and the corresponding enable bit is set to 1
Plane 5	Plane 5 is selected in one among priority positions 1 to 8, and the corresponding enable bit is set to 1
Plane 6	Plane 6 is selected in one among priority positions 1 to 8, and the corresponding enable bit is set to 1
Plane 7	Plane 7 is selected in one among priority positions 1 to 8, and the corresponding enable bit is set to 1
Plane 8	Plane 8 is selected in one among priority positions 1 to 8, and the corresponding enable bit is set to 1

**Table 21.28 Turning On and Off the Display of Planes 1 to 8 (when the DPRS Bit of DORCRm\*<sup>3</sup> is 1)**

Display Plane	Display Superimpose 0 Priority Register m (DS0PRm* <sup>3</sup> ) Display Superimpose 1 Priority Register (DS1PR)
Plane 1	Plane 1 is selected in one among priority positions 1 to 8 (setting to select the plane: 0001)
Plane 2	Plane 2 is selected in one among priority positions 1 to 8 (setting to select the plane: 0010)
Plane 3	Plane 3 is selected in one among priority positions 1 to 8 (setting to select the plane: 0011)
Plane 4	Plane 4 is selected in one among priority positions 1 to 8 (setting to select the plane: 0100)
Plane 5	Plane 5 is selected in one among priority positions 1 to 8 (setting to select the plane: 0101)
Plane 6	Plane 6 is selected in one among priority positions 1 to 8 (setting to select the plane: 0110)
Plane 7	Plane 7 is selected in one among priority positions 1 to 8 (setting to select the plane: 0111)
Plane 8	Plane 8 is selected in one among priority positions 1 to 8 (setting to select the plane: 1000)

Note: Even if display on is set using DPPRm\*<sup>3</sup>, DS0PRm\*<sup>3</sup>, or DS1PR under the following conditions, the setting is handled as display off, and the corresponding plane is not displayed.

- Planes for which the value set in PnDPXRm\*<sup>4</sup> is greater than the screen size (horizontal display end (HDE) - horizontal display start (HDS))
- Planes for which the value set in PnDPYRm\*<sup>4</sup> is greater than the screen size (vertical display end (VDE) - vertical display start (VDS))
- Planes for which the value set in PnDSXRm\*<sup>4</sup> is 0
- Planes for which the value set in PnDSYRm\*<sup>4</sup> is 0
- Planes for which the value set in PnMWRm\*<sup>4</sup> is 0
- Planes for which the value set in PnSPXRm\*<sup>4</sup> is equal to or greater than twice the value set in PnMWRm\*<sup>4</sup>

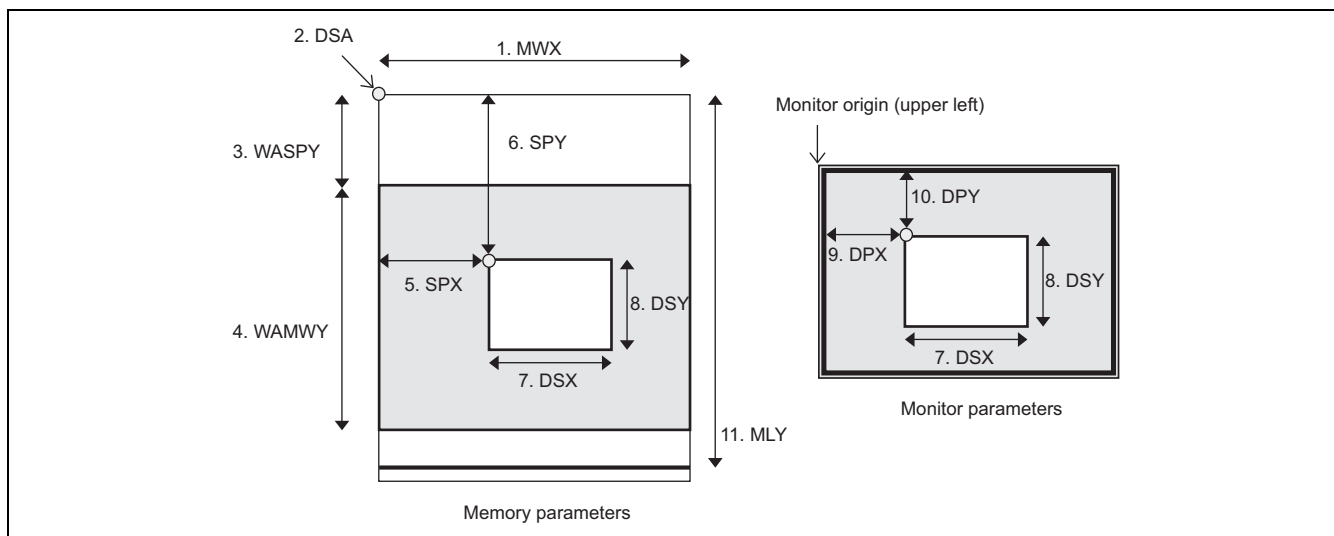
1. m = 0 and 2 for RZ/G1H, m = 0 for RZ/G1M/N/E

2. n = 0 to 2 for RZ/G1H, n = 0 and 1 for RZ/G1M/N/E
3. m = 0 and 2, suffix “m” is only for RZ/G1H.
4. m = 0 and 2, suffix “m” is only for RZ/G1H. n = 1 to 8

### 21.4.3 Plane Parameter

For each plane, a display area start position, memory width, display start position, and display size are set using registers.

The followings are the schematic diagram of start positions and sizes related to planes and the registers used for setting start positions and sizes.



**Figure 21.3 Parameters**

**Table 21.29 Memory Parameter/Monitor Parameter Setting Registers**

No.	Name Used in the Figure	Register	Description
1	MWX (Plane memory width)	PnMWRm*	The plane X-direction memory width is set between 16 and 4096 pixels, in 16 pixel units.
2	DSA (Display area start address)	PnDSA0Rm* to PnDSA2Rm*	The start address in memory area is set for plane.
3	WASPY (Wrap-around start position)	PnWASPRm*	The Y direction start position of the wrap-around area is set in line units, with the address set by DSA as reference.
4	WAMWY (Wrap-around memory width)	PnWAMWRm*	The wrap-around Y-direction memory width is set to a desired value in the range from 240 to 4095 (representing line units).
5	SPX (Start position X)	PnSPXRm*	The distance in the X direction to the display start position is set in pixel units, taking the address set by DSA as the origin.
6	SPY (Start position Y)	PnSPYRm*	The distance in the Y direction to the display start position is set in raster line units, taking the address set by DSA as the origin.
7	DSX (Display size X)	PnDSXRm*	The X-direction display size of plane is set in dot-clock units.
8	DSY (Display size Y)	PnDSYRm*	The Y-direction display size of plane is set in raster line units.
9	DPX (Display position X)	PnDPXRm*	The X-direction distance to the display position is set in dot-clock units, taking the upper-left corner of the monitor as the origin.
10	DPY (Display position Y)	PnDPYRm*	The Y-direction distance to the display position is set in raster line units, taking the upper-left corner of the monitor as the origin.
11	MLY (Memory length Y)	PnMLRm*	The Y-direction memory area of plane is set in line units.

Note: m = 0 and 2 for RZ/G1H, suffix "m" is only for RZ/G1H  
n = 1 to 8



#### 21.4.4 Memory Allocation

A display start address for the display screen, drawing screen 1, and drawing screen 2 used for video display can be set individually for each plane. The start addresses for the memory areas used are set in each of the display area start address registers.

In the display unit (DU), when the display plane is video captured, the display area start addresses 0, 1, and 2 for each plane are used to perform triple-buffering control and display the plane. When the display plane is not video captured, the display area start addresses 0 and 1 for each plane are used to perform double-buffering control and display the plane.

The double-buffering control can be performed for alpha planes. In display capture, only a single area can be set to store the data.

Below is a list of display area start address registers used for each of the planes.

**Table 21.30 Memory Allocation Registers**

Display Screen	Register Name	
Plane n	Plane n display area start address 0 register o	PnDSA0Ro
	Plane n display area start address 1 register o	PnDSA1Ro
	Plane n display area start address 2 register o	PnDSA2Ro
$\alpha$ plane m	Alpha plane m display area start address 0 register o	APmDSA0Ro
	Alpha plane m display area start address 1 register o	APmDSA1Ro
Display capture	Display capture area start address register o	DCSARo
Display capture 2	Display capture 2 area start address register p	DC2SARp

Notes: n = 1 to 8.

m = 1 and 2.

o = 0 and 2 for RZ/G1H, suffix "o" is only for RZ/G1H

p = 0 for RZ/G1H, suffix "p" is only for RZ/G1H.

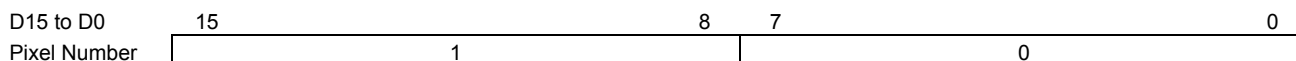
### 21.4.5 Display Data Format

The following format is used for color data used in display. A data configuration is shown in which data is allocated to the unified memory in little endian.

#### (1) 8-bit/pixel

A color palette index is used. The color palette is used to convert and display image data into RGB data with 6 bits for each RGB color (RGB666).

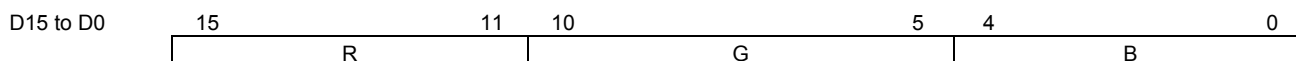
#### 8-bit/pixel data (index color)



#### (2) 16-bit/pixel: RGB

The RGB levels are represented using 5 bits for R, 6 bits for G, and 5 bits for B (RGB565).

#### 16-bit/pixel data (RGB data) format

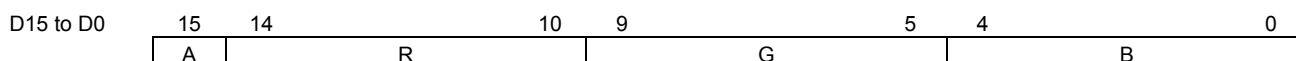


#### (3) 16-bit/pixel: ARGB

Levels for A, R, G, and B are represented by 1, 5, 5, and 5 bits respectively (ARGB1555). In addition to the R, G, and B values, this format includes a bit that represents  $\alpha$  blending control. In this section, "ARGB" indicates ARGB1555 and "ARGB8888" indicates the 32-bit/pixel format unless otherwise specified.

$\alpha$  blending control using the A value is valid when the PnSPIM\* bit in PnMRm\* is set to perform  $\alpha$  blending. When the PnABIT\* bits of PnALPHARm\* are B'00,  $\alpha$  blending is performed when A = 1. When the PnABIT\* bits are B'01,  $\alpha$  blending is performed when A = 0. When the PnABIT\* bits are B'10 or B'11,  $\alpha$  blending is performed regardless of the A value. When the PnSPIM\* bit is not set to perform  $\alpha$  blending,  $\alpha$  blending is not performed regardless of the A value.

#### 16-bit/pixel data (ARGB data) format



#### (4) YC: YUV422

Image data has the format YC (YCbCr) = 4:2:2. A calculation circuit is used to convert each of the 8 bits of the RGB colors (RGB888) of image data. Transparent color processing is not possible.

The YC data order corresponds to the UYVY format and YUYV format. The UYVY format and YUYV format can be selected using the PnYCDF\* bits in PnMRm\*.

The formulae for YC-RGB conversion are given below. The underlined coefficients are defined by the settings in the corresponding registers.

$$\begin{aligned}
 R &= \underline{YNC} \times (Y - \underline{YNO}) + \underline{RCRC} \times (Cr - \underline{CRNO}) \\
 G &= \underline{YNC} \times (Y - \underline{YNO}) - \underline{GCRCR} \times (Cr - \underline{CRNO}) - \underline{GCBC} \times (Cb - \underline{CBNO}) \\
 B &= \underline{YNC} \times (Y - \underline{YNO}) + \underline{BCBC} \times (Cb - \underline{CBNO})
 \end{aligned}$$

The formulae for YC-RGB conversion in the default state are thus as follows.

$$R = Y + 1.37 \times (Cr - 128)$$

$$G = Y - 0.698 \times (Cr - 128) - 0.336 \times (Cb - 128)$$

$$B = Y + 1.73 \times (Cb - 128)$$

**(a) UYVY format**

D63 to D48	63	56	55	48
Image data 3 and 4	Y3		V2	
D47 to D32	47	40	39	32
Image data 3 and 4	Y2		U2	
D31 to D16	31	24	23	16
Image data 1 and 2	Y1		V0	
D15 to D0	15	8	7	0
Image data 1 and 2	Y0		U0	

**(b) YUYV format**

D63 to D48	63	56	55	48
Image data 3 and 4	V2		Y3	
D47 to D32	47	40	39	32
Image data 3 and 4	U2		Y2	
D31 to D16	31	24	23	16
Image data 1 and 2	V0		Y1	
D15 to D0	15	8	7	0
Image data 1 and 2	U0		Y0	

**(c) RGB color-space conversion format**

Image data 4	23	16	15	8	7	0
	Y3		U2		V2	
Image data 3	23	16	15	8	7	0
	Y2		U2		V2	
Image data 2	23	16	15	8	7	0
	Y1		U0		V0	
Image data 1	23	16	15	8	7	0
	Y0		U0		V0	

**(5) YC: YUV420**

Image data has the format YC (YCbCr) = 4:2:0. A calculation circuit is used to convert each of the 8 bits of the RGB colors (RGB888) of image data. Transparent color processing is not possible.

The UV data order corresponds to the NV12 format and NV21 format. The NV12 format and NV21 format can be selected using the PnNV21\* bit in PnDDC2Rm\*.

The formulae for YC-RGB conversion are the same as those for YC:YUV422.

**(a) Y data**

D63 to D48	63	56	55	48
Image data 8 and 7	Y7		Y6	
D47 to D32	47	40	39	32
Image data 6 and 5	Y5		Y4	
D31 to D16	31	24	23	16
Image data 4 and 3	Y3		Y2	
D15 to D0	15	8	7	0
Image data 2 and 1	Y1		Y0	

**(b) UV data (NV12)**

D63 to D48	63	56	55	48
Image data 8 and 7	V6		U6	
D47 to D32	47	40	39	32
Image data 6 and 5	V4		U4	
D31 to D16	31	24	23	16
Image data 4 and 3	V2		U2	
D15 to D0	15	8	7	0
Image data 2 and 1	V0		U0	

**(c) UV data (NV21)**

D63 to D48	63	56	55	48
Image data 8 and 7	U6		V6	
D47 to D32	47	40	39	32
Image data 6 and 5	U4		V4	
D31 to D16	31	24	23	16
Image data 4 and 3	U2		V2	
D15 to D0	15	8	7	0
Image data 2 and 1	U0		V0	

**(d) RGB color-space conversion format**

Image data 4 (Line 0)	23	16	15	8	7	0
	Y3 (Line 0)		U2 (Line 0)		V2 (Line 0)	
Image data 3 (Line 0)	23	16	15	8	7	0
	Y2 (Line 0)		U2 (Line 0)		V2 (Line 0)	
Image data 2 (Line 0)	23	16	15	8	7	0
	Y1 (Line 0)		U0 (Line 0)		V0 (Line 0)	
Image data 1 (Line 0)	23	16	15	8	7	0
	Y0 (Line 0)		U0 (Line 0)		V0 (Line 0)	
Image data 4 (Line 1)	23	16	15	8	7	0
	Y3 (Line 1)		U2 (Line 0)		V2 (Line 0)	
Image data 3 (Line 1)	23	16	15	8	7	0
	Y2 (Line 1)		U2 (Line 0)		V2 (Line 0)	
Image data 2 (Line 1)	23	16	15	8	7	0
	Y1 (Line 1)		U0 (Line 0)		V0 (Line 0)	
Image data 1 (Line 1)	23	16	15	8	7	0
	Y0 (Line 1)		U0 (Line 0)		V0 (Line 0)	

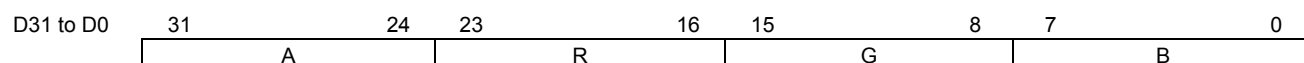
**(6) 32-bit/pixel: ARGB8888**

Levels for A, R, G, and B are represented by 8 bits each (ARGB8888). Note that the format includes a setting for alpha ratio in addition to the R, G, and B values. In this section, "32-bit/pixel" refers to the ARGB8888 format unless otherwise specified.

$\alpha$  blending control using the A value is valid when the PnSPIM\* bit in PnMRm\* is set so that  $\alpha$  blending is performed. This means that the blending ratio selected in the plane n blending ratio register m (PnALPHARm\*) is invalid.

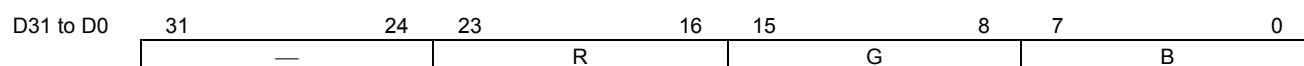
A 32-bit/pixel (ARGB8888) display should be specified with the PnLRGB1\* or PnLRGB0\* bit in the plane n display data control register m (PnDDCRm\*) or the PnEDF\* bits in plane n display data control 4 register (PnDDC4Rm\*). When using the PnLRGB1\* or PnLRGB0\* bit in PnDDCRm\*, the following restrictions apply.

- Two planes, plane 1 and plane 2, need to be used.
- Transparent color processing is not possible.
- $\alpha$  blending or EOR operations must be performed in an area where a lower plane exists. If the setting of the PnSPIM\* bits allows  $\alpha$  blending or an EOR operation but there is no lower plane, display of 32-bit/pixel data will not be possible without superposition.

**32-bit/pixel data (ARGB8888 data) format****(7) 32-bit/pixel: RGB888**

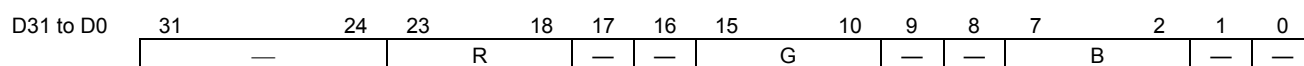
Levels for R, G, and B are represented by 8 bits each (RGB888). "—" indicates any desired value.

A 32-bit/pixel (RGB888) display should be specified with the PnEDF\* bits in plane n display data control 4 register m (PnDDC4Rm\*).

**32-bit/pixel data (RGB888 data) format****(8) 32-bit/pixel: RGB666**

Levels for R, G, and B are represented by 6 bits each (RGB666). "—" indicates any desired value.

A 32-bit/pixel (RGB666) display should be specified with the PnEDF\* bits in plane n display data control 4 register m (PnDDC4Rm\*).

**32-bit/pixel data (RGB666 data) format**

Note: \* m = 0 and 2 for RZ/G1H, suffix "m" is only for RZ/G1H.  
n = 1 to 8.

### 21.4.6 Data Formats for Output and Display Capture

In the case of digital RGB output from a display unit (DU), superpositioning in the form of  $\alpha$  blending and EOR operations is performed after the display data format has been expanded into the RGB888 format, and then the data are output. In data capture, display data are captured and stored as RGB888 or the five higher-order bits from both the red pins and blue pins and six bits from the green pins. The supplementary formats and data formats in the case of expansion to RGB888 are as indicated in the following table.

**Table 21.31 Output Data Format**

		Red								Green								Blue							
		7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Expanded data	8-bit/pixel (after conversion from a color palette)	R (6 bits)						0	0	G (6 bits)						0	0	B (6 bits)						0	0
	16-bit/pixel	R (5 bits)					0	0	0	G (6 bits)					0	0	0	B (5 bits)					0	0	0
	ARGB	R (5 bits)					0	0	0	G (5 bits)					0	0	0	B (5 bits)					0	0	0
	YC after RGB conversion	R (8 bits)								G (8 bits)								B (8 bits)							
	32-bit/pixel (ARGB8888)	R (8 bits)								G (8 bits)								B (8 bits)							
	32-bit/pixel (RGB888)	R (8 bits)								G (8 bits)								B (8 bits)							
	32-bit/pixel (RGB666)	R (6 bits)						0	0	G (6 bits)						0	0	B (6 bits)						0	0
After superpositioning		R (8 bits)								G (8 bits)								B (8 bits)							
DU0 display data		R (8 bits)								G (8 bits)								B (8 bits)							
DU1 display data		R (8 bits)								G (8 bits)								B (8 bits)							
DU2 display data [RZ/G1H]		R (8 bits)								G (8 bits)								B (8 bits)							

### 21.4.7 Endian Conversion

The display unit (DU) can perform big-endian/little-endian conversion according to the setting of bit 20 in DSYSRn\*<sup>1</sup>. If image data are in 32-bit/pixel format, big-endian/little-endian conversion for the data involves the use of the plane n swap control register m (PnSWAPRm\*<sup>2</sup>). Then set bit 20 in DSYSRn\*<sup>1</sup> to 0.

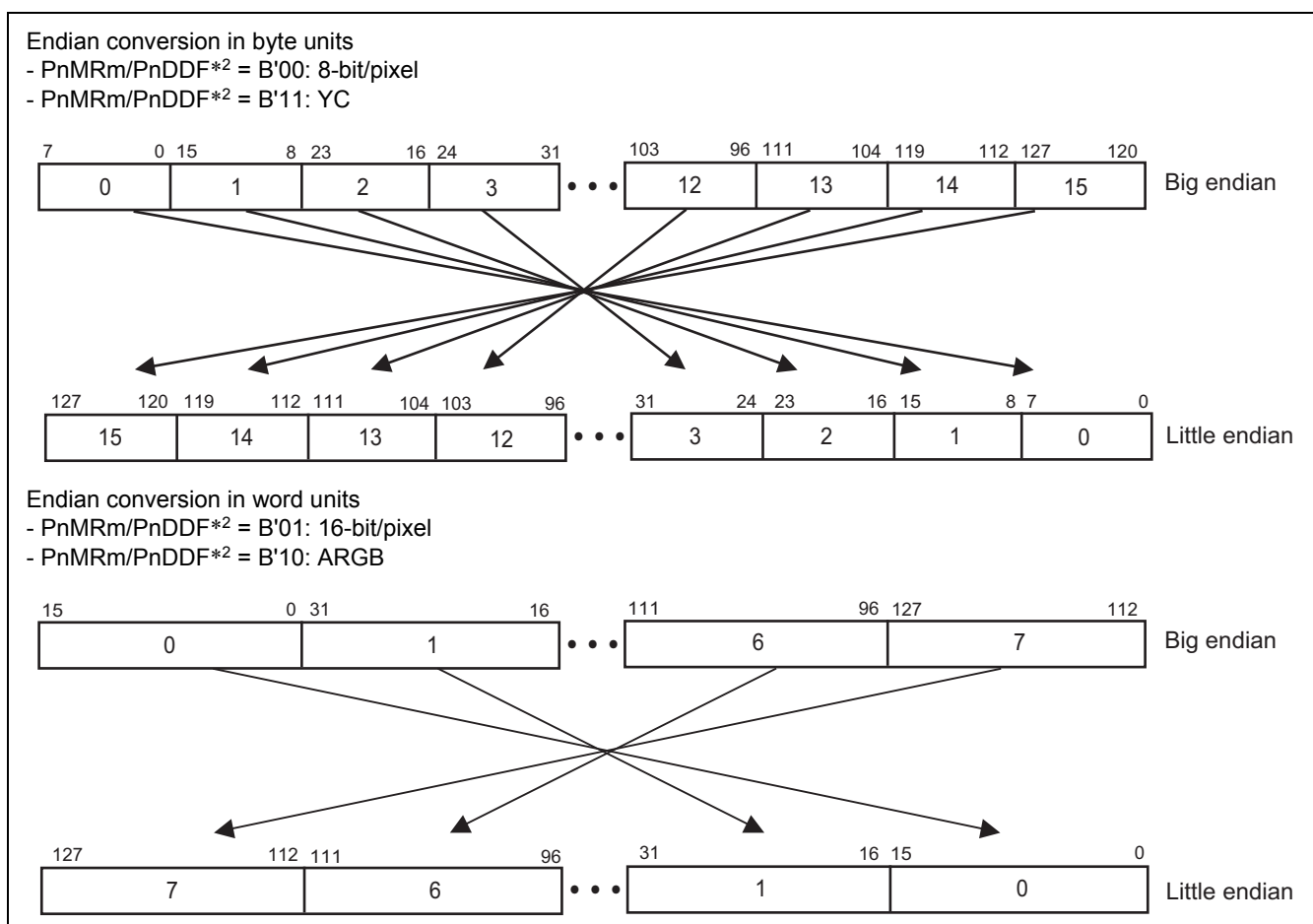
The internal data format in the display unit (DU) is fixed to little-endian; by setting bit 20 in DSYSRn\*<sup>1</sup> to 1, image data arranged in big-endian format in memory are converted into little-endian format and read.

The unit for endian conversion (byte/word) is determined by the setting of the PnDDF\*<sup>2</sup> bits in PnMRm\*<sup>2</sup>.

**Table 21.32 Endian Conversion**

PnMRm/PnDDF* <sup>2</sup>	Data Format	Units for Endian Conversion
B'00	8-bit/pixel	Byte
B'01	16-bit/pixel	Word
B'10	ARGB	Word
B'11	YC	Byte

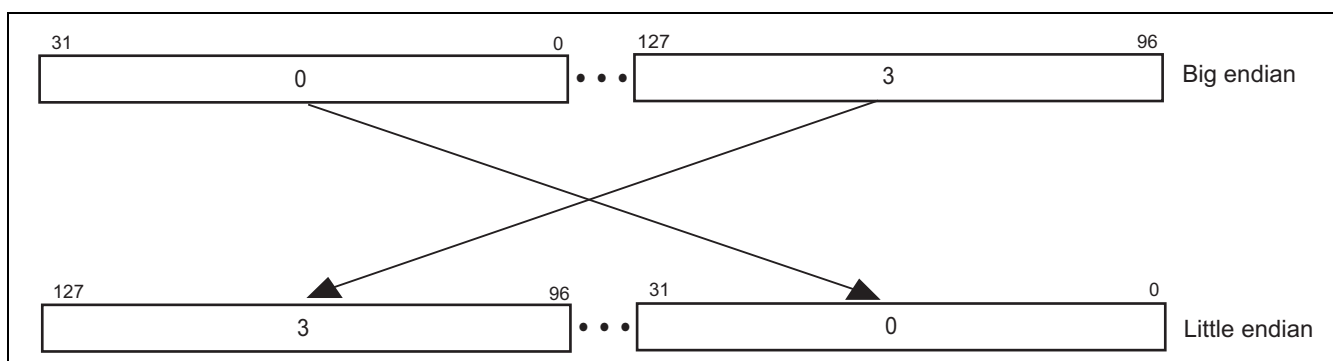
Endian conversion in each of the units indicated below is shown in Figure 21.4.



**Figure 21.4 Endian Conversion**



Since bits 3 and 2 in the plane n swap control register m ( $PnSWAPRm^{*2}$ ) are set to 1 and bits 1 and 0 in  $PnSWAPRm^{*2}$  are set to 0 in the 32-bit/pixel case, the endian must be converted as shown in the figure below. Bit 4 in  $PnSWAPRm^{*2}$  may be set to either 1 or 0. At this time, set bit 20 in the display unit system control register n ( $DSYSRn^{*1}$ ) to 0.



**Figure 21.5 Endian Conversion for 32-bit/pixel**

- Notes: 1.  $n = 0$  to 2 for RZ/G1H,  $n = 0$  to 1 for RZ/G1M/N/E  
 2.  $m = 0$  and 2, suffix “m” is only for RZ/G1H.  
 $n = 1$  to 8.

### 21.4.8 Color Palette

8-bit/pixel data employs color palettes. The DU has four color palettes which are only accessible to superposition processors 0<sup>\*1</sup> and 2<sup>\*2</sup>.

The color palette for use in plane n is determined by the setting of the  $PnCPSL^{*3}$  bits in  $PnMRm^{*3}$ . Each of the color palettes consists of two alternate buffers; one serves as a display buffer, and the other is for CPU access. After setting each color palette, by setting the color palette switching enable bit CP4CE, CP3CE, CP2CE, or CP1CE in  $CPCRm^{*4}$  to 1, the color palette thus set becomes valid at the next VSYNC falling edge (internal update timing), or upon display reset (when the DRES bit in  $DSYSRm^{*5}$  is changed from 1 to 0).

#### (1) Notes on Use of Color Palettes

1. Because palettes consist of alternate buffers, complete overwriting is necessary upon a color palette update. However, when the details of color palette updates are being managed, there is no problem with overwriting only the relevant part.
2. Upon completion of color palette settings, the switching enable bit must always be set to 1.
3. When reading a color palette from the CPU, reading should be performed before setting the switching enabled bit to 1.

#### (2) Procedure for Setting a Color Palette

##### (a) Procedure for switching from the initial state

The initial state (after power-on reset) is the display reset state.

1. Set the display unit system control register.
2. Set color palette 1, 2, 3, or 4.
3. After setting the color palette, set the color palette switching enable bit to 1.
4. Cancel the display reset.

##### (b) Procedure for switching from display state

In the display state, the DRES bit and DEN bit in  $DSYSRm^{*5}$  are 0 and 1 respectively.

1. Confirm that the color palette switching enable bit is 0.
2. Set color palette 1, 2, 3, or 4.
3. After setting the color palette, set the color palette switching enable bit to 1.

Notes:

1. Superposition processor 0 is valid for RZ/G1H/M/N/E.
2. Superposition processors 2 is valid for RZ/G1H.
3.  $m = 0$  and 2, suffix “m” is only for RZ/G1H.  
 $n = 1$  to 8.
4.  $m = 0$  and 2, suffix “m” is only for RZ/G1H.
5.  $m = 0$  and 2 for RZ/G1H,  $m = 0$  for RZ/G1M/N/E.

### 21.4.9 Superpositioning of Planes

For each plane, three types of combined superpositioning are possible:  $\alpha$  blending, transparent colors, and EOR operations. By setting the PnSPIM\*<sup>3</sup> bits in PnMRm\*<sup>3</sup>, the superpositioned display type can be selected.

However,  $\alpha$  blending and EOR operation cannot be performed simultaneously on the same plane.

Transparent color processing for YC data is not possible.

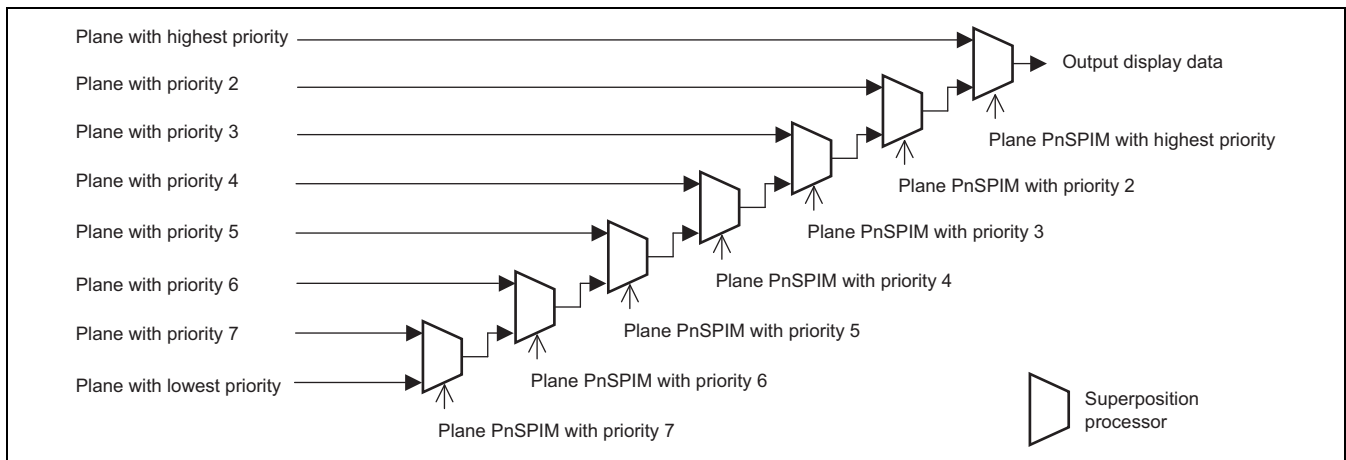
When 32-bit/pixel data is specified with the PnLRGB1\*<sup>3</sup> or PnLRGB0\*<sup>3</sup> bit in the plane n display data control register m (PnDDCRm\*<sup>3</sup>), the following restrictions apply to superpositioning. These restrictions do not apply when using the PnEDF\*<sup>3</sup> bits in plane n display data control 4 register m (PnDDC4Rm\*<sup>3</sup>).

- Transparent color processing is not possible. Bit 2 in PnSPIM\*<sup>3</sup> must be set to 1.
- When  $\alpha$  blending or an EOR operation has been specified but all of the lower planes are off, the display of 32-bit/pixel data is not possible.
- The alpha ratio of the 32-bit/pixel data (ARGB8888) can only be the higher-order eight bits (A value).

**Table 21.33 Superpositioning**

PnSPIM	Superpositioning	YC Data or 32-bit/pixel Data* <sup>2</sup>
B'000	Transparent color processing is performed for the specified plane. When the specified plane is a transparent color, the lower plane is displayed. (Default)	Prohibited
B'001	Blending of the specified plane with the lower plane is performed. When the specified plane is a transparent color, blending is not performed and the lower plane is displayed.	Prohibited
B'010	EOR operation of the specified plane and the lower plane is performed. When the specified plane is a transparent color, EOR operation is not performed and the lower plane is displayed.	Prohibited
B'011	Setting prohibited (The lower plane is displayed.)	Prohibited
B'100	Transparent color processing is not performed for the specified plane. The specified plane is displayed.	Possible
B'101	Blending of the specified plane with the lower plane is performed. Transparent color specification for the specified plane is ignored, and blending of all the pixels in the specified plane with the lower plane is performed.	Possible* <sup>1</sup>
B'110	EOR operation of the specified plane and the lower plane is performed. Transparent color specification for the specified plane is ignored, and EOR operation of all the pixels in the specified plane and the lower plane is performed	Possible* <sup>1</sup>
B'111	Setting prohibited (The lower plane is displayed.)	Prohibited

After the image data format has been expanded to RGB888,  $\alpha$  blending or EOR operation is performed. The complementary format of each display data format is shown in Table 21.31.  $\alpha$  blending and EOR operation are performed in the sequence of the lower plane to the upper plane. The block diagram is shown below.



**Figure 21.6 Plane Processing Sequence in  $\alpha$  Blending and EOR Operation**

When the format of display data for  $\alpha$  blending or EOR operation is 8-bit/pixel, after selection in advance of the color palette to be used, the  $\alpha$  blending or EOR operation on/off should be specified. At this time, when both planes for  $\alpha$  blending or for EOR operation have the same color palette selected (color palette contention), only the specified plane is displayed, with no  $\alpha$  blending or EOR operation performed. When display of all lower planes is turned off, the specified plane is displayed. That is,  $\alpha$  blending or EOR operation of the specified plane with the image data specified in  $BPOR_n^{*3}$  is not performed. Note however that when a 32-bit/pixel display is set by the  $PnLRGB1^{*3}$  or  $PnLRGB0^{*3}$  bit in the plane  $n$  display data control register  $m$  ( $PnDDCRm^{*3}$ ), display of 32-bit/pixel data is not possible when  $\alpha$  blending or an EOR operation has been specified but all of the lower planes are off.

### (1) $\alpha$ Blending

In  $\alpha$  blending, blending processing is performed according to the alpha ( $\alpha$ ) ratio set by the  $PnALPHA^{*3}$  bits in  $PnALPHARm^{*3}$ , the alpha ( $\alpha$ ) ratio set by the blending ratio bits in the color palette, the alpha ( $\alpha$ ) ratio of the image data of the display plane, or the data in an  $\alpha$  plane.

In the case of 32-bit/pixel data (ARGB8888), the alpha ratio can only be the higher-order eight bits (A value) of the 32-bit/pixel data (ARGB8888).

$$\text{Result of blending} \approx (\text{specified plane} \times \alpha/255 + \text{lower plane} \times (1 - \alpha/255)) \quad (\text{Approximation})$$

In the above formula, the blending result,  $\alpha$ , the specified plane, and the lower plane are all given as 8-bit data.

When the alpha ratio is set to H'00, only the lower plane is displayed. When the alpha ratio is set to H'FF, only the specified plane is displayed. When the  $PnDDF^{*3}$  bits in  $PnMRm^{*3}$  are set to ARGB, and moreover the  $PnSPIM^{*3}$  bit in  $PnMRm^{*3}$  is set to perform  $\alpha$  blending,  $\alpha$  blending is performed according to the A value of the ARGB data format and by the  $\alpha$  value specified by the  $PnALPHA^{*3}$  bits in  $PnALPHARm^{*3}$ .

When the  $PnABIT^{*3}$  bits of  $PnALPHARm^{*3}$  are B'00,  $\alpha$  blending is performed when the A value is 1. When the  $PnABIT^{*3}$  bits are B'01,  $\alpha$  blending is performed when the A value is 0. When the  $PnABIT^{*3}$  bits are B'10 or B'11,  $\alpha$  blending is performed regardless of the A value.

### (2) Transparent Colors

For each plane, transparent color processing can be performed between the specified plane and the lower plane by setting  $PnSPIM^{*3}$  bit in  $PnMRm^{*3}$  to 0. However, transparent color processing cannot be performed for YC data and 32-bit/pixel data (when set with the  $PnLRGB1^{*3}$  or  $PnLRGB0^{*3}$  bit in  $PnDDCRm^{*3}$ ).

**(a) 8-bit/pixel Mode**

When the PnTC\*<sup>3</sup> bit in PnMRm\*<sup>3</sup> is 0 (initial value), transparent color processing is performed according to the setting in the plane n transparent color 1 register m (PnTC1Rm\*<sup>3</sup>). When the PnTC\*<sup>3</sup> bit in PnMRm\*<sup>3</sup> is 1, CP1TRm\*<sup>3</sup> to CP4TRm\*<sup>3</sup> can be used to set up to 16 colors in each of color palettes 1 to 4 as transparent colors. Only the indexes H'00 to H'0F can be specified as transparent colors; H'10 to H'FF cannot be specified as transparent colors.

The color palette transparent color register m 1 to 4 (CP1TRm\*<sup>3</sup> to CP4TRm\*<sup>3</sup>) can be selected using the PnCPSL\*<sup>3</sup> bits in PnMRm\*<sup>3</sup>.

**(b) 16-bit/pixel Mode and ARGB Mode**

Transparent color processing is performed according to PnTC2Rm\*<sup>3</sup>, regardless of the setting of the PnTC\*<sup>3</sup> bit in PnMRm\*<sup>3</sup>.

In the case of ARGB, bits 14 to 0 of PnTC2Rm\*<sup>3</sup> are compared, and bit 15 is ignored.

**(c) 32-bit/pixel Mode**

Transparent color processing is performed according to PnTC3Rm\*<sup>3</sup>, regardless of the setting of the PnTC\*<sup>3</sup> bit in PnMRm\*<sup>3</sup>.

For the bits to be compared, see Table 21.24.

The above is summarized in Table 21.34, which indicates the transparent color specification registers which are valid when the PnTC\*<sup>3</sup> bit is 0 and 1.

**Table 21.34 Transparent Color Specification Registers**

Data Format	Transparent Color Specification Bit (PnMRm* <sup>3</sup> ) /PnTC* <sup>3</sup>	Color Palette Select Bit (PnMRm* <sup>3</sup> ) /PnCPSL* <sup>3</sup>	Transparent Color Specification Register
8-bit/pixel	0	—	PnTC1R* <sup>3</sup>
	1	B'000	CP1TR
	1	B'001	CP2TR
	1	B'010	CP3TR
	1	B'011	CP4TR
16-bit/pixel	—	—	PnTC2R* <sup>3</sup>
ARGB	—	—	PnTC2R* <sup>3</sup>
32-bit/pixel	—	—	PnTC3R* <sup>3</sup>

**(3) EOR Operation**

EOR operation of the specified plane with the lower plane is performed.

- Notes: 1. Display of 32-bit/pixel data is not possible when all of the lower planes are off.  
 2. When a 32-bit/pixel display is set by the PnLRGB1\*<sup>3</sup> or PnLRGB0\*<sup>3</sup> bit in PnDDCRm\*<sup>3</sup>.  
 3. m = 0 and 2, suffix “m” is only for RZ/G1H.  
 n = 1 to 8.

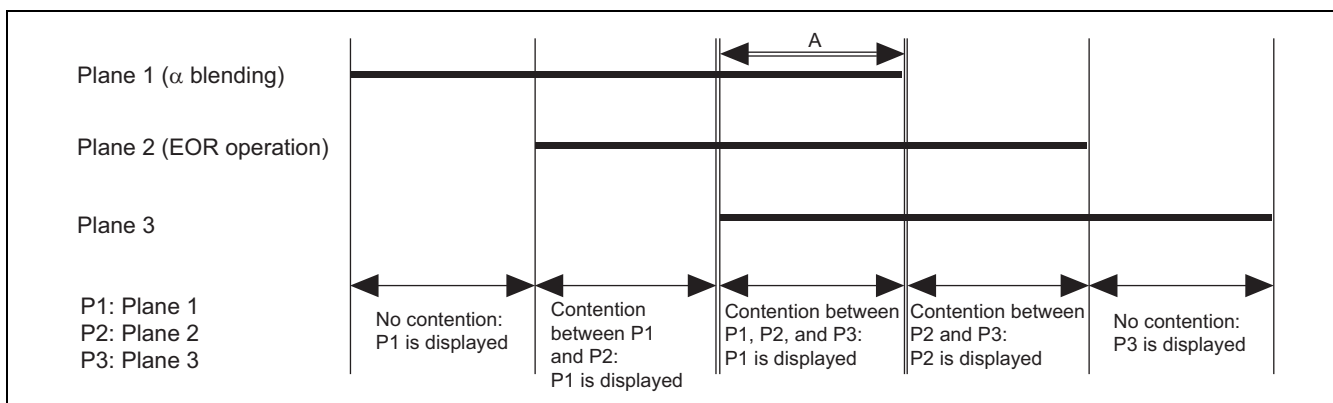
### 21.4.10 Contention

#### (1) Contention for a Color Palette

When the same color palette has been specified for two or more planes in the 8-bit/pixel format, contention for that color palette between the planes may arise in  $\alpha$  blending and EOR operations. Whether or not contention has occurred is judged on a per-pixel rather than per-plane basis.

In the figure below, planes 1 to 3 are in 8-bit/pixel format with  $\alpha$  blending specified for plane 1 and an EOR operation specified for planes 2 and 3. The figure shows the results in cases where contention has arisen because the same color palette has been specified for all of the planes (we assume that none of these planes includes transparent-color pixels).

In the event of contention,  $\alpha$  blending and EOR operations do not proceed and the uppermost plane is displayed.



**Figure 21.7 Contention for a Color Palette  
(When Multiple Planes Have the Same Color Palette)**

Figure 21.8 shows the results of all patterns of contention and the presence of transparent colors to be displayed during period A in the above figure.

- $P1 \alpha P2$  indicates  $\alpha$  blending of planes 1 and 2.
- $P2 \odot P3$  indicates an EOR operation for planes 2 and 3.
- $P1 \alpha (P2 \odot P3)$  indicates  $\alpha$  blending of plane 1 with the result of the EOR operation for planes 2 and 3.
- BPOR indicates data specified by the background plane output register n (BPORn\*).

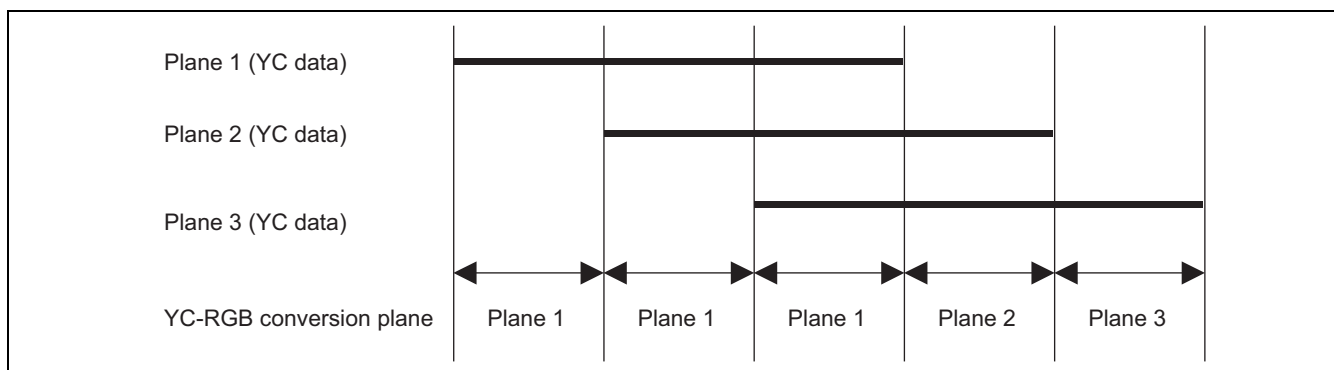
Note: \* n = 0 to 2 for RZ/G1H. n = 0 and 1 for RZ/G1M/N/E.

				√: Contention, —: No contention					
				P1	√	√	√	—	—
				P2	√	√	—	√	—
				P3	√	—	√	√	—
○: Transparent, ●: Non-transparent	P1	P2	P3		P1	P1	P1 α P2	P1 α P2	P1 α (P2⊕P3)
	●	●	●		P1	P1	P1 α P2	P1 α P2	P1 α P2
	●	●	○		P1	P1	P1 α P2	P1 α P2	P1 α P2
	●	○	●		P1	P1 α P3	P1	P1 α P3	P1 α P3
	●	○	○		P1	P1	P1	P1	P1
	○	●	●		P2	P2⊕P3	P2⊕P3	P2	P2⊕P3
	○	●	○		P2	P2	P2	P2	P2
	○	○	●		P3	P3	P3	P3	P3
○	○	○		BPOR	BPOR	BPOR	BPOR	BPOR	

Figure 21.8 Contention for a Color Palette and Transparent Colors

**(2) YC Data Contention**

The display unit (DU) has only one YC-RGB conversion circuit internally, and so YC-RGB conversion cannot be performed simultaneously for two or more planes. When there are pixels requiring YC-RGB conversion on two or more planes simultaneously, the pixels on the uppermost plane are YC-RGB converted, and the lower plane is not displayed. Figure 21.9 describes YC-RGB conversion when the data for three planes is in YC format.



**Figure 21.9 YC Data Contention**

**(3) Plane Priority Order**

The display priority order for planes is set using DPPRm\*, DS0PRm\*, or DS1PR; if one plane is set in two or more places in the priority order, the place with highest priority is selected.

For example, if the setting in DPPRm\* is H'00CB\_D888, then the results of the priority order and display on/off settings are as follows.

Plane with priority 1	Plane 1
Plane with priority 2	No corresponding plane
Plane with priority 3	No corresponding plane
Plane with priority 4	Plane 6
Plane with priority 5	Plane 4
Plane with lowest priority	Plane 5
Display off planes	Plane 2, plane 3, plane 7, and plane 8

Note \* m = 0 and 2, suffix "m" is only for RZ/G1H.

### 21.4.11 Blinking

For each plane, blinking operation can be performed by using the display area start addresses 0 and 1.

Usually, double-buffering control is performed for each plane according to the setting of the PnBM\* bit in PnMRm\*. However, blinking is performed with the period specified by the PnBTA\* and PnBTB\* bits in PnBTRm\* by setting the PnBM\* bits in PnMRm\* to B'10 (auto display change mode (blinking mode)). When the blinking period is set to 1, the display area start addresses 0 and 1 can be switched for every VSYNC; the same function as the auto display change mode can be achieved.

Notes: Set a value other than 0 to the PnBTA\* and PnBTB\* bits in PnBTRm\*.

- \* m = 0 and 2, suffix "m" is only for RZ/G1H.
- n = 1 to 8.

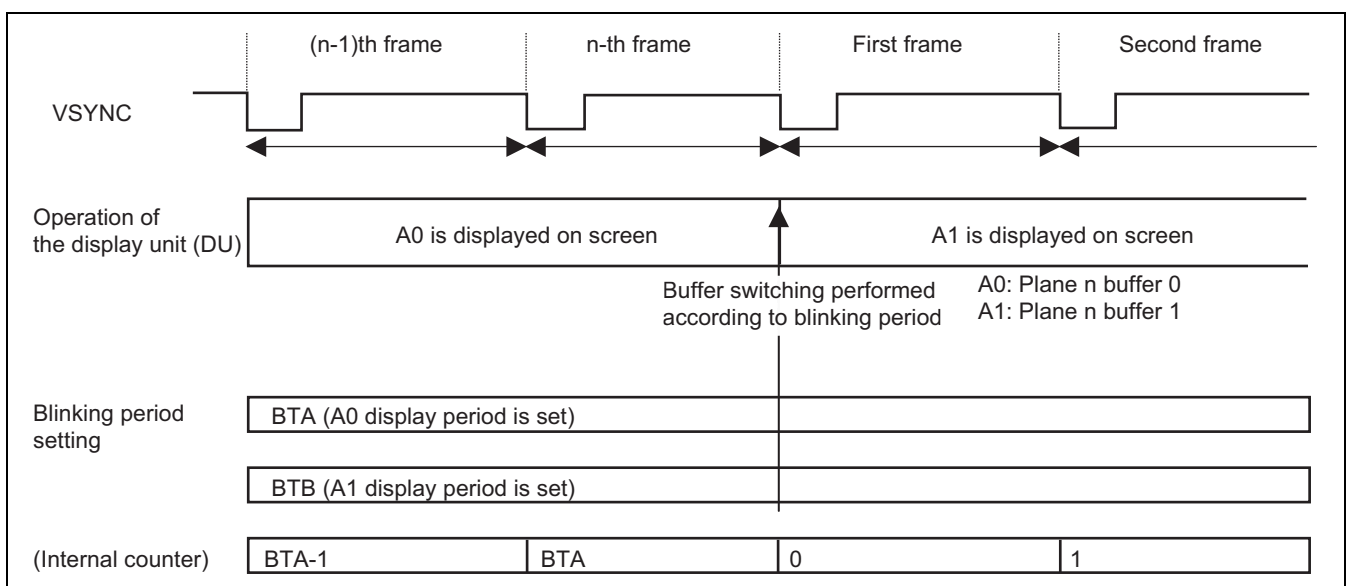


Figure 21.10 Blinking



### 21.4.12 Scroll Display

By setting display area and display screen sizes and start positions independently for each plane, smooth scroll processing can be performed independently for each plane.

The display can be scrolled by cyclically setting the values of display start positions X and Y (coordinates specified by PnSPXRm\* and PnSPYRm\*), taking as the origin the start address in memory specified by PnDSA0Rm\* to PnDSA2Rm\* for each plane.

Figure 21.11 summarizes display scrolling. The display is scrolled by setting the display start position from A to B.

Notes: Display sizes and other area settings for each plane should be set such that there is no data display outside the memory configuration area.

- \* m = 0 and 2, suffix “m” is only for RZ/G1H.
- n = 1 to 8.

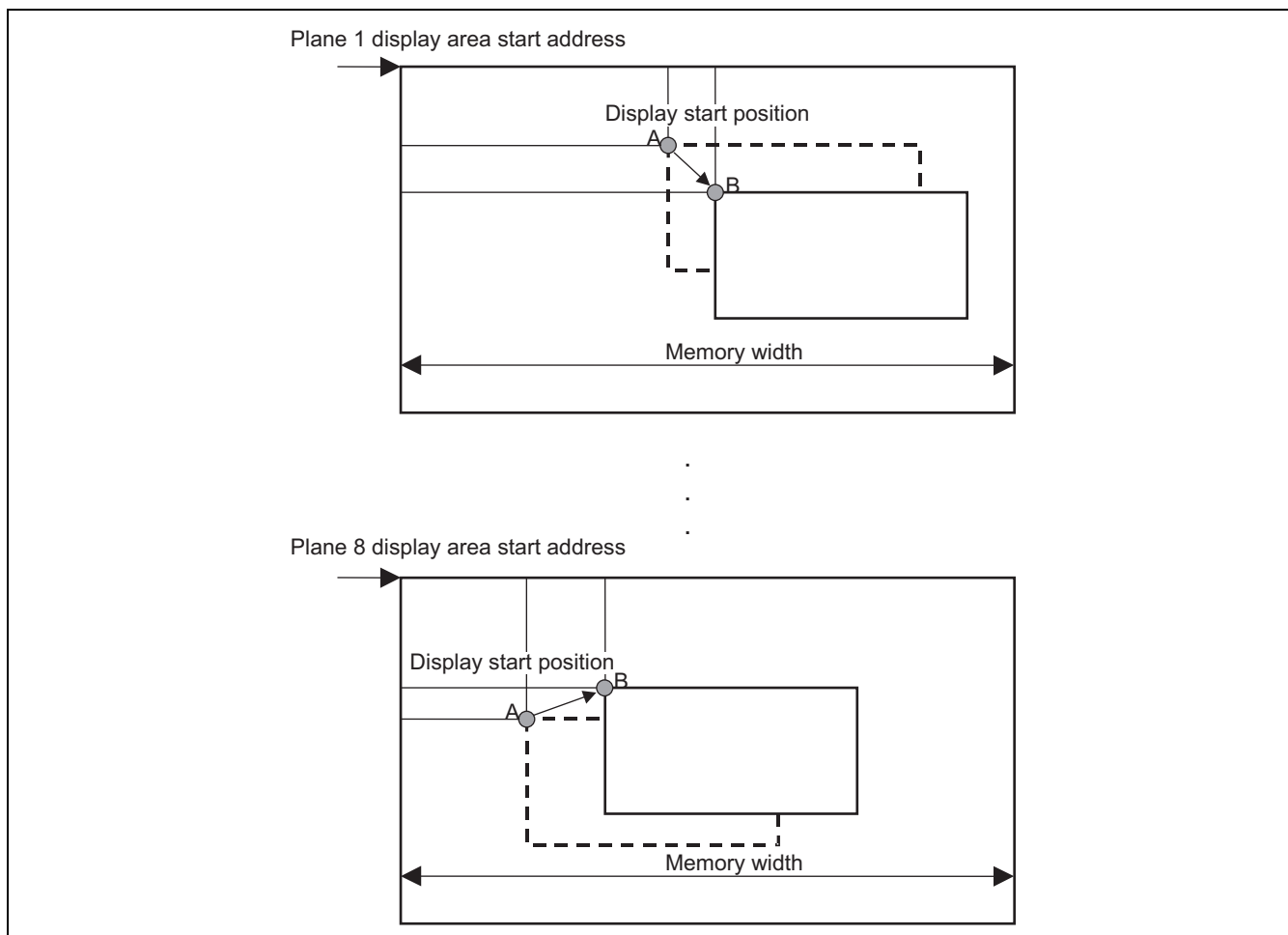
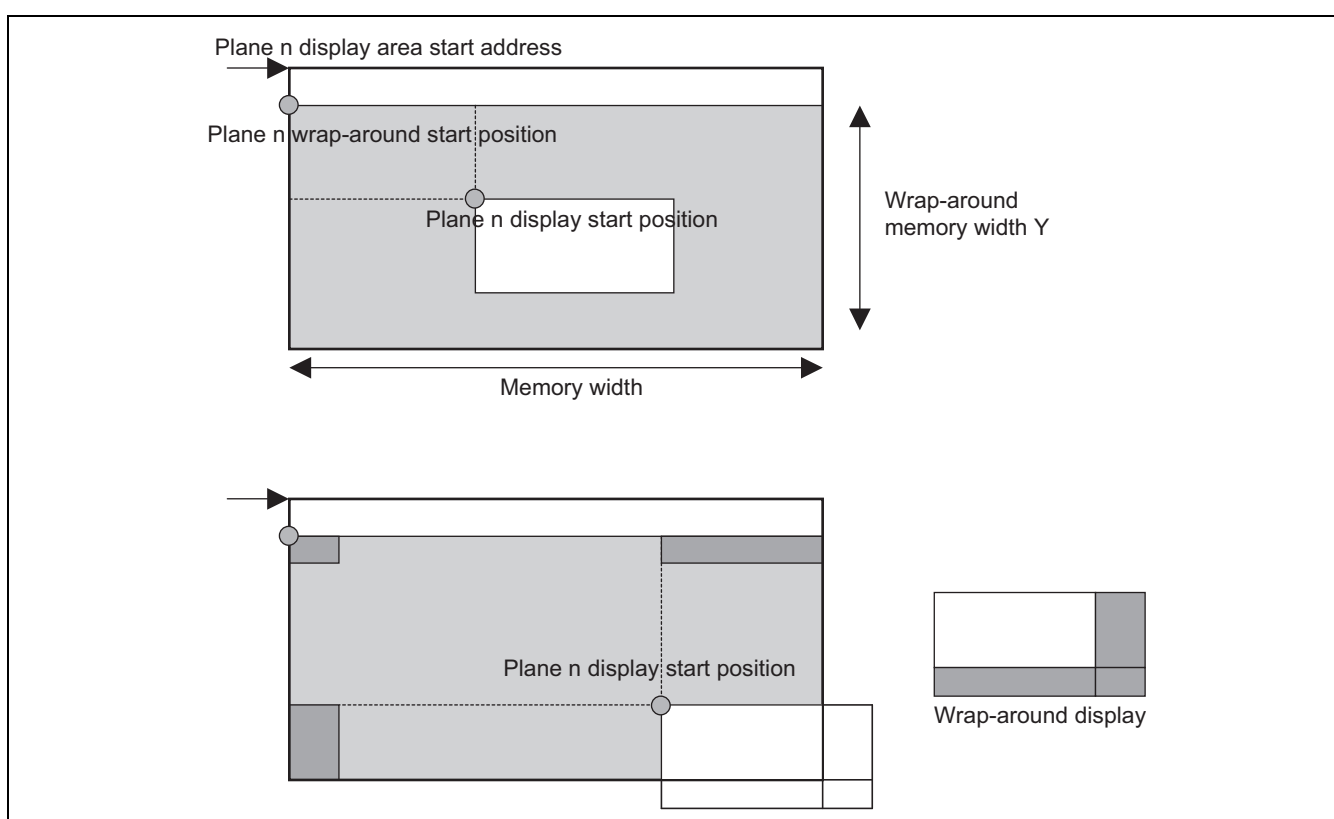


Figure 21.11 Schematic Diagram of Scroll Display

### 21.4.13 Wrap-Around Display

In addition to display scrolling, wrap-around display, which can be used in spherical scrolling, is possible for each plane. When enabling wrap-around display, the  $PnWAE^{*1}$  bit in  $PnMRm^{*1}$  is set to 1. As a result of changing the values of display start positions X and Y (the plane n start position X set in  $PnSPXRm^{*1}$  and the plane n start position Y set in  $PnSPYRm^{*1}$ ) in order to scroll the display, even when plane n overflows the wrap-around area, the wrap-around area is seen as a spherical surface in wrap-around display, as in Figure 21.12, and the part overflowing is complemented and displayed. The method used to specify the wrap-around area is described below.

1. The start address of the memory used for plane n is specified in  $PnDSA0Rm^{*1}$  to  $PnDSA2Rm^{*1}$ .
2. With the beginning of the specified memory as origin, the upper-left coordinates of the wrap-around area are specified in  $PnWASPRm^{*1}$ . The X-direction width of the wrap-around area is the memory width set in  $PnMWRm^{*1}$ .
3. The Y-direction width of the wrap-around area is set in  $PnWAMWRm^{*1}$ .



**Figure 21.12 Schematic Diagram of Wrap-Around Display**

Note: When wrap-around display is disabled (when the  $PnWAE^{*1}$  bit in  $PnMRm^{*1}$  is 0), the part overflowing the wrap-around area becomes the color specified by  $BPORn^{*2}$ , and superposition processing using this color is performed.

1.  $m = 0$  and 2, suffix “m” is only for RZ/G1H.  
 $n = 1$  to 8.
2.  $n = 0$  to 2 for RZ/G1H,  $n = 0$  and 1 for RZ/G1M/N/E.

### 21.4.14 Upper-Left Overflow Display

For each plane, a display start position in memory ( $PnSPXRm^*$ ,  $PnSPYRm^*$ ) and display size ( $PnDSXRm^*$ ,  $PnDSYRm^*$ ) can be set arbitrarily, so that by combining and using these registers, areas overflowing the upper-left relative to the monitor origin (upper-left corner) can be displayed without overwriting display data in memory.

For a picture of size ( $DSX$ ,  $DSY$ ) and with start position ( $SPX$ ,  $SPY$ ), by setting the size to  $(DSX-\Delta X, DSY-\Delta Y)$  and the start position to  $(SPX+\Delta X, SPY+\Delta Y)$ , the  $\Delta X$  part overflowing on the left side and the  $\Delta Y$  part overflowing on top can be displayed. At this time, the display position ( $PnDPXRm^*$ ,  $PnDPYRm^*$ ) is fixed at 0.

Note: \*  $m = 0$  and  $2$ , suffix “m” is only for RZ/G1H.  
 $n = 1$  to  $8$ .

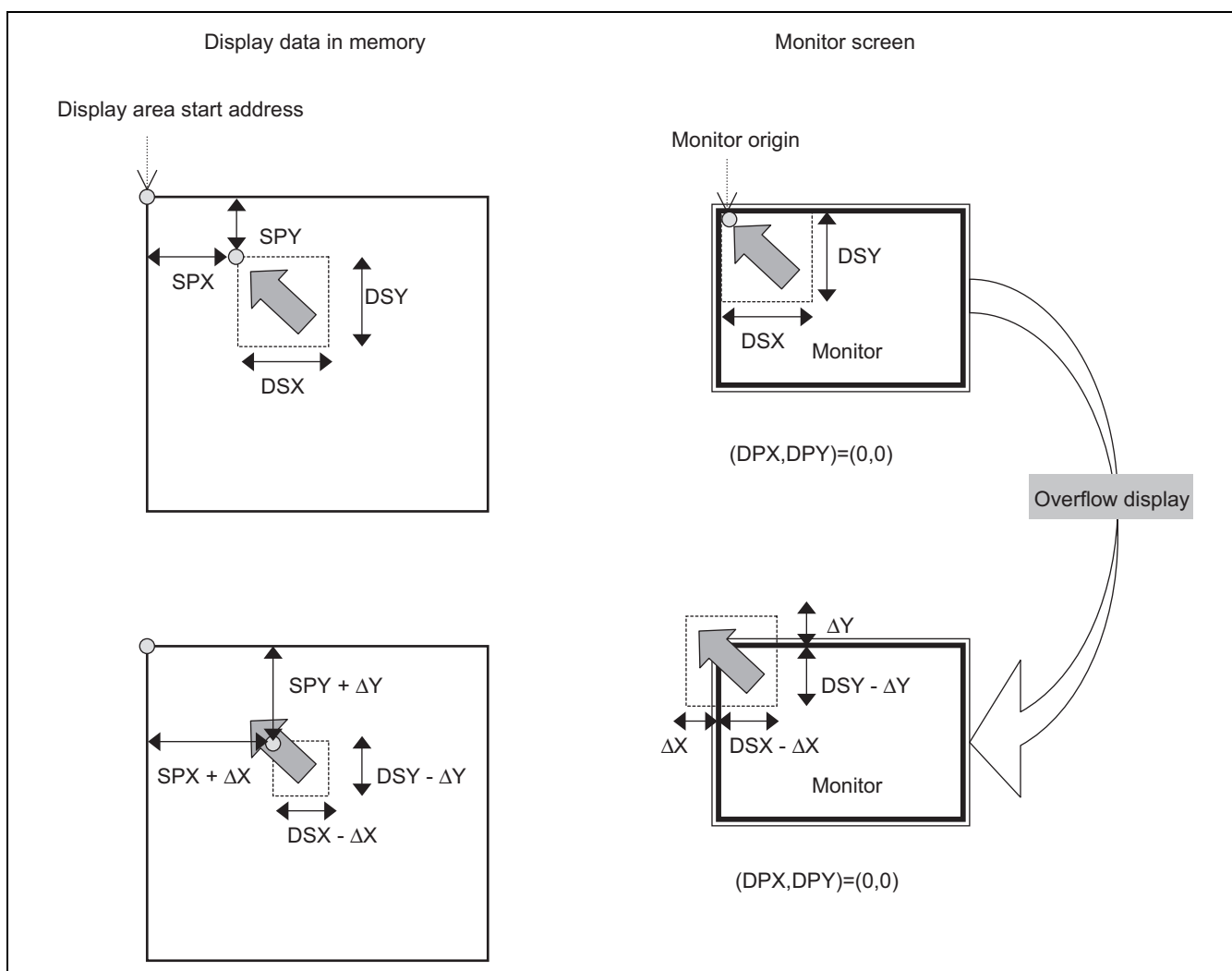


Figure 21.13 Schematic Diagram of Upper-Left Overflow Display

### 21.4.15 Double-Buffering Control

The double-buffering control of the display unit (DU) includes four types of functions, which are a auto rendering mode that does not switch the display until drawing is completed, a manual display change mode in which display or drawing switching is all controlled by software, an auto display change mode that realize blinking, and a video capture mode that is based on a frame ID of the video input (VIN) module.

In the case of auto rendering mode and manual display change mode, the display change is performed in frame units for non-interlaced and interlaced sync display, and in field units for interlaced sync & video display. In the case of auto display change mode, all switching is performed in field units. For video capture mode, all switching is performed in frame units.

**Auto Rendering Mode:** In auto rendering mode, display is not switched until drawing is completed. Even if drawing is not completed within a single frame period, drawing operation continues as it is.

**Manual Display Change Mode:** In manual display change mode, display frame switching and start of drawing are controlled by software. Display switching can either be performed by software using the PnDC\*1 bit in PnMRm\*1, or by setting the buffer 0 or buffer 1 start address in PnDSA0Rm\*1 and PnDSA1Rm\*1 indicated by the DFBn\*1 bit in DSSRm\*2.

The rendering start bit (i.e. the RS bit in the system control register (SCLR) in the R-GP2D) controls the start of drawing. An interrupt set up by using bit 11 in DSSRn\*3 or the trap flag (i.e. the TRA bit in the status register (SR) in the R-GP2D) determines the timing of this control. When making a transition from this mode to another mode, the PnDC\*1 bit in PnMRm\*1 should always be set to 1 first.

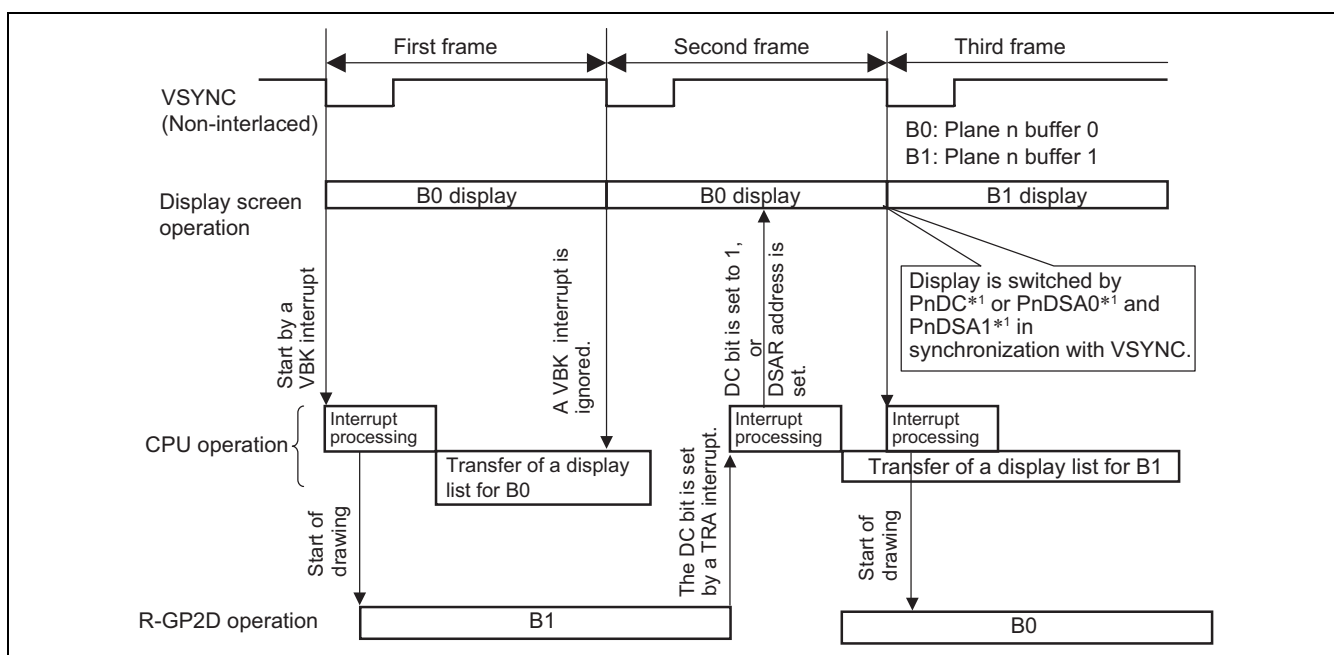


Figure 21.14 Manual Display Change Mode

**Auto Display Change Mode:** For information on the auto display change mode, refer to section 21.4.11, Blinking.

**Video Capture Mode:** In video capture mode, a display frame buffer is switched in frame units according to a frame ID, indicating the latest capture frame, output from the video input modules 0 to m (VIN0 to VINm\*4).

The video input modules 0 to m (VIN0 to VINm\*4) are selected by the PnVISL\*1 bit in the plane n mode register (PnMRm\*1).

Notes 1. m = 0 and 2, suffix "m" is only for RZ/G1H.

- n = 1 to 8.
2. RZ/G1H is valid. m = 0 and 2.
  3. n = 0 to 2 for RZ/G1H, n = 0 and 1 for RZ/G1M/N/E.
  4. m = 3 for RZ/G1H, m = 2 for RZ/G1M/N, m = 1 for RZ/G1E.

### 21.4.16 Sync Mode

In order to facilitate synchronization with external equipment, in addition to master mode, a TV synchronization function is provided. Selection of master mode and TV sync mode is performed using bits 7 and 6 in DSYSRn\*. In master mode (internal sync mode), the position of the falling edge of the vertical sync signal (VSYNC) set by VSPRn\* is detected. In TV sync mode (external sync mode), the position of the falling edge of the EXVSYNC signal is detected. The results are then reflected in the bits 14 and 11 of DSSRn\*.

**Master Mode (Internal Sync Mode):** By setting the period and pulse width of the horizontal and vertical sync signals (HSYNC, VSYNC) in the display timing generation registers, the corresponding waveforms are output. Also, display data is output in sync with these signals.

In interlaced sync mode and interlaced sync & video mode, a signal is output to the ODDF pin indicating odd/even fields.

**TV Sync Mode (External Sync Mode):** In TV sync mode, display data is output in sync with a horizontal sync signal and vertical sync signal (EXHSYNC, EXVSYNC) input from a TV, video, or other external sync signal generation circuit. Display data is output with reference to the falling edge of the EXHSYNC signal and the rising edge of the EXVSYNC signal.

The horizontal sync signal, vertical sync signal, and clock signal from the external sync signal generation circuit are input to the EXHSYNC, EXVSYNC, and DCLKIN pins, respectively. CSYNC is at high level. In interlaced sync mode and interlaced sync & video mode, a signal should be input to the EXODDF pin indicating odd/even fields. In non-interlaced mode, the input to the EXODDF pin should be fixed at low level or at high level.

When operating the unit in TV sync mode also, values must be set in horizontal sync width register n (HSWRn\*), horizontal cycle register n (HCRn\*), vertical sync point register n (VSPRn\*), and vertical cycle register n (VCRn\*) in section 21.3.2, Display Timing Generation Registers.

When the EXVSYNC signal is input, either before or after completion of display of the display size portion set in the display unit (DU), the display unit (DU) performs vertical display completion operation and transitions to control for the next screen. When the EXVSYNC signal is not input, the unit continues to wait for the EXVSYNC signal while remaining in the vertical blanking interval (auto-control is not performed). Similarly, when the EXHSYNC signal is input the display unit (DU) performs horizontal display completion operation and transitions to control for the next raster line; but if the EXHSYNC signal is not input, the unit continues to wait for the EXHSYNC signal while remaining in the horizontal blanking interval (auto-control is not performed).

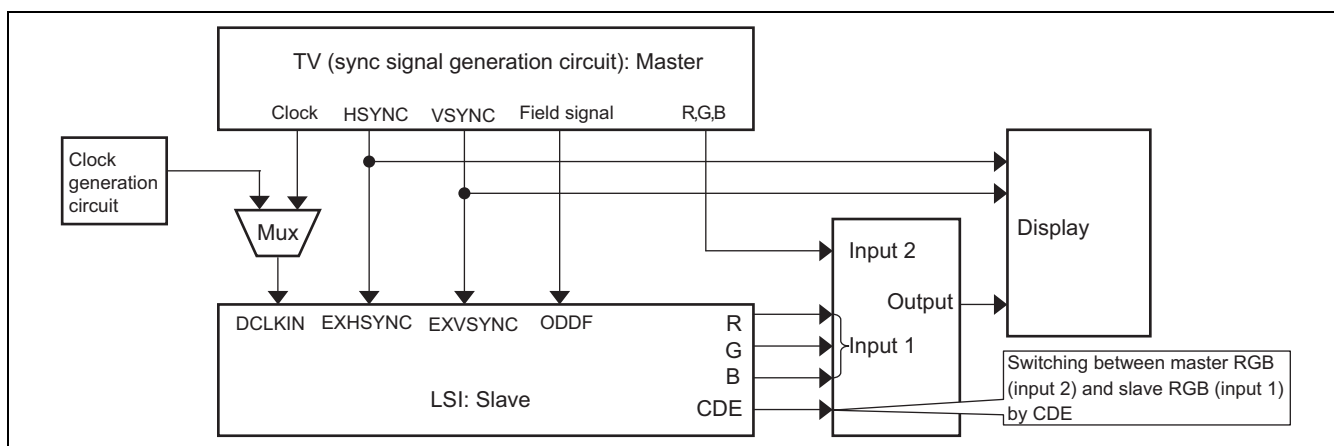


Figure 21.15 Signal Flow in TV Sync Mode

**Sync Method Switching Mode:** When switching from master mode into TV sync mode, or from TV sync mode into master mode, when necessary this mode should be switched into first. Even if a transition to this mode is not made first, switching of the synchronization method is possible.

In this mode, input/output pins connected to the display unit (DU) are for input, and so collision of pin signals can be avoided. Also, in this mode the internal dot clock is stopped, so that disorder in the input dot clock has no effect on display operation.

Notes: \* n = 0 to 2 for RZ/G1H, n = 0 and 1 for RZ/G1M/N/E

#### 21.4.17 Alpha-Ratio Planes

$\alpha$  blending can be performed by using the eight planes (display planes) that can display the current image data with the alpha ratio, plus two planes for the alpha ratio (alpha-ratio planes). Data in the alpha ratio planes are limited to the alpha ratio; they cannot be composed as display data.

To enable the alpha-ratio planes, set the AP1E or AP2E bit of DAPCRm\*<sup>1</sup> to 1. PnALPHARm\*<sup>1</sup> is used to select the alpha-ratio planes. Set the PnBRSL\*<sup>1</sup> bits in PnALPHARm\*<sup>1</sup> to B'111 and bits 2 to 0 in PnALPHA\*<sup>1</sup> to B'000 or B'001.

Notes: These alpha-ratio planes are not usable when 32-bit/pixel data are being displayed.

1. m = 0 and 2, suffix "m" is only for RZ/G1H.  
n = 1 to 8.

#### 21.4.18 Display Capture

In display capture, display data (RGB888 or RGB666) that have been composed for output on the relevant pins are converted to ARGB888, RGB565 or ARGB1555 data, stored in a buffer having the same configuration as the read buffer, and then stored in the area specified by DCnSARm\* via AXI. To capture the display data, set the DCE or DC2E bit of DCPCRm\* to 1. Capturing starts from the next frame after this setting has been made. The specifications for display capturing are as follows:

<b>Data formats:</b>	Refer to Table 21.31, Output Data Format. In the case of ARGB1555, the A value is determined by the setting of DCPCRm*. In the case of ARGB8888, the A value is determined by the setting of DCnMRm*.
<b>Capture area start address:</b>	Only a single address can be specified.
<b>Capture size X:</b>	The same as the monitor size (horizontal display end position (HDE) – horizontal display start position (HDS))
<b>Capture size Y:</b>	The same as the monitor size (vertical display end position (VDE) – vertical display start position (VDS))
<b>Memory width X:</b>	Specified by a register. Writing to the buffer ends when the memory width is exceeded.
<b>Memory length Y:</b>	Specified by a register. Storage of data in the memory ends when the memory length (in lines) is exceeded.

When the following display functions are set, the display capture function cannot be used.

- RGB-YC conversion performed by setting the RGBYC0 bits in the Display Unit Extensional Function Control 5 Register (DEF5R) [RZ/G1M/N/E]
- DRC processing performed by setting the DRC0 bits in the display unit extensional function control 5 register m (DEF5Rm\*) [RZ/G1H]

- DRC processing performed by setting the DRC1 bits in the display unit extensional function control 5 register m (DEF5Rm\*) [RZ/G1H]
- YC-RGB conversion performed by setting the YCRGB0 bits in the display unit extensional function control5 register m (DEF5Rm\*) [RZ/G1H]
- YC-RGB conversion performed by setting the YCRGB1 bits in the display unit extensional function control 5 register m (DEF5Rm\*) [RZ/G1H]

Notes: \* m = 0 and 2, suffix "m" is only for RZ/G1H.  
n = no number or 2.

### 21.4.19 Dual Display Output

The display unit (DU) has superposition processors, display-timing generators, pin controllers, and dot-clock generators, each of which is independently controllable. The DU0 and DU1 realize various types of display because two channels are available for selecting from among the eight display planes and two alpha-ratio planes.

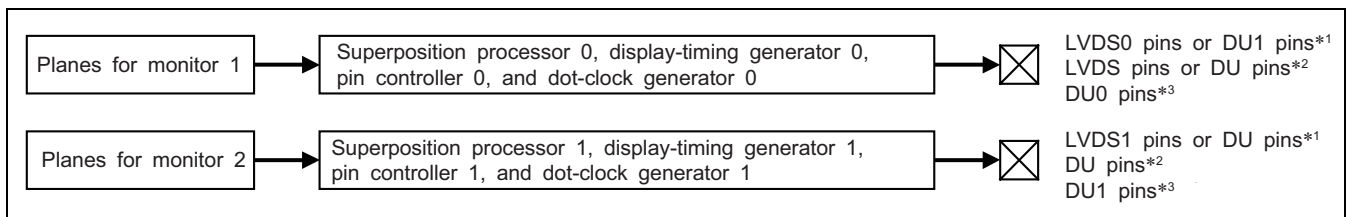
This section describes the dual display output using the DU0 and DU1.

#### (1) Independent Display

Different images can be displayed with different sizes by specifying different superposition processors, display-timing generators, pin controllers, and dot-clock generators. Captured video data can also be separately stored.

However, separate output images cannot be produced from a single plane. To display a single set of image data in separate output images, two planes must be used.

It is impossible to output the image data only via the digital RGB pins; the image data is output only via the LVDS pins [RZ/G1H] or via both the LVDS pins and digital RGB pins.[RZ/G1H/M/N]



**Figure 21.16 Independent Display**

#### (2) Display of Different Images on Monitors of the Same Size

Different images can be displayed on monitors of the same size when the same display-timing generator and dot-clock generator have been specified but the superposition processors and pin controllers are different. Captured video data can also be separately stored.

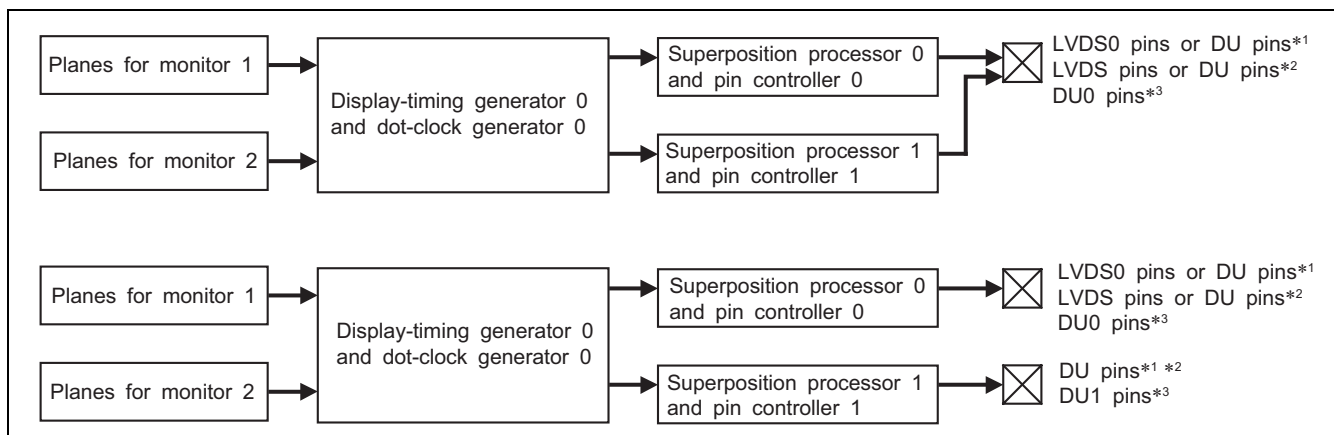
Images can be output to two monitors through a single set of pins by switching the display data in synchronization with the output dot clock. Output through two sets of pins is also possible.

When images are output to two monitors through a single set of pins, the image data can be output only via the digital RGB or LVDS0. [RZ/G1H]

When images are output to two monitors through a single set of pins, the image data can be output only via the digital RGB or LVDS. [RZ/G1M/N]

When images are output through two sets of pins, it is impossible to output the image data only via the digital RGB pins; the image data is output only via the LVDS pins or via both the LVDS pins and digital RGB pins.[RZ/G1H]

When images are output through two sets of pins, it is impossible to output the image data only via the digital RGB pins; the image data is output via both the LVDS pins and digital RGB pins. [RZ/G1M/N]



**Figure 21.17 Display of Different Images on Monitors of the Same Size**

**(3) Display of the Same Image on Monitors of the Same Size**

The same image can be displayed on different monitors when the same superposition processor, display-timing generator, and dot-clock generator have been specified but the pin controllers are different.

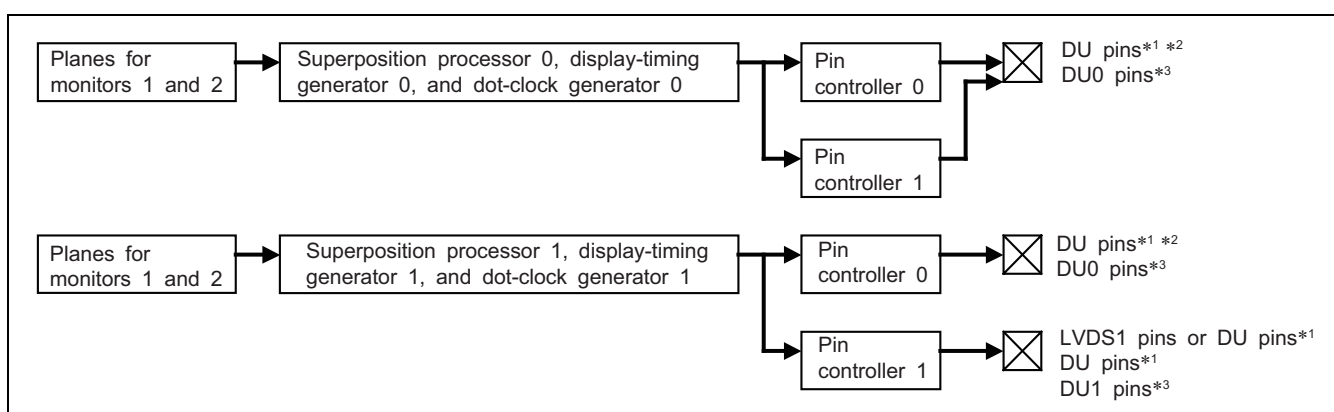
Images can be output to two monitors through a single set of pins by switching the display data in synchronization with the output dot clock. Output through two sets of pins is also possible.

When images are output to two monitors through a single set of pins, the image data can be output only via the digital RGB or LVDS0. [RZ/G1H]

When images are output to two monitors through a single set of pins, the image data can be output only via the digital RGB or LVDS. [RZ/G1M/N]

When images are output through two sets of pins, it is impossible to output the image data only via the digital RGB pins; the image data is output only via the LVDS pins or via both the LVDS pins and digital RGB pins. [RZ/G1H]

When images are output through two sets of pins, it is impossible to output the image data only via the digital RGB pins; the image data is output via both the LVDS pins and digital RGB pins. [RZ/G1M/N]

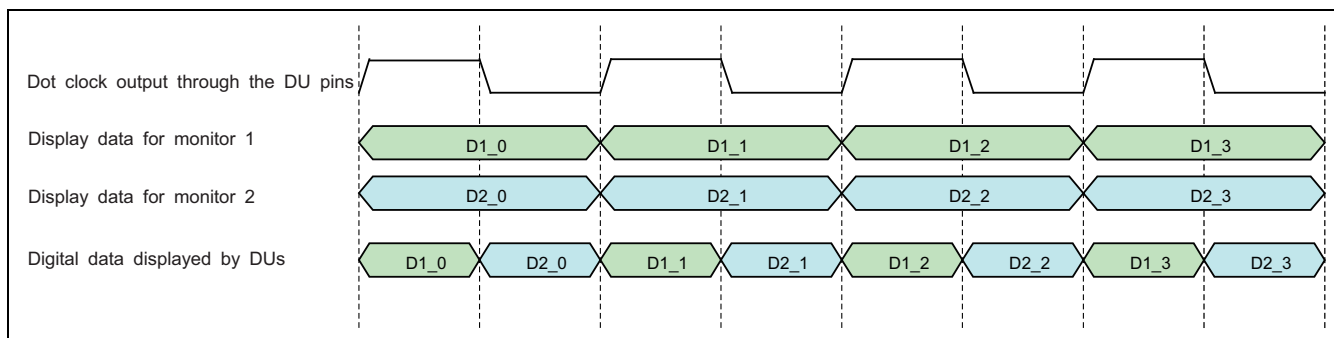


**Figure 21.18 Display of the Same Image on Monitors of the Same Size**

The timing for switching of display data in synchronization with the output dot clock is shown below. This feature is only supported by DU0 or DU0 via LVDS0\*1 or DU0 via LVDS\*2.

With the DU1 pin, data cannot be displayed by switching in synchronization with the output dot clock. For switching display data in synchronization with the output dot clock, the output dot clock should be set to be division by two or more of the input dot clock.





**Figure 21.19 Switching Display Data in Synchronization with the Output Dot Clock**

#### (4) Combinations of Blocks for Dual Display Output

For dual display output, the dot clock to be supplied to blocks in the display unit (DU), timing signals including SYNC, and display data are specifiable by setting the corresponding registers. Table 21.35 is a matrix of the combinations of blocks, and Table 21.36 gives the meanings of the symbols used in Table 21.35.

When the input block is superposition processor 0, for example, the information indicated in the table is as follows.

- The dot clock is that from dot-clock generator 0 or 1 as selected by the DR0D and DK1S bits of DORCR0\*<sup>1</sup> / DORCR\*<sup>2\*3</sup> (No. 5 in the table).
- The timing signal is that from display-timing generator 0 or 1 as selected by the DR0D and PG1T bits of DORCR0\*<sup>1</sup> / DORCR\*<sup>2\*3</sup> (No. 3 in the table).
- The planes for superpositioning of data are selected in DS0PR0\*<sup>1</sup> / DS0PR\*<sup>2\*3</sup> (No. 15 in the table).

Take care with register settings because timing signals such as the dot clock, sync signals and so on are freely specifiable, but if the dot clock or other timing signals differ from block to block, a normal display will not be possible.

Table 21.35 Combinations of Blocks

	Output Block																	
	Dot-clock generator 0 (clock)	Dot-clock generator 0 (external SYNC)	Dot-clock generator 1 (clock)	Dot-clock generator 1 (external SYNC)	Display-timing generator 0	Display-timing generator 1	Superposition processor 0	Superposition processor 1	Pin controller (output timing adjustment) 0	Pin controller (output timing adjustment) 1	Planes 1 to 8	Alpha-ratio planes 1 to 2	Display capture 1	Display capture 2	DU0 pins	DU1 pins		
Dot-clock generator 0 (clock)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	✓	—
Dot-clock generator 0 (external SYNC)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	✓	—
Dot-clock generator 1 (clock)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	✓
Dot-clock generator 1 (external SYNC)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	✓
Display-timing generator 0	✓	✓	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Display-timing generator 1	1	—	1	✓	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Superposition processor 0	4	—	4	—	2	2	—	—	—	—	13	△	—	—	—	—	—	—
Superposition processor 1	5	—	5	—	3	3	—	—	—	—	14	△	—	—	—	—	—	—
Pin controller (output timing adjustment) 0	✓	—	—	—	✓	—	6	6	—	—	—	—	—	—	—	—	—	—
Pin controller (output timing adjustment) 1	1	—	1	—	8	8	7	7	—	—	—	—	—	—	—	—	—	—
Planes 1 to 8	9	—	9	—	10	10	—	—	—	—	—	—	—	—	—	—	—	—
Alpha-ratio planes 1 to 2	11	—	11	—	12	12	—	—	—	—	—	—	—	—	—	—	—	—
Display capture 1	4	—	4	—	2	2	✓	—	—	—	—	—	—	—	—	—	—	—
Display capture 2	5	—	5	—	3	3	—	✓	—	—	—	—	—	—	—	—	—	—
DU0 pins	—	—	—	—	—	—	—	—	✓	—	—	—	—	—	—	—	—	—
DU1 pins	—	—	—	—	—	—	—	—	—	✓	—	—	—	—	—	—	—	—

Table 21.36 Meanings of Symbols and Numbers

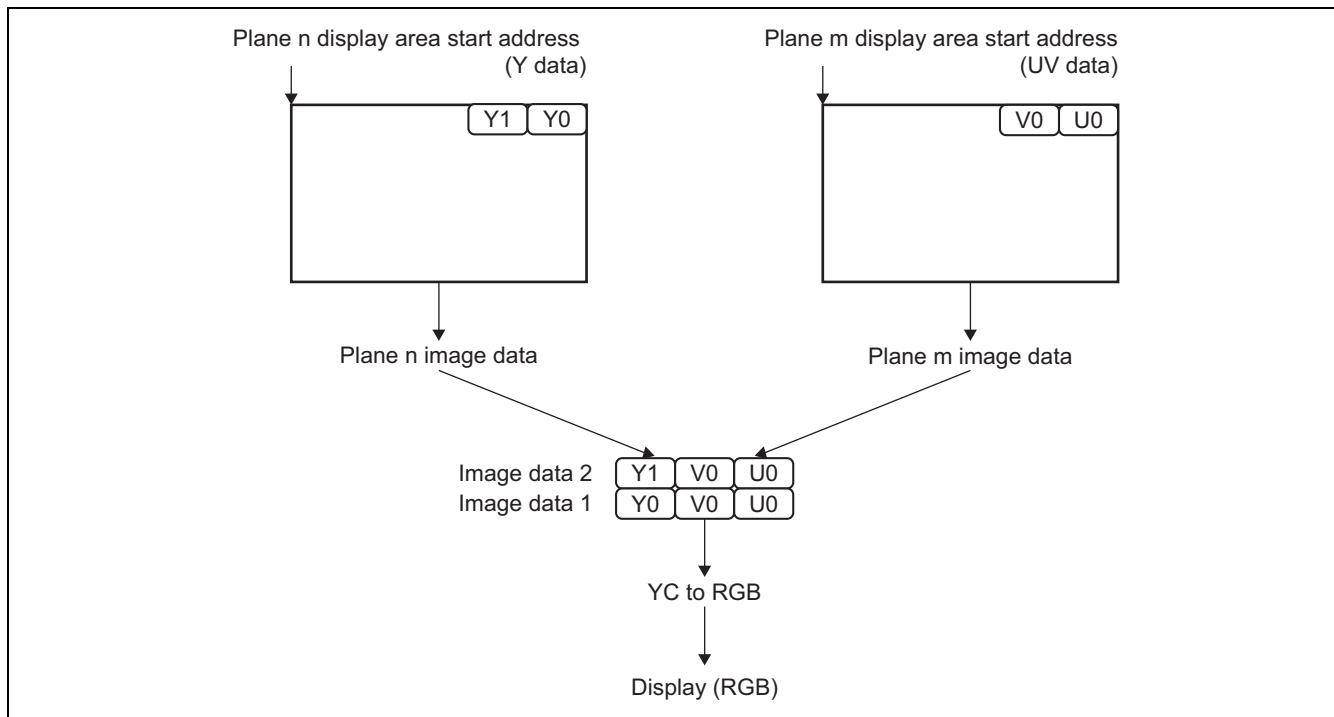
Symbol or No.	Register Name	Bit Name	Description
✓	—	—	One-to-one combination
—	—	—	No combination
△	—	—	Depends on the values in DS0PR0*1 / DS0PR*2*3, DS1PR, and PnALPHARm*4.
1	Display unit output route control register 0 (DORCR0)*1 / Display unit output route control register (DORCR)*2*3	DK1S	0: Dot-clock generator 0 (clock) 1: Dot-clock generator 1 (clock)
2	Display unit output route control register 0 (DORCR0)*1 / Display unit output route control register (DORCR)*2*3	PG0D PG1T	Other than 01_1: Display-timing generator 0 01_1: Display-timing generator 1
3	Display unit output route control register 0 (DORCR0)*1 / Display unit output route control register (DORCR)*2*3	PG0D PG1T	Other than 00_1: Display-timing generator 0 00_1: Display-timing generator 1
4	Display unit output route control register 0 (DORCR0)*1 / Display unit output route control register (DORCR)*2	PG0D DK1S	Other than 01_1: Dot-clock generator 0 (clock) 01_1: Dot-clock generator 1 (clock)
5	Display unit output route control register 0 (DORCR0)*1 / Display unit output route control register (DORCR)*2*3	PG0D DK1S	Other than 00_1: Dot-clock generator 0 (clock) 00_1: Dot-clock generator 1 (clock)
6	Display unit output route control register 0 (DORCR0)*1 / Display unit output route control register (DORCR)*2*3	PG0D	00: Superposition processor 0 01: Superposition processor 1 10: Fixed to 0 11: The value of DOOR0
7	Display unit output route control register 0 (DORCR0)*1 / Display unit output route control register (DORCR)*2*3	PG1D	00: Superposition processor 0 01: Superposition processor 1 10: Fixed to 0 11: The value of DOOR1
8	Display unit output route control register 0 (DORCR0)*1 / Display unit output route control register (DORCR)*2*3	PG1T	0: Display-timing generator 0 1: Display-timing generator 1

Symbol or No.	Register Name	Bit Name	Description
9	Display unit plane timing select register (DPTSR)	P1DK to P8DK	0: Dot-clock generator 0 (clock) 1: Dot-clock generator 1 (clock)
10	Display unit plane timing select register (DPTSR)	P1TS to P8TS	0: Display-timing generator 0 1: Display-timing generator 1
11	Display unit alpha plane timing select register (DAPTSR)	AP1DK to AP2DK	0: Dot-clock generator 0 (clock) 1: Dot-clock generator 1 (clock)
12	Display unit alpha plane timing select register (DAPTSR)	AP1TS to AP2TS	0: Display-timing generator 0 1: Display-timing generator 1
13	Display superimpose 0 priority register 0 (DS0PRO)* <sup>1</sup>  Display superimpose 0 priority register (DS0PR)* <sup>2*3</sup>	—	See the description of DS0PRO* <sup>1</sup> / DS0PR* <sup>2*3</sup> .
14	Display superimpose 1 priority register (DS1PR)	—	See the description of DS1PR.

Notes: 1. RZ/G1H is valid.  
 2. RZ/G1M/N are valid.  
 3. RZ/G1E is valid.  
 4. m = 0 and 2, suffix “m” is only for RZ/G1H.  
 n = 1 to 8.

### 21.4.20 Divided YUV Display

An image that has been divided up into separate Y and UV data for separate storage in memory can be displayed as YUV422 or YUV420 data by using two planes.



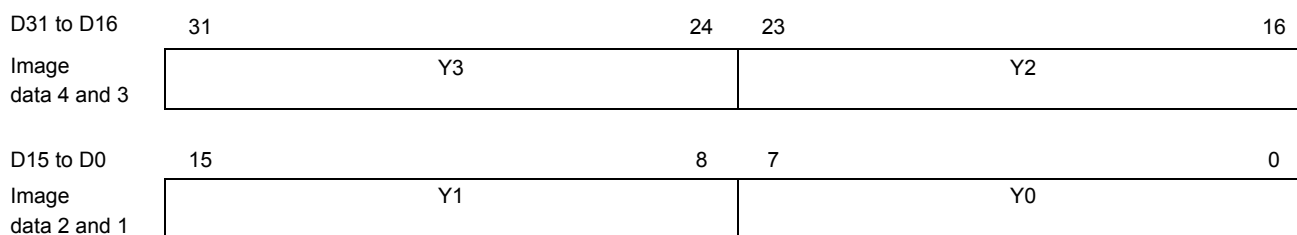
**Figure 21.20 Overview of Divided YUV Display Function (Little Endian)**

#### (1) Image Data Format

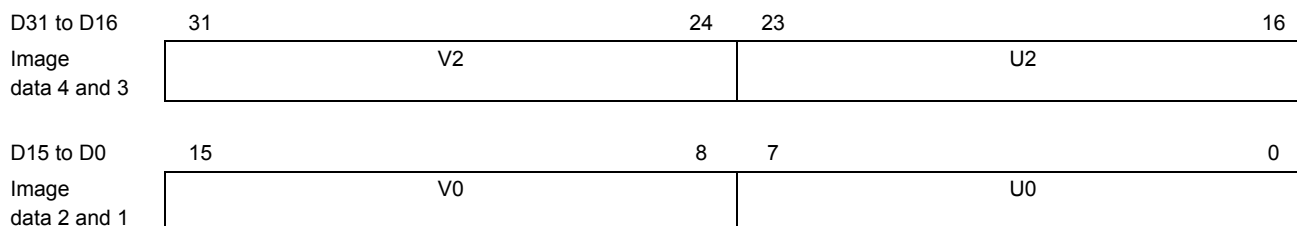
The following figures show the configuration of YUV422 data divided for separate storage in little endian in memory. The configuration of YUV420 data is the same as that shown in section 21.4.5 (5), YC: YUV420.

The formulae for YC-RGB conversion are the same as those shown in section 21.4.5 (4), YC: YUV422.

##### (a) Y data



##### (b) UV data



## (2) Register Setting Examples

Two planes are used to display the divided YUV data. The methods for specifying Y data in plane 1 and UV data in plane 2 to display the divided YUV data are described below.

- The following is the setting made by the plane n display data control 2 register m (PnDDC2Rm<sup>\*1</sup>).

### YUV422 data

Bit :	7	6	5	4	3	2	1	0
			PnNV21	PnY420			PnDIVU	PnDIVY
Plane 1 (Y data)	–	–	0	0	–	–	0	1
Plane 2 (UV data)	–	–	0	0	–	–	1	0

### YUV420 data

Bit :	7	6	5	4	3	2	1	0
			PnNV21	PnY420			PnDIVU	PnDIVY
Plane 1 (Y data)	–	–	0	0	–	–	0	1
Plane 2 (UV data)	–	–	0/1	1	–	–	1	0

- Set the start address of Y data in the plane 1 display area start address 0 to 2 registers m (P1DSA0Rm<sup>\*1</sup> to P1DSA2Rm<sup>\*1</sup>).
- Set the start address of UV data in the plane 2 display area start address 0 to 2 registers m (P2DSA0Rm<sup>\*1</sup> to P2DSA2Rm<sup>\*1</sup>).
- The same settings should be made in the plane 1 and plane 2 registers of display plane registers other than the registers described above (PnDDC2Rm<sup>\*1</sup>, P1DSA0Rm<sup>\*1</sup> to P1DSA2Rm<sup>\*1</sup>, and P2DSA0Rm<sup>\*1</sup> to P2DSA2Rm<sup>\*1</sup>). Set the PnDDF<sup>\*1</sup> bits in the plane n mode register (PnMRm<sup>\*1</sup>) to B'11.
- Set bit 20 in the display unit system control register n (DSYSRn<sup>\*2</sup>) to 1 if data is stored in big endian in memory.
- Turn on the display of planes 1 and 2, and give plane 2 the next order of priority for processing after plane 1. For details on turning on the display, see section 21.4.2, Display On/Off.

## (3) Combinations of Planes

Display as YUV422 or YUV420 data is obtained by using the combinations of planes listed below. UV data should be on the plane immediately below that for the Y data.

**Table 21.37 Possible Combinations of Planes**

Y Data Obtained by Dividing up YUV	UV Data Obtained by Dividing up YUV
Plane 1	Plane 2
Plane 2	Plane 3
Plane 3	Plane 4
Plane 4	Plane 5
Plane 5	Plane 6
Plane 6	Plane 7
Plane 7	Plane 8
Plane 8	Plane 1

- Notes: 1. m = 0 and 2, suffix "m" is only for RZ/G1H.  
n = 1 to 8.  
2. n = 0 to 2 for RZ/G1H, n = 0 and 1 for RZ/G1M/N/E.

### 21.4.21 Multiple Output Display

The 24-bit data of the DU0/DU2 display digital data (RGB888) can be multiplexed 12 bits each and output.

For a multiple output, set both the MLOS1 bit in display unit extensional function control 6 register m (DEF6Rm<sup>\*4</sup>) and the DCKOINV bit in the external synchronization control register m (ESCRm<sup>\*4</sup>) to 1.[RZ/G1H]

The 24-bit data of the DU0/DU1 display digital data (RGB888) can be multiplexed 12 bits each and output.

For a DU0 multiple output, set both the MLOS0 bit in display unit extensional function control 6 register (DEF6R) and the DCKOINV bit in the external synchronization control register 0 (ESCR0) to 1. For a DU1 multiple output, set both the MLOS1 bit in display unit extensional function control 6 register (DEF6R) and the DCKOINV bit in the external synchronization control register 1(ESCR1) to 1. [RZ/G1M/N/E]

The output dot clock should be set so that its frequency is equal to or smaller than half of the input dot clock frequency. The pin functions for a multiple output display are shown in Tables 21.38a to 21.38c.

Figure 21.21 shows the timing of the output dot clock, display control signal, and display digital data. The display control signal is output in synchronization with the falling edge of the output dot clock. As for display digital data, the Df data (Tables 21.38a to 21.38c) is output in synchronization with the falling edge of the output dot clock and the Dr data (Tables 21.38a to 21.38c) is output in synchronization with the rising edge.

**Table 21.38a Pin Functions of Multiple Output Display[RZ/G1H]**

Pin Name	DU0/DU2 Display Digital Data	
	Df Data	Dr Data
DU_DR0	DU0/DU2 digital red 0	DU0/DU2 digital green 4
DU_DR1	DU0/DU2 digital red 1	DU0/DU2 digital green 5
DU_DR2	DU0/DU2 digital red 2	DU0/DU2 digital green 6
DU_DR3	DU0/DU2 digital red 3	DU0/DU2 digital green 7
DU_DR4	DU0/DU2 digital red 4	DU0/DU2 digital blue 0
DU_DR5	DU0/DU2 digital red 5	DU0/DU2 digital blue 1
DU_DR6	DU0/DU2 digital red 6	DU0/DU2 digital blue 2
DU_DR7	DU0/DU2 digital red 7	DU0/DU2 digital blue 3
DU_DG0	DU0/DU2 digital green 0	DU0/DU2 digital blue 4
DU_DG1	DU0/DU2 digital green 1	DU0/DU2 digital blue 5
DU_DG2	DU0/DU2 digital green 2	DU0/DU2 digital blue 6
DU_DG3	DU0/DU2 digital green 3	DU0/DU2 digital blue 7

**Table 21.38b Pin Functions of Multiple Output Display [RZ/G1M/N]**

Pin Name	DU0/DU1 Display Digital Data	
	Df Data	Dr Data
DU1_DR0	DU0/DU1 digital red 0	DU0/DU1 digital green 4
DU1_DR1	DU0/DU1 digital red 1	DU0/DU1 digital green 5
DU1_DR2	DU0/DU1 digital red 2	DU0/DU1 digital green 6
DU1_DR3	DU0/DU1 digital red 3	DU0/DU1 digital green 7
DU1_DR4	DU0/DU1 digital red 4	DU0/DU1 digital blue 0
DU1_DR5	DU0/DU1 digital red 5	DU0/DU1 digital blue 1
DU1_DR6	DU0/DU1 digital red 6	DU0/DU1 digital blue 2
DU1_DR7	DU0/DU1 digital red 7	DU0/DU1 digital blue 3
DU1_DG0	DU0/DU1 digital green 0	DU0/DU1 digital blue 4
DU1_DG1	DU0/DU1 digital green 1	DU0/DU1 digital blue 5
DU1_DG2	DU0/DU1 digital green 2	DU0/DU1 digital blue 6
DU1_DG3	DU0/DU1 digital green 3	DU0/DU1 digital blue 7

**Table 21.38c Pin Functions of Multiple Output Display [RZ/G1E]**

Pin Name	DU0 Display Digital Data	
	Df Data	Dr Data
DU0_DR0	DU0 digital red 0	DU0 digital green 4
DU0_DR1	DU0 digital red 1	DU0 digital green 5
DU0_DR2	DU0 digital red 2	DU0 digital green 6
DU0_DR3	DU0 digital red 3	DU0 digital green 7
DU0_DR4	DU0 digital red 4	DU0 digital blue 0
DU0_DR5	DU0 digital red 5	DU0 digital blue 1
DU0_DR6	DU0 digital red 6	DU0 digital blue 2
DU0_DR7	DU0 digital red 7	DU0 digital blue 3
DU0_DG0	DU0 digital green 0	DU0 digital blue 4
DU0_DG1	DU0 digital green 1	DU0 digital blue 5
DU0_DG2	DU0 digital green 2	DU0 digital blue 6
DU0_DG3	DU0 digital green 3	DU0 digital blue 7



DU1 Display Digital Data		
Pin Name	Df Data	Dr Data
DU1_DR0	DU1 digital red 0	DU1 digital green 4
DU1_DR1	DU1 digital red 1	DU1 digital green 5
DU1_DR2	DU1 digital red 2	DU1 digital green 6
DU1_DR3	DU1 digital red 3	DU1 digital green 7
DU1_DR4	DU1 digital red 4	DU1 digital blue 0
DU1_DR5	DU1 digital red 5	DU1 digital blue 1
DU1_DR6	DU1 digital red 6	DU1 digital blue 2
DU1_DR7	DU1 digital red 7	DU1 digital blue 3
DU1_DG0	DU1 digital green 0	DU1 digital blue 4
DU1_DG1	DU1 digital green 1	DU1 digital blue 5
DU1_DG2	DU1 digital green 2	DU1 digital blue 6
DU1_DG3	DU1 digital green 3	DU1 digital blue 7

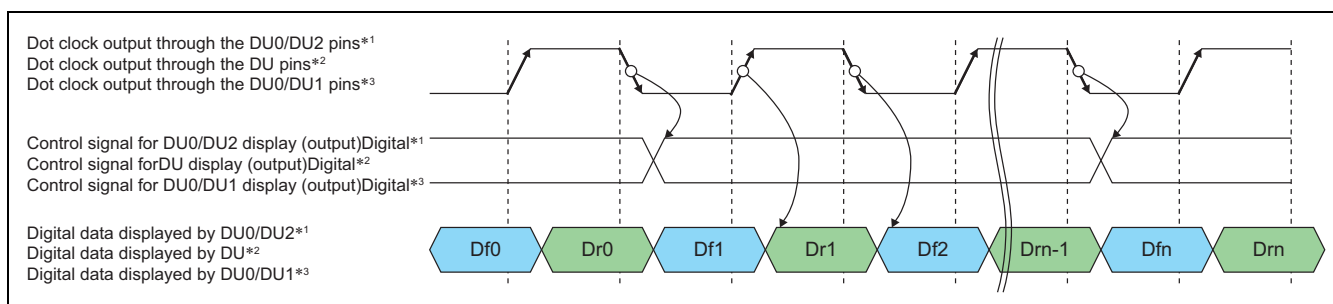


Figure 21.21 Multiple Output Display Timing

- Notes:
1. RZ/G1H is valid.
  2. RZ/G1M/N are valid.
  3. RZ/G1E is valid.
  4.  $m = 0$  and 2, suffix "m" is only for RZ/G1H.

#### 21.4.22 YC Format Display [RZ/G1M/N/E]

In addition to RGB format display, data stored in YC format can be displayed unmodified in YC format. RGB format display data can also be RGB-YC converted and displayed as YC format. Data stored in YC format cannot be superpositioned; however, different planes can be displayed on the different display areas in the divided screen.

In DU0, to display data stored in YC format unmodified in YC format, select YC format rather than RGB format by setting bits 9 and 8 in the display unit extended function control register n (DEFRn\*1). Bits 9 and 8 setting of B'10 selects 16-bit YC format display (non-multiplexed), and a setting of B'11 selects 8-bit YC format display (multiplexed). A setting of B'00 selects RGB format.

In DU0, to use RGB-YC conversion for YC format display, set the RGBYC0 bits in display unit extended function control 5 register (DEF5R). A RGBYC0 setting of B'10 selects 18-bit display (non-multiplexed), and a setting of B'01 selects 10-bit display (multiplexed).

When YC format is displayed by the timing as shown in Figure 21.22 and Figure 21.23, input 2 clocks to DCLKIN and specify division by 2. Also output 2 clocks from DCLKOUT. Both 2 clocks output and division by 2 are specified by settings in the external synchronization control register n (ESCRn\*1). Non-multiplexed YC format can be displayed in Figure 21.22a and Figure 21.22b, this setting is not required.

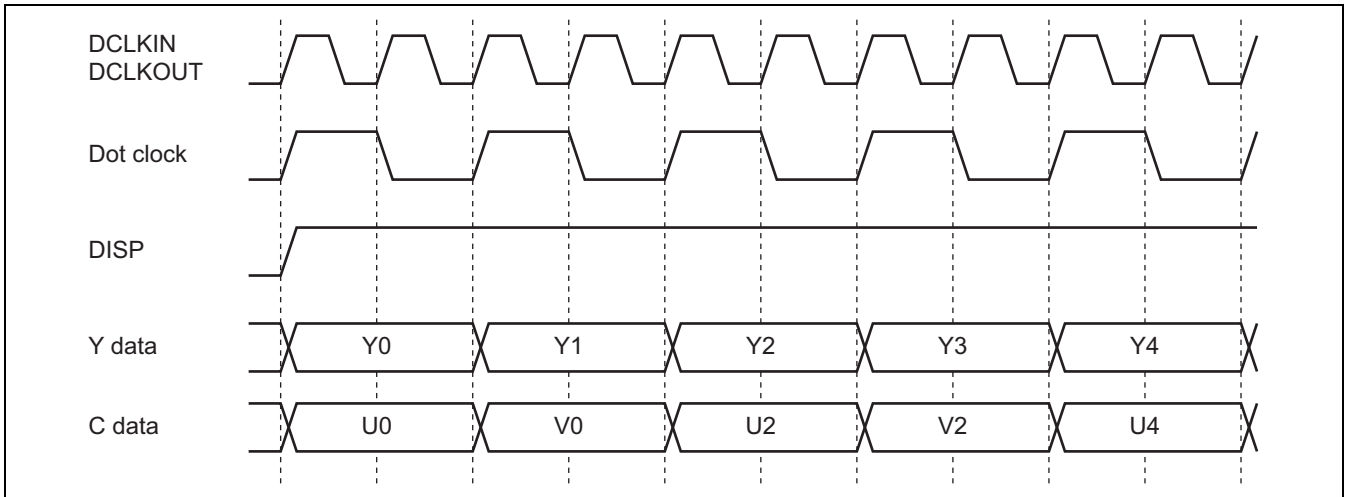


Figure 21.22 YC Non-Multiplexed

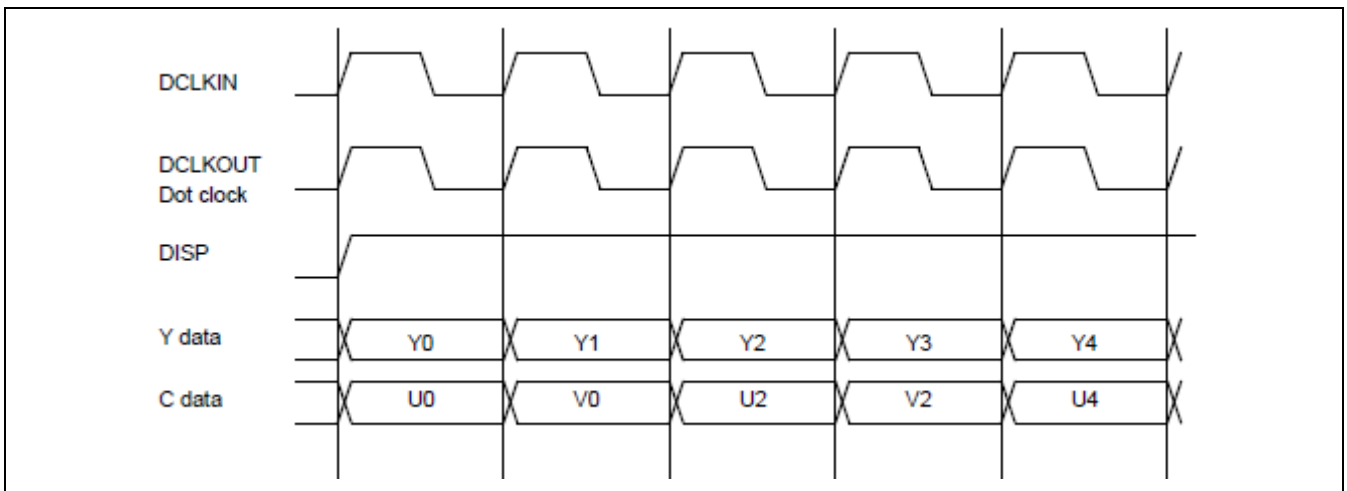


Figure 21.22a YC Non-Multiplexed (no division)

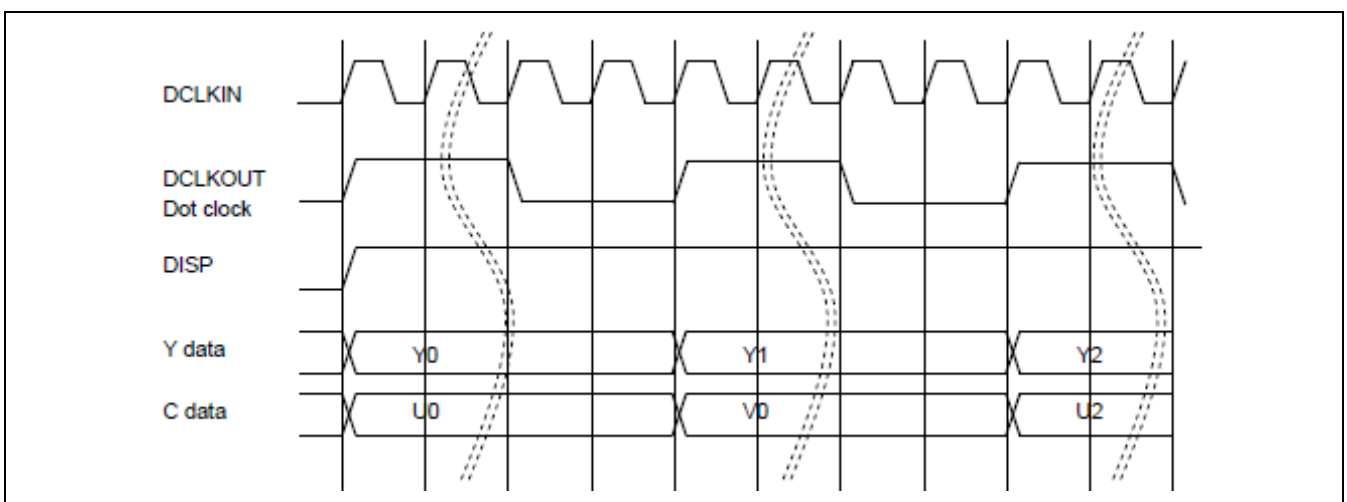


Figure 21.22b YC Non-Multiplexed (division by x)

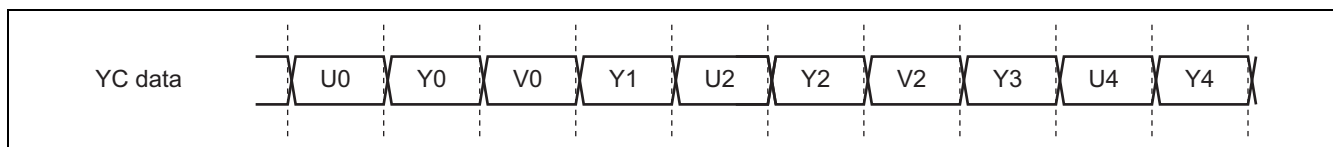


Figure 21.23 YC Multiplexed

Table 21.39a Pin Names and YC Data for YC Format Display[RZ/G1M/N]

Pin Name	YC Format Display (Only for DU1)		RGB-YC Conversion Display (Only for DU0)	
	Non-Multiplexed	Multiplexed	Non-Multiplexed	Multiplexed
DU1_DR2	Y2	Y2, C2	Y4	Y4, C4
DU1_DR3	Y3	Y3, C3	Y5	Y5, C5
DU1_DR4	Y4	Y4, C4	Y6	Y6, C6
DU1_DR5	Y5	Y5, C5	Y7	Y7, C7
DU1_DR6	Y6	Y6, C6	Y8	Y8, C8
DU1_DR7	Y7	Y7, C7	Y9	Y9, C9
DU1_DG2	C6	—	C8	—
DU1_DG3	C7	—	C9	—
DU1_DG4	—	—	Y0	Y0, C0
DU1_DG5	—	—	Y1	Y1, C1
DU1_DG6	Y0	Y0, C0	Y2	Y2, C2
DU1_DG7	Y1	Y1, C1	Y3	Y3, C3
DU1_DB2	C0	—	C2	—
DU1_DB3	C1	—	C3	—
DU1_DB4	C2	—	C4	—
DU1_DB5	C3	—	C5	—
DU1_DB6	C4	—	C6	—
DU1_DB7	C5	—	C7	—

**Table 21.39b Pin Names and YC Data for YC Format Display[RZ/G1E]**

DU0 Pin Name	DU1 Pin Name	YC Format Display (Only for DU1 Pin)		RGB-YC Conversion Display (Only for DU0 Pin)	
		Non-Multiplexed	Multiplexed	Non-Multiplexed	Multiplexed
DU0_DR2	DU1_DR2	Y2	Y2, C2	Y4	Y4, C4
DU0_DR3	DU1_DR3	Y3	Y3, C3	Y5	Y5, C5
DU0_DR4	DU1_DR4	Y4	Y4, C4	Y6	Y6, C6
DU0_DR5	DU1_DR5	Y5	Y5, C5	Y7	Y7, C7
DU0_DR6	DU1_DR6	Y6	Y6, C6	Y8	Y8, C8
DU0_DR7	DU1_DR7	Y7	Y7, C7	Y9	Y9, C9
DU0_DG2	DU1_DG2	C6	—	C8	—
DU0_DG3	DU1_DG3	C7	—	C9	—
DU0_DG4	DU1_DG4	—	—	Y0	Y0, C0
DU0_DG5	DU1_DG5	—	—	Y1	Y1, C1
DU0_DG6	DU1_DG6	Y0	Y0, C0	Y2	Y2, C2
DU0_DG7	DU1_DG7	Y1	Y1, C1	Y3	Y3, C3
DU0_DB2	DU1_DB2	C0	—	C2	—
DU0_DB3	DU1_DB3	C1	—	C3	—
DU0_DB4	DU1_DB4	C2	—	C4	—
DU0_DB5	DU1_DB5	C3	—	C5	—
DU0_DB6	DU1_DB6	C4	—	C6	—
DU0_DB7	DU1_DB7	C5	—	C7	—

Notes: 1. n = 1.

### 21.4.23 RGB → YC Color Space Conversion Formula [RZ/G1M/N/E]

The formulae for RGB-YC conversion are given below. The underlined coefficients are defined by the settings in the corresponding registers.

$$Y = \underline{YCLRP} \times R + \underline{YCLGP} \times G + \underline{YCLBP} \times B + \underline{YCLAP}$$

$$Cb = \underline{CBCLRP} \times R + \underline{CBCLGP} \times G + \underline{CBCLBP} \times B + \underline{CBCLAP}$$

$$Cr = \underline{CRCLRP} \times R + \underline{CRCLGP} \times G + \underline{CRCLBP} \times B + \underline{CRCLAP}$$

Values to be set for full scale to ITU-R BT.601 conversion are as follows.

$$Y = 0.257 \times R + 0.504 \times G + 0.098 \times B + 16$$

$$Cb = -0.148 \times R - 0.291 \times G + 0.439 \times B + 128$$

$$Cr = 0.439 \times R - 0.368 \times G - 0.071 \times B + 128$$

Values to be set for full scale to full scale conversion are as follows.

$$Y = 0.299 \times R + 0.587 \times G + 0.114 \times B + 0$$

$$Cb = -0.169 \times R - 0.331 \times G + 0.550 \times B + 128$$

$$Cr = 0.500 \times R - 0.419 \times G - 0.081 \times B + 128$$

## 21.5 Display Control

RZ/G1H

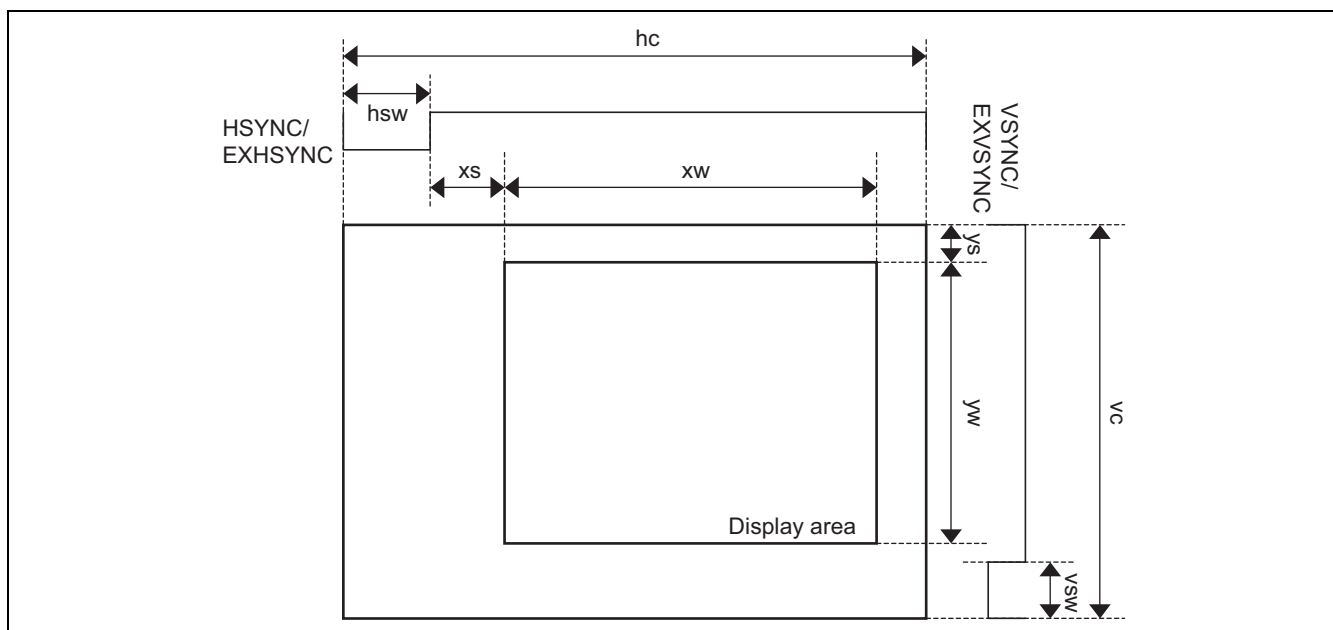
RZ/G1N

RZ/G1M

RZ/G1E

### 21.5.1 Display Timing Generation

In the display unit (DU), display timing is generated for the horizontal direction and vertical direction of the display screen. Display timing is set by using display timing generation registers in section 21.3.2. Figure 21.24 shows the display timing in non-interlaced mode. Here, the display screen is defined in terms of the variables of Table 21.40.



**Figure 21.24 Display Timing Generation for Horizontal Direction and Vertical Direction of Display Screen**

**Table 21.40 Variables Defined in Display Screen**

Variables	Contents	Units
hc*1	Horizontal scan period	Dot clock
hsw	Horizontal sync pulse width	Dot clock
xs	From rise of HSYNC to display start position in the horizontal direction of the display screen	Dot clock
xw	Display width per 1 raster of display screen	Dot clock
vc*2	Vertical scan period	Raster line
vsw	Vertical sync pulse width	Raster line
ys	From rise of VSYNC to display start position in the vertical direction of the display screen	Raster line
yw	Vertical display period of display screen	Raster line

Notes: 1. Should be set such that  $hsw + xs + xw < hc$   
 2. Should be set such that  $vsw + ys + yw < vc$

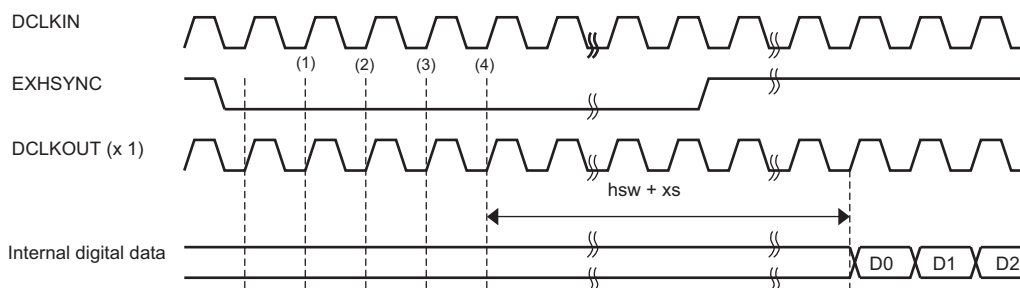
The display timing generation register settings are different depending on the scan method and synchronization method. Hence the value of the display timing generation registers should be set after performing calculations like those indicated in Table 21.41.

**Table 21.41 Correspondence Table of Settings of Display Timing Generation Registers**

Register Name	Bit Name	Synchronization Method	
		Master Mode	TV Sync Mode
Horizontal display start register n (HDSRn)	HDS	$hsw + xs - 19^{*5}$	$hsw + xs - 25^{*2*5}$
Horizontal display end register n (HDERn)	HDE	$hsw + xs - 19^{*5} + xw$	$hsw + xs - 25 + xw^{*2*5}$
Vertical display start register n (VDSRn)	VDS	$ys - 2^{*3}$	$ys - 2^{*3}$
Vertical display end register n (VDERn)	VDE	$ys - 2 + yw$	$ys - 2 + yw$
Horizontal synch width register n (HSWRn)	HSW	$hsw - 1$	$hsw - 1$
Horizontal cycle register n (HCRn)	HC	$hc - 1$	$hc - 1$
Vertical synch point register n (VSPRn)	VSP	$vc - vsw - 1$	$vc - vsw - 1$
Vertical cycle register n (VCRn)	VC	$vc - 1$	$vc - 1$

Notes: n = 0 to 2 for RZ/G1H; n = 0 and 1 for RZ/G1M/N/E

1. In all scan modes, VDS, VDE, VSP, VC settings are in single-field units.
2. The values of HDS and HDE are from the fourth rising edge of DCLKOUT after detection of the falling edge of EXHSYNC through the rising edge of DCLKOUT.



3. VDS should be set to 1 or greater.
4. HC should be set so as to satisfy  $HC > HDE$ .
5. If the function below is used, the following correction value is subtracted from both HDS and HDE in Table 21.41.

- When using the RGB-YC conversion function (RGBYC0 bits in the display unit extensional function control 5 register (DEF5R) are set to 1), 3 should be subtracted. [RZ/G1M/N/E]
- When using the YC-RGB conversion function (YCRGB0 or YCRGB1 bits in the display unit extensional function control 5 register m (DEF5Rm\*) are set to 1), 3 should be subtracted. [RZ/G1H]
- When using the DRC function (DRC0 or DRC1 bits in the display unit extensional function control 5 register (DEF5Rm\*) are set to 1), 3 should be subtracted. [RZ/G1H]

Note: \* m = 0 and 2, suffix "m" is only for RZ/G1H.

### 21.5.2 CSYNC

In master mode, a CSYNC (composite sync) signal is output. EQWRn\* is used to set the low-level pulse width of the CSYNC equivalent pulse. SPWRn\* is used to set the low-level pulse width of the CSYNC serration pulse.

The CSYNC waveform is selected using the CSY bit in DSMRn\*.

Note: \* n = 0 to 2 for RZ/G1H, n = 0 and 1 for RZ/G1M/N/E

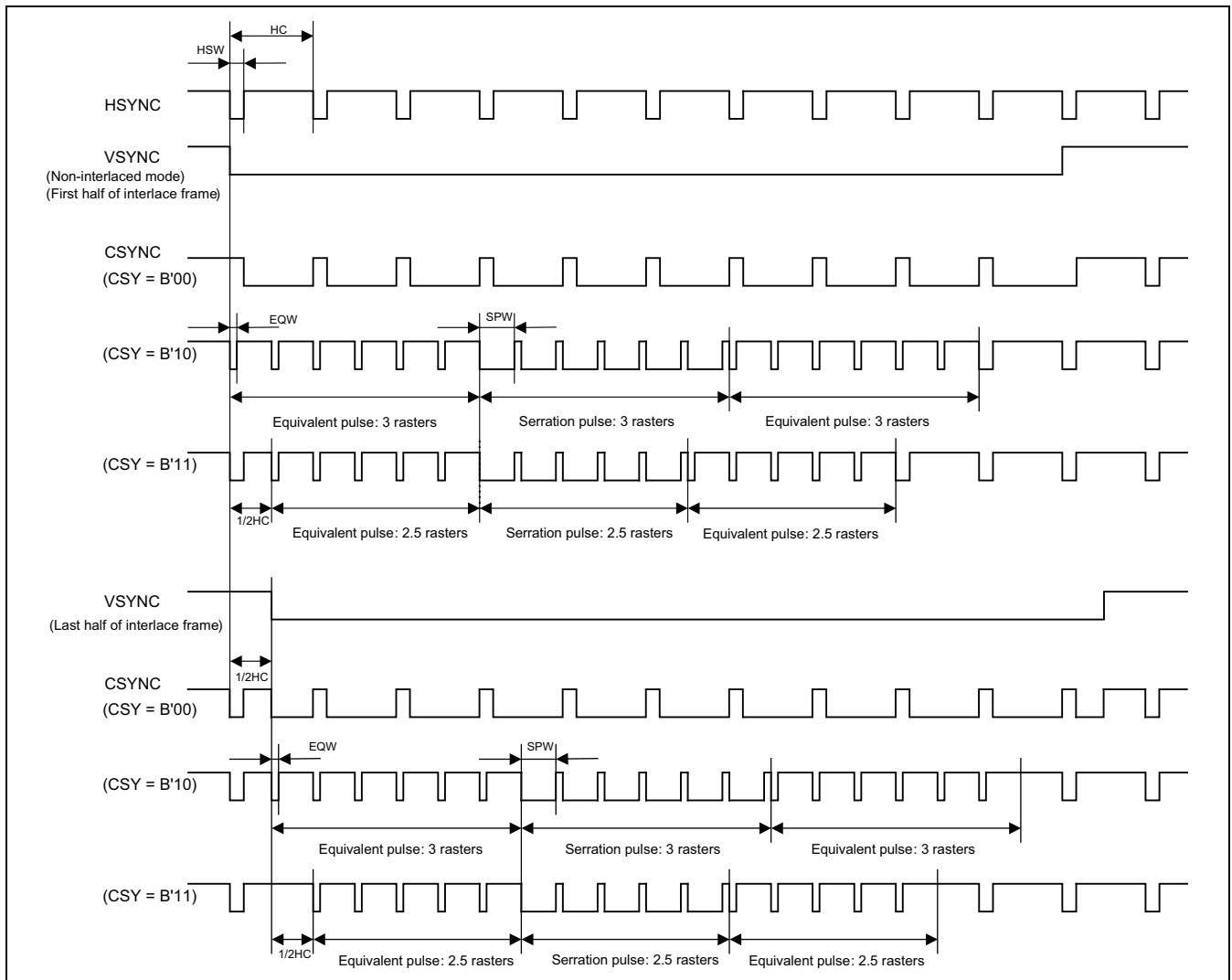


Figure 21.25 CSYNC Timing Chart

### 21.5.3 Scan Method

The scan method can be selected from among non-interlaced mode, interlaced sync mode, and interlaced sync & video mode. The mode is selected using bit 5 and bit 4 in DSYSRn\*.

- Non-interlaced mode  
In this scan method, one frame consists of a single field.
- Interlaced sync mode  
In this scan method, one frame consists of two fields. The two fields are an even field and an odd field, displaying the same data.
- Interlaced sync & video mode  
In this scan method, one frame consists of two fields. The two fields are an even field and an odd field, displaying different data.

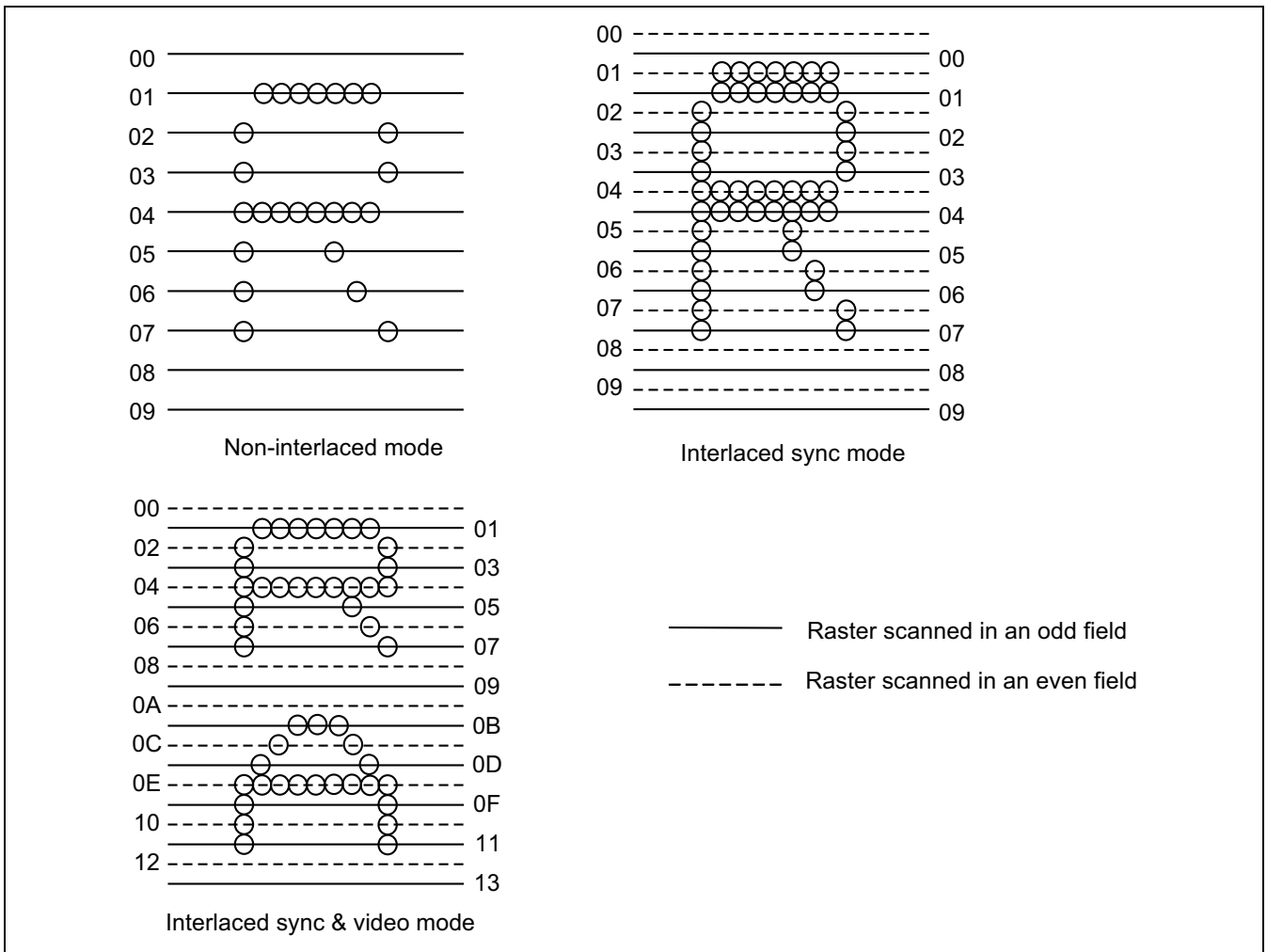
The ODEV bit in DSMRn\* is used to set the display order of fields in interlaced sync mode and in interlaced sync & video mode. When the ODEV bit is 0, the display order for one frame is odd field, then even field; when the ODEV bit is 1, the order for one frame is even field, then odd field.

In master mode, high level is output from the ODDF pin during even field display, and low level is output during odd field display. In TV sync mode, high level is input to the EXODDF pin to cause display of the even field, and low level is input to cause display of the odd field.

Notes: When non-interlaced mode is selected in TV sync mode, the EXODDF pin should be fixed at low level or high level.

\* n = 0 to 2 for RZ/G1H, n = 0 and 1 for RZ/G1M/N/E.





**Figure 21.26 Example of Display in Each Scan Mode**

- Example of vertical scan period  
 Non-interlaced mode: 1/60 second/field, 1/30 second/field  
 Interlaced sync mode: 1/30 second/frame  
 Interlaced sync & video mode: 1/30 second/frame
- Display in non-interlaced method  
 In this method, all lines are displayed at once without providing intervals between input video signals.  
 This input method is for monitors capable of high-resolution display.

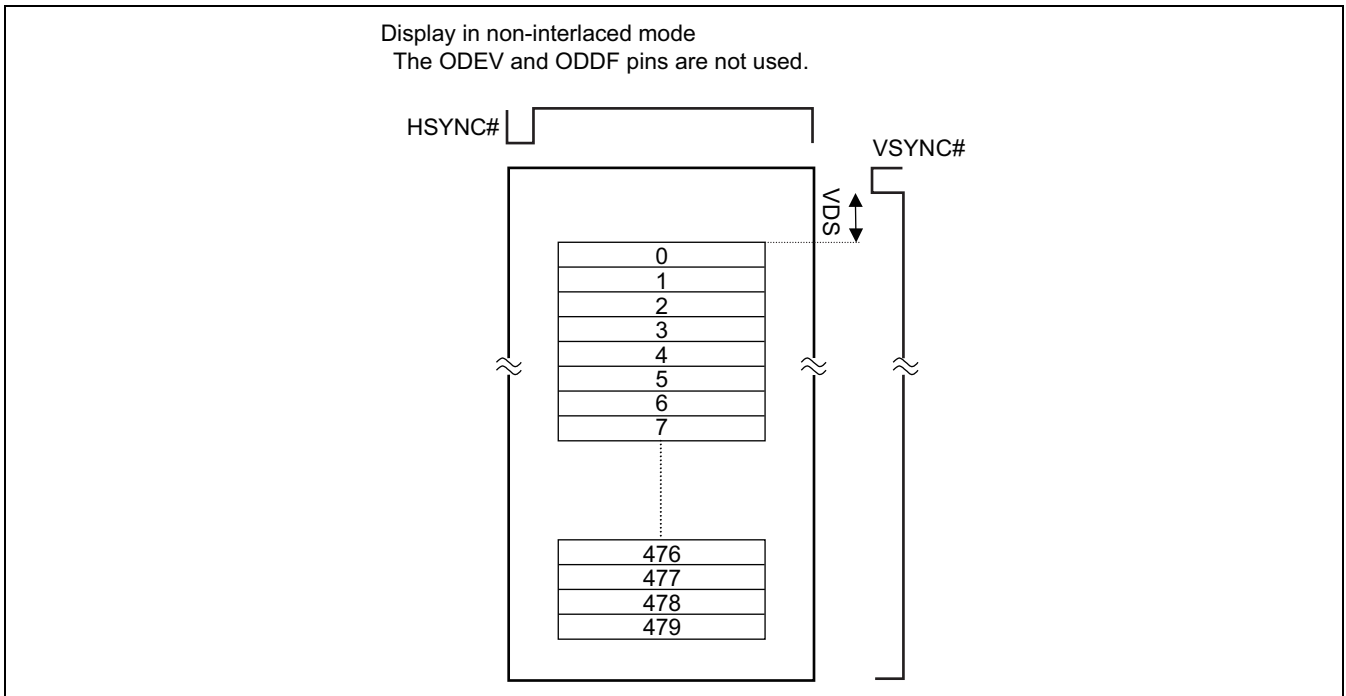


Figure 21.27 Display in Non-Interlaced Method

• Display in interlaced method

At every scan period VC of the input video signal, even lines and odd lines are switched and displayed in alternation, and a single screen (one frame) is combined and displayed (with the afterimage of the preceding VC) with a period of 2VC. This is a basic TV input method.

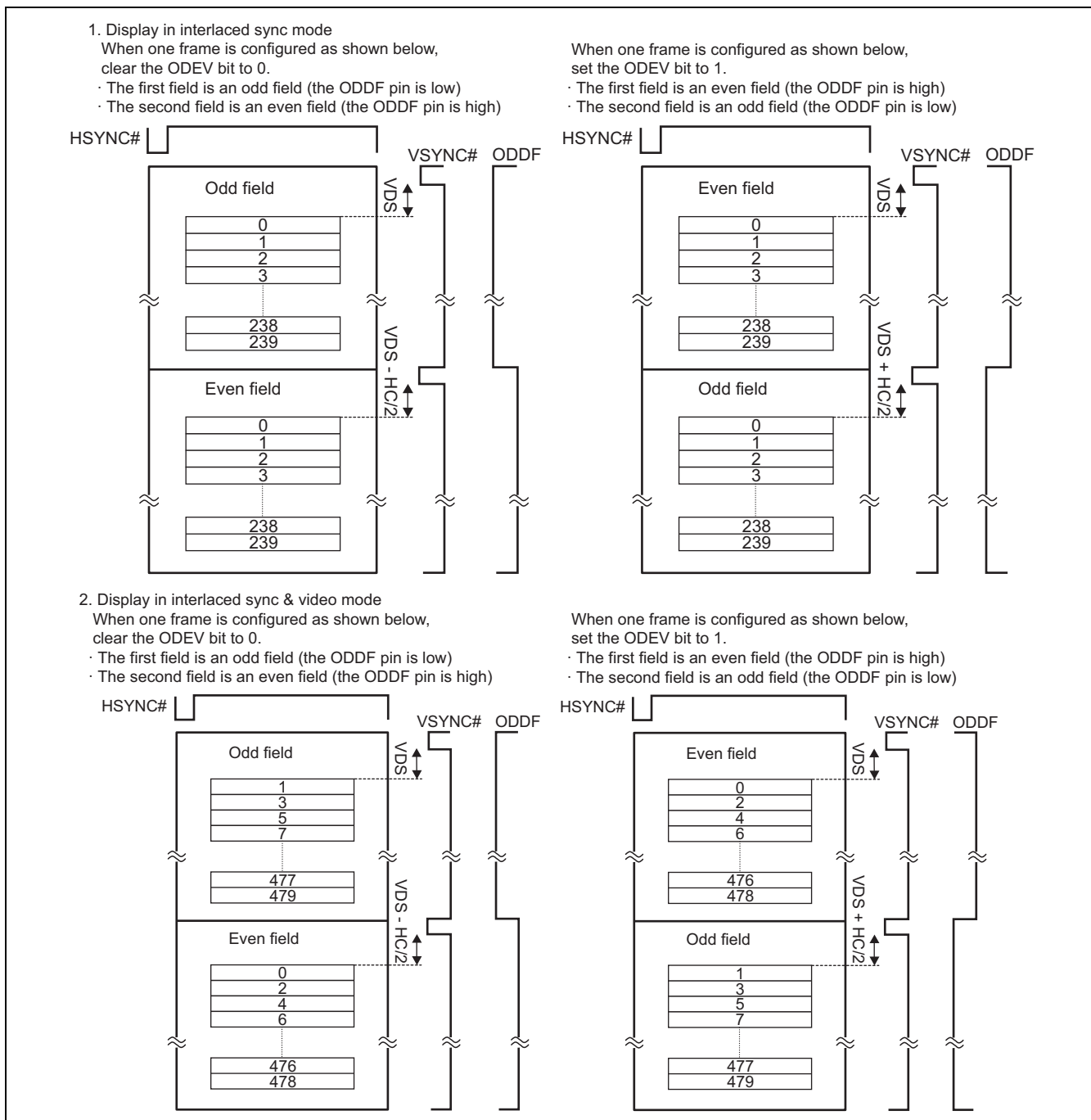


Figure 21.28 Display in Interlaced Method

### 21.5.4 Color Detection

When output display data matches a color set in CDERn\*<sup>1</sup>, high level is output from the CDE pin. The CDEM bit in DSMRn\*<sup>1</sup> can be used to fix the level outside display intervals. Also, the CDEL bit in DSMRn\*<sup>1</sup> can be used to select the polarity of the output level.

When the following display functions are set, the color detection function cannot be used.

- DRC processing performed by setting the DRC0 bits in the display unit extensional function control 5 register m (DEF5Rm\*<sup>2</sup>) [RZ/G1H]
- DRC processing performed by setting the DRC1 bits in the display unit extensional function control 5 register m (DEF5Rm\*<sup>2</sup>) [RZ/G1H]
- YC-RGB conversion performed by setting the YCRGB0 bits in the display unit extensional function control 5 register m (DEF5Rm\*<sup>2</sup>) [RZ/G1H]
- YC-RGB conversion performed by setting the YCRGB1 bits in the display unit extensional function control 5 register m (DEF5Rm\*<sup>2</sup>) [RZ/G1H]
- RGBYC processing performed by setting the RGBYC0 bits in the display unit extensional function control 5 register (DEF5R) [RZ/G1M/N/E]

Notes: 1. n = 0 to 2 for RZ/G1H, n = 0 and 1 for RZ/G1M/N/E.  
2. m = 0 and 2, suffix "m" is only for RZ/G1H.

**Table 21.42 Output Level of the CDE Pin**

CDEL	CDEM	The CDE pin in display intervals		The CDE pin outside display intervals	
		Result of Comparison of Output Display Data and Color Detection Register		Value of Color Detection Register*	
		Same	Different	0	Other than 0
0	B'00	High level	Low level	High level	Low level
0	B'01	High level	Low level	High level	Low level
0	B'10	High level	Low level	Low level	Low level
0	B'11	High level	Low level	High level	High level
1	B'00	Low level	High level	Low level	High level
1	B'01	Low level	High level	Low level	High level
1	B'10	Low level	High level	High level	High level
1	B'11	Low level	High level	Low level	Low level

Note: \* Output display data is 0 outside display intervals.

### 21.5.5 External Sync Control

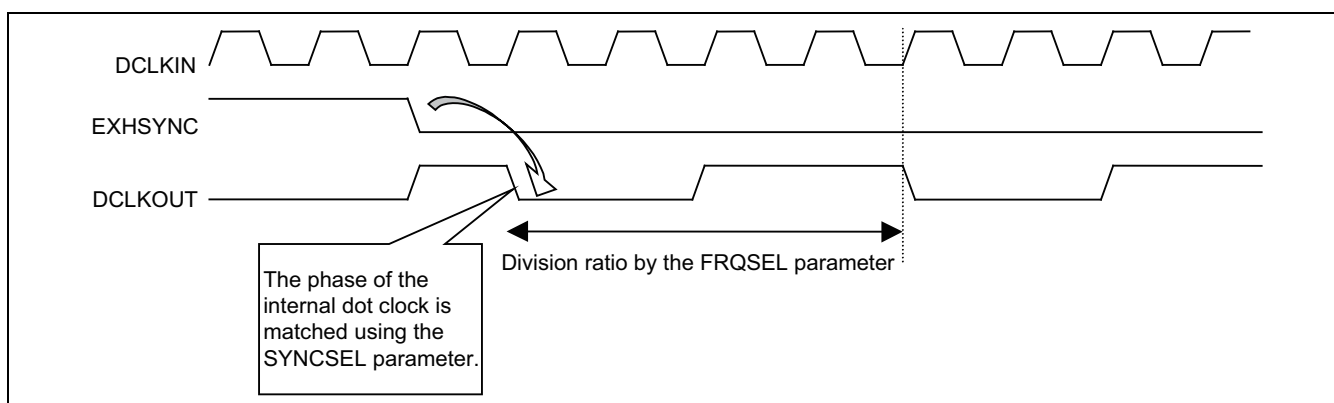
In TV-sync mode, the display unit (DU) is capable of using an externally input dot clock (clock signal for frequency multiplication: DCLKIN) to generate a dot clock (output dot clock: DCLKOUT) that is in accord with external synchronizing signals (EXHSYNC, EXVSYNC). Supply the externally input dot clock (multiplication clock: DCLKIN) and set the following parameters in ESCRn\*.

**Table 21.43 External Sync Control Parameters**

Variable	Function
ESCRn*/SYNCSEL	Selects the sync signal (EXHSYNC or EXVSYNC) to use in phase matching of the dot clock.
ESCRn*/FRQSEL	Selects the dot-clock division ratio.

1. Use the SYNCSEL bits of ESCRn\* to set the sync timing of the dot clock (output dot clock: DCLKOUT) generated from the internal dot clock.
2. Use the FRQSEL bits of ESCRn\* to set the division ratio for generation of the internal dot clock. The following figure shows the internal dot clock timing where the input dot clock has been synchronized with EXHSYNC and then divided by four.

Note \* n = 0 to 2 for RZ/G1H, n = 0 and 1 for RZ/G1M/N/E.



**Figure 21.29 DCLKOUT Timing Chart where DCLKIN Synchronized with EXHSYNC is divided by Four**

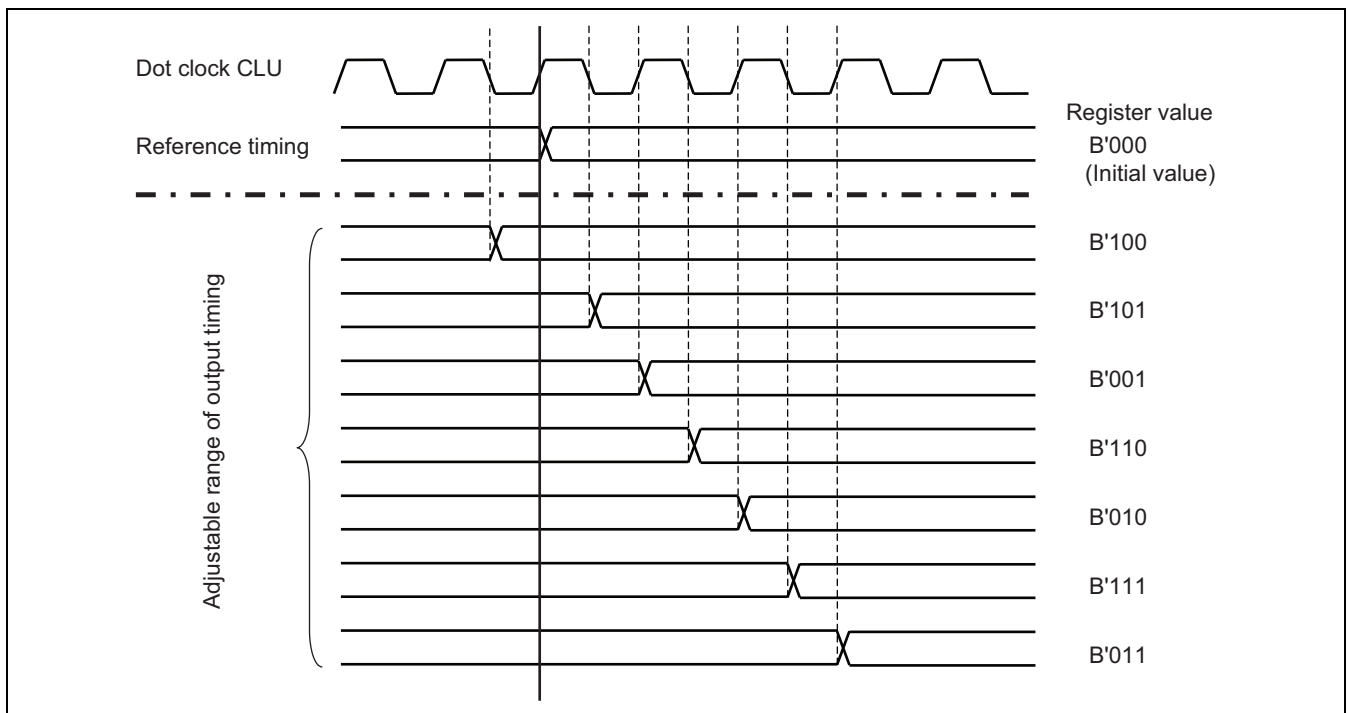
### 21.5.6 Output Signal Timing Adjustment

The display unit (DU) enables selection of output timing, with respect to the output dot clock, of the various output signals (the four sync signals HSYNC, VSYNC, CSYNC, ODDF, as well as DISP, CDE, CLAMP, DE, digital RGB signals). Timing is selected by setting OTARn\*.

Note \* n = 0 to 2 for RZ/G1H, n = 0 and 1 for RZ/G1M/N/E.

**Table 21.44 Output Signal Timing Setting Parameters**

Variable	Description
SYNCA	Sets output timing of the HSYNC, VSYNC, CSYNC, ODDF signal
DISPA	Sets output timing of the DISP signal
CDEA	Sets output timing of the CDE signal
DRGBA	Sets output timing of digital RGB signal
CLAMPA	Sets output timing of the CLAMP signal
DEA	Sets output timing of the DE signal



**Figure 21.30 Adjustable Range of Output Timing**

## 21.6 Notes on Usage

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

### 21.6.1 Module Standby Mode

Module Standby mode, in which supply of the clock signal to the display unit (DU) is stopped, is supported.

Even when the display unit (DU) enters the standby mode, the register values are retained. Do not access the display unit (DU) during periods in standby mode.

### 21.6.2 Transition to Module Standby Mode

1. Set both the DEN and DRES bits in DSYSRm\*<sup>1</sup> to 0 to stop access to the AXI.
2. Test bit 11 in DSSRn\*<sup>2</sup> to confirm the next VBK flag. The setting made in step 1 becomes effective with the timing of VBK and access to AXI is stopped. The value of the display data becomes the value set in DOORn\*<sup>2</sup>  
When DU0, DU1 and DU2 are running, test bit 11 of all of DSSR0, DSSR1 and DSSR2. [RZ/G1H]  
When DU0 and DU1 are running, test bit 11 of both DSSR0 and DSSR1.
3. Stop the clock.
4. When the DRC is running, after step 3, stop the clock of the module to be stopped. [RZ/G1H]

Notes: 1. m = 0 and 2 for RZ/G1H, m = 0 for RZ/G1M/N/E.  
2. n = 0 to 2 for RZ/G1H, n = 0 and 1 for RZ/G1M/N/E.

### 21.6.3 Release from Module Standby Mode and Restarting Display

1. When running the DRC, start the clock of the module to be run. [RZ/G1H]
2. Start the clock.
3. Make settings to turn the display on by setting the DEN and DRES bits in DSYSRm\* to 1 and 0 respectively.

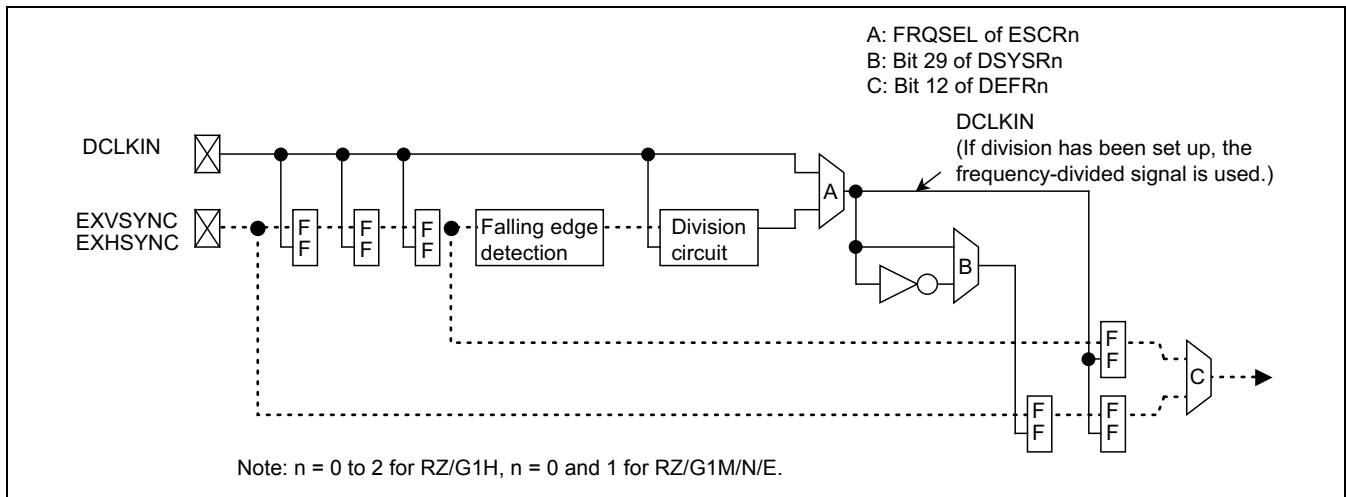
Note: \* 1: m = 0 and 2 for RZ/G1H, m = 0 for RZ/G1M/N/E.

### 21.6.4 Acquisition of External Sync Signal

The following three ways of acquiring the external SYNC signal are available.

- (a) The SYNC signal is acquired on rising edges of DCLKIN (or the frequency-divided clock signal derived from this if division has been set up).
- (b) The SYNC signal is acquired on falling edges of DCLKIN (or the frequency-divided clock signal derived from this if division has been set up).
- (c) Assuming that division has been set up, the SYNC signal that is acquired by the pre-division clock signal is latched on edges of the frequency-divided clock signal.

The electrical characteristics (AC spec.) are only guaranteed for case (a) above. There is no guarantee of electrical characteristics (AC spec.) for cases (b) and (c).



**Figure 21.31 Diagram of Circuit that Generates the Display Timing from an External Sync Signal**

### 21.6.5 Restrictions on Changing the Synchronization of the External SYNC Signal

When electrical characteristics (AC spec.) related to the acquisition of an external signal are not satisfied, ensure an interval of at least two cycles between changes of EXHSYNC or EXVSYNC, i.e. the external SYNC signals.

The frequency-divided dot clock is used as the basis of the cycle period when bit 12 of DEFRn\* is 0. The pre-division dot clock is used when bit 12 is 1.

Note: \* n = 0 to 2 for RZ/G1H, n = 0 and 1 for RZ/G1M/N/E.

### 21.6.6 Note on Register Settings

At the time of a reset, some registers of the DU have fixed initial values but others do not. The initial values of the latter when the power for the LSI is turned on can be either 0 or 1. From the initial state after power is switched on, be sure to set all of the registers in the DU to the desired values before starting synchronization of the display\*<sup>1</sup>.

If turning on the display\*<sup>2</sup>,  $\alpha$  planes\*<sup>3</sup>, or capturing\*<sup>4</sup> is attempted while values in registers are unknown, operation may be incorrect due to access by the DU to areas other than those intended (the DU is capable of access to any area).

- Notes:
- Setting (a) or (b) starts synchronization of the display.
    - The DRES and DEN bits in DSYSRm\*<sup>5</sup> are B'00.
    - The DRES and DEN bits in DSYSRm\*<sup>5</sup> are B'01.
  - Setting (a) or (b) turns the display on.
    - When the DPRS bit in DORCRm\*<sup>6</sup> is 0:  
With setting (b) in note 1, setting any of bits DPE8 to DPE1 in DPPRm\*<sup>6</sup> to 1.
    - When the DPRS bit in DORCRm\*<sup>6</sup> is 1:  
With setting (b) in note 1, setting bits S0S8 to S0S1 in DS0PRm\*<sup>6</sup> or bits S1S8 to S1S1 in DS1PR to any value from B'0001 to B'1000.
  - $\alpha$  planes are turned on by the combination of setting (b) in note 1 and any of bits AP2E or AP1E in DAPCRm\*<sup>6</sup> being set to 1.
  - Capturing is turned on by the combination of setting (b) in note 1 and the DC2E or DCE bit in DCPCRm\*<sup>6</sup> being set to 1.
  - m = 0 and 2 for RZ/G1H, m = 0 for RZ/G1M/N/E.
  - m = 0 and 2 for RZ/G1H, suffix "m" is only for RZ/G1H.



## 22. LVDS Interface

RZ/G1H	RZ/G1N
RZ/G1M	RZ/G1E

### 22.1 Overview

The LVDS (low voltage differential signaling) module converts an RGB signal output by the DU module to the LVDS format and outputs those signals.

The LVDS interface supports 8 output data formats with the conversion formats selected by register settings. The output control signals can also be selected freely.

#### 22.1.1 Features

This module has the following features.

- Output pins: Five differential output pairs (4 data and 1 clock) that conform to the TIA/EIA-644 standard.
- Operating frequency: A maximum dot clock frequency of 31 to 148.5 MHz
- Supports eight output data formats

#### 22.1.2 Block Diagram

Figures 22.1a and 22.1b show the block diagrams of the LVDS module.

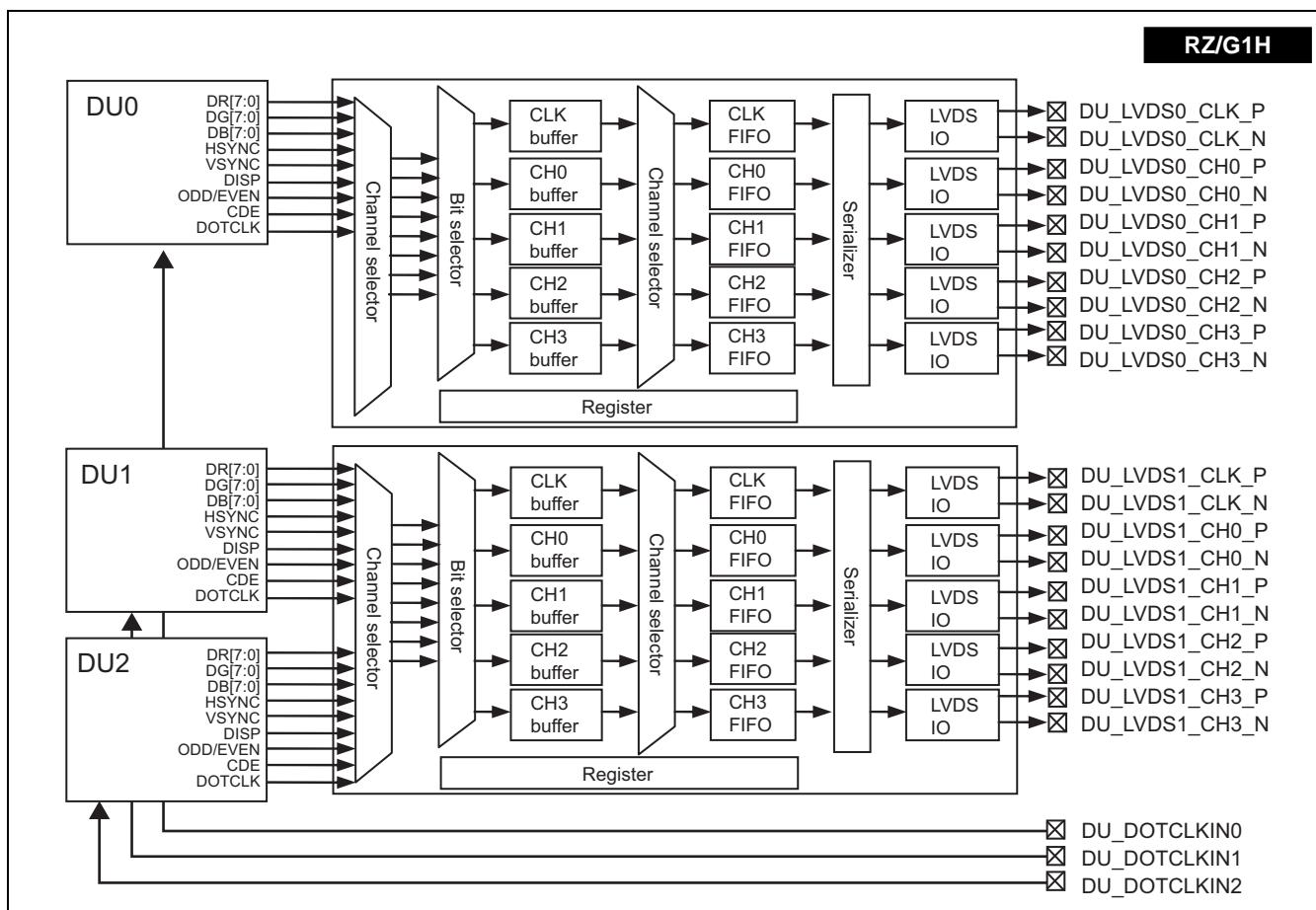


Figure 22.1a LVDS Block Diagram [RZ/G1H]

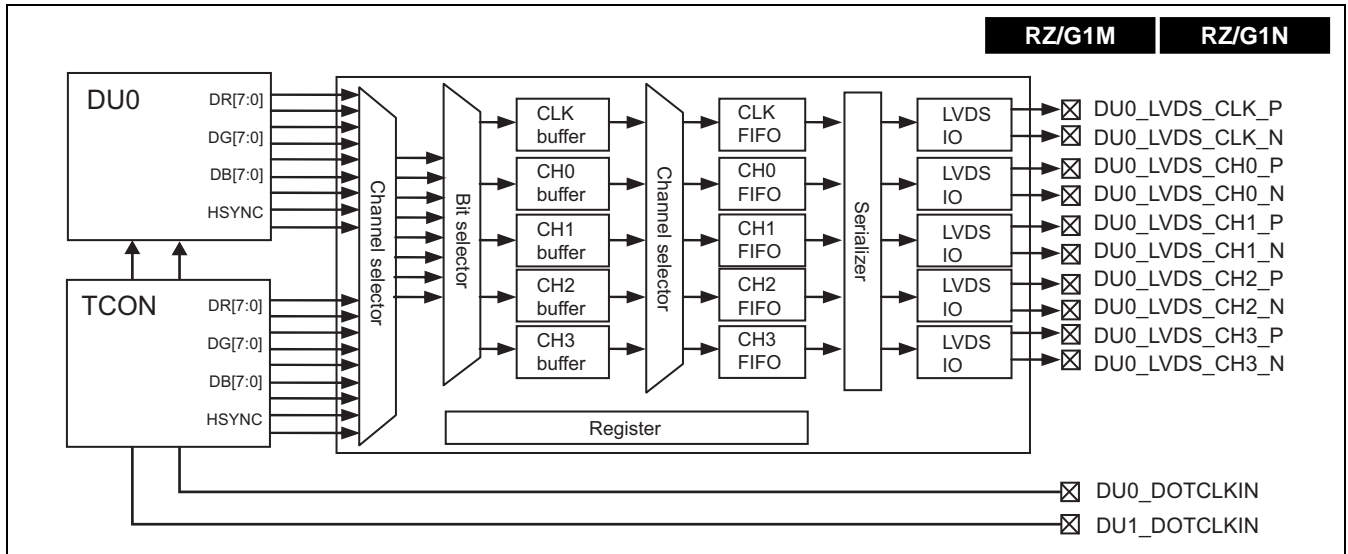


Figure 22.1b LVDS Block Diagram [RZ/G1M, RZ/G1N]

### 22.1.3 Input/Output Pins

**Table 22.1 Pin Configuration**

Pin Name	I/O	Description
DU_LVDS0_CLK_P [RZ/G1H] DU0_LVDS_CLK_P [RZ/G1M, RZ/G1N]	Output	LVDS differential clock (pos)
DU_LVDS0_CLK_N [RZ/G1H] DU0_LVDS_CLK_N [RZ/G1M, RZ/G1N]	Output	LVDS differential clock (neg)
DU_LVDS0_CH0_P [RZ/G1H] DU0_LVDS_CH0_P [RZ/G1M, RZ/G1N]	Output	LVDS differential Ch0 data (pos)
DU_LVDS0_CH0_N [RZ/G1H] DU0_LVDS_CH0_N [RZ/G1M, RZ/G1N]	Output	LVDS differential Ch0 data (neg)
DU_LVDS0_CH1_P [RZ/G1H] DU0_LVDS_CH1_P [RZ/G1M, RZ/G1N]	Output	LVDS differential Ch1 data (pos)
DU_LVDS0_CH1_N [RZ/G1H] DU0_LVDS_CH1_N [RZ/G1M, RZ/G1N]	Output	LVDS differential Ch1 data (neg)
DU_LVDS0_CH2_P [RZ/G1H] DU0_LVDS_CH2_P [RZ/G1M, RZ/G1N]	Output	LVDS differential Ch2 data (pos)
DU_LVDS0_CH2_N [RZ/G1H] DU0_LVDS_CH2_N [RZ/G1M, RZ/G1N]	Output	LVDS differential Ch2 data (neg)
DU_LVDS0_CH3_P [RZ/G1H] DU0_LVDS_CH3_P [RZ/G1M, RZ/G1N]	Output	LVDS differential Ch3 data (pos)
DU_LVDS0_CH3_N [RZ/G1H] DU0_LVDS_CH3_N [RZ/G1M, RZ/G1N]	Output	LVDS differential Ch3 data (neg)
DU_LVDS1_CLK_P [RZ/G1H]	Output	LVDS differential clock (pos)
DU_LVDS1_CLK_N [RZ/G1H]	Output	LVDS differential clock (neg)
DU_LVDS1_CH0_P [RZ/G1H]	Output	LVDS differential Ch0 data (pos)
DU_LVDS1_CH0_N [RZ/G1H]	Output	LVDS differential Ch0 data (neg)
DU_LVDS1_CH1_P [RZ/G1H]	Output	LVDS differential Ch1 data (pos)
DU_LVDS1_CH1_N [RZ/G1H]	Output	LVDS differential Ch1 data (neg)
DU_LVDS1_CH2_P [RZ/G1H]	Output	LVDS differential Ch2 data (pos)
DU_LVDS1_CH2_N [RZ/G1H]	Output	LVDS differential Ch2 data (neg)
DU_LVDS1_CH3_P [RZ/G1H]	Output	LVDS differential Ch3 data (pos)
DU_LVDS1_CH3_N [RZ/G1H]	Output	LVDS differential Ch3 data (neg)
DU_DOTCLKIN0 [RZ/G1H] DU0_DOTCLKIN [RZ/G1M, RZ/G1N]	Input	LVDS Dotclk input (31 to 148.5 MHz)*
DU_DOTCLKIN1 [RZ/G1H] DU1_DOTCLKIN [RZ/G1M, RZ/G1N]	Input	LVDS Dotclk input (31 to 148.5 MHz)*
DU_DOTCLKIN2 [RZ/G1H]	Input	LVDS Dotclk input (31 to 148.5 MHz)*

Note: \* Either an internal clock or the LVDS\_DOTCLKIN clock can be used as the LVDS Dotclk. The DU register is used to select the clock source and the clock divisor. See section 22.3.4, Dotclk Settings, for details.

The state of the LVDS pin is determined by the LVDCR register.

**Table 22.2 Pin State**

Bit Name		Pin State	Notes
LVRES	LVEN		
0	0	X (Irrelevant (L or H))	Set at reset and as the initial value.
0	1	Hi-Z (High Impedance)	When the display is off.
1	0	L (DU_LVDS_xxx_P), H (DU_LVDS_xxx_N)	Operation is not guaranteed.
1	1	Output	During normal operation.

## 22.2 Register Description

Table 22.3 lists the register configuration. Only use the longword access size to access these registers. Operation is not guaranteed if any access size other than longword is used to access these registers.

**Table 22.3 Register Configuration**

Name	Abbreviation	R/W	LVDS0 Address	LVDS1 Address [Only RZ/G1H]	Access Size	RZ/G Series Products			
						RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
LVDS control register 0	LVDCR0	R/W	H'FEB9 0000	H'FEB9 4000	32	√	√	√	—
LVDS control register 1	LVDCR1	R/W	H'FEB9 0004	H'FEB9 4004	32	√	√	√	—
PLL control register	LVDPLLCR	R/W	H'FEB9 0008	H'FEB9 4008	32	√	√	√	—
CTR control register	LVDCTRCR	R/W	H'FEB9 000C	H'FEB9 400C	32	√	√	√	—
CH control register	LVDCHCR	R/W	H'FEB9 0010	H'FEB9 4010	32	√	√	√	—

**Table 22.4 Register States in the Various Processing Modes**

Name	Abbreviation	Power-On Reset	Module Standby	RZ/G Series Products			
				RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
LVDS control register 0	LVDCR0	H'0000 0000	Retained	√	√	√	—
LVDS control register 1	LVDCR1	H'0000 0000	Retained	√	√	√	—
PLL control register	LVDPLLCR	H'0000 0000	Retained	√	√	√	—
CTR control register	LVDCTRCR	H'0000 0000	Retained	√	√	√	—
CH control register	LVDCHCR	H'0000 0000	Retained	√	√	√	—

[Legend]

Initial value: Register value after a reset

—: Undefined value

R/W: Readable/writable. The written value can be read.

R: Read-only. The write value should always be 0.

### 22.2.1 LVDS Control Register 0 (LVDCR0)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DU SEL	—	—	DMD	LVMD			—	—	—	PLL ON	—	BEN	LVEN	LVRES	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R	R	R	R/W	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15	DUSEL	0	R/W	[RZ/G1H] DU Channel Select Selects the DU channel for LVDS input. LVDS0: [RZ/G1H] 0: DU0 is selected. 1: Setting prohibited. LVDS1: [RZ/G1H] 0: DU1 is selected. 1: DU2 is selected. [RZ/G1M, RZ/G1N] DU Channel Select Selects the DU channel for LVDS input. 0: DU0 is selected. 1: Setting prohibited.
14, 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12	DMD	0	R/W	Double Edge Input Select Selects the DU output mode for LVDS input (only valid for DU0). 0: One edge mode 1: Both edge mode (DU dotclk frequency is the double of LVDS dotclk)

Bit	Bit Name	Initial Value	R/W	Description
11 to 8	LVMD	0000	R/W	LVDS Mode Selects the LVDS module output data format (see Figure 22.2). 0000: MODE0 0001: MODE1 0010: MODE2 0011: MODE3 0100: MODE4 0101: MODE5 0110: MODE6 0111: MODE7 All other values: Setting prohibited
7 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	PLLON	0	R/W	PLL Enable Controls the PLL operation. 0: PLL stopped. 1: PLL operates.
3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
2	BEN	0	R/W	BIAS Enable Controls the LVDS BIAS circuit operation. 0: BIAS circuit stopped. 1: BIAS circuit operates.
1	LVEN	0	R/W	LVDS Enable Bit Controls the LVDS operation. 0: Stopped 1: Normal operation
0	LVRES	0	R/W	LVDS Reset Bit Controls the LVDS output. 0: Output off 1: Output on

**22.2.2 LVDS Control Register 1 (LVDCR1)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CKSEL	—	—	—	—	—	CH3STBY	CH2STBY	CH1STBY	CH0STBY	CLKSTBY					
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15	CKSEL	0	R/W	CLK Signal Select 0 Selects the Dotclk signal to be used. 0: DU output clock is selected. 1: du_clkin pin input is selected.
14 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9, 8	CH3STBY	00	R/W	CH3 Control Controls the CH3 pin. 00: Standby mode 11: Operating mode Other settings are prohibited.
7, 6	CH2STBY	00	R/W	CH2 Control Controls the CH2 pin. 00: Standby mode 11: Operating mode Other settings are prohibited.
5, 4	CH1STBY	00	R/W	CH1 Control Controls the CH1 pin. 00: Standby mode 11: Operating mode Other settings are prohibited.
3, 2	CH0STBY	00	R/W	CH0 Control Controls the CH0 pin. 00: Standby mode 11: Operating mode Other settings are prohibited.



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Bit	Bit Name	Initial Value	R/W	Description
1, 0	CLKSTBY	00	R/W	CLK Control Controls the CLK pin. 00: Standby mode 11: Operating mode Other settings are prohibited.

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### 22.2.3 PLL Control Register (LVDPLLCR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	CEEN	—	COSEL	—	PLLDLYCNT										
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 15	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
14	CEEN	0	R/W	PLLCLK Control Sets the PLL divider according to the Dotclk frequency. 0: Division circuit off (when Dotclk is 121 MHz or more). 1: Division circuit on (when Dotclk is less than 121 MHz).
13	—	0	R	Reserved. This bit is always read as 0. The write value should always be 0.
12	COSEL	0	R/W	PLLCLK Select Sets the PLL divider according to the Dotclk frequency. 0: Undivided clock is selected (when Dotclk is 121 MHz or more). 1: Divided clock is selected (when Dotclk is less than 121 MHz).
11	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
10 to 0	PLLDLYCNT	000 0000 0000	R/W	PLL Setting Sets the PLL multiplication rate. 110 1001 1010: When Dotclk is less than 39MHz 111 0111 1011: When Dotclk is 39 MHz or more less than 61 MHz 010 0010 1100: When Dotclk is 61 MHz or more less than 121 MHz 001 1011 1111: When Dotclk is 121 MHz or more Other settings are prohibited.

**22.2.4 CTR Control Register (LVDCTRCR)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	CTR3SEL			—	CTR2SEL			—	CTR1SEL			—	CTR0SEL		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 15	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
14 to 12	CTR3SEL	000	R/W	CTR3 Select Selects data to be output to CTR3 (see section 22.3.3, CH Selection). 000: 0 001: Odd/even 010: CDE Other settings are prohibited.
11	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
10 to 8	CTR2SEL	000	R/W	CTR2 Select Selects data to be output to CTR2 (see section 22.3.3, CH Selection). 000: DISP 001: Odd/even 010: CDE 011: HSYNC 100: VSYNC Other settings are prohibited.
7	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
6 to 4	CTR1SEL	000	R/W	CTR1 Select Selects data to be output to CTR1 (see section 22.3.3, CH Selection). 000: VSYNC 001: DISP 010: Odd/even 011: CDE 100: HSYNC Other settings are prohibited.

---

Bit	Bit Name	Initial Value	R/W	Description
3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
2 to 0	CTR0SEL	000	R/W	CTR0 Select Selects data to be output to CTR0 (see section 22.3.3, CH Selection). 000: HSYNC 001: VSYNC 020: DISP 010: Odd/even 100: CDE Other settings are prohibited.

---

**22.2.5 CH Control Register (LVDCHCR)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	CH3SEL	—	—	CH2SEL	—	—	CH1SEL	—	—	CH0SEL	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R	R	R/W	R/W	R	R	R/W	R/W	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13, 12	CH3SEL	00	R/W	CH3 Select Selects data to be output to CH3 (see section 22.3.3, CH Selection). 00: CH3 01: CH0 10: CH1 11: CH2
11, 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9, 8	CH2SEL	00	R/W	CH2 Select Selects data to be output to CH2 (see section 22.3.3, CH Selection). 00: CH2 01: CH3 10: CH0 11: CH1
7, 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5, 4	CH1SEL	00	R/W	CH1 Select Selects data to be output to CH1 (see section 22.3.3, CH Selection). 00: CH1 01: CH2 10: CH3 11: CH0
3, 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

---

Bit	Bit Name	Initial Value	R/W	Description
1, 0	CH0SEL	00	R/W	CH0 Select Selects data to be output to CH0 (see section 22.3.3, CH Selection). 00: CH0 01: CH1 10: CH2 11: CH3

---

## 22.3 Operation

RZ/G1H	RZ/G1N
RZ/G1M	RZ/G1E

The LVDS module converts the RGB signals output by DU to the LVDS format and outputs those signals. Since the output data format can be selected by register settings, this module can convert to any of the LVDS formats. The output data format is determined by (1) the mode selection, (2) the Ctrl signal selection, and (3) the CH selection.

The registers concerned with the output data format must be set before the LVDS module is started and must not be changed during module operation. (See section 22.3.5, Setting Procedure, for details.)

### 22.3.1 Mode Selection

The mode is selected by the LDMD bits in the LVDS control register 0. Figure 22.2 shows the modes that can be set.

Here, R0 to R7, G0 to G7, and B0 to B7 are the RGB signals and Ctrl0 to Ctrl3 are control signals (such as HSYNC and VSYNC). The Ctrl signals can be set by the CTR control register.

CH0, CH1, CH2, and CH3 are buffers that hold data temporarily. The default is for the CH0, CH1, CH2, and CH3 data to be output directly without change to DU\_LVDS0/1\_CH0\_P/N, DU\_LVDS0/1\_CH1\_P/N, DU\_LVDS0/1\_CH2\_P/N, and DU\_LVDS0/1\_CH3\_P/N. The CH assignment can be switched with the CH control register settings.

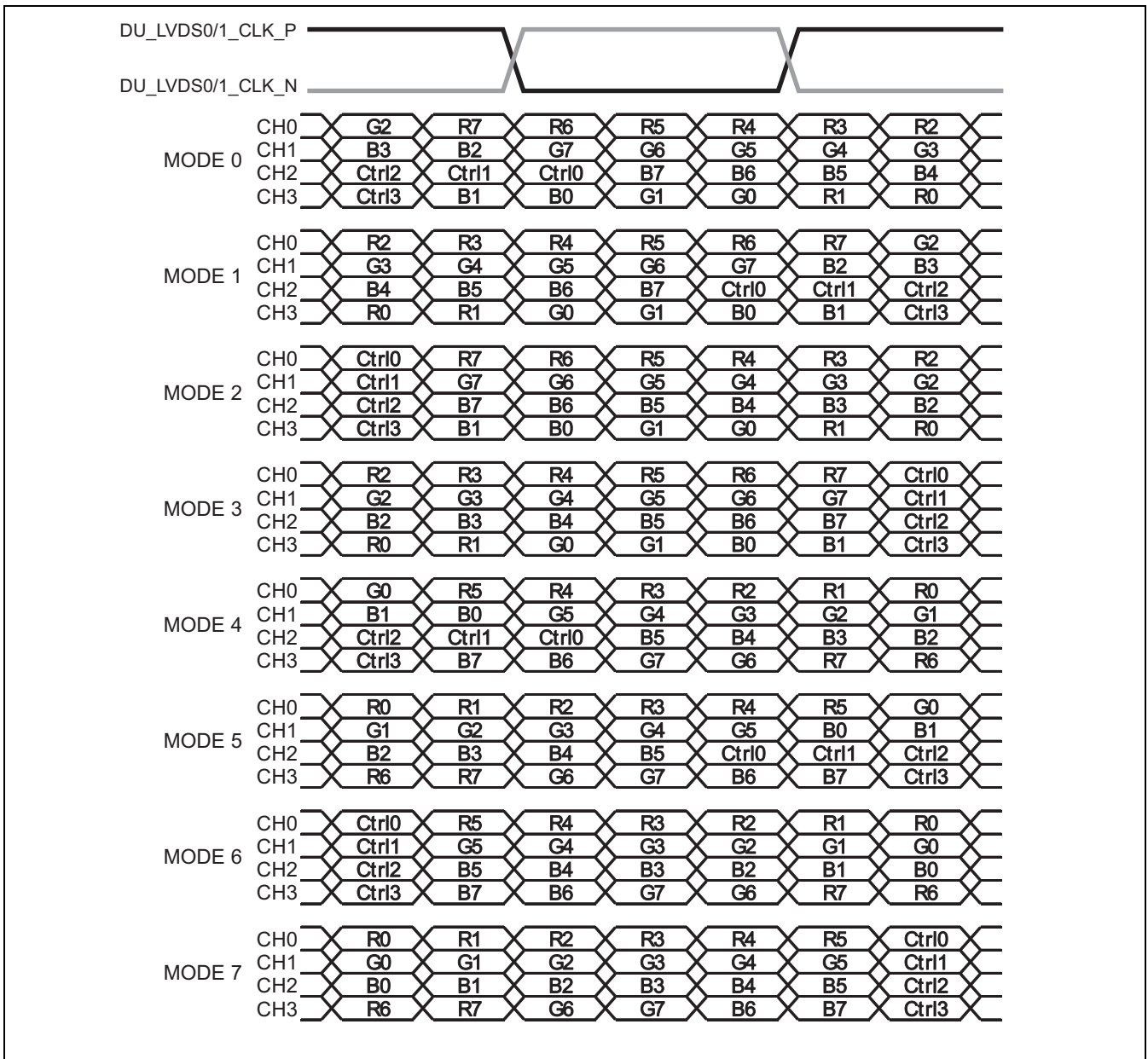


Figure 22.2 Output Data Format (1)



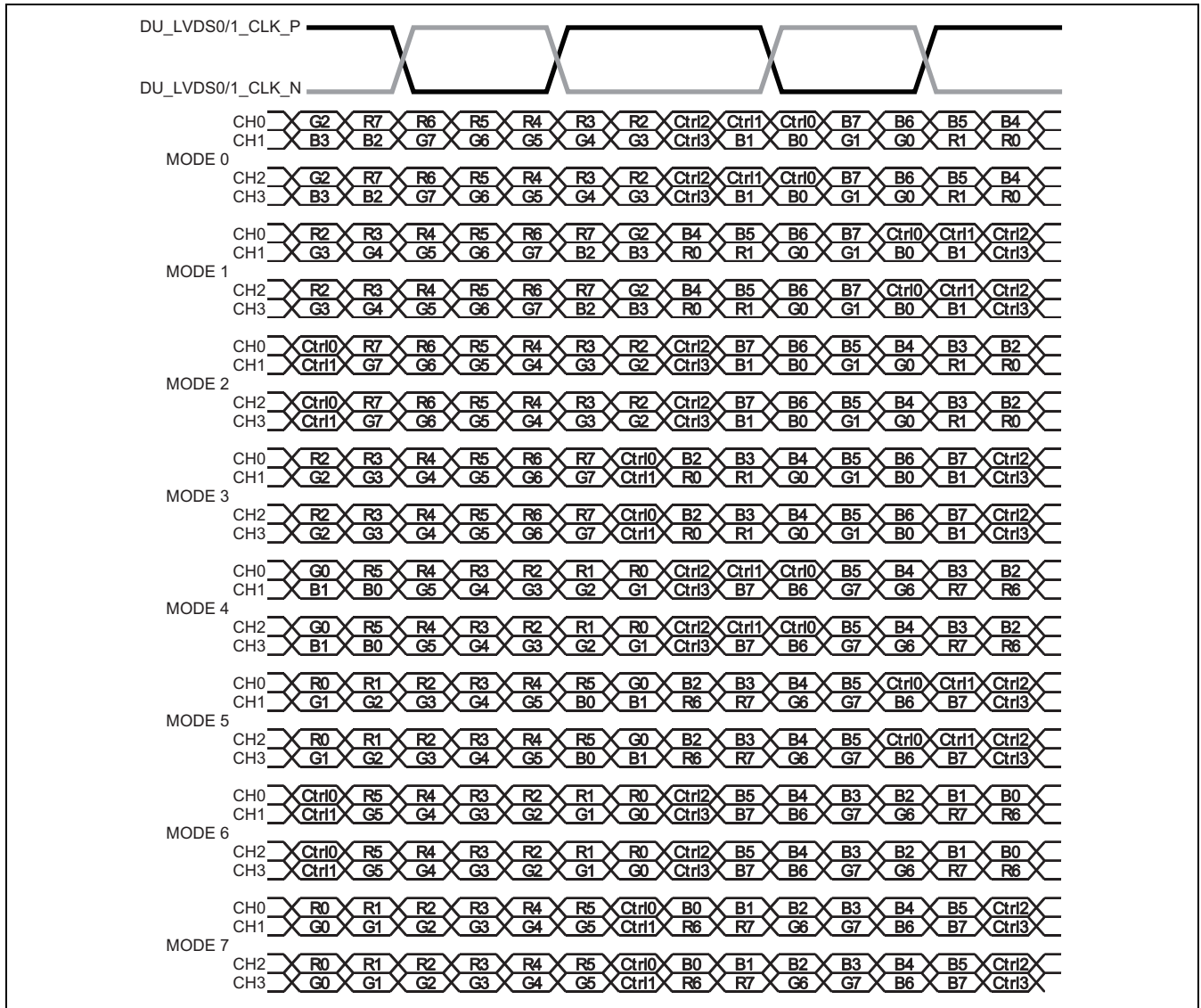


Figure 22.3 Output Data Formats (2)

### 22.3.2 Ctrl Signal Selection

The two stage settings shown below are required to select the Ctrl signals.

#### (1) DU Output Signal Selection

The DU output ports are multiplexed. The signals that you want to output are set up with the corresponding register. The specified signals are input to the LVDS module ports.

#### (2) LVDS Port Selection

The LVDS ports used to output to the Ctrl signals are selected with the CTR control register (LVDCTRCR). This results in the signals input to the LVDS ports being output as Ctrl signals.

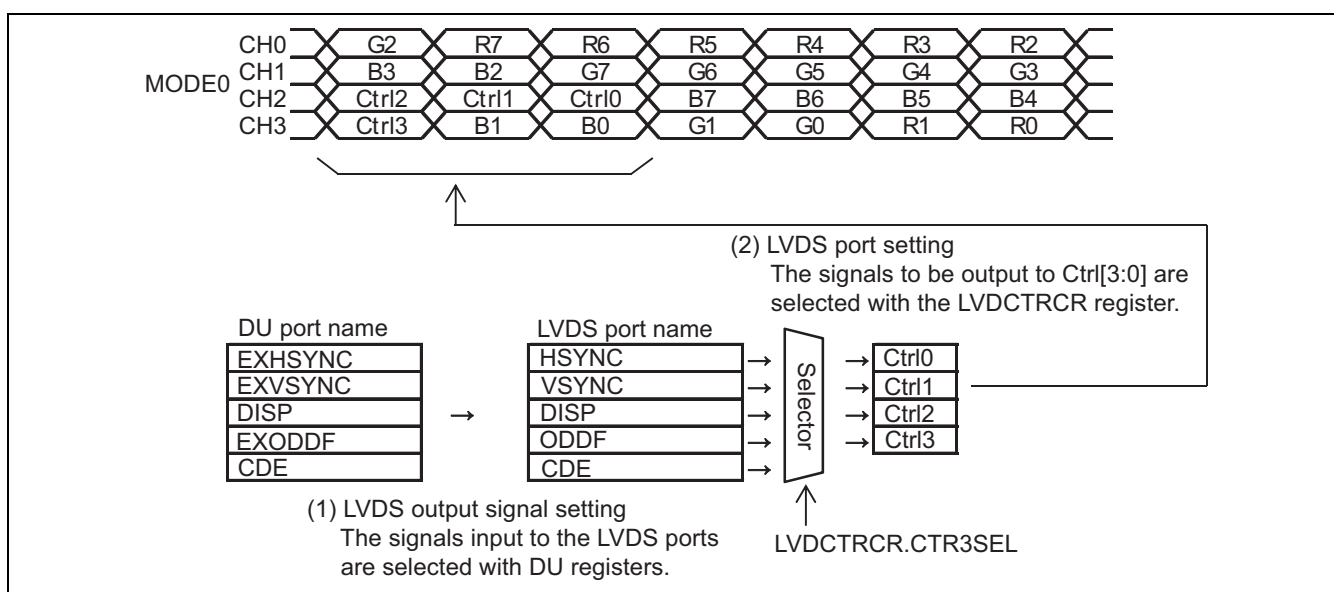


Figure 22.4 Ctrl Signal Selection

Set the desired Ctrl signal characteristics with the DU registers.

For example, to reverse the polarity of the HSYNC signal, the polarity must be set with DU register settings. (The LVDS module only converts the signals output from DU to the LVDS format.)

An example of Ctrl signal settings is shown below.

1. Ctrl0 = HSYNC, Ctrl1 = VSYNC, and Ctrl2 = DISP

Set the DU registers so that HSYNC, VSYNC, and DISP are output.

Then set the CTR control register (LVDCTRCR) so that CTR0SEL = B'000, CTR1SEL = B'000, and CTR2SEL = B'000.

2. Ctrl0 = CSYNC, Ctrl1 = ODDF, and Ctrl2 = CDE

Set the DU registers so that CSYNC, ODDF, and CDE are output.

Then set the LVDS register (LVDCSCR) so that CTR0SEL = B'000, CTR1SEL = B'010, and CTR2SEL = B'010.

(Note that since CSYNC can also be output from other ports, CTR0SEL must be set to match the port from which DU outputs CSYNC.)

### 22.3.3 CH Selection

The LVDS module stores the RGB signal data in CH0, CH1, CH2, and CH3 according to the mode selection and Ctrl signal selection registers.

The CH0, CH1, CH2, and CH3 data is then stored in the CH0, CH1, CH2, and CH3 FIFOs according to the CH selection register setting. The data stored in the CH0, CH1, CH2, and CH3 FIFOs is output from the external pins after passing through the LVDS buffers.

### 22.3.4 Dotclk Settings

The LVDS module Dotclk frequency is determined by the clock source selected and the divisor settings. This section describes how this frequency is set.

The individual settings are made with the DU (Display Unit) and PFC (Pin Function Controller) registers. Refer to the corresponding sections for details on the registers, notes, and other information on these settings.

- Clock source selection

The clock source can be selected to be either the internal clock (clkp) or an external input (DU\_DOTCLKIN0, DU\_DOTCLKIN1 or DU\_DOTCLKIN2\*).

This is set with the DCLK SEL bit in the DU external sync control register n (ESCRn (n = 0, 1, 2\*)).

When an external input (DU[01]\_DOTCLKIN, DU\_DOTCLKIN2\*) is used, set the DU[01]\_DOTCLKIN function in the PFC GPIO peripheral function selection (GPSR). See the section on PFC pin multiplexing settings for details.)

- Divisor setting

This setting specifies the divisor applied to the clock source.

This is set with the FRQSEL field in the DU external sync control register n (ESCRn (n = 0, 1, 2\*)).

Note: \* Only RZ/G1H

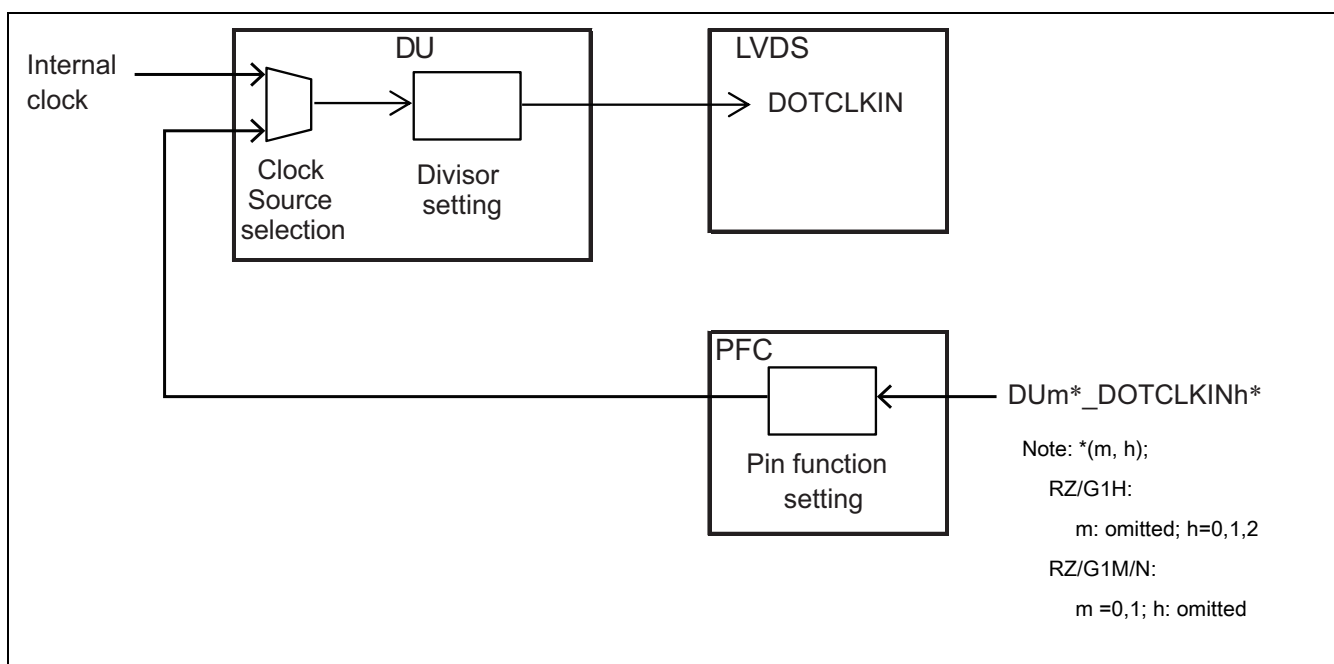


Figure 22.5 Dotclk Settings

### 22.3.5 Setting Procedure

The procedure for using the LVDS module is shown below.

#### Startup Procedure

1. Clear the DU and LDVS module standby states using CPG: MSTPCR.\*<sup>1</sup>
2. Set the DU register.\*<sup>2</sup>
3. Set the LVDS registers other than LVDCR0.PLLON, BEN, LVEN, LVRES and LVDCR1.CHnSTBY.\*<sup>3</sup>
4. Set LVDCR1.CHnSTBY to B'11 to turn on the LVDS IO.
5. Set LVDCR0.BEN and LVEN to 1 to enable the LVDS logic.
6. Set LVDCR0.PLLON to 1 to turn on the PLL.
7. When all of the following conditions have been met, set LVDCR.LVRES to 1.
  - At least 100  $\mu$ s has elapsed since LVDCR0.PLLON was set to 1.
8. Signals will be output from the LVDS pins after LVDCR0.LVRES is set to 1.

Notes: 1. For both the DU and LVDS modules, the initial state is the module standby state. When starting the module immediately after a reset, the module standby state must be cleared.

2. Here, it is possible to proceed as long as the Dotclk signal is output. (The LVDS PLL must be started.) Other items may be set while waiting for the conditions of step 6 to be met.

3. This refers to settings other than those that are concerned with LVDS startup. These items may be set while waiting for the conditions of step 6 to be met.

#### Turning the Display On or Off

##### Display Off

1. Set LVDCR0.LVRES to 0 to turn the display off.
2. Set LVDCR0.PLLON to 0 to turn the LVDS PLL circuit off.
3. Set LVDCR0.BEN and LVEN to 0 to disable the LVDS logic.
4. Set LVDCR1.CHnSTBY to B'00 to turn off the LVDS IO.
5. Set CPG: SRCR\* to 1 to reset LVDS module.

##### Display On

6. Set CPG: SRSTCLR\* to 1 to clear reset of LVDS module.
7. Re-perform the above procedure [Startup Procedure]

## 22.4 Usage Notes

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

The following notes must be observed when using the LVDS module.

Incorrect operation and damage to the device itself may occur if these notes are not followed.

- Since the LVDS module includes logic that operates from the dot clock (Dotclk) signal output by the DU module, incorrect operation may occur if the DU registers are not set appropriately. Also, do not change any DU register values during LVDS operation. (If Dotclk output is not stable, the LVDS PLL is unlocked, and thus operation cannot be guaranteed.) There are two DU registers related to Dotclk: Display unit SYStem control Register n (DSYSRn, n = 0, 1, 2\*) and External Synchronization Control Register n (ESCRn, n = 0, 1, 2\*). These registers must not be changed during LVDS operation.
- Set the Dotclk signal input to the LVDS module to a frequency within the LVDS module's guaranteed operating range (31 to 148.5 MHz).
- Application systems should be implemented in a failsafe manner, such as by connecting the LVDS outputs to a failsafe receiver or by connecting terminators, so that no problems in or damage to the application can occur if the LVDS pins become unstable (for example, going to the high-impedance state or the differential outputs going to the same level).

Note: \* Only RZ/G1H

## 22.5 Notes on Board Design

### 22.5.1 Notes on Using the PLL Oscillator Circuit

Isolate the VDD-LVDSPLL and VSS-LVDSPLL levels from other VDD and VSS levels at the board power supply sources. Also, insert the resistor RCB and the bypass capacitor CB in the power supply circuit near these pins.

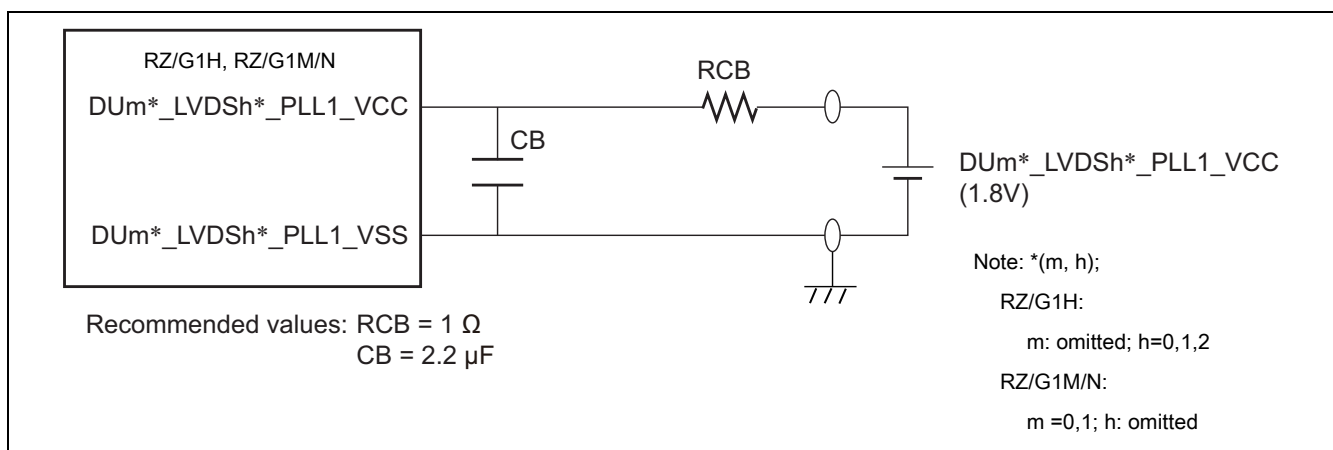


Figure 22.6 Notes on Using the PLL Oscillator Circuit

## 23. Video Input Module (VIN)

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

### 23.1 Overview

The video input module (hereinafter abbreviated as VIN) is a video capture module that stores in external memory YCbCr-422 data through the ITU-R BT.601, ITU-R BT.656, or ITU-R BT.709 interface and RGB data through the ITU-R BT.601 or ITU-R BT.709 interface.

The module has up to six video channels that can independently control the capture of data into a capture area of up to  $2048 \times 2048$  pixels. It can also provide vertical and horizontal scaling of the data by up to three and two times, respectively.

For captured video data, the VIN provides a color space conversion function from YCbCr-422 to RGB, a format conversion function from RGB to ARGB.

As the VIN internally generates a field signal, it can capture progressive data.

- Notes:
1. The maximum frequency of the video clock is 100 MHz when bit 31 (FAST) in the main control register is set to support the 100 MHz clock input, except during vertical or horizontal scaling up.
  2. When the ITU-R BT.709 interface is in use, the maximum frequency of the video clock is 74.5 MHz.
  3. The number of video input channels for each product is as follows:
    - RZ/G1H: 4 channels
    - RZ/G1M/N: 3 channels
    - RZ/G1E: 2 channels

### 23.1.1 Features

#### (1) Video Channels 0 and 1 (RZ/G1H, M/N) and Video Channel 0 (RZ/G1E)

The following input interfaces can be selected for these channels.

**Table 23.1 Input Interface for Video Channels 0 and 1 for RZ/G1H, M/N, Channel 0 for RZ/G1E**

Interface	Data Width	Data Type	RZ/G Series Products			
			RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
ITU-R BT.601/BT.709*1,*3	8/10/12 bits	YCbCr-422 data (UYVY format)	√	√	√	√
ITU-R BT.601/BT.709	4/8 bits	YCbCr-422 data (UYVY format) Double-edge capture mode	√	—	—	—
ITU-R BT.601/BT.709*3/ BT.1358*2	16/20/24 bits	YCbCr-422 data (8/10/12 bits (Y) + 8/10/12 bits (CbCr) format)	√	√	√	√
ITU-R BT.656*1	8/10/12 bits	YCbCr-422 data (UYVY format)	√	√	√	√
ITU-R BT.656	4/8 bits	YCbCr-422 data (UYVY format) Double-edge capture mode	√	—	—	—
ITU-R BT.601/BT.709*3	18 bits	RGB-666 data	√	√	√	√
ITU-R BT.601/BT.709*3	12 bits	RGB-888 data Double-edge capture mode	√	—	—	—
ITU-R BT.601/BT.709*3	24 bits	RGB-888 data	√	√	√	√

- Notes:
1. Disable the XY scaling settings when using the 10/12-bit YCbCr-422 format in the ITU-R BT.601, BT.709, or BT.656 interface (only the 100% scaling is enabled).
  2. Disable the XY scaling settings when using the 20/24-bit YCbCr-422 format in the ITU-R BT.601, BT.709, or BT.1358 interface (only the 100% scaling is enabled).
  3. When the ITU-R BT.709 interface is in use, the maximum frequency of the video clock is 74.5 MHz.
  4. RZ/G1E channel 0 (excluding RZ/G1E channel 1).

**(2) Video Channel 2 (RZ/G1H, M/N), Channel 1(RZ/G1E)**

The following input interfaces can be selected for this channel.

**Table 23.2 Input Interface for Video Channel 2 for RZ/G1H, M/N, Channel 1 for RZ/G1E**

Interface	Data Width	Data Type	RZ/G Series Products			
			RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
ITU-R BT.601*1/BT.709*2	8 bits	YCbCr-422 data (UYVY format)	√	√	√	—
	8/10/12 bits		—	—	—	√
ITU-R BT.601/BT.709*2	4/8 bits	YCbCr-422 data (UYVY format) Double-edge capture mode	√	—	—	—
ITU-R BT.601/BT.709*2/ BT.1358	16 bits	YCbCr-422 data (8 bits (Y) + 8 bits (CbCr) format)	√	—	—	—
ITU-R BT.656*1	8 bits	YCbCr-422 data (UYVY format)	√	√	√	—
	8/10/12 bits		—	—	—	√
ITU-R BT.656	4/8 bits	YCbCr-422 data (UYVY format) Double-edge capture mode	√	—	—	—
ITU-R BT.601/BT.709*2	18 bits	RGB-666 data	√	—	—	—
ITU-R BT.601/BT.709*2	24 bits	RGB-888 data	√	—	—	—

Notes: 1. Disable the XY scaling settings when using the 10/12-bit YCbCr-422 format in the ITU-R BT.601, BT.709, or BT.656 interface. (Only the 100% scaling is enabled.)  
2. When the ITU-R BT.709 interface is in use, the maximum frequency of the video clock is 74.5 MHz.

**(3) Video Channel 3 (RZ/G1H)**

The following input interfaces can be selected for this channel.

**Table 23.3 Input Interface for Video Channel 3 for RZ/G1H**

Interface	Data Width	Data Type	RZ/G Series Products			
			RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
ITU-R BT.601/BT.709*1, *2	8 bits	YCbCr-422 data (UYVY format)	√	—	—	—
ITU-R BT.656*1	8 bits	YCbCr-422 data (UYVY format)	√	—	—	—

Notes: 1. Disable the XY scaling settings when using the 10/12-bit YCbCr-422 format in the ITU-R BT.601, BT.709, or BT.656 interface. (Only the 100% scaling is enabled.)  
2. When the ITU-R BT.709 interface is in use, the maximum frequency of the video clock is 74.5 MHz.



#### (4) Internal Sync Signal Generation

For video data capturing through the ITU-R BT.601 or ITU-R BT.709 interface, the field signal can be internally generated even if the input sync signals stops (In video data capture through the ITU-R BT.656 interface, only the field signal is generated).

#### (5) Capture Mode

The following four modes can be selected to capture the interlace images. In addition, single frame capture or continuous frame capture mode can be selected.

Triple-buffering control is provided in accordance with the captured field image and frame image to coordinate with the video capture mode of the display module.

- Odd-field capture mode
- Even-/odd-field capture mode
- Even-field capture mode
- Full interlace capture mode

#### (6) Vertical and Horizontal Scaling

The image can be scaled up and down up to three times in the vertical and two times in the horizontal directions.

#### (7) Size Clipping

The VIN has two clipping circuits, which independently handle images with up to  $2048 \times 2048$  pixels. Any capture size within this limit can be specified before or after scaling.

#### (8) Color Space Conversion

Color space conversion can be performed from YC to RGB or from RGB to YC. Desired conversion coefficients can be specified through registers to adjust colors.

#### (9) Lookup Table (LUT) Density Conversion

The lookup table (LUT) density can be converted from 10 bits to 8 bits for each pixel according to the color space conversion result.

Note: When the density conversion function is not used, the upper 8 bits of data are output.

#### (10) Image Data Format Conversion

To the density-converted YCbCr444 or RGB888 image data, the following data format conversions are available:

- YCbCr image data
  - Y/Cb/Cr 8-bit multiplex conversion
  - YCbCr444 → YC separation (separated into Y and CbCr components.)
  - YCbCr444 → Y component extraction
- RGB image data
  - RGB-888 → 32 bits/pixel conversion
  - RGB-888 → RGB-565 (16 bits/pixel) conversion
  - RGB-888 → ARGB-1555 (16 bits/pixel) conversion
  - RGB-888 → ARGB-888 (32 bits/pixel) conversion

Note: The lookup table is common to the YCbCr and RGB formats.

#### (11) Local Video Interface Output

By using the local video interface output control function, operation can be linked with the IMR-LSX2.

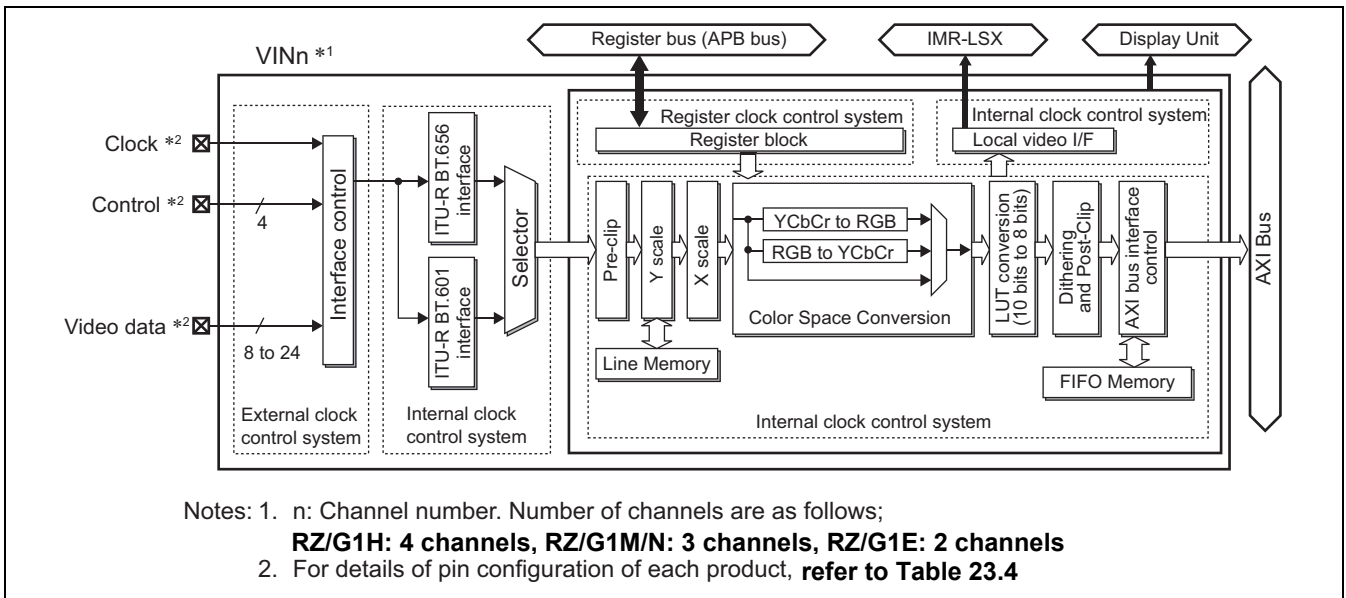
- Notes: 1. The distortion correction or scaling processing should be implemented with the IMR-LSX2 module.  
 2. Post-clipping processing cannot be provided for the image data output from the local video interface.

**(12) Memory Output Data Format**

Format-converted image data can be transferred to the memory. The following shows the available formats of the data stored.

- YCbCr image data
  - Y/Cb/Cr, 8-bit multiplexed
  - YC separation, YCbCr422, Y, 8-bit Cb/Cr, 8-bit multiplexed
  - YC separation, YCbCr422, Y, 10-bit Cb/Cr, 8-bit multiplexed
  - YC separation, YCbCr422, Y, 12-bit Cb/Cr, 8-bit multiplexed
  - YC separation, Y data, 8-bit
  - YC separation, Y data, 10-bit
  - YC separation, Y data, 12-bit
- RGB image data
  - RGB-565 (16 bits/pixel)
  - ARGB-1555 (16 bits/pixel)
  - RGB-888 (32 bits/pixel)
  - ARGB-8888 (32 bits/pixel)

**23.1.2 Block Diagram**



**Figure 23.1 VIN Channel n (VINn) Functional Block Diagram**

### 23.1.3 Input/Output Pins

**Table 23.4 Pin Configuration**

Pin Name	Function	I/O	Description	RZ/G Series Products			
				RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
VIN0 video clock (clock)	VI0_CLK	Input	External video clock in the ITU-R BT.601, ITU-R BT.656, ITU-R BT.1358, or ITU-R BT.709 interface	√	√	√	√
VIN0 field signal (control)	VI0_FIELD	Input	Field signal in the ITU-R BT.601 or ITU-R BT.709 interface Fix this pin high or low when the pin is not used.	√	√	√	√
VIN0 vertical sync signal (control)	VI0_VSYNC#	Input	Vertical sync signal in the ITU-R BT.601, ITU-R BT.1358, or ITU-R BT.709 interface Fix this pin high or low when the pin is not used.	√	√	√	√
VIN0 horizontal sync signal (control)	VI0_HSYNC#	Input	Horizontal sync signal in the ITU-R BT.601, ITU-R BT.1358, or ITU-R BT.709 interface Fix this pin high or low when the pin is not used.	√	√	√	√
VIN0 data enable (control)	VI0_CLKENB	Input	Data enable signal in the ITU-R BT.601, ITU-R BT.1358, or ITU-R BT.709 interface Fix this pin high or low when the pin is not used. If the signal is not present in the ITU-R BT.601, ITU-R BT.1358, or ITU-R BT.709 interface, connect the pin to a horizontal sync signal.	√	√	√	√
VIN0 video data (video data)	VI0_R7 to VI0_R0 VI0_G7 to VI0_G0 VI0_B7 to VI0_B0	Input	Data signals in the ITU-R BT.601, ITU-R BT.656, ITU-R BT.1358, or ITU-R BT.709 interface Fix these pins high or low respectively when these pins are not used in whole or in part.	√	√	√	—
	VI0_R7 to VI0_R0 VI0_G7 to VI0_G0 VI0_DATA7/VI0_B7 to VI0_DATA0/VI0_B0		—	—	—	√	
VIN1 video clock (clock)	VI1_CLK	Input	External video clock in the ITU-R BT.601, ITU-R BT.656, ITU-R BT.1358, or ITU-R BT.709 interface	√	√	√	√
VIN1 field signal (control)	VI1_FIELD	Input	Field signal in the ITU-R BT.601 or ITU-R BT.709 interface Fix this pin high or low when the pin is not used.	√	√	√	√
VIN1 vertical sync signal (control)	VI1_VSYNC#	Input	Vertical sync signal in the ITU-R BT.601, ITU-R BT.1358, or ITU-R BT.709 interface Fix this pin high or low when the pin is not used.	√	√	√	√
VIN1 horizontal sync signal (control)	VI1_HSYNC#	Input	Horizontal sync signal in the ITU-R BT.601, ITU-R BT.1358, or ITU-R BT.709 interface Fix this pin high or low when the pin is not used.	√	√	√	√

Pin Name	Function	I/O	Description	RZ/G Series Products			
				RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
VIN1 data enable (control)	VI1_CLKENB	Input	Data enable signal in the ITU-R BT.601, ITU-R BT.1358, or ITU-R BT.709 interface Fix this pin high or low when the pin is not used. If the signal is not present in the ITU-R BT.601, ITU-R BT.1358, or ITU-R BT.709 interface, connect the pin to a horizontal sync signal.	√	√	√	√
VIN1 video data (video data)	VI1_R7 to VI1_R0 VI1_G7 to VI1_G0 VI1_B7 to VI1_B0	Input	Data signals in the ITU-R BT.601, ITU-R BT.656, ITU-R BT.1358, or ITU-R BT.709 interface Fix these pins high or low respectively when these pins are not used in whole or in part.	√	√	√	—
	VI1_DATA7 to VI1_DATA0 VI1_DATA11 to VI1_DATA8 (VI1_G3_B to VI1_G0_B)			—	—	—	√
VIN2 video clock (clock)	VI2_CLK	Input	External video clock in the ITU-R BT.601, ITU-R BT.656, ITU-R BT.1358 (excluding RZ/G1M/N channel 2), or ITU-R BT.709 interface	√	√	√	—
VIN2 field signal (control)	VI2_FIELD	Input	Field signal in the ITU-R BT.601 or ITU-R BT.709 interface Fix these pins high or low when these pins are not used.	√	√	√	—
VIN2 vertical sync signal (control)	VI2_VSYNC#	Input	Vertical sync signal in the ITU-R BT.601, ITU-R BT.1358 (excluding RZ/G1M/N channel 2), or ITU-R BT.709 interface Fix this pin high or low when the pin is not used.	√	√	√	—
VIN2 horizontal sync signal (control)	VI2_HSYNC#	Input	Horizontal sync signal in the ITU-R BT.601, ITU-R BT.1358 (excluding RZ/G1M/N channel 2), or ITU-R BT.709 interface Fix this pin high or low when the pin is not used.	√	√	√	—
VIN2 data enable (control)	VI2_CLKENB	Input	Data enable signal in the ITU-R BT.601, ITU-R BT.1358 (excluding RZ/G1M/N channel 2), or ITU-R BT.709 interface Fix this pin high or low when the pin is not used. If the signal is not present in the ITU-R BT.601, ITU-R BT.1358, or ITU-R BT.709 interface, connect the pin to a horizontal sync signal.	√	√	√	—
VIN2 video data (video data)	VI2_R7 to VI2_R0 VI2_G7 to VI2_G0 VI2_B7 to VI2_B0	Input	Data signals in the ITU-R BT.601, ITU-R BT.656, ITU-R BT.1358 (excluding RZ/G1M/N channel 2), or ITU-R BT.709 interface Fix these pins high or low respectively when these pins are not used in whole or in part.	√	√	√	—
VIN3 video clock (clock)	VI3_CLK	Input	External video clock in the ITU-R BT.601, ITU-R BT.656, or ITU-R BT.709 interface	√	—	—	—

Pin Name	Function	I/O	Description	RZ/G Series Products			
				RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
VIN3 field signal (control)	VI3_FIELD	Input	Field signal in the ITU-R BT.601 or ITU-R BT.709 interface Fix this pin high or low when the pin is not used.	√	—	—	—
VIN3 vertical sync signal (control)	VI3_VSYNC#	Input	Vertical sync signal in the ITU-R BT.601 or ITU-R BT.709 interface Fix this pin high or low when the pin is not used.	√	—	—	—
VIN3 horizontal sync signal (control)	VI3_HSYNC#	Input	Horizontal sync signal in the ITU-R BT.601 or ITU-R BT.709 interface Fix this pin high or low when the pin is not used.	√	—	—	—
VIN3 data enable (control)	VI3_CLKENB	Input	Data enable signal in the ITU-R BT.601 or ITU-R BT.709 interface Fix this pin high or low when the pin is not used. If the signal is not present in the ITU-R BT.601 or ITU-R BT.709 interface, connect the pin to a horizontal sync signal.	√	—	—	—
VIN3 video data (video data)	VI3_DATA7 to VI3_DATA0	Input	Data signals in the ITU-R BT.601, ITU-R BT.656, or ITU-R BT.709 interface Fix these pins high or low respectively when these pins are not used in whole or in part.	√	—	—	—

**Table 23.5 Channel 0 Data Pin Connections (RZ/G1H, M/N and E)**

Input data format	RZ/G1H, M/N and E: VI0_R[7:0]								RZ/G1H, M/N and E: VI0_G[7:0]								RZ/G1H and M/N: VI0_B[7:0]/ RZ/G1E: VI0_DATA[7:0]/VI0_B[7:0]										
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0			
ITU-R BT.601/BT.709/BT.656 8-bit YCbCr-422 (bit width: 4 bits) (double edge) (RZ/G1H only)	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	Y/Cb/Cr video data[7:4]			
	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	Y/Cb/Cr video data[3:0]			
ITU-R BT.601/BT.709/BT.656 8-bit YCbCr-422 (VnDMR2/YDS = 0) (RZ/G1H, M/N and E)	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	Y/Cb/Cr video data[7:0]										
ITU-R BT.601/BT.709/BT.656 8-bit YCbCr-422 (VnDMR2/YDS = 1) (RZ/G1H, M/N and E)	*	*	*	*	*	*	*	*	Y/Cb/Cr video data[7:0]								*	*	*	*	*	*	*	*	*	*	*
ITU-R BT.601/BT.709/BT.656 8-bit YCbCr-422 (bit width: 8 bits) (double edge) (RZ/G1H only)	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	Cb/Cr video data[7:0]										
	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	Y video data[7:0]										
ITU-R BT.601/BT.709/BT.656 10-bit YCbCr-422 (RZ/G1H, M/N and E)	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	Y/Cb/Cr video data[9:0]											
ITU-R BT.601/BT.709/BT.656 12-bit YCbCr-422 (RZ/G1H, M/N and E)	*	*	*	*	*	*	*	*	*	*	*	*	*	*	Y/Cb/Cr video data[11:0]												
ITU-R BT.601/BT.709/BT.1358 16-bit YCbCr-422 (RZ/G1H, M/N and E)	*	*	*	*	*	*	*	*	Y video data[7:0]								Cb/Cr video data[7:0]										
ITU-R BT.601/BT.709/BT.1358 20-bit YCbCr-422 (RZ/G1H, M/N and E)	*	*	*	*	Y video data[9:0]												Cb/Cr video data[9:0]										
ITU-R BT.601/BT.709/BT.1358 24-bit YCbCr-422 (RZ/G1H, M/N and E)	Y video data[11:0]																Cb/Cr video data[11:0]										
ITU-R BT.601/BT.709 RGB-666 (RZ/G1H, M/N and E)	R video data[5:0]				*	*	G video data[5:0]				*	*	B video data[5:0]				*	*									
ITU-R BT.601/BT.709 RGB-888 (data width: 12 bits) (double edge) (RZ/G1H only)	*	*	*	*	*	*	*	*	*	*	*	*	G video data[3:0]				B video data[7:0]										
	*	*	*	*	*	*	*	*	*	*	*	*	R video data[7:0]				G video data[7:4]										
ITU-R BT.601/BT.709 24-bit RGB-888 (RZ/G1H, M/N and E)	R video data[7:0]								G video data[7:0]								B video data[7:0]										

Note: \* Fix the pins at a high or low level.

**Table 23.6 Channel 1 Data Pin Connections (RZ/G1H, M/N and E)**

Input data format	RZ/G1H and M/N: VI1_R[7:0]								RZ/G1H and M/N: VI1_G[7:0]/ RZ/G1E: VI1_DATA[11:8] (VI1_G[3:0]_B)								RZ/G1H and M/N: VI1_B[7:0]/ RZ/G1E: VI1_DATA[7:0]											
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0				
ITU-R BT.601/BT.709/BT.656 8-bit YCbCr-422 (bit width: 4 bits) (double edge) (RZ/G1H only)	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	Y/Cb/Cr video data[7:4]				
	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	Y/Cb/Cr video data[3:0]				
ITU-R BT.601/BT.709/BT.656 8-bit YCbCr-422 (VnDMR2/YDS = 0) (RZ/G1H and M/N) (VnDMR/YMODE = B'000) (RZ/G1E only)	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	Y/Cb/Cr video data[7:0]										
ITU-R BT.601/BT.709/BT.656 8-bit YCbCr-422 (VnDMR2/YDS = 1) (RZ/G1H and M/N)	*	*	*	*	*	*	*	*	Y/Cb/Cr video data[7:0]								*	*	*	*	*	*	*	*	*	*	*	*
ITU-R BT.601/BT.709/BT.656 8-bit YCbCr-422 (bit width: 8 bits) (double edge) (RZ/G1H only)	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	Cb/Cr video data[7:0]										
	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	Y video data[7:0]										
ITU-R BT.601/BT.709/BT.656 10-bit YCbCr-422 (RZ/G1H, M/N and E)	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	Y/Cb/Cr video data[9:0]											
ITU-R BT.601/BT.709/BT.656 12-bit YCbCr-422 (RZ/G1H, M/N and E)	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	Y/Cb/Cr video data[11:0]											
ITU-R BT.601/BT.709/BT.1358 16-bit YCbCr-422 (RZ/G1H, M/N)	*	*	*	*	*	*	*	*	Y video data[7:0]								Cb/Cr video data[7:0]											
ITU-R BT.601/BT.709/BT.1358 20-bit YCbCr-422 (RZ/G1H, M/N)	*	*	*	*	Y video data[9:0]												Cb/Cr video data[9:0]											
ITU-R BT.601/BT.709/BT.1358 24-bit YCbCr-422 (RZ/G1H, M/N)	Y video data[11:0]																Cb/Cr video data[11:0]											
ITU-R BT.601/BT.709 RGB-666 (RZ/G1H, M/N)	R video data[5:0]					*	*	G video data[5:0]					*	*	B video data[5:0]					*	*							
ITU-R BT.601/BT.709 RGB-888 (data width: 12 bits) (double edge) (RZ/G1H only)	*	*	*	*	*	*	*	*	*	*	*	*	*	G video data[3:0]				B video data[7:0]										
	*	*	*	*	*	*	*	*	*	*	*	*	*	R video data[7:0]								G video data[7:4]						
ITU-R BT.601/BT.709 24-bit RGB-888 (RZ/G1H, M/N)	R video data[7:0]								G video data[7:0]								B video data[7:0]											

Note: \* Fix the pins at a high or low level.

**Table 23.7 Channel 2 Data Pin Connections (RZ/G1H, M/N)**

Input data format	RZ/G1H: VI2_R[7:0]/ RZ/G1M/N: -								RZ/G1H: VI2_G[7:0]/ RZ/G1M/N: -								RZ/G1H: VI2_B[7:0]/ RZ/G1M/N: VI2_DATA[7:0]										
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0			
ITU-R BT.601/BT.709/BT.656 8-bit YCbCr-422 (bit width: 4 bits) (double edge) (RZ/G1H only)	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	Y/Cb/Cr video data[7:4]		
	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	Y/Cb/Cr video data[3:0]		
ITU-R BT.601/BT.709/BT.656 8-bit YCbCr-422 (VnDMR2/YDS = 0) (RZ/G1H only) (VnDMR/YMODE = B'000) (RZ/G1M/N)	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	Y/Cb/Cr video data[7:0]			
ITU-R BT.601/BT.709/BT.656 8-bit YCbCr-422 (VnDMR2/YDS=1) (RZ/G1H only)	*	*	*	*	*	*	*	*	Y/Cb/Cr video data[7:0]								*	*	*	*	*	*	*	*	*	*	*
ITU-R BT.601/BT.709/BT.656 8-bit YCbCr-422 (bit width: 8 bits) (double edge) (RZ/G1H only)	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	Cb/Cr video data[7:0]						
	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	Y video data[7:0]						
ITU-R BT.601/BT.709/BT.1358 16-bit YCbCr-422 (RZ/G1H only)	*	*	*	*	*	*	*	*	Y video data[7:0]								Cb/Cr video data[7:0]										
ITU-R BT.601/BT.709 RGB-666 (RZ/G1H only)	R video data[5:0]							*	*	G video data[5:0]						*	*	B video data[5:0]				*	*				
ITU-R BT.601/BT.709 24-bit RGB-888 (RZ/G1H only)	R video data[7:0]							G video data[7:0]								B video data[7:0]											

Note: \* Fix the pins at a high or low level.

**Table 23.8 Channel 3 Data Pin Connections (RZ/G1H)**

Input data format	RZ/G1H: VI3_DATA[7:0]							
	7	6	5	4	3	2	1	0
ITU-R BT.601/BT.709/BT.656 8-bit YCbCr-422 (RZ/G1H only)	Y/Cb/Cr video data[7:0]							



### 23.1.4 Register Configuration

Tables 23.9 (1) through 23.9 (4) show the VIN register configuration for each channel.

Notes: Do not write to any addresses other than listed below. Operations cannot be guaranteed if writing is attempted. Values read from addresses other than those listed below are undefined.

\* For the internal update mode, refer to the description of the VUP bit in the main control register (VnMC).

#### (1) Channel 0

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

All registers of channel 0 are the same for RZ/G1H, M/N and E, however, some bit function may not be supported by products.

**Table 23.9 (1) VIN Registers**

#### Channel 0 (RZ/G1H, M/N and E)

Channel	Name	Symbol	R/W	Address	Initial Value	Access Size	Internal Update Mode Support*
0	Video 0 main control register	V0MC	R/W	H'E6EF0000	H'00000000	32	Δ
	Video 0 module status register	V0MS	R	H'E6EF0004	H'00000018	32	—
	Video 0 frame capture register	V0FC	R/W	H'E6EF0008	H'00000000	32	—
	Video 0 start line pre-clip register	V0SLPrC	R/W	H'E6EF000C	H'00000000	32	Supported
	Video 0 end line pre-clip register	V0ELPrC	R/W	H'E6EF0010	H'00000000	32	Supported
	Video 0 start pixel pre-clip register	V0SPPrC	R/W	H'E6EF0014	H'00000000	32	Supported
	Video 0 end pixel pre-clip register	V0EPPrC	R/W	H'E6EF0018	H'00000000	32	Supported
	Video 0 start line post-clip register	V0SLPoC	R/W	H'E6EF001C	H'00000000	32	Supported
	Video 0 end line post-clip register	V0ELPoC	R/W	H'E6EF0020	H'00000000	32	Supported
	Video 0 start pixel post-clip register	V0SPPoC	R/W	H'E6EF0024	H'00000000	32	Supported
	Video 0 end pixel post-clip register	V0EPPoC	R/W	H'E6EF0028	H'00000000	32	Supported
	Video 0 image stride register	V0IS	R/W	H'E6EF002C	H'00000000	32	Supported
	Video 0 memory base 1 register	V0MB1	R/W	H'E6EF0030	H'00000000	32	Supported
	Video 0 memory base 2 register	V0MB2	R/W	H'E6EF0034	H'00000000	32	Supported
	Video 0 memory base 3 register	V0MB3	R/W	H'E6EF0038	H'00000000	32	Supported
	Video 0 line count register	V0LC	R	H'E6EF003C	H'00000000	32	—
	Video 0 interrupt enable register	V0IE	R/W	H'E6EF0040	H'00000000	32	—

Channel	Name	Symbol	R/W	Address	Initial Value	Access Size	Internal Update Mode Support*
0	Video 0 interrupt status register	V0INTS	R/W	H'E6EF0044	H'00000000	32	—
	Video 0 scanline interrupt register	V0SI	R/W	H'E6EF0048	H'00000000	32	Supported
	Video 0 Memory Transfer Control register	V0MTC	R/W	H'E6EF004C	H'0A080108	32	Supported
	Video 0 Y scale register	V0YS	R/W	H'E6EF0050	H'00000000	32	Supported
	Video 0 X scale register	V0XS	R/W	H'E6EF0054	H'00000000	32	Supported
	Video 0 data mode register	V0DMR	R/W	H'E6EF0058	H'00000000	32	Supported
	Video 0 data mode register 2	V0DMR2	R/W	H'E6EF005C	H'00000000	32	—
	Video 0 UV address offset register	V0UVAOF	R/W	H'E6EF0060	H'00000000	32	Supported
	Video 0 color space change coefficient 1 register	V0CSCC1	R/W	H'E6EF0064	H'01291080	32	Supported
	Video 0 color space change coefficient 2 register	V0CSCC2	R/W	H'E6EF0068	H'019800D0	32	Supported
	Video 0 color space change coefficient 3 register	V0CSCC3	R/W	H'E6EF006C	H'00640204	32	Supported
	Video 0 coefficient set C1A register	V0C1A	R/W	H'E6EF0080	H'00000000	32	—
	Video 0 coefficient set C1B register	V0C1B	R/W	H'E6EF0084	H'00000000	32	—
	Video 0 coefficient set C1C register	V0C1C	R/W	H'E6EF0088	H'00000000	32	—
	Video 0 coefficient set C2A register	V0C2A	R/W	H'E6EF0090	H'00000000	32	—
	Video 0 coefficient set C2B register	V0C2B	R/W	H'E6EF0094	H'00000000	32	—
	Video 0 coefficient set C2C register	V0C2C	R/W	H'E6EF0098	H'00000000	32	—
	Video 0 coefficient set C3A register	V0C3A	R/W	H'E6EF00A0	H'00000000	32	—
	Video 0 coefficient set C3B register	V0C3B	R/W	H'E6EF00A4	H'00000000	32	—
	Video 0 coefficient set C3C register	V0C3C	R/W	H'E6EF00A8	H'00000000	32	—
	Video 0 coefficient set C4A register	V0C4A	R/W	H'E6EF00B0	H'00000000	32	—
	Video 0 coefficient set C4B register	V0C4B	R/W	H'E6EF00B4	H'00000000	32	—
	Video 0 coefficient set C4C register	V0C4C	R/W	H'E6EF00B8	H'00000000	32	—
	Video 0 coefficient set C5A register	V0C5A	R/W	H'E6EF00C0	H'00000000	32	—
	Video 0 coefficient set C5B register	V0C5B	R/W	H'E6EF00C4	H'00000000	32	—
	Video 0 coefficient set C5C register	V0C5C	R/W	H'E6EF00C8	H'00000000	32	—

Channel	Name	Symbol	R/W	Address	Initial Value	Access Size	Internal Update Mode Support*
0	Video 0 coefficient set C6A register	V0C6A	R/W	H'E6EF00D0	H'00000000	32	—
	Video 0 coefficient set C6B register	V0C6B	R/W	H'E6EF00D4	H'00000000	32	—
	Video 0 coefficient set C6C register	V0C6C	R/W	H'E6EF00D8	H'00000000	32	—
	Video 0 coefficient set C7A register	V0C7A	R/W	H'E6EF00E0	H'00000000	32	—
	Video 0 coefficient set C7B register	V0C7B	R/W	H'E6EF00E4	H'00000000	32	—
	Video 0 coefficient set C7C register	V0C7C	R/W	H'E6EF00E8	H'00000000	32	—
	Video 0 coefficient set C8A register	V0C8A	R/W	H'E6EF00F0	H'00000000	32	—
	Video 0 coefficient set C8B register	V0C8B	R/W	H'E6EF00F4	H'00000000	32	—
	Video 0 coefficient set C8C register	V0C8C	R/W	H'E6EF00F8	H'00000000	32	—
	Video 0 lookup table pointer	V0LUTP	R/W	H'E6EF0100	H'00000000	32	—
	Video 0 lookup table data register	V0LUTD	R/W	H'E6EF0104	H'xxxxxxxx	32	—
	Video 0 RGB→Y calculation setting register 1	V0YCCR1	R/W	H'E6EF0228	H'00000107	32	Supported
	Video 0 RGB→Y calculation setting register 2	V0YCCR2	R/W	H'E6EF022C	H'00640204	32	Supported
	Video 0 RGB→Y calculation setting register 3	V0YCCR3	R/W	H'E6EF0230	H'0A000010	32	Supported
	Video 0 RGB→Cb calculation setting register 1	V0CBCCR1	R/W	H'E6EF0234	H'00001F68	32	Supported
	Video 0 RGB→Cb calculation setting register 2	V0CBCCR2	R/W	H'E6EF0238	H'01C21ED6	32	Supported
	Video 0 RGB→Cb calculation setting register 3	V0CBCCR3	R/W	H'E6EF023C	H'0A000080	32	Supported
	Video 0 RGB→Cr calculation setting register 1	V0CRCCR1	R/W	H'E6EF0240	H'000001C2	32	Supported
	Video 0 RGB→Cr calculation setting register 2	V0CRCCR2	R/W	H'E6EF0244	H'1FB71E87	32	Supported
	Video 0 RGB→Cr calculation setting register 3	V0CRCCR3	R/W	H'E6EF0248	H'0A000080	32	Supported
	Video 0 YC→RGB calculation setting register 1	V0CSCE1	R/W	H'E6EF0300	H'0000129F	32	Supported
	Video 0 YC→RGB calculation setting register 2	V0CSCE2	R/W	H'E6EF0304	H'01000800	32	Supported
	Video 0 YC→RGB calculation setting register 3	V0CSCE3	R/W	H'E6EF0308	H'19890D02	32	Supported
	Video 0 YC→RGB calculation setting register 4	V0CSCE4	R/W	H'E6EF030C	H'06452045	32	Supported

## (2) Channel 1

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Channel 1 registers include special registers for each product.

Table 23.9 (2) VIN Registers

## Channel 1 (RZ/G1H, M/N and E)

Channel	Name	Symbol	R/W	Address	Initial Value	Access Size	Internal Update Mode Support*
1 (RZ/G1H, M/N and E)	Video 1 main control register	V1MC	R/W	H'E6EF1000	H'00000000	32	Δ
	Video 1 module status register	V1MS	R	H'E6EF1004	H'00000018	32	—
	Video 1 frame capture register	V1FC	R/W	H'E6EF1008	H'00000000	32	—
	Video 1 start line pre-clip register	V1SLPrC	R/W	H'E6EF100C	H'00000000	32	Supported
	Video 1 end line pre-clip register	V1ELPrC	R/W	H'E6EF1010	H'00000000	32	Supported
	Video 1 start pixel pre-clip register	V1SPPrC	R/W	H'E6EF1014	H'00000000	32	Supported
	Video 1 end pixel pre-clip register	V1EPPrC	R/W	H'E6EF1018	H'00000000	32	Supported
	Video 1 start line post-clip register	V1SLPoC	R/W	H'E6EF101C	H'00000000	32	Supported
	Video 1 end line post-clip register	V1ELPoC	R/W	H'E6EF1020	H'00000000	32	Supported
	Video 1 start pixel post-clip register	V1SPPoC	R/W	H'E6EF1024	H'00000000	32	Supported
	Video 1 start pixel pre-clip register	V1SPPrC	R/W	H'E6EF1014	H'00000000	32	Supported
	Video 1 end pixel pre-clip register	V1EPPrC	R/W	H'E6EF1018	H'00000000	32	Supported
	Video 1 start line post-clip register	V1SLPoC	R/W	H'E6EF101C	H'00000000	32	Supported
	Video 1 end line post-clip register	V1ELPoC	R/W	H'E6EF1020	H'00000000	32	Supported
	Video 1 start pixel post-clip register	V1SPPoC	R/W	H'E6EF1024	H'00000000	32	Supported
	Video 1 end pixel post-clip register	V1EPPoC	R/W	H'E6EF1028	H'00000000	32	Supported
	Video 1 image stride register	V1IS	R/W	H'E6EF102C	H'00000000	32	Supported
	Video 1 memory base 1 register	V1MB1	R/W	H'E6EF1030	H'00000000	32	Supported
	Video 1 memory base 2 register	V1MB2	R/W	H'E6EF1034	H'00000000	32	Supported
	Video 1 memory base 3 register	V1MB3	R/W	H'E6EF1038	H'00000000	32	Supported
Video 1 line count register	V1LC	R	H'E6EF103C	H'00000000	32	—	

Channel	Name	Symbol	R/W	Address	Initial Value	Access Size	Internal Update Mode Support*
1 (RZ/G1H, M/N and E)	Video 1 interrupt enable register	V1IE	R/W	H'E6EF1040	H'00000000	32	—
	Video 1 interrupt status register	V1INTS	R/W	H'E6EF1044	H'00000000	32	—
	Video 1 scanline interrupt register	V1SI	R/W	H'E6EF1048	H'00000000	32	Supported
	Video 1 Memory Transfer Control register	V1MTC	R/W	H'E6EF104C	H'0A080108	32	Supported
	Video 1 Y scale register	V1YS	R/W	H'E6EF1050	H'00000000	32	Supported
	Video 1 X scale register	V1XS	R/W	H'E6EF1054	H'00000000	32	Supported
	Video 1 data mode register	V1DMR	R/W	H'E6EF1058	H'00000000	32	Supported
	Video 1 data mode register 2	V1DMR2	R/W	H'E6EF105C	H'00000000	32	—
	Video 1 UV address offset register	V1UVAOF	R/W	H'E6EF1060	H'00000000	32	Supported
	Video 1 color space change coefficient 1 register	V1CSCC1	R/W	H'E6EF1064	H'01291080	32	Supported
	Video 1 color space change coefficient 2 register	V1CSCC2	R/W	H'E6EF1068	H'019800D0	32	Supported
	Video 1 color space change coefficient 3 register	V1CSCC3	R/W	H'E6EF106C	H'00640204	32	Supported
	Video 1 coefficient set C1A register	V1C1A	R/W	H'E6EF1080	H'00000000	32	—
	Video 1 coefficient set C1B register	V1C1B	R/W	H'E6EF1084	H'00000000	32	—
	Video 1 coefficient set C1C register	V1C1C	R/W	H'E6EF1088	H'00000000	32	—
	Video 1 coefficient set C2A register	V1C2A	R/W	H'E6EF1090	H'00000000	32	—
	Video 1 coefficient set C2B register	V1C2B	R/W	H'E6EF1094	H'00000000	32	—
	Video 1 coefficient set C2C register	V1C2C	R/W	H'E6EF1098	H'00000000	32	—
	Video 1 coefficient set C3A register	V1C3A	R/W	H'E6EF10A0	H'00000000	32	—
	Video 1 coefficient set C3B register	V1C3B	R/W	H'E6EF10A4	H'00000000	32	—
	Video 1 coefficient set C3C register	V1C3C	R/W	H'E6EF10A8	H'00000000	32	—
	Video 1 coefficient set C4A register	V1C4A	R/W	H'E6EF10B0	H'00000000	32	—
	Video 1 coefficient set C4B register	V1C4B	R/W	H'E6EF10B4	H'00000000	32	—
	Video 1 coefficient set C4C register	V1C4C	R/W	H'E6EF10B8	H'00000000	32	—
Video 1 coefficient set C5A register	V1C5A	R/W	H'E6EF10C0	H'00000000	32	—	
Video 1 coefficient set C5B register	V1C5B	R/W	H'E6EF10C4	H'00000000	32	—	

Channel	Name	Symbol	R/W	Address	Initial Value	Access Size	Internal Update Mode Support*
1 (RZ/G1H, M/N and E)	Video 1 coefficient set C5C register	V1C5C	R/W	H'E6EF10C8	H'00000000	32	—
	Video 1 coefficient set C6A register	V1C6A	R/W	H'E6EF10D0	H'00000000	32	—
	Video 1 coefficient set C6B register	V1C6B	R/W	H'E6EF10D4	H'00000000	32	—
	Video 1 coefficient set C6C register	V1C6C	R/W	H'E6EF10D8	H'00000000	32	—
	Video 1 coefficient set C7A register	V1C7A	R/W	H'E6EF10E0	H'00000000	32	—
	Video 1 coefficient set C7B register	V1C7B	R/W	H'E6EF10E4	H'00000000	32	—
	Video 1 coefficient set C7C register	V1C7C	R/W	H'E6EF10E8	H'00000000	32	—
	Video 1 coefficient set C8A register	V1C8A	R/W	H'E6EF10F0	H'00000000	32	—
	Video 1 coefficient set C8B register	V1C8B	R/W	H'E6EF10F4	H'00000000	32	—
	Video 1 coefficient set C8C register	V1C8C	R/W	H'E6EF10F8	H'00000000	32	—
	Video 1 lookup table pointer register	V1LUTP	R/W	H'E6EF1100	H'00000000	32	—
	Video 1 lookup table data register	V1LUTD	R/W	H'E6EF1104	H'xxxxxxxx	32	—
1 (RZ/G1H, M/N)	Video 1 RGB→Y calculation setting register 1	V1YCCR1	R/W	H'E6EF1228	H'00000107	32	Supported
	Video 1 RGB→Y calculation setting register 2	V1YCCR2	R/W	H'E6EF122C	H'00640204	32	Supported
	Video 1 RGB→Y calculation setting register 3	V1YCCR3	R/W	H'E6EF1230	H'0A000010	32	Supported
	Video 1 RGB→Cb calculation setting register 1	V1CBCCR1	R/W	H'E6EF1234	H'00001F68	32	Supported
	Video 1 RGB→Cb calculation setting register 2	V1CBCCR2	R/W	H'E6EF1238	H'01C21ED6	32	Supported
	Video 1 RGB→Cb calculation setting register 3	V1CBCCR3	R/W	H'E6EF123C	H'0A000080	32	Supported
	Video 1 RGB→Cr calculation setting register 1	V1CRCCR1	R/W	H'E6EF1240	H'000001C2	32	Supported
	Video 1 RGB→Cr calculation setting register 2	V1CRCCR2	R/W	H'E6EF1244	H'1FB71E87	32	Supported
	Video 1 RGB→Cr calculation setting register 3	V1CRCCR3	R/W	H'E6EF1248	H'0A000080	32	Supported
1 (RZ/G1H, M/N and E)	Video 1 YC→RGB calculation setting register 1	V1CSCE1	R/W	H'E6EF1300	H'0000129F	32	Supported
	Video 1 YC→RGB calculation setting register 2	V1CSCE2	R/W	H'E6EF1304	H'01000800	32	Supported
	Video 1 YC→RGB calculation setting register 3	V1CSCE3	R/W	H'E6EF1308	H'19890D02	32	Supported
	Video 1 YC→RGB calculation setting register 4	V1CSCE4	R/W	H'E6EF130C	H'06452045	32	Supported

**(3) Channel 2**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

Channel 2 registers include special registers for each product.

**Table 23.9 (3) VIN Registers****Channel 2 (RZ/G1H, M/N)**

Channel	Name	Symbol	R/W	Address	Initial Value	Access Size	Internal Update Mode Support*
2 (RZ/G1H, M/N)	Video 2 main control register	V2MC	R/W	H'E6EF2000	H'00000000	32	Δ
	Video 2 module status register	V2MS	R	H'E6EF2004	H'00000018	32	—
	Video 2 frame capture register	V2FC	R/W	H'E6EF2008	H'00000000	32	—
	Video 2 start line pre-clip register	V2SLPrC	R/W	H'E6EF200C	H'00000000	32	Supported
	Video 2 end line pre-clip register	V2ELPrC	R/W	H'E6EF2010	H'00000000	32	Supported
	Video 2 start pixel pre-clip register	V2SPPrC	R/W	H'E6EF2014	H'00000000	32	Supported
	Video 2 end pixel pre-clip register	V2EPPrC	R/W	H'E6EF2018	H'00000000	32	Supported
	Video 2 start line post-clip register	V2SLPoC	R/W	H'E6EF201C	H'00000000	32	Supported
	Video 2 end line post-clip register	V2ELPoC	R/W	H'E6EF2020	H'00000000	32	Supported
	Video 2 start pixel post-clip register	V2SPPoC	R/W	H'E6EF2024	H'00000000	32	Supported
	Video 2 end pixel post-clip register	V2EPPoC	R/W	H'E6EF2028	H'00000000	32	Supported
	Video 2 image stride register	V2IS	R/W	H'E6EF202C	H'00000000	32	Supported
	Video 2 memory base 1 register	V2MB1	R/W	H'E6EF2030	H'00000000	32	Supported
	Video 2 memory base 2 register	V2MB2	R/W	H'E6EF2034	H'00000000	32	Supported
	Video 2 memory base 3 register	V2MB3	R/W	H'E6EF2038	H'00000000	32	Supported
	Video 2 line count register	V2LC	R	H'E6EF203C	H'00000000	32	—
	Video 2 interrupt enable register	V2IE	R/W	H'E6EF2040	H'00000000	32	—
	Video 2 interrupt status register	V2INTS	R/W	H'E6EF2044	H'00000000	32	—
	Video 2 scanline interrupt register	V2SI	R/W	H'E6EF2048	H'00000000	32	Supported
	Video 2 Memory Transfer Control register	V2MTC	R/W	H'E6EF204C	H'0A080108	32	Supported
Video 2 Y scale register	V2YS	R/W	H'E6EF2050	H'00000000	32	Supported	
Video 2 X scale register	V2XS	R/W	H'E6EF2054	H'00000000	32	Supported	
Video 2 data mode register	V2DMR	R/W	H'E6EF2058	H'00000000	32	Supported	

Channel	Name	Symbol	R/W	Address	Initial Value	Access Size	Internal Update Mode Support*
2 (RZ/G1H, M/N)	Video 2 data mode register	V2DMR2	R/W	H'E6EF205C	H'00000000	32	—
	Video 2 UV address offset register	V2UVAOF	R/W	H'E6EF2060	H'00000000	32	Supported
	Video 2 color space change coefficient 1 register	V2CSCC1	R/W	H'E6EF2064	H'01291080	32	Supported
	Video 2 color space change coefficient 2 register	V2CSCC2	R/W	H'E6EF2068	H'019800D0	32	Supported
	Video 2 color space change coefficient 3 register	V2CSCC3	R/W	H'E6EF206C	H'00640204	32	Supported
	Video 2 coefficient set C1A register	V2C1A	R/W	H'E6EF2080	H'00000000	32	—
	Video 2 coefficient set C1B register	V2C1B	R/W	H'E6EF2084	H'00000000	32	—
	Video 2 coefficient set C1C register	V2C1C	R/W	H'E6EF2088	H'00000000	32	—
	Video 2 coefficient set C2A register	V2C2A	R/W	H'E6EF2090	H'00000000	32	—
	Video 2 coefficient set C2B register	V2C2B	R/W	H'E6EF2094	H'00000000	32	—
	Video 2 coefficient set C3C register	V2C2C	R/W	H'E6EF2098	H'00000000	32	—
	Video 2 coefficient set C3A register	V2C3A	R/W	H'E6EF20A0	H'00000000	32	—
	Video 2 coefficient set C3B register	V2C3B	R/W	H'E6EF20A4	H'00000000	32	—
	Video 2 coefficient set C3C register	V2C3C	R/W	H'E6EF20A8	H'00000000	32	—
	Video 2 coefficient set C4A register	V2C4A	R/W	H'E6EF20B0	H'00000000	32	—
	Video 2 coefficient set C4B register	V2C4B	R/W	H'E6EF20B4	H'00000000	32	—
	Video 2 coefficient set C4C register	V2C4C	R/W	H'E6EF20B8	H'00000000	32	—
	Video 2 coefficient set C5A register	V2C5A	R/W	H'E6EF20C0	H'00000000	32	—
	Video 2 coefficient set C5B register	V2C5B	R/W	H'E6EF20C4	H'00000000	32	—
	Video 2 coefficient set C5C register	V2C5C	R/W	H'E6EF20C8	H'00000000	32	—
	Video 2 coefficient set C6A register	V2C6A	R/W	H'E6EF20D0	H'00000000	32	—
	Video 2 coefficient set C6B register	V2C6B	R/W	H'E6EF20D4	H'00000000	32	—
	Video 2 coefficient set C6C register	V2C6C	R/W	H'E6EF20D8	H'00000000	32	—
Video 2 coefficient set C7A register	V2C7A	R/W	H'E6EF20E0	H'00000000	32	—	
Video 2 coefficient set C7B register	V2C7B	R/W	H'E6EF20E4	H'00000000	32	—	



Channel	Name	Symbol	R/W	Address	Initial Value	Access Size	Internal Update Mode Support*
2 (RZ/G1H, M/N)	Video 2 coefficient set C7C register	V2C7C	R/W	H'E6EF20E8	H'00000000	32	—
2 (RZ/G1H only)	Video 2 coefficient set C8A register	V2C8A	R/W	H'E6EF20F0	H'00000000	32	—
	Video 2 coefficient set C8B register	V2C8B	R/W	H'E6EF20F4	H'00000000	32	—
	Video 2 coefficient set C8C register	V2C8C	R/W	H'E6EF20F8	H'00000000	32	—
	Video 2 lookup table pointer	V2LUTP	R/W	H'E6EF2100	H'00000000	32	—
	Video 2 lookup table data register	V2LUTD	R/W	H'E6EF2104	H'xxxxxxxx	32	—
	Video 2 RGB→Y calculation setting register 1	V2YCCR1	R/W	H'E6EF2228	H'00000107	32	Supported
	Video 2 RGB→Y calculation setting register 2	V2YCCR2	R/W	H'E6EF222C	H'00640204	32	Supported
	Video 2 RGB→Y calculation setting register 3	V2YCCR3	R/W	H'E6EF2230	H'0A000010	32	Supported
	Video 2 RGB→Cb calculation setting register 1	V2CBCCR1	R/W	H'E6EF2234	H'00001F68	32	Supported
	Video 2 RGB→Cb calculation setting register 2	V2CBCCR2	R/W	H'E6EF2238	H'01C21ED6	32	Supported
	Video 2 RGB→Cb calculation setting register 3	V2CBCCR3	R/W	H'E6EF223C	H'0A000080	32	Supported
	Video 2 RGB→Cr calculation setting register 1	V2CRCCR1	R/W	H'E6EF2240	H'000001C2	32	Supported
	Video 2 RGB→Cr calculation setting register 2	V2CRCCR2	R/W	H'E6EF2244	H'1FB71E87	32	Supported
Video 2 RGB→Cr calculation setting register 3	V2CRCCR3	R/W	H'E6EF2248	H'0A000080	32	Supported	

**(4) Channel 3**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	—	—	—

Channel 3 registers include special registers for each product.

**Table 23.9 (4) VIN Registers****Channel 3 (RZ/G1H)**

Channel	Name	Symbol	R/W	Address	Initial Value	Access Size	Internal Update Mode Support*
3 (RZ/G1H only)	Video 3 main control register	V3MC	R/W	H'E6EF3000	H'00000000	32	Δ
	Video 3 module status register	V3MS	R	H'E6EF3004	H'00000018	32	—
	Video 3 frame capture register	V3FC	R/W	H'E6EF3008	H'00000000	32	—
	Video 3 start line pre-clip register	V3SLPrC	R/W	H'E6EF300C	H'00000000	32	Supported
	Video 3 end line pre-clip register	V3ELPrC	R/W	H'E6EF3010	H'00000000	32	Supported
	Video 3 start pixel pre-clip register	V3SPPrC	R/W	H'E6EF3014	H'00000000	32	Supported
	Video 3 end pixel pre-clip register	V3EPPrC	R/W	H'E6EF3018	H'00000000	32	Supported
	Video 3 start line post-clip register	V3SLPoC	R/W	H'E6EF301C	H'00000000	32	Supported
	Video 3 end line post-clip register	V3ELPoC	R/W	H'E6EF3020	H'00000000	32	Supported
	Video 3 start pixel post-clip register	V3SPPoC	R/W	H'E6EF3024	H'00000000	32	Supported
	Video 3 end pixel post-clip register	V3EPPoC	R/W	H'E6EF3028	H'00000000	32	Supported
	Video 3 image stride register	V3IS	R/W	H'E6EF302C	H'00000000	32	Supported
	Video 3 memory base 1 register	V3MB1	R/W	H'E6EF3030	H'00000000	32	Supported
	Video 3 memory base 2 register	V3MB2	R/W	H'E6EF3034	H'00000000	32	Supported
	Video 3 memory base 3 register	V3MB3	R/W	H'E6EF3038	H'00000000	32	Supported
	Video 3 line count register	V3LC	R	H'E6EF303C	H'00000000	32	—
	Video 3 interrupt enable register	V3IE	R/W	H'E6EF3040	H'00000000	32	—
	Video 3 interrupt status register	V3INTS	R/W	H'E6EF3044	H'00000000	32	—
	Video 3 scanline interrupt register	V3SI	R/W	H'E6EF3048	H'00000000	32	Supported
	Video 3 Memory Transfer Control register	V3MTC	R/W	H'E6EF304C	H'0A080108	32	Supported
Video 3 Y scale register	V3YS	R/W	H'E6EF3050	H'00000000	32	Supported	
Video 3 X scale register	V3XS	R/W	H'E6EF3054	H'00000000	32	Supported	
Video 3 data mode register	V3DMR	R/W	H'E6EF3058	H'00000000	32	Supported	

Channel	Name	Symbol	R/W	Address	Initial Value	Access Size	Internal Update Mode Support*
3 (RZ/G1H only)	Video 3 data mode register 2	V3DMR2	R/W	H'E6EF305C	H'00000000	32	—
	Video 3 UV address offset register	V3UVAOF	R/W	H'E6EF3060	H'00000000	32	Supported
	Video 3 color space change coefficient 1 register	V3CSCC1	R/W	H'E6EF3064	H'01291080	32	Supported
	Video 3 color space change coefficient 2 register	V3CSCC2	R/W	H'E6EF3068	H'019800D0	32	Supported
	Video 3 color space change coefficient 3 register	V3CSCC3	R/W	H'E6EF306C	H'00640204	32	Supported
	Video 3 coefficient set C1A register	V3C1A	R/W	H'E6EF3080	H'00000000	32	—
	Video 3 coefficient set C1B register	V3C1B	R/W	H'E6EF3084	H'00000000	32	—
	Video 3 coefficient set C1C register	V3C1C	R/W	H'E6EF3088	H'00000000	32	—
	Video 3 coefficient set C2A register	V3C2A	R/W	H'E6EF3090	H'00000000	32	—
	Video 3 coefficient set C2B register	V3C2B	R/W	H'E6EF3094	H'00000000	32	—
	Video 3 coefficient set C2C register	V3C2C	R/W	H'E6EF3098	H'00000000	32	—
	Video 3 coefficient set C3A register	V3C3A	R/W	H'E6EF30A0	H'00000000	32	—
	Video 3 coefficient set C3B register	V3C3B	R/W	H'E6EF30A4	H'00000000	32	—
	Video 3 coefficient set C3C register	V3C3C	R/W	H'E6EF30A8	H'00000000	32	—
	Video 3 coefficient set C4A register	V3C4A	R/W	H'E6EF30B0	H'00000000	32	—
	Video 3 coefficient set C4B register	V3C4B	R/W	H'E6EF30B4	H'00000000	32	—
	Video 3 coefficient set C4C register	V3C4C	R/W	H'E6EF30B8	H'00000000	32	—
	Video 3 coefficient set C5A register	V3C5A	R/W	H'E6EF30C0	H'00000000	32	—
	Video 3 coefficient set C5B register	V3C5B	R/W	H'E6EF30C4	H'00000000	32	—
	Video 3 coefficient set C5C register	V3C5C	R/W	H'E6EF30C8	H'00000000	32	—
	Video 3 coefficient set C6A register	V3C6A	R/W	H'E6EF30D0	H'00000000	32	—
	Video 3 coefficient set C6B register	V3C6B	R/W	H'E6EF30D4	H'00000000	32	—
	Video 3 coefficient set C6C register	V3C6C	R/W	H'E6EF30D8	H'00000000	32	—
Video 3 coefficient set C7A register	V3C7A	R/W	H'E6EF30E0	H'00000000	32	—	
Video 3 coefficient set C7B register	V3C7B	R/W	H'E6EF30E4	H'00000000	32	—	

Channel	Name	Symbol	R/W	Address	Initial Value	Access Size	Internal Update Mode Support*
3 (RZ/G1H only)	Video 3 coefficient set C7C register	V3C7C	R/W	H'E6EF30E8	H'00000000	32	—
	Video 3 coefficient set C8A register	V3C8A	R/W	H'E6EF30F0	H'00000000	32	—
	Video 3 coefficient set C8B register	V3C8B	R/W	H'E6EF30F4	H'00000000	32	—
	Video 3 coefficient set C8C register	V3C8C	R/W	H'E6EF30F8	H'00000000	32	—

## 23.2 Register Descriptions

RZ/G1H	RZ/G1N
RZ/G1M	RZ/G1E

[Legend]

—: Reserved. The write value should always be 0.

Initial value: Register value after a reset

R/W: Readable/writable. The written value can be read.

R: Read-only. The write value should always be 0.

Vn: Video Channel n

### 23.2.1 Video n Main Control Register (VnMC)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√*	√	√	√

Notes: Availability of channels:

n = 0 to 3 (RZ/G1H), 0 to 2 (RZ/G1M/N), 0 and 1 (RZ/G1E)

\* For RZ/G1H, special function (bit 25) is available.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	FAST	—	CLP[1:0]		—	—	RIS/ —	—	—	—	FOC	LUTE	YCAL	INF[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R/W	R/W	R	R	R/W	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DC[1:0]		EXINF[1:0]		—	VUP	—	—	—	EN	EC	IM[1:0]		—	BPS	ME
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R	R/W	R	R	R	R/W	R/W	R/W	R/W	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description																	
31	FAST	0	R/W	High-Speed Video Clock Support Mode Set this bit to 1 to input 100-MHz video clock. 0: 100-MHz video clock input is not supported. 1: 100-MHz video clock input is supported. Note: Do not perform vertical or horizontal scaling up when this bit is 1.																	
30	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.																	
29, 28	CLP[1:0]	00	R/W	Pixel Data Clipping When the input image data is in the YCbCr format, these bits specify the data clip value for clipping the YCbCr-RGB color conversion input data to the nominal range prescribed in the ITU-R BT.601 standard. <table border="1"> <thead> <tr> <th>CLP</th> <th>Luminance</th> <th>Color Difference</th> <th>Initial value</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>No clipping</td> <td>16 or a smaller value is clipped to 16. 240 or a greater value is clipped to 240.</td> <td rowspan="4">Initial value</td> </tr> <tr> <td>01</td> <td>16 or a smaller value is clipped to 16. 240 or a greater value is clipped to 240.</td> <td>16 or a smaller value is clipped to 16. 240 or a greater value is clipped to 240.</td> </tr> <tr> <td>10</td> <td>No clipping</td> <td>16 or a smaller value is clipped to 128. 240 or a greater value is clipped to 128.</td> </tr> <tr> <td>11</td> <td>No clipping</td> <td>No clipping</td> </tr> </tbody> </table> Note: These bits support the internal update mode.	CLP	Luminance	Color Difference	Initial value	00	No clipping	16 or a smaller value is clipped to 16. 240 or a greater value is clipped to 240.	Initial value	01	16 or a smaller value is clipped to 16. 240 or a greater value is clipped to 240.	16 or a smaller value is clipped to 16. 240 or a greater value is clipped to 240.	10	No clipping	16 or a smaller value is clipped to 128. 240 or a greater value is clipped to 128.	11	No clipping	No clipping
CLP	Luminance	Color Difference	Initial value																		
00	No clipping	16 or a smaller value is clipped to 16. 240 or a greater value is clipped to 240.	Initial value																		
01	16 or a smaller value is clipped to 16. 240 or a greater value is clipped to 240.	16 or a smaller value is clipped to 16. 240 or a greater value is clipped to 240.																			
10	No clipping	16 or a smaller value is clipped to 128. 240 or a greater value is clipped to 128.																			
11	No clipping	No clipping																			
27, 26	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.																	

Bit	Bit Name	Initial Value	R/W	Description
25	RIS/—	0	R/W	<p>RGB/YCbCr Interface Select [RZ/G1H]</p> <p>This bit chooses capturing method of the video clock.</p> <p>0: Sync data are captured on rising edges of the video clock signal.</p> <p>1: Sync data are captured on rising and falling edges of the video clock signal.</p> <hr/> <p>Reserved [RZ/G1M/N, E]</p> <p>This bit is always read as 0. The write value should always be 0.</p>
24 to 22	—	All 0	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>
21	FOC	0	R/W	<p>Field Order Control</p> <p>This bit controls the field order for full interlace capturing.</p> <p>0: Top field = Odd field (field 1)</p> <p>1: Top field = Even field (field 2)</p> <p>Note: This bit supports the internal update mode.</p>
20	LUTE	0	R/W	<p>Lookup Table Enable</p> <p>This bit enables lookup table conversion from 10 bits to 8 bits.</p> <p>0: LUT is not used.</p> <p>1: LUT is used.</p> <p>Notes: 1. To perform LUT conversion, the conversion table should be set with VnLUTP and VnLUTD.</p> <p>2. This bit supports the internal update mode.</p>
19	YCAL	0	R/W	<p>YCbCr-422 Input Data Alignment</p> <p>This bit controls data alignment for YCbCr-422 input.</p> <p>0: When the multiplexed CbCr interface is set, capturing is performed with Y in the upper bits and CbCr in the lower bits.</p> <p>1: When the multiplexed CbCr interface is set, capturing is performed with CbCr in the upper bits and Y in the lower bits.</p>
18 to 16	INF[2:0]	000	R/W	<p>Input Interface Format</p> <p>These bits specify the image format input to the VIN.</p> <p>000: ITU-R BT.656 8-bit YCbCr-422 or ITU-R BT.656 8-bit YCbCr422 4-bit input*<sup>1</sup></p> <p>001: ITU-R BT.601/BT.709 8-bit YCbCr-422 or ITU-R BT.601/BT.709 8-bit YCbCr422 4-bit input *<sup>1</sup></p> <p>010: ITU-R BT.656 10/12-bit YCbCr-422*<sup>1</sup></p> <p>011: ITU-R BT.601/BT.709 10/12-bit YCbCr-422*<sup>1</sup></p> <p>100: Setting prohibited</p> <p>101: ITU-R BT.601/BT.1358 16-bit YCbCr-422 or ITU-R BT.601/BT.709/BT.656 8-bit YCbCr422 8-bit input*<sup>1</sup></p> <p>110: ITU-R BT.601/BT.709 24-bit RGB-888*<sup>1</sup></p> <p>111: ITU-R BT.601/BT.709 18-bit RGB-666 or ITU-R BT.601/BT.709 RGB-888 12-bit input*<sup>1</sup></p>

Bit	Bit Name	Initial Value	R/W	Description
15, 14	DC[1:0]	00	R/W	<p>Dithering Mode Control</p> <p>These bits select the dithering mode for conversion from RGB888 to RGB565/ARGB1565.</p> <p>00: Dithering with cumulative addition  01: Ordered dithering  10: Setting prohibited  11: Setting prohibited</p>
13, 12	EXINF[1:0]	00	R/W	<p>Extension Interface Select</p> <p>00: Data extension is not performed  01: Combined with the INF setting, 8-bit data extension is performed.  10: Combined with the INF setting, 10-bit data extension is performed.  11: Combined with the INF setting, 12-bit data extension is performed.</p>
11	—	0	R	<p>Reserved</p> <p>This bit is always read as 0. The write value should always be 0.</p>
10	VUP	0	R/W	<p>VIN Register Update Control</p> <p>This bit specifies the internal register update timing after register writing. See the list of registers for applicable registers.</p> <p>0: The register contents are updated immediately after register writing.  1: The register contents are updated after a valid field is detected in the ITU-R BT.601 data or the field (F) bit changes in the ITU-R BT.656 data.</p>
9 to 7	—	All 0	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>
6	EN	0	R/W	<p>Endian Type</p> <p>This bit specifies the endian type for data to be output to external memory.</p> <p>0: Image data is packed and allocated in little endian.  1: Image data is packed and allocated in big endian.</p> <p>Note: When allocating the YCbCr422 (UYVY format) data in big endian, be sure to set the BPSM bit in VnDMR to 1.</p>
5	EC	0	R/W	<p>Error Correction Control</p> <p>This bit specifies whether error correction with the parity bit is performed on the ITU-R BT.656 input.</p> <p>0: Error correction is not performed on the ITU-R BT.656 input.  1: Error correction with the parity bit is performed on the ITU-R BT.656 input.</p> <p>Error correction must not be performed in the following cases:</p> <ul style="list-style-type: none"> <li>• When data is captured in the ITU-R BT.601 interface</li> <li>• When input data does not meet the standard of the ITU-R BT.656 parity bit</li> </ul>



Bit	Bit Name	Initial Value	R/W	Description
4, 3	IM[1:0]	00	R/W	<p>Interlace Mode</p> <p>These bits specify the capture mode. Do not modify this setting during capture operation.</p> <p>00: Odd-field (field 1) capture mode Handles only odd fields as frames and stores them in external memory.</p> <p>01: Odd-/even-field capture mode Handles odd and even fields as separate frames and stores them in external memory. This mode is available only in continuous frame capture mode.</p> <p>10: Even-field (field 2) capture mode Handles only even fields as frames and stores them in external memory.</p> <p>11: Full interlace mode Handles combinations of odd and even fields as single frames and stores them in external memory.</p>
2	—	0	R	<p>Reserved</p> <p>This bit is always read as 0. The write value should always be 0.</p>
1	BPS	0	R/W	<p>Color Space Conversion Bypass Mode</p> <p>0: The input YCbCr data is converted into the RGB color space and RGB data is converted into the YCbCr color space*<sup>2</sup>.</p> <p>1: Color space conversion is not performed.</p> <p>Note: YCbCr→RGB or RGB→YCbCr conversion is performed with the coefficients specified by the YC-RGB conversion coefficient register or RGB-YC coefficient register.</p>
0	ME	0	R/W	<p>Module Enable</p> <p>This is the enable bit for the VIN. Set this bit before setting the Frame Capture (VnFC) register.</p> <p>0: The module operation is stopped.</p> <p>1: The module operation is enabled. *<sup>3</sup></p>

- Notes:
1. Table 23.10 shows the combinations of interfaces which can be set by the input interface format (the INF bits in VnMC) and extension interface select (the EXINF bit in VnMC). Do not make the other settings.
  2. Table 23.11 shows the image data which can be converted according to the color space conversion bypass mode settings (set by the BPS bit in VnMC).
  3. To stop capturing operation, only set the ME bit to 0. Do not change the other bit settings.

**Table 23.10 Capture Interface Settings**

Interface		VnMC/EXINF	VnMC/RIS*	VnMC/INF
ITU-R BT.656 (multiplexed YCbCr422)	8 bits	00	0	000
	10 bits	00	0	010
	12 bits	11	0	010
ITU-R BT.656 (multiplexed YCbCr422/4-bit input, double-edge capture)*	4 bits	00	1	000
ITU-R BT.601/BT.709 (multiplexed YCbCr422)	8 bits	00	0	001
	10 bits	00	0	011
	12 bits	11	0	011
ITU-R BT.601/BT.709 (multiplexed YCbCr422/4-bit input, double-edge capture)*	4 bits	00	1	001
ITU-R BT.601/BT.709/BT.1358 (non-multiplexed Y/multiplexed CbCr)	16 bits	00	0	101
	20 bits	10	0	101
	24 bits	11	0	101
ITU-R BT.656 (multiplexed YCbCr422/8-bit input, double-edge capture)*	8 bits	01	1	101
ITU-R BT.601/BT.709 (multiplexed YCbCr422/8-bit input, double-edge capture)*	8 bits	00	1	101
ITU-R BT.601/BT.709 (RGB666)	18 bits	00	0	111
ITU-R BT.601/BT.709 (RGB888/double-edge capture)*	12 bits	00	1	111
ITU-R BT.601/BT.709 (RGB888/single-edge capture)	24 bits	00	0	110

Note: \* RZ/G1H only.

**Table 23.11 Captured Data Formats**

Input Data Format	VnMC/INF	VnMC/BPS	Captured Data Format
ITU-R BT.656/BT.601/BT.709/BT.1358 YCbCr	000/001	0	RGB format
	010/011	1	YCbCr format
	100/101		
ITU-R BT.601/BT.709 RGB	110/111	0	YCbCr format
		1	RGB format

### 23.2.2 Video n Module Status Register (VnMS)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Note: Availability of channels:

n = 0 to 3 (RZ/G1H), 0 to 2 (RZ/G1M/N), 0 and 1 (RZ/G1E)

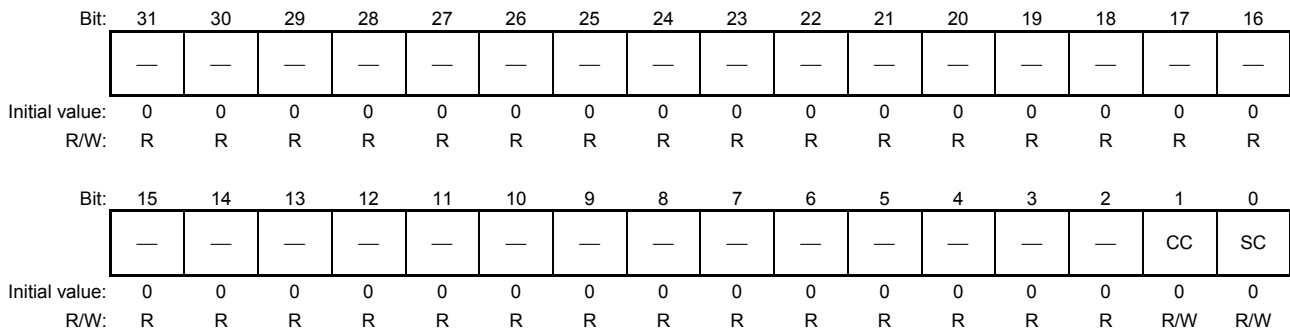
Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	FBS[1:0]	FS	AV	CA	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4, 3	FBS[1:0]	11	R	Frame Buffer Status These bits show the frame buffer status. 00: The latest valid frame buffer has the base address defined by the memory base 1 register. 01: The latest valid frame buffer has the base address defined by the memory base 2 register. 10: The latest valid frame buffer has the base address defined by the memory base 3 register. 11: There is no valid frame buffer.
2	FS	0	R	Field Status This bit shows the type of the current capture field. 0: The current field is an odd field (field 1). 1: The current field is an even field (field 2).
1	AV	0	R	Active Video Status This bit shows whether the current field is in the active video area defined by the pre-clipping register. 0: The current field is not in the active video area. 1: The current field is in the active video area. Note: This bit will be 0 if no input data is captured.
0	CA	0	R	Video Capture Active Status This bit shows the current video capture operation status. This bit is updated by the captured field signal. 0: Video capture is not operating. 1: Video capture is operating. Note: In field capture mode, this bit is set to 1 even for the field that does not capture data.

**23.2.3 Video n Frame Capture Register (VnFC)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Note: Availability of channels:  
 n = 0 to 3 (RZ/G1H), 0 to 2 (RZ/G1M/N), 0 and 1 (RZ/G1E)



Bit	Bit Name	Initial Value	R/W	Description
31 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	CC	0	R/W	Continuous Frame Capture Mode  This bit specifies the continuous frame capture mode. In this mode, the first capture frame is written into the memory address specified by the memory base 1 (VnMB1) register. After that, the capture operation is repeated in the order of MB2, MB3, MB1, MB2, and such.  Writing 0 into this bit during continuous capture operation will immediately terminate the capture operation if the current frame is completed or it has not been captured.  0: The continuous frame capture mode is not set. 1: The continuous frame capture mode is set.
0	SC	0	R/W	Single Frame Capture Mode  This bit specifies the single frame capture mode. In this mode, the capture frame is written into the memory address specified by the memory base 1 (VnMB1) register.  Immediately after this bit is set to 1, the frame buffer status (FBS) bits in MS are initialized and the SC bit is also cleared to 0.  0: The single frame capture mode is not set. 1: The single frame capture mode is set.  Note: Do not set this bit to 1 when the interlace mode (IM) bits in the main control register (VnMC) are set to 01 (odd-/even-field capture mode).

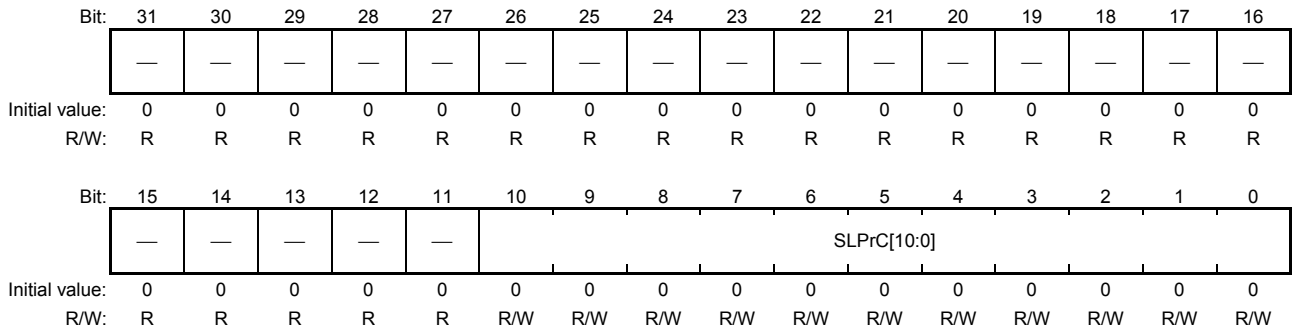
Note: Do not specify the single frame capture mode and continuous frame capture mode at the same time.

**23.2.4 Video n Start Line Pre-Clip Register (VnSLPrC)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Note: Availability of channels:

n = 0 to 3 (RZ/G1H), 0 to 2 (RZ/G1M/N), 0 and 1 (RZ/G1E)



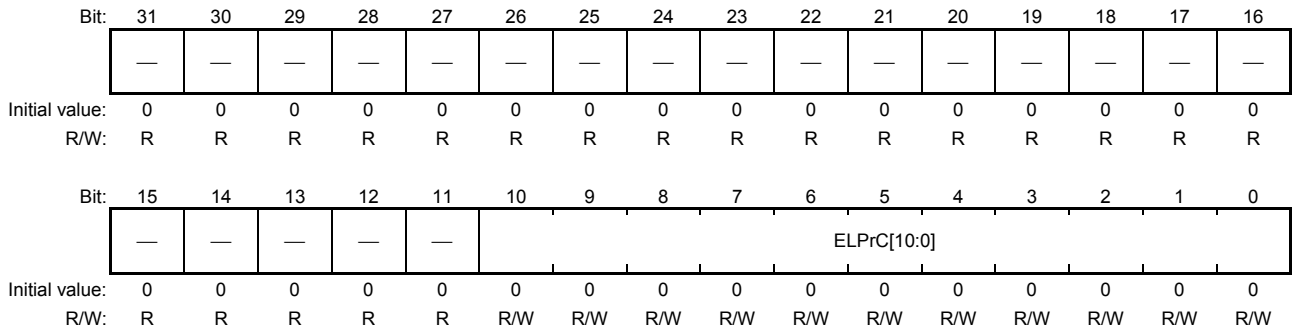
Bit	Bit Name	Initial Value	R/W	Description
31 to 11	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
10 to 0	SLPrC[10:0]	H'000	R/W	Start Line Pre-Clip These bits specify the (pre-clipping start line – 1) value in line units. This value is used before scaling. Specify a value in the range from 0 to 2046 so that the number of lines after pre-clipping will be 2 or more. (The value of 0 indicates the first valid line.)

**23.2.5 Video n End Line Pre-Clip Register (VnELPrC)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Note: Availability of channels:

n = 0 to 3 (RZ/G1H), 0 to 2 (RZ/G1M/N), 0 and 1 (RZ/G1E)



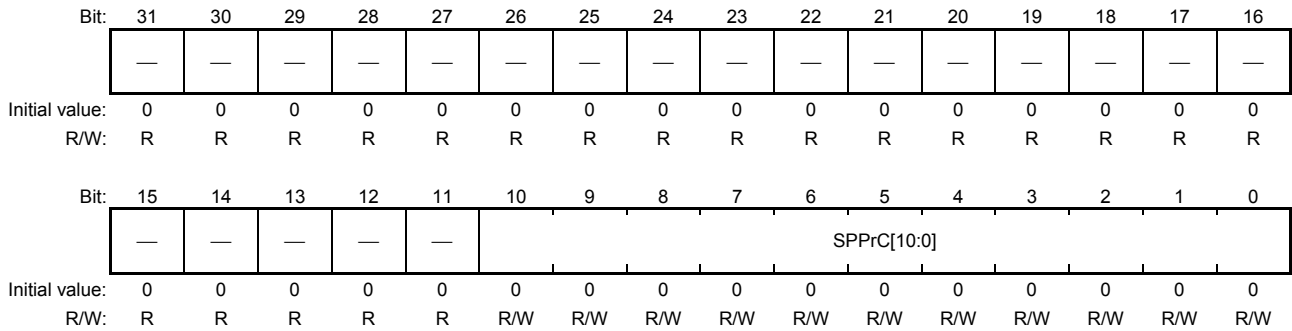
Bit	Bit Name	Initial Value	R/W	Description
31 to 11	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
10 to 0	ELPrC[10:0]	H'000	R/W	End Line Pre-Clip These bits specify the (pre-clipping end line – 1) value in line units. This value is used before scaling. Specify a value in the range from 1 to 2047 so that the number of lines after pre-clipping will be 2 or more.

**23.2.6 Video n Start Pixel Pre-Clip Register (VnSPPrC)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Note: Availability of channels:

n = 0 to 3 (RZ/G1H), 0 to 2 (RZ/G1M/N), 0 and 1 (RZ/G1E)



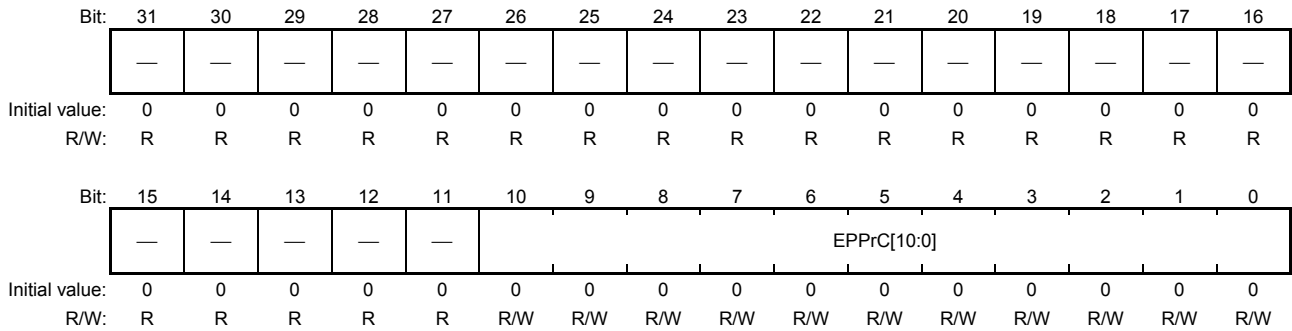
Bit	Bit Name	Initial Value	R/W	Description
31 to 11	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
10 to 0	SPPrC[10:0]	H'000	R/W	Start Pixel Pre-Clip These bits specify the (pre-clipping start pixel – 1) value in pixel units. This value is used before scaling. Specify a value in the range from 0 to 2042 so that the number of pixels after pre-clipping will be an even number than 6. Notes: 1. When SPPrC is set to 0x0, the first valid pixel is specified. 2. Specify an even number. 3. The capacity of the internal buffer is limited, so if the horizontal scaling up function is in use, the value here should be such that EPPrC – SPPrC is no greater than 2048 pixels.

**23.2.7 Video n End Pixel Pre-Clip Register (VnEPPrC)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Note: Availability of channels:

n = 0 to 3 (RZ/G1H), 0 to 2 (RZ/G1M/N), 0 and 1 (RZ/G1E)



Bit	Bit Name	Initial Value	R/W	Description
31 to 11	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
10 to 0	EPPrC[10:0]	H'000	R/W	End Pixel Pre-Clip These bits specify the (pre-clipping end pixel – 1) value in pixel units. This value is used before scaling. Specify a value in the range from 5 to 2047 so that the number of pixels after pre-clipping will be an even number than 6. Notes: 1. Set this bit so that the (EPPrC – SPPrC) value is an odd number. 2. The capacity of the internal buffer is limited, so if the horizontal scaling up function is in use, the value here should be such that EPPrC – SPPrC is no greater than 2048 pixels.

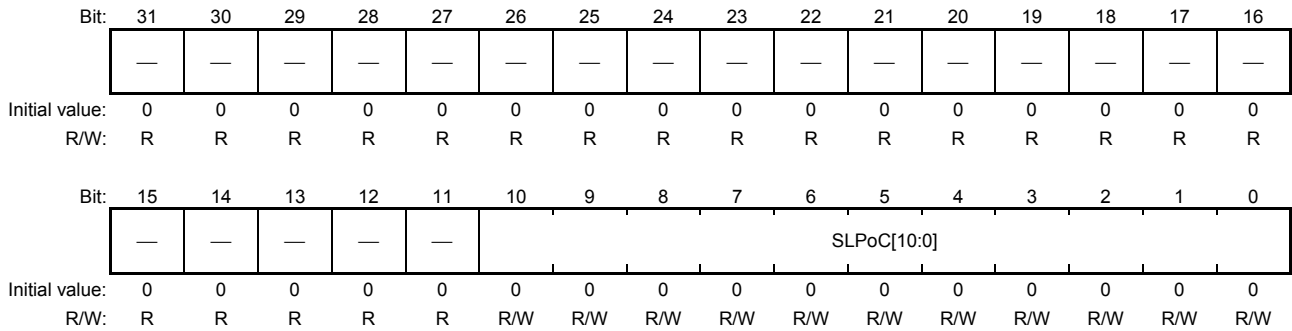


**23.2.8 Video n Start Line Post-Clip Register (VnSLPoC)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Note: Availability of channels:

n = 0 to 3 (RZ/G1H), 0 to 2 (RZ/G1M/N), 0 and 1 (RZ/G1E)



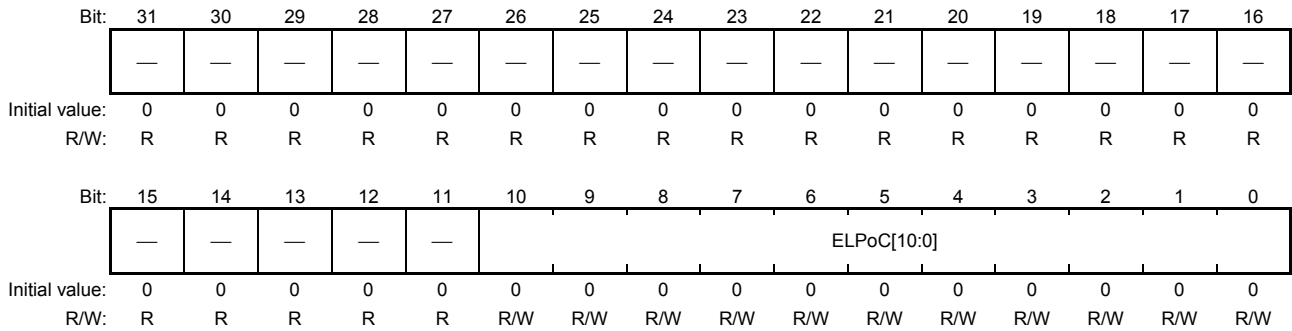
Bit	Bit Name	Initial Value	R/W	Description
31 to 11	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
10 to 0	SLPoC[10:0]	H'000	R/W	Start Line Post-Clip These bits specify the (post-clipping start line – 1) value in line units. This value is used after scaling. Specify a value in the range from 0 to 2046 so that the number of lines after post-clipping will be 2 or more. (The value of 0 indicates the start line after scaling.)

**23.2.9 Video n End Line Post-Clip Register (VnELPoC)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Note: Availability of channels:

n = 0 to 3 (RZ/G1H), 0 to 2 (RZ/G1M/N), 0 and 1 (RZ/G1E)



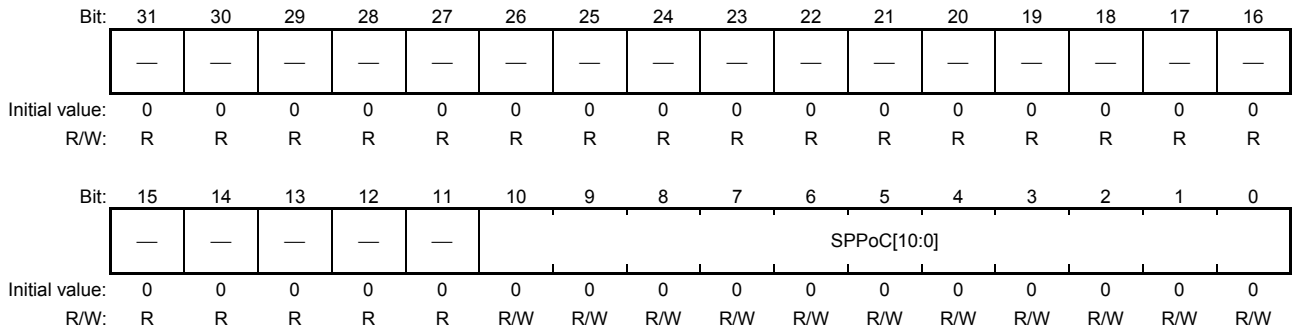
Bit	Bit Name	Initial Value	R/W	Description
31 to 11	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
10 to 0	ELPoC[10:0]	H'000	R/W	End Line Post-Clip These bits specify the (post-clipping end line – 1) value in line units. This value is used after scaling. Specify a value in the range from 1 to 2047 so that the number of lines after post-clipping will be 2 or more.

**23.2.10 Video n Start Pixel Post-Clip Register (VnSPPoC)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Note: Availability of channels:

n = 0 to 3 (RZ/G1H), 0 to 2 (RZ/G1M/N), 0 and 1 (RZ/G1E)



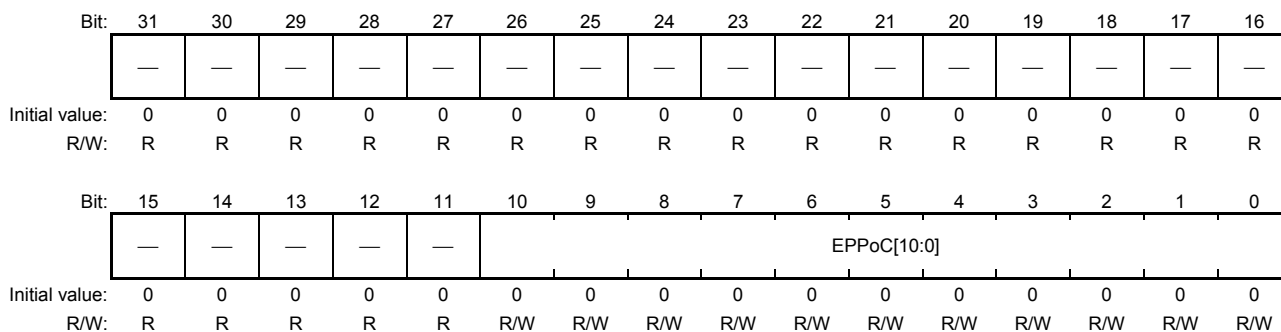
Bit	Bit Name	Initial Value	R/W	Description
31 to 11	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
10 to 0	SPPoC[10:0]	H'000	R/W	Start Pixel Post-Clip These bits specify the (post-clipping start pixel – 1) value in pixel units. This value is used after scaling. Specify a value in the range from 0 to 2042 so that the number of pixels after post-clipping will be 5 or more.

### 23.2.11 Video n End Pixel Post-Clip Register (VnEPPoC)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Note: Availability of channels:

n = 0 to 3 (RZ/G1H), 0 to 2 (RZ/G1M/N), 0 and 1 (RZ/G1E)



Bit	Bit Name	Initial Value	R/W	Description
31 to 11	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
10 to 0	EPPoC[10:0]	H'000	R/W	End Pixel Post-Clip These bits specify the (post-clipping end pixel – 1) value in pixel units. This value is used after scaling. Specify a value in the range from 5 to 2047 so that the number of pixels after post-clipping will be 5 or more.

Note: When the output format is YCbCr-422, even if the settings produce a post-clipping size in pixels that is an odd number, the output to memory will be in even pixel units. Note that if the clipping values specify an odd size (i.e. if EPPoC – SPPoC is odd), one will be added to round the value up to an even number.

Example: When SPPoC is set to 0 and EPPoC is set to 62:

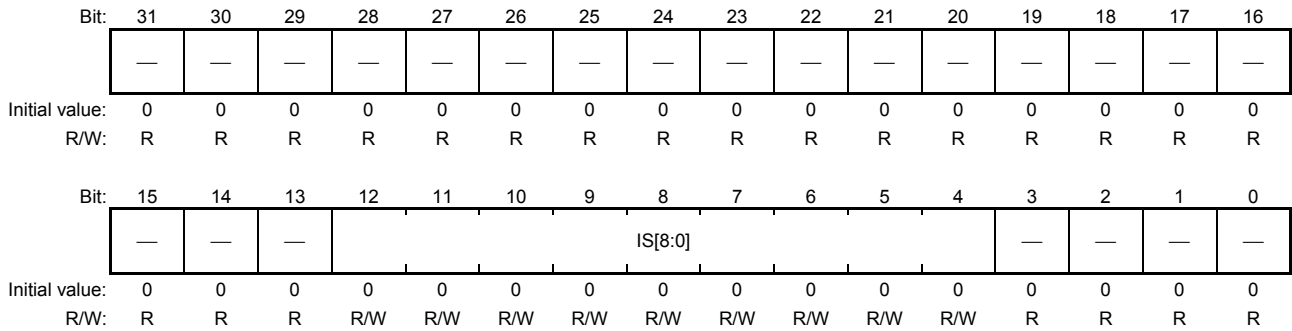
The actual processing is done for 64 pixels.  
 62 - 0 = 62 (63 pixels)  
 63 pixels + 1 = 64 pixels

**23.2.12 Video n Image Stride Register (VnIS)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Note: Availability of channels:

n = 0 to 3 (RZ/G1H), 0 to 2 (RZ/G1M/N), 0 and 1 (RZ/G1E)



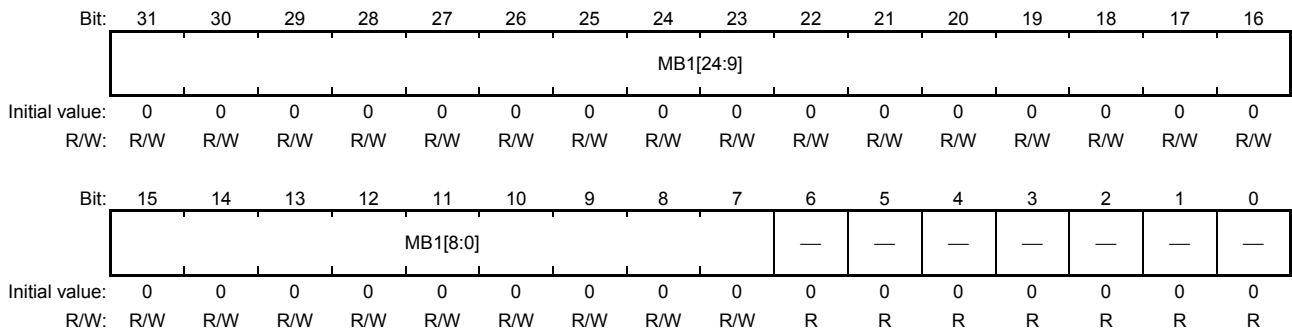
Bit	Bit Name	Initial Value	R/W	Description
31 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12 to 4	IS[8:0]	H'000	R/W	Image Stride These bits specify the width of the transfer destination memory. Specify a value no less than the post-clipping width (EPPoC - SPPoC) and aligned with a 32-byte boundary (i.e. bit 4 should be specified as 0). For 16 bits/pixel data, word addresses are generated. For 8 bits/pixel data in YC separation mode, byte addresses are generated.
3 to 0	—	All 0	R	Reserved bits that indicate the lower-order four bits of the image stride. These bits are always read as 0. The write value should always be 0.

**23.2.13 Video n Memory Base 1 Register (VnMB1)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Note: Availability of channels:

n = 0 to 3 (RZ/G1H), 0 to 2 (RZ/G1M/N), 0 and 1 (RZ/G1E)



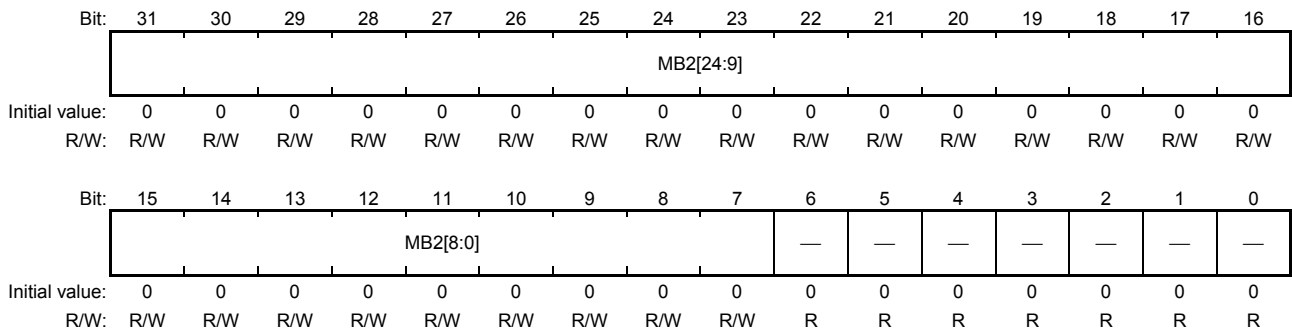
Bit	Bit Name	Initial Value	R/W	Description
31 to 7	MB1[24:0]	H'0000000	R/W	<p>Memory Base Address 1</p> <p>These bits specify the transfer start address in frame buffer 1. Specify a value for physical address bits [31:7] in units of 128 bytes.</p> <p>If the module is in continuous frame capture mode, this value is used as the MB1 address in the following capture sequence: MB1 → MB2 → MB3 → MB1 → MB2 → MB3.</p> <p>In single frame capture mode, this value is used as the capture address.</p> <p>Specify a memory address taking into account the image size so that the image data does not exceed an area boundary on the address map.</p>
6 to 0	—	All 0	R	<p>Reserved bits that indicate the lower-order seven bits of memory base address 1 (a multiple of 128 bytes).</p> <p>These bits are always read as 0. The write value should always be 0.</p>

**23.2.14 Video n Memory Base 2 Register (VnMB2)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Note: Availability of channels:

n = 0 to 3 (RZ/G1H), 0 to 2 (RZ/G1M/N), 0 and 1 (RZ/G1E)

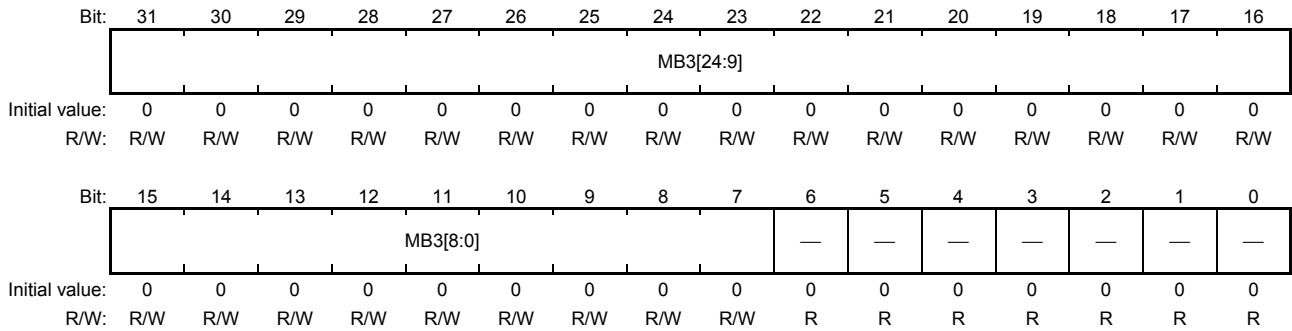


Bit	Bit Name	Initial Value	R/W	Description
31 to 7	MB2[24:0]	H'0000000	R/W	<p>Memory Base Address 2</p> <p>These bits specify the transfer start address in frame buffer 2. Specify a value for physical address bits [31:7] in units of 128 bytes.</p> <p>If the module is in continuous frame capture mode, this value is used as the MB2 address in the following capture sequence: MB1 → MB2 → MB3 → MB1 → MB2 → MB3.</p> <p>Specify a memory address taking into account the image size so that the image data does not exceed an area boundary on the address map.</p>
6 to 0	—	All 0	R	<p>Reserved bits that indicate the lower-order seven bits of memory base address 2 (a multiple of 128 bytes).</p> <p>These bits are always read as 0. The write value should always be 0.</p>

**23.2.15 Video n Memory Base 3 Register (VnMB3)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Note: Availability of channels:  
 n = 0 to 3 (RZ/G1H), 0 to 2 (RZ/G1M/N), 0 and 1 (RZ/G1E)



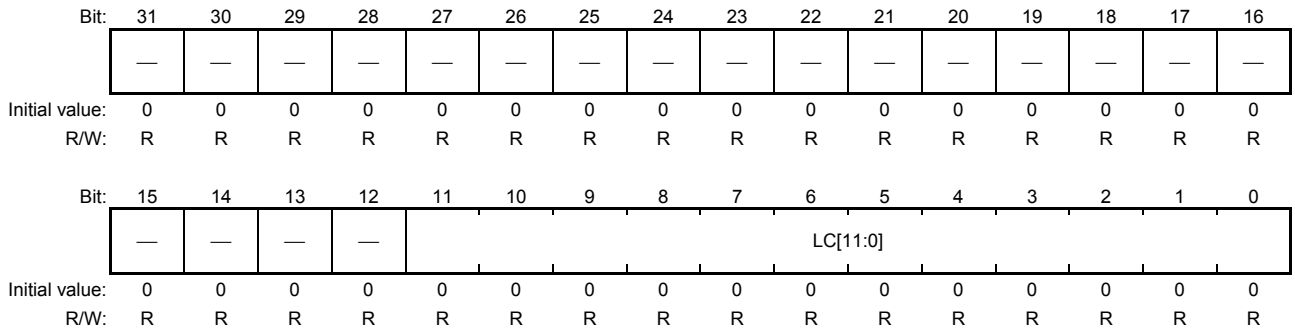
Bit	Bit Name	Initial Value	R/W	Description
31 to 7	MB3[24:0]	H'0000000	R/W	<p>Memory Base Address 3</p> <p>These bits specify the transfer start address in frame buffer 3. Specify a value for physical address bits [31:7] in units of 128 bytes.</p> <p>If the module is in continuous frame capture mode, this value is used as the MB3 address in the following capture sequence: MB1 → MB2 → MB3 → MB1 → MB2 → MB3.</p> <p>Specify a memory address taking into account the image size so that the image data does not exceed an area boundary on the address map.</p>
6 to 0	—	All 0	R	<p>Reserved bits that indicate the lower-order seven bits of memory base address 3 (a multiple of 128 bytes).</p> <p>These bits are always read as 0. The write value should always be 0.</p>



**23.2.16 Video n Line Count Register (VnLC)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Note: Availability of channels:  
 n = 0 to 3 (RZ/G1H), 0 to 2 (RZ/G1M/N), 0 and 1 (RZ/G1E)



Bit	Bit Name	Initial Value	R/W	Description
31 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11 to 0	LC[11:0]	All 0	R	Line Count These bits show the line position in the current capture field.

**23.2.17 Video n Interrupt Enable Register (VnIE)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Note: Availability of channels:

n = 0 to 3 (RZ/G1H), 0 to 2 (RZ/G1M/N), 0 and 1 (RZ/G1E)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	FIE2	—	—	—	—	—	—	—	—	—	—	—	—	—	VFE	VRE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	FIE	CEE	SIE	EFE	FOE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	FIE2	0	R/W	Field Interrupt Enable 2 This bit enables or disables INTC output for field interrupts. Interrupt signals by this enable bit is asserted irrespective of whether capture is taking place. 0: Field interrupts are disabled. 1: Field interrupts are enabled.
30 to 18	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
17	VFE	0	R/W	VSYNC Falling Edge Detect Interrupt Enable This bit enables or disables VSYNC falling edge detect interrupts. Interrupt signals by this enable bit is asserted irrespective of whether capture is taking place. 0: VSYNC falling edge detect interrupts are disabled. 1: VSYNC falling edge detect interrupts are enabled.
16	VRE	0	R/W	VSYNC Rising Edge Detect Interrupt Enable This bit enables or disables VSYNC rising edge detect interrupts. Interrupt signals by this enable bit is asserted irrespective of whether capture is taking place. 0: VSYNC rising edge detect interrupts are disabled. 1: VSYNC rising edge detect interrupts are enabled.
15 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	FIE	0	R/W	Field Interrupt Enable This bit enables or disables field-switching interrupts. This interrupt enable setting is valid when the CA bit in VnMS is 1. 0: Field-switching interrupts are disabled. 1: Field-switching interrupts are enabled.

Bit	Bit Name	Initial Value	R/W	Description
3	CEE	0	R/W	<p>Correction Error Interrupt Enable</p> <p>This bit enables or disables interrupts due to error correction in the timing reference code (SAV/EAV) described in the ITU-R BT.656 specification. This interrupt enable setting is valid when the CA bit in VnMS is 1.</p> <p>0: ITU-R BT.656 timing reference code error interrupts are disabled. 1: ITU-R BT.656 timing reference code error interrupts are enabled.</p>
2	SIE	0	R/W	<p>Scanline Interrupt Enable</p> <p>This bit enables or disables scanline interrupts. This interrupt enable setting is valid when the CA bit in VnMS is 1.</p> <p>0: Scanline interrupts are disabled. 1: Scanline interrupts are enabled.</p>
1	EFE	0	R/W	<p>End of Frame Interrupt Enable</p> <p>This bit enables or disables end of frame interrupts. This interrupt enable setting is valid when the CA bit in VnMS is 1.</p> <p>0: End of frame interrupts are disabled. 1: End of frame interrupts are enabled.</p>
0	FOE	0	R/W	<p>FIFO Overflow Interrupt Enable</p> <p>This bit enables or disables FIFO overflow interrupts. This interrupt enable setting is valid when the CA bit in VnMS is 1.</p> <p>0: FIFO overflow interrupts are disabled. 1: FIFO overflow interrupts are enabled.</p>

### 23.2.18 Video n Interrupt Status Register (VnINTS)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

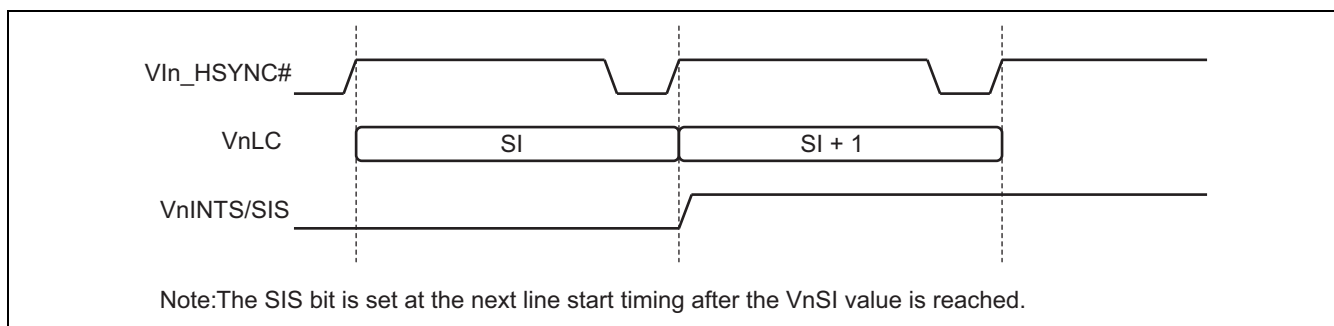
Note: Availability of channels:

n = 0 to 3 (RZ/G1H), 0 to 2 (RZ/G1M/N), 0 and 1 (RZ/G1E)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	FIS2	—	—	—	—	—	—	—	—	—	—	—	—	—	VFS	VRS
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	FIS	CES	SIS	EFS	FOS
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	FIS2	0	R/W	<p>Field Interrupt Status 2</p> <p>This bit shows that the field has changed. This bit is set to 1 when a valid field is detected in the ITU-R BT.601 interface or the F bit defined in ITU-R BT.656 changes. After being set to 1, this bit is cleared to 0 by writing 1.</p> <p>Note: This bit is set to 1 irrespective of whether or not capture is taking place. Be sure to clear this bit to 0 before using it.</p>
30 to 18	—	All 0	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>
17	VFS	0	R/W	<p>VSYNC Falling Edge Detect Interrupt Status</p> <p>This bit shows that a VSYNC falling edge has been detected in the ITU-R BT.601 input. After being set to 1, this bit is cleared to 0 by writing 1.</p> <p>Note: This bit is set to 1 irrespective of whether or not capture is taking place. Be sure to clear this bit to 0 before using it.</p>
16	VRS	0	R/W	<p>VSYNC Rising Edge Detect Interrupt Status</p> <p>This bit shows that a VSYNC rising edge has been detected in the ITU-R BT.601 input. After being set to 1, this bit is cleared to 0 by writing 1.</p> <p>Note: This bit is set to 1 irrespective of whether or not capture is taking place. Be sure to clear this bit to 0 before using it.</p>
15 to 5	—	All 0	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>
4	FIS	0	R/W	<p>Field Interrupt Status</p> <p>This bit shows that a field has been captured in the active capture operation.</p> <p>This bit is set to 1 when a valid field is detected in the ITU-R BT.601 interface or the F bit defined in ITU-R BT.656 changes. After being set to 1, this bit is cleared to 0 by writing 1.</p>

Bit	Bit Name	Initial Value	R/W	Description
3	CES	0	R/W	<p>Correction Error Interrupt Status</p> <p>This bit shows that the timing reference code in the active capture operation has an error involving at least two bits. After being set to 1, this bit is cleared to 0 by writing 1.</p> <p>This bit is set to 1 if the EC bit in VnMC is enabled and the timing reference code has an error involving at least two bits. If a 1-bit error occurs when the EC bit is enabled, this bit is not set to 1.</p>
2	SIS	0	R/W	<p>Scanline Interrupt Status</p> <p>This bit shows that the number of lines specified by VnSI has been reached in the active capture operation. After being set to 1, this bit is cleared to 0 by writing 1.</p> <p>This bit is set to 1 at the next line start timing after the value in the VnLC register matches the VnSI register setting. This timing is shown in Figure 23.2, Scanline Interrupt Status Generation Timing.</p>
1	EFS	0	R/W	<p>End of Frame Interrupt Status</p> <p>This bit shows that the last frame has been reached in the active capture operation. This bit is set to 1 at the end of even field (field 2). After being set to 1, this bit is cleared to 0 by writing 1.</p>
0	FOS	0	R/W	<p>FIFO Overflow Interrupt Status</p> <p>This bit shows that the FIFO has overflowed in the active capture operation. After being set to 1, this bit is cleared to 0 by writing 1.</p> <p>If the FIFO overflows, the FIFO data is overwritten by the pixel data captured after the overflow, and the resultant data is sent to the frame buffer.</p>



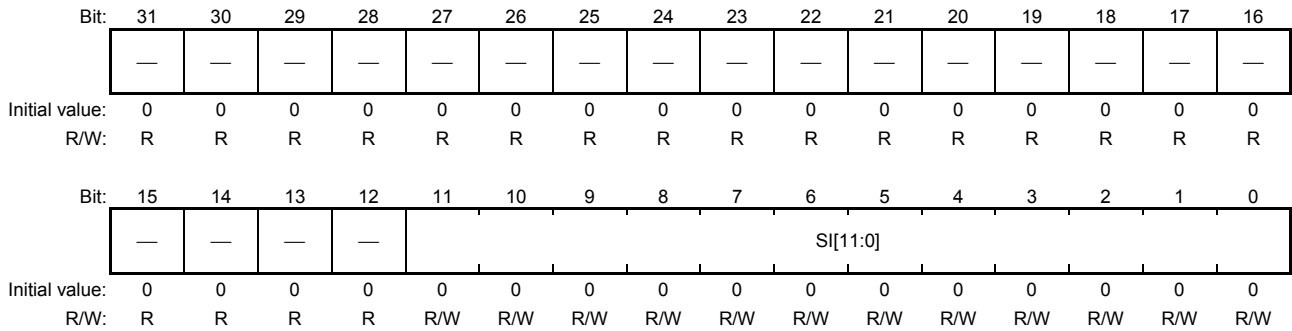
**Figure 23.2 Scanline Interrupt Status Generation Timing**

**23.2.19 Video n Scanline Interrupt Register (VnSI)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Note: Availability of channels:

n = 0 to 3 (RZ/G1H), 0 to 2 (RZ/G1M/N), 0 and 1 (RZ/G1E)



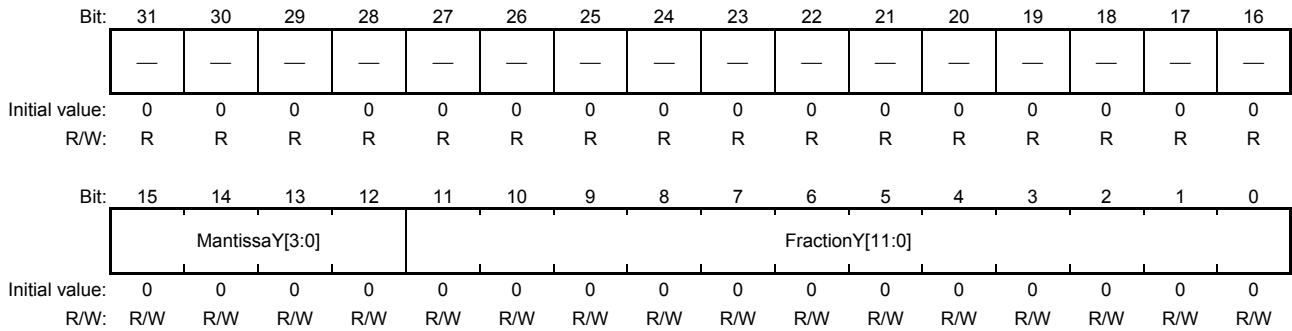
Bit	Bit Name	Initial Value	R/W	Description
31 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11 to 0	SI[11:0]	All 0	R/W	Scanline Interrupt Setting These bits specify a value to be compared with the VnLC register value in each field while the SIE bit in the VnIE register is set to 1. When this value matches the VnLC register value, an interrupt signal is asserted.

**23.2.20 Video n Y Scale Register (VnYS)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Note: Availability of channels:

n = 0 to 3 (RZ/G1H), 0 to 2 (RZ/G1M/N), 0 and 1 (RZ/G1E)



Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 12	MantissaY [3:0]	H'0	R/W	The scaling ratio in the Y direction should be specified through MantissaY and FractionY. This register specifies the value of (number of lines output to memory per field) / (number of capture lines per field) and it is calculated from MantissaY and FractionY by the following equation. $Y \text{ scaling} = 4096 / (4096 \times \text{MantissaY} + \text{FractionY})$ For example, to obtain a Y scaling ratio of 1/2, specify MantissaY = H'2 and FractionY = H'000. Note that the maximum scaling-up ratio is $\times 3$ . When both MantissaY and FractionY are set to 0, the scaling function is disabled. To specify a scaling ratio of $\times 1$ , disabling of the scaling function is recommended.
11 to 0	FractionY [11:0]	H'000	R/W	

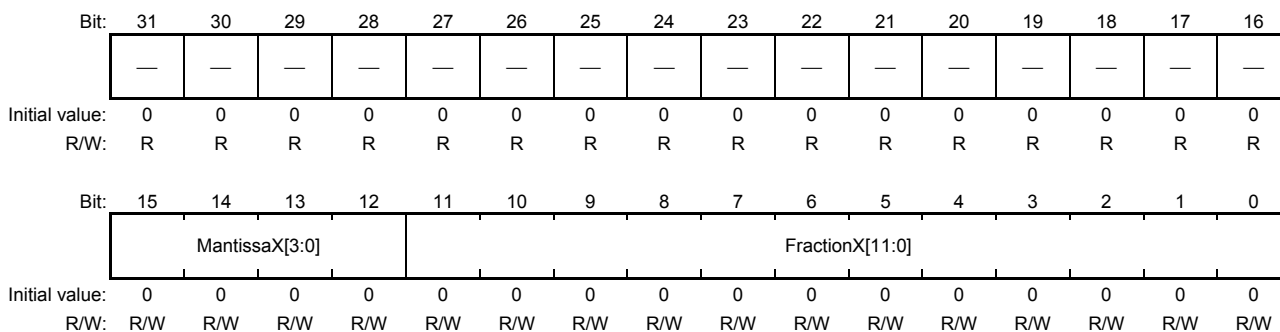
- Notes:
- Do not make the scaling-up setting when the FAST bit in MC is set to enable the applicable function.
  - Disable the scaling function when using the 10/12-bit YCbCr-422 format in the ITU-R BT.601, BT.709, or BT656 interface or the 20/24-bit YCbCr-422 format in the ITU-R BT.1358 interface.
  - The minimum scaling-down ratio is:  
Mantissa[3:0] = H'E, Fraction[11:0] = H'FFF

**23.2.21 Video n X Scale Register (VnXS)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Note: Availability of channels:

n = 0 to 3 (RZ/G1H), 0 to 2 (RZ/G1M/N), 0 and 1 (RZ/G1E)



Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 12	MantissaX [3:0]	H'0	R/W	The scaling ratio in the X direction should be specified through MantissaX and FractionX. This register specifies the value of (number of pixels output to memory per line) / (number of input pixels per line) and it is calculated from MantissaX and FractionX by the following equation. $X \text{ scaling} = 4096 / (4096 \times \text{MantissaX} + \text{FractionX})$ As the multiphase filter specified by the coefficient set CmA (m = 1 to 8) registers are used for scaling, be sure to specify the coefficient set registers for scaling. Note that the maximum scaling-up ratio is $\times 2$ . When both MantissaX and FractionX are set to 0, the scaling function is disabled. To specify a scaling ratio of $\times 1$ , set both the mantissaX and fractionX to 0. Typical examples of this register setting and scaling ratio for 720 input pixels are shown in Table 23.12.
11 to 0	FractionX [11:0]	H'000	R/W	

- Notes: 1. Do not make the scaling-up setting when the FAST bit in MC is set to enable the applicable function.  
2. Disable the scaling function when using the 10/12-bit YCbCr-422 format in the ITU-R BT.601, BT.709, or BT656 interface or the 20/24-bit YCbCr-422 format in the ITU-R BT.1358 interface.

**Table 23.12 Examples of Scaling Setting (Input Pixels: 720 Pixels)**

Output Pixels	Scaling Ratio	Setting
680	0.943	H'10F8
800	1.111	H'0E68
854	1.185	H'0D80



### 23.2.22 Video n Data Mode Register (VnDMR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Notes: Availability of channels:

n = 0 to 3 (RZ/G1H), 0 to 2 (RZ/G1M/N), 0 and 1 (RZ/G1E)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	A8BIT[7:0]														EVA	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	YMODE[2:0]			—	—	—	EXR GB	—	—	—	BP SM	—	ABIT	DTMD[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R	R	R	R/W	R	R	R	R/W	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	A8BIT[7:0]	H'00	R/W	Alpha 8 These bits set the alpha value for the ARGB8888 format output.
23 to 17	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
16	EVA	0	R/W	Even Field Address Offset This bit specifies the address offset of the even field (field 2) in memory in odd-/even-field capture mode. 0: Data are stored from the base address in external memory. 1: Data are stored from the base address plus the memory width in external memory.
15	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
14 to 12	YMODE[2:0]	000	R/W	YC Data Transfer Mode These bits specify the transfer method of Y/CbCr when the data conversion mode (DTMD) is 10 (YC separation). 000: Both Y and CbCr data are transferred to memory 001: Only Y data is transferred to memory as 8-bit data 010: 10-bit Y data is converted to 16-bit data and both Y and CbCr data are transferred to memory. 011: 10-bit Y data is converted to 16-bit data and only Y data is transferred to memory. 100: 12-bit Y data is converted to 16-bit data and both Y and CbCr data are transferred to memory. 101: 12-bit Y data is converted to 16-bit data and only Y data is transferred to memory. 110: Setting prohibited 111: Setting prohibited
11 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
8	EXRGB	0	R/W	Extension RGB Conversion Mode 0: RGB data extension processing is not performed. 1: Data is extended to 32-bit RGB conversion when DTMD[1:0] is set to 00 or 01 as the data conversion mode.
7 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	BPSM	0	R/W	Output Data Byte Swap Mode 0: Bytes are not swapped in output data. 1: Bytes are swapped in output data. Note: When YCbCr-422 data is output in big endian, data is transferred in the YUYV format in most cases. To transfer data in the UYVY format, set this bit to 1.
3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
2	ABIT	0	R/W	Alpha Bit This bit specifies the alpha value for data in ARGB-1555 output mode. 0: The alpha value is set to 0. 1: The alpha value is set to 1.
1, 0	DTMD[1:0]	00	R/W	Data Conversion Mode These bits set the format for storing RGB888 or YCbCr444 data after LUT conversion, in the external memory. *1 00: Data is not converted. 01: RGB is converted to ARGB before output. 10: YC is separated before output. *2 11: Setting prohibited.

Notes: 1. The data conversion modes that can be set are shown in Table 23.12. Do not set any other mode that is not listed in the table. RGB and YCbCr data after LUT conversion should be set as shown in Tables 23.10 and 23.11.

2. Do not set for any other data format except for YCbCr422; set YC separation only for YCbCr data format.

**Table 23.13 Data Conversion Settings**

## • RGB Data Conversion Modes

Format of Data Stored in Memory	VnDMR/ YMODE[2:0]	VnDMR/ EXRGB	VnDMR/ DTMD[1:0]	Remarks
RGB-565 (16 bits/pixel) format	000	0	00	
RGB-888 (32 bits/pixel) format	000	1	00	
ARGB-1555 (16 bits/pixel) format	000	0	01	The alpha bit is set with the ABIT bit in VnDMR.
ARGB-8888 (32 bits/pixel) format	000	1	01	The alpha bit is set with the A8BIT bit in VnDMR.

## • YCbCr Data Conversion Modes

Format of Data Stored in Memory	VnDMR/ YMODE[2:0]	VnDMR/ EXRGB	VnDMR/ DTMD[1:0]	Remarks
YCbCr-422 ( 8 bits) transfer	000	0	00	Set the BPSM bit in VnDMR to 1 to transfer in UYVY format in big endian.
Y (8 bits)/CbCr separation transfer	000	0	10	CbCr transfer destination is determined by the VnUVAOF register setting.
Y (8 bits) transfer	001	0	10	
Y (16 bits)/CbCr separation transfer	010/100	0	10	CbCr transfer destination is determined by the VnUVAOF register setting.
Y (16 bits) transfer	011/101	0	10	

Notes: If any combination of values not listed above is specified, correct operation is not guaranteed.

### 23.2.23 Video n Data Mode Register 2 (VnDMR2)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√*	√*	√*	√*

Note: Availability of channels:

n = 0 to 3 (RZ/G1H), 0 to 2 (RZ/G1M/N), 0 and 1 (RZ/G1E)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	FPS	VPS	HPS	CES	DES	—	—	—	CHS	YDS	—	—	—	—	FT EV	FT EH
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R	R	R	R/W	R/W	R	R	R	R	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VLV[3:0]				HLV[11:0]											
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	FPS	0	R/W	Field Signal Polarity Select This bit specifies the polarity of the input field signal in the ITU-R BT.601 interface. 0: 0/1 = Odd field (field 1)/Even field (field 2) 1: 0/1 = Even field (field 2)/Odd field (field 1)
30	VPS	0	R/W	Vsync Signal Polarity Select This bit specifies the polarity of the input vertical sync signal in the ITU-R BT.601 interface. 0: Active low 1: Active high
29	HPS	0	R/W	Hsync Signal Polarity Select This bit specifies the polarity of the input horizontal sync signal in the ITU-R BT.601 interface. 0: Active low 1: Active high
28	CES	0	R/W	Clock Enable Signal Polarity Select This bit specifies the polarity of the input clock enable signal in the ITU-R BT.601. 0: Active high 1: Active low
27	DES	0	R/W	Data Extension Select This bit is used to select how data are expanded to 12 bits within the VIN module. 0: Empty bits in the input data are repeatedly expanded from the highest-order bit. 1: Empty bits will be padded with zeros. This bit must be set to 1 when the YCbCr-422 interface is in use.
26 to 24	—	000	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
23	CHS	0	R/W	<p>Clock Enable Hsync Select</p> <p>The HSYNC signal (VIn_HSYNC#) input from the pin is internally used as the clock enable signal.</p> <p>0: Clock enable signal (VIn_CLKENB) input from the pin is internally used as the clock enable signal.</p> <p>1: HSYNC signal (VIn_HSYNC#) input from the pin is internally used as the clock enable signal.</p> <p>Note: When using the ITU-R BT.601, BT.709, or BT.1358 interface, the CHS bit must be set to 1 if the VIn_CLKENB pin is not in use.</p>
22	YDS	0	R/W	<p>YCbCr422 8-bit Data Input Pin Select</p> <p>This bit specifies the YCbCr422 8-bit data input pins.</p> <p>0: VIn_B[7:0] pins</p> <p>1: VIn_G[7:0] pins</p> <p>Note: This bit can only be set when the YCbCr-422 interface is in use.</p>
21 to 18	—	All 0	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>
17	FTEV	0	R/W	<p>VSYNC Field Toggle Mode Enable</p> <p>The VSYNC field toggle mode changes the capture field signal level according to the count of input VSYNC signal assertion. As the VIN controls capture operation only when the input field signal level changes, select the VSYNC field toggle mode when capturing progressive images.</p> <p>0: The field toggle function according to the VSYNC count is disabled.</p> <p>1: The field toggle function according to the VSYNC count is enabled. The period before a toggle should be specified in the VLV bits.</p> <p>Note: Do not set both FTEH and FTEV at the same time.</p>
16	FTEH	0	R/W	<p>HSYNC Field Toggle Counter Enable</p> <p>0: The field toggle function according to the capture active line is disabled.</p> <p>1: The field toggle function according to the capture active line is enabled. The period before a toggle should be specified in the HLV bits.</p> <p>Note: Do not set both FTEH and FTEV at the same time.</p>
15 to 12	VLV[3:0]	H'0	R/W	<p>VSYNC Field Toggle Mode Transition Period</p> <p>These bits specify the count of vertical sync signal input before the VSYNC field toggle mode is entered. After a transition to the VSYNC field toggle mode, the capture field signal is toggled every time VSYNC is input.</p> <p>When a change in the input field signal is detected, the toggle mode is canceled.</p> <p>H'0: The field signal is toggled at every VSYNC input.</p> <p>H'1: Toggle mode is entered after VSYNC is input once.</p> <p>H'2: Toggle mode is entered after VSYNC is input two times.</p> <p>H'3: Toggle mode is entered after VSYNC is input three times.</p> <p>:</p> <p>H'E: Toggle mode is entered after VSYNC is input 14 times</p> <p>H'F: Toggle mode is entered after VSYNC is input 15 times.</p> <p>Note: If the field signal changes while the transition period is counted, the counter is initialized.</p>

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Bit	Bit Name	Initial Value	R/W	Description
11 to 0	HLV[11:0]	H'000	R/W	<p>HSYNC Field Toggle Count Value</p> <p>The HSYNC field toggle counter counts the capture active lines. If the external field signal does not change before the prespecified counter value is reached, the capture field signal is toggled.</p> <p>H'000: The field signal is toggled for every valid line.</p> <p>H'001: The field signal is toggled for every single valid line.</p> <p>H'002: The field signal is toggled for every two valid lines.</p> <p>:</p> <p>H'FFF: The field signal is toggled for every 4095 valid lines.</p> <p>Note: For the period before a toggle, specify a value greater than one VSYNC period.</p>

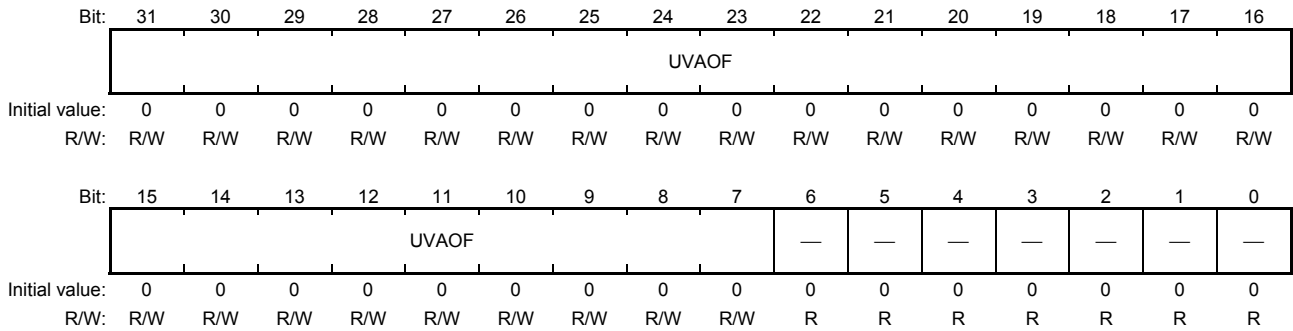
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**23.2.24 Video n UV Address Offset Register (VnUVAOF)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Note: Availability of channels:

n = 0 to 3 (RZ/G1H), 0 to 2 (RZ/G1M/N), 0 and 1 (RZ/G1E)



Bit	Bit Name	Initial Value	R/W	Description
31 to 7	UVAOF[24:0]	All 0	R/W	<p>UV Data Address Offset</p> <p>These bits specify the transfer offset address for the YC separation YCbCr-422 UV data.</p> <p>Specify bits 31 to 7 of the physical address in 128-byte units.</p> <p>Note: The specified address should be equal to or greater than the Y transfer size. Otherwise, the overwriting of Y data occurs.</p>
6 to 0	—	All 0	R	<p>Reserved bits that indicate the 128-byte boundary of the UVAOF value.</p> <p>These bits are always read as 0. The write value should always be 0.</p>

### 23.2.25 YC-RGB Conversion Coefficient Registers

YC→RGB color space conversion is performed with the following formula. Each of the coefficients can be set through the registers. Here, if 8-bit data format is set, the coefficient registers set with the YMUL, CSUB, and YSUB bits in the VnCSCC1 register, RCRMU and GCRMUL bits in the VnCSCC2 register and GCBMUL and BCBMUL bits in the VnCSCC3 register are used to convert the color space. When 10-bit/12-bit data format is set, the YMUL2 bit in the VnCSCE1 register, CSUB2 and YSUB2 bits in the VnCSCE2 register, RCRMUL2 and GCRMUL2 bits in the VnCSCE3 register, GCBMUL2 and BCBMUL2 bits in the VnCSCE4 register are used in color space conversion.

$$\begin{aligned}
 R &= \begin{pmatrix} VnCSCC1/ \\ YMUL[9:0] \\ or \\ VnCSCE1/ \\ YMUL2[13:0] \end{pmatrix} \times (Y - \begin{pmatrix} VnCSCC1/ \\ YSUB[7:0] \\ or \\ VnCSCE1/ \\ YSUB2[11:0] \end{pmatrix}) + \begin{pmatrix} VnCSCC2/ \\ RCRMUL[9:0] \\ or \\ VnCSCE3/ \\ RCRMUL2[13:0] \end{pmatrix} \times (Cr - \begin{pmatrix} VnCSCC1/ \\ CSUB[7:0] \\ or \\ VnCSCE1/ \\ CSUB2[11:0] \end{pmatrix}) \\
 G &= \begin{pmatrix} VnCSCC1/ \\ YMUL[9:0] \\ or \\ VnCSCE1/ \\ YMUL2[13:0] \end{pmatrix} \times (Y - \begin{pmatrix} VnCSCC1/ \\ YSUB[7:0] \\ or \\ VnCSCE1/ \\ YSUB2[11:0] \end{pmatrix}) - \begin{pmatrix} VnCSCC2/ \\ GCRMUL[9:0] \\ or \\ VnCSCE3/ \\ GCRMUL2[13:0] \end{pmatrix} \times (Cr - \begin{pmatrix} VnCSCC1/ \\ CSUB[7:0] \\ or \\ VnCSCE1/ \\ CSUB2[11:0] \end{pmatrix}) - \begin{pmatrix} VnCSCC3/ \\ GCBMUL[9:0] \\ or \\ VnCSCE4/ \\ GCBMUL2[13:0] \end{pmatrix} \times (Cb - \begin{pmatrix} VnCSCC1/ \\ CSUB[7:0] \\ or \\ VnCSCE1/ \\ CSUB2[11:0] \end{pmatrix}) \\
 B &= \begin{pmatrix} VnCSCC1/ \\ YMUL[9:0] \\ or \\ VnCSCE1/ \\ YMUL2[13:0] \end{pmatrix} \times (Y - \begin{pmatrix} VnCSCC1/ \\ YSUB[7:0] \\ or \\ VnCSCE1/ \\ YSUB2[11:0] \end{pmatrix}) + \begin{pmatrix} VnCSCC3/ \\ BCBMUL[9:0] \\ or \\ VnCSCE4/ \\ BCBMUL2[13:0] \end{pmatrix} \times (Cb - \begin{pmatrix} VnCSCC1/ \\ CSUB[7:0] \\ or \\ VnCSCE1/ \\ CSUB2[11:0] \end{pmatrix})
 \end{aligned}$$

Note: Set the coefficients for ITU-R BT.601 (8 bits) as the initial value.

$$R = 1.164 \times (Y - 16) + 1.596 \times (Cr - 128)$$

$$G = 1.164 \times (Y - 16) - 0.813 \times (Cr - 128) - 0.392 \times (Cb - 128)$$

$$B = 1.164 \times (Y - 16) + 2.017 \times (Cb - 128)$$



### 23.2.25.1 Video n Color Space Change Coefficient 1 Register (VnCSCC1)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Note: Availability of channels:

n = 0 to 2 (RZ/G1H and M/N), 0 and 1 (RZ/G1E)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	YMUL[9:0]									
Initial value:	0	0	0	0	0	0	0	1	0	0	1	0	1	0	0	1
R/W:	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	YSUB[7:0]								CSUB[7:0]							
Initial value:	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

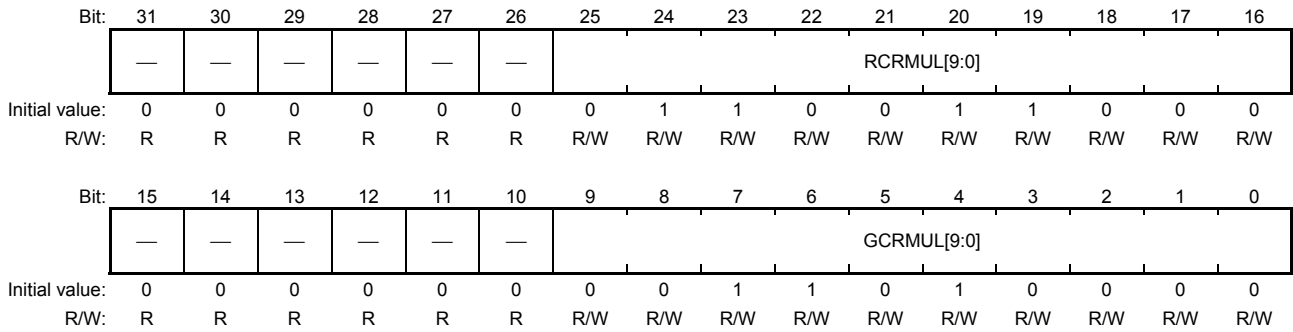
Bit	Bit Name	Initial Value	R/W	Description
31 to 26	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
25 to 16	YMUL[9:0]	H'129	R/W	Y Data Multiplication Coefficient These bits specify the multiplication coefficient for Y data in YCbCr-444→RGB-888 color space conversion. (Initial value: 1.164) Specify an unsigned 10-bit integer obtained by multiplying the desired coefficient value by 256.
15 to 8	YSUB[7:0]	H'10	R/W	Y Data Subtraction Coefficient These bits specify the subtraction coefficient for Y data in YCbCr-444→RGB-888 color space conversion. (Initial value: H'16) Specify an unsigned 8-bit integer.
7 to 0	CSUB[7:0]	H'80	R/W	CbCr Data Subtraction Coefficient These bits specify the subtraction coefficient for Cb and Cr data in YCbCr-444→RGB-888 color space conversion. (Initial value: H'128) Specify an unsigned 8-bit integer.

**23.2.25.2 Video n Color Space Change Coefficient 2 Register (VnCSCC2)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Note: Availability of channels:

n = 0 to 2 (RZ/G1H and M/N), 0 and 1 (RZ/G1E)



Bit	Bit Name	Initial Value	R/W	Description
31 to 26	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
25 to 16	RCRMUL [9:0]	H'198	R/W	Cr Multiplication Coefficient for R Data Calculation These bits specify the Cr multiplication coefficient for the R data calculation equation in YCbCr-444→RGB-888 color space conversion. (Initial value: 1.596) Specify an unsigned 10-bit integer obtained by multiplying the desired coefficient value by 256.
15 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9 to 0	GCRMUL [9:0]	H'0D0	R/W	Cr Multiplication Coefficient for G Data Calculation These bits specify the Cr multiplication coefficient for the G data calculation equation in YCbCr-444→RGB-888 color space conversion. (Initial value: 0.813) Specify an unsigned 10-bit integer obtained by multiplying the desired coefficient value by 256.

### 23.2.25.3 Video n Color Space Change Coefficient 3 Register (VnCSCC3)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Note: Availability of channels:

n = 0 to 2 (RZ/G1H and M/N), 0 and 1 (RZ/G1E)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
	—	—	—	—	—	—	GCBMUL[9:0]											
Initial value:	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0		
R/W:	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
	—	—	—	—	—	—	BCBMUL[9:0]											
Initial value:	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0		
R/W:	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		

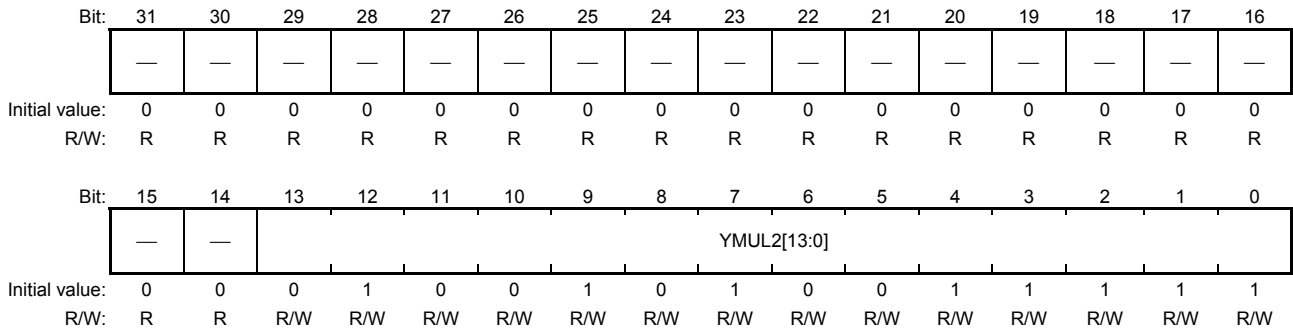
Bit	Bit Name	Initial Value	R/W	Description
31 to 26	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
25 to 16	GCBMUL [9:0]	H'064	R/W	Cb Multiplication Coefficient for G Data Calculation These bits specify the Cb multiplication coefficient for the G data calculation equation in YCbCr-444→RGB-888 color space conversion. (Initial value: 0.392) Specify an unsigned 10-bit integer obtained by multiplying the desired coefficient value by 256.
15 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9 to 0	BCBMUL [9:0]	H'204	R/W	Cb Multiplication Coefficient for B Data Calculation These bits specify the Cb multiplication coefficient for the B data calculation equation in YCbCr-444→RGB-888 color space conversion. (Initial value: 2.017) Specify an unsigned 10-bit integer obtained by multiplying the desired coefficient value by 256.

**23.2.25.4 Video n YC → RGB Calculation Setting Extension Register 1 (VnCSCE1)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Note: Availability of channels:

n = 0 and 1 (RZ/G1H and M/N), 0 and 1 (RZ/G1E)



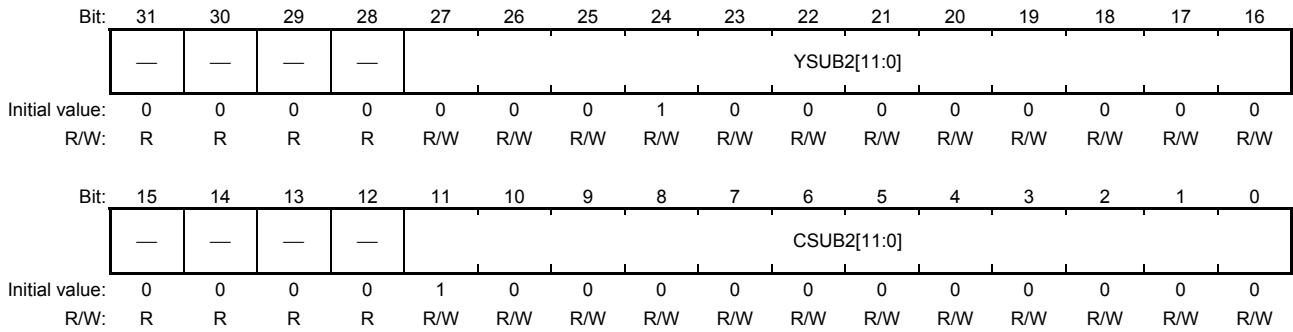
Bit	Bit Name	Initial Value	R/W	Description
31 to 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13 to 0	YMUL2[13:0]	H'129F	R/W	Y Multiplication Coefficient 2 for RGB Calculation These bits specify the multiplication coefficient for Y data in YCbCr-444→RGB-101010/RGB121212 color space conversion. (Initial value: 1.164) Specify an unsigned 12-bit integer obtained by multiplying the desired coefficient value by 4096.

**23.2.25.5 Video n YC → RGB Calculation Setting Extension Register 2 (VnCSCE2)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Note: Availability of channels:

n = 0 and 1 (RZ/G1H and M/N), 0 and 1 (RZ/G1E)



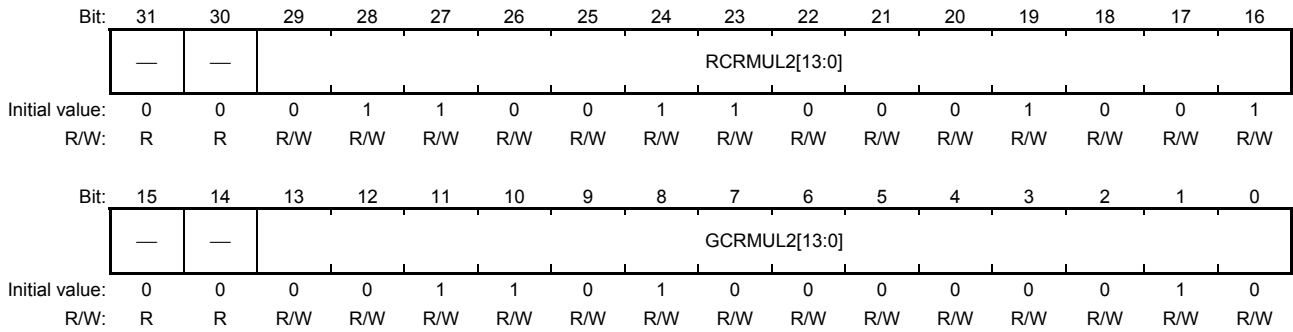
Bit	Bit Name	Initial Value	R/W	Description
31 to 28	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
27 to 16	YSUB[11:0]	H'100	R/W	Y Subtraction Coefficient 2 for RGB Calculation These bits specify the subtraction coefficient for Y data in YCbCr-444→RGB-101010/RGB121212 color space conversion. (Initial value: 256) Specify an unsigned 12-bit integer.
15 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11 to 0	CSUB[11:0]	H'800	R/W	CbCr Subtraction Coefficient 2 for RGB Calculation These bits specify the subtraction coefficient for Cb and Cr data in YCbCr-444→RGB-101010/RGB121212 color space conversion. (Initial value: 2048) Specify an unsigned 12-bit integer.

**23.2.25.6 Video n YC → RGB Calculation Setting Extension Register 3 (VnCSCE3)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Note: Availability of channels:

n = 0 and 1 (RZ/G1H and M/N), 0 and 1 (RZ/G1E)



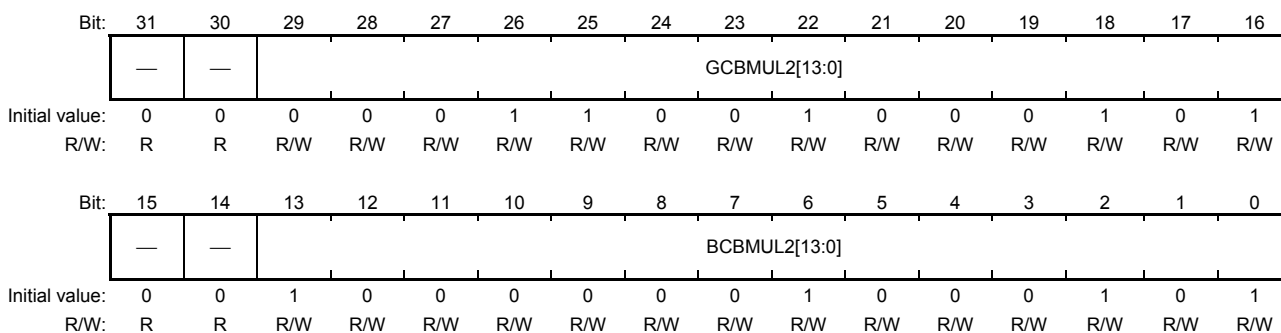
Bit	Bit Name	Initial Value	R/W	Description
31, 30	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
29 to 16	RCRMUL2[13:0]	H'1989	R/W	Cr Multiplication Coefficient 2 for R Calculation These bits specify the Cr multiplication coefficient for the R data calculation equation in YCbCr-444→RGB-101010/RGB121212 color space conversion. (Initial value: 1.596) Specify an unsigned 14-bit integer obtained by multiplying the desired coefficient value by 4096.
15, 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13 to 0	GCRMUL2[13:0]	H'0D02	R/W	Cr Multiplication Coefficient 2 for G Calculation These bits specify the Cr multiplication coefficient for the G data calculation equation in YCbCr-444→RGB-101010/RGB121212 color space conversion. (Initial value: 0.813) Specify an unsigned 14-bit integer obtained by multiplying the desired coefficient value by 4096.

**23.2.25.7 Video n YC → RGB Calculation Setting Extension Register 4 (VnCSCE4)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Note: Availability of channels:

n = 0 and 1 (RZ/G1H and M/N), 0 and 1 (RZ/G1E)



Bit	Bit Name	Initial Value	R/W	Description
31, 30	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
29 to 16	GCBMUL2[13:0]	H'0645	R/W	Cb Multiplication Coefficient 2 for G Calculation These bits specify the Cb multiplication coefficient for the G data calculation equation in YCbCr-444→RGB-101010/RGB121212 color space conversion. (Initial value: 0.392) Specify an unsigned 14-bit integer obtained by multiplying the desired coefficient value by 4096.
15, 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13 to 0	BCBMUL2[13:0]	H'2045	R/W	Cb Multiplication Coefficient 2 for B Calculation These bits specify the Cb multiplication coefficient for the B data calculation equation in YCbCr-444→RGB-101010/RGB121212 color space conversion. (Initial value: 2.017) Specify an unsigned 14-bit integer obtained by multiplying the desired coefficient value by 4096.

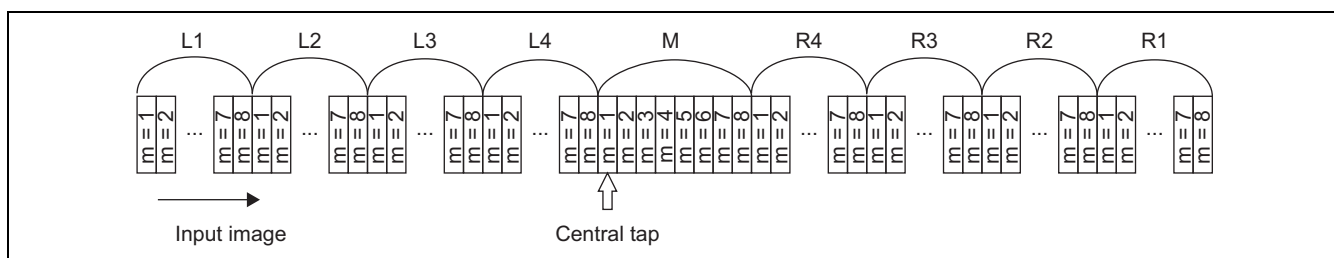
### 23.2.26 Video n Coefficient Set Registers

The coefficient set registers specify the coefficients used for calculation of X scaling specified in XS. The X scaling function processes input pixels with 8-step resolution and generates scaled pixels by using nine calculation coefficients (nine taps) around the determined pixel.

The following is an overview of nine tap coefficients. The MSB of each coefficient is a sign bit.

**Table 23.14 Bit Count for Tap Coefficients**

Register Name (m = 1 to 8)	CmA			CmC			CmB		
Nine tap coefficients	L1	L2	L3	L4	M	R4	R3	R2	R1
Bit width	10	10	10	10	10	10	10	10	10



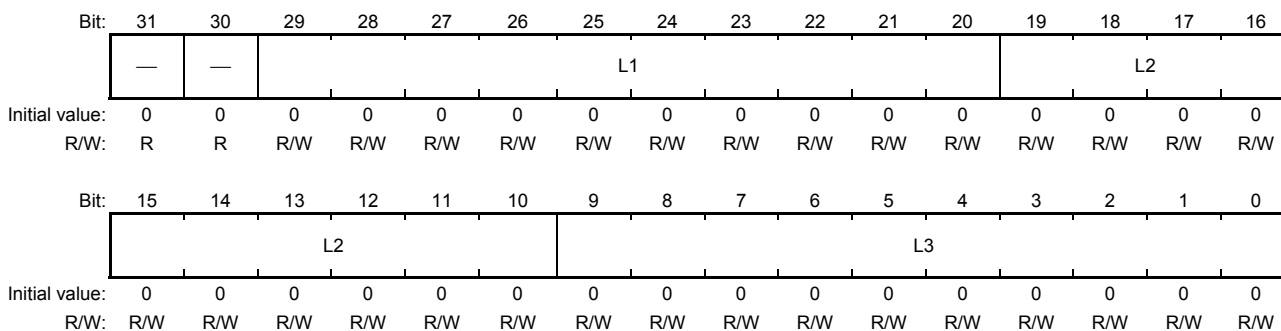
**Figure 23.3 Bit Count for Tap Coefficients**

#### 23.2.26.1 Video n Coefficient Set CmA Register (VnCmA) (m = 1 to 8)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Note: Availability of channels:

n = 0 to 3 (RZ/G1H), 0 to 2 (RZ/G1M/N), 0 and 1 (RZ/G1E)



Bit	Bit Name	Initial Value	R/W	Description
31, 30	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
29 to 20	L1[9:0]	H'000	R/W	L1 coefficient
19 to 10	L2[9:0]	H'000	R/W	L2 coefficient
9 to 0	L3[9:0]	H'000	R/W	L3 coefficient

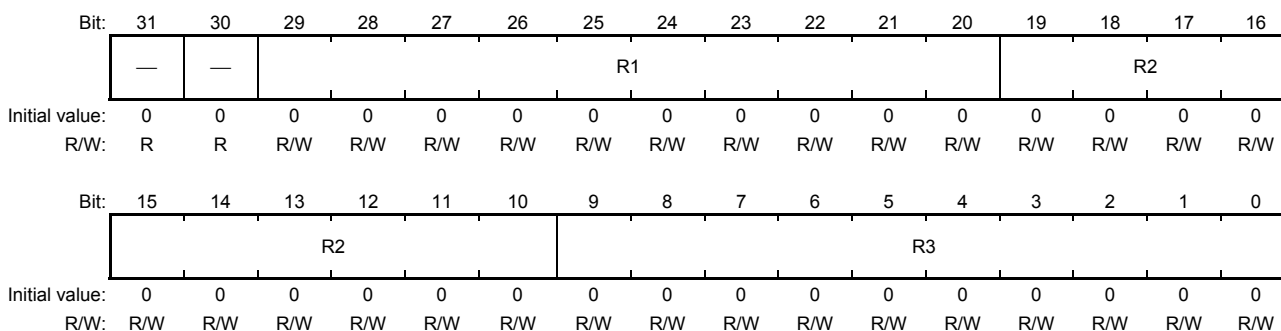


**23.2.26.2 Video n Coefficient Set CmB Register (VnCmB) (m = 1 to 8)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Note: Availability of channels:

n = 0 to 3 (RZ/G1H), 0 to 2 (RZ/G1M/N), 0 and 1 (RZ/G1E)



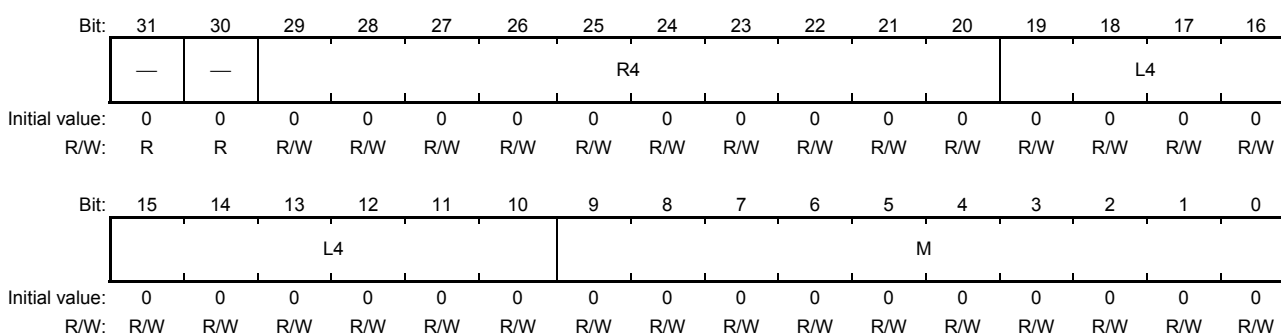
Bit	Bit Name	Initial Value	R/W	Description
31, 30	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
29 to 20	R1[9:0]	H'000	R/W	R1 coefficient
19 to 10	R2[9:0]	H'000	R/W	R2 coefficient
9 to 0	R3[9:0]	H'000	R/W	R3 coefficient

**23.2.26.3 Video n Coefficient Set CmC Register (VnCmC) (m = 1 to 8)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Note: Availability of channels:

n = 0 to 3 (RZ/G1H), 0 to 2 (RZ/G1M/N), 0 and 1 (RZ/G1E)

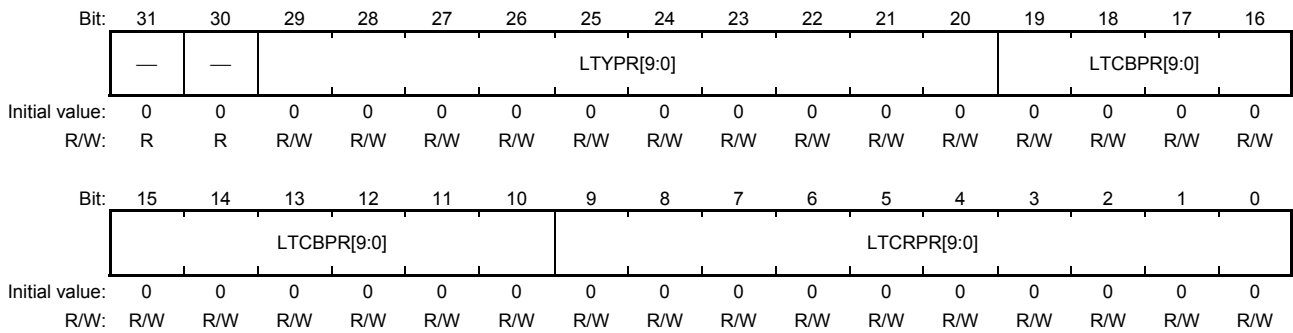


Bit	Bit Name	Initial Value	R/W	Description
31, 30	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
29 to 20	R4[9:0]	H'000	R/W	R4 coefficient
19 to 10	L4[9:0]	H'000	R/W	L4 coefficient
9 to 0	M[9:0]	H'000	R/W	M coefficient

**23.2.27 Video n Lookup Table Pointer (VnLUTP)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Note: Availability of channels:  
 n = 0 to 2 (RZ/G1H), 0 and 1 (RZ/G1M/N), 0 and 1 (RZ/G1E)



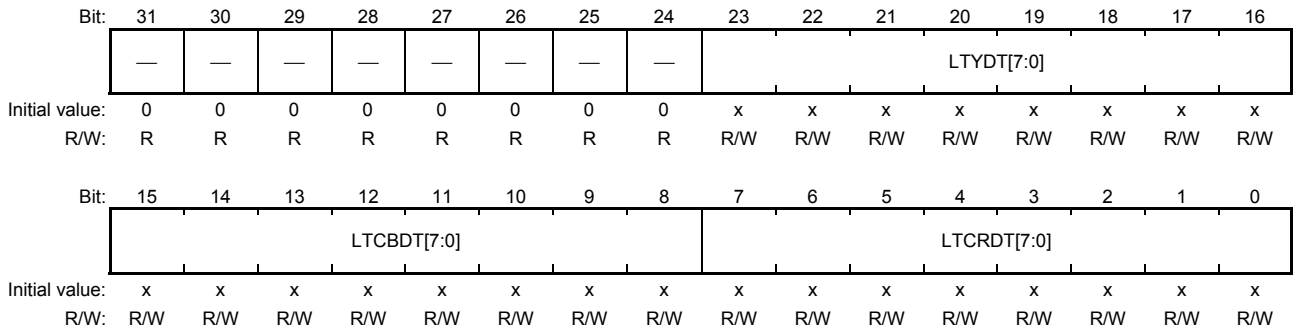
Bit	Bit Name	Initial Value	R/W	Description
31, 30	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
29 to 20	LTYPR[9:0]	All 0	R/W	Lookup Table Y Pointer These bits set the LUT pointer to Y and R data after color space conversion.
19 to 10	LTCBPR[9:0]	All 0	R/W	Lookup Table Cb Pointer These bits set the LUT pointer to Cb and G data after color space conversion.
9 to 0	LTCRPR[9:0]	All 0	R/W	Lookup Table Cr Pointer These bits set the LUT pointer to Cr and G data after color space conversion.

Note: Set the LUT pointer to the upper 10 bits of the 12-bit data for the color space conversion result.  
 The access pointer to the LUT will be automatically incremented by writing to the VnLUTD register.  
 There will be no automatic increment at read access.

**23.2.28 Video n Lookup Table Data Register (VnLUTD)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Note: Availability of channels:  
 n = 0 to 2 (RZ/G1H), 0 and 1 (RZ/G1M/N), 0 and 1 (RZ/G1E)



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 16	LTYDT[7:0]	H'x	R/W	Lookup Table Y Data These bits set the LUT conversion data for Y and R data after color space conversion.
15 to 8	LTCBDT[7:0]	H'x	R/W	Lookup Table Cb Data These bits set the LUT conversion data for Cb and G data after color space conversion.
7 to 0	LTCRDT[7:0]	H'x	R/W	Lookup Table Cr Data These bits set the LUT conversion data for Cr and B data after color space conversion.

Note: The 8-bit data after LUT conversion is subjected to upper shift to carry out capture control as 12-bit data.  
 As for reading from the VnLUTD register, the data read the second time, including dummy read, after the VnLUTP register has been set is valid.

### 23.2.29 RGB-YC Conversion Coefficient Registers

Color space conversion from RGB to YC is done with the following formula. Each of the coefficients can be set with the registers.

$$\begin{aligned}
 Y &= YCLRP \times R + YCLGP \times G + YCLBP \times B + YCLAP \\
 Cb &= CBCLRP \times R + CBCLGP \times G + CBCLBP \times B + CBCLAP \\
 Cr &= YCLRP \times R + YCLGP \times G + YCLBP \times B + YCLAP
 \end{aligned}$$

Note: Set the coefficients for ITU-R BT.601 (8 bits) as the initial value.

$$\begin{aligned}
 Y &= 0.257 \times R + 0.504 \times G + 0.098 \times B + 16 \\
 Cb &= -0.148 \times R - 0.291 \times G + 0.439 \times B + 128 \\
 Cr &= 0.439 \times R - 0.368 \times G - 0.071 \times B + 128
 \end{aligned}$$

#### 23.2.29.1 Video n RGB → YC Calculation Setting Register 1 (VnYCCR1)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Note: Availability of channels:

n = 0 to 2 (RZ/G1H), 0 and 1 (RZ/G1M/N), 0 only (RZ/G1E)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	YCLRP[12:0]												
Initial value:	0	0	0	0	0	0	0	1	0	0	0	0	0	1	1	1
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

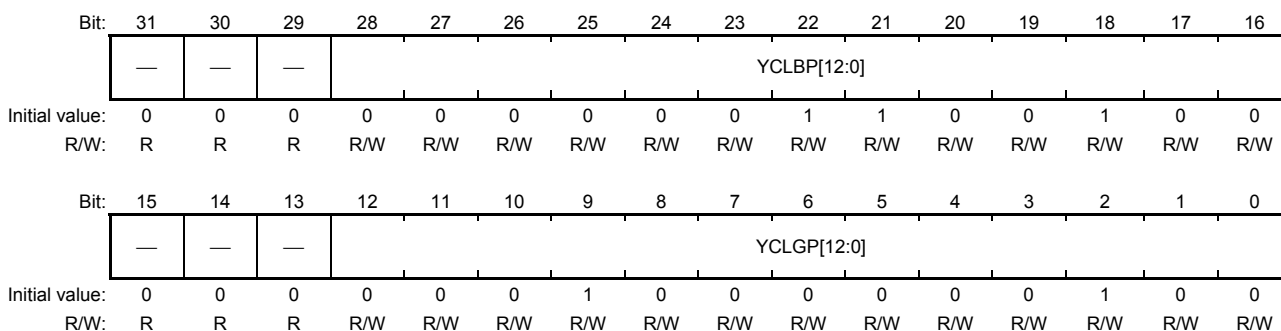
Bit	Bit Name	Initial Value	R/W	Description
31 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12 to 0	YCLRP[12:0]	H'0107	R/W	R Multiplication Coefficient for Y Calculation These bits specify the R multiplication coefficient for the Y data calculation equation in RGB-888→YCbCr-444 color space conversion. (Initial value: 263) The MSB is a sign bit.

**23.2.29.2 Video n RGB → YC Calculation Setting Register 2 (VnYCCR2)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Note: Availability of channels:

n = 0 to 2 (RZ/G1H), 0 and 1 (RZ/G1M/N), 0 only (RZ/G1E)



Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28 to 16	YCLBP[12:0]	H'0064	R/W	B Multiplication Coefficient for Y Calculation These bits specify the B multiplication coefficient for the Y data calculation equation in RGB-888→YCbCr-444 color space conversion. (Initial value: 100) The MSB is a sign bit.
15 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12 to 0	YCLGP[12:0]	H'0204	R/W	G Multiplication Coefficient for Y Calculation These bits specify the G multiplication coefficient for the Y data calculation equation in RGB-888→YCbCr-444 color space conversion. (Initial value: 516) The MSB is a sign bit.

**23.2.29.3 Video n RGB → YC Calculation Setting Register 3 (VnYCCR3)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Note: Availability of channels:

n = 0 to 2 (RZ/G1H), 0 and 1 (RZ/G1M/N), 0 only (RZ/G1E)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	YEXPEN	—	—	YCLSFT[4:0]				YCLHEN	—	—	—	—	—	—	—	YCLCEN
Initial value:	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—				YCLAP[11:0]											
Initial value:	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

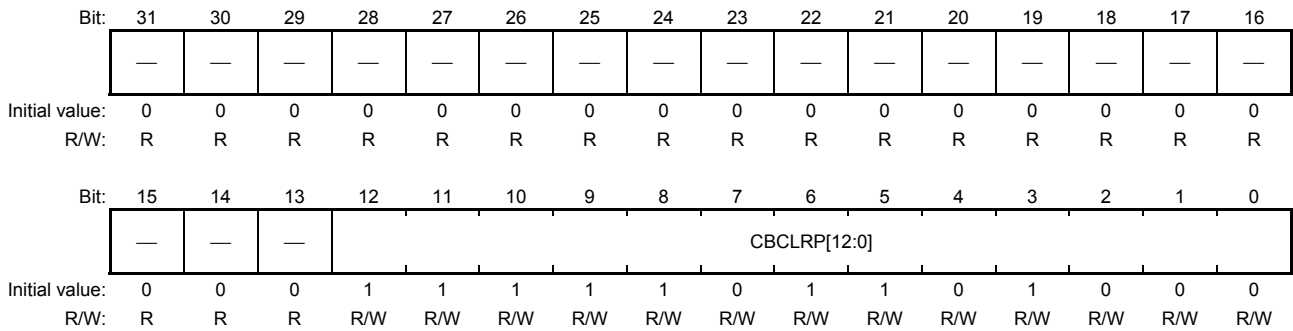
Bit	Bit Name	Initial Value	R/W	Description
31	YEXPEN	0	R/W	Y Calculation Sign Extension Enable This bit controls the sign extension for Y data calculation in RGB888→YCbCr444 color space conversion. 0: Disables YC conversion sign bit. 1: Enables YC conversion sign bit.
30, 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28 to 24	YCLSFT[4:0]	H'0A	R/W	Y Calculation Shift Down Volume These bits set the amount of down shift for Y calculation in RGB888→YCbCr444 color space conversion (Initial value: 10) Unit: Bit shift count
23	YCLHEN	0	R/W	Y Calculation Shift Down Result Round-Off Enable This bit enables round-off process for Y data calculation in RGB888→YCbCr444 color space conversion 0: Round down to down shift process 1: Round-off to down shift process is enabled.
22 to 17	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
16	YCLCEN	0	R/W	Y Calculation Data Clip Enable This bit enables data clipping process for Y data calculation in RGB888→YCbCr444 color space conversion. 0: Data clipping process is disabled. 1: Data clipping process is enabled.
15 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11 to 0	YCLAP[11:0]	H'010	R/W	Y Calculation Data Normalized Additional Value These bits set the Y data addition constant for RGB888→YCbCr444 color space conversion. (Initial value: 16)

**23.2.29.4 Video n RGB → Cb Calculation Setting Register 1 (VnCBCCR1)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Note: Availability of channels:

n = 0 to 2 (RZ/G1H), 0 and 1 (RZ/G1M/N), 0 only (RZ/G1E)



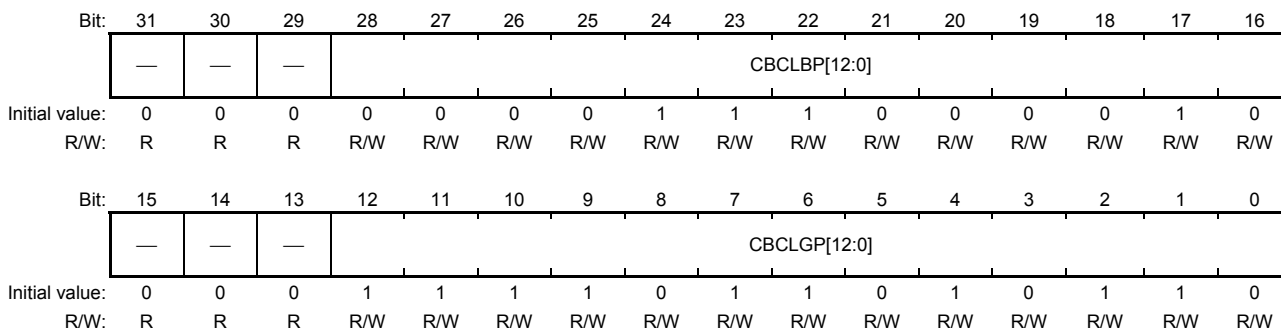
Bit	Bit Name	Initial Value	R/W	Description
31 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12 to 0	CBCLRP[12:0]	H'1F68	R/W	R Multiplication Coefficient for Cb Calculation These bits specify the R multiplication coefficient for the Cb data calculation equation in RGB-888→YCbCr-444 color space conversion. (Initial value: -152) The MSB is a sign bit.

**23.2.29.5 Video n RGB → Cb Calculation Setting Register 2 (VnCBCCR2)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Note: Availability of channels:

n = 0 to 2 (RZ/G1H), 0 and 1 (RZ/G1M/N), 0 only (RZ/G1E)



Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28 to 16	CBCLBP[12:0]	H'01C2	R/W	B Multiplication Coefficient for Cb Calculation These bits specify the B multiplication coefficient for the Cb data calculation equation in RGB-888→YCbCr-444 color space conversion. (Initial value: 450) The MSB is a sign bit.
15 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12 to 0	CBCLGP[12:0]	H'1ED6	R/W	G Multiplication Coefficient for Cb Calculation These bits specify the B multiplication coefficient for the Cb data calculation equation in RGB-888→YCbCr-444 color space conversion. (Initial value: -298) The MSB is a sign bit.



**23.2.29.6 Video n RGB → Cb Calculation Setting Register 3 (VnCBCCR3)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Note: Availability of channels:

n = 0 to 2 (RZ/G1H), 0 and 1 (RZ/G1M/N), 0 only (RZ/G1E)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CBEXP EN	—	—	CBCLSFT[4:0]				CBCLH EN	—	—	—	—	—	—	—	CBCLC EN
Initial value:	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	CBCLAP[11:0]											
Initial value:	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

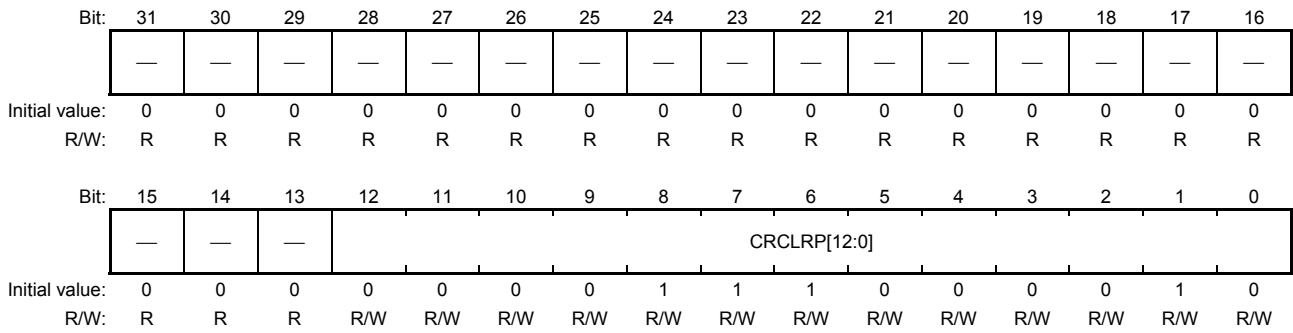
Bit	Bit Name	Initial Value	R/W	Description
31	CBEXPEN	0	R/W	Cb Calculation Sign Extension Enable This bit controls the sign extension for Cb data calculation in RGB888→YCbCr444 color space conversion. 0: Disables YC conversion sign bit. 1: Enables YC conversion sign bit.
30, 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28 to 24	CBCLSFT[4:0]	H'0A	R/W	Cb Calculation Shift Down Volume These bits set the amount of down shift for Cb calculation in RGB888→YCbCr444 color space conversion (Initial value: 10) Unit: Bit shift count
23	CBCLHEN	0	R/W	Cb Calculation Shift Down Result Round-Off Enable This bit enables round-off process for Cb data calculation in RGB888→YCbCr444 color space conversion 0: Round down to down shift process 1: Round-off to down shift process is enabled.
22 to 17	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
16	CBCLCEN	0	R/W	Cb Calculation Data Clip Enable This bit enables data clipping process for Cb data calculation in RGB888→YCbCr444 color space conversion. 0: Data clipping process is disabled. 1: Data clipping process is enabled.
15 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11 to 0	CBCLAP[11:0]	H'080	R/W	Cb Calculation Data Normalized Additional Value These bits set the Cb data addition constant for RGB888→YCbCr444 color space conversion. (Initial value: 128)

**23.2.29.7 Video n RGB → Cr Calculation Setting Register 1 (VnCRCCR1)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Note: Availability of channels:

n = 0 to 2 (RZ/G1H), 0 and 1 (RZ/G1M/N), 0 only (RZ/G1E)



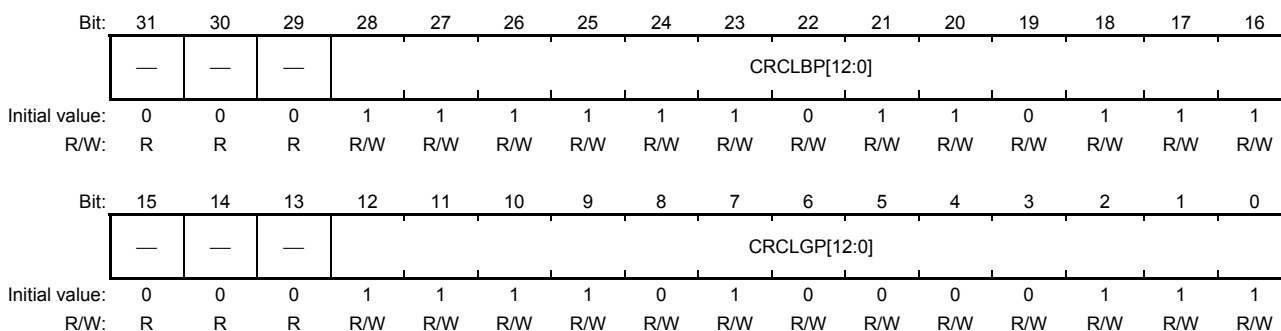
Bit	Bit Name	Initial Value	R/W	Description
31 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12 to 0	CRCLRP[12:0]	H'01C2	R/W	R Multiplication Coefficient for Cr Calculation These bits specify the R multiplication coefficient for the Cr data calculation equation in RGB-888→YCbCr-444 color space conversion. (Initial value: 450) The MSB is a sign bit.

**23.2.29.8 Video n RGB → Cr Calculation Setting Register 2 (VnCRCCR2)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Note: Availability of channels:

n = 0 to 2 (RZ/G1H), 0 and 1 (RZ/G1M/N), 0 only (RZ/G1E)



Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28 to 16	CRCLBP[12:0]	H'1FB7	R/W	B Multiplication Coefficient for Cr Calculation These bits specify the B multiplication coefficient for the Cr data calculation equation in RGB-888→YCbCr-444 color space conversion. (Initial value: -73) The MSB is a sign bit.
15 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12 to 0	CRCLGP[12:0]	H'1E87	R/W	G Multiplication Coefficient for Cr Calculation These bits specify the G multiplication coefficient for the Cr data calculation equation in RGB-888→YCbCr-444 color space conversion. (Initial value: -377) The MSB is a sign bit.

**23.2.29.9 Video n RGB → Cr Calculation Setting Register 3 (VnCRCCR3)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Note: Availability of channels:

n = 0 to 2 (RZ/G1H), 0 and 1 (RZ/G1M/N), 0 only (RZ/G1E)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CREXP EN	—	—	CRCLSFT[4:0]				CRCLH EN	—	—	—	—	—	—	—	CRCLC EN
Initial value:	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	CRCLAP[11:0]											
Initial value:	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	CREXPEN	0	R/W	Cr Calculation Sign Extension Enable This bit controls the sign extension for Cr data calculation in RGB888→YCbCr444 color space conversion. 0: Disables YC conversion sign bit. 1: Enables YC conversion sign bit.
30, 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28 to 24	CRCLSFT[4:0]	H'0A	R/W	Cr Calculation Shift Down Volume These bits set the amount of down shift for Cr calculation in RGB888→YCbCr444 color space conversion (Initial value: 10) Unit: Bit shift count
23	CRCLHEN	0	R/W	Cr Calculation Shift Down Result Round-Off Enable This bit enables round-off process for Cr data calculation in RGB888→YCbCr444 color space conversion 0: Round down to down shift process 1: Round-off to down shift process is enabled.
22 to 17	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
16	CRCLCEN	0	R/W	Cr Calculation Data Clip Enable This bit enables data clipping process for Cr data calculation in RGB888→YCbCr444 color space conversion. 0: Data clipping process is disabled. 1: Data clipping process is enabled.
15 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11 to 0	CRCLAP[11:0]	H'080	R/W	Cr Calculation Data Normalized Additional Value These bits set the Cr data addition constant for RGB888→YCbCr444 color space conversion. (Initial value: 128)

### 23.2.30 Video n Memory Transfer Control Register (VnMTC)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Note: Availability of channels:

n = 0 to 3 (RZ/G1H), 0 and 2 (RZ/G1M/N), 0 and 1 (RZ/G1E)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	PRIH[3:0]				—	—	—	—	PRIL[3:0]			
Initial value:	x	x	x	x	1	0	1	0	x	x	x	x	1	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R	R	R	R	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	SIZE	—	—	—	—	BSIZE[3:0]			
Initial value:	x	x	x	x	x	x	x	1	x	x	x	x	1	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 28	—	-	R	Reserved These bits are undefined. The write value should always be 0.
27 to 24	PRIH[3:0]	H'A	R/W	Priority High Level Value Setting. These bits specify priority high level for second packet from VIN I/F. Please do not change value from H'A.
23 to 20	—	-	R	Reserved These bits are undefined. The write value should always be 0.
19 to 16	PRIL[3:0]	H'8	R/W	Priority Low Level Value Setting. These bits specify priority low level for first packet from VIN I/F. H'8:normal priority. H'9:high priority than other VIN channel. Set these bits to H'9 on high bit rate channel when a system input video data more than two channel.
15 to 9	—	-	R	Reserved These bits are undefined. The write value should always be 0.
8	SIZE	H'1	R/W	Transaction Size Unit setting. 0: 16Byte unit 1: 32Byte unit (default) These bits set the LUT conversion data for Cr and B data after color space conversion.
7 to 4	—	-	R	Reserved These bits are undefined. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
3 to 0	BSIZE[3:0]	H'8	R/W	<p>Burst Size Setting</p> <p>These bits specify VIN's burst transaction size.</p> <p>When bit SIZE is set to 1'b0:</p> <p>H'0: No transfer (prohibited)</p> <p>H'1: 16Byte</p> <p>H'2: 32Byte</p> <p>...</p> <p>H'F: 240Byte</p> <p>When bit SIZE is set to 1'b1:</p> <p>H'0: No transfer (prohibited)</p> <p>H'1: 32Byte</p> <p>H'2: 64Byte (recommended setting)</p> <p>...</p> <p>H'8: 256Byte (default)</p> <p>...</p> <p>H'F: 480Byte (prohibited)</p> <p>Set these bits to specify burst size less than 256Byte.</p> <p>SIZE=1'b1, BSIZE[3:0]=H'2 is recommended setting to consider VIN capture stability.</p>

## 23.3 Operation

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

### 23.3.1 Input Interface

The VIN captures video data in the ITU-R BT.601, ITU-R BT.656, ITU-R BT.1358, or ITU-R BT.709 interface and stores it in external memory. The module has four input-interface channels. The interface and data format can be set as desired for each video channel.

The following tables show the interface and data format supported in each product and its channels.

Note: When the ITU-R BT.709 interface is in use, the maximum frequency of the video clock is 74.5 MHz.

**Table 23.15 Video Channels and Supported Interfaces (RZ/G1H)**

				Channel 0	Channel 1	Channel 2	Channel 3
Input interface	ITU-R BT.656	YCbCr-422	8 bits	Supported	Supported	Supported	Supported
			10 bits	Supported	Supported	—	—
			12 bits	Supported	Supported	—	—
		YCbCr-422 (double edge)	4 bits	Supported	Supported	Supported	—
			8 bits	Supported	Supported	Supported	—
			16 bits	Supported	Supported	Supported	—
	ITU-R BT.1358	YCbCr-422	20 bits	Supported	Supported	—	—
			24 bits	Supported	Supported	—	—
			8 bits	Supported	Supported	Supported	Supported
	ITU-R BT.601/	YCbCr-422	10 bits	Supported	Supported	—	—
	ITU-R BT.709		8 bits	Supported	Supported	—	—

				Channel 0	Channel 1	Channel 2	Channel 3
			12 bits	Supported	Supported	—	—
		YCbCr-422 (double edge)	4 bits	Supported	Supported	Supported	—
			8 bits	Supported	Supported	Supported	—
		RGB-666	18 bits	Supported	Supported	Supported	—
		RGB-888	12 bits	Supported	Supported	—	—
			24 bits	Supported	Supported	Supported	—
Output interface	RGB output	RGB-565	16 bits	Supported	Supported	Supported	Supported
		ARGB-1555	16 bits	Supported	Supported	Supported	Supported
		RGB-888	32 bits	Supported	Supported	Supported	Supported
		ARGB-8888	32 bits	Supported	Supported	Supported	Supported
	YCbCr output	YCbCr-422 multiplexed	8 bits	Supported	Supported	Supported	Supported
		YCbCr-422 separated Y/CbCr	Y: 8 bits CbCr: 8 bits	Supported	Supported	Supported	Supported
			Y: 10 bits CbCr: 8 bits	Supported	Supported	—	—
			Y: 12 bits CbCr: 8 bits	Supported	Supported	—	—
		YCbCr-422 separated Only Y	8 bits	Supported	Supported	Supported	Supported
			10 bits	Supported	Supported	—	—
12 bits	Supported		Supported	—	—		

- Notes: 1. When capturing progressive images, be sure to enable the internal field signal generation function.  
2. Dithering is performed for RGB-888→RGB-565 conversion.  
3. RGB data is converted and transferred to memory from the video module after 8-bit precision conversion.  
4. For details of output interfaces, see section 23.3.11, Output Data Format.

**Table 23.16 Video Channels and Supported Interfaces (RZ/G1M/N)**

				Channel 0	Channel 1	Channel 2
Input interface	ITU-R BT.656	YCbCr-422	8 bits	Supported	Supported	Supported
			10 bits	Supported	Supported	—
			12 bits	Supported	Supported	—
	ITU-R BT.1358/ ITU-R BT.601/ ITU-R BT.709	YCbCr-422	16 bits	Supported	Supported	—
			20 bits	Supported	Supported	—
			24 bits	Supported	Supported	—
	ITU-R BT.601/ ITU-R BT.709	YCbCr-422	8 bits	Supported	Supported	Supported
			10 bits	Supported	Supported	—
			12 bits	Supported	Supported	—
			RGB-666	18 bits	Supported	Supported
		RGB-888	24 bits	Supported	Supported	—
Output interface	RGB output	RGB-565	16 bits	Supported	Supported	Supported
		ARGB-1555	16 bits	Supported	Supported	Supported
		RGB-888	32 bits	Supported	Supported	Supported
		ARGB-8888	32 bits	Supported	Supported	Supported
	YCbCr output	YCbCr-422 multiplexed	8 bits	Supported	Supported	Supported

		<b>Channel 0</b>	<b>Channel 1</b>	<b>Channel 2</b>
YCbCr-422 separated Y/CbCr	Y: 8 bits CbCr: 8 bits	Supported	Supported	Supported
	Y: 10 bits CbCr: 8 bits	Supported	Supported	—
	Y: 12 bits CbCr: 8 bits	Supported	Supported	—
YCbCr-422 separated Only Y	8 bits	Supported	Supported	Supported
	10 bits	Supported	Supported	—
	12 bits	Supported	Supported	—

- Notes:
1. When capturing progressive images, be sure to enable the internal field signal generation function.
  2. Dithering is performed for RGB-888→RGB-565 conversion.
  3. RGB data is converted and transferred to memory from the video module after 8-bit precision conversion.
  4. For details of output interfaces, see section 23.3.11, Output Data Format.



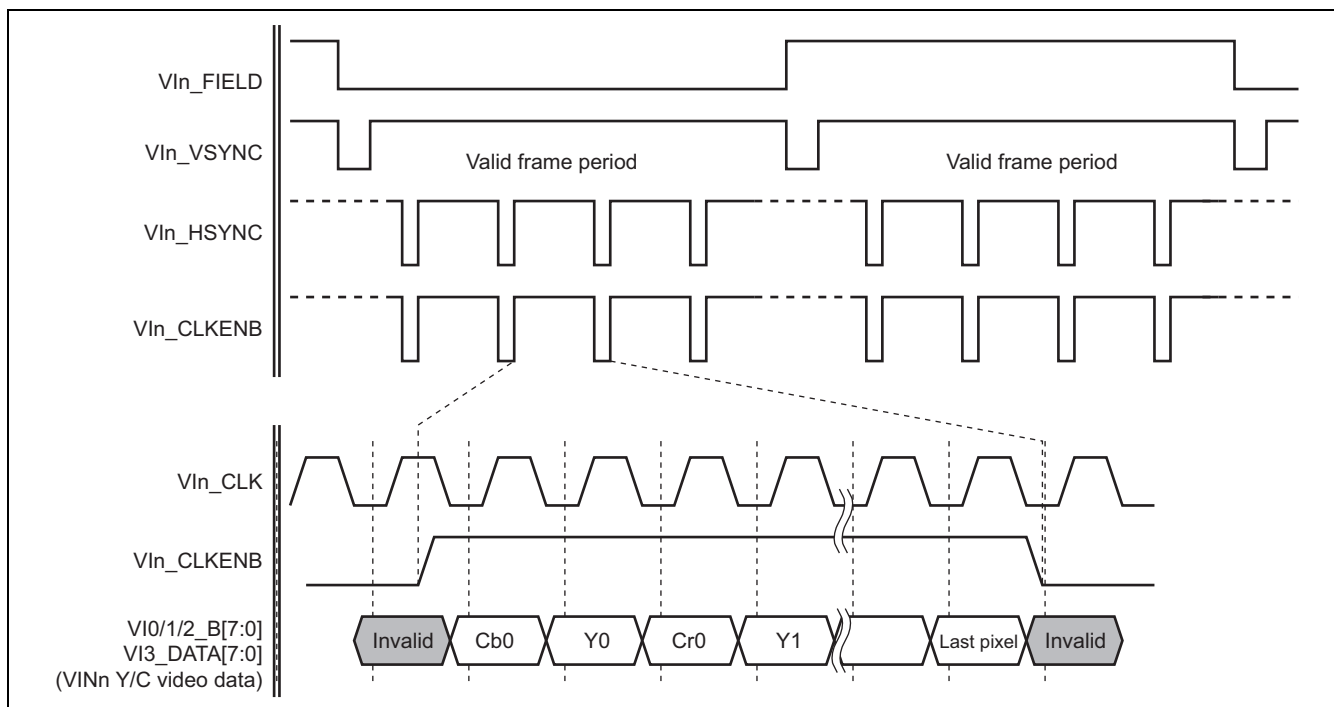
**Table 23.17 Video Channels and Supported Interfaces (RZ/G1E)**

				Channel 0	Channel 1	
Input interface	ITU-R BT.656	YCbCr-422	8 bits	Supported	Supported	
			10 bits	Supported	Supported	
			12 bits	Supported	Supported	
	ITU-R BT.1358/ ITU-R BT.601/ ITU-R BT.709	YCbCr-422	16 bits	Supported	—	
			20 bits	Supported	—	
			24 bits	Supported	—	
	ITU-R BT.601/ ITU-R BT.709	YCbCr-422	8 bits	Supported	Supported	
			10 bits	Supported	Supported	
			12 bits	Supported	Supported	
			RGB-666	Supported	—	
			RGB-888	Supported	—	
	Output interface	RGB output	RGB-565	16 bits	Supported	Supported
ARGB-1555			16 bits	Supported	Supported	
RGB-888			32 bits	Supported	Supported	
ARGB-8888			32 bits	Supported	Supported	
YCbCr output		YCbCr-422 multiplexed	8 bits	Supported	Supported	
			YCbCr-422 separated	Y: 8 bits CbCr: 8 bits	Supported	Supported
			Y/CbCr	Y: 10 bits CbCr: 8 bits	Supported	Supported
			Y: 12 bits CbCr: 8 bits	Supported	Supported	
			YCbCr-422 separated	8 bits	Supported	Supported
			10 bits	Supported	Supported	
			Only Y	12 bits	Supported	Supported

- Notes: 1. When capturing progressive images, be sure to enable the internal field signal generation function.  
2. Dithering is performed for RGB-888→RGB-565 conversion.  
3. RGB data is converted and transferred to memory from the video module after 8-bit precision conversion.  
4. For details of output interfaces, see section 23.3.11, Output Data Format.

**(1) Multiplexed YCbCr-422 Data Format in ITU-R BT.601 Interface**

Data in the multiplexed YCbCr-422 format is a UYVY format (U0Y0V0Y1 format) YCbCr data. The Y, Cb, Cr image data is captured at the rising edges of the input video clock signal.

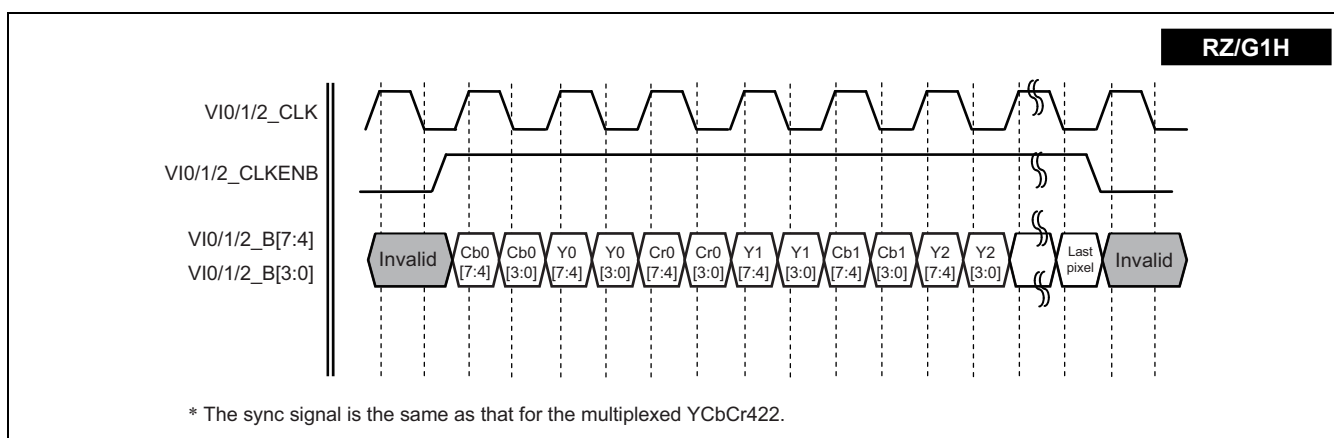


**Figure 23.4 Multiplexed YCbCr-422 Data Format (Example of RZ/G1H)**

**(2) Multiplexed YCbCr-422 (4 Bits) Data Format in ITU-R BT.601 Interface (RZ/G1H only)**

Data in the multiplexed YCbCr-422 format is a UYVY format (U0Y0V0Y1 format) YCbCr data. The Y, Cb, Cr image data is captured at the rising and falling edges of the input video clock signal.

When data are captured via this interface, the RIS bit in the main control register (VnMC) should be set to 1.

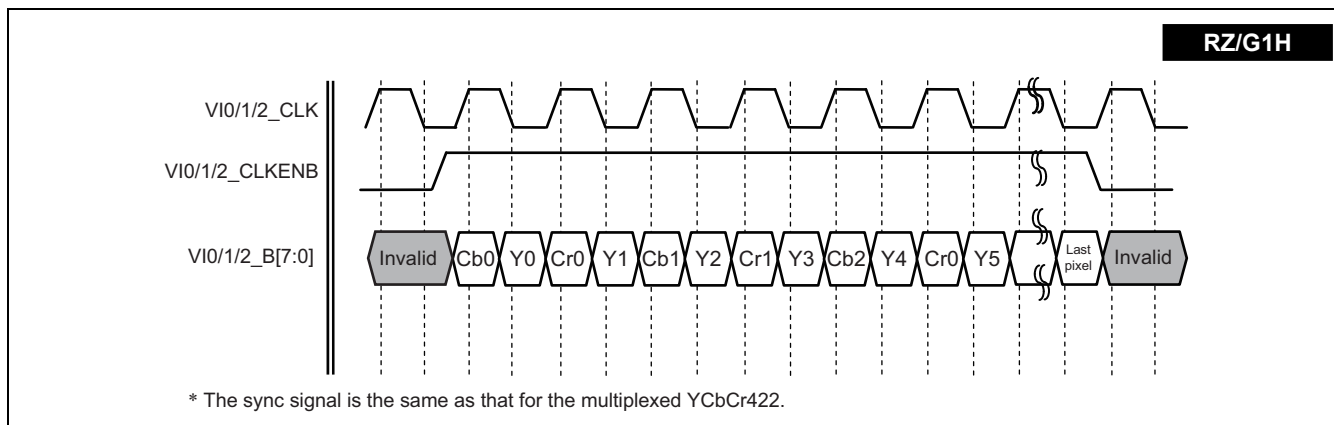


**Figure 23.5 Multiplexed YCbCr-422 (4 Bits) Data Format [RZ/G1H]**

**(3) Multiplexed YCbCr-422 (8 Bits) Data Format in ITU-R BT.601 Interface (RZ/G1H only)**

Data in the multiplexed YCbCr-422 format is a UYVY format (U0Y0V0Y1 format) YCbCr data. The Cb, Cr image data is captured at the rising edges of the input video clock signal and the Y image data is captured at the falling edges of the input video clock signal.

When data are captured via this interface, the RIS bit in the main control register (VnMC) should be set to 1.

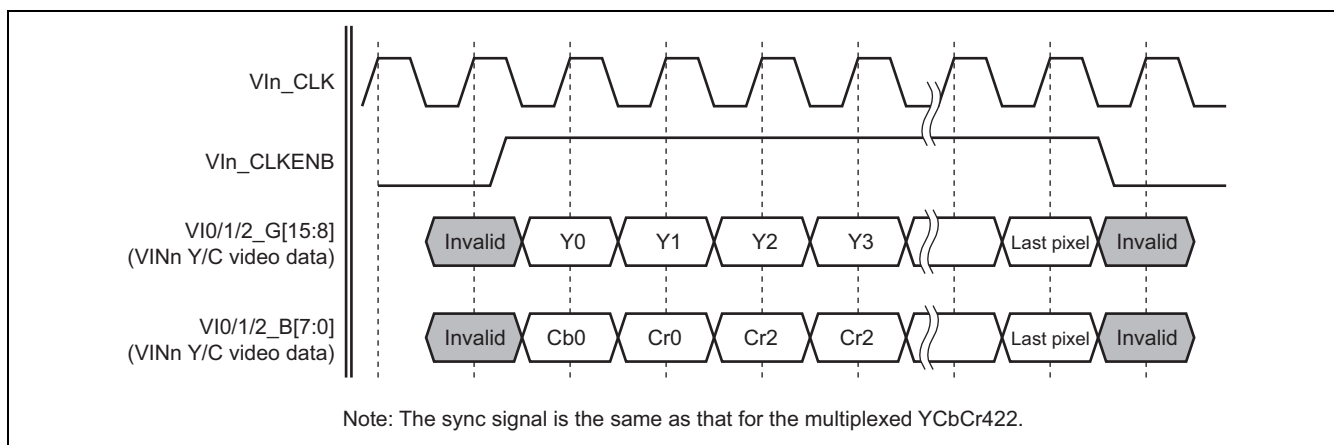


**Figure 23.6 Multiplexed YCbCr-422 (8 Bits) Data Format [RZ/G1H]**

**(4) CbCr Multiplexed YCbCr-422 Data Format in ITU-R BT.601/1358 Interface**

Data in the CbCr multiplexed YCbCr-422 format is YCbCr data with only the CbCr data being multiplexed. The Y and CbCr image data are captured at the rising edges of the input video clock signal.

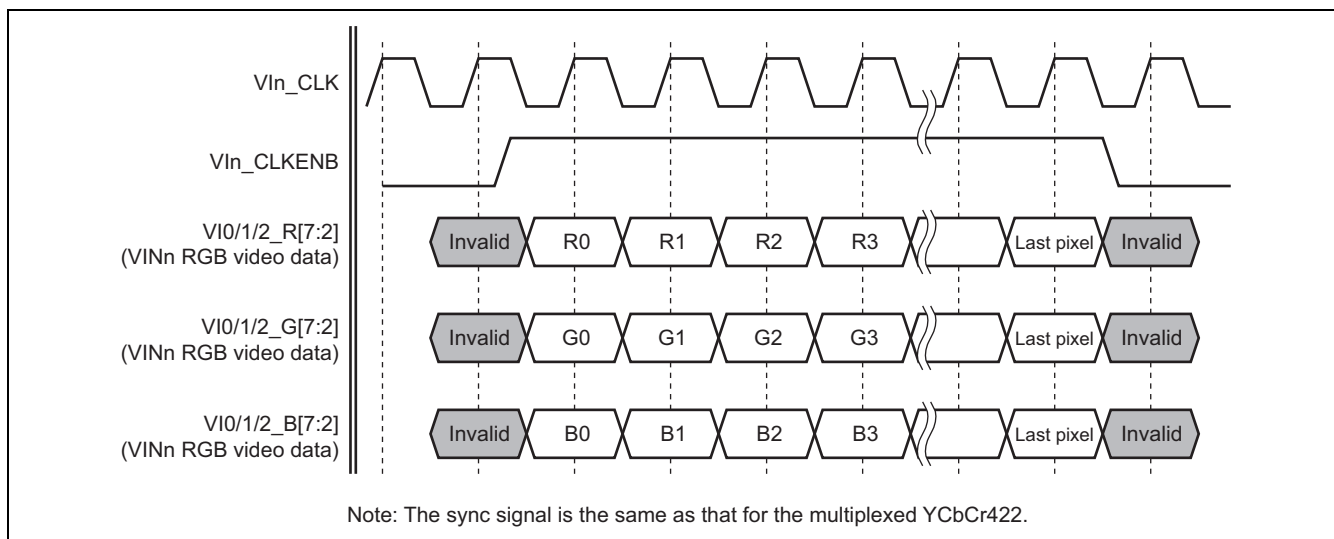
Setting the YCAL bit in VnMC to 1 enables the capturing of image data with CbCr data in the upper bits and Y data in the lower bits.



**Figure 23.7 CbCr Multiplexed YCbCr-422 Data Format (Y Data in Upper Bits) (Example of RZ/G1H)**

**(5) RGB-666 Data Format in ITU-R BT.601 Interface**

This data format can be used for the color conversion space in the RGB=4:4:4 format defined in the ITU-R BT.601 standard. The R, G, B image data are captured at the rising edges of the input video clock signal.

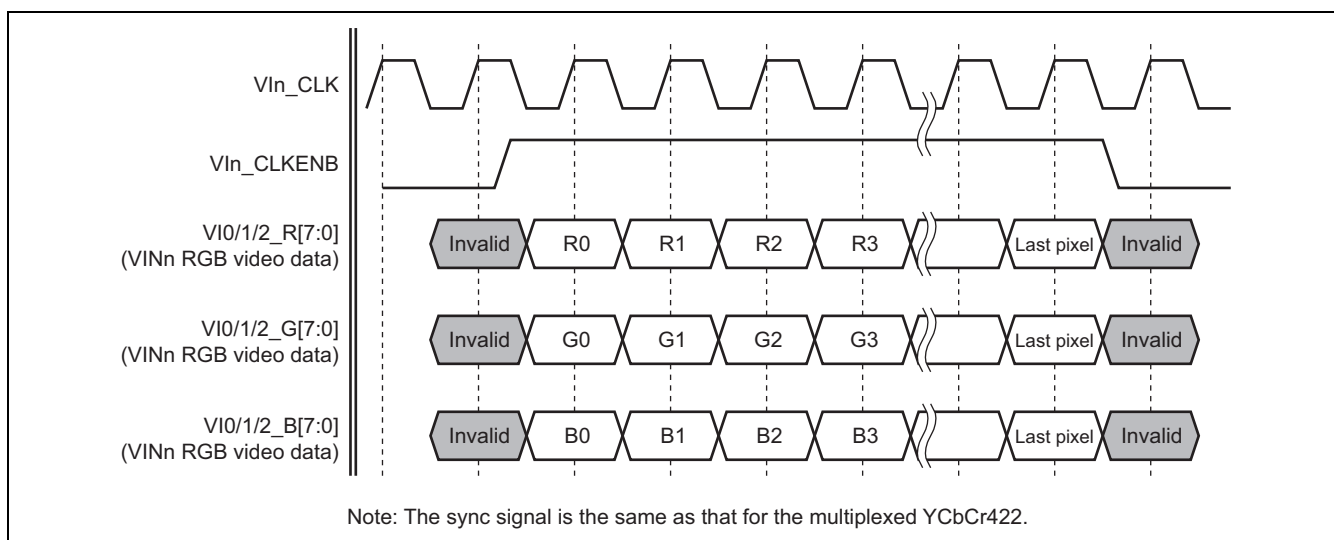


**Figure 23.8 RGB-666 Data Format (Example of RZ/G1H)**

**(6) RGB-888 (24 bits) Data Format in ITU-R BT.601 Interface**

This data format can be used for the color conversion space in the RGB=4:4:4 format defined in the ITU-R BT.601. The R, G, B image data are captured at the rising edges of the input video clock signal.

For the RZ/G1H, when data are captured via this interface, the RIS bit in the main control register (VnMC) should be set to 0.

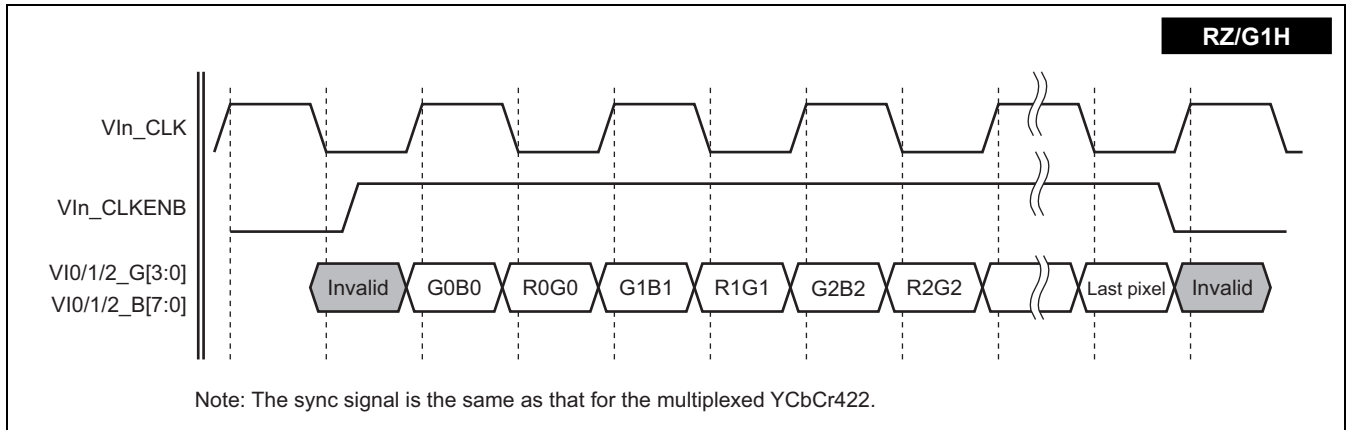


**Figure 23.9 RGB-888 (24 Bits) Data Format (Example of RZ/G1H)**

**(7) RGB-888 (12 bits) Data Format in ITU-R BT.601 Interface (RZ/G1H only)**

This data format can be used for the color conversion space in the RGB=4:4:4 format defined in the ITU-R BT.601. The R, G, B image data are captured at the rising and falling edges of the input video clock signal.

When data are captured via this interface, the RIS bit in the main control register (VnMC) should be set to 1.



**Figure 23.10 RGB-888 (12 Bits) Data Format (RZ/G1H Only)**

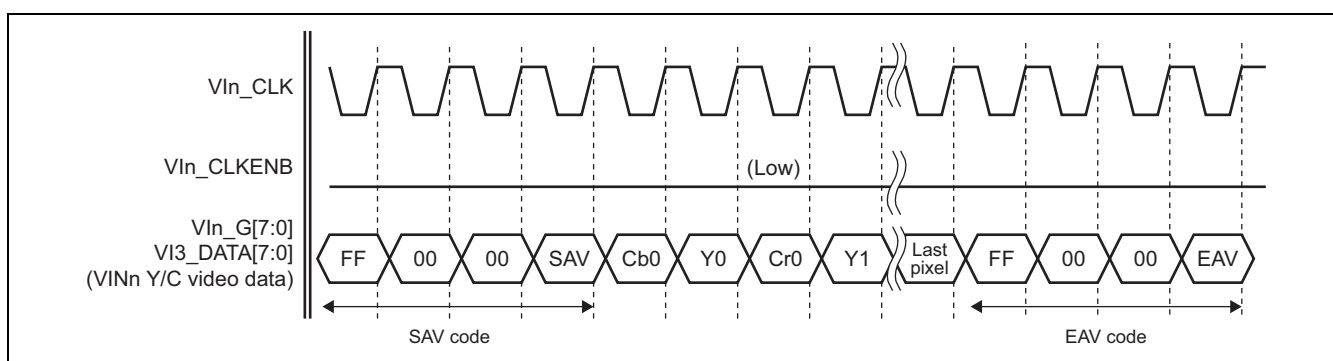
**(8) Multiplexed YCbCr-422 Data Format in ITU-R BT.656 Interface**

In the ITU-R BT.656 interface, active data between the start of active video (SAV) and the end of active video (EAV) indicated with the timing reference code is captured.

**Table 23.18 Video Timing Reference Code**

VINn Image Data			First Word	Second Word	Third Word	Fourth Word (XY)	
12 bits	10 bits	8 bits					
VIn_G[3]	VIn_G[1]	VIn_B[7]	1	0	0	1	
VIn_G[2]	VIn_G[0]	VIn_B[6]	1	0	0	F	0: Field 1 1: Field 2
VIn_G[1]	VIn_B[7]	VIn_B[5]	1	0	0	V	0: elsewhere 1: Field Blanking
VIn_G[0]	VIn_B[6]	VIn_B[4]	1	0	0	H	0: SAV 1: EAV
VIn_B[7]	VIn_B[5]	VIn_B[3]	1	0	0	P3	Protection bit 3
VIn_B[6]	VIn_B[4]	VIn_B[2]	1	0	0	P2	Protection bit 2
VIn_B[5]	VIn_B[3]	VIn_B[1]	1	0	0	P1	Protection bit 1
VIn_B[4]	VIn_B[2]	VIn_B[0]	1	0	0	P0	Protection bit 0
VIn_B[3]	VIn_B[1]	—	1	0	0	0	
VIn_B[2]	VIn_B[0]	—	1	0	0	0	
VIn_B[1]	—	—	1	0	0	0	
VIn_B[0]	—	—	1	0	0	0	

Active data is available with the multiplexed YCbCr-422 data format in the UYVY (U0Y0V0Y1) format. In this interface, timing reference and Y, Cb, Cr image data are captured at the rising edges of the input clock signal.



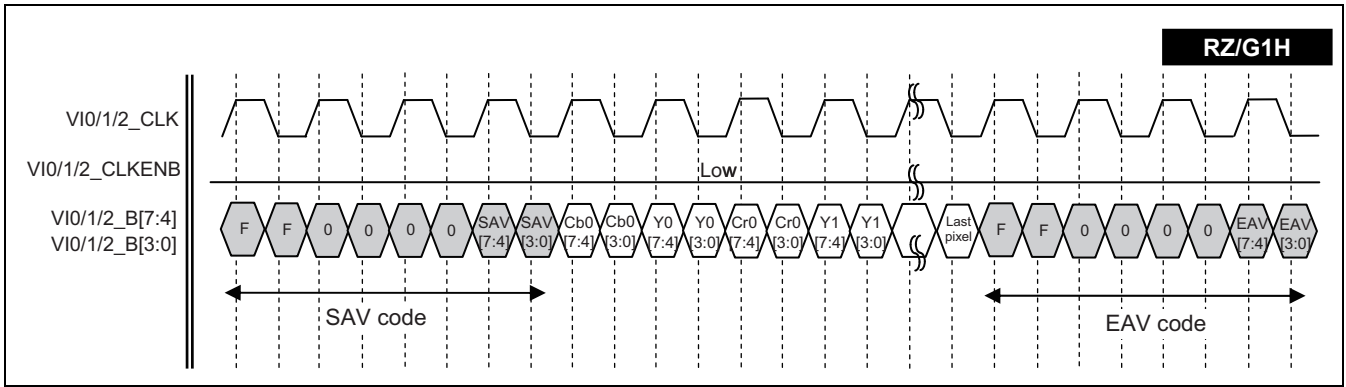
**Figure 23.11 Multiplexed YCbCr-422 Data Format (Example of RZ/G1H)**

Capturing is controlled based on field information. Therefore, the field signal and timing reference codes should be correct.

**(9) Multiplexed YCbCr-422 (4 Bits) Data Format in ITU-R BT.656 Interface (RZ/G1H only)**

Active data is available with the multiplexed YCbCr-422 data format in the UYVY (U0Y0V0Y1) format. In this interface, timing reference and Y, Cb, Cr image data are captured at the rising and falling edges of the input clock signal.

When data are captured via this interface, the RIS bit in the main control register (VnMC) should be set to 1.



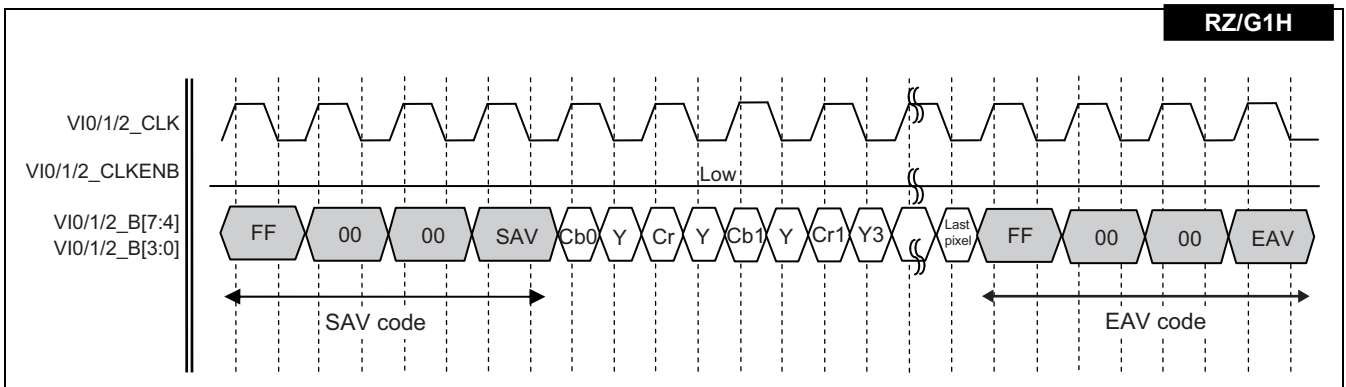
**Figure 23.12 Multiplexed YCbCr-422 (4 Bits) Data Format [RZ/G1H]**

Capturing is controlled based on field information. Therefore, the field signal and timing reference codes should be correct.

**(10) Multiplexed YCbCr-422 (8 Bits) Data Format in ITU-R BT.656 Interface (RZ/G1H only)**

Active data is available with the multiplexed YCbCr-422 data format in the UYVY (U0Y0V0Y1) format. In this interface, timing reference and Cb, Cr image data are captured at the rising and falling edges of the input clock signal, and timing reference and Y image data are captured at the falling edges.

When data are captured via this interface, the RIS bit in the main control register (VnMC) should be set to 1.



**Figure 23.13 Multiplexed YCbCr-422 (8 Bits) Data Format [RZ/G1H]**

Capturing is controlled based on field information. Therefore, the field signal and timing reference codes should be correct.

The same timing reference codes should be input for the rising and falling edges.

**23.3.2 Error Correction**

At the time of capturing with ITU-R BT.656, the VIN allows errors to be corrected with the timing reference code (SAV/EAV). The timing reference code (SAV/EAV) of ITU-R BT.656 has four protection bits, which can be used to correct only one-bit errors in the interface.

If the VIN cannot correct errors while the CEE bit in the interrupt enable register (VnIE) has been set to 1, an interrupt signal is generated as soon as the CES bit in the interrupt status (VnINTS) register is set. Note that no interrupt signal is generated if errors can be corrected.

### 23.3.3 Capture Mode

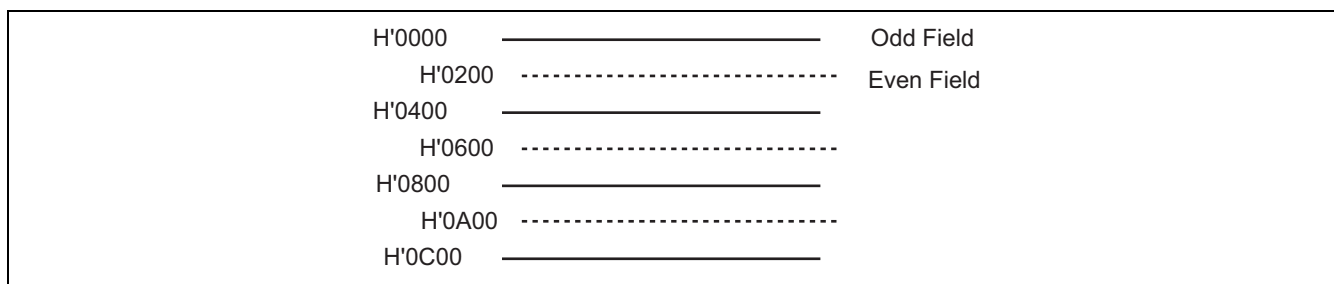
With the VIN, either of the single frame capture mode or continuous frame capture mode can be selected.

Specifying the capture field in IM bits of the main control (VnMC) register and then setting the SC bit in the frame capture (VnFC) register to 1 provides single frame capture mode. In this mode, the current frame is captured when the SC bit write timing (current scanline position) is smaller than the value of the start line pre-clip (VnSLPrC) register, or the next frame is captured in other cases. The capture data is transferred to the memory address that is set in the memory base 1 (VnMB1) register.

Specifying the capture field in IM bits of VnMC and then setting the CC bit of VnFC to 1 provides continuous frame capture mode, in which capture data is sequentially transferred to the addresses that are set in MB1 to MB3. In this case, the latest captured frame ID is shown in the FBS bits in the module status (VnMS) register.

When the IM bits in VnMC are set to the full interlace mode, data in the capture start field is stored in every other line in the memory as the odd field (field 1) data and then data in the next field is stored as the even field (field 2) between the written lines so that the top and bottom field lines alternate with each other for interlace composition. The capture start field (top field) can be changed through the FOC bit in VnMC.

The following is a schematic diagram of capturing in full interlace mode when the odd field (field 1) is selected as the top field, the memory width is set to H'200, and VnMB1 is set to H'0000.



**Figure 23.14 Example of Capturing Full Interlace**

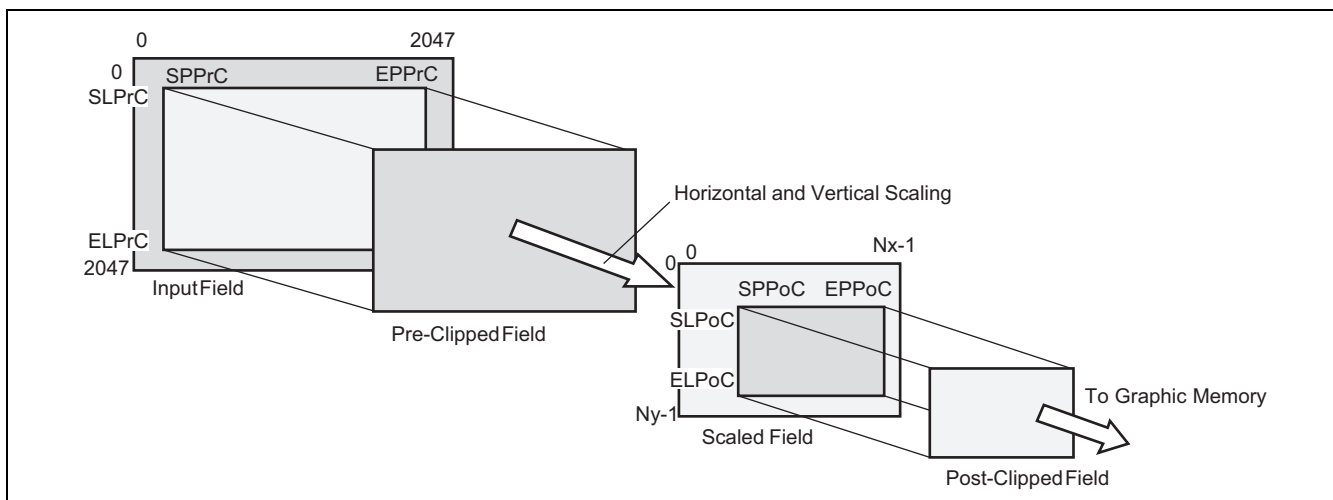
The VIN starts capture operation after detecting a frame signal switching in the ITU-R BT.601 or 656 interface. When capturing progressive data, in which the field signal does not change, use the internal field signal generation function to toggle the internal field signal.

### 23.3.4 Size Clipping

Image data that has been captured is pre-clipped according to the settings of the following registers: start line pre-clip (VnSLPrC), end line pre-clip (VnELPrC), start pixel pre-clip (VnSPPrC), and end pixel pre-clip (VnEPPrC).

After the horizontal and vertical scaling, post-clipping takes place according to the settings of the following registers: start line post-clip (VnSLPoC), end line post-clip (VnELPoC), start pixel post-clip (VnSPPoC), and end pixel post-clip (VnEPPoC). The following shows an example of size clipping.





**Figure 23.15 Example of Clipping**

For all the post-clipped lines, the lengths of individual lines written into the memory are defined by the image stride (VnIS) register. The setting can be larger than the post-clipped frame width, but cannot be smaller than the width. The VnIS register must be filled with a value larger than the horizontal post-clipping width. The input field in the above figure shows an effective image area from the video decoder; the VIN does not allow anything exceeding the image area to be captured.

Note: Each of the following registers specifies a distance from the starting point in the effective image area: start line pre-clip (VnSLPrC), end line pre-clip (VnELPrC), start pixel pre-clip (VnSPPrC), and end pixel pre-clip (VnEPPrC). Specifically, in ITU-R BT.601, the distance is from the starting point of Vin\_CLKENB (data enable); in ITU-R BT.656, the distance is from the SAV (start of active video) signal.

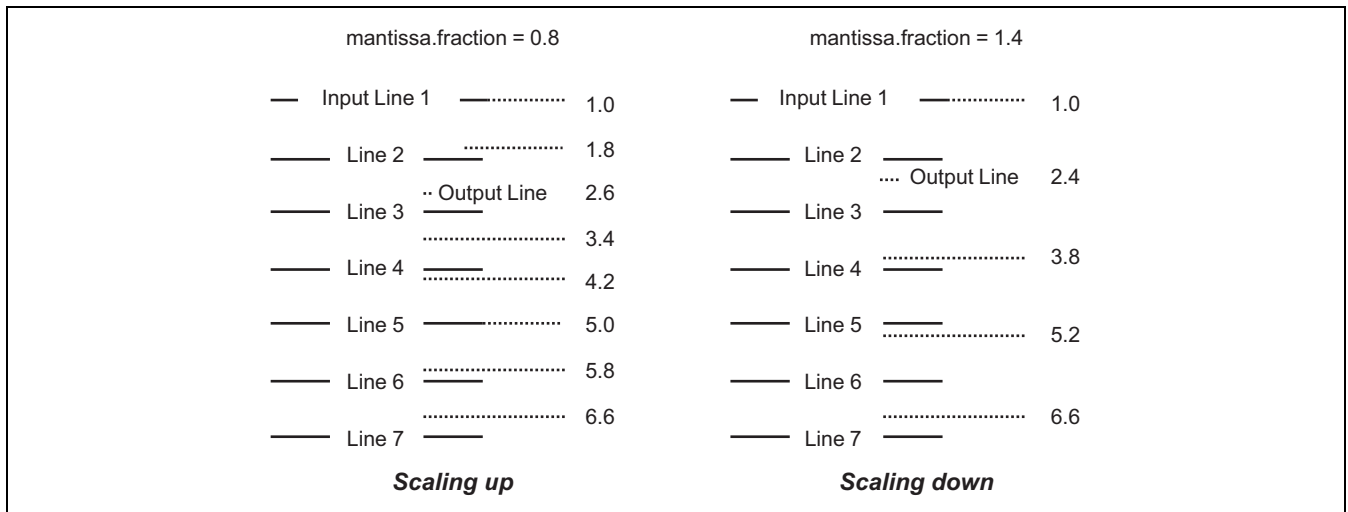
### 23.3.5 Vertical Scaling

The vertical scaling function in the VIN creates lines by scaling up or down in the vertical direction through interpolation between two points in the neighborhood of captured lines. With the combinations of mantissaY and fractionY in the Y scaling (VnYS) register, the vertical scaling creates new lines by selecting line positions from captured lines.

The Y scaling function is disabled if mantissaY and fractionY are both cleared to 0 in VnYS.

Scaling down is implemented by creating fewer lines than captured lines. Examples of scaling up and down are shown in the following figure.

Note: When vertical scaling up is specified in full interlace capture mode, the scaling-up processing is applied separately to each field before full interlace composition on memory. Accordingly, the top and bottom field lines are inverted in some cases depending on the scaling ratio. Be sure to evaluate the scaled image quality before practical application.



**Figure 23.16 Examples of Scaling Up and Down in Vertical Direction**

The number of lines created by the vertical scaling block is expressed by the following equation:

$$N_y = \begin{cases} \frac{4096 \times (ELPrC - SLPrC)}{4096 \times MantissaY + FractionY} - 1, & \text{when } \{4096 \times (ELPrC - SLPrC)\} \% (4096 \times MantissaY + FractionY) = 0 \\ Int \left( \frac{4096 \times (ELPrC - SLPrC)}{4096 \times MantissaY + FractionY} \right), & \text{otherwise} \end{cases}$$

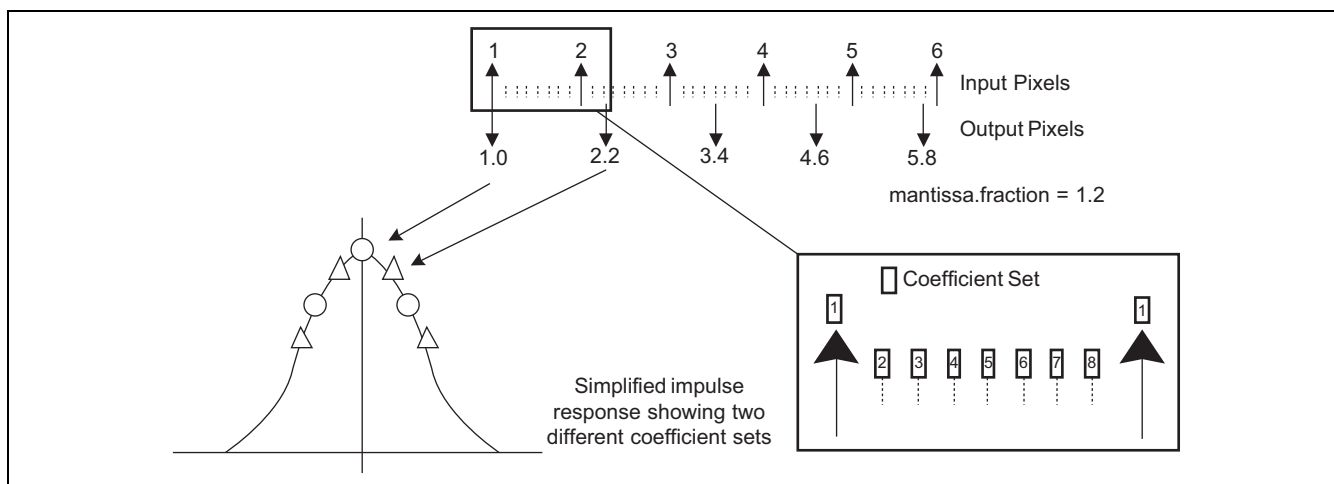
where:

ELPrC is the value in the end line pre-clip (VnELPrC) register.  
 SLPrC is the value in the start line pre-clip (VnSLPrC) register.  
 MantissaY and FractionY are the values in VnYS.

### 23.3.6 Horizontal Scaling

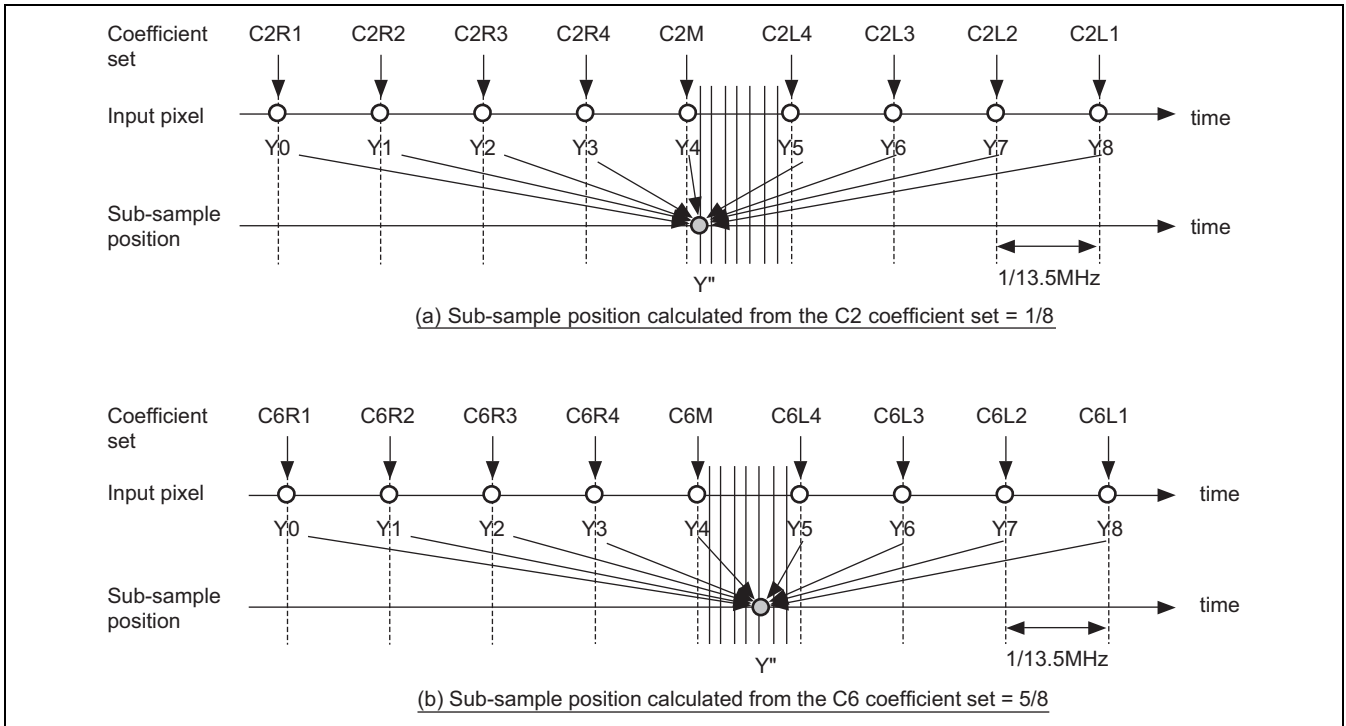
Using a 9-tap multiphase filter, the VIN creates pixels by scaling down in the horizontal direction. The horizontal scaling-up doubles the number of input pixels captured and provides the function of expansion of up to two-fold by the scaling-down in the 9-tap multiphase filter. The horizontal scaling, which is set through combinations of mantissaX and fractionX in the X scale (VnXS) register, determines the position of new pixels with a poly-phase filter. The selected coefficient, which is one of the eight coefficients, is determined by the position of output pixels.

In the example shown below, mantissaX and fractionX are set at 1.2. In this case, coefficient set C2 is selected.



**Figure 23.17 Pixel Position and Coefficient Set**

The following figure shows an example in which different coefficient sets are used for different output pixel positions. Nine coefficient sets are assigned to each. A total of 72 coefficients are used in the horizontal scaling. Each of the coefficients in these sets has a width of 10 bits, where the MSB serves as the sign bit. By setting the same coefficients into the entire eight coefficient set registers, the horizontal scaling allows the use of a multiphase filter just like a single-phase filter.



**Figure 23.18 Example of Coefficients in Selected Coefficient Set**

This scaling mechanism requires different coefficient values dependent on the scaling ratio. Here is an example of coefficient sets to be selected. The coefficients,  $C_{mM}$ ,  $C_{mLi}$ , and  $C_{mRi}$  ( $m = 1, 2, 3, \dots, 8$ ;  $i = 1, 2, 3, \text{ and } 4$ ), are determined by the following equations:

$$C_{nM} = \beta \times h(-(n-1))$$

$$C_{nRi} = \beta \times h(-(n-1) - 8(5-i))$$

$$C_{nLi} = \beta \times h(-(n-1) + 8(5-i))$$

$$h(t) = \frac{\sin\left(\frac{\pi t}{T}\right)}{\frac{\pi t}{T}} \times \frac{\cos\left(\frac{\alpha \pi t}{T}\right)}{1 - \frac{4\alpha^2 t^2}{T^2}}$$

$$T = 8 \times \text{MantissaX} + \text{FractionX} \text{ [11:9]}$$

Mantissa X and Fraction X are the values in VnXS.

The parameter  $\beta$  is a standardized one. In the equation,  $h(t)$  follows the cosine characteristic and is executed with a 9-tap filter if the value of  $\alpha$  is in the  $0 < \alpha \leq 1$  range.

Obtaining dependable scale images requires you to use and meet the following equation in which all the coefficient sets are standardized.

This must be executed with the inherent  $\beta$  value that has been selected from the equation above.

$$C_{nM} + \sum_{i=1}^4 C_{nRi} + \sum_{i=1}^4 C_{nLi} = 512$$

The number of pixels created by the horizontal scaling block is calculated by the following equation.

$$N_x = \text{Int} \left( \frac{4096 \times (EPPrC - SPPrC)}{4096 \times \text{MantissaX} + \text{FractionX}} \right) + 1$$

where:

EPPrC is the value in the end pixel pre-clip (VnEPPrC) register.

SPPrC is the value in the start pixel pre-clip (VnSPPrC) register.

Mantissa X and Fraction X are the values in VnXS.

### 23.3.7 Color Conversion Function

#### (1) YC-RGB Color Conversion

When the data input format is YCbCr, set the BPS bit in the VnMC register to 0 to convert YCbCr data to RGB data. If an 8-bit data format is used for the capture interface, the color conversion is carried out according to the matrix coefficients set in the VnCSCC1, VnCSCC2, and VnCSCC3 registers. Otherwise, it is carried out according to the matrix coefficients set in the VnCSCE1, VnCSCE2, VnCSCE3, and VnCSCE4 registers. All of the input YCbCr data is extended to 12-bit data before carrying out color conversion.

Here, if the BPS bit in VnMC is set to 1, the data is stored in memory as it is in YCbCr format.

$$\begin{aligned}
 R &= \begin{pmatrix} VnCSCC1/ \\ YMUL[9:0] \\ or \\ VnCSCE1/ \\ YMUL2[13:0] \end{pmatrix} \times (Y - \begin{pmatrix} VnCSCC1/ \\ YSUB[7:0] \\ or \\ VnCSCE1/ \\ YSUB2[11:0] \end{pmatrix}) + \begin{pmatrix} VnCSCC2/ \\ RCRMUL[9:0] \\ or \\ VnCSCE3/ \\ RCRMUL2[13:0] \end{pmatrix} \times (Cr - \begin{pmatrix} VnCSCC1/ \\ CSUB[7:0] \\ or \\ VnCSCE1/ \\ CSUB2[11:0] \end{pmatrix}) \\
 G &= \begin{pmatrix} VnCSCC1/ \\ YMUL[9:0] \\ or \\ VnCSCE1/ \\ YMUL2[13:0] \end{pmatrix} \times (Y - \begin{pmatrix} VnCSCC1/ \\ YSUB[7:0] \\ or \\ VnCSCE1/ \\ YSUB2[11:0] \end{pmatrix}) - \begin{pmatrix} VnCSCC2/ \\ GCRMUL[9:0] \\ or \\ VnCSCE3/ \\ GCRMUL2[13:0] \end{pmatrix} \times (Cr - \begin{pmatrix} VnCSCC1/ \\ CSUB[7:0] \\ or \\ VnCSCE1/ \\ CSUB2[11:0] \end{pmatrix}) - \begin{pmatrix} VnCSCC3/ \\ GCBMUL[9:0] \\ or \\ VnCSCE4/ \\ GCBMUL2[13:0] \end{pmatrix} \times (Cb - \begin{pmatrix} VnCSCC1/ \\ CSUB[7:0] \\ or \\ VnCSCE1/ \\ CSUB2[11:0] \end{pmatrix}) \\
 B &= \begin{pmatrix} VnCSCC1/ \\ YMUL[9:0] \\ or \\ VnCSCE1/ \\ YMUL2[13:0] \end{pmatrix} \times (Y - \begin{pmatrix} VnCSCC1/ \\ YSUB[7:0] \\ or \\ VnCSCE1/ \\ YSUB2[11:0] \end{pmatrix}) + \begin{pmatrix} VnCSCC3/ \\ BCBMUL[9:0] \\ or \\ VnCSCE4/ \\ BCBMUL2[13:0] \end{pmatrix} \times (Cb - \begin{pmatrix} VnCSCC1/ \\ CSUB[7:0] \\ or \\ VnCSCE1/ \\ CSUB2[11:0] \end{pmatrix})
 \end{aligned}$$

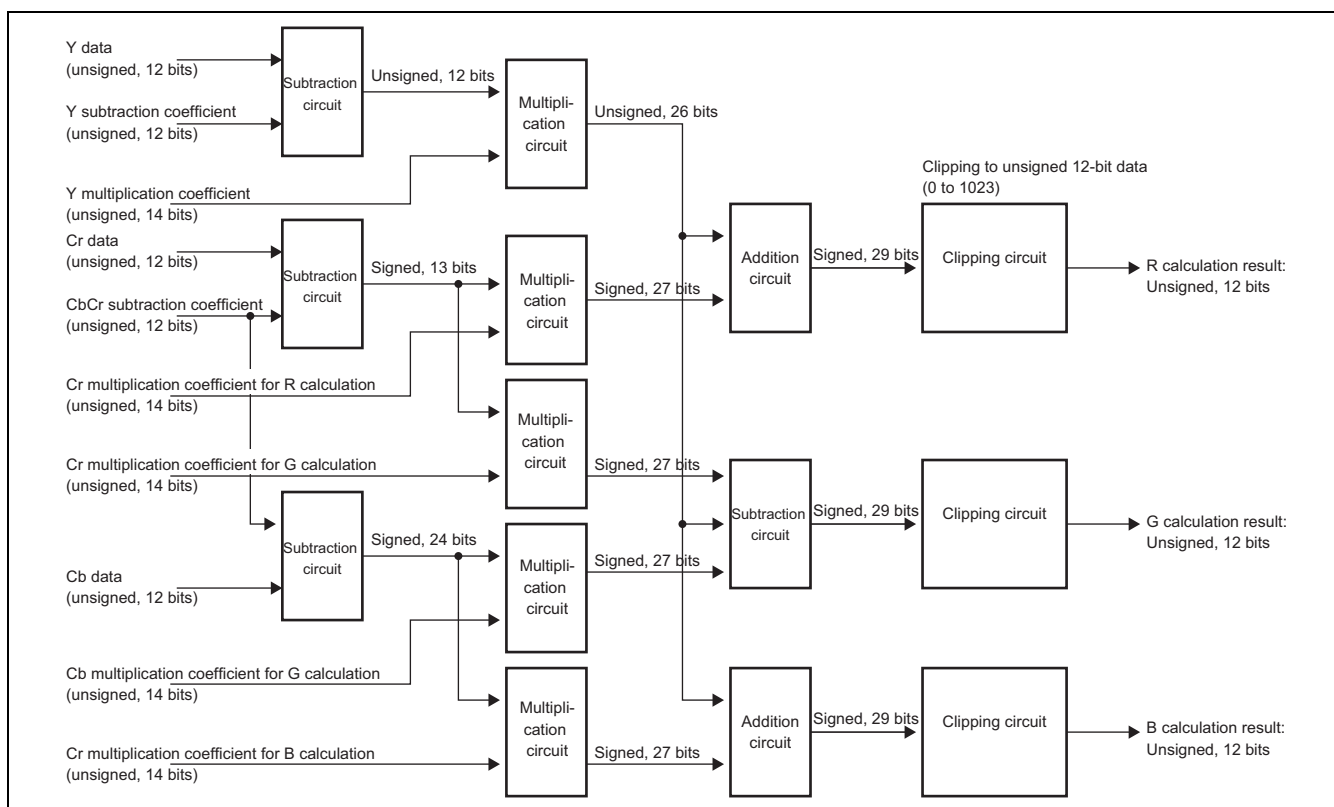


Figure 23.19 YCbCr→RGB Calculation Circuit Configuration

Examples of color space that can be set in YC-RGB conversion coefficient registers are shown below. See the register descriptions for details of the coefficients.

**Table 23.19 Examples of YC-RGB Conversion Coefficient Register Settings**

YC-RGB Conversion Coefficient	YMUL	YSUB	CSUB	RCRMUL	GCRMUL	GCBMUL	BCBMUL
ITU-R BT.601 (initial value) 16 ≤ Y ≤ 235, 16 ≤ Cb, Cr ≤ 240	1.164	16	128	1.596	0.813	0.392	2.017
Luminance expansion example 1 ≤ Y ≤ 254, 16 ≤ Cb, Cr ≤ 240	1.008	1	128	1.596	0.392	0.813	2.017

Specify an integer in each addition coefficient bit field. For each multiplication coefficient, specify a value obtained by multiplying the desired coefficient value by 256.

Example: When the desired multiplication coefficient is 1.164

$$1.164 \times 256 = 297 \text{ (set value: B'0100101001)}$$

- Notes:
1. In order to process the data outside the range prescribed by the ITU-R BT.601 standard, set the CLP[1:0] bits in VnMC to 11. The data is clipped to the specified value before color space conversion.
  2. The YC-RGB color conversion data is unconditionally rounded to the  $0 \leq R, G, B \leq 255$  range.

## (2) RGB-YC Color Conversion

When the data input format is RGB, set the BPS bit in VnMC to 0 for color conversion of RGB data into YCbCr data format. Color conversion from RGB to YCbCr is done according to the matrix coefficients set in RGB-YC conversion coefficient registers (VnYCCR1-VnYCCR3/VnCBCCR1-VnCBCCR3/VnCRCCR1-VnCRCCR3). All of the input RGB data is extended to 12-bit data before color conversion.

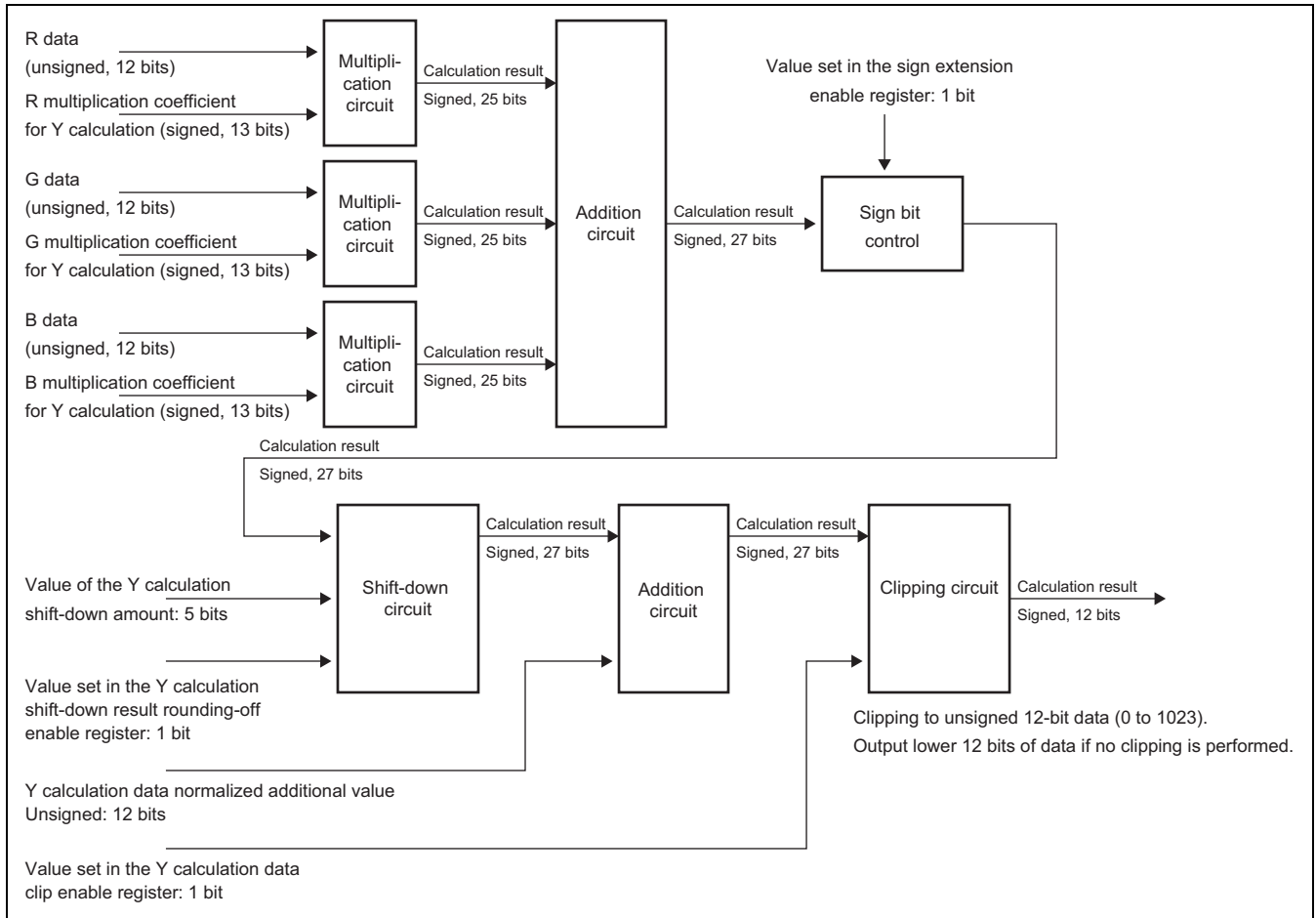
If 1 is set to the BPS bit in VnMC, the data will be stored in the memory as it is in RGB format.

$$\begin{aligned}
 Y &= (( YCLRP \times R + YCLGP \times G + YCLGP \times B) \times 2^{YCLSFT}) + YCALP \\
 Cb &= (( CBCLRP \times R + CBCLGP \times G + CBCLGP \times B) \times 2^{CBCLSFT}) + CBCALP \\
 Cr &= (( CRCLRP \times R + CRCLGP \times G + CRCLGP \times B) \times 2^{CRCLSFT}) + CRCALP
 \end{aligned}$$

The following data rounding functions of RGB-YCbCr color conversion function can be independently set to each pixel. The circuit configuration of Y data is given below.

**Table 23.20 Data Rounding Functions of RGB-YC Color Conversion Function**

Function	Symbol	Description
Sign extension enable	YEXPEN	Enables/disables signed bits of the matrix multiplication result.
Multiplication result shift down amount	YCLSFT[4:0]	Amount of shift down in the matrix multiplication result
Rounding off enable	YCLHEN	Enables/disables rounding off to the shift down amount.
Clipping enable	YLCEN	Enables/disables data rounding process between 0 to 1023 of the output data.



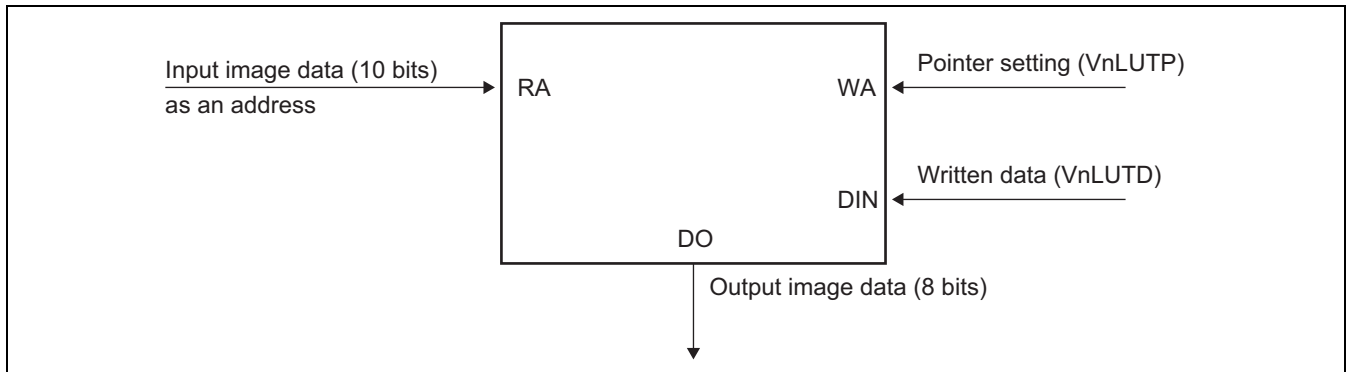
**Figure 23.20 Y Data Circuit Configuration of RGB → YCbCr Color Conversion Function**



### 23.3.8 Image Data Format Conversion Functions

#### (1) Lookup Table (LUT) Density Conversion Function

Set the LUTE bit in VnMC to 1 to enable table conversion of each pixel data of Y, Cb, Cr and R, G, B data after color conversion.



**Figure 23.21 Lookup Table**

#### Pointer Access:

The pointer is incremented every time a write access to the VnLUTD register is made.

The incremented data is read when the VnLUTP register is read. Since data is not incremented at read access, the pointer should be set just before reading.

The procedure given below must be followed to access the lookup table.

The lookup table cannot be accessed from the CPU during the conversion process.

(For write/read access to the LUT from the CPU, the LUTE bit in VnMC should be 0.)

#### Write access:

1. Write the access destination address in VnLUTP.
2. Write the data in VnLUTD.  
Thereby the data will be reflected in the lookup table.  
Also the pointer will automatically increase by 1.
3. Writing to VnLUTD will consecutively update the lookup table.

#### Read Access:

1. Write the access destination address in VnLUTP.
2. Read VnLUTD. This is dummy read; thus the read data needs to be discarded.
3. Read VnLUTD. This reading allows the address data written in VnLUTP to be acquired.

#### [Notes on Using the Lookup Table]

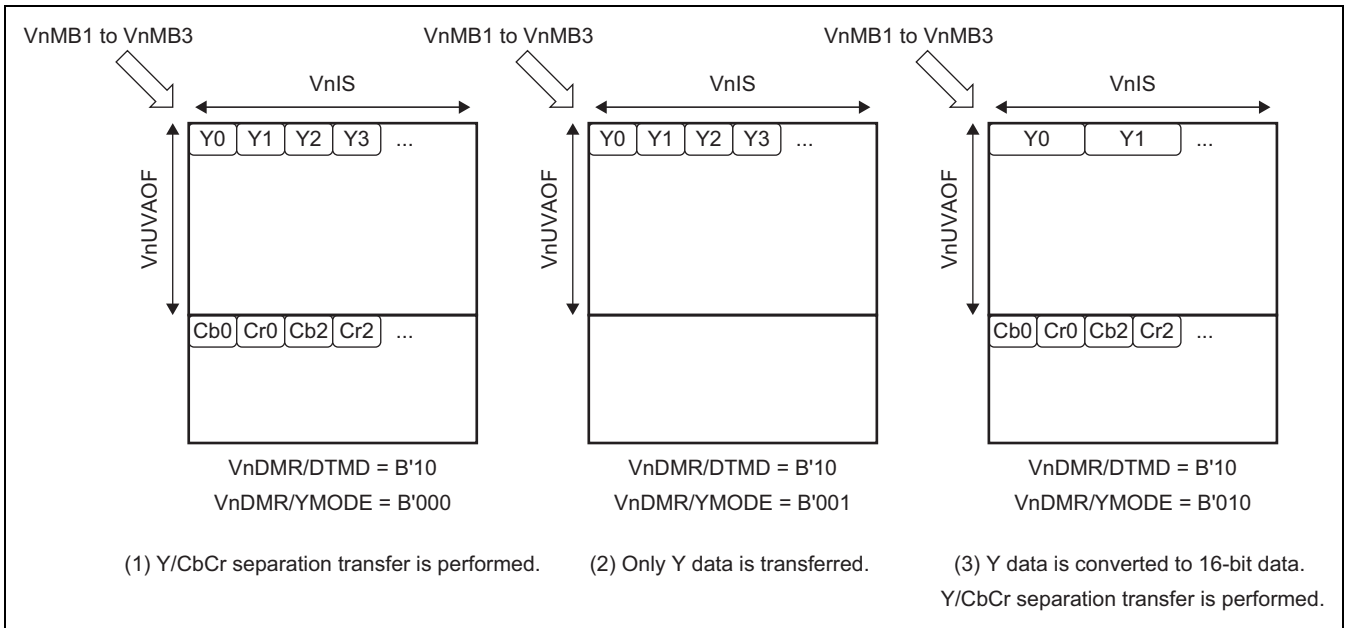
1. Set the lookup table only after capture operation has stopped.
2. Rewrite all before using the lookup table.
3. Data set to the lookup table should be within the range compatible to the input bit width.

**(2) YCbCr444→YC Separation Function**

When transferring YCbCr data to memory, Y data and CbCr data can be separated and transferred to different address spaces.

To perform YCbCr separation transfer, set the DTMD[1:0] bits in the VnDMR register to B'10. In this case, the Y data will be transferred to the address set in the memory base address register and CbCr data will be transferred to the address obtained by adding the value set in the VnUVAOF register to the memory base address register.

If the YMODE[2:0] bits in the VnDMR register are set, only Y data will be transferred to memory and CbCr data is not transferred to memory.



**Figure 23.22 Y/Cb/Cr Separation in Big Endian**

**(3) Dithering Function**

Dithering is performed when the internal RGB-888 format after color space conversion is converted to the RGB-565 or RGB-1555 format. The dithering mode can be selected with the DC[1:0] bits in VnMC.

**(a) Dithering with Cumulative Addition**

Set the DC[1:0] bits in VnMC to B'00 to perform dithering using the cumulative addition method in horizontal pixel units.

$$R_n [7:3] \leq (R_x[7:0] + R_{n-1}[2:0]) \gg 3$$

$$G_n [7:2] \leq (G_x[7:0] + G_{n-1}[1:0]) \gg 2$$

$$B_n [7:3] \leq (B_x[7:0] + B_{n-1}[2:0]) \gg 3$$

Where:

( $R_n, G_n, B_n$ ) = Output RGB-565 pixel

( $R_x, G_x, B_x$ ) = Input RGB-888 pixel

( $R_{n-1}, G_{n-1}, B_{n-1}$ ) = Pseudo random error (LSB of the cumulative error)

**(b) Ordered Dithering**

Set the DC[1:0] bits in VnMC to B'01 to perform dithering using the ordered dithering method.

$$R_n [7:3] \leq (R_x[7:0] + D_{42_{xy}}) \gg 3$$

$$G_n [7:2] \leq (G_x[7:0] + D_{22_{xy}}) \gg 2$$

$$B_n [7:3] \leq (B_x[7:0] + D_{42_{xy}}) \gg 3$$

Where:

( $R_n$ ,  $G_n$ ,  $B_n$ ) = Output RGB-565 pixel

( $R_x$ ,  $G_x$ ,  $B_x$ ) = Input RGB-888 pixel

( $D_{22_{xy}}$ ,  $D_{42_{xy}}$ ) = Input x, y coordinate dithering matrix result

$$D_{22} = \begin{bmatrix} 0 & 3 \\ 2 & 1 \end{bmatrix}, D_{42} = \begin{bmatrix} 0 & 3 & 4 & 7 \\ 2 & 1 & 6 & 5 \end{bmatrix}$$

### 23.3.9 Internal Field Signal Generation

As the video input module controls capture of data in interlaced mode, correct capture control is not achieved if the external field signal level does not change.

Through the internal field signal generation function, the VIN can control the capture field signal even when the input field signal does not change, such as during progressive data capturing. The following settings can be made for the internal field generation function through the FTEV and FTEH bits in the data mode register 2 (VnDMR2).

- VSYNC field toggle mode (FTEV = 1 in VnDMR2)

When this setting is made, the VSYNC field toggle mode is entered for capture field signal control if the input field signal does not change for the VSYNC cycles specified by the VLV bits in VnDMR2. The toggle mode is canceled when a change in the external field signal level is detected (the capture operation is controlled according to the input field signal).
- HSYNC field toggle counter (FTEH = 1 in VnDMR2)

This counter counts the capture active lines. If the external field signal does not change until the count reaches the HLV setting in VnDMR2, the capture field signal is controlled.

Notes: 1. Do not set both the FTEV and FTEH bits in VnDMR2 at the same time.  
 2. Immediately after cancellation of the toggle mode, capture control is skipped for one VSYNC cycle in some cases depending on the input field signal state.

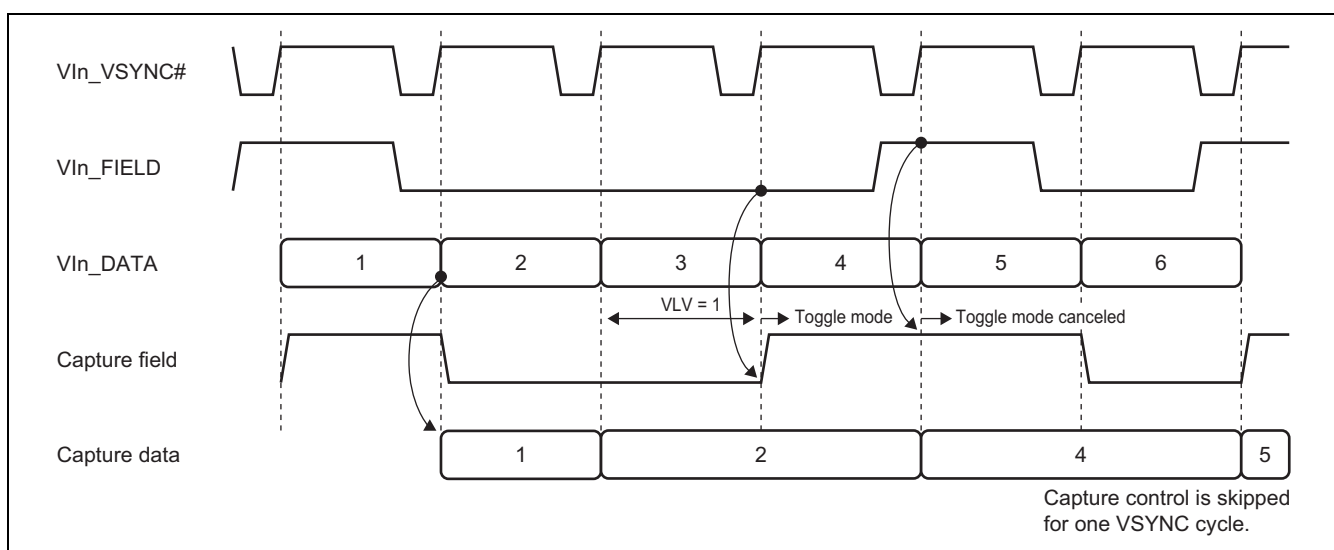


Figure 23.23 Overview and Notes of VSYNC Field Toggle Mode

### 23.3.10 Local Video Interface Output

A local video interface can be provided for each video channel to transfer captured data of the video channels to the IMR-LSX2 module.

- If distortion correction and scaling process are performed, use the IMR-LSX2 module.
- Post-clipping cannot be performed for image data output from a local video interface.

### 23.3.11 Output Data Format

The VIN can output image data in the following formats. The figures in this section assume that data is stored in unified memory in little endian.

#### (1) YC: YCbCr-422, 8 bits

The 8-bit YUV image data in the YC (YCbCr) = 4:2:2 format is shown below. YC data can be switched between the UYVY format and YUYV format through the BPSM bit in VnDMR.

- BPSM = 0 in VnDMR: UYVY format

8-bit YCbCr-422 data (UYVY format)

D63 to D48	63	56	55	48
Image data 3 and 4	Y3[7:0]		Cr2[7:0]	
D47 to D32	47	40	39	32
Image data 3 and 4	Y2[7:0]		Cb2[7:0]	
D31 to D16	31	24	23	16
Image data 1 and 2	Y1[7:0]		Cr0[7:0]	
D15 to D0	15	8	7	0
Image data 1 and 2	Y0[7:0]		Cb0[7:0]	

- BPSM = 1 in VnDMR: YUYV format

8-bit YCbCr-422 data (YUYV format)

D63 to D48	63	56	55	48
Image data 3 and 4	Cr2[7:0]		Y3[7:0]	
D47 to D32	47	40	39	32
Image data 3 and 4	Cb2[7:0]		Y2[7:0]	
D31 to D16	31	24	23	16
Image data 1 and 2	Cr0[7:0]		Y1[7:0]	
D15 to D0	15	8	7	0
Image data 1 and 2	Cb0[7:0]		Y0[7:0]	

**(2) YC: YC Separation YCbCr-422, 8 bits**

This is 8-bit YUV image data in the YC separated YC (YCbCr) = 4:2:2 format. UV data is supported by the NV12 format only.

If the YMODE[2:0] bits in the data mode register (VnDMR) are set to B'000 or B'001, setting the DTMD[1:0] bits in VnDMR to B'10 changes the format to 4:2:2 and transfers the UV data to an address which is specified by the addition of the value set in the UV address offset register (VnUVAOF) to the Memory Base. If the YMODE[2:0] bits in VnDMR are set to B'001, only Y data can be transferred and UV data cannot be transferred.

## Y data

D31 to D16	31	24	23	16
Image data 3 and 4	Y3[7:0]		Y2[7:0]	

D15 to D0	15	8	7	0
Image data 1 and 2	Y1[7:0]		Y0[7:0]	

## Cb, Cr data

D31 to D16	31	24	23	16
Image data 3 and 4	Cr2[7:0]		Cb2[7:0]	

D15 to D0	15	8	7	0
Image data 1 and 2	Cr0[7:0]		Cb0[7:0]	

**(3) YC: YC Separation YCbCr-422, 10 bits**

This is 10-bit YUV image data in the YC separated YC (YCbCr) = 4:2:2 format. UV data is supported by the NV12 format only.

If the YMODE[2:0] bits in the data mode register (VnDMR) are set to B'010 or B'011, setting the DTMD[1:0] bits in VnDMR to B'10 converts 10-bit Y data to 16-bit and changes the format to 4:2:2. UV data is transferred to the address obtained by adding the value set in the UV address offset register (VnUVAOF) to Memory Base. If the YMODE[2:0] bits in VnDMR are set to B'011, only Y data can be transferred and UV data cannot be transferred.

- Notes: 1. A word address is output for Y data according to the VnIS register setting.  
2. A byte address is output for CbCr data according to the VnIS register setting.

## Y data

D31 to D16	31	26	25	16
Image data 3 and 4	0	0	0	0
	0	0	0	0
				Y1[9:0]

D15 to D0	15	10	9	0
Image data 1 and 2	0	0	0	0
	0	0	0	0
				Y0[9:0]

## Cb, Cr data

D31 to D16	31	24	23	16
Image data 3 and 4	Cb2[7:0]			
	Cr2[7:0]			

D15 to D0	15	8	7	0
Image data 1 and 2	Cb0[7:0]			
	Cr0[7:0]			

**(4) YC: YC Separation YCbCr-422, 12 bits**

This is 12-bit YUV image data in the YC separated YC (YCbCr) = 4:2:2 format. UV data is supported by the NV12 format only.

If the YMODE[2:0] bits in the data mode register (VnDMR) are set to B'100 or B'101, setting the DTMD[1:0] bits in VnDMR to B'10 converts 12-bit Y data to 16-bit and changes the format to 4:2:2. UV data is transferred to the address obtained by adding the value set in the UV address offset register (VnUVAOF) to Memory Base. If the YMODE[2:0] bits in VnDMR are set to B'101, only Y data can be transferred and UV data cannot be transferred.

- Notes: 1. A word address is output for Y data according to the VnIS register setting.  
2. A byte address is output for CbCr data according to the VnIS register setting.

Y data

D31 to D16	31	28	27	16	
Image data 3 and 4	0	0	0	0	Y1[11:0]

D15 to D0	15	12	11	0	
Image data 1 and 2	0	0	0	0	Y0[11:0]

Cb, Cr data

D31 to D16	31	24	23	16	
Image data 3 and 4	Cr2[7:0]			Cb2[7:0]	

D15 to D0	15	8	7	0	
Image data 1 and 2	Cr0[7:0]			Cb0[7:0]	

**(5) 16 Bits/Pixel: RGB-565**

The RGB levels are expressed through 5 bits for R, 6 bits for G, and 5 bits for B.

16 bits/pixel data (RGB data) format

D15 to D0	15	11	10	5	4	0
Image data	R[4:0]			G[5:0]		B[4:0]

**(6) 16 Bits/Pixel: ARGB-1555**

The ARGB levels are expressed through 1 bit for A, 5 bits for R, 5 bits for G, and 5 bits for B. For data conversion to ARGB-1555, the lowest bit of the G data in RGB-565 data is truncated, and the A value specified through the register is added.

Set the DTMD[1:0] bits in the data mode register (VnDMR) to B'01 to specify conversion to ARGB-1555, and specify the A value in the ABIT bit in VnDMR.

16 bits/pixel data (ARGB data) format

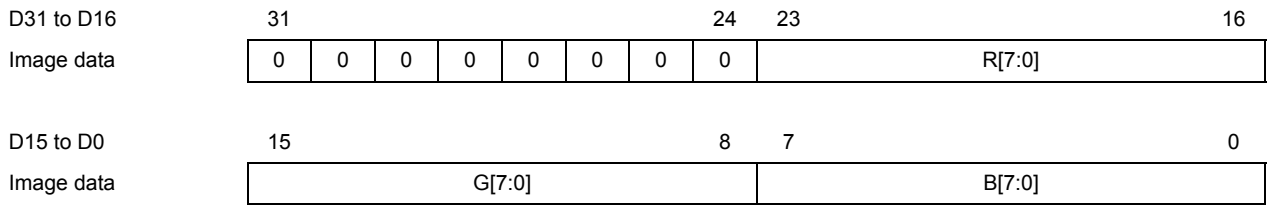
D15 to D0	15	14	10	9	5	4	0
Image data	A	R[4:0]			G[4:0]		B[4:0]



**(7) 32 Bits/Pixel: RGB-888**

The RGB levels are expressed through 8 bits for R, 8 bits for G, and 8 bits for B. Bits 31 to 24 are fixed to 0.

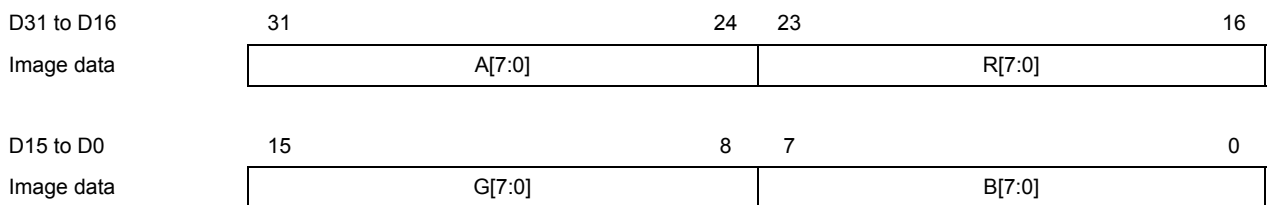
32 bits/pixel data (RGB data) format



**(8) 32 Bits/Pixel: ARGB-8888**

The ARGB levels are expressed through 8 bits for A, 8 bits for R, 8 bits for G, and 8 bits for B. The A value specified by the A8BIT[7:0] bits in VnDMR is set in bits 31 to 24.

32 bits/pixel data (ARGB data) format



### 23.3.12 Endian Conversion

The VIN stores captured data in memory in little endian with the initial settings. Set the EN bit in the main control register (VnMC) to 1 to convert data into big endian before storing in memory.

Endian conversion in word units is controlled through the EN bit in VnMC, and swapping in byte units is controlled through the BPSM bit in the data mode register (VnDMR). For conversion to big endian, specify the BPSM bit as shown in the following table according to the data format specified through the DTMD bits in VnDMR and BPS bit in VnMC.

**Table 23.21 Endian Conversion Unit**

Data Format	BPS in VnMC	DTMD[1:0] in VnDMR	EXRGB in VnDMR	BPSM in VnDMR	Endian Conversion Unit
RGB-565	0	00	0	0	Word units
RGB-888	0	00	1	0	Longword units
YCbCr-422	1	00	0	1	Byte units
ARGB-1555	0	01	0	0	Word units
ARGB-8888	0	01	1	0	Longword units
YC	1	10	0	0	Byte units

The following figures show endian conversions in byte, word, and longword units.

Endian conversion in byte units:

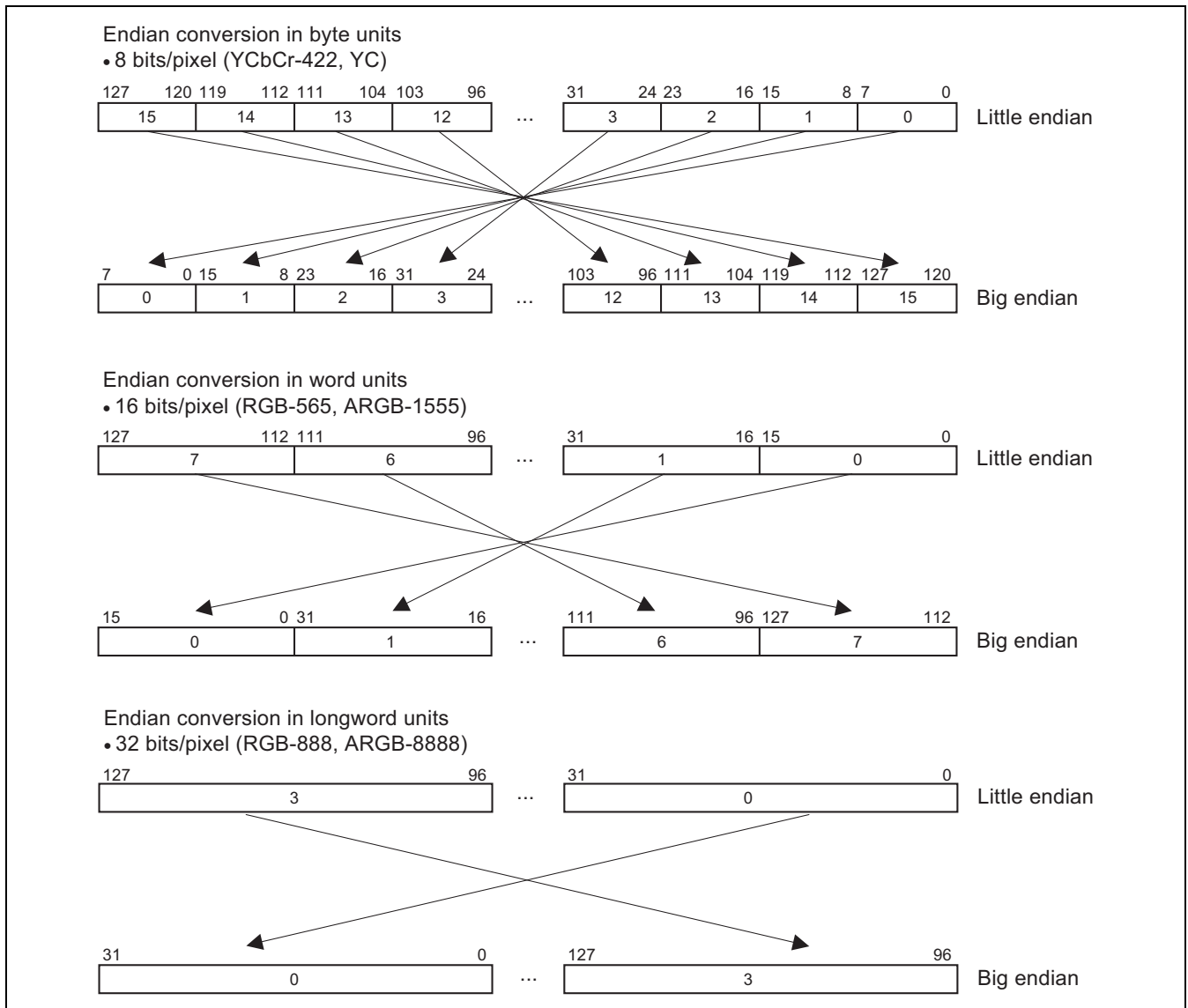


Figure 23.24 Data Alignment Conversion from Little Endian to Big Endian

## 23.4 Usage Notes

### 23.4.1 Module Standby Mode

The LSI supports module standby mode in which clock supply to the VIN is stopped. The video input module should not be accessed during module standby mode.

### 23.4.2 Transition to Module Standby Mode

1. Clear the module enable (ME) bit in the main control register (VnMC) and the continuous frame capture (CC) bit and the single frame capture (SC) bit in the frame capture register (VnFC) to 0 to stop the video input module.
2. Confirm that the capture active (CA) bit in the module status register (VnMS) is cleared to 0.
3. Stop the clock supply.

### 23.4.3 Cancellation of Module Standby Mode and Restarting of Video Input Module

1. Start the clock supply.
2. Set the module enable (ME) bit in the main control register (VnMC) to 1 to start the video input module.
3. Set the continuous frame capture (CC) bit or the single frame capture (SC) bit in the frame capture register (VnFC) to 1.

### 23.4.4 Limitations on Usage

The VIN does not operate correctly in some cases depending on the usage. The following shows cases that require attention.

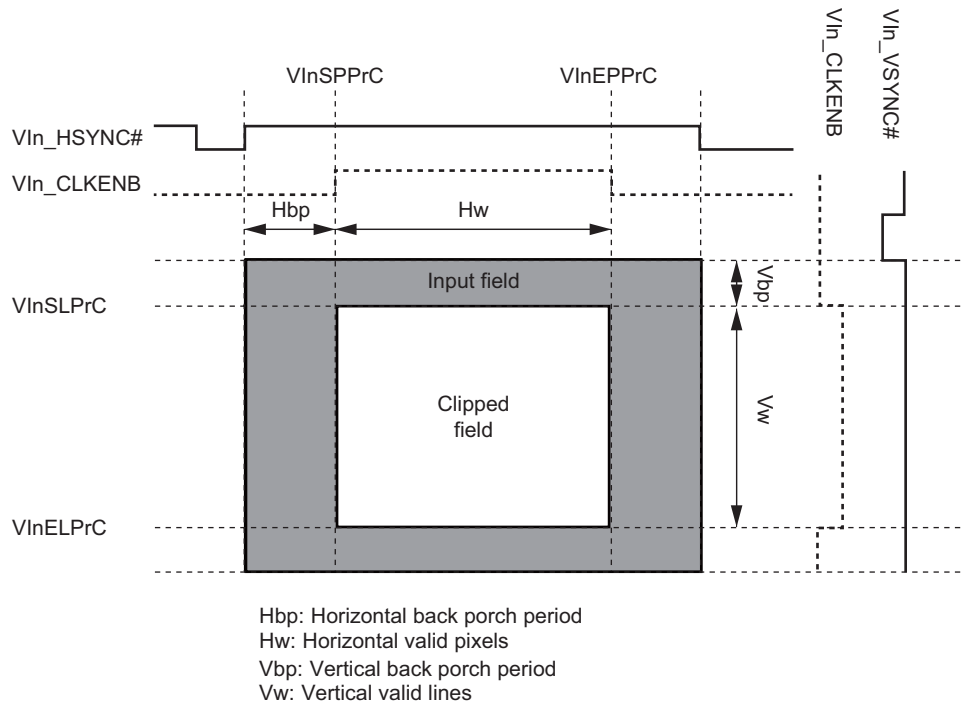
**Table 23.22 Limitations on Usage**

Item	Description	Upper limits on video-clock frequency for this module as a stand-alone unit						
		Horizontal Scaling Ratio XS	VnMC. FAST Mode	Vertical Scaling Ratio YS				
				0.0 ≤ YS ≤ 1.0	1.0 < YS ≤ 2.0	2.0 < YS ≤ 3.0		
Limits on input video clock	The upper limit on frequency of the input video clock varies with the clock mode, capture interface and scaling ratio. The upper limits on frequency of the video clock for this module as a stand-alone unit are shown below. Usage of other modules may make reaching the upper limits impossible. Fully evaluate performance before deciding on the settings for the input video clock, particularly if you are using magnification.	ITU-R BT.601, YCbCr-422, 8 bits	0.0 ≤ XS ≤ 1.0	1	100 MHz	Setting prohibited	Setting prohibited	
				0	80 MHz	80 MHz	80 MHz	
		ITU-R BT.656, YCbCr-422, 8 bits	1.0 < XS ≤ 2.0	1	Setting prohibited	Setting prohibited	Setting prohibited	
				0	70 MHz	70 MHz	50 MHz	
		ITU-R BT.1358, YCbCr-422, 16 bits	0.0 ≤ XS ≤ 1.0	1	100 MHz	Setting prohibited	Setting prohibited	
				0	60 MHz	60 MHz	60 MHz	
		ITU-R BT.601, RGB-888, 12 bits	0.0 ≤ XS ≤ 1.0	1	100 MHz	Setting prohibited	Setting prohibited	
				0	80 MHz	80 MHz	60 MHz	
		ITU-R BT.601, RGB-666, 18 bits	1.0 < XS ≤ 2.0	1	Setting prohibited	Setting prohibited	Setting prohibited	
				0	20 MHz	20 MHz	20 MHz	
		ITU-R BT.601, RGB-888, 24 bits	1.0 < XS ≤ 2.0	1	Setting prohibited	Setting prohibited	Setting prohibited	
				0	20 MHz	20 MHz	20 MHz	
		ITU-R BT.709 interface	When the ITU-R BT.709 interface is in use, the maximum frequency of the video clock is 74.5 MHz.					
		Capture in progressive mode	Use the internal field signal generation function in combination with an input interface in progressive mode.					
Limitation on register update	If a register is updated during capture, data captured immediately after the register update cannot be guaranteed. To update a register which supports the internal update mode as shown in Table 23.9, VIN Registers, specify an internal update for VIN registers by using the MC/VUP bit. To update other registers, stop capture operation and then update them.							
Field capture mode image quality	Images of odd-numbered, odd/even-numbered and even-numbered fields, captured by VnMC/IM interlace mode bit settings, contain every other line from the input interlace images. Therefore, note that the horizontal resolution for video display is in units of fields.							
Full interlace mode image quality	In full interlace composition mode, horizontal stripe noise (such as combing noise) is generated in composite images as fields based on different timelines are combined in memory due to the interlacing method.							
Limitation on vertical scaling	For vertical scaling and full interlace composition, the capture lines are inverted in some cases depending on the scaling ratio because the scaling processing is applied before interlace composition in memory. Be sure to evaluate the image quality before practical application.							
Interrupt event timing	Interrupt event asserted by this module indicates the time when an interrupt event occurs in VIN, not the time when the transfer of capture data to memory is completed.							

Item	Description
Pixel post-clip setting	When the output format is YCbCr-422, after pixel post-clip setting is performed for the clipping data, this data is transferred in YCbCr-422 data format to memory. Therefore, if the EPPoC-SPPoC clipping size is an odd number, it is normalized to an even size which is the sum of that odd number and 1.
Coefficient settings for color space conversion	Specify appropriate values in the color space change coefficient 1 to 3 registers (VnCSCC1 to VnCSCC3) to keep the RGB image data within the range $0 \leq R', G', B' \leq 255$ . After calculation for color space conversion, minus pixel data is normalized to 0 and pixel data more than or equal to 255 is normalized to 255.
Scaling up	When horizontal and vertical scaling up is specified, the amount of memory transfer becomes greater with an increase in traffic. Note the amount of traffic on the entire system when using the scaling-up function because the overall transfer efficiency of the system might degrade due to the increased use of the internal buses.
YC Restrictions on YC separation function	Set the offset register that stores UV data (VnUVAOF) such that the storage areas of Y and UV data are not the same. If the same storage area is set for both data, Y data will be overwritten. It is not allowed to set the YC separate transfer or Y transfer with the vertical scaling-up.
RGB-888→RGB-565 conversion function	In the dithering process by cumulative addition, if the same color is captured as in blue back image, periodic noise may be generated by the cumulative addition process (carried by addition). In this case, set the DC[1:0] bits in VnMC to the ordered dithering.
Video display operation	This module performs capture control based on the external input synchronization signal. Note that it is not synchronous to the timing of frame update set in the Display Unit and thus video display in sync with the capture frame is disabled.  Scaling-up/down process of video capture data via the local video IF can be implemented in conjunction with the IMR-LSX2 module. The following should be noted:  Post-clipping of video capture data is not possible.  Set memory storage data format of this module to YCbCr.  *For data format after LUT conversion, see Table 23.10, Capture Interface Settings, and Table 23.11, Captured Data Formats.  The IMR-LSX2 data is processed based on the synchronization signal from this module. Accordingly, if the scaling-up process is performed on high-definition video input, take the data traffic, memory transfer time and input synchronization signal timing into consideration before using it.  For operation in conjunction with other modules, memory data transfer is performed in the respective modules. If the amount of memory transfer is increased, the internal bus usage is raised, possibly reducing the transfer efficiency of the entire system. For this reason, the amount of traffic for the entire system should be considered in advance.

**Item Description**

The maximum size that can be captured when the HSYNC signal is connected to the VIn\_CLKENB pin (including the case where the CHS bit of the VnDMR2 register is set to 1).



Capture area when the HSYNC signal is connected to the VIn\_CLKENB pin

When the ITU-R BT.601/709/1358 interface is in use, so the HSYNC signal is connected to the VIn\_CLKENB pin (including the case where the CHS bit of the VnDMR2 register is set to 1), the VIN also captures data during the horizontal and vertical back porch periods (Hbp and Vbp). Thus, capturing only the valid data is required by setting the clipping registers as shown below.

- VnSLPrC (start line pre-clip register) = vertical back porch period (Vbp)
- VnELPrC (end line pre-clip register) = vertical back porch period (Vbp) + number of valid lines (Vw) - 1
- VnSPPrC (start pixel pre-clip register) = horizontal back porch period (Hbp)
- VnEPPrC (end pixel pre-clip register) = horizontal back porch period (Hbp) + number of valid pixels (Hw) - 1

The maximum number of lines and pixels that can be captured at this time is as shown below. When this size is exceeded, use the VIN with the data enable signal connected to the VIn\_CLKENB pin.

- The maximum number of lines that can be captured = 2048 (the maximum value of the clipping register) - vertical back porch period (Vbp)
- The maximum number of pixels that can be captured = 2048 (the maximum value of the clipping register) - horizontal back porch period (Hbp)

## 23.5 Supplementary Information

### 23.5.1 Example of Coefficient Set Register Settings for Horizontal Scaling

Table 23.23 shows the example of coefficient set register settings for horizontal (X) scaling (Recommended values).

**Table 23.23 Coefficient Set Register Settings**

- $\alpha = 0.6$  and X Scale (XS) = H'0000 1600

n	CmA	CmB	CmC
1	H'0000 0BDD	H'0000 0BDD	H'0651 9578
2	H'3FF0 07DA	H'0000 0BE3	H'03C2 4973
3	H'3FF0 03D9	H'0000 0BE9	H'01B3 0D5F
4	H'3FFF F7DF	H'0010 03F1	H'0003 C542
5	H'000F DFEC	H'0010 03F7	H'3EC4 711D
6	H'000F C400	H'002F FFFD	H'3DF5 04F1
7	H'001F A81A	H'002F FC00	H'3D95 78C3
8	H'002F 8C3C	H'0010 0000	H'3DB5 C492

- $\alpha = 0.6$  and X Scale (XS) = H'0000 2000

n	CmA	CmB	CmC
1	H'000F A400	H'000F A400	H'0962 5902
2 to 8	H'0000 0000	H'0000 0000	H'0000 0000



## 24. Distortion Correction Engine (IMR-X2)

<b>RZ/G1H</b>	RZ/G1N
RZ/G1M	RZ/G1E

The contents of this section are available upon non-disclosure agreement.

For details, contact your local sales representatives.

## 25. Distortion Correction Engine (IMR-LSX2)

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

The contents of this section are available upon non-disclosure agreement.  
For details, contact your local sales representatives.

## 26. VCP3

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

### 26.1 Overview

The VCP3 is a multi-codec module which provides encoding and decoding capabilities on the basis of multiple video coding schemes, e.g., H.264/AVC, MPEG-4, MPEG-2 and VC-1. This module is a multi codec that processes the frame or each field by controlling software for VCP3 executed on host CPU.

#### 26.1.1 Features

The VCP3 has the following excellent features.

- Support for multiple codecs
  - H.264/MPEG-4 AVC HP (High Profile) and MVC SHP (Stereo High Profile) encoding and decoding
  - H.262/MPEG-2 MP (Main Profile) decoding
  - MPEG-4 ASP (Advanced Simple Profile) decoding
  - VC-1 SP/MP/AP (Simple, Main, Advanced Profile) decoding
  - H.263 Baseline and decoding
  - AVS Jizhun Profile decoding
  - VP8 decoding Support for HDTV resolutions
  - 1,920 pixels × 1,080 lines @ 60 frames/second
- Number of channels
  - Two channels in the RZ/G1H
  - One channel in the RZ/G1M, RZ/G1N, and RZ/G1E
- Data handling on a picture-by-picture basis
  - Encode/decode data one picture (frame or field) at a time.
- High picture quality
  - Support the H.264 high-efficiency coding tools (CABAC, 8 × 8 frequency conversion, and quantization matrix).
  - High-efficiency motion vector detection by a combination of discrete search and trace search
  - Highly efficient real-time intra-prediction by Prediction from Original Image (POI)
  - Optimal-mode selection by Rate-Distortion (RD) cost evaluation
  - Picture quality control based on activity analysis results which match visual models
- Dedicated cache memory for VCP3 is integrated on this LSI. (64 Kbytes)

**Table 26.1 Main Function of VCP3**

Item	Description
Encoding standard supported	<ul style="list-style-type: none"> <li>H.264/AVC High Profile@Level 4.2, Main Profile@Level 4.2, Baseline Profile@Level 3</li> <li>H.264/MVC Stereo High Profile@Level 4.1</li> </ul>
Decoding standard supported	<ul style="list-style-type: none"> <li>H.264/AVC High Profile@Level 4.2, Main Profile@Level 4.2, Baseline Profile@Level 3, Constrained Baseline Profile@Level 4.2 H.264/MVC (Error resilience tools (ASO, FMO, and RS) are not supported.) Stereo High Profile@Level 4.1</li> <li>MPEG-2 Main Profile@High Level</li> <li>MPEG-4 Advanced Simple Profile3@Level 5 (GMC and QMC are not supported), Simple Profile@Level 6</li> <li>VC-1 Simple Profile@Medium Level, Main Profile@High Level, Advanced Profile@Level 3</li> <li>H.263 Baseline@Level 40</li> <li>VP8</li> <li>AVS Jizhun Profile@Level 6.2 (picture format 4:2:0 only)</li> </ul>
Maximum throughput	1,920 × 1,080p, 60 frame In VP8 decoding, the maximum ratio of non-display frame is once every five frames.
Maximum bit rate	80 Mbps (40 Mbps × 2 ch). For MPEG-4 Data Partition, and VP8, the maximum bit rate is 60 (30 Mbps × 2 ch).
Picture size supported	Minimum: Horizontal 80 pixels × Vertical 80 lines (except for H.263), 128 pixels × Vertical 96 lines (H.263) Maximum: Horizontal 1,920 pixels × Vertical 1,088 lines Horizontal size is a multiple of 2 pixels, and vertical size is a multiple of 2 lines. 1,080 × 1,920 and 1,088 × 1,920 are supported.
Color format	YCbCr 4:2:0 format NV12, NV21, YV12 and IYUV are supported.
Bit stream format	Video elementary stream. Table 26.2 shows the range of data which can be encoded and decoded. Function to add/remove the emulation prevention byte in the H.264 VCL-NAL unit. (VCL (Video Coding Layer), NAL (Network Abstraction Layer)) Function to remove the emulation prevention byte in the VC-1 AP bit stream data unit. Function to remove the emulation prevention bit for AVS.
Picture structure	Frame structure and field structure

Item	Description
Motion detection	Motion search accuracy: 1/4 pixels (1/2 pixels for MPEG-2, MPEG-4, and H.263) Motion search range: 1. frame reference Horizontal $\pm$ 64 pixels, Vertical $\pm$ 32 lines 2. frame references (Wide side) Horizontal $\pm$ 48 pixels, Vertical $\pm$ 24 lines (Narrow side) Horizontal $\pm$ 32 pixels, Vertical $\pm$ 16 lines

**Table 26.2 Data Format Handled by the VCP3**

Standard	Encoding Range	Decoding Range
MPEG-4	Not supported	Video packet header/Motion shape texture and subsequent data
H.264	Slice header and subsequent data	Slice header and subsequent data (Except for first slice header in a picture)
H.263	Not supported	Macroblock and subsequent data
MPEG-2	Not supported	Picture data and subsequent data
MPEG-1	Not supported	Picture data and subsequent data
VC-1	Not supported	Slice data and subsequent data
AVS	Not supported	Picture data and subsequent data
VP8	Not supported	Frame header and subsequent data

## 26A. Video Processing Unit Cache (VPC)

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

### 26A.1 Overview

This LSI incorporates cache memory exclusively for use in image reference by the VCP3. This can reduce the amount of bus access for decoding.

#### 26A.1.1 Features

The video processing unit cache (VPC) has the following features.

- 64-Kbyte cache
- Eight-way set-associative cache
- Line size: 64 or 128 bytes
- Number of entries: 128 entry/way (64-byte line size) or 64 entry/way (128-byte line size)
- Exclusively for reading
- FIFO (first-in first-out) replacement algorithm

#### 26A.1.2 Block Diagram

Figure 26A.1 shows connection between VCP3, VPC, and system bus.

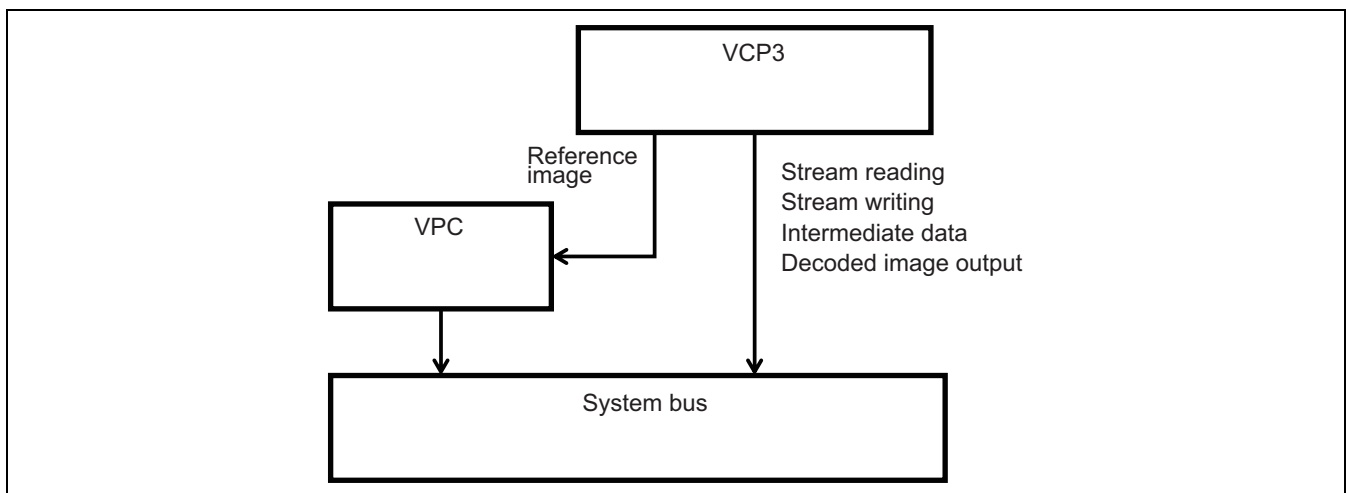


Figure 26A.1 Connection between VCP3, VPC, and System Bus

### 26A.1.3 Register Configuration

Table 26A.1 shows the VPC register configuration and table 26A.2 shows the states of the registers in each of the processing modes. The registers can be accessed only in longwords.

#### Base address:

VPC for VCP ch0 (VPC0\_BASE): H'FE90 8000

VPC for VCP ch1 (VPC1\_BASE): H'FE91 8000 [RZ/G1H only]

**Table 26A.1 Register Configuration**

						<u>RZ/G Series Products</u>			
Register Name	Abbreviation	R/W	Address	Access Size	RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E	
VPC control register	VPCCTL	R/W	VPCn_BASE + H'0004	32	√	√	√	√	
VPC status register	VPCSTS	R	VPCn_BASE + H'0008	32	√	√	√	√	
VPC configuration register	VPCCFG	R/W	VPCn_BASE + H'0078	32	√	√	√	√	
XY setting register for ch0	VPC0XY	R/W	H'FE96 0380	32	√	—	—	—	
XY setting register for ch1	VPC1XY	R/W	H'FE96 0384	32	√	—	—	—	

Note: Do not access addresses other than those listed above. Operations cannot be guaranteed if access is attempted.

**Table 26A.2 States of Registers in Each Processing Mode**

Register Abbreviation	Power-On Reset	Module Standby
All registers	Initialized	Retained

## 26A.2 Register Descriptions

### 26A.2.1 VPC Control Register (VPCCTL)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	F64	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	LWS WAP	—	—	—	—	—	—	—	—	STRIDE	CLR	ENB	
Initial value:	0	0	0	0	1	0	1	0	1	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	All 0	R	Reserved The write value should always be 0.
28	F64	0	R/W	64 Byte/Line Cache Mode When this bit is set to 1, the cache is configured as 64 bytes per line mode. 128 bytes per line mode is selected as initial value setting. On this product, this bit should be set to 1.
27 to 13	—	All 0	R	Reserved The write value should always be 0.
12	LWSWAP	0	R/W	Longword Swap 0: No longword swap 1: Longword swap When 8-, 16-, or 32-byte access is made with this bit set to 1, the read data is swapped in longwords.
11 to 8	—	H'A	R	Reserved Modifying these bits may affect the performance; usually leave the initial value unmodified.
7 to 4	—	H'8	R	Reserved Modifying these bits may affect the performance; usually leave the initial value unmodified.
3, 2	STRIDE	00	R/W	VPC Stride Setting These bits set the stride for VPC operation. 00: 256-byte stride mode 01: 512-byte stride mode 10: 1024-byte stride mode 11: 2048-byte stride mode The VPC access hit ratio depends on this setting; set these bits appropriately for the size to be processed. Note: XY mode case by setting VPCCFG.MODE to 1. Be sure the stride size of VCP3 is same as this setting.



Bit	Bit Name	Initial Value	R/W	Description
1	CLR	0	R/W	<p>VPC Clear</p> <p>Clears the VPC state.</p> <p>0: VPC operates normally.</p> <p>1: VPC is cleared.</p> <p>Before modifying the VPC stride setting, write 1 to this bit to clear the VPC.</p> <p>After the VPC is cleared by writing 1 to this bit, this bit automatically returns to 0.</p>
0	ENB	0	R/W	<p>VPC Enable</p> <p>Enables the VPC.</p> <p>0: Disables the VPC</p> <p>1: Enables the VPC</p> <p>Set this bit to 1 to use the VPC.</p> <p>Do not modify this bit during VCP3 operation; otherwise, correct operation cannot be guaranteed. (Modify this bit after checking the VPCSTS register.)</p>

**26A.2.2 VPC Status Register (VPCSTS)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IDL
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	—	R	Reserved The read value is undefined. The write value should be 0 or 1, which has been read immediately before writing (read-modify-write).
0	IDL	—	R	VPC Idle 0: VPC is operating. 1: VPC is in the idle state. Indicates the VPC processing state. Confirm that this bit is 1 before clearing the cache.

**26A.2.3 VPC Configuration Register (VPCCFG)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	CTLH		CTLW			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	YTLH		YTLW			TL	MODE	
Initial value:	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 22	—	All 0	R	Reserved The write value should always be 0.
21 to 19	CTLH	000	R/W	Tile Height Size Setting for Chroma (CbCr) data 000: 32 001: 64 010: 128 011: 256 100: 512 101: 16 Others: Settings are prohibited.
18 to 16	CTLW	000	R/W	Tile Width Size Setting for Chroma (CbCr) data 000: 32 001: 64 010: 128 011: 256 100: 512 101: 16 Others: Settings are prohibited.
15 to 8	—	H'03	R	Reserved The write value should always be H'03.
7 to 5	YTLH	000	R/W	Tile Height Size Setting for Luminance (Y) data 000: 32 001: 64 010: 128 011: 256 100: 512 101: 16 Others: Settings are prohibited.

Bit	Bit Name	Initial Value	R/W	Description
4 to 2	YTLW	000	R/W	Tile Width Size Setting for Luminance (Y) data 000: 32 001: 64 010: 128 011: 256 100: 512 101: 16 Others: Settings are prohibited.
1	TL	0	R/W	Tile Mode Setting 0: Linear Mode 1: Tile Mode
0	MODE	0	R/W	VPC addressing mode select 0: Linear addressing 1: XY addressing

**26A.2.4 VPC XY Setting for ch0/ch1 (VPCCFG0/1)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	—	—	—

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	STRIDE								AC	—	BT	AD
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 12	—	All 0	R	Reserved The write value should always be 0.
11 to 4	STRIDE	H'00	R/W	This value should always be set as same as VPCCTL.STRIDE.
3	AC	0	R/W	This value should always be set to 0.
2	—	0	R	Reserved. The write value should always be 0.
1	BT	1	R/W	This value should be set based on the value of VPCCFG.MODE VPCCFG.MODE = 1 set this bit to 1. VPCCFG.MODE = 0 set this bit to 0.
0	AD	1	R/W	This value should be set based on the value of VPCCFG.MODE VPCCFG.MODE = 1 set this bit to 1. VPCCFG.MODE = 0 set this bit to 0.

## 26A.3 Operation

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

### 26A.3.1 Initialization

When using the VPC, before accessing the VPC from the VCP3, be sure to make the necessary settings as described in 1 to 4 below.

1. Set the stride and cache line size.
  - Set the stride appropriate for the image size to be processed. (Set as same stride size as VCP3 stride size)
  - The stride can be set using bits 3 and 2 in the VPCCTL register.
  - Set the cache line size to 64 byte / line by setting bit 29 in VPCCTL register to 1.
2. Set the VPC mode
  - Set the VPC mode by setting VPCCFG.MODE.
  - VPCCFG.MODE = 0
    - Set H'0000 0000 to VPCnXY register. (n: 0, 1)
    - Set bits[11:8] in S3CTRL.XYMODECONF to H'F.
  - VPCCFG.MODE = 1
    - Set bits [11:8] in S3CTRL.XYMODECONF to H'F
3. Set the tile size
  - Set appropriate tile size in the VPCCFG register
  - The tile size can be set using bit 21 to 16 and bit 7 to 2 for Chroma data and Luminance data respectively.
3. Clear the VPC.
  - Clear the VPC after confirming that bit 0 in the VPCSTS register is 1.
  - The VPC can be cleared by writing 1 to bit 1 in the VPCCTL register.
4. Enable the VPC.
  - Enable the VPC after confirming that bit 0 in the VPCSTS register is 1.
  - The VPC can be enabled by writing 1 to bit 0 in the VPCCTL register.

### 26A.3.2 Clearing VPC at the Beginning of a Frame

Before accessing the beginning of a frame, clear the VPC following steps 1 and 2 below.

1. Check the status.
  - Confirm that bit 0 in the VPCSTS register is 1.
2. Clear the VPC.
  - Clear the VPC by writing 1 to bit 1 in the VPCCTL register.

## 26A.4 Usage Notes

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

### 26A.4.1 Coherency

At the beginning of a frame, be sure to clear the VPC according to the procedure given in section 26A.3.2, Clearing VPC at the Beginning of a Frame.

### 26A.4.2 Tile Size

Appropriate tile size for this LSI: 128 × 32

# 27. Fine Display Processor (FDP1)

RZ/G1H	RZ/G1N
RZ/G1M	RZ/G1E

## 27.1 Functional Description

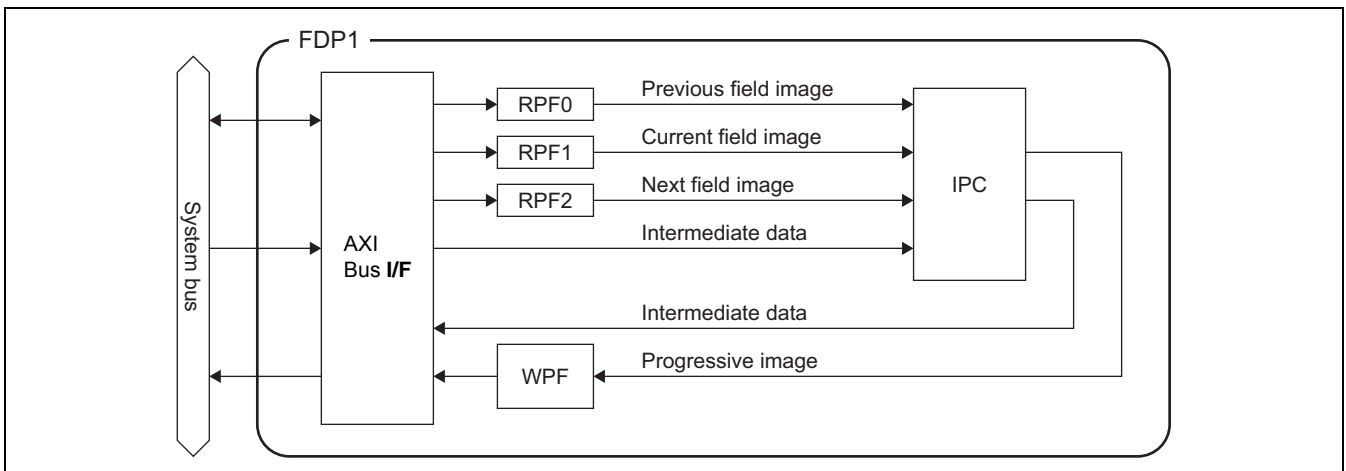
### 27.1.1 Overview

The FDP1 is the de-interlacing module which converts the interlaced video to progressive video. The RZ/G1H provides three channels. The RZ/G1M and RZ/G1N provide two channels and the RZ/G1E provides one channel. This module has the following features.

1. Supports various data formats
  - Input: YCbCr444/422/420
  - Output : YCbCr444/422/420 and RGB/αRGB
2. Full HD video processing performance
  - Can handle conversion from full HD 60i to 60p in operation at 266 MHz.
3. High image-quality de-interlacing algorithm (based only on the luma component)
  - Motion adaptive de-interlacing
  - Accurate still detection
  - Diagonal line interpolation (DLI)

### 27.1.2 FDP1 Architecture

Figure 27.1 shows the block diagram of the FDP1. In this figure, only the luma images are used in processing the images for the previous and next fields.



**Figure 27.1 FDP1 Block Diagram**

The following gives an overview of each block function shown in Figure 27.1. The operation of these functions is determined by the register setting explained in section 27.3. Refer to section 27.3 for the relationship between the register setting and the functional behavior.



**(1) ABI (AXI Bus Interface)**

The FDP1 applies processing to the image data stored in the external memory and writes the resultant data back to the external memory. The data transfer between the external memory and FDP1 necessary for this operation is done by the ABI, which works as the bus master, according to the register settings. The ABI executes this data transfer between the external memory and FDP1.

**(2) RPF (Read Pixel Formatter)**

The RPF reads image data from the external memory through the ABI, unpacks data according to the specified format, and outputs the resultant data to the IPC. The input format unpacking unit expands the image data input from the ABI into the image format for internal processing.

The FDP1 provides three RPF modules (RPF0 to RPF2). RPF0 reads the previous field, RPF1 reads the current field and RPF2 reads the next field for processing de-interlacing operation.

**(3) IPC (Interlace to Progressive Converter)**

The IPC is the de-interlacing module which reads the field image through RPF<sub>n</sub> and writes back the progressive image to the external memory through WPF. The IPC uses the motion adaptive algorithm which enhances the image resolution of still pixels compared with conventional 2D de-interlacing.

Note: Only the luma component is used in the motion adaptive algorithm. The chroma components are still used in conventional 2D de-interlacing.

**(4) WPF (Write Pixel Formatter)**

The WPF is an output module that receives image data from the IPC, converts the color space, number of colors, and format of the data, and outputs the results of FDP1 image processing to external memory through the ABI. The WPF is mainly configured from a color space converter and an output format converter (the packing unit).

The color space converter converts the color space between RGB and YCbCr, and the packing unit converts the format into the picture plane storing format. The FDP1 provides one WPF.

## 27.2 Function List

Table 27.1 shows a functional overview of the FDP1 module.

**Table 27.1 Function List**

<b>Read Pixel Formatter (RPF)</b>			
Number of channels		Three channels (RPF0 to RPF2)	
Image Format	Input* <sup>3</sup>	YCbCr	YCbCr444-PL, SP, ILV* <sup>1</sup> YCbCr422-PL, SP, ILV* <sup>1</sup> YCbCr420-PL, SP* <sup>1</sup>
		Maximum size	H2048 × V2048 pixels (Frame) H2048 × V1024 pixels (Field)
		Minimum size	H80 × V80 pixel (Frame) H80 × V40 pixel (Field)
		Size setting unit	YCbCr420: 2-pixel units both horizontally and vertically. YCbCr422: 2-pixel units horizontally and 1-pixel units vertically. In other formats, the size can be set in 1-pixel units.
<b>Write Pixel Formatter (WPF)</b>			
Number of channels		One channel (WPF)	
Image format	Output	RGB	RGB332, RGB444, RGB565, RGB666, RGB888, $\alpha$ RGB8666, $\alpha$ RGB8888, $\alpha$ RGB4444, $\alpha$ RGB1555 $\alpha$ value is fixed.
		YCbCr	YCbCr444-PL, SP, ILV* <sup>1</sup> YCbCr422-PL, SP, ILV* <sup>1</sup> YCbCr420-PL, SP* <sup>1</sup>
		Maximum size	H2048 × V2048 pixels
		Minimum size	H80 × V80 pixel
		Size setting unit	YCbCr420: 2-pixel units both horizontally and vertically. YCbCr422: 2-pixel units horizontally and 1-pixel units vertically. In other formats, the size can be set in 1-pixel units.
Color space conversion	YCbCr to RGB	Conversion expression	BT.601 (16, 235/240) to RGB (0, 255) BT.709 (16, 235/240) to RGB (0, 255) BT.601 (0, 255) to RGB (0, 255) BT.709 (16, 235/240) to RGB (16, 235)
Changing number of colors	Output	Reducing RGB color depth	Dithering, lower-order bit truncation, or rounding
		YCbCr422/420	CbCr skipping or CbCr vertical skipping and horizontal skipping

**Interlace to Progressive Converter (IPC)**

De-interlacing	Mode	Frame rate	Equal rate (60i to 60p) Half rate (60i to 30p)
		Interpolation (luma)	2D-3D adaptive* <sup>2</sup> 2D fixed 3D fixed* <sup>2</sup>
		Interpolation (chroma)	2D fixed
		Algorithm	Motion adaptive (luma only)
Diagonal line interpolation		Supported (luma only)	

Notes: 1. PL: Planar, SP: Semi-planar, ILV: Interleaved

2. Source picture structures (field-structure or frame-structure) should be the same structure among the all input pictures.
3. In processing by RPF0 and RPF2, the chroma components (Cb and Cr, or U and V) are not read from the system bus when the format is planar or semi-planar. The chroma components are discarded once they are read in combination with the luma components when the format is interleaved because the RPF0 and RPF2 only handle fixed 2D de-interlacing of the luma components, and so do not require the chroma components.

## Preface

Definition of operators and functions

The following operators, notations are defined for explaining the functions of the FDP1.

$\langle x \rangle$

Discard decimal places of value x

H'

The notation “H” is used as prefix for hexadecimal numbers. For example, H'80 means 80 in hexadecimal and 128 in decimal.

B'

The notation “B” is used as prefix for binary numbers. For example, B'10000000 means 80 in hexadecimal and 128 in decimal. When a number is used without prefix, it means decimal number.

–

The notation “\_” is used as a separator of binary digit for binary number. There is no functional and logical meaning. The meaning of B'10101 and B'1\_0101 is the same.

[msb:lsb]

This notation specifies a part of bits or all bits of registers and signals. For example, eval[3:0] means bits 3 to 0 of the signal or register whose name is “eval”.

clip0 (x)

Clip to 0 value if x is less than 0. [  $x = (x < 0) ? 0 : x$  ]

clip3 (min., max., x)

The value x shall be clipped so that x shall be min. < x < max. [  $x = (x < \text{min}) ? \text{min} : ((x > \text{max}) ? \text{max} : )$  ]

## Unit

The unit is defined here for explaining FDP1's functions.

[bpp]: bits per pixel

The FDP1 can handle a number of image formats. Each image format has different number of data bits. The unit [bpp] shows a number of data bits for one pixel. For example, RGB 8 bpp means that its format is RGB and the pixel consists of 8 data bits.

## 27.3 Registers

### 27.3.1 Access Restrictions

FDP1 supports only 32-bit access to read or write all addresses in FDP1 area. Do not access any of otherwise access units.

### 27.3.2 Register Type Definitions

There are 3 types of registers in FDP1: immediate register, V-update Register and V-update Status Register. The values of immediate registers are reflected to H/W behavior immediately after the changing its values. Hence, do not change these immediate registers while FDP1 is processing unless this manual allows it explicitly. The values of V-update registers are reflected to H/W behavior at the timing of V-interruption (at the timing of FD1\_CTL\_IRQSTA.VINT is set to 1). Users can change these V-update registers while FDP1 is processing. To reflect V-update registers to the H/W, users have to set FD1\_CTL\_REGEND.REGEND to 1 after the all V-update registers which are intended to be changed are completely set. The values of V-update Status Registers are updated at the timing of V-interruption. Therefore, the status (FD1\_CTL\_STATUS) of de-interlacing process which is conducted before a V-interruption must be referred after that V-interruption.

To confirm the types of registers, refer to Table 27.4.

### 27.3.3 Notational Conventions for Registers and Bit Fields

This document uses the following notational conventions for the FDP1 registers and bit fields.

1. The names of registers and bits are written in uppercase.
2. A bit or bit field in a register is indicated as [register name.bit name]. For example, the STRCMD bit in the FD1\_CTL\_CMD register is indicated as FD1\_CTL\_CMD.STRCMD.
3. Lowercase "n" in a register name or a bit name indicates an integer and the range of value n is defined when necessary. For example, FD1\_RPFn\_ADDR\_Y.PSRC\_ADDR (n = 0, 1, 2) indicates the PSRC\_ADDR bits in three registers FD1\_RPF0\_ADDR\_Y.PSRC\_ADDR and FD1\_RPF1\_ADDR\_Y.PSRC\_ADDR, and FD1\_RPF2\_ADDR\_Y.PSRC\_ADDR. For RPFn when the range of value n is not defined, RPFn (n = 0, 1, 2) are assumed.
4. In each subsection for register description in section 27.3, when only a bit name is written without showing its register name, the bit is in the register described in that subsection.
5. A wildcard (\*) indicates any characters in a name and represents all registers or bits that match the specified first part of a name. For example, when there are three registers FD1\_RPF0\_ADDR\_Y, FD1\_RPF1\_ADDR\_C0 and FD1\_RPF1\_ADDR\_C1, FD1\_RPF1\_ADDR\_\* indicates three registers.

### 27.3.4 Register Configuration

The FDP1 registers are arranged in the following order; the general control registers control the operation of the entire FDP1, and the other registers control each image processing and specify parameters for the processing. The functions of the registers are described in this order starting from section 27.3.7.

1. General control registers (FD1\_CTL\_\*)
2. RPF control registers (FD1\_RPF\_\*)
3. WPF control registers (FD1\_WPF\_\*)
4. IPC control registers (FD1\_IPC\_\*)

### 27.3.5 Restrictions on Access to Registers and Lookup Tables

The FDP1 has control registers and lookup tables. When accessing the addresses where these registers and lookup tables are allocated, the following restrictions should be satisfied. If any restriction is violated, the FDP1 will not operate correctly.

1. For the read-only bits and reserved bits in all FDP1 registers, writing 1 is prohibited unless otherwise specified.
2. Addresses undefined in section 27.3.7, Memory Map, are reserved areas and write access is prohibited in these areas.
3. For all immediate registers and lookup tables, except FD1\_CTL\_SGCMD, FD1\_CTL\_SRESET and FD1\_CTL\_IRQ\*, modifying register values during operation of the module is prohibited. Modify registers while the FDP1 is stopped. For the operating status of the FDP1, refer to section 27.3.8.8.

### 27.3.6 Procedure of FDP1 Start and Stop

#### 27.3.6.1 Register usages for FDP1 Start and Stop

Registers FD1\_CTL\_CMD, FD1\_CTL\_SGCMD, and FD1\_CTL\_REGEND must be used correctly in the procedures of FDP1 start and stop as specified in Tables 27.2 and 27.3.

**Table 27.2 Register Usages for Starting FDP1**

Register	Start the First Frame (FR[0])	Start the Second or Later Frame (FR[f], f = 1, 2, 3, ...)
FD1_CTL_SGCMD.SGEN	After all registers have been set completely, it must be set as 1 to generate V-Interruption.	It must be kept as 1 from the previous frame FR[f-1].
FD1_CTL_REGEND.REGEND	After all registers except FD1_CTL_SGCMD.SGEN have been set completely, it must be set 1. As the results, at the first V-interruption, all V-update registers are reflected for hardware reference, FD1_CTL_CMD.STRCMD is referred to start the first frame.	After V-interruption of starting the previous frame FR[f-1], it must be set 1 after all registers about FR[f] have been set completely. As the results, at the V-interruption of the end of frame FR[f-1], the V-update registers will be reflected to hardware reference, FD1_CTL_CMD.STRCMD is referred to start the frame FR[f].
FD1_CTL_CMD.STRCMD	It must be set 1 when all registers except FD1_CTL_SGCMD.SGEN, FD1_CTL_REGEND.REGEND are set. At the first V-Interruption it is referred by hardware to start the frame.	It must be set 1 when all registers except FD1_CTL_REGEND.REGEND are set. At the next V-Interruption (boundary between FR[t-1] and FR[t]) it is referred by hardware to start the frame.

**Table 27.3 Register Usages for Stopping FDP1**

Register	Stopping Immediately by Software Reset	Stopping after Current Process Finished
FD1_CTL_SGCMD.SGEN	It must be cleared before setting the value of FD1_CTL_SRESET.SRST as 1 so that no more V-Interruption after FDP1 stopped.	After V-interruption at the final frame end (FD1_CTL_IRQSTA.FRE is set as 1) occurred, it must be cleared so that no more V-Interruption is generated after FDP1 stopped
FD1_CTL_REGEND.REGEND		No Interrupt Mode  After V-interruption of starting the final frame, it must be set 1 right after clearing FD1_CTL_CMD.STRCMD so that the final V-interruption occurs and operation status of the final frame is updated to V-update status registers for Software reference.  Other modes  Right after V-interruption at starting the final frame, it must be set 1 right after clearing FD1_CTL_CMD.STRCMD so that operation status of the final frame is updated to V-update status registers for Software reference.
FD1_CTL_CMD.STRCMD	After FDP1 stopped successfully (FD1_CTL_IRQSTA.FRE is set as 1), it must be cleared to prevent wrong operation when the FDP1 is restarted.	After V-interruption of starting the final frame, it must be cleared to prevent wrong operation when the FDP1 is restarted.

### 27.3.6.2 Register Setting Order for FDP1 Start and Stop

#### (1) Interrupt Mode or Best Effort Mode

##### (a) To start the first frame of FDP1 process, set registers in following order.

1. Set all registers other than FD1\_CTL\_CMD, FD1\_CTL\_SGCMD, and FD1\_CTL\_REGEND.  
Set FD1\_CTL\_CMD.STRCMD to the value 1.
2. Set FD1\_CTL\_REGEND.REGEND to the value 1.
3. Set FD1\_CTL\_SGCMD.SGEN to the value 1, then FDP1 starts its process. FD1\_CTL\_SGCMD.SGEN must be not cleared to continue the second or later frames.

##### (b) To start the second or later frame, set registers in following order:

1. After V-interruption of the previous frame start timing occurred, set all registers other than FD1\_CTL\_CMD and FD1\_CTL\_REGEND.
2. Set FD1\_CTL\_CMD.STRCMD to the value 1.
3. Set FD1\_CTL\_REGEND.REGEND to the value 1.
4. At the V-interruption of the previous frame end timing, FDP1 starts the target frame. The V-interruption of the previous frame end timing and the one of the target frame start timing are the same.

##### (c) To stop FDP1 operation after currently frame finished, set registers as the following.

1. After V-interruption of the current frame start timing occurred, set FD1\_CTL\_CMD.STRCMD to the value 0. Set FD1\_CTL\_REGEND.REGEND to the value 1. If this register was completed before the V-Interruption of frame end timing, FDP1 stops its operation and currently frame becomes the last frame of the image sequence. If these register setting could not be completed before the V-Interruption of frame end timing, FDP1 stops its operation in the next V-

interruption. In the latter case, V-update status registers are not updated at V-interruption of frame end but at the next V-interruption at which DF1\_CTL\_REGEND.REGEND is set as 1.

2. Set FD1\_CTL\_SGCMD.SGEN to the value 0, then FDP1 will stop generating V-interruption.

**(d) To stop FDP1 operation immediately, set registers as the following.**

1. Set FD1\_CTL\_SGCMD.SGEN to the value 0, then FDP1 will stop generating V-interruption.
2. Set FD1\_CTL\_SRESET.SRST to the value 1. FDP1 will invoke termination process immediately.
3. Wait frame end interrupt from FDP1 or until the register bit FD1\_CTL\_IRQSTA.FRE is set to 1. After it occurs, FDP1 have finished its processing. With this operation, FDP1 can stop its process quickly, but the output frame of the last frame is corrupted.

**(2) No interrupt mode**

**(a) To start the first frame, set registers in following order.**

Same as (1) (a).

**(b) To start the second or later frame, set registers in following order.**

Same as (1) (b).

**(c) To stop FDP1 operation after current frame finished, set registers as the following.**

1. After V-interruption of the current frame start timing occurred, set FD1\_CTL\_CMD.STRCMD to the value 0.
2. Set FD1\_CTL\_REGEND.REGEND to the value 1. At the V-Interruption of frame end timing, FDP1 stops its operation and current frame becomes the last frame of the image sequence.
3. Set FD1\_CTL\_SGCMD.SGEN to the value 0, then FDP1 will stop generating V-interruption.

**(d) To stop FDP1 operation after current frame finished, set registers as the following.**

Same as (1) (d).



### 27.3.7 Memory Map

Table 27.4 shows the FDP1 memory map. Immediate registers are specified as “Imm”, the V-update registers are indicated as “Vupdt” and the V-update status registers are indicated as “VupdtSt” in register type column in Table 27.4.

#### Base address of each FDP1:

Ch0: H'FE94 0000

Ch1: H'FE94 4000 [RZ/G1H/M/N only]

Ch2: H'FE94 8000 [RZ/G1H only]

**Table 27.4 FDP1 Memory Map**

Space	Register Type	Register Name	Abbreviation	Relative Address	Register Type	RZ/G Series Products			
						RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Register	General control registers	FDP1 Start Register	FD1_CTL_CMD	H'0000	Imm	√	√	√	√
		Sync Generator Register	FD1_CTL_SGCMD	H'0004	Imm	√	√	√	√
		Register Set End Register	FD1_CTL_REGEND	H'0008	Imm	√	√	√	√
		Channel Activation Register	FD1_CTL_CHACT	H'000C	Vupdt	√	√	√	√
		Operation Mode Register	FD1_CTL_OPMODE	H'0010	Vupdt	√	√	√	√
		V-Period Register	FD1_CTL_VPERIOD	H'0014	Vupdt	√	√	√	√
		Software Reset Register	FD1_CTL_SRESET	H'001C	Imm	√	√	√	√
		Operating Status Register	FD1_CTL_STATUS	H'0024	VupdtSt	√	√	√	√
		V-Cycles Status Register	FD1_CTL_VCYCLE_STAT	H'0028	VupdtSt	√	√	√	√
		Interrupt Enable Register	FD1_CTL_IRQENB	H'0038	Imm	√	√	√	√
		Interrupt Status Register	FD1_CTL_IRQSTA	H'003C	Imm	√	√	√	√
		RPF control registers		Source Picture Size Register	FD1_RPF_SIZE	H'0060	Vupdt	√	√
Source Picture Format Register	FD1_RPF_FORMAT			H'0064	Vupdt	√	√	√	√
Source Picture Stride Register	FD1_RPF_PSTRIDE			H'0068	Vupdt	√	√	√	√
RPFn Source Component-Y Address Register (n = 0, 1, 2)	FD1_RPFn_ADDR_Y			H'006C + H'C × n	Vupdt	√	√	√	√
RPF1 Source Component-C0 Address Register	FD1_RPF1_ADDR_C0			H'007C	Vupdt	√	√	√	√
RPF1 Source Component-C1 Address Register	FD1_RPF1_ADDR_C1			H'0080	Vupdt	√	√	√	√
Still Mask Address Register	FD1_RPF_SMSK_ADDR			H'0090	Vupdt	√	√	√	√
RPF Data Swap Register	FD1_RPF_SWAP			H'0094	Vupdt	√	√	√	√

Space	Register Type	Register Name	Abbreviation	Relative Address	Register Type	RZ/G Series Products			
						RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Register	WPF control registers	Destination Picture Format Register	FD1_WPF_FORMAT	H'00C0	Vupdt	√	√	√	√
		Destination Picture Rounding Control Register	FD1_WPF_RNDCTL	H'00C4	Vupdt	√	√	√	√
		Destination Picture Stride Register	FD1_WPF_PSTRIDE	H'00C8	Vupdt	√	√	√	√
		Destination Component-Y Address Register	FD1_WPF_ADDR_Y	H'00CC	Vupdt	√	√	√	√
		Destination Component-C0 Address Register	FD1_WPF_ADDR_C0	H'00D0	Vupdt	√	√	√	√
		Destination Component-C1 Address Register	FD1_WPF_ADDR_C1	H'00D4	Vupdt	√	√	√	√
		WPF Data Swap Register	FD1_WPF_SWAP	H'00D8	Vupdt	√	√	√	√
IPC control registers	IPC Mode Register	FD1_IPC_MODE	H'0100	Vupdt	√	√	√	√	
	Still Mask Threshold Register	FD1_IPC_SMSK_THRESH	H'0104	Vupdt	√	√	√	√	
	Comb Detection Parameter Register	FD1_IPC_COMB_DET	H'0108	Vupdt	√	√	√	√	
	Motion Decision Parameter Register	FD1_IPC_MOTDEC	H'010C	Vupdt	√	√	√	√	
	DLI Blend Parameter Register	FD1_IPC_DLI_BLEND	H'0120	Vupdt	√	√	√	√	
	DLI Horizontal Frequency Gain Register	FD1_IPC_DLI_HGAIN	H'0124	Vupdt	√	√	√	√	
	DLI Suppression Parameter Register	FD1_IPC_DLI_SPRS	H'0128	Vupdt	√	√	√	√	
	DLI Angle Parameter Register	FD1_IPC_DLI_ANGLE	H'012C	Vupdt	√	√	√	√	
	DLI Isolated Pixel Parameter Register 0	FD1_IPC_DLI_ISOPIX0	H'0130	Vupdt	√	√	√	√	
	DLI Isolated Pixel Parameter Register 1	FD1_IPC_DLI_ISOPIX1	H'0134	Vupdt	√	√	√	√	
	IPC Sensor Threshold Register 0	FD1_IPC_SENSOR_TH0	H'0140	Vupdt	√	√	√	√	
	IPC Sensor Threshold Register 1	FD1_IPC_SENSOR_TH1	H'0144	Vupdt	√	√	√	√	
	Sensor Control Register 0	FD1_SENSOR_CTL0	H'0170	Vupdt	√	√	√	√	
	Sensor Control Register 1	FD1_SENSOR_CTL1	H'0174	Vupdt	√	√	√	√	
	Sensor Control Register 2	FD1_SENSOR_CTL2	H'0178	Vupdt	√	√	√	√	
Sensor Control Register 3	FD1_SENSOR_CTL3	H'017C	Vupdt	√	√	√	√		

Space	Register Type	Register Name	Abbreviation	Relative Address	Register Type	RZ/G Series Products			
						RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Register	IPC control registers	Sensor Register m (m= 0 to 17)	FD1_SENSOR_m	H'0180 + H'4 × m	—	√	√	√	√
		Line Memory Pixel Number Register	FD1_IPC_LMEM	H'01E0	—	√	√	√	√
		IP Internal Data Register	FD1_IP_INDATA	H'0800	—	√	√	√	√
LUT	DIF_ADJM		FD1_DIF_ADJ_00	H'1000		√	√	√	√
			↓	↓					
			FD1_DIF_ADJ_FF	H'13FF					
	SAD_ADJ		FD1_SAD_ADJ_00	H'1400		√	√	√	√
			↓	↓					
			FD1_SAD_ADJ_FF	H'17FF					
	BLD_GAIN		FD1_BLD_GAIN_00	H'1800		√	√	√	√
			↓	↓					
			FD1_BLD_GAIN_FF	H'1BFF					
	DIF_GAIN		FD1_DIF_GAIN_00	H'1C00		√	√	√	√
			↓	↓					
			FD1_DIF_GAIN_FF	H'1FFF					
MDET		FD1_MDET_00	H'2000		√	√	√	√	
		↓	↓						
		FD1_MDET_FF	H'23FF						

### 27.3.8 General Control Registers

#### 27.3.8.1 FDP1 Start Register (FD1\_CTL\_CMD)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	STR CMD
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	STRCMD	0	R/W	Start Command FDP1 starts the de-interlacing processing if this bit is set to 1. Set this bit after all relevant registers are surely set except for FD1_CTL_REGEN and FD1_CTL_SGCM. Set this bit to 1 before the FD1_CTL_REGEN.REGEN and FD1_CTL_SGCM. if FDP1 has to execute process. This bit will keep the value 1 after the set. To clear this bit, write the value 0 to this bit. 0: NOP or stops process at the next timing of V-Interruption. 1: Start FDP1 process at the next timing of V-Interruption. Note that setting of this registers are valid if the register FD1_CTL_REGEN.REGEN is set to the value 1 at the timing of next V-Interruption.

**27.3.8.2 Sync Generator Register (FD1\_CTL\_SGCMD)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SGEN
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	SGEN	0	R/W	<p>V-Interruption Generator Enable</p> <p>This bit controls V-Interruption. This bit should be set to the value 1 after other all registers are set, and only at the first field of the sequence.</p> <p>Set this bit to the value 1 to execute process in all V-Interruption modes described in section 27.3.8.5.</p> <p>0: Disable V-Interruption 1: Enable V-Interruption</p> <p>[Important]</p> <p>In case of software reset (FD1_CTL_SRESET.SRST), set this SGEN bit to the value 0.</p> <p>If this bit is cleared during process V-interruption will not occur after FDP1 finished current frame. As a result, FDP1 will not start the next frame because STRCMD is not captured and V-update status registers will not be updated about process information of current frame.</p>

**27.3.8.3 Register Set End Register (FD1\_CTL\_REGEND)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	REG END
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	REGEND	0	R/W	Register Setting Ready Flag Set the value 1 to this bit after complete the setting of parameter registers. Do not write the value 0 to this bit. This bit will be cleared by FDP1 automatically. 0: <u>Writing 0 is prohibited</u> except for after the completion of S/W reset sequence. 1: Registers which are set by SW is ready to be reflected for Hardware reference. The V-update status registers is ready to be reflected for Software reference. The second or later V-interruption in the case No interrupt mode can be generated.

**27.3.8.4 Channel Activation Register (FD1\_CTL\_CHACT)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	SMW	WR	—	—	—	—	SMR	RD[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9	SMW	0	R/W	Refer to Table 27.5 for setting these register fields. The setting of each register field depends on the setting of FD1_IPC_MODE.DIM register bits. Do not set the other values which are specified in Table 27.5.
8	WR	0	R/W	
7 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3	SMR	0	R/W	Refer to Table 27.5 for setting these register fields. The setting of each register field depends on the setting of FD1_IPC_MODE.DIM register bits. Do not set the other values which are specified in Table 27.5.
2 to 0	RD[2:0]	000	R/W	

**Table 27.5 FD1\_CTL\_CHACT Setting for FD1\_IPC\_MODE.DIM Parameter**

PRG*1	DIM[2:0]*2		SMW	WR	SMR	RD2	RD1	RD0	LWord Expression
0 (Interlace Mode)	B'000 (Adaptive2D/3D)	First field	1	1	0	0	1	0	H'0000_0302
		Second field	1	1	0	1	1	1	H'0000_0307
		Final field	0	1	0	0	1	0	H'0000_0102
		Otherwise	1	1	1	1	1	1	H'0000_030F
	B'010 (Fixed 3D)	First field	0	1	0	0	1	0	H'0000_0102
		Second field	0	1	0	1	1	1	H'0000_0107
		Final field	0	1	0	0	1	0	H'0000_0102
		Otherwise	0	1	0	1	1	1	H'0000_0107
B'001 (Fixed 2D)		0	1	0	0	1	0	H'0000_0102	
B'011 (Previous field)		0	1	0	0*3	1	1	H'0000_0103	
B'100 (Next field)		0	1	0	1	1	0*3	H'0000_0106	
1 (Progressive Mode)	Set DIM [2:0] as B'001		0	1	0	0	1	0	H'0000_0102

Notes: Field order means an input field order to the FDP1.

For example, the first field is the first input field to the FDP1; the first field is processed but not output.

1. FD1\_CTL\_OPMODE.PRG

2. FD1\_CTL\_IPC\_MODE.DIM[2:0]
3. Value 1 can be set but the corresponding data is not read

### 27.3.8.5 Operation Mode Register (FD1\_CTL\_OPMODE)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

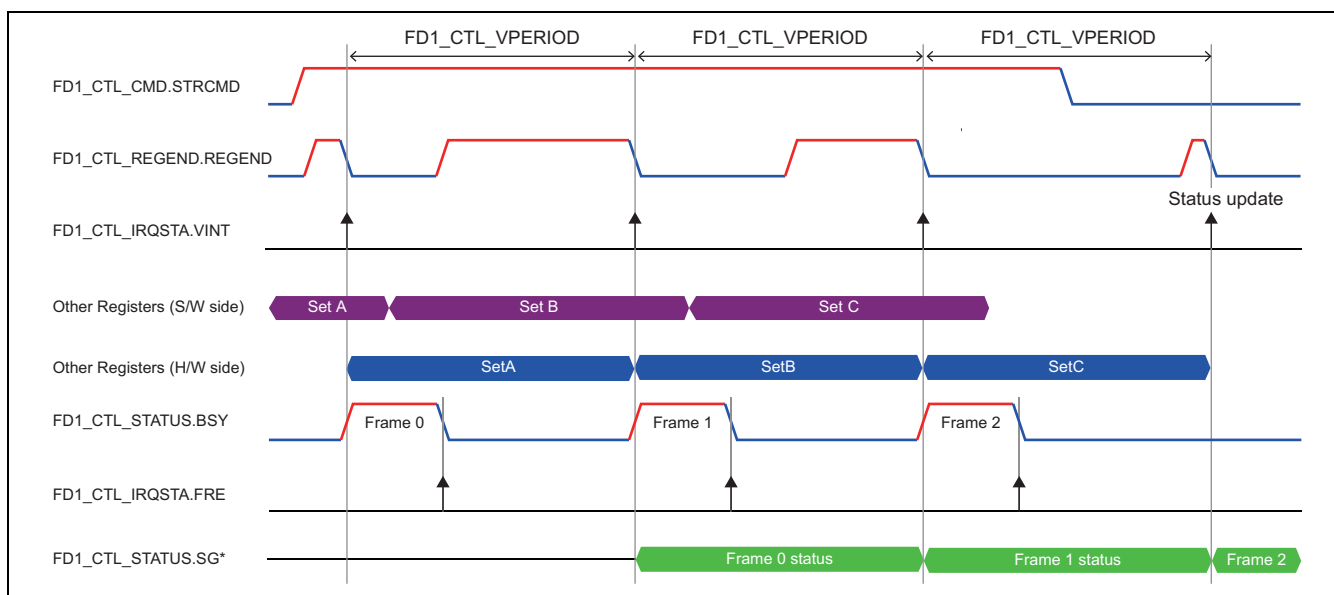
Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	PRG	—	—	VIMD[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	PRG	0	R/W	Progressive Mode When the register field is set to 1, the de-interlacing processing is not executed and the incoming image data is passed through IPC module. 0: Interlace Mode 1: Progressive Mode
3, 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1, 0	VIMD[1:0]	00	R/W	V-Interruption Mode This register field sets V-Interruption mode of FDP1. Refer to Table 27.6 for detail. 00: Normal 01: Best Effort 10: No interrupt



**Table 27.6 V-Interruption Mode**

VIMD[1:0]	V-Interruption Mode Timing		STRCMD Captured Timing
	First Time	Second Time or Later	
B'00 (Normal)	V-Interruption occurs when changes FD1_CTL_SGCMD.SGEN from 0 to 1 and FDP1 is not doing de-interlacing process.	Fixed period interrupt specified by FD1_CTL_VPERIOD in spite of the de-interlacing processing.	Captured at V-Interruption
B'01 (Best effort)		Fixed period interrupt specified by FD1_CTL_VPERIOD  If the de-interlacing processing is not completed at the timing specified by FD1_CTL_VPERIOD, V-Interruption is deferred to the end of the processing.	
B'10 (No interrupt)		If FD1_CTL_REGEND is set 1 before the end of the processing (frame end interruption FD1_CTL_IRQSTA .FRE is set as 1) V-Interruption occurs right after the end of the processing.  If FD1_CTL_REGEND is set 1 after the end of processing (frame end interruption FD1_CTL_IRQSTA .FRE is set as 1) V-Interruption occurs right after FD1_CTL_REGEND is set.  If FD1_CTL_REGEND is not set 1 V-Interruption does not occur.	



**Figure 27.2 Timing Chart of Normal Mode (VIMD = 0) and Best Effort Mode (VIMD = 1)**

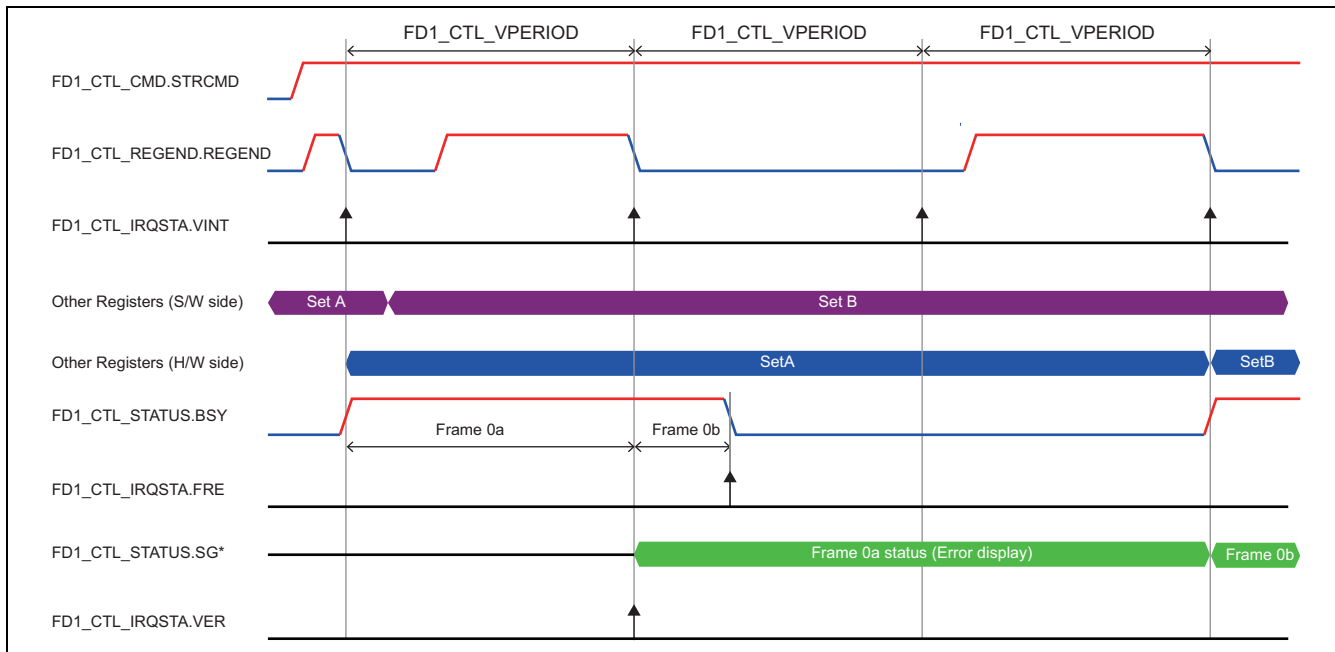


Figure 27.3 Timing Chart of Normal Mode (VIMD = 0) with Error

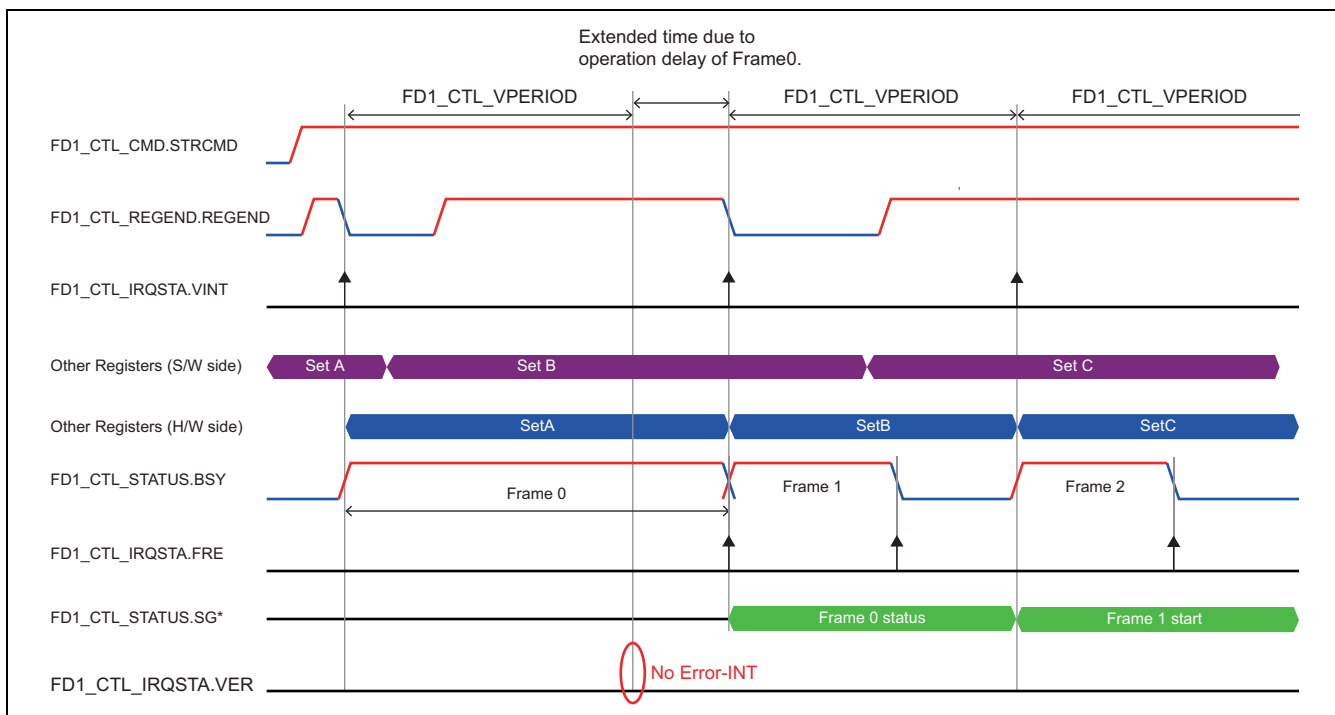


Figure 27.4 Timing Chart of Best Effort Mode (VIMD = 1) (in Case of Error at Normal Mode)

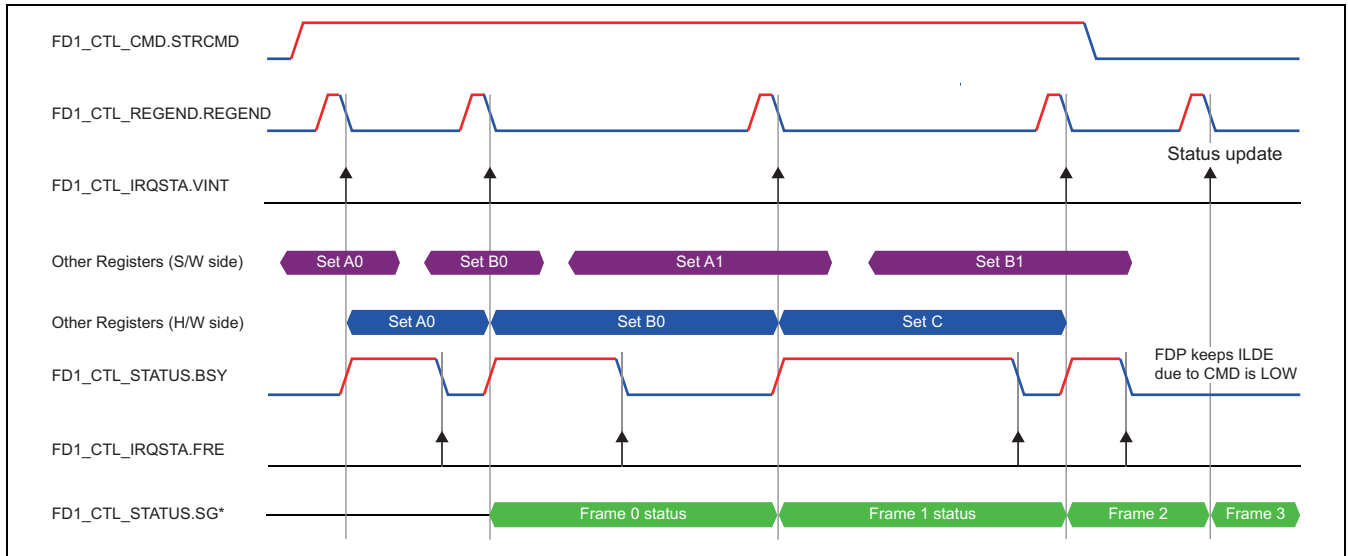
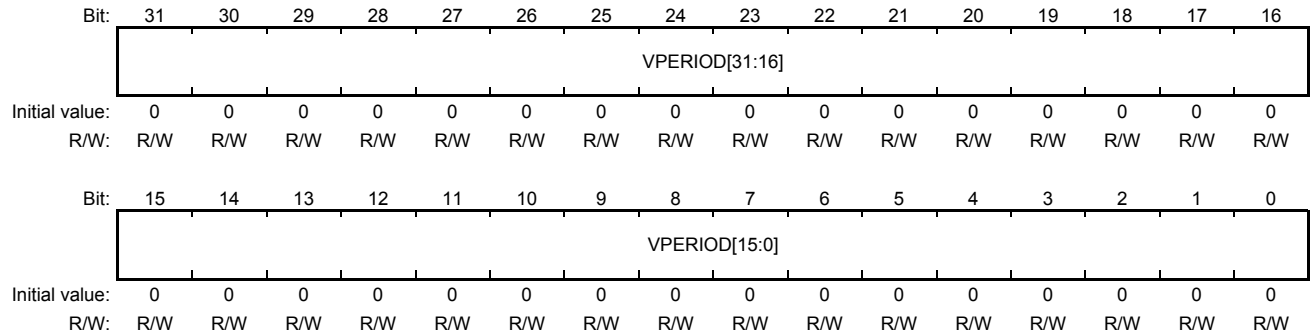


Figure 27.5 Timing Chart of No Interrupt Mode (VIMD = 2)

**27.3.8.6 V-Period Register (FD1\_CTL\_VPERIOD)**

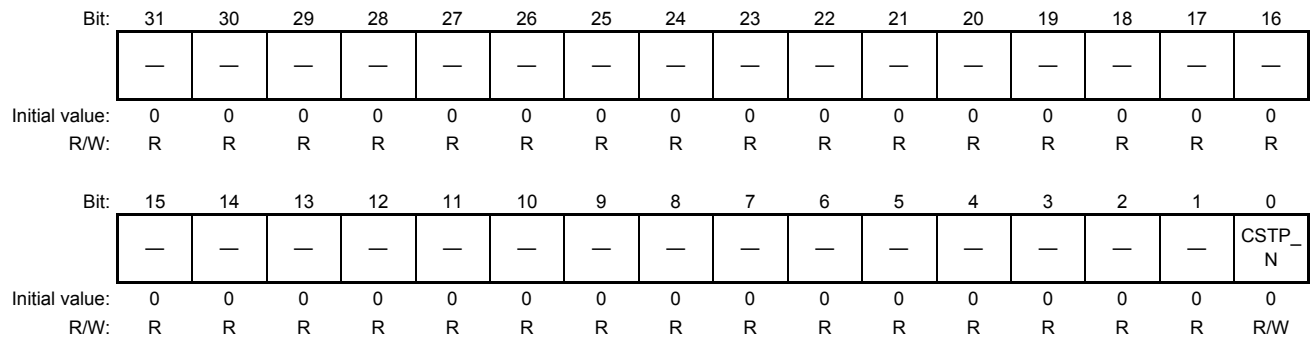
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	VPERIOD [31:0]	All 0	R/W	V-Sync Period Set the period from the V-Sync to the next V-Sync in the unit of FDP1 clock frequency cycles.

**27.3.8.7 Clock Control Register (FD1\_CTL\_CLKCTRL)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√



Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are read as 0. The write value should be 0.
0	CSTP_N	0	R/W	Set the value 1 to this bit

**27.3.8.8 Software Reset Register (FD1\_CTL\_SRESET)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SRST
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	SRST	0	R/W	<p>FDP1 Software Reset</p> <p>FDP1 stops its operation after this bit is set to 1. FDP1 aborts all processings and quits bus/memory accesses. Do not start next process by FD1_CTL_CMD until the software processing is completed. When this processing is completed, the FD1_CTL_IRQSTA.FRE interrupt source bit is set to 1, when the FRE interrupt is enabled. This interrupt notifies the end of the reset processing.</p> <p>The end of software reset processing is notified through the FRE bit, but the software reset issued while FDP1 is stopped is ignored as NOP. As it takes a while until the reset is actually issued after the reset bit is set, the FDP1 may complete operation before the reset is actually issued. In this case, no interrupt is output for the software reset that is issued after the FDP1 completes operation. But even through in this case, not that the output image may be destroyed due to software reset process.</p> <p>This bit is always read as 0.</p> <p>0: NOP 1: Software Reset</p> <p>[Important ] Set FD1_CTL_SGCMD.SGEN to the value 0 before write 1 to this SRST bit.</p>

## 27.3.8.9 Operating Status Register (FD1\_CTL\_STATUS)

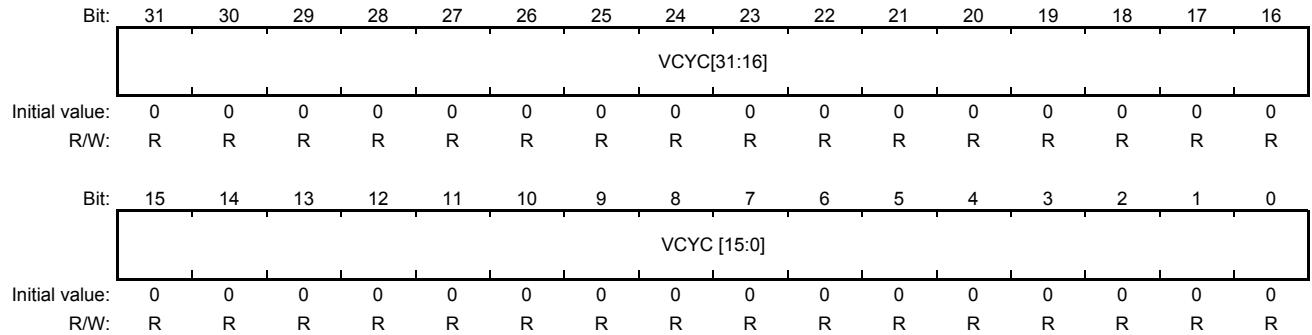
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	VINT_CNT [15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	SGREGSET	SGVERR	SGFREND	—	—	—	—	—	—	—	BSY
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	VINT_CNT [15:0]	H'0000	R	V-Sync Interrupt Counter Status This bit field shows the number of interruption times of V-Sync interrupt. Hence, the value of this bit indicates the number of progressive output frames which is generated by FDP1. This counter value is reset to 0 when FD1_CTL_SGCMD.SGEN is set to 1.
15 to 11	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
10	SGREGSET	0	R	Register Set End Status This bit represents the register set status updated at V-Sync. The status is controlled by FD1_CTL_REGEND.REGEND bit and the internal timing. 0: Registers are not set for the operation 1: Registers are set for the operation
9	SGVERR	0	R	V-Sync End Error Status This bit represents the V-Sync end error status updated at V-Sync. 0: No error 1: V-Sync end error (De-interlacing cannot be finished by the timing of V-Sync)
8	SGFREND	0	R	Frame End Status This bit represents the frame end status updated at V-Sync. 0: The de-interlacing is not finished 1: Frame end (The de-interlacing is finished)
7 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	BSY	0	R	FDP1 Operating Status This bit indicates the operating or stopped state of control FDP1. 0: FDP1 is stopped. 1: FDP1 is operating.

**27.3.8.10 V-Cycles Status Register (FD1\_CTL\_VCYCLE\_STAT)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	VCYC[31:0]	H'0000_000 0	R	Number of Cycles of the Previous Frame Processing  This status register shows the number of cycles of previous frame de-interlacing processing. FDP1 updates this register at the timing of V-Sync interrupt.

### 27.3.8.11 Interrupt Enable Register (FD1\_CTL\_IRQENB)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VERE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	VINTE	—	—	—	FREE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 17	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
16	VERE	0	R/W	Interrupt Enable for V-Sync End Error The interrupt of V-Sync end error is asserted at the timing that FDP1 does not complete the de-interlacing processing at the V-Sync. 0: Interrupt Disabled 1: Interrupt Enabled
15 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	VINTE	0	R/W	Interrupt Enable for V-Sync The interrupt of V-Sync is asserted at the timing of V-Sync specified by FD1_CTL_OPMODE.VIMD register field. If VIMD is set to 2, this interrupt is not asserted. 0: Interrupt Disabled 1: Interrupt Enabled
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	FREE	0	R/W	Interrupt Enable for Frame End The interrupt of frame end is asserted at the timing that FDP1 completes the de-interlacing processing. 0: Interrupt Disabled 1: Interrupt Enabled

Each bit controls the interrupt enable of the corresponding interrupt source.

Each bit in FD1\_CTL\_IRQSTA is set to 1 when the corresponding interrupt source is generated. FD1\_CTL\_IRQENB specifies whether to output an interrupt signal for the generated source. When an interrupt is disabled in this register, no interrupt signal is generated even when the corresponding bit in FD1\_CTL\_IRQSTA is set to 1. When an interrupt is enabled in this register, an interrupt signal is output when the corresponding bit in FD1\_CTL\_IRQSTA is set to 1.



**27.3.8.12 Interrupt Status Register (FD1\_CTL\_IRQSTA)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VER
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	VINT	—	—	—	FRE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 17	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
16	VER	0	R/W	Interrupt Status and Clear for V-Sync End Error [Read Access] Interrupt Status 0: No interrupt 1: Interrupt activated [Write Access] Interrupt Clear 0: The interrupt status is cleared to 0 1: Hold the interrupt status value
15 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	VINT	0	R/W	Interrupt Status and Clear for V-Sync [Read Access] Interrupt Status 0: No interrupt 1: Interrupt activated [Write Access] Interrupt Clear 0: The interrupt status is cleared to 0 1: Hold the interrupt status value
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	FRE	0	R/W	Interrupt Status and Clear for Frame End [Read Access] Interrupt Status 0: No interrupt 1: Interrupt activated [Write Access] Interrupt Clear 0: The interrupt status is cleared to 0 1: Hold the interrupt status value

The read value from each bit is the status of the interrupt source, and the write access to each bit controls the interrupt status.

FD1\_CTL\_IRQSTA indicates the state of the interrupt sources generated in the FDP1. Whether to output a FDP1 interrupt when an interrupt source is generated and the corresponding bit is set to 1 is determined by the corresponding bit setting in FD1\_CTL\_IRQENB.

While an interrupt is disabled in FD1\_CTL\_IRQENB, the FDP1 does not output an interrupt signal even when an interrupt source is generated, but the source flag in this register is set to 1.

**27.3.8.13 Interrupt Control Register (FD1\_CTL\_IRQFSET)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

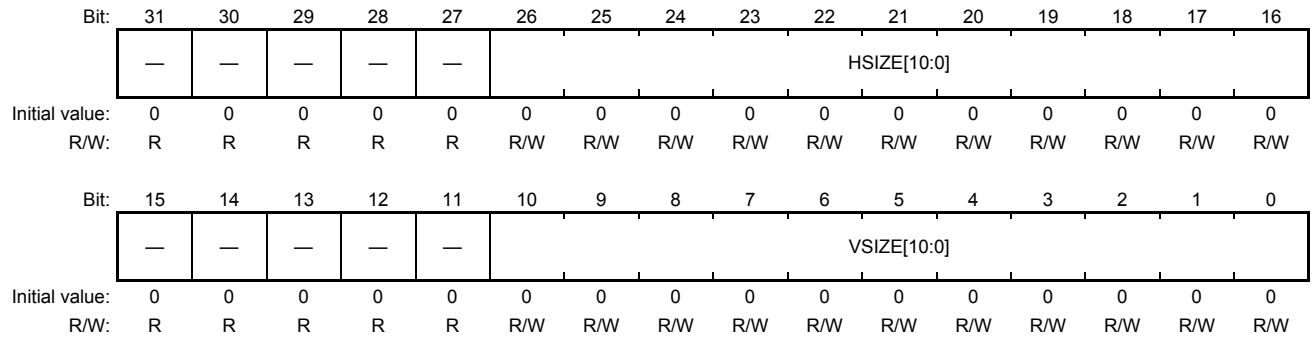
Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VER
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	VINT	—	—	—	FRE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 17	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
16	VER	0	R/W	Set the value 0 to this bit.
15 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	VINT	0	R/W	Set the value 0 to this bit.
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	FRE	0	R/W	Set the value 0 to this bit.

### 27.3.9 RPF Control Registers

#### 27.3.9.1 Source Picture Size Register (FD1\_RPF\_SIZE)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√



Bit	Bit Name	Initial Value	R/W	Description
31 to 27	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
26 to 16	HSIZE[10:0]	All 0	R/W	Horizontal Source Picture Size Specify the horizontal picture size of each input field in unit of pixels.
15 to 11	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
10 to 0	VSIZE[10:0]	All 0	R/W	Vertical Source Picture Size Specify the vertical picture size of each input field in unit of pixels.

### 27.3.9.2 Source Picture Format Register (FD1\_RPF\_FORMAT)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CIPM
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	RSPYCS	RSPUVS	—	—	—	CF	—	RDFMT[6:0]						
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R	R	R	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 17	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
16	CIPM	0	R/W	Set 0 when FD1_CTL_OPMODE.PRG is set to 1, otherwise set the value 1 to this bit.
15, 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13	RSPYCS	0	R/W	RPF Input Mode Setting 1 When the input format is YUY2, set this bit to 1 and set the RDFMT bits to 71 (H'47). When the input format is YVYU, set this bit and the RSPUVS bit to 1 and set the RDFMT bits to 71 (H'47). In other cases, set this bit to 0.
12	RSPUVS	0	R/W	RPF Input Mode Setting 2 When the input format is NV61, set this bit to 1 and set the RDFMT bits to 65 (H'41). When the input format is NV21, set this bit to 1 and set the RDFMT bits to 66 (H'42). When the input format is YVYU, set this bit and the RSPYCS bit to 1 and set the RDFMT bits to 71 (H'47). In other cases, set this bit to 0.
11 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	CF	0	R/W	Current Field This bit specifies current field parity. Note that the previous or next field pictures should be the opposite parity of the current field specified by this bit. 0: Current field is top field 1: Current field Bottom field
7	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
6 to 0	RDFMT [6:0]	All 0	R/W	<p>RPF Input Image Format Setting</p> <p>These bits select the format of the image input from the external SDRAM to the RPFn. Select a value corresponding to the desired format from those shown in Table 27.7.</p> <p>Note: Number of input pixels When YCbCr4:2:2 is selected through the RDFMT bits, the horizontal size of the input image should be specified in 2-pixel units. When YCbCr4:2:0 is selected, the vertical and horizontal sizes should be specified in 2-pixel units.</p>

**Table 27.7 YCbCr Formats for RPF Input\*<sup>5</sup> and WPF Output\*<sup>4</sup>**

RDFMT[6:0], WRFMT[6:0]	Packed YCbCr Input Format	Reference
H'00 to H'3F	Reserved	—
H'40	YCbCr4:4:4 semi-planar	Figure 27.6
H'41	YCbCr4:2:2 semi-planar (NV16, NV61* <sup>1</sup> )	
H'42	YCbCr4:2:0 semi-planar (NV12, NV21* <sup>1</sup> )	
H'43 to H'45	Reserved	—
H'46	YCbCr4:4:4 interleaved	Figure 27.7
H'47	YCbCr4:2:2 interleaved type 0 (UYVY, YUY2* <sup>2</sup> , YVYU* <sup>3</sup> )	
H'48	YCbCr4:2:2 interleaved type 1	
H'49	Reserved	
H'4A	YCbCr4:4:4 planar	Figure 27.8
H'4B	YCbCr4:2:2 planar (YV16)	
H'4C	YCbCr4:2:0 planar (YV12, YU12)	
H'4D to H'7F	Reserved	—

- Notes:
- When the input format is NV61 or NV21, set the RSPUVS bit to 1.
  - When the input format is YUY2, set the RSPYCS bit to 1.
  - When the input format is YVYU, set the RSPUVS bit to 1 and RSPYCS bit to 1.
  - The performance of FDP1 depends on the format because of the limited bus buffer size. The following formats may decrease the tolerance of the bus latency and may decrease the performance of FDP1.
    - YCbCr 4:4:4 interleaved
    - YCbCr 4:4:4 semi-planar
    - YCbCr 4:2:2 interleaved type0 and 1
  - In processing by RPF0 and RPF2, the chroma components (Cb and Cr, or U and V) are not read from the system bus when the format is planar or semi-planar. The chroma components are discarded once they are read in combination with the luma component when the format is interleaved because the RPF0 and RPF2 only handle fixed 2D de-interlacing of the luma component, and so do not require the chroma components.

In write format case shown in section 27.3.10.1, FD1\_WPF\_FORMAT.WSPYCS and WSPUVS correspond to RSPYCS and RSPUVS, respectively.

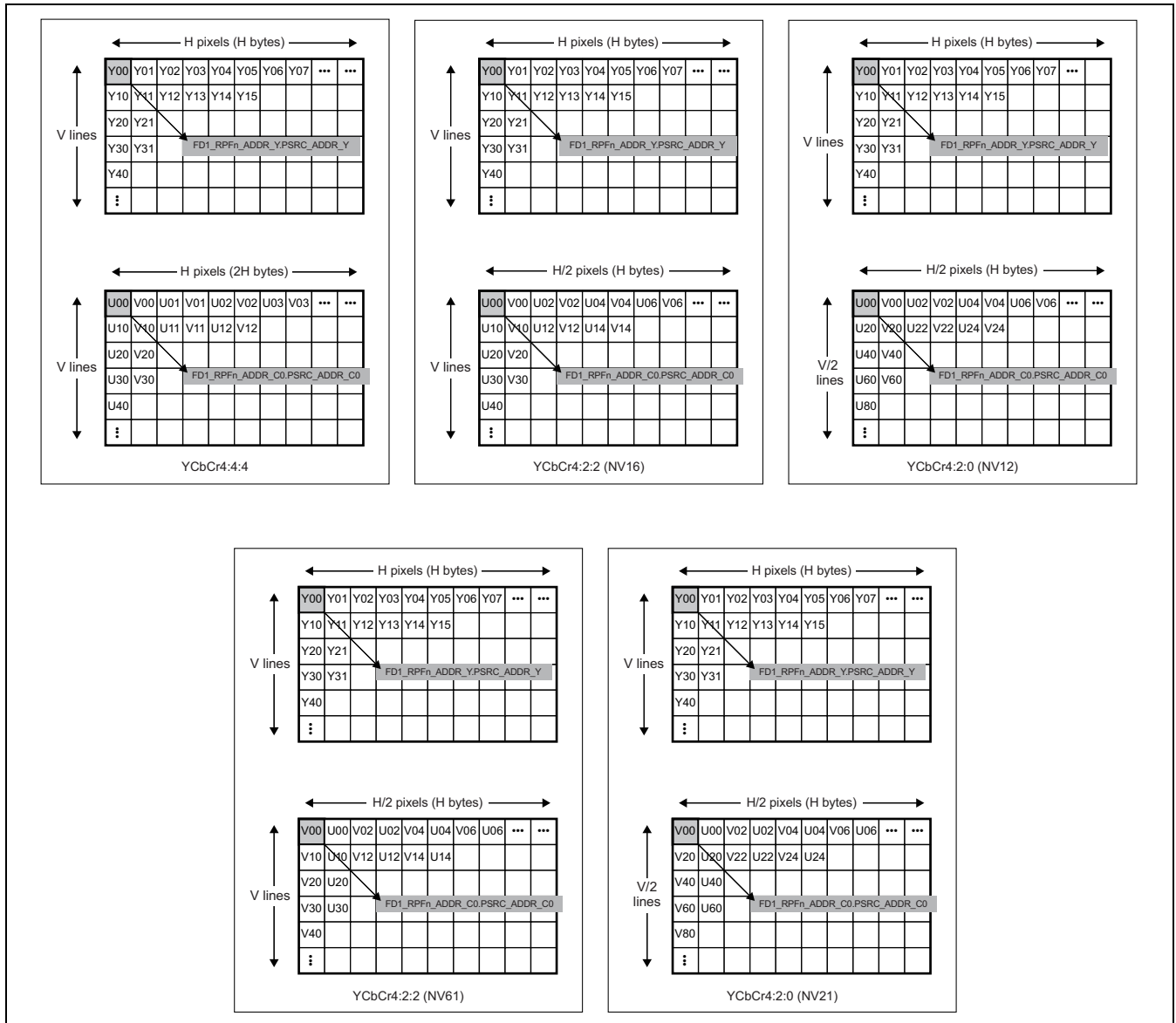


Figure 27.6 YCbCr Semi-Planar Formats

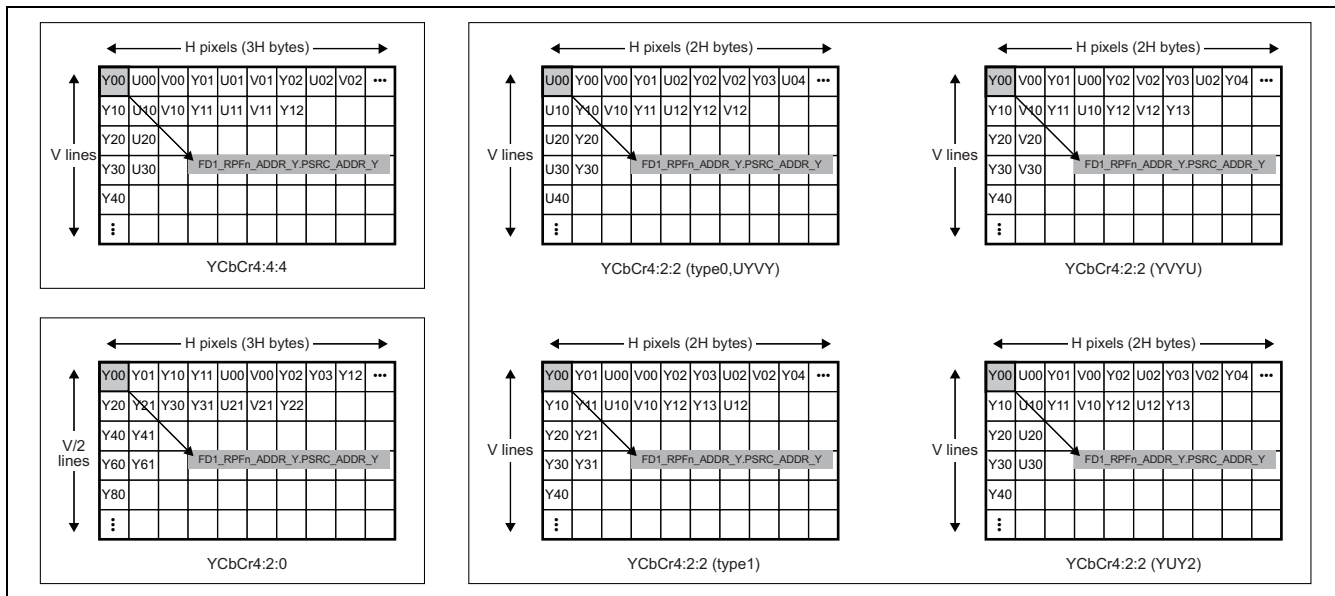


Figure 27.7 YCbCr Interleaved Formats

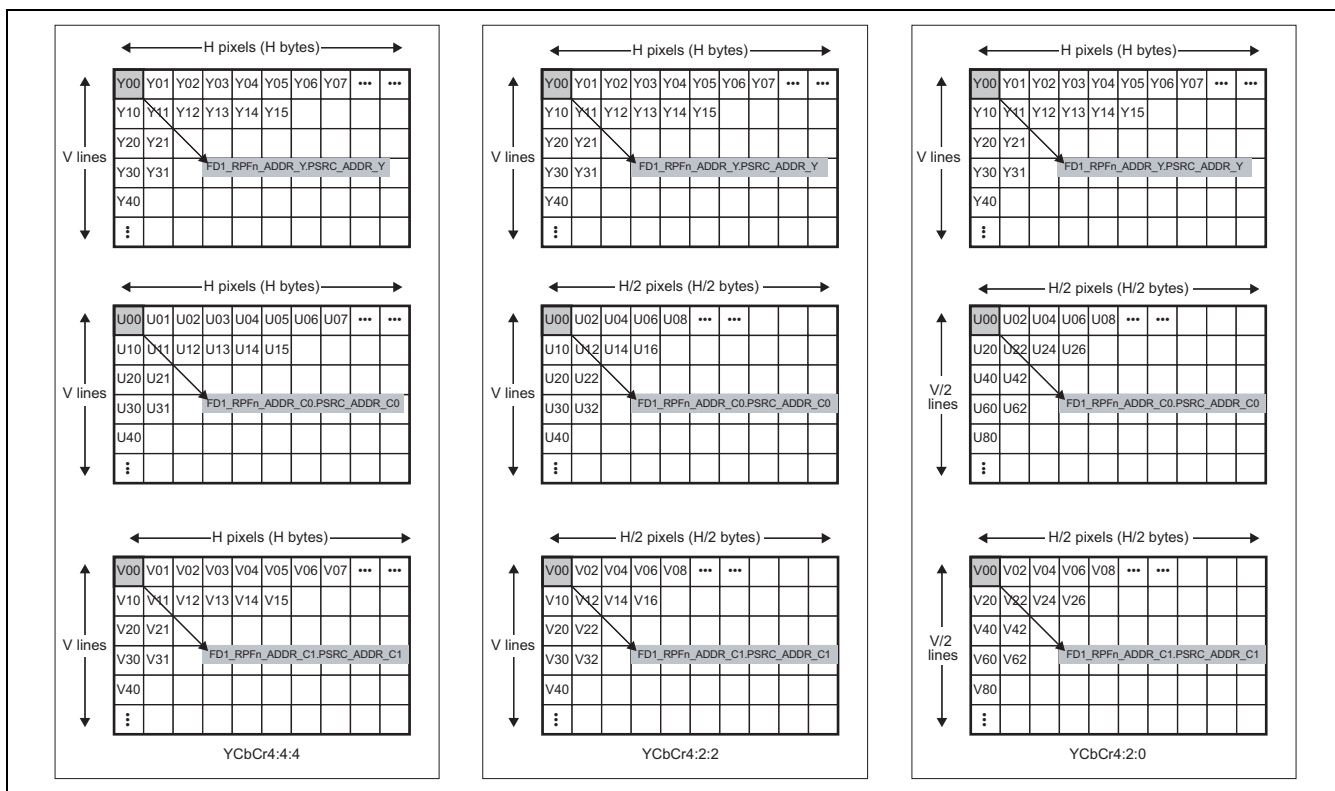
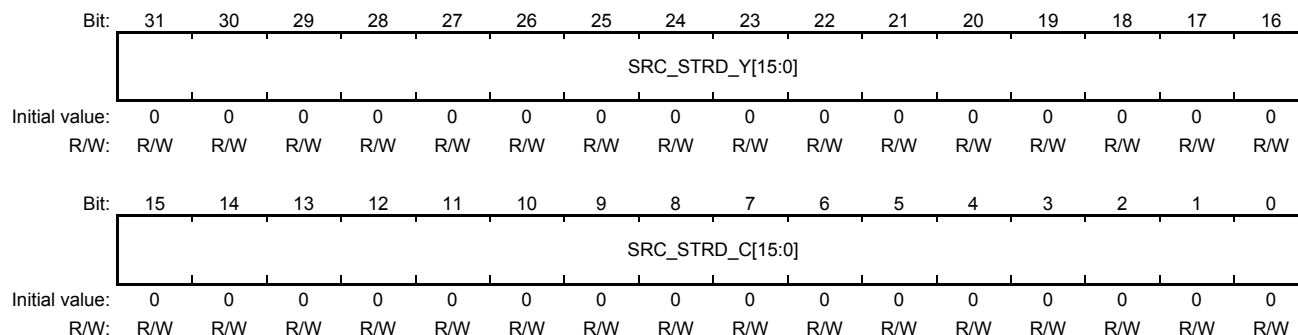


Figure 27.8 YCbCr Planar Formats



**27.3.9.3 Source Picture Stride Register (FD1\_RPF\_PSTRIDE)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

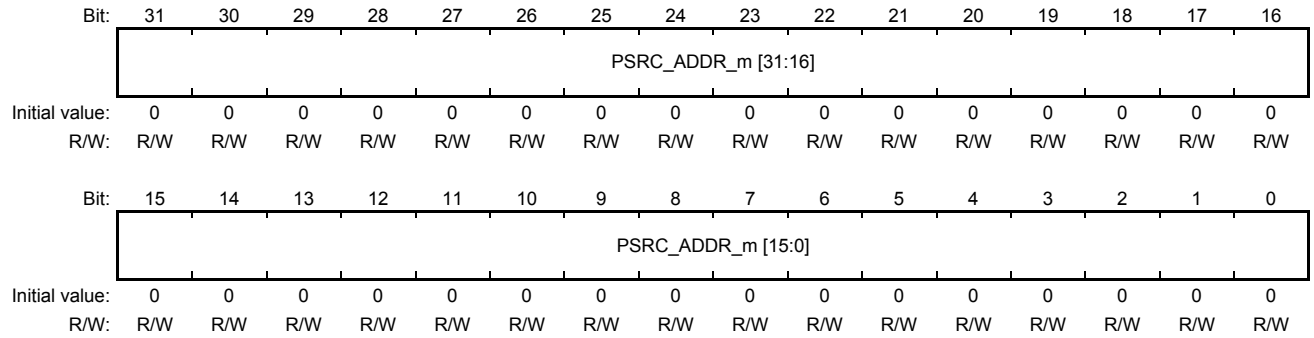


Bit	Bit Name	Initial Value	R/W	Description
31 to 16	SRC_STRD_Y [15:0]	H'0000	R/W	Memory Stride of Source Picture Y Plane These bits specify in 1-byte units the memory stride of the source picture Y plane read by the RPFn (n=0, 1, 2). A value from H'0050 to H'1FFE can be specified.
15 to 0	SRC_STRD_C [15:0]	H'0000	R/W	Memory Stride of Source Picture C Plane These bits specify in 1-byte units the memory stride of the source picture C plane read by the RPF1. A value from H'0050 to H'1FFE can be specified. In the YCbCr planar format, this setting is used as the memory stride of the Cb and Cr planes.

Note: As described above, stride value of source pictures (past, current, future) are common one. Therefore frame structures of all input pictures should be the same format. For example, the case that past picture which is supplied to RPF0 is frame-structure, and other input pictures to RPF1 and 2 are field picture, is prohibited.

**27.3.9.4 RPFn Source Component-m Address Register**  
**(FD1\_RPFn\_ADDR\_m: where {n, m} is any of {0, Y}, {1, Y}, {1, C0}, {1, C1}, or {2, Y}))**

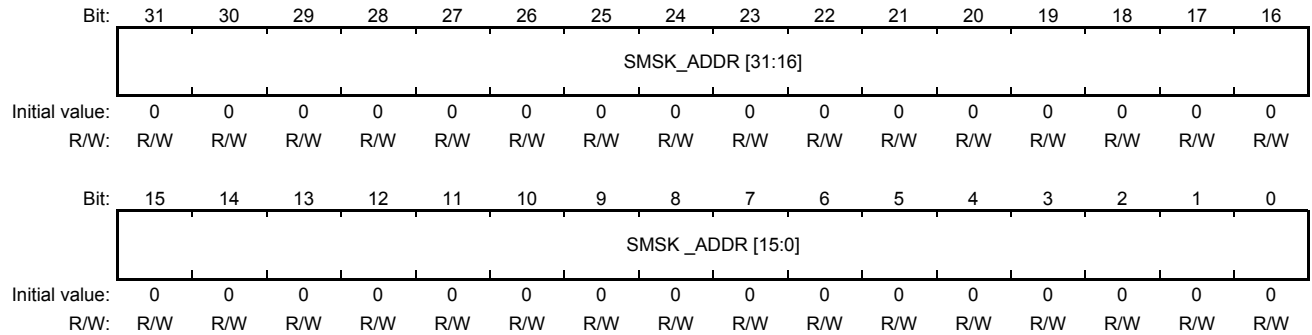
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	PSRC_ADDR_m [31:0]	H'0000_0000	R/W	<p>RPFn Source Field Address for Component-m (where {n, m} is any of {0, Y}, {1, Y}, {1, C0}, {1, C1}, or {2, Y})</p> <p>These bits specify in 1-byte units the start address of the source component-m plane read by the RPFn.</p> <p>A value from H'0000_0000 to H'FFFF_FFFF can be specified.</p>

**27.3.9.5 Still Mask Address Register (FD1\_RPF\_SMSK\_ADDR)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	SMSK_ADDR [31:0]	H'0000_0000	R/W	<p>Still Mask Buffer Address.</p> <p>These bits specify the memory address at which the still mask data is located.</p> <p>These bits should be set to a value ranging from H'0000_0000 to H'FFFF_FFFF.</p> <p>The still mask is intermediate data generated during IP conversion only when adaptive 2D/3D (FD1_CTL_OPMODE.PRG = 0 and FD1_CTL_IPC_MODE.DIM [2:0] = 0) is specified. The still mask setting is effective when either of bits FD1_CTL_CHACT.SMW or FD1_CTL_CHACT.SMR is set to 1. The still mask data is generated and repeatedly used by the FDP1. The still mask data should be stored in the SDRAM.</p> <p>The FDP1 needs two separate buffers of the same size for this data; one is common to all top fields and the other is common to all bottom fields. Therefore, the top and bottom fields must have different source addresses. When FD1_RPF_FORMAT.CF is 0, set the buffer address of the top field in these bits. Otherwise, set the buffer address of the bottom field in these bits.</p> <p>The memory stride of each buffer is expressed as the following equation.</p> $2 \times \{(FD1\_RPF\_SIZE.HSIZE + 7)/8\} \text{ [byte]}$ <p>The memory space of each buffer is expressed as below.</p> $2 \times \{(FD1\_RPF\_SIZE.HSIZE + 7)/8\} \times FD1\_RPF\_SIZE.VSIZE \text{ [byte]}$ <p>Figure 27.9 shows the usage of the still mask data buffers and Table 27.8 shows how to set this register.</p>

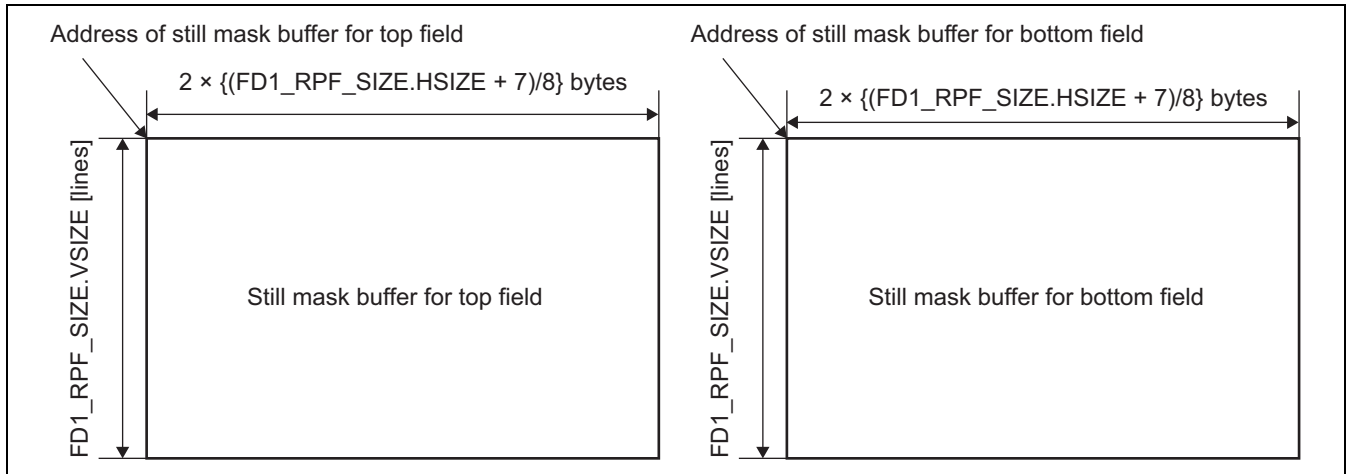


Figure 27.9 Usage of Still Mask Buffers

Table 27.8 Setting of Still Mask Address Register

Current Field Parity	FD1_RPF_FORMAT.CF	FD1_RPF_SMSK_ADDR.SMSK_ADDR
Top field	0	Address of still mask buffer for top field
Bottom field	1	Address of still mask buffer for bottom field

**27.3.9.6 RPF Data Swap Register (FD1\_RPF\_SWAP)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	ISWAP[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3 to 0	ISWAP[3:0]	H'0	R/W	Input Swap Setting for Image Data This bit field specifies the data swapping function. Each bit corresponds to the following data swapping. Refer to Table 27.9 for the data alignment after data swapping. Bit[3]: Long longword (64-bit) swap Bit[2]: Longword (32-bit) swap Bit[1]: Word (16-bit) swap Bit[0]: Byte (8-bit) swap

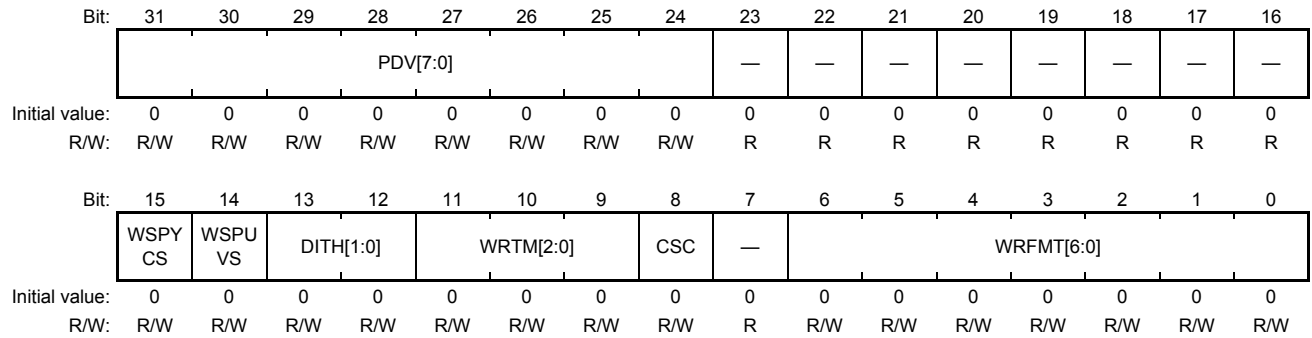
**Table 27.9 Data Order after Swapping Function**

ISWAP[3:0]/OSWAP[3:0]				Input →	Changed Order of Data (Each Value Indicates One Byte)															
Bit3	Bit2	Bit1	Bit0		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	0	Output →	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	1		1	0	3	2	5	4	7	6	9	8	11	10	13	12	15	14
0	0	1	0		2	3	0	1	6	7	4	5	10	11	8	9	14	15	12	13
0	0	1	1		3	2	1	0	7	6	5	4	11	10	9	8	15	14	13	12
0	1	0	0		4	5	6	7	0	1	2	3	12	13	14	15	8	9	10	11
0	1	0	1		5	4	7	6	1	0	3	2	13	12	15	14	9	8	11	10
0	1	1	0		6	7	4	5	2	3	0	1	14	15	12	13	10	11	8	9
0	1	1	1		7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8
1	0	0	0		8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7
1	0	0	1		9	8	11	10	13	12	15	14	1	0	3	2	5	4	7	6
1	0	1	0		10	11	8	9	14	15	12	13	2	3	0	1	6	7	4	5
1	0	1	1		11	10	9	8	15	14	13	12	3	2	1	0	7	6	5	4
1	1	0	0		12	13	14	15	8	9	10	11	4	5	6	7	0	1	2	3
1	1	0	1		13	12	15	14	9	8	11	10	5	4	7	6	1	0	3	2
1	1	1	0		14	15	12	13	10	11	8	9	6	7	4	5	2	3	0	1
1	1	1	1		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

**27.3.10 WPF Control Registers**

**27.3.10.1 Destination Picture Format Register (FD1\_WPF\_FORMAT)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	PDV[7:0]	H'00	R/W	<p>PAD Value in Output Packed Data</p> <p>These bits specify the value to be stored in the bit field indicated as PAD or P in the output formats shown in Table 27.7. A value from 0 to 255 can be specified.</p>
23 to 16	—	All 0	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>
15	WSPYCS	0	R/W	<p>WPF Output Mode Setting 1</p> <p>When the output format is YUY2, set this bit to 1 and set the WRFMT bits to 71 (H'47).</p> <p>When the output format is YVYU, set this bit and the WSPUVS bit to 1 and set the WRFMT bits to 71 (H'47).</p> <p>In other cases, set this bit to 0.</p>
14	WSPUVS	0	R/W	<p>WPF Output Mode Setting 2</p> <p>When the output format is NV61, set this bit to 1 and set the WRFMT bits to 65 (H'41).</p> <p>When the output format is NV21, set this bit to 1 and set the WRFMT bits to 66 (H'42).</p> <p>When the output format is YVYU, set this bit and the WSPYCS bit to 1 and set the WRFMT bits to 71 (H'47).</p> <p>In other cases, set this bit to 0.</p>

Bit	Bit Name	Initial Value	R/W	Description
13, 12	DITH[1:0]	00	R/W	<p>Dithering Enable/Disable</p> <p>When the output format specified through the WRFMT bits is RGB with 18 bpp (262144 colors) or less, the color reduction processing is applied to match the number of colors. The color reduction processing may generate the artifacts of pseudo gradation, which can be suppressed through dithering. The DITH bits enable or disable dithering during color reduction.</p> <p>When the output format specified through the WRFMT bits is YCbCr, specify 0 in these bits.</p> <p>00: Dithering is disabled 01: Setting prohibited 10: Setting prohibited 11: Dithering is enabled</p>
11 to 9	WRTM[2:0]	000	R/W	<p>CSC Conversion Expression Setting</p> <p>These bits select the expression for color space conversion. The conversion direction is RGB to YCbCr when the format specified in the WRFMT bits is RGB, or YCbCr to RGB when the format is YCbCr.</p> <p>000: BT.601 YCbCr [16,235/240] → RGB [0,255] 001: BT.601 YCbCr [0,255] → RGB [0,255] 010: BT.709 YCbCr [16,235/240] → RGB [0,255] 011: BT.709 YCbCr [16,235/240] → RGB [16,235] 100 to 111: Setting prohibited</p>
8	CSC	0	R/W	<p>Color Space Conversion Setting</p> <p>Enables or disables YCbCr ↔ RGB color space conversion to be executed in the WPF. The characteristics of color space conversion are determined by the WRTM setting.</p> <p>0: Color space is not converted. 1: Color space is converted.</p>
7	—	0	R	<p>Reserved</p> <p>This bit is always read as 0. The write value should always be 0.</p>
6 to 0	WRFMT[6:0]	All 0	R/W	<p>WPF Output Image Format Setting</p> <p>These bits select the format of the image output from the WPF to the external memory from among those listed in Tables 27.10 and 27.7.</p> <p>Note: Number of output pixels When YCbCr4:2:2 is specified through WRFMT, the horizontal size of the output image should be a multiple of 2 pixels. When YCbCr4:2:0 is specified, the vertical and horizontal sizes of the output image should be multiples of 2 pixels.</p>



**Table 27.10 Packed RGB Formats for WPF Output**

WRFMT	Bit per pixel	Phase	Bit field																																		
			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
H'00	8	—	R0	R0	R0	G0	G0	G0	B0	B0	R1	R1	R1	G1	G1	G1	B1	B1	R2	R2	R2	G2	G2	G2	B2	B2	R3	R3	R3	G3	G3	G3	B3	B3			
H'01	12	—	0	0	0	0	R0	R0	R0	R0	G0	G0	G0	G0	B0	B0	B0	B0	0	0	0	0	R1	R1	R1	R1	G1	G1	G1	G1	B1	B1	B1	B1			
H'02		—	R0	R0	R0	R0	G0	G0	G0	G0	B0	B0	B0	B0	0	0	0	0	R1	R1	R1	R1	G1	G1	G1	G1	B1	B1	B1	B1	0	0	0	0			
H'03	—	—	Reserved								Reserved								Reserved								Reserved										
H'04	15	—	0	R0	R0	R0	R0	R0	G0	G0	G0	G0	B0	B0	B0	B0	B0	0	R1	R1	R1	R1	R1	G1	G1	G1	G1	G1	G1	B1	B1	B1	B1				
H'05		—	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	0	R1	R1	R1	R1	R1	G1	G1	G1	G1	G1	B1	B1	B1	B1	B1	0			
H'06	16	—	R0	R0	R0	R0	R0	G0	G0	G0	G0	B0	B0	B0	B0	B0	B0	R1	R1	R1	R1	R1	G1	G1	G1	G1	G1	G1	B1	B1	B1	B1					
H'07	18	—	PAD0								0	0	0	0	0	0	R0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0					
H'08		—	R0	R0	R0	R0	R0	R0	G0	G0	G0	G0	B0	B0	B0	B0	B0	0	0	0	0	0	0	0	0	0	PAD0										
H'09		—	0	0	0	0	0	0	R0	R0	R0	R0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	B0	B0	B0	PAD0											
H'0A		—	PAD0								R0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	B0	0	0	0	0	0	0	0		
H'0B		—	PAD0								0	0	R0	R0	R0	R0	R0	R0	0	0	G0	G0	G0	G0	G0	G0	0	0	B0	B0	B0	B0	B0	B0			
H'0C		—	0	0	R0	R0	R0	R0	R0	0	0	G0	G0	G0	G0	G0	G0	0	0	B0	B0	B0	B0	B0	B0	PAD0											
H'0D		—	PAD0								R0	R0	R0	R0	R0	R0	0	0	G0	G0	G0	G0	G0	G0	0	0	B0	B0	B0	B0	B0	0	0	B0	B0	B0	B0
H'0E		—	R0	R0	R0	R0	R0	R0	0	0	G0	G0	G0	G0	G0	G0	0	0	B0	B0	B0	B0	B0	B0	0	0	PAD0										
H'0F		0	0	0	0	0	0	0	0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	B0	0	0	0	0	0	0	R1	R1	
		1	R1	R1	R1	R1	G1	G1	G1	G1	G1	G1	B1	B1	B1	B1	B1	B1	0	0	0	0	0	0	0	0	R2	R2	R2	R2	R2	R2	G2	G2	G2	G2	
		2	G2	G2	B2	B2	B2	B2	B2	B2	0	0	0	0	0	0	0	R3	R3	R3	R3	R3	R3	G3	G3	G3	G3	G3	G3	B3	B3	B3	B3	B3	B3	B3	
H'10		0	R0	R0	R0	R0	R0	R0	G0	G0	G0	G0	B0	B0	B0	B0	B0	0	0	0	0	0	0	0	0	0	R1	R1	R1	R1	R1	R1	G1	G1			
		1	G1	G1	G1	G1	B1	B1	B1	B1	B1	B1	0	0	0	0	0	0	R2	R2	R2	R2	R2	R2	G2	G2	G2	G2	G2	G2	G2	G2	B2	B2	B2	B2	
		2	B2	B2	0	0	0	0	0	0	0	R3	R3	R3	R3	R3	R3	G3	G3	G3	G3	G3	G3	B3	B3	B3	B3	B3	B3	0	0	0	0	0	0	0	
H'11	0	0	0	R0	R0	R0	R0	R0	0	0	G0	G0	G0	G0	G0	G0	0	0	B0	B0	B0	B0	B0	B0	0	0	R1	R1	R1	R1	R1	R1	R1	R1			
	1	0	0	G1	G1	G1	G1	G1	0	0	B1	B1	B1	B1	B1	B1	0	0	R2	R2	R2	R2	R2	R2	0	0	G2	G2	G2	G2	G2	G2	G2	G2			
	2	0	0	B2	B2	B2	B2	B2	B2	0	0	R3	R3	R3	R3	R3	R3	0	0	G3	G3	G3	G3	G3	G3	0	0	B3	B3	B3	B3	B3	B3	B3	B3		
H'12	0	R0	R0	R0	R0	R0	R0	0	0	G0	G0	G0	G0	G0	G0	0	0	B0	B0	B0	B0	B0	B0	0	0	R1	R1	R1	R1	R1	R1	0	0				
	1	G1	G1	G1	G1	G1	G1	0	0	B1	B1	B1	B1	B1	B1	0	0	R2	R2	R2	R2	R2	R2	0	0	G2	G2	G2	G2	G2	G2	G2	0	0			
	2	B2	B2	B2	B2	B2	B2	0	0	R3	R3	R3	R3	R3	R3	0	0	G3	G3	G3	G3	G3	G3	0	0	B3	B3	B3	B3	B3	B3	B3	0	0			
H'13	24	—	PAD0								R0	R0	R0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	B0	B0						
H'14		—	R0	R0	R0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	B0	B0	B0	B0	B0	B0	B0	B0	B0	B0				
H'15		0	R0	R0	R0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	B0	B0	B0	B0	B0	R1	R1	R1	R1	R1	R1	R1		
		1	G1	G1	G1	G1	G1	G1	G1	G1	B1	B1	B1	B1	B1	B1	B1	B1	R2	R2	R2	R2	R2	R2	R2	R2	R2	R2	G2	G2	G2	G2	G2	G2	G2		
H'16	18	—	0	0	0	0	0	0	0	R0	R0	R0	R0	R0	G0	G0	G0	0	0	0	0	0	0	0	0	G0	G0	G0	B0	B0	B0	B0					
H'17		—	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	B0	B0	B0	B0					
H'18	24	0	B0	B0	B0	B0	B0	B0	B0	G0	G0	G0	G0	G0	G0	G0	G0	R0	R0	R0	R0	R0	R0	R0	R0	R0	B1	B1	B1	B1	B1	B1	B1	B1			
		1	G1	G1	G1	G1	G1	G1	G1	R1	R1	R1	R1	R1	R1	R1	R1	B2	B2	B2	B2	B2	B2	B2	B2	G2	G2	G2	G2	G2	G2	G2	G2				
		2	R2	R2	R2	R2	R2	R2	R2	R2	B3	B3	B3	B3	B3	B3	B3	B3	G3	G3	G3	G3	G3	G3	G3	G3	R3	R3	R3	R3	R3	R3	R3	R3			
H'19	12	—	PAD0				R0	R0	R0	R0	G0	G0	G0	G0	B0	B0	B0	PAD1				R1	R1	R1	R1	G1	G1	G1	G1	B1	B1	B1	B1				
H'1A		—	R0	R0	R0	R0	G0	G0	G0	G0	B0	B0	B0	B0	PAD0				R1	R1	R1	R1	G1	G1	G1	G1	B1	B1	B1	B1	PAD1						
H'1B		—	P0	R0	R0	R0	R0	R0	G0	G0	G0	G0	B0	B0	B0	B0	B0	P0	R1	R1	R1	R1	R1	R1	G1	G1	G1	G1	B1	B1	B1	B1	B1				
H'1C		—	R0	R0	R0	R0	R0	R0	G0	G0	G0	G0	B0	B0	B0	B0	B0	P0	R1	R1	R1	R1	R1	R1	G1	G1	G1	G1	B1	B1	B1	B1	B1	P1			
H'1D	12	—	PAD0				B0	B0	B0	B0	G0	G0	G0	G0	R0	R0	R0	PAD1				B1	B1	B1	B1	G1	G1	G1	G1	R1	R1	R1	R1				
H'1E		—	B0	B0	B0	B0	G0	G0	G0	G0	R0	R0	R0	R0	PAD0				B1	B1	B1	B1	G1	G1	G1	G1	R1	R1	R1	R1	PAD1						
H'1F		—	P0	B0	B0	B0	B0	B0	G0	G0	G0	G0	R0	R0	R0	R0	R0	P0	B1	B1	B1	B1	B1	B1	G1	G1	G1	G1	R1	R1	R1	R1	R1				
H'20		—	B0	B0	B0	B0	B0	B0	G0	G0	G0	G0	R0	R0	R0	R0	R0	P0	B1	B1	B1	B1	B1	B1	G1	G1	G1	G1	R1	R1	R1	R1	R1	P1			
H'21	18	0	0	0	0	B0	B0	B0	B0	B0	0	0	G0	G0	G0	G0	G0	0	0	R0	R0	R0	R0	R0	R0	0	0	B1	B1	B1	B1	B1	B1				
		1	0	0	G1	G1	G1	G1	G1	G1	0	0	R1	R1	R1	R1	R1	R1	0	0	B2	B2	B2	B2	B2	B2	0	0	G2	G2	G2	G2	G2	G2			
		2	0	0	R2	R2	R2	R2	R2	R2	0	0	B3	B3	B3	B3	B3	B3	0	0	G3	G3	G3	G3	G3	G3	0	0	R3	R3	R3	R3	R3	R3			
H'22	24	—	PAD0								B0	B0	B0	B0	B0	B0	B0	B0	G0	G0	G0	G0	G0	G0	G0	G0	R0	R0	R0	R0	R0	R0	R0	R0			
H'23	16	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0				
H'24~H'3F	—	—	Reserved								Reserved								Reserved								Reserved										

Refer to Table 27.7 for YCbCr formats.

### 27.3.10.2 Destination Picture Rounding Control Register (FD1\_WPF\_RNDCTL)

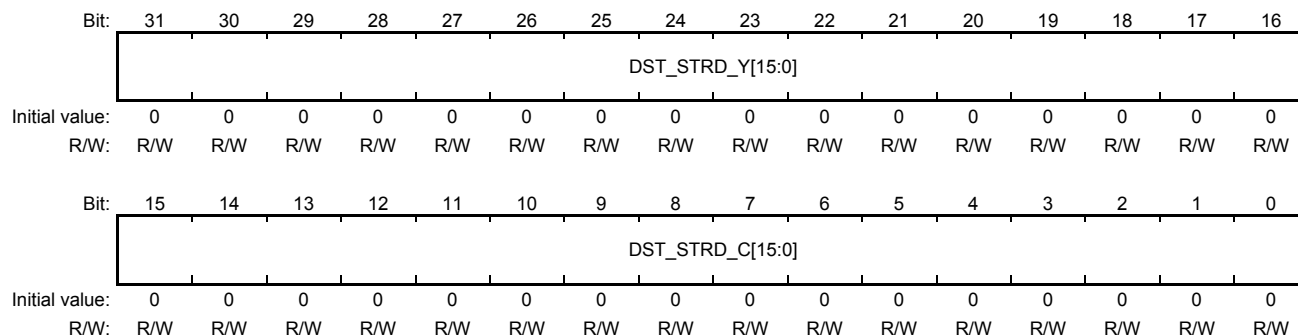
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	CBRM	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	CLMD[1:0]	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28	CBRM	0	R/W	Bit Count Reduction Selection for Data Storage in Packed RGB This bit specifies the method for reducing the number of bits when data is stored in the bit fields indicated as R, G, and B in Table 27.10 and the target bit fields are not eight bits. 0: Bit count conversion: The lower-order bits are truncated 1: Bit count conversion: Rounding (rounding off)
27 to 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13, 12	CLMD[1:0]	00	R/W	Color Data Clipping These bits specify the method for clipping the YCbCr color data output from the WPF. When RGB color data is output from the WPF, specify 0 in these bits. 00: Output value is not clipped (0-255) 01: Output value is clipped: YCbCr mode 1 (16-235 (Y), 16-240 (Cb/Cr)) 10: Output value is clipped: YCbCr mode 2 (Y/Cb/Cr = 1-254) 11: Setting prohibited
11 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

**27.3.10.3 Destination Picture Stride Register (FD1\_WPF\_PSTRIDE)**

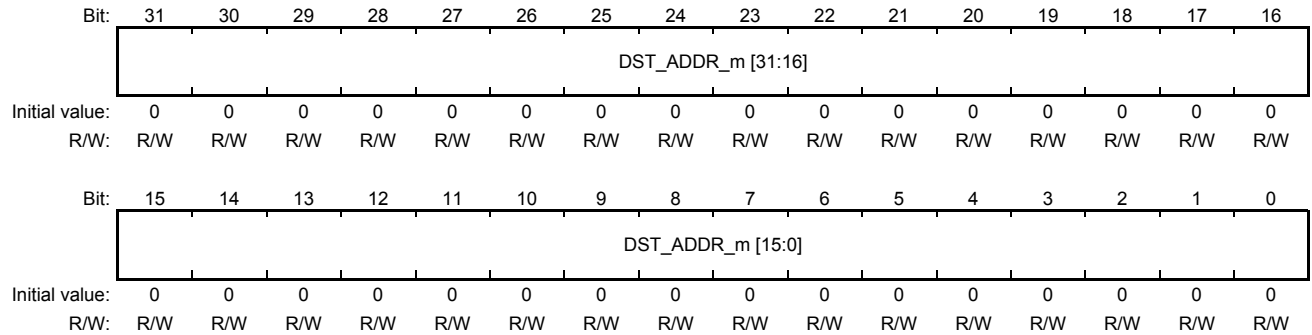
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√



Bit	Bit Name	Initial Value	R/W	Description
31 to 16	DST_STRD_Y [15:0]	H'0000	R/W	<p>Memory Stride of Destination Picture Y/RGB Plane</p> <p>These bits specify in 1-byte units the memory stride of the destination picture in the external memory to be written to by the WPF.</p> <p>A value from H'0050 to H'1FFE can be specified.</p>
15 to 0	DST_STRD_C [15:0]	H'0000	R/W	<p>Memory Stride of Destination Picture C Plane</p> <p>These bits specify in 1-byte units the memory stride for the C plane of the destination picture in the external memory to be written to by the WPF. When the WPF outputs images in an RGB format, this setting is not used. When the WPF outputs images in YCbCr planar format, this setting is applied to both the Cb and Cr planes.</p> <p>A value from H'0050 to H'1FFE can be specified.</p>

**27.3.10.4 Destination Component-m Address Register (FD1\_WPF\_ADDR\_m: m = Y, C0, C1)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	DST_ADDR_m [31:0]	H'0000_0000	R/W	Destination Address for Component-m (m = Y, C0, C1) These bits specify in 1-byte units the address for storing the destination component-m plane to be written to the external memory by the WPF. A value from H'0000_0000 to H'FFFF_FFFF can be specified.

**27.3.10.5 WPF Data Swap Register (FD1\_WPF\_SWAP)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	SSWAP[3:0]				OSWAP[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7 to 4	SSWAP[3:0]	H'0	R/W	Set the same value with FD1_RPF_SWAP.ISWAP.
3 to 0	OSWAP[3:0]	H'0	R/W	Output Swap Setting for Image Data This bit field specifies the data swapping function. Each bit corresponds to the following data swapping. Refer to Table 27.9 for the data alignment after data swapping. Bit[3]: Long longword (64-bit) swap Bit[2]: Longword (32-bit) swap Bit[1]: Word (16-bit) swap Bit[0]: Byte (8-bit) swap

### 27.3.11 IPC Control Registers

**Table 27.11** IPC registers categorized in function

Function	Registers
IP Conversion Control	FD1_IPC_MODE
3D de-interlace	FD1_IPC_COMB_DET
Adaptive 2D/3D de-interlacing	FD1_IPC_MOTDEC
Diagonal line interpolation	FD1_IPC_DLI_BLEND FD1_IPC_DLI_HGAIN FD1_IPC_DLI_SPRS FD1_IPC_DLI_ANGLE FD1_IPC_DLI_ISOPIX0 FD1_IPC_DLI_ISOPIX1
Film detection	FD1_SENSOR_m (m = 0,1,...,17) FD1_SENSOR_CTL0 FD1_SENSOR_CTL1 FD1_SENSOR_CTL2 FD1_SENSOR_CTL3 SENSOR_TH0 SENSOR_TH1

For chroma component, IPC cannot process 3D de-interlace, adaptive 2D/3D de-interlacing, diagonal line interpolation and film detection but can process fixed 2D IP conversion.

**27.3.11.1 IPC Mode Register (FD1\_IPC\_MODE)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	DLI	—	—	—	—	—	DIM[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R	R	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	DLI	0	R/W	Set the value 1 to this bit.
7 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2 to 0	DIM[2:0]	000	R/W	De-Interlacing Mode These bits specify the de-interlacing mode of luma component as following. The de-interlacing process of chroma component is fixed 2D de-interlacing regardless of these bits. 000: Adaptive 2D/3D de-interlacing 001: Fixed 2D de-interlacing 010: Fixed 3D de-interlacing 011: Select previous field for interpolated lines 100: Select next field for interpolated lines

**27.3.11.2 Still Mask Threshold Register (FD1\_IPC\_SMSK\_THRESH)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

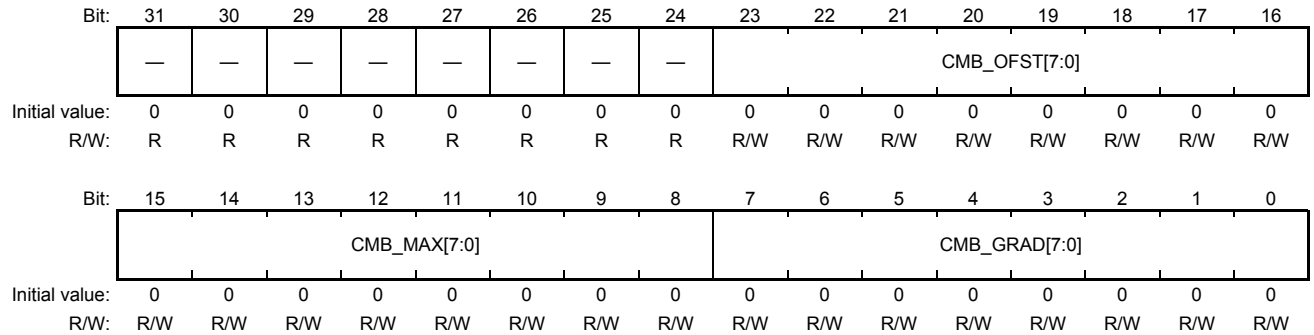
Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FSM0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	SMSK_TH[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 17	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
16	FSM0	0	R/W	Set the value 1 to this bit. Other setting value is used for purpose of h/w debugging. Do not set other value.
15 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7 to 0	SMSK_TH [7:0]	H'00	R/W	Set the value 2 to this bit. Other setting value is used for purpose of h/w debugging. Do not set other value.



**27.3.11.3 Comb Detection Parameter Register (FD1\_IPC\_COMB\_DET)**

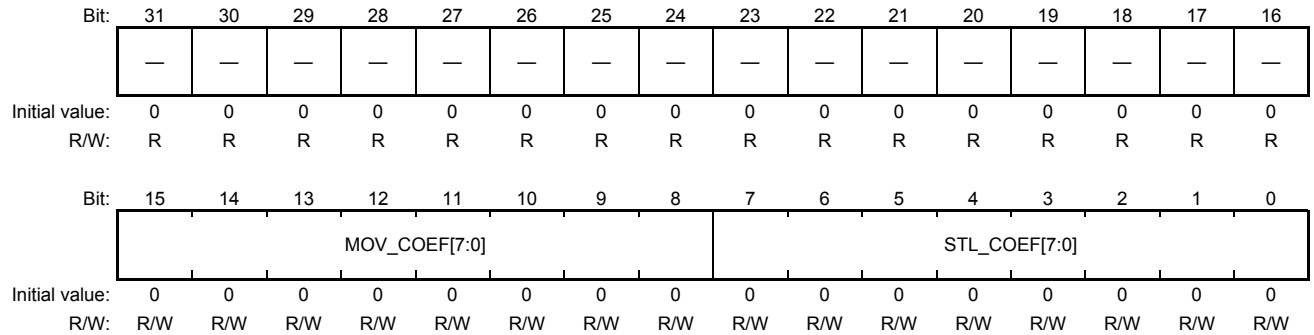
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 16	CMB_OFST [7:0]	H'00	R/W	Set the value H'20 to this bit. Other setting value is used for purpose of h/w debugging. Do not set other value.
15 to 8	CMB_MAX [7:0]	H'00	R/W	Set the value 0 to this bit. Other setting value is used for purpose of h/w debugging. Do not set other value.
7 to 0	CMB_GRAD [7:0]	H'00	R/W	Set the value H'40 to this bit. Other setting value is used for purpose of h/w debugging. Do not set other value.

**27.3.11.4 Motion Decision Parameter Register (FD1\_IPC\_MOTDEC)**

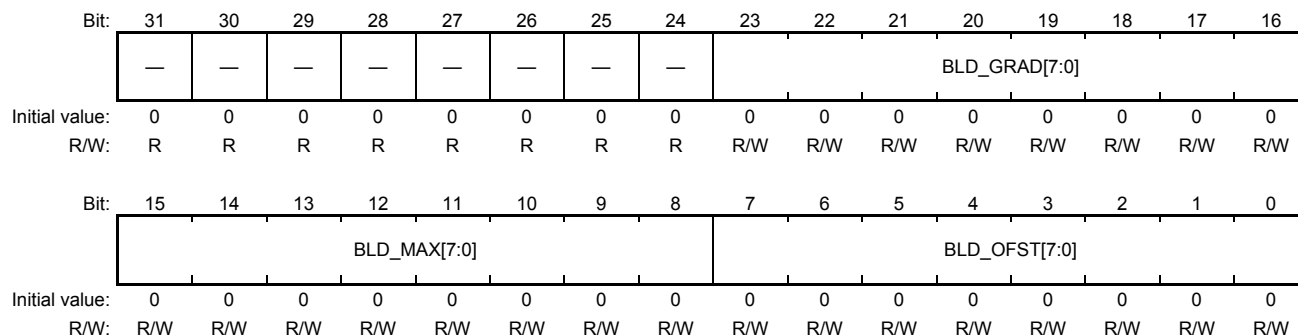
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√



Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 8	MOV_COEF [7:0]	H'00	R/W	Set the value H'80 to this bit. Other setting value is used for purpose of h/w debugging. Do not set other value.
7 to 0	STL_COEF [7:0]	H'00	R/W	Set the value H'20 to this bit. Other setting value is used for purpose of h/w debugging. Do not set other value.

**27.3.11.5 DLI Blend Parameter Register (FD1\_IPC\_DLI\_BLEND)**

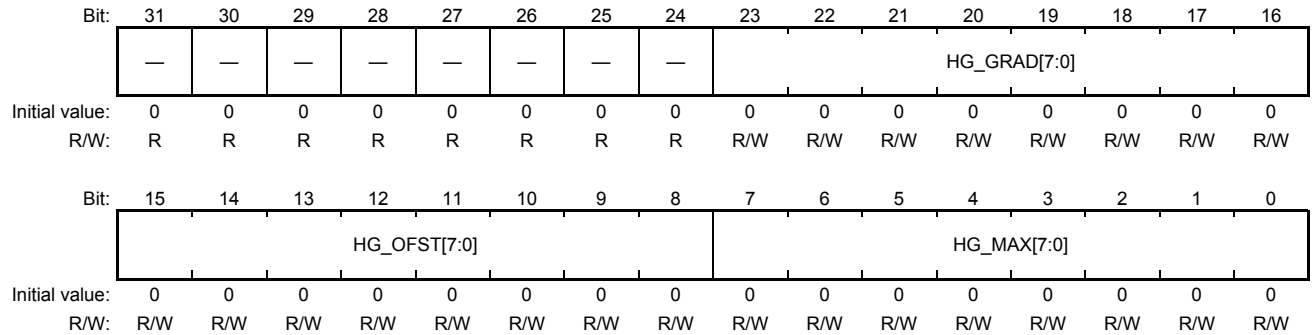
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 16	BLD_GRAD [7:0]	H'00	R/W	Set the value H'80 to this bit. Other setting value is used for purpose of h/w debugging. Do not set other value.
15 to 8	BLD_MAX [7:0]	H'00	R/W	Set the value H'FF to this bit. Other setting value is used for purpose of h/w debugging. Do not set other value.
7 to 0	]BLD_OFST [7:0]	H'00	R/W	Set the value H'02 to this bit. Other setting value is used for purpose of h/w debugging. Do not set other value.

**27.3.11.6 DLI Horizontal Frequency Gain Register (FD1\_IPC\_DLI\_HGAIN)**

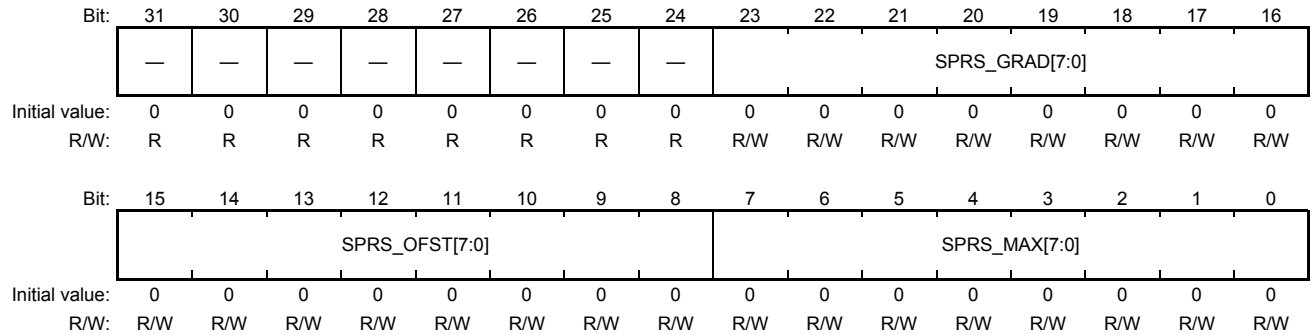
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 16	HG_GRAD [7:0]	H'00	R/W	Set the value H'10 to this bit. Other setting value is used for purpose of h/w debugging. Do not set other value.
15 to 8	HG_OFST [7:0]	H'00	R/W	Set the value H'00 to this bit. Other setting value is used for purpose of h/w debugging. Do not set other value.
7 to 0	HG_MAX [7:0]	H'00	R/W	Set the value H'FF to this bit. Other setting value is used for purpose of h/w debugging. Do not set other value.

**27.3.11.7 DLI Suppression Parameter register (FD1\_IPC\_DLI\_SPRS)**

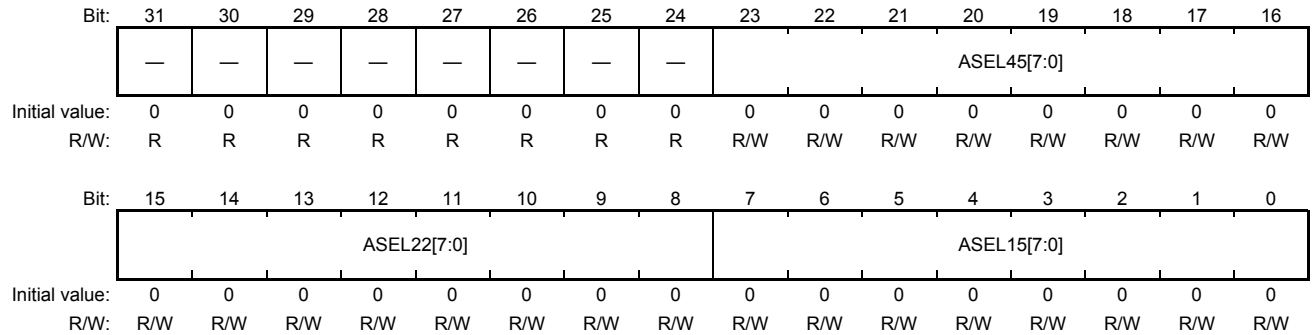
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 16	SPRS_GRAD [7:0]	H'00	R/W	Set the value H'90 to this bit. Other setting value is used for purpose of h/w debugging. Do not set other value.
15 to 8	SPRS_OFST [7:0]	H'00	R/W	Set the value H'04 to this bit. Other setting value is used for purpose of h/w debugging. Do not set other value.
7 to 0	SPRS_MAX [7:0]	H'00	R/W	Set the value H'FF to this bit. Other setting value is used for purpose of h/w debugging. Do not set other value.

**27.3.11.8 DLI Angle Parameter Register (FD1\_IPC\_DLI\_ANGLE)**

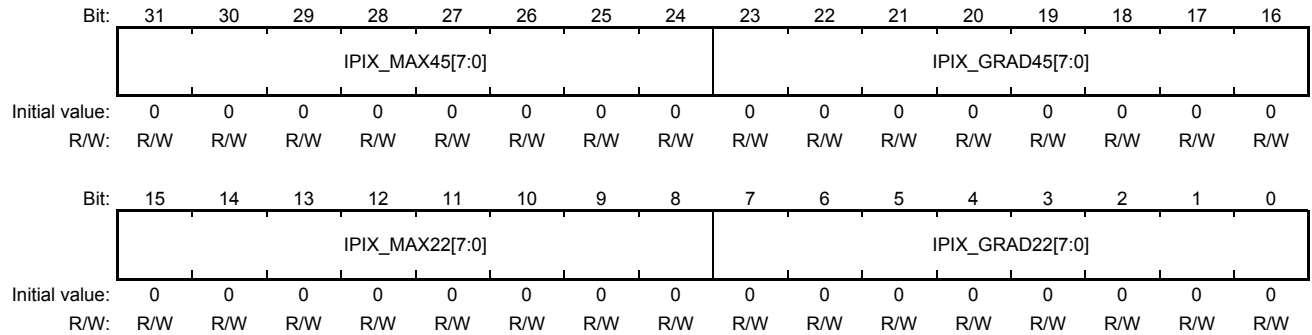
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 16	ASEL45 [7:0]	H'00	R/W	Set the value H'04 to this bit. Other setting value is used for purpose of h/w debugging. Do not set other value.
15 to 8	ASEL22 [7:0]	H'00	R/W	Set the value H'08 to this bit. Other setting value is used for purpose of h/w debugging. Do not set other value.
7 to 0	ASEL15 [7:0]	H'00	R/W	Set the value H'0C to this bit. Other setting value is used for purpose of h/w debugging. Do not set other value.

**27.3.11.9 DLI Isolated Pixel Parameter Register 0 (FD1\_IPC\_DLI\_ISOPIX0)**

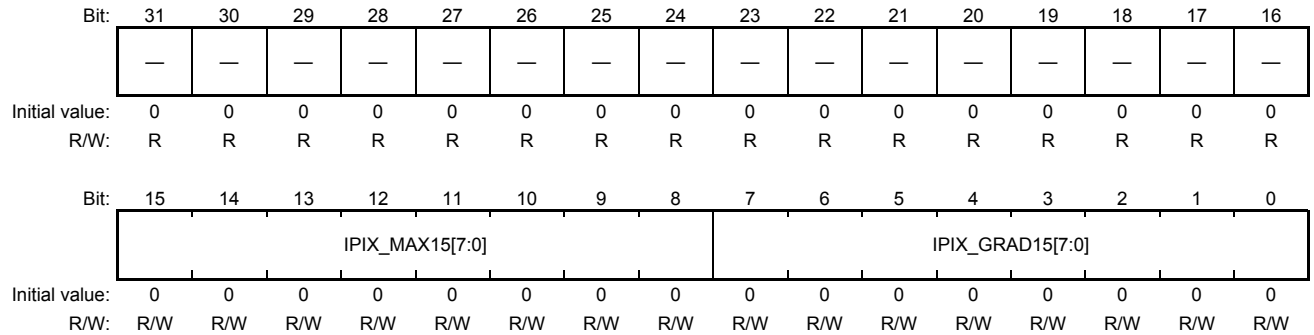
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	IPIX_MAX45 [7:0]	H'00	R/W	Set the value H'FF to this bit. Other setting value is used for purpose of h/w debugging. Do not set other value.
23 to 16	IPIX_GRAD45 [7:0]	H'00	R/W	Set the value H'10 to this bit. Other setting value is used for purpose of h/w debugging. Do not set other value.
15 to 8	IPIX_MAX22 [7:0]	H'00	R/W	Set the value H'FF to this bit. Other setting value is used for purpose of h/w debugging. Do not set other value.
7 to 0	IPIX_GRAD22 [7:0]	H'00	R/W	Set the value H'10 to this bit. Other setting value is used for purpose of h/w debugging. Do not set other value.

**27.3.11.10 DLI Isolated Pixel Parameter Register 1 (FD1\_IPC\_DLI\_ISOPIX1)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

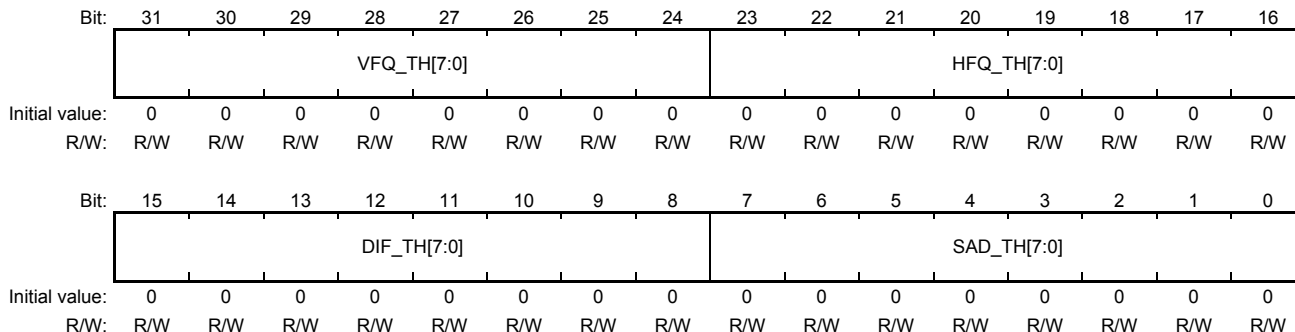


Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 8	IPIX_MAX15 [7:0]	H'00	R/W	Set the value H'FF to this bit. Other setting value is used for purpose of h/w debugging. Do not set other value.
7 to 0	IPIX_GRAD15 [7:0]	H'00	R/W	Set the value H'10 to this bit. Other setting value is used for purpose of h/w debugging. Do not set other value.



**27.3.11.11 IPC Sensor Threshold Register 0 (FD1\_IPC\_SENSOR\_TH0)**

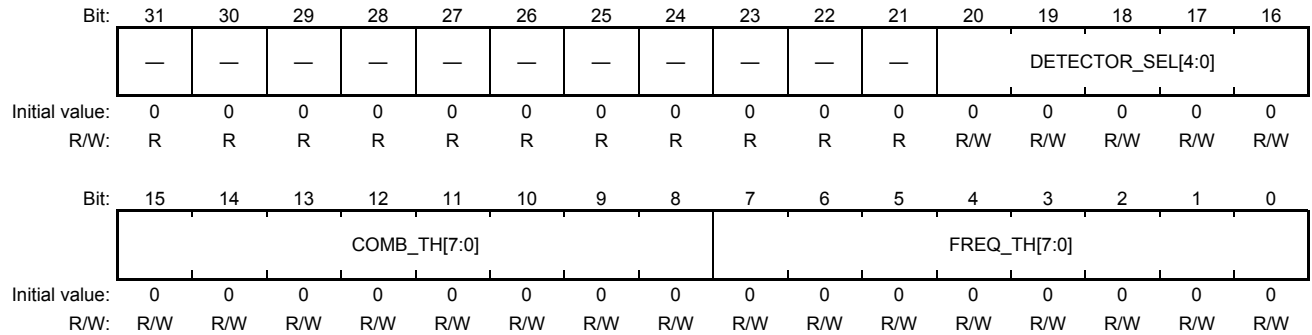
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	VFQ_TH[7:0]	H'00	R/W	Set the value H'20 to this bit. Other setting value is used for purpose of h/w debugging. Do not set other value.
23 to 16	HFQ_TH[7:0]	H'00	R/W	Set the value H'20 to this bit. Other setting value is used for purpose of h/w debugging. Do not set other value.
15 to 8	DIF_TH[7:0]	H'00	R/W	Set the value H'80 to this bit. Other setting value is used for purpose of h/w debugging. Do not set other value.
7 to 0	SAD_TH[7:0]	H'00	R/W	Set the value H'80 to this bit. Other setting value is used for purpose of h/w debugging. Do not set other value.

**27.3.11.12 IPC Sensor Threshold Register 1 (FD1\_IPC\_SENSOR\_TH1)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√



Bit	Bit Name	Initial Value	R/W	Description
31 to 21	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
20 to 16	DETECTOR_SEL[4:0]	All 0	R/W	Set the value H'00 to this bit. Other setting value is used for purpose of h/w debugging. Do not set other value.
15 to 8	COMB_TH [7:0]	H'00	R/W	Set the value H'00 to this bit. Other setting value is used for purpose of h/w debugging. Do not set other value.
7 to 0	FREQ_TH [7:0]	H'00	R/W	Set the value H'00 to this bit. Other setting value is used for purpose of h/w debugging. Do not set other value.

**27.3.11.13 Sensor Control Register 0 (FD1\_SENSOR\_CTL0)**

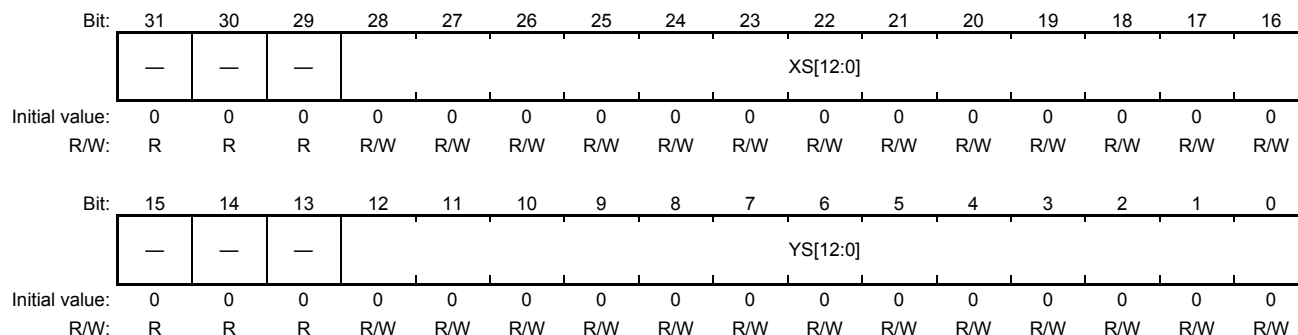
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FRM_LVTH[3:0]				FLD_LVTH[3:0]				—	—	—	—	—	—	—	FD_EN
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 12	FRM_LVTH [3:0]	H'0	R/W	Set the value 2 to this bit. Other setting value is used for purpose of h/w debugging. Do not set other value.
11 to 8	FLD_LVTH [3:0]	H'0	R/W	Set the value 2 to this bit. Other setting value is used for purpose of h/w debugging. Do not set other value.
7 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	FD_EN	0	R/W	Set the value 1 to this bit.

**27.3.11.14 Sensor Control Register 1 (FD1\_SENSOR\_CTL1)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√



Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28 to 16	XS[12:0]	All 0	R/W	Set the value H'000 to this bit. Other setting value is used for purpose of h/w debugging. Do not set other value.
15 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12 to 0	YS[12:0]	All 0	R/W	Set the value H'000 to this bit. Other setting value is used for purpose of h/w debugging. Do not set other value.

**27.3.11.15 Sensor Control Register 2 (FD1\_SENSOR\_CTL2)**

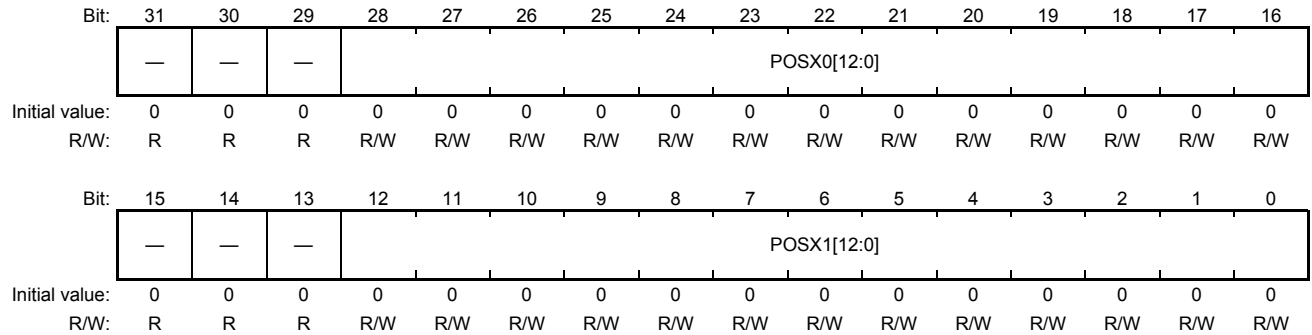
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	XE[12:0]												
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	YE[12:0]												
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28 to 16	XE[12:0]	All 0	R/W	Set the value (FD1_RPF_SIZE.HSIZE - 1) to this bit.
15 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12 to 0	YE[12:0]	All 0	R/W	Set the value (FD1_RPF_SIZE.VSIZE - 1) to this bit if input picture is progressive. Set the value (FD1_RPF_SIZE.VSIZE × 2 - 1) to this bit if input picture is interlaced.

**27.3.11.16 Sensor Control Register 3 (FD1\_SENSOR\_CTL3)**

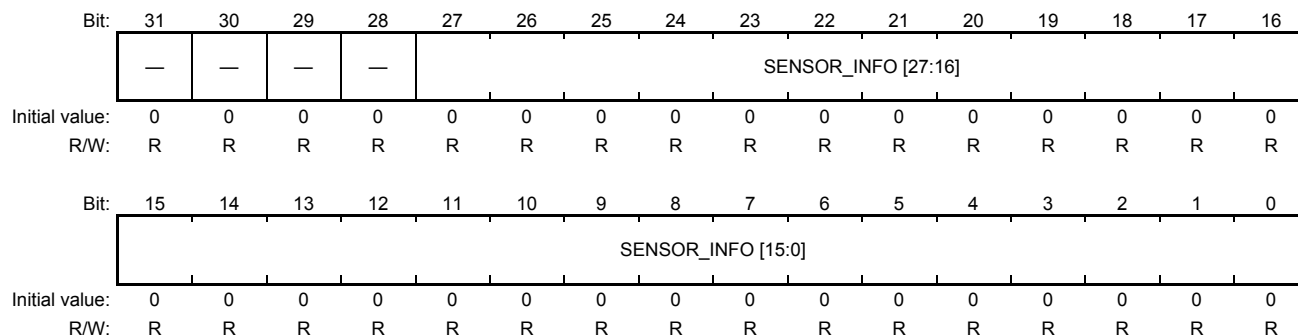
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√



Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28 to 16	POSX0[12:0]	All 0	R/W	Set the value INT (FD1_RPF_SIZE.HSIZE/3) to this bit.
15 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12 to 0	POSX1[12:0]	All 0	R/W	Set the value INT (2 × FD1_RPF_SIZE.HSIZE/3) to this bit.

**27.3.11.17 Sensor Register (FD1\_SENSOR\_m: m = 0, 1, ... 17)**

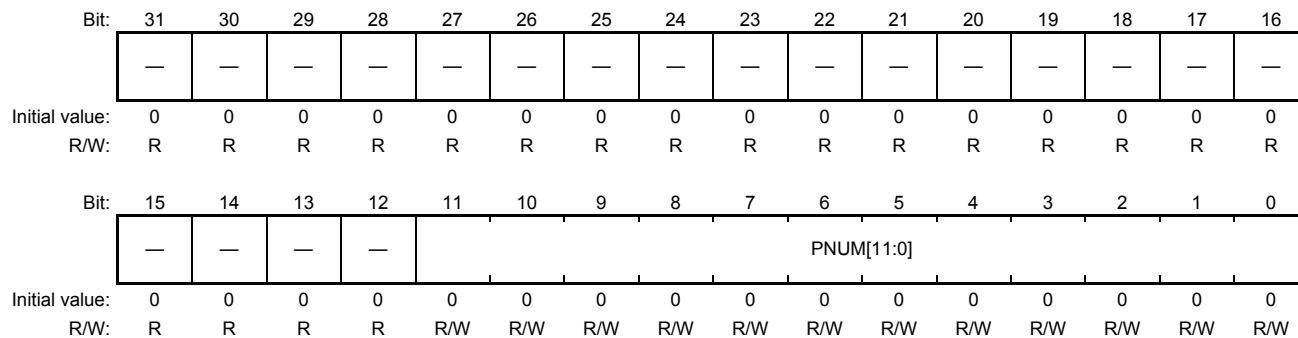
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√



Bit	Bit Name	Initial Value	R/W	Description
31 to 28	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
27 to 0	SENSOR_IN FO[27:0]	H'000 0000	R	Sensor information of FDP1

**27.3.11.18 Line Memory Pixel Number Register (FD1\_IPC\_LMEM)**

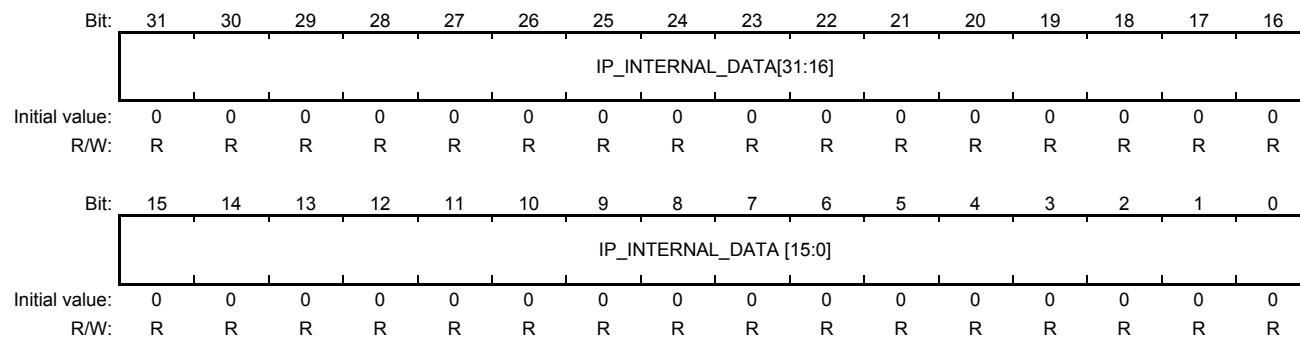
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√



Bit	Bit Name	Initial Value	R/W	Description
31 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11 to 0	PNUM[11:0]	H'000	R/W	Specify 1024 in decimal (H'400)

**27.3.11.19 IP Internal Data Register (FD1\_IP\_INDATA)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√



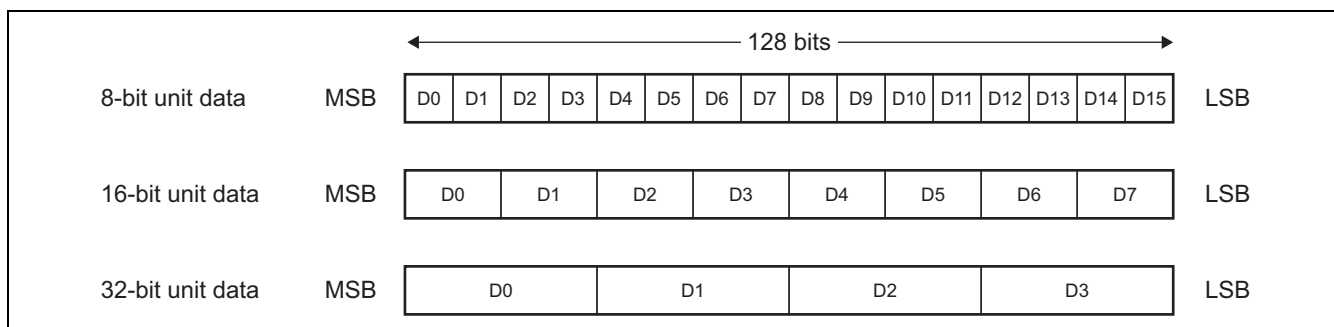
Bit	Bit Name	Initial Value	R/W	Description
31 to 0	IP_INTERNA L_DATA [31:0]	All 0	R	Internal data



<b>RZ/G1H</b>	<b>RZ/G1N</b>
<b>RZ/G1M</b>	<b>RZ/G1E</b>

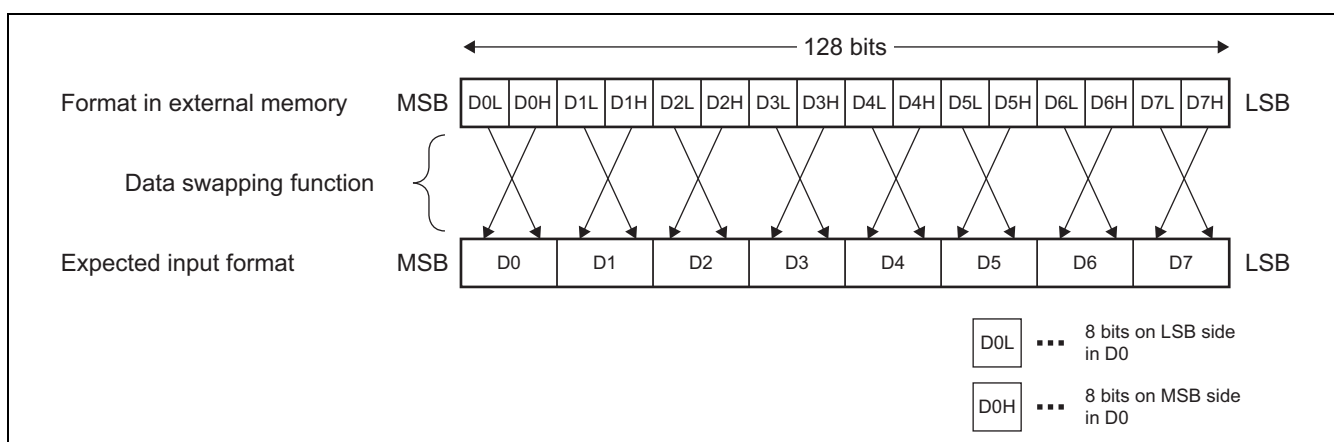
### 27.4 Input/Output Data Format

The FDP1 input/output data should be stored in a format where the address is incremented in the direction from the MSB to the LSB as in big endian. For example, the FDP1 reads and writes data to and from the external memory through the dedicated bus interface with a 128-bit width, and the data that should come first should be stored in the MSB side regardless of the unit data size as shown in Figure 27.10.



**Figure 27.10 FDP1 Input/Output Data Format**

However, data may be arranged in a way unexpected by the FDP1 depending on the address handling method (such as little endian) of the FDP1 access destination in some cases as in the external memory format shown in Figure 27.10. In such a case, use the data swapping function (refer to sections 27.3.9.6 and 27.3.10.5) in the FDP1 to convert the data format to be suitable for the FDP1.



**Figure 27.11 Input Data Alignment by Data Swapping Function**

## 27.5 Lookup Table (LUT) Setting

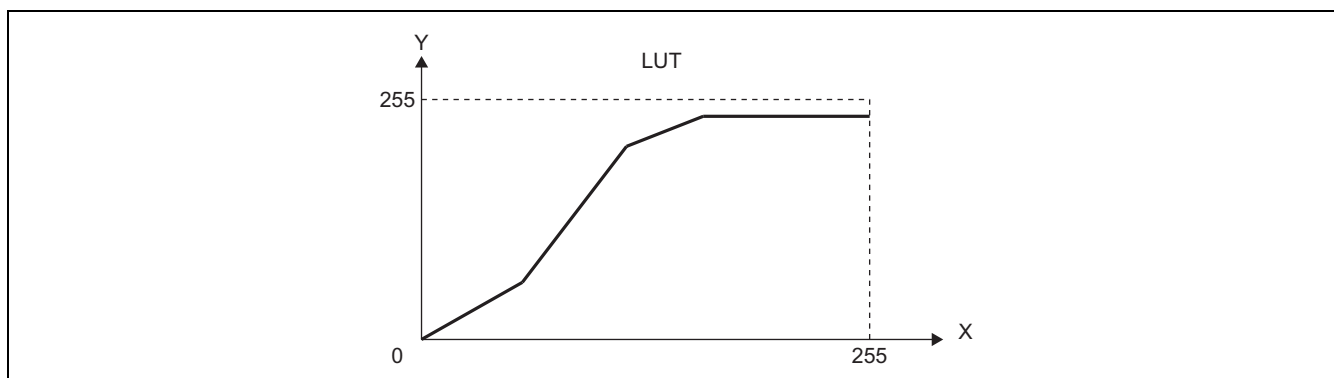
RZ/G1H	RZ/G1N
RZ/G1M	RZ/G1E

FDP1 has the lookup tables (LUT) shown in Table 27.12 to change the characteristic of the de-interlacing function. The LUT is an 8-bit entry and 8-bit output table. Note that users can access to LUT only by 32 bits access. Do not access other bit length such as 8 bits access or 16 bits access. LUT behaves like immediate registers described in section 27.3.2, so do not change the value in LUT while FDP1 is under processing.

**Table 27.12 List of LUT**

LUT Name
DIF_ADJ
SAD_ADJ
BLD_GAIN
DIF_GAIN
MDET

The LUT is used for making the non-linear characteristic shown in Figure 27.12 where X and Y are input and output of LUT respectively.



**Figure 27.12. LUT for Changing the De-Interlacing Characteristic**

For MDET-LUT, the 2D interpolating likelihood is the input to the LUT and the blending coefficient (Alpha) is the output from the LUT. The final output image is expressed by the following equation.

$$(\text{Output image}) = (\text{Alpha}/255) \times (2\text{D interpolated image}) + ((255-\text{Alpha})/255) \times (3\text{D interpolated image})$$

When the output value of the LUT is set to 0 for all input value, the output image from FDP1 is always 3D interpolated image in spite of the motion in the video.

Table 27.13 indicates the setting of each LUT. Note that other setting is used for purpose of h/w debugging. Do not set other value to LUT except for MDET.

Table 27.13 Meaning of X/Y Axis of LUT

Index	DIF_ADJ []	SAD_ADJ []	BLD_GAIN []	DIF_GAIN []	MDET []
0	H'00	H'00	H'80	H'80	H'00
1	H'24	H'24	H'80	H'80	H'01
2	H'43	H'43	H'80	H'80	H'02
3	H'5E	H'5E	H'80	H'80	H'03
4	H'76	H'76	H'80	H'80	H'04
5	H'8C	H'8C	H'80	H'80	H'05
6	H'9E	H'9E	H'80	H'80	H'06
7	H'AF	H'AF	H'80	H'80	H'07
8	H'BD	H'BD	H'80	H'80	H'08
9	H'C9	H'C9	H'80	H'80	H'09
10	H'D4	H'D4	H'80	H'80	H'0A
11	H'DD	H'DD	H'80	H'80	H'0B
12	H'E4	H'E4	H'80	H'80	H'0C
13	H'EA	H'EA	H'80	H'80	H'0D
14	H'EF	H'EF	H'80	H'80	H'0E
15	H'F3	H'F3	H'80	H'80	H'0F
16	H'F6	H'F6	H'80	H'80	H'10
17	H'F9	H'F9	H'80	H'80	H'11
18	H'FB	H'FB	H'80	H'80	H'12
19	H'FC	H'FC	H'80	H'80	H'13
20	H'FD	H'FD	H'80	H'80	H'14
21	H'FE	H'FE	H'80	H'80	H'15
22	H'FE	H'FE	H'80	H'80	H'16
23	H'FF	H'FF	H'80	H'80	H'17
24	H'FF	H'FF	H'80	H'80	H'18
25	H'FF	H'FF	H'80	H'80	H'19
26	H'FF	H'FF	H'80	H'80	H'1A
27	H'FF	H'FF	H'80	H'80	H'1B
28	H'FF	H'FF	H'80	H'80	H'1C
29	H'FF	H'FF	H'80	H'80	H'1D
30	H'FF	H'FF	H'80	H'80	H'1E
31	H'FF	H'FF	H'80	H'80	H'1F
32	H'FF	H'FF	H'80	H'80	H'20
33	H'FF	H'FF	H'80	H'80	H'21
34	H'FF	H'FF	H'80	H'80	H'22
35	H'FF	H'FF	H'80	H'80	H'23
36	H'FF	H'FF	H'80	H'80	H'24
37	H'FF	H'FF	H'80	H'80	H'25
38	H'FF	H'FF	H'80	H'80	H'26
39	H'FF	H'FF	H'80	H'80	H'27
40	H'FF	H'FF	H'80	H'80	H'28
41	H'FF	H'FF	H'80	H'80	H'29

Index	DIF_ADJ []	SAD_ADJ []	BLD_GAIN []	DIF_GAIN []	MDET []
42	H'FF	H'FF	H'80	H'80	H'2A
43	H'FF	H'FF	H'80	H'80	H'2B
44	H'FF	H'FF	H'80	H'80	H'2C
45	H'FF	H'FF	H'80	H'80	H'2D
46	H'FF	H'FF	H'80	H'80	H'2E
47	H'FF	H'FF	H'80	H'80	H'2F
48	H'FF	H'FF	H'80	H'80	H'30
49	H'FF	H'FF	H'80	H'80	H'31
50	H'FF	H'FF	H'80	H'80	H'32
51	H'FF	H'FF	H'80	H'80	H'33
52	H'FF	H'FF	H'80	H'80	H'34
53	H'FF	H'FF	H'80	H'80	H'35
54	H'FF	H'FF	H'80	H'80	H'36
55	H'FF	H'FF	H'80	H'80	H'37
56	H'FF	H'FF	H'80	H'80	H'38
57	H'FF	H'FF	H'80	H'80	H'39
58	H'FF	H'FF	H'80	H'80	H'3A
59	H'FF	H'FF	H'80	H'80	H'3B
60	H'FF	H'FF	H'80	H'80	H'3C
61	H'FF	H'FF	H'80	H'80	H'3D
62	H'FF	H'FF	H'80	H'80	H'3E
63	H'FF	H'FF	H'80	H'80	H'3F
64	H'FF	H'FF	H'80	H'80	H'40
65	H'FF	H'FF	H'80	H'80	H'41
66	H'FF	H'FF	H'80	H'80	H'42
67	H'FF	H'FF	H'80	H'80	H'43
68	H'FF	H'FF	H'80	H'80	H'44
69	H'FF	H'FF	H'80	H'80	H'45
70	H'FF	H'FF	H'80	H'80	H'46
71	H'FF	H'FF	H'80	H'80	H'47
72	H'FF	H'FF	H'80	H'80	H'48
73	H'FF	H'FF	H'80	H'80	H'49
74	H'FF	H'FF	H'80	H'80	H'4A
75	H'FF	H'FF	H'80	H'80	H'4B
76	H'FF	H'FF	H'80	H'80	H'4C
77	H'FF	H'FF	H'80	H'80	H'4D
78	H'FF	H'FF	H'80	H'80	H'4E
79	H'FF	H'FF	H'80	H'80	H'4F
80	H'FF	H'FF	H'80	H'80	H'50
81	H'FF	H'FF	H'80	H'80	H'51
82	H'FF	H'FF	H'80	H'80	H'52
83	H'FF	H'FF	H'80	H'80	H'53
84	H'FF	H'FF	H'80	H'80	H'54
85	H'FF	H'FF	H'80	H'80	H'55

Index	DIF_ADJ []	SAD_ADJ []	BLD_GAIN []	DIF_GAIN []	MDET []
86	H'FF	H'FF	H'80	H'80	H'56
87	H'FF	H'FF	H'80	H'80	H'57
88	H'FF	H'FF	H'80	H'80	H'58
89	H'FF	H'FF	H'80	H'80	H'59
90	H'FF	H'FF	H'80	H'80	H'5A
91	H'FF	H'FF	H'80	H'80	H'5B
92	H'FF	H'FF	H'80	H'80	H'5C
93	H'FF	H'FF	H'80	H'80	H'5D
94	H'FF	H'FF	H'80	H'80	H'5E
95	H'FF	H'FF	H'80	H'80	H'5F
96	H'FF	H'FF	H'80	H'80	H'60
97	H'FF	H'FF	H'80	H'80	H'61
98	H'FF	H'FF	H'80	H'80	H'62
99	H'FF	H'FF	H'80	H'80	H'63
100	H'FF	H'FF	H'80	H'80	H'64
101	H'FF	H'FF	H'80	H'80	H'65
102	H'FF	H'FF	H'80	H'80	H'66
103	H'FF	H'FF	H'80	H'80	H'67
104	H'FF	H'FF	H'80	H'80	H'68
105	H'FF	H'FF	H'80	H'80	H'69
106	H'FF	H'FF	H'80	H'80	H'6A
107	H'FF	H'FF	H'80	H'80	H'6B
108	H'FF	H'FF	H'80	H'80	H'6C
109	H'FF	H'FF	H'80	H'80	H'6D
110	H'FF	H'FF	H'80	H'80	H'6E
111	H'FF	H'FF	H'80	H'80	H'6F
112	H'FF	H'FF	H'80	H'80	H'70
113	H'FF	H'FF	H'80	H'80	H'71
114	H'FF	H'FF	H'80	H'80	H'72
115	H'FF	H'FF	H'80	H'80	H'73
116	H'FF	H'FF	H'80	H'80	H'74
117	H'FF	H'FF	H'80	H'80	H'75
118	H'FF	H'FF	H'80	H'80	H'76
119	H'FF	H'FF	H'80	H'80	H'77
120	H'FF	H'FF	H'80	H'80	H'78
121	H'FF	H'FF	H'80	H'80	H'79
122	H'FF	H'FF	H'80	H'80	H'7A
123	H'FF	H'FF	H'80	H'80	H'7B
124	H'FF	H'FF	H'80	H'80	H'7C
125	H'FF	H'FF	H'80	H'80	H'7D
126	H'FF	H'FF	H'80	H'80	H'7E
127	H'FF	H'FF	H'80	H'80	H'7F
128	H'FF	H'FF	H'80	H'80	H'80
129	H'FF	H'FF	H'80	H'80	H'81

Index	DIF_ADJ []	SAD_ADJ []	BLD_GAIN []	DIF_GAIN []	MDET []
130	H'FF	H'FF	H'80	H'80	H'82
131	H'FF	H'FF	H'80	H'80	H'83
132	H'FF	H'FF	H'80	H'80	H'84
133	H'FF	H'FF	H'80	H'80	H'85
134	H'FF	H'FF	H'80	H'80	H'86
135	H'FF	H'FF	H'80	H'80	H'87
136	H'FF	H'FF	H'80	H'80	H'88
137	H'FF	H'FF	H'80	H'80	H'89
138	H'FF	H'FF	H'80	H'80	H'8A
139	H'FF	H'FF	H'80	H'80	H'8B
140	H'FF	H'FF	H'80	H'80	H'8C
141	H'FF	H'FF	H'80	H'80	H'8D
142	H'FF	H'FF	H'80	H'80	H'8E
143	H'FF	H'FF	H'80	H'80	H'8F
144	H'FF	H'FF	H'80	H'80	H'90
145	H'FF	H'FF	H'80	H'80	H'91
146	H'FF	H'FF	H'80	H'80	H'92
147	H'FF	H'FF	H'80	H'80	H'93
148	H'FF	H'FF	H'80	H'80	H'94
149	H'FF	H'FF	H'80	H'80	H'95
150	H'FF	H'FF	H'80	H'80	H'96
151	H'FF	H'FF	H'80	H'80	H'97
152	H'FF	H'FF	H'80	H'80	H'98
153	H'FF	H'FF	H'80	H'80	H'99
154	H'FF	H'FF	H'80	H'80	H'9A
155	H'FF	H'FF	H'80	H'80	H'9B
156	H'FF	H'FF	H'80	H'80	H'9C
157	H'FF	H'FF	H'80	H'80	H'9D
158	H'FF	H'FF	H'80	H'80	H'9E
159	H'FF	H'FF	H'80	H'80	H'9F
160	H'FF	H'FF	H'80	H'80	H'A0
161	H'FF	H'FF	H'80	H'80	H'A1
162	H'FF	H'FF	H'80	H'80	H'A2
163	H'FF	H'FF	H'80	H'80	H'A3
164	H'FF	H'FF	H'80	H'80	H'A4
165	H'FF	H'FF	H'80	H'80	H'A5
166	H'FF	H'FF	H'80	H'80	H'A6
167	H'FF	H'FF	H'80	H'80	H'A7
168	H'FF	H'FF	H'80	H'80	H'A8
169	H'FF	H'FF	H'80	H'80	H'A9
170	H'FF	H'FF	H'80	H'80	H'AA
171	H'FF	H'FF	H'80	H'80	H'AB
172	H'FF	H'FF	H'80	H'80	H'AC
173	H'FF	H'FF	H'80	H'80	H'AD

Index	DIF_ADJ []	SAD_ADJ []	BLD_GAIN []	DIF_GAIN []	MDET []
174	H'FF	H'FF	H'80	H'80	H'AE
175	H'FF	H'FF	H'80	H'80	H'AF
176	H'FF	H'FF	H'80	H'80	H'B0
177	H'FF	H'FF	H'80	H'80	H'B1
178	H'FF	H'FF	H'80	H'80	H'B2
179	H'FF	H'FF	H'80	H'80	H'B3
180	H'FF	H'FF	H'80	H'80	H'B4
181	H'FF	H'FF	H'80	H'80	H'B5
182	H'FF	H'FF	H'80	H'80	H'B6
183	H'FF	H'FF	H'80	H'80	H'B7
184	H'FF	H'FF	H'80	H'80	H'B8
185	H'FF	H'FF	H'80	H'80	H'B9
186	H'FF	H'FF	H'80	H'80	H'BA
187	H'FF	H'FF	H'80	H'80	H'BB
188	H'FF	H'FF	H'80	H'80	H'BC
189	H'FF	H'FF	H'80	H'80	H'BD
190	H'FF	H'FF	H'80	H'80	H'BE
191	H'FF	H'FF	H'80	H'80	H'BF
192	H'FF	H'FF	H'80	H'80	H'C0
193	H'FF	H'FF	H'80	H'80	H'C1
194	H'FF	H'FF	H'80	H'80	H'C2
195	H'FF	H'FF	H'80	H'80	H'C3
196	H'FF	H'FF	H'80	H'80	H'C4
197	H'FF	H'FF	H'80	H'80	H'C5
198	H'FF	H'FF	H'80	H'80	H'C6
199	H'FF	H'FF	H'80	H'80	H'C7
200	H'FF	H'FF	H'80	H'80	H'C8
201	H'FF	H'FF	H'80	H'80	H'C9
202	H'FF	H'FF	H'80	H'80	H'CA
203	H'FF	H'FF	H'80	H'80	H'CB
204	H'FF	H'FF	H'80	H'80	H'CC
205	H'FF	H'FF	H'80	H'80	H'CD
206	H'FF	H'FF	H'80	H'80	H'CE
207	H'FF	H'FF	H'80	H'80	H'CF
208	H'FF	H'FF	H'80	H'80	H'D0
209	H'FF	H'FF	H'80	H'80	H'D1
210	H'FF	H'FF	H'80	H'80	H'D2
211	H'FF	H'FF	H'80	H'80	H'D3
212	H'FF	H'FF	H'80	H'80	H'D4
213	H'FF	H'FF	H'80	H'80	H'D5
214	H'FF	H'FF	H'80	H'80	H'D6
215	H'FF	H'FF	H'80	H'80	H'D7
216	H'FF	H'FF	H'80	H'80	H'D8
217	H'FF	H'FF	H'80	H'80	H'D9

Index	DIF_ADJ []	SAD_ADJ []	BLD_GAIN []	DIF_GAIN []	MDET []
218	H'FF	H'FF	H'80	H'80	H'DA
219	H'FF	H'FF	H'80	H'80	H'DB
220	H'FF	H'FF	H'80	H'80	H'DC
221	H'FF	H'FF	H'80	H'80	H'DD
222	H'FF	H'FF	H'80	H'80	H'DE
223	H'FF	H'FF	H'80	H'80	H'DF
224	H'FF	H'FF	H'80	H'80	H'E0
225	H'FF	H'FF	H'80	H'80	H'E1
226	H'FF	H'FF	H'80	H'80	H'E2
227	H'FF	H'FF	H'80	H'80	H'E3
228	H'FF	H'FF	H'80	H'80	H'E4
229	H'FF	H'FF	H'80	H'80	H'E5
230	H'FF	H'FF	H'80	H'80	H'E6
231	H'FF	H'FF	H'80	H'80	H'E7
232	H'FF	H'FF	H'80	H'80	H'E8
233	H'FF	H'FF	H'80	H'80	H'E9
234	H'FF	H'FF	H'80	H'80	H'EA
235	H'FF	H'FF	H'80	H'80	H'EB
236	H'FF	H'FF	H'80	H'80	H'EC
237	H'FF	H'FF	H'80	H'80	H'ED
238	H'FF	H'FF	H'80	H'80	H'EE
239	H'FF	H'FF	H'80	H'80	H'EF
240	H'FF	H'FF	H'80	H'80	H'F0
241	H'FF	H'FF	H'80	H'80	H'F1
242	H'FF	H'FF	H'80	H'80	H'F2
243	H'FF	H'FF	H'80	H'80	H'F3
244	H'FF	H'FF	H'80	H'80	H'F4
245	H'FF	H'FF	H'80	H'80	H'F5
246	H'FF	H'FF	H'80	H'80	H'F6
247	H'FF	H'FF	H'80	H'80	H'F7
248	H'FF	H'FF	H'80	H'80	H'F8
249	H'FF	H'FF	H'80	H'80	H'F9
250	H'FF	H'FF	H'80	H'80	H'FA
251	H'FF	H'FF	H'80	H'80	H'FB
252	H'FF	H'FF	H'80	H'80	H'FC
253	H'FF	H'FF	H'80	H'80	H'FD
254	H'FF	H'FF	H'80	H'80	H'FE
255	H'FF	H'FF	H'80	H'80	H'FF



## 28. VSP1

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

This section describes the configurations of VSP1 on this LSI. Descriptions in this section show the full-function specifications of the VSP1 IP. Some of the functions described in this section are not available on VSP1 with restrictions written here.

### Configurations of VSP1

This LSI incorporates three different types of VSP1 modules (VSPR, VSPS, VSPD) as image processing systems.

**VSPR:** VSPR stands for VSP for “Resizing”. [RZ/G1H only]

**VSPS:** VSPS stands for VSP Standard which supports various functions of the VSP1 IP.

**VSPD:** VSPD stands for VSP for the display unit (DU) which outputs the display data to DU directly. Two channels are supported for RZ/G1H/M/N. Single channel is supported for RZ/G1E.

Tables 28.1 to 28.3 show the restrictions of each type of VSP1 unit on this LSI.

All the registers and functions listed in Tables 28.1 to 28.3 should be treated as un-implemented functions in each VSP1 unit. Do not set any registers related to the restricted function without any statement.

**Table 28.1 VSPS Configuration [RZ/G1H/M/N/E]**

Category	Restriction Target	Restriction Description
Module	LIF	[RZ/G1H only]
	UDS1-2 [RZ/G1M/N/E]	LIF is not implemented on VSPS. Functions and registers cannot be used. In addition, a setting of DPR routing with LIF is prohibited. [RZ/G1M/N/E] These modules listed at left column are not implemented on VSPS. Functions and registers cannot be used. In addition, a setting of DPR routing with these modules is prohibited.
Function	RPF/CLUT	CLUT is only available on RPF ch1 and ch2 (not available on ch0, ch3, and ch4). Related register: VI6_RPFn_INFMT.RDFMT, VI6_CLUT0_TBL*, VI6_CLUT3_TBL*, VI6_CLUT4_TBL*

**Table 28.2 VSPR Configuration [RZ/G1H Only]**

Category	Restriction Target	Restriction Description
Module	CLU	These modules listed at left column are not implemented on VSPR. Functions and registers cannot be used. In addition, a setting of DPR routing with these modules is prohibited.
	LUT	
	UDS1-2	
	HGO	
	HGT	
	LIF	
Function	RPF/CLUT	CLUT is only available on RPF ch2 (not available on ch0, ch1, ch3, and ch4). Related register: VI6_RPFn_INFMT.RDFMT, VI6_CLUT0_TBL*, VI6_CLUT1_TBL*, VI6_CLUT3_TBL*, VI6_CLUT4_TBL*

**Table 28.3 VSPD Configuration [RZ/G1H/M/N/E]**

Category	Restriction Target	Restriction Description
Module	RPF4	These modules listed at left column are not implemented on VSPD. Functions and registers cannot be used. In addition, a setting of DPR routing with these modules is prohibited.
	CLU	
	UDS1-2	
	SRU	
	WPF1-3	
	HGT	
Function	RPF/CLUT	CLUT is only available on RPF ch2 (not available on ch0, ch1, and ch3). Related register: VI6_RPFn_INFMT.RDFMT, VI6_CLUT0_TBL*, VI6_CLUT1_TBL*, VI6_CLUT3_TBL*
	WPF/Vertical Flipping	Vertical flipping function is not implemented. Related register: VI6_WPF0_OUTFMT.FLP

## Preface

### Terminology

The terminology for VSP1. Refer to section 28.1, Overview for detail.

#### Read Pixel Formatter (RPF)

The RPF can read image data from external memory such as SDRAM. The RPF supplies image data to the internal sub modules in VSP1. At the same time, RPF can execute format conversion, color space conversion and color keying for each input image source. There are five RPFs in VSP1, and each RPF is called as RPF0, RPF1 and so on.

#### Virtual RPF

There is an image compositing sub module named as BRU which can execute image blending or raster operation. The BRU has 4 input ports for compositing multiple images. There must be a RPF module as the start of data processing. Each RPF can be a source of data input to BRU. In addition to these RPF modules, the BRU has a function which generates monochrome color image internally. This functionality is useful because the data access to an external memory is not required. This function is called as virtual RPF.

Refer to sections 28.2.8.1, 28.2.16.2, 28.2.16.3 and 28.2.16.4 for virtual RPF.

#### Write Pixel Formatter (WPF)

The WPF can input image data from internal image processing and output to the external memory such as SDRAM. At the same time, the WPF can execute color space conversion and format conversion. There are four WPFs in VSP1, and each WPF is called as WPF0, WPF1 and so on. The start of VSP1 equals to the start of each WPF by setting registers shown in section 28.2.5.1.

#### Target WPF

The VSP1 has five RPFs (RPF 0 to 4) and four WPFs (WPF0 to 3) and execute image processing. One data path consists of more than one RPF, one WPF and other image functional modules if necessary. The WPF which is reached from specific RPF(s) in the data path is called as target WPF for the RPF(s). The number of target WPFs is always one for the data path.

#### Source RPF

The data source in the data path for the specific WPF is called as source RPF for that WPF. The number of source RPFs is not always one, may be more than one for image blend operation or raster operation.

#### Layer

In case of image composite operation such as image blending or raster operation for multiple images, there is hierarchical relationship for each image. One layer is assigned to one RPF or one virtual RPF indicating one image in hierarchical relationship.

#### Master Layer

The master layer is a base layer for image compositing of multiple images, and the size of the master layer equals to that of BRU output. When the image compositing is not applied, there is one layer. This layer is also called as the master layer.

#### Sub Layer

The Layers except the master layer are called as sub layer.

### Alpha

The VSP1 can execute both color data and its transparent data. The alpha is 8-bit data and expresses the transparency of pixel. The value H'FF represents opaque pixel, and the value H'00 represents transparent pixel.

### Plane

One layer consists of color components such as R/G/B or Y/Cb/Cr, and alpha data representing its transparency of the pixel. The frame which is one of color components and alpha data is called as a plane.

### Picture Plane

The picture plane represents color data in one layer.

### Alpha Plane

The alpha plane represents transparent data in one layer.

### Blending

The image blending means the image composite operation with alpha data. The composite ratio of image blending depends on the relationship of each layer and alpha values.

### Raster Operation (ROP)

The bitwise operation such as AND or OR is called as raster operation (ROP).

### Color Space Conversion (CSC)

The CSC means the conversion of YCbCr, RGB and HSV color spaces.

### **Definition of operators and functions**

The following operators, notations are defined for explaining the functions of VSP1.

$\langle x \rangle$

Discard decimal places of value x

H'

The notation “H” is used as prefix for hexadecimal numbers. For example, H'80 means 80 in hexadecimal and 128 in decimal.

B'

The notation “B” is used as prefix for binary numbers. For example, B'10000000 means 80 in hexadecimal and 128 in decimal. When a number is used without prefix, it means decimal number.

—

The notation “\_” is used as a separator of binary digit for binary number. There is no functional and logical meaning. The meaning of B'10101 and B'1\_0101 is the same.

[msb:lsb]

This notation specifies a part of bits or all bits of registers and signals. For example, eval[3:0] means bit 3 to 0 of the signal or register which name is “eval” .

clip0 (x)

Clip to 0 value if x is less than 0. [  $x = (x < 0)? 0 : x$  ]

clip3 (min, max, x)

The value x shall be clipped so that x shall be  $min < x < max$ .

[  $x = (x < min)? min : ((x > max)? max : x)$  ]

### **Unit**

The unit is defined here for explaining VSP1’s functions.

[bpp] : bits per pixel

VSP1 can handle a number of image formats. Each image format has different number of data bits. The unit [bpp] shows a number of data bits for one pixel. For example, RGB 8 bpp means that its format is RGB and the pixel consists of 8 data bits.

## 28.1 Overview

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

The VSP1 is the successor IP of Renesas' VIO6-IP series which supports image processing such as image enhancing, up/down scaling, color management function with lookup tables, image blending.

### 28.1.1 Features

1. Supports Various Data Formats and Conversion
  - Supports YCbCr444/422/420, RGB,  $\alpha$ RGB,  $\alpha$  plane
  - Color space conversion and changes to the number of colors by dithering
  - Color keying
  - Vertical flipping
2. Full HD Video Processing
  - Up and down scaling with arbitrary scaling ratio
  - Super resolution processing
  - Blending of four picture layers and raster operations (ROPs)
3. Full HD Picture Quality/Color Correction
  - $\gamma$  correction and gain correction
  - Correction of color (to adjust skin tones or colors in memory)
  - Hue, brightness, and saturation adjustment
  - 1D and 2D histogram
4. Direct Connection to Display Module
  - Display Unit (DU) supported

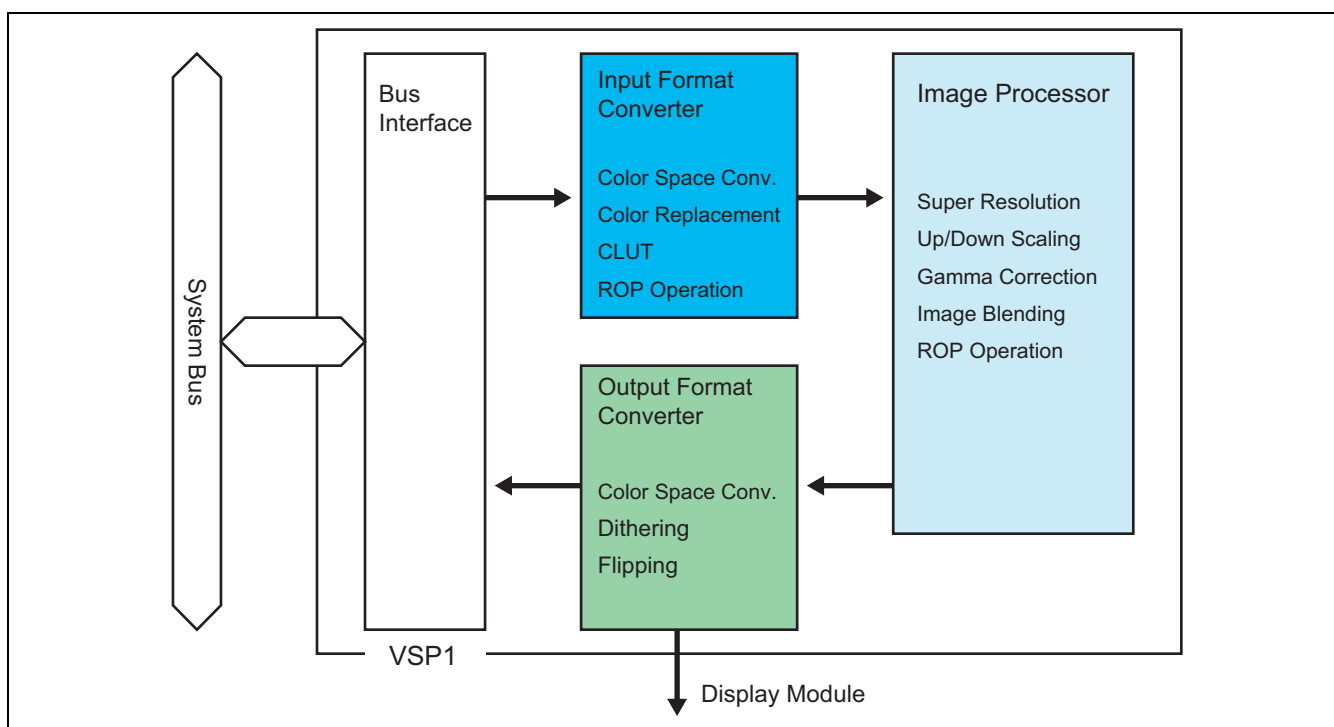
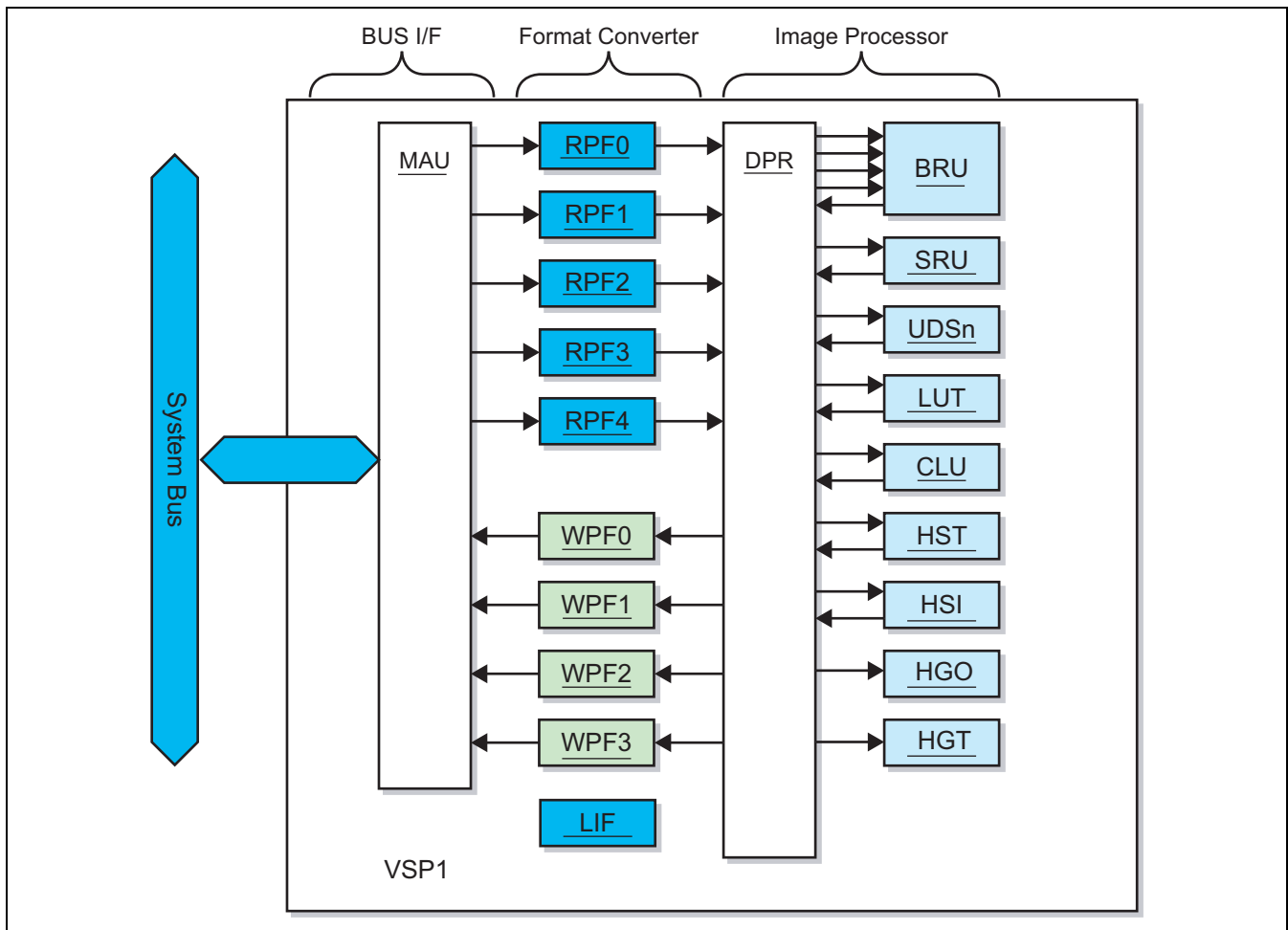


Figure 28.1 Top Level Architecture of VSP1

### 28.1.2 VSP1 Architecture

Figure 28.2 shows the configuration of VSP1 sub modules.



**Figure 28.2 VSP1 Module Configuration**

The following gives an overview of each block function shown in Figure 28.2. The operation of these functions is determined by the register setting explained in section 28.2. Refer to section 28.2 for the relationship between the register setting and the functional behavior.

**(1) Memory Access Unit (MAU)**

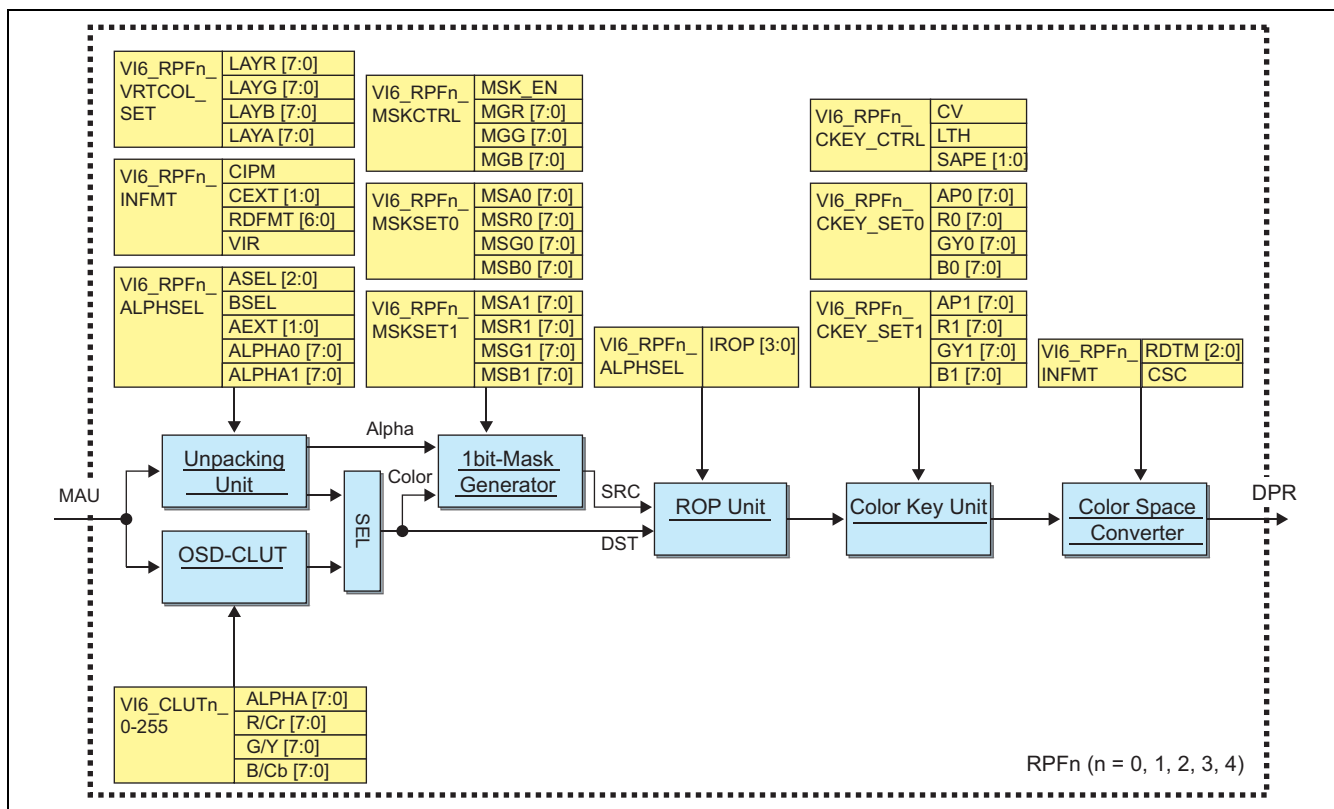
The VSP1 applies processing to the image data stored in the external memory and writes the resultant data back to the external memory. The data transfer between the external memory and VSP1 necessary for this operation is done by the MAU, which works as the bus master, according to the register settings. The MAU executes this data transfer between the external memory and VSP1.

**(2) Command Transfer Unit (CTU)**

The VSP1 can directly read register parameters for image processing by display lists stored in external memory. The CTU module is a bus interface and controls display lists when the CTU reads display lists as a bus master.

**(3) Read Pixel Formatter (RPF)**

The RPF reads image data from the external memory through the MAU, unpacks data according to the specified format, converts the color space, converts the number of colors, executes color keying, ROP operation, and OSD processing, and outputs the resultant data to the DPR. The RPF has an input format unpacking unit, an index color expanding unit (OSD-CLUT), a 1-bit mask generator, a raster operation unit (ROP unit), a color keying unit, and a color space converter. Figure 28.3 shows the processing flow in the RPF.



**Figure 28.3 RPF Processing Flow**

The input format unpacking unit and index color expanding unit (OSD-CLUT) expand the image data input from the MAU into the image format for internal processing, and the 1-bit mask generator generates a 1-bit image mask from the image data expanded through the unpacking unit and OSD-CLUT. Alternately, a 1-bit image mask can be generated from the alpha plane that is different from the picture plane read through the MAU.

The raster operation unit (ROP unit) executes raster operation between the data from the 1-bit mask generator and the image data expanded from the input format, and the color keying unit applies color replacement and specifies the transparent color for the image data input from the ROP unit. The color space converter converts the color space (RGB-YCbCr) of the image data input from the color keying unit as necessary.



The VSP1 provides maximum five RPF modules (RPF0 to RPF4). The implementation of OSD-CLUT depends on the configuration of each LSI.

#### **(4) Data Path Router (DPR)**

The DPR controls the data paths among RPFs, function modules, and WPFs. The DPR selects one of the images input from RPFs, outputs it to a function module (BRU, SRU, UDS<sub>n</sub> (n = 0 to 2), MED, LUT, CLU, HST, HSI, HGO, HGT or ILV), and selects one of WPFs as the destination where the image data processed in the function module will be output. Before output to the WPF, the output from each function module can be input to another function module, which enables multiple image processing functions to be executed continuously without involving the external memory.

#### **(5) Super Resolution Unit (SRU)**

The SRU is a module connected to the DPR, which executes the super resolution processing.

#### **(6) Up/Down Scaler (UDS)**

The UDS is a module connected to the DPR, which upscales or downscales the image size. It can also upscale or downscale the alpha value.

#### **(7) LUT (LookUp Table)**

This is a 1D-LUT that converts each of three color components by using a lookup table. The LUT is connected to the DPR and can be used for gamma correction, negative-positive conversion, posterization, and binarization through desired tone curve settings.

### (8) Blend ROP Unit (BRU)

The BRU is a module connected to the DPR, which executes the image blending processing and ROP operation. The BRU has four blend/ROP operation units (blend/ROP unit m, m = A to D), an ROP operation unit, a blend/ROP input switch (SEL) for selecting the input to these operation units, and a divider for normalization (div unit).

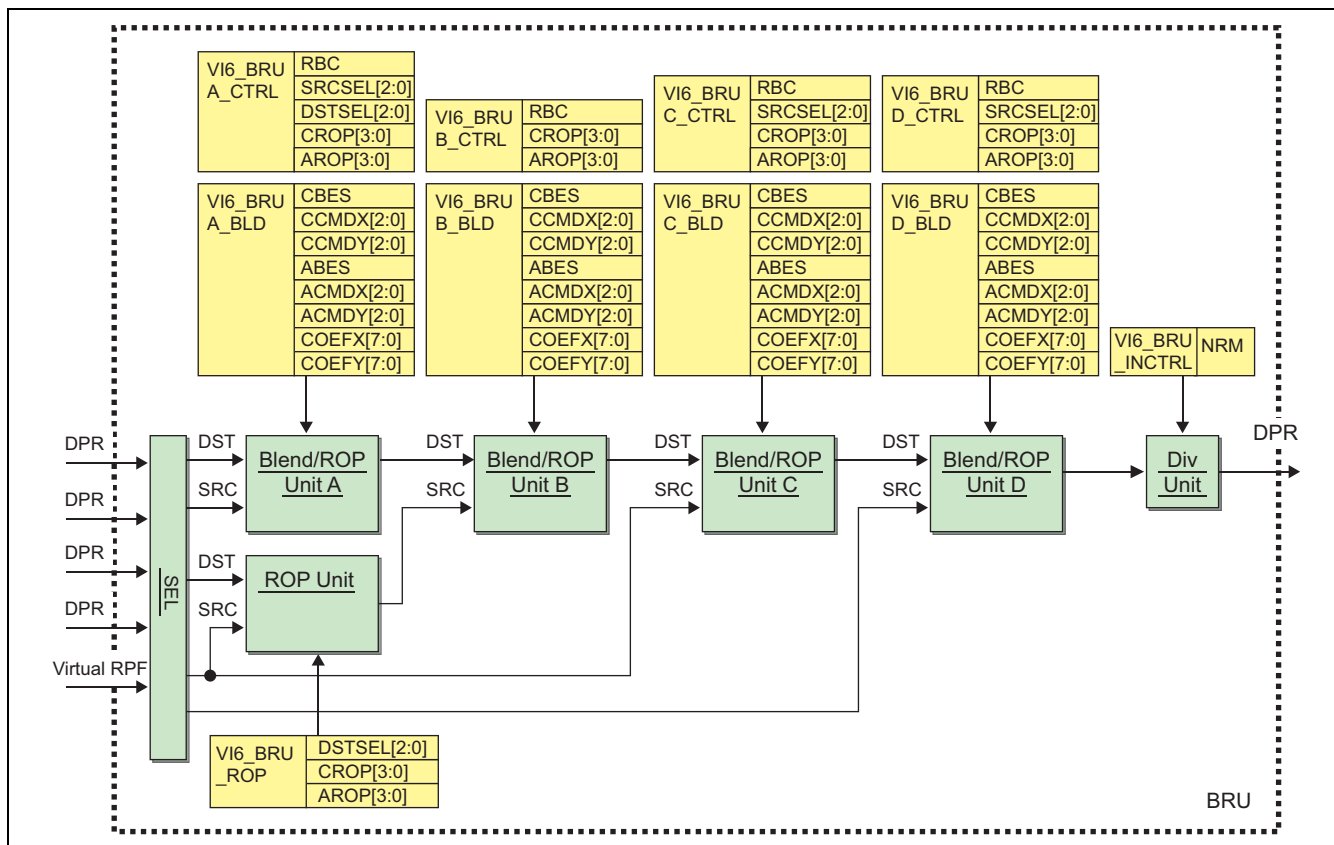


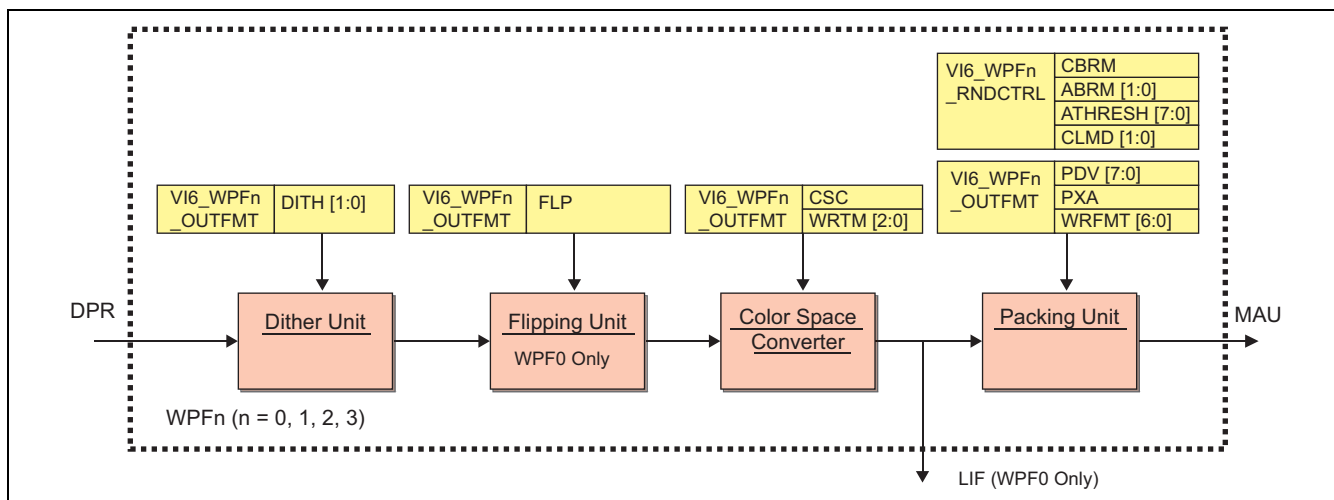
Figure 28.4 BRU Processing Flow

Each of the four blend-ROP operation units (blend/ROP unit m) receives the output from the SEL, blend/ROP Unit m, or ROP unit, and executes blending or raster operation (ROP) of images. The ROP unit receives the output from the SEL and executes 2-input raster operation (ROP2). By combining the ROP operation in the blend/ROP unit m and ROP2 operation in the ROP unit, 256-type 3-input raster operation (ROP3) can be implemented.

The divider for normalization (div unit) divides the pixel value by the  $\alpha$  value.

### (9) Write Pixel Formatter (WPF)

The WPF is an output module that receives image data from the DPR, converts the color space, number of colors, and format of the data, and outputs the results of VSP1 image processing to external memory through the MAU. The WPF is mainly configured from a color space converter and an output format converter (the packing unit).



**Figure 28.5 WPF Processing Flow**

The color space converter converts the color space between RGB and YCbCr, and the packing unit converts the format into the picture plane storing format. The VSP1 provides maximum four WPFs (WPF0 to WPF3). The WPF0 has the output to LIF module after the color space conversion for transferring the video data to the display module.

#### (10) Cubic LookUp table (CLU)

This is a three-dimensional LUT (3D-LUT) that converts the input three-color-component data into desired three color components by using a lookup table. The 1D-LUT can only control each of three color components separately, but the 3D-LUT can convert a specified color into a different color. The CLU is connected to the DPR and can be used for specific color adjustment, such as correction to memorable color.

#### (11) Hue Saturation value Transform (HST)

The HST is a module connected to the DPR, which converts the RGB color space into the HSV color space. The HSV color space can represent a color with the hue, saturation, and value (brightness), and it makes color control through the LUT easier than in the RGB color space.

#### (12) Hue Saturation value Inverse transform (HSI)

The HSI is a module connected to the DPR, which converts the HSV color space into the RGB color space. It executes conversion in the direction opposite to that of the HST.

#### (13) Histogram Generator-One dimension (HGO)

The HGO is a module connected to the DPR and generates the one-dimensional histogram for the dynamic gamma correction. There is no output port of the image data. The middleware of the dynamic gamma correction will be released by Renesas.

#### (14) Histogram Generator-Two dimension (HGT)

The HGT is a module connected to the DPR and generates the two-dimensional histogram for the dynamic color correction. There is no output port of the image data. The middleware of the dynamic color correction will be released by Renesas.

#### (15) Lcdc InterFace (LIF)

The LIF module is used for transferring image data to the display module such as DU (Display Unit). The input port of the LIF module is connected to WPF0, and the output port of the LIF module is connected to DU.

### 28.1.3 Function List

Table 28.4 shows a functional overview of the VSP1 module.

**Table 28.4 Functional Overview of VSP1**

<b>Data Transfer Function</b>			
Bus interface	Data alignment	Conversion method	Byte, Word, LW, or LLW data swapping
	Data alignment	Channel	Data alignment can be specified separately for each input/output channel
	Input	Address setting	1-byte units
Image memory	Output	Address setting	1-byte units
	Output	Memory area	Images can be written to the same memory area where the master layer is stored.
	Supported by RPF0 to RPF4		Note the restrictions shown in Table 28.5.
Tile transfer mode		Interleaved, planer, or semi-planer	
<b>Read Pixel Formatter (RPF)</b>			
Number of channels		Five channels (RPF0 to RPF4)	
Image format	Input	RGB	RGB888, RGB565, RGB666, αRGB8888, αRGB4444, αRGB1555, α plane (8 bpp, 1 bpp)
		YCbCr	YCbCr4:4:4/YCbCr4:2:2/YCbCr4:2:0 α plane (8 bpp, 1 bpp)
		Maximum size	8,190 × 8,190 pixels. The internal data path modules have separate restrictions on the maximum image size. For details, refer to Table 28.6.
		Minimum size	1 × 1 pixel The internal data path modules have separate restrictions on the minimum image size. For details, refer to Table 28.6.
		Size setting unit	YCbCr420: 2-pixel units both horizontally and vertically. YCbCr422: 2-pixel units horizontally and 1-pixel units vertically. In other formats, the size can be set in 1-pixel units.
Color keying	Color replacement	Compared data	RGB888 or Y
		Replaced data	αRGB8888 or αYCbCr
		Comparison Mode	Matched color mode
		Input source	RPF0 to RPF4
	Transparent color	Compared data	RGB888 or Y
		Replaced data	α
		Comparison Mode	Matched color mode, luma threshold mode
		Input source	RPF0 to RPF4
OSD/CLUT	Format	Memory storage format	8 bpp
		Image format	αRGB32 or αYCbCr32
	Input channel	RPF0 to RPF4	

**Read Pixel Formatter (RPF)**

Raster operation	ROP2 (within input channels)	Operator	16 types (OpenGL2.0 is supported)
		Sources of operation	ROP2 operation between the 1-bpp $\alpha$ plane and RGB/YCbCr data in RPF0 to RPF4. Note that 1-bpp $\alpha$ is converted to $\alpha$ RGB888 or $\alpha$ YCbCr4:4:4.
Color space conversion	RGB to YCbCr	Conversion expression	RGB (0, 255) to BT601 (16, 235/240) RGB (0, 255) to BT709 (16, 235/240) RGB (0, 255) to BT601 (0, 255) RGB (16, 235) to BT709 (16, 235/240)
		Target of conversion	RPF0 to RPF4
	YCbCr to RGB	Conversion expression	BT.601 (16, 235/240) to RGB (0, 255) BT.709 (16, 235/240) to RGB (0, 255) BT.601 (0, 255) to RGB (0, 255) BT.709 (16, 235/240) to RGB (16, 235)
		Target of conversion	RPF0 to RPF4
Changing number of colors	Reducing RGB color depth	Target format	RGB666, RGB565, RGB555, RGB444, or RGB332
		Target of conversion	RPF0 to RPF4
	Increasing RGB color depth		Padded with 0. Copied from the most significant bits.
	YCbCr444 generation		CbCr copying or CbCr vertical copying and horizontal interpolation.
Virtual display	RPF0 to RPF4	Color format	$\alpha$ RGB8888 or $\alpha$ YCbCr4:4:4 single-color
		Display size	Same as the size of the input channel
	Virtual RPF	Color format	$\alpha$ RGB8888 or $\alpha$ YCbCr4:4:4 single-color
		Display size	Maximum: 8,190 × 8,190 pixels Minimum: 4 × 4 pixels
$\alpha$ bit count conversion	Input	Bit increase	Padded with 0. Copied from the most significant bits.

**Write Pixel Formatter (WPF)**

Number of channels			Four channels (WPF0 to WPF3)
Image format	Output	RGB	RGB332, RGB444, RGB565, RGB666, RGB888, αRGB8666, αRGB8888, αRGB4444, αRGB1555
		YCbCr	YCbCr4:4:4, YCbCr4:2:2, YCbCr4:2:0
		Maximum size	2,048 × 2,048 The internal data path modules have separate restrictions on the maximum image size. For details, refer to Table 28.6.
		Minimum size	1 × 1 pixel The internal data path modules have separate restrictions on the minimum image size. For details, refer to Table 28.6.
		Size setting unit	YCbCr420: 2-pixel units both horizontally and vertically. YCbCr422: 2-pixel units horizontally and 1-pixel units vertically. In other formats, the size can be set in 1-pixel units.
Color space conversion	RGB to YCbCr	Conversion expression	RGB (0, 255) to BT.601 (16, 235/240) RGB (0, 255) to BT.709 (16, 235/240) RGB (0, 255) to BT.601 (0, 255) RGB (16, 235) to BT.709 (16, 235/240)
		Target of conversion	WPF0 to WPF3
	YCbCr to RGB	Conversion expression	BT.601 (16, 235/240) to RGB (0, 255) BT.709 (16, 235/240) to RGB (0, 255) BT.601 (0, 255) to RGB (0, 255) BT.709 (16, 235/240) to RGB (16, 235)
		Target of conversion	WPF0 to WPF3
Changing number of colors	Output	Reducing RGB color depth	Dithering, lower-order bit truncation, or rounding
		YCbCr422/420	CbCr skipping or CbCr vertical skipping and horizontal skipping
α bit count conversion	Output	Bit reduction	Truncation, rounding, or comparison with threshold (for 1 bpp)

**Image Compositing**

α blending	Input α value selection	RGB	Pixel α, fixed α value, α plane, or 1-bit α converted from the color specified for pixels
		YCbCr	α plane, fixed α value, or 1-bit α converted from the color specified for pixels
	α blending expression	Plane A: Upper plane Plane B: Lower plane	$x_A + y_B$ , $x_A - y_B$ Coefficients x and y should be selected from the following. Fixed α value, (α for plane A), (1 - α for plane A), (α for plane B), (1 - α for plane B)
α blending	Output α value selection	RGB	Fixed α value, $x \cdot (\alpha \text{ for plane A}) + y \cdot (\alpha \text{ for plane B})$ , $x \cdot (\alpha \text{ for plane A}) - y \cdot (\alpha \text{ for plane B})$ Coefficients x and y should be selected from the following. Fixed α value, (α for plane A), (1 - α for plane A), (α for plane B), (1 - α for plane B)
		Blending planes	Number of planes
		Order of planes	The order of five planes selected from RPF0 to RPF4, virtual RPF, and video processing function output can be changed as desired.
	α plane	Format	8 bpp or 1 bpp (α value can be specified through register)
		Input source	RPF0 to RPF4
	Fixed α value	Format	8 bpp
Input source		RPF0 to RPF4, virtual RPF, or video processing function output	
Raster operation	ROP2 (between input channels)	Operator	16 types (OpenGL2.0 is supported)
		Sources of operation	RPF0 to RPF4, virtual RPF, and video processing function output
		Operation control	RGB/YCbCr and α are operated separately.
	ROP3 (between input channels)	Operator	256-type ROP3 is available by combining ROP2 operations
		Sources of operation	RPF0 to RPF4, virtual RPF, and video processing function output
		Operation control	RGB/YCbCr and α are operated separately.

**Video Processing Functions**

Super resolution	Processing method		Processing within one frame
	Scaling ratio		$\times 1$ (same size) or $\times 2$
	Arbitrary scaling ratio		Super resolution processing can be combined with the arbitrary ratio scaling function.
	$\alpha$ processing		Fixed $\alpha$ output
Scaler with arbitrary scaling ratio	Scaling factor		1/16 to 16
	Scaling ratio setting	Expression	1/[Mant.Frac]
		Precision	Mant = 4 bits, Frac = 12 bits
	$\alpha$ processing		Supported (for scale-up or scale-down to 1/4 to 1/1)
Simultaneous processing	All video processing functions and color adjustment functions can be processed simultaneously (the order of function execution is limited).		

**Color Adjustment Function**

1D-LUT	LUT configuration	Independent R/Y, G/Cb, and B/Cr. 256 entries each
3D-LUT	Number of grid points	$17 \times 17 \times 17$
HSV color space conversion	RGB to HSV	Eight bits each for H/S/V
	HSV to RGB	Eight bits each for H/S/V
1D Histogram	Letter box detection	Supported
	Number of bins	64 for each color component
2D Histogram	Letter box detection	Supported
	Number of hue areas	6
	Number of bins	32 for each hue area

When the data output from the VSP1 is written back to the same memory area where the input data for the VSP1 has been read, the VSP1 has the following restrictions.

1. The access order and format on the frame memory are the same between the input pixels and output pixels.
2. Specifying a larger output image size than the input image size, either vertically or horizontally or both vertically and horizontally, is prohibited.
3. When the YCbCr4:2:0 format is input, operation between color components is prohibited.



These restrictions are summarized in Table 28.5. Refer to the descriptions of the registers related to each restriction. In the table, RPF<sub>m</sub> indicates the RPF<sub>n</sub> that inputs the master layer, and WPF<sub>wb</sub> indicates the WPF<sub>n</sub> that writes back the output image to the source image area for the master layer.

**Table 28.5 Restrictions on Use when Output Data is Written Back to Input Data Area**

No.	Restriction	Related Registers
Restriction 1	The RPF <sub>m</sub> input format and the WPF <sub>wb</sub> output format should be the same.	VI6_RPFn_INFMT.RDFMT VI6_RPFn_INFMT.VIR
	The RPF <sub>m</sub> source image storing address and the WPF <sub>wb</sub> destination address should be the same.	VI6_RPFn_SRCM_ADDR_*
	The RPF <sub>m</sub> source picture memory stride and the WPF <sub>wb</sub> destination memory stride should be the same.	VI6_RPFn_SRCM_PSTRIDE VI6_RPFn_SRCM_ASTRIDE
	The RPF <sub>m</sub> and WPF <sub>wb</sub> data swapping settings should be the same.	VI6_WPFn_DSWAP
	The image vertical flipping function cannot be used if WPF <sub>wb</sub> is WPF0.	VI6_WPFn_OUTFMT.FLP
Restriction 2	Super resolution processing with double scale-up by the SRU is prohibited (super resolution processing of the same size is allowed).	VI6_SRU_CTRL0
	Scale-up and color filling by UDSn is prohibited.	VI6_UDSn_SCALE VI6_UDSn_CLIP_SIZE
	The value of scaling filter horizontal and vertical phase registers should be zero in case of using UDSn.	VI6_UDSn_IPC
	The RPF <sub>m</sub> basic read size and extended read size should be the same.	VI6_RPFn_SRC_BSIZE VI6_RPFn_SRC_ESIZE
Restriction 3*	Color space conversion is prohibited in RPF <sub>m</sub> and WPF <sub>wb</sub> .	VI6_RPFn_INFMT.CSC VI6_WPFn_OUTFMT.CSC
	Use of the CLU is prohibited. Make sure that the CLU is not used in DPR routing.	VI6_DPR_CLU_ROUTE.RT
	NOP should be specified for IROP operation.	VI6_RPFn_ALPH_SEL.IROP
	Color keying is prohibited.	VI6_RPFn_CKEY_CTRL.CV

Note: \* When the input format is not YCbCr4:2:0, restriction 3 in not applied.

### 28.1.4 VSP1 Input Size

Table 28.6 is a list of input size specifications.

**Table 28.6 List of Input Size Specifications**

Module	Min. Input Size	Max. Input Size	Restrictions on Setting Unit
RPF	1 (horizontal) × 1 (vertical) pixel	8,190 (horizontal) × 8,190 (vertical) pixels	<p>YCbCr422: 2-pixel units horizontally and 1-pixel units vertically.</p> <p>YCbCr420: 2-pixel units both horizontally and vertically.</p> <p>Other formats: 1-pixel units both horizontally and vertically.</p> <p>Notes: 1. When the 1-bpp alpha plane*1 is input, the size can always be specified in 8-pixel units both horizontally and vertically regardless of the input format.</p> <p>2. These restrictions including note 1 are applied to the following.</p> <p>VI6_RPFn_SRC_BSIZE</p> <p>VI6_RPFn_SRC_ESIZE</p>
SRU	4 (horizontal) × 4 (vertical) pixels	<p>Without scaling (same size):</p> <p>2,048 (horizontal) × 8,190 (vertical) pixels</p> <p>With double scale-up :</p> <p>1,024 (horizontal) × 4,095 (vertical) pixels</p>	1-pixel units both horizontally and vertically.
UDSn (n = 0, 1, 2)	4 (horizontal) × 4 (vertical) pixels	8,190 (horizontal)*2 × 8,190 (vertical) pixels	1-pixel units both horizontally and vertically.
LUT	1 (horizontal) × 1 (vertical) pixel	8,190 (horizontal) × 8,190 (vertical) pixels	1-pixel units both horizontally and vertically.
CLU	1 (horizontal) × 1 (vertical) pixel	8,190 (horizontal) × 8,190 (vertical) pixels	1-pixel units both horizontally and vertically.
HST	1 (horizontal) × 1 (vertical) pixel	8,190 (horizontal) × 8,190 (vertical) pixels	1-pixel units both horizontally and vertically.
HSI	1 (horizontal) × 1 (vertical) pixel	8,190 (horizontal) × 8,190 (vertical) pixels	1-pixel units both horizontally and vertically.
BRU	1 (horizontal) × 1 (vertical) pixel	8,190 (horizontal) × 8,190 (vertical) pixels	1-pixel units both horizontally and vertically.
HGO	1 (horizontal) × 1 (vertical) pixel	8,190 (horizontal) × 8,190 (vertical) pixels	1-pixel units both horizontally and vertically.
HGT	1 (horizontal) × 1 (vertical) pixel	8,190 (horizontal) × 8,190 (vertical) pixels	1-pixel units both horizontally and vertically.
LIF	1 (horizontal) × 1 (vertical) pixel	8,190 (horizontal) × 8,190 (vertical) pixels	1-pixel units both horizontally and vertically.
WPF	1 (horizontal) × 1 (vertical) pixel	2,048 (horizontal) × 2,048 (vertical) pixels	<p>YCbCr422: 2-pixel units horizontally and 1-pixel units vertically.</p> <p>YCbCr420: 2-pixel units both horizontally and vertically.</p> <p>Other formats: 1-pixel units both horizontally and vertically.</p> <p>Note: This restriction on the WPF only applies to the WPF output size. The WPF input size should be specified in 1-pixel units.</p>

- Notes: 1. When VI6\_RPFn\_ALPH\_SEL.ASEL is set to B'011.  
 2. When the image size is downscaled and the horizontal UDS output size is 2,048 pixels or smaller, the UDS input size can be 2,048 pixels or larger.

The most important restriction shown in Table 28.6 is the setting unit. Make appropriate register settings so that the size of the image input to each module does comply with setting units and does not exceed the limits shown in Table 28.6. Especially for the register settings of SRU and UDSn, where the size can be changed within the modules, be careful not to exceed the input size limit for the module connected behind each of them.

### 28.1.5 VSP1 Output Size

The size of the output from each WPF is determined by the results of processing in the modules connected with the DPR. As shown in Figure 28.2, the data input to the VSP1 is sent to the WPF output modules through the RPF and the modules connected with the DPR. When there is no processing that changes the image size through this data path, the WPF output size is the same as the RPF input size. Table 28.7 is a list of the processing that changes image size.

**Table 28.7 Image Processing that Changes Image Size**

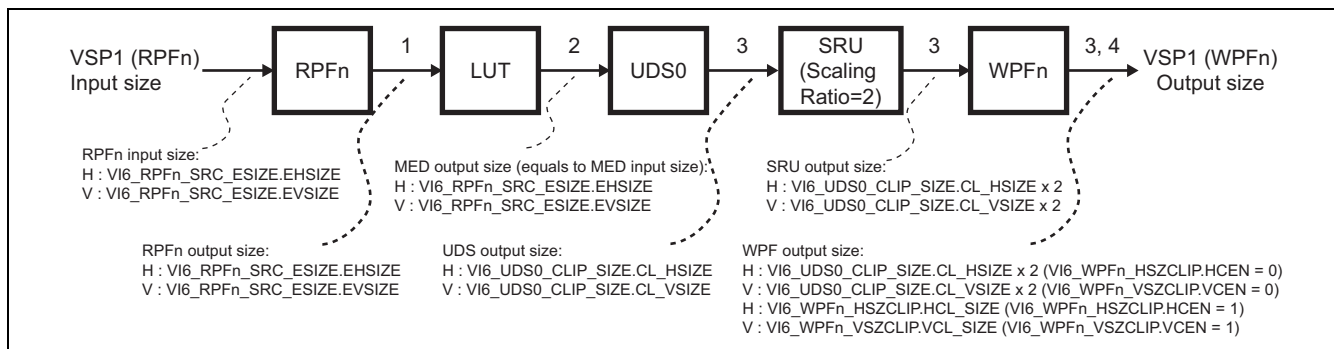
Module	Function*1	Related Register	Size of Output from Module
SRU	Super resolution with double scale-up	VI6_SRU_CTRL0	Super resolution without scaling (same size): Input size Super resolution with double scale-up: Input size × 2
UDSn	Output size clipping	VI6_UDSn_CLIP_SIZE	Horizontal output size: VI6_UDSn_CLIP_SIZE.CL_HSIZE setting Vertical output size: VI6_UDSn_CLIP_SIZE.CL_VSIZE setting
WPF	Input size clipping	VI6_WPFn_HSZCLIP VI6_WPFn_VSZCLIP	When this function is disabled, the input size and the output size are the same. When this function is enabled, the output is in the following size. Horizontal output size: VI6_WPFn_HSZCLIP.HCL_SIZE *2 setting Vertical output size: VI6_WPFn_VSZCLIP.VCL_SIZE *2 setting

- Notes: 1. For details of each function, refer to the descriptions of the related registers.  
 2. Refer to section 28.2.1, Notational Conventions for Registers and Bit Fields for explanation of register bit field.

The input image size can be changed only with the modules and functions shown in Table 28.7. With the other modules and functions, the input size and output size are the same. Accordingly, after module connections with the DPR are determined, the VSP1 output size can also be determined through the following steps.

1. The image size (VI6\_RPFn\_SRC\_ESIZE) read from the external memory and sent to the DPR by the RPFn is the initial value.
2. When the module connected with the DPR is not a module (function) shown in Table 28.7, the output size from the module is the same as the input size; the image size does not need to be updated.
3. When a module connected with the DPR is a module (function) shown in Table 28.7, the output image size should be updated to the size shown in the table, which should be used as the input image size for the module connected behind it.
4. When the final image size at the WPFn is determined, this size is the VSP1 output size for that WPFn path.

Figure 28.6 shows how to determine the image size in a sample DPR connection through the above steps. The related conditions that determine the image size are also shown.

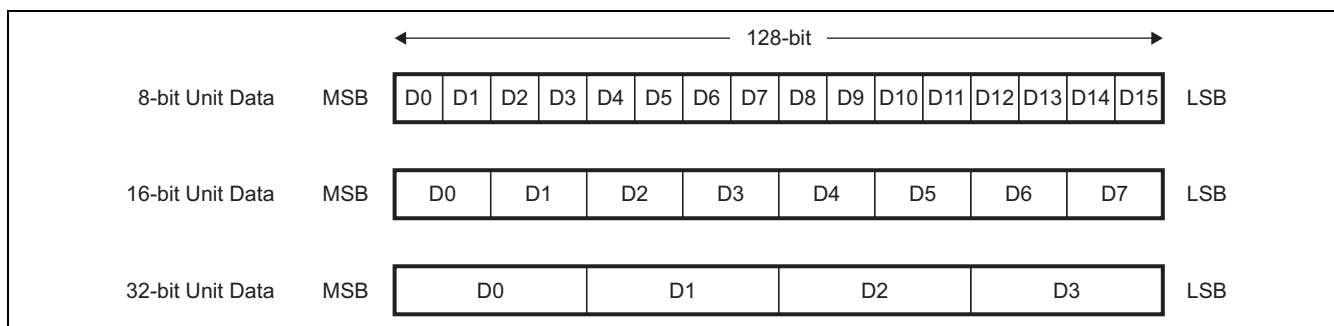


**Figure 28.6 Input/Output Size for Each Module in a Sample DPR Connection**

Make appropriate register settings in each module so that the VSP1 output image size determined as shown in the figure does not violate the restrictions shown in Table 28.7.

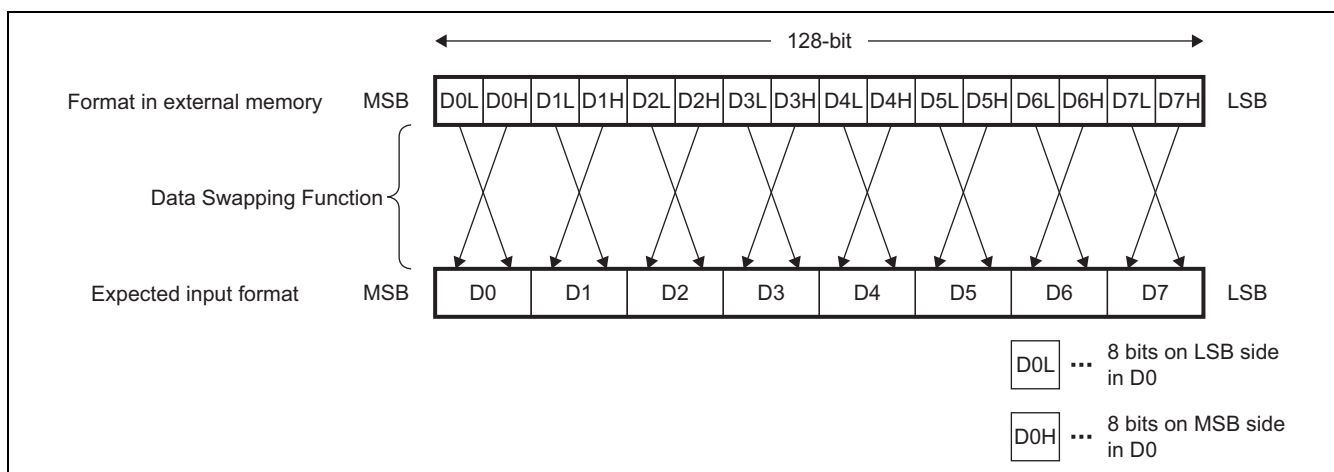
**28.1.6 Input/Output Data Format**

The VSP1 input/output data should be stored in a format where the address is incremented in the direction from the MSB to the LSB as in big endian. For example, the VSP1 reads and writes data to and from the external memory through the dedicated bus interface with a 128-bit width, and the data that should come first should be stored in the MSB side regardless of the unit data size as shown in Figure 28.7.



**Figure 28.7 VSP1 Input/Output Data Format**

However, data may be arranged in a way unexpected by the VSP1 depending on the address handling method (such as little endian) of the VSP1 access destination in some cases as in the external memory format shown in Figure 28.8. In such a case, use the data swapping function (refer to sections 28.2.7.4 and 28.2.8.5) in the VSP1 to convert the data format to be suitable for the VSP1.



**Figure 28.8 Input Data Alignment by Data Swapping Function**

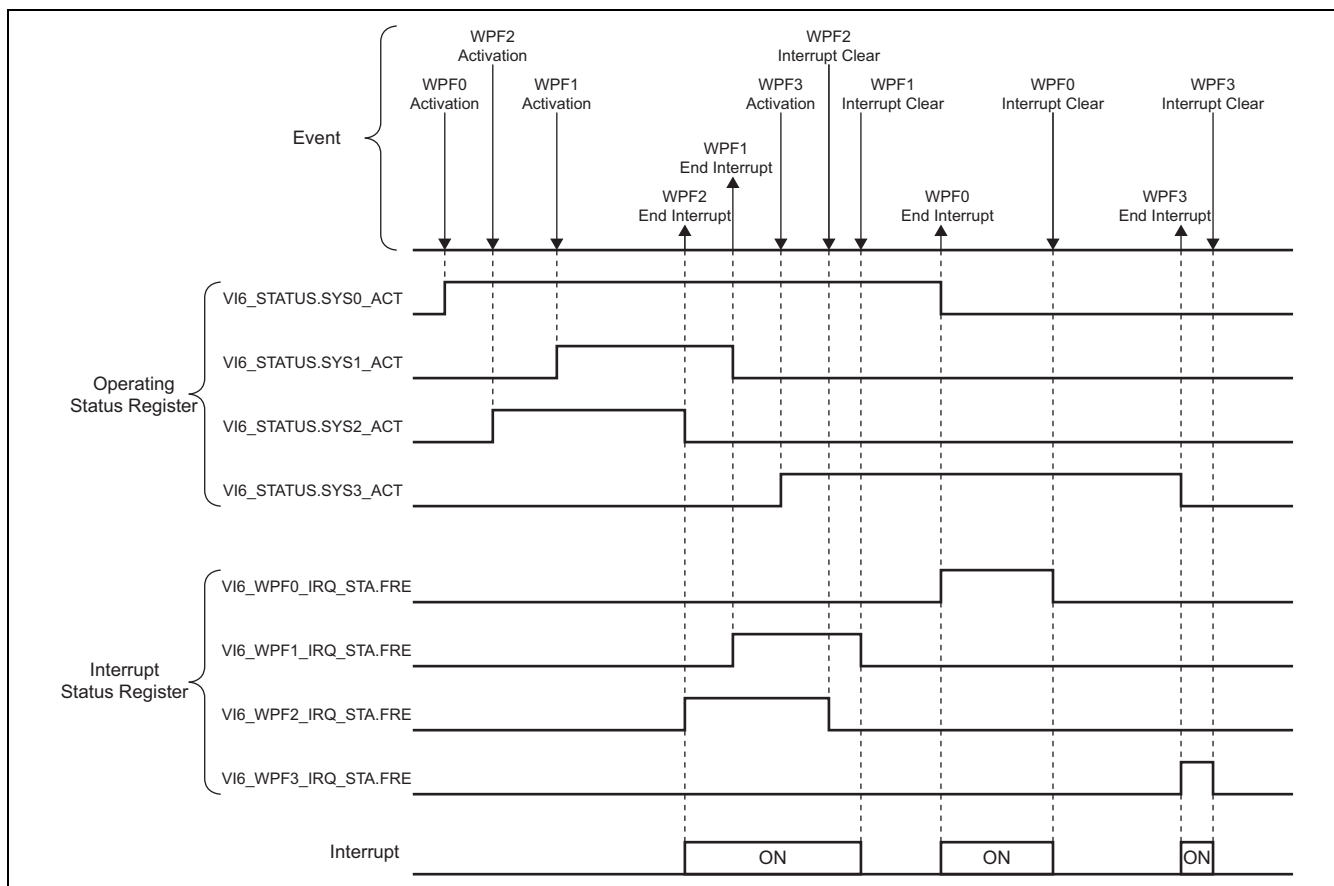
### 28.1.7 Concept of VSP1 Operation Starting and Stopping

The VSP1 provides four channels of image processing. Each channel is started by setting the corresponding start register. Here, starting a processing channel means starting one of WPF0 to WPF3, which are output modules of the VSP1. Use the start registers shown in Table 28.8 to start WPF modules.

After a WPF module is started and specified processing is completed, the corresponding channel stops operation and notifies the end of processing through an end interrupt. End interrupts are generated through the end interrupt source registers shown in Table 28.8; clearing a source register cancels the corresponding interrupt signal (for details of interrupt processing, refer to section 28.1.9, Interrupt Processing). Each of the operating status registers shown in the table indicates the busy state after the corresponding channel is started through the start register until processing is completed and operation stops. Figure 28.9 shows these operation timings.

**Table 28.8 Target Module and Corresponding Registers for Starting and Stopping Operation**

Target Module	Start Register	End Interrupt Source Register	Operating Status Register
WPF0	VI6_CMD0.STRCMD	VI6_WPF0_IRQ_STA. FRE	VI6_STATUS.SYS0_ACT
WPF1	VI6_CMD1.STRCMD	VI6_WPF1_IRQ_STA. FRE	VI6_STATUS.SYS1_ACT
WPF2	VI6_CMD2.STRCMD	VI6_WPF2_IRQ_STA. FRE	VI6_STATUS.SYS2_ACT
WPF3	VI6_CMD3.STRCMD	VI6_WPF3_IRQ_STA. FRE	VI6_STATUS.SYS3_ACT



**Figure 28.9 VSP1 Startup and Status of Each Register and Interrupt**

The following describes the operating states (operating or stopped) of VSP1 internal modules. As described in section 28.1.2, the VSP1 has several image processing modules and the connections between modules are determined by the DPR. Accordingly, the operating state of a module is the same as that of the target WPF for that module. For example, when the target WPF for the CLU is WPF2, the CLU operating state is the same as that of WPF2; that is, the CLU operating state is indicated by the VI6\_STATUS.SYS2\_ACT as shown in Table 28.8 and the status change timing is shown as VI6\_STATUS.SYS 2\_ACT in Figure 28.9. Likewise, the operating states of all modules connected to WPF2 are indicated by VI6\_STATUS.SYS 2\_ACT.

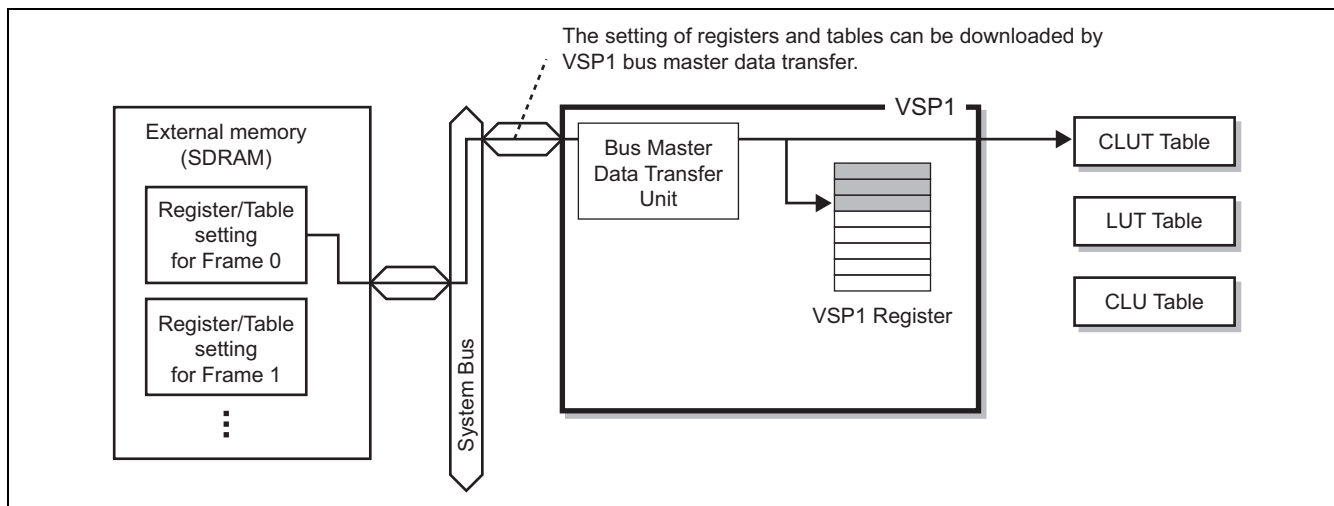
After connections through the DPR are changed and the target WPF for a module is changed, refer to the correct register for the new target WPF to check the operating state of that module. In the above example, after the target WPF for the CLU is changed from WPF2 to WPF0, the CLU operating state is indicated by VI6\_STATUS.SYS 0\_ACT.

Connections should be changed through the DPR-related registers (described later) while all modules to be affected by any change in connections are stopped. If connections through the DPR are changed during operation, the VSP1 will hang.

### 28.1.8 Display List

#### (1) Functional Description

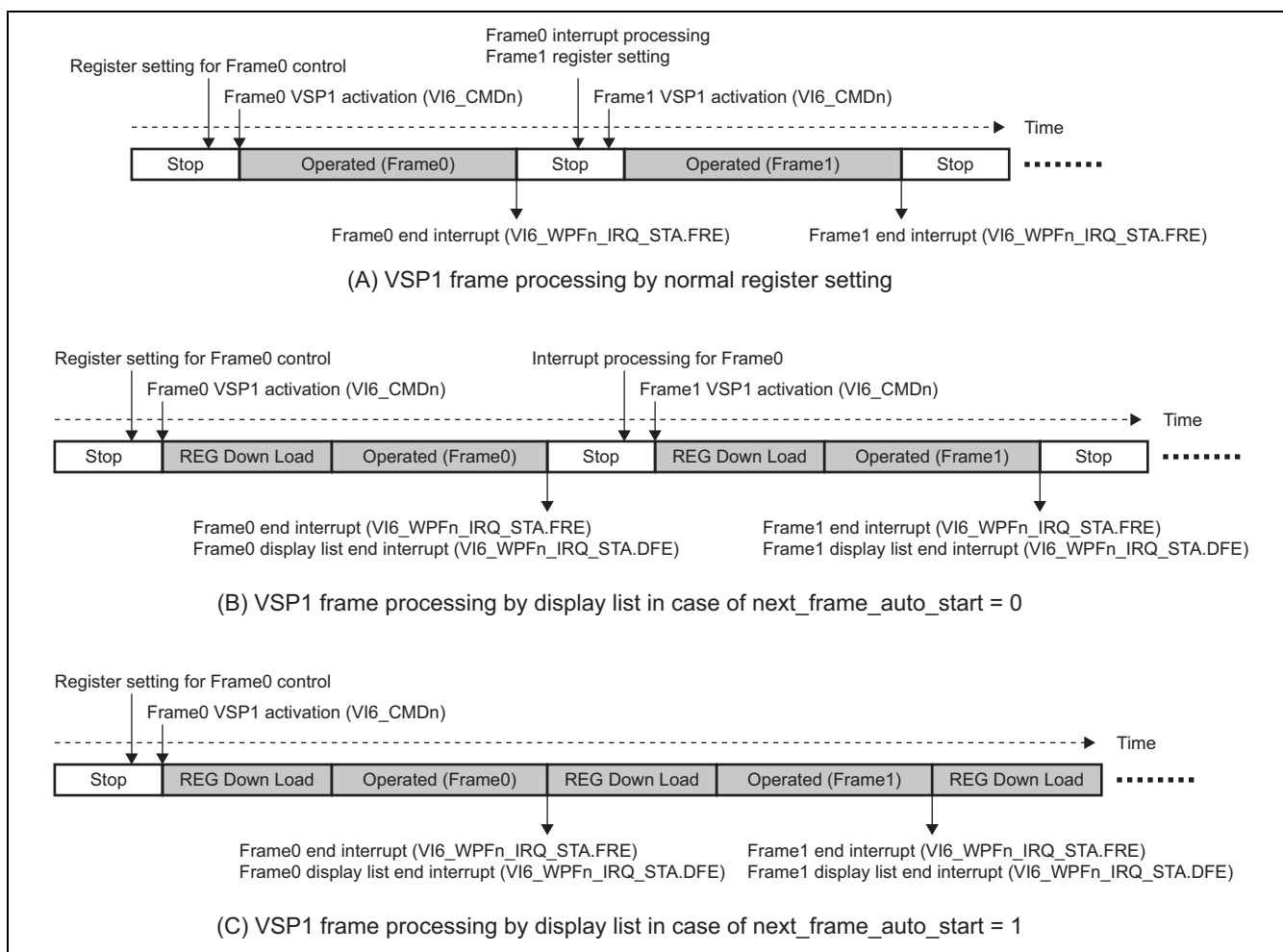
The VSP1 provides the display list function. As a display list, the VSP1 automatically downloads the register settings except for the control registers (sections 28.2.5 and 28.2.6) from external memory and stores the settings in the VSP1 registers. This function is advantageous in that the interrupt processing or register setting modification processing can be executed without CPU intervention during multiple-frame processing because the register settings used for VSP1 processing are prepared in advance in external memory such as SDRAM.



**Figure 28.10 Concept of Display List**

To use display lists, specify the external memory addresses to the display list control registers described in section 28.2.6. The register settings or various types of information should be stored in external memory in the format described in section 28.1.8 (2).

Figure 28.11 shows the difference between VSP1 operation through normal register settings and through display lists.



**Figure 28.11 Comparison of VSP1 Operation between Normal Register Settings and Display Lists**

As shown in Figure 28.11 (A), in the VSP1 processing through normal register settings, all registers should be set up before the VSP1 is started for each frame. After the VSP1 processing is completed, the VSP1 outputs a frame end interrupt (`VI6_WPFn_IRQ_STA.FRE`). This method requires a certain amount of time for register settings or interrupt processing by the CPU between frames. In contrast, when display lists are used, the VSP1 automatically downloads register settings from external memory as shown in Figure 28.11 (B) and (C), which reduces the load on the CPU between frames.

Figure 28.11 (B) shows the display list usage where the VSP1 stops at the end of every frame; only the VSP1 start processing for each frame is done by the CPU. This is suitable for the cases when the CPU controls synchronization of frame processing in frame buffer management or when the amount of register values or table data to be set in the VSP1 is large. In the case shown in Figure 28.11 (C), as soon as the frame processing ends, the VSP1 automatically begins next frame operation and starts downloading new register settings. This is the fastest operation using display lists.

Table 28.9 shows the modes of the display list and the supported functions for each mode. The detail of each mode is described in the following sections.

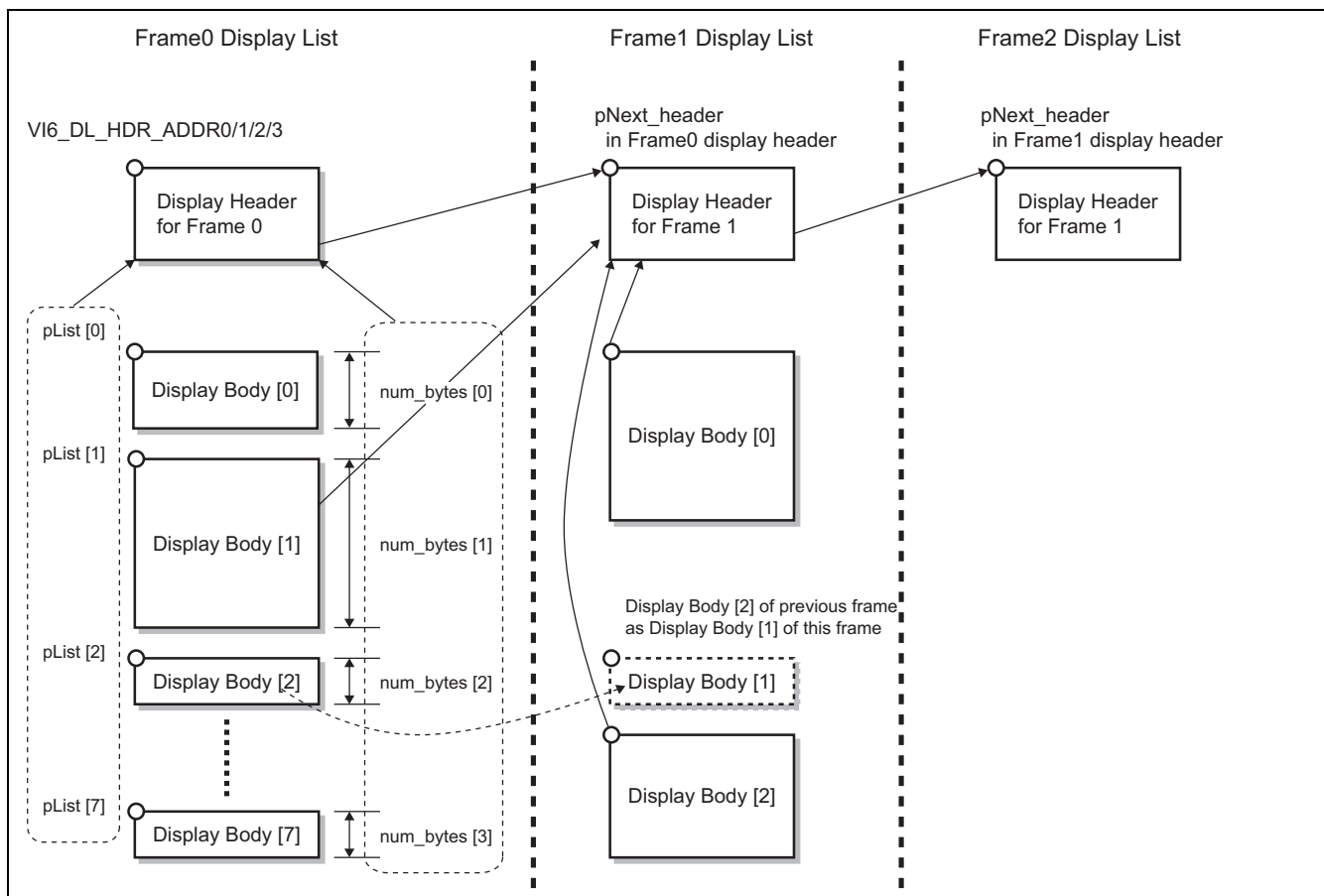
**Table 28.9 Display List Mode and Supported Functions**

Mode	Extended Display List	Continuous Frames
Normal Display List Mode	Supported	Controlled by “ <code>next_frame_auto_start</code> ” in the header of the display list.
Header-less Display List Mode	Not Supported	Controlled by <code>VI6_DL_CTRL.CFM0</code> bit.



## (2) Normal Display List Mode

The VSP1 display lists include control information as well as simple register settings in order to control multiple-frame processing in an optimum way for each application. Figure 28.12 shows the display list structure.



**Figure 28.12 Structure and Concept of VSP1 Display List**

A VSP1 display list consists of two sections; a header section for storing various information and control flags and a body section for storing register and table settings. A combination of these two sections is defined as a display list for a frame. The register and table settings can be divided and stored in up to eight separate bodies allocated in memory. Therefore, the separate bodies storing the register settings for one frame (for example, frame 0) can have non-sequential start addresses; that is, the bodies for one frame can be allocated to areas distant from each other in memory. To gather these bodies and configure the register settings for one frame, a header is used. A display header stores the number of bodies linked with the header and the start address and size of each body.

The VSP1 analyzes the header to gather register and table settings stored in separate memory areas and reconfigure the complete register settings.

The addresses of display headers should be specified in the VSP1 registers described in section 28.2.6. When activated in a mode that uses display lists, the VSP1 downloads display headers from the addresses specified in `VI6_DL_HDR_ADDR0/1/2/3` (numbers 0 to 3 correspond to the WPF channel index numbers), analyzes the numbers of bodies and the address and data size of each body, downloads the bodies, and completes register and table settings. After display list downloading is completed, the VSP1 becomes ready for frame image processing; the VSP1 then starts the actual frame processing.

After processing of a frame ends, the VSP1 proceeds to the next frame processing. Here, there are two modes for starting the next frame processing as shown in Figure 28.11. In one mode, the VSP1 stops operation and waits for the next activation by the CPU in the same way as when display lists are not used. In this mode, the address used for downloading

the display header of the next frame is kept by the internal hardware. Therefore, if valid address information is not stored in the display header for the previous frame, a correct value should be specified in VI6\_DL\_HDR\_ADDR0/1/2/3 while the VSP1 is stopped. When the VSP1 is started after a correct value is specified, the VSP1 starts next frame processing with the same procedure for the previous frame. In contrast to this mode, which stops the VSP1 after the end of one-frame processing, there is another mode for automatically starting next frame processing. In automatic start mode, the VSP1 downloads the next display header as soon as the previous frame processing ends. After downloading ends, the VSP1 starts image processing. The information regarding mode selection, that is, whether to automatically start next frame processing, should be stored in the display header downloaded for the previous frame.

In the automatic start mode, the VSP1 continues processing until the display header for a frame specifies that the next frame should not be started automatically. To stop processing during automatic execution, use a software reset (VI6\_SRESET).

To strictly define the display list format described above, the following shows the grammatical structure of a display list using pseudo-code. First, to simplify the description of the display list format in the following pages, Table 28.10 defines a function. Function `zero_bits (num_bits)` generates a string of one-bit 0s for the number of bits specified by the parameter for the function. By using this function, Table 28.11 defines the header section format of a display list and Table 28.12 defines the body section format.

Table 28.10 Definition of a Function for Simple Description

Syntax	Bit Count
zero_bits (num_bits)	
{	
for (i=0; i<num_bits; i++) {	
<b>zero_bit</b>	1
}	
}	

Bit String	Contents
zero_bit	zero_bit indicates a 1-bit integer having a value of 0.

Table 28.11 Format of Display List Header Section

Syntax	Bit Count
display_header () /* Fixed length */	
{	
zero_bits (29)	
<b>num_list_minus1</b>	3
for (i=0; i<8; i++)	
zero_bits (15)	
<b>num_bytes [i]</b>	17
<b>pList [i]</b>	32
}	
<b>pNext_header</b>	32
zero_bits (30)	
<b>current_frame_int_enable</b>	1
<b>next_frame_auto_start</b> /* 76 bytes from the beginning of this header*/	1
if (VI6_DL_EXT_CTRL.EXT) {	
zero_bits (32) /* padding zero 4 bytes for alignment */	
zero_bits (6)	
<b>pre_ext_dl_exec</b>	1
<b>post_ext_dl_exec</b>	1
zero_bits (8)	
<b>pre_ext_dl_num_cmd</b>	16
<b>pre_ext_dl_pList</b>	32
zero_bits (16)	
<b>post_ext_dl_num_cmd</b>	16
<b>post_ext_dl_pList</b> /* 96 bytes from the beginning of this header*/	32
}	
}	

Bit String	Contents
num_list_minus1	Specifies the value obtained by subtracting 1 from the total number of display list bodies linked with the display header. For example, when this bit field is set to 0, this display list uses one body.
num_bytes [i]	Specifies the number of bytes in the i-th display list body (indicated by index i). Be sure to specify a multiple of eight bytes. For the bodies that are not defined in num_list_minus1 (for example, i = 5 to 7 when num_list_minus1 is set to 4), specify 0.
pList [i]	Specifies the start address of the i-th display list body (indicated by index i). Be sure to specify an address aligned with an 8-byte boundary (the lower-order three bits are 0). For the bodies that are not defined in num_list_minus1 (for example, i = 5 to 7 when num_list_minus1 is set to 4), specify 0.
pNext_header	Specifies the address of the display list header for the next frame. After display list downloading ends, the VSP1 keeps its value in the internal memory and uses it in the next display list header downloading.
current_frame_int_enable	<p>This is a flag that indicates whether to set the display list end interrupt source (VI6_WPFn_IRQ_STA.DFE) to 1 when the current frame processing ends. If this flag is set to 0, the display list end interrupt source (VI6_WPFn_IRQ_STA.DFE) is not set to 1 when one-frame processing by this display header ends. In this state, even if the display list end interrupt is enabled (VI6_WPFn_IRQ_ENB.DFEE is set to 1), no interrupt will be generated.</p> <p>If this flag is set to 1, the display list end interrupt source (VI6_WPFn_IRQ_STA.DFE) is set to 1 when one-frame processing by this display header ends. In this state, if the display list end interrupt is enabled (VI6_WPFn_IRQ_ENB.DFEE is set to 1), the VSP1 generates an interrupt.</p>
Next_frame_auto_start	Enables or disables automatic start of next frame processing when one-frame processing by this display header ends. If this bit is set to 1, the VSP1 starts next frame processing as soon as one-frame processing by this display header ends, and starts downloading the next frame display header from the pNext_header address specified in this display header. If this bit is set to 0, the VSP1 stops operation when one-frame processing by this display header ends. In this case, start the VSP1 through VI6_CMDn to process the next frame.
pre_ext_dl_exec	Enables execution of the extended display list for frame preprocessing when VI6_DL_EXT_CTRL.EXT is 1. If this bit is set to 1, the VSP1 executes the extended display list for frame preprocessing. The VSP1 does not execute it if this bit is set to 0. This bit setting is ignored when VI6_DL_EXT_CTRL.EXT is 0.
post_ext_dl_exec	Enables execution of the extended display list for frame post processing when VI6_DL_EXT_CTRL.EXT is 1. If this bit is set to 1, the VSP1 executes the extended display list for frame post processing. The VSP1 does not execute it if this bit is set to 0. This bit setting is ignored when VI6_DL_EXT_CTRL.EXT is 0.
pre_ext_dl_num_cmd	Specifies the number of commands in the extended display list body section for frame preprocessing when VI6_DL_EXT_CTRL.EXT is 1. The number of commands that can be specified is 1 to 65,535, and a command is 16 bytes. When pre_ext_dl_exec is set to 0, the extended display list for frame preprocessing is not executed; specify 0 in this bit. This bit setting is ignored when VI6_DL_EXT_CTRL.EXT is 0.
pre_ext_dl_pList	Specifies the start address of the area where the extended display list body section for frame preprocessing is stored when VI6_DL_EXT_CTRL.EXT is 1. Be sure to specify an address aligned with a 16-byte boundary (lower-order four bits are 0). When pre_ext_dl_exec is set to 0, the extended display list for frame preprocessing is not executed; specify 0 in this bit. This bit setting is ignored when VI6_DL_EXT_CTRL.EXT is 0.
post_ext_dl_num_cmd	Specifies the number of commands in the extended display list body section for frame post processing when VI6_DL_EXT_CTRL.EXT is 1. The number of commands that can be specified is 1 to 65,535, and a command is 16 bytes. When post_ext_dl_exec is set to 0, the extended display list for frame post processing is not executed; specify 0 in this bit. This bit setting is ignored when VI6_DL_EXT_CTRL.EXT is 0.

Bit String	Contents
post_ext_dl_pList	Specifies the start address of the area where the extended display list body section for frame post processing is stored when VI6_DL_EXT_CTRL.EXT is 1. Be sure to specify an address aligned with a 16-byte boundary (lower-order four bits are 0). When post_ext_dl_exec is set to 0, the extended display list for frame post processing is not executed; specify 0 in this bit. This bit setting is ignored when VI6_DL_EXT_CTRL.EXT is 0.

Table 28.12 Format of Display List Body Section

Syntax	Bit Count
display_list (num_bytes) /* Variable length (num_bytes) */	
for (i=0; i<num_bytes; i+=8) {	
<b>set_address</b>	32
<b>set_data</b>	32
}	
}	

Bit String	Contents
set_address	Specifies the address where the value specified by set_data is to be stored. Specify a register address.
set_data	Specifies the value to be stored in the address specified by set_address. Specify a value to be set in a register.

**Table 28.13 Format of Extended Display List Body Section**

Syntax	Bit width
ext_dl_display_list (num_llw) /* Variable length (pre/post_ext_dl_num_bytes) */	
for (i=0; i<num_llw; i+=2) {	
<b>ext_dl_cmd</b>	64
<b>ext_dl_data</b>	64
}	
}	

Bit string	Contents								
ext_dl_cmd	<p>ext_dl_cmd specifies a 64-bit control command for the extended display list. The upper-order 32 bits hold a command and the lower-order 32 bits are bits for masking or enabling data to be handled by the command. In the upper-order 32 bits (command), bits 63 to 43 should always be set to 0, bits 42 to 40 specify data swapping during command execution (described later), and bits 39 to 32 specify the command type.</p> <p><u>Bit 42: Data swapping in long word (32-bit) units during command execution</u> When this bit is 1, the data read or written for command execution is swapped in long word (32-bit) units.</p> <p><u>Bit 41: Data swapping in word (16-bit) units during command execution</u> When this bit is 1, the data read or written for command execution is swapped in word (16-bit) units.</p> <p><u>Bit 40: Data swapping in byte (8-bit) units during command execution</u> When this bit is 1, the data read or written for command execution is swapped in byte (8-bit) units.</p> <p><u>Bits 39 to 32 are H'00: Write Data</u> The value stored in ext_dl_data [31:0] is written to the address stored in ext_dl_data [63:32] specified after this command. In the lower-order 32 bits of this command (ext_dl_cmd [31:0]), specify the bits whose value should be updated with the value of ext_dl_data [31:0]. Specify 1 for the bits whose value should be updated, and specify 0 for the bits whose current value should be retained.</p> <p><u>Bits 39 to 32 are H'01: Wait Event</u> Until the value stored in the address indicated by ext_dl_data [63:32] specified after this command matches the value stored in ext_dl_data [31:0], processing of this extended display list body section is stalled. The bits used for comparison are masked with the lower-order 32 bits of this command (ext_dl_cmd [31:0]). To compare all bits, the lower-order 32 bits of this command should be set to all 1s.</p>								
ext_dl_data	<p>Specifies the data used by ext_dl_cmd [63:0].</p> <p>When ext_dl_cmd [39:32] is H'0000, specify these bits as follows.</p> <table border="1"> <tr> <td>ext_dl_data [63:32]:</td> <td>Write destination address</td> </tr> <tr> <td>ext_dl_data [31:0]:</td> <td>Write data</td> </tr> </table> <p>When ext_dl_cmd [39:32] is H'0001, specify these bits as follows.</p> <table border="1"> <tr> <td>ext_dl_data [63:32]:</td> <td>Reference address</td> </tr> <tr> <td>ext_dl_data [31:0]:</td> <td>Comparison data</td> </tr> </table>	ext_dl_data [63:32]:	Write destination address	ext_dl_data [31:0]:	Write data	ext_dl_data [63:32]:	Reference address	ext_dl_data [31:0]:	Comparison data
ext_dl_data [63:32]:	Write destination address								
ext_dl_data [31:0]:	Write data								
ext_dl_data [63:32]:	Reference address								
ext_dl_data [31:0]:	Comparison data								

### (3) Header-less Display List Mode

The header-less display list does not have the display header listed in Table 28.11, and it has the simplest structure that has only single body. The extended display list function is not available in case of the header-less display list mode. Set the value 1 to VI6\_DL\_CTRL.NH0 (see section 28.2.6.1) to use the header-less display list. The start address downloaded by the header-less display list should be set to VI6\_DL\_HDR\_ADDR0. And the size of the display body which is originally defined in the display header should be set to VI6\_DL\_BODY\_SIZE0. The header-less display list is available only in WPF0.

### (4) Restrictions on Display List Usage

Access to the general control registers and display list control registers through a display list is prohibited. When using display lists, be sure to observe the following restrictions on register access by the CPU.

1. Do not execute write access to the same register (same address) from the CPU and through a display list at the same time. If such a conflict occurs, correct operation of the VSP1 is not guaranteed.
2. Do not execute write access to the same CLUT, CLU, or LUT lookup table from the CPU and through a display list at the same time. If such a conflict occurs, correct operation of the VSP1 is not guaranteed. Here, the same lookup table means the address space having the same space name shown in Table 28.37 or Table 28.38.
3. When read access by the CPU and write access through a display list to the same register (same address) occur at the same time, the read value returned to the CPU is not guaranteed.
4. When read access by the CPU and write access through a display list to the same CLUT, CLU, or LUT lookup table occur at the same time, the read value returned to the CPU is not guaranteed. Here, the same lookup table means the address space having the same space name shown in Table 28.37 or Table 28.38.
5. For other restrictions on values and timing of register setting through display lists, refer to the restrictions on normal register settings described in section 28.2.3.
6. Manipulation and setting of the registers described in sections 28.2.4 and 28.2.6 through a display list is prohibited.
7. Do not use extended display lists on this LSI.

## 28.1.9 Interrupt Processing

The VSP1 provides multiple image processing channels (WPF0 to WPF3) and they can operate simultaneously in parallel. When a WPF module generates an internal source that should be notified, an interrupt signal is output. As internal sources are generated in each WPF independently, the VSP1 has the following registers to control interrupts in each WPF.

- WPF Interrupt Enable Registers (VI6\_WPFn\_IRQ\_ENB: n = 0, 1, 2, 3) (refer to section 28.2.5.5)
- WPF Interrupt Status Registers (VI6\_WPFn\_IRQ\_STA: n = 0, 1, 2, 3) (refer to section 28.2.5.6)

While multiple WPF modules operate in parallel, they may output interrupt requests at the same time (this is called a multiple interrupt state). Read the WPF Interrupt Status Registers (VI6\_WPFn\_IRQ\_STA: n = 0, 1, 2, 3) in sequence and execute the interrupt response processing for each interrupt source.

Note: To use interrupts, enable them through WPF interrupt enable registers. If an interrupt source register has already been set to 1 for some reason, an unintended interrupt will occur as soon as the corresponding interrupt enable register is set as enabled. To avoid this, before enabling interrupts through WPF interrupt enable registers, be sure to clear all WPF interrupt sources to be enabled to 0. Be careful about this procedure when setting up registers before starting the VSP1.

## 28.2 Registers

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

### 28.2.1 Notational Conventions for Registers and Bit Fields

This document uses the following notational conventions for the VSP1 registers and bit fields.

1. The names of registers and bits are written in uppercase.
2. A bit or bit field in a register is indicated as [register name.bit name]. For example, the STRCMD bit in the VI6\_CMD0 register is indicated as VI6\_CMD0.STRCMD.
3. Lowercase "n" in a register name or a bit name indicates an integer and the range of value n is defined when necessary. For example, VI6\_CMDn.STRCMD (n = 0, 1) indicates the STRCMD bit in two registers VI6\_CMD0.STRCMD and VI6\_CMD1.STRCMD. For RPFn, WPFn, and UDSn, when the range of value n is not defined, RPFn (n = 0, 1, 2, 3, 4), WPFn (n = 0, 1, 2, 3), and UDSn (n = 0, 1, 2) are assumed.
4. In each subsection for register description in section 28.2, when only a bit name is written without showing its register name, the bit is in the register described in that subsection.
5. A wildcard (\*) indicates any characters in a name and represents all registers or bits that match the specified first part of a name. For example, VI6\_RPF\_SRC\_\* indicates both VI6\_RPF\_SRC\_BSIZE and VI6\_RPF\_SRC\_ESIZE register.

### 28.2.2 Register Configuration

The VSP1 registers are arranged in the following order; the general control registers to frame sync control registers control operation of the entire R-VSP1, and the other registers control each image processing and specify parameters for the processing. The functions of the registers are described in this order starting from section 28.2.4.

1. General control registers (VI6\_CMDn (n = 0, 1, 2, 3), VI6\_SRESET, VI6\_STATUS, VI6\_WPFn\_IRQ\_\* (n = 0, 1, 2, 3))
2. Display list control registers (VI6\_DL\_\*)
3. RPF control registers (VI6\_RPFn\_\* (n = 0, 1, 2, 3, 4))
4. WPF control registers (VI6\_WPFn\_\* (n = 0, 1, 2, 3))
5. DPR control registers (VI6\_DPR\_\*)
6. SRU control registers (VI6\_SRU\_\*)
7. UDSn control registers (VI6\_UDSn\_\* (n = 0, 1, 2))
8. LUT control register (VI6\_LUT\_CTRL)
9. CLU control register (VI6\_CLU\_CTRL)
10. HST control register (VI6\_HST\_CTRL)
11. HSI control register (VI6\_HSI\_CTRL)
12. BRU control registers (VI6\_BRU\_\*)
13. HGO control registers (VI6\_HGO\_\*)
14. HGT control registers (VI6\_HGT\_\*)
15. LIF control registers (VI6\_LIF\_\*)
16. Security control registers (VI6\_SECURE\_\*)

The VSP1 has five RPF channels and the register configuration is the same for all of RPF0 to RPF4. However, some bit fields have restrictions in certain RPFs. These restrictions are included in the description of the corresponding bit fields and registers. Likewise, the register configuration is the same for all four WPF channels (WPF0 to WPF3), but some bit fields have restrictions in certain WPFs; the restrictions are included in the description of the corresponding bit fields and registers.

For each register address, refer to section 28.2.4, Memory Map.



### 28.2.3 Restrictions on Access to Registers and Lookup Tables

The VSP1 has control registers and lookup tables. When accessing the addresses where these registers and lookup tables are allocated, the following restrictions should be satisfied. If any restriction is violated, the VSP1 will not operate correctly.

1. For the read-only bits and reserved bits in all VSP1 registers, writing 1 is prohibited unless otherwise specified.
2. Addresses undefined in section 28.2.4, Memory Map, are reserved areas and write access is prohibited in these areas.
3. For all registers and lookup tables, except VI6\_SRESET and VI6\_\*IRQ\*, modifying register values during operation of the module is prohibited. Modify registers while the corresponding module is stopped. For the operating status of the target module, refer to section 28.1.7.

**Table 28.14 Correspondence between Modules and Register Names**

Module Name	Register Name
RPFn (n = 0 to 4)	VI6_RPFn_*
WPFn (n = 0 to 3)	VI6_WPFn_*
DPR	VI6_DPR_*
SRU	VI6_SRU_*
UDSn (n = 0 to 2)	VI6_UDSn_*
LUT	VI6_LUT_CTRL
CLU	VI6_CLU_CTRL
HST	VI6_HST_CTRL
HSI	VI6_HSI_CTRL
BRU	VI6_BRU_*
HGO	VI6_HGO_*
HGT	VI6_HGT_*
LIF	VI6_LIF_*

## 28.2.4 Memory Map

### (1) Base Address

Below are the base addresses of each VSP unit (\$VSP\_BASE) in this LSI:

VSPR:	H'FE92 0000 [RZ/G1H only]
VSPS:	H'FE92 8000
VSPD0:	H'FE93 0000
VSPD1:	H'FE93 8000 [RZ/G1H/M/N only]

### (2) Register/Table Address

Table 28.15 shows the VSP1 memory map (represents in relative address).

**Table 28.15 VSP1 Memory Map**

Space	Register Type	Register Name	Relative Address from Base Address of Each VSP Unit	RZ/G Series Products			
				RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Register	General control registers	VI6_CMD0	\$VSP_BASE + H'0000	√	√	√	√
		VI6_CMD1 (VSPS and VSPR) [RZ/G1H only] (VSPS only) [RZ/G1M/N/E]	\$VSP_BASE + H'0004	√	√	√	√
		VI6_CMD2 (VSPS and VSPR) [RZ/G1H only] (VSPS only) [RZ/G1M/N/E]	\$VSP_BASE + H'0008	√	√	√	√
		VI6_CMD3 (VSPS and VSPR) [RZ/G1H only] (VSPS only) [RZ/G1M/N/E]	\$VSP_BASE + H'000C	√	√	√	√
		VI6_CLK_DCSWT	\$VSP_BASE + H'0018	√	√	√	√
		VI6_SRESET	\$VSP_BASE + H'0028	√	√	√	√
		VI6_STATUS	\$VSP_BASE + H'0038	√	√	√	
		VI6_WPF0_IRQ_ENB	\$VSP_BASE + H'0048	√	√	√	√
		VI6_WPF0_IRQ_STA	\$VSP_BASE + H'004C	√	√	√	√
		VI6_WPF1_IRQ_ENB (VSPS and VSPR) [RZ/G1H only] (VSPS only) [RZ/G1M/N/E]	\$VSP_BASE + H'0054	√	√	√	√
		VI6_WPF1_IRQ_STA (VSPS and VSPR) [RZ/G1H only] (VSPS only) [RZ/G1M/N/E]	\$VSP_BASE + H'0058	√	√	√	√
		VI6_WPF2_IRQ_ENB (VSPS and VSPR) [RZ/G1H only] (VSPS only) [RZ/G1M/N/E]	\$VSP_BASE + H'0060	√	√	√	√
		VI6_WPF2_IRQ_STA (VSPS and VSPR) [RZ/G1H only] (VSPS only) [RZ/G1M/N/E]	\$VSP_BASE + H'0064	√	√	√	√

Space	Register Type	Register Name	Relative Address from Base Address of Each VSP Unit	RZ/G Series Products				
				RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E	
Register	General control registers	VI6_WPF3_IRQ_ENB (VSPS and VSPR) [RZ/G1H only] (VSPS only) [RZ/G1M/N/E]	\$VSP_BASE + H'006C	√	√	√	√	
		VI6_WPF3_IRQ_STA (VSPS and VSPR) [RZ/G1H only] (VSPS only) [RZ/G1M/N/E]	\$VSP_BASE + H'0070	√	√	√	√	
		VI6_DISP_IRQ_ENB	\$VSP_BASE + H'0078	√	√	√	√	
		VI6_DISP_IRQ_STA	\$VSP_BASE + H'007C	√	√	√	√	
		VI6_WPF0_LINE_CNT	\$VSP_BASE + H'0084	√	√	√	√	
		VI6_WPF1_LINE_CNT (VSPS and VSPR) [RZ/G1H only] (VSPS only) [RZ/G1M/N/E]	\$VSP_BASE + H'0088	√	√	√	√	
		VI6_WPF2_LINE_CNT (VSPS and VSPR) [RZ/G1H only] (VSPS only) [RZ/G1M/N/E]	\$VSP_BASE + H'008C	√	√	√	√	
		VI6_WPF3_LINE_CNT (VSPS and VSPR) [RZ/G1H only] (VSPS only) [RZ/G1M/N/E]	\$VSP_BASE + H'0090	√	√	√	√	
		Display list control registers	VI6_DL_CTRL	\$VSP_BASE + H'0100	√	√	√	√
			VI6_DL_HDR_ADDR0	\$VSP_BASE + H'0104	√	√	√	√
			VI6_DL_HDR_ADDR1	\$VSP_BASE + H'0108	√	√	√	√
			VI6_DL_HDR_ADDR2	\$VSP_BASE + H'010C	√	√	√	√
			VI6_DL_HDR_ADDR3	\$VSP_BASE + H'0110	√	√	√	√
			VI6_DL_SWAP	\$VSP_BASE + H'0114	√	√	√	√
VI6_DL_EXT_CTRL	\$VSP_BASE + H'011C		√	√	√	√		
VI6_DL_BODY_SIZE0	\$VSP_BASE + H'0120		√	√	√	√		
RPFn control registers	VI6_RPFn_SRC_BSIZE	\$VSP_BASE + H'0300 + H'0100 × n	√	√	√	√		
	VI6_RPFn_SRC_ESIZE n = 0, 1, 2, 3, 4: (VSPS and VSPR) [RZ/G1H only]	\$VSP_BASE + H'0304 + H'0100 × n	√	√	√	√		
	VI6_RPFn_INFMT (VSPS) [RZ/G1M/N/E]	\$VSP_BASE + H'0308 + H'0100 × n	√	√	√	√		
	VI6_RPFn_DSWAP n = 0, 1, 2, 3: (VSPD)	\$VSP_BASE + H'030C + H'0100 × n	√	√	√	√		
	VI6_RPFn_LOC See Tables 28.1 to 28.3. [RZ/G1H]	\$VSP_BASE + H'0310 + H'0100 × n	√	√	√	√		
VI6_RPFn_ALPH_SEL See Tables 28.1 and 28.3. [RZ/G1M/N/E]	\$VSP_BASE + H'0314 + H'0100 × n	√	√	√	√			
	VI6_RPFn_VRTCOL_SET	\$VSP_BASE + H'0318 + H'0100 × n	√	√	√	√		

				RZ/G Series Products			
Space	Register Type	Register Name	Relative Address from Base Address of Each VSP Unit	RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Register	RPFn control registers	VI6_RPFn_MSKCTRL	\$VSP_BASE + H'031C + H'0100 × n	√	√	√	√
	n = 0, 1, 2, 3, 4: (VSPS and VSPR)	VI6_RPFn_MSKSET0	\$VSP_BASE + H'0320 + H'0100 × n	√	√	√	√
	[RZ/G1H only]	VI6_RPFn_MSKSET1	\$VSP_BASE + H'0324 + H'0100 × n	√	√	√	√
	(VSPS)						
	[RZ/G1M/N/E]	VI6_RPFn_CKEY_CTRL	\$VSP_BASE + H'0328 + H'0100 × n	√	√	√	√
	n = 0, 1, 2, 3: (VSPD)	VI6_RPFn_CKEY_SET0	\$VSP_BASE + H'032C + H'0100 × n	√	√	√	√
	See Tables 28.1 to 28.3. [RZ/G1H]	VI6_RPFn_CKEY_SET1	\$VSP_BASE + H'0330 + H'0100 × n	√	√	√	√
	See Tables 28.1 and 28.3. [RZ/G1M/N/E]	VI6_RPFn_SRCM_PSTRIDE	\$VSP_BASE + H'0334 + H'0100 × n	√	√	√	√
		VI6_RPFn_SRCM_ASTRIDE	\$VSP_BASE + H'0338 + H'0100 × n	√	√	√	√
		VI6_RPFn_SRCM_ADDR_Y	\$VSP_BASE + H'033C + H'0100 × n	√	√	√	√
		VI6_RPFn_SRCM_ADDR_C0	\$VSP_BASE + H'0340 + H'0100 × n	√	√	√	√
		VI6_RPFn_SRCM_ADDR_C1	\$VSP_BASE + H'0344 + H'0100 × n	√	√	√	√
		VI6_RPFn_SRCM_ADDR_AI	\$VSP_BASE + H'0348 + H'0100 × n	√	√	√	√
	WPFn control registers	VI6_WPFn_SRCRPF	\$VSP_BASE + H'1000 + H'0100 × n	√	√	√	√
	(VSPS and VSPR)	VI6_WPFn_HSZCLIP	\$VSP_BASE + H'1004 + H'0100 × n	√	√	√	√
	[RZ/G1H only]						
(VSPS)	VI6_WPFn_VSZCLIP	\$VSP_BASE + H'1008 + H'0100 × n	√	√	√	√	
[RZ/G1M/N/E]	VI6_WPFn_OUTFMT	\$VSP_BASE + H'100C + H'0100 × n	√	√	√	√	
See Table 28.3. [RZ/G1H]	VI6_WPFn_DSWAP	\$VSP_BASE + H'1010 + H'0100 × n	√	√	√	√	
See Table 28.3. [RZ/G1M/N/E]	VI6_WPFn_RNDCTRL	\$VSP_BASE + H'1014 + H'0100 × n	√	√	√	√	
	VI6_WPFn_DSTM_STRIDE_Y	\$VSP_BASE + H'101C + H'0100 × n	√	√	√	√	
	VI6_WPFn_DSTM_STRIDE_C	\$VSP_BASE + H'1020 + H'0100 × n	√	√	√	√	
	VI6_WPFn_DSTM_ADDR_Y	\$VSP_BASE + H'1024 + H'0100 × n	√	√	√	√	
	VI6_WPFn_DSTM_ADDR_C0	\$VSP_BASE + H'1028 + H'0100 × n	√	√	√	√	
	VI6_WPFn_DSTM_ADDR_C1	\$VSP_BASE + H'102C + H'0100 × n	√	√	√	√	

Space	Register Type	Register Name	Relative Address from Base Address of Each VSP Unit	RZ/G Series Products			
				RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Register	WPF0 control register	VI6_WPF0_WRBCK_CTRL	\$VSP_BASE + H'1034	√	√	√	√
	DPR control registers	VI6_DPR_RPF0_ROUTE	\$VSP_BASE + H'2000	√	√	√	√
		VI6_DPR_RPF1_ROUTE	\$VSP_BASE + H'2004	√	√	√	√
		VI6_DPR_RPF2_ROUTE	\$VSP_BASE + H'2008	√	√	√	√
		VI6_DPR_RPF3_ROUTE	\$VSP_BASE + H'200C	√	√	√	√
		VI6_DPR_RPF4_ROUTE	\$VSP_BASE + H'2010	√	√	√	√
		(VSPS and VSPR) [RZ/G1H]					
		(VSPS only) [RZ/G1M/N/E]					
		VI6_DPR_WPF0_FPORCH	\$VSP_BASE + H'2014	√	√	√	√
		VI6_DPR_WPF1_FPORCH	\$VSP_BASE + H'2018	√	√	√	√
		(VSPS and VSPR) [RZ/G1H]					
		(VSPS only) [RZ/G1M/RZ/G1N/E]					
		VI6_DPR_WPF2_FPORCH	\$VSP_BASE + H'201C	√	√	√	√
		(VSPS and VSPR) [RZ/G1H]					
		(VSPS only) [RZ/G1M/N/E]					
		VI6_DPR_WPF3_FPORCH	\$VSP_BASE + H'2020	√	√	√	√
		(VSPS and VSPR) [RZ/G1H]					
		(VSPS only) [RZ/G1M/N/E]					
		VI6_DPR_SRU_ROUTE	\$VSP_BASE + H'2024	√	√	√	√
		(VSPS and VSPR) [RZ/G1H]					
		(VSPS only) [RZ/G1M/N/E]					
		VI6_DPR_UDS0_ROUTE	\$VSP_BASE + H'2028	√	√	√	√
		VI6_DPR_UDS1_ROUTE	\$VSP_BASE + H'202C	√	–	–	–
		VI6_DPR_UDS2_ROUTE	\$VSP_BASE + H'2030	√	–	–	–
	VI6_DPR_LUT_ROUTE	\$VSP_BASE + H'203C	√	√	√	√	
	(VSPS and VSPD) [RZ/G1H only]						
	VI6_DPR_CLU_ROUTE	\$VSP_BASE + H'2040	√	√	√	√	
	(VSPS only)						
	VI6_DPR_HST_ROUTE	\$VSP_BASE + H'2044	√	√	√	√	
	VI6_DPR_HSI_ROUTE	\$VSP_BASE + H'2048	√	√	√	√	
	VI6_DPR_BRU_ROUTE	\$VSP_BASE + H'204C	√	√	√	√	
	VI6_DPR_HGO_SMPPT	\$VSP_BASE + H'2054	√	√	√	√	
	(VSPS and VSPR) [RZ/G1H]						
	(VSPS only) [RZ/G1M/N/E]						
	VI6_DPR_HGT_SMPPT	\$VSP_BASE + H'2058	√	√	√	√	
	(VSPS only)						

Space	Register Type	Register Name	Relative Address from Base Address of Each VSP Unit	RZ/G Series Products			
				RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Register	SRU control registers	VI6_SRU_CTRL0	\$VSP_BASE + H'2200	√	√	√	√
		VI6_SRU_CTRL1	\$VSP_BASE + H'2204	√	√	√	√
	(VSPS and VSPR) [RZ/G1H]	VI6_SRU_CTRL2	\$VSP_BASE + H'2208	√	√	√	√
	(VSPS only) [RZ/G1M/N/E]						
Register	UDS0 control registers	VI6_UDS0_CTRL	\$VSP_BASE + H'2300	√	√	√	√
		VI6_UDS0_SCALE	\$VSP_BASE + H'2304	√	√	√	√
		VI6_UDS0_ALPTH	\$VSP_BASE + H'2308	√	√	√	√
		VI6_UDS0_ALPVAL	\$VSP_BASE + H'230C	√	√	√	√
		VI6_UDS0_PASS_BWIDTH	\$VSP_BASE + H'2310	√	√	√	√
		VI6_UDS0_IPC	\$VSP_BASE + H'2318	√	√	√	√
		VI6_UDS0_CLIP_SIZE	\$VSP_BASE + H'2324	√	√	√	√
		VI6_UDS0_FILL_COLOR	\$VSP_BASE + H'2328	√	√	√	√
Register	UDSn control registers n = 1, 2 (VSPS only)  [RZ/G1H only]	VI6_UDSn_CTRL	\$VSP_BASE + H'2300 + H'0100 × n	√	–	–	–
		VI6_UDSn_SCALE	\$VSP_BASE + H'2304 + H'0100 × n	√	–	–	–
		VI6_UDSn_ALPTH	\$VSP_BASE + H'2308 + H'0100 × n	√	–	–	–
		VI6_UDSn_ALPVAL	\$VSP_BASE + H'230C + H'0100 × n	√	–	–	–
		VI6_UDSn_PASS_BWIDTH	\$VSP_BASE + H'2310 + H'0100 × n	√	–	–	–
		VI6_UDSn_IPC	\$VSP_BASE + H'2318 + H'0100 × n	√	–	–	–
		VI6_UDSn_CLIP_SIZE	\$VSP_BASE + H'2324 + H'0100 × n	√	–	–	–
		VI6_UDSn_FILL_COLOR	\$VSP_BASE + H'2328 + H'0100 × n	√	–	–	–
Register	LUT control register (VSPS and VSPD)	VI6_LUT_CTRL	\$VSP_BASE + H'2800	√	√	√	√
Register	CLU control register (VSPS only)	VI6_CLU_CTRL	\$VSP_BASE + H'2900	√	√	√	√
Register	HST control register	VI6_HST_CTRL	\$VSP_BASE + H'2A00	√	√	√	√
Register	HSI control register	VI6_HSI_CTRL	\$VSP_BASE + H'2B00	√	√	√	√

				RZ/G Series Products			
Space	Register Type	Register Name	Relative Address from Base Address of Each VSP Unit	RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Register	BRU control registers	VI6_BRU_INCTRL	\$VSP_BASE + H'2C00	√	√	√	√
		VI6_BRU_VIRRRPF_SIZE	\$VSP_BASE + H'2C04	√	√	√	√
		VI6_BRU_VIRRRPF_LOC	\$VSP_BASE + H'2C08	√	√	√	√
		VI6_BRU_VIRRRPF_COL	\$VSP_BASE + H'2C0C	√	√	√	√
		VI6_BRUA_CTRL	\$VSP_BASE + H'2C10	√	√	√	√
		VI6_BRUA_BLD	\$VSP_BASE + H'2C14	√	√	√	√
		VI6_BRUB_CTRL	\$VSP_BASE + H'2C18	√	√	√	√
		VI6_BRUB_BLD	\$VSP_BASE + H'2C1C	√	√	√	√
		VI6_BRUC_CTRL	\$VSP_BASE + H'2C20	√	√	√	√
		VI6_BRUC_BLD	\$VSP_BASE + H'2C24	√	√	√	√
		VI6_BRUD_CTRL	\$VSP_BASE + H'2C28	√	√	√	√
		VI6_BRUD_BLD	\$VSP_BASE + H'2C2C	√	√	√	√
		VI6_BRU_ROP	\$VSP_BASE + H'2C30	√	√	√	√
HGO control registers (VSPS and VSPD)	VI6_HGO_OFFSET	\$VSP_BASE + H'3000	√	√	√	√	
	VI6_HGO_SIZE	\$VSP_BASE + H'3004	√	√	√	√	
	VI6_HGO_MODE	\$VSP_BASE + H'3008	√	√	√	√	
	VI6_HGO_LB_TH	\$VSP_BASE + H'300C	√	√	√	√	
	VI6_HGO_LB0_H	\$VSP_BASE + H'3010	√	√	√	√	
	VI6_HGO_LB0_V	\$VSP_BASE + H'3014	√	√	√	√	
	VI6_HGO_LB1_H	\$VSP_BASE + H'3018	√	√	√	√	
	VI6_HGO_LB1_V	\$VSP_BASE + H'301C	√	√	√	√	
	VI6_HGO_LB2_H	\$VSP_BASE + H'3020	√	√	√	√	
	VI6_HGO_LB2_V	\$VSP_BASE + H'3024	√	√	√	√	
	VI6_HGO_LB3_H	\$VSP_BASE + H'3028	√	√	√	√	
	VI6_HGO_LB3_V	\$VSP_BASE + H'302C	√	√	√	√	
	VI6_HGO_R_HISTO_n (n = 0 to 63)	\$VSP_BASE + H'3030 + 4n	√	√	√	√	
	VI6_HGO_R_MAXMIN	\$VSP_BASE + H'3130	√	√	√	√	
	VI6_HGO_R_SUM	\$VSP_BASE + H'3134	√	√	√	√	
	VI6_HGO_R_LB_DET	\$VSP_BASE + H'3138	√	√	√	√	
	VI6_HGO_G_HISTO_n (n = 0 to 63)	\$VSP_BASE + H'3140 + 4n	√	√	√	√	
	VI6_HGO_G_MAXMIN	\$VSP_BASE + H'3240	√	√	√	√	
	VI6_HGO_G_SUM	\$VSP_BASE + H'3244	√	√	√	√	
	VI6_HGO_G_LB_DET	\$VSP_BASE + H'3248	√	√	√	√	
	VI6_HGO_B_HISTO_n (n = 0 to 63)	\$VSP_BASE + H'3250 + 4n	√	√	√	√	
	VI6_HGO_B_MAXMIN	\$VSP_BASE + H'3350	√	√	√	√	
	VI6_HGO_B_SUM	\$VSP_BASE + H'3354	√	√	√	√	
	VI6_HGO_B_LB_DET	\$VSP_BASE + H'3358	√	√	√	√	
	VI6_HGO_REGRST	\$VSP_BASE + H'33FC	√	√	√	√	

				RZ/G Series Products				
Space	Register Type	Register Name	Relative Address from Base Address of Each VSP Unit	RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E	
Register	HGT control registers (VSPS only)	VI6_HGT_OFFSET	\$VSP_BASE + H'3400	√	√	√	√	
		VI6_HGT_SIZE	\$VSP_BASE + H'3404	√	√	√	√	
		VI6_HGT_MODE	\$VSP_BASE + H'3408	√	√	√	√	
		VI6_HGT_HUE_AREA0	\$VSP_BASE + H'340C	√	√	√	√	
		VI6_HGT_HUE_AREA1	\$VSP_BASE + H'3410	√	√	√	√	
		VI6_HGT_HUE_AREA2	\$VSP_BASE + H'3414	√	√	√	√	
		VI6_HGT_HUE_AREA3	\$VSP_BASE + H'3418	√	√	√	√	
		VI6_HGT_HUE_AREA4	\$VSP_BASE + H'341C	√	√	√	√	
		VI6_HGT_HUE_AREA5	\$VSP_BASE + H'3420	√	√	√	√	
		VI6_HGT_LB_TH	\$VSP_BASE + H'3424	√	√	√	√	
		VI6_HGT_LB0_H	\$VSP_BASE + H'3428	√	√	√	√	
		VI6_HGT_LB0_V	\$VSP_BASE + H'342C	√	√	√	√	
		VI6_HGT_LB1_H	\$VSP_BASE + H'3430	√	√	√	√	
		VI6_HGT_LB1_V	\$VSP_BASE + H'3434	√	√	√	√	
		VI6_HGT_LB2_H	\$VSP_BASE + H'3438	√	√	√	√	
		VI6_HGT_LB2_V	\$VSP_BASE + H'343C	√	√	√	√	
		VI6_HGT_LB3_H	\$VSP_BASE + H'3440	√	√	√	√	
		VI6_HGT_LB3_V	\$VSP_BASE + H'3444	√	√	√	√	
		VI6_HGT_HISTO_m_n (m = 0 to 5, n = 0 to 31)	\$VSP_BASE + H'3450 + 128m + 4n	√	√	√	√	
		VI6_HGT_MAXMIN	\$VSP_BASE + H'3750	√	√	√	√	
	VI6_HGT_SUM	\$VSP_BASE + H'3754	√	√	√	√		
	VI6_HGT_LB_DET	\$VSP_BASE + H'3758	√	√	√	√		
	VI6_HGT_REGRST	\$VSP_BASE + H'37FC	√	√	√	√		
	LIF control registers (VSPD only)	VI6_LIF_CTRL	\$VSP_BASE + H'3B00	√	√	√	√	
		VI6_LIF_CSBTH	\$VSP_BASE + H'3B04	√	√	√	√	
	Security control registers	VI6_SECURE_CTRL0	\$VSP_BASE + H'3D00	√	√	√	√	
		VI6_SECURE_CTRL1	\$VSP_BASE + H'3D04	√	√	√	√	
	CLUT	RPFn-CLUT (n = 0, 1, 2, 3, 4)	VI6_CLUTn_TBL0 ↓	\$VSP_BASE + H'4000 + H'0400 × n	√	√	√	√
		See Tables 28.1 to 28.3. [RZ/G1H]  See Tables 28.1 and 28.3. [RZ/G1M/N/E]	VI6_CLUTn_TBL255	↓ \$VSP_BASE + H'43FF + H'0400 × n				



Space	Register Type	Register Name	Relative Address from Base Address of Each VSP Unit	RZ/G Series Products			
				RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
LUT	1D-LUT (VSPS and VSPD)	VI6_LUT_TBL_0	\$VSP_BASE + H'7000	√	√	√	√
		↓	↓				
		VI6_LUT_TBL_255	\$VSP_BASE + H'73FF				
	3D-LUT (VSPS only)	VI6_CLU_ADDR	\$VSP_BASE + H'7400	√	√	√	√
		VI6_CLU_DATA	\$VSP_BASE + H'7404	√	√	√	√

Note: Do not access addresses other than listed above. Operations cannot be guaranteed if access is attempted.

## 28.2.5 General Control Registers

### 28.2.5.1 VSP1 Start Registers n (VI6\_CMDn: n = 0, 1, 2, 3)

Note: See Table 28.15 for details on which RZ/G series products have which registers.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	STRCMD
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	STRCMD	0	R/W	Start Command VSP1 has four output channels (WPFs). Starting WPF0 to WPF3 starts operation of VSP1. Only a single WPF can be started, and all four WPFs can also be started at the same time. VI6_CMD0.STRCMD to VI6_CMD3.STRCMD respectively control WPF0 to WPF3. Writing 1 to this bit starts WPFn in VSP1. Set this bit for activation only after all register settings in each output channel have been completed. This bit is always read as 0. 0: NOP 1: WPFn is started (VSP1 is started).

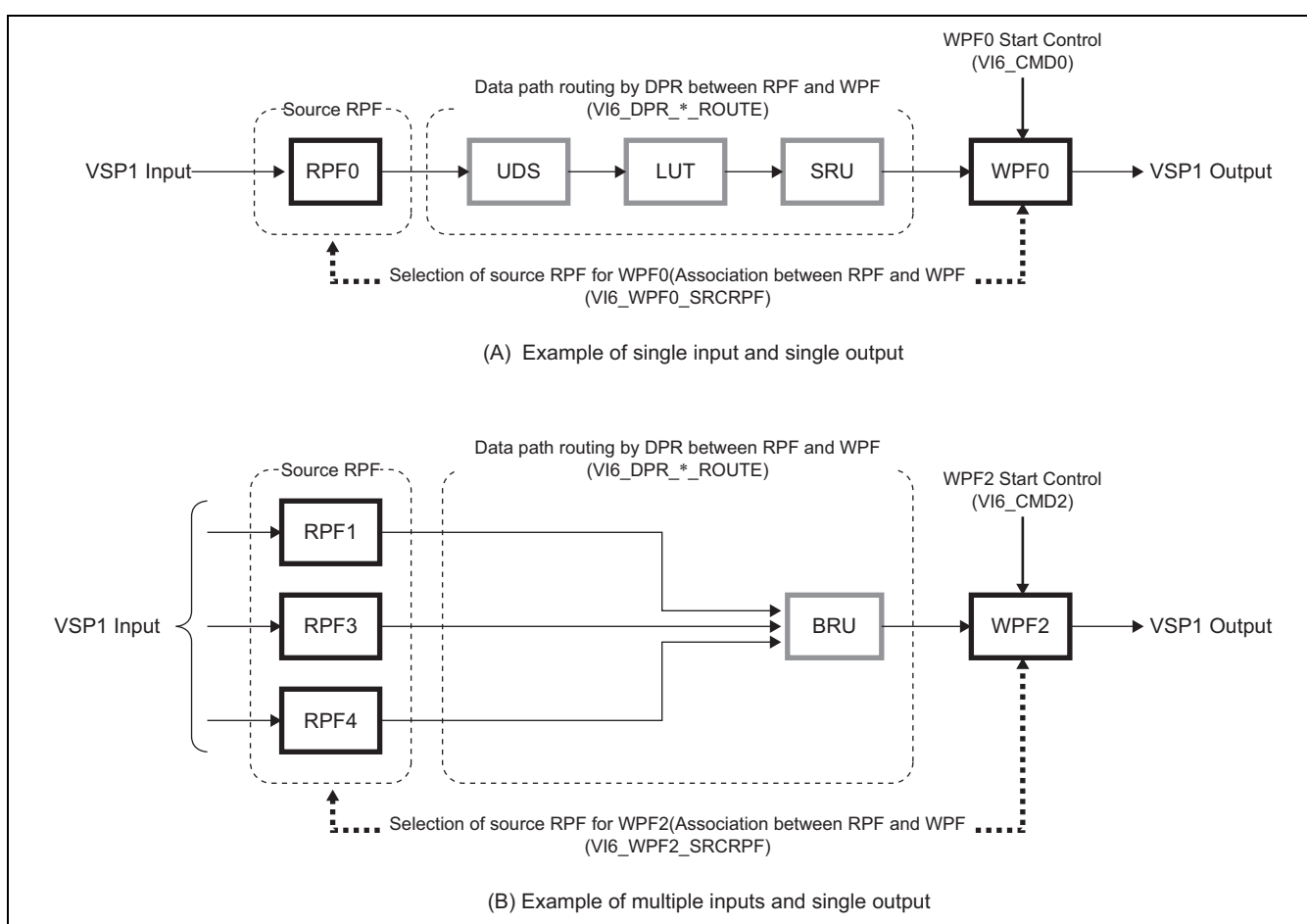
The basic concept of image processing operation started by activating the VSP1 is shown in Figure 28.13. The actual data input/output is executed by the MAU, which is the bus interface module, as described in section 28.1.2, but conceptually the RPF works as the data entry point to the VSP1 and the WPF works as the data exit point. To process images through the VSP1, the RPF (entrance) and WPF (exit) should be connected and a data path from the RPF to the WPF should be formed.

To connect RPFn to WPFn, specify RPFn as the source RPF for WPFn in VI6\_WPFn\_SRCRPF, which is a register for WPFn (refer to section 28.2.8.1). This setting determines that RPFn will be started when WPFn is started through VI6\_CMDn.

A data path to execute desired image processing should then be formed between the RPF (entrance) and WPF (exit). To form a data path, connect the necessary function modules in the VSP1 between RPF and WPF. This function is provided by the DPR; specify the information for each module connection in data path routing registers VI6\_DPR\_\*\_ROUTE (refer to section 28.2.9).

After a data path is formed (RPF<sub>n</sub> → WPF<sub>n</sub>) as described above, starting output module WPF<sub>n</sub> in the VSP1 through VI6\_CMD<sub>n</sub> starts all function modules connected to WPF<sub>n</sub> and the desired image processing is executed. According to this design concept, starting a WPF module means starting the VSP1.

There are two types of data path configuration in the VSP1; one is "a single input module to a single output module" as shown in Figure 28.13 (A), and the other is "multiple input modules to a single output module" as shown in Figure 28.13 (B). Figure 28.13 (A) shows an example of a configuration where modules with single input and single output are implemented through the DPR. Figure 28.13 (B) shows another configuration example where the module with multiple input and single output is implemented through the DPR. As shown in the figure, there is no conflict over internal module resources between these two connection examples, and the data paths in Figure 28.13 (A) and (B) can be started at the same time (for details of the DPR, refer to section 28.2.9). To start them together, make the register settings related to the modules used in each data path, and then set VI6\_CMD0 and VI6\_CMD2 to start WPF0 and WPF2, respectively. These two paths are completely independent. Even if the register settings for path (B) are incomplete, path (A) can be started regardless of the state of path (B) when the register settings for path (A) are complete.



**Figure 28.13 Basic Concept of VSP1 Startup**

The DPR in the VSP1 can realize more advanced data paths than those shown in Figure 28.13. For example, two activations are necessary for the combination of paths (A) and (B) in Figure 28.13. However, the same processing may be started through one activation by improving the data path configuration, depending on the data processing flow in some cases, as shown in Figure 28.14. When the data path configuration is improved, the capacity of memory used and the amount of bus transfer in the system can be reduced. When determining the starting units in the VSP1, carefully examine the data processing flow and configure an optimal data path.

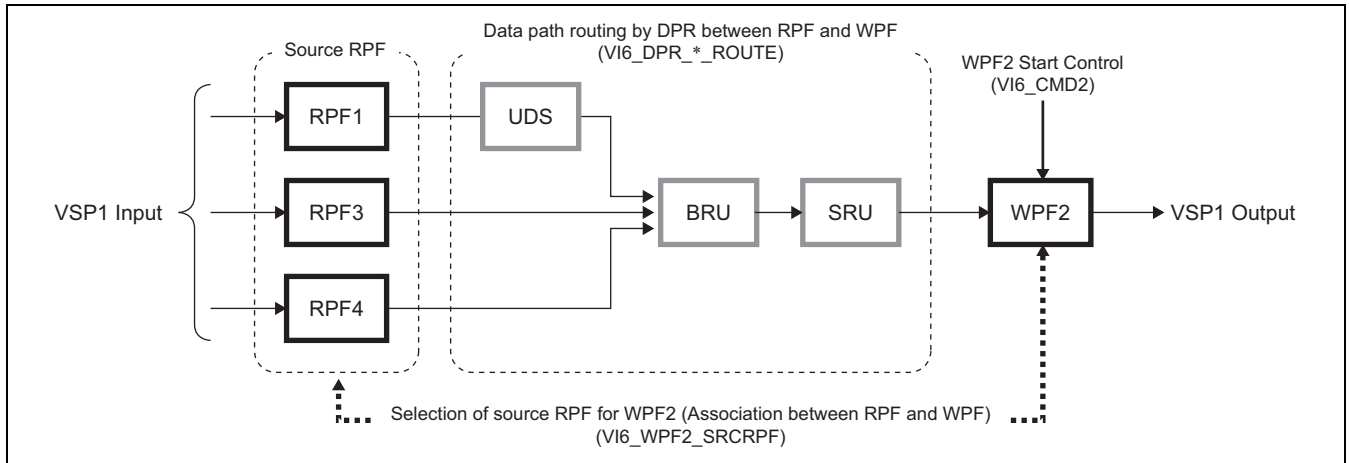


Figure 28.14 Sample Configuration of Combining Data Paths in Figure

### 28.2.5.2 Dynamic Clock Stop Control Register (VI6\_CLK\_DCSWT)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CSTPW [7:0]								CSTRW [7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 8	CSTPW[7:0]	H'00	R/W	Dynamic Clock Stop Control 1 Always specify 8.
7 to 0	CSTRW[7:0]	H'00	R/W	Dynamic Clock Stop Control 2 Always specify 8.

### 28.2.5.3 Software Reset Register (VI6\_SRESET)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	SRST3	SRST2	SRST1	SRST0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3	SRST3	0	R/W	WPFn Software Reset (SRSTn, n = 0 to 3)
2	SRST2	0	R/W	Writing 1 to this bit aborts the current processing in WPFn (the partially-completed image undergoing processing is output). The period until this software reset processing is completed depends on the bus state.
1	SRST1	0	R/W	When this reset processing is completed, the VI6_WPFn_IRQ_STA.FRE interrupt source bit is set to 1; when the FRE interrupt is enabled, the FRE end interrupt is output to notify the end of the reset processing.
0	SRST0	0	R/W	This bit is always read as 0. 0: NOP 1: WPF3 software reset*

Notes: \* Applying a software reset to each WPF has the following restrictions.

1. A software reset can be applied to only one of WPF0 to WPF3 through single write access to VI6\_SRESET.
2. After a software reset is issued, no more software reset can be issued to another WPF until the issued software reset processing is completed
3. After a software reset is issued to a channel, correct operation of other channels cannot be guaranteed; apply software reset to all channels in sequence.
4. The end of software reset processing is notified through the FRE bit in VI6\_WPFn\_IRQ\_STA, but the software reset issued while WPF is stopped is ignored as NOP. As it takes a while until the reset is actually issued after the reset bit is set, the VSP1 may complete operation before the reset is actually issued. In this case, no interrupt is output for the software reset that is issued after the VSP1 completes operation.
5. If a software reset is issued during downloading of a display list, the downloading processing is not aborted. After the end of downloading that is in progress when a software reset is issued, a frame end interrupt is output.

### 28.2.5.4 Operating Status Register (VI6\_STATUS)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	SYS3_ACT	SYS2_ACT	SYS1_ACT	SYS0_ACT	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 12	—	All 0	R	Reserved These bits are read as 0 or 1. Don't care about this value. Write access is prohibited.
11	SYS3_ACT	0	R	WPFn Operating Status (SYSn_ACT, n = 0 to 3)
10	SYS2_ACT	0	R	Each bit indicates the operating or stopped state of control channel n (WPFn). 0: WPFn is stopped. 1: WPFn is operating.
9	SYS1_ACT	0	R	
8	SYS0_ACT	0	R	
7 to 4	—	All 0	R	Reserved These bits are read as 0 or 1. Don't care about this value. Write access is prohibited.
3	—	0	R	WPFn Internal Control Monitor Signal
2	—	0	R	Each bit indicates a value of 0 or 1. Don't use the value read from this bit.
1	—	0	R	
0	—	0	R	

### 28.2.5.5 WPF Interrupt Enable Registers (VI6\_WPFn\_IRQ\_ENB: n = 0, 1, 2, 3)

Note: See Table 28.15 for details on which RZ/G series products have which registers.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DFEE	FREE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	DFEE	0	R/W	Interrupt Enable for WPFn (n = 0 to 3) Display List Frame End 0: Interrupt Disabled 1: Interrupt Enabled
0	FREE	0	R/W	Interrupt Enable for WPFn (n = 0 to 3) Frame End 0: Interrupt Disabled 1: Interrupt Enabled

Each bit in VI6\_WPFn\_IRQ\_STA is set to 1 when the corresponding interrupt source is generated.

VI6\_WPFn\_IRQ\_ENB specifies whether to output an interrupt signal for the generated source. When an interrupt is disabled in this register, no interrupt signal is generated even when the corresponding bit in VI6\_WPFn\_IRQ\_STA is set to 1. When an interrupt is enabled in this register, an interrupt signal is output when the corresponding bit in VI6\_WPFn\_IRQ\_STA is set to 1.



### 28.2.5.6 WPF Interrupt Status Registers (VI6\_WPFn\_IRQ\_STA: n = 0, 1, 2, 3)

Note: See Table 28.15 for details on which RZ/G series products have which registers.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DFE	FRE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 2	—	All 0	R	Reserved These bits are read as 0 or 1. Don't care about this value. The write value should always be 0.
1	DFE	0	R/W	Interrupt Status and Clear for WPFn (n = 0 to 3) Display List Frame End This interrupt source bit is set to 1 when VSP1 completes one-frame processing while the <code>current_frame_int_enable</code> value stored in the display list header is 1 (refer to section 28.1.8 (2)). When display lists are not used, this bit is not used. In this case, clear <code>VI6_WPFn_IRQ_ENB.DFEE</code> to 0 to mask the interrupt generation by this interrupt source. [Read Access] Interrupt Status 0: No interrupt 1: Interrupt activated [Write Access] Interrupt Clear 0: The interrupt status is cleared to 0 1: Hold the interrupt status value
0	FRE	0	R/W	Interrupt Status and Clear for WPFn (n = 0 to 3) Frame End This interrupt source bit is set to 1 when VSP1 completes one-frame processing. This bit is also set to 1 when one-frame processing using a display list is completed. [Read Access] Interrupt Status 0: No interrupt 1: Interrupt activated [Write Access] Interrupt Clear 0: The interrupt status is cleared to 0 1: Hold the interrupt status value

VI6\_WPFn\_IRQ\_STA indicates the state of the interrupt sources generated in the VSP1. Whether to output a VSP1 interrupt when an interrupt source is generated and the corresponding bit is set to 1 is determined by the corresponding

bit setting in VI6\_WPFn\_IRQ\_ENB. While an interrupt is disabled in VI6\_WPFn\_IRQ\_ENB, the VSP1 does not output an interrupt signal even when an interrupt source is generated, but the source flag in this register is set to 1.

Note that the interrupt source bits in this register cannot be cleared by write access using a display list.

### 28.2.5.7 Display Interrupt Enable Register (VI6\_DISP\_IRQ\_ENB)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	DSTE	—	—	MAEE	LNE4E	LNE3E	LNE2E	LNE1E	LNE0E
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	DSTE	0	R/W	Interrupt Enable for Display Start 0: Interrupt Disabled 1: Interrupt Enabled
7, 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5	MAEE	0	R/W	Interrupt Enable for Display Read Data End 0: Interrupt Disabled 1: Interrupt Enabled
4	LNE4E	0	R/W	Interrupt Enable for 1 Line Data Read End of RFP4 0: Interrupt Disabled 1: Interrupt Enabled
3	LNE3E	0	R/W	Interrupt Enable for 1 Line Data Read End of RFP3 0: Interrupt Disabled 1: Interrupt Enabled
2	LNE2E	0	R/W	Interrupt Enable for 1 Line Data Read End of RFP2 0: Interrupt Disabled 1: Interrupt Enabled
1	LNE1E	0	R/W	Interrupt Enable for 1 Line Data Read End of RFP1 0: Interrupt Disabled 1: Interrupt Enabled
0	LNE0E	0	R/W	Interrupt Enable for 1 Line Data Read End of RFP0 0: Interrupt Disabled 1: Interrupt Enabled

### 28.2.5.8 Display Interrupt Status Register (VI6\_DISP\_IRQ\_STA)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	DST	—	—	MAE	LNE4	LNE3	LNE2	LNE1	LNE0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W

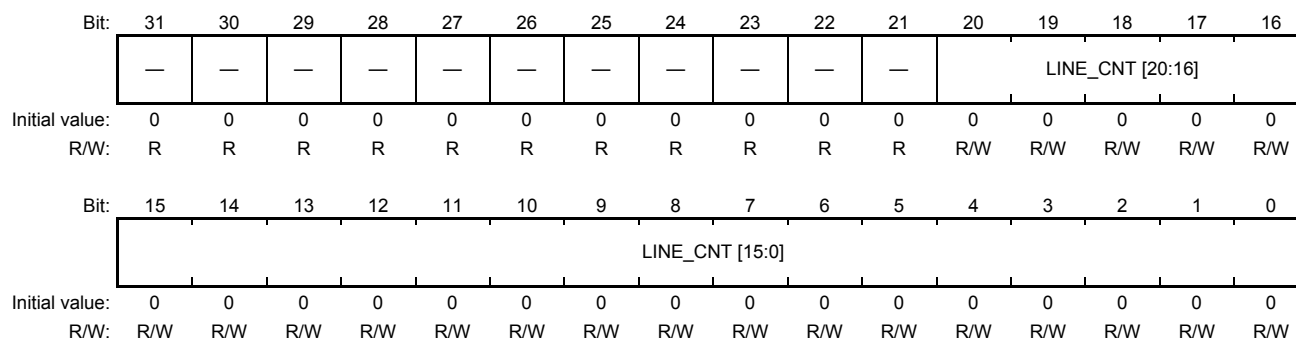
Bit	Bit Name	Initial Value	R/W	Description
31 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	DST	0	R/W	Interrupt Status and Clear for Display Start This bit is set to 1 when LIF module transfers the first data to the display module at the beginning of each frame. The timing depends on the output buffer status of LIF module. [Read Access] Interrupt Status 0: No interrupt 1: Interrupt activated [Write Access] Interrupt Clear 0: The interrupt status is cleared to 0 1: Hold the interrupt status value
7, 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5	MAE	0	R/W	Interrupt Status and Clear for Display Read Data End This bit is set to 1 when all RPFs transfer the last data of the frame to LIF module. The RPF module which is not used by LIF module does not affect this bit. [Read Access] Interrupt Status 0: No interrupt 1: Interrupt activated [Write Access] Interrupt Clear 0: The interrupt status is cleared to 0 1: Hold the interrupt status value

Bit	Bit Name	Initial Value	R/W	Description
4	LNE4	0	R/W	Interrupt Status and Clear for 1 Line Data Read End of RFP4 This bit is set to 1 when RPF4 completes 1-line data transfer. [Read Access] Interrupt Status 0: No interrupt 1: Interrupt activated [Write Access] Interrupt Clear 0: The interrupt status is cleared to 0 1: Hold the interrupt status value
3	LNE3	0	R/W	Interrupt Status and Clear for 1 Line Data Read End of RFP3 [Read Access] Interrupt Status 0: No interrupt 1: Interrupt activated [Write Access] Interrupt Clear 0: The interrupt status is cleared to 0 1: Hold the interrupt status value
2	LNE2	0	R/W	Interrupt Status and Clear for 1 Line Data Read End of RFP2 [Read Access] Interrupt Status 0: No interrupt 1: Interrupt activated [Write Access] Interrupt Clear 0: The interrupt status is cleared to 0 1: Hold the interrupt status value
1	LNE1	0	R/W	Interrupt Status and Clear for 1 Line Data Read End of RFP1 [Read Access] Interrupt Status 0: No interrupt 1: Interrupt activated [Write Access] Interrupt Clear 0: The interrupt status is cleared to 0 1: Hold the interrupt status value
0	LNE0	0	R/W	Interrupt Status and Clear for 1 Line Data Read End of RFP0 [Read Access] Interrupt Status 0: No interrupt 1: Interrupt activated [Write Access] Interrupt Clear 0: The interrupt status is cleared to 0 1: Hold the interrupt status value

### 28.2.5.9 WPFn Output Line Count Register (VI6\_WPFn\_LINE\_CNT: n = 0, 1, 2, 3)

Note: See Table 28.15 for details on which RZ/G series products have which registers.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√



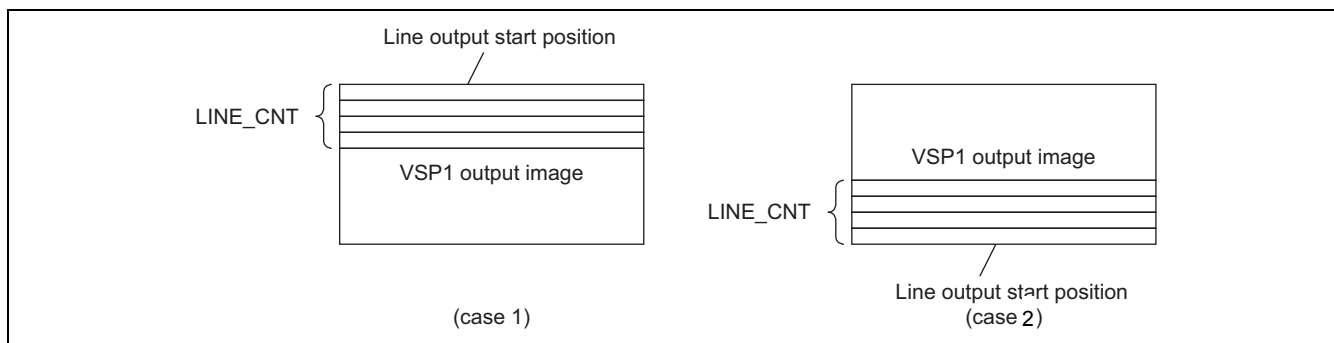
Bit	Bit Name	Initial Value	R/W	Description
31 to 21	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
20 to 0	LINE_CNT [20:0]	All 0	R	Number of WPFn Output Lines From the value read from these bits, the number of lines output from VSP1 can be obtained. <u>The value of these bits can be read only within a limited period; read these bits with the timing described later.</u> These bits indicate the number of lines output from WPFn as an immediate value. In the frame buffer starting from VI6_WPFn_DSTN_ADDR_*, WPFn has completed data output up to the line number indicated in these bits. For example, when these bits are set to 1, valid data is output only in the first line. When one-frame processing is completed correctly, this value indicates the number of lines output from WPFn.

The LINE\_CNT value is valid only for the period between a frame end interrupt (section 28.2.5.6) and next frame startup (section 28.2.5.1) or the period between a display list frame end interrupt (section 28.2.5.6) and next frame startup. This register value read outside these periods cannot be used.

The LINE\_CNT value depends on the flipping mode (VI6\_WPFn\_OUTFMT.FLP) as shown in Figure 28.15. This correspondence is shown in Table 28.16.

**Table 28.16 VSP1 Output Line Count According to VI6\_WPFn\_OUTFMT.FLP Setting**

VI6_WPFn_OUTFMT.FLP Setting	Corresponding Case Shown in Figure 28.15
0	case 1
1	case 2



**Figure 28.15 Definition of VSP1 Output Line Count**

## 28.2.6 Display List Control Registers

### 28.2.6.1 Display List Control Register (VI6\_DL\_CTRL)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	AR_WAIT [15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	DC2	—	—	—	DC1	—	—	—	DC0	—	CFM0	NH0	DLE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R	R	R	R/W	R	R	R	R/W	R	R/W	R/W	R/W

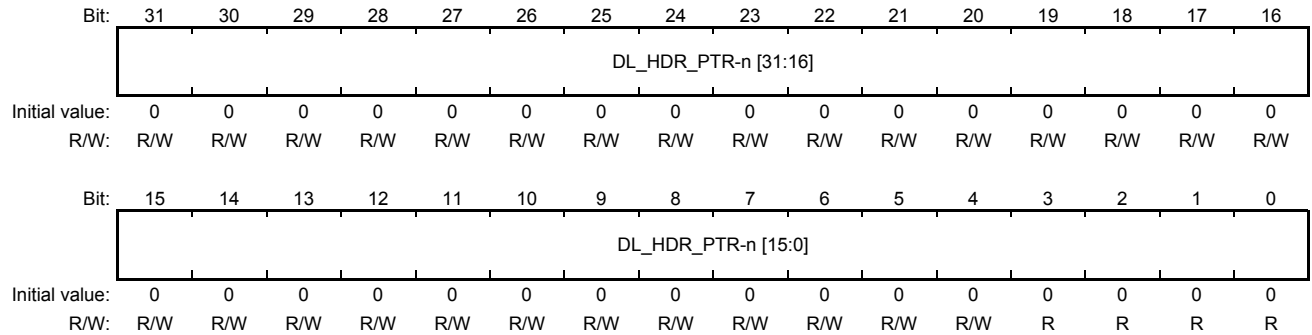
Bit	Bit Name	Initial Value	R/W	Description
31 to 16	AR_WAIT [15:0]	H'0000	R/W	Display List Control Setting Always specify 256.
15 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12	DC2	0	R/W	Display List Control 2 Specify the same value as the DLE bit.
11 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	DC1	0	R/W	Display List Control 1 Specify the same value as the DLE bit.
7 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	DC0	0	R/W	Display List Control 0 Specify the same value as the DLE bit.
3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
2	CFM0	0	R/W	Continuous Frame Mode for Header-less Display List This bit determines whether the next frame is automatically started or not. When the updated flag of the display list, VI6_DL_BODY_SIZE0.UPD0, is not updated, the display list of the next frame is not transferred and the same register values are used for the next frame. When the value of VI6_DL_BODY_SIZE0.UPD0 is updated, the new display list is transferred. 0: Stopped at the end of every frame 1: The next frame is automatically started



Bit	Bit Name	Initial Value	R/W	Description
1	NH0	0	R/W	<p>Header-less Display List Mode</p> <p>This bit is used for specifying the header-less display list mode. In case of header-less mode, the number of the display lists is 1. The address of the display body is set in VI6_DL_HDR_ADDR0 register, and the body size is set in VI6_DL_BODY_SIZE0 register.</p> <p>When this bit is changed, make sure that VSP1 is stopped. And also make sure the following before starting VSP1.</p> <ul style="list-style-type: none"> <li>- Header Address (VI6_DL_HDR_ADDR0)</li> <li>- Body Size (VI6_DL_BODY_SIZE0) in case of header-less mode</li> </ul> <p>0: Use Display List Header (Normal DL Mode) 1: Don't use Display List Header (Header-less Mode)</p> <p>Note: Only WPF0 supports header-less display list. WPFn (n = 1 to 3) work as the normal display list mode even if the WPF0 is set to header-less display list mode.</p>
0	DLE	0	R/W	<p>Display List Enable/Disable</p> <p>Enables or disables the VSP1 display list function. When the display list function is enabled through this bit, all WPF processing channels work in display list mode.</p> <p>When using display lists, note the restrictions in section 28.2.3.</p> <p>0: The display list function is disabled 1: The display list function is enabled</p>

### 28.2.6.2 Display List-n Header Address Register (VI6\_DL\_HDR\_ADDRn: n = 0, 1, 2, 3)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	DL_HDR_PTR-n [31:0]	H'0000 0000	R/W [31:4] R [3:0]	<p>Display List-n Header Address</p> <p>These bits specify the address of the display list header to be read for display list-n in 16-byte units (the lower-order four bits are read-only). When WPFn is first started in display list mode, the display list header is loaded from the address specified in this register. After loading of the header is completed, the register value of the display list address is updated to the next header address stored in the loaded header to prepare for loading of the next display list header. After that, this header address updating is repeated.</p> <p>A value from H'00000000 to H'FFFFFFF0 can be specified.</p>

### 28.2.6.3 Display List Data Swapping Register (VI6\_DL\_SWAP)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	LWS	WDS	BTS
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2	LWS	0	R/W	Display List Data Swapping in Longword Units 0: Data swapping in longword (32-bit) units is disabled 1: Data swapping in longword (32-bit) units is enabled
1	WDS	0	R/W	Display List Data Swapping in Word Units 0: Data swapping in word (16-bit) units is disabled 1: Data swapping in word (16-bit) units is enabled
0	BTS	0	R/W	Display List Data Swapping in Byte Units 0: Data swapping in byte (8-bit) units is disabled 1: Data swapping in byte (8-bit) units is enabled

### 28.2.6.4 Extended Display List Control Register (VI6\_DL\_EXT\_CTRL)

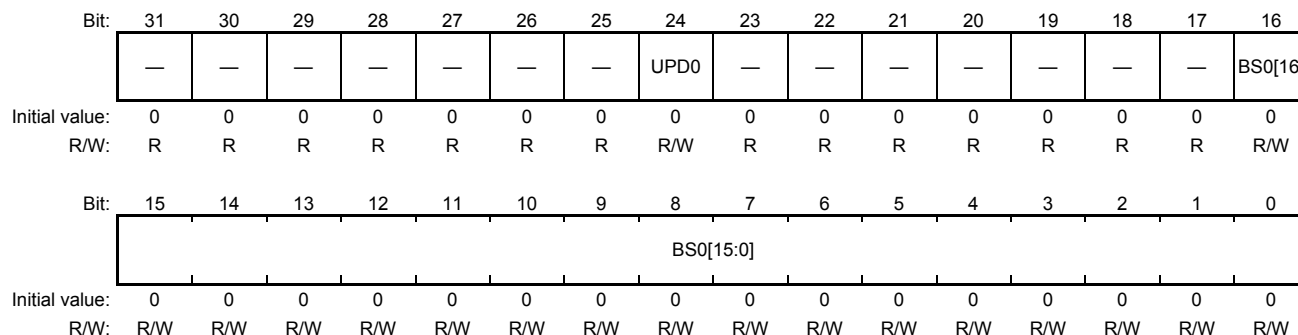
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	NWE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	POLINT [5:0]					—	—	DLPRI	EXPRI	—	—	—	—	EXT
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 17	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
16	NWE	0	R/W	No Wait for Polling When this bit is set to 1, the polling condition for extended display lists is always assumed to be true.
15, 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13 to 8	POLINT[5:0]	All 0	R/W	Extended Display List Command Control Always specify 2.
7, 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5	DLPRI	0	R/W	Display List Control 0 Always specify 1.
4	EXPRI	0	R/W	Display List Control 1 Always specify 0.
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	EXT	0	R/W	Extended Display List Enables or disables the extended display list function. When extended display lists are used, the display list header size is 96 bytes; when they are not used, the header size is 80 bytes. 0: No extended display lists are used 1: Extended display lists are used Note: When using extended display lists, be sure to also use normal display list mode (VI6_DL_CTRL.DLE); executing only extended display lists is not possible. When the header-less display list mode is activated, this bit should be set to 0. The extended display list cannot be used with the header-less display list mode.

### 28.2.6.5 Display List Body Size Register-n (VI6\_DL\_BODY\_SIZE<sub>n</sub>: n = 0)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√



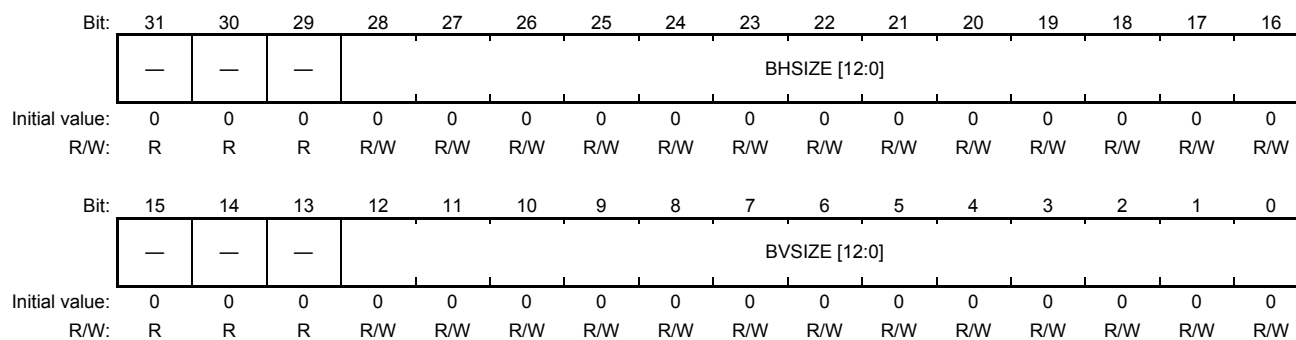
Bit	Bit Name	Initial Value	R/W	Description
31 to 25	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
24	UPD0	0	R/W	Update Flag This bit controls the download of the display list at the next downloading timing in case that the header-less display list mode is used. When this bit is set to 1, the value of VI6_DL_HDR_ADDR <sub>n</sub> and VI6_DL_BODY_SIZE <sub>n</sub> .BS0 (n = 0) should not be changed. 0: Display List is not downloaded (Registers are not updated) 1: Display List is downloaded (Registers are updated)
23 to 17	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
16 to 0	BS0[16:0]	All 0	R/W	Header-less Display List Body Size (WPF <sub>n</sub> , n = 0) These bits are used for specifying the body size of the display list in case of header-less display list mode. The unit of the size is byte. The value should be set in multiples of 8.

## 28.2.7 RPF Control Registers

### 28.2.7.1 RPFn Basic Read Size Registers (VI6\_RPFn\_SRC\_BSIZE)

Note: See Table 28.15 for details on which RZ/G series products have which registers.

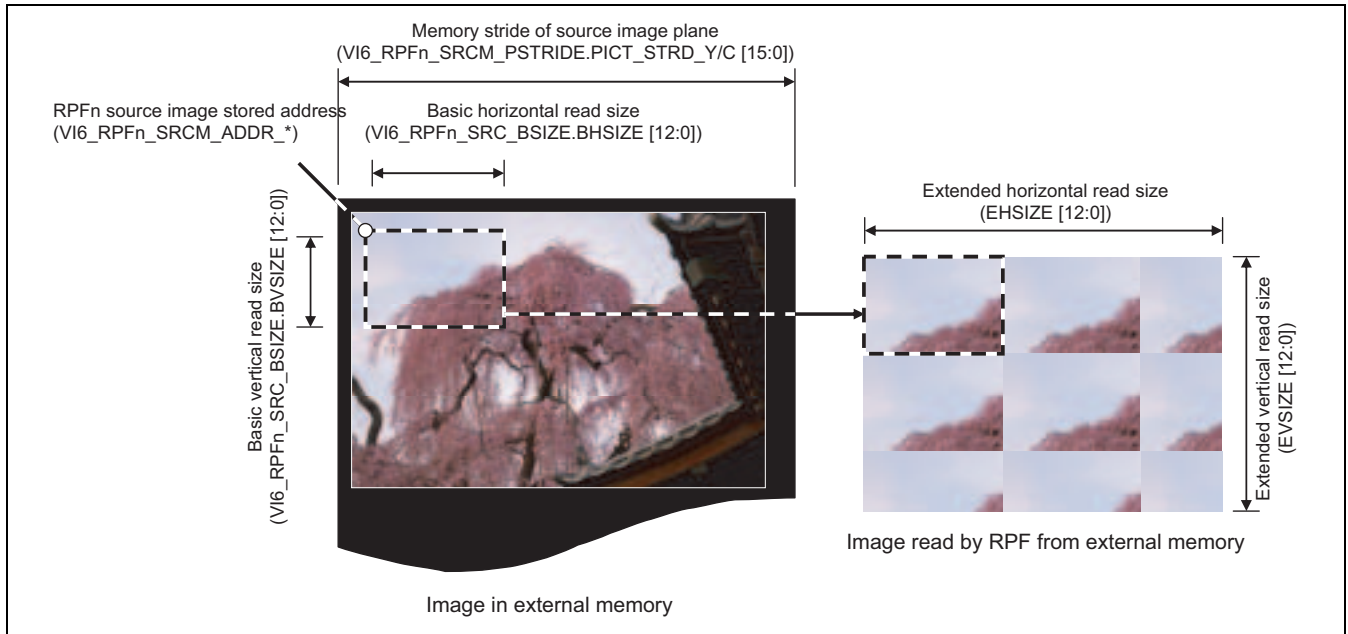
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√



Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28 to 16	BHSIZE [12:0]	H'0000	R/W	Horizontal Size of RPF Basic Read Area These bits specify the horizontal size of the basic area to be read from the external RAM by the RPFn. When the input format is YCbCr4:2:2 or YCbCr4:2:0, specify the size in 2-pixel units. A value from 1 to 8,190 can be specified. Specify a value equal to or smaller than the extended read size (VI6_RPFn_SRC_ESIZE.EHSIZE).
15 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12 to 0	BVSIZ [12:0]	H'0000	R/W	Vertical Size of RPF Basic Read Area These bits specify the vertical size of the basic area to be read from the external RAM by the RPFn. When the input format is YCbCr4:2:0, specify the size in 2-pixel units. A value from 1 to 8,190 can be specified. Specify a value equal to or smaller than the extended read size (VI6_RPFn_SRC_ESIZE.EVSIZE).

Figure 28.16 shows the relationship between the basic read size and extended read size. The RPF reads data from the source memory area specified by the basic read size. The RPF repeats reading the basic read area in the horizontal and vertical directions up to the extended read size and sends the read data to the processing modules in the VSP1.

For basic read size reading, the reading start address, called the RPFn source image storing address, should be specified in VI6\_RPFn\_SRCM\_ADDR\_\*. In the memory area where the basic read area image is stored, the distance (number of bytes) between addresses for lines n and n + 1 of two-dimensional image data, called the memory stride, should be specified in VI6\_RPFn\_SRCM\_PSTRIDE.



**Figure 28.16 Relationship between Basic Read Size and Extended Read Size**

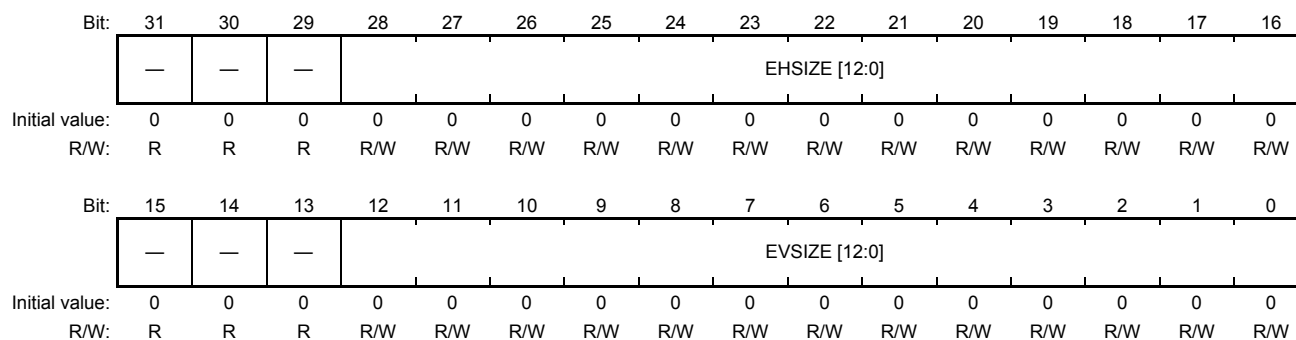
Refer also to the following sections.

- Section 28.2.7.2, RPFn Extended Read Size Registers (VI6\_RPFn\_SRC\_ESIZE)
- Section 28.2.7.13, RPFn Source Picture Memory Stride Setting Registers (VI6\_RPFn\_SRCM\_PSTRIDE)
- Section 28.2.7.15, RPFn Source Y/RGB Address Registers (VI6\_RPFn\_SRCM\_ADDR\_Y)
- Section 28.2.7.16, RPFn Source Chroma Address Registers 0 (VI6\_RPFn\_SRCM\_ADDR\_C0)
- Section 28.2.7.17, RPFn Source Chroma Address Registers 1 (VI6\_RPFn\_SRCM\_ADDR\_C1)

### 28.2.7.2 RPFn Extended Read Size Registers (VI6\_RPFn\_SRC\_ESIZE)

Note: See Table 28.15 for details on which RZ/G series products have which registers.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√



Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28 to 16	EHSIZE [12:0]	H'0000	R/W	RPF Extended Horizontal Read Size These bits specify the horizontal size of the extended read area to which the RPFn reads data from the external RAM. As shown in Figure 28.16, the basic read area image is repeatedly placed in the extended read area; in the EHSIZE bits, specify a value not smaller than the horizontal size of the basic read area. When the input format is YCbCr4:2:2 or YCbCr4:2:0, specify the size in 2-pixel units (an even value). A value from 1 to 8,190 can be specified.
15 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12 to 0	EVSIZE [12:0]	H'0000	R/W	RPF Extended Vertical Read Size These bits specify the vertical size of the extended read area to which the RPFn reads data from the external RAM. As shown in Figure 28.16, the basic read area image is repeatedly placed in the extended read area; in the EVSIZE bits, specify a value not smaller than the vertical size of the basic read area. When the input format is YCbCr4:2:0, specify the size in 2-pixel units (an even value). A value from 1 to 8,190 can be specified.

VI6\_RPFn\_SRC\_ESIZE specifies the extended size for RPFn. The extended horizontal and vertical sizes should be equal to or greater than the basic sizes specified in VI6\_RPFn\_SRC\_BSIZE. The RPF internal data processing described later and image processing described in section 28.2.9 and later sections are all applied to the image in the extended read size shown on the right side in Figure 28.16.



### 28.2.7.3 RPFn Input Format Registers (VI6\_RPFn\_INFMT)

Note: See Table 28.15 for details on which RZ/G series products have which registers.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	VIR	—	—	—	—	—	—	—	—	—	—	—	CIPM
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R	R	R	R	R	R	R	R	R	R	R	R/W

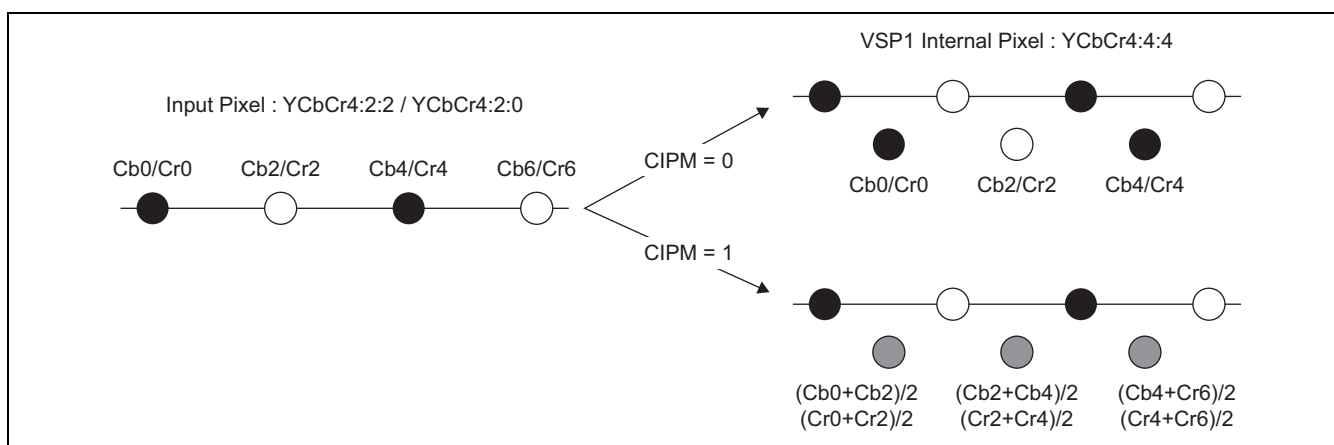
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SPYCS	SPUVS	CEXT [1:0]		RDTM [2:0]		CSC	—	RDFMT [6:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28	VIR	0	R/W	Virtual Input Enable Enables or disables the virtual input function of the RPFn. The image to be processed by the RPFn is usually read from the external memory by the MAU. Instead of this input, the virtual input function generates a single-color image within the RPFn and sends it to the modules in VSP1. When the virtual input function is enabled, the fixed value specified in VI6_RPFn_VRTCOL_SET is used as the input to the RPFn. While the virtual input function is enabled, data is not read from the external memory; that is, the $\alpha$ plane is not read and the IROP calculation thus cannot be executed. In this case, set VI6_RPFn_ALPH_SEL.ASEL to 4. Neither the color space conversion through CSC nor the color keying described in section 28.2.7.11 can be used. 0: RPFn uses general input. 1: RPFn uses virtual input.
27 to 17	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
16	CIPM	0	R/W	Horizontal Chrominance Interpolation Method Setting Image data is processed in the YCbCr444 format inside VSP1 in case of YCbCr color space. When the chrominance format of the input image is YCbCr422 or YCbCr420, data is upsampled as shown in Figure 28.17 for internal processing. This bit specifies the method of upsampling for this purpose. 0: The nearest-neighbor method is used for horizontal chrominance interpolation. 1: The bilinear method is used for horizontal chrominance interpolation.

Bit	Bit Name	Initial Value	R/W	Description
15	SPYCS	0	R/W	<p>RPF Input Mode Setting 1</p> <p>When the input format is YUY2, set this bit to 1 and set the RDFMT bits to 71 (H'47).</p> <p>When the input format is YVYU, set this bit and the SPUVS bit to 1 and set the RDFMT bits to 71 (H'47).</p> <p>In other cases, set this bit to 0.</p>
14	SPUVS	0	R/W	<p>RPF Input Mode Setting 2</p> <p>When the input format is NV61, set this bit to 1 and set the RDFMT bits to 65 (H'41).</p> <p>When the input format is NV21, set this bit to 1 and set the RDFMT bits to 66 (H'42).</p> <p>When the input format is YVYU, set this bit and the SPYCS bit to 1 and set the RDFMT bits to 71 (H'47).</p> <p>In other cases, set this bit to 0.</p>
13, 12	CEXT[1:0]	00	R/W	<p>Lower-Bit Color Data Extension Method Setting</p> <p>When an RGB input format where each color component is expressed in less than eight bits are selected from Table 28.18 through the RDFMT bits, VSP1 internally extends each color component to eight bits before using the data. These bits select this extension method.</p> <p>00: Lower-order bits of color data are extended with 0.</p> <p>01: Upper-order bits of color data are copied to the lower -order bits.</p> <p>10: Lower-order bits of color data are extended with 0. The maximum value is limited to H'FF.</p> <p>11: Setting prohibited</p>
11 to 9	RDTM[2:0]	000	R/W	<p>CSC Conversion Expression Setting</p> <p>These bits select the expression used for color space conversion. The conversion direction is RGB → YCbCr when RGB is selected through the RDFMT bits; the direction is YCbCr → RGB when YCbCr is selected.</p> <p>000: BT.601 YCbCr [16,235/240] ↔ RGB [0,255]</p> <p>001: BT.601 YCbCr [0,255] ↔ RGB [0,255]</p> <p>010: BT.709 YCbCr [16,235/240] ↔ RGB [0,255]</p> <p>011: BT.709 YCbCr [16,235/240] ↔ RGB [16,235]</p> <p>100 to 111: Setting prohibited</p>
8	CSC	0	R/W	<p>Color Space Conversion Enable</p> <p>Enables or disables color space conversion between YCbCr and RGB to be executed in RPFn. The characteristics of color space conversion are determined by the RDTM bit setting. *</p> <p>When using the virtual input (VIR = 1), specify 0.</p> <p>0: Color space conversion is disabled.</p> <p>1: Color space conversion is enabled.</p>
7	—	0	R	<p>Reserved</p> <p>This bit is always read as 0. The write value should always be 0.</p>

Bit	Bit Name	Initial Value	R/W	Description
6 to 0	RDFMT [6:0]	H'00	R/W	<p>RPF Input Image Format Setting</p> <p>These bits select the format of the image input from the external RAM to the RPFn. Select a value corresponding to the desired format from those shown in Tables 28.18 and 28.19.</p> <p>When the virtual input function is used (VIR = 1), the color information for the virtual input should be specified in VI6_RPFn_VRTCOL_SET. If this color information is in the RGB format, set the RDFMT bits to 19. If the color information is in the YCbCr format, set these bits to 64.</p> <p>Notes: 1. Number of input pixels</p> <p>When YCbCr4:2:2 is selected through the RDFMT bits, the horizontal size of the input image should be specified in 2-pixel units. When YCbCr4:2:0 is selected, the vertical and horizontal sizes should be specified in 2-pixel units. Observe these restrictions when specifying the image size in VI6_RPFn_SRC_BSIZE and VI6_RPFn_SRC_ESIZE.</p> <p>2. CLUT Setting</p> <p>When the RDFMT bits are set to H'3F, RGB color data should be stored in the CLUT. When these bits are set to H'7F, YCbCr color data should be stored in the CLUT. Note that while the target WPF is operating, the RPF is also operating and the CLUT cannot be read or written to.</p>

Note: \* Note on color space settings



**Figure 28.17 Chrominance Interpolation Methods Selectable through CIPM Setting**

The color space for the image output from the RPF to VSP1 internal modules is determined by the combination of the color space for the image input to the RPF, which is selected through the VI6\_RPFn\_INFMT.RDFMT setting, and the enabled or disabled state of the color space conversion function, which is selected through the VI6\_RPFn\_INFMT.CSC setting (Table 28.17). For example, when the image input to the RPF is in the YCbCr format, the RPF outputs data to VSP1 internal modules in the YCbCr format if color space conversion is disabled through the CSC bit, and the RPF outputs data in the RGB format if color space conversion is enabled. When the image input to the RPF is in the RGB format, the relationship between the output format and the color space conversion setting is the opposite of the YCbCr case. For some VSP1 internal modules, the YCbCr format is recommended for image processing because of the characteristics of the processing, or the same color space needs to be specified between multiple RPF outputs. In these cases, set VI6\_RPFn\_INFMT.RDFMT and VI6\_RPFn\_INFMT.CSC appropriately so that the RPFs can output the required color space according to the color space conditions described above.

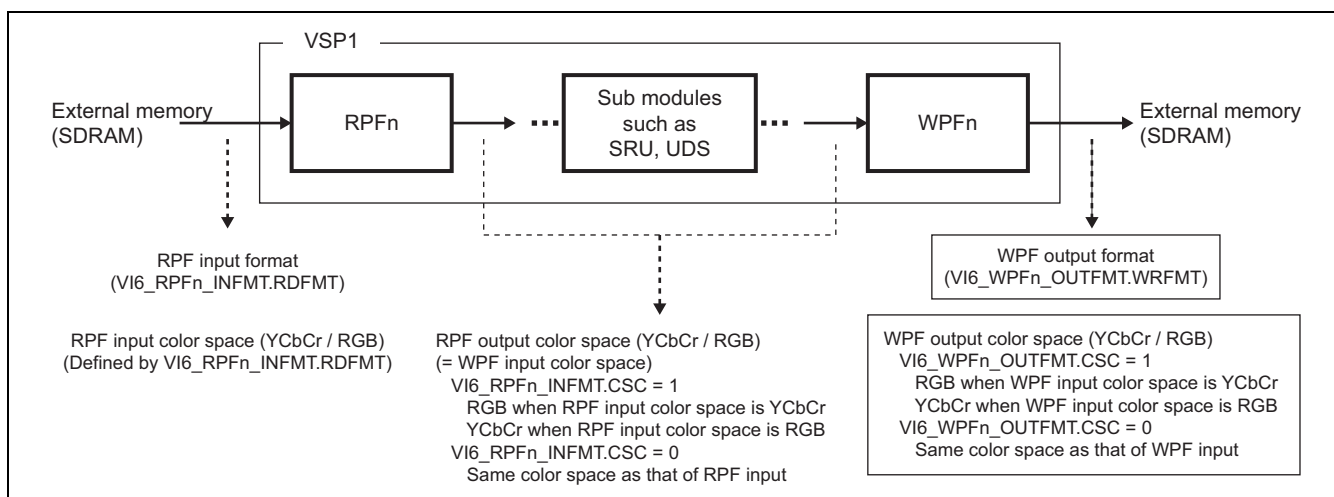
**Table 28.17 RPFn Input Color Space and Output Color Space**

RPFn Input Color Space (VI6_RPFn_INFMT.RDFMT)		Color Space Conversion Setting (VI6_RPFn_INFMT.CSC)		RPFn Output Color Space
RGB	(H'00 to H'3F)*	Disabled	(0) *	RGB
		Enabled	(1) *	YCbCr
YCbCr	(H'40 to H'7F)*	Disabled	(0) *	YCbCr
		Enabled	(1) *	RGB

Note: \* Value specified in the register

A color space conversion function equivalent to that in the RPFn is also provided by the WPF. As shown in Table 28.17, the color space (YCbCr or RGB) output from the RPF becomes the input format for the WPF. Here, the color space of the output image obtained by the color space conversion function of the WPF must match the color space of the format specified through VI6\_WPFn\_OUTFMT.WRFMT.

Figure 28.18 shows the relationship between the input/output format and color space. The input color space for the RPF is determined when the input image format for the RPF is specified through the RDFMT bits. The color space for the image output from the RPF to subsequent VSP1 internal modules depends on the combination of the RPF input format and CSC (color space conversion function) enabled or disabled state in the RPF as shown in Table 28.17 and Figure 28.18. The user should first determine whether the image processing in the VSP1 is done in YCbCr or RGB, and then specify the RPF input format and CSC enabled or disabled state to obtain the desired color space. The color space of the RPF output image is also that of the WPF input image; the color space of the data output from the WPF to the outside of VSP1 depends on the combination of the WPF input color space and the enabled or disabled state of the CSC implemented in the WPF as shown in Figure 28.18. The color space of the WPF output image must match that of the WPF output format (determined by VI6\_WPFn\_OUTFMT.WRFMT). For example, in the flow shown in Figure 28.18, YCbCr should not be specified as the WPF output format regardless of the fact that the color space of the WPF output image is in RGB format.

**Figure 28.18 Relationship between Input/Output Format and Color Space**



**Table 28.19 Packed YCbCr Formats for RPF Input**

<b>RDFMT [6:0]</b>	<b>Packed YCbCr Input Format</b>	<b>Reference</b>
H'40	YCbCr4:4:4 semi-planar	Figure 28.19
H'41	YCbCr4:2:2 semi-planar (NV16, NV61* <sup>1</sup> )	
H'42	YCbCr4:2:0 semi-planar (NV12, NV21* <sup>1</sup> )	
H'43 to H'45	Reserved	—
H'46	YCbCr4:4:4 interleaved	Figure 28.20
H'47	YCbCr4:2:2 interleaved type 0 (UYVY, YUY2* <sup>2</sup> , YVYU* <sup>3</sup> )	
H'48	YCbCr4:2:2 interleaved type 1	
H'49	YCbCr4:2:0 interleaved	
H'4A	YCbCr4:4:4 planar	Figure 28.21
H'4B	YCbCr4:2:2 planar (YV16)	
H'4C	YCbCr4:2:0 planar (YV12, YU12)	
H'4D to H'7E	Reserved	—
H'7F	YCBCR_CLUT_DATA* <sup>4</sup> * <sup>5</sup>	—

- Notes:
1. When the input format is NV61 or NV21, set the SPUVS bit to 1.
  2. When the input format is YUY2, set the SPYCS bit to 1.
  3. When the input format is YVYU, set the SPUVS bit to 1 and SPYCS bit to 1.
  4. When the RDFMT[6:0] bits are set to H'7F, it is necessary to set up the CLUT in the YCbCr color space.
  5. The Monochrome format can be implemented through the CLUT.

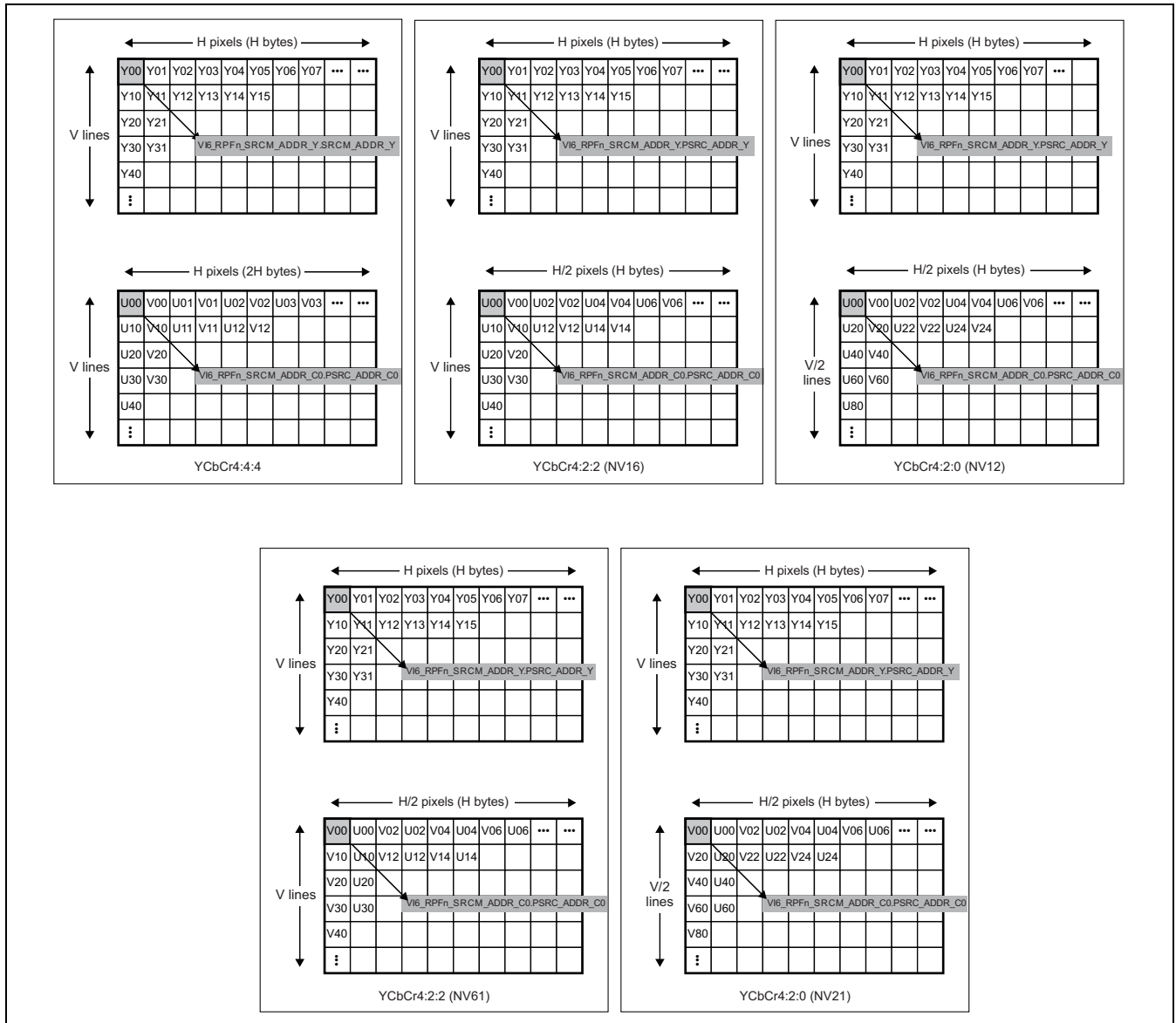


Figure 28.19 YCbCr Semi-Planar Formats

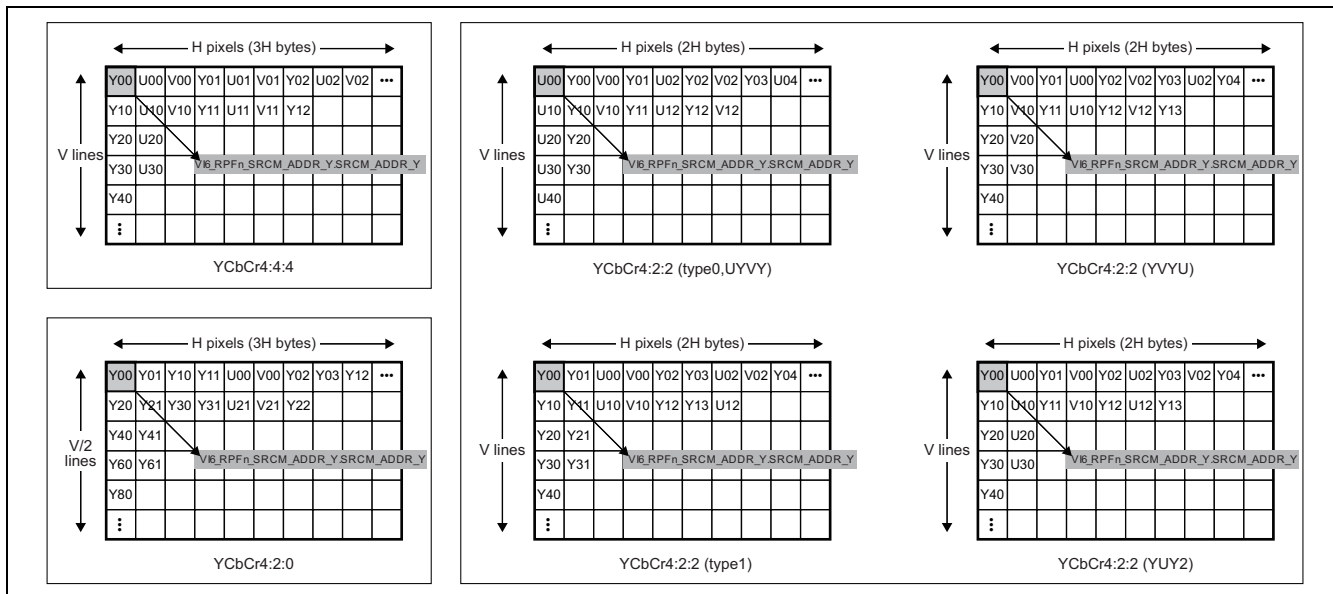


Figure 28.20 YCbCr Interleaved Formats

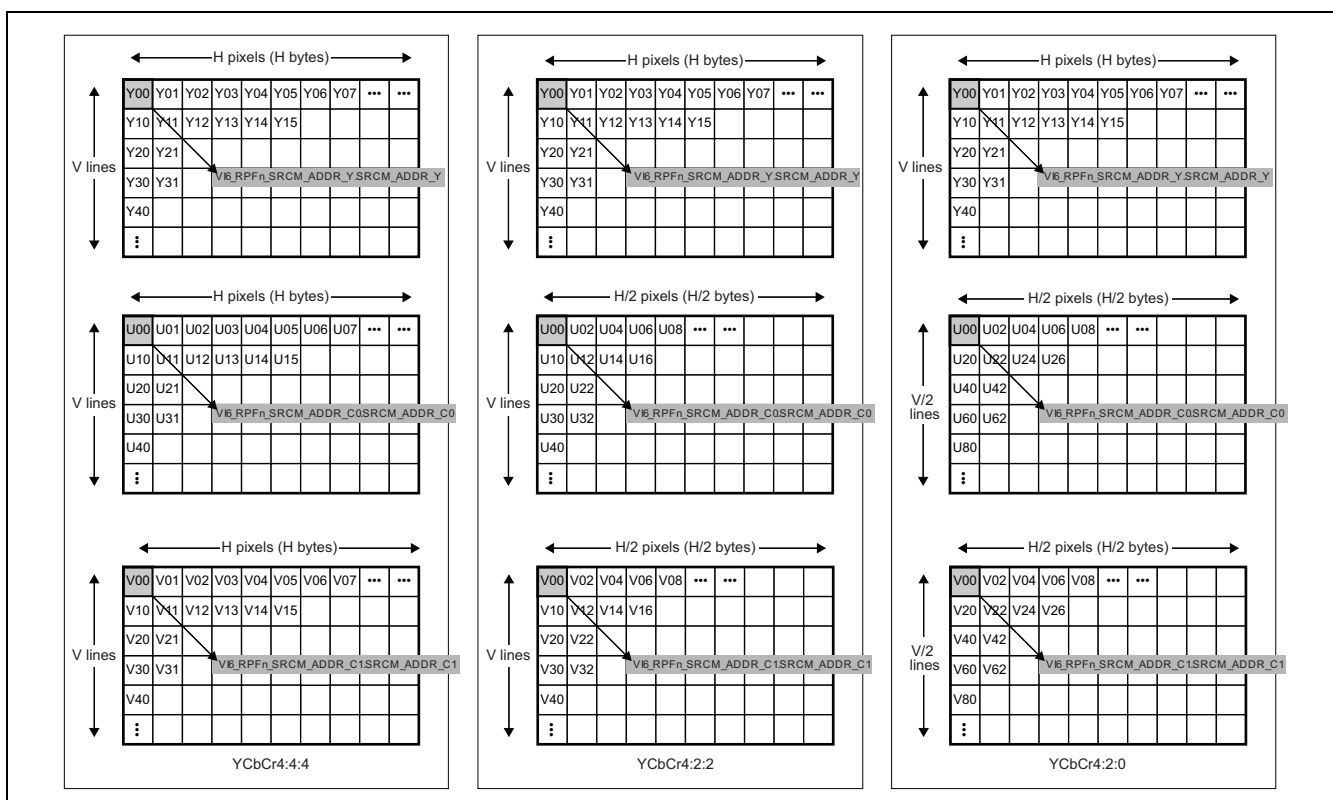


Figure 28.21 YCbCr Planar Formats



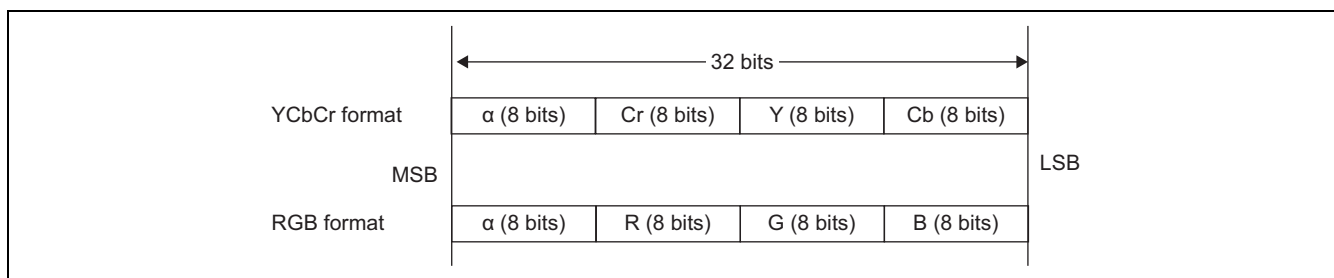
**[CLUT Setting]**

To set up the CLUT, store the values to replace each of R (Cr), G (Y), and B (Cb) components in the CLUT allocated as shown in Table 28.20. The CLUT space has 256 32-bit entries, which should be accessed in 32 bits in the same way as for register access. The address for each entry is obtained from the start address of each space (Table 28.20) + entry number × 4. For example, the CLUT address of entry 7 for RPF2 is \$VSP\_BASE + H'481C.

Figure 28.22 shows the CLUT format.

**Table 28.20 CLUT Space for Each RPF**

RPF	Address Area for CLUT Space
RPF0	\$VSP_BASE + H'4000 to \$VSP_BASE + H'43FF
RPF1	\$VSP_BASE + H'4400 to \$VSP_BASE + H'47FF
RPF2	\$VSP_BASE + H'4800 to \$VSP_BASE + H'4BFF
RPF3	\$VSP_BASE + H'4C00 to \$VSP_BASE + H'4FFF
RPF4	\$VSP_BASE + H'5000 to \$VSP_BASE + H'53FF

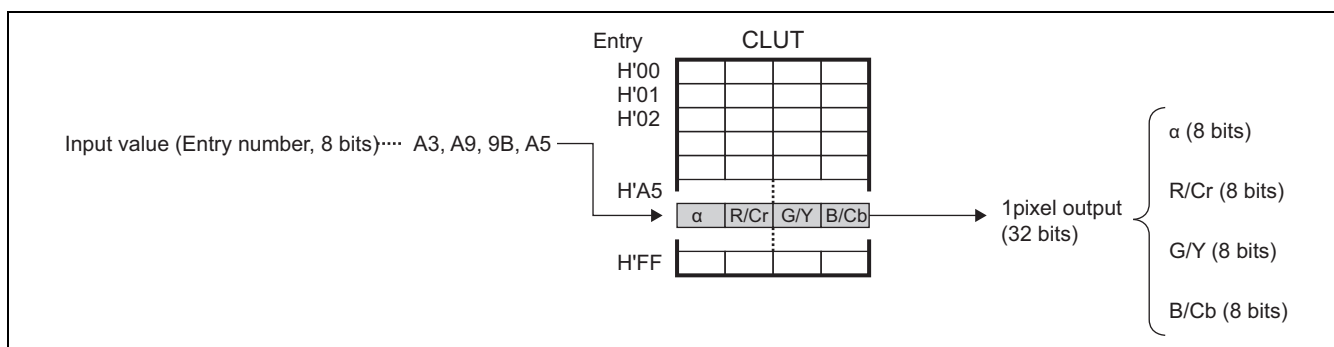


**Figure 28.22 CLUT Format**

According to the specified 256-entry replacement table (CLUT), input data is replaced as shown in Figure 28.23. Input data is eight bits but output data is 32 bits including  $\alpha$  and RGB or YCbCr components.

When writing to an entry in the CLUT, the host CPU writes all components at the same time. Therefore, specify replacement data for all components in the CLUT at the same time as shown in Figure 28.22.

Note that write access to the CLUT space is prohibited while the RPF is operating.



**Figure 28.23 Replacement of Input Data with Pixel Values Specified in CLUT**

### 28.2.7.4 RPFn Data Swapping Registers (VI6\_RPFn\_DSWAP)

Note: See Table 28.15 for details on which RZ/G series products have which registers.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11	A_LLS	0	R/W	α Plane Data Swapping in LONG LWORD Units 0: Data swapping in LONG LWORD (64-bit) units is disabled 1: Data swapping in LONG LWORD (64-bit) units is enabled This should be set to 1 in most cases, but when data has been swapped in 64-bit units by another data processing channel, specify 0
10	A_LWS	0	R/W	α Plane Data Swapping in Longword Units 0: Data swapping in long word (32-bit) units is disabled 1: Data swapping in longword (32-bit) units is enabled This should be set to 1 in most cases, but when data has been swapped in 32-bit units by another data processing channel, specify 0
9	A_WDS	0	R/W	α Plane Data Swapping in Word Units 0: Data swapping in word (16-bit) units is disabled 1: Data swapping in word (16-bit) units is enabled
8	A_BTS	0	R/W	α Plane Data Swapping in Byte Units 0: Data swapping in byte (8-bit) units is disabled 1: Data swapping in byte (8-bit) units is enabled
7 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3	P_LLS	0	R/W	Picture Plane Data Swapping in LONG LWORD Units 0: Data swapping in LONG LWORD (64-bit) units is disabled 1: Data swapping in LONG LWORD (64-bit) units is enabled This should be set to 1 in most cases, but when data has been swapped in 64-bit units by another data processing channel, specify 0
2	P_LWS	0	R/W	Picture Plane Data Swapping in Longword Units 0: Data swapping in longword (32-bit) units is disabled 1: Data swapping in longword (32-bit) units is enabled This should be set to 1 in most cases, but when data has been swapped in 32-bit units by another data processing channel, specify 0

Bit	Bit Name	Initial Value	R/W	Description
1	P_WDS	0	R/W	Picture Plane Data Swapping in Word Units 0: Data swapping in word (16-bit) units is disabled 1: Data swapping in word (16-bit) units is enabled
0	P_BTS	0	R/W	Picture Plane Data Swapping in Byte Units 0: Data swapping in byte (8-bit) units is disabled 1: Data swapping in byte (8-bit) units is enabled

When the virtual input function of the RPFn is used (VI6\_RPFn\_INFMT.VIR = 1), this register setting is ignored. Swapping of RPF input data can be specified separately for the  $\alpha$  plane and picture plane. Table 28.21 shows the data order before and after swapping according to the LONG LWORD, longword, word, and byte swapping settings.

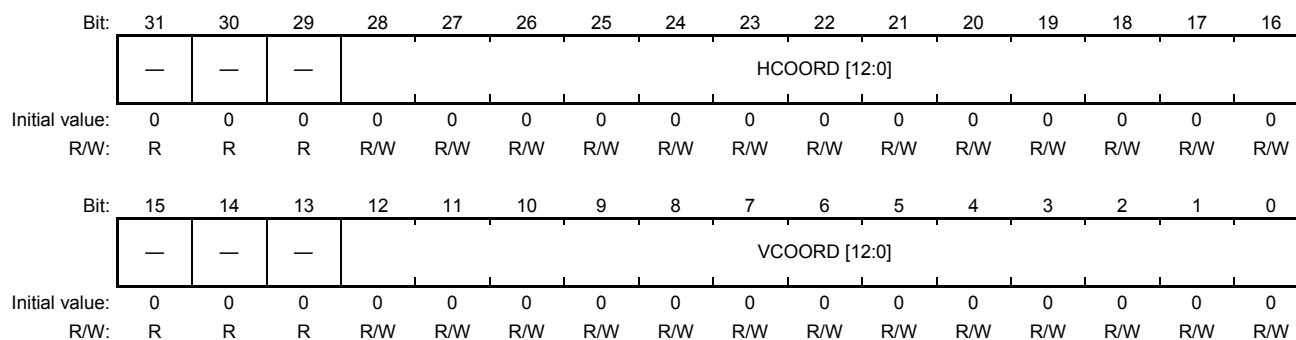
**Table 28.21 Data Order after Swapping according to Swapping Register Settings**

VI6_PRFn_DSWAP				Changed Order of Data (Each value indicates one byte)																
*_LLS	*_LWS	*_WDS	*_BTS	Input →	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	0	Output →	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	1		1	0	3	2	5	4	7	6	9	8	11	10	13	12	15	14
0	0	1	0		2	3	0	1	6	7	4	5	10	11	8	9	14	15	12	13
0	0	1	1		3	2	1	0	7	6	5	4	11	10	9	8	15	14	13	12
0	1	0	0		4	5	6	7	0	1	2	3	12	13	14	15	8	9	10	11
0	1	0	1		5	4	7	6	1	0	3	2	13	12	15	14	9	8	11	10
0	1	1	0		6	7	4	5	2	3	0	1	14	15	12	13	10	11	8	9
0	1	1	1		7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8
1	0	0	0		8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7
1	0	0	1		9	8	11	10	13	12	15	14	1	0	3	2	5	4	7	6
1	0	1	0		10	11	8	9	14	15	12	13	2	3	0	1	6	7	4	5
1	0	1	1		11	10	9	8	15	14	13	12	3	2	1	0	7	6	5	4
1	1	0	0		12	13	14	15	8	9	10	11	4	5	6	7	0	1	2	3
1	1	0	1		13	12	15	14	9	8	11	10	5	4	7	6	1	0	3	2
1	1	1	0		14	15	12	13	10	11	8	9	6	7	4	5	2	3	0	1
1	1	1	1		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

### 28.2.7.5 RPFn Display Location Registers (VI6\_RPFn\_LOC)

Note: See Table 28.15 for details on which RZ/G series products have which registers.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√



Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28 to 16	HCOORD [12:0]	All 0	R/W	Horizontal Coordinate of Sub layer Display Location on Master Layer These bits specify the left-end location of the sub layer displayed by the RPFn and the subsequent module connected through the DPR. Specify the horizontal coordinate of the location in pixel units with the left-end pixel of the master layer set at coordinate 0. When the RPFn is the master layer, set these bits to 0.  If the sub layer extends beyond the master layer according to the HCOORD setting, the extended section is cut off at the right end of the master layer. Even in this case, however, a bus transfer that is unnecessary for output image generation is executed since the whole sub layer data is read from the external memory. Appropriate coordinate setting is recommended so that the sub layer does not extend beyond the right end of the master layer.  If the HCOORD value is larger than the horizontal size of the master layer image, the entire sub layer goes outside of the master layer. Such setting is prohibited.  A value from 0 to 8,189 can be specified.
15 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
12 to 0	VCOORD [12:0]	All 0	R/W	<p>Vertical Coordinate of Sub layer Display Location on Master Layer</p> <p>These bits specify the top-end location of the sub layer displayed by the RPFn and the subsequent module connected through the DPR. Specify the vertical coordinate of the location in pixel units with the top-end pixel of the master layer set at coordinate 0. When the RPFn is the master layer, set these bits to 0.</p> <p>If the sub layer extends beyond the master layer according to the VCOORD setting, the extended section is cut off at the bottom end of the master layer. Even in this case, however, a bus transfer that is unnecessary for output image generation is executed since the whole sub layer data is read from the external memory. Appropriate coordinate setting is recommended so that the sub layer does not extend beyond the bottom end of the master layer.</p> <p>If the VCOORD value is larger than the vertical size of the master layer image, the entire sub layer goes outside of the master layer. Such setting is prohibited.</p> <p>A value from 0 to 8,189 can be specified.</p>

Figure 28.24 shows an example of RPF1 and RPF2 offsets with respect to master layer RPF0. Although this figure only shows sub layers RPF1 and RPF2, specify offsets for all RPFs other than the master layer in the same way as shown in this example.

Whether an RPFn is the master layer or a sub layer is determined through the selection of the source RPF for WPFn (the VI6\_WPFn\_SRCRPF setting). For details, refer to section 28.2.8.1.

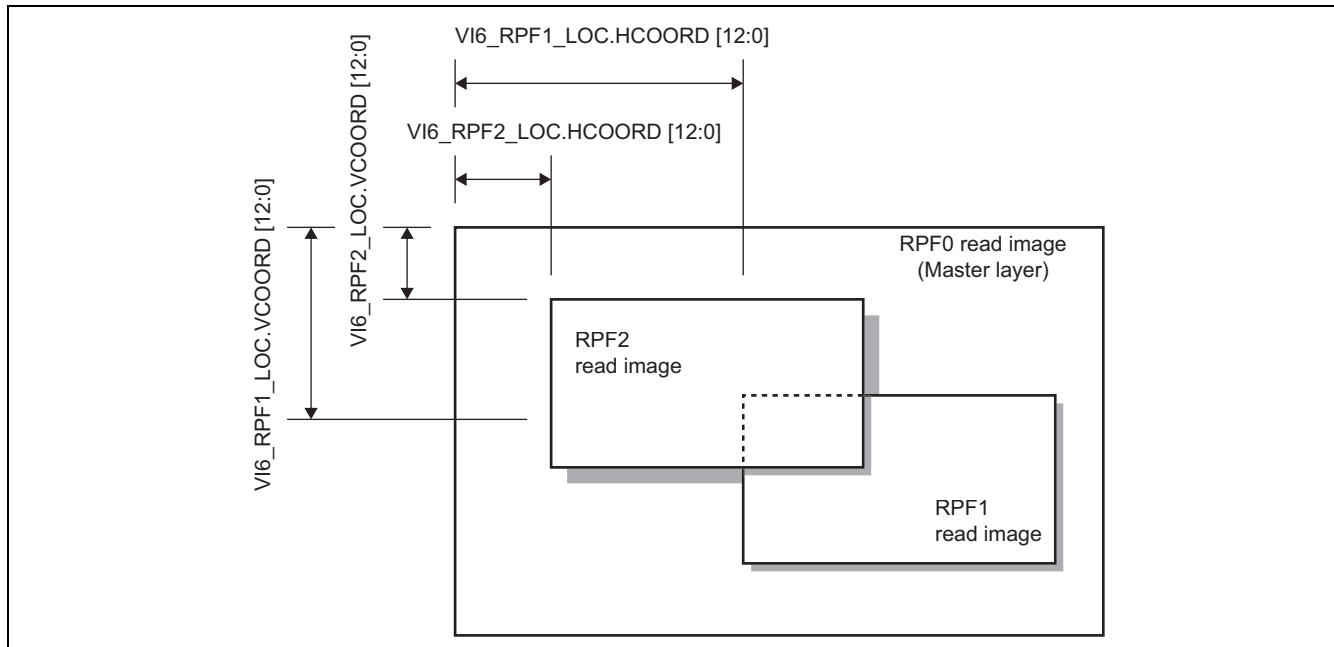


Figure 28.24 RPF1 and RPF2 Offsets from Master Layer

### 28.2.7.6 RPFn $\alpha$ Plane Selection Control Registers (VI6\_RPFn\_ALPH\_SEL)

Note: See Table 28.15 for details on which RZ/G series products have which registers.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	ASEL [2:0]			IROP [3:0]				BSEL	—	—	—	AEXT [1:0]		—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R/W	R/W	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ALPHA1 [7:0]								ALPHA0 [7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
30 to 28	ASEL[2:0]	000	R/W	<p><math>\alpha</math> Format and Processing Method Select</p> <p>These bits select how to handle the <math>\alpha</math> value to be used. The RPF handles two types of <math>\alpha</math> value; 8-bit and 1-bit values. When a 1-bit <math>\alpha</math> value is used, VSP1 assumes that the 1-bpp <math>\alpha</math> value for each pixel is stored in the order from MSB to LSB in each byte (big endian).</p> <p>The <math>\alpha</math> value is used as either transparency information or mask information. Transparency information is included in the <math>\alpha</math> plane read from external memory when the ASEL bits are set to 1 or 3 and in the <math>\alpha</math> value stored in the packed RGB bit field when these bits are set to 0 or 2. The <math>\alpha</math> value as transparency information is sent as the destination value to the IROP as shown in Figure 28.25 and then output to the subsequent modules. The output <math>\alpha</math> value is used, for example, for blending in the BRU.</p> <p>The <math>\alpha</math> value as mask information is used for IROP operation in the RPF. The mask information is included in the <math>\alpha</math> plane read from external RAM when the ASEL bits are set to 0 or 2 and the source value is used in IROP operation (IROP setting other than 0, 5, 10, or 15). This <math>\alpha</math> value is sent as the source value to the IROP as shown in Figure 28.25.</p> <p>Note that the <math>\alpha</math> value selected through the ASEL bits has a lower priority than the VI6_RPFn_CKEY_SET*.AP* value replaced through the color keying function. When the color keying function is used, the <math>\alpha</math> value may be replaced with the VI6_RPFn_CKEY_SET*.AP* value regardless of the ASEL bit setting.</p> <p>When using the virtual input function (VI6_RPFn_INFMT.VIR = 1), specify 4.</p>

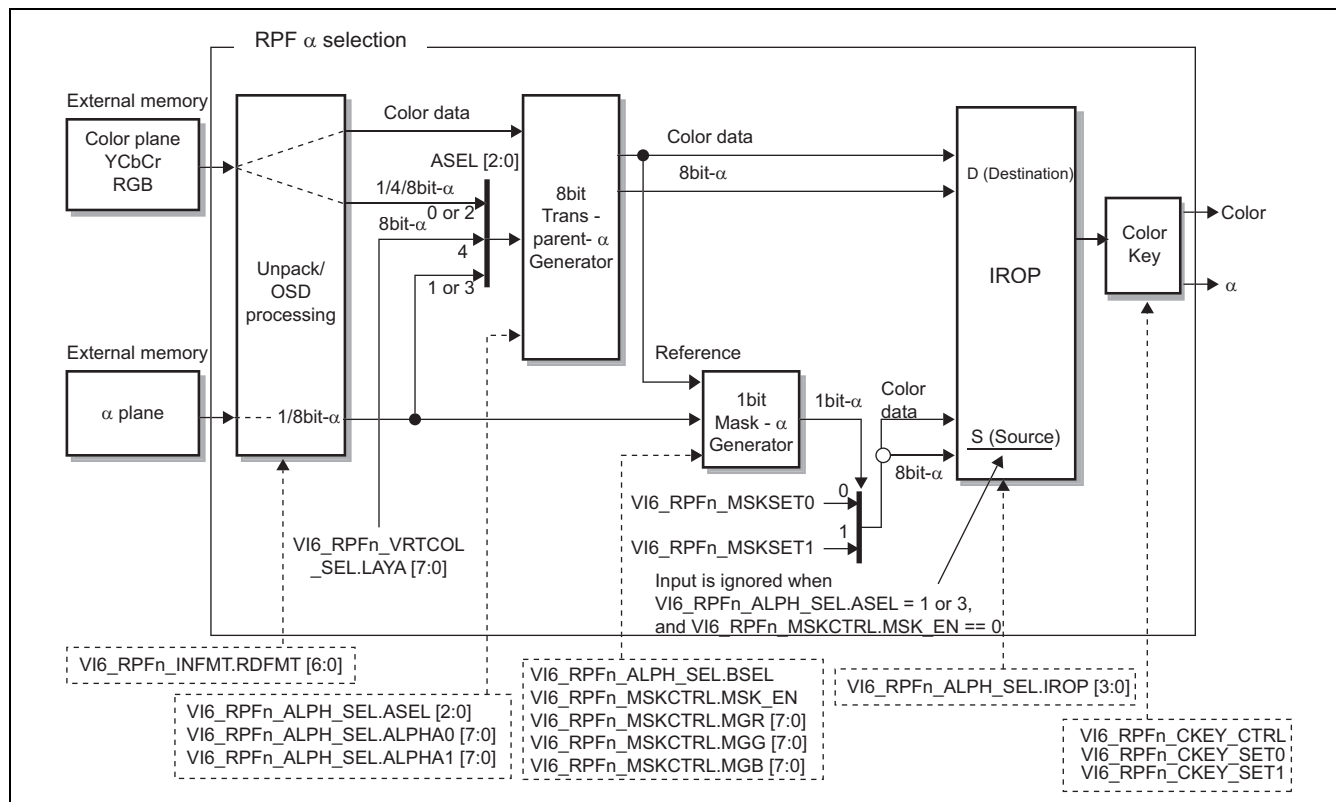
Bit	Bit Name	Initial Value	R/W	Description
30 to 28	ASEL[2:0]	000	R/W	<p><u>000: 1, 4, or 8-bit packed <math>\alpha</math> + plane <math>\alpha</math> (IROP ! = 0, 5, 10, 15)</u></p> <p>The <math>\alpha</math> bit field in 1, 4, or 8-bit packed <math>\alpha</math> is handled as transparency information. Be sure to specify the packed format that includes <math>\alpha</math> through VI6_RPFn_INFMT.RDFMT.</p> <p>When VI6_RPFn_MSKCTRL.MSK_EN is 0 and the IROP bit value is not 0, 5, 10, or 15, the <math>\alpha</math> plane should be read as mask information. Specify the number of <math>\alpha</math> data bits (BSEL) stored in the <math>\alpha</math> plane and the <math>\alpha</math> plane read start address (VI6_RPFn_SRCM_ADDR_AI). When the IROP bits are set to 0, 5, 10, or 15, the <math>\alpha</math> plane is not read.</p> <p><u>001: 8-bit plane <math>\alpha</math></u></p> <p>The 8-bit <math>\alpha</math> plane is read from external RAM as transparency information. When the packed RGB format has a bit field for <math>\alpha</math>, the information in the <math>\alpha</math> bit field is discarded. The <math>\alpha</math> plane read start address (VI6_RPFn_SRCM_ADDR_AI) should be specified. The <math>\alpha</math> value goes through the 8-bit transparent <math>\alpha</math> generator shown in Figure 28.25 without change.</p> <p>When VI6_RPFn_MSKCTRL.MSK_EN is 0, IROP operation cannot be executed; set the IROP bits to 0 in this case. When VI6_RPFn_MSKCTRL.MSK_EN is 1, IROP operation can be executed.</p> <p><u>010: 1-bit packed <math>\alpha</math> + plane <math>\alpha</math> (IROP ! = 0, 5, 10, 15)</u></p> <p>The 1-bit packed <math>\alpha</math> input is converted by the 8-bit transparent <math>\alpha</math> generator shown in Figure 28.25 according to the ALPHA0/1 setting into the 8-bit <math>\alpha</math> value as transparency information. Select the packed input format that includes a 1-bit <math>\alpha</math> field.</p> <p>When VI6_RPFn_MSKCTRL.MSK_EN is 0 and the IROP value is not 0, 5, 10, or 15, the <math>\alpha</math> plane should be read as mask information. Specify the number of <math>\alpha</math> data bits (BSEL) stored in the <math>\alpha</math> plane and the <math>\alpha</math> plane read start address (VI6_RPFn_SRCM_ADDR_AI). When the IROP bits are set to 0, 5, 10, or 15, the <math>\alpha</math> plane is not read.</p> <p><u>011: 1-bit plane <math>\alpha</math></u></p> <p>The 1-bit <math>\alpha</math> plane is read from external RAM and converted by the 8-bit transparent <math>\alpha</math> generator shown in Figure 28.25 according to the ALPHA0/1 setting into the 8-bit <math>\alpha</math> value as transparency information. When the packed RGB format has a bit field for <math>\alpha</math>, the information in the <math>\alpha</math> bit field is discarded. The <math>\alpha</math> plane read start address (VI6_RPFn_SRCM_ADDR_AI) should be specified.</p> <p>When VI6_RPFn_MSKCTRL.MSK_EN is 0, IROP operation cannot be executed; set the IROP bits to 0 in this case. When VI6_RPFn_MSKCTRL.MSK_EN is 1, IROP operation can be executed.</p> <p><u>100: Fixed <math>\alpha</math></u></p> <p>The fixed <math>\alpha</math> value (VI6_RPFn_VRTCOL_SET.LAYA value) is output from the RPF. IROP operation cannot be executed; set the IROP bits to 0 in this case.</p> <p><u>101 to 111: Setting prohibited.</u></p>

Bit	Bit Name	Initial Value	R/W	Description
27 to 24	IROP[3:0]	0000	R/W	<p>IROP Operation Setting</p> <p>These bits specify the operator to be executed in the IROP operation unit shown in Figure 28.25. The source (S) for the IROP operation is the pixel data and <math>\alpha</math> data specified in the VI6_RPFn_MSKSET0 or VI6_RPFn_MSKSET1 IROP input value register, which is selected according to the value (0 or 1) generated by the 1-bit mask generator. The destination (D) is the image data (RGB/YCbCr) and 8-bit <math>\alpha</math> data output from the unpack/OSD processor. IROP operation is applied both for the image data and <math>\alpha</math> data between the source and destination data.</p> <p>If these bits are set to the operation that involves the source (S) (IROP setting other than 0, 5, 10, or 15) while VI6_RPFn_MSKCTRL.MSK_EN is 0, the <math>\alpha</math> plane is read from the external RAM to be used for the <math>\alpha</math> value for IROP operation; specify the <math>\alpha</math> plane read start address (VI6_RPFn_SRCM_ADDR_A).</p> <p>When the virtual input function is used (VI6_RPFn_INFMT.VIR = 1), IROP operation is not available; set these bits to B'0000.</p> <p>0000: NOP(D)  0001: AND(S &amp; D)  0010: AND_REVERSE(S &amp; ~D)  0011: COPY(S)  0100: AND_INVERTED(~S &amp; D)  0101: CLEAR(0)  0110: XOR(S ^ D)  0111: OR(S   D)  1000: NOR(~(S   D))  1001: EQUIV(~(S ^ D))  1010: INVERT(~D)  1011: OR_REVERSE(S   ~D)  1100: COPY_INVERTED(~S)  1101: OR_INVERTED(~S   D)  1110: NAND(~(S &amp; D))  1111: SET(all 1)</p>
23	BSEL	0	R/W	<p><math>\alpha</math> Bit Count Conversion Selection for 1-Bit Mask Generator</p> <p>Specifies the number of bits in the <math>\alpha</math> plane to be read as mask information from the external RAM. The <math>\alpha</math> value in mask information is used for the source (S) in IROP. When <math>\alpha</math> plane data is eight bits, it is converted to one bit through the 1-bit mask generator shown in Figure 28.25.</p> <p>Note that this bit setting is valid when the ASEL bits are set to 0 or 2 and VI6_RPFn_MSKCTRL.MSK_EN is set to 0. In other cases, this bit setting has no effect.</p> <p><u>0: 8-bit <math>\alpha</math> is converted to 1-bit <math>\alpha</math> through the 1-bit mask generator.</u>  When the 8-bit <math>\alpha</math> value input to the RPF is not 0, it is converted to 1; when the value is 0, it is converted to 0.</p> <p><u>1: <math>\alpha</math> value goes through the 1-bit mask generator.</u>  The 1-bit <math>\alpha</math> value input to the RPF is output through the 1-bit mask generator without change.</p>
22 to 20	—	000	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>



Bit	Bit Name	Initial Value	R/W	Description
19, 18	AEXT[1:0]	00	R/W	<p>Lower-Bit <math>\alpha</math> Value Extension Method Set</p> <p>These bits specify the method for extending the input <math>\alpha</math> data to eight bits through the unpack processing.</p> <p>00: The lower-order bits of <math>\alpha</math> value are extended with 0.</p> <p>01: The upper-order bits of <math>\alpha</math> value are copied to the lower-order bits.</p> <p>10: The lower-order bits of <math>\alpha</math> value are extended with 0. The maximum value is limited to H'FF.</p> <p>11: Setting prohibited</p>
17, 16	—	All 0	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>
15 to 8	ALPHA1 [7:0]	H'00	R/W	<p>8-Bit <math>\alpha</math> Value Output when 1-Bit <math>\alpha</math> Value is 1</p> <p>These bits specify the 8-bit <math>\alpha</math> value to be output when 1-bit <math>\alpha</math> data is input and the <math>\alpha</math> value input to the 8-bit transparent <math>\alpha</math> generator shown in Figure 28.25 is 1. This setting is valid when the ASEL bits are set to B'010 or B'011.</p> <p>A value from 0 to 255 can be specified.</p>
7 to 0	ALPHA0 [7:0]	H'00	R/W	<p>8-Bit <math>\alpha</math> Value Output when 1-Bit <math>\alpha</math> Value is 0</p> <p>These bits specify the 8-bit <math>\alpha</math> value to be output when 1-bit <math>\alpha</math> data is input and the <math>\alpha</math> value input to the 8-bit transparent <math>\alpha</math> generator shown in Figure 28.25 is 0. This setting is valid when the ASEL bits are set to B'010 or B'011.</p> <p>A value from 0 to 255 can be specified.</p>

Figure 28.25 shows the relationship between the  $\alpha$  selector, IROP operation unit, color keying unit, and related registers (color space conversion is omitted but is behind the color keying unit as shown in Figure 28.3). The IROP operation unit receives two inputs, source and destination. The image data input from the external memory is processed through the unpack processor and 8-bit transparent  $\alpha$  generator and then input to the IROP operation unit as destination data. The  $\alpha$  plane data input from the external memory is sent to the 8-bit transparent  $\alpha$  generator when the ASEL bits are set to 1 or 3, or sent to the 1-bit mask  $\alpha$  generator when the ASEL bits are set to 0 or 2. For the pixel data and 8-bit  $\alpha$  value on the source side of the IROP operation unit, either the VI6\_RPFn\_MSKSET0 value or VI6\_RPFn\_MSKSET1 values will be selected according to the 1-bit  $\alpha$  value output by the 1-bit mask  $\alpha$  generator.



**Figure 28.25 Configuration of  $\alpha$  Selector and IROP Operation Unit in RPF**

The following describes the function of each block shown in Figure 28.25. Read the following while referring to the figure as necessary.

#### Unpack/OSD processor:

Unpacks each component and  $\alpha$  value of the image data according to the packed format specified in VI6\_RPFn\_INFMT.RDFMT.

#### 8-bit transparent $\alpha$ generator:

Converts the input  $\alpha$  value into 8-bit  $\alpha$  when the input  $\alpha$  is four bits or one bit.

When VI6\_RPFn\_ALPH\_SEL.ASEL are set to 0 (8-, 4-, or 1-bit packed  $\alpha$ ), this generator outputs the input  $\alpha$  value without change if the  $\alpha$  bit field in the packed  $\alpha$  data is eight bits; if the  $\alpha$  bit field is less than eight bits, it is converted to an 8-bit  $\alpha$  value by extending the LSB side according to the VI6\_RPFn\_ALPH\_SEL.AEXT setting.

When VI6\_RPFn\_ALPH\_SEL.ASEL are set to 1 (8-bit plane  $\alpha$ ) or 4 (fixed  $\alpha$ ), this generator outputs the input 8-bit plane  $\alpha$  without change. If a packed  $\alpha$  value is included in RGB data, it is discarded.

When VI6\_RPFn\_ALPH\_SEL.ASEL are set to 2 (1-bit packed  $\alpha$ ) or 3 (8-bit  $\alpha$  generated from 1-bit plane  $\alpha$ ), an 8-bit  $\alpha$  value is generated by using the VI6\_RPFn\_ALPH\_SEL.ALPHA0[7:0] value when the input 1-bit  $\alpha$  value is 0 or by using the VI6\_RPFn\_ALPH\_SEL.ALPHA1[7:0] value when the input 1-bit  $\alpha$  value is 1. When VI6\_RPFn\_ALPH\_SEL.ASEL is set to 3, a packed  $\alpha$  value that is included in RGB data is discarded.

**1-bit mask  $\alpha$  generator:**

Generates 1-bit  $\alpha$  data from the input 8-bit  $\alpha$  data or pixel data. When the input  $\alpha$  data is one bit, this generator outputs it without change.

When VI6\_RPFn\_ALPH\_SEL.ASEL are set to 0 (8-, 4-, or 1-bit packed  $\alpha$ ) or 2 (plane  $\alpha$ ) and VI6\_RPFn\_MSKCTRL.MSK\_EN is set to 0, the  $\alpha$  plane read from the external memory to be used in IROP is converted to 1-bit  $\alpha$  data when necessary. When the  $\alpha$  plane data read from the external RAM is eight bits (BSEL = 0), if the value is 0, a 1-bit  $\alpha$  value of 0 is generated; if the value is not 0, a 1-bit  $\alpha$  value of 1 is generated. When the  $\alpha$  plane data is one bit (BSEL = 1), this generator outputs it without change.

When the value of the 1-bit  $\alpha$  generated by the 1-bit mask  $\alpha$  generator is 0, the 8-bit  $\alpha$  and pixel data specified in VI6\_RPFn\_MSKSET0 are output as the source. When the generated 1-bit  $\alpha$  value is 1, the 8-bit  $\alpha$  and pixel data specified in VI6\_RPFn\_MSKSET1 are output as the source.

As shown in Figure 28.25, when VI6\_RPFn\_ALPH\_SEL.ASEL are set to 1 (8-bit plane  $\alpha$ ) or 3 (1-bit plane  $\alpha$ ), the  $\alpha$  plane read from the external RAM is sent to the 8-bit transparent  $\alpha$  generator as transparency information. When VI6\_RPFn\_MSKCTRL.MSK\_EN is set to 0, the 1-bit  $\alpha$  for masking is generated according to the input  $\alpha$  plane (refer to section 28.2.7.8), but the 1-bit mask  $\alpha$  generator does not refer to the input  $\alpha$  plane because it is input to the 8-bit transparent  $\alpha$  generator as transparency information. Accordingly, the 1-bit mask  $\alpha$  generator does not generate a 1-bit  $\alpha$  for masking and the data on the source side becomes invalid; that is, IROP operation cannot be executed. Set the IROP bits to 0 in this case. In contrast, when VI6\_RPFn\_MSKCTRL.MSK\_EN is set to 1, the 1-bit mask  $\alpha$  generator creates  $\alpha$  data for masking according to the pixel data instead of the input  $\alpha$  plane data, and IROP operation can be executed in this case.

**IROP operation unit**

Executes ROP operation according to the opcode specified in VI6\_RPFn\_ALPH\_SEL.IROP. For ROP operation (other than NOP), valid values should be input both for the source and destination. As described in the above (description of the 1-bit mask  $\alpha$  generator), when VI6\_RPFn\_ALPH\_SEL.ASEL are set to 1 or 3 and VI6\_RPFn\_MSKCTRL.MSK\_EN is set to 0, the source data for the IROP operation unit is treated as invalid; set VI6\_RPFn\_ALPH\_SEL.IROP to 0 (NOP). When VI6\_RPFn\_ALPH\_SEL.ASEL are set to 4, a fixed  $\alpha$  value is output from the RFP and IROP operation is not available. In the same way as the above case, set VI6\_RPFn\_ALPH\_SEL.IROP to 0 (NOP).

To specify a valid source value for the IROP operation unit and execute IROP operation (specify an opcode other than NOP in the IROP bits), specify register values as shown in Table 28.22. Where the source input state is indicated as "Valid" in the table, IROP operation can be executed. In the cases where IROP operation is not available, set the IROP bits to 0 (NOP).

**Table 28.22 Source Input State in IROP Operation Unit**

		VI6_RPFn_MSKCTRL.MSK_EN		
		0 (Source data is generated according to input $\alpha$ plane)		1 (Source data is generated according to the destination-side pixel data)
VI6_RPFn_ALPH_SEL.ASEL [2:0]				
B'000	(1-, 4-, or 8-bit packed $\alpha$ + plane $\alpha$ )	Valid	( $\alpha$ plane input)	Valid
B'001	(8-bit $\alpha$ plane)	Invalid	(IROP operation is not available; $\alpha$ plane is output to the subsequent modules behind RPF)	Valid
B'010	(8-bit $\alpha$ generated from 1-bit packed $\alpha$ + plane $\alpha$ )	Valid	( $\alpha$ plane input)	Valid
B'011	(8-bit $\alpha$ generated from 1-bit plane $\alpha$ )	Invalid	(IROP operation is not available; $\alpha$ plane is output to the subsequent modules behind RPF)	Valid
B'100	(Fixed $\alpha$ )	Invalid (IROP operation is not available; fixed $\alpha$ is output to the subsequent modules behind RPF)		

For the handling of the  $\alpha$  values shown in Figure 28.25 and Table 28.22, the relationship between the RPF input format and RPF output  $\alpha$  value is shown in Table 28.23. Where only bit names are shown in the table, the bits are in VI6\_RPFn\_ALPH\_SEL described in this section.

**Table 28.23  $\alpha$  Value Selected and Output according to ASEL Bits in Each Input Format**

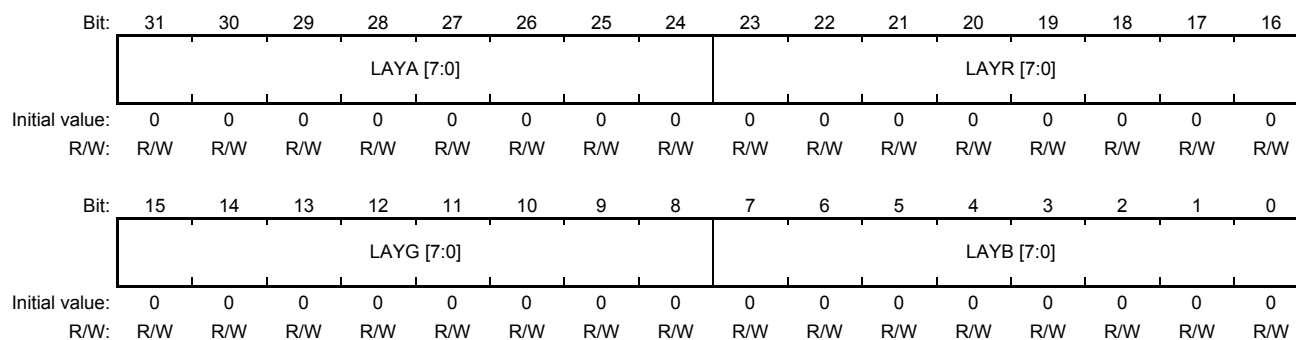
ASEL Setting		$\alpha$ Value Output for Each Input Format		
		RGB	YCbCr	OSD-CLUT
B'000	(8-, 4-, or 1-bit packed $\alpha$ is input)	1-, 4-, or 8-bit pixel $\alpha$	H'FF*	$\alpha$ value in CLUT
B'001	(8-bit plane $\alpha$ is input)	8-bit $\alpha$ plane	8-bit $\alpha$ plane	8-bit $\alpha$ plane
B'010	(8-bit $\alpha$ is generated from the 1-bit packed $\alpha$ input)	ALPHA0 or ALPHA1 setting	H'FF*	H'FF
B'011	(8-bit $\alpha$ is generated from the 1-bit plane $\alpha$ input)	ALPHA0 or ALPHA1 setting	ALPHA0 or ALPHA1 setting	ALPHA0 or ALPHA1 setting
B'100	(Fixed $\alpha$ is output)	VI6_RPFn_VRTCOL_SET.LAYA setting		

Note: \* Fixed value H'FF is output because packed  $\alpha$  is not included in YCbCr.

### 28.2.7.7 RPFn Virtual Plane Color Information Registers (VI6\_RPFn\_VRTCOL\_SET)

Note: See Table 28.15 for details on which RZ/G series products have which registers.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

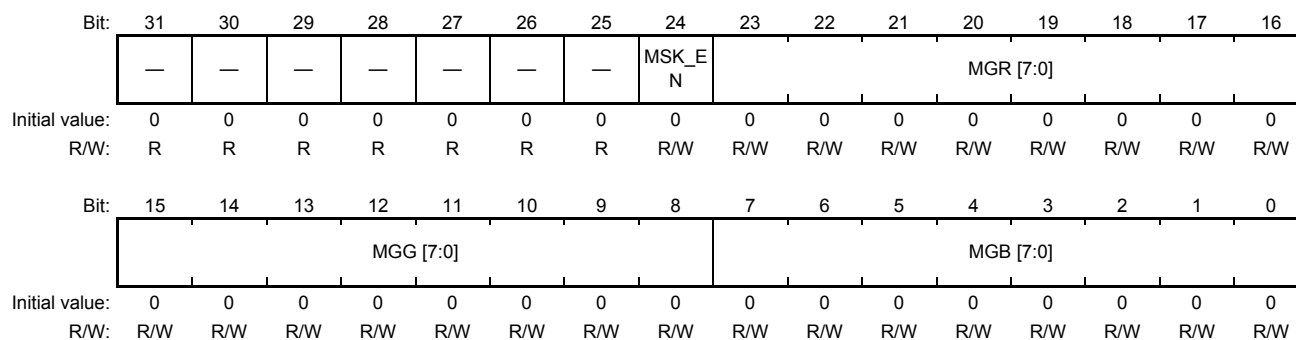


Bit	Bit Name	Initial Value	R/W	Description
31 to 24	LAYA [7:0]	H'00	R/W	<p>Virtual-Input Fixed <math>\alpha</math> Value</p> <p>These bits specify the fixed <math>\alpha</math> value generated in the RPFn when the virtual input function is enabled through the VI6_RPFn_INFMT.VIR setting.</p> <p>When the virtual input function is disabled (VI6_RPFn_INFMT.VIR = 0), these bits are used to specify the fixed <math>\alpha</math> value to be output from the RPF while VI6_RPFn_ALPH_SEL.ASEL are set to 4. A value from 0 to 255 can be specified.</p>
23 to 16	LAYR [7:0]	H'00	R/W	<p>Virtual-Input Fixed R/Cr Component Value</p> <p>These bits specify the fixed R or Cr value generated in the RPFn when the virtual input function is enabled through the VI6_RPFn_INFMT.VIR setting. When VI6_RPFn_INFMT.RDFMT is set to 19, the value specified in these bits is used as the R value. When VI6_RPFn_INFMT.RDFMT is set to 64, the value specified in these bits is used as the Cr value. A value from 0 to 255 can be specified.</p>
15 to 8	LAYG [7:0]	H'00	R/W	<p>Virtual-Input Fixed G/Y Component Value</p> <p>These bits specify the fixed G or Y value generated in the RPFn when the virtual input function is enabled through the VI6_RPFn_INFMT.VIR setting. When VI6_RPFn_INFMT.RDFMT is set to 19, the value specified in these bits is used as the G value. When VI6_RPFn_INFMT.RDFMT is set to 64, the value specified in these bits is used as the Y value. A value from 0 to 255 can be specified.</p>
7 to 0	LAYB [7:0]	H'00	R/W	<p>Virtual-Input Fixed B/Cb Component Value</p> <p>These bits specify the fixed B or Cb value generated in the RPFn when the virtual input function is enabled through the VI6_RPFn_INFMT.VIR setting. When VI6_RPFn_INFMT.RDFMT is set to 19, the value specified in these bits is used as the B value. When VI6_RPFn_INFMT.RDFMT is set to 64, the value specified in these bits is used as the Cb value. A value from 0 to 255 can be specified.</p>

### 28.2.7.8 RPFn Mask Control Registers (VI6\_RPFn\_MSKCTRL)

Note: See Table 28.15 for details on which RZ/G series products have which registers.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√



Bit	Bit Name	Initial Value	R/W	Description
31 to 25	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
24	MSK_EN	0	R/W	Mask Generation Specification Specifies the method of $\alpha$ value generation in the 1-bit mask $\alpha$ generator shown in Figure 28.25. 0: A 1-bit mask value is generated according to the input $\alpha$ plane value. When the input $\alpha$ is in the 1-bit format (VI6_RPFn_ALPH_SEL.BSEL = 1), the 1-bit mask value is output without change. When the input $\alpha$ is in the 8-bit format (VI6_RPFn_ALPH_SEL.BSEL = 0), the 1-bit mask value is 0 if the $\alpha$ value is H'00; otherwise, the 1-bit mask value is 1. 1: The R/Cr, G/Y, and B/Cb components of the image input to the destination side of the IROP operation unit are compared with the values specified in the MGR, MGG, and MGB bits, respectively. When all values match, 1 is output as the 1-bit mask value, and in other cases, 0 is output. When the generated 1-bit mask data is not used, set VI6_RPFn_ALPH_SEL.IROP to 0.
23 to 16	MGR [7:0]	H'00	R/W	R/Cr Comparison Value for 1-Bit $\alpha$ Generation These bits specify the R/Cr value to be compared for 1-bit $\alpha$ generation by using the pixel data on the destination side. When RGB is specified as the RPFn input format through VI6_RPFn_INFMT.RDFMT, specify an R value for comparison. When YCbCr is specified, specify a Cr value for comparison. This setting is ignored when the MSK_EN bit is set 0. A value from 0 to 255 can be specified.
15 to 8	MGG [7:0]	H'00	R/W	G/Y Comparison Value for 1-Bit $\alpha$ Generation These bits specify the G/Y value to be compared for 1-bit $\alpha$ generation by using the pixel data on the destination side. When RGB is specified as the RPFn input format through VI6_RPFn_INFMT.RDFMT, specify a G value for comparison. When YCbCr is specified, specify a Y value for comparison. This setting is ignored when MSK_EN is set to 0. A value from 0 to 255 can be specified.

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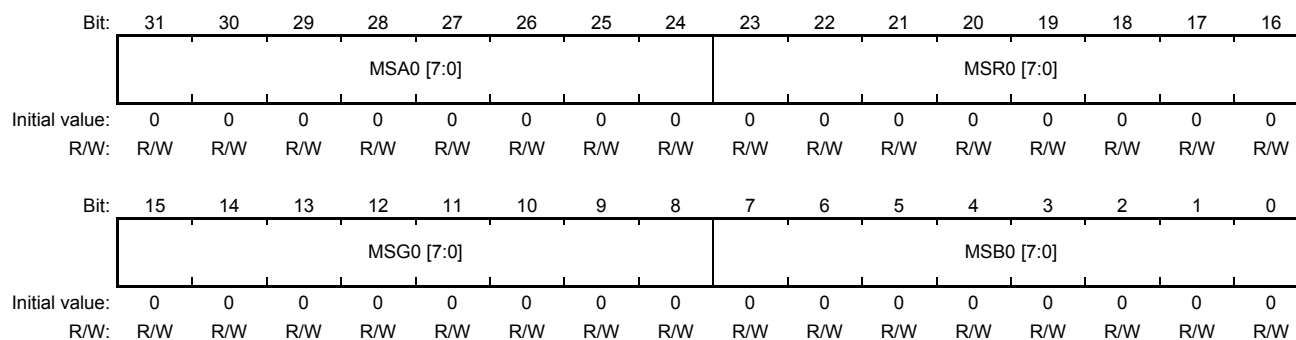
Bit	Bit Name	Initial Value	R/W	Description
7 to 0	MGB [7:0]	H'00	R/W	<p>B/Cb Comparison Value for 1-Bit <math>\alpha</math> Generation</p> <p>These bits specify the B/Cb value to be compared for 1-bit <math>\alpha</math> generation by using the pixel data on the destination side. When RGB is specified as the RPFn input format through VI6_RPFn_INFMT.RDFMT, specify a B value for comparison. When YCbCr is specified, specify a Cb value for comparison.</p> <p>This setting is ignored when MSK_EN is set to 0.</p> <p>A value from 0 to 255 can be specified.</p>

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### 28.2.7.9 RPFn IROP-SRC Input Value Registers 0 (VI6\_RPFn\_MSKSET0)

Note: See Table 28.15 for details on which RZ/G series products have which registers.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√



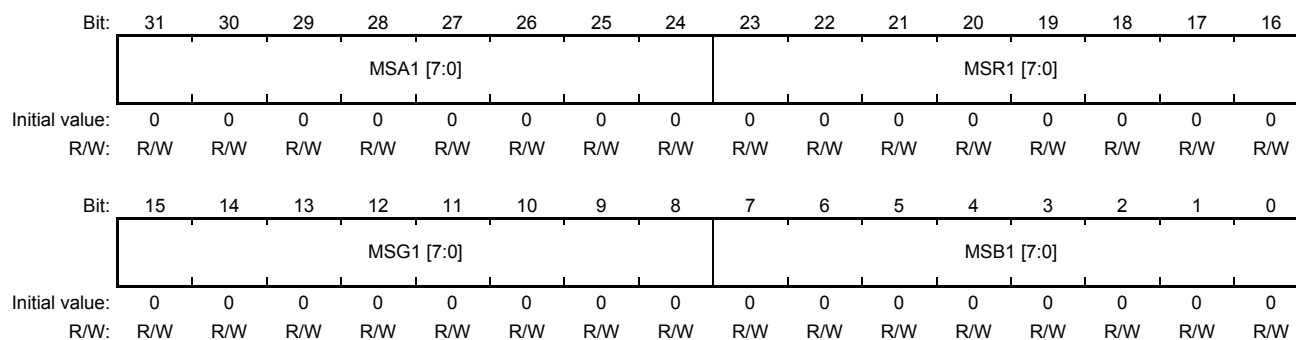
Bit	Bit Name	Initial Value	R/W	Description
31 to 24	MSA0 [7:0]	H'00	R/W	IROP-Source Input $\alpha$ Value when 1-Bit $\alpha$ is 0 These bits specify the 8-bit $\alpha$ value to be input as the source to the IROP operation unit when the internal 1-bit $\alpha$ value generated through the 1-bit mask generator is 0 (Figure 28.25). A value from 0 to 255 can be specified.
23 to 16	MSR0 [7:0]	H'00	R/W	IROP-Source Input R/Cr Value when 1-Bit $\alpha$ is 0 These bits specify the R/Cr value to be input as the source to the IROP operation unit when the internal 1-bit $\alpha$ value generated through the 1-bit mask generator is 0 (Figure 28.25). When RGB is specified as the RPFn input format through VI6_RPFn_INFMT.RDFMT, specify an R component value. When YCbCr is specified, specify a Cr component value. A value from 0 to 255 can be specified.
15 to 8	MSG0 [7:0]	H'00	R/W	IROP-Source Input G/Y Value when 1-Bit $\alpha$ is 0 These bits specify the G/Y value to be input as the source to the IROP operation unit when the internal 1-bit $\alpha$ value generated through the 1-bit mask generator is 0 (Figure 28.25). When RGB is specified as the RPFn input format through VI6_RPFn_INFMT.RDFMT, specify a G component value. When YCbCr is specified, specify a Y component value. A value from 0 to 255 can be specified.
7 to 0	MSB0 [7:0]	H'00	R/W	IROP-Source Input B/Cb Value when 1-Bit $\alpha$ is 0 These bits specify the B/Cb value to be input as the source to the IROP operation unit when the internal 1-bit $\alpha$ value generated through the 1-bit mask generator is 0 (Figure 28.25). When RGB is specified as the RPFn input format through VI6_RPFn_INFMT.RDFMT, specify a B component value. When YCbCr is specified, specify a Cb component value. A value from 0 to 255 can be specified.



### 28.2.7.10 RPFn IROP-SRC Input Value Registers 1 (VI6\_RPFn\_MSKSET1)

Note: See Table 28.15 for details on which RZ/G series products have which registers.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	MSA1 [7:0]	H'00	R/W	IROP-Source Input $\alpha$ Value when 1-Bit $\alpha$ is 1 These bits specify the 8-bit $\alpha$ value to be input as the source to the IROP operation unit when the internal 1-bit $\alpha$ value generated through the 1-bit mask generator is 1. A value from 0 to 255 can be specified (Figure 28.25).
23 to 16	MSR1 [7:0]	All 0	R/W	IROP-Source Input R/Cr Value when 1-Bit $\alpha$ is 1 These bits specify the R/Cr value to be input as the source to the IROP operation unit when the internal 1-bit $\alpha$ value generated through the 1-bit mask generator is 1 (Figure 28.25). When RGB is specified as the RPFn input format through VI6_RPFn_INFMT.RDFMT, specify an R component value. When YCbCr is specified, specify a Cr component value. A value from 0 to 255 can be specified.
15 to 8	MSG1 [7:0]	All 0	R/W	IROP-Source Input G/Y Value when 1-Bit $\alpha$ is 1 These bits specify the G/Y value to be input as the source to the IROP operation unit when the internal 1-bit $\alpha$ value generated through the 1-bit mask generator is 1 (Figure 28.25). When RGB is specified as the RPFn input format through VI6_RPFn_INFMT.RDFMT, specify a G component value. When YCbCr is specified, specify a Y component value. A value from 0 to 255 can be specified.
7 to 0	MSB1 [7:0]	All 0	R/W	IROP-Source Input B/Cb Value when 1-Bit $\alpha$ is 1 These bits specify the B/Cb value to be input as the source to the IROP operation unit when the internal 1-bit $\alpha$ value generated through the 1-bit mask generator is 1 (Figure 28.25). When RGB is specified as the RPFn input format through VI6_RPFn_INFMT.RDFMT, specify a B component value. When YCbCr is specified, specify a Cb component value. A value from 0 to 255 can be specified.

### 28.2.7.11 RPFn Color Keying Control Registers (VI6\_RPFn\_CKEY\_CTRL)

Note: See Table 28.15 for details on which RZ/G series products have which registers.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	CV	—	—	SAPE1	SAPE0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R/W	R/W

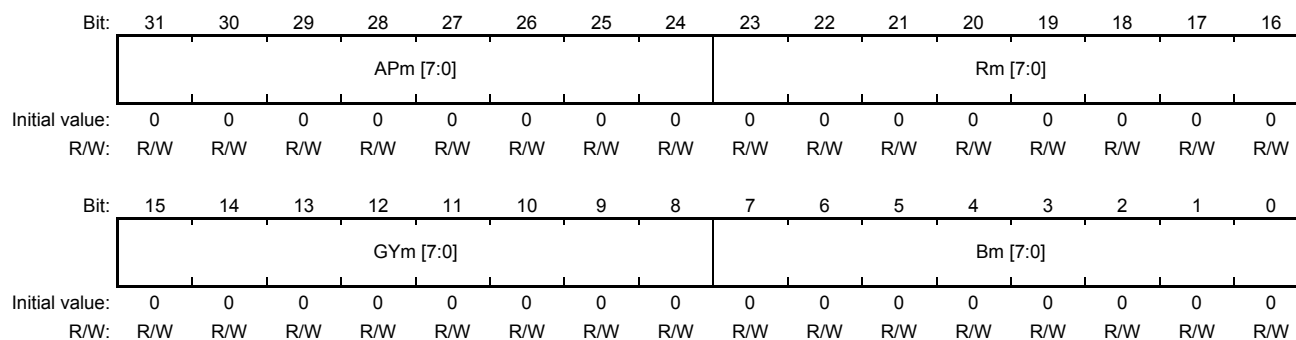
Bit	Bit Name	Initial Value	R/W	Description
31 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	CV	0	R/W	Color Replacement Control This bit controls the color replacement function in the color keying module shown in Figure 28.3. When an RGB format is specified as the color space of the RPFn input data through VI6_RPFn_INFMT.RDFMT, and if all components of an input pixel match the color components specified in VI6_RPFn_CKEY_SET0, the color replacement function replaces the values of the input $\alpha$ and all RGB components with the $\alpha$ and color components specified in VI6_RPFn_CKEY_SET1. When a YCbCr format is specified as the color space of the RPFn input data through VI6_RPFn_INFMT.RDFMT, only the Y data is compared; if the luminance component of an input pixel matches the value specified in VI6_RPFn_CKEY_SET0.GY0, the color replacement function replaces the values of the input $\alpha$ and all YCbCr components with the $\alpha$ and color components specified in VI6_RPFn_CKEY_SET1. When the CV bit is set to 1, the color replacement function is enabled. When using the virtual input function (VI6_RPFn_INFMT.VIR = 1), set this bit to 0. 0: Color replacement function is disabled (transparent color mode). 1: Color replacement function is enabled.
3, 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
1	SAPE1	0	R/W	<p>Comparison Color Data Setting 1 Enable/Disable</p> <p>This bit enables or disables comparison color data setting 1 in the transparent color-matched color mode for the color keying module. <u>This bit setting is valid only when the CV bit is set to 0 and LTH bit is set to 0; it is ignored when the CV bit is set to 1 or LTH bit is set to 1.</u></p> <p>In transparent color-matched color mode, color information 1 (VI6_RPFn_CKEY_SET1.R1/GY1/B1) specified in VI6_RPFn_CKEY_SET1 is compared with the input component values. When the input data is in an RGB format, and if all input values match the specified color information, the input <math>\alpha</math> value is replaced with the value specified in VI6_RPFn_CKEY_SET1.AP. When the input data is in YCbCr format, only the Y data is compared.</p> <p>When using the virtual input function (VI6_RPFn_INFMT.VIR = 1), set this bit to 0.</p> <p>0: Comparison color data setting 1 is disabled. 1: Comparison color data setting 1 is enabled.</p>
0	SAPE0	0	R/W	<p>Comparison Color Data Setting 0 Enable/Disable</p> <p>This bit enables or disables comparison color data setting 0 in the transparent color-matched color mode for the color keying module. <u>This bit setting is valid only when the CV bit is set to 0 and LTH bit is set to 0; it is ignored when the CV bit is set to 1 or LTH bit is set to 1.</u></p> <p>In transparent color-matched color mode, color information 0 (VI6_RPFn_CKEY_SET0.R0/GY0/B0) specified in VI6_RPFn_CKEY_SET0 is compared with the input component values. When the input data is in an RGB format, and if all input values match the specified color information, the input <math>\alpha</math> value is replaced with the value specified in VI6_RPFn_CKEY_SET0.AP. When the input data is in YCbCr format, only the Y data is compared.</p> <p>When using the virtual input function (VI6_RPFn_INFMT.VIR = 1), clear this bit to 0.</p> <p>0: Comparison color data setting 0 is disabled. 1: Comparison color data setting 0 is enabled.</p>

### 28.2.7.12 RPFn Color Keying Color Setting Registers-m (VI6\_RPFn\_CKEY\_SETm: m = 0, 1)

Note: See Table 28.15 for details on which RZ/G series products have which registers.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	APm [7:0]	H'00	R/W	<p><math>\alpha</math> Data in Color Keying Color Information-m</p> <ul style="list-style-type: none"> <li>In transparent color-matched color mode for color keying When the input data matches color setting-m (Rm, GYm, and Bm) for transparent color comparison in the color keying module, the input <math>\alpha</math> value is replaced with the value specified in these bits. Specify the <math>\alpha</math> value to replace the input value.</li> <li>In transparent color-luma threshold mode for color keying When the input data is in YCbCr format, and if input Y value is equal to or smaller than GY0, the input <math>\alpha</math> value is replaced with the value specified in this bit field (AP0). Specify the <math>\alpha</math> value in this bit field (AP0) to replace the input value. AP1 is not used in this mode. Set AP1 to 0 value.</li> <li>In color replacement mode for color keying These bits are not used in this mode. Clear them to 0.</li> </ul> <p><math>\alpha</math> value replacement through these bits in transparent color mode for color keying takes priority over the <math>\alpha</math> value selected through the VI6_RPFn_ALPH_SEL.ASEL setting. A value from 0 to 255 can be specified.</p>
23 to 16	Rm [7:0]	H'00	R/W	<p>R*/Cr Component Data in Color Keying Color Information-m</p> <ul style="list-style-type: none"> <li>In transparent color-matched color mode for color keying Specify the R component value for comparison enabled through the VI6_RPFn_CKEY_CTRL.SAPEm setting. When the RPFn input is in YCbCr format, the color keying module does not compare the Cr component, and the setting of these bits is ignored.</li> <li>In transparent color-luma threshold mode for color keying The color keying module does not refer this bit field, and the setting of these bits is ignored.</li> <li>In color replacement mode for color keying Specify the R component value to be compared with the input data in the color replacement function of the color keying module. A value from 0 to 255 can be specified.</li> </ul>

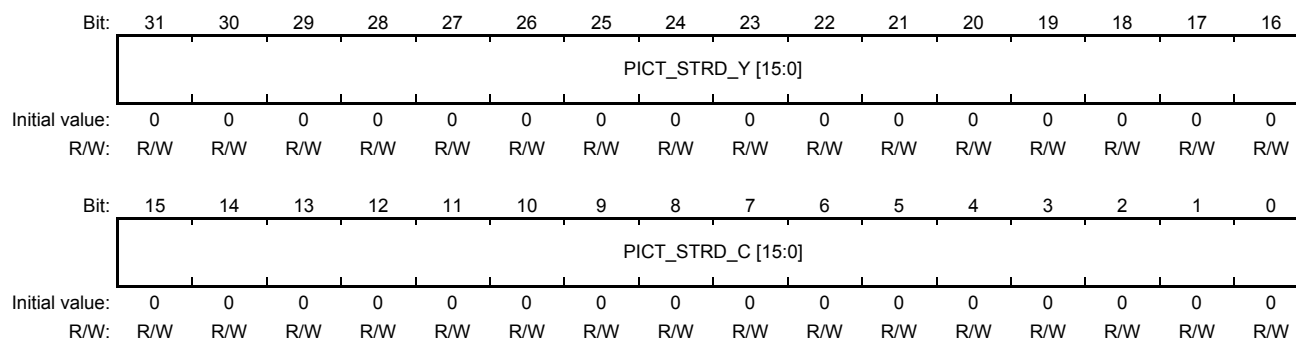
Bit	Bit Name	Initial Value	R/W	Description
15 to 8	GYm [7:0]	H'00	R/W	<p>G*/Y Component Data in Color Keying Color Information-m</p> <ul style="list-style-type: none"> <li>In transparent color-matched color mode for color keying Specify the G/Y component value for comparison enabled through the VI6_RPFn_CKEY_CTRL.SAPEm setting.</li> <li>In transparent color-luma threshold mode for color keying Specify the Y component value in the GY0 to be compared.</li> <li>In color replacement mode for color keying Specify the G/Y component value to be compared with the input data in the color replacement function of the color keying module. A value from 0 to 255 can be specified.</li> </ul>
7 to 0	Bm [7:0]	H'00	R/W	<p>B*/Cb Component Data in Color Keying Color Information-m</p> <ul style="list-style-type: none"> <li>In transparent color-matched color mode for color keying Specify the B component value for comparison enabled through the VI6_RPFn_CKEY_CTRL.SAPEm setting. When the RPFn input is in YCbCr format, the color keying module does not compare the Cb component, and the setting of these bits is ignored.</li> <li>In transparent color-luma threshold mode for color keying The color keying module does not refer this bit field, and the setting of these bits is ignored.</li> <li>In color replacement mode for color keying Specify the B component value to be compared with the input data in the color replacement function of the color keying module. A value from 0 to 255 can be specified.</li> </ul>

Note: \* When comparison data is specified in an RGB format, if a packed format is selected for RGB input and each of the RGB components is not eight bits, the lower-order bits of input data are extended as specified through VI6\_RPFn\_INFMT.CEXT before comparison. The RGB components to be compared with the input should also be extended in the same way and the extended values should be specified in this register.

### 28.2.7.13 RPFn Source Picture Memory Stride Setting Registers (VI6\_RPFn\_SRCM\_PSTRIDE)

Note: See Table 28.15 for details on which RZ/G series products have which registers.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√



Bit	Bit Name	Initial Value	R/W	Description
31 to 16	PICT_STRD_Y [15:0]	H'0000	R/W	<p>Memory Stride of Source Picture Y/RGB Plane</p> <p>These bits specify in 1-byte units the memory stride of the source picture Y/RGB plane read by the RPFn.</p> <p>A value from 0 to 65,535 can be specified. Refer to Figure 28.26 for settings.</p>
15 to 0	PICT_STRD_C [15:0]	H'0000	R/W	<p>Memory Stride of Source Picture C Plane</p> <p>These bits specify in 1-byte units the memory stride of the source picture C plane read by the RPFn. When an RGB-format picture is read, these bits do not need to be set.</p> <p>A value from 0 to 65,535 can be specified. Refer to Figure 28.26 for settings.</p> <p>In the YCbCr planar format, this setting is used as the memory stride of the Cb and Cr planes.</p>

This register specifies the memory stride of the picture planes in the source area as shown in Figure 28.26. The memory stride of the  $\alpha$  plane should be specified through VI6\_RPFn\_SRCM\_ASTRIDE.ALPH\_STRD. When the RPF input is in an RGB format, only the RGB plane is read; when the input is in YCbCr format, the Y and C planes are read as shown in Figure 28.26. When the  $\alpha$  plane is used, the  $\alpha$  plane is also read. According to the image format and the necessity of the  $\alpha$  plane, specify the necessary addresses where the source image is stored (VI6\_RPFn\_SRCM\_ADDR\_Y, VI6\_RPFn\_SRCM\_ADDR\_C, and VI6\_RPFn\_SRCM\_ADDR\_AI).

Whether the  $\alpha$  plane needs to be read is determined according to the  $\alpha$  plane selection method and IROP operation type. For details, refer to section 28.2.7.6.

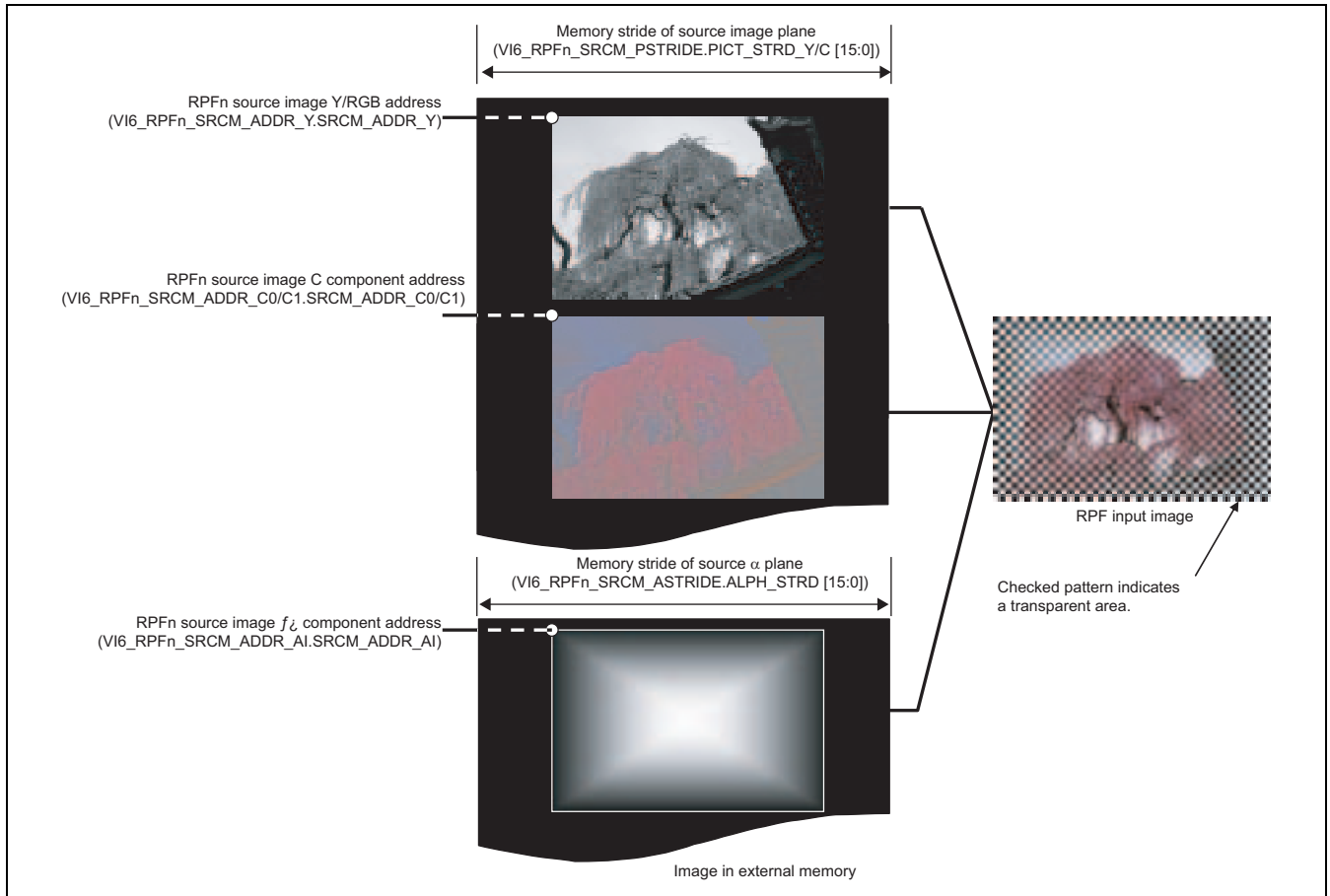


Figure 28.26 Reading an Image from RPFn Source Area

### 28.2.7.14 RPFn Source $\alpha$ Memory Stride Setting Registers (VI6\_RPFn\_SRCM\_ASTRIDE)

Note: See Table 28.15 for details on which RZ/G series products have which registers.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ALPH_STRD [15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

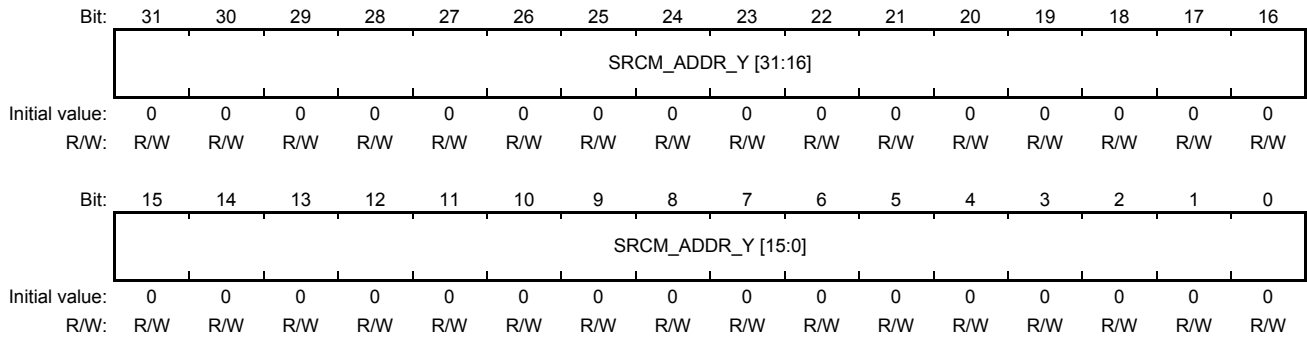
Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 0	ALPH_STRD [15:0]	H'0000	R/W	Memory Stride of Source $\alpha$ Plane These bits specify in 1-byte units the memory stride of the source $\alpha$ plane read by the RPFn. A value from 0 to 65,535 can be specified. Refer to Figure 28.26 for settings.



### 28.2.7.15 RPFn Source Y/RGB Address Registers (VI6\_RPFn\_SRCM\_ADDR\_Y)

Note: See Table 28.15 for details on which RZ/G series products have which registers.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

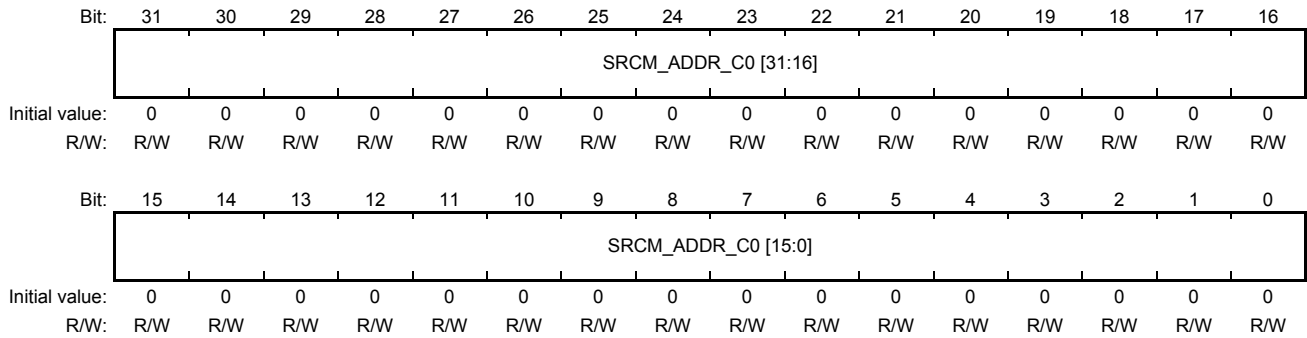


Bit	Bit Name	Initial Value	R/W	Description
31 to 0	SRCM_ADDR_Y [31:0]	H'0000 0000	R/W	<p>Source Image Y/RGB Plane Storing Address</p> <p>These bits specify in 1-byte units the start address of the source image Y plane and packed RGB plane read by the RPFn.</p> <p>A value from H'00000000 to H'FFFFFFFF can be specified. Refer to Figure 28.26 in section 28.2.7.13 for settings.</p>

### 28.2.7.16 RPFn Source Chroma Address Registers 0 (VI6\_RPFn\_SRCM\_ADDR\_C0)

Note: See Table 28.15 for details on which RZ/G series products have which registers.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

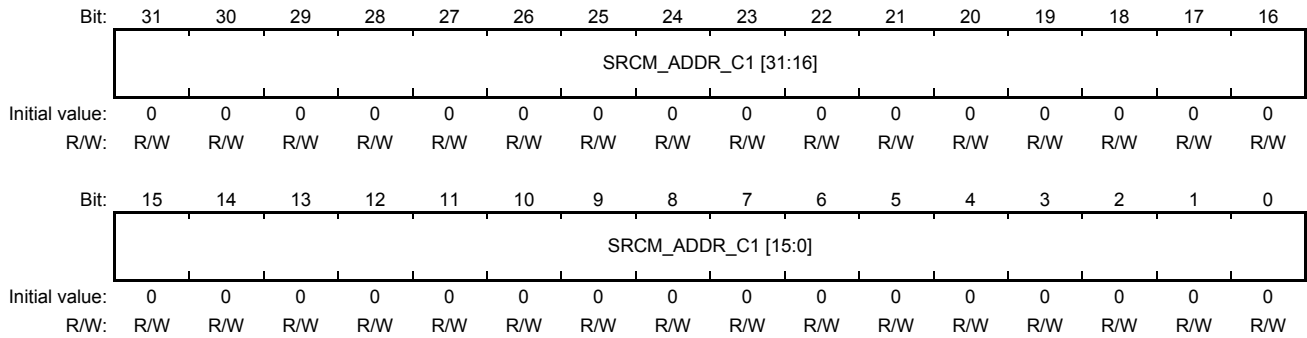


Bit	Bit Name	Initial Value	R/W	Description
31 to 0	SRCM_ADDR_C0 [31:0]	H'0000 0000	R/W	<p>Source Image C Plane Storing Address 0</p> <p>These bits specify in 1-byte units the start address of the source image C plane read by the RPFn. Here, the C plane indicates the combined CbCr plane when a semi-planar format is selected from the packed YCbCr formats shown in Table 28.19 or the Cb plane when a planar format is selected. When an interleaved format is selected or the RPF input is in an RGB format, this setting is not used.</p> <p>A value from H'00000000 to H'FFFFFFFF can be specified. Refer to Figure 28.26 in section 28.2.7.13 for settings.</p>

### 28.2.7.17 RPFn Source Chroma Address Registers 1 (VI6\_RPFn\_SRCM\_ADDR\_C1)

Note: See Table 28.15 for details on which RZ/G series products have which registers.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

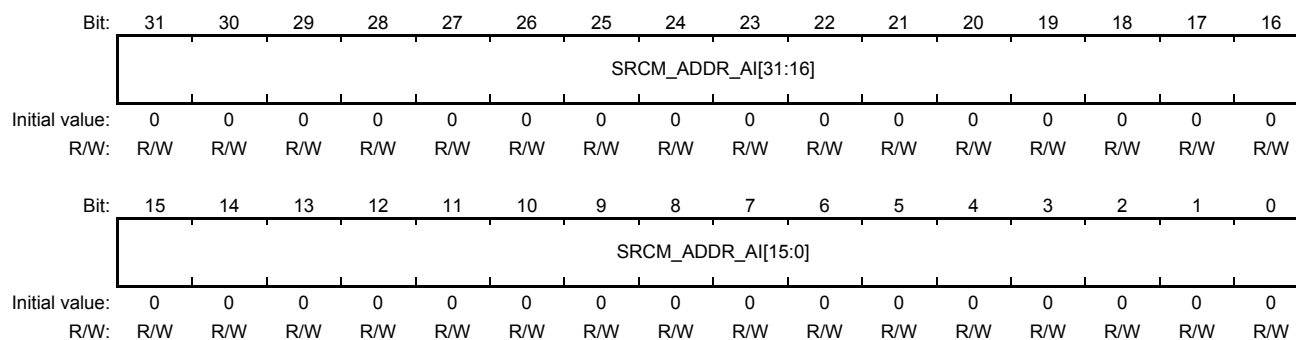


Bit	Bit Name	Initial Value	R/W	Description
31 to 0	SRCM_ADDR_C1 [31:0]	H'0000 0000	R/W	<p>Source Image C Plane Storing Address 1</p> <p>These bits specify in 1-byte units the start address of the Cr plane when a planar YCbCr format shown in Table 28.19 is read by the RPFn.</p> <p>This setting is not used when the RPF input is in YCbCr format that is not a planar format or in an RGB format.</p> <p>A value from H'00000000 to H'FFFFFFFF can be specified. Refer to Figure 28.26 in section 28.2.7.13 for settings.</p>

### 28.2.7.18 RPFn Source $\alpha$ Address Registers (VI6\_RPFn\_SRCM\_ADDR\_AI)

Note: See Table 28.15 for details on which RZ/G series products have which registers.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	SRCM_ADDR_AI [31:0]	H'0000 0000	R/W	<p>Source Image <math>\alpha</math> Plane Storing Address</p> <p>These bits specify in 1-byte units the start address of the <math>\alpha</math> plane of the source image read by the RPFn. Specify in the same way as the start address of the picture plane. When the <math>\alpha</math> plane is not read from the source area, these bits do not need to be set.</p> <p>A value from H'00000000 to H'FFFFFFFF can be specified. Refer to Figure 28.26 in section 28.2.7.13 for settings.</p>

## 28.2.8 WPF Control Registers

### 28.2.8.1 WPFn-Source-RPF Registers (VI6\_WPFn\_SRCRPF)

Note: See Table 28.15 for details on which RZ/G series products have which registers.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	VIR_ACT [1:0]		—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	RPF4_ACT [1:0]		RPF3_ACT [1:0]		RPF2_ACT [1:0]		RPF1_ACT [1:0]		RPF0_ACT [1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31, 30	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
29, 28	VIR_ACT [1:0]	00	R/W	Virtual RPF Start Enable in BRU These bits enable start of the virtual RPF in the BRU as the source RPF for the WPFn when the WPFn is started. For details of the virtual RPF, refer to the following. Section 28.2.16.1, BRU Input Control Register (VI6_BRU_INCTRL) Section 28.2.16.2, Size Register of BRU Input Virtual RPF (VI6_BRU_VIRRRPF_SIZE) Section 28.2.16.3, Display Location Register of BRU Input Virtual RPF (VI6_BRU_VIRRRPF_LOC) Section 28.2.16.4, Color Information Register of BRU Input Virtual RPF (VI6_BRU_VIRRRPF_COL) Note that the virtual RPF is in the BRU as shown in Figure 28.44 and there are no register bits for DPR setting related to the virtual RPF. 00: The virtual RPF in the BRU is not started. 01: The virtual RPF in the BRU is started as a sub layer source RPF for the WPFn. 10: The virtual RPF in the BRU is started as the master-layer source RPF for the WPFn. 11: Setting prohibited
27 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
9, 8	RPF4_ACT [1:0]	00	R/W	RPFn Start Enable (RPFn_ACT, n = 0 to 4)
7, 6	RPF3_ACT [1:0]	00	R/W	These bits enable start of RPFn as the source RPF for the WPFn when the WPFn is started. When RPFn is not started by any of the WPF0 to WPF3, set the VI6_DPR_RPFn_ROUTE.RT_RPFn bits to 63 (H'3F).
5, 4	RPF2_ACT [1:0]	00	R/W	00: RPFn is not started.
3, 2	RPF1_ACT [1:0]	00	R/W	01: RPFn is started as a sub layer source RPF for the WPFn. 10: RPFn is started as the master-layer source RPF for the WPFn.
1, 0	RPF0_ACT [1:0]	00	R/W	11: Setting prohibited

When the WPFn is started through the VSP1 start register n (VI6\_CMDn: n = 0, 1, 2, 3), the RPF and virtual RPF in the BRU specified as the source RPF in this register are also started to supply data to the VSP1 internal modules.

Note the following when specifying the source RPF.

- Each source RPF can be assigned to only one target WPFn; a single RPF cannot be assigned as the source RPF for multiple WPFs. For example, when setting VI6\_WPF0\_SRCRPF to H'00000008 and VI6\_WPF1\_SRCRPF to H'00000004 is attempted, the VSP1 will not operate correctly (these settings are prohibited) because RPF1 is assigned as both the master-layer source RPF for WPF0 and a sub layer source RPF for WPF1.
- When blending or ROP operation is applied to multiple images through the BRU, multiple source RPFs are necessary for one WPF. When multiple source RPFs are used, images should be classified into a master layer and sub layers; assign one of the source RPFs as the master-layer source RPF and other RPFs as sub layer source RPFs. Do not assign all RPFs as sub layer source RPFs (VI6\_WPF1\_SRCRPF = H'00000015) or two or more RPFs as the master-layer source RPF (VI6\_WPF3\_SRCRPF = H'0000025A) (such settings are prohibited).
- When the BRU is not used, there should be only one source RPF for one WPF. In this case, the source RPF should be assigned as the master-layer source RPF.
- Calculate the master layer and sub layer sizes as described in section 28.1.5. When the BRU is used and the SRU or UDS is used between the RPF and BRU, the master layer and sub layer sizes may have been upscaled or downscaled before input to the BRU with respect to the sizes output from the source RPF. When determining the relative locations among layers for blending or ROP operation, take account of the size of each image input to the BRU. In particular, be careful not to place the entire sub layer outside the master layer as explained in the description of the HCOORD and VCOORD bits in VI6\_RPFn\_LOC in section 28.2.7.5.

### 28.2.8.2 WPFn Horizontal Input Size Clipping Registers (VI6\_WPFn\_HSZCLIP)

Note: See Table 28.15 for details on which RZ/G series products have which registers.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	HCEN	—	—	—	—	HCL_OFST [7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	HCL_SIZE [11:0]											
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28	HCEN	0	R/W	Horizontal Size Clipping Enable/Disable Enables or disables clipping of the horizontal size of the WPFn input image. 0: Horizontal size clipping is disabled 1: Horizontal size clipping is enabled
27 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 16	HCL_OFST [7:0]	H'00	R/W	Horizontal Size Clipping Offset Value Setting These bits specify the offset size (pixels) from the left end of the image in horizontal size clipping when the HCEN bit is 1 (Figure 28.27). The left side of the image input to the WPF is cut off for the size specified in these bits. When the HCEN bit is 0, this setting is ignored. A value from 0 to 255 can be specified. (HCL_OFST + HCL_SIZE) should not exceed the horizontal size of the WPF input. If the setting shown in the bottom example in Figure 28.27 is made, VSP1 does not operate correctly.
15 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
11 to 0	HCL_SIZE [11:0]	H'000	R/W	<p>Horizontal Clipping Size Setting</p> <p>When the HCEN bit is 1, these bits specify the clipping size for horizontal clipping processing. Through this processing, the area of the horizontal size specified through the HCL_SIZE bits starting from the offset position specified through the HCL_OFST bits is determined as the valid image area. Accordingly, the right-side pixels beyond the (HCL_OFST + HCL_SIZE) size in the WPFn input image are discarded. When the HCEN bit is 0, this setting is ignored.</p> <p>A value from 1 to 2,048 can be specified. (HCL_OFST + HCL_SIZE) should not exceed the horizontal size of the WPF input. If the setting shown in the bottom example in Figure 28.27 is made, VSP1 does not operate correctly.</p> <p>Note: When the WPFn output format is YCbCr4:2:2 or YCbCr4:2:0, specify an even value in these bits.</p>

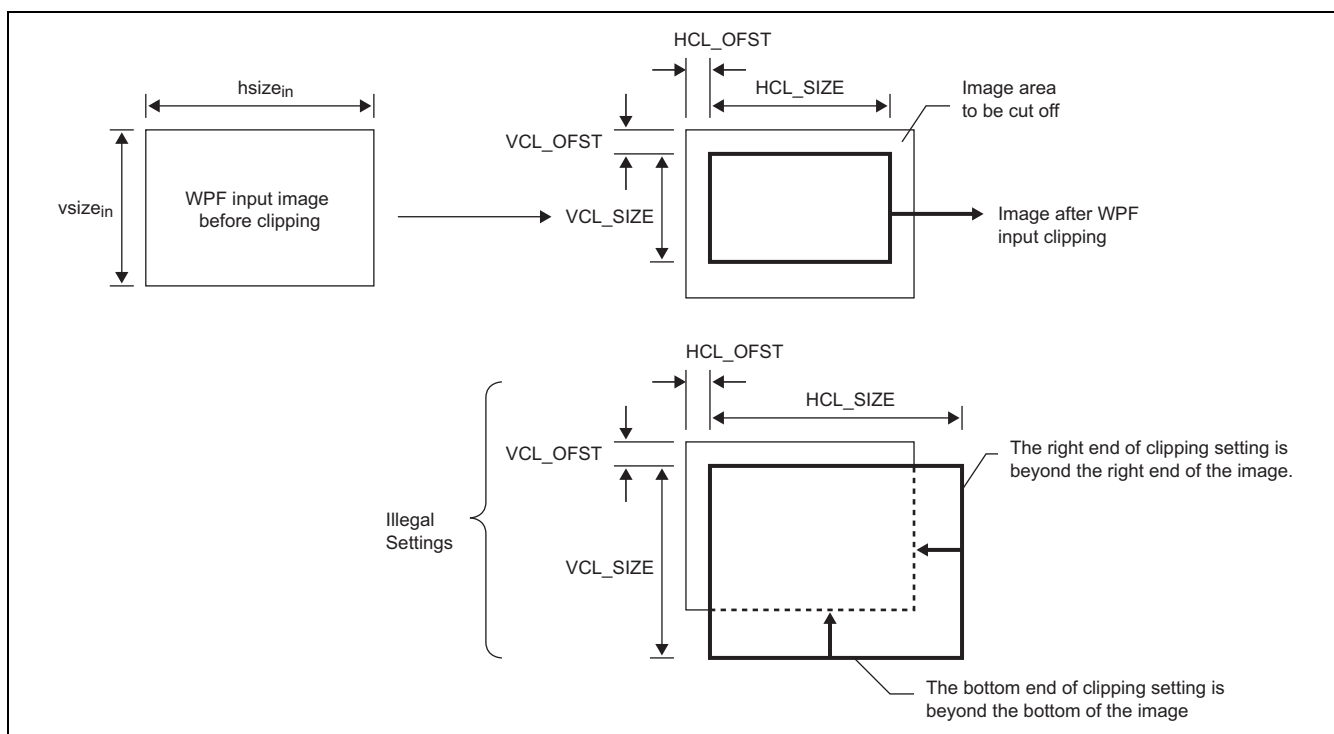


Figure 28.27 Image Clipping in WPF Input Section



### 28.2.8.3 WPFn Vertical Input Size Clipping Registers (VI6\_WPFn\_VSZCLIP)

Note: See Table 28.15 for details on which RZ/G series products have which registers.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	VCEN	—	—	—	—	VCL_OFST [7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	VCL_SIZE [11:0]											
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28	VCEN	0	R/W	Vertical Size Clipping Enable/Disable Enables or disables clipping of the vertical size of the WPFn input image. 0: Vertical size clipping is disabled 1: Vertical size clipping is enabled
27 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 16	VCL_OFST [7:0]	H'00	R/W	Vertical Size Clipping Offset Value Setting These bits specify the offset size (pixels) from the top end of the image in vertical size clipping when the VCEN bit is 1 (Figure 28.27). The top of the image input to the WPF is cut off for the size specified in these bits. When the VCEN bit is 0, this setting is ignored. A value from 0 to 255 can be specified. (VCL_OFST + VCL_SIZE) should not exceed the vertical size of the WPF input. If the setting shown in the bottom example in Figure 28.27 is made, VSP1 does not operate correctly.
15 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

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Bit	Bit Name	Initial Value	R/W	Description
11 to 0	VCL_SIZE [11:0]	H'000	R/W	<p>Vertical Clipping Size Setting</p> <p>When the VCEN bit is 1, these bits specify the clipping size for vertical clipping processing. Through this processing, the area of the vertical size specified through the VCL_SIZE bits starting from the offset position specified through the VCL_OFST bits is determined as the valid image area. Accordingly, the bottom pixels beyond the (VCL_OFST + VCL_SIZE) size in the WPFn input image are discarded. When the VCEN bit is 0, this setting is ignored.</p> <p>A value from 1 to 2,048 can be specified. (VCL_OFST + VCL_SIZE) should not exceed the vertical size of the WPF input. If the setting shown in the bottom example in Figure 28.27 is made, VSP1 does not operate correctly.</p> <p>Note: When the WPFn output format is YCbCr4:2:0, specify an even value in these bits.</p>

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### 28.2.8.4 WPFn Output Format Registers (VI6\_WPFn\_OUTFMT)

Note: See Table 28.15 for details on which RZ/G series products have which registers.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PDV [7:0]								PXA	—	—	—	—	—	—	FLP
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SPYCS	SPUVS	DITH [1:0]		WRM [2:0]		CSC	—	WRFMT [6:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	PDV [7:0]	H'00	R/W	<p>PAD Value in Output Packed Data</p> <p>These bits specify the value to be stored in the bit field indicated as PAD or P in the output formats shown in Table 28.24. To store this value in PAD, specify 0 in the PXA bit. A value from 0 to 255 can be specified.</p>
23	PXA	0	R/W	<p>PAD Data Select</p> <p>Selects the value to be stored in the bit field indicated as PAD or P in the packed RGB output formats shown in Table 28.24. Both the value specified in the PDV bits and the <math>\alpha</math> data input from the DPR to WPF are eight bits, but some of the PAD and P bit fields shown in Table 28.24 are four bits or one bit. When the target bit field is not eight bits, the number of bits in the PDV value and the <math>\alpha</math> data input from the DPR to WPF is reduced according to the VI6_WPFn_RNDCTRL.ABRM setting. For bit count reduction, refer to Figure 28.28 and the description of VI6_WPFn_RNDCTRL.ABRM.</p> <p>0: The value specified in the PDV bits is stored in the PAD shown in Table 28.24.</p> <p>1: The <math>\alpha</math> value output from DPR in pixel units is stored in the PAD shown in Table 28.24.</p>
22 to 17	—	All 0	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>

Bit	Bit Name	Initial Value	R/W	Description
16	FLP	0	R/W	<p>Vertical flipping Select</p> <p>This bit selects the vertical flipping processing to be applied to the WPFn output image. Figure 28.29 shows the correspondence between the original image and the vertical flipping result according to this setting.</p> <p>0: No vertical flipping 1: vertical flipping</p> <p><u>Flipping can be specified only in WPF0. In other channels, always specify 0 in these bits.</u></p> <p>Note that the destination address setting should be changed according to the setting of these bits. For details, refer to section 28.2.8.9.</p> <p>When the LIF module is used (VI6_LIF_CTRL.LIF_EN = 1), set 0 to FLP.</p>
15	SPYCS	0	R/W	<p>WPF Output Mode Setting 1</p> <p>When the output format is YUY2, set this bit to 1 and set the WRFMT bits to 71 (H'47).</p> <p>When the output format is YVYU, set this bit and the SPUVS bit to 1 and set the WRFMT bits to 71 (H'47).</p> <p>In other cases, set this bit to 0.</p>
14	SPUVS	0	R/W	<p>WPF Output Mode Setting 2</p> <p>When the output format is NV61, set this bit to 1 and set the WRFMT bits to 65 (H'41).</p> <p>When the output format is NV21, set this bit to 1 and set the WRFMT bits to 66 (H'42).</p> <p>When the output format is YVYU, set this bit and the SPYCS bit to 1 and set the WRFMT bits to 71 (H'47).</p> <p>In other cases, set this bit to 0.</p>
13, 12	DITH[1:0]	00	R/W	<p>Dithering Enable/Disable</p> <p>When the output format specified through the WRFMT bits is RGB with 18 bpp (262,144 colors) or less, the color reduction processing is applied to match the number of colors. The color reduction processing may generate the artifacts of pseudo gradation, which can be suppressed through dithering. The DITH bits enable or disable dithering during color reduction.</p> <p>When the output format specified through the WRFMT bits is YCbCr, specify 0 in these bits.</p> <p>And when VI6_WPFn_OUTFMT.CSC is set to 1, specify 0 in these bits even in the case that the output format specified through the WRFMT bits is RGB.</p> <p>00: Dithering is disabled 11: Dithering is enabled 01, 10: Setting prohibited</p>

Bit	Bit Name	Initial Value	R/W	Description
11 to 9	WRTM[2:0]	000	R/W	<p>CSC Conversion Expression Setting</p> <p>These bits select the expression for color space conversion. The conversion direction is RGB to YCbCr when the format specified in the WRFMT bits is RGB, or YCbCr to RGB when the format is YCbCr.</p> <p>000: BT.601 YCbCr [16,235/240] ↔ RGB [0,255]            001: BT.601 YCbCr [0,255] ↔ RGB [0,255]            010: BT.709 YCbCr [16,235/240] ↔ RGB [0,255]            011: BT.709 YCbCr [16,235/240] ↔ RGB [16,235]            100 to 111: Setting prohibited</p>
8	CSC	0	R/W	<p>Color Space Conversion Setting</p> <p>Enables or disables YCbCr ↔ RGB color space conversion to be executed in the WPFn. The characteristics of color space conversion are determined by the WRTM setting.</p> <p>There are some points to be noted about the relationship between the CSC setting and output format (WRFMT). For details refer to section 28.2.7.3, RPFn Input Format Registers (VI6_RPFn_INFMT).</p> <p>0: Color space is not converted.            1: Color space is converted.</p>
7	—	0	R	<p>Reserved</p> <p>This bit is always read as 0. The write value should always be 0.</p>
6 to 0	WRFMT[6:0]	H'00	R/W	<p>WPF Output Image Format Setting</p> <p>These bits select the format of the image output from the WPFn to the external memory from among those listed in Tables 28.24 and 28.25.</p> <p>Notes:</p> <ol style="list-style-type: none"> <li>Number of output pixels           <p>When YCbCr4:2:2 is specified through WRFMT, the horizontal size of the output image should be a multiple of 2 pixels. When YCbCr4:2:0 is specified, the vertical and horizontal sizes of the output image should be multiples of 2 pixels. Specify an appropriate data flow of the source RPF → DPR → target WPF so that the size of the image input to the target WPF satisfies the above restrictions. In particular, when the data flow includes a module or a function that modifies (upscales, downscales, or clips) the image size, take special care about the module or function settings.</p> </li> <li>Output lines in YCbCr4:2:0           <p>In the YCbCr4:2:0 output format, the number of chrominance lines in the vertical direction is one-half the number of luminance lines. For this reason, the WPF outputs only even-numbered chrominance lines (lines 0, 2, 4, 6, ...) (conversion from (A) to (B) in Figure 28.30). When vertical flipping is also specified through the FLP bits, the flipping processing is executed last and the chrominance line locations are inverted (lines 1, 3, 5, 7, ...) in the output image ((C) in Figure 28.30).</p> </li> </ol>

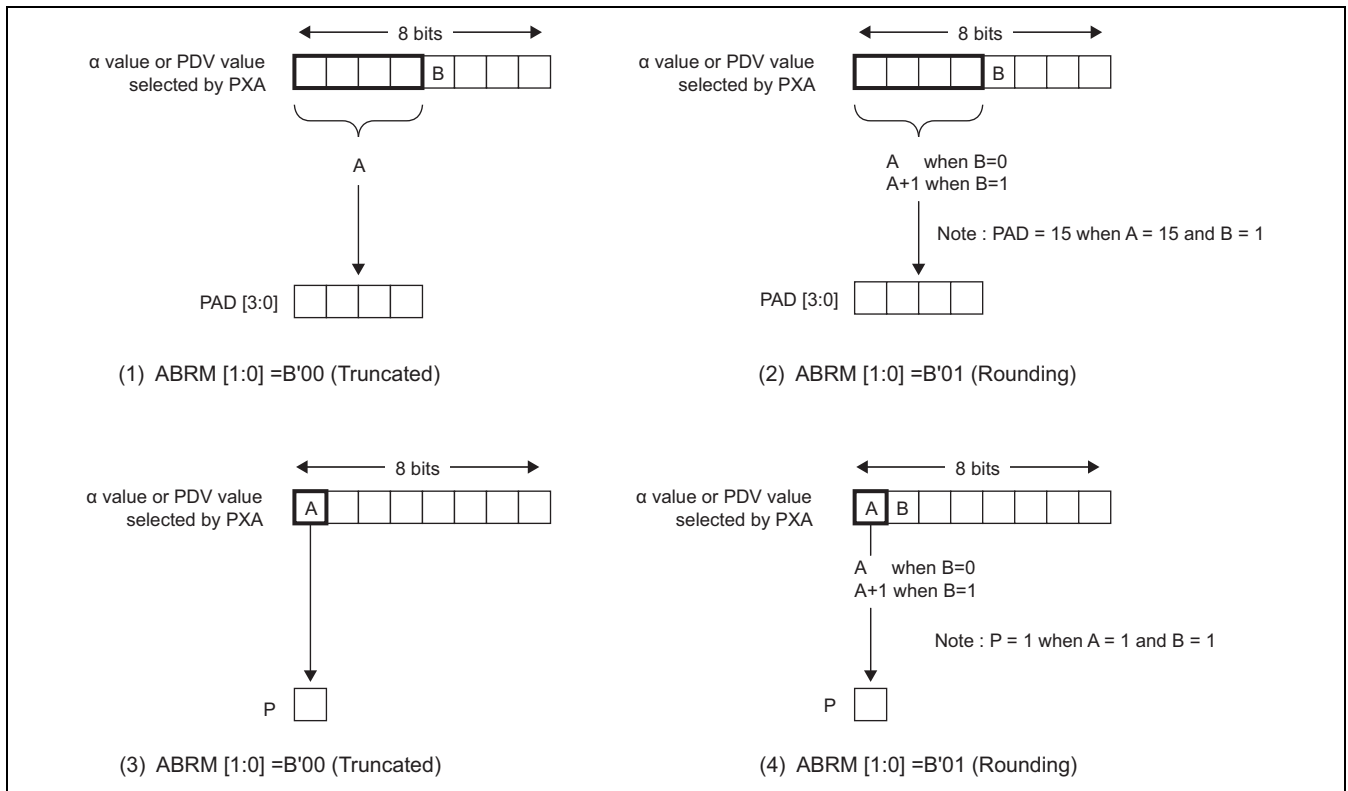


Figure 28.28 Selection of PAD Value and Reduction of Bit Count through PXA Setting

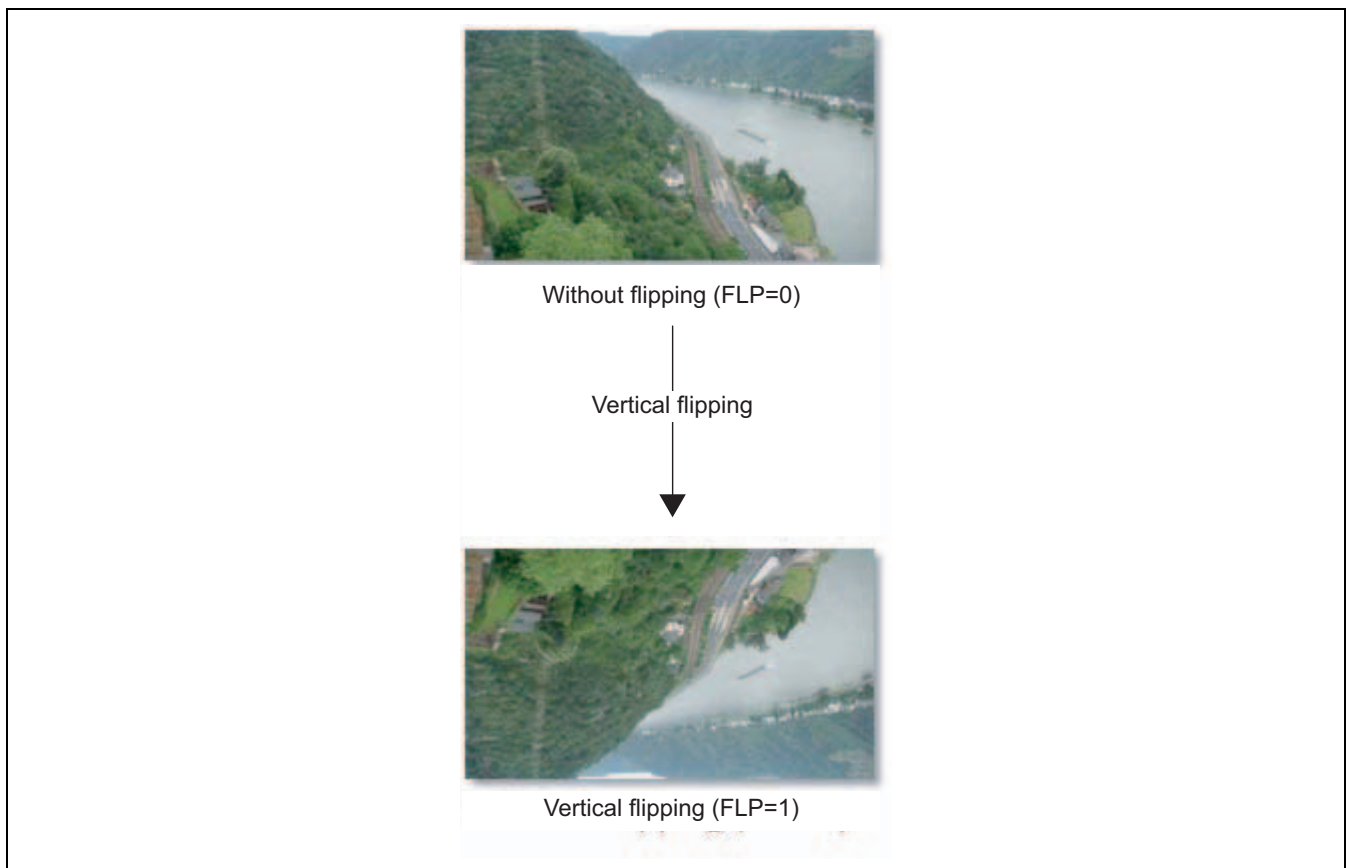
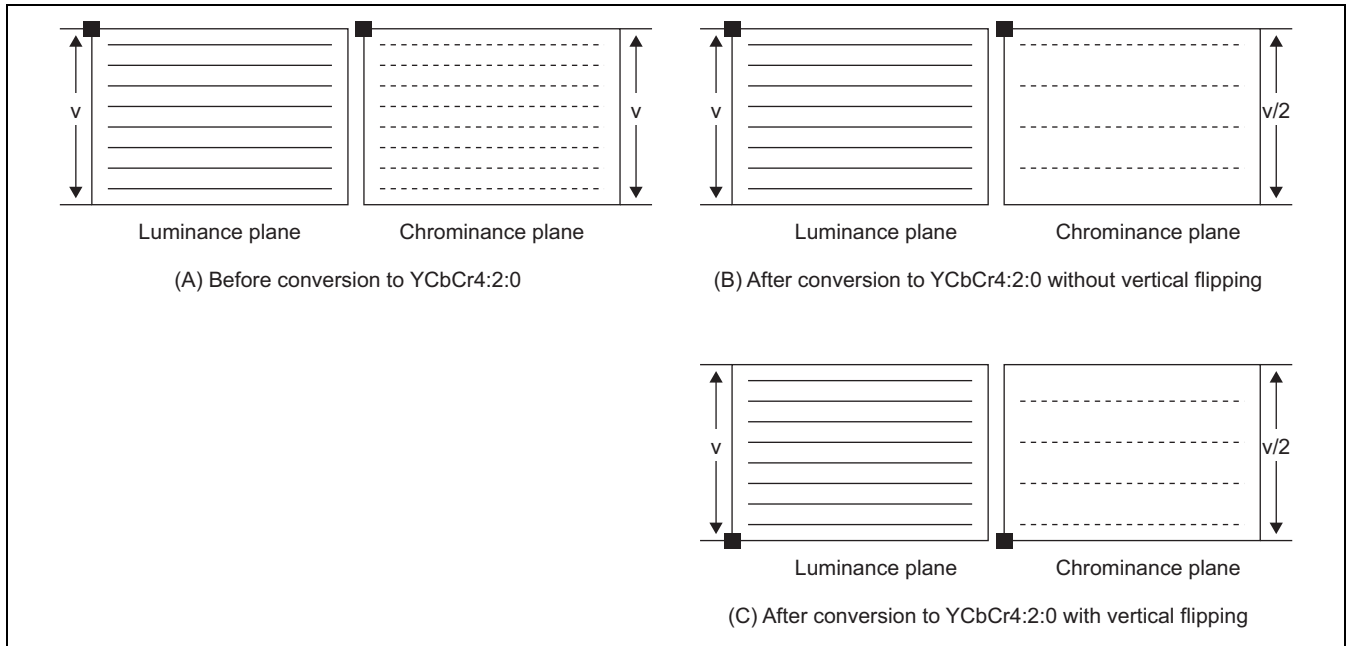


Figure 28.29 Correspondence between Original Image and Vertical Flipping Result according to FLP Setting



**Figure 28.30 Chrominance Output Lines in YCbCr4:2:0 and Vertical Flipping Result**

**Table 28.24 Packed RGB Formats for WPF Output**

WRFMT	Bit per pixel	Phase	Bit field																																			
			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
H'00	8	—	R0	R0	R0	G0	G0	G0	B0	B0	R1	R1	R1	G1	G1	G1	B1	B1	R2	R2	R2	G2	G2	G2	B2	B2	R3	R3	R3	G3	G3	G3	B3	B3				
H'01	12	—	0	0	0	0	R0	R0	R0	R0	G0	G0	G0	G0	B0	B0	B0	B0	0	0	0	0	R1	R1	R1	R1	G1	G1	G1	G1	B1	B1	B1	B1				
H'02		—	R0	R0	R0	R0	G0	G0	G0	G0	B0	B0	B0	B0	0	0	0	0	R1	R1	R1	R1	G1	G1	G1	G1	B1	B1	B1	B1	0	0	0	0				
H'03	—	—	Reserved								Reserved								Reserved								Reserved											
H'04	15	—	0	R0	R0	R0	R0	R0	G0	G0	G0	G0	B0	B0	B0	B0	B0	0	R1	R1	R1	R1	R1	G1	G1	G1	G1	G1	G1	B1	B1	B1	B1					
H'05		—	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	0	R1	R1	R1	R1	R1	G1	G1	G1	G1	G1	B1	B1	B1	B1	B1	0				
H'06	16	—	R0	R0	R0	R0	R0	G0	G0	G0	G0	B0	B0	B0	B0	B0	B0	R1	R1	R1	R1	R1	G1	G1	G1	G1	G1	G1	B1	B1	B1	B1						
H'07	18	—	PAD0								0	0	0	0	0	0	R0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0						
H'08		—	R0	R0	R0	R0	R0	R0	G0	G0	G0	G0	B0	B0	B0	B0	B0	0	0	0	0	0	0	0	0	0	PAD0											
H'09		—	0	0	0	0	0	0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	B0	B0	PAD0											
H'0A		—	PAD0								R0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	B0	B0	B0	0	0	0	0	0	0		
H'0B		—	PAD0								0	0	R0	R0	R0	R0	R0	R0	0	0	G0	G0	G0	G0	G0	G0	0	0	B0	B0	B0	B0	B0	B0				
H'0C		—	0	0	R0	R0	R0	R0	R0	0	0	G0	G0	G0	G0	G0	G0	0	0	B0	B0	B0	B0	B0	B0	B0	PAD0											
H'0D		—	PAD0								R0	R0	R0	R0	R0	R0	0	0	G0	G0	G0	G0	G0	G0	0	0	B0	B0	B0	B0	B0	B0	0	0	B0	B0	B0	B0
H'0E		—	R0	R0	R0	R0	R0	0	0	G0	G0	G0	G0	G0	G0	0	0	B0	B0	B0	B0	B0	B0	B0	B0	0	0	PAD0										
H'0F		0	0	0	0	0	0	0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	B0	0	0	0	0	0	0	R1	R1				
		1	R1	R1	R1	R1	G1	G1	G1	G1	G1	G1	B1	B1	B1	B1	B1	B1	0	0	0	0	0	0	0	R2	R2	R2	R2	R2	R2	G2	G2	G2	G2			
		2	G2	G2	B2	B2	B2	B2	B2	B2	0	0	0	0	0	0	0	R3	R3	R3	R3	R3	R3	G3	G3	G3	G3	G3	G3	B3	B3	B3	B3	B3	B3			
H'10		0	R0	R0	R0	R0	R0	R0	G0	G0	G0	G0	B0	B0	B0	B0	B0	0	0	0	0	0	0	0	0	0	R1	R1	R1	R1	R1	R1	G1	G1				
		1	G1	G1	G1	G1	B1	B1	B1	B1	B1	B1	0	0	0	0	0	0	R2	R2	R2	R2	R2	R2	G2	G2	G2	G2	G2	G2	B2	B2	B2	B2				
		2	B2	B2	0	0	0	0	0	0	0	0	R3	R3	R3	R3	R3	R3	G3	G3	G3	G3	G3	G3	B3	B3	B3	B3	B3	B3	0	0	0	0				
H'11	0	0	0	R0	R0	R0	R0	R0	0	0	G0	G0	G0	G0	G0	G0	0	0	B0	B0	B0	B0	B0	B0	0	0	R1	R1	R1	R1	R1	R1						
	1	0	0	G1	G1	G1	G1	G1	0	0	B1	B1	B1	B1	B1	B1	0	0	R2	R2	R2	R2	R2	R2	0	0	G2	G2	G2	G2	G2	G2						
	2	0	0	B2	B2	B2	B2	B2	0	0	R3	R3	R3	R3	R3	R3	0	0	G3	G3	G3	G3	G3	G3	0	0	B3	B3	B3	B3	B3	B3						
H'12	0	R0	R0	R0	R0	R0	R0	0	0	G0	G0	G0	G0	G0	0	0	B0	B0	B0	B0	B0	B0	0	0	R1	R1	R1	R1	R1	R1	0	0						
	1	G1	G1	G1	G1	G1	0	0	B1	B1	B1	B1	B1	0	0	R2	R2	R2	R2	R2	R2	0	0	G2	G2	G2	G2	G2	G2	0	0							
	2	B2	B2	B2	B2	B2	0	0	R3	R3	R3	R3	R3	0	0	G3	G3	G3	G3	G3	G3	0	0	B3	B3	B3	B3	B3	B3	0	0							
H'13	—	PAD0								R0	R0	R0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	B0								
H'14	24	—	R0	R0	R0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	B0	B0	B0	PAD0											
H'15		0	R0	R0	R0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	B0	B0	B0	R1	R1	R1	R1	R1	R1	R1	R1				
		1	G1	G1	G1	G1	G1	G1	G1	G1	B1	B1	B1	B1	B1	B1	B1	B1	R2	R2	R2	R2	R2	R2	R2	R2	G2	G2	G2	G2	G2	G2	G2	G2				
		2	B2	B2	B2	B2	B2	B2	B2	B2	R3	R3	R3	R3	R3	R3	R3	R3	G3	G3	G3	G3	G3	G3	G3	G3	B3	B3	B3	B3	B3	B3	B3	B3				
H'16	18	—	0	0	0	0	0	0	0	R0	R0	R0	R0	R0	G0	G0	G0	0	0	0	0	0	0	0	G0	G0	G0	B0	B0	B0	B0							
H'17		—	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	B0	B0	B0	B0							
H'18	24	0	B0	B0	B0	B0	B0	B0	B0	G0	G0	G0	G0	G0	G0	G0	G0	R0	R0	R0	R0	R0	R0	R0	R0	B1	B1	B1	B1	B1	B1	B1	B1					
		1	G1	G1	G1	G1	G1	G1	G1	R1	R1	R1	R1	R1	R1	R1	R1	B2	B2	B2	B2	B2	B2	B2	B2	G2	G2	G2	G2	G2	G2	G2	G2					
		2	R2	R2	R2	R2	R2	R2	R2	R2	B3	B3	B3	B3	B3	B3	B3	B3	G3	G3	G3	G3	G3	G3	G3	R3	R3	R3	R3	R3	R3	R3	R3					
H'19	12	—	PAD0								R0	R0	R0	R0	G0	G0	G0	G0	B0	B0	B0	PAD1					R1	R1	R1	R1	G1	G1	G1	G1	B1	B1	B1	B1
H'1A		—	R0	R0	R0	R0	G0	G0	G0	G0	B0	B0	B0	B0	PAD0				R1	R1	R1	R1	G1	G1	G1	G1	B1	B1	B1	B1	PAD1							
H'1B	15	—	P0	R0	R0	R0	R0	R0	G0	G0	G0	G0	B0	B0	B0	B0	B0	A0	R1	R1	R1	R1	R1	R1	G1	G1	G1	G1	G1	B1	B1	B1	B1					
H'1C		—	R0	R0	R0	R0	R0	G0	G0	G0	G0	B0	B0	B0	B0	B0	A0	R1	R1	R1	R1	R1	R1	G1	G1	G1	G1	G1	B1	B1	B1	B1						
H'1D		—	PAD0								B0	B0	B0	B0	G0	G0	G0	G0	R0	R0	R0	R0	PAD1					B1	B1	B1	B1	G1	G1	G1	G1	R1	R1	R1
H'1E	15	—	B0	B0	B0	B0	G0	G0	G0	G0	R0	R0	R0	R0	PAD0				B1	B1	B1	B1	G1	G1	G1	G1	R1	R1	R1	R1	PAD1							
H'1F		—	A0	B0	B0	B0	B0	G0	G0	G0	G0	R0	R0	R0	R0	R0	P0	B1	B1	B1	B1	B1	B1	G1	G1	G1	G1	G1	G1	R1	R1	R1	R1					
H'20		—	B0	B0	B0	B0	B0	G0	G0	G0	G0	R0	R0	R0	R0	R0	P0	B1	B1	B1	B1	B1	B1	G1	G1	G1	G1	G1	R1	R1	R1	R1						
H'21	18	0	0	0	B0	B0	B0	B0	B0	0	0	G0	G0	G0	G0	G0	0	0	R0	R0	R0	R0	R0	R0	0	0	B1	B1	B1	B1	B1	B1						
		1	0	0	G1	G1	G1	G1	G1	0	0	R1	R1	R1	R1	R1	R1	0	0	B2	B2	B2	B2	B2	B2	0	0	G2	G2	G2	G2	G2	G2					
		2	0	0	R2	R2	R2	R2	R2	0	0	B3	B3	B3	B3	B3	B3	0	0	G3	G3	G3	G3	G3	G3	0	0	R3	R3	R3	R3	R3	R3					
H'22	24	—	PAD0								B0	B0	B0	B0	B0	B0	B0	B0	G0	G0	G0	G0	G0	G0	G0	R0	R0	R0	R0	R0	R0	R0	R0					
H'23	16	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	B0	B0	B0	B0							
H'24~H'3F	—	—	Reserved								Reserved								Reserved								Reserved											



**Table 28.25 Packed YCbCr Formats for WPF Output**

WRFMT [6:0]	Packed YCbCr Output Format	Reference
H'40	YCbCr4:4:4 semi-planar	Figure 28.19
H'41	YCbCr4:2:2 semi-planar (NV16, NV61* <sup>1</sup> )	
H'42	YCbCr4:2:0 semi-planar (NV12, NV21* <sup>1</sup> )	
H'43 to H'45	Reserved	—
H'46	YCbCr4:4:4 interleaved	Figure 28.20
H'47	YCbCr4:2:2 interleaved type 0 (UYVY, YUY2* <sup>2</sup> , YVYU* <sup>3</sup> )	
H'48	YCbCr4:2:2 interleaved type 1	
H'49	YCbCr4:2:0 interleaved	
H'4A	YCbCr4:4:4 planar	Figure 28.21
H'4B	YCbCr4:2:2 planar (YV16)	
H'4C	YCbCr4:2:0 planar (YV12, YU12)	
H'4D to H'7F	Reserved	—

Notes: 1. When the output format is NV61 or NV21, set SPUVS (bit 14) to 1.  
 2. When the output format is YUY2, set SPYCS (bit 15) to 1.  
 3. When the output format is YVYU, set SPUVS (bit 14) to 1 and SPYCS (bit 15) to 1.

For details of each YCbCr format, refer to Figures 28.19, 28.20, and 28.21. In these figures, registers for the RPF are indicated; read them as registers for the WPF as follows.

(RPF registers in the figures)	→	(Corresponding WPF registers)
VI6_RPFn_SRCM_ADDR_Y.SRCM_ADDR_Y	→	VI6_WPFn_DSTM_ADDR_Y.DSTM_ADDR_Y
VI6_RPFn_SRCM_ADDR_C0.SRCM_ADDR_C0	→	VI6_WPFn_DSTM_ADDR_C0.DSTM_ADDR_C0
VI6_RPFn_SRCM_ADDR_C1.SRCM_ADDR_C1	→	VI6_WPFn_DSTM_ADDR_C1.DSTM_ADDR_C1

### 28.2.8.5 WPFn Data Swapping Registers (VI6\_WPFn\_DSWAP)

Note: See Table 28.15 for details on which RZ/G series products have which registers.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3	P_LLS	0	R/W	WPF Output Data Swapping in LONG LWORD Units 0: Data swapping in LONG LWORD (64-bit) units is disabled 1: Data swapping in LONG LWORD (64-bit) units is enabled This should be set to 1 in most cases, but when data has been swapped in 64-bit units by another data processing channel, specify 0
2	P_LWS	0	R/W	WPF Output Data Swapping in Longword Units 0: Data swapping in longword (32-bit) units is disabled 1: Data swapping in longword (32-bit) units is enabled This should be set to 1 in most cases, but when data has been swapped in 32-bit units by another data processing channel, specify 0
1	P_WDS	0	R/W	WPF Output Data Swapping in Word Units The effect of this bit setting is the same as data swapping in the RPF; refer to Table 28.21. 0: Data swapping in word (16-bit) units is disabled 1: Data swapping in word (16-bit) units is enabled
0	P_BTS	0	R/W	WPF Output Data Swapping in Byte Units The effect of this bit setting is the same as data swapping in the RPF; refer to Table 28.21. 0: Data swapping in byte (8-bit) units is disabled 1: Data swapping in byte (8-bit) units is enabled

### 28.2.8.6 WPFn Rounding Control Registers (VI6\_WPFn\_RNDCTRL)

Note: See Table 28.15 for details on which RZ/G series products have which registers.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	CBRM	—	—	ABRM [1:0]		ATHRESH [7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	CLMD [1:0]		—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28	CBRM	0	R/W	Bit Count Reduction Method Selection for Data Storage in Packed RGB  This bit specifies the method for reducing the number of bits when data is stored in the bit fields indicated as R, G, and B in Table 28.24 and the target bit fields are not eight bits.  0: Bit count conversion: The lower-order bits are truncated 1: Bit count conversion: Rounding (rounding off)
27, 26	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
25, 24	ABRM[1:0]	00	R/W	Bit Count Reduction Method Selection for Data Storage in PAD  These bits specify the method for reducing the number of bits when the data selected through VI6_WPFn_OUTFMT.PXA is stored in the bit fields indicated as PAD or P in Table 28.24 and the target bit field is four bits or one bit.  A value of B'10 can be specified only when the packed RGB format specified through VI6_WPFn_OUTFMT.WRFMT includes a 1-bit P field. In this case, when the data selected through VI6_WPFn_OUTFMT.PXA is greater than the ATHRESH value, 1 is stored in the P field; when the selected data is not greater than the ATHRESH value, 0 is stored.  00: Bit count conversion: The lower-order bits are truncated 01: Bit count conversion: Rounding (rounding off) 10: Bit count conversion: Comparison with the threshold value (this setting is allowed only when the storage field is one bit) 11: Setting prohibited

Bit	Bit Name	Initial Value	R/W	Description
23 to 16	ATHRESH [7:0]	H'00	R/W	<p>Threshold for Conversion to 1-Bit <math>\alpha</math> Data</p> <p>These bits specify the threshold value used for conversion from 8-bit <math>\alpha</math> data to one bit when the ABRM bits are set to B'10. When the 8-bit <math>\alpha</math> value before bit count reduction is equal to or smaller than the ATHRESH value, 0 is stored as the reduced 1-bit <math>\alpha</math> data. In other cases, 1 is stored as the 1-bit <math>\alpha</math> data.</p> <p>A value from 0 to 255 can be specified.</p>
15, 14	—	All 0	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>
13, 12	CLMD[1:0]	00	R/W	<p>Color Data Clipping</p> <p>These bits specify the method for clipping the YCbCr color data output from the WPF. When RGB color data is output from the WPF, specify 0 in these bits.</p> <p>00: Output value is not clipped (0 to 255)</p> <p>01: Output value is clipped: YCbCr mode 1 (16 to 235 (Y), 16 to 240 (Cb/Cr))</p> <p>10: Output value is clipped: YCbCr mode 2 (Y/Cb/Cr = 1 to 254)</p> <p>11: Setting prohibited</p>
11 to 0	—	All 0	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>

### 28.2.8.7 WPFn Destination Y Plane Memory Stride Registers (VI6\_WPFn\_DSTM\_STRIDE\_Y)

Note: See Table 28.15 for details on which RZ/G series products have which registers.

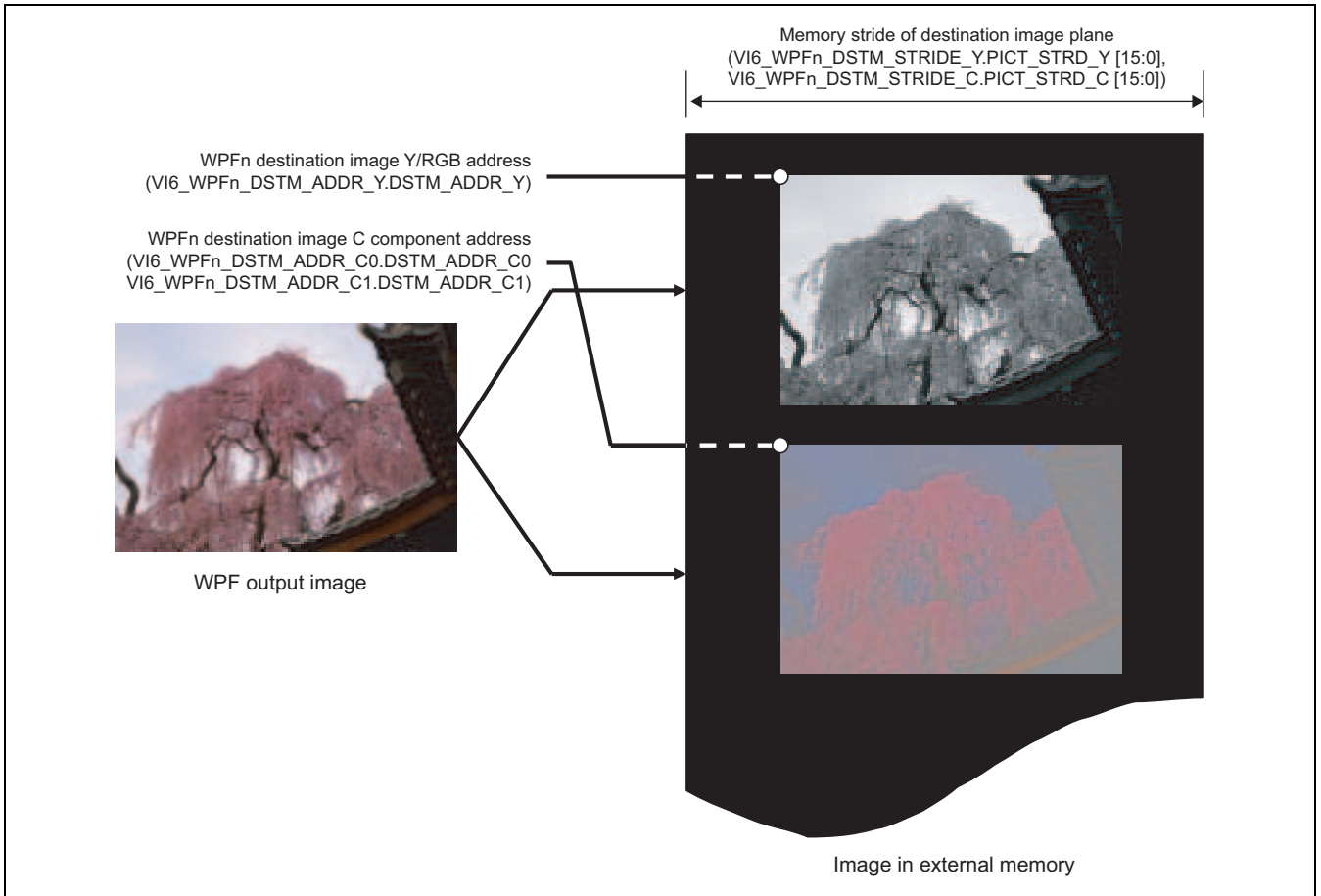
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PICT_STRD_Y [15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 0	PICT_STRD_Y [15:0]	H'0000	R/W	Memory Stride of Destination Picture Y/RGB Plane These bits specify in 1-byte units the memory stride of the destination picture in the external memory to be written to by the WPFn as shown in Figure 28.31. A value from H'0000 to H'FFFF can be specified.



**Figure 28.31 Writing Image Data to Destination Area in WPFn**

### 28.2.8.8 WPFn Destination C Plane Memory Stride Registers (VI6\_WPFn\_DSTM\_STRIDE\_C)

Note: See Table 28.15 for details on which RZ/G series products have which registers.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

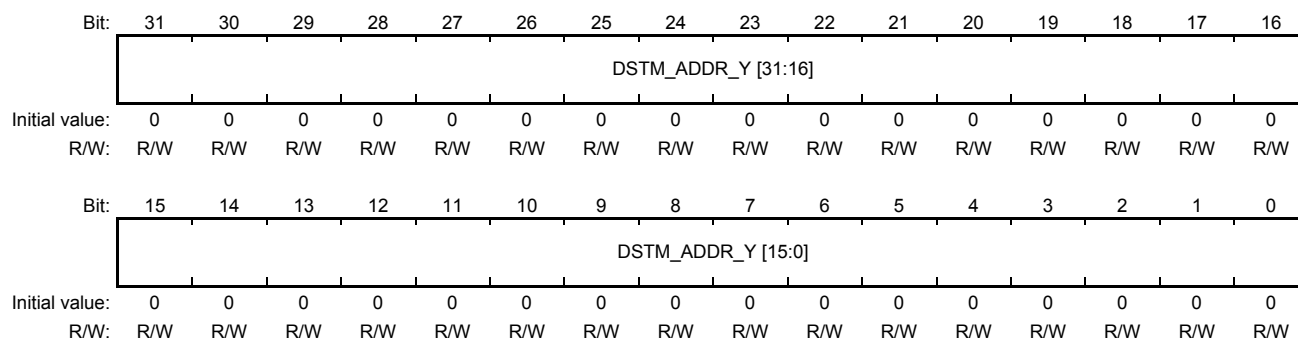
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PICT_STRD_C [15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 0	PICT_STRD_C [15:0]	H'0000	R/W	Memory Stride of Destination Picture C Plane These bits specify in 1-byte units the memory stride for the C plane of the destination picture in the external memory to be written to by the WPFn as shown in Figure 28.31. When the WPFn outputs images in an RGB format, this setting is not used. When the WPFn outputs images in YCbCr planar format, this setting is applied to both the Cb and Cr planes. A value from H'0000 to H'FFFF can be specified.

### 28.2.8.9 WPFn Destination Y/RGB Address Registers (VI6\_WPFn\_DSTM\_ADDR\_Y)

Note: See Table 28.15 for details on which RZ/G series products have which registers.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	DSTM_ADDR_Y [31:0]	H'0000 0000	R/W	<p>Destination Image Y/RGB Plane Storing Address</p> <p>These bits specify in 1-byte units the address for storing the destination-image Y plane or packed RGB plane to be written to by the WPFn in the method described later.</p> <p>A value from H'00000000 to H'FFFFFFFF can be specified.</p>

#### (Destination Address Specification Method)

When flipping is not used, the start address of a frame (address FHA shown in Figure 28.32) should be specified as the destination address. When flipping is used, the destination address is not the frame head address (FHA); one of addresses A0 to A1 shown in Figure 28.32 should be selected according to the combination of desired and flipping (VI6\_WPFn\_OUTFMT.FLP setting).

To strictly define locations A0 to A1, let the memory stride (VI6\_WPFn\_DSTM\_STRIDE\_Y/C setting) be S as shown in Figure 28.32). Calculate the destination address (one of A0 to A1) using the formula shown in Table 28.26 and specify it in the destination address storing register.

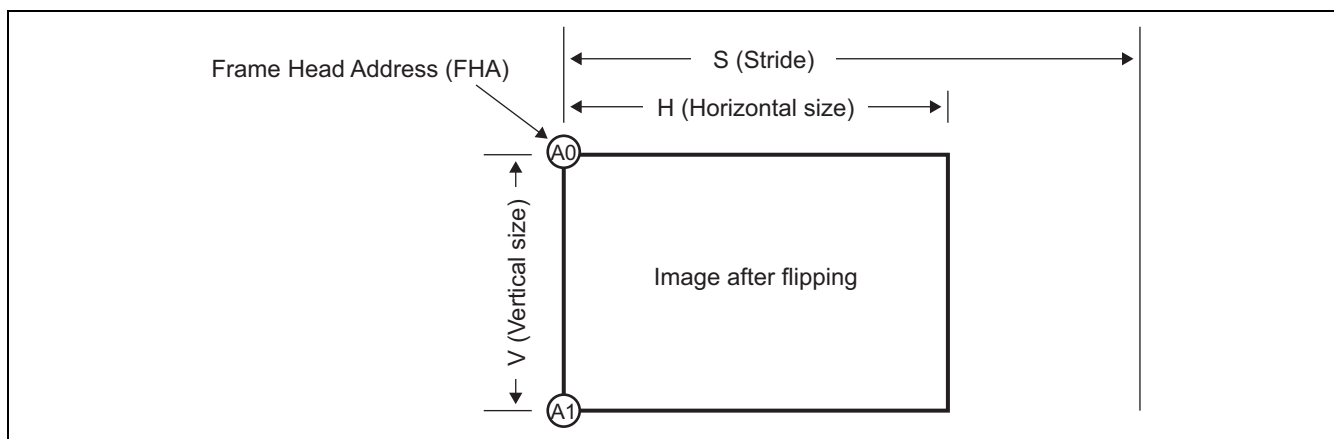


Figure 28.32 Location of Destination Address to be Specified for Vertical Flipping



**Table 28.26 Destination Address A<sub>0</sub>, and A<sub>1</sub> Calculation Formulas**

VI6_WPFn_OUTFMT.FLP Setting	Formula for Calculating Address to be Set in VI6_WPFn_DSTM_ADDR_Y, VI6_WPFn_DSTM_ADDR_C0, and VI6_WPFn_DSTM_ADDR_C1
0	$A_0 = FHA$
1	$A_1 = FHA + (V \times L - 1) \times S$

**Table 28.26a Value of L according to VI6\_WPFn\_OUTFMT.WRFMT Setting (for RGB and Luminance Y Address Calculation)**

VI6_WPFn_OUTFMT.WRFMT	L
73	0.5
0 to 2, 4 to 35, 64 to 66, 70 to 72, or 74 to 76	1

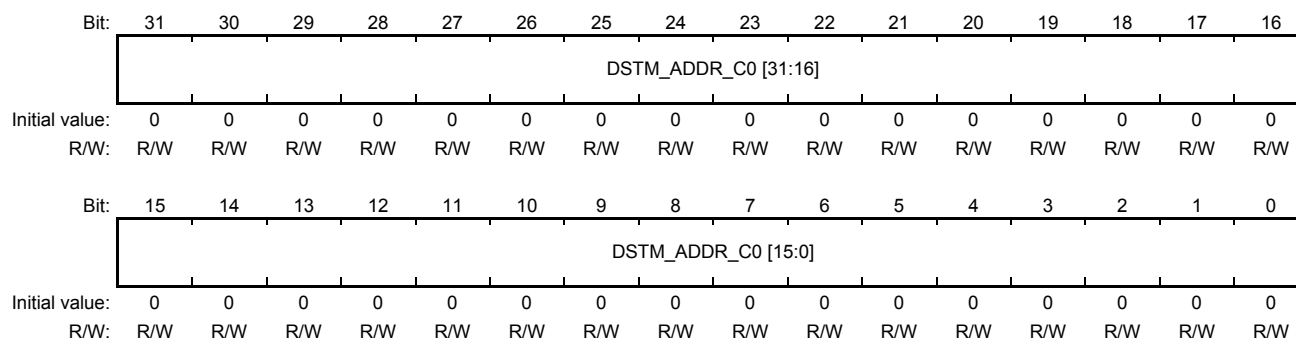
**Table 28.26b Value of L according to VI6\_WPFn\_OUTFMT.WRFMT Setting (for Chrominance C0 and C1 Address)**

VI6_WPFn_OUTFMT.WRFMT	L
70 to 73	Not defined
66, 76	0.5
64 to 65, 74 to 75	1

### 28.2.8.10 WPFn Destination Chroma Address Registers 0 (VI6\_WPFn\_DSTM\_ADDR\_C0)

Note: See Table 28.15 for details on which RZ/G series products have which registers.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

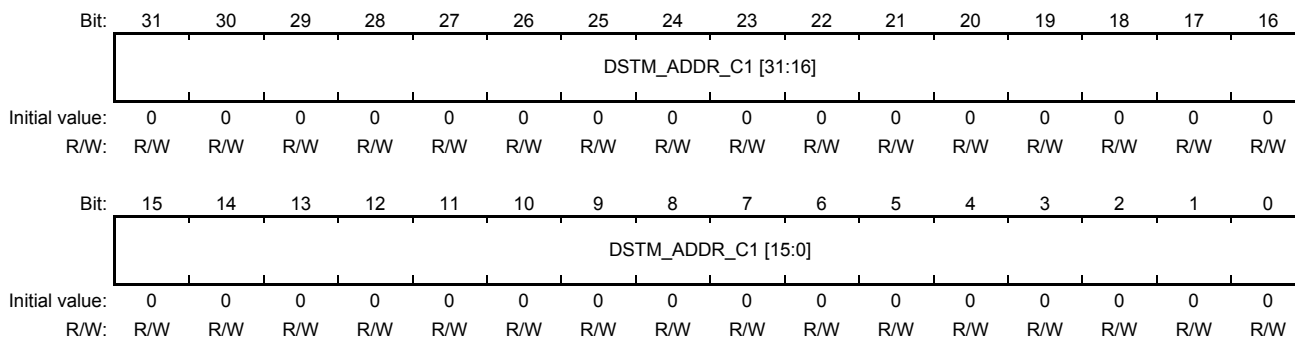


Bit	Bit Name	Initial Value	R/W	Description
31 to 0	DSTM_ADDR_C0 [31:0]	H'0000 0000	R/W	<p>Destination Image C Plane Storing Address 0</p> <p>These bits specify in 1-byte units the address for storing the destination-image C plane to be written to by the WPFn. Refer to the description of VI6_WPFn_DSTM_ADDR_Y for settings.</p> <p>Here, the C plane indicates the combined CbCr plane when a semi-planar format is selected from the packed YCbCr formats shown in Table 28.25 or the Cb plane when a planar format is selected. When an interleaved format is selected or the output is in an RGB format, this setting is not used.</p> <p>A value from H'00000000 to H'FFFFFFFF can be specified. Refer to Figure 28.32 in section 28.2.8.9 for settings.</p>

**28.2.8.11 WPFn Destination Chroma Address Registers 1 (VI6\_WPFn\_DSTM\_ADDR\_C1)**

Note: See Table 28.15 for details on which RZ/G series products have which registers.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	DSTM_ADDR_C1 [31:0]	H'0000 0000	R/W	<p>Destination Image C Plane Storing Address 1</p> <p>These bits specify in 1-byte units the address for storing the Cr plane when the WPFn outputs images to the external memory in YCbCr planar format shown in Table 28.25. Refer to the description of VI6_WPFn_DSTM_ADDR_Y for settings.</p> <p>This setting is not used when the WPF outputs in YCbCr format that is not a planar format or in an RGB format.</p> <p>A value from H'00000000 to H'FFFFFFFF can be specified. Refer to Figure 28.32 in section 28.2.8.9 for settings.</p>

**28.2.8.12 WPF0 LIF Write Back Control Registers (VI6\_WPF0\_WRBCK\_CTRL)**

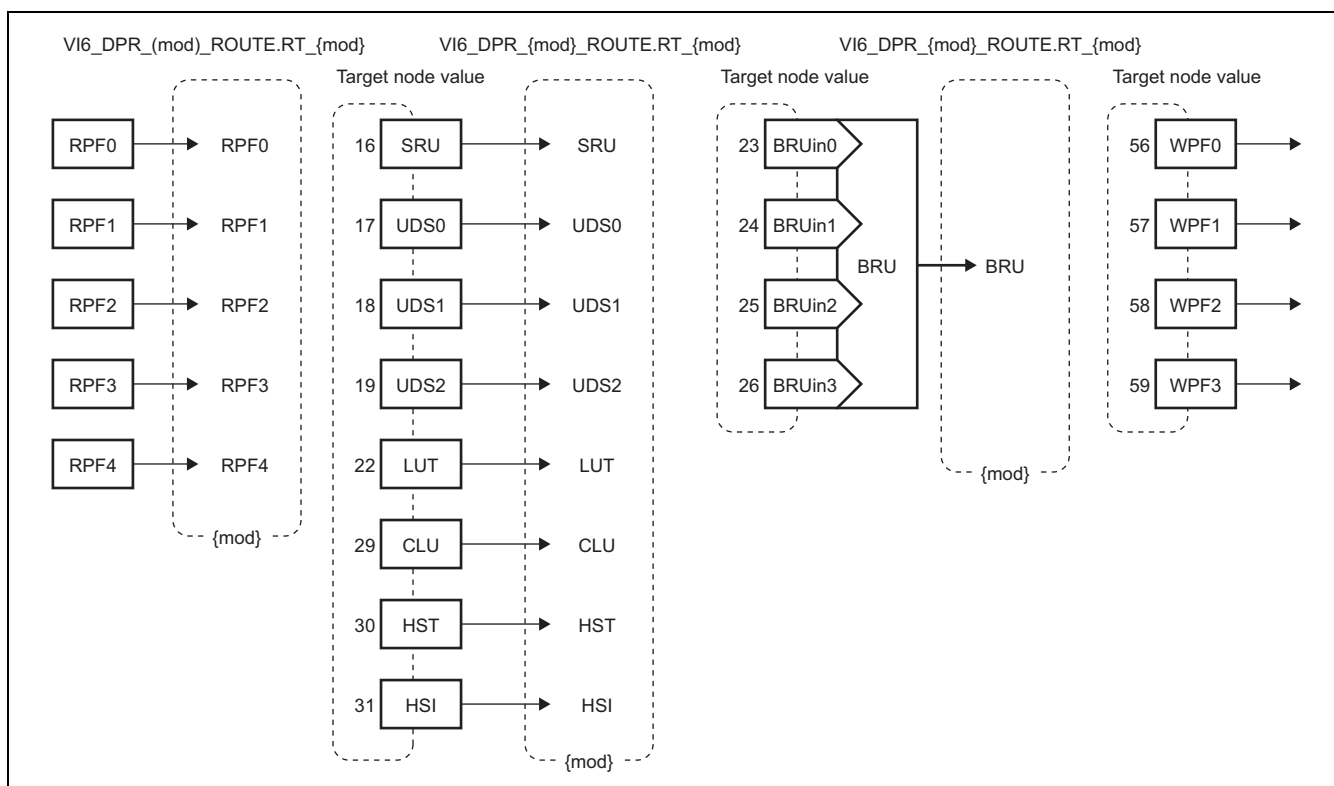
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	WBMD[1:0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1, 0	WBMD[1:0]	00	R/W	Display Data Write Back Control This bit is used for selecting the write back mode when the value of VI6_LIF_CTRL.LIF_EN bit is set to 1. 00: Write Back Disabled 01: Write Back Enabled

## 28.2.9 DPR Control Registers

### 28.2.9.1 Concept of DPR Settings



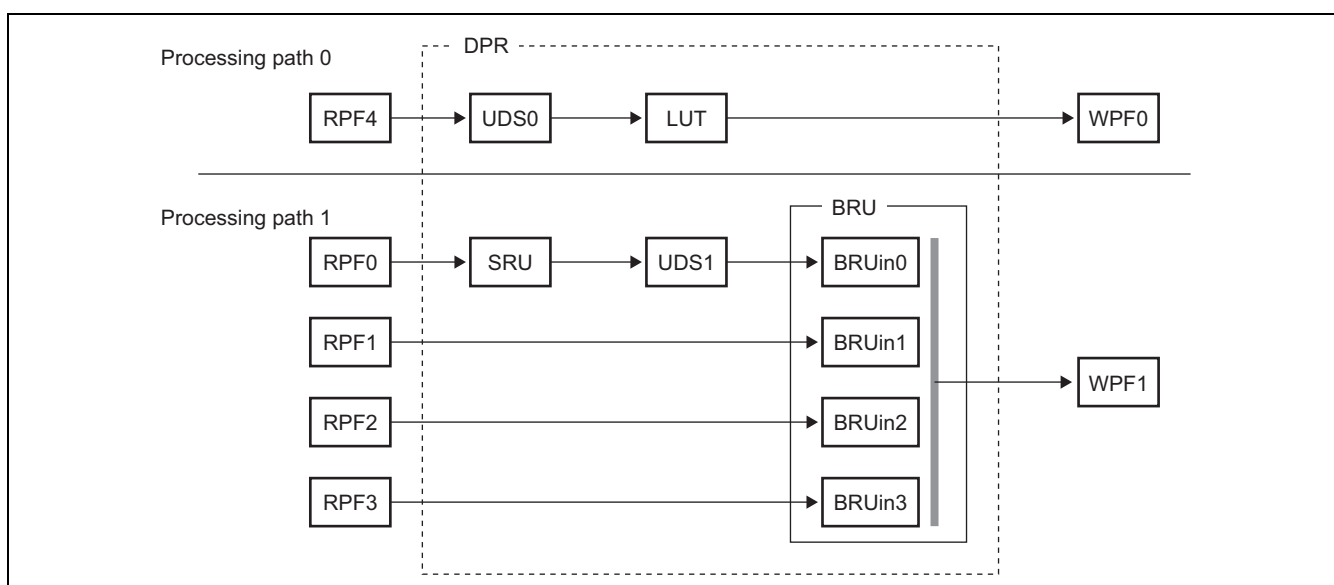
**Figure 28.33 Node Register Names and Target Node Values on Data Path Router**

In the VSP1 internal data path, the order of processes can be specified as desired. The module for performing each process has a unique node value. Set each bit field in `VI6_DPR_*_ROUTE` to an appropriate node value shown in Figure 28.33 to specify the target node to be connected behind each module.

For DPR settings, all of the following restrictions should be observed. If any of them is violated, even the WPF paths operating correctly at that time will be affected as well as the WPF paths connected through the DPR, and correct operation will not be guaranteed (for example, if a restriction is violated for the DPR setting related to WPF2, even WPF0 and WPF1 that are operating correctly will be affected).

1. Specify 63 for the output node values of all RPFs and processing modules that are not used in the DPR. Here, make sure that no module is connected to a module for which 63 is specified as the node value.
2. When specifying a value other than 63 for an output node value in the DPR, make sure that valid inputs (RPF0 to RPF4 or virtual RPF) and a target WPF are determined.
3. When a certain module is not implemented due to the LSI-specific restrictions described in Tables 28.1 to 28.3, specify 63 for the corresponding `VI6_DPR_*_ROUTE.RT_*`.
4. Only one module can be connected to each module; specifying the same target node value for two or more modules is prohibited.
5. Desired modules can be connected between each RPF and BRU input port, but all RPFs specified as the sources for a BRU input port should have the same target WPF.
6. Make appropriate routing or RPF register settings so that the color space formats (RGB/YCbCr) for all BRU input ports are the same.
7. Connect data paths appropriately so that each of UDS0 to UDS2 is used only once throughout all paths from RPF<sub>n</sub> (n = 0 to 4) to WPF<sub>n</sub> (n = 0 to 3). Connecting UDS0 to UDS2 in serial is prohibited even when there is another module between them.

8. When the BRU is connected between RPF<sub>n</sub> and WPF<sub>n</sub>, any of UDS0 to UDS2 can be connected in parallel with each path from RPF<sub>n</sub> to BRU input ports 0 to 3. Note that when any of UDS0 to UDS2 is connected before BRU input ports 0 to 3, UDS0 to UDS2 cannot be used behind the BRU. In such a parallel UDS connection, the performance may be degraded. For details, contact a Renesas Electronics sales representative.
9. Do not connect the output of any module as the input to the same module (in the BRU case, any input port) even when there is another module between the output and input (creating a loop is prohibited).
10. Each node can be used only once throughout all paths from RPF<sub>n</sub> to WPF<sub>n</sub>. When a module shown in Figure 28.33 is assigned in one RPF – WPF path, it cannot be used in another RPF – WPF path.
11. While a WPF is operating, modifying the DPR connection settings in VI6\_DPR\_\*\_ROUTE is prohibited for modules used by the WPF but allowed for modules not used by the WPF. Be careful not to accidentally modify the settings of the modules included in the WPF path that is operating.



**Figure 28.34 Examples of Internal Data Path Routing**

Figure 28.34 shows examples of internal data path routing. Path 0 is assigned to WPF0 (RPF4 is the source RPF), and path 1 is assigned to WPF1 (RPF0 to RPF3 are the source RPFs). Each path has the configuration shown in Figure 28.34. Path 0 performs UDS and LUT processing (e.g., up/down scaling and  $\gamma$  correction). Path 1 performs super resolution processing and scaling for input 0 (RPF0) and then applies blending or raster operation between the resultant data and input data 1 to 3 (RPF1 to RPF3). The VI6\_DPR\_\*\_ROUTE settings for these examples are shown in Table 28.27. The bit fields for the modules that are not used in the examples should be set to 63.

**Table 28.27 VI6\_DPR\*\_ROUTE Register Settings in Connection Examples Shown in Figure 28.34**

Register Name	Setting	
VI6_DPR_RPF0_ROUTE	16	(To SRU)
VI6_DPR_RPF1_ROUTE	24	(To BRUin1)
VI6_DPR_RPF2_ROUTE	25	(To BRUin2)
VI6_DPR_RPF3_ROUTE	26	(To BRUin3)
VI6_DPR_RPF4_ROUTE	17	(To UDS0)
VI6_DPR_SRU_ROUTE	18	(To UDS1)
VI6_DPR_UDS0_ROUTE	22	(To LUT)
VI6_DPR_UDS1_ROUTE	23	(To BRUin0)
VI6_DPR_UDS2_ROUTE	63	(UNUSED)
VI6_DPR_LUT_ROUTE	56	(To WPF0)
VI6_DPR_CLU_ROUTE	63	(UNUSED)
VI6_DPR_HST_ROUTE	63	(UNUSED)
VI6_DPR_HSI_ROUTE	63	(UNUSED)
VI6_DPR_BRU_ROUTE	57	(To WPF1)

Although both examples shown in Figure 28.34 include operation in image processing modules, connect the RPF to the WPF directly when only image format conversion or packed format conversion is required.

### 28.2.9.2 RPFn Routing Register (VI6\_DPR\_RPFn\_ROUTE: n = 0, 1, 2, 3, 4)

Note: See Table 28.15 for details on which RZ/G series products have which registers.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	RT_RPFn [5:0]					
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5 to 0	RT_RPFn [5:0]	H'00	R/W	RPFn Target Node Value These bits specify the target node value for RPFn. When using RPFn, refer to Figure 28.33 for settings. When RPFn is not started through the VI6_WPFn_SRCRPF setting, specify 63.



### 28.2.9.3 WPFn Timing Control Register (VI6\_DPR\_WPFn\_FPORCH: n = 0, 1, 2, 3)

Note: See Table 28.15 for details on which RZ/G series products have which registers.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13 to 8	FP_WPFn [5:0]	H'00	R/W	WPFn Internal Operation Timing Setting <b>Specify 5.</b>
7 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

### 28.2.9.4 {mod} Routing Register (VI6\_DPR\_{mod}\_ROUTE: {mod} = SRU, UDSn, LUT, CLU, HST, HSI, BRU)

Note: See Table 28.15 for details on which RZ/G series products have which registers.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
	—	—	—	—	—	—	—	—	FXA [7:0]								
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	—	—	FP [5:0]					—	—	RT [5:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 16	FXA [7:0]	H'00	R/W	{mod} Fixed $\alpha$ Output Value for {mod} The {mod} does not support input/output of the $\alpha$ value. The $\alpha$ value input to the {mod} is discarded, and the fixed $\alpha$ value specified in these bits is always output from the {mod}. A value from 0 to 255 can be specified. These bits are valid for SRU, LUT, CLU, HST and HSI modules. For UDSn, and BRU modules, these bits are reserved.
15, 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13 to 8	FP [5:0]	H'00	R/W	{mod} Internal Operation Timing Setting Specify 0.
7, 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5 to 0	RT [5:0]	H'00	R/W	{mod} Target Node Value These bits specify the target node value for the {mod}. When using the {mod}, refer to Figure 28.33 for settings. When not using the {mod}, specify 63.

### 28.2.9.5 {mod} Sampling Point Register (VI6\_DPR\_{mod}\_SMPPT: {mod} = HGO, HGT)

Note: See Table 28.15 for details on which RZ/G series products have which registers.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	TGW [2:0]		—	—	PT [5:0]						
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 11	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
10 to 8	TGW [2:0]	000	R/W	Target WPF Index for {mod} These bits are used for specifying the target WPF index of {mod}. If {mod} is not used, set B'111 to these bits.
7, 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5 to 0	PT[5:0]	H'00	R/W	Target Node Index for {mod} Histogram Sampling {mod} generates the histogram for the target node specified by these bits. For example, if these bits are set to 0, {mod} module generates the histogram for the output data of RPF0. Refer to Table 28.28 for the target node index which can be used for {mod}. If {mod} is not used, set 63 to these bits.

**Table 28.28 Target Node Index for {mod} Module**

Node Index	Module for Histogram Generation
0 to 4	RPF0 to 4
16	SRU
17 to 19	UDS0 to 2
22	LUT
27	BRU
29	CLU
30	HST
31	HSI
55	LIF*

Note: \* Do not set the value 55 to PT in case of LIF write back is used (i.e. VI6\_WPF0\_WRBACK\_CTRL.WBMD [1:0] = 1).

## 28.2.10 SRU Control Registers

### 28.2.10.1 Super Resolution Control Register 0 (VI6\_SRU\_CTRL0)

Note: See Table 28.15 for details on which RZ/G series products have which registers.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	SRU_PARAM0 [8:0]								
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	SRU_PARAM1 [4:0]				—	SRU_MODE [2:0]		SRU_PARAM2	SRU_PARAM3	SRU_PARAM4	SRU_EN		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 25	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
24 to 16	SRU_PARAM0 [8:0]	All 0	R/W	Super Resolution Parameter 0 Specify an appropriate value shown in Table 28.29; do not specify any other value.
15 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12 to 8	SRU_PARAM1 [4:0]	All 0	R/W	Super Resolution Parameter 1 Specify an appropriate value shown in Table 28.29; do not specify any other value.
7	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
6 to 4	SRU_MODE [2:0]	000	R/W	Super Resolution Mode Setting These bits specify a super resolution mode. In super resolution without scaling, the output size is the same as the input size. In super resolution with double scale-up, the output size is twice the input size. 000: Super resolution without scaling 100: Super resolution with double scale-up Other settings are prohibited.
3	SRU_PARAM2	0	R/W	Super Resolution Parameter 2 This parameter setting depends on the color space of the image input to the SRU. Specify an appropriate value shown in Table 28.30; do not specify any other value.
2	SRU_PARAM3	0	R/W	Super Resolution Parameter 3 Specify an appropriate value shown in Table 28.30; do not specify any other value.

Bit	Bit Name	Initial Value	R/W	Description
1	SRU_PARAM4	0	R/W	Super Resolution Parameter 4 This parameter setting depends on the color space of the image input to the SRU. Specify an appropriate value shown in Table 28.30; do not specify any other value.
0	SRU_EN	0	R/W	Super Resolution Processing Enable/Disable Enables or disables super resolution processing. This setting has the highest priority over all other SRU registers. 0: Super resolution processing is disabled (input goes through the SRU without change) 1: Super resolution processing is enabled

YCbCr format is recommended for the super resolution processing. If the super resolution processing is applied to an RGB-format image, adverse effects such as color blur may be generated; when using an RGB format, evaluate the image quality carefully before applying the processing to practical use.

To execute the super resolution processing in YCbCr format, set up the RPF and DPR appropriately so that YCbCr-format image data is input to the SRU. Specifically, make the RPFn output YCbCr-format image data and send the output data to the SRU through the DPR. For details of RPFn input/output settings, refer to section 28.2.7.3. For DPR settings, refer to sections 28.2.9.1 to 28.2.9.4.

**Table 28.29 Super Resolution Parameter Setting 1**

	VI6_SRU_CTRL0			VI6_SRU_CTRL1	VI6_SRU_CTRL2			
	SRU_MODE	SRU_PARAM0	SRU_PARAM1	SRU_PARAM5	SRU_PARAM6	SRU_PARAM7	SRU_PARAM8	
Weak	1	0 or 4	256	4	H'7FF	24	40	255
	2	0 or 4	256	4	H'7FF	8	16	255
	3	0 or 4	384	5	H'7FF	36	60	255
	4	0 or 4	384	5	H'7FF	12	27	255
	5	0 or 4	511	6	H'7FF	48	80	255
Strong	6	0 or 4	511	6	H'7FF	16	36	255

**Table 28.30 Super Resolution Parameter Setting 2**

Color Space of SRU Input Image	SRU_PARAM2	SRU_PARAM3	SRU_PARAM4
YCbCr*	0	1	0
RGB	1	1	1

Note: \* YCbCr format is recommended for the image input to the SRU.

### 28.2.10.2 Super Resolution Control Register 1 (VI6\_SRU\_CTRL1)

Note: See Table 28.15 for details on which RZ/G series products have which registers.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	SRU_PARAM5 [10:0]										
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 11	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
10 to 0	SRU_PARAM5 [10:0]	All 0	R/W	Super Resolution Parameter 5 Specify an appropriate value shown in Table 28.29; do not specify any other value.

### 28.2.10.3 Super Resolution Control Register 2 (VI6\_SRU\_CTRL2)

Note: See Table 28.15 for details on which RZ/G series products have which registers.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	SRU_PARAM6 [7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SRU_PARAM7 [7:0]								SRU_PARAM8 [7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 16	SRU_PARAM6 [7:0]	H'00	R/W	Super Resolution Parameter 6 Specify an appropriate value shown in Table 28.29; do not specify any other value.
15 to 8	SRU_PARAM7 [7:0]	H'00	R/W	Super Resolution Parameter 7 Specify an appropriate value shown in Table 28.29; do not specify any other value.
7 to 0	SRU_PARAM8 [7:0]	H'00	R/W	Super Resolution Parameter 8 Specify an appropriate value shown in Table 28.29; do not specify any other value.

## 28.2.11 UDS Control Registers

### 28.2.11.1 Scaling Control Registers (VI6\_UDSn\_CTRL)

Note: See Table 28.15 for details on which RZ/G series products have which registers.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	AMD	FMD	BLADV	—	—	AON	ATHON	—	—	—	BC	NE_A	NE_RC R	NE_GY	NE_BC B
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R	R	R/W	R/W	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TDIPC	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R

Bit	Bit Name	Initial Value	R/W	Description
31	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
30	AMD	0	R/W	Pixel Count at Scale-Up Specifies the number of pixels generated through scale-up in the UDS. This bit setting is ignored for scale-down. 0: Pixel count after scale-up is $1 + \langle n - 1 \rangle \times \text{scale-up factor}$ 1: Pixel count after scale-up is $\langle n \rangle \times \text{scale-up factor}$ Note: n: Number of pixels input to UDS
29	FMD	0	R/W	Padding for Insufficient Clipping Size When the scaling filter outputs an image that is smaller than the clipping size (VI6_UDSn_CLIP_SIZE), pixels are interpolated to match the clipping size. This bit specifies the pixel filling method. 0: Pixels are filled by copying pixels at the right edge and the bottom edge. 1: Pixels are filled with the color specified by VI6_UDSn_FILL_COLOR.
28	BLADV	0	R/W	Bilinear or Nearest Neighbor Interpolation Characteristic Control Controls the characteristics of bilinear or nearest neighbor interpolation. Setting this bit to 1 improves the aliasing characteristics at $\times 1/2$ to $1/8$ scaling (VI6_UDS_SCALE.VMANT/HMANT = 2 to 8). Note that the apparent resolution around edges may deteriorate. In multi-tap mode, this control is not available; to use this control, set the BC bit to 0.
27, 26	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.



Bit	Bit Name	Initial Value	R/W	Description
25	AON	0	R/W	<p>Scale-Up/Down of <math>\alpha</math> Plane</p> <p>These bits specify whether to enable or disable scale-up/down of the <math>\alpha</math> plane when scaling up/down in the RGB format. When the AON bit is set to 0, the UDS outputs the value of the VI6_UDSn_ALPVAL.ALPH_VAL0 bits as a fixed <math>\alpha</math> value.</p> <p>0: <math>\alpha</math> scale-up/-down is not performed 1: <math>\alpha</math> scale-up/-down is performed</p>
24	ATHON	0	R/W	<p><math>\alpha</math> Output Data Threshold Comparison Enable/Disable</p> <p>Enables or disables comparison with the <math>\alpha</math> output data threshold. When this bit is 1, the output <math>\alpha</math> value is replaced according to the VI6_UDSn_ALPTH and VI6_UDSn_ALPVAL values.</p> <p>When the AON bit is 0 (scale-up/-down of the <math>\alpha</math> plane is disabled), this bit setting has no effect.</p> <p>0: <math>\alpha</math> output data threshold comparison is disabled 1: <math>\alpha</math> output data threshold comparison is enabled</p>
23 to 21	—	All 0	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>
20	BC	0	R/W	<p>Pixel Component Interpolation Method at Scale-Up/Down</p> <p>Specifies the method for interpolating pixel components at scale-up/-down.</p> <p>0: Bilinear or nearest neighbor interpolation method is used 1: Interpolation method equivalent to 4 to 17 taps in accordance with the scaling factor is used (multi-tap mode)</p> <p>Note that the <math>\alpha</math> component is interpolated by the method specified in the NE_A bit instead of the multi-tap method.</p> <p>When the BC and AON bits are both set to 1, the scaling shall be scale-up, no scaling, or scale-down with scaling factor 1/1 to 1/2.</p>
19	NE_A	0	R/W	<p><math>\alpha</math> Interpolation Method</p> <p>Specifies the interpolation method of the <math>\alpha</math> plane. When the AON bit is 0 (scale-up/-down of the <math>\alpha</math> plane is disabled), this bit setting has no effect.</p> <p>0: Bilinear method 1: Nearest neighbor method*</p>
18	NE_RCR	0	R/W	<p>R/Cr Interpolation Method When Bilinear/Nearest Neighbor Interpolation is Selected</p> <p>Specifies the interpolation method of the R/Cr component when bilinear/nearest neighbor interpolation is selected (BC = 0).</p> <p>0: Bilinear method 1: Nearest neighbor method*</p>
17	NE_GY	0	R/W	<p>G/Y Interpolation Method When Bilinear/Nearest Neighbor Interpolation is Selected</p> <p>Specifies the interpolation method of the G/Y component when bilinear/nearest neighbor interpolation is selected (BC = 0).</p> <p>0: Bilinear method 1: Nearest neighbor method*</p>

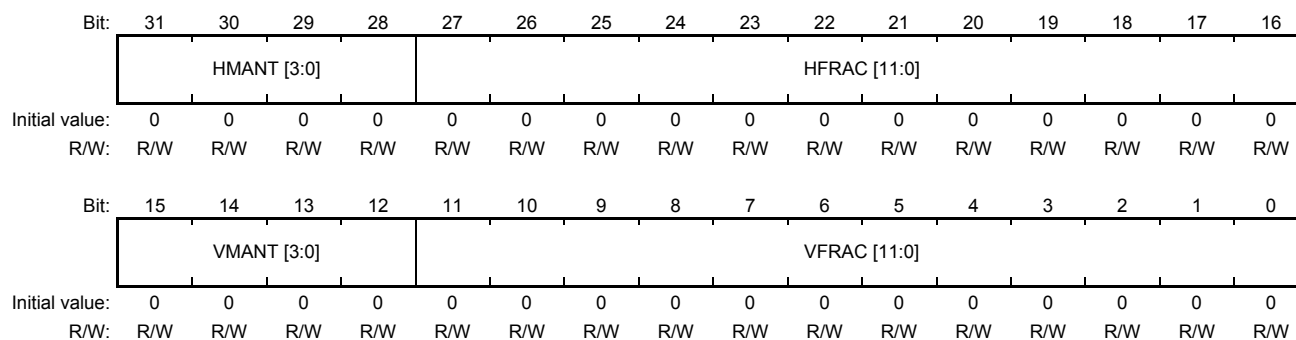
Bit	Bit Name	Initial Value	R/W	Description
16	NE_BCB	0	R/W	B/Cb Interpolation Method When Bilinear/Nearest Neighbor Interpolation is Selected Specifies the interpolation method of the B/Cb component when bilinear/nearest neighbor interpolation is selected (BC = 0). 0: Bilinear method 1: Nearest neighbor method*
15 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	TDIPC	0	R/W	2D-IPC function Enable/Disable Select 0: 2D IPC function Disable 1: 2D IPC function Enable UDSn execute 2D IPC function based on this bit and the setting of VI6_UDSn_IPC register. See section 28.2.11.6, 2D IPC Setting Register (VI6_UDSn_IPC) for more details.
0	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Note: \* This method can be used only when the scale-up/-down factor is 1/1 to 1/4.

### 28.2.11.2 Scaling Factor Registers (VI6\_UDSn\_SCALE)

Note: See Table 28.15 for details on which RZ/G series products have which registers.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√



Bit	Bit Name	Initial Value	R/W	Description
31 to 28	HMANT[3:0]	H'0	R/W	<p>Multiplier (Integral Part) of Horizontal Scaling Factor</p> <p>These bits specify the integral part of the horizontal scaling factor. The image size to be obtained changes according to this setting. Calculate an appropriate value using the formula shown later to obtain a desired image size.</p> <p>A value from H'0 to H'F can be specified. Select a value within the range shown in Table 28.31.</p>
27 to 16	HFRAC[11:0]	H'000	R/W	<p>Multiplier (Fractional Part) of Horizontal Scaling Factor</p> <p>These bits specify the fractional part of the horizontal scaling factor. The image size to be obtained changes according to this setting. Calculate an appropriate value using the formula shown later to obtain a desired image size.</p> <p>A value from H'100 to H'FFF can be specified when an image is upsampled (the HMANT value is 0) in the horizontal direction. A value from H'000 to H'FFF can be specified when an image is downsampled (the HMANT value is not 0) in the horizontal direction. Select a value within the range shown in Table 28.31.</p>
15 to 12	VMANT[3:0]	H'0	R/W	<p>Multiplier (Integral Part) of Vertical Scaling Factor</p> <p>These bits specify the integral part of the vertical scaling factor. The image size to be obtained changes according to this setting. Calculate an appropriate value using the formula shown later to obtain a desired image size.</p> <p>A value from H'0 to H'F can be specified. Select a value within the range shown in Table 28.31.</p>
11 to 0	VFRAC[11:0]	H'000	R/W	<p>Multiplier (Fractional Part) of Vertical Scaling Factor</p> <p>These bits specify the fractional part of the vertical scaling factor. The image size to be obtained changes according to this setting. Calculate an appropriate value using the formula shown later to obtain a desired image size.</p> <p>A value from H'100 to H'FFF can be specified when an image is upsampled (the VMANT value is 0) in the vertical direction. A value from H'000 to H'FFF can be specified when an image is downsampled (the VMANT value is not 0) in the vertical direction. Select a value within the range shown in Table 28.31.</p>

The HMANT and HFRAC bits set the scale-up/-down factor for an image in the horizontal direction, and the VMANT and VFRAC bits set the scale-up/-down factor for an image in the vertical direction. The UDS operation switches between horizontal scale-up and horizontal scale-down according to the HMANT and HFRAC bit settings, as shown in Table 28.31. (Setting a value outside the ranges of Table 28.31 in UDS operation is prohibited). Table 28.31 is for the horizontal direction, but it is similar for the vertical direction. In this case, replace HMANT with VMANT and HFRAC with VFRAC when reading.

Note that settings for scaling in the horizontal direction and settings for scaling in the vertical direction can be made independently. Therefore, a setting for scale-up in the horizontal direction and scale-down in the vertical direction is possible. In such a case, because the formula (described later) for obtaining the image size after scale-up/-down is different between scale-up and scale-down, a formula matching the scale-up or scale-down operation should be selected independently for the horizontal direction and vertical direction.

**Table 28.31 Switching of Horizontal Scale-Up/Down Operation According to HMANT and HFRAC Bit Settings**

HMANT	HFRAC	UDS Operation
H'0	H'100 to H'FFF	Scale-up
H'1	H'000	Same size (no scale-up/-down)
	H'001 to H'FFF	Scale-down
H'2 to H'F	H'000 to H'FFF	

Described here is the method for calculating the size of the upscaled/downscaled image that was obtained based on this register setting. First, define the variables necessary for calculating the horizontal size of the upscaled/downscaled image, as shown below.

$$h_{scale} = \frac{4096}{4096 \times m_h + f_h}$$

$m_h$  is the value of VI6\_UDSn\_SCALE.HMANT, and  $f_h$  is the value of VI6\_UDSn\_SCALE.HFRAC. This formula expresses the estimate of the scale-up/-down factor processed by the UDS. If the horizontal size of the image before scale-up/-down is set as  $h_{size_{org}}$ , the horizontal size of the image after scale-up/-down can be roughly obtained through  $h_{size_{org}} \times h_{scale}$ .

Similarly, define the variables necessary for calculating the vertical size of the upscaled/downscaled image.

$$v_{scale} = \frac{4096}{4096 \times m_v + f_v}$$

When setting  $m_v$  as the value of VI6\_UDSn\_SCALE.VMANT,  $f_v$  as the value of VI6\_UDSn\_SCALE.VFRAC, and  $v_{size_{org}}$  as the vertical size of the image before scale-up/-down, the vertical size of the image after scale-up/-down can be roughly obtained through  $v_{size_{org}} \times v_{scale}$ .

When the UDSn performs scale-down with the settings of Table 28.31, using the variables defined so far, the horizontal size of the downscaled image  $h_{size_{down\_scaled}}$  and the vertical size of the downscaled image  $v_{size_{down\_scaled}}$  become as follows:

$$hsize_{down\_scaled} = \left\langle 1 + \left( \left\langle 1 + \frac{\langle hsize_{org} - 1 \rangle}{m_h'} \right\rangle - 1 \right) \times m_h' \times hscale \right\rangle$$

$$vsize_{down\_scaled} = \left\langle 1 + \left( \left\langle 1 + \frac{\langle vsize_{org} - 1 \rangle}{m_v'} \right\rangle - 1 \right) \times m_v' \times vscale \right\rangle$$

Since the division of *hscale* and *vscale* has to be executed at the end of the above formulas, respectively, formulas considering the order of operation become as follows:

$$hsize_{down\_scaled} = \left\langle 1 + \left( \left( \left\langle 1 + \frac{\langle hsize_{org} - 1 \rangle}{m_h'} \right\rangle - 1 \right) \times m_h' \times 4096 \right) / (4096 \times m_h + f_h) \right\rangle$$

$$vsize_{down\_scaled} = \left\langle 1 + \left( \left( \left\langle 1 + \frac{\langle vsize_{org} - 1 \rangle}{m_v'} \right\rangle - 1 \right) \times m_v' \times 4096 \right) / (4096 \times m_v + f_v) \right\rangle$$

The value of  $m_h'$  or  $m_v'$ , which is shown in Table 28.32, changes according to the setting of VI6\_UDSn\_SCALE.HMANT or VI6\_UDSn\_SCALE.VMANT.

**Table 28.32**  $m_h'$  or  $m_v'$  Setting

VI6_UDSn_SCALE.HMANT Setting (VI6_UDSn_SCALE.VMANT Setting)	$m_h'$ ( $m_v'$ )
1 to 3	1
4 to 7	2
8 to 15	4

When the UDSn performs scale-up with the settings of Table 28.31 and VI6\_UDSn\_CTRL.AMD is 0, the horizontal size of the upscaled image  $hsize_{up\_scaled}$  and the vertical size of the upscaled image  $vsize_{up\_scaled}$  become as follows:

$$hsize_{up\_scaled} = \left\langle 1 + (hsize_{org} - 1) \times hscale \right\rangle$$

$$vsize_{up\_scaled} = \left\langle 1 + (vsize_{org} - 1) \times vscale \right\rangle$$

Similar to the scale-down case, formulas considering the division of *hscale* and *vscale* become as follows:

$$hsize_{up\_scaled} = \left\langle 1 + ((hsize_{org} - 1) \times 4096) / (4096 \times m_h + f_h) \right\rangle$$

$$vsize_{up\_scaled} = \left\langle 1 + ((vsize_{org} - 1) \times 4096) / (4096 \times m_v + f_v) \right\rangle$$

When VI6\_UDSn\_CTRL.AMD is 1, the horizontal size of the upscaled image  $hsize_{up\_scaled}$  and the vertical size of the upscaled image  $vsize_{up\_scaled}$  become as follows:

$$hsize_{up\_scaled} = \langle hsize_{org} \times hscale \rangle$$

$$vsize_{up\_scaled} = \langle vsize_{org} \times vscale \rangle$$

After considering the division of hscale and vscale, the formulas become as follows:

$$hsize_{up\_scaled} = \langle (hsize_{org} \times 4096) / (4096 \times m_h + f_h) \rangle$$

$$vsize_{up\_scaled} = \langle (vsize_{org} \times 4096) / (4096 \times m_v + f_v) \rangle$$

### 28.2.11.3 $\alpha$ Data Threshold Setting Registers (VI6\_UDSn\_ALPTH)

Note: See Table 28.15 for details on which RZ/G series products have which registers.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

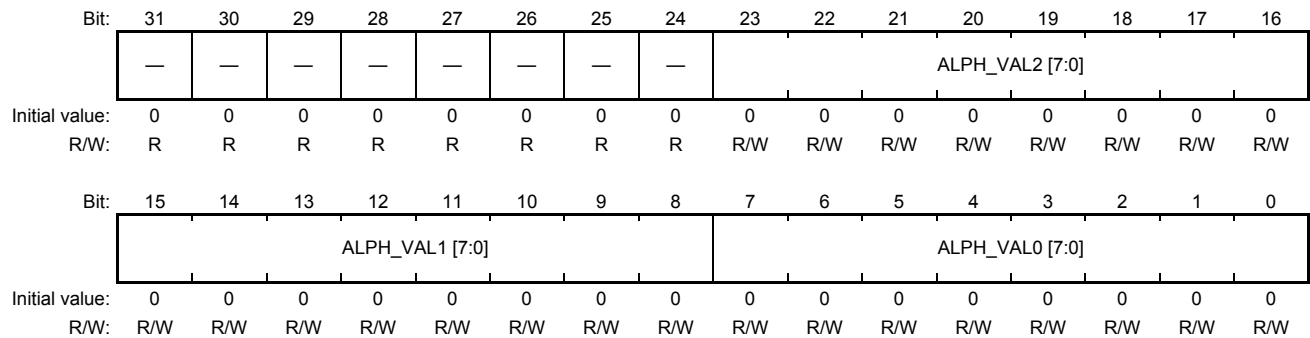
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ALPH_TH1 [7:0]								ALPH_TH0 [7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 8	ALPH_TH1 [7:0]	H'00	R/W	$\alpha$ Data Threshold Setting 1 When the $\alpha$ value is equal to or greater than the value of the ALPH_TH1 bits, the $\alpha$ value is replaced with that of VI6_UDSn_ALPVAL.ALPH_VAL2. When VI6_UDSn_CTRL.AON is 0 (scale-up/-down of the $\alpha$ plane is disabled), the setting of these bits has no effect. A value from H'00 to H'FF can be specified.
7 to 0	ALPH_TH0 [7:0]	H'00	R/W	$\alpha$ Data Threshold Setting 0 When the $\alpha$ value is equal to or smaller than the value of the ALPH_TH0 bits, the $\alpha$ value is replaced with that of VI6_UDSn_ALPVAL.ALPH_VAL0. When VI6_UDSn_CTRL.AON is 0 (scale-up/-down of the $\alpha$ plane is disabled), the setting of these bits has no effect. A value from H'00 to H'FF can be specified.

### 28.2.11.4 $\alpha$ Data Replacing Value Setting Registers (VI6\_UDSn\_ALPVAL)

Note: See Table 28.15 for details on which RZ/G series products have which registers.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 16	ALPH_VAL2 [7:0]	H'00	R/W	Replacing $\alpha$ Value Setting 2 These bits set a value that replaces the $\alpha$ value when it is equal to or greater than the value of VI6_UDSn_ALPTH.ALPH_TH1. When VI6_UDSn_CTRL.AON is 0 (scale-up/-down of the $\alpha$ plane is disabled), the setting of these bits has no effect. A value from H'00 to H'FF can be specified.
15 to 8	ALPH_VAL1 [7:0]	H'00	R/W	Replacing $\alpha$ Value Setting 1 These bits set a value that replaces the $\alpha$ value when it is greater than the value of VI6_UDSn_ALPTH.ALPH_TH0 and also smaller than that of VI6_UDSn_ALPTH.ALPH_TH1. When VI6_UDSn_CTRL.AON is 0 (scale-up/-down of the $\alpha$ plane is disabled), the setting of these bits has no effect. A value from H'00 to H'FF can be specified.
7 to 0	ALPH_VAL0 [7:0]	H'00	R/W	Replacing $\alpha$ Value Setting 0 These bits set a value that replaces the $\alpha$ value when it is equal to or smaller than the value of VI6_UDSn_ALPTH.ALPH_TH0. When VI6_UDSn_CTRL.AON is 0 (scale-up/-down of the $\alpha$ plane is disabled), $\alpha$ output value for the UDS is the fixed value specified in these bits. A value from H'00 to H'FF can be specified.



### 28.2.11.5 Passband Registers (VI6\_UDSn\_PASS\_BWIDTH)

Note: See Table 28.15 for details on which RZ/G series products have which registers.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16			
	—	—	—	—	—	—	—	—	—	BWIDTH_H [6:0]						—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
R/W:	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
	—	—	—	—	—	—	—	—	—	BWIDTH_V [6:0]						—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
R/W:	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W			

Bit	Bit Name	Initial Value	R/W	Description
31 to 23	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
22 to 16	BWIDTH_H [6:0]	All 0	R/W	Horizontal Signal Passband at Image Scale-Up/Down Set these bits following the method described later.
15 to 7	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
6 to 0	BWIDTH_V [6:0]	All 0	R/W	Vertical Signal Passband at Image Scale-Up/Down Set these bits following the method described later.

The method for setting the passband in the horizontal direction of an image is described. When the VI6\_UDSn\_SCALE.HMANT bits for horizontal scale-up/-down factor setting are not 0, set the BWIDTH\_H bits according to the following formula. When the VI6\_UDSn\_SCALE.HMANT bits are 0, set 64 in the BWIDTH\_H bits.

$$BWIDTH\_H = \left\langle 64 \times \frac{4096 \times m_h'}{4096 \times m_h + f_h} \right\rangle \quad (VI6\_UDSn\_SCALE.HMANT \neq 0)$$

$$BWIDTH\_H = 64 \quad (VI6\_UDSn\_SCALE.HMANT = 0)$$

$m_h$  is the value of VI6\_UDSn\_SCALE.HMANT, and  $f_h$  is the value of VI6\_UDSn\_SCALE.HFRAC. For the  $m_h'$  value, see Table 28.32. The method for setting the passband in the vertical direction of an image is similar to that for the horizontal direction described earlier. Since only the correspondence relationship of the registers is changed as shown below, replace the variables in the previous explanation as shown below when reading.

BWIDTH\_H → BWIDTH\_V

$m_h'$  →  $m_v'$

$m_h$  →  $m_v$

$f_h$  →  $f_v$

VI6\_UDSn\_SCALE.HMANT → VI6\_UDSn\_SCALE.VMANT

VI6\_UDSn\_SCALE.HFRAC → VI6\_UDSn\_SCALE.VFRAC

### 28.2.11.6 2D IPC Setting Register (VI6\_UDSn\_IPC)

Note: See Table 28.15 for details on which RZ/G series products have which registers.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	FIELD	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 28	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
27	FIELD	0	R/W	Top/Bottom Field Select Select Top/Bottom Field of image data when 2D IPC function is enabled (VI6_UDSn_CTRL.TDIPC = 1). 0: Top Field 1: Bottom Field
26 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

- Set 1 to VI6\_UDSn\_CTRL.TDIPC.
- Set appropriate setting of processing image  
Top Field: H'0000 0000  
Bottom Field: H'0800 0000

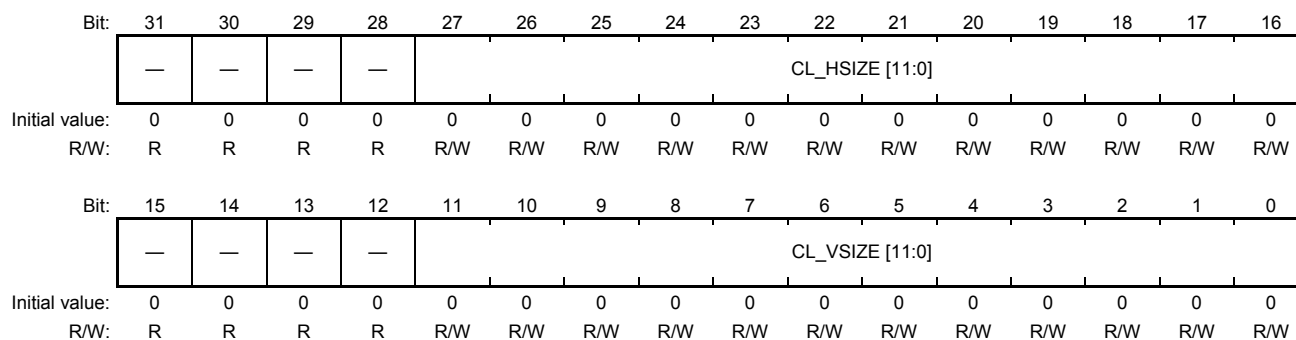
Notes: 1. Recommend usage case: Frame rate after 2D UPC is more than 50 fps.  
2. Be sure to set H'0000 0000 this register and set VI6\_UDSn\_CTRL.TDIPC

This register can be used for the image division mode or 2D interlace to progressive conversion (2D-IPC). When this register is not used, set VI6\_UDSn\_CTRL.TDIPC to 00. If the 2D-IPC mode is used, contact to Renesas for detail.

### 28.2.11.7 UDS Output Size Clipping Registers (VI6\_UDSn\_CLIP\_SIZE)

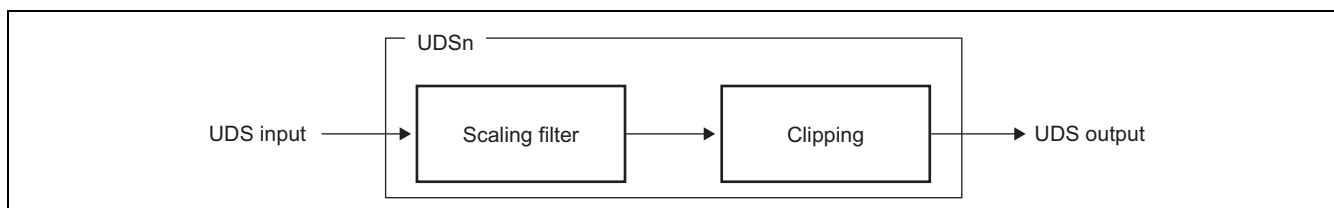
Note: See Table 28.15 for details on which RZ/G series products have which registers.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√



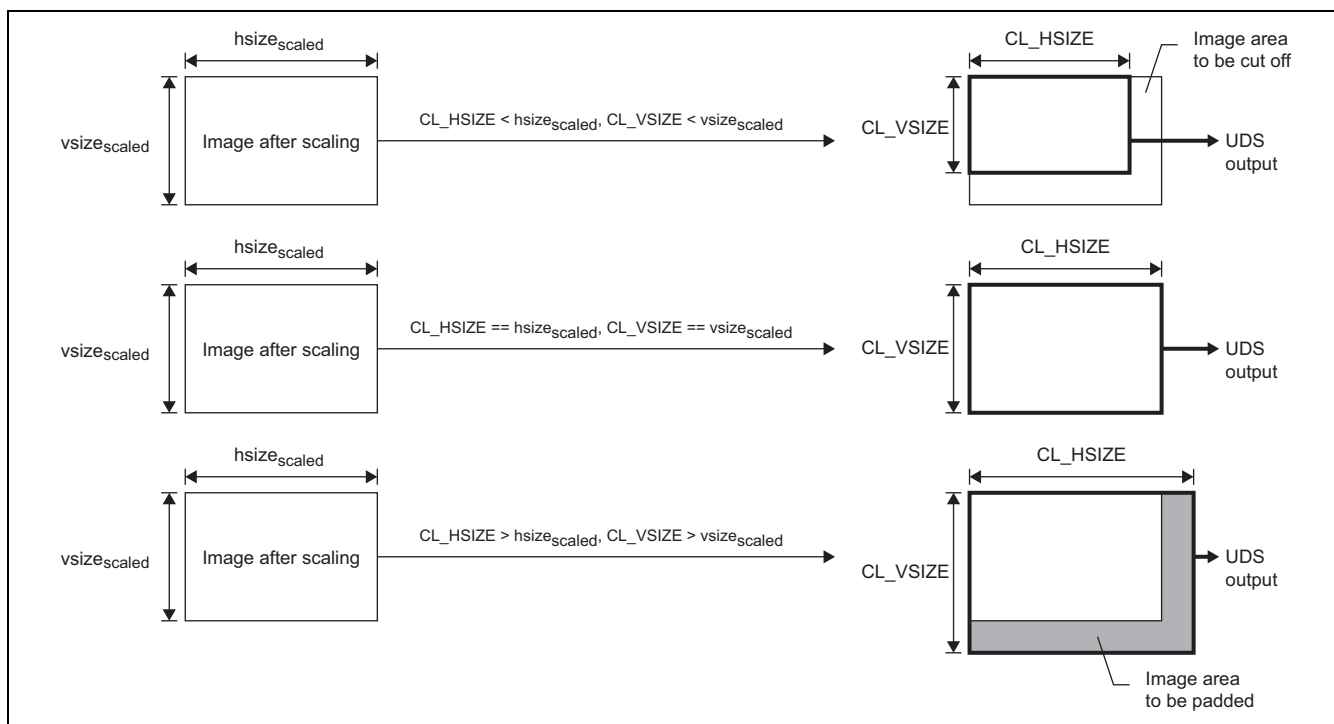
Bit	Bit Name	Initial Value	R/W	Description
31 to 28	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
27 to 16	CL_HSIZE [11:0]	H'000	R/W	Clipping Size of Horizontal Pixel Count after Scale-Up/-Down The horizontal width of an image output from the scaling filter is adjusted (clipped or padded) to match the pixel count set in the CL_HSIZE bits. The setting range is 4 to 2,048 in a scale-down operation (see Table 28.31) and 4 to 2,048 in a scale-up operation. These bits always have to be set when using the UDSn, regardless of the scale-up, scale-down, or no-scaling setting by the VI6_UDSn_SCALE register.
15 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11 to 0	CL_VSIZE [11:0]	H'000	R/W	Clipping Size of Vertical Pixel Count after Scale-Up/-Down The vertical width of an image output from the scaling filter is adjusted (clipped or padded) to match the pixel count set in the CL_VSIZE bits. The setting range is 4 to 2,048 in a scale-down operation (see Table 28.31) and 4 to 2,048 in a scale-up operation. These bits always have to be set when using the UDSn, regardless of the scale-up, scale-down, or no-scaling setting by the VI6_UDSn_SCALE register.

Figure 28.35 shows the configuration of the UDSn. The UDSn consists of a scaling filter and clipping circuit, such as the configuration shown in Figure 28.35. The scaling filter and clipping circuit are independent of each other.



**Figure 28.35 UDSn Configuration**

The size of the image actually output by the scaling filter (refer to section 28.2.11.2 for calculation) is determined from the size of the image input to the scaling filter and the VI6\_UDSn\_SCALE setting; that is, three types of image are output by the UDSn according to the relationship between the size of the image actually output from the scaling filter ( $hsize_{scaled}$  and  $vsize_{scaled}$ ) and this register setting as shown in Figure 28.36.



**Figure 28.36 UDS Output Image for Each CL\_HSIZE/VSIZE Setting**

When the settings of the CL\_HSIZE and CL\_VSIZE bits are smaller than the horizontal and vertical pixel counts ( $hsize_{scaled}$  and  $vsize_{scaled}$ ) actually output by the scaling filter, the upscaled/downscaled image is clipped to become the UDSn output image.

When the settings of the CL\_HSIZE and CL\_VSIZE bits are equal to the horizontal and vertical pixel counts ( $hsize_{scaled}$  and  $vsize_{scaled}$ ) actually output by the scaling filter, the image actually output by the scaling filter becomes the UDSn output image without change.

When the settings of the CL\_HSIZE and CL\_VSIZE bits are greater than the horizontal and vertical pixel counts ( $hsize_{scaled}$  and  $vsize_{scaled}$ ) actually output by the scaling filter, in order to obtain the UDSn output image, the image is padded in the mode set by VI6\_UDSn\_CTRL.FMD for the area in which the settings of the CL\_HSIZE and CL\_VSIZE bits have exceeded the number of pixels actually output by the scaling filter.

### 28.2.11.8 Color Fill Register (VI6\_UDSn\_FILL\_COLOR)

Note: See Table 28.15 for details on which RZ/G series products have which registers.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	RFILC [7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GFILC [7:0]								BFILC [7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 16	RFILC[7:0]	H'00	R/W	R/Cr Component of Fill Color A value from H'00 to H'FF can be specified.
15 to 8	GFILC[7:0]	H'00	R/W	G/Y Component of Fill Color A value from H'00 to H'FF can be specified.
7 to 0	BFILC[7:0]	H'00	R/W	B/Cb Component of Fill Color A value from H'00 to H'FF can be specified.

The scaling filter creates an upscaled/downscaled image based on the scaling factor settings of the VI6\_UDSn\_SCALE register. If the size of the upscaled/downscaled image created by the scaling filter smaller than the clipping size set in the VI6\_UDSn\_CLIP\_SIZE register (lowest case in Figure 28.36) while VI6\_UDSn\_CTRL.FMD is set to 1, the color specified by this register is used to fill the space until the clipping size is reached.

The  $\alpha$  value of the area to be padded by this register is dependent on VI6\_UDSn\_CTRL.FMD setting. When VI6\_UDSn\_CTRL.FMD is 0 (repetition), the pixel value at the right edge (bottom edge) of the image is repeated as the  $\alpha$  value. When VI6\_UDSn\_CTRL.FMD is 1 (color information of this register is used), the  $\alpha$  value is 0.

## 28.2.12 LUT Control Register

### 28.2.12.1 LUT Control Register (VI6\_LUT\_CTRL)

Note: See Table 28.15 for details on which RZ/G series products have which registers.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	LUT_EN
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	LUT_EN	0	R/W	1D-LUT Enable/Disable Enables or disables the 1D-LUT function by the LUT. When the 1D-LUT is used, the color component curve information needs to be set separately in the LUT table. For the LUT table settings, refer to section 28.3.1. 0: 1D-LUT function is disabled 1: 1D-LUT function is enabled

In the LUT, various image processing, such as curves with high operation load (e.g.,  $\gamma$  correction), negative-positive conversion, and gain adjustment of images, can be achieved by the data replacement processing by the 1D-LUT. As shown in Figure 28.37, the LUT replaces each component of the input pixel data using the set replacement table of 256 entries. For example, if the LUT is set as in Figure 28.38, when there is an input of 150, the data stored in address 150 of the 1D-LUT is read and output as the LUT output. Figure 28.38 shows a case in which the input and output become equal for convenience in explaining.

In the LUT settings shown in Figure 28.39, the input bits are reversed. This has the effect of negative-positive flipping. In Figure 28.40,  $\gamma$  correction ( $\gamma = 1.8$  is shown as an example) is possible. As described above, information to be set in the LUT indicates LUT processing characteristics. If the same value is set for each component in the LUT, an equal effect can be obtained for each component of the input image when it is processed. If the LUT is set with different characteristics for each component, the processing characteristics can be changed for each component.

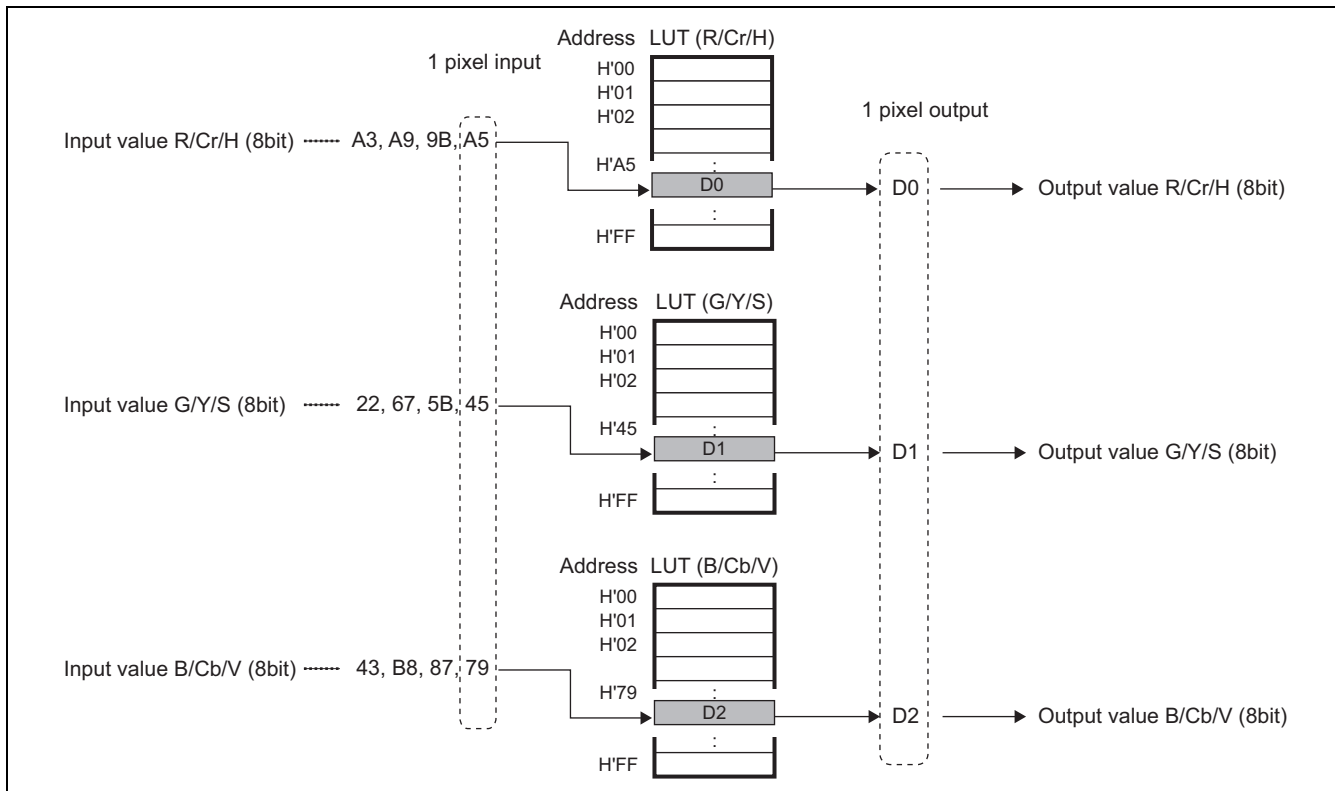


Figure 28.37 Relationship between Input and Output for 1D-LUT Table

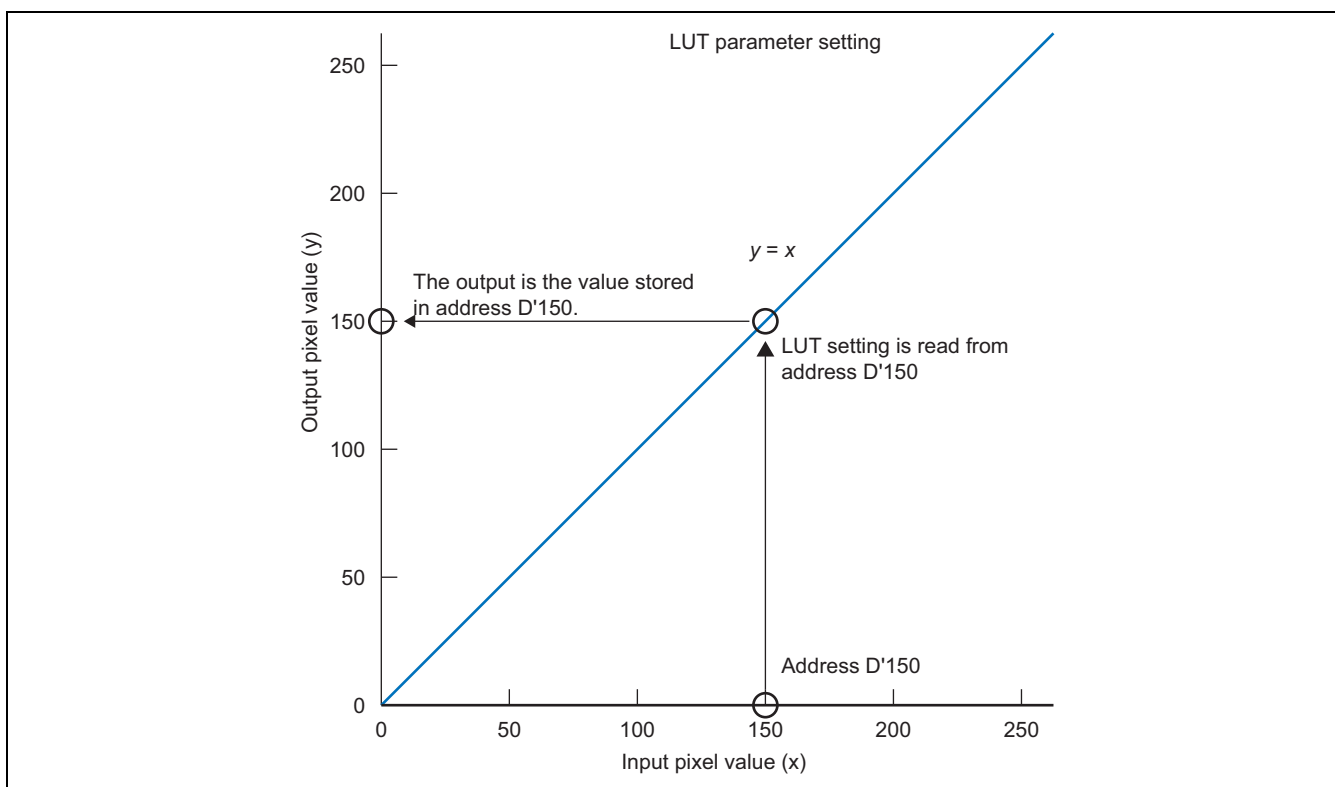


Figure 28.38 Setting Example in Which Output Becomes Equal to Input

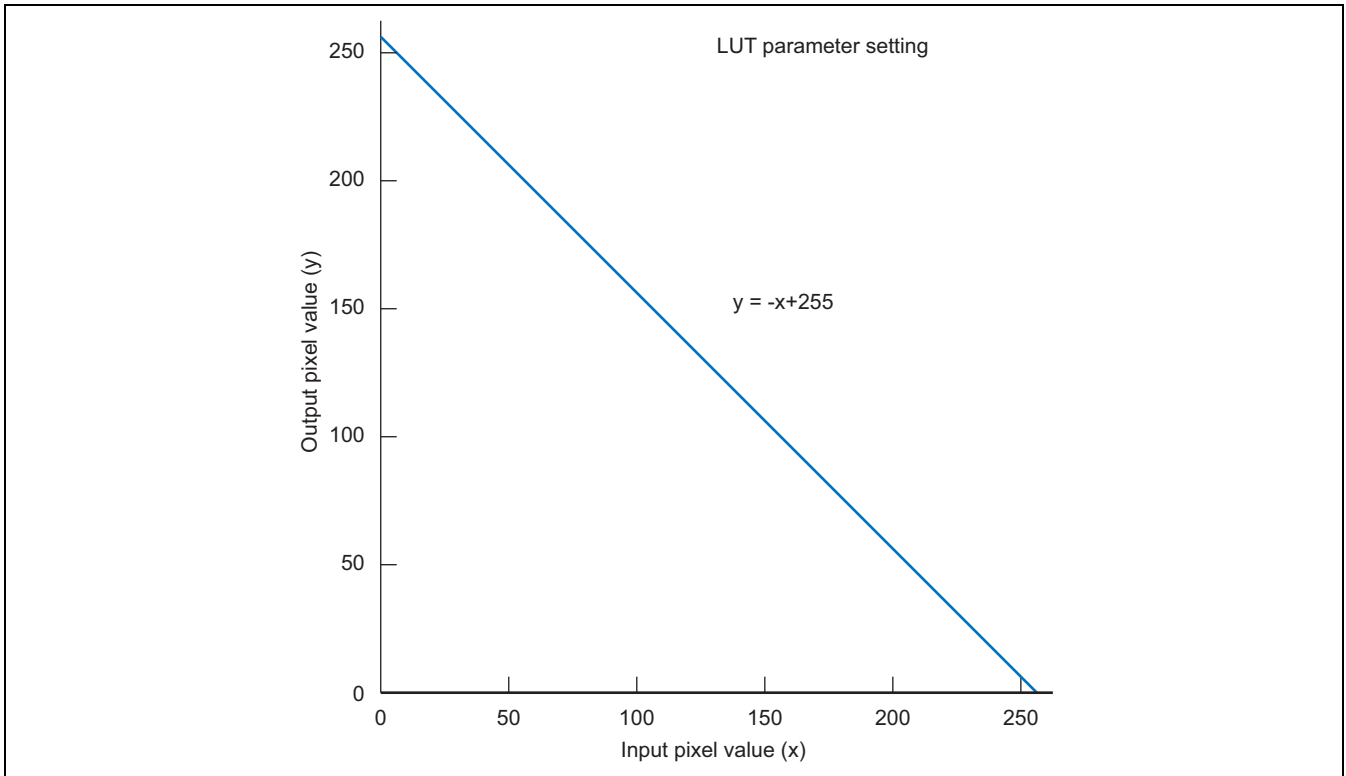


Figure 28.39 Setting Example of Negative-Positive Conversion

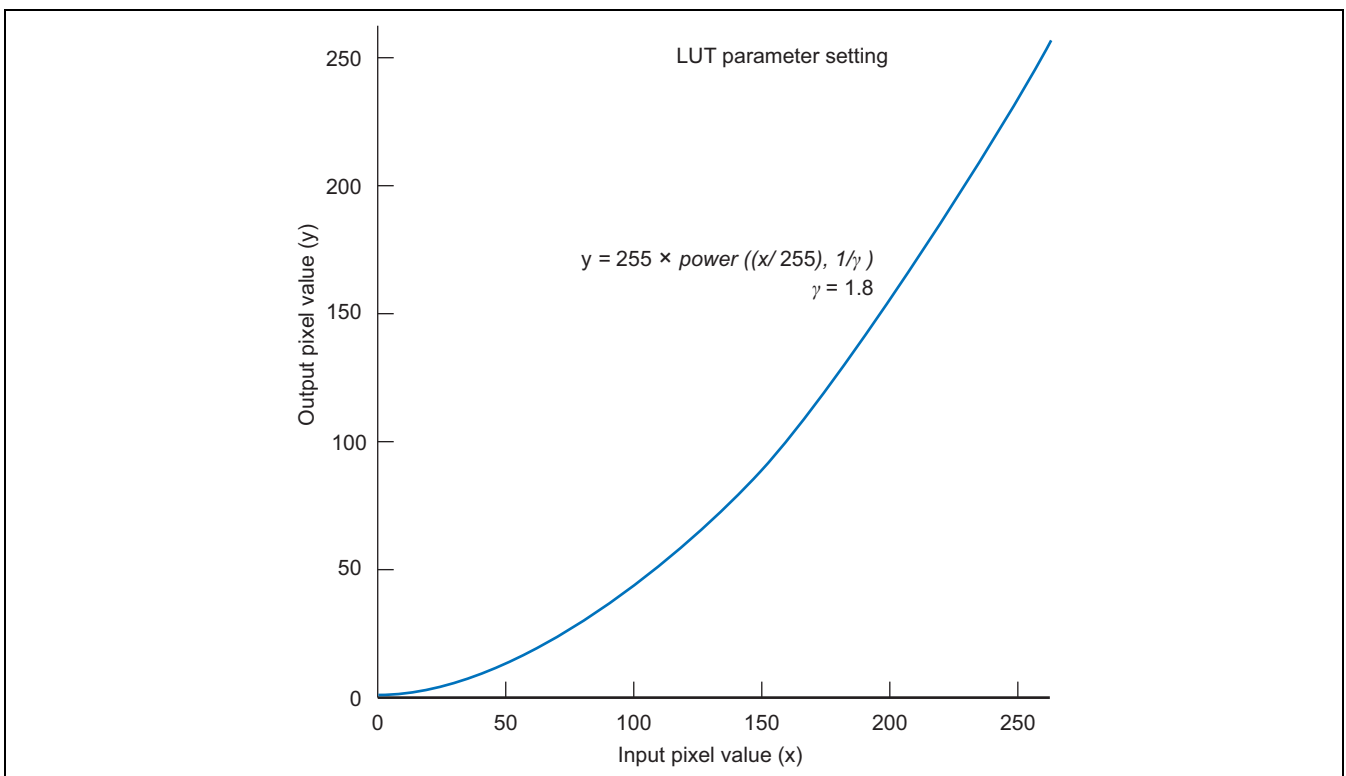


Figure 28.40 Setting Example of  $\gamma$  Correction



## 28.2.13 CLU Control Register

### 28.2.13.1 CLU Control Register (VI6\_CLU\_CTRL)

Note: See Table 28.15 for details on which RZ/G series products have which registers.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	AAI	—	—	—	MVS	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R	R	R	R/W	R	R	R	R	R	R	R	R

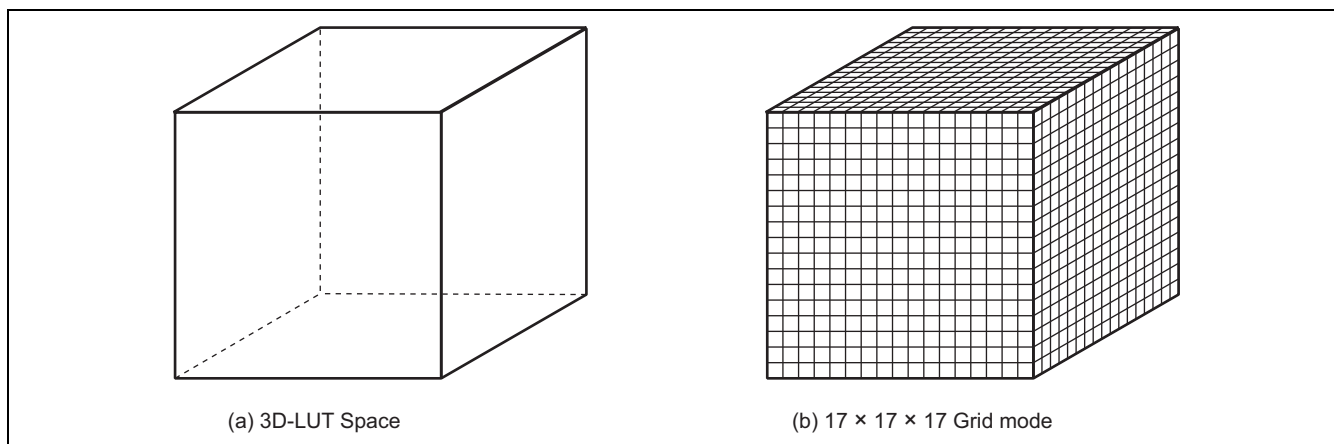
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	AX1I [1:0]		AX2I [1:0]		—	—	OS0 [1:0]		OS1 [1:0]		OS2 [1:0]		—	—	M2D	CLU_EN
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28	AAI	0	R/W	Automatic Table Address Increment Selects whether to specify the CLU table address in VI6_CLU_ADDR (refer to section 28.3.2) every time or update the address automatically. For details, refer to section 28.3.2. 0: CLU table address should be specified every time 1: CLU table address is automatically incremented
27 to 25	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
24	MVS	0	R/W	Max Value Stretch Select calculation method in max value region. 0: Method 0 (Lower compatible) 1: Method 1 (Improved characteristics)
23 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15, 14	AX1I [1:0]	00	R/W	Input Control 0 in 2D Mode When setting the M2D bit to 0, be sure to set these bits to 0. When setting the M2D bit to 1, be sure to set these bits to 3.
13, 12	AX2I [1:0]	00	R/W	Input Control 1 in 2D Mode When setting the M2D bit to 0, be sure to set these bits to 0. When setting the M2D bit to 1, be sure to set these bits to 1.
11, 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

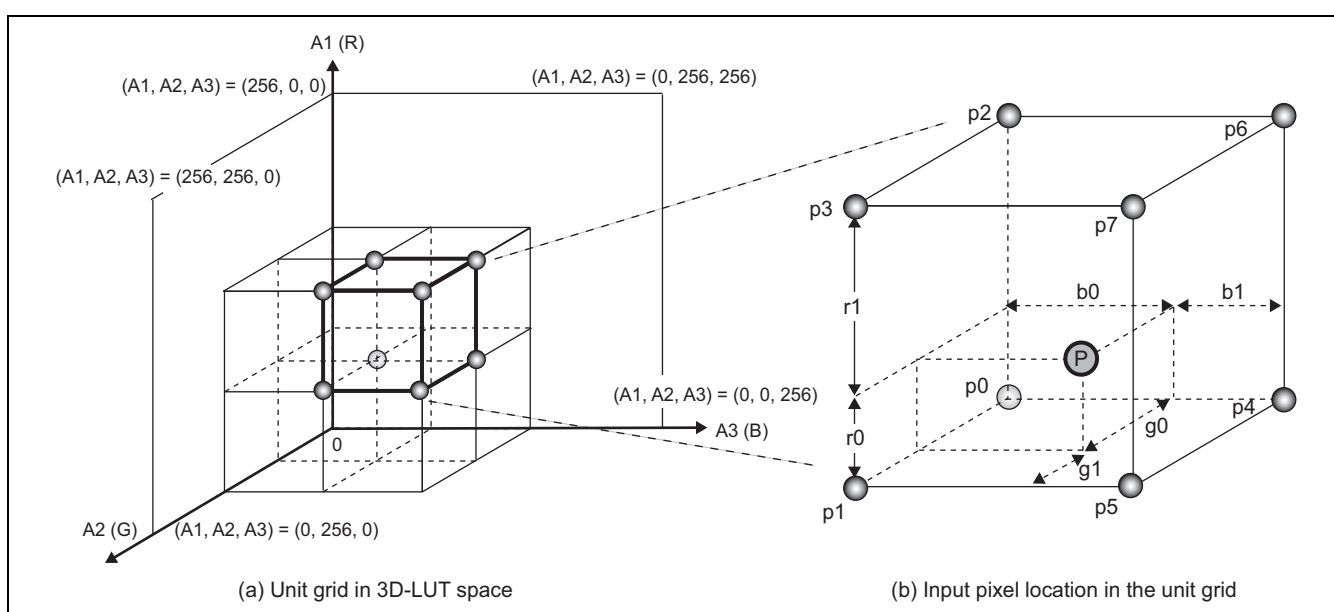
Bit	Bit Name	Initial Value	R/W	Description
9, 8	OS0 [1:0]	00	R/W	Output Control 0 in 2D Mode When setting the M2D bit to 0, be sure to set these bits to 0. When setting the M2D bit to 1, be sure to set these bits to 3.
7, 6	OS1 [1:0]	00	R/W	Output Control 1 in 2D Mode When setting the M2D bit to 0, be sure to set these bits to 0. When setting the M2D bit to 1, be sure to set these bits to 1.
5, 4	OS2 [1:0]	00	R/W	Output Control 2 in 2D Mode When setting the M2D bit to 0, be sure to set these bits to 0. When setting the M2D bit to 1, be sure to set these bits to 3.
3, 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	M2D	0	R/W	LUT Dimension Number Specifies the number of LUT dimensions. The details of each mode will be described later. 2D mode can be used only when the CLU input color space is YCbCr. 0: Operates in 3D mode 1: Operates in 2D mode
0	CLU_EN	0	R/W	CLU Processing Enable/Disable Enables or disables the 3D/2D color correction function by the CLU. When the CLU is used, the color component information needs to be set in the CLU table. For how to set data in the CLU table, see section 28.3.2. 0: CLU color correction is disabled 1: CLU color correction is enabled

The CLU handles three-dimensional or two-dimensional LUTs. A three-dimensional LUT is called a 3D-LUT and a two-dimensional LUT is called a 2D-LUT. The 3D or 2D operating mode of the CLU is selected by the M2D bit.

In 3D mode, a three-dimensional space such as that shown in Figure 28.41 (a) is considered. The total number of coordinate points that can exist in this three-dimensional space is the total number of combinations of input data. For the CLU, this becomes the cube of each 8-bit component (= 16,777,216 points). Since it is impractical to have table values (= table memory) for the same number of these coordinate points, the CLU divides the three-dimensional space of Figure 28.41 (a) into grids as shown in Figure 28.41 (b) in 3D mode. The apex in each divided grid is defined as the coordinate point in the three-dimensional space, and a table value with three component values is set for all of these coordinate points. The total number of coordinate points in Figure 28.41 (b) is  $173 = 4,913$ . For the method of setting the table value for these 4,913 points, refer to section 28.3.2.



**Figure 28.41 Concept and Division Count of a 3-Dimensional LUT**



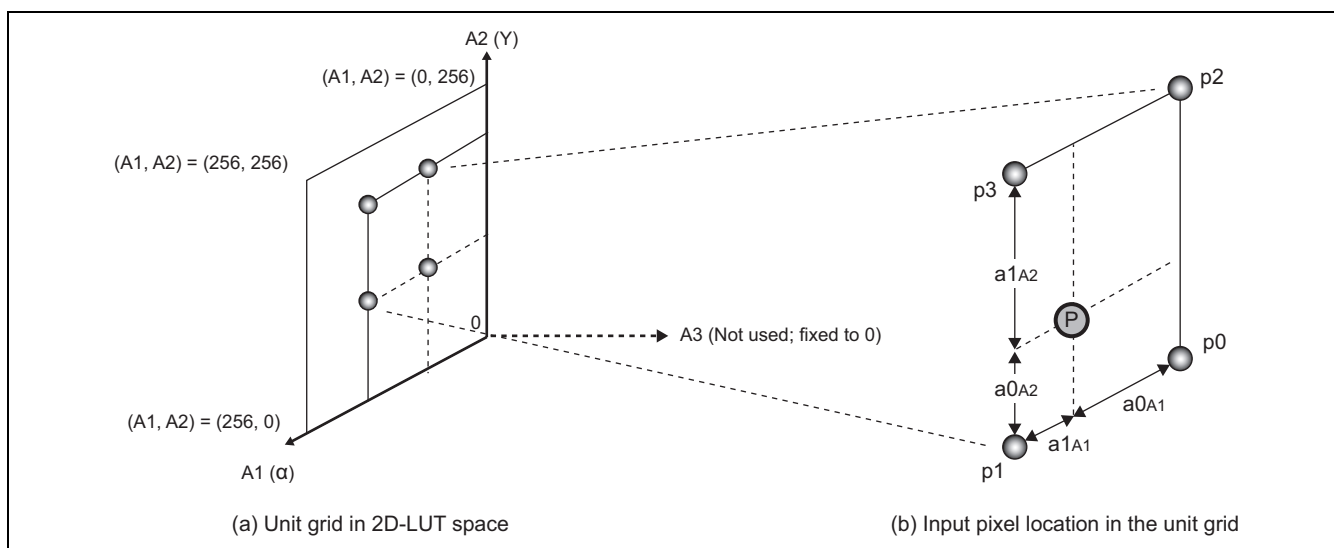
**Figure 28.42 Conceptual Diagram of LUT Space When CLU Is in 3D Mode**

To express a three-dimensional space such as that shown in Figure 28.41, consider the three-dimensional coordinates and axes shown in Figure 28.42 and define the minimum value and maximum value of each axis as 0 and 256, respectively. In 3D-LUT operation, the CLU forcibly assigns the four components of input data ( $\alpha$ , R/Cr/H, G/Y/S, and B/Cb/V) to axes: R, Cr, and H components to the first axis (A1), G, Y, and S components to the second axis (A2), and B, Cb, and V components to the third axis (A3). (The case of 2D mode is described later.) Among multiple components assigned to each axis (e.g., R, Cr, and H components for the first axis), one component is selected according to the format of the data input to the CLU. For example, when the color space of the data input to the CLU is RGB, the first axis (A1) shows the R component, the second axis (A2) shows the G component, and the third axis (A3) shows the B component. In a YCbCr color space, the first axis (A1) shows the Cr component, the second axis (A2) shows the Y component, and the third axis (A3) shows the Cb component.

Each component value of the CLU input data becomes a value on each axis. Since the input data ranges from 0 to 255, the maximum value of 256 is handled as a virtual point in a grid space like that shown in Figure 28.41. In a case where the coordinates obtained by plotting the values of the input three components on axes are exactly on a grid point (e.g.,  $p_0$  in Figure 28.42 (b)), the 3-component value of the table value ( $p_0$ ) set to that location becomes the CLU output. If the input value of the three components result in an intermediate location between grid points and not on a grid point, such as position P in Figure 28.42 (b), value P of the three components is interpolated from the table values ( $p_0$  to  $p_7$  in Figure 28.42 (b)) for the eight surrounding grid points and this is used as the CLU output.

By setting arbitrary table value for a three-dimensional LUT space (three-dimensional color space) such as that shown in Figure 28.41 using the processing described above, not only color conversion or color correction for the entire color space, but color conversion or color correction (memory color correction, skin smoothing, etc.) for a particular color area can be achieved.

Next, a 2D-LUT that is used when the CLU is operating in 2D mode is described (M2D bit should be set to 1 for operation in 2D mode). 2D-LUT mode is similar to 3D-LUT mode. However, since the axes for selecting the LUT become two-dimensional, the concept of a 3D-LUT space illustrated in Figure 28.42 changes to a 2D-LUT space like that shown in Figure 28.43.



**Figure 28.43 Conceptual Diagram of LUT Space when CLU is in 2D Mode**

As shown in Figure 28.43 (a), the first axis (A1) and second axis (A2) are used, and the A1-A2 plane becomes the LUT space in 2D mode. Because the third axis (A3) is not used, the CLU always handles the value on the A3 axis as 0.

2D mode can be used only when the CLU input is in the YCbCr color space. The input value of axis A1 is the input  $\alpha$  value of the CLU, and the input value of axis A2 is the input luminance Y of the CLU. If the coordinates in the 2D-LUT space which were determined by the input values are exactly on a grid point (e.g., p2 in Figure 28.43 (b)), the table value (p2) set to that location becomes the output value of the 2D-LUT. If the input 2-component value exists at an intermediate location between grid points and not on a grid point, such as position P in Figure 28.43 (b), value P is interpolated from the table values (p0 to p3 in Figure 28.43 (b)) for the four surrounding grid points and this is used as the 2D-LUT output. The interpolated component of the second axis of the 2D-LUT output acquired in this manner becomes the Y component output of the CLU. In 2D mode, the Cb/Cr component is a pass-through output.

For the CLU table values in Figure 28.43 in 2D mode, set a value for only the component value of the second axis, and set 0 for the component values of the first and third axes. For details on the setting method, see section 28.3.2.

## 28.2.14 HST Control Register

### 28.2.14.1 HST Control Register (VI6\_HST\_CTRL)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	HST_EN
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	HST_EN	0	R/W	HSV Conversion (RGB → HSV) Enable/Disable Enables or disables RGB → HSV conversion. H indicates hue, S indicates saturation, and V indicates a value (brightness). 0: RGB → HSV conversion is disabled 1: RGB → HSV conversion is enabled

Various color correction processing can be applied to HSV-format images by combining the 1D-LUT and 3D-LUT. For details on the 1D-LUT and 3D-LUT, see sections 28.2.12.1 and 28.2.13.1.

To return HSV-converted data to RGB data, HSV → RGB conversion is used (see section 28.2.15.1). RGB ↔ HSV conversion causes an operation error. Therefore, even when only just performing conversion of RGB → HSV → RGB, the original RGB value and converted RGB value will not completely match.

## 28.2.15 HSI Control Register

### 28.2.15.1 HSI Control Register (VI6\_HSI\_CTRL)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	HSI_EN
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	HSI_EN	0	R/W	Reversed HSV Conversion (HSV → RGB) Enable/Disable Enables or disables HSV → RGB conversion to return HSV data that was converted by HSV conversion (see section 28.2.14.1) back to RGB data. 0: HSV → RGB conversion is disabled 1: HSV → RGB conversion is enabled

RGB ↔ HSV conversion causes an operation error. Therefore, even when only just performing conversion of RGB → HSV → RGB, the original RGB value and converted RGB value will not completely match.

## 28.2.16 BRU Control Registers

### 28.2.16.1 BRU Input Control Register (VI6\_BRU\_INCTRL)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	NRM	—	—	—	—	—	—	—	—	D3ON	D2ON	D1ON	D0ON
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	DITH3 [2:0]			—	DITH2 [2:0]			—	DITH1 [2:0]			—	DITH0 [2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W

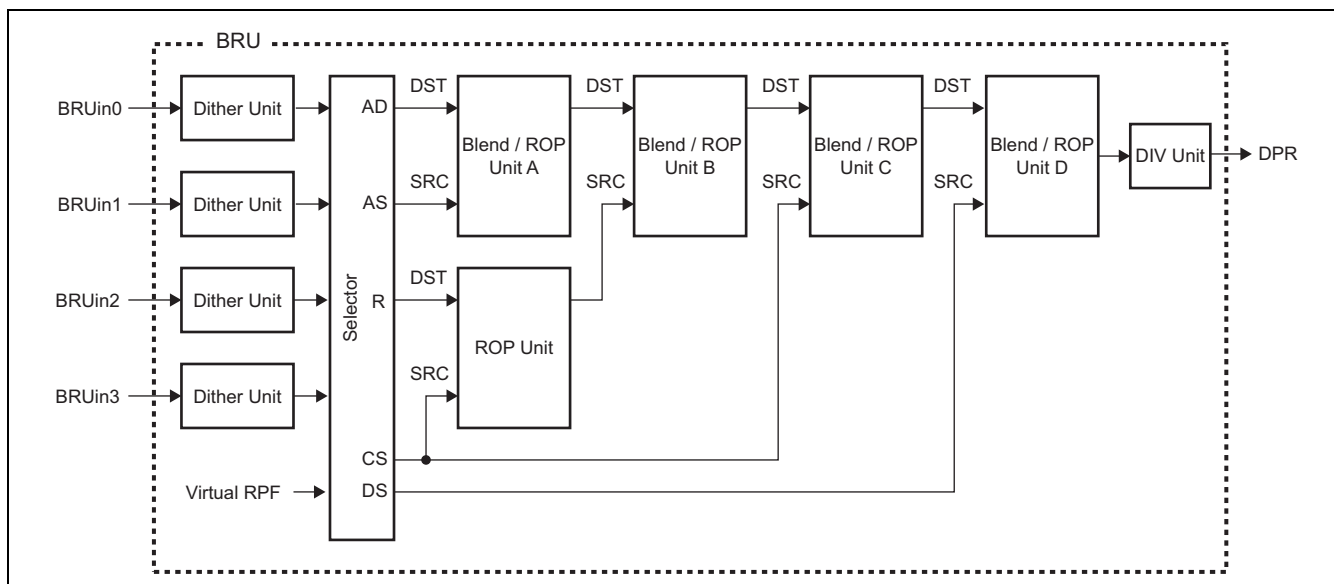
Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28	NRM	0	R/W	Color Data Normalization Enables or disables division by the $\alpha$ value of the color data in BRU blending operation. This is used when converting the RGB color data format to which the $\alpha$ value is multiplied (premultiplied color) into the RGB color data format to which the $\alpha$ value is not multiplied (non-premultiplied color). Do not use this for the YCbCr format. 0: Divider (DIV unit in Figure 28.44) does not divide the color value by $\alpha$ 1: Divider (DIV unit in Figure 28.44) divides the color value by $\alpha$
27 to 20	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
19	D3ON	0	R/W	Dithering Enable of BRU Input 3 Enables or disables dithering (color reduction) of BRU input 3 (BRUin3 in Figure 28.44). 0: Dithering of BRUin3 is disabled 1: Dithering of BRUin3 is enabled
18	D2ON	0	R/W	Dithering Enable of BRU Input 2 Enables or disables dithering (color reduction) of BRU input 2 (BRUin2 in Figure 28.44). 0: Dithering of BRUin2 is disabled 1: Dithering of BRUin2 is enabled
17	D1ON	0	R/W	Dithering Enable of BRU Input 1 Enables or disables dithering (color reduction) of BRU input 1 (BRUin1 in Figure 28.44). 0: Dithering of BRUin1 is disabled 1: Dithering of BRUin1 is enabled

Bit	Bit Name	Initial Value	R/W	Description
16	D0ON	0	R/W	Dithering Enable of BRU Input 0 Enables or disables dithering (color reduction) of BRU input 0 (BRUin0 in Figure 28.44). 0: Dithering of BRUin0 is disabled 1: Dithering of BRUin0 is enabled
15	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
14 to 12	DITH3 [2:0]	000	R/W	Dithering of CH3 Input to BRU These bits specify the number of colors for pixels after dithering (color reduction) when dithering (color reduction) for pixel information is enabled through the D3ON bit. When dithering (color reduction) for pixel information is disabled, specify 0 in these bits. 000: Dithering of BRUin3 input image is disabled 001: Dithering of BRUin3 input image at 18 bpp (RGB666: 262,144 colors) 010: Dithering of BRUin3 input image at 16 bpp (RGB565: 65,536 colors) 011: Dithering of BRUin3 input image at 15 bpp (RGB555: 32,768 colors) 100: Dithering of BRUin3 input image at 12 bpp (RGB444: 4,096 colors) 101: Dithering of BRUin3 input image at 8 bpp (RGB332: 256 colors) 110, 111: Setting prohibited
11	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
10 to 8	DITH2 [2:0]	000	R/W	Dithering of CH2 Input to BRU These bits specify how to perform dithering of the CH2 input to the BRU. The setting method is the same as that for the DITH3 bits. Read the description of the DITH3 bits with BRUin2 and D2ON replacing BRUin3 and D3ON, respectively.
7	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
6 to 4	DITH1 [2:0]	000	R/W	Dithering of CH1 Input to BRU These bits specify how to perform dithering of the CH1 input to the BRU. The setting method is the same as that for the DITH3 bits. Read the description of the DITH3 bits with BRUin1 and D1ON replacing BRUin3 and D3ON, respectively.
3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
2 to 0	DITH0 [2:0]	000	R/W	Dithering of CH0 Input to BRU These bits specify how to perform dithering of the CH0 input to the BRU. The setting method is the same as that for the DITH3 bits. Read the description of the DITH3 bits with BRUin0 and D0ON replacing BRUin3 and D3ON, respectively.

Figure 28.44 shows the configuration of the BRU. For the BRU inputs, there are four inputs from the DPR and one internal input as a virtual RPF. BRUin0 to BRUin3 are input ports that have the target node values shown in Figure 28.33, and they can be connected to any module on the DPR. The same color space (YCbCr or RGB) has to be used for the four inputs from the DPR to the BRU.



The virtual RPF inside the BRU is an input unit not connected to the DPR. It is called the "virtual RPF" because it outputs images internally created by the BRU. Starting of the virtual RPF is controlled by VI6\_WPFn\_SRCRPF.VIR\_ACT, and the single-color data created at the virtual RPF can be used for blending or raster operation (ROP) with data from the other input units BRUin0 to BRUin3. The color space for the single color to be set for the virtual RPF needs to match the color space of the four inputs from the DPR to the BRU. For this setting method, see section 28.2.16.4.



**Figure 28.44 BRU Configuration**

The selector in Figure 28.44 is used to select the SRC and DST inputs to blending/ROP units A to D and the ROP unit from BRUin0 to BRUin3 which are inputs from the DPR and the virtual RPF. The SRC and DST input sources for blending/ROP units A to D and the ROP unit are either uniquely determined based on the configuration shown in Figure 28.44 (Table 28.33) or selected as desired by registers. The input sources that can be arbitrarily selected by registers are AD, AS, R, CS, and DS, which correspond to the registers shown in Table 28.34.

**Table 28.33 SRC and DST with Unique Input Sources**

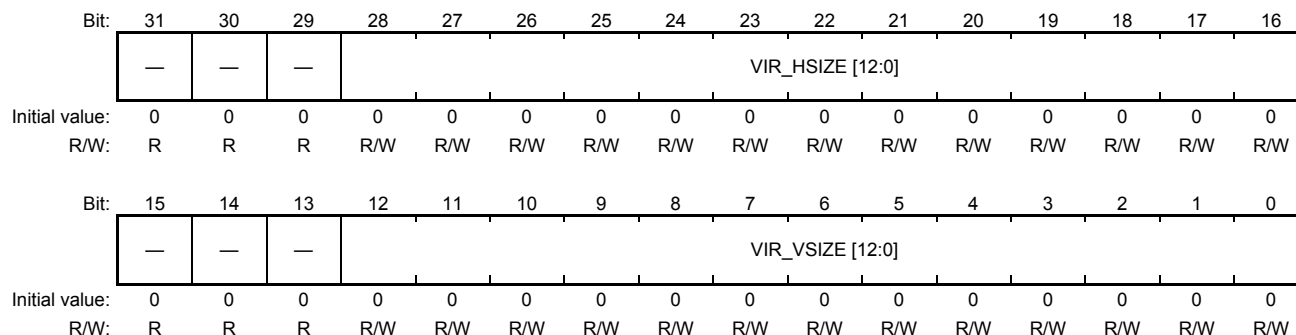
Input	Input Source	Register Bits
Blending/ROP unit B - DST	Output from blending/ROP unit A	—
Blending/ROP unit B - SRC	Output from ROP unit	—
Blending/ROP unit C - DST	Output from blending/ROP unit B	—
Blending/ROP unit D - DST	Output from blending/ROP unit C	—
ROP unit - SRC	CS which is a selector output	VI6_BRUC_CTRL.SRCSEL

**Table 28.34 Correspondence between Selector Output Destinations and Register Bits**

Selector Output	Output Destination	Register Bits
AD	Blending/ROP unit A - DST	VI6_BRUA_CTRL.DSTSEL
AS	Blending/ROP unit A - SRC	VI6_BRUA_CTRL.SRCSEL
R	ROP unit - DST	VI6_BRU_ROP.DSTSEL
CS	Blending/ROP unit C - SRC	VI6_BRUC_CTRL.SRCSEL
DS	Blending/ROP unit D - SRC	VI6_BRUD_CTRL.SRCSEL

### 28.2.16.2 Size Register of BRU Input Virtual RPF (VI6\_BRU\_VIRRPF\_SIZE)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√



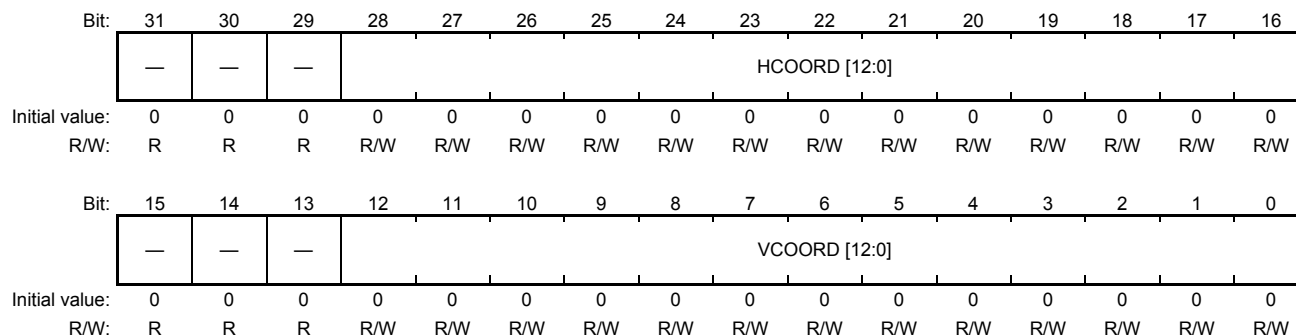
Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28 to 16	VIR_HSIZE [12:0]	H'0000	R/W	Virtual RPF Horizontal Size These bits set the horizontal size of an image from the virtual RPF shown in Figure 28.44. A value from 1 to 8,190 can be specified.
15 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12 to 0	VIR_VSIZE [12:0]	H'0000	R/W	Virtual RPF Vertical Size These bits set the vertical size of an image from the virtual RPF shown in Figure 28.44. A value from 1 to 8,190 can be specified.

The virtual RPF has only a function to output a fixed  $\alpha$  value and a fixed pixel value. The virtual RPF can internally create a single-color image without accessing external memory via the MAU. Same as images from the other BRU input ports, a sub layer can be blended on an image created in this manner with the image used as the background (master layer). In turn, when using the image as a sub layer, it can be drawn on the master layer as a window.

Note that the virtual RPF is fixed to input port 5 of the BRU, and the data path route cannot be changed by the DPR.

### 28.2.16.3 Display Location Register of BRU Input Virtual RPF (VI6\_BRU\_VIRRPF\_LOC)

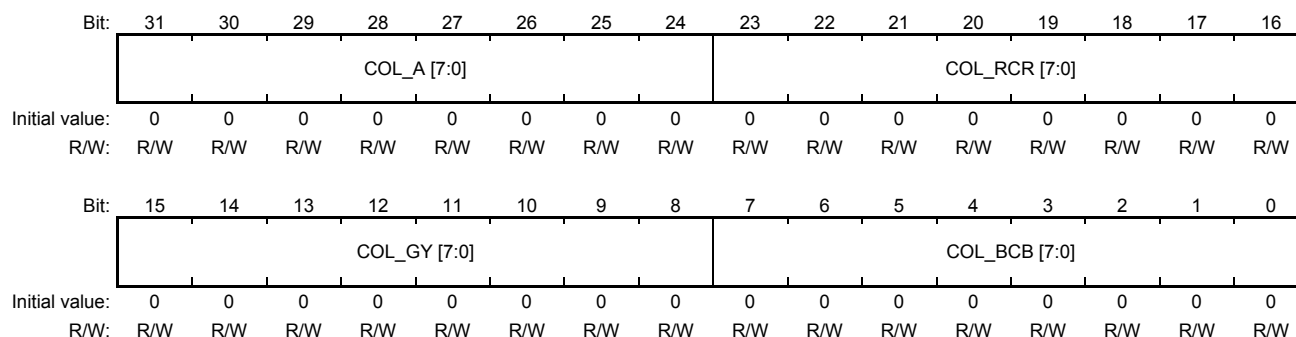
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√



Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28 to 16	HCOORD [12:0]	H'0000	R/W	Horizontal Coordinate of Virtual RPF Location on Master Layer These bits specify the horizontal coordinate of where to locate the left-edge pixel of the virtual RPF's layer, with the left-edge pixel of the master layer set at coordinate 0. This setting should be made in pixel units. A value from 0 to 8,189 can be specified. When the virtual RPF is specified as the master layer by VI6_WPFn_SRCRPF.VIR_ACT, set these bits to 0.
15 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12 to 0	VCOORD [12:0]	H'0000	R/W	Vertical Coordinate of Virtual RPF Location on Master Layer These bits specify the vertical coordinate of where to locate the top-edge pixel of the virtual RPF's layer, with the top-edge pixel of the master layer set at coordinate 0. This setting should be made in pixel units. A value from 0 to 8,189 can be specified. When the virtual RPF is specified as the master layer by VI6_WPFn_SRCRPF.VIR_ACT, set these bits to 0.

### 28.2.16.4 Color Information Register of BRU Input Virtual RPF (VI6\_BRU\_VIRRPF\_COL)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	COL_A[7:0]	H'00	R/W	Fixed $\alpha$ of Virtual RPF These bits set the fixed $\alpha$ value when the virtual RPF creates a virtual plane. A value from 0 to 255 can be specified.
23 to 16	COL_RCR [7:0]	H'00	R/W	Fixed R/Cr of Virtual RPF These bits set the fixed R/Cr value when the virtual RPF creates a virtual plane. A value from 0 to 255 can be specified.
15 to 8	COL_GY [7:0]	H'00	R/W	Fixed G/Y of Virtual RPF These bits set the fixed G/Y value when the virtual RPF creates a virtual plane. A value from 0 to 255 can be specified.
7 to 0	COL_BCB [7:0]	H'00	R/W	Fixed B/Cb of Virtual RPF These bits set the fixed B/Cb value when the virtual RPF creates a virtual plane. A value from 0 to 255 can be specified.

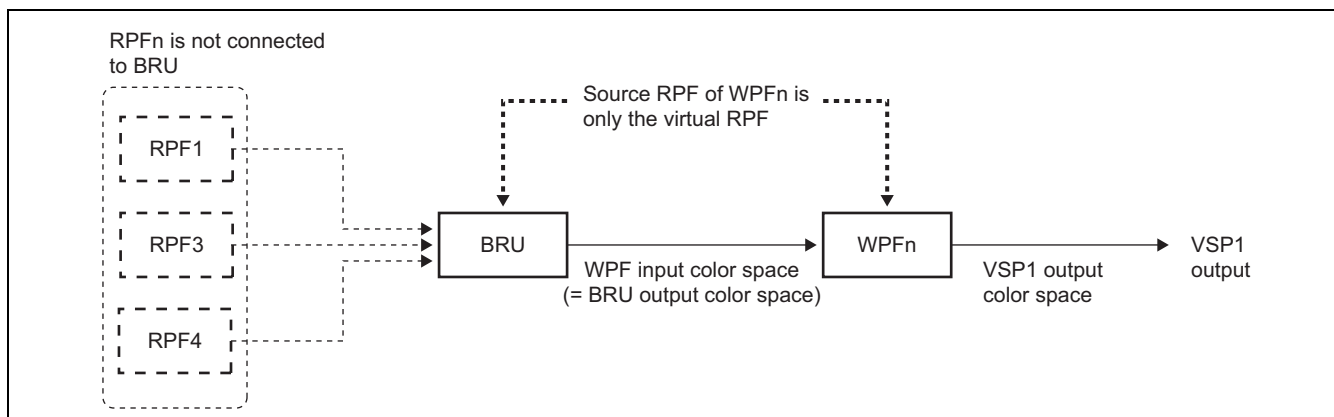
The transparency information and color information of the single color that is created by the virtual RPF are set in the bits of this register. As described earlier, the color information is set for the YCbCr or RGB color space. The color space to be set in this register depends on the register settings of the environment and other modules to which the BRU is connected by the DPR. Two cases can be considered. Since the  $\alpha$  value (COL\_A) is transparency information and irrelevant to the concept of color space, the same setting is made for either the YCbCr or RGB color space.

#### (Case 1: When an input other than the virtual RPF is used)

When the source RPF is connected to any one of the BRU input ports (BRUin0 to BRUin3) other than the virtual RPF and valid data is being supplied, the same color space data as the color space for the BRU inputs should be set in this register as the color space for the virtual RPF's color information. This is based on the restriction of "all BRU inputs must have the same color space", as described in section 28.2.9.1 or 28.2.16.1.

#### (Case 2: When only the virtual RPF is used)

When only the virtual RPF is used as the source RPF of WPFn, RPFn is not connected to the BRU, as shown in Figure 28.45. Thus, there is no color space for another input that the color space for the virtual RPF has to follow, as in case 1. This means that the color space of the data output by the BRU is determined by the WPF setting.



**Figure 28.45 Relationship between DPR Connection and Color Space when Only Virtual RPF is Used**

As shown in Figure 28.45, the output color space of the VSP1 (= output color space of WPFn) is determined by VI6\_WPFn\_OUTFMT.WRFMT. When bit 6 in VI6\_WPFn\_OUTFMT.WRFMT (WRFMT[6]) is 0, the color space is RGB, while when it is 1, the color space is YCbCr. Next, the WPF input color space (= BRU output color space) is determined by the relationship between the WPF output color space and VI6\_WPFn\_OUTFMT.CSC. When VI6\_WPFn\_OUTFMT.CSC is 0, the WPF output color space and WPF input color space (= BRU output color space) are the same. When VI6\_WPFn\_OUTFMT.CSC is 1, the WPF output color space and WPF input color space (= BRU output color space) are the opposite. This relationship is summarized in Table 28.35.

The color space for the virtual RPF's color information should be set in this register according to the "BRU output color space" shown in Table 28.35.

**Table 28.35 Relationship between WPF Output Color Space and BRU Output Color Space**

VI6_WPFn_OUTFMT Register Bit Settings		BRU Output Color Space (= WPF Input Color Space)	
Bit 6 in WRFMT	CSC		
0 (WPF output is RGB)	0 (YCbCr → RGB conversion is disabled)	RGB	
0 (WPF output is RGB)	1 (YCbCr → RGB conversion is enabled)	YCbCr	
1 (WPF output is YCbCr)	0 (RGB → YCbCr conversion is disabled)	YCbCr	
1 (WPF output is YCbCr)	1 (RGB → YCbCr conversion is enabled)	RGB	

### 28.2.16.5 BRU Control Registers (VI6\_BRUm\_CTRL: m = A, B, C, D)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	RBC	—	—	—	—	—	—	—	—	DSTSEL [2:0]			—	SRCSEL [2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	CROP [3:0]			AROP [3:0]				
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	RBC	0	R/W	<p>Operation Type of Blending/ROP Unit m (m = A, B, C, D)</p> <p>Specifies the operation type for blending/ROP unit m (m = A, B, C, D) shown in Figure 28.44.</p> <p>0: ROP (raster operation)</p> <p>1: Blending operation</p>
30 to 23	—	All 0	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>
22 to 20	DSTSEL[2:0]	000	R/W	<p>Input Selection for DST Side of Blending/ROP Unit A</p> <p>These bits select the input for the DST side of blending/ROP unit A shown in Figure 28.44. These bits specify the connection between the BRU input port and the DST separately from the setting of connections between other modules and the BRU input port through the DPR.</p> <p>000: BRU input 0 (BRUin0) is input to DST</p> <p>001: BRU input 1 (BRUin1) is input to DST</p> <p>010: BRU input 2 (BRUin2) is input to DST</p> <p>011: BRU input 3 (BRUin3) is input to DST</p> <p>100: Virtual RPF is input to DST</p> <p>101 to 111: Setting prohibited</p> <p>Note: The DSTSEL bits for blending/ROP unit m (m = B, C, D) are reserved according to Table 28.33. The write value should always be 0.</p>
19	—	0	R	<p>Reserved</p> <p>This bit is always read as 0. The write value should always be 0.</p>

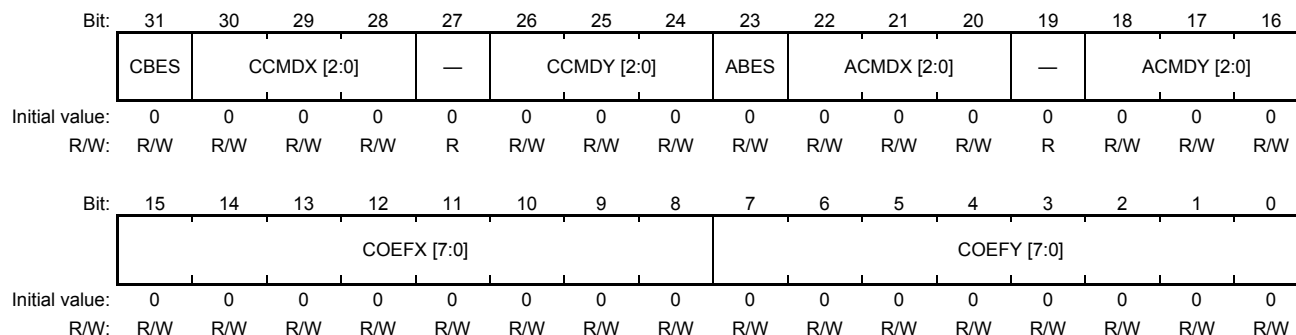
Bit	Bit Name	Initial Value	R/W	Description
18 to 16	SRCSEL[2:0]	000	R/W	<p>Input Selection for SRC Side of Blending/ROP Unit m (m = A, C, D)</p> <p>These bits select the input for the SRC side of blending/ROP unit m (m = A, C, D) shown in Figure 28.44. These bits specify the connection between the BRU input port and the SRC separately from the setting of connections between other modules and the BRU input port through the DPR.</p> <p>000: BRU input 0 (BRUin0) is input to SRC            001: BRU input 1 (BRUin1) is input to SRC            010: BRU input 2 (BRUin2) is input to SRC            011: BRU input 3 (BRUin3) is input to SRC            100: Virtual RPF is input to SRC            101 to 111: Setting prohibited</p> <p>Note: The SRCSEL bits for blending/ROP unit B are reserved according to Table 28.33. The write value should always be 0.</p>
15 to 8	—	All 0	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>
7 to 4	CROP[3:0]	0000	R/W	<p>Color Data ROP Operator</p> <p>These bits select the ROP operator of the color data in blending/ROP unit m (m = A, B, C, D). Select the opcode for ROP operation from Table 28.36.</p>
3 to 0	AROP[3:0]	0000	R/W	<p><math>\alpha</math> Data ROP Operator</p> <p>These bits select the ROP operator of the <math>\alpha</math> data in blending/ROP unit m (m = A, B, C, D). Select the opcode for ROP operation from Table 28.36.</p>

**Table 28.36 ROP Operator of Blending/ROP Unit m (m = A, B, C, D)**

Opcode	Operator
B'0000	NOP(D)
B'0001	AND(S & D)
B'0010	AND_REVERSE(S & ~D)
B'0011	COPY(S)
B'0100	AND_INVERTED(~S & D)
B'0101	CLEAR(0)
B'0110	XOR(S ^ D)
B'0111	OR(S   D)
B'1000	NOR(~(S   D))
B'1001	EQUIV(~(S ^ D))
B'1010	INVERT(~D)
B'1011	OR_REVERSE(S   ~D)
B'1100	COPY_INVERTED(~S)
B'1101	OR_INVERTED(~S   D)
B'1110	NAND(~(S & D))
B'1111	SET(all1)

### 28.2.16.6 BRU Blend Control Registers (VI6\_BRUm\_BLD: m = A, B, C, D)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√



Bit	Bit Name	Initial Value	R/W	Description
31	CBES	0	R/W	Blending Expression Selection Selects the blending expression of the color data in the BRU (VI6_BRUm_CTRL.RBC = 1). Blending coefficients are specified by the CCMDX and CCMDY bits. 0: $CCMDX \times (DST \text{ color data}) + CCMDY \times (SRC \text{ color data})$ 1: $CCMDX \times (DST \text{ color data}) - CCMDY \times (SRC \text{ color data})$
30 to 28	CCMDX[2:0]	000	R/W	Blending Coefficient X Selection These bits specify coefficient X used in the blending expression determined by the CBES bit. 000: DST $\alpha$ data is used as blending coefficient X 001: $255 - (DST \alpha \text{ data})$ is used as blending coefficient X 010: SRC $\alpha$ data is used as blending coefficient X 011: $255 - (SRC \alpha \text{ data})$ is used as blending coefficient X 100: Fixed $\alpha$ value 0 (COEFX setting)
27	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
26 to 24	CCMDY[2:0]	000	R/W	Blending Coefficient Y Selection These bits specify coefficient Y used in the blending expression determined by the CBES bit. 000: DST $\alpha$ data is used as blending coefficient Y 001: $255 - (DST \alpha \text{ data})$ is used as blending coefficient Y 010: SRC $\alpha$ data is used as blending coefficient Y 011: $255 - (SRC \alpha \text{ data})$ is used as blending coefficient Y 100: Fixed $\alpha$ value 1 (COEFY setting)
23	ABES	0	R/W	Blending $\alpha$ Creation Expression Specifies the expression for creating $\alpha$ data after blending by blending/ROP unit m (m = A, B, C, D). $\alpha$ creation coefficients are specified by the ACMDX and ACMDY bits. 0: $ACMDX \times (DST \alpha \text{ data}) + ACMDY \times (SRC \alpha \text{ data})$ 1: $ACMDX \times (DST \alpha \text{ data}) - ACMDY \times (SRC \alpha \text{ data})$



Bit	Bit Name	Initial Value	R/W	Description
22 to 20	ACMDX[2:0]	000	R/W	<p><math>\alpha</math> Creation Coefficient X</p> <p>These bits specify <math>\alpha</math> creation coefficient X used in the <math>\alpha</math> creation expression determined by the ABES bit.</p> <p>000: (<math>\alpha</math> creation coefficient X) = (DST <math>\alpha</math> data)            001: (<math>\alpha</math> creation coefficient X) = 255 – (DST <math>\alpha</math> data)            010: (<math>\alpha</math> creation coefficient X) = (SRC <math>\alpha</math> data)            011: (<math>\alpha</math> creation coefficient X) = 255 – (SRC <math>\alpha</math> data)            100: (<math>\alpha</math> creation coefficient X) = Fixed <math>\alpha</math> value 0 (COEFX setting)            101 to 111: Setting prohibited</p>
19	—	0	R	<p>Reserved</p> <p>This bit is always read as 0. The write value should always be 0.</p>
18 to 16	ACMDY[2:0]	000	R/W	<p><math>\alpha</math> Creation Coefficient Y</p> <p>These bits specify <math>\alpha</math> creation coefficient Y used in the <math>\alpha</math> creation expression determined by the ABES bit.</p> <p>000: (<math>\alpha</math> creation coefficient Y) = (DST <math>\alpha</math> data)            001: (<math>\alpha</math> creation coefficient Y) = 255 – (DST <math>\alpha</math> data)            010: (<math>\alpha</math> creation coefficient Y) = (SRC <math>\alpha</math> data)            011: (<math>\alpha</math> creation coefficient Y) = 255 – (SRC <math>\alpha</math> data)            100: (<math>\alpha</math> creation coefficient Y) = Fixed <math>\alpha</math> value 1 (COEFY setting)            101 to 111: Setting prohibited</p>
15 to 8	COEFX[7:0]	H'00	R/W	<p>Fixed <math>\alpha</math> Value 0</p> <p>These bits specify fixed <math>\alpha</math> value 0 used when the CCMDX or ACMDX bits are set to B'100. A value from H'00 to H'FF can be specified.</p>
7 to 0	COEFY[7:0]	H'00	R/W	<p>Fixed <math>\alpha</math> Value 1</p> <p>These bits specify fixed <math>\alpha</math> value 1 used when the CCMDY or ACMDY bits are set to B'100. A value from H'00 to H'FF can be specified.</p>

### 28.2.16.7 BRU Raster Operation Control Register (VI6\_BRU\_ROP)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	DSTSEL [2:0]			—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	CROP [3:0]				AROP [3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

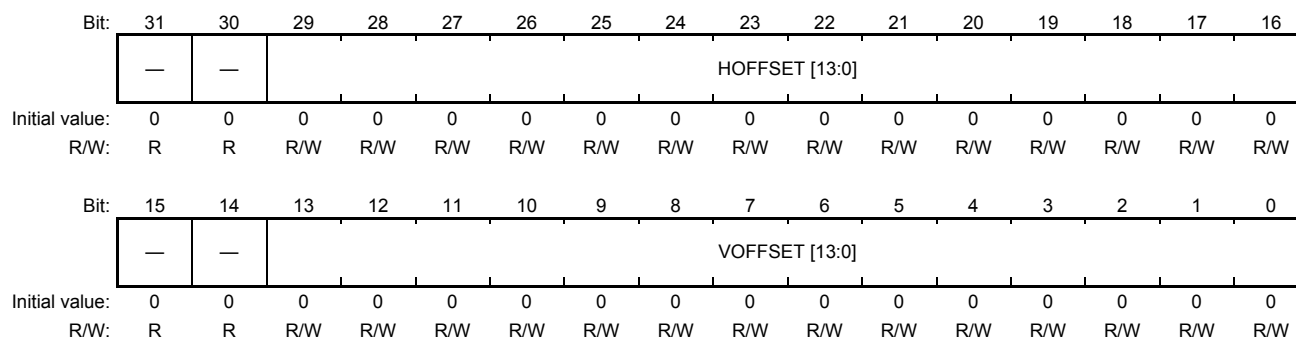
Bit	Bit Name	Initial Value	R/W	Description
31 to 23	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
22 to 20	DSTSEL[2:0]	000	R/W	Input Selection for DST Side of ROP Unit These bits select the input for the DST side of the ROP unit. For the SRC side, the same data as the input for the SRC side of blending/ROP unit C is input. 000: BRU input 0 (BRUin0) is input to DST 001: BRU input 1 (BRUin1) is input to DST 010: BRU input 2 (BRUin2) is input to DST 011: BRU input 3 (BRUin3) is input to DST 100: Virtual RPF is input to DST 101 to 111: Setting prohibited
19 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7 to 4	CROP[3:0]	0000	R/W	Color Data ROP Operator These bits select the ROP operator of the color data in the ROP unit. Select the opcode for ROP operation from Table 28.36.
3 to 0	AROP[3:0]	0000	R/W	$\alpha$ Data ROP Operator These bits select the ROP operator of the $\alpha$ data in the ROP unit. Select the opcode for ROP operation from Table 28.36.

## 28.2.17 HGO Control Registers

### 28.2.17.1 HGO Detection Window Offset Register (VI6\_HGO\_OFFSET)

Note: See Table 28.15 for details on which RZ/G series products have which registers.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√



Bit	Bit Name	Initial Value	R/W	Description
31, 30	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
29 to 16	HOFFSET[13:0]	H'0000	R/W	Horizontal Offset of Histogram Detection Window The HGO creates a histogram for the detection window in the input image (Figure 28.46). In these bits, specify the value of horizontal offset (hoffset shown in Figure 28.46) in pixel units. A value from 0 to 8,191 can be specified. The value of HOFFSET shall be smaller than that of the input image size of HGO.
15, 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13 to 0	VOFFSET[13:0]	H'0000	R/W	Vertical Offset of Histogram Detection Window The HGO creates a histogram for the detection window in the input image (Figure 28.46). In these bits, specify the value of vertical offset (voffset shown in Figure 28.46) in pixel units. A value from 0 to 8,191 can be specified. The value of VOFFSET shall be smaller than that of the input image size of HGO.

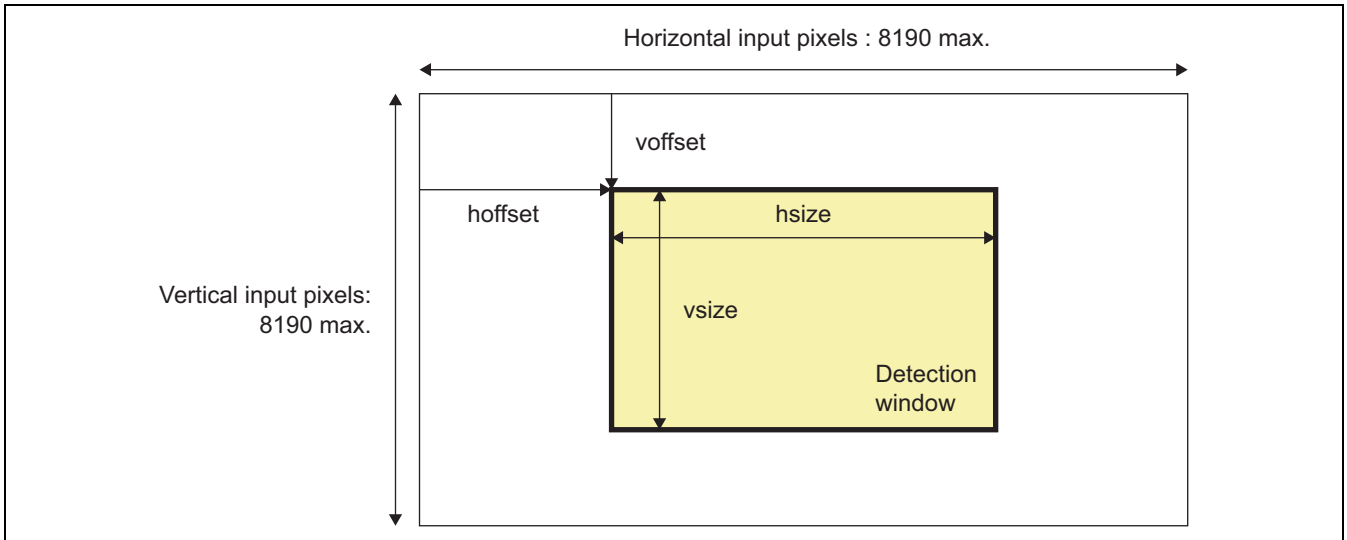
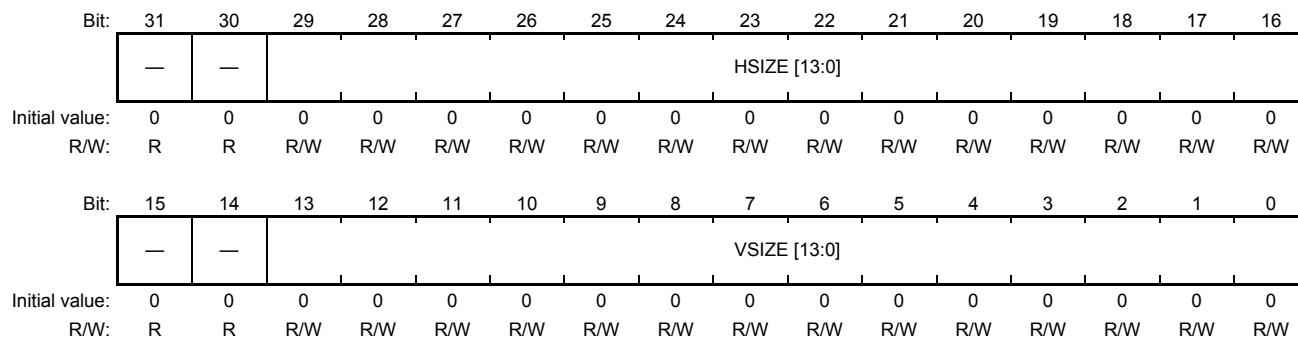


Figure 28.46 Histogram Detection Window of HGO

### 28.2.17.2 HGO Detection Window Size Register (VI6\_HGO\_SIZE)

Note: See Table 28.15 for details on which RZ/G series products have which registers.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√



Bit	Bit Name	Initial Value	R/W	Description
31, 30	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
29 to 16	HSIZE[13:0]	H'0000	R/W	Horizontal Size of Histogram Detection Window The HGO creates a histogram for the detection window in the input image (Figure 28.46). In these bits, specify the value of horizontal size (hsize shown in Figure 28.46) in pixel units. A value from 1 to 8,192 can be specified.
15, 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13 to 0	VSIZ[13:0]	H'0000	R/W	Vertical Size of Histogram Detection Window The HGO creates a histogram for the detection window in the input image (Figure 28.46). In these bits, specify the value of vertical size (vsize shown in Figure 28.46) in pixel units. A value from 1 to 8,192 can be specified.

### 28.2.17.3 HGO Mode Register (VI6\_HGO\_MODE)

Note: See Table 28.15 for details on which RZ/G series products have which registers.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7	MAXRGB	0	R/W	Histogram Source Component Setting 0: The histogram is generated from 3 color components independently. 1: The histogram is generated from the maximum value of input R, G and B data.
6	OFSB_R	0	R/W	Offset Binary Mode for R/Cr/H Component 0: Straight binary 1: Offset binary In offset binary mode, values are converted to absolute values before they are used to detect the maximum value, minimum value, sum, and black band. Note that values without conversion are always used for histogram creation regardless of this mode setting.
5	OFSB_G	0	R/W	Offset Binary Mode for G/Y/S/max (R, G, B) Component 0: Straight binary 1: Offset binary In offset binary mode, values are converted to absolute values before they are used to detect the maximum value, minimum value, sum, and black band. Note that values without conversion are always used for histogram creation regardless of this mode setting.
4	OFSB_B	0	R/W	Offset Binary Mode for B/Cb/V Component 0: Straight binary 1: Offset binary In offset binary mode, values are converted to absolute values before they are used to detect the maximum value, minimum value, sum, and black band. Note that values without conversion are always used for histogram creation regardless of this mode setting.

Bit	Bit Name	Initial Value	R/W	Description
3, 2	HRATIO[1:0]	00	R/W	<p>Horizontal Pixel Skipping Mode for Histogram Detection</p> <p>00: No skipping for horizontal pixels.</p> <p>01: Horizontal 1/2 skipping. One pixel is discarded from every two pixels before a histogram is created.</p> <p>10: Horizontal 1/4 skipping. Three pixels are discarded from every four pixels before a histogram is created.</p> <p>The first pixel in the horizontal direction is not discarded but subsequent pixels are discarded (regardless of the histogram detection window). Among the pixels that have not been discarded, only the pixels within the detection window are used to create a histogram.</p>
1, 0	VRATIO[1:0]	00	R/W	<p>Vertical Pixel Skipping Mode for Histogram Detection</p> <p>00: No skipping for vertical pixels.</p> <p>01: Vertical 1/2 skipping. One pixel is discarded from every two pixels before a histogram is created.</p> <p>10: Vertical 1/4 skipping. Three pixels are discarded from every four pixels before a histogram is created.</p> <p>The first pixel in the vertical direction is not discarded but subsequent pixels are discarded (regardless of the histogram detection window). Among the pixels that have not been discarded, only the pixels within the detection window are used to create a histogram.</p>

**28.2.17.4 HGO LB Detection Threshold Register (VI6\_HGO\_LB\_TH)**

Note: See Table 28.15 for details on which RZ/G series products have which registers.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	BLACK_TH [7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

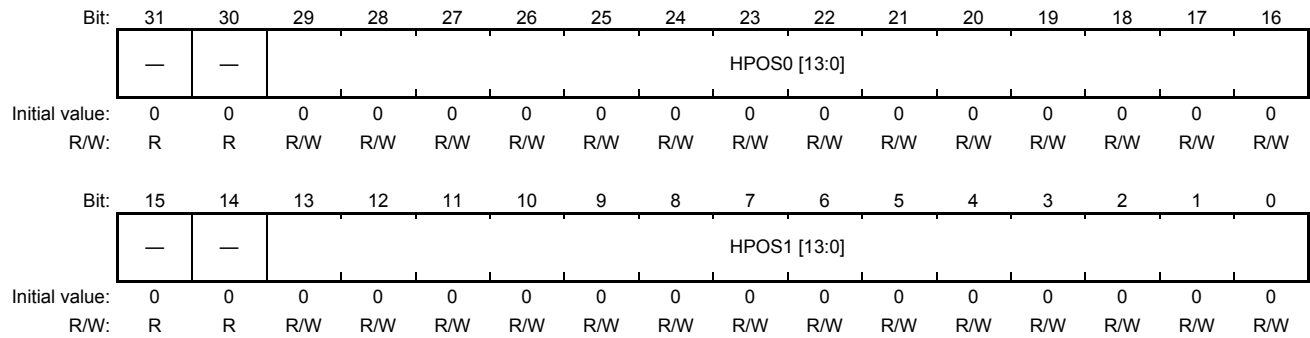
Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7 to 0	BLACK_TH[7:0]	H'00	R/W	Threshold for Black Level Determination in Letter Box Detection In letter box detection, when all input pixels have the value equal to or smaller than the value specified in these bits, the image data is determined as black. Note that the letter box detection is not affected by the histogram detection window illustrated in Figure 28.46. A value from 0 to 255 can be specified.



### 28.2.17.5 HGO Horizontal Position Register for LB Detection Zone-n (VI6\_HGO\_LBn\_H: n = 0, 1, 2, 3)

Note: See Table 28.15 for details on which RZ/G series products have which registers.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√



Bit	Bit Name	Initial Value	R/W	Description
31, 30	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
29 to 16	HPOS0[13:0]	H'0000	R/W	Horizontal Start Position for Letter Box Detection Zone-n When all pixels on a line (shown in Figure 28.47) in the input image have the value equal to or smaller than the threshold value, the HGO determines that there is a letter box. In these bits, specify the value of hpos0 of the detection zone-n (Figure 28.47) in pixel units. A value from 0 to 8,191 can be specified. $HPOS0 \leq HPOS1$ should be satisfied. These bits are valid for Zone-0 and 1. For Zone-2 and 3, these bits are reserved.
15, 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13 to 0	HPOS1[13:0]	H'0000	R/W	Horizontal End Position for Letter Box Detection Zone-n When all pixels on a line (shown in Figure 28.47) in the input image have the value equal to or smaller than the threshold value, the HGO determines that there is a letter box. In these bits, specify the value of hpos1 of the detection zone-n (Figure 28.47) in pixel units. A value from 0 to 8,191 can be specified. $HPOS0 \leq HPOS1$ should be satisfied.

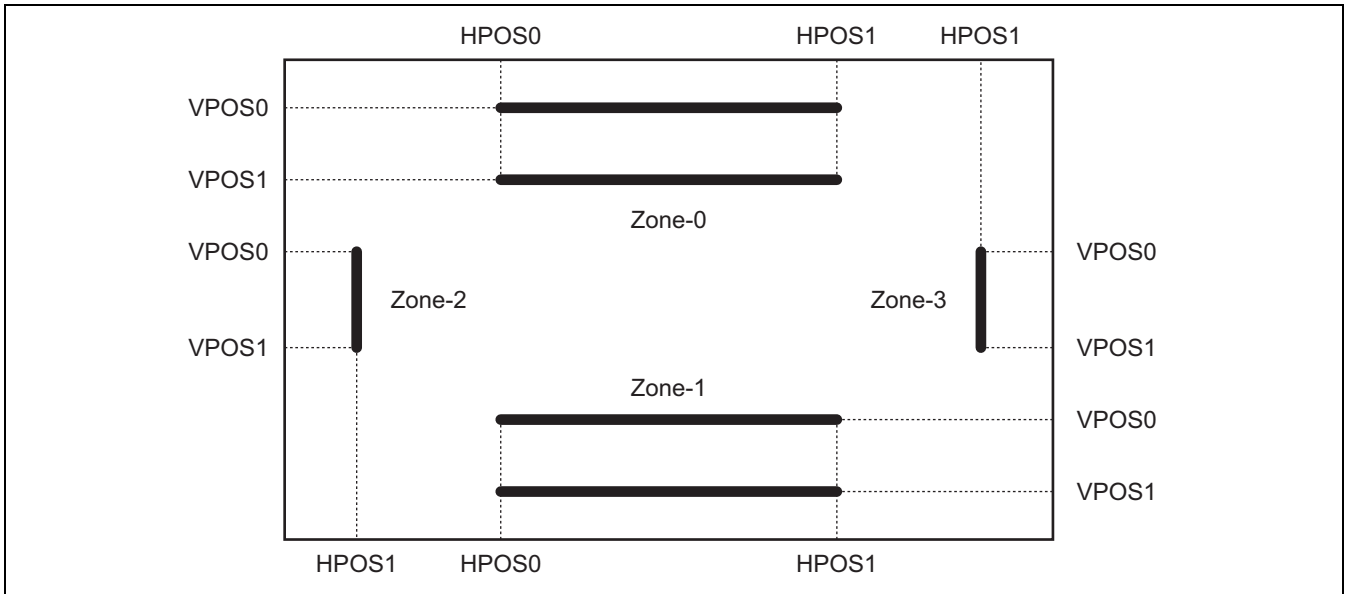
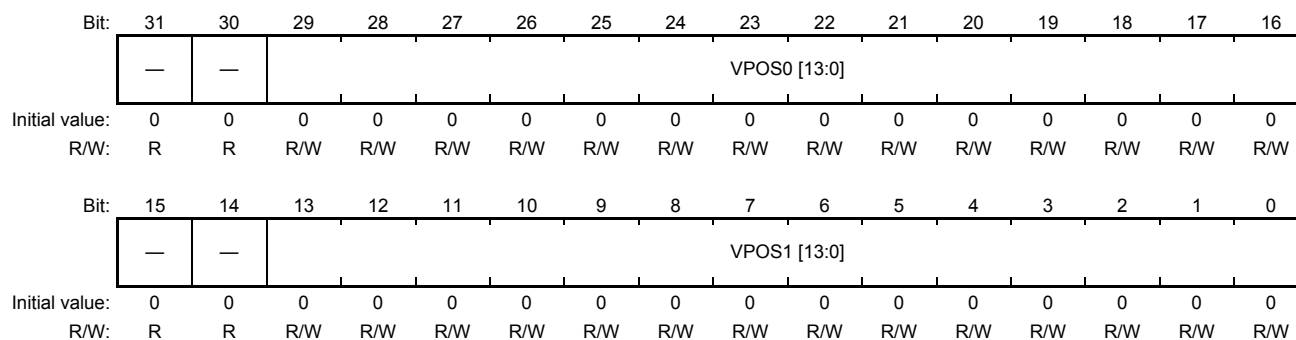


Figure 28.47 Letter Box Detection Position Settings for HGO

### 28.2.17.6 HGO Vertical Position Register for LB Detection Zone-n (VI6\_HGO\_LBn\_V: n = 0, 1, 2, 3)

Note: See Table 28.15 for details on which RZ/G series products have which registers.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√



Bit	Bit Name	Initial Value	R/W	Description
31, 30	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
29 to 16	VPOS0 [13:0]	H'0000	R/W	Vertical Start Position for Letter Box Detection Zone-n When all pixels on a line (shown in Figure 28.47) in the input image have the value equal to or smaller than the threshold value, the HGO determines that there is a letter box In these bits, specify the value of vpos0 of the detection zone-n (Figure 28.47) in pixel units. A value from 0 to 8,191 can be specified. $VPOS0 \leq VPOS1$ should be satisfied.
15, 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13 to 0	VPOS1 [13:0]	H'0000	R/W	Vertical End Position for Letter Box Detection Zone-n When all pixels on a line (shown in Figure 28.47) in the input image have the value equal to or smaller than the threshold value, the HGO determines that there is a letter box. In these bits, specify the value of vpos1 of the detection zone-n (Figure 28.47) in pixel units. A value from 0 to 8,191 can be specified. $VPOS0 \leq VPOS1$ should be satisfied.

### 28.2.17.7 HGO Component-m Histogram Register (VI6\_HGO\_m\_HISTO\_n: m = R, G, B, n = 0 to 63)

Note: See Table 28.15 for details on which RZ/G series products have which registers.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	HISTOGRAM_n [21:16]					
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	HISTOGRAM_n [15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 22	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
21 to 0	HISTOGRAM_n [21:0]	H'00 0000	R	Frequency of Component-m in the value range-n From these bits, the count of the pixels whose component-m value (val) satisfies the following condition within the histogram detection window (Figure 28.46) is read (after pixel skipping is applied when skipping mode is selected). $4 \times n \leq \text{val} < 4 \times (n + 1)$ Counting starts after the HGO is activated. To read the histogram, read these bits after the HGO has completed processing of one screen of data and before the HGO is activated again.

The component-m in a color space is determined by the following table.

Index-m	Color Space			
	RGB		YCbCr	HSV
	VI6_HGO_MODE. MAXRGB = 0	VI6_HGO_MODE. MAXRGB = 1	VI6_HGO_MODE. MAXRGB = 0*1	VI6_HGO_MODE. MAXRGB = 0*1
R	R	n/a*2	Cr	H
G	G	max (R, G, B)*3	Y	S
B	B	n/a*2	Cb	V

- Notes: 1. When color space of input data is in YCbCr or HSV, set VI6\_HGO\_MODE.MAXRGB = 0.  
2. When VI6\_HGO\_MODE.MAXRGB = 1, the histogram of index-R / index-B are not ensured.  
3. max (R, G, B) indicates maximum value of input R, G and B data.

### 28.2.17.8 HGO Component-m Min/Max Value Register (VI6\_HGO\_m\_MAXMIN: m = R, G, B)

Note: See Table 28.15 for details on which RZ/G series products have which registers.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	MAXVAL [7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

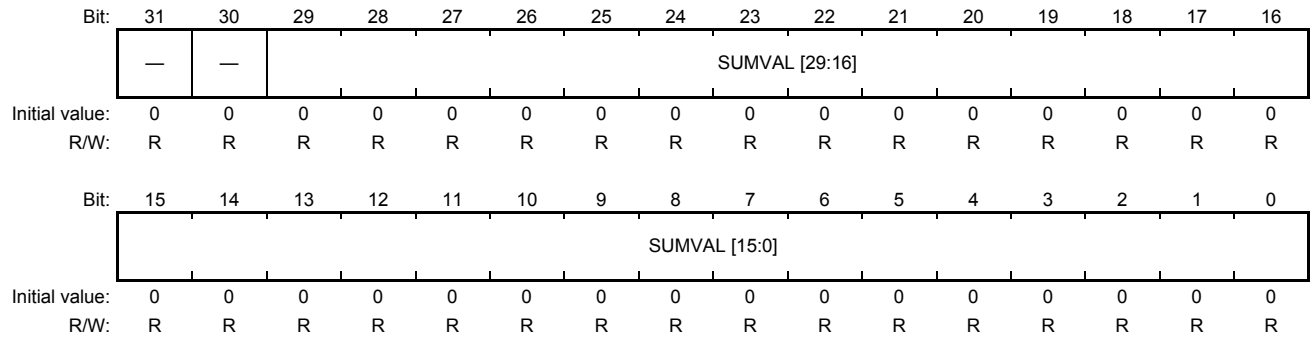
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	MINVAL [7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 16	MAXVAL[7:0]	H'00	R	Maximum Value of Component-m From these bits, the maximum value of the component-m of the pixels within the histogram detection window (Figure 28.46) is read (after pixel skipping is applied when skipping mode is selected). Maximum value detection starts after the HGO is activated. To read the maximum value, read these bits after the HGO has completed processing of one screen of data and before the HGO is activated again.
15 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7 to 0	MINVAL[7:0]	H'00	R	Minimum Value of Component-m From these bits, the minimum value of the component-m of the pixels within the histogram detection window (Figure 28.46) is read (after pixel skipping is applied when skipping mode is selected). Minimum value detection starts after the HGO is activated. To read the minimum value, read these bits after the HGO has completed processing of one screen of data and before the HGO is activated again.

### 28.2.17.9 HGO Component-m Sum Register (VI6\_HGO\_m\_SUM: m = R, G, B)

Note: See Table 28.15 for details on which RZ/G series products have which registers.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√



Bit	Bit Name	Initial Value	R/W	Description
31, 30	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
29 to 0	SUMVAL[29:0]	H'0000 0000	R	Sum of Component-m From these bits, the sum of the component-m of the pixels within the histogram detection window (Figure 28.46) is read (after pixel skipping is applied when skipping mode is selected). Accumulation starts after the HGO is activated. To read the sum, read these bits after the HGO has completed processing of one screen of data and before the HGO is activated again.

### 28.2.17.10 HGO Component-m LB Detection Result Register (VI6\_HGO\_m\_LB\_DET: m = R, G, B)

Note: See Table 28.15 for details on which RZ/G series products have which registers.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	LTRBO X1	LTRBO X2	SIDE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2	LTRBOX1	0	R	Letter Box Detection Result #1 of Zone-0/1 for Component-m This bit is set to 1 when none of the component-m of the pixels on the lines of zone-0/vpos0 and zone-1/vpos1 (two lines in total) in Figure 28.47 exceeds the threshold (BLACK_TH). If any pixel is greater than the threshold, this bit is set to 0. Read this bit after the HGO has completed processing of one screen of data and before the HGO is activated again. The value read during processing is not guaranteed to be correct.
1	LTRBOX2	0	R	Letter Box Detection Result #2 of Zone-0/1 for Component-m This bit is set to 1 when none of the component-m of the pixels on the four lines of zone-0 and 1 in Figure 28.47 exceeds the threshold (BLACK_TH). If any pixel is greater than the threshold, this bit is set to 0. Read this bit after the HGO has completed processing of one screen of data and before the HGO is activated again. The value read during processing is not guaranteed to be correct.
0	SIDE	0	R	Letter Box Detection Result of Zone-2/3 for Component-m This bit is set to 1 when none of the component-m of the pixels on the two lines of zone-2 and 3 in Figure 28.47 exceeds the threshold (BLACK_TH). If any pixel is greater than the threshold, this bit is set to 0. Read this bit after the HGO has completed processing of one screen of data and before the HGO is activated again. The value read during processing is not guaranteed to be correct.

### 28.2.17.11 HGO Parameter Register Reset (VI6\_HGO\_REGRST)

Note: See Table 28.15 for details on which RZ/G series products have which registers.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	RCLEA	0	W	Register Reset Writing 1 to this bit resets all read-only registers (sections 28.2.17.7 to 28.2.17.10) to their initial values. This register is write-only and is always read as 0. Note that R/W registers (sections 28.2.17.1 to 28.2.17.6) are not affected by write access to this register.

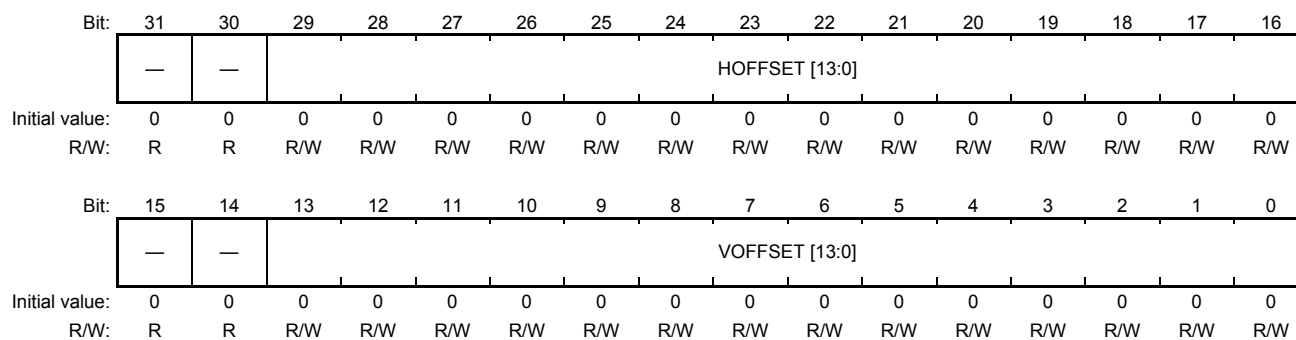


## 28.2.18 HGT Control Registers

### 28.2.18.1 HGT Detection Window Offset Register (VI6\_HGT\_OFFSET)

Note: See Table 28.15 for details on which RZ/G series products have which registers.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√



Bit	Bit Name	Initial Value	R/W	Description
31, 30	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
29 to 16	HOFFSET[13:0]	H'0000	R/W	Horizontal Offset of Histogram Detection Window The HGT creates a histogram for the detection window in the input image (Figure 28.48). In these bits, specify the value of horizontal offset (hoffset shown Figure 28.48) in pixel units. A value from 0 to 8,191 can be specified. The value of HOFFSET shall be smaller than that of the input image size of HGT.
15, 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13 to 0	VOFFSET[13:0]	H'0000	R/W	Vertical Offset of Histogram Detection Window The HGT creates a histogram for the detection window in the input image (Figure 28.48). In these bits, specify the value of vertical offset (voffset shown in Figure 28.48) in pixel units. A value from 0 to 8,191 can be specified. The value of VOFFSET shall be smaller than that of the input image size of HGT.

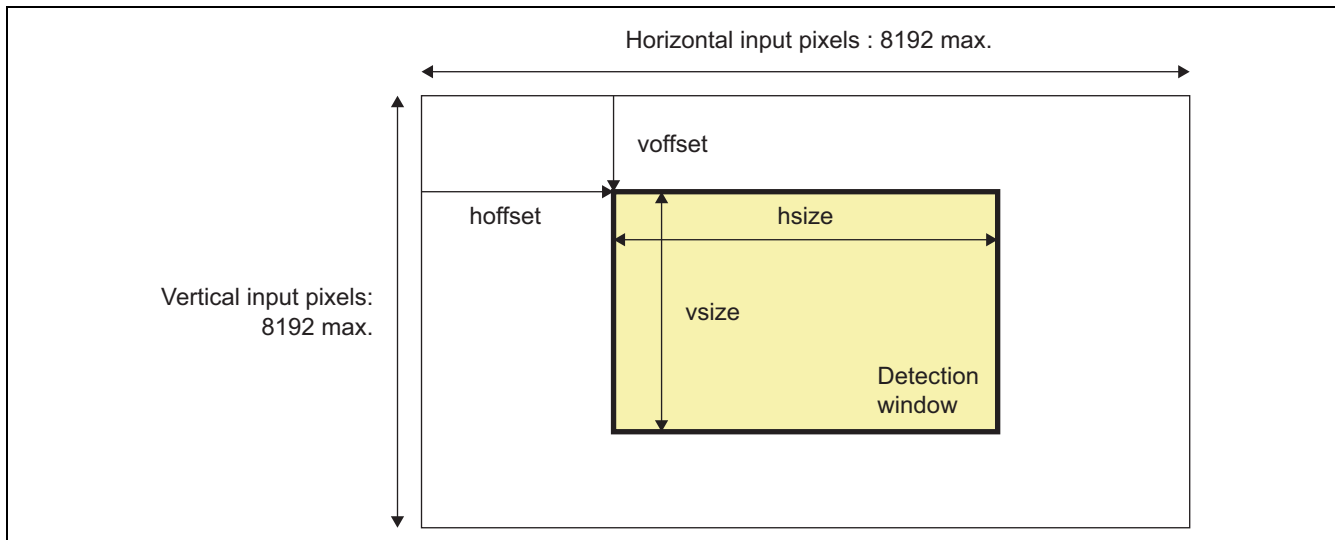
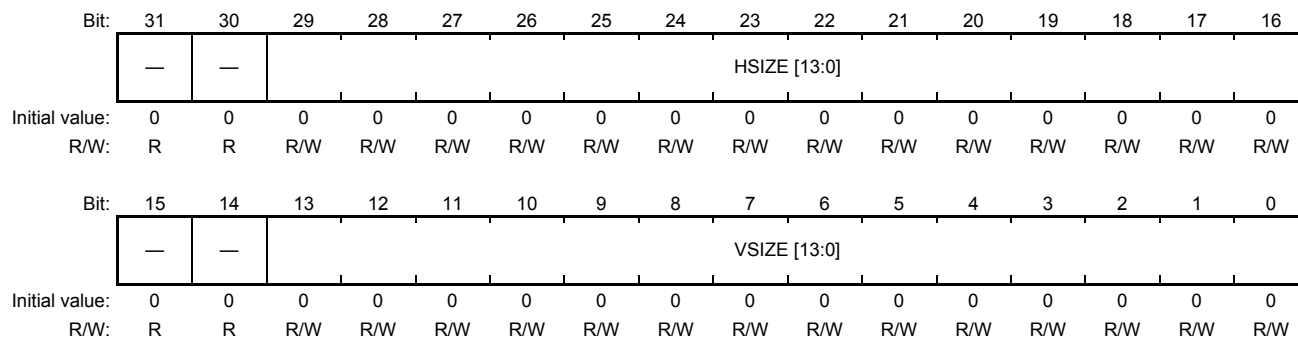


Figure 28.48 Histogram Detection Window of HGT

**28.2.18.2 HGT Detection Window Size Register (VI6\_HGT\_SIZE)**

Note: See Table 28.15 for details on which RZ/G series products have which registers.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√



Bit	Bit Name	Initial Value	R/W	Description
31, 30	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
29 to 16	HSIZE[13:0]	H'0000	R/W	Horizontal Size of Histogram Detection Window The HGT creates a histogram for the detection window in the input image (Figure 28.48). In these bits, specify the value of horizontal offset (hsize shown in Figure 28.48) in pixel units. A value from 1 to 8,192 can be specified.
15, 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13 to 0	VSIZE[13:0]	H'0000	R/W	Vertical Size of Histogram Detection Window The HGT creates a histogram for the detection window in the input image (Figure 28.48). In these bits, specify the value of vertical offset (vsize shown in Figure 28.48) in pixel units. A value from 1 to 8,192 can be specified.

### 28.2.18.3 HGT Mode Register (VI6\_HGT\_MODE)

Note: See Table 28.15 for details on which RZ/G series products have which registers.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	HRATIO [1:0]		VRATIO [1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3, 2	HRATIO[1:0]	00	R/W	Horizontal Pixel Skipping Mode for Histogram Detection 00: No skipping for horizontal pixels. 01: Horizontal 1/2 skipping. One pixel is discarded from every two pixels before a histogram is created. 10: Horizontal 1/4 skipping. Three pixels are discarded from every four pixels before a histogram is created. The first pixel in the horizontal direction is not discarded but subsequent pixels are discarded (regardless of the histogram detection window). Among the pixels that have not been discarded, only the pixels within the detection window are used to create a histogram.
1, 0	VRATIO[1:0]	00	R/W	Vertical Pixel Skipping Mode for Histogram Detection 00: No skipping for vertical pixels. 01: Vertical 1/2 skipping. One pixel is discarded from every two pixels before a histogram is created. 10: Vertical 1/4 skipping. Three pixels are discarded from every four pixels before a histogram is created. The first pixel in the vertical direction is not discarded but subsequent pixels are discarded (regardless of the histogram detection window). Among the pixels that have not been discarded, only the pixels within the detection window are used to create a histogram.

### 28.2.18.4 HGT Hue Area Register (VI6\_HGT\_HUE\_AREA\_n: n = 0 to 5)

Note: See Table 28.15 for details on which RZ/G series products have which registers.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	HUE_LOWER_n [7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	HUE_UPPER_n [7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 16	HUE_LOWER_n [7:0]	H'00	R/W	Lower Boundary Value for Hue Area - n The HGT creates a two-dimensional histogram of H (hue) and S (saturation) components. Division of hue areas and overlapping of adjacent hue areas can be specified through these bits. In these bits, specify the value of n L (hue_lower n) shown in Figure 28.49. A value from 0 to 255 can be specified. The specified value should satisfy the restrictions shown in Figure 28.49.
15 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7 to 0	HUE_UPPER_n [7:0]	H'00	R/W	Upper Boundary Value for Hue Area - n The HGT creates a two-dimensional histogram of H (hue) and S (saturation) components. Division of hue areas and overlapping of adjacent hue areas can be specified through these bits. In these bits, specify the value of n U (hue_upper n) shown in Figure 28.49. A value from 0 to 255 can be specified. The specified value should satisfy the restrictions shown in Figure 28.49.

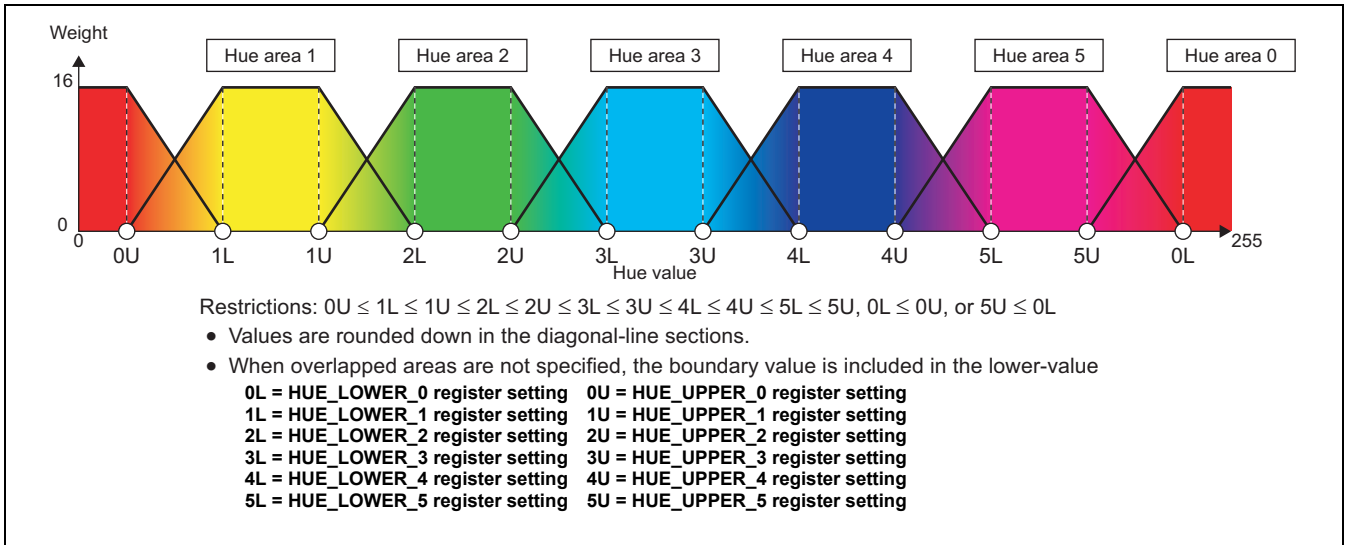


Figure 28.49 Weighting Histogram Using Hue

### 28.2.18.5 HGT LB Detection Threshold Register (VI6\_HGT\_LB\_TH)

Note: See Table 28.15 for details on which RZ/G series products have which registers.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

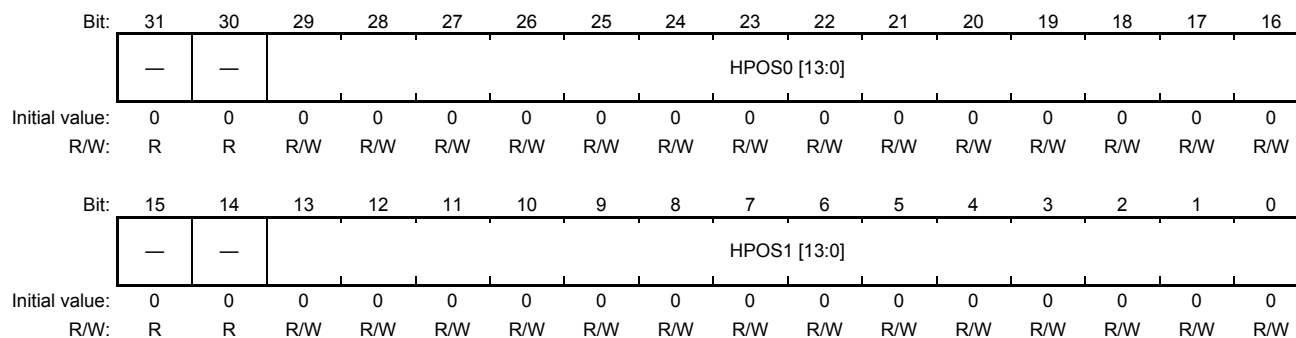
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	BLACK_TH [7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7 to 0	BLACK_TH[7:0]	H'00	R/W	Threshold for Black Level Determination in Letter Box Detection In letter box detection, when all pixels of the input image data have the value equal to or smaller than the value specified in these bits, the data is determined as black. Note that the letter box detection is not affected by the histogram detection window illustrated in Figure 28.48 A value from 0 to 255 can be specified.

### 28.2.18.6 HGT Horizontal Position Register for LB Detection Zone-n (VI6\_HGT\_LBn\_H: n = 0, 1, 2, 3)

Note: See Table 28.15 for details on which RZ/G series products have which registers.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√



Bit	Bit Name	Initial Value	R/W	Description
31, 30	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
29 to 16	HPOS0[13:0]	H'0000	R/W	Horizontal Start Position for Letter Box Detection Zone-n When all pixels on a line (shown in Figure 28.50) in the input image have the value equal to or smaller than the threshold value, the HGT determines that there is a letter box. In these bits, specify the value of hpos0 of the detection zone-n (Figure 28.50) in pixel units. A value from 0 to 8,191 can be specified. $HPOS0 \leq HPOS1$ should be satisfied. These bits are valid for Zone-0 and 1. For Zone-2 and 3, these bits are reserved.
15, 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13 to 0	HPOS1[13:0]	H'0000	R/W	Horizontal End Position for Letter Box Detection Zone-n When all pixels on a line (shown in Figure 28.50) in the input image have the value equal to or smaller than the threshold value, the HGT determines that there is a letter box. In these bits, specify the value of hpos1 of the detection zone-n (Figure 28.50) in pixel units. A value from 0 to 8,191 can be specified. $HPOS0 \leq HPOS1$ should be satisfied.



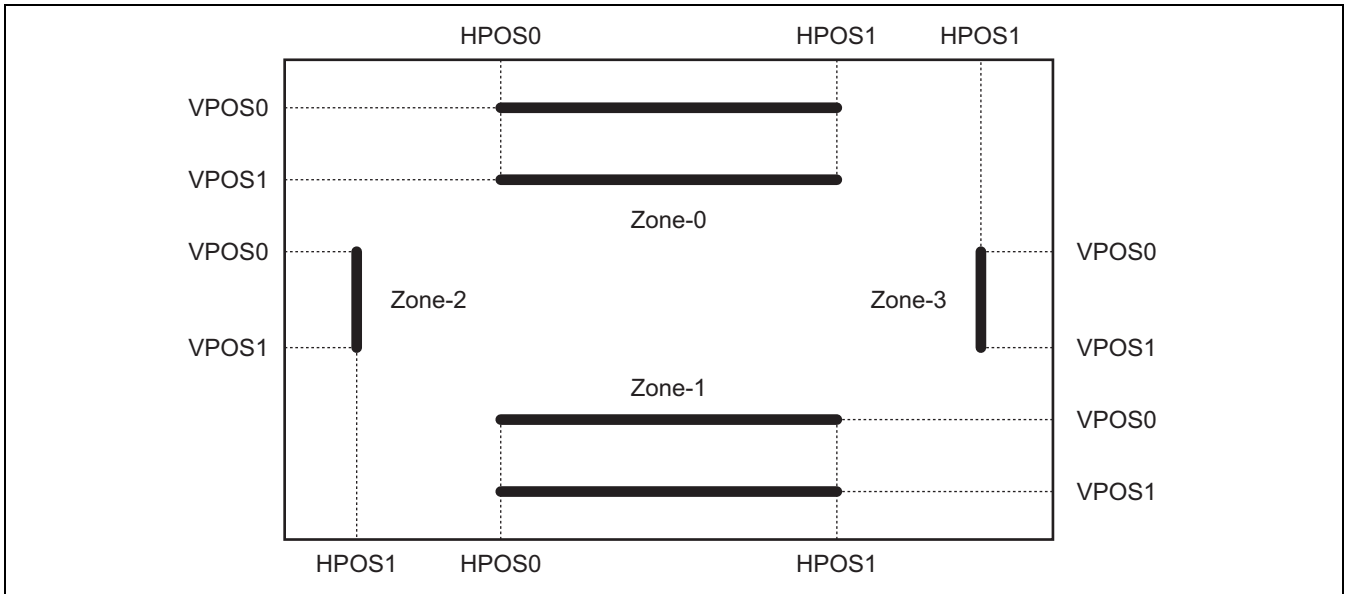
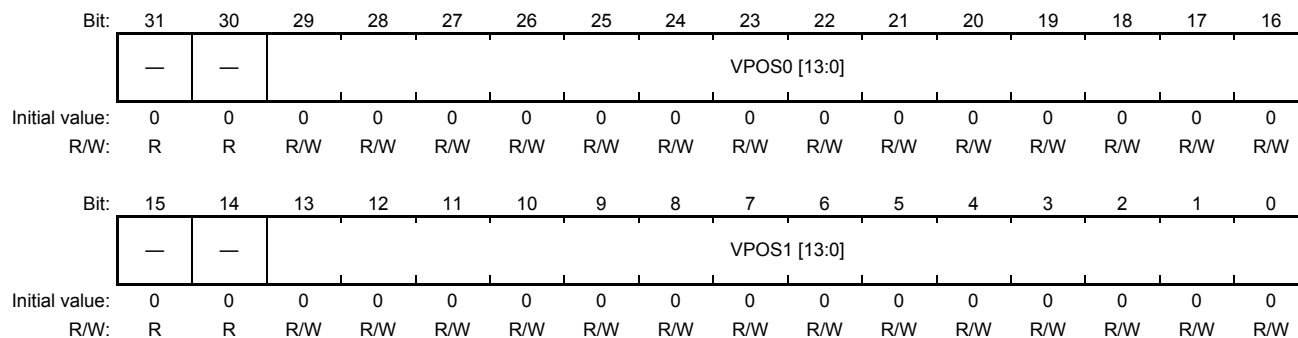


Figure 28.50 Letter Box Detection Position Settings for HGT

**28.2.18.7 HGT Vertical Position Register for LB Detection Zone-n (VI6\_HGT\_LBn\_V: n = 0, 1, 2, 3)**

Note: See Table 28.15 for details on which RZ/G series products have which registers.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√



Bit	Bit Name	Initial Value	R/W	Description
31, 30	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
29 to 16	VPOS0[13:0]	H'0000	R/W	Vertical Start Position for Letter Box Detection Zone-n When all pixels on a line (shown in Figure 28.50) in the input image have the value equal to or smaller than the threshold value, the HGT determines that there is a letter box. In these bits, specify the value of vpos0 of the detection zone-n (Figure 28.50) in pixel units. A value from 0 to 8,191 can be specified. $VPOS0 \leq VPOS1$ should be satisfied.
15, 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13 to 0	VPOS1[13:0]	H'0000	R/W	Vertical Position for Letter Box Detection Zone-n When all pixels on a line (shown in Figure 28.50) in the input image have the value equal to or smaller than the threshold value, the HGT determines that there is a letter box. In these bits, specify the value of vpos1 of the detection zone-n (Figure 28.50) in pixel units. A value from 0 to 8,191 can be specified. $VPOS0 \leq VPOS1$ should be satisfied.

### 28.2.18.8 HGT Histogram Register (VI6\_HGT\_HISTO\_m\_n: m = 0 to 5, n = 0 to 31)

Note: See Table 28.15 for details on which RZ/G series products have which registers.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	HISTOGRAM_m_n [25:16]									
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	HISTOGRAM_m_n [15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 26	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
25 to 0	HISTOGRAM_m_n [25:0]	H'000 0000	R	Weighted Frequency of Hue Area-m and Saturation Area-n From these bits, the count of weighting for the pixels whose H component value is in hue area m (Figure 28.49) and whose S component value (val) satisfies the following condition within the histogram detection window (Figure 28.48) is read (after pixel skipping is applied when skipping mode is selected). $8 \times n \leq \text{val} < 8 \times (n + 1)$ The weight is determined by the H component value as shown in Figure 28.49 and the maximum weight is 16. Counting starts after the HGT is activated. To read the histogram, read these bits after the HGT has completed processing of one screen of data and before the HGT is activated again.

### 28.2.18.9 HGT Max/Min Value Register (VI6\_HGT\_MAXMIN)

Note: See Table 28.15 for details on which RZ/G series products have which registers.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	MAXVAL [7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	MINVAL [7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 16	MAXVAL[7:0]	H'00	R	Maximum Value of S Components From these bits, the maximum value of the S components of the pixels within the histogram detection window (Figure 28.48) is read (after pixel skipping is applied when skipping mode is selected). Maximum value detection starts after the HGT is activated. To read the maximum value, read these bits after the HGT has completed processing of one screen of data and before the HGT is activated again.
15 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7 to 0	MINVAL[7:0]	H'00	R	Minimum Value of S Components From these bits, the minimum value of the S components of the pixels within the histogram detection window (Figure 28.48) is read (after pixel skipping is applied when skipping mode is selected). Minimum value detection starts after the HGT is activated. To read the minimum value, read these bits after the HGT has completed processing of one screen of data and before the HGT is activated again.

**28.2.18.10 HGT Sum Register (VI6\_HGT\_SUM)**

Note: See Table 28.15 for details on which RZ/G series products have which registers.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	SUMVAL [29:16]													
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SUMVAL [15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31, 30	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
29 to 0	SUMVAL[29:0]	H'0000 0000	R	Sum of V Components From these bits, the sum of the V components of the pixels within the histogram detection window (Figure 28.48) is read (after pixel skipping is applied when skipping mode is selected). Accumulation starts after the HGT is activated. To read the sum, read these bits after the HGT has completed processing of one screen of data and before the HGT is activated again.

**28.2.18.11 HGT LB Detection Result Register (VI6\_HGT\_LB\_DET)**

Note: See Table 28.15 for details on which RZ/G series products have which registers.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	LTRBO X1	LTRBO X2	SIDE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2	LTRBOX1	0	R	Letter Box Detection Result #1 of Zone-0/1 for V Component This bit is set to 1 when none of the V components of the pixels on the lines of zone-0/VPOS0 and zone-1/VPOS1 (two lines in total) in Figure 28.50 exceeds the threshold (BLACK_TH). If any pixel is greater than the threshold, this bit is set to 0. Read this bit after the HGT has completed processing of one screen of data and before the HGT is activated again. The value read during processing is not guaranteed to be correct.
1	LTRBOX2	0	R	Letter Box Detection Result #2 of Zone-0/1 for V Component This bit is set to 1 when none of the V components of the pixels on the four lines of zone-0 and 1 in Figure 28.50 exceeds the threshold (BLACK_TH). If any pixel is greater than the threshold, this bit is set to 0. Read this bit after the HGT has completed processing of one screen of data and before the HGT is activated again. The value read during processing is not guaranteed to be correct.
0	SIDE	0	R	Letter Box Detection Result of Zone-2/3 for V Component This bit is set to 1 when none of the V components of the pixels on the two lines of zone-2 and 3 in Figure 28.50 exceeds the threshold (BLACK_TH). If any pixel is greater than the threshold, this bit is set to 0. Read this bit after the HGT has completed processing of one screen of data and before the HGT is activated again. The value read during processing is not guaranteed to be correct.

**28.2.18.12 HGT Parameter Register Reset (VI6\_HGT\_REGRST)**

Note: See Table 28.15 for details on which RZ/G series products have which registers.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RCLEA
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	RCLEA	0	W	Register Reset Writing 1 to this bit resets all read-only registers (sections 28.2.18.8 to 28.2.18.11) to their initial values. This register is write-only and is always read as 0. Note that R/W registers (sections 28.2.18.1 to 28.2.18.7) are not affected by write access to this register.

## 28.2.19 LIF Control Registers

### 28.2.19.1 LIF Control Register (VI6\_LIF\_CTRL)

Note: See Table 28.15 for details on which RZ/G series products have which registers.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	OBTH [10:0]										
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	CFMT	—	—	REQSE L	LIF_EN
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 27	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
26 to 16	OBTH [10:0]	All 0	R/W	Buffer Threshold for Start Ready Notification to Display Module When outputting data to the external module, the VSP stores data in the buffer in the LIF. When the amount of data stored in the buffer reaches the value specified in these bits, the VSP notifies the external display module of the start of a frame through an interrupt source (VI6_DISP_IRQ_STA.DST: see section 28.2.5.8). A value from 1 to 1,536 can be specified. Note: The OBTH value should satisfy the following conditions. <ul style="list-style-type: none"> <li>The value should not be larger than the VI6_LIF_CSBTH.HBTH bit setting.</li> <li>When the horizontal and vertical sizes of the image input to the LIF are <math>h_{lif\_in}</math>, and <math>v_{lif\_in}</math>, OBTH should be specified so that the following is satisfied. <math display="block">(&lt; h_{lif\_in} + 1 &gt; / 2) \times v_{lif\_in} - 4 \geq OBTH</math> </li> </ul> The recommended value of OBTH is 128. The LIF input image size ( $h_{lif\_in}$ , and $v_{lif\_in}$ ) is the same as the WPF0 output image size.
15 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	CFMT	0	R/W	Chroma Format This bit selects the output format from the LIF module to the display module. When RGB format is used, this bit shall be set to 0. 0: YCbCr444 or RGB Format 1: Reserved (setting prohibited) Note: ARBG8888 or RGB888 can be used for the DU input format.



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<b>Bit</b>	<b>Bit Name</b>	<b>Initial Value</b>	<b>R/W</b>	<b>Description</b>
3, 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	REQSEL	0	R/W	External Display Module Selection This bit should always be set to 1. 0: Prohibited. 1: DU is selected as the destination external display module.
0	LIF_EN	0	R/W	Enable/Disable of Data Output to External Display Module Enables or disables data output from the LIF to DU. 0: Data output to the DU is disabled. 1: Data output to the DU is enabled.

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### 28.2.19.2 LIF Clock Stop Buffer Control Register (VI6\_LIF\_CSBTH)

Note: See Table 28.15 for details on which RZ/G series products have which registers.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	HBTH [10:0]										
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	LBTH [10:0]										
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 27	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
26 to 16	HBTH [10:0]	All 0	R/W	Buffer Threshold for Clock Stop in Dynamic Clock Control When the remaining data amount in the buffer in the LIF reaches the value specified in these bits while data is output from the LIF to the external display module, the VSP clock is stopped. A value from 2 to 1,536 can be specified. The specified value should satisfy HBTH > LBTH. The recommended value of HBTH is 1536.
15 to 11	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
10 to 0	LBTH [10:0]	All 0	R/W	Buffer Threshold for Clock Start in Dynamic Clock Control When the remaining data amount in the buffer in the LIF decreases to the value specified in these bits while data is output from the LIF to the external display module and the clock is stopped through the setting in the HBTH bits, the VSP clock supply is restarted. A value from 1 to 1,535 can be specified. The specified value should satisfy LBTH < HBTH. The recommended value of LBTH is 1520.

## 28.2.20 Security Control Registers

### 28.2.20.1 Secure Access Control Register 0 (VI6\_SECURE\_CTRL0)

Note: See Table 28.15 for details on which RZ/G series products have which registers.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	SCCH3	SCCH2	SCCH1	SCCH0	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	SCWPF3	SCWPF2	SCWPF1	SCWPF0	—	—	—	SCRPF4	SCRPF3	SCRPF2	SCRPF1	SCRPF0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R	R	R	R/W	R/W	R/W	R/W	R/W

Each bit is used for specifying the secure attribute of the corresponding registers. If a bit is set to 1 (secure), the corresponding registers can be written only by the secure CPU access.

Bit	Bit Name	Initial Value	R/W	Description
31 to 28	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
27	SCCH3	0	R/W	Secure Attribute for Display List 3 Registers 0: Non-secure 1: Secure
26	SCCH2	0	R/W	Secure Attribute for Display List 2 Registers 0: Non-secure 1: Secure
25	SCCH1	0	R/W	Secure Attribute for Display List 1 Registers 0: Non-secure 1: Secure
24	SCCH0	0	R/W	Secure Attribute for Display List 0 Registers 0: Non-secure 1: Secure
23 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11	SCWPF3	0	R/W	Secure Attribute for WPF3 Registers 0: Non-secure 1: Secure
10	SCWPF2	0	R/W	Secure Attribute for WPF2 Registers 0: Non-secure 1: Secure

Bit	Bit Name	Initial Value	R/W	Description
9	SCWPF1	0	R/W	Secure Attribute for WPF1 Registers 0: Non-secure 1: Secure
8	SCWPF0	0	R/W	Secure Attribute for WPF0 Registers 0: Non-secure 1: Secure
7 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	SCRPF4	0	R/W	Secure Attribute for RPF4 Registers 0: Non-secure 1: Secure
3	SCRPF3	0	R/W	Secure Attribute for RPF3 Registers 0: Non-secure 1: Secure
2	SCRPF2	0	R/W	Secure Attribute for RPF2 Registers 0: Non-secure 1: Secure
1	SCRPF1	0	R/W	Secure Attribute for RPF1 Registers 0: Non-secure 1: Secure
0	SCRPF0	0	R/W	Secure Attribute for RPF0 Registers 0: Non-secure 1: Secure

### 28.2.20.2 Secure Access Control Register 1 (VI6\_SECURE\_CTRL1)

Note: See Table 28.15 for details on which RZ/G series products have which registers.

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	SCLIF	SCHGT	SCHGO	—	SCBRU	SCHSI	SCHST	SCCLU	SCLUT	—	—	SCUDS 2	SCUDS 1	SCUDS 0	SCSRU
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W

Each bit is used for specifying the secure attribute of the corresponding registers. If a bit is set to 1 (secure), the corresponding registers can be read or written only by the secure CPU access.

Bit	Bit Name	Initial Value	R/W	Description
31 to 15	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
14	SCLIF	0	R/W	Secure Attribute for LIF Registers 0: Non-secure 1: Secure
13	SCHGT	0	R/W	Secure Attribute for HGT Registers 0: Non-secure 1: Secure
12	SCHGO	0	R/W	Secure Attribute for HGO Registers 0: Non-secure 1: Secure
11	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
10	SCBRU	0	R/W	Secure Attribute for BRU Registers 0: Non-secure 1: Secure
9	SCHSI	0	R/W	Secure Attribute for HSI Registers 0: Non-secure 1: Secure
8	SCHST	0	R/W	Secure Attribute for HST Registers 0: Non-secure 1: Secure
7	SCCLU	0	R/W	Secure Attribute for CLU Registers 0: Non-secure 1: Secure

Bit	Bit Name	Initial Value	R/W	Description
6	SCLUT	0	R/W	Secure Attribute for LUT Registers 0: Non-secure 1: Secure
5, 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3	SCUDS2	0	R/W	Secure Attribute for UDS2 Registers 0: Non-secure 1: Secure
2	SCUDS1	0	R/W	Secure Attribute for UDS1 Registers 0: Non-secure 1: Secure
1	SCUDS0	0	R/W	Secure Attribute for UDS0 Registers 0: Non-secure 1: Secure
0	SCSRU	0	R/W	Secure Attribute for SRU Registers 0: Non-secure 1: Secure

## 28.3 Lookup Table Settings

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

### 28.3.1 CLUT or LUT

For a single entry to the CLUT space (see Table 28.37) or LUT space (see Table 28.37) of the VSP1, the CLUT or LUT data is set by a write access in the format shown in Figure 28.51.

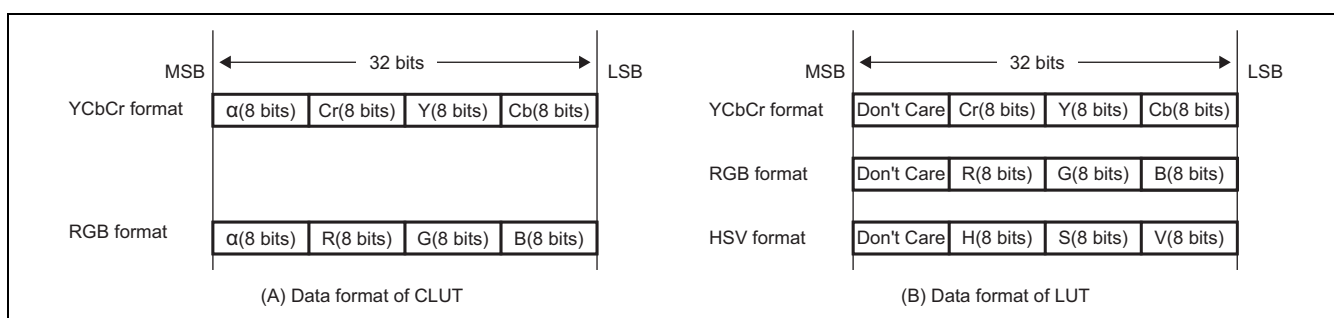
The entry address of each space is (start address of the space) + (entry number counting from the base point  $0 \times 4$ ). For example, the address of entry 7 to the LUT space is  $\$VSP\_BASE + H'7000 + 7 \times 4$  (H'FE92\_701C (VSPR case)).

Table 28.37 shows the spaces for which entries can be made. Note that if the module that references that space is operating, write accesses to the relevant space are prohibited. For example, while RPF2 is operating, accesses to the entire space of VI6\_CLUT2\_TBL are prohibited. When a read access is made to the relevant space during operation of the referencing module, undefined values will be read out.

The operating/stopped state of each module in Table 28.37 is the operating state of the WPF to which each module is connected. Determine whether the module is operating or stopped using each WPF operating status bit in the VI6\_STATUS register.

**Table 28.37 CLUT Space and LUT Space Addresses**

Space Name	Space Addresses	Entry Count	Module that References the Space in the Left Column	RZ/G Series Products			
				RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
VI6_CLUT0_TBL	$\$VSP\_BASE + H'4000$ to $\$VSP\_BASE + H'43FF$	256	RPF0	√	√	√	√
VI6_CLUT1_TBL	$\$VSP\_BASE + H'4400$ to $\$VSP\_BASE + H'47FF$	256	RPF1	√	√	√	√
VI6_CLUT2_TBL	$\$VSP\_BASE + H'4800$ to $\$VSP\_BASE + H'4BFF$	256	RPF2	√	√	√	√
VI6_CLUT3_TBL	$\$VSP\_BASE + H'4C00$ to $\$VSP\_BASE + H'4FFF$	256	RPF3	√	√	√	√
VI6_CLUT4_TBL	$\$VSP\_BASE + H'5000$ to $\$VSP\_BASE + H'53FF$	256	RPF4	√	√	√	√
VI6_LUT_TBL	$\$VSP\_BASE + H'7000$ to $\$VSP\_BASE + H'73FF$	256	LUT	√	√	√	√



**Figure 28.51 VI6\_CLUT\_TBL and VI6\_LUT\_TBL Formats**

### 28.3.2 CLU Table

Data is set in the CLU table in the space shown in Table 28.38 through indirect addressing.

**Table 28.38 CLU Space Addresses**

Space Name	Space Addresses	Module that References the Space in the Left Column	RZ/G Series Products			
			RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
VI6_CLU_TBL	\$VSP_BASE + H'7400 to \$VSP_BASE + H'7407	CLU	√	√	√	√

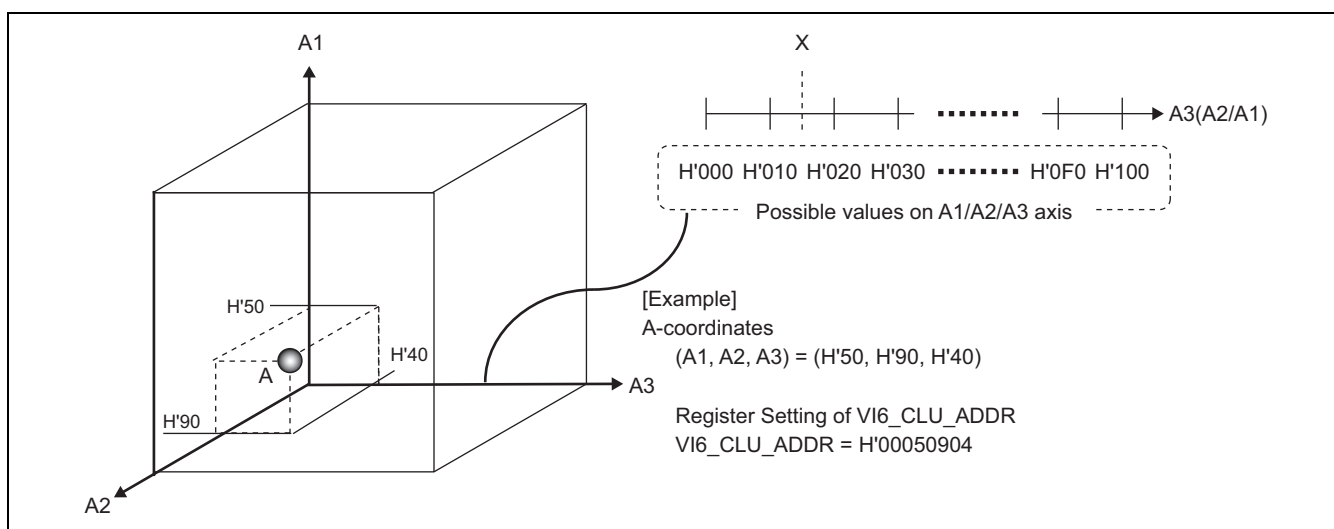
The addresses used in indirect addressing (VI6\_CLU\_ADDR, VI6\_CLU\_DATA) are shown in Table 28.39. The CLU table can be accessed by setting the VI6\_CLU\_ADDR register and then reading from or writing to the VI6\_CLU\_DATA register. To write-access the CLU table continuously, such as when setting data to the CLU table, perform the following.

- (1) Set the first CLU table coordinates in VI6\_CLU\_ADDR.
  - (2) Write the first data to be set in VI6\_CLU\_DATA.
  - (3) Set the next CLU table coordinates in VI6\_CLU\_ADDR.
  - (4) Write the next data to be set in VI6\_CLU\_DATA.
- ... Execute these processes in a similar manner.

Accesses to VI6\_CLU\_ADDR and VI6\_CLU\_DATA registers are repeated in this way. The location where to access the CLU table to write the VI6\_CLU\_DATA contents immediately takes effect after a value is set in the VI6\_CLU\_ADDR register.

To read-access the CLU table continuously, change the write-access operation to the read-access operation in the sequence of processes of (1) to (4) above.

The following describes how to specify VI6\_CLU\_ADDR.



**Figure 28.52 VI6\_CLU\_ADDR Setting**

In the CLU table, a table value should be specified for every increase by H'10 along each of the axes and for every intersection between two axes. For a certain axis, as shown in the top right of Figure 28.52, a value to be set in the table



corresponds to a scale mark at an interval of H'10. The location of a point between two scale marks (for example, point X in Figure 28.52) is calculated through interpolation by the CLU (refer to section 28.2.13.1). Accordingly, the lower four bits of table settings for each axis has no meaning; only the upper-order five bits of the desired coordinate for each component should be specified in VI6\_CLU\_ADDR (which should be shifted to the right by four bits) as shown in Figure 28.52.

**Table 28.39 Address Spaces Used in Indirect Addressing to CLU Table**

Address (Name)	Bit	Initial Value	R/W	Description	RZ/G Series Products			
					RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
\$VSP_BASE + H'7400 (VI6_CLU_ADDR)	31 to 24	All 0	R	Reserved  These bits are always read as 0. The write value should always be 0.	√	√	√	√
	23 to 16	All 0	R/W	Coordinate Value of First Axis  These bits set the coordinate value of the first axis on the three-dimensional space coordinates of the CLU table. A value from 0 to 16 can be specified.	√	√	√	√
	15 to 8	All 0	R/W	Coordinate Value of Second Axis  These bits set the coordinate value of the second axis on the three-dimensional space coordinates of the CLU table. A value from 0 to 16 can be specified.	√	√	√	√
	7 to 0	All 0	R/W	Coordinate Value of Third Axis  These bits set the coordinate value of the third axis on the three-dimensional space coordinates of the CLU table. A value from 0 to 16 can be specified when the CLU is in 3D mode. In 2D mode, these bits must be set to 0.	√	√	√	√
\$VSP_BASE + H'7404 (VI6_CLU_DATA)	31 to 24	Undefined	R	Reserved  These bits are always read as 0. The write value should always be 0.	√	√	√	√
	23 to 16	Undefined	R/W	Component Value of First Axis  These bits set the component value of the first axis on the three-dimensional space coordinates of the CLU table, which is defined by the VI6_CLU_ADDR register.  A value from 0 to 255 can be specified when the CLU is in 3D mode. In 2D mode, these bits must be set to 0.	√	√	√	√

Address (Name)	Bit	Initial Value	R/W	Description	RZ/G Series Products			
					RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
\$VSP_BASE + H'7404 (VI6_CLU_DATA)	15 to 8	Undefined	R/W	Component Value of Second Axis  These bits set the component value of the second axis on the three-dimensional space coordinates of the CLU table, which is defined by the VI6_CLU_ADDR register.  A value from 0 to 255 can be specified.	√	√	√	√
	7 to 0	Undefined	R/W	Component Value of Third Axis  These bits set the component value of the third axis on the three-dimensional space coordinates of the CLU table, which is defined by the VI6_CLU_ADDR register.  A value from 0 to 255 can be specified when the CLU is in 3D mode. In 2D mode, these bits must be set to 0.	√	√	√	√

## 28.4 Operation Linked with Display Unit (DU)

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

### 28.4.1 Starting LCD Display

Use the following procedure to display images on the LCD by operating the VSP1 and DU together.

To display images on the LCD by inputting VSYNC to the DU:

- (1) Activate the VSP1.
- (2) After the VSP1 starts operation, wait until a VI6\_DISP\_IRQ\_STA.DST interrupt source is generated.
- (3) After a VI6\_DISP\_IRQ\_STA.DST interrupt source is generated, activate the DU.

To display images on the LCD with VSYNC being output from the DU:

- (1) Activate the VSP.
- (2) After that, activate the DU.

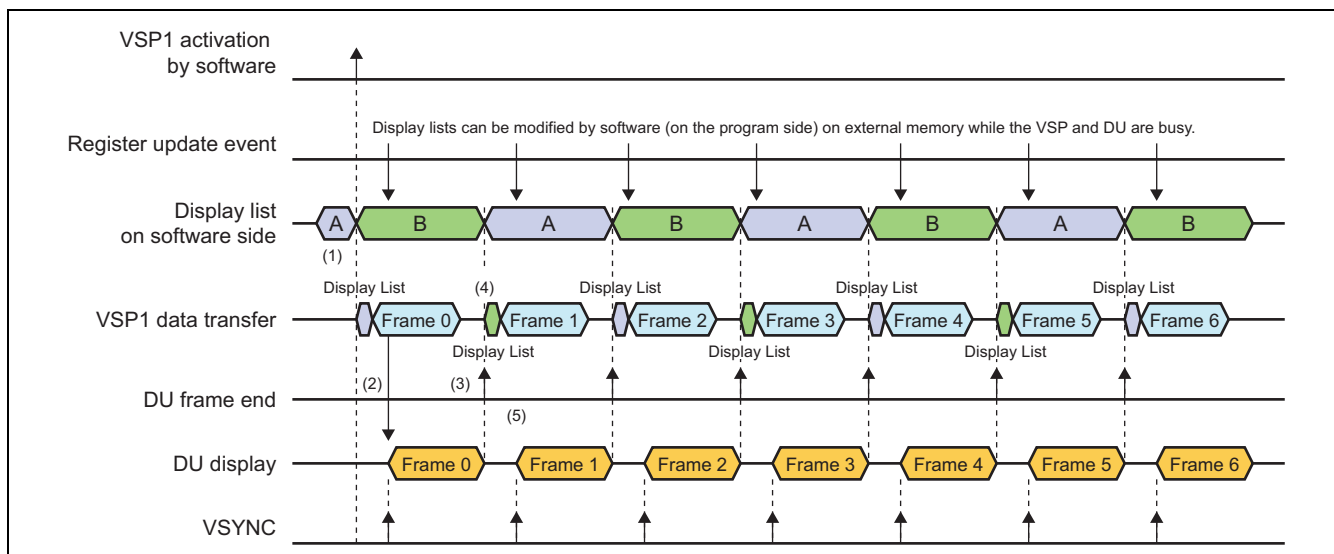
### 28.4.2 Stopping LCD Display

To stop the image display on the LCD while the VSP1 and DU work together to display images, stop the DU first by a software reset or the like (refer to section 21, Display Unit (DU) for the software reset of the DU). After checking that the DU has stopped, apply software reset to the VSP1. After both the DU and VSP1 software reset processes are complete, the LCD display stop process ends.

### 28.4.3 Entire Operation Flow

The VSP1 operation is linked with the DU operation. As the DU operates in real-time, the VSP1 also operates in real-time. However, the VSP1 only provides one plane of registers. Accordingly, modifying registers between frames should be done within the short blanking period between the end of one-frame display (VI6\_WPFn\_IRQ\_STA.FRE interrupt) and the start of the next frame display (VSYNC). To do this, use the display list function of the VSP1 (see section 28.1.8 (3)) to implement two virtual register planes and ensure the one-frame time for modifying registers by software (see section 28.4.4). When using the display list function, make the current-frame settings in a register plane and store the next-frame settings as a display list in external memory such as SDRAM. In this way, the next-frame settings can be modified in the display list in external memory until the end of the current frame processing.

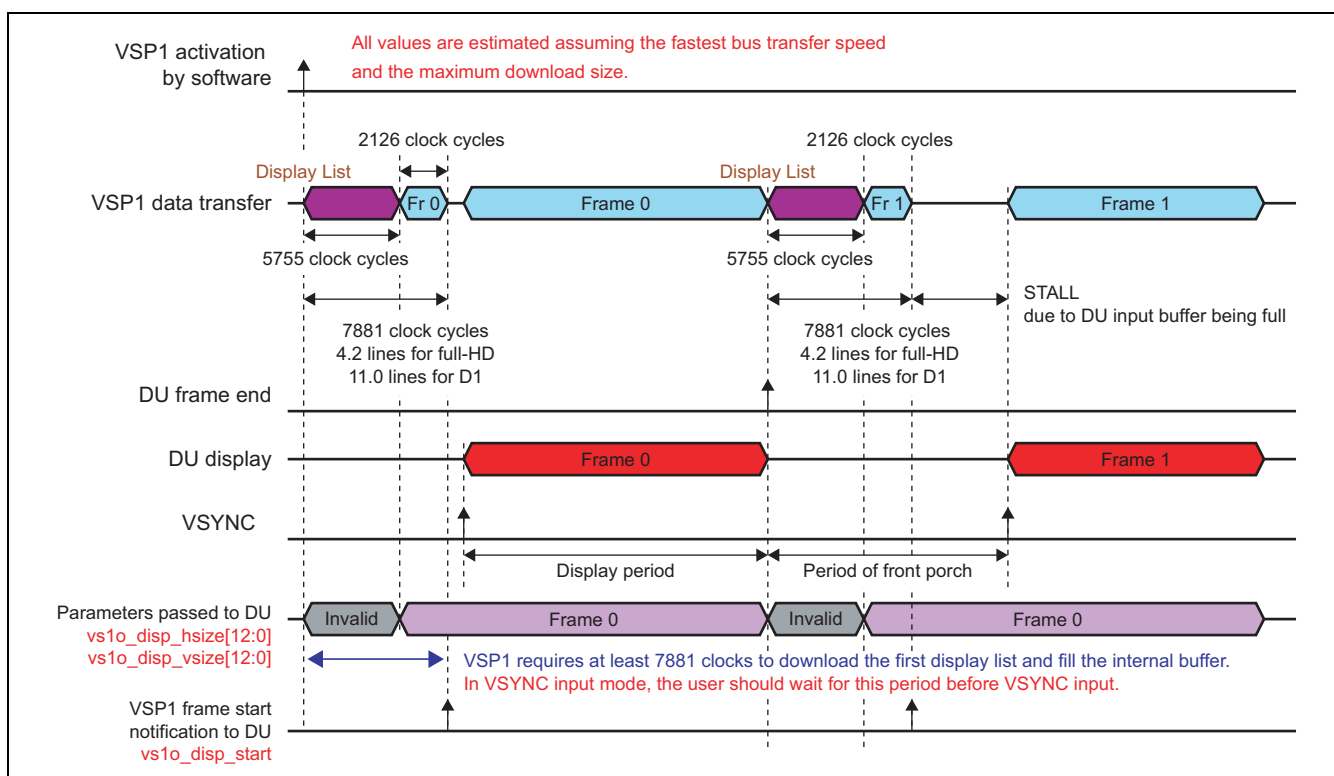
The timing chart of this procedure is shown in Figure 28.53



**Figure 28.53 Timing when VSP1 Operation is linked with DU**

- (1) The VSP1 is activated by software, and then the VSP1 downloads a display list.
- (2) The VSP1 informs the ready state to the DU, and then the DU starts the display process.
- (3) The DU generates a frame end interrupt.
- (4) The VSP updates its register settings by downloading the next display list. After that, the VSP reads the next frame data.
- (5) The DU generates VSYNC for the next frame and starts transfer of display data.

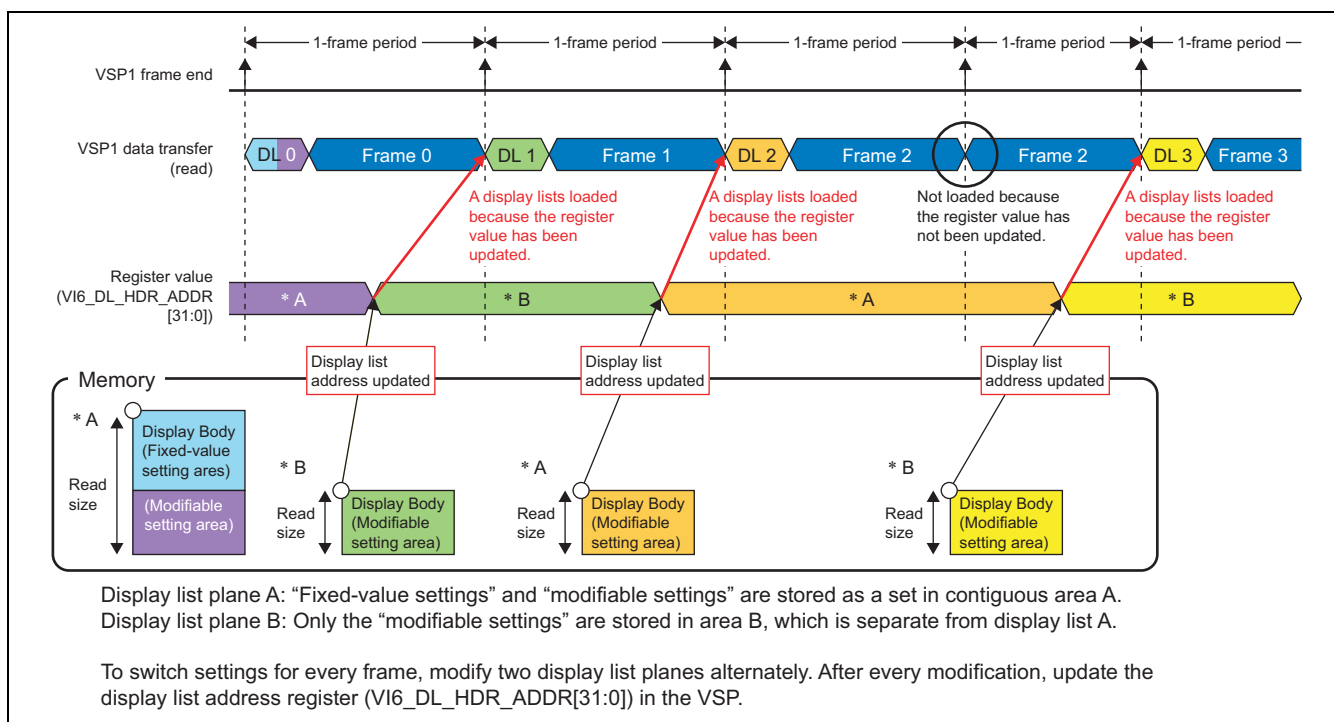
Figure 28.53 shows the detailed timing of frame switching. The number of VSP1 operating clock cycles necessary for each timing is shown as a reference value in Figure 28.54 where it is assumed that the bus transfer is at the logically fastest speed and the size of the display list to be downloaded is the worst case (downloading of data for all registers and tables in the VSP1).



**Figure 28.54 Detailed Timing of Frame Switching**

### 28.4.4 Controlling Two Register Planes Using Display Lists

Figure 28.55 shows the control of two register planes using header-less display lists (see section 28.1.8 (3)) and its timing. In the description hereafter, the use of header-less display lists is always assumed and they are simply called display lists.



**Figure 28.55 Controlling Two Register Planes Using a Display List**

The VSP1 downloads a display list immediately after activation. In the start frame, download the display list that contains all necessary settings. From the next frame on, only the necessary register or table values should be specified in a display list.

Only when the destination address (VI6\_DL\_HDR\_ADDR0; see section 28.2.6.2) or the display body size (VI6\_DL\_BODY\_SIZE0; see section 28.2.6.5) has been written to, the VSP1 downloads a new display list at the start of the next frame. When the update flag of VI6\_DL\_BODY\_SIZE0.UPD0 is set to 0, the register settings acquired from the display list previously downloaded are retained and used for the next operation without downloading a new display list.

## 28.5 Assignment in Memory Space

RZ/G1H	RZ/G1N
RZ/G1M	RZ/G1E

Make sure that VSP1 memory space shall be mapped to Non-Cache region.

## 29. Image Extraction Direct Memory Access Controller (2D-DMAC)

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

This LSI has an image extraction direct memory access controller (2D-DMAC). This module reads the image data in the frame buffer memory, performs image extraction/shift/simple magnification and format conversion, and then rewrites the processed image data to the frame buffer memory.

### 29.1 Features

- Image extraction  
2D-DMAC extracts an image in the rectangular area from a point (Sx, Sy) shifting from the source image data origin to a point in the frame memory, and then writes the extracted image data to another frame memory. Extraction of data is possible in two-pixel units for YCbCr formats and in one-pixel units for RGB formats. This function is available for image clipping and image motion compensation.
- Image rotation/inversion  
Vertical/horizontal inversion and the 90°/270° rotation can be performed.
- Simple enlargement  
When writing a destination image, it can simply be enlarged twice in the X and Y directions.
- Format conversion  
RGB formats can be converted to each other.  
YCbCr formats (YCbCr4:2:0 and YCbCr4:2:2) can be converted to each other.  
No format conversion is possible between RGB and YCbCr.  
The format conversion method is equivalent to that of VSP.
- Channels  
Settings for eight channels are enabled. For the YCbCr formats, settings for one channel for each Y plane and C plane are enabled. Therefore, concurrent processing is possible for up to four planes (YCbCr formats) or up to eight planes (RGB formats).  
Provided with an outstanding buffer for each channel, even if data transfer of a channel is blocked, 2D-DMAC can continue operation of other channels. Transition of processing between channels is performed upon completion of each line processing.
- Interrupt  
Each channel has interrupt request signals that can be output at the time of data transfer half end and data transfer end respectively.

Figure 29.1 shows a block diagram of 2D-DMAC and Figure 29.2 shows a flow for the pixel processing block.

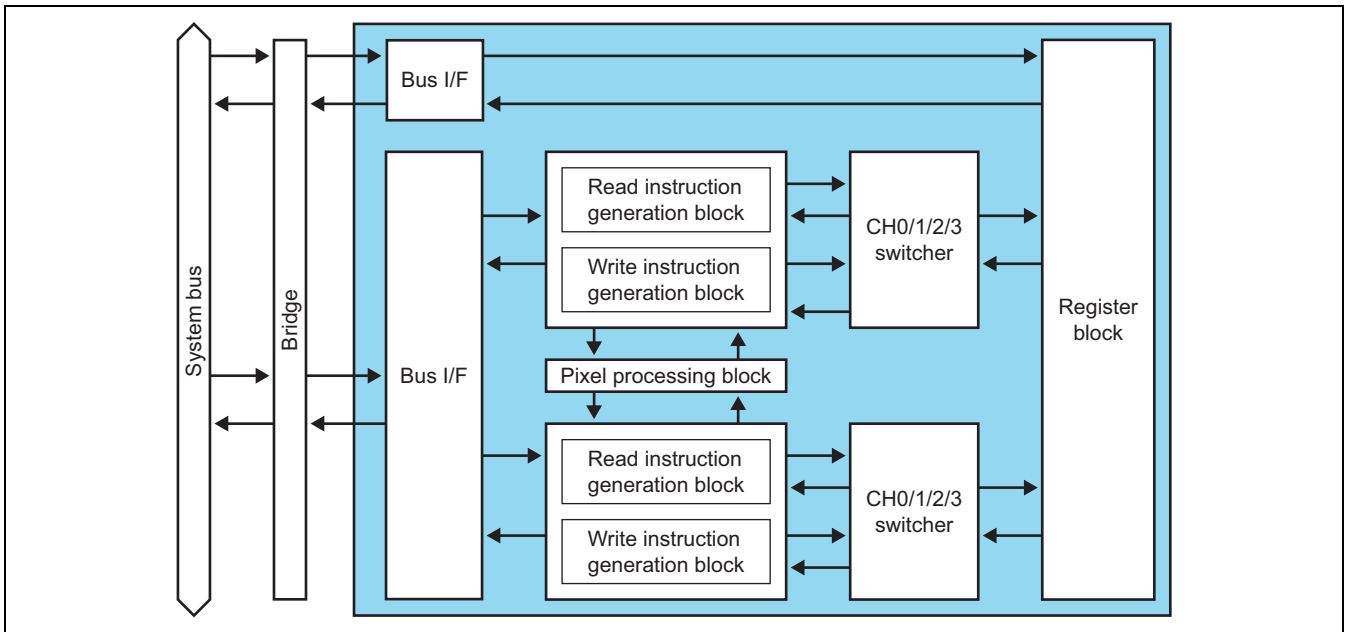


Figure 29.1 Block Diagram of 2D-DMAC

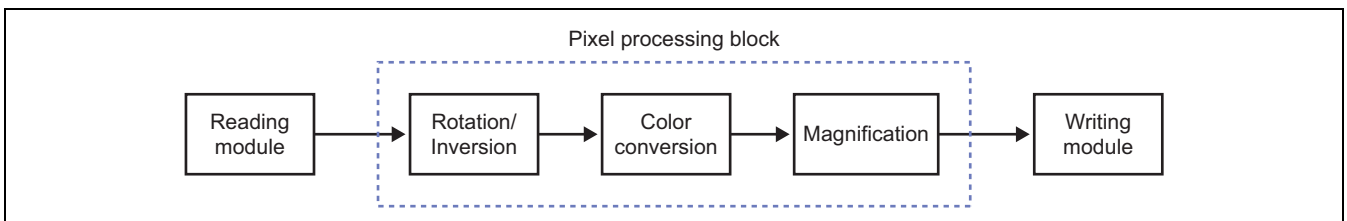


Figure 29.2 Block Flow of Pixel Block



## 29.2 Register Descriptions

Table 29.1 lists the registers used in 2D-DMAC. Table 29.2 shows the register status in each processing mode.

**Table 29.1 Register Configuration**

Register Name	Abbreviation	R/W	Address	Access Size	RZ/G Series Products			
					RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Transaction control register	CHTCTRL	R/W	H'FEA0 0008	32	√	√	√	√
Interrupt status clear register	CHSTCLR	R/W	H'FEA0 0010	32	√	√	√	√
CH0 control register	CH0CTRL	R/W	H'FEA0 0020	32	√	√	√	√
CH1 control register	CH1CTRL	R/W	H'FEA0 0024	32	√	√	√	√
CH2 control register	CH2CTRL	R/W	H'FEA0 0028	32	√	√	√	√
CH3 control register	CH3CTRL	R/W	H'FEA0 002C	32	√	√	√	√
CH4 control register	CH4CTRL	R/W	H'FEA0 0120	32	√	√	√	√
CH5 control register	CH5CTRL	R/W	H'FEA0 0124	32	√	√	√	√
CH6 control register	CH6CTRL	R/W	H'FEA0 0128	32	√	√	√	√
CH7 control register	CH7CTRL	R/W	H'FEA0 012C	32	√	√	√	√
CH0 input/output swap register	CH0SWAP	R/W	H'FEA0 0030	32	√	√	√	√
CH1 input/output swap register	CH1SWAP	R/W	H'FEA0 0034	32	√	√	√	√
CH2 input/output swap register	CH2SWAP	R/W	H'FEA0 0038	32	√	√	√	√
CH3 input/output swap register	CH3SWAP	R/W	H'FEA0 003C	32	√	√	√	√
CH4 input/output swap register	CH4SWAP	R/W	H'FEA0 0130	32	√	√	√	√
CH5 input/output swap register	CH5SWAP	R/W	H'FEA0 0134	32	√	√	√	√
CH6 input/output swap register	CH6SWAP	R/W	H'FEA0 0138	32	√	√	√	√
CH7 input/output swap register	CH7SWAP	R/W	H'FEA0 013C	32	√	√	√	√
CH0 source address register	CH0SAR	R/W	H'FEA0 0080	32	√	√	√	√
CH0 destination address register	CH0DAR	R/W	H'FEA0 0084	32	√	√	√	√
CH0 destination pixel register	CH0DPXL	R/W	H'FEA0 0088	32	√	√	√	√
CH0 source format register	CH0SFMT	R/W	H'FEA0 008C	32	√	√	√	√
CH0 destination format register	CH0DFMT	R/W	H'FEA0 0090	32	√	√	√	√
CH0 source line address register	CH0SARE	R	H'FEA0 0094	32	√	√	√	√
CH0 destination line address register	CH0DARE	R	H'FEA0 0098	32	√	√	√	√
CH0 destination pixel processing Register	CH0DPXLE	R	H'FEA0 009C	32	√	√	√	√
CH1****	CH1****	—	H'FEA0 00A0 to H'FEA0 00BC	32	√	√	√	√
CH2****	CH2****	—	H'FEA0 00C0 to H'FEA0 00DC	32	√	√	√	√
CH3****	CH3****	—	H'FEA0 00E0 to H'FEA0 00FC	32	√	√	√	√
CH4****	CH4****	—	H'FEA0 0180 to H'FEA0 019C	32	√	√	√	√

Register Name	Abbreviation	R/W	Address	Access Size	RZ/G Series Products			
					RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
CH5****	CH5****	—	H'FEA0 01A0 to H'FEA0 01BC	32	√	√	√	√
CH6****	CH6****	—	H'FEA0 01C0 to H'FEA0 01DC	32	√	√	√	√
CH7****	CH7****	—	H'FEA0 01E0 to H'FEA0 01FC	32	√	√	√	√

**Table 29.2 Register Status in Each Processing Mode**

Abbreviation	Power-on Reset	Module Standby
CHSTCLR	Initialized	Retained
CHnCTRL	Initialized	Retained
CHnSWAP	Initialized	Retained
CHnSAR	Initialized	Retained
CHnDAR	Initialized	Retained
CHnDPXL	Initialized	Retained
CHnSFMT	Initialized	Retained
CHnDFMT	Initialized	Retained
CHnSARE	Initialized	Retained
CHnDARE	Initialized	Retained
CHnDPXLE	Initialized	Retained

Note n: 0 to 7

**29.2.1 Transaction Control Register (CHTCTRL)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CHTCTRL register is a 32-bit readable/writeable register that controls bus transaction among all channels.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	OUT	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 6	—	All 0	R	Reserved These bits are read as 0. The write value should be 0.
5	OUT	0	R/W	Transaction control When operating 2D-DMAC, this bit should always be 1.
4 to 0	—	All 0	R	Reserved These bits are read as 0. The write value should be 0.

### 29.2.2 Control Registers (CHnCTRL)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CHnCTRL (n = 0 to 7) is a 32-bit readable/writable register that controls transfer mode.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	HMRR	VMRR	ROTL	ROTR	—	MX	—	MY	HIE	HE	TIE	TE	LINK[1] /—	LINK[0] /—	STP	DMAE N
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15	HMRR	0	R/W	Horizontal Inversion (symmetric to the vertical axis) The source image inverted horizontally is output. See Table 29.5 for details on the relations between this bit and inversion/rotation. 0: Horizontal inversion is not performed. 1: Inverted horizontally source image is output.
14	VMRR	0	R/W	Vertical Inversion (symmetric to the horizontal axis) The source image inverted vertically is output. See Table 29.5 for details on the relations between this bit and inversion/rotation. 0: Vertical inversion is not performed. 1: Inverted vertically source image is output.
13	ROTL	0	R/W	270° Rotation (clockwise) The source image rotated 270° is output. When this bit is 1, set the ROTR bit to 0. See Table 29.5 for details on the relations between this bit and inversion/rotation. 0: 270° rotation is not performed. 1: Rotated 270° source image is output.
12	ROTR	0	R/W	90° Rotation (clockwise) The source image rotated 90° is output. When this bit is 1, set the ROTR bit to 0. See Table 29.5 for details on the relations between this bit and inversion/rotation. 0: 90° rotation is not performed. 1: Rotated 90° source image is output.
11	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
10	MX	0	R/W	Magnify X Direction 0: No magnification 1: Outputs with double magnification in the X direction. When ROTR or ROTL is 1, set this bit to 0.

Bit	Bit Name	Initial Value	R/W	Description
9	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
8	MY	0	R/W	Magnify Y Direction 0: No magnification 1: Outputs with double magnification in the Y direction. When ROTR or ROTL is 1, set this bit to 0.
7	HIE	0	R/W	Half End Interrupt Enable Specifies whether to output the half end flag as an interrupt request. 0: A half end interrupt is disabled. 1: A half end interrupt is enabled.
6	HE	0	R/W	Half End Indicates that data transfer for half the setting lines has been completed. This bit is set to 1 when the DVPXLE bit in CHnDPXLE becomes half (a value of 1-bit right shift) of the DVPXL bit value in CHnDPXL that was set before starting transfer. If CHnCTRL.ROTR = 1 or CHnCTRL.ROTL = 1, this bit is set to 1 when the DHPXLE bit in CHnDPXLE becomes half of the DHPXL bit value in CHnDPXL that was set before starting transfer. Only clearing to 0 after reading 1 is enabled. Clearing by the CHSTCLR register is also enabled.
5	TIE	0	R/W	Transfer End Interrupt Enable Specifies whether to output the transfer end flag as an interrupt request. 0: A transfer end interrupt is disabled. 1: A transfer end interrupt is enabled.
4	TE	0	R/W	Transfer End This bit is set to 1 when the DVPXL bit in CHxDPXL that was set by the DVPXLE bit in CHxDPXLE before starting transfer and the entire DMA transfer are completed. When this bit is set to 1, the DMAEN bit is automatically cleared. Only clearing to 0 after reading 1 is enabled. Clearing by the CHSTCLR register is also enabled.

Bit	Bit Name	Initial Value	R/W	Description
3, 2	LINK[1:0] (n = 0, 2, 4, 6) — (n = 1, 3, 5, 7)	00	R/W  R  R	<p>(n = 0, 2, 4, 6) Link Transfer Mode</p> <p>This mode enables alternate block line transfers between a master channel (CHn) and a slave channel (CHn+1). When these bits are set to 10, specify the DVPXL bit in CH(n+1)DPXL equal to half of the DVPXL in CHnDPXL. When these bits are set to 11, specify the DVPXL bit in CH(n+1)DPXL equal to the DVPXL in CHnDPXL.</p> <p>In this mode, start the transfer of the master channel before that of the slave channel.</p> <p>00: Link transfer mode is disabled. 01: Setting prohibited. 10: A block line transfer of a slave channel is performed every two block line transfers of a master channel. 11: Alternate transfers are performed.</p> <p>(n = 1, 3, 5, 6) Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>
1	STP	0	R/W	<p>Transfer Stop</p> <p>Stops DMA transfer temporarily. When this bit is set to 1, DMA transfer is suspended upon completion of the line that is being transferred, and the DMAEN bit is cleared to 0. At this time, this bit is also cleared.</p> <p>To restart DMA transfer after that, set the DMAEN bit to 1. To reset the operation of a channel, rewrite data to the SAR, DAR, and DPXL registers of the channel.</p> <p>[Writing] 0: NOP 1: Stops DMA transfer temporarily.</p> <p>[Reading] 0: Transfer is in progress or suspended. 1: Pending until the line being transferred is completed</p>
0	DMAEN	0	R/W	<p>DMA Transfer Enable</p> <p>Enables DMA transfer. Only writing 1 is enabled. This bit shows 1 during transfer, and is automatically cleared when a DMA transfer is completed.</p> <p>Writing 0 to this bit is disabled. A DMA transfer can be suspended by setting the STP bit to 1.</p> <p>[Writing] 0: NOP 1: Performs DMA transfer.</p> <p>[Reading] 0: No DMA transfer is in progress. 1: A DMA transfer is in progress.</p>

**29.2.3 Input/Output Swap Register (CHnSWAP)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CHnSWAP (n = 0 to 7) controls 64-bit data swapping in the data input/output section of 2D-DMAC.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	OLS	OWS	OBS	—	ILS	IWS	IBS
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 7	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
6	OLS	0	R/W	Output Longword Swap Setting In the output section of 2D-DMAC, 64 bits of data are swapped with 32 bits of the MSB and 32 bits of the LSB in longword units. 0: Output longword swap is not performed. 1: Output longword swap is performed.
5	OWS	0	R/W	Output Word Swap Setting In the output section of 2D-DMAC, 64 bits of data are swapped with 32 bits of the MSB and 32 bits of the LSB in word units. 0: Output word swap is not performed. 1: Output word swap is performed.
4	OBS	0	R/W	Output Byte Swap Setting In the output section of 2D-DMAC, 64 bits of data are swapped with 16-bit groups in byte units. 0: Output byte swap is not performed. 1: Output byte swap is performed.
3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
2	ILS	0	R/W	Input Longword Swap Setting In the input section of 2D-DMAC, 64 bits of data are swapped with 32 bits of the MSB and 32 bits of the LSB in longword units. 0: Input longword swap is not performed. 1: Input longword swap is performed.
1	IWS	0	R/W	Input Word Swap Setting In the input section of 2D-DMAC, 64 bits of data are swapped with 32 bits of the MSB and 32 bits of the LSB in word units. 0: Input word swap is not performed. 1: Input word swap is performed.

Bit	Bit Name	Initial Value	R/W	Description
0	IBS	0	R/W	Input Byte Swap Setting In the input section of 2D-DMAC, 64 bits of data are swapped with 16-bit groups in byte units. 0: Input byte swap is not performed. 1: Input byte swap is performed.

When the system is operated in little-endian mode, this register should be used to select the swapping method conforming to the input/output format. The data relationships available when swapping methods are set are shown in Figures 29.3, 29.4, and 29.5.

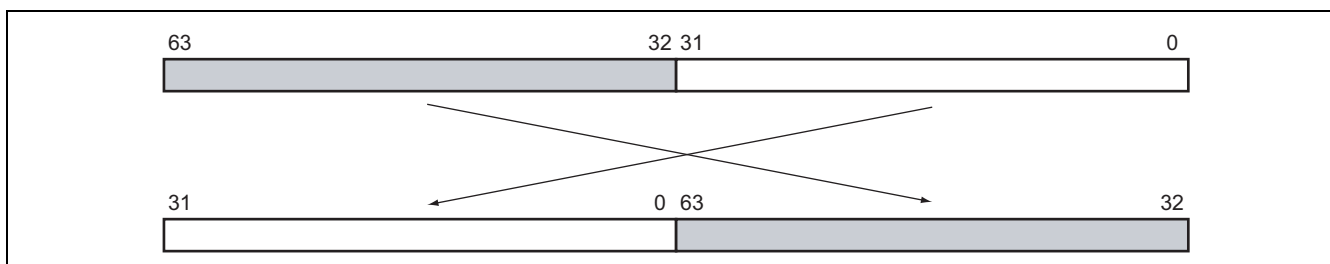


Figure 29.3 Data Relationship Before and After Longword Swapping

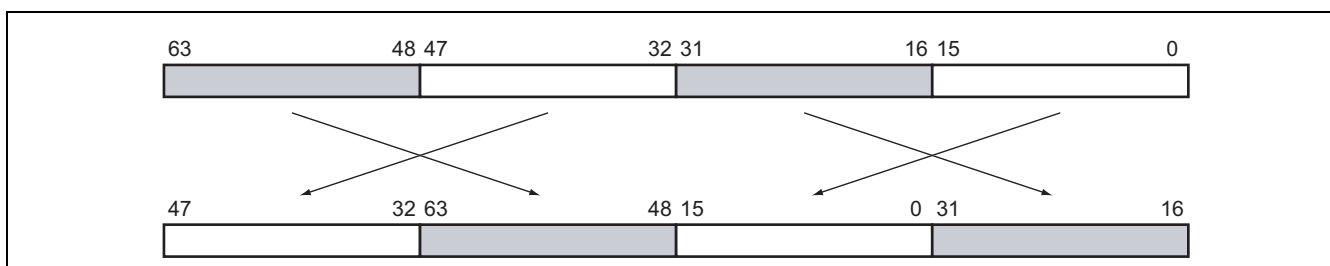


Figure 29.4 Data Relationship Before and After Word Swapping

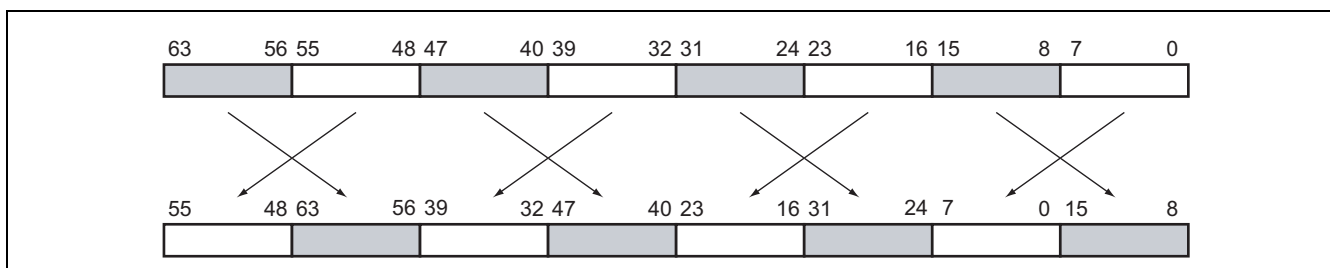


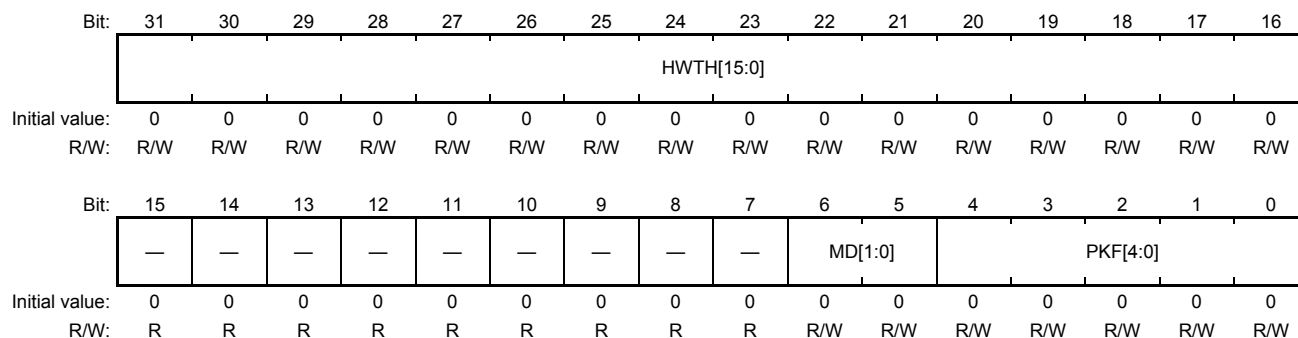
Figure 29.5 Data Relationship Before and After Byte Swapping



### 29.2.4 Source Format Registers (CHnSFMT)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CHnSFMT (n = 0 to 7) is a 32-bit readable/writable register for setting the source image.



Bit	Bit Name	Initial Value	R/W	Description
31 to 16	HWTH[15:0]	H'0000	R/W	Source Image Horizontal Byte Size Specify the one-line width of the source image in units of bytes. This value should be a multiple of the pack size. When ROTR or ROTL is 1, set these bits to 16n.
15 to 7	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
6, 5	MD[1:0]	00	R/W	Source Image Format 00: RGB data 01: Y data 10: CbCr data (YCbCr4:2:0) 11: CbCr data (YCbCr4:2:2)
4 to 0	PKF[4:0]	00000	R/W	Source Image RGB Data Packed Format Specify the packed format for source image data in the RGB format. These bits are available only when MD = 00. Table 29.3 shows the packed RGB formats.

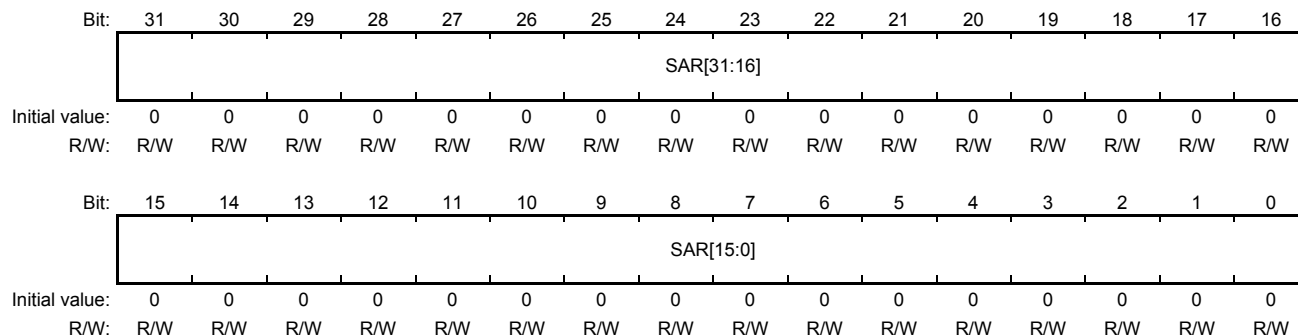
**Table 29.3 Packed RGB Formats**

PKF[4:0]	Format	Bit Rate	Phase	Bit field																																											
				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0												
B'00000	ARGB8888	24	—	a	a	a	a	a	a	a	a	a	a	a	a	a	a	R0	R0	R0	R0	R0	R0	R0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	B0	B0	B0		
B'00001	RGBA8888	24	—	R0	R0	R0	R0	R0	R0	R0	R0	R0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	B0	B0	B0	B0	a	a	a	a	a	a	a	a	
B'00010	RGB888	24	0	R0	R0	R0	R0	R0	R0	R0	R0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	B0	B0	B0	B0	R1	R1	R1	R1	R1	R1	R1	R1		
			1	G1	G1	G1	G1	G1	G1	G1	G1	G1	G1	G1	G1	G1	B1	B1	B1	B1	B1	B1	B1	B1	B1	B1	B1	B1	R2	R2	R2	R2	R2	R2	R2	R2	R2	G2	G2	G2	G2	G2	G2	G2	G2		
			2	B2	B2	B2	B2	B2	B2	B2	B2	B2	B2	B2	B2	B2	R3	R3	R3	R3	R3	R3	R3	R3	R3	R3	R3	R3	G3	G3	G3	G3	G3	G3	G3	G3	G3	B3	B3	B3	B3	B3	B3	B3	B3		
B'00011	RGB565	16	—																									R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	B0		
B'00100	RGB332	8	—																																												
B'00111	pRGB14-666	18	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	B0		
B'01000	pRGB4-444	12	—																									0	0	0	0	0	R0	R0	R0	R0	G0	G0	G0	G0	B0	B0	B0	B0	B0	B0	
B'01001	RGB666	18	0	0	0	R0	R0	R0	R0	R0	R0	0	0	G0	G0	G0	G0	G0	G0	0	0	B0	B0	B0	B0	B0	B0	0	0	R1	R1	R1	R1	R1	R1	R1	R1	R1	R1	R1	R1	R1	R1	R1	R1	R1	
			1	0	0	G1	G1	G1	G1	G1	G1	0	0	B1	B1	B1	B1	B1	B1	0	0	R2	R2	R2	R2	R2	R2	0	0	G2	G2	G2	G2	G2	G2	G2	G2	G2	G2	G2	G2	G2	G2	G2	G2	G2	
			2	0	0	B2	B2	B2	B2	B2	B2	0	0	R3	R3	R3	R3	R3	R3	0	0	G3	G3	G3	G3	G3	G3	0	0	B3	B3	B3	B3	B3	B3	B3	B3	B3	B3	B3	B3	B3	B3	B3	B3	B3	B3
B'01010	BGR666	18	0	0	0	B0	B0	B0	B0	B0	B0	0	0	G0	G0	G0	G0	G0	G0	0	0	R0	R0	R0	R0	R0	R0	0	0	B1	B1	B1	B1	B1	B1	B1	B1	B1	B1	B1	B1	B1	B1	B1	B1	B1	B1
			1	0	0	G1	G1	G1	G1	G1	G1	0	0	R1	R1	R1	R1	R1	R1	0	0	B2	B2	B2	B2	B2	B2	0	0	G2	G2	G2	G2	G2	G2	G2	G2	G2	G2	G2	G2	G2	G2	G2	G2	G2	G2
			2	0	0	R2	R2	R2	R2	R2	R2	0	0	B3	B3	B3	B3	B3	B3	0	0	G3	G3	G3	G3	G3	G3	0	0	R3	R3	R3	R3	R3	R3	R3	R3	R3	R3	R3	R3	R3	R3	R3	R3	R3	R3
B'01011	BGR888	24	0	B0	B0	B0	B0	B0	B0	B0	B0	G0	G0	G0	G0	G0	G0	G0	R0	R0	R0	R0	R0	R0	R0	R0	R0	B1	B1	B1	B1	B1	B1	B1	B1	B1	B1	B1	B1	B1	B1	B1	B1	B1	B1	B1	B1
			1	G1	G1	G1	G1	G1	G1	G1	R1	R1	R1	R1	R1	R1	R1	R1	R1	B2	B2	B2	B2	B2	B2	B2	B2	G2	G2	G2	G2	G2	G2	G2	G2	G2	G2	G2	G2	G2	G2	G2	G2	G2	G2	G2	G2
			2	R2	R2	R2	R2	R2	R2	R2	B3	B3	B3	B3	B3	B3	B3	B3	B3	G3	G3	G3	G3	G3	G3	G3	G3	R3	R3	R3	R3	R3	R3	R3	R3	R3	R3	R3	R3	R3	R3	R3	R3	R3	R3	R3	R3
B'01100	ABGR888	24	—	a	a	a	a	a	a	a	a	a	a	a	a	a	B0	B0	B0	B0	B0	B0	B0	B0	B0	B0	B0	G0	G0	G0	G0	G0	G0	G0	G0	R0	R0	R0	R0	R0	R0	R0	R0				
B'01101	RGB565	16	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	B0			

**29.2.5 Source Address Registers (CHnSAR)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CHnSAR (n = 0 to 7) is a 32-bit readable/writable register for setting the transfer start address of the source image.



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	SAR[31:0]	H'00000000	R/W	Source Image Extraction Start Address Specify the address of the extraction start pixel in the source image data.

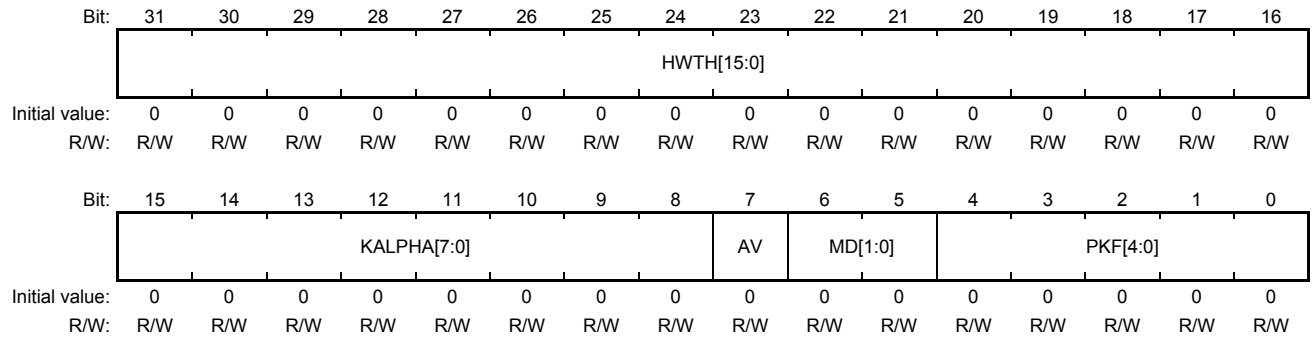
When the source image fills CHnSAR ≠ 16n and cutting out effective pixel bytes number ≤ 16-byte, line finality access = address where line terminal address is rounded up to 16n + 16-byte.

Address where source image final pixel address of cutting out object is rounded up to 16n + 16, secure it as an input image area.

### 29.2.6 Destination Format Registers (CHnDFMT)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CHnDFMT (n = 0 to 7) is a 32-bit readable/writable register for setting a destination image format and so on.

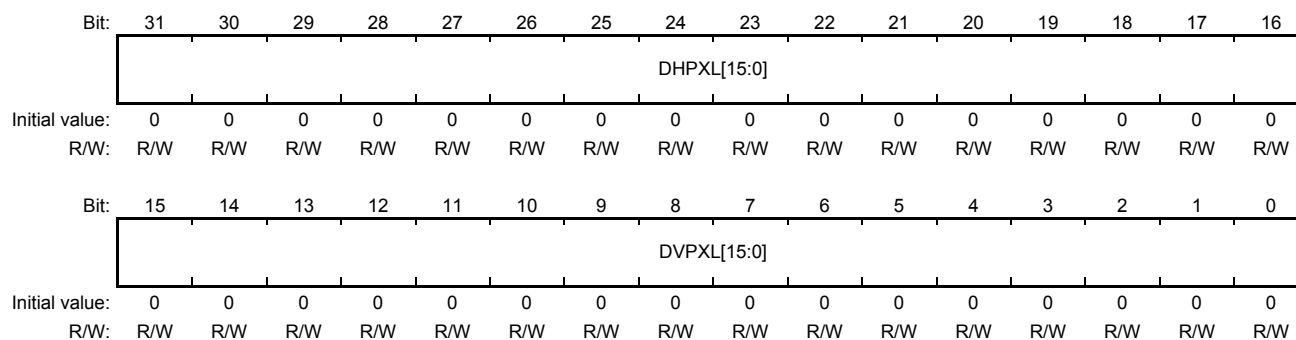


Bit	Bit Name	Initial Value	R/W	Description
31 to 16	HWTH[15:0]	H'0000	R/W	Destination Image Horizontal Byte Size Specify the one-line width of the destination image in units of bytes. Set a multiple of 16. When CTRL.MX is 1, set a value after magnification.
15 to 8	KALPHA[7:0]	H'00	R/W	Alpha Value Specify an alpha value used for output if the source image is in a format without alpha or the AV bit is set to 0.
7	AV	0	R/W	Alpha Enable 0: Disables the alpha value when the source image is in a format with alpha. When the output is in a format with alpha, the KALPHA value is output. 1: Enables the alpha value when the source image is in a format with alpha, and outputs the alpha value when the output is in a format with alpha.
6, 5	MD[1:0]	00	R/W	Destination Image Format 00: RGB data 01: Y data 10: CbCr data (YCbCr4:2:0) 11: CbCr data (YCbCr4:2:2)
4 to 0	PKF[4:0]	00000	R/W	Destination Image RGB Data Packed Format Specify the packed format for destination image data in the RGB format. These bits are available only when MD = 00. Table 29.3 shows the packed RGB formats.

### 29.2.7 Destination Pixel Registers (CHnDPXL)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

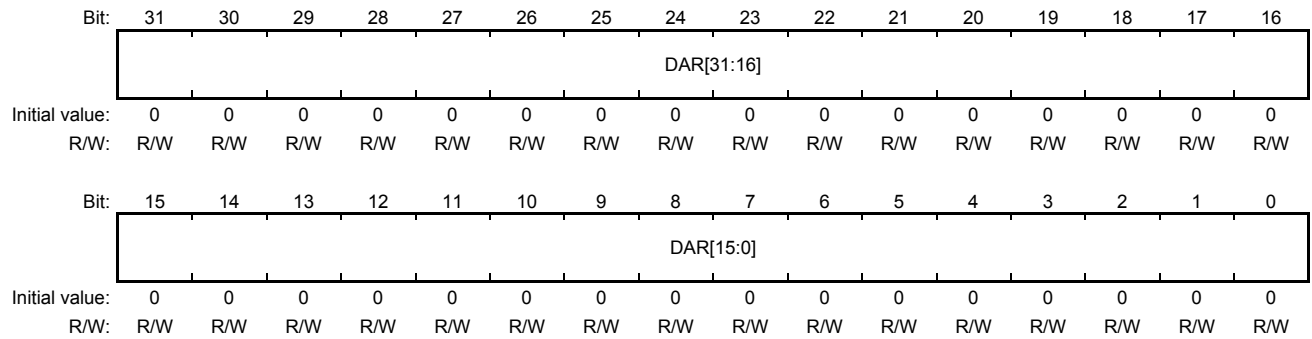
CHnDPXL (n = 0 to 7) is a 32-bit readable/writable register for setting the horizontal pixel size and vertical pixel size of the destination image.



Bit	Bit Name	Initial Value	R/W	Description
31 to 16	DHPXL[15:0]	H'0000	R/W	<p>Destination Image Horizontal Pixel Size</p> <p>Specify the horizontal pixel size of the destination image. When the MX bit in CTRL is 1, set a value before magnification.</p> <p>For the CbCr plane in YCbCr4:2:2 or YCbCr4:2:0, set a value of half of the number of pixels.</p> <p>The minimum pixel size will be 1; set 1 or a larger value.</p>
15 to 0	DVPXL[15:0]	H'0000	R/W	<p>Destination Image Vertical Pixel Size</p> <p>Specify the vertical pixel size of the destination image. When the MY bit in CTRL is 1, set a value before magnification.</p> <p>For the CbCr plane in YCbCr4:2:0, set a value of half of the number of lines.</p> <p>The minimum pixel size will be 1; set 1 or a larger value.</p>

### 29.2.8 Destination Address Registers (CHnDAR)

CHnDAR (n = 0 to 7) is a 32-bit readable/writable register for setting the transfer start address of the destination image.

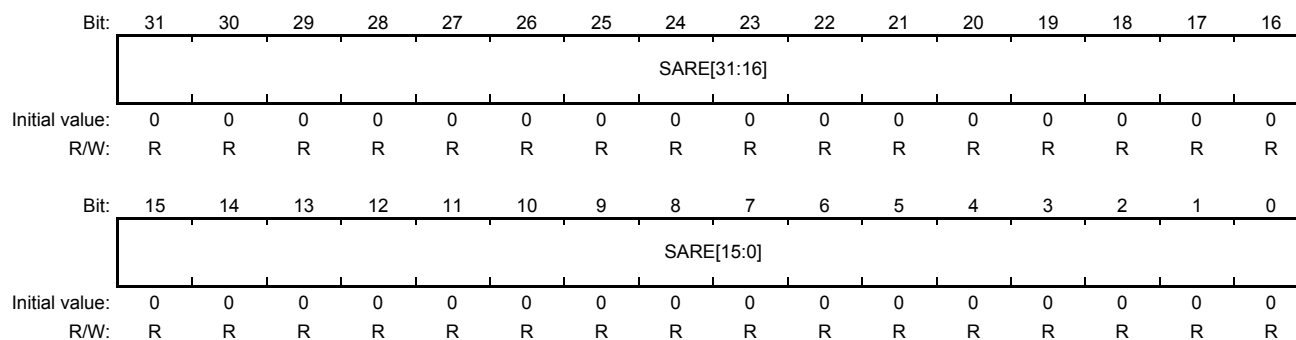


Bit	Bit Name	Initial Value	R/W	Description
31 to 0	DAR[31:0]	H'00000000	R/W	Specify the start address of the destination image. Only a multiple of 16 can be set.  The specified address point is to be changed according to the settings to the VMRR, HMRR, ROTR, ROTL, and MY bits. For details, see section 29.3.2, Image Rotation/Inversion.

### 29.2.9 Source Line Address Registers (CHnSARE)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CHnSARE (n = 0 to 7) is a 32-bit read-only register that shows the start address of the line in processing of the source image.

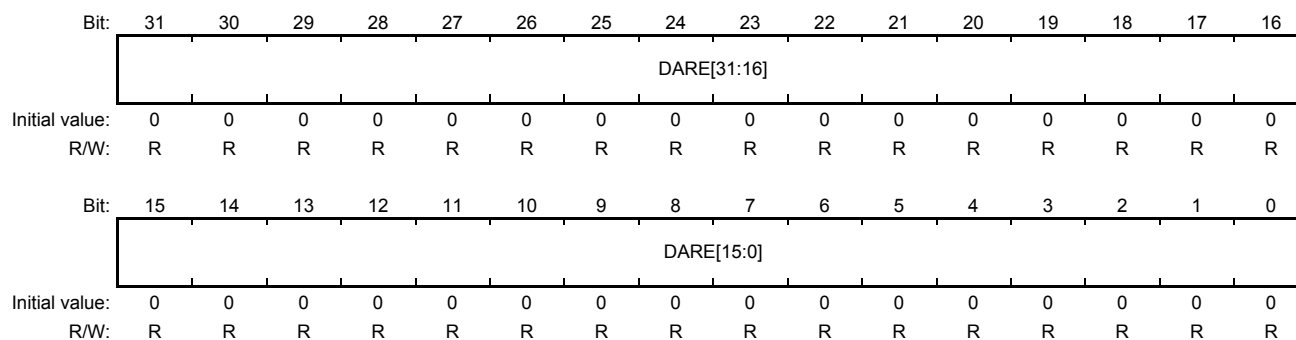


Bit	Bit Name	Initial Value	R/W	Description
31 to 0	SARE[31:0]	H'00000000	R	This read-only register used for internal processing shows the start address of the line in processing of the source image.

### 29.2.10 Destination Line Address Registers (CHnDARE)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CHnDARE (n = 0 to 7) is a 32-bit read-only register that shows the start address of the line in processing of the destination image.

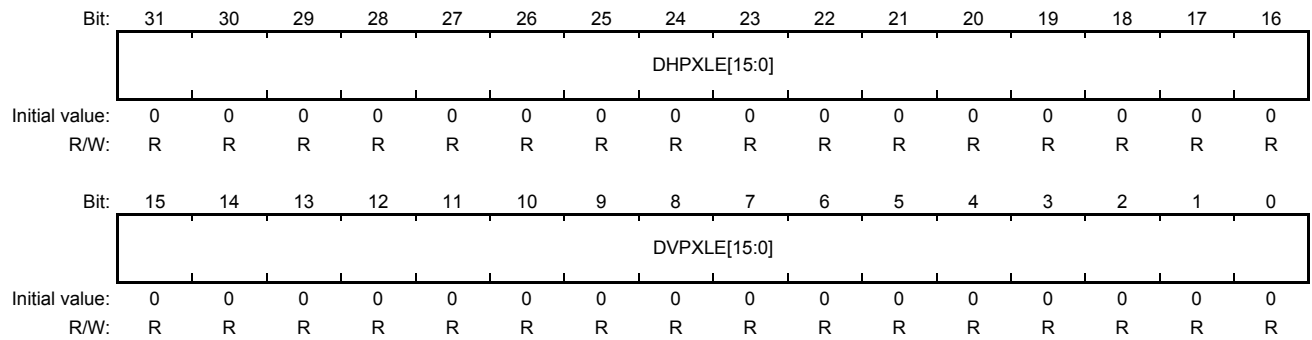


Bit	Bit Name	Initial Value	R/W	Description
31 to 0	DARE[31:0]	H'00000000	R	This read-only register used for internal processing shows the start address of the line in processing of the destination image.

**29.2.11 Destination Pixel Processing Registers (CHnDPXLE)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CHnDPXLE (n = 0 to 7) is a 32-bit read-only register that shows the number of unprocessed lines of the destination image.



Bit	Bit Name	Initial Value	R/W	Description
31 to 16	DHPXLE[15:0]	H'0000	R	This read-only register used for internal processing shows the number of unprocessed horizontal lines of the destination image.
15 to 0	DVPXLE[15:0]	H'0000	R	This read-only register used for internal processing shows the number of unprocessed vertical lines of the destination image.



### 29.2.12 Interrupt Status Clear Register (CHSTCLR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CHSTCLR is a register that indicates the status of HE and TE bits in each channel. By writing 1 in a bit in CHSTCLR, HE or TE bit in the corresponding channel is to be cleared.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CHnHE[7:0]							CHnTE[7:0]								
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 8	CHnHE[7:0]	H'00	R/W	Indicates the status of the HE bit in CHnCTRL (n = 0 to 7). Writing 1 in this bit, the HE bit in corresponding channel is to be cleared. [Writing] 0: NOP 1: HE bit is cleared. [Reading] 0: 0 is set in the HE bit. 1: 1 is set in the HE bit.
7 to 0	CHnTE[7:0]	H'00	R/W	Indicates the status of the TE bit in CHnCTRL (n = 0 to 7). Writing 1 in this bit, the TE bit in corresponding channel is to be cleared. [Writing] 0: NOP 1: TE bit is cleared. [Reading] 0: 0 is set in the TE bit. 1: 1 is set in the TE bit.

## 29.3 Operation

RZ/G1H

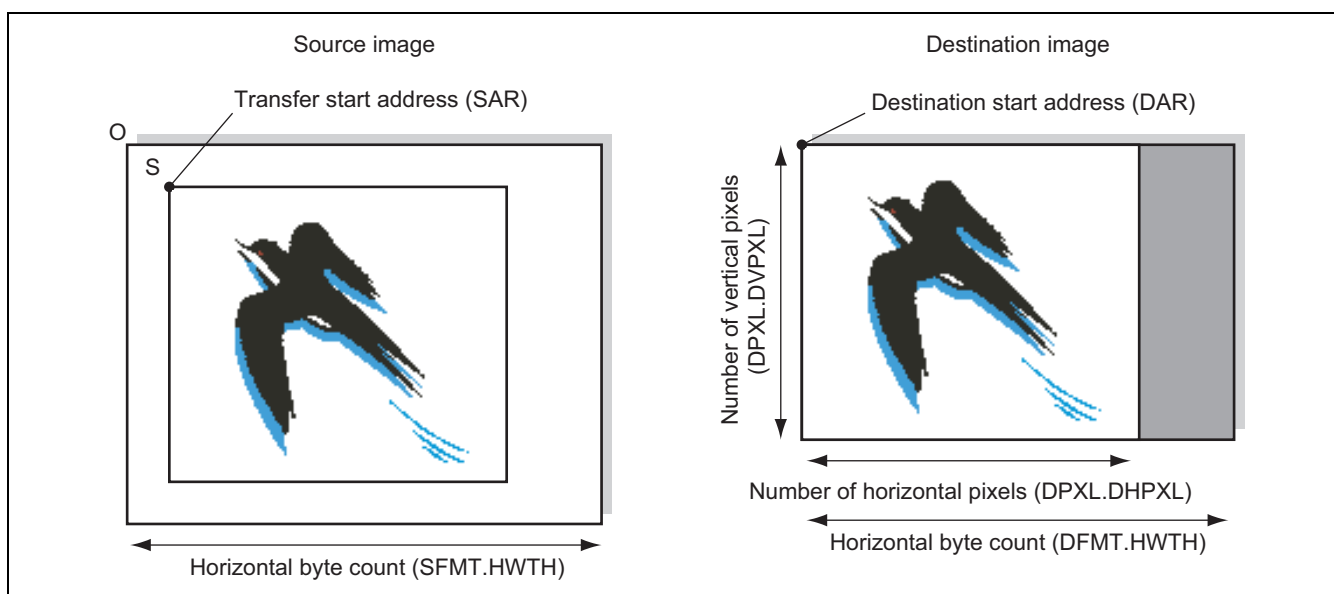
RZ/G1N

RZ/G1M

RZ/G1E

This module can extract image data of required size from the source image and store it as a destination image, and also can convert the format, rotation/inversion, and magnify the image at that time.

### 29.3.1 Image Extraction



**Figure 29.6 Schematic Diagram of Image Extraction**

Figure 29.6 shows a schematic diagram of image extraction.

The image format conforms to the YCbCr4:2:0, YCbCr4:2:2, and RGB formats. Extraction of data is possible in two-pixel units for YCbCr formats and in one-pixel units for RGB formats. However, since the Y data and C data are independently stored in the memory in the YCbCr format, set them in different channels respectively.

For source images, the address of extraction start coordinates S and the horizontal byte size must be set in respective registers. Set the start address of the extraction start pixel in SAR. If the X coordinate of extraction start coordinates S (SAR) is an odd number with origin O in the YCbCr format, a deviation is generated between Y data and C data in the horizontal direction. Furthermore, in the YCbCr4:2:0 format, if the Y coordinate of extraction start coordinates S is an odd number with origin O, a deviation is generated between Y data and C data in the vertical direction. For each case, extract image data from the even pixel coordinates where truncation is made.

For destination images, destination start address, numbers of horizontal and vertical pixels, and the horizontal byte size must be set. Set an integer multiple of 16 ( $\geq$  DHPXL in DPXL x bytes per pixel) for the horizontal byte size (HWTH in DFMT). Discard the gray area in Figure 29.6 as invalid data. For YCbCr formats, set an even number for the number of Y data horizontal pixels. In addition, for the YCbCr4:2:0 format, the number of vertical pixels must also be set to an even number.

Table 29.4 lists these restrictions.

**Table 29.4 Restrictions for Each Format**

Format	Item	Restrictions
Common	Destination image horizontal byte size (CHnDFMT.HWTH)	Set an integer multiple of 16.
Y data (YCbCr4:2:2)	Source image horizontal extraction start position (CHnSAR.SAR)	In a case that the X-coordinate of starting coordinate-S (SAR) relative to the coordinate origin 0 of source image is odd number, a deviation is generated between Y data and C data in the horizontal direction.
	Destination image horizontal pixel size (CHnDPXL.DHPXL)	In a case that the horizontal pixel size is odd number of the destination image, the invalid data might be generated right side in the image.
Y data (YCbCr4:2:0)	Source image horizontal extraction start position (CHnSAR.SAR)	In a case that the X-coordinate of starting coordinate-S (SAR) relative to the coordinate origin 0 of source image is odd number, a deviation is generated between Y data and C data in the horizontal direction.
	Source image vertical extraction start position (CHnSAR.SAR)	In a case that the Y-coordinate of starting coordinate-S (SAR) relative to the coordinate origin 0 of source image is odd number, the vertical throw between Y and CbCr is to be generated.
	Destination image horizontal pixel size (CHnDPXL.DHPXL)	In a case that the horizontal pixel size is odd number of the destination image, the invalid data might be generated right side in the image.
	Destination image vertical pixel size (CHnDPXL.DVPXL)	In a case that the vertical pixel size is odd number of the destination image, the invalid data might be generated bottom in the image.

### 29.3.2 Image Rotation/Inversion

**Table 29.5 The Combination of the Bits, VMRR, HMRR, ROTL, and ROTR and the Rotation/Inversion**

VMRR bit	HMRR bit	ROTL bit	ROTR bit	DAR specified point	Rotation/Inversion Performance
0	0	0	0	A	Rotation/Inversion is not performed
0	0	0	1	C	Clockwise 90 degrees rotation
0	0	1	0	B	Clockwise 270 degrees rotation
0	1	0	1	A	After rotating clockwise 90 degrees, inverse horizontally
1	0	1	0		(After rotating clockwise 270 degrees, inverse vertically)
1	0	0	1	D	After rotating clockwise 90 degrees, inverse vertically
0	1	1	0		(After rotating clockwise 270 degrees, inverse horizontally)
0	1	0	0	C	Inversing horizontally
1	0	0	0	B	Inversing vertically
1	1	0	0	D	180 degrees rotation
Others				—	Setting prohibited

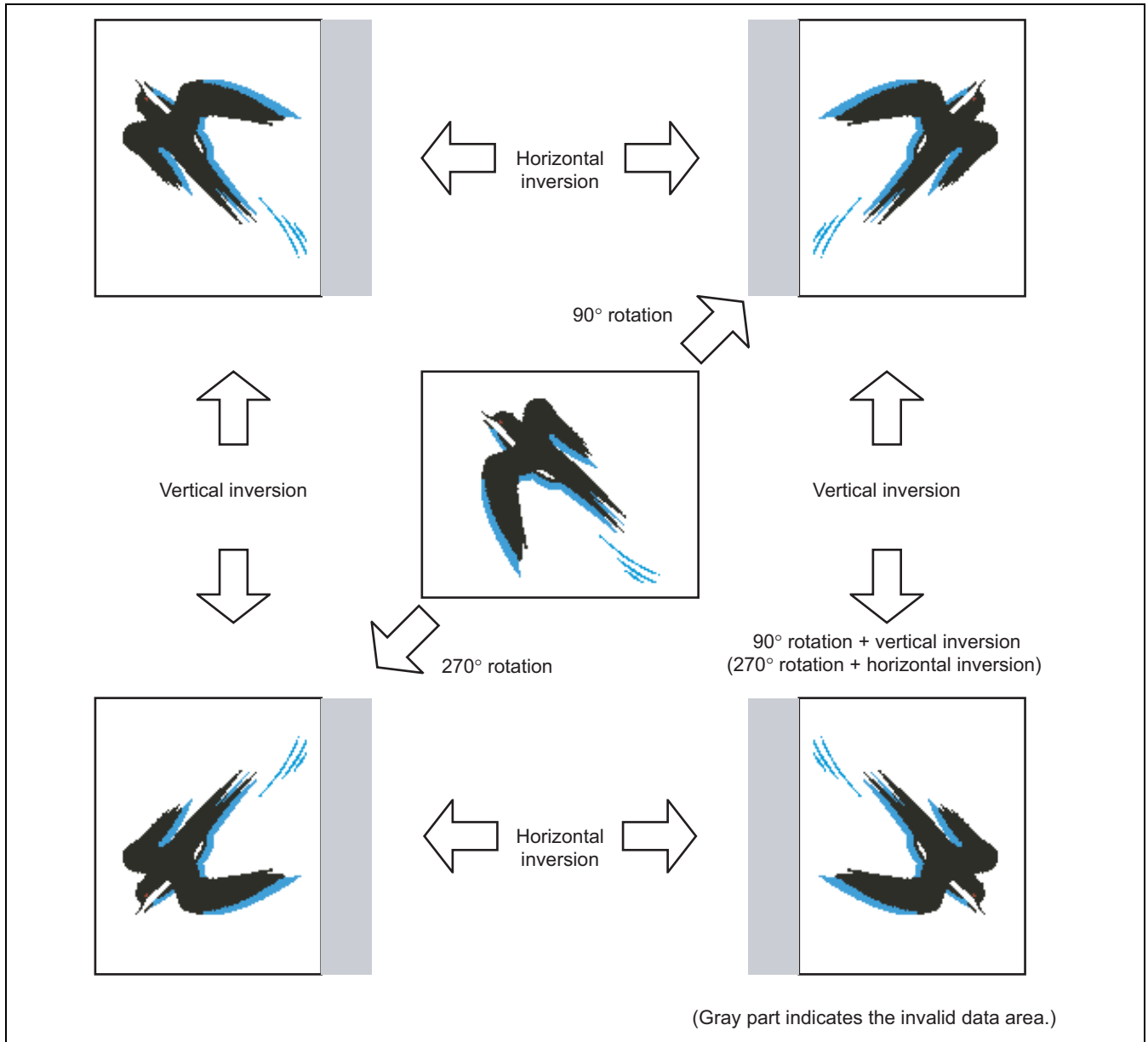
The rotation/inversion performance in 90 degrees units can be executed arbitrarily effects of combination of the bits, VMRR, HMRR, ROTR, and ROTL as shown in Table 29.5. Figure 29.7 shows the relations between the source image and the destination image in operating with rotation/inversion performance and Figure 29.8 shows only with inversion performance.

During the rotation/ inversion operating, the address specified point setting in CHnDAR is to be changed according to the setting of the bits, VMRR, HMRR, ROTR, and ROTL. See Figure 29.9 for details on the specified address point corresponding to the processing respectively.

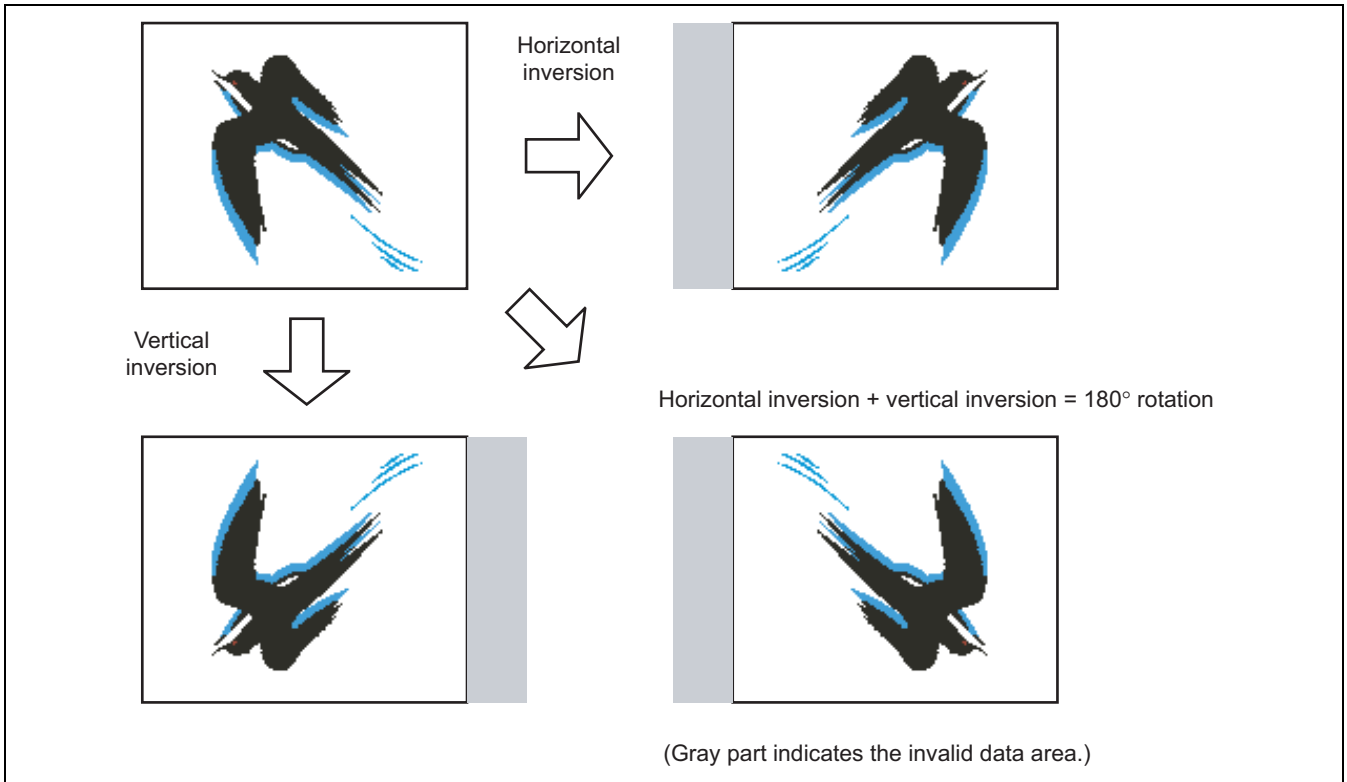
Lists the formulas for the address settings as follows.

offset\_add      Address at the left above end of the destination image.  
 dest\_hwidth    Horizontal byte size of the destination image (CHnDFMT.DHWTH)  
 dest\_vpxl      Vertical pixel size of the destination image (CHnDPXL.DVPXL)

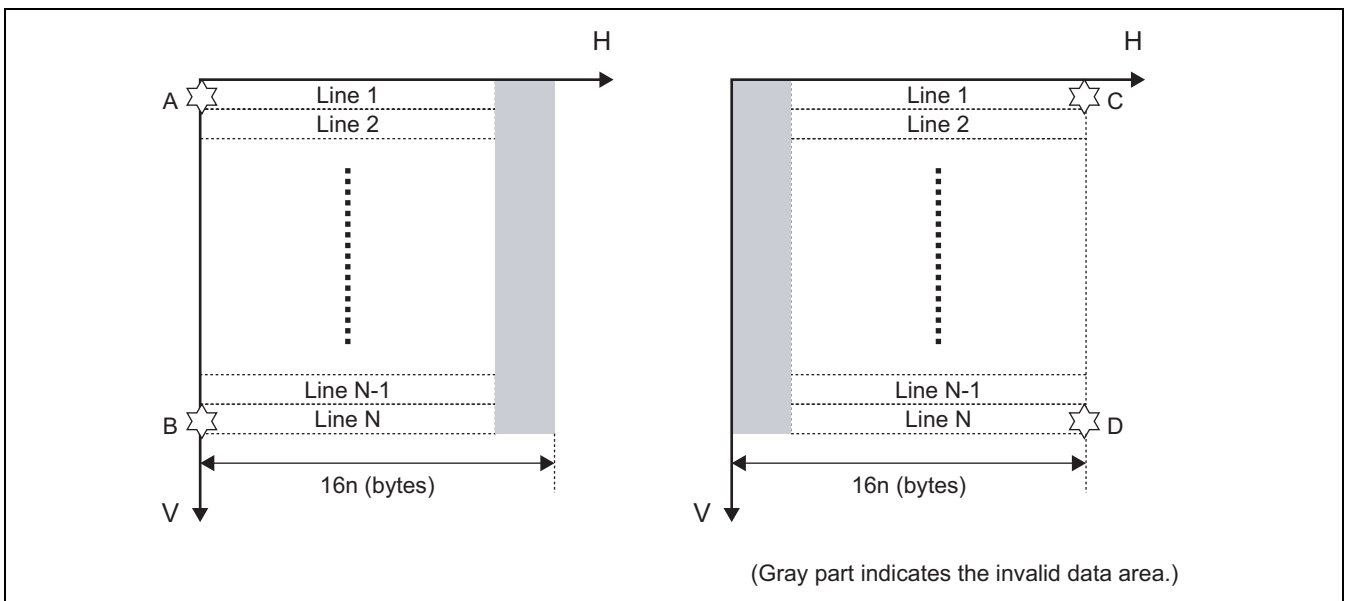
- A     $DAR = offset\_add$
- B     $DAR = offset\_add + (dest\_hwidth \times (dest\_vpxl - 1))$
- C     $DAR = offset\_add + dest\_hwidth$
- D     $DAR = offset\_add + (dest\_hwidth \times dest\_vpxl)$



**Figure 29.7 Relations between the Source Image and the Destination Image in Operating with Rotation/Inversion Performance**



**Figure 29.8 Relations between the Source Image and the Destination Image in Operating with Inversion Performance**



**Figure 29.9 The specified Address point of CHnDAR**

### 29.3.3 Format Conversion

Conversions are possible between RGB formats and between YCbCr formats (YCbCr4:2:0 and YCbCr4:2:2). For available RGB formats, see Table 29.3. However, no format conversion is possible between RGB and YCbCr.

### 29.3.4 Simple Magnification

Setting the MX and MY bits in CTRL allows enlarged output in the X and Y directions respectively.

Simple magnification method is used for the magnification processing where the pixels in the source image are copied in the X and Y directions and are then output.

Figure 29.10 is a schematic diagram of simple magnification of pixels.

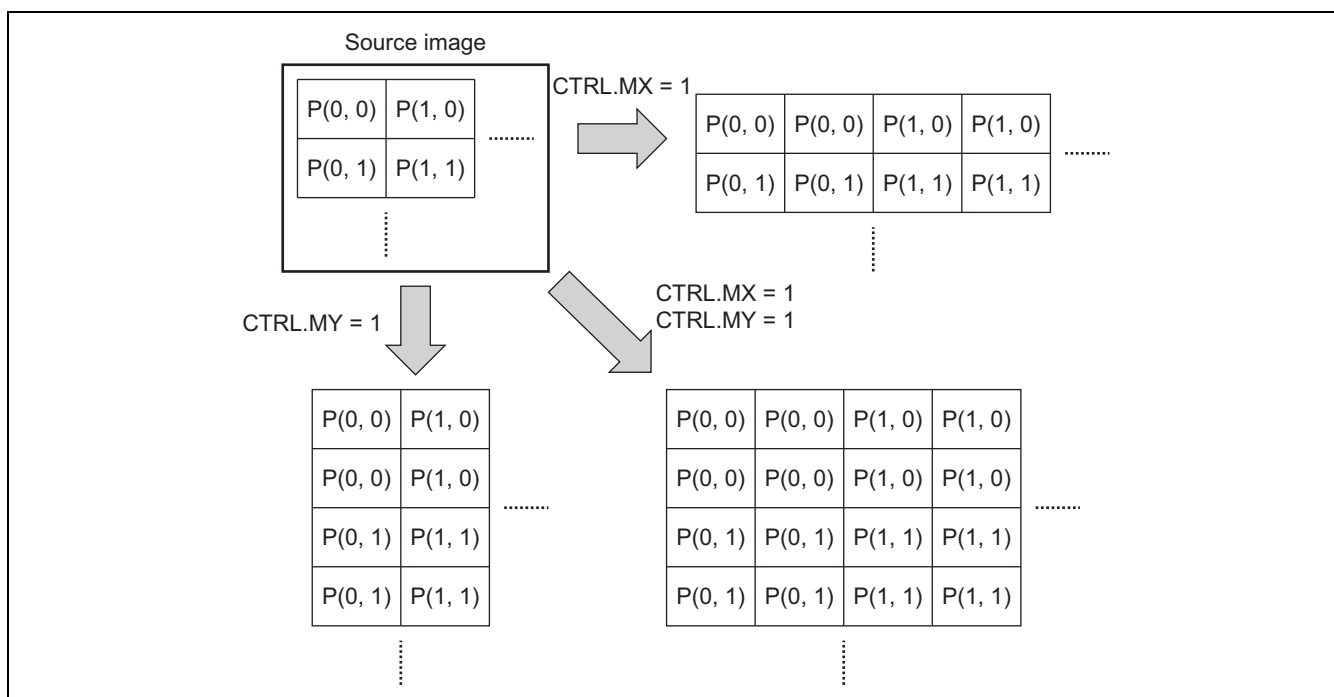


Figure 29.10 Enlarged Output of Pixels

29.4 Transfer Flow

RZ/G1H	RZ/G1N
RZ/G1M	RZ/G1E

Figure 29.11 shows a flowchart of DMAC transfer using 2D-DMAC.

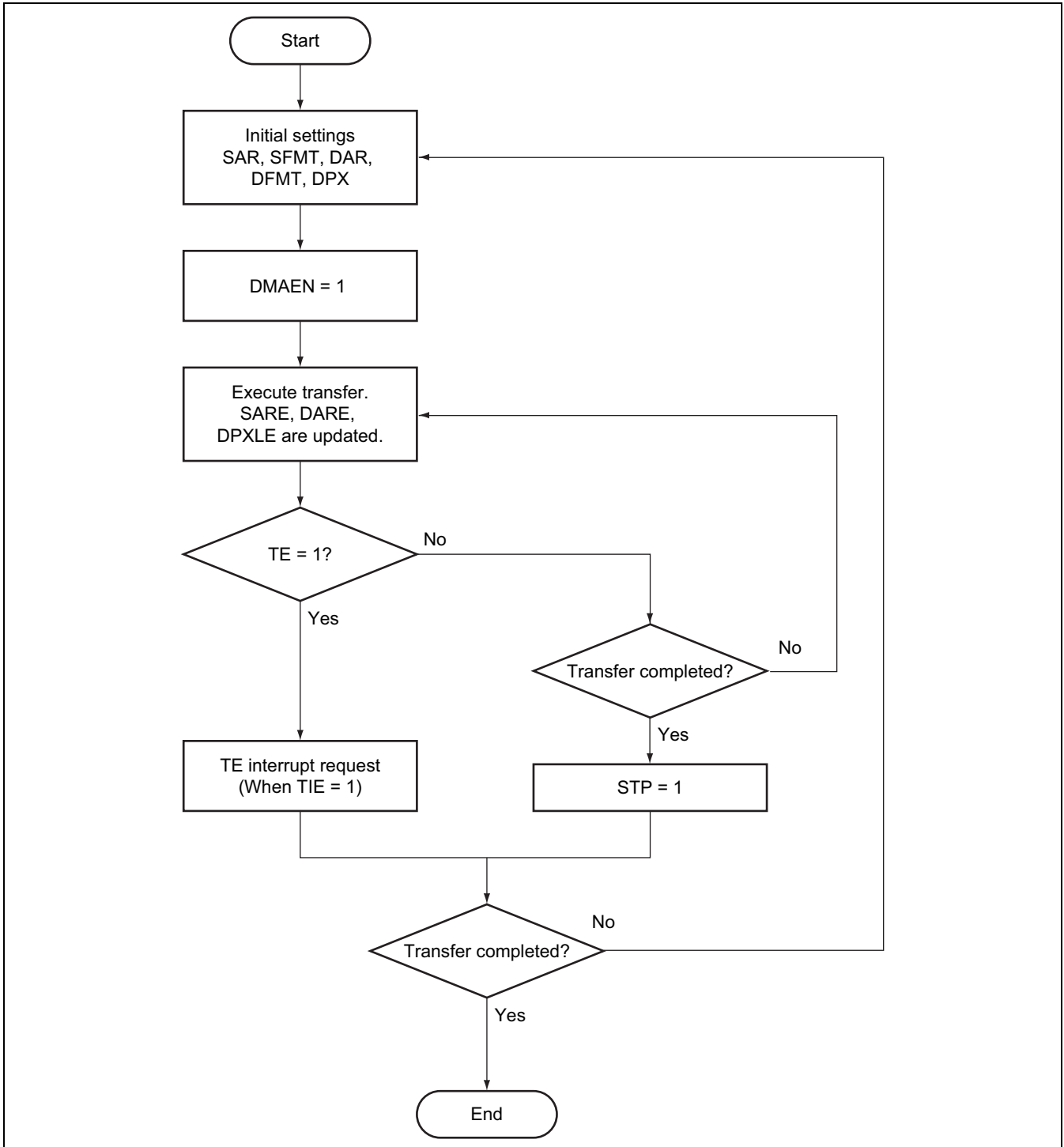


Figure 29.11 Flowchart of DMAC Transfer Using 2D-DMAC



## 29.5 Handling Interrupts from the 2D-DMAC

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

The 2D-DMAC module issues an interrupt (TEI = 1) when it completes data output without receiving a confirmation of completion of the data transaction with external memory. This raises the possibility of unexpected (out-of-date) data being read from external memory when a request for access from any module reaches external memory ahead of the 2D-DMAC's interrupt request. This behavior will only appear if the module is accessing 2D-DMAC output data for the part of the bottom line in the right corner (e.g. the CPU is reading image data for 180-degree image rotation.). Avoiding this behavior requires either of the procedures described below.

### 1. Dummy transaction

After detecting the TE interruption, set up a dummy transfer with the below conditions:

Stride size of source image: 2048 bytes

Output image size: W: 128, H: 32

Image format: ARGB8888 (PKF = B'00000)

No image rotation and scaling

The TE interrupt in response to the dummy transfer guarantees the completion of data output for the target transaction to external memory.

### 2. Insertion of a wait period

After detecting the TE interrupt, insert 20  $\mu$ s of waiting to guarantee completion of the data transaction with external memory.

## 30. TS Interface (TSIF)



The transport stream interface (TSIF) is a module for receiving the MPEG2 transport stream (TS) used in a segment broadcasting implemented as part of the digital terrestrial broadcasting services. The TSIF extracts packet data and controls PCR, which are required to decode the system layer of the MPEG2 standard.

### 30.1 Features

The TSIF has the following features.

- Serial data input
- Support for TS data transfer by DMA auto request
- Acquisition of TS packets
  - Filters 67 kinds of PIDs (packet ID) in total (the PID values of PAT and CAT packets are fixed. For PCR, video, and audio packets, the PID values are predefined).
  - Supports all valid packet receive mode (null packet is deleted).
  - Supports all packet receive mode including null packet.
  - Supports duplicate packet delete mode.
  - Capable of specifying the endian type when TS packet data is read.
  - Supports timestamping TS packet data with timing of obtaining it.
- TS data analysis
  - Detects random access indicator.
  - Detects discontinuity indicator.
  - Detects video start code and short header.
- Extraction of PCR information
- Support for system clock generation

[Legend]

MPEG:	Moving picture expert group
TS:	Transport stream
PID:	Packet ID
PAT:	Program association table
CAT:	Conditional access table
PCR:	Program clock reference
ES:	Elementary stream

Figure 30.1 shows a block diagram of the TSIF.

The signals to transfer or control TS data are input as an input signal, and the TS packet data filtered by this module will be output as an output signal.

The serially input TS data is converted into 8-bit parallel data and the header of the TS packet is detected by the TS synchronous detection circuit. The TS filter circuit then determines and filters the PID of the TS packet according to the predefined PID table and stores the TS packet in the buffer for TS packets. Following these processes, only predefined TS packets are stored in the buffer and transferred to memories via a bus interface.

The analysis circuit of a TS header is a block that analyses the header of a TS packet, acquires the header information, and generates a trigger signal sent to other blocks. The ES data search circuit searches the start code and short header of an elementary stream (ES) contained in a TS packet. This result can be used as supplementary data to control the start timing of image decoding through the upper-level software that controls image decoding.

Based on the PCR information extracted from the TS packet, the PCR control unit outputs information needed for system clock control.

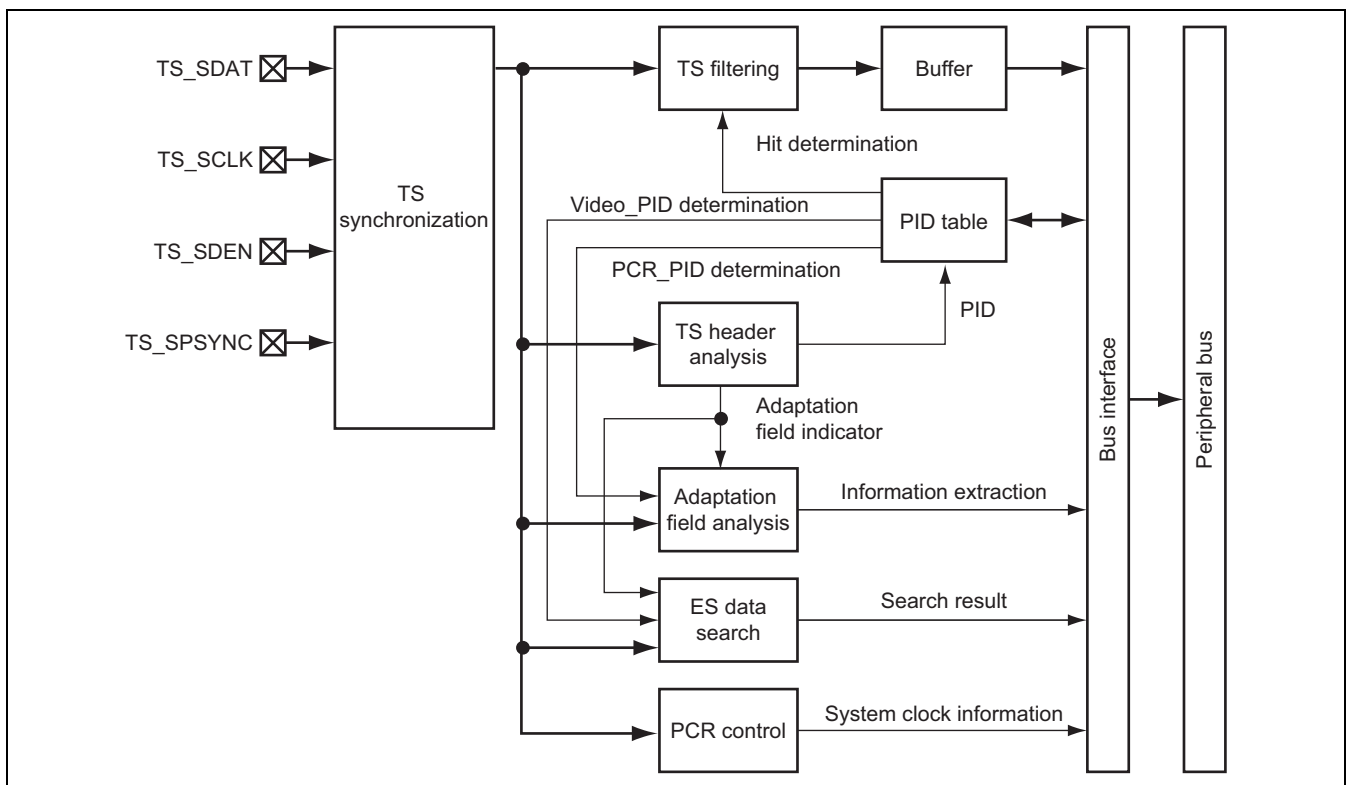


Figure 30.1 TSIF Block Diagram [RZ/G1M]

## 30.2 Input/Output Pins

Table 30.1 shows the pin configuration.

**Table 30.1 Pin Configuration**

Pin Name	Function	I/O	Description	RZ/G Series Products			
				RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
TS_SDAT0	TS serial data	Input	Serial Input Pin of TS Packet Data Polarity inversion is enabled by register setting.	—	√	—	—
TS_SCK0	TS serial clock	Input	Serial Input Clock Pin Polarity inversion is enabled by register setting. The initial value is synchronized with the rising edge.	—	√	—	—
TS_SDEN0	TS data enable	Input	Serial Input Enable Signal Pin Polarity inversion and on/off setting are enabled by register setting. The initial value is on and enabled after the TS_SDEN signal is driven high.	—	√	—	—
TS_SPSYNC0	TS data synchronization	Input	Byte Boundary Signal Pin Polarity inversion is enabled by register setting. The initial value is set on a byte boundary at the rising edge. If an LSI that does not have the TS_SPSYNC signal is connected, follow the method of handling synchronization signals in the LSI. Signals that have the same waveform of the TS_SDEN signal described in this section can be connected to this pin.	—	√	—	—

### 30.3 Register Descriptions

Table 30.2 shows the TSIF register configuration. Table 30.3 shows the register states in each operating mode.

Base address is listed below.

TSIF0: H'FFE8 0000

**Table 30.2 Register Configuration (n = 0)**

						RZ/G Series Products			
Register Name	Abbreviation	R/W	Address	Access Size	RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E	
TSIFn control register	TSnCTRLR	R/W	H'0000	32	—	√	—	—	
TSIFn PID data register	TSnPIDR	R/W	H'0004	32	—	√	—	—	
TSIFn command register	TSnCMDR	R/W	H'0008	32	—	√	—	—	
TSIFn interrupt status register	TSnSTR	R/W	H'000C	32	—	√	—	—	
TSIFn TS data register	TSnTSDR	R	H'0010	32	—	√	—	—	
TSIFn buffer clear register	TSnBUFCLRR	R/W	H'0014	32	—	√	—	—	
TSIFn interrupt enable register	TSnINTER	R/W	H'0018	32	—	√	—	—	
TSIFn PSCALE register	TSnPSCALER	R/W	H'0020	32	—	√	—	—	
TSIFn PSCALE_R register	TSnPSCALEERR	R/W	H'0024	32	—	√	—	—	
TSIFn PCRADC mode register	TSnPCRADCMDR	R/W	H'0028	32	—	√	—	—	
TSIFn PCRADC register	TSnPCRADCR	R	H'002C	32	—	√	—	—	
TSIFn TR_PCRADC register	TSnTRPCRADCR	R	H'0030	32	—	√	—	—	
TSIFn D_PCRADC register	TSnDPCRADCR	R	H'0034	32	—	√	—	—	
TSIFn free run counter L	TSnFRCL	R/W	H'0040	32	—	√	—	—	
TSIFn free run counter H	TSnFRCH	R/W	H'0044	32	—	√	—	—	
TSIFn FSCALE register	TSnFSCALER	R/W	H'0048	32	—	√	—	—	
TSIFn FSCALE R register	TSnFSCALEERR	R/W	H'004C	32	—	√	—	—	
TSIFn compare match control register	TSnCMCTRLR	R/W	H'0050	32	—	√	—	—	
TSIFn compare match counter 0	TSnCMCNT0	R/W	H'0054	32	—	√	—	—	
TSIFn compare match counter 1	TSnCMCNT1	R/W	H'005C	32	—	√	—	—	
TSIFn compare match constant register 0	TSnCMCOR0	R/W	H'0064	32	—	√	—	—	
TSIFn compare match constant register 1	TSnCMCOR1	R/W	H'006C	32	—	√	—	—	
TSIFn TS packet count register	TSnPCNT	R/W	H'0074	32	—	√	—	—	
TSIFn TS packet count keep register	TSnPCNTKP	R/W	H'0078	32	—	√	—	—	
TSIFn TS packet count push register	TSnPCNTPSH	R/W	H'007C	32	—	√	—	—	

Note: Do not access addresses other than listed above. Operations cannot be guaranteed if access is attempted.

**Table 30.3 Register States in Each Operating Mode (n = 0)**

Register Abbreviation	Reset *	Module Standby	RZ/G Series Products			
			RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
TSnCTLR	Initialized	Retained	—	√	—	—
TSnPIDR	Initialized	Retained	—	√	—	—
TSnCMDR	Initialized	Retained	—	√	—	—
TSnSTR	Initialized	Retained	—	√	—	—
TSnTSDR	Initialized	Retained	—	√	—	—
TSnBUFCLRR	Initialized	Retained	—	√	—	—
TSnINTER	Initialized	Retained	—	√	—	—
TSnPSCALER	Initialized	Retained	—	√	—	—
TSnPSCALERR	Initialized	Retained	—	√	—	—
TSnPCRADCMDR	Initialized	Retained	—	√	—	—
TSnPCRADCR	Initialized	Retained	—	√	—	—
TSnTRPCRADCR	Initialized	Retained	—	√	—	—
TSnDPCRADCR	Initialized	Retained	—	√	—	—
TSnFRCL	Initialized	Retained	—	√	—	—
TSnFRCH	Initialized	Retained	—	√	—	—
TSnFSCALER	Initialized	Retained	—	√	—	—
TSnFSCALERR	Initialized	Retained	—	√	—	—
TSnCMCTLR	Initialized	Retained	—	√	—	—
TSnCMCNT0	Initialized	Retained	—	√	—	—
TSnCMCNT1	Initialized	Retained	—	√	—	—
TSnCMCOR0	Initialized	Retained	—	√	—	—
TSnCMCOR1	Initialized	Retained	—	√	—	—
TSnPCNT	Initialized	Retained	—	√	—	—
TSnPCNTKP	Initialized	Retained	—	√	—	—
TSnPCNTPSH	Initialized	Retained	—	√	—	—

Note: \* Refer the contents of section 8, Reset (RST).

### 30.3.1 TSIF Control Register (TSCTLR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
—	√	—	—

TSCTLR is a register for controlling the TSIF.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	PLNGT H	TSDAT P	TSCLK P	TSVLD P	—	PSYCP	—	—	SDENE	—	—	BUF4	TFA	DPDM D	DREQ MD
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R/W	R	R/W	R	R	R/W	R	R	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EN	PCRM D	FRCM D	FRCSE L	FRCLA TCH	FRCADD[1:0]	FRCST R	FRCPSC[7:0]								
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
30	PLNGTH	0	R/W	Byte Configuration Set of TS Packet Data 0: TS packet is 204-byte configuration. 1: TS packet is 188-byte configuration.
29	TSDATP	0	R/W	Input Polarity Set of TS Packet Data 0: TS data input is positive polarity. 1: TS data input is negative polarity (used after polarity inversion).
28	TSCLKP	0	R/W	Input Polarity Set of TS Clock 0: TS data clock input is positive polarity (TS data is received at the rising edge). 1: TS data clock input is negative polarity (TS data is received at the falling edge).
27	TSVLDP	0	R/W	Input Polarity Set of TS Packet Data Enable Signal 0: The TS_SDEN signal from the TS decoder is positive polarity (enabled at high). 1: The TS_SDEN signal from the TS decoder is negative polarity (enabled at low).
26	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
25	PSYCP	0	R/W	Input Polarity Set of TS Packet Data Sync Signal 0: TS packet sync signal TS_SPSYNC is positive polarity (sync byte at high). 1: TS packet sync signal TS_SPSYNC is negative polarity (sync byte at low).
24, 23	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
22	SDENE	0	R/W	TS Packet Data Enable Signal Enabled/Disabled 0: The TS_SDEN signal from the TS decoder is enabled. 1: The TS_SDEN signal from the TS decoder is disabled.

Bit	Bit Name	Initial Value	R/W	Description
21, 20	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
19	BUF4	0	R/W	Buffer Area Number Set 0: 2 areas 1: 4 areas
18	TFA	0	R/W	Software Reset Signal in the TSIF This bit automatically enters the reset state on startup. Writing 1 releases the reset. The TSIF internal registers are not initialized with this bit. When a reset is issued, confirm that this bit is set to 0 before releasing the reset. Note: Set this bit to 1 after eight cycles or more of TS_SCK is input. 0: The TSIF is reset internally (except internal registers). 1: Reset is released.
17	DPDMD	0	R/W	Duplicate Data of Consecutive TS Packets (Duplicate Packets) Delete When the PID of the previous consecutive packet matches continuity_counter, the data is deleted. However, when adaptation_field_control = x0 (x: don't care), the data is not deleted. 0: Duplicate data valid mode Even when the PID of the consecutive packet and continuity_counter match, the data is not deleted. 1: Duplicate data delete mode When the PID of the previous consecutive packet and continuity_counter match, the data is deleted. Note that this is valid only when adaptation_field_control = x1 (x: don't care).
16	DREQMD	0	R/W	After one packet (188 or 192 bytes) of TS data transfer by DMAC, selects whether the PEC bit in TSBUFFCLRR is set to 1 automatically. 0: DMA interrupt transfer mode After one packet (188 or 192 bytes) of TS data transfer, the PEC bit is not set to 1. 1: DMA auto-transfer mode After one packet (188 or 192 bytes) of TS data transfer, the PEC bit is set to 1 and the internal buffer is cleared.
15	EN	0	R/W	Specifies the endian type for reading TS packet data from TSTSDR. 0: Big endian 1: Little endian
14	PCRMD	0	R/W	Specifies settings for displaying time indicated by TSPCRADCR and TSTRPCRADCR. 0: Displays the time in 90 kHz units. 1: Displays the time in 45 kHz units.
13	FRCMD	0	R/W	Clock Setting of TSFRC 0: Displays the time in 90 kHz units. 1: Displays the time in 45 kHz units. This setting is only effective if FRCSEL = 1. It is ineffective if FRCSEL = 0.
12	FRCSEL	0	R/W	Setting of Base Clock of TSFRC 0: The divider clock set in FRCPSC is used. 1: The internal prescaler (TSFSCALER) is used.



Bit	Bit Name	Initial Value	R/W	Description
11	FRCLATCH	0	R/W	<p>Snapshot Setting of the Internal Free-Run Counter</p> <p>This bit acts as the trigger for taking a snapshot of the internal free-running counter's value.</p> <p>The value retained is readable from TSFRCL and TSFRCH.</p> <p>The snapshot is updated by again writing 1 to this bit.</p> <p>The FRCSTR bit is used to start or stop the internal free-running counter.</p> <p>0: The snapshot setting of TSFRCL/TSFRCH is off.</p> <p>1: The snapshot setting of TSFRCL/TSFRCH is on (the snapshot is updated when 1 is again written to this bit).</p>
10, 9	FRCADD [1:0]	00	R/W	<p>Determines whether to append a TSFRC value (as a timestamp) at the times of PID matches.</p> <p>00: TSFRC values are not appended to TSTSDR (TSTSDR reads 188-byte TS packet data).</p> <p>01: TSFRC values are appended to the 189th to 192nd bytes of TSTSDR (TSTSDR reads 188-byte TS packet data plus the 4-byte TSFRC value).</p> <p>10: Reserved</p> <p>11: 64-bit TSFRC values are appended to the 189th to 196th bytes of TSTSDR (TSTSDR reads 188-byte TS packet data plus the 8-byte TSFRC value).</p>
8	FRCSTR	0	R/W	<p>Specifies stopping or operation of the TSFRC.</p> <p>0: Stops counting by the TSFRC.</p> <p>1: The TSFRC counts up.</p>
7 to 0	FRCPSC [7:0]	H'00	R/W	<p>Sets a division clock for TSFRC.</p> <p>To set the clock to <math>HP\phi</math> divided by <math>n</math>, set FRCPSC to <math>n - 1</math>.</p> <p>Example:</p> <p>To set the clock to 1 MHz (divided by 130) while <math>HP\phi</math> is 130 MHz, set FRCPSC[7:0] to 129 (H'81).</p> <p>This setting is only effective when the setting of FRCSEL is 0.</p> <p>It is ineffective when FRCSEL = 1.</p>

The table below shows the conditions where the TFA bit is reflected in the TSIF.

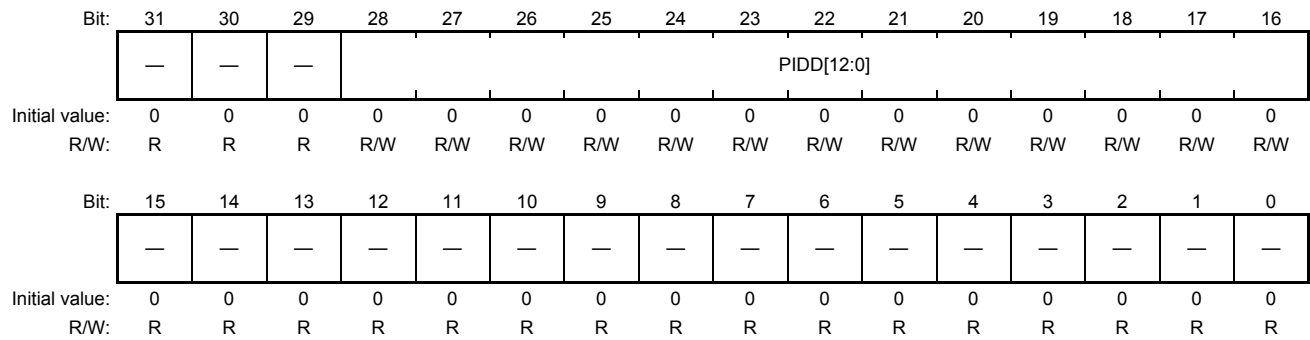
The TFA bit is reflected in the TSIF depending on the condition of the DREQMD bit with the following timing.

DREQMD Bit	TFA Bit	Reflection Timing
0	0 → 1	Reflected accordingly by register setting
	1 → 0	Reflected accordingly by register setting
1	0 → 1	Reflected accordingly by register setting
	1 → 0	Timing when the PEC bit is automatically set to 1

### 30.3.2 TSIF PID Data Register (TSPIDR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
—	√	—	—

TSPIDR is a register used to set the PID value that sets the section table of the PID filter. The settings of PIDD can be reflected by writing to TSCMDR after this register is written to.



Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28 to 16	PIDD[12:0]	H'0000	R/W	Byte Configuration Set of TS Packet Data These bits set the PID value that sets the section table of the PID filter. The setting of this register can be reflected by writing to TSCMDR after setting PIDD.
15 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

### 30.3.3 TSIF Command Register (TSCMDR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
—	√	—	—

TSCMDR is a register that sets the value set by TSPIDR in the PID table.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	PT[5]	—	—	ALLPID MD	PIDMD	TFE	—	PPS	PT[4:0]				
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28	PT[5]	0	R/W	Selects a section for setting the PID table (see Table 30.4). This bit is valid only when the PIDMD bit and the TFE bit are 0.
27, 26	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
25	ALLPIDMD	0	R/W	PID Filter Mode Set ALLPIDMD PIDMD 0 0: A value set in the PID table is valid (PID filter mode).
24	PIDMD	0	R/W	0 1: All PIDs other than null packet (PID = H'1FFF) are valid (all valid packet receive mode). 1 *: All PIDs including null packet (PID = H'1FFF) are valid (all packet receive mode).
23	TFE	0	R/W	Content of the PID Table Cleared 0: — 1: The content of the PID table is cleared.
22	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
21	PPS	0	R/W	Select a section for setting the PID table (see Table 30.4).
20 to 16	PT[4:0]	H'00	R/W	These bits are valid only when the PIDMD bit and the TFE bit are 0.
15 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Write a value to be set in the section table of the PID filter for TSPIDR while the PIDMD bit is 0. Then, writing one of the following values in Table 30.4 sets a PID value in the specified select section.

In addition to the PID value set above, PIDs for PAT (fixed to H'0000) and CAT (fixed to H'0001) are set.

**Table 30.4 Relation among PPS, PT Setting, and PID Values**

PPS	PT[5:0]	Select Section
1	xxxxxx	PCR_PID
0	000000	Video
0	000001	Audio
0	000010	PID_1
0	000011	PID_2
0	000100	PID_3
0	000101	PID_4
0	000110	PID_5
0	000111	PID_6
0	001000	PID_7
0	001001	PID_8
0	001010	PID_9
0	001011	PID_10
0	001100	PID_11
0	001101	PID_12
0	001110	PID_13
0	001111	PID_14
0	010000	PID_15
0	010001	PID_16
0	010010	PID_17
0	010011	PID_18
0	010100	PID_19
0	010101	PID_20
0	010110	PID_21
0	010111	PID_22
0	011000	PID_23
0	011001	PID_24
0	011010	PID_25
0	011011	PID_26
0	011100	PID_27
0	011101	PID_28
0	011110	PID_29
0	011111	PID_30
0	100000	PID_31
0	100001	PID_32
0	100010	PID_33
0	100011	PID_34
0	100100	PID_35
0	100101	PID_36
0	100110	PID_37
0	100111	PID_38
0	101000	PID_39

PPS	PT[5:0]	Select Section
0	101001	PID_40
0	101010	PID_41
0	101011	PID_42
0	101100	PID_43
0	101101	PID_44
0	101110	PID_45
0	101111	PID_46
0	110000	PID_47
0	110001	PID_48
0	110010	PID_49
0	110011	PID_50
0	110100	PID_51
0	110101	PID_52
0	110110	PID_53
0	110111	PID_54
0	111000	PID_55
0	111001	PID_56
0	111010	PID_57
0	111011	PID_58
0	111100	PID_59
0	111101	PID_60
0	111110	PID_61
0	111111	PID_62

Note: X: Don't care

### 30.3.4 TSIF Interrupt Status Register (TSSTR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
—	√	—	—

TSSTR is a register that indicates the internal status of the TSIF. Each bit in TSSTR can be cleared by writing 0. Bits other than the SYNCF bit are set when a packet is received. Each bit in TSSTR (except for the SYNCF bit) is initialized by the TFA bit in TSCTLR.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	PID[12:0]												
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	CM1MF	CM0MF	—	ADCF	PIDF	STOF	RANDF	DISCF	SYNCF	OFEF	—	VSCF	VSHF	TSIFIN TF
Initial value:	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
R/W:	R	R	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R	R/W	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28 to 16	PID[12:0]	H'0000	R/W	These bits indicate the PID of the TS packet input immediately before.
15, 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13	CM1MF	0	R/W	COMPARE MATCH1 Matching Flag This is a flag to indicate that the compare match counter has counted down from the value set in TSCMCOR1 and reached 0. Software is not able to write 1 to this bit. 0: The value of TSCMCNT1 hasn't reached H'0000 0000. 1: The value of TSCMCNT1 has reached H'0000 0000. [Clearing condition] 0 being written to CM1MF.
12	CM0MF	0	R/W	COMPARE MATCH0 Matching Flag This is a flag to indicate that the compare match counter has counted down from the value set in TSCMCOR0 and reached 0. Software is not able to write 1 to this bit. 0: The value of TSCMCNT0 hasn't reached H'0000 0000. 1: The value of TSCMCNT0 has reached H'0000 0000. [Clearing condition] 0 being written to CM0MF.
11	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
10	ADCF	0	R/W	0: — 1: Indicates that PCRADC was updated (the PCR packet was input).

Bit	Bit Name	Initial Value	R/W	Description
9	PIDF	0	R/W	0: — 1: Indicates that the set PID packet was received in the PID filter mode (ALLPIDMD = 0 and PIDMD = 0).
8	STOF	0	R/W	0: — 1: Indicates that the interrupt in response to the completion of a next packet has been generated and that other bits have been updated.
7	RANDF	0	R/W	0: — 1: Indicates that random_access_indicator of the TS packet input immediately before is 1.
6	DISCF	0	R/W	0: — 1: Indicates that discontinuity_indicator of the PCR packet input immediately before shows the PCR discontinuous state.
5	SYNCF	1	R	Internal Synchronous/Asynchronous Mode State Caused by Detection of the TS Packet Sync Signal When the sync signal (H'47) is detected three times consecutively in asynchronous mode, the TSIF enters the synchronous mode. When the sync signal is not detected four times consecutively in synchronous mode, it enters the asynchronous mode. The write value should always be 0. 0: Indicates that the TSIF is in synchronous mode (the TS packet is synchronized). 1: Indicates that the TSIF is in asynchronous mode (the TS packet is not synchronized).
4	OFEF	0	R/W	TSIF Internal Buffer Overflow 0: — 1: Indicates that an overflow error occurred in the internal buffer.
3	—	Undefined	R	Reserved The write value should always be 0.
2	VSCF	0	R/W	Video Packet Start Code Detection Flag 0: — 1: Indicates that the TS packet input immediately before is a video packet and its payload contains a start code (B'0000 0000 0000 0000 0000 0001 xxxx xxxx).
1	VSHF	0	R/W	Video Packet Short Header Detection Flag 0: — 1: Indicates that the TS packet input immediately before is a video packet and its payload contains a short header (B'0000 0000 0000 0000 1000 00xx xxxx xxxx).
0	TSIFINTF	0	R/W	TSIF Transfer Request Flag Indicates that the internal buffer contains one packet (188 bytes) of TS data. 0: — 1: Indicates that the internal buffer contains one packet of TS data.

### 30.3.5 TSIF TS Data Register (TSTSDR)

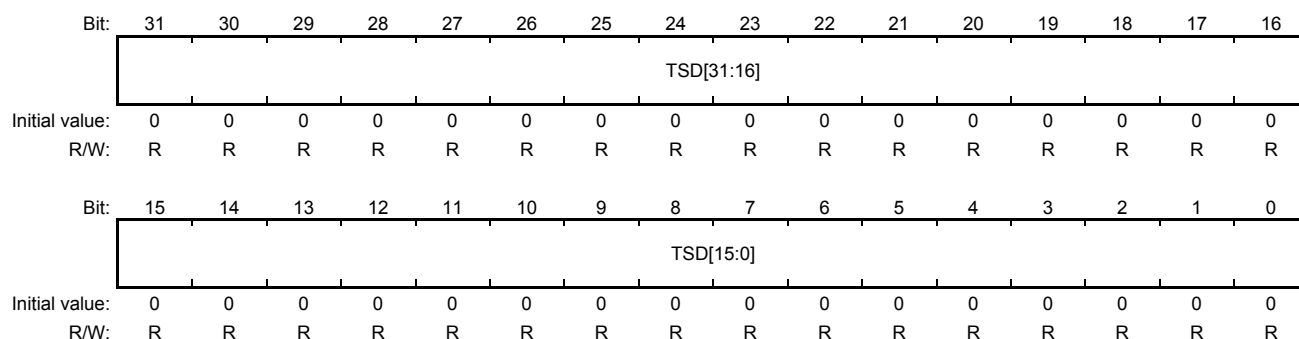
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
—	√	—	—

TSTSDR is a register to read TS packet data extracted by the set PID. Setting the EN bit in TSCTLR specifies the endian type.

When FRCADD[1:0] in TSCTLR is B'01, the TSFRC value (timestamp), which is recorded at the times of PID matches, is stored in the 189th to 192nd bytes. This value can be used as packet management data.

The timestamp is stored in the 189th to 196th bytes when of FRCADD[1:0] = B'11.

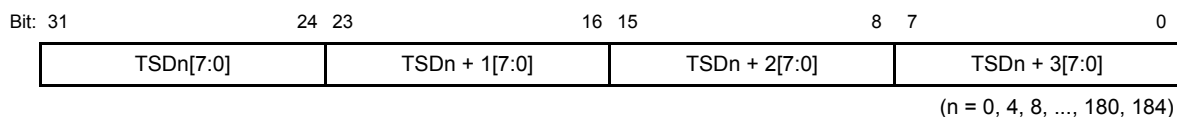
After reading one packet (188 bytes) of TS data from this register, the PEC bit in TSBUFCLRR should be set to 1 (unless it is in DMA auto-transfer mode).



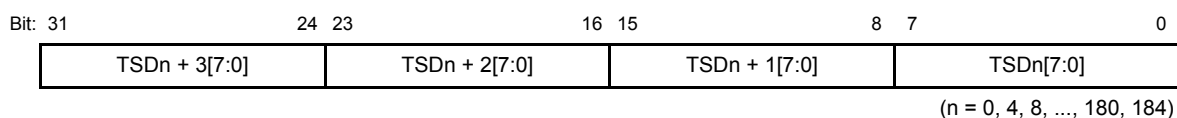
Bit	Bit Name	Initial Value	R/W	Description
31 to 0	TSD[31:0]	H'0000 0000	R	FRCADD in TSCTLR = 00: 1 to 188 bytes: TS packet data extracted by the set PID FRCADD in TSCTLR = 01: 1 to 188 bytes: TS packet data extracted by the set PID 189 to 192 bytes: TSFRC value recorded at the times of PID matches FRCADD in TSCTLR = 11: 1 to 188 bytes: TS packet data extracted by the set PID 189 to 196 bytes: TSFRC (H/L) value recorded at the times of PID matches

• TS packet data format

[Big endian] EN bit in TSCTLR = 0:



[Little endian] EN bit in TSCTLR = 1:

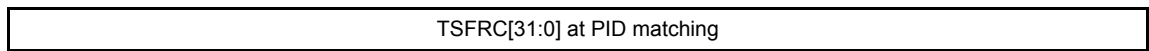




Note: Since the TSFRC (H/L) value, which is recorded at the times of PID matches and is in the 189th to 192nd (196th) bytes, is a 32-bit counter value, it is always read as longword data.

Bit: 31

0



### 30.3.6 TSIF Buffer Clear Register (TSBUFCLRR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
—	√	—	—

TSBUFCLRR is a register that clears the internal buffer of the TSIF after TS packet data is read.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PEC
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	PEC	0	R/W	Internal Buffer Clear This bit should be set to 1 immediately after TS packet data is read. When one packet of TS data is discarded because of a transfer error or such, this bit should be set to 1. This bit is automatically cleared to 0 after it has been set to 1. Do not access this register, while the DREQMD bit in TSCTLR is set to 1, or after TS packet data is read. 0: — 1: Clears the internal buffer after the TS packet is transferred (automatically returns to 0 after 1 is set). When one packet of data transferred is discarded because of a transfer error or such, 1 should always be set.

### 30.3.7 TSIF Interrupt Enable Register (TSINTER)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
—	√	—	—

TSINTER is a register that controls an interrupt request from the TSIF.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	CM1ME	CM0ME	—	ADCE	PIDE	STOE	RANDE	DISCE	SYNCE	OFEE	—	VSCE	VSHE	TSIFINTF
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W

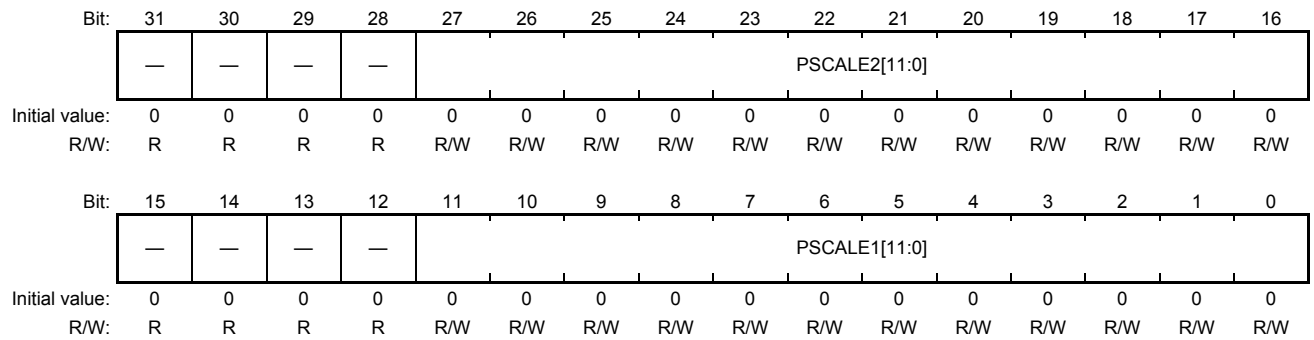
Bit	Bit Name	Initial Value	R/W	Description
31 to 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13	CM1ME	0	R/W	0: — 1: Generates an interrupt when TSCMCNT1 counts down and a value reaches H'0000 0000.
12	CM0ME	0	R/W	0: — 1: Generates an interrupt when TSCMCNT0 counts down and a value reaches H'0000 0000.
11	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
10	ADCE	0	R/W	0: — 1: Generates an interrupt when PCRADC is updated (PCR packet is input).
9	PIDE	0	R/W	0: — 1: Generates an interrupt when the set PID packet is received in PID filter mode.
8	STOE	0	R/W	0: — 1: Generates an interrupt when the interrupt in response to the completion of a next packet is generated and the status is updated (interrupt time is over).
7	RANDE	0	R/W	0: — 1: Generates an interrupt when random_access_indicator of the TS packet input immediately before is 1.
6	DISCE	0	R/W	0: — 1: Generates an interrupt when discontinuity_indicator of the PCR packet input immediately before indicates PCR discontinuity.
5	SYNCE	0	R/W	0: — 1: Generates an interrupt when the TSIF is in asynchronous mode.

Bit	Bit Name	Initial Value	R/W	Description
4	OFEE	0	R/W	0: — 1: Generates an interrupt when an overflow error occurs in the internal buffer.
3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
2	VSCE	0	R/W	0: — 1: Generates an interrupt when the start code of a video packet is detected in the TS packet input immediately before.
1	VSHE	0	R/W	0: — 1: Generates an interrupt when the short header of a video packet is detected in the TS packet input immediately before.
0	TSIFINTE	0	R/W	0: — 1: Generates an interrupt when the internal buffer contains one packet (188 bytes) of TS data.

### 30.3.8 TSIF PSCALE Register (TSPSCALER)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
—	√	—	—

TSPSCALER is a register that sets counter values 1 and 2 of the internal prescaler. When EXT\_MODE = 0, set the value of the PSCALE2 bit so that the value is equivalent to the value of the PSCALE1 bit plus 1.



Bit	Bit Name	Initial Value	R/W	Description
31 to 28	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
27 to 16	PSCALE2 [11:0]	H'000	R/W	These bits set counter value 2 of the internal prescaler.
15 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11 to 0	PSCALE1 [11:0]	H'000	R/W	These bits set counter value 1 of the internal prescaler.

### 30.3.9 TSIF PSCALE\_R Register (TSPSCALERR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
—	√	—	—

TSPSCALERR is a register that sets the ratio of counter values 1 and 2 of the internal prescaler.

When EXT\_MODE = 0, set the values of the PSCALE\_R1 bit and the PSCALE\_R2 bit so that the sum of these two bits is 9.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	PSCALE_R2[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	PSCALE_R1[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 20	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
19 to 16	PSCALE_R2 [3:0]	H'0	R/W	These bits set the ratio of counter value 2 of the internal prescaler.
15 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3 to 0	PSCALE_R1 [3:0]	H'0	R/W	These bits set the ratio of counter value 1 of the internal prescaler.

After setting TSPSCALERR while TSPSCALER is H'0000 0000, set TSPSCALER.

When EXT\_MODE = 0, set TSPSCALER and TSPSCALERR so that the following equation is satisfied.

$$\left\{ \frac{\text{PSCALE\_R1} + \text{PSCALE\_R2}}{\text{PSCALE1} \times \text{PSCALE\_R1} + \text{PSCALE2} \times \text{PSCALE\_R2}} \right\} \times \text{HP}\phi = 90 \text{ kHz}$$

$$\text{PSCALE\_R1} + \text{PSCALE\_R2} = 9$$

$$\text{PSCALE2} = \text{PSCALE1} + 1$$

The examples below show register settings of TSPSCALER and TSPSCALERR corresponding to each operating frequency of the TSIF. When EXT\_MODE = 1, operating frequencies listed in Table 30.5 are only supported.

**Table 30.5 Setting Example of TSPSCALER and TSPSCALERR Corresponding to Each Operating Frequency**

- EXT\_MODE = 0

Operating Frequency [MHz]	PSCALE2	PSCALE1	PSCALE_R2	PSCALE_R1
10.0	H'070	H'06F	H'1	H'8
12.0	H'086	H'085	H'3	H'6
12.6	H'08C	H'08B	H'9	H'0
12.8	H'08F	H'08E	H'2	H'7
14.4	H'0A1	H'0A0	H'0	H'9
16.0	H'0B2	H'0B1	H'7	H'2
19.2	H'0D6	H'0D5	H'3	H'6
20.0	H'0DF	H'0DE	H'2	H'7
27.0	H'12D	H'12C	H'0	H'9
33.0	H'16F	H'16E	H'6	H'3
48.0	H'216	H'215	H'3	H'6
50.0	H'22C	H'22B	H'5	H'4
54.0	H'259	H'258	H'0	H'9
66	H'2DE	H'2DD	H'3	H'6
83.4	H'39F	H'39E	H'6	H'3
100	H'458	H'457	H'1	H'8
130	H'5A5	H'5A4	H'4	H'5

- EXT\_MODE = 1

Operating Frequency [MHz]	PSCALE2	PSCALE1	PSCALE_R2	PSCALE_R1
13.5	H'000	H'001	H'0	H'1
27.0	H'000	H'002	H'0	H'1
40.5	H'000	H'003	H'0	H'1
54.0	H'000	H'004	H'0	H'1

Note: The operating frequency is a frequency of HP $\phi$ .

### 30.3.10 TSIF PCRADC Mode Register (TSPCRADCMDR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
—	√	—	—

TSPCRADCMDR is a register that sets the PCRADC mode.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	EXT_M ODE	—	TR_SEL[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5	EXT_MODE	0	R/W	Sets whether PCR_extension is included in the calculation of D_PCRADC. The EXT_MODE bit can be set to 1 only when this block operates at (13.5 × n) MHz (n = 1, 2, 3, 4). 0: PCR_extension is not included in the D_PCRADC calculation. 1: PCR_extension is included in the D_PCRADC calculation.
4	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
3 to 0	TR_SEL[3:0]	H'0	R/W	These bits select a trigger signal for PCRADC to be input to the TSIF. 0000: A trigger signal is not selected. Other than above: Setting prohibited



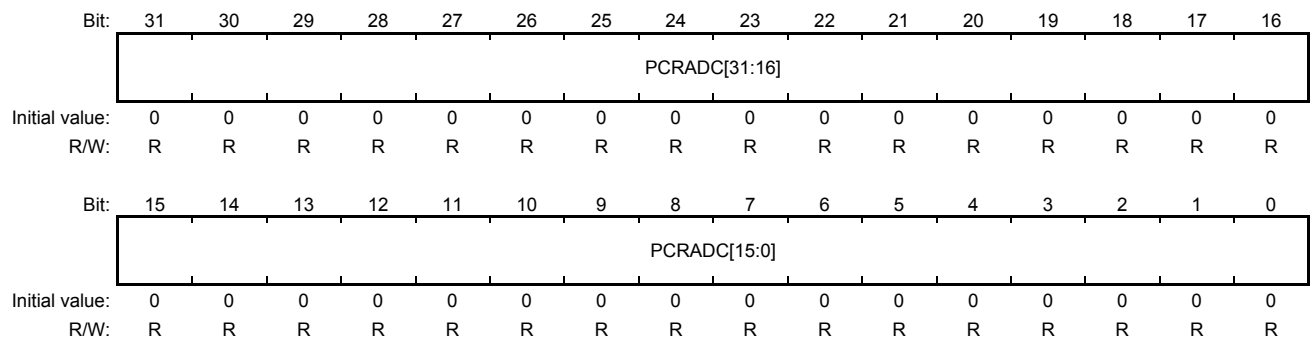
### 30.3.11 TSIF PCRADC Register (TSPCRADCR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
—	√	—	—

TSPCRADCR is a register that indicates the PCR value incremented by the internal clock (indicates time in a unit of 90 kHz).

After a reset is released, inputting a PCR packet starts counting up. Then, the counter value is corrected by using the PCR value in the stream each time a PCR packet is input.

This register is also updated in the packet asynchronous state.

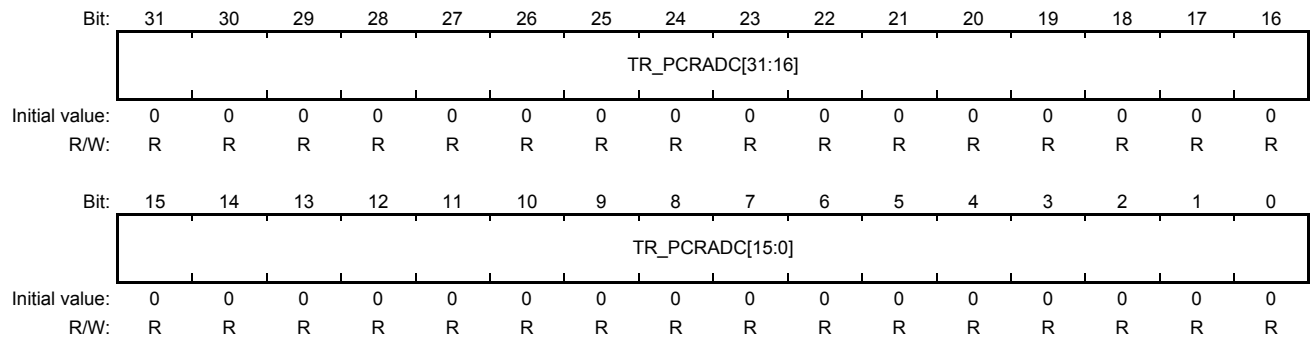


Bit	Bit Name	Initial Value	R/W	Description
31 to 0	PCRADC [31:0]	H'0000 0000	R	These bits indicate the PCR value incremented by the internal clock. PCRMD in TSCTLR = 0: These bits indicate time in 90-kHz units. PCRMD in TSCTLR = 1: These bits indicate time in 45-kHz units.

**30.3.12 TSIF TR\_PCRADC Register (TSTRPCRADCR)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
—	√	—	—

TSTRPCRADCR indicates the value of PCRADC read by a trigger signal for PCRADC selected by the TR\_SEL bit (indicates time in a unit of 90 kHz).



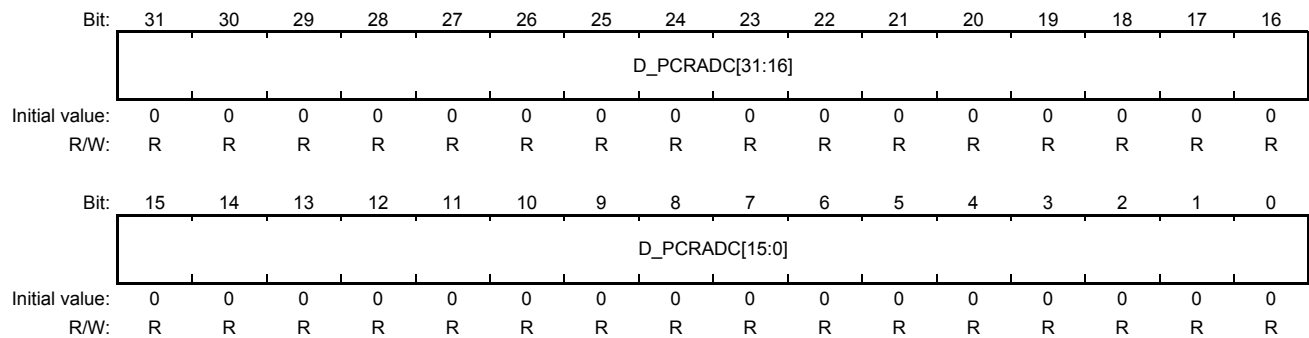
Bit	Bit Name	Initial Value	R/W	Description
31 to 0	TR_PCRADC [31:0]	H'0000 0000	R	These bits indicate the PCRADC value read by a trigger signal for PCRADC selected by the TR_SEL bit. PCRMD in TSCTLR = 0: These bits indicate time in 90-kHz units. PCRMD in TSCTLR = 1: These bits indicate time in 45-kHz units.

**30.3.13 TSIF D\_PCRADC Register (TSDPCRADC)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
—	√	—	—

TSDPCRADC indicates the value of the stream PCR minus PCRADC. After a reset is released and a second packet is input, the value of this register is valid.

When the value of the stream PCR minus PCRADC is greater than 32767 or smaller than -32768, the bits D\_PCRADC[31:16] indicate H'8000. (The setting of PCRMD in TSCTLR does not affect D\_PCRADC. D\_PCRADC[31:16] and D\_PCRADC[15:0] indicate a clock difference in a unit of 90 kHz and 27 MHz, respectively.)



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	D_PCRADC [31:0]	H'0000 0000	R	These bits indicate the value of the stream PCR minus PCRADC.

### 30.3.14 TSIF Free Run Counter L (TSFRCL)

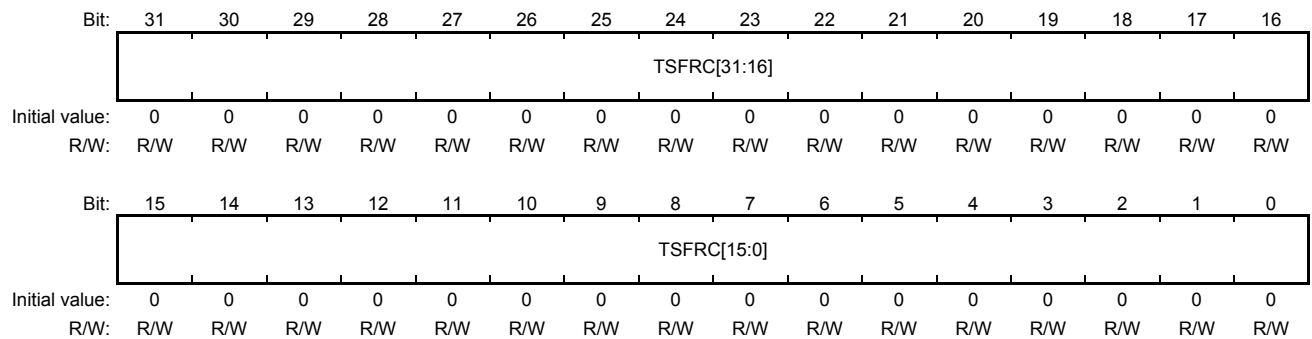
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
—	√	—	—

TSFRCL is a 32-bit free-running counter that counts up cycles of the clock set by FRCPSC[7:0] in TSCTLR or the clock from the internal prescaler.

This counter starts counting up after the clock signal selected by the FRCSEL and FRCPSC bits in TSCTLR is set to 1.

TSFRCL is initialized to H'00000000 by a power-on reset or manual reset. Setting TFA in TSCTLR to 0 does not initialize this counter.

Setting FRCADD in TSCTLR to B'01 stores the TSFRCL value (timestamp), which is recorded at the times of PID matches, in the 189th to 192nd bytes of TSTDR.



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	TSFRC[31:0]	H'0000 0000	R/W	Indicate the value of the free-running counter (lower).

### 30.3.15 TSIF Free Run Counter H (TSFRCH)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
—	√	—	—

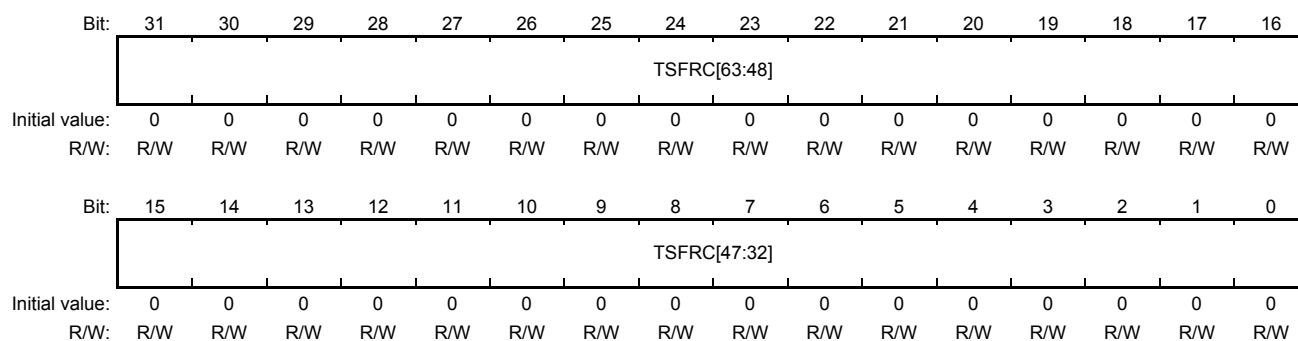
TSFRCH is cascade-connectable to TSFRCL (both are 32-bit free-running counters) to function as a 64-bit free-running counter.

Obtaining operation as a 64-bit counter requires setting the FRCADD bits in TSCTLR to B'11.

This counter starts counting up once the clock signal selected by the FRCSEL and FRCPSC bits in TSCTLR is set to 1.

TSFRCH is initialized to H'00000000 by a power-on reset or manual reset. Setting TFA in TSCTLR to 0 does not initialize this counter.

Setting FRCADD in TSCTLR to B'11 stores the TSFRC (H/L) value (timestamp), which is recorded at the times of PID matches, in the 189th to 196th bytes of TSTDR.



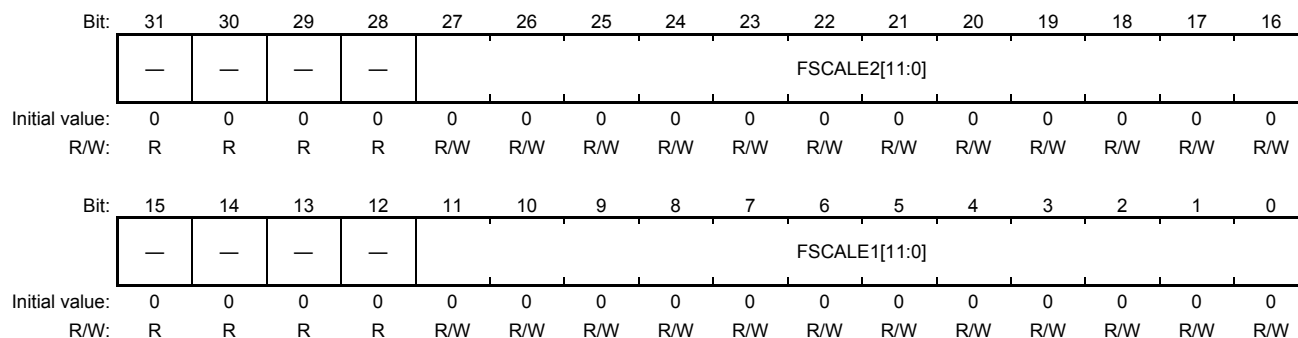
Bit	Bit Name	Initial Value	R/W	Description
31 to 0	TSFRC[63:32]	H'0000 0000	R/W	Indicate the value of the free-running counter (upper).

### 30.3.16 TSIF FSCALE Register (TSFSCALER)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
—	√	—	—

TSFSCALER is a register that sets counter values 1 and 2 of the internal prescaler used in TSFRC. Set the value of the FSCALE2 bit so that the value is equivalent to the value of the FSCALE1 bit plus 1.

The specifications of the setting follow TSFSCALER.



Bit	Bit Name	Initial Value	R/W	Description
31 to 28	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
27 to 16	FSCALE2 [11:0]	H'000	R/W	These bits set counter value 2 of the internal prescaler used in TSFRC.
15 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11 to 0	FSCALE1 [11:0]	H'000	R/W	These bits set counter value 1 of the internal prescaler used in TSFRC.

**30.3.17 TSIF FSCALE\_R Register (TSFSCALERR)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
—	√	—	—

TSFSCALERR is a register that sets the ratio of counter values 1 and 2 of the internal prescaler used in TSFRC.

Set the values of the FSCALE\_R1 bit and the FSCALE\_R2 bit so that the sum of these two bits is 9.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	FSCALE_R2[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	FSCALE_R1[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 20	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
19 to 16	FSCALE_R2 [3:0]	H'0	R/W	These bits set the ratio of counter value 2 of the internal prescaler used in TSFRC.
15 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3 to 0	FSCALE_R1 [3:0]	H'0	R/W	These bits set the ratio of counter value 1 of the internal prescaler used in TSFRC.

**30.3.18 TSIF Compare Match Control Register (TSCMCTLR)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
—	√	—	—

TSCMCTLR chooses running or stopping of TSIF compare match counter 0 and TSIF compare match counter 1.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PIDEX	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	CM1GO	—	—	—	CM0GO
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	PIDEX	0	R/W	This bit chooses use or not use from select sections PID_34 to PID_64. 0: Not use 1: Use
30 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	CM1GO	0	R/W	This bit chooses running or stopping of TSIF compare match counter 1 (TSCMCNT1). 0: TSCMCNT1 stops counting. 1: TSCMCNT1 starts counting.
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	CM0GO	0	R/W	This bit chooses running or stopping of TSIF compare match counter 0 (TSCMCNT0). 0: TSCMCNT0 stops counting. 1: TSCMCNT0 starts counting.



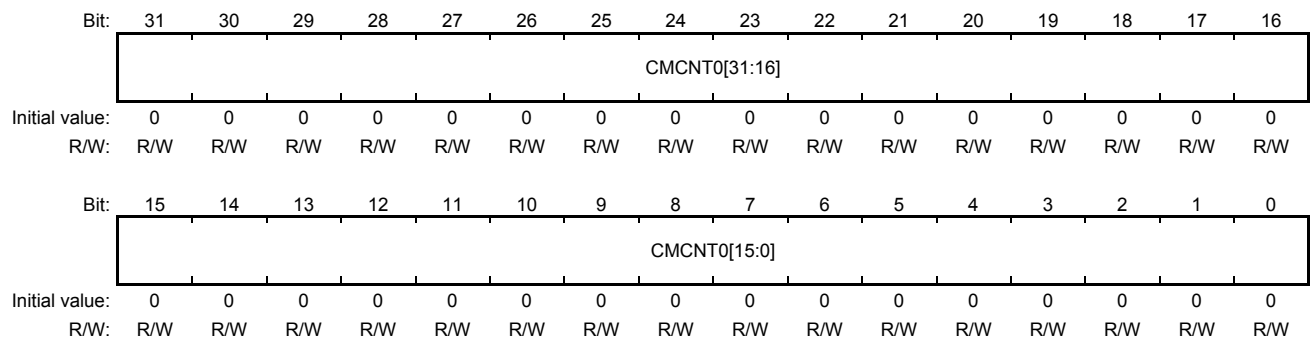
### 30.3.19 TSIF Compare Match Counter 0 (TSCMCNT0)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
—	√	—	—

TSCMCNT0 is a 32-bit free-running counter that counts down cycles of the clock set by TSCTLR.FRCPSC[7:0] or the clock from the internal prescaler used in TSFRC.

This counter starts counting down after the CM0GO bit in TSCMCTLR is set to 1.

TSCMCNT0 then counts down from the value set in TSCMCOR0, and if the setting of CM0GO is still 1 after the value of TSCMCNT0 reaches H'0000\_0000, TSCMCNT0 again starts counting down from the value set in TSCMCOR0.



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	CMCNT0 [31:0]	H'0000 0000	R/W	These bits show a value of the TSIF compare match counter 0.

### 30.3.20 TSIF Compare Match Counter 1 (TSCMCNT1)

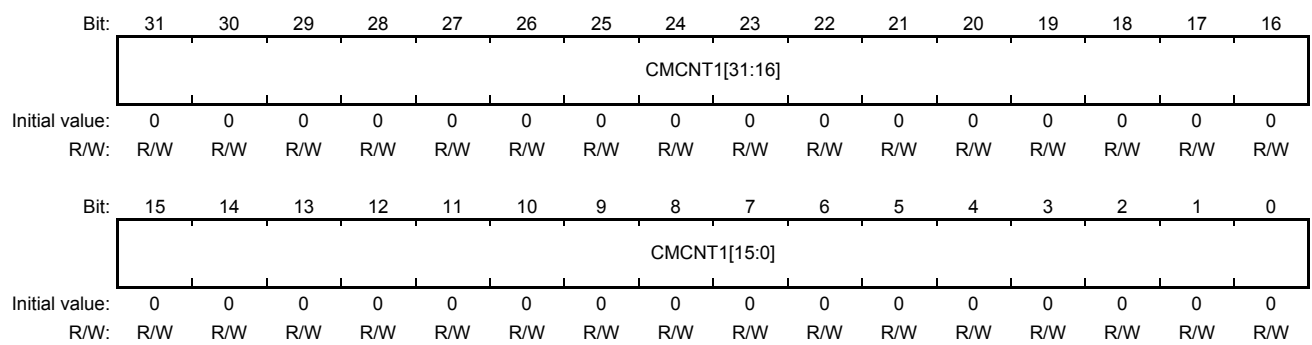
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
—	√	—	—

TSCMCNT1 is a one-shot (i.e., not cyclic) 32-bit counter that counts down cycles of the clock set in TSCTLR.FRCPSC[7:0] or the clock from the internal prescaler used in TSFRC.

This counter starts counting down after the CM1GO bit in TSCMCTLR is set to 1.

TSCMCNT1 stops after the value has reached H'0000\_0000.

To make the counter run again, write 0 and then 1 to CM1GO.



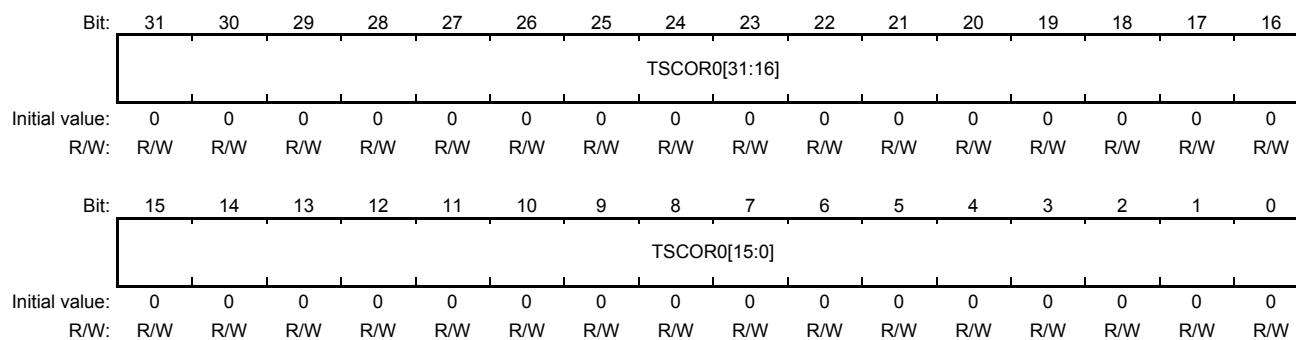
Bit	Bit Name	Initial Value	R/W	Description
31 to 0	CMCNT1 [31:0]	H'0000 0000	R/W	These bits show a value of the TSIF compare match counter 1.

### 30.3.21 TSIF Compare Match Constant Register 0 (TSCMCOR0)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
—	√	—	—

TSCMCOR0 sets a value when TSIF compare match counter 0 (TSCMCNT0) starts counting down..

A value of TSCMCOR0 is loaded to TSCMCNT0 after the CM0GO bit in TSCMCTLR is set to 1.



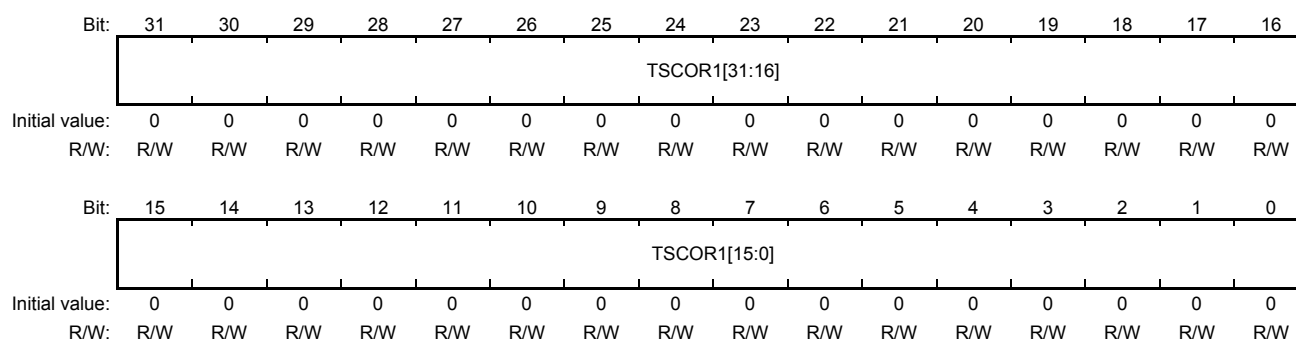
Bit	Bit Name	Initial Value	R/W	Description
31 to 0	TSCOR0 [31:0]	H'0000 0000	R/W	These bits set a value when the TSIF compare match counter 0 starts counting down.

### 30.3.22 TSIF Compare Match Constant Register 1 (TSCMCOR1)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
—	√	—	—

TSCMCOR1 sets a value when TSIF compare match counter 1 (TSCMCNT1) starts counting down..

A value of TSCMCOR1 is loaded to TSCMCNT1 after the CM1GO bit in TSCMCTLR is set to 1.



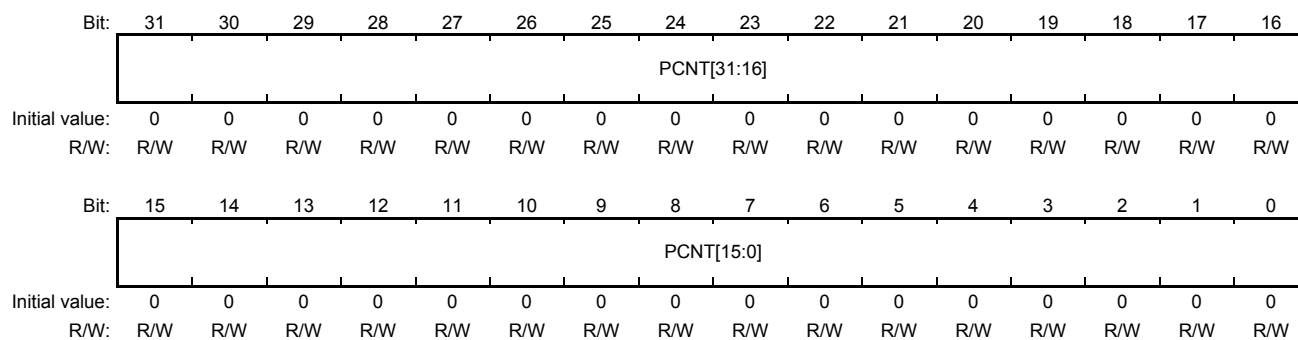
Bit	Bit Name	Initial Value	R/W	Description
31 to 0	TSCOR1 [31:0]	H'0000 0000	R/W	These bits set a value when the TSIF compare match counter 1 starts counting down.

### 30.3.23 TSIF TS Packet Count Register (TSPCNT)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
—	√	—	—

TSPCNT is a 32-bit register showing the number of TS packets to be read by DMA from TSTSDR.

Writing 1 to TSPCNTPSH.PCTPH initializes TSPCNT to H'0000\_0000.



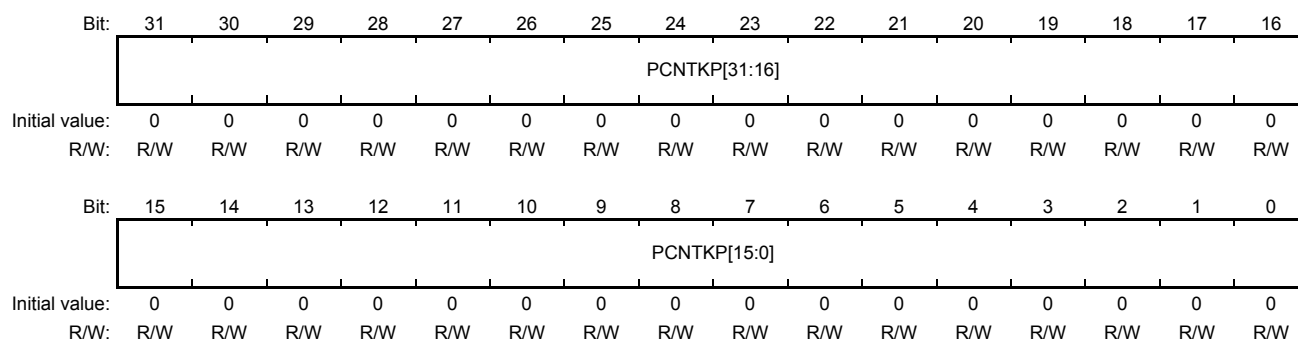
Bit	Bit Name	Initial Value	R/W	Description
31 to 0	PCNT[31:0]	H'0000 0000	R/W	These bits show a TS packet number read by DMA from TSTSDR. Counting up stops when the value has reached H'FFFF FFFF.

### 30.3.24 TSIF TS Packet Count Keep Register (TSPCNTKP)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
—	√	—	—

TSPCNTKP is a 32-bit register.

TSPCNTKP retains the number of TS packets indicated by TSPCNT when 1 is written to TSPCNTPSH.PCTPH.



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	PCNTKP [31:0]	H'0000 0000	R/W	After writing 1 to TSPCNTPSH.PCTPH, these bits indicate the number of TS packet read by DMA from TSTSDR at that time.

**30.3.25 TSIF TS Packet Count Push Register (TSPCNTPSH)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
—	√	—	—

TSPCNTPSH is a 32-bit register.

Writing 1 to PCTPH causes copying of the TSPCNT value at that time to TSPCNTKP, which retains that value.

The PCTPH bit must be cleared whenever you want to copy the retained value again.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PCTPH
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	PCTPH	0	R/W	Writing 1 to this bit causes copying of the TSPCNT value at that time to TSPCNTKP. The PCTPH bit must be cleared whenever you want to copy the retained value again.

## 30.4 Operation

RZ/G1H	RZ/G1N
RZ/G1M	RZ/G1E

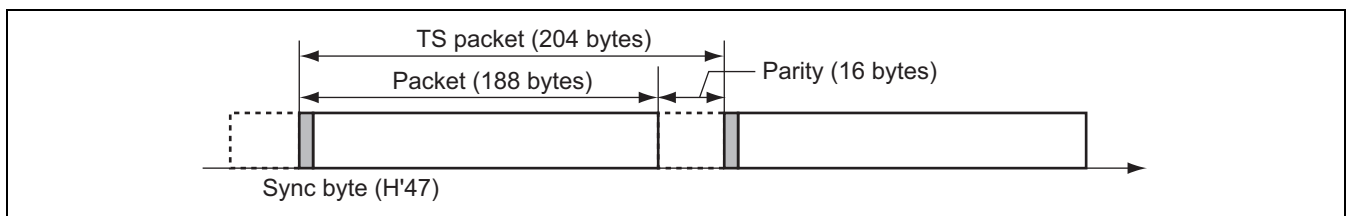
### 30.4.1 TS Data Protocol

The TS packet supported by this LSI consists of 188-byte execution data including the sync byte and 16-byte Reed-Solomon code (parity data) for an error correction, with configuration of 204 bytes in total (Figure 30.2). The TSIF supports 188 bytes (without parity) and 204 bytes (with parity) of TS data formats.

The data input pins consist of the following.

- Serial data (TS\_SDAT) input
- Serial data clock (TS\_SCK) input
- Synchronous (TS\_SPSYNC) input
- Enable (TS\_SDEN) input

Depending on the specifications of the LSI to be connected, the polarity of these pins can be switched by software (Figure 30.3).



**Figure 30.2 MPEG2-TS Packet Configuration**

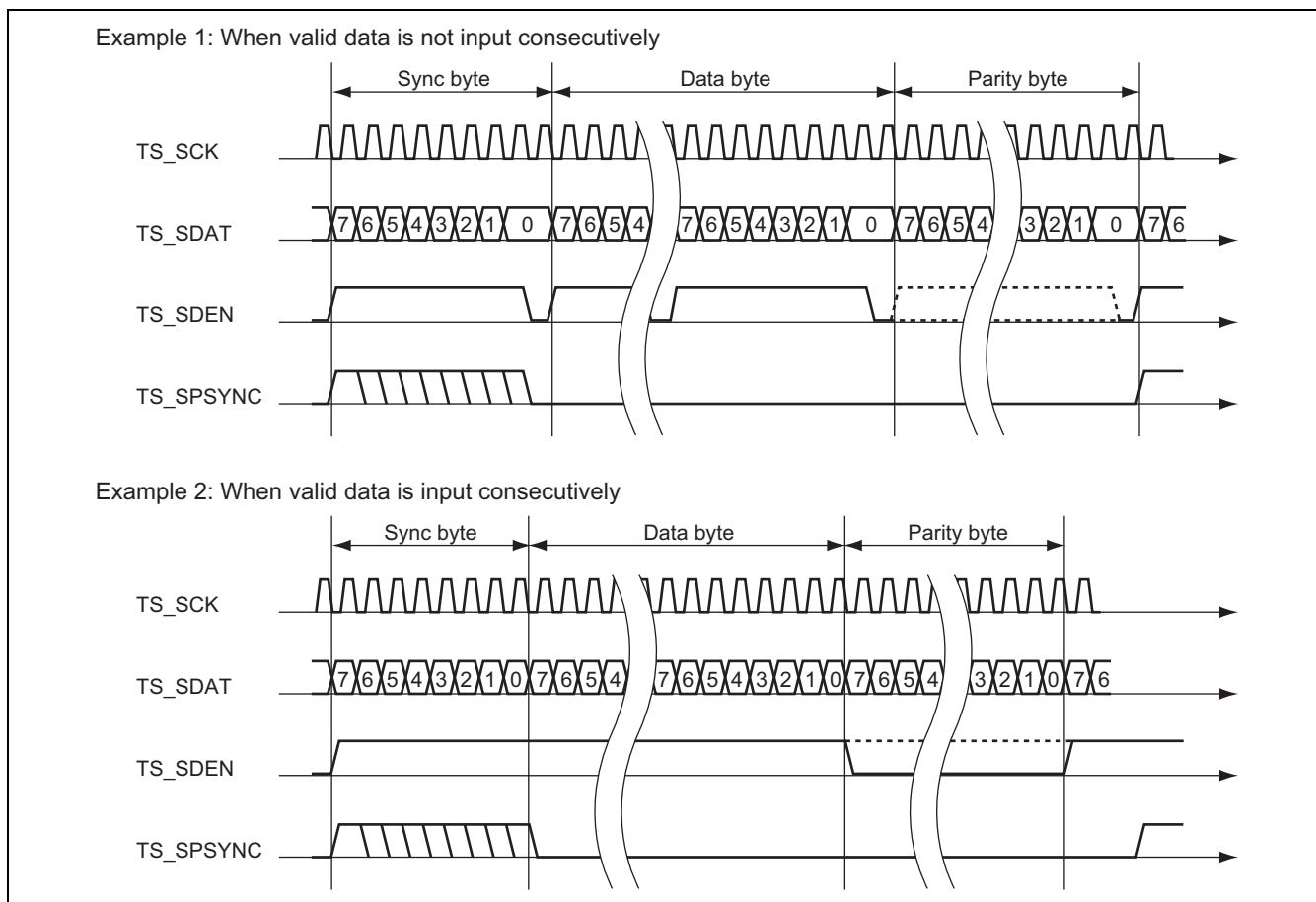


Figure 30.3 Timing of TS Data Serial Input

### 30.4.2 Synchronous Processing Unit

The function of synchronous processing is to synchronize packets for carrying out the subsequent PID filtering and such.

The TS packet data is constantly sent from a terrestrial station. The receiving terminal starts receiving the data regardless of the timing of the sender. This causes the receiving terminal to receive an incomplete packet. The synchronous processing is essential to identify the start of TS packet data that are not played from the start and accurately process various data in the packet.

Moreover, as the signal quality of input data may deteriorate according to the transmission status, the TS packet data received via a tuner, OFDM demodulator, and the like may contain errors. The synchronous processing includes protection against such errors.

When the receiving terminal is started up, it searches for the sync byte (H'47). If the sync byte is detected, the receiving terminal checks whether or not the sync byte will appear again after one packet cycle (188 bytes or 204 bytes). If the sync byte appears twice consecutively, synchronization is confirmed. Once synchronized, even when the sync byte does not appear at a fixed position, an error is not generated immediately and the regular processing is continued.

When the sync byte has not appeared 4 times consecutively, the receiving terminal determines that synchronization is lost. Once synchronization is lost, the process for synchronization starts in the same way as when the receiving terminal is started up.

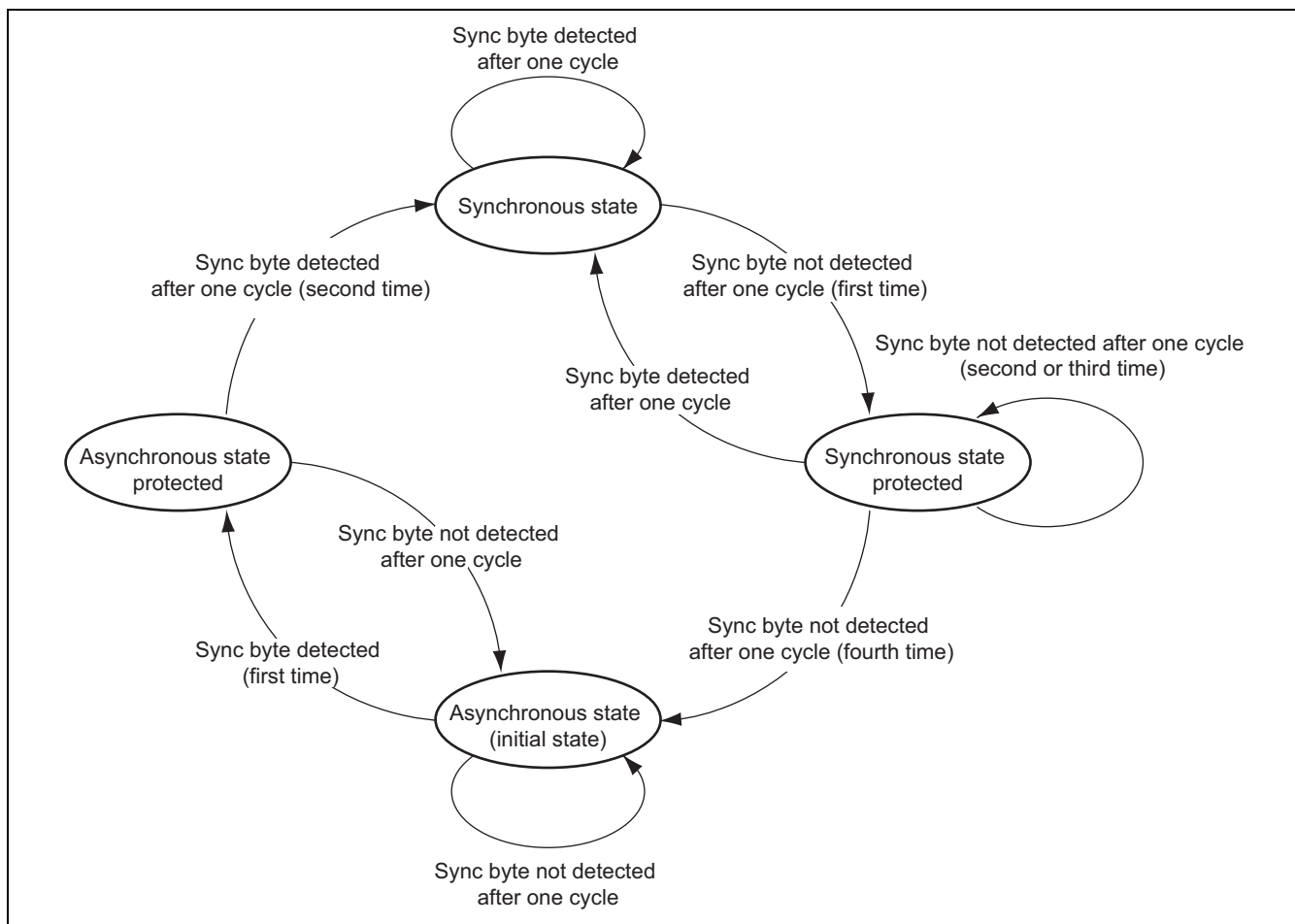


Figure 30.4 Detection State Configuration of Sync Byte

### 30.4.3 PID Filter Unit

PID filtering checks the PIDs of TS packets. If they match the predefined PID table values, the packets are stored in the buffer.

A total of 67 values can be registered as PID values. However, the values for PAT (H'0000) and CAT (H'0001) are fixed and not changeable. Even though the PID values for the PCR packet, video packet, and audio packet should be specified in the dedicated sections, respectively, another 62 PID values can be specified in any of the sections.

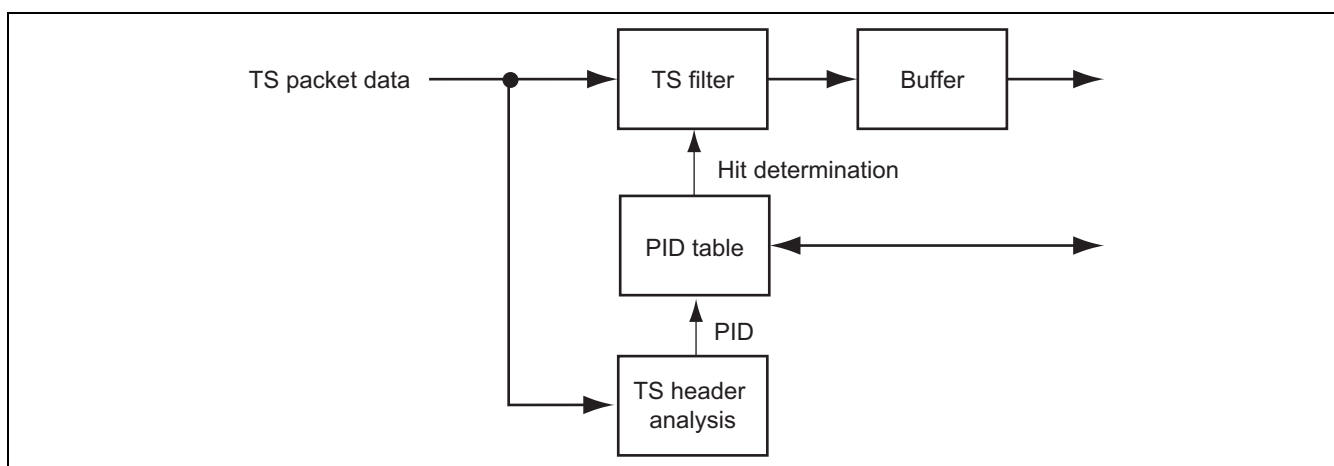


Figure 30.5 Block Diagram of PID Filtering



**Table 30.6 PID Table**

No.	Section	PID Value (12 Bits)	Description
1	Video	Any setting	Dedicated for video packet
2	Audio	Any setting	Dedicated for audio packet
3	PID1	Any setting	For any packet
4	PID2	Any setting	For any packet
5	PID3	Any setting	For any packet
6	PID4	Any setting	For any packet
7	PID5	Any setting	For any packet
8	PID6	Any setting	For any packet
9	PID7	Any setting	For any packet
10	PID8	Any setting	For any packet
11	PID9	Any setting	For any packet
12	PID10	Any setting	For any packet
13	PID11	Any setting	For any packet
14	PID12	Any setting	For any packet
15	PID13	Any setting	For any packet
16	PID14	Any setting	For any packet
17	PID15	Any setting	For any packet
18	PID16	Any setting	For any packet
19	PID17	Any setting	For any packet
20	PID18	Any setting	For any packet
21	PID19	Any setting	For any packet
22	PID20	Any setting	For any packet
23	PID21	Any setting	For any packet
24	PID22	Any setting	For any packet
25	PID23	Any setting	For any packet
26	PID24	Any setting	For any packet
27	PID25	Any setting	For any packet
28	PID26	Any setting	For any packet
29	PID27	Any setting	For any packet
30	PID28	Any setting	For any packet
31	PID29	Any setting	For any packet
32	PID30	Any setting	For any packet
33	PID31	Any setting	For any packet
34	PID32	Any setting	For any packet
35	PID33	Any setting	For any packet
36	PID34	Any setting	For any packet
37	PID35	Any setting	For any packet
38	PID36	Any setting	For any packet
39	PID37	Any setting	For any packet
40	PID38	Any setting	For any packet
41	PID39	Any setting	For any packet
42	PID40	Any setting	For any packet

No.	Section	PID Value (12 Bits)	Description
43	PID41	Any setting	For any packet
44	PID42	Any setting	For any packet
45	PID43	Any setting	For any packet
46	PID44	Any setting	For any packet
47	PID45	Any setting	For any packet
48	PID46	Any setting	For any packet
49	PID47	Any setting	For any packet
50	PID48	Any setting	For any packet
51	PID49	Any setting	For any packet
52	PID50	Any setting	For any packet
53	PID51	Any setting	For any packet
54	PID52	Any setting	For any packet
55	PID53	Any setting	For any packet
56	PID54	Any setting	For any packet
57	PID55	Any setting	For any packet
58	PID56	Any setting	For any packet
59	PID57	Any setting	For any packet
60	PID58	Any setting	For any packet
61	PID59	Any setting	For any packet
62	PID60	Any setting	For any packet
63	PID61	Any setting	For any packet
64	PID62	Any setting	For any packet
65	PAT	Fixed to H'0000	Dedicated for PAT packet
66	CAT	Fixed to H'0001	Dedicated for CAT packet
67	PCR	Any setting	Dedicated for PCR packet

### 30.4.4 Bitstream Search Unit

The function of the bitstream search unit is to check the contents of the PCR and video packets to reduce the load of software. The functions listed below are available.

1. PCR discontinuity check

PCR discontinuity (discontinuity-indicator) is automatically detected and reflected in the status register. This is to reduce the delay in software processing if a PCR packet is input. PCR is a reference clock sent from a base station (broadcasting station) and may be switched to another PCR because of program changes and so on.

2. PCR\_flag detection

The PCR\_flag is detected from the adaptation\_field of the TS packet and reflected in the status register.

3. random\_access\_indicator detection

The random\_access\_indicator is detected from the adaptation\_field of the TS packet and reflected in the status register.

4. Duplicate packet delete

The PID and continuity\_counter are checked from consecutive TS packets to prevent duplicate TS data from being stored in the buffer.

5. Start code check

When a start code (H'0000 01xx) is contained in a video stream, it is reflected in the status register. The start code marks the boundary in image data of the MPEG standard and is applied at the start of a sequence, image, and such.

6. Short header check

When a short header (B'0000 0000 0000 0000 1000 00xx xxxx xxxx) is contained in a video stream, it is reflected in the status register.

These processes are performed in the adaptation field analysis unit and the ES data search unit.

At the time of TS header analysis for PID filtering, the presence of an adaptation field is analyzed. When hit information of a PCR packet or video packet in the PID table is input, the necessary process at each block is initiated.

Each result is reflected in the status register.

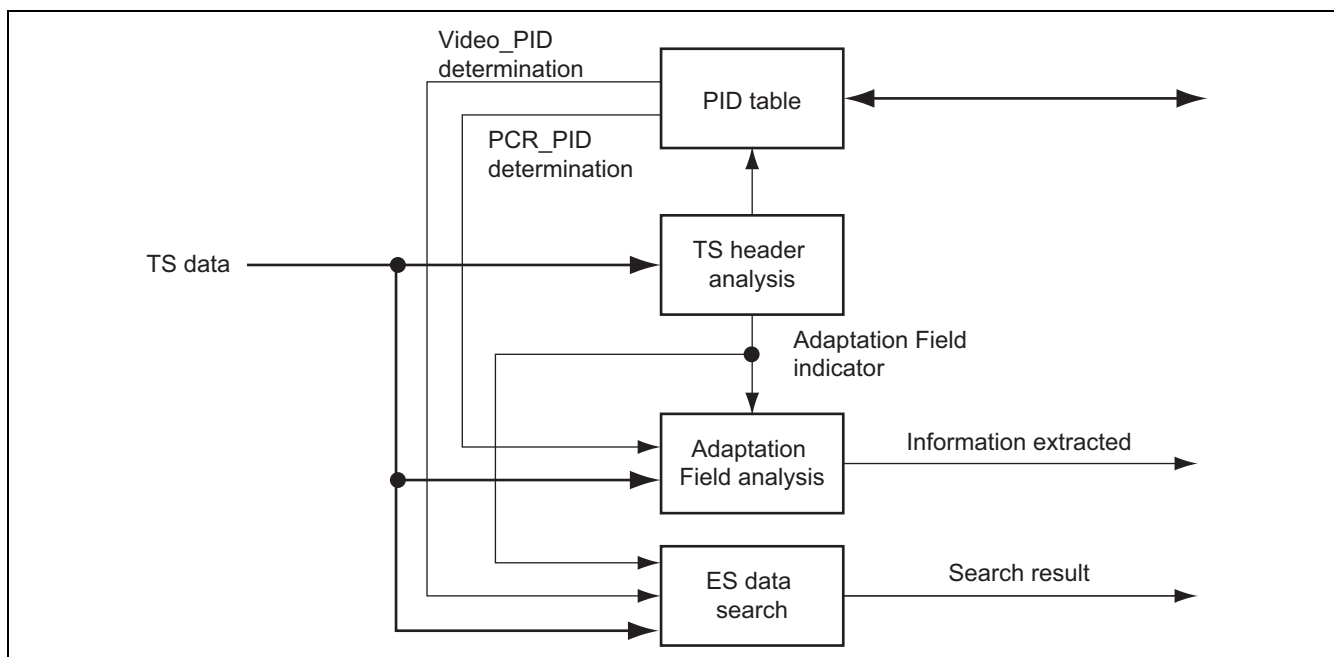
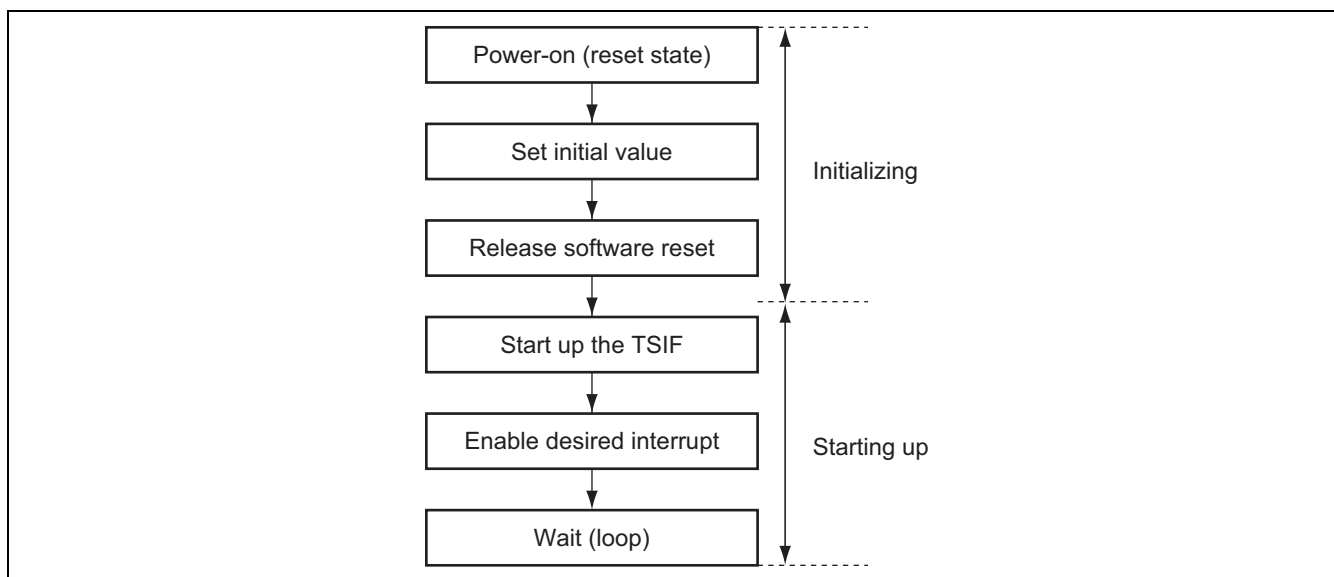


Figure 30.6 Block Diagram of Stream Search Unit

### 30.4.5 Process Flow

Figure 30.7 shows an outline of the process flow in the TSIF module.

Since the TSIF is in the reset state at power-on, it does not generate any signals until the initialization is completed. A TS packet ID (PID) to be extracted by the TSIF is set in the PID table. After other necessary settings have been completed, software reset is released and the TSIF is started up while a desired interrupt is allowed at the same time. After this, the TSIF waits until the necessary TS packet is extracted.



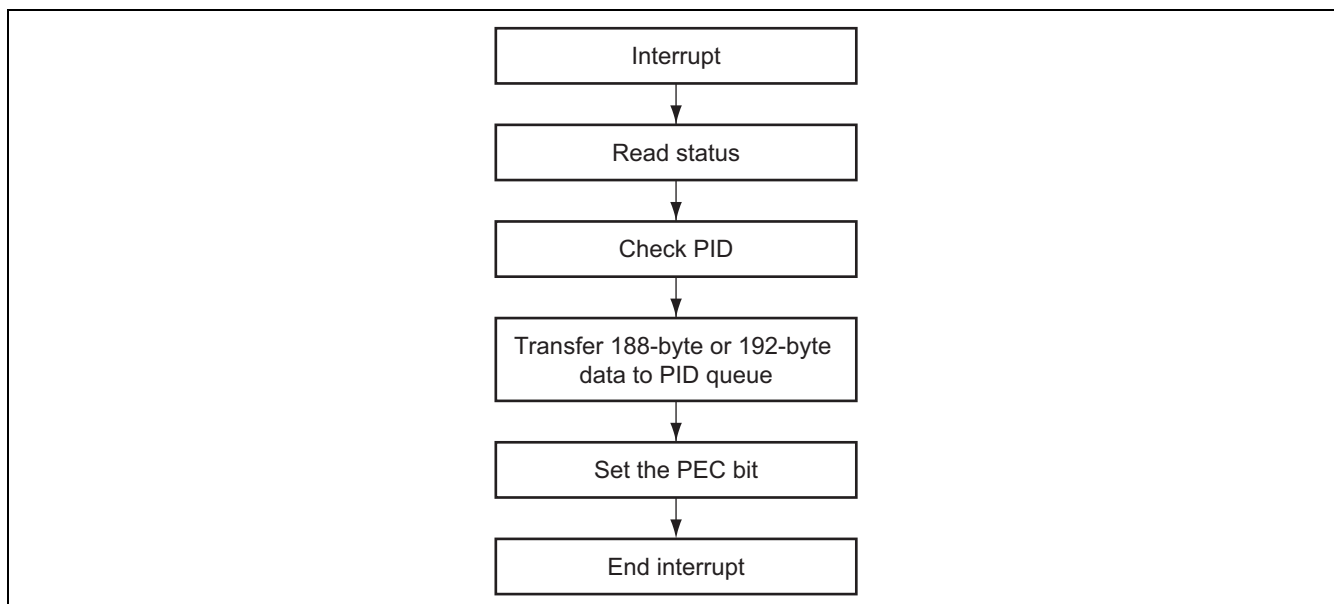
**Figure 30.7 TSIF Process Flow**

Two types of TS packet transfer are available as described below.

#### (1) DMA interrupt transfer mode (Figure 30.8)

The interrupt routine transfers the packet data stored in the buffer to a queue created in memory. Multiple queues must be created depending on the values of PIDs (e.g., video or audio). When an interrupt is generated, the TSSTR register is read first. If a status error is detected during reading, and the packet data is going to be discarded, the PEC bit in the TSBUFCLRR register should be set. The value of the PID bit in the TSSTR register should then be checked.

For example, if the packet is a video packet, it will be transferred to a video packet queue by DMA and so on. After 188-byte data is transferred or TS data plus TSFRC (192 bytes or 196 bytes) is transferred, the PEC bit must be set to clear the internal buffer.



**Figure 30.8 TSIF Interrupt Process Flow**

## (2) DMA auto-transfer mode

To use this mode, the necessary setting should be made in the DMAC block before starting up the TSIF. When a single TS packet (188 bytes) is input or a single TS packet plus TSFRC (192 bytes or 196 bytes) is input, the TSIF automatically issues a transfer request signal to the DMA and starts DMA transfer. Using this mode reduces the frequency of interrupts.

# 31. Audio

RZ/G1H	RZ/G1N
RZ/G1M	RZ/G1E

## 31.1 Overview

This section describes the data path between audio modules, list of routings, and transfer flow.

### 31.1.1 Data Paths between Audio Modules

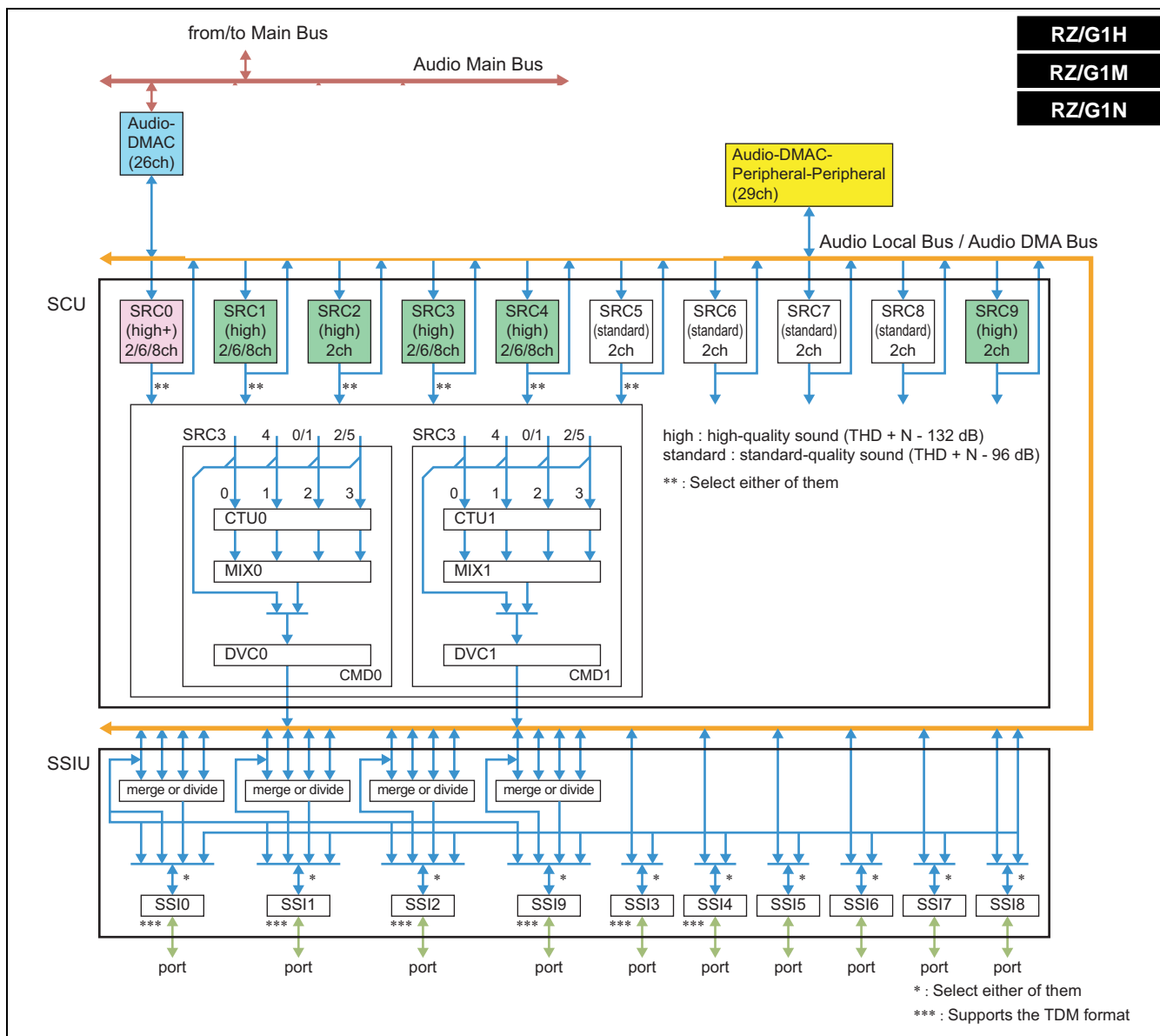


Figure 31.1a Data Paths between Audio Modules [RZ/G1H, RZ/G1M, and RZ/G1N]

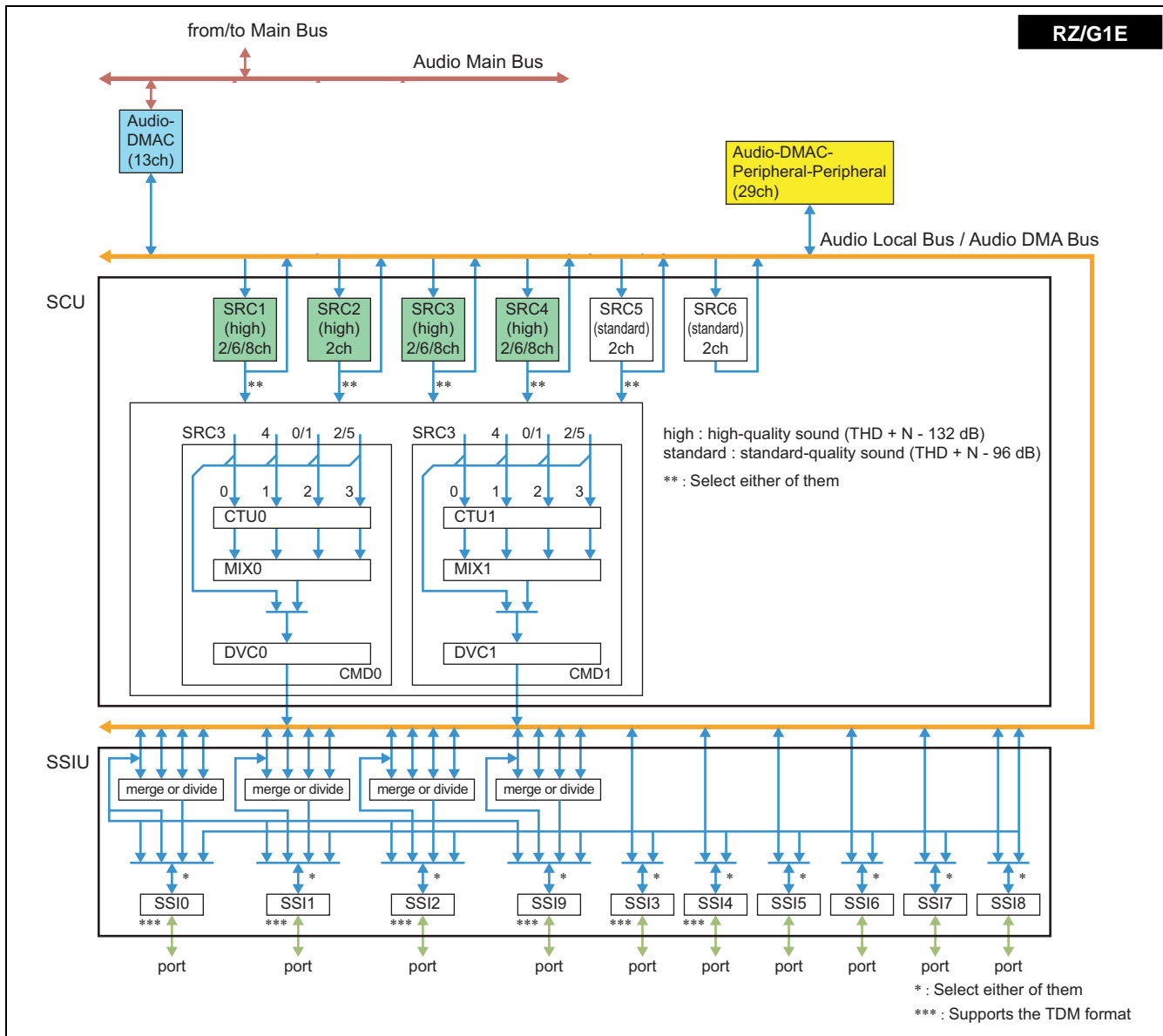


Figure 31.1b Data Paths between Audio Modules [RZ/G1E]

31.1.2 List of Routings

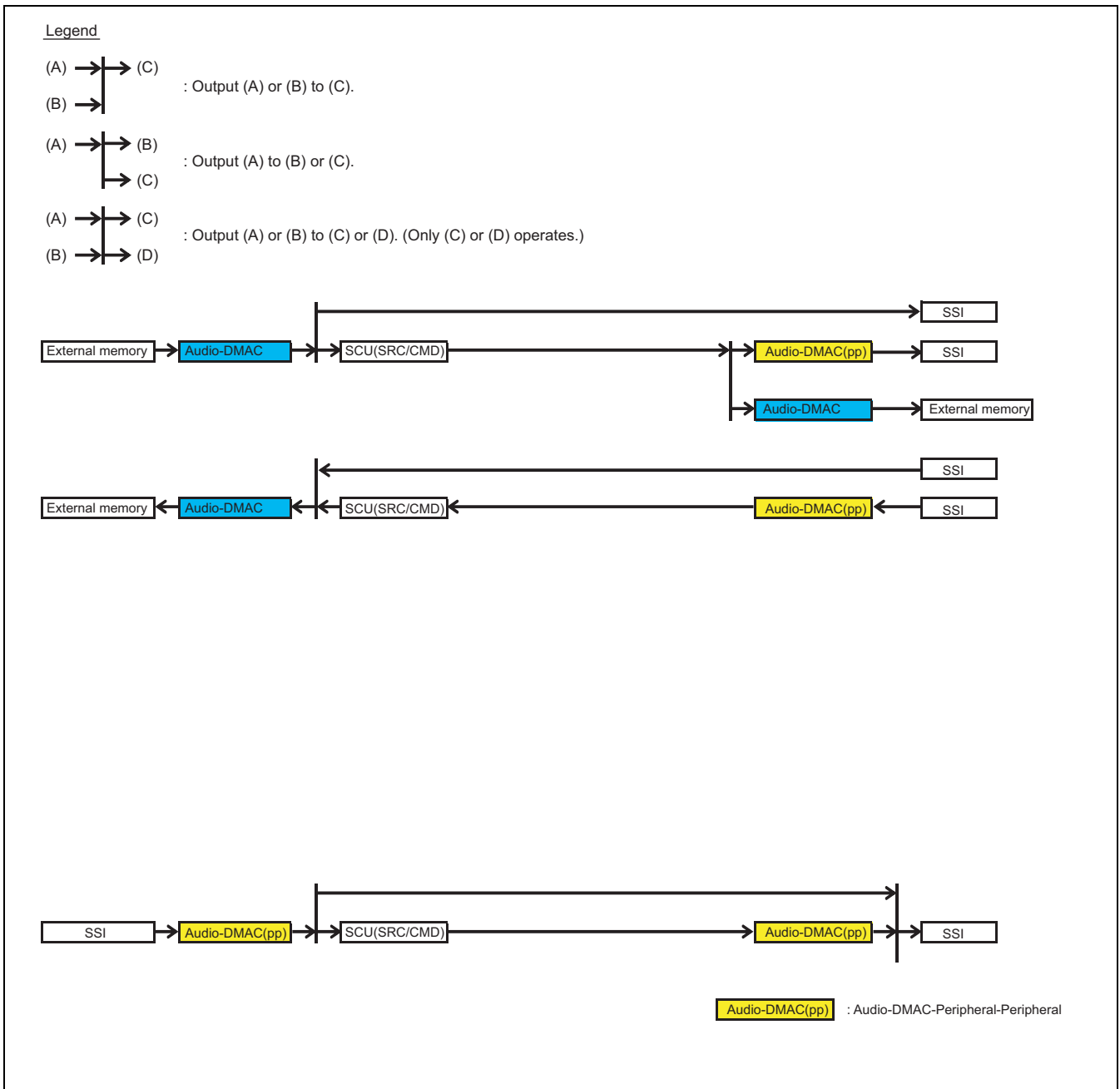


Figure 31.2 List of Routings



### 31.1.3 Audio-DMAC

The Audio-DMAC is used by data transfer between the external memory and audio modules. The setting values of DMASAR and DMADAR of the Audio-DMAC are shown in Table 31.1.

**Table 31.1 Setting Values of DMASAR and DMADAR of Audio-DMAC**

Name of Register	DMASAR/DMADAR	RZ/G Series Products			
		RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
SSI0-0_BUSIF	H'EC10_ 0000	√	√	√	√
SSI0-1_BUSIF	0400	√	√	√	√
SSI0-2_BUSIF	0800	√	√	√	√
SSI0-3_BUSIF	0C00	√	√	√	√
SSI1-0_BUSIF	1000	√	√	√	√
SSI1-1_BUSIF	1400	√	√	√	√
SSI1-2_BUSIF	1800	√	√	√	√
SSI1-3_BUSIF	1C00	√	√	√	√
SSI2-0_BUSIF	2000	√	√	√	√
SSI2-1_BUSIF	2400	√	√	√	√
SSI2-2_BUSIF	2800	√	√	√	√
SSI2-3_BUSIF	2C00	√	√	√	√
SSI3_BUSIF	3000	√	√	√	√
SSI4_BUSIF	4000	√	√	√	√
SSI5_BUSIF	5000	√	√	√	√
SSI6_BUSIF	6000	√	√	√	√
SSI7_BUSIF	7000	√	√	√	√
SSI8_BUSIF	8000	√	√	√	√
SSI9-0_BUSIF	9000	√	√	√	√
SSI9-1_BUSIF	9400	√	√	√	√
SSI9-2_BUSIF	9800	√	√	√	√
SSI9-3_BUSIF	9C00	√	√	√	√
SSITDR0*2	H'EC24_ 1008	√	√	√	√
SSIRDR0*1	100C	√	√	√	√
SSITDR1*2	1048	√	√	√	√
SSIRDR1*1	104C	√	√	√	√
SSITDR2*2	1088	√	√	√	√
SSIRDR2*1	108C	√	√	√	√
SSITDR3*2	10C8	√	√	√	√
SSIRDR3*1	10CC	√	√	√	√
SSITDR4*2	1108	√	√	√	√
SSIRDR4*1	110C	√	√	√	√
SSITDR5*2	1148	√	√	√	√
SSIRDR5*1	114C	√	√	√	√

## RZ/G Series Products

Name of Register	DMASAR/DMADAR		RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
SSITDR6*2	H'EC24_	1188	√	√	√	√
SSIRDR6*1		118C	√	√	√	√
SSITDR7*2		11C8	√	√	√	√
SSIRDR7*1		11CC	√	√	√	√
SSITDR8*2		1208	√	√	√	√
SSIRDR8*1		120C	√	√	√	√
SSITDR9*2		1248	√	√	√	√
SSIRDR9*1		124C	√	√	√	√
SRC0in_BUSIF*2	H'EC00_	0000	√	√	√	—
SRC1in_BUSIF*2		0400	√	√	√	√
SRC2in_BUSIF*2		0800	√	√	√	√
SRC3in_BUSIF*2		0C00	√	√	√	√
SRC4in_BUSIF*2		1000	√	√	√	√
SRC5in_BUSIF*2		1400	√	√	√	√
SRC6in_BUSIF*2		1800	√	√	√	√
SRC7in_BUSIF*2		1C00	√	√	√	—
SRC8in_BUSIF*2		2000	√	√	√	—
SRC9in_BUSIF*2		2400	√	√	√	—
SRC0out_BUSIF*1		4000	√	√	√	—
SRC1out_BUSIF*1		4400	√	√	√	√
SRC2out_BUSIF*1		4800	√	√	√	√
SRC3out_BUSIF*1		4C00	√	√	√	√
SRC4out_BUSIF*1		5000	√	√	√	√
SRC5out_BUSIF*1		5400	√	√	√	√
SRC6out_BUSIF*1		5800	√	√	√	√
SRC7out_BUSIF*1		5C00	√	√	√	—
SRC8out_BUSIF*1		6000	√	√	√	—
SRC9out_BUSIF*1		6400	√	√	√	—
CMD0out_BUSIF*1		8000	√	√	√	√
CMD1out_BUSIF*1		8400	√	√	√	√

Notes: 1. Used only by DMASAR.  
2. Used only by DMADAR.

### 31.1.4 Data Format on Audio Local Bus

Figure 31.3 shows the data formats handled in the audio local bus. When writing or reading data through the Audio-DMAC, align data to match the appropriate data format from those in Figure 31.3.

24-bit stereo data or multichannel data	
17- to 23-bit stereo data or multichannel data	
16-bit stereo data or multichannel data	
9- to 15-bit stereo data or multichannel data	
8-bit stereo data	
16-bit monaural data	
8-bit monaural data	





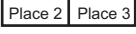
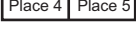

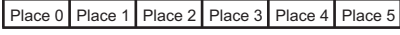


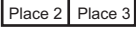
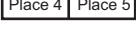
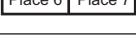

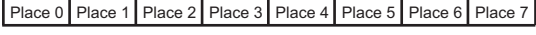
**Figure 31.3 Data Format**

- Notes: 1 Write 0 to the \* bits in the figure when writing data. When reading data, ignore the values read from these bits.
2. In the 8-bit stereo data format, (Lch/1) and (Rch/1) indicate the data pair to be processed first and (Lch/2) and (Rch/2) indicate the next data pair to be processed.
3. Only the MSB-first data formats can be used.
4. In the data formats of 16-bit stereo data or multichannel data and 9- to 15-bit stereo data or multichannel data, set SSI\_MODE0.ind\_word\_swap\* (\* = 0 to 9) in setting up of an independent SSI transmission (SSI\_MODE0.ind\* (\* = 0 to 9) = 1) in the SSIU module.

### 31.1.5 Rearranging the Order of Data

For the audio modules (SSI, and SCU), rearranging the order of data is possible in the channel unit. Places of data in each data format are defined as in Tables 31.2 to 31.4.

**Table 31.2 Definition of Data Places in Each Data Format (1)**

SSI · Stereo (2 channels)	SSI_WS0129  SSI_SDATA0 
SSI · Stereo x 3 (6 channels)	SSI_WS0129  SSI_SDATA0  SSI_SDATA1  SSI_SDATA2 
SSI · TDM (6 channels)	SSI_WS0129  SSI_SDATA0 
SSI · Stereo x 4 (8 channels)	SSI_WS0129  SSI_SDATA0  SSI_SDATA1  SSI_SDATA2  SSI_SDATA9 
SSI · TDM (8 channels)	SSI_WS0129  SSI_SDATA0 

**Table 31.3 Definition of Data Places in Each Data Format (2)**

<p>BUSIF · Stereo (2 channels) · 24 bits</p>	<p>External memory image</p> <table style="margin-left: 100px;"> <tr> <td></td> <td style="text-align: right;">31</td> <td style="text-align: left;">0</td> </tr> <tr> <td>H'00</td> <td style="border: 1px solid black; padding: 2px;">Place 0</td> <td style="border: 1px solid black; padding: 2px;">*</td> </tr> <tr> <td>H'04</td> <td style="border: 1px solid black; padding: 2px;">Place 1</td> <td style="border: 1px solid black; padding: 2px;">*</td> </tr> <tr> <td>H'08</td> <td style="border: 1px solid black; padding: 2px;">Place 0</td> <td style="border: 1px solid black; padding: 2px;">*</td> </tr> <tr> <td>H'0C</td> <td style="border: 1px solid black; padding: 2px;">Place 1</td> <td style="border: 1px solid black; padding: 2px;">*</td> </tr> <tr> <td>...</td> <td style="border: 1px solid black; padding: 2px;">...</td> <td style="border: 1px solid black; padding: 2px;">*</td> </tr> </table>		31	0	H'00	Place 0	*	H'04	Place 1	*	H'08	Place 0	*	H'0C	Place 1	*	...	...	*												
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H'00	Place 0	*																													
H'04	Place 1	*																													
H'08	Place 0	*																													
H'0C	Place 1	*																													
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<p>BUSIF · Stereo (2 channels) · 16 bits</p>	<p>External memory image</p> <table style="margin-left: 100px;"> <tr> <td></td> <td style="text-align: right;">31</td> <td style="text-align: left;">0</td> </tr> <tr> <td>H'00</td> <td style="border: 1px solid black; padding: 2px;">Place 0</td> <td style="border: 1px solid black; padding: 2px;">Place 1</td> </tr> <tr> <td>H'04</td> <td style="border: 1px solid black; padding: 2px;">Place 0</td> <td style="border: 1px solid black; padding: 2px;">Place 1</td> </tr> <tr> <td>H'08</td> <td style="border: 1px solid black; padding: 2px;">Place 0</td> <td style="border: 1px solid black; padding: 2px;">Place 1</td> </tr> <tr> <td>H'0C</td> <td style="border: 1px solid black; padding: 2px;">Place 0</td> <td style="border: 1px solid black; padding: 2px;">Place 1</td> </tr> <tr> <td>...</td> <td style="border: 1px solid black; padding: 2px;">...</td> <td style="border: 1px solid black; padding: 2px;">...</td> </tr> </table>		31	0	H'00	Place 0	Place 1	H'04	Place 0	Place 1	H'08	Place 0	Place 1	H'0C	Place 0	Place 1	...	...	...												
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H'04	Place 0	Place 1																													
H'08	Place 0	Place 1																													
H'0C	Place 0	Place 1																													
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<p>BUSIF · Stereo (2 channels) · 8 bits</p>	<p>External memory image</p> <table style="margin-left: 100px;"> <tr> <td></td> <td style="text-align: right;">31</td> <td style="text-align: left;">0</td> </tr> <tr> <td>H'00</td> <td style="border: 1px solid black; padding: 2px;">Place 1</td> <td style="border: 1px solid black; padding: 2px;">Place 0</td> <td style="border: 1px solid black; padding: 2px;">Place 1</td> <td style="border: 1px solid black; padding: 2px;">Place 0</td> </tr> <tr> <td>H'04</td> <td style="border: 1px solid black; padding: 2px;">Place 1</td> <td style="border: 1px solid black; padding: 2px;">Place 0</td> <td style="border: 1px solid black; padding: 2px;">Place 1</td> <td style="border: 1px solid black; padding: 2px;">Place 0</td> </tr> <tr> <td>...</td> <td style="border: 1px solid black; padding: 2px;">...</td> <td style="border: 1px solid black; padding: 2px;">...</td> <td style="border: 1px solid black; padding: 2px;">...</td> <td style="border: 1px solid black; padding: 2px;">...</td> </tr> </table>		31	0	H'00	Place 1	Place 0	Place 1	Place 0	H'04	Place 1	Place 0	Place 1	Place 0	...	...	...	...	...												
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H'04	Place 1	Place 0	Place 1	Place 0																											
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<p>BUSIF · Monaural (1 channel) · 8/16 bits</p>	<p>External memory image</p> <table style="margin-left: 100px;"> <tr> <td></td> <td style="text-align: right;">31</td> <td style="text-align: left;">0</td> </tr> <tr> <td>H'00</td> <td style="border: 1px solid black; padding: 2px;">Place 0</td> <td style="border: 1px solid black; padding: 2px;">*</td> </tr> <tr> <td>H'04</td> <td style="border: 1px solid black; padding: 2px;">Place 0</td> <td style="border: 1px solid black; padding: 2px;">*</td> </tr> <tr> <td>H'08</td> <td style="border: 1px solid black; padding: 2px;">Place 0</td> <td style="border: 1px solid black; padding: 2px;">*</td> </tr> <tr> <td>H'0C</td> <td style="border: 1px solid black; padding: 2px;">Place 0</td> <td style="border: 1px solid black; padding: 2px;">*</td> </tr> <tr> <td>...</td> <td style="border: 1px solid black; padding: 2px;">...</td> <td style="border: 1px solid black; padding: 2px;">*</td> </tr> </table>		31	0	H'00	Place 0	*	H'04	Place 0	*	H'08	Place 0	*	H'0C	Place 0	*	...	...	*												
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H'00	Place 0	*																													
H'04	Place 0	*																													
H'08	Place 0	*																													
H'0C	Place 0	*																													
...	...	*																													
<p>BUSIF · Multichannel (4 channels) · 24 bits</p>	<p>External memory image</p> <table style="margin-left: 100px;"> <tr> <td></td> <td style="text-align: right;">31</td> <td style="text-align: left;">0</td> </tr> <tr> <td>H'00</td> <td style="border: 1px solid black; padding: 2px;">Place 0</td> <td style="border: 1px solid black; padding: 2px;">*</td> </tr> <tr> <td>H'04</td> <td style="border: 1px solid black; padding: 2px;">Place 1</td> <td style="border: 1px solid black; padding: 2px;">*</td> </tr> <tr> <td>H'08</td> <td style="border: 1px solid black; padding: 2px;">Place 2</td> <td style="border: 1px solid black; padding: 2px;">*</td> </tr> <tr> <td>H'0C</td> <td style="border: 1px solid black; padding: 2px;">Place 3</td> <td style="border: 1px solid black; padding: 2px;">*</td> </tr> <tr> <td>H'10</td> <td style="border: 1px solid black; padding: 2px;">Place 0</td> <td style="border: 1px solid black; padding: 2px;">*</td> </tr> <tr> <td>H'14</td> <td style="border: 1px solid black; padding: 2px;">Place 1</td> <td style="border: 1px solid black; padding: 2px;">*</td> </tr> <tr> <td>H'18</td> <td style="border: 1px solid black; padding: 2px;">Place 2</td> <td style="border: 1px solid black; padding: 2px;">*</td> </tr> <tr> <td>H'1C</td> <td style="border: 1px solid black; padding: 2px;">Place 3</td> <td style="border: 1px solid black; padding: 2px;">*</td> </tr> <tr> <td>...</td> <td style="border: 1px solid black; padding: 2px;">...</td> <td style="border: 1px solid black; padding: 2px;">*</td> </tr> </table>		31	0	H'00	Place 0	*	H'04	Place 1	*	H'08	Place 2	*	H'0C	Place 3	*	H'10	Place 0	*	H'14	Place 1	*	H'18	Place 2	*	H'1C	Place 3	*	...	...	*
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H'1C	Place 3	*																													
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<p>BUSIF · Multichannel (4 channels) · 16 bits</p>	<p>External memory image</p> <table style="margin-left: 100px;"> <tr> <td></td> <td style="text-align: right;">31</td> <td style="text-align: left;">0</td> </tr> <tr> <td>H'00</td> <td style="border: 1px solid black; padding: 2px;">Place 0</td> <td style="border: 1px solid black; padding: 2px;">Place 1</td> </tr> <tr> <td>H'04</td> <td style="border: 1px solid black; padding: 2px;">Place 2</td> <td style="border: 1px solid black; padding: 2px;">Place 3</td> </tr> <tr> <td>H'08</td> <td style="border: 1px solid black; padding: 2px;">Place 0</td> <td style="border: 1px solid black; padding: 2px;">Place 1</td> </tr> <tr> <td>H'0C</td> <td style="border: 1px solid black; padding: 2px;">Place 2</td> <td style="border: 1px solid black; padding: 2px;">Place 3</td> </tr> <tr> <td>...</td> <td style="border: 1px solid black; padding: 2px;">...</td> <td style="border: 1px solid black; padding: 2px;">...</td> </tr> </table>		31	0	H'00	Place 0	Place 1	H'04	Place 2	Place 3	H'08	Place 0	Place 1	H'0C	Place 2	Place 3	...	...	...												
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H'08	Place 0	Place 1																													
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...	...	...																													

**Table 31.4 Definition of Data Places in Each Data Format (3)**

<p>BUSIF                  · Multichannel (6 channels)                  · 24 bits</p>	<p>External memory image</p> <table border="1" style="margin-left: 20px;"> <tr> <td></td> <td style="text-align: right;">31</td> <td style="text-align: left;">0</td> </tr> <tr> <td>H'00</td> <td>Place 0</td> <td>*</td> </tr> <tr> <td>H'04</td> <td>Place 1</td> <td>*</td> </tr> <tr> <td>H'08</td> <td>Place 2</td> <td>*</td> </tr> <tr> <td>H'0C</td> <td>Place 3</td> <td>*</td> </tr> <tr> <td>H'10</td> <td>Place 4</td> <td>*</td> </tr> <tr> <td>H'14</td> <td>Place 5</td> <td>*</td> </tr> <tr> <td>H'18</td> <td>Place 0</td> <td>*</td> </tr> <tr> <td>H'1C</td> <td>Place 1</td> <td>*</td> </tr> <tr> <td>...</td> <td>...</td> <td>*</td> </tr> </table>		31	0	H'00	Place 0	*	H'04	Place 1	*	H'08	Place 2	*	H'0C	Place 3	*	H'10	Place 4	*	H'14	Place 5	*	H'18	Place 0	*	H'1C	Place 1	*	...	...	*			
	31	0																																
H'00	Place 0	*																																
H'04	Place 1	*																																
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H'0C	Place 3	*																																
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H'1C	Place 1	*																																
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<p>BUSIF                  · Multichannel (6 channels)                  · 16 bits</p>	<p>External memory image</p> <table border="1" style="margin-left: 20px;"> <tr> <td></td> <td style="text-align: right;">31</td> <td style="text-align: left;">0</td> </tr> <tr> <td>H'00</td> <td>Place 0</td> <td>Place 1</td> </tr> <tr> <td>H'04</td> <td>Place 2</td> <td>Place 3</td> </tr> <tr> <td>H'08</td> <td>Place 4</td> <td>Place 5</td> </tr> <tr> <td>H'0C</td> <td>Place 0</td> <td>Place 1</td> </tr> <tr> <td>...</td> <td>...</td> <td>...</td> </tr> </table>		31	0	H'00	Place 0	Place 1	H'04	Place 2	Place 3	H'08	Place 4	Place 5	H'0C	Place 0	Place 1	...	...	...															
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<p>BUSIF                  · Multichannel (8 channels)                  · 24 bits</p>	<p>External memory image</p> <table border="1" style="margin-left: 20px;"> <tr> <td></td> <td style="text-align: right;">31</td> <td style="text-align: left;">0</td> </tr> <tr> <td>H'00</td> <td>Place 0</td> <td>*</td> </tr> <tr> <td>H'04</td> <td>Place 1</td> <td>*</td> </tr> <tr> <td>H'08</td> <td>Place 2</td> <td>*</td> </tr> <tr> <td>H'0C</td> <td>Place 3</td> <td>*</td> </tr> <tr> <td>H'10</td> <td>Place 4</td> <td>*</td> </tr> <tr> <td>H'14</td> <td>Place 5</td> <td>*</td> </tr> <tr> <td>H'18</td> <td>Place 6</td> <td>*</td> </tr> <tr> <td>H'1C</td> <td>Place 7</td> <td>*</td> </tr> <tr> <td>H'20</td> <td>Place 0</td> <td>*</td> </tr> <tr> <td>...</td> <td>...</td> <td>*</td> </tr> </table>		31	0	H'00	Place 0	*	H'04	Place 1	*	H'08	Place 2	*	H'0C	Place 3	*	H'10	Place 4	*	H'14	Place 5	*	H'18	Place 6	*	H'1C	Place 7	*	H'20	Place 0	*	...	...	*
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<p>BUSIF                  · Multichannel (8 channels)                  · 16 bits</p>	<p>External memory image</p> <table border="1" style="margin-left: 20px;"> <tr> <td></td> <td style="text-align: right;">31</td> <td style="text-align: left;">0</td> </tr> <tr> <td>H'00</td> <td>Place 0</td> <td>Place 1</td> </tr> <tr> <td>H'04</td> <td>Place 2</td> <td>Place 3</td> </tr> <tr> <td>H'08</td> <td>Place 4</td> <td>Place 5</td> </tr> <tr> <td>H'0C</td> <td>Place 6</td> <td>Place 7</td> </tr> <tr> <td>H'10</td> <td>Place 0</td> <td>Place 1</td> </tr> <tr> <td>...</td> <td>...</td> <td>...</td> </tr> </table>		31	0	H'00	Place 0	Place 1	H'04	Place 2	Place 3	H'08	Place 4	Place 5	H'0C	Place 6	Place 7	H'10	Place 0	Place 1	...	...	...												
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H'08	Place 4	Place 5																																
H'0C	Place 6	Place 7																																
H'10	Place 0	Place 1																																
...	...	...																																

### 31.1.6 Transfer Flow

When data transfer is performed between the audio modules which are used in a set of audio routing, use the Audio-DMAC and Audio-DMAC-Peripheral-Peripheral to perform settings in accord with the transfer flow shown in Figure 31.4.

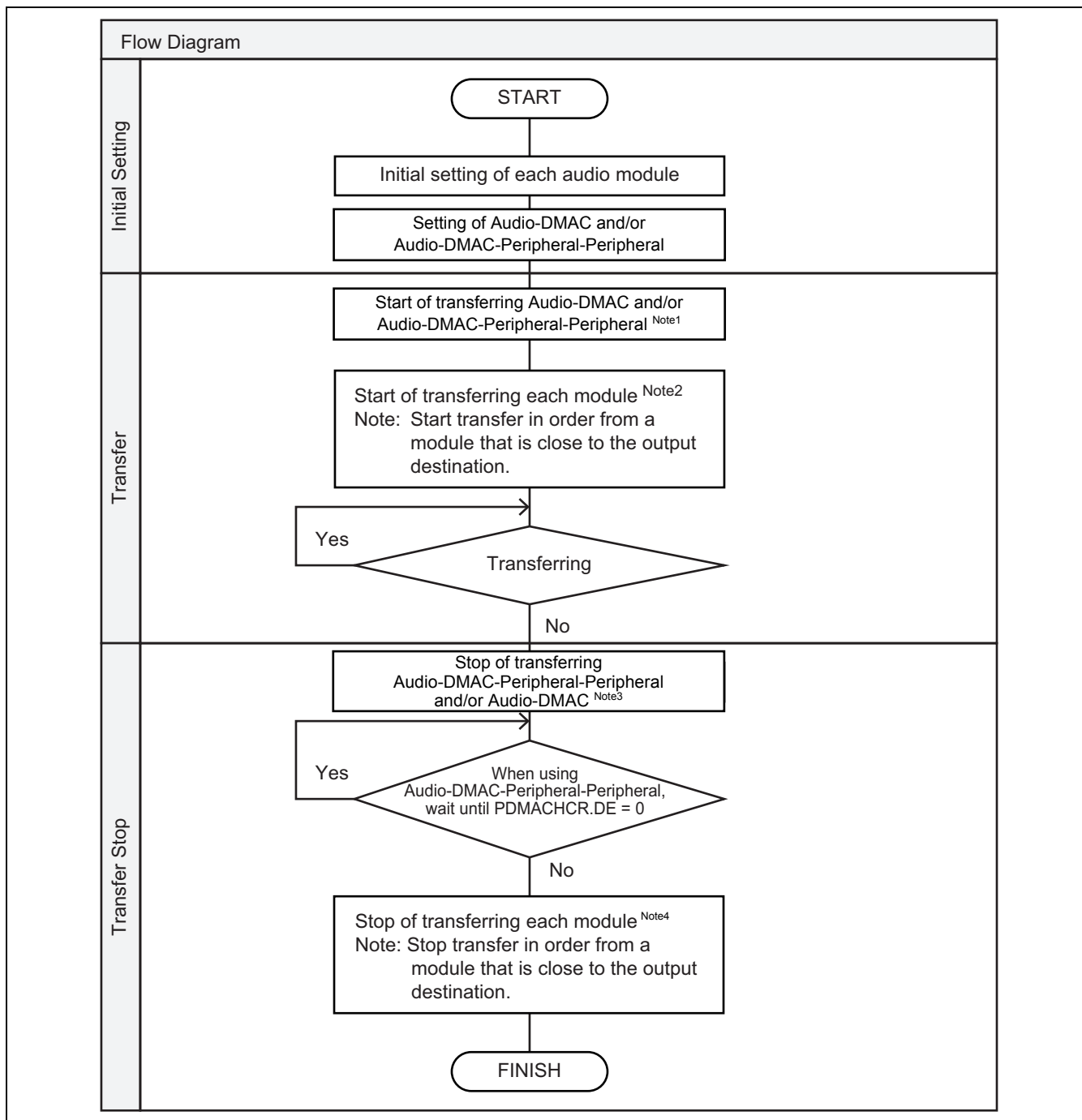


Figure 31.4 Transfer Flow

Notes: 1. For Audio-DMAC, set DMACHCR.DE.

For Audio-DMAC-Peripheral-Peripheral, set PDMACHCR.DE.

Set up registers except the above in "Setting of Audio-DMAC and/or Audio-DMAC-Peripheral-Peripheral".

2. For SSI (except for the case when TDM split mode, SSI independent transfer, SSI0, SSI1, SSI2, or SSI9, and SSI3 or SSI4 are used at the same time), when transmitting (from the external device to SSI), set

SSIq/r\_CONTROL.start after setting SSICR.en/dmen. When receiving (from SSI to the external device), set SSICR.en/dmen after setting SSIq/r\_CONTROL.start.

For SSI (In the case of TDM split mode), regardless of transmission and reception, set SSIq/r\_CONTROL.start after setting SSICR.en/dmen.

For SSI (In the case of SSI independent transfer), set SSICR.en/dmen.

For SSI (When using SSI0, SSI1, SSI2, or SSI9 and SSI3 or SSI4 at the same time), when transmitting (from the external device to SSI) set SSIq/r\_CONTROL.start after setting SSI\_CONTROL. When receiving (from SSI to the external device), set SSI\_CONTROL after setting SSIq/r\_CONTROL.start. (Set SSICR.dmen at the time of the initial setting.)

For SCU, Set SRCm\_CONTROL and CMDn\_CONTROL.

Set up registers except the above in "Initial setting of each audio module".

3. For Audio-DMAC-Peripheral-Peripheral, clear PDMACHCR.DE. (mandatory)  
For Audio-DMAC, clear DMACHCR.DE. Clear processing of Audio-DMAC can be cleared anywhere in a TransferStop sequence.
4. For SSI (except for the case when TDM split mode, SSI independent transfer, SSI0, SSI1, SSI2, or SSI9, and SSI3 or SSI4 are used at the same time), when transmitting (from the external device to SSI), clear SSIq/r\_CONTROL.start after clearing SSICR.en/dmen. When receiving (from SSI to the external device), clear SSICR.en/dmen after clearing SSIq/r\_CONTROL.start.

For SSI (In the case of TDM split mode), regardless of transmission and reception, clear all SSIq/r\_CONTROL.start of the relevant channels to clear SSICR.en/dmen.

For SSI (In the case of SSI independent transfer), clear SSICR.en/dmen.

For SSI (When using SSI0, SSI1, SSI2, or SSI9 and SSI3 or SSI4 at the same time), when transmitting (from the external device to SSI) clear SSIq/r\_CONTROL.start after clearing SSICR.dmen of each module and SSI\_CONTROL. When receiving (from SSI to the external device), clear SSICR.dmen of each module and SSI\_CONTROL after clearing SSIq/r\_CONTROL.start.

For SCU, Clear SRCm\_CONTROL and CMDn\_CONTROL.



### 31.1.7 Module Standby Function

For the register settings to make a transition to or from module standby mode, refer to section 7A, Module Standby and Software Reset.

#### (1) Transition to Module Standby Mode

To make a transition to module standby mode by the module standby function, refer to the following transition procedure for each module.

##### (a) SSIU/SSI

1. Check the following registers' settings.

[SSIU]

- All bits in the SSIq control register (SSIq\_CONTROL) (q = 0-0, 1-0, 2-0, or 9-0) are cleared to 0 (data transfer stopped).
- All bits in the SSIr control register (SSIr\_CONTROL) (r = 3 to 8) are cleared to 0 (data transfer stopped).
- All bits in the SSIq interrupt enable register (SSIq\_INT\_ENABLE\_MAIN) (q = 0-0, 1-0, 2-0, or 9-0) are cleared to 0 (interrupt disabled).
- All bits in the SSIr interrupt enable register (SSIr\_INT\_ENABLE\_MAIN) (r = 3 to 8) are cleared to 0 (interrupt disabled).
- All bits in the SSI control register (SSI\_CONTROL) are cleared to 0 (data transfer stopped)

[SSI]

- The DMEN and EN bits in the control register (SSICRn) (n = 0 to 9) are cleared to 0 (disabled).
- The IDST bit in the status register (SSISRn) (n = 0 to 9) is set to 1.
- The CONT bit in the WS mode register (SSIWSRn) (n = 0 to 9) is cleared to 0 (disabled).

2. Set the MSTP1005 to MSTP1015 bits in the module stop control register (SMSTPCR10)

Note: The above bits should be set while the module operation has been completed and is placed in the idle state in which the module cannot be activated by external pins or other modules.

##### (b) SCU

1. Check the following registers' settings.

- All bits in the SRCm control register (SRCm\_CONTROL) (m = 0 to 9 / (1 to 6)\*) are cleared to 0 (data transfer stopped).
- All bits in the CMDn control register (CMDn\_CONTROL) (n = 0, 1) are cleared to 0 (data transfer stopped).
- All bits in the SRCm interrupt enable register 0 (SRCm\_INT\_ENABLE0) (m = 0 to 5 / (1 to 5)\*) are cleared to 0 (interrupt disabled).
- All bits in the SRCn interrupt enable register 0 (SRCn\_INT\_ENABLE0) (n = 6 to 9 / 6\*) are cleared to 0 (interrupt disabled).

2. Set the MSTP1017 to MSTP1031 bits (MSTP1017 to MSTP1021 and MSTP1025 to MSTP1030 bits)\* in the module stop control register (SMSTPCR10)

Notes: The above bits should be set while the module operation has been completed and is placed in the idle state in which the module cannot be activated by external pins or other modules.

\* Applicable to the RZ/G1E

**(2) Releasing and Restarting from Module Standby Mode**

After the transition to module standby mode, modules can be released from module standby mode by a power-on reset or the appropriate procedure from the list below.

**(a) SSIU/SSI**

1. Supply the clock signal to the ADG and SSIU/SSI modules.
2. Clear the MSTP1005 to MSTP1015 bits in the module stop control register (SMSTPCR10).

**(b) SCU**

1. Clear the MSTP1017 to MSTP1031 (MSTP1017 to MSTP1021 and MSTP1025 to MSTP1030 bits)\* bits in the module stop control register (SMSTPCR10).

Note: \* Applicable to the RZ/G1E

## 31.2 Usage Notes

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

### 31.2.1 Notes on Route Switching and Setting Changes

When switching the transfer route, stop the current transfer, specify the new transfer route, and then start transfer. Also, when changing the quantization bit count or the formats, once stop transfer, and then start transfer again after resetting. If this procedure is not followed, correct operation is not guaranteed.

### 31.2.2 Use of SSI3 and SSI4

Table 31.5 shows the combinations of SSI3 and SSI4 usage and register settings.

**Table 31.5 Combinations of SSI3 and SSI4 Usage and Register Settings**

	SSI_MODE1 Register Settings		Bit Used to Control Start or Stop Operation
	ssi34_sync	ssi4_pin	
Operating SSI3 and SSI4 independently	0	00	SSICRn.EN (n = 3 and 4)
Operating SSI4 with the SCK and WS signals of SSI3 being <u>shared by</u> both SSI3 and SSI4	0	01 or 10	SSICRn.EN (n = 3 and 4)
<u>Synchronizing</u> serial data of SSI3 and SSI4	1	01 or 10	SSI_CONTROL.ssi34

### 31.2.3 Notes on CMD Block Usage

When a single sound source is split into two routes, CMD0 and CMD1, and output to SSI3 and SSI4, use the settings for "Synchronizing serial data of SSI3 and SSI4" in Table 31.5, Combinations of SSI3 and SSI4 Usage and Register Settings. The quantization bit count and sampling frequency settings should be the same between SSI3 and SSI4. Note that only the stereo format can be specified for SSI3 and SSI4. For example, it is not possible to output TDM-format data from SSI3 and stereo-format data from SSI4. The reverse combination is not possible either (stereo-format data from SSI3 or TDM-format data from SSI4).

### 31.2.4 Note when SSI0, SSI1, and SSI2, or SSI0, SSI1, SSI2, and SSI9 are Used for Single-Source Audio Data

When SSI0, SSI1, and SSI2, or SSI0, SSI1, SSI2, and SSI9 are used for single-source audio data, specifying eight-bit quantization and six- or eight-channel operation at the same time is not possible.

### 31.2.5 Note on Transfer

When an underflow or an overflow occurs in any audio module, stop the transfer.

### 31.2.6 Note on Usage of the SCU Module

Before starting data transfer, the input and output data timing signals must be input to the SCU module.

Otherwise, the SCU does not operate correctly.

Set SSIWSRn.CONT to 1 when the SSI module operates in master mode and the WS signal is used as an input or output timing signal for the SRC.

## 32. Serial Sound Interface Unit (SSIU)

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

### 32.1 Overview

The SSIU, incorporating ten SSI modules, allows independent operation of SSI modules, operation of multiple SSI modules sharing the same serial clock, and connection or split of multichannel data.

Note: Configure the system so that connected external devices can operate on the same clock source.

#### 32.1.1 Features

- Incorporates ten SSI modules.
- Supports 6 channels/1 sound source with three SSI modules (SSI0, SSI1, and SSI2).
- Supports 8 channels/1 sound source with four SSI modules (SSI0, SSI1, SSI2, and SSI9).
- Operation of multiple modules on the same serial clock (SSI0/SSI1/SSI2/SSI9, SSI3/SSI4, or SSI7/SSI8).
- TDM format (normal) corresponds to 4-, 6-, or 8-channel data.
- Handles 8-channel data on the serial bus and 6-channel data in the RZ/G (TDM extend mode).
- Handles 6-channel data on the serial bus and 8-channel data in the RZ/G (TDM extend mode).
- Connects monaural or stereo data to output TDM format data (TDM split mode).
- Splits TDM format input data into monaural or stereo data (TDM split mode).
- The frequency range of SCK signal is from 297.3 kHz to 12.5MHz at master mode, and from 297.3 kHz to 15.1 MHz at slave mode.

### 32.1.2 Block Diagram

Figures 32.1 to 32.2 show the SSIU block diagrams.

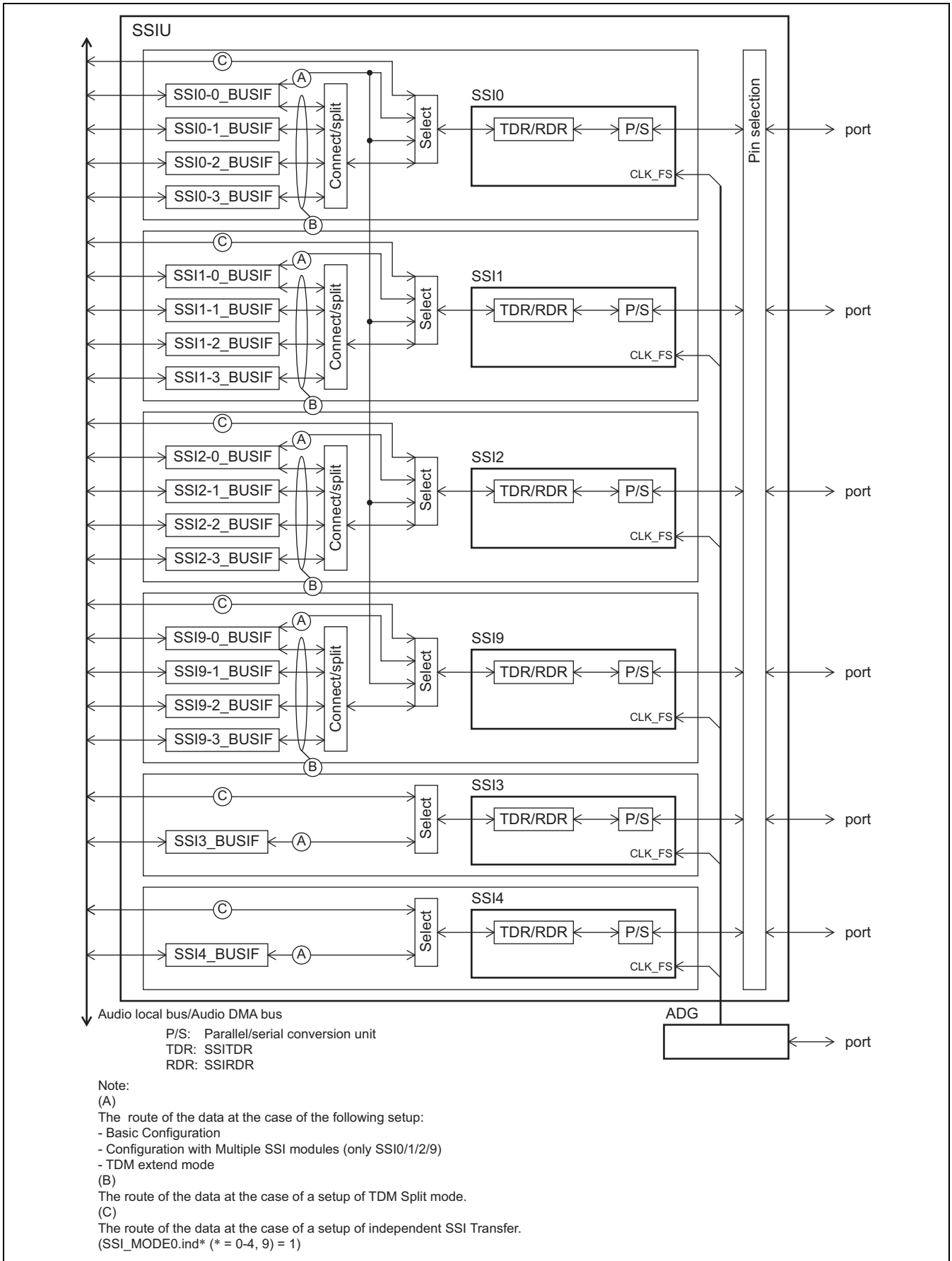


Figure 32.1 Block Diagram of SSIU (SSI0, SSI1, SSI2, SSI3, SSI4, and SSI9)

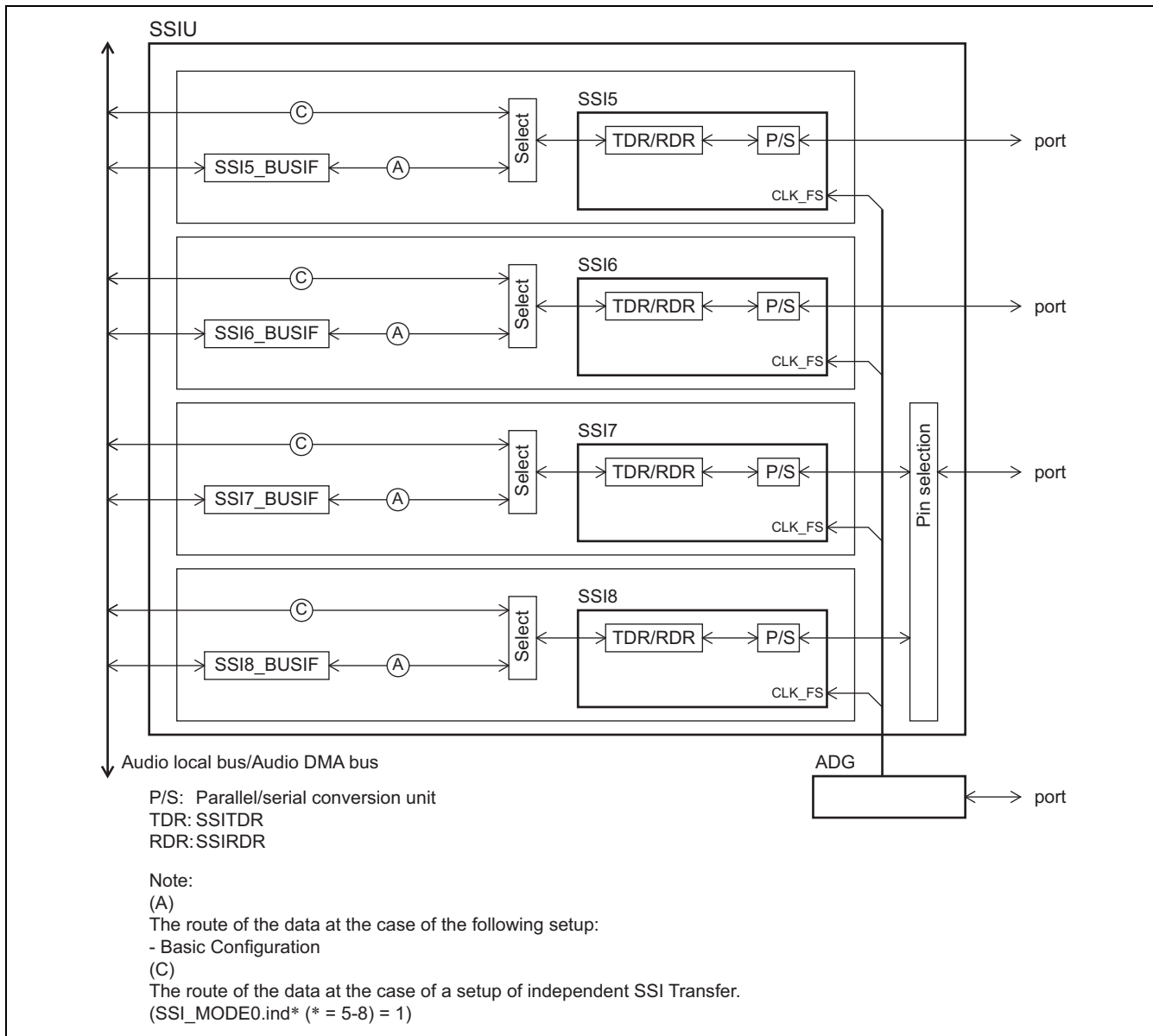


Figure 32.2 Block Diagram of SSIU (SSI5, SSI6, SSI7, and SSI8)

### 32.1.3 Input/Output Pins

Table 32.1 shows the pin configuration.

**Table 32.1 Pin Configuration**

Name	Pin Name	I/O	Function	RZ/G Series Products			
				RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Serial clock pin for SSI0, SSI1, SSI2, SSI3 and SSI9	SSI_SCK0129 (SSI_SCK01239)	I/O	Serial clock (SSI0 only or combination of SSI0, SSI1, SSI2, SSI3, and SSI9)	√	√	√	√
Word select pin for SSI0, SSI1, SSI2, SSI3 and SSI9	SSI_WS0129 (SSI_WS01239)	I/O	Word select (SSI0 only or combination of SSI0, SSI1, SSI2, SSI3, and SSI9)	√	√	√	√
Serial data pin for SSI0	SSI_SDATA0	I/O	Serial data	√	√	√	√
Serial clock pin for SSI1	SSI_SCK1	I/O	Serial clock	√	√	√	√
Word select pin for SSI1	SSI_WS1	I/O	Word select	√	√	√	√
Serial data pin for SSI1	SSI_SDATA1	I/O	Serial data	√	√	√	√
Serial clock pin for SSI2	SSI_SCK2	I/O	Serial clock	√	√	√	√
Word select pin for SSI2	SSI_WS2	I/O	Word select	√	√	√	√
Serial data pin for SSI2	SSI_SDATA2	I/O	Serial data	√	√	√	√
Serial clock pin for SSI3, SSI4 and SSI9	SSI_SCK34 (SSI_SCK349)	I/O	Serial clock (SSI3 only, common to SSI3 and SSI4, or combination of SSI3, SSI4, and SSI9)	√	√	√	√
Word select pin for SSI3, SSI4 and SSI9	SSI_WS34 (SSI_WS349)	I/O	Word select (SSI3 only, common to SSI3 and SSI4, or combination of SSI3, SSI4, and SSI9)	√	√	√	√
Serial data pin for SSI3	SSI_SDATA3	I/O	Serial data	√	√	√	√
Serial clock pin for SSI4	SSI_SCK4	I/O	Serial clock	√	√	√	√
Word select pin for SSI4	SSI_WS4	I/O	Word select	√	√	√	√
Serial data pin for SSI4	SSI_SDATA4	I/O	Serial data	√	√	√	√
Serial clock pin for SSI5	SSI_SCK5	I/O	Serial clock	√	√	√	√
Word select pin for SSI5	SSI_WS5	I/O	Word select	√	√	√	√
Serial data pin for SSI5	SSI_SDATA5	I/O	Serial data	√	√	√	√
Serial clock pin for SSI6	SSI_SCK6	I/O	Serial clock	√	√	√	√
Word select pin for SSI6	SSI_WS6	I/O	Word select	√	√	√	√
Serial data pin for SSI6	SSI_SDATA6	I/O	Serial data	√	√	√	√
Serial clock pin for SSI7 and SSI8	SSI_SCK78	I/O	Serial clock (common to SSI7 and SSI8)	√	√	√	√
Word select pin for SSI7 and SSI8	SSI_WS78	I/O	Word select (common to SSI7 and SSI8)	√	√	√	√
Serial data pin for SSI7	SSI_SDATA7	I/O	Serial data	√	√	√	√
Serial data pin for SSI8	SSI_SDATA8	I/O	Serial data	√	√	√	√
Serial clock pin for SSI9	SSI_SCK9	I/O	Serial clock	√	√	√	√



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**RZ/G Series  
Products**


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Name	Pin Name	I/O	Function	RZ/G Series Products			
				RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Word select pin for SSI9	SSI_WS9	I/O	Word select	√	√	√	√
Serial data pin for SSI9	SSI_SDATA9	I/O	Serial data	√	√	√	√

Note: Although each SSI is multiplexed on multiple LSI pins, the combinations of pins in use must be from the same group. For Example, the use of combinations such as SSI\_SCK78, SSI\_WS78, and SSI\_SDATA8\_B is prohibited. Please refer to section 5, Pin Function Controller (PFC) for details.

### 32.1.4 Register Configuration

Table 32.2 shows the register configuration. Do not write to any addresses other than listed below. Operations cannot be guaranteed if writing is attempted. Values read from addresses other than those listed below are undefined. Access the register as a longword (32 bits). Operation cannot be guaranteed if the register is not accessed as a longword.

**Table 32.2 Register Configuration**

Name	Abbreviation	R/W	Address	Initial Value	Access Size	RZ/G Series Products			
						RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
SSI0_0 BUSIF mode register	SSI0-0_BUSIF_MODE	R/W	H'EC54 0000	H'00000001	32	√	√	√	√
SSI0_0 BUSIF audio information register	SSI0-0_BUSIF_ADINR	R/W	H'EC54 0004	H'00000000	32	√	√	√	√
SSI0_0 BUSIF data align register	SSI0-0_BUSIF_DALIGN	R/W	H'EC54 0008	H'76543210	32	√	√	√	√
SSI0_0 mode register	SSI0-0_MODE	R/W	H'EC54 000C	H'00000000	32	√	√	√	√
SSI0_0 control register	SSI0-0_CONTROL	R/W	H'EC54 0010	H'00000000	32	√	√	√	√
SSI0_0 status register	SSI0-0_STATUS	R	H'EC54 0014	H'00000000	32	√	√	√	√
SSI0_0 interrupt enable register	SSI0-0_INT_ENABLE_MAIN	R/W	H'EC54 0018	H'00000000	32	√	√	√	√
SSI0_1 BUSIF mode register	SSI0-1_BUSIF_MODE	R/W	H'EC54 0020	H'00000001	32	√	√	√	√
SSI0_1 BUSIF audio information register	SSI0-1_BUSIF_ADINR	R/W	H'EC54 0024	H'00000000	32	√	√	√	√
SSI0_1 BUSIF data align register	SSI0-1_BUSIF_DALIGN	R/W	H'EC54 0028	H'00000010	32	√	√	√	√
SSI0_2 BUSIF mode register	SSI0-2_BUSIF_MODE	R/W	H'EC54 0040	H'00000001	32	√	√	√	√
SSI0_2 BUSIF audio information register	SSI0-2_BUSIF_ADINR	R/W	H'EC54 0044	H'00000000	32	√	√	√	√
SSI0_2 BUSIF data align register	SSI0-2_BUSIF_DALIGN	R/W	H'EC54 0048	H'00000010	32	√	√	√	√
SSI0_3 BUSIF mode register	SSI0-3_BUSIF_MODE	R/W	H'EC54 0060	H'00000001	32	√	√	√	√
SSI0_3 BUSIF audio information register	SSI0-3_BUSIF_ADINR	R/W	H'EC54 0064	H'00000000	32	√	√	√	√
SSI0_3 BUSIF data align register	SSI0-3_BUSIF_DALIGN	R/W	H'EC54 0068	H'00000010	32	√	√	√	√
SSI1_0 BUSIF mode register	SSI1-0_BUSIF_MODE	R/W	H'EC54 0080	H'00000001	32	√	√	√	√
SSI1_0 BUSIF audio information register	SSI1-0_BUSIF_ADINR	R/W	H'EC54 0084	H'00000000	32	√	√	√	√
SSI1_0 BUSIF data align register	SSI1-0_BUSIF_DALIGN	R/W	H'EC54 0088	H'76543210	32	√	√	√	√
SSI1_0 mode register	SSI1-0_MODE	R/W	H'EC54 008C	H'00000000	32	√	√	√	√
SSI1_0 control register	SSI1-0_CONTROL	R/W	H'EC54 0090	H'00000000	32	√	√	√	√
SSI1_0 status register	SSI1-0_STATUS	R	H'EC54 0094	H'00000000	32	√	√	√	√

Name	Abbreviation	R/W	Address	Initial Value	Access Size	RZ/G Series Products			
						RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
SSI1_0 interrupt enable register	SSI1-0_INT_ENABLE_MAIN	R/W	H'EC54 0098	H'00000000	32	√	√	√	√
SSI1_1 BUSIF mode register	SSI1-1_BUSIF_MODE	R/W	H'EC54 00A0	H'00000001	32	√	√	√	√
SSI1_1 BUSIF audio information register	SSI1-1_BUSIF_ADINR	R/W	H'EC54 00A4	H'00000000	32	√	√	√	√
SSI1_1 BUSIF data align register	SSI1-1_BUSIF_DALIGN	R/W	H'EC54 00A8	H'00000010	32	√	√	√	√
SSI1_2 BUSIF mode register	SSI1-2_BUSIF_MODE	R/W	H'EC54 00C0	H'00000001	32	√	√	√	√
SSI1_2 BUSIF audio information register	SSI1-2_BUSIF_ADINR	R/W	H'EC54 00C4	H'00000000	32	√	√	√	√
SSI1_2 BUSIF data align register	SSI1-2_BUSIF_DALIGN	R/W	H'EC54 00C8	H'00000010	32	√	√	√	√
SSI1_3 BUSIF mode register	SSI1-3_BUSIF_MODE	R/W	H'EC54 00E0	H'00000001	32	√	√	√	√
SSI1_3 BUSIF audio information register	SSI1-3_BUSIF_ADINR	R/W	H'EC54 00E4	H'00000000	32	√	√	√	√
SSI1_3 BUSIF data align register	SSI1-3_BUSIF_DALIGN	R/W	H'EC54 00E8	H'00000010	32	√	√	√	√
SSI2_0 BUSIF mode register	SSI2-0_BUSIF_MODE	R/W	H'EC54 0100	H'00000001	32	√	√	√	√
SSI2_0 BUSIF audio information register	SSI2-0_BUSIF_ADINR	R/W	H'EC54 0104	H'00000000	32	√	√	√	√
SSI2_0 BUSIF data align register	SSI2-0_BUSIF_DALIGN	R/W	H'EC54 0108	H'76543210	32	√	√	√	√
SSI2_0 mode register	SSI2-0_MODE	R/W	H'EC54 010C	H'00000000	32	√	√	√	√
SSI2_0 control register	SSI2-0_CONTROL	R/W	H'EC54 0110	H'00000000	32	√	√	√	√
SSI2_0 status register	SSI2-0_STATUS	R	H'EC54 0114	H'00000000	32	√	√	√	√
SSI2_0 interrupt enable register	SSI2-0_INT_ENABLE_MAIN	R/W	H'EC54 0118	H'00000000	32	√	√	√	√
SSI2_1 BUSIF mode register	SSI2-1_BUSIF_MODE	R/W	H'EC54 0120	H'00000001	32	√	√	√	√
SSI2_1 BUSIF audio information register	SSI2-1_BUSIF_ADINR	R/W	H'EC54 0124	H'00000000	32	√	√	√	√
SSI2_1 BUSIF data align register	SSI2-1_BUSIF_DALIGN	R/W	H'EC54 0128	H'00000010	32	√	√	√	√
SSI2_2 BUSIF mode register	SSI2-2_BUSIF_MODE	R/W	H'EC54 0140	H'00000001	32	√	√	√	√
SSI2_2 BUSIF audio information register	SSI2-2_BUSIF_ADINR	R/W	H'EC54 0144	H'00000000	32	√	√	√	√
SSI2_2 BUSIF data align register	SSI2-2_BUSIF_DALIGN	R/W	H'EC54 0148	H'00000010	32	√	√	√	√
SSI2_3 BUSIF mode register	SSI2-3_BUSIF_MODE	R/W	H'EC54 0160	H'00000001	32	√	√	√	√

Name	Abbreviation	R/W	Address	Initial Value	Access Size	RZ/G Series Products			
						RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
SSI2_3 BUSIF audio information register	SSI2-3_BUSIF_ADINR	R/W	H'EC54 0164	H'00000000	32	√	√	√	√
SSI2_3 BUSIF data align register	SSI2-3_BUSIF_DALIGN	R/W	H'EC54 0168	H'00000010	32	√	√	√	√
SSI3 BUSIF mode register	SSI3_BUSIF_MODE	R/W	H'EC54 0180	H'00000001	32	√	√	√	√
SSI3 BUSIF audio information register	SSI3_BUSIF_ADINR	R/W	H'EC54 0184	H'00000000	32	√	√	√	√
SSI3 BUSIF data align register	SSI3_BUSIF_DALIGN	R/W	H'EC54 0188	H'76543210	32	√	√	√	√
SSI3 mode register	SSI3_MODE	R/W	H'EC54 018C	H'00000000	32	√	√	√	√
SSI3 control register	SSI3_CONTROL	R/W	H'EC54 0190	H'00000000	32	√	√	√	√
SSI3 status register	SSI3_STATUS	R	H'EC54 0194	H'00000000	32	√	√	√	√
SSI3 interrupt enable register	SSI3_INT_ENABLE_MAIN	R/W	H'EC54 0198	Undefined	32	√	√	√	√
SSI4 BUSIF mode register	SSI4_BUSIF_MODE	R/W	H'EC54 0200	H'00000001	32	√	√	√	√
SSI4 BUSIF audio information register	SSI4_BUSIF_ADINR	R/W	H'EC54 0204	H'00000000	32	√	√	√	√
SSI4 BUSIF data align register	SSI4_BUSIF_DALIGN	R/W	H'EC54 0208	H'76543210	32	√	√	√	√
SSI4 mode register	SSI4_MODE	R/W	H'EC54 020C	H'00000000	32	√	√	√	√
SSI4 control register	SSI4_CONTROL	R/W	H'EC54 0210	H'00000000	32	√	√	√	√
SSI4 status register	SSI4_STATUS	R	H'EC54 0214	H'00000000	32	√	√	√	√
SSI4 interrupt enable register	SSI4_INT_ENABLE_MAIN	R/W	H'EC54 0218	Undefined	32	√	√	√	√
SSI5 BUSIF mode register	SSI5_BUSIF_MODE	R/W	H'EC54 0280	H'00000001	32	√	√	√	√
SSI5 BUSIF audio information register	SSI5_BUSIF_ADINR	R/W	H'EC54 0284	H'00000000	32	√	√	√	√
SSI5 BUSIF data align register	SSI5_BUSIF_DALIGN	R/W	H'EC54 0288	H'76543210	32	√	√	√	√
SSI5 control register	SSI5_CONTROL	R/W	H'EC54 0290	H'00000000	32	√	√	√	√
SSI5 status register	SSI5_STATUS	R	H'EC54 0294	H'00000000	32	√	√	√	√
SSI5 interrupt enable register	SSI5_INT_ENABLE_MAIN	R/W	H'EC54 0298	Undefined	32	√	√	√	√
SSI6 BUSIF mode register	SSI6_BUSIF_MODE	R/W	H'EC54 0300	H'00000001	32	√	√	√	√
SSI6 BUSIF audio information register	SSI6_BUSIF_ADINR	R/W	H'EC54 0304	H'00000000	32	√	√	√	√
SSI6 BUSIF data align register	SSI6_BUSIF_DALIGN	R/W	H'EC54 0308	H'76543210	32	√	√	√	√
SSI6 control register	SSI6_CONTROL	R/W	H'EC54 0310	H'00000000	32	√	√	√	√
SSI6 status register	SSI6_STATUS	R	H'EC54 0314	H'00000000	32	√	√	√	√

Name	Abbreviation	R/W	Address	Initial Value	Access Size	RZ/G Series Products			
						RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
SSI6 interrupt enable register	SSI6_INT_ENABLE_MAIN	R/W	H'EC54 0318	Undefined	32	√	√	√	√
SSI7 BUSIF mode register	SSI7_BUSIF_MODE	R/W	H'EC54 0380	H'00000001	32	√	√	√	√
SSI7 BUSIF audio information register	SSI7_BUSIF_ADINR	R/W	H'EC54 0384	H'00000000	32	√	√	√	√
SSI7 BUSIF data align register	SSI7_BUSIF_DALIGN	R/W	H'EC54 0388	H'76543210	32	√	√	√	√
SSI7 control register	SSI7_CONTROL	R/W	H'EC54 0390	H'00000000	32	√	√	√	√
SSI7 status register	SSI7_STATUS	R	H'EC54 0394	H'00000000	32	√	√	√	√
SSI7 interrupt enable register	SSI7_INT_ENABLE_MAIN	R/W	H'EC54 0398	Undefined	32	√	√	√	√
SSI8 BUSIF mode register	SSI8_BUSIF_MODE	R/W	H'EC54 0400	H'00000001	32	√	√	√	√
SSI8 BUSIF audio information register	SSI8_BUSIF_ADINR	R/W	H'EC54 0404	H'00000000	32	√	√	√	√
SSI8 BUSIF data align register	SSI8_BUSIF_DALIGN	R/W	H'EC54 0408	H'76543210	32	√	√	√	√
SSI8 control register	SSI8_CONTROL	R/W	H'EC54 0410	H'00000000	32	√	√	√	√
SSI8 status register	SSI8_STATUS	R	H'EC54 0414	H'00000000	32	√	√	√	√
SSI8 interrupt enable register	SSI8_INT_ENABLE_MAIN	R/W	H'EC54 0418	Undefined	32	√	√	√	√
SSI9_0 BUSIF mode register	SSI9-0_BUSIF_MODE	R/W	H'EC54 0480	H'00000001	32	√	√	√	√
SSI9_0 BUSIF audio information register	SSI9-0_BUSIF_ADINR	R/W	H'EC54 0484	H'00000000	32	√	√	√	√
SSI9_0 BUSIF data align register	SSI9-0_BUSIF_DALIGN	R/W	H'EC54 0488	H'76543210	32	√	√	√	√
SSI9_0 mode register	SSI9-0_MODE	R/W	H'EC54 048C	H'00000000	32	√	√	√	√
SSI9_0 control register	SSI9-0_CONTROL	R/W	H'EC54 0490	H'00000000	32	√	√	√	√
SSI9_0 status register	SSI9-0_STATUS	R	H'EC54 0494	H'00000000	32	√	√	√	√
SSI9_0 interrupt enable register	SSI9-0_INT_ENABLE_MAIN	R/W	H'EC54 0498	H'00000000	32	√	√	√	√
SSI9_1 BUSIF mode register	SSI9-1_BUSIF_MODE	R/W	H'EC54 04A0	H'00000001	32	√	√	√	√
SSI9_1 BUSIF audio information register	SSI9-1_BUSIF_ADINR	R/W	H'EC54 04A4	H'00000000	32	√	√	√	√
SSI9_1 BUSIF data align register	SSI9-1_BUSIF_DALIGN	R/W	H'EC54 04A8	H'00000010	32	√	√	√	√
SSI9_2 BUSIF mode register	SSI9-2_BUSIF_MODE	R/W	H'EC54 04C0	H'00000001	32	√	√	√	√
SSI9_2 BUSIF audio information register	SSI9-2_BUSIF_ADINR	R/W	H'EC54 04C4	H'00000000	32	√	√	√	√
SSI9_2 BUSIF data align register	SSI9-2_BUSIF_DALIGN	R/W	H'EC54 04C8	H'00000010	32	√	√	√	√

Name	Abbreviation	R/W	Address	Initial Value	Access Size	RZ/G Series Products			
						RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
SSI9_3 BUSIF mode register	SSI9-3_BUSIF_MODE	R/W	H'EC54 04E0	H'00000001	32	√	√	√	√
SSI9_3 BUSIF audio information register	SSI9-3_BUSIF_ADINR	R/W	H'EC54 04E4	H'00000000	32	√	√	√	√
SSI9_3 BUSIF data align register	SSI9-3_BUSIF_DALIGN	R/W	H'EC54 04E8	H'00000010	32	√	√	√	√
SSI mode register 0	SSI_MODE0	R/W	H'EC54 0800	H'00000000	32	√	√	√	√
SSI mode register 1	SSI_MODE1	R/W	H'EC54 0804	H'00000000	32	√	√	√	√
SSI mode register 2	SSI_MODE2	R/W	H'EC54 0808	H'00000000	32	√	√	√	√
SSI mode register 3	SSI_MODE3	R/W	H'EC54 080C	H'00000000	32	√	√	√	√
SSI control register	SSI_CONTROL	R/W	H'EC54 0810	H'00000000	32	√	√	√	√
SSI system status register 0	SSI_SYSTEM_STATUS0	R/WC1	H'EC54 0840	H'00000000	32	√	√	√	√
SSI system status register 1	SSI_SYSTEM_STATUS1	R/WC1	H'EC54 0844	H'00000000	32	√	√	√	√
SSI system status register 2	SSI_SYSTEM_STATUS2	R/WC1	H'EC54 0848	H'00000000	32	√	√	√	√
SSI system status register 3	SSI_SYSTEM_STATUS3	R/WC1	H'EC54 084C	H'00000000	32	√	√	√	√
SSI system interrupt enable register 0	SSI_SYSTEM_INT_ENABLE0	R/W	H'EC54 0850	H'00000000	32	√	√	√	√
SSI system interrupt enable register 1	SSI_SYSTEM_INT_ENABLE1	R/W	H'EC54 0854	H'00000000	32	√	√	√	√
SSI system interrupt enable register 2	SSI_SYSTEM_INT_ENABLE2	R/W	H'EC54 0858	H'00000000	32	√	√	√	√
SSI system interrupt enable register 3	SSI_SYSTEM_INT_ENABLE3	R/W	H'EC54 085C	H'00000000	32	√	√	√	√
-BUSIF									
SSI0-0_BUSIF data register	SSI0-0_BUSIF	R/W	H'EC10 0000/ H'EC40 0000*	H'00000000	32	√	√	√	√
SSI0-1_BUSIF data register	SSI0-1_BUSIF	R/W	H'EC10 0400/ H'EC40 0400*	H'00000000	32	√	√	√	√
SSI0-2_BUSIF data register	SSI0-2_BUSIF	R/W	H'EC10 0800/ H'EC40 0800*	H'00000000	32	√	√	√	√
SSI0-3_BUSIF data register	SSI0-3_BUSIF	R/W	H'EC10 0C00/ H'EC40 0C00*	H'00000000	32	√	√	√	√
SSI1-0_BUSIF data register	SSI1-0_BUSIF	R/W	H'EC10 1000/ H'EC40 1000*	H'00000000	32	√	√	√	√
SSI1-1_BUSIF data register	SSI1-1_BUSIF	R/W	H'EC10 1400/ H'EC40 1400*	H'00000000	32	√	√	√	√
SSI1-2_BUSIF data register	SSI1-2_BUSIF	R/W	H'EC10 1800/ H'EC40 1800*	H'00000000	32	√	√	√	√

Name	Abbreviation	R/W	Address	Initial Value	Access Size	RZ/G Series Products			
						RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
SSI1-3_BUSIF data register	SSI1-3_BUSIF	R/W	H'EC10 1C00/ H'EC40 1C00*	H'00000000	32	√	√	√	√
SSI2-0_BUSIF data register	SSI2-0_BUSIF	R/W	H'EC10 2000/ H'EC40 2000*	H'00000000	32	√	√	√	√
SSI2-1_BUSIF data register	SSI2-1_BUSIF	R/W	H'EC10 2400/ H'EC40 2400*	H'00000000	32	√	√	√	√
SSI2-2_BUSIF data register	SSI2-2_BUSIF	R/W	H'EC10 2800/ H'EC40 2800*	H'00000000	32	√	√	√	√
SSI2-3_BUSIF data register	SSI2-3_BUSIF	R/W	H'EC10 2C00/ H'EC40 2C00*	H'00000000	32	√	√	√	√
SSI3_BUSIF data register	SSI3_BUSIF	R/W	H'EC10 3000/ H'EC40 3000*	H'00000000	32	√	√	√	√
SSI4_BUSIF data register	SSI4_BUSIF	R/W	H'EC10 4000/ H'EC40 4000*	H'00000000	32	√	√	√	√
SSI5_BUSIF data register	SSI5_BUSIF	R/W	H'EC10 5000/ H'EC40 5000*	H'00000000	32	√	√	√	√
SSI6_BUSIF data register	SSI6_BUSIF	R/W	H'EC10 6000/ H'EC40 6000*	H'00000000	32	√	√	√	√
SSI7_BUSIF data register	SSI7_BUSIF	R/W	H'EC10 7000/ H'EC40 7000*	H'00000000	32	√	√	√	√
SSI8_BUSIF data register	SSI8_BUSIF	R/W	H'EC10 8000/ H'EC40 8000*	H'00000000	32	√	√	√	√
SSI9-0_BUSIF data register	SSI9-0_BUSIF	R/W	H'EC10 9000/ H'EC40 9000*	H'00000000	32	√	√	√	√
SSI9-1_BUSIF data register	SSI9-1_BUSIF	R/W	H'EC10 9400/ H'EC40 9400*	H'00000000	32	√	√	√	√
SSI9-2_BUSIF data register	SSI9-2_BUSIF	R/W	H'EC10 9800/ H'EC40 9800*	H'00000000	32	√	√	√	√
SSI9-3_BUSIF data register	SSI9-3_BUSIF	R/W	H'EC10 9C00/ H'EC40 9C00*	H'00000000	32	√	√	√	√

Note: \* Address H'EC10 XXXX is used for data transfer with the audio-DMAC. Address H'EC40 XXXX is used for data transfer with the audio-DMAC (peripheral-peripheral).

## 32.2 Register Description

### Legend for Register Description

Initial value: Register value after a reset. H'xxxx represents a hexadecimal number. Others are represented in binary numbers.

—: Undefined value

R/W: Readable/writable. The written value can be read.

R: Read-only. The write value should always be 0.

R/WC0: Readable/writable. Writing 0 initializes the bit. Writing 1 is ignored.

R/WC1: Readable/writable. Writing 1 initializes the bit. Writing 0 is ignored.

W: Write-only. Reading this bit is prohibited. When the bit is reserved, the write value should always be 0.

—/W: Write-only. The read value is undefined.

All access to registers is made in longword units.



### 32.2.1 SSIn BUSIF Mode Register (SSIn\_BUSIF\_MODE)

Note: n = 0-0 to 0-3, 1-0 to 1-3, 2-0 to 2-3, 3 to 8, or 9-0 to 9-3

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: SSIn\_BUSIF\_MODE determines the initial settings of the bus interface.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
	—	—	—	—	—	—	—	—	—	—	—	sft_dir	sft_num				
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	—	—	—	—	—	—	—	word_s wap	—	—	—	—	—	—	—	—	dma
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W:	R	R	R	R	R	R	R	R/W	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 21	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
20	sft_dir	0	R/W	ssin_busif_shift_dir Selects the bit-shift direction for valid bit position adjustment in the SSIn_BUSIF input and output data. 0: Shift to left. 1: Shift to right.
19 to 16	sft_num	0000	R/W	ssin_busif_shift_num Selects the bit-shift count for valid bit position adjustment in the SSIn_BUSIF input and output data. 0000: 0 bit 0001: 1 bit 0010: 2 bits 0011: 3 bits 0100: 4 bits 0101: 5 bits 0110: 6 bits 0111: 7 bits 1000: 8 bits 1001: 9 bits 1010: 10 bits 1011: 11 bits 1100: 12 bits 1101: 13 bits 1110: 14 bits 1111: 15 bits
15 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

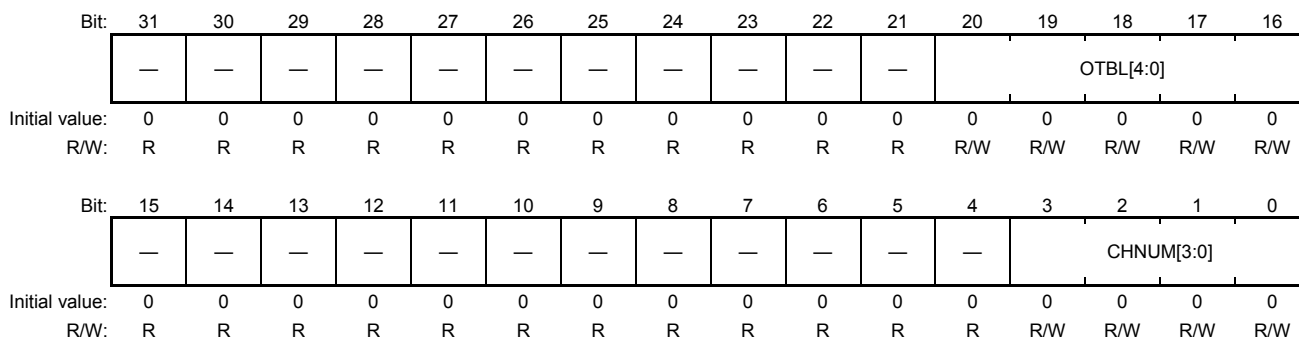
Bit	Bit Name	Initial Value	R/W	Description
8	word_swap	0	R/W	word_swap_en Swaps the word order in SSI $n$ _BUSIF. 0: Word order is not swapped. 1: Word order is swapped. Note: Select this function only when the data length is 16 bits.
7 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	dma	1	R/W	ssi $n$ _dma Selects the access type for SSI $n$ _BUSIF. 0: PIO access (setting prohibited) 1: DMA access Be sure to specify the DMA access.

### 32.2.2 SSIm BUSIF Audio Information Register (SSIm\_BUSIF\_ADINR)

Note: m = 0-0, 1-0, 2-0, 3 to 8, or 9-0

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: SSIm\_BUSIF\_ADINR is a 32-bit readable/writable register that selects channel number and bit length of output audio data.



Bit	Bit Name	Initial Value	R/W	Description
31 to 21	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
20 to 16	OTBL[4:0]	00000	R/W	Bit Length of Output Audio Data. These bits set the bit length of output audio data. 00000: 24 bits 00001: Reserved 00010: 22 bits 00011: Reserved 00100: 20 bits 00101: Reserved 00110: 18 bits 00111: Reserved 01000: 16 bits 01001 to 01111: Reserved 10000: 8 bits 10001 to 11111: Reversed
15 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

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Bit	Bit Name	Initial Value	R/W	Description
3 to 0	CHNUM[3:0]	0000	R/W	Channel Number
				These bits set the channel number.
				0000: 0 (None)
				0001: 1 channel
				0010: 2 channels
				0011: Reserved
				0100: 4 channels
				0101: Reserved
				0110: 6 channels
				0111: Reserved
				1000: 8 channels
				1001 to 1111: Reserved

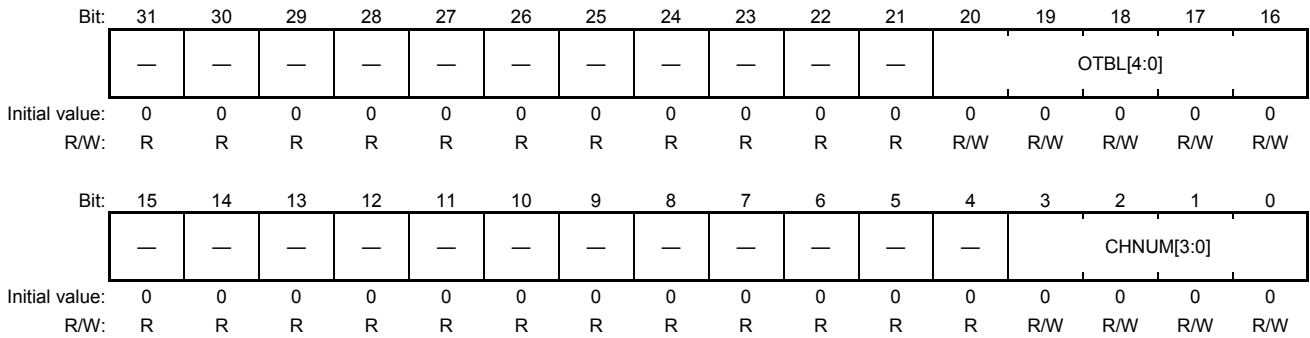
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### 32.2.3 SSIP BUSIF Audio Information Register (SSIP\_BUSIF\_ADINR)

Note: p = 0-1 to 0-3, 1-1 to 1-3, 2-1 to 2-3, or 9-1 to 9-3

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: SSIP\_BUSIF\_ADINR is a 32-bit readable/writable register that selects channel number and bit length of output audio data.



Bit	Bit Name	Initial Value	R/W	Description
31 to 21	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
20 to 16	OTBL[4:0]	00000	R/W	Bit Length of Output Audio Data. These bits set the bit length of output audio data. 00000: 24 bits 00001: Reserved 00010: 22 bits 00011: Reserved 00100: 20 bits 00101: Reserved 00110: 18 bits 00111: Reserved 01000: 16 bits 01001 to 11111: Reserved
15 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3 to 0	CHNUM[3:0]	0000	R/W	Channel Number These bits set the channel number. 0000: 0 (none) 0001: 1 channel 0010: 2 channels 0011 to 1111: Reserved

### 32.2.4 SSIm BUSIF Data Align Register (SSIm\_BUSIF\_DALIGN)

Note: m = 0-0, 1-0, 2-0, 3 to 8, or 9-0

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: SSIm\_BUSIF\_DALIGN determines the initial settings of the SSIm route.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	place7			—	place6			—	place5			—	place4		
Initial value:	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	0
R/W:	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	place3			—	place2			—	place1			—	place0		
Initial value:	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0
R/W:	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
30 to 28	place7	111	R/W	Changes the stream data order. These bits are used for the 8-channel setting. <b>For the 6- or less channel setting or TDM split mode setting (tdm_split = 1), the initial value should not be changed.</b> The data order is changed between the SSI and bus interface. Selects the input-side data to be output to place 7 on the output side. 000: Data at input-side place 0 is sent to output-side place 7. 001: Data at input-side place 1 is sent to output-side place 7. 010: Data at input-side place 2 is sent to output-side place 7. 011: Data at input-side place 3 is sent to output-side place 7. 100: Data at input-side place 4 is sent to output-side place 7. 101: Data at input-side place 5 is sent to output-side place 7. 110: Data at input-side place 6 is sent to output-side place 7. 111: Data at input-side place 7 is sent to output-side place 7.
27	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
26 to 24	place6	110	R/W	<p>Changes the stream data order. These bits are used for the 8-channel setting. <b>For the 6- or less channel setting or TDM split mode setting (tdm_split = 1), the initial value should not be changed.</b></p> <p>The data order is changed between the SSI and bus interface.</p> <p>Selects the input-side data to be output to place 6 on the output side.</p> <p>000: Data at input-side place 0 is sent to output-side place 6.            001: Data at input-side place 1 is sent to output-side place 6.            010: Data at input-side place 2 is sent to output-side place 6.            011: Data at input-side place 3 is sent to output-side place 6.            100: Data at input-side place 4 is sent to output-side place 6.            101: Data at input-side place 5 is sent to output-side place 6.            110: Data at input-side place 6 is sent to output-side place 6.            111: Data at input-side place 7 is sent to output-side place 6.</p>
23	—	0	R	<p>Reserved</p> <p>This bit is always read as 0. The write value should always be 0.</p>
22 to 20	place5	101	R/W	<p>Changes the stream data order. These bits are used for the 6- or more channel setting. <b>For the 4- or less channel setting or TDM split mode setting (tdm_split = 1), the initial value should not be changed.</b></p> <p>The data order is changed between the SSI and bus interface.</p> <p>Selects the input-side data to be output to place 5 on the output side.</p> <p>000: Data at input-side place 0 is sent to output-side place 5.            001: Data at input-side place 1 is sent to output-side place 5.            010: Data at input-side place 2 is sent to output-side place 5.            011: Data at input-side place 3 is sent to output-side place 5.            100: Data at input-side place 4 is sent to output-side place 5.            101: Data at input-side place 5 is sent to output-side place 5.            110: Data at input-side place 6 is sent to output-side place 5.            111: Data at input-side place 7 is sent to output-side place 5.</p>
19	—	0	R	<p>Reserved</p> <p>This bit is always read as 0. The write value should always be 0.</p>
18 to 16	place4	100	R/W	<p>Changes the stream data order. These bits are used for the 6- or more channel setting. <b>For the 4- or less channel setting or TDM split mode setting (tdm_split = 1), the initial value should not be changed.</b></p> <p>The data order is changed between the SSI and bus interface.</p> <p>Selects the input-side data to be output to place 4 on the output side.</p> <p>000: Data at input-side place 0 is sent to output-side place 4.            001: Data at input-side place 1 is sent to output-side place 4.            010: Data at input-side place 2 is sent to output-side place 4.            011: Data at input-side place 3 is sent to output-side place 4.            100: Data at input-side place 4 is sent to output-side place 4.            101: Data at input-side place 5 is sent to output-side place 4.            110: Data at input-side place 6 is sent to output-side place 4.            111: Data at input-side place 7 is sent to output-side place 4.</p>

Bit	Bit Name	Initial Value	R/W	Description
15	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
14 to 12	place3	011	R/W	Changes the stream data order. These bits are used for the 4- or more channel setting. <b>For the 2- or less channel setting or TDM split mode setting (tdm_split = 1), the initial value should not be changed.</b> The data order is changed between the SSI and bus interface. Selects the input-side data to be output to place 3 on the output side. 000: Data at input-side place 0 is sent to output-side place 3. 001: Data at input-side place 1 is sent to output-side place 3. 010: Data at input-side place 2 is sent to output-side place 3. 011: Data at input-side place 3 is sent to output-side place 3. 100: Data at input-side place 4 is sent to output-side place 3. 101: Data at input-side place 5 is sent to output-side place 3. 110: Data at input-side place 6 is sent to output-side place 3. 111: Data at input-side place 7 is sent to output-side place 3.
11	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
10 to 8	place2	010	R/W	Changes the stream data order. These bits are used for the 4- or more channel setting. <b>For the 2- or less channel setting or TDM split mode setting (tdm_split = 1), the initial value should not be changed.</b> The data order is changed between the SSI and bus interface. Selects the input-side data to be output to place 2 on the output side. 000: Data at input-side place 0 is sent to output-side place 2. 001: Data at input-side place 1 is sent to output-side place 2. 010: Data at input-side place 2 is sent to output-side place 2. 011: Data at input-side place 3 is sent to output-side place 2. 100: Data at input-side place 4 is sent to output-side place 2. 101: Data at input-side place 5 is sent to output-side place 2. 110: Data at input-side place 6 is sent to output-side place 2. 111: Data at input-side place 7 is sent to output-side place 2.
7	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.



Bit	Bit Name	Initial Value	R/W	Description
6 to 4	place1	001	R/W	<p>Changes the stream data order. The data order is changed between the SSI and bus interface.</p> <p>Selects the input-side data to be output to place 1 on the output side.</p> <ul style="list-style-type: none"> <li>When TDM split mode is used (tdm_split = 1)           <ul style="list-style-type: none"> <li>000: Data at input-side place 0 is sent to output-side place 1.</li> <li>001: Data at input-side place 1 is sent to output-side place 1.</li> </ul> </li> <li>Other settings are prohibited.</li> <li>When TDM split mode is not used (tdm_split = 0)           <ul style="list-style-type: none"> <li>000: Data at input-side place 0 is sent to output-side place 1.</li> <li>001: Data at input-side place 1 is sent to output-side place 1.</li> <li>010: Data at input-side place 2 is sent to output-side place 1.</li> <li>011: Data at input-side place 3 is sent to output-side place 1.</li> <li>100: Data at input-side place 4 is sent to output-side place 1.</li> <li>101: Data at input-side place 5 is sent to output-side place 1.</li> <li>110: Data at input-side place 6 is sent to output-side place 1.</li> <li>111: Data at input-side place 7 is sent to output-side place 1.</li> </ul> </li> </ul>
3	—	0	R	<p>Reserved</p> <p>This bit is always read as 0. The write value should always be 0.</p>
2 to 0	place0	000	R/W	<p>Changes the stream data order. The data order is changed between the SSI and bus interface.</p> <p>Selects the input-side data to be output to place 0 on the output side.</p> <ul style="list-style-type: none"> <li>When TDM split mode is used (tdm_split = 1)           <ul style="list-style-type: none"> <li>000: Data at input-side place 0 is sent to output-side place 0.</li> <li>001: Data at input-side place 1 is sent to output-side place 0.</li> </ul> </li> <li>Other settings are prohibited.</li> <li>When TDM split mode is not used (tdm_split = 0)           <ul style="list-style-type: none"> <li>000: Data at input-side place 0 is sent to output-side place 0.</li> <li>001: Data at input-side place 1 is sent to output-side place 0.</li> <li>010: Data at input-side place 2 is sent to output-side place 0.</li> <li>011: Data at input-side place 3 is sent to output-side place 0.</li> <li>100: Data at input-side place 4 is sent to output-side place 0.</li> <li>101: Data at input-side place 5 is sent to output-side place 0.</li> <li>110: Data at input-side place 6 is sent to output-side place 0.</li> <li>111: Data at input-side place 7 is sent to output-side place 0.</li> </ul> </li> </ul>

### 32.2.5 SSIP BUSIF Data Align Register (SSIP\_BUSIF\_DALIGN)

Note: p = 0-1 to 0-3, 1-1 to 1-3, 2-1 to 2-3, or 9-1 to 9-3

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: SSIP\_BUSIF\_DALIGN determines the initial settings of the SSIP route.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	place1	—	—	—	place0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	place1	1	R/W	Changes the stream data order. The data order is changed between the SSI and bus interface. Selects the input-side data to be output to place 1 on the output side. 0: Data at input-side place 0 is sent to output-side place 1. 1: Data at input-side place 1 is sent to output-side place 1.
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	place0	0	R/W	Changes the stream data order. The data order is changed between the SSI and bus interface. Selects the input-side data to be output to place 0 on the output side. 0: Data at input-side place 0 is sent to output-side place 0. 1: Data at input-side place 1 is sent to output-side place 0.

### 32.2.6 SSIIq Mode Register (SSIIq\_MODE)

Note:  $q = 0-0, 1-0, 2-0, \text{ or } 9-0$

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: SSIIq\_MODE determines the initial settings of the SSIIq route.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	fs_mod e	—	—	—	—	tdm_spl it	—	—	—	—	—	—	—	tdm_ext
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R	R	R	R	R/W	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13	fs_mode	0	R/W	ssii_fs_mode ( $i = 0, 1, 2, \text{ or } 9$ ) Selects fs to be used with TDM split mode for ssii. 0: ssii TDM split mode is used with 256 fs (stereo x 4). 1: ssii TDM split mode is used with 128 fs (monaural x 4).
12 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	tdm_split	0	R/W	ssii_tdm_split ( $i = 0, 1, 2, \text{ or } 9$ ) Selects whether or not TDM split mode is used for ssii. 0: TDM split mode is not used for ssii (only ssii-0_BUSIF is used). 1: TDM split mode is used for ssii (ssii-1_BUSIF to ssii-3_BUSIF are also used).
7 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	tdm_ext	0	R/W	ssii_tdm_ext ( $i = 0, 1, 2, \text{ or } 9$ ) Selects whether or not TDM extend mode is used for ssii. 0: ssii TDM extend mode is not used. 1: ssii TDM extend mode is used.

Note: Bit 0 (tdm\_ext) and bit 8 (tdm\_split) cannot be set to 1 at the same time.

**32.2.7 SSIr Mode Register (SSIr\_MODE)**

Note: r = 3 or 4

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: SSIr\_MODE determines the initial settings of the SSIr route.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	tdm_ext
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	tdm_ext	0	R/W	ssir_tdm_ext Selects whether or not TDM extend mode is used for ssir. 0: ssir TDM extend mode is not used. 1: ssir TDM extend mode is used.

### 32.2.8 SSIIq Control Register (SSIIq\_CONTROL)

Note: q = 0-0, 1-0, 2-0, or 9-0

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: SSIIq\_CONTROL controls the start and stop of data transfer.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	start_3	—	—	—	start_2	—	—	—	start_1	—	—	—	start_0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R	R	R	R/W	R	R	R	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12	start_3	0	R/W	SSII-3_start_flag (i = 0 to 2, 9) Starts or stops data transfer through SSII-3. 0: Transfer is stopped. 1: Transfer is started.
11 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	start_2	0	R/W	SSII-2_start_flag (i = 0 to 2, 9) Starts or stops data transfer through SSII-2. 0: Transfer is stopped. 1: Transfer is started.
7 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	start_1	0	R/W	SSII-1_start_flag (i = 0 to 2, 9) Starts or stops data transfer through SSII-1. 0: Transfer is stopped. 1: Transfer is started.
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	start_0	0	R/W	SSII-0_start_flag (i = 0 to 2, 9) Starts or stops data transfer through SSII-0. 0: Transfer is stopped. 1: Transfer is started.

Note: If only SSII-0 is used and TDM split mode is not used, SSII-1\_start flag to SSII-3\_start flag should be set to 0 (transfer stopped).

### 32.2.9 SSIr Control Register (SSIr\_CONTROL)

Note: r = 3 to 8

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: SSIr\_CONTROL controls the start and stop of data transfer.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	start
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	start	0	R/W	SSIr_start_flag Starts or stops data transfer through SSIr. 0: Transfer is stopped. 1: Transfer is started.

### 32.2.10 SSIq Status Register (SSIQ\_STATUS)

Note: q = 0-0, 1-0, 2-0, 9-0

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: SSIq\_STATUS indicates the internal buffer state. When a bit in this register is set, its status is indicated by the corresponding interrupt signal. However, when the interrupt output is masked by the SSIq interrupt enable register, the interrupt signal is not output.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	FCST	DTST	UIRQ	OIRQ	IIRQ	DIRQ	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	uf_3	uf_2	uf_1	uf_0	of_3	of_2	of_1	of_0	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31, 30	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
29	FCST	0	R	SSII_FCST (i = 0 to 2, 9) Indicates the state of SSIFSRi_FCST. 0: — 1: The WS signal has stopped.
28	DTST	0	R	SSII_DTST (i = 0 to 2, 9) Indicates the state of SSIFSRi_DTST. 0: — 1: The frequency switching has been detected.
27	UIRQ	0	R	SSII_UIRQ (i = 0 to 2, 9) Indicates the state of SSISRi_UIRQ. 0: — 1: An underflow has occurred. Note: Not indicated by the interrupt signal when SSCRi.UIEN = 0.
26	OIRQ	0	R	SSII_OIRQ (i = 0 to 2, 9) Indicates the state of SSISRi_OIRQ. 0: — 1: An overflow has occurred. Note: Not indicated by the interrupt signal when SSCRi.OIEN = 0.
25	IIRQ	0	R	SSII_IIRQ (i = 0 to 2, 9) Indicates the state of SSISRi_IIRQ. 0: — 1: Idle state Note: Not indicated by the interrupt signal when SSCRi.IIEN = 0.

Bit	Bit Name	Initial Value	R/W	Description
24	DIRQ	0	R	<p>SSI<math>i</math>_DIRQ (i = 0 to 2, 9)</p> <p>Indicates the state of SSISR<math>i</math>_DIRQ.</p> <p>0: —</p> <p>1: When SSICR<math>i</math>.TRMD is 0, DIRQ = 1 indicates that there are unread data in SSIRDR. When SSICR<math>i</math>.TRMD is 1, DIRQ = 1 indicates that data can be written to SSITDR.</p> <p>Note: Not indicated by the interrupt signal when SSICR<math>i</math>.DIEN = 0.</p>
23 to 16	—	All 0	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>
15	uf_3	0	R	<p>buf_under_flow<math>i-3</math> (i = 0 to 2, 9)</p> <p>Indicates the state of SSI_SYSTEM_STATUS2/3.uf<math>i-3</math>.</p> <p>0: —</p> <p>1: An underflow has occurred.</p> <p>Note: Not indicated by the interrupt signal when SSI_SYSTEM_INT_ENABLE2/3.uf<math>i-3</math>_ie = 0.</p>
14	uf_2	0	R	<p>buf_under_flow<math>i-2</math> (i = 0 to 2, 9)</p> <p>Indicates the state of SSI_SYSTEM_STATUS2/3.uf<math>i-2</math>.</p> <p>0: —</p> <p>1: An underflow has occurred.</p> <p>Note: Not indicated by the interrupt signal when SSI_SYSTEM_INT_ENABLE2/3.uf<math>i-2</math>_ie = 0.</p>
13	uf_1	0	R	<p>buf_under_flow<math>i-1</math> (i = 0 to 2, 9)</p> <p>Indicates the state of SSI_SYSTEM_STATUS2/3.uf<math>i-1</math>.</p> <p>0: —</p> <p>1: An underflow has occurred.</p> <p>Note: Not indicated by the interrupt signal when SSI_SYSTEM_INT_ENABLE2/3.uf<math>i-1</math>_ie = 0.</p>
12	uf_0	0	R	<p>buf_under_flow<math>i-0</math> (i = 0 to 2, 9)</p> <p>Indicates the state of SSI_SYSTEM_STATUS2/3.uf<math>i-0</math>.</p> <p>0: —</p> <p>1: An underflow has occurred.</p> <p>Note: Not indicated by the interrupt signal when SSI_SYSTEM_INT_ENABLE2/3.uf<math>i-0</math>_ie = 0.</p>
11	of_3	0	R	<p>buf_over_flow<math>i-3</math> (i = 0 to 2, 9)</p> <p>Indicates the state of SSI_SYSTEM_STATUS2/3.of<math>i-3</math>.</p> <p>0: —</p> <p>1: An overflow has occurred.</p> <p>Note: Not indicated by the interrupt signal when SSI_SYSTEM_INT_ENABLE2/3.of<math>i-3</math>_ie = 0.</p>
10	of_2	0	R	<p>buf_over_flow<math>i-2</math> (i = 0 to 2, 9)</p> <p>Indicates the state of SSI_SYSTEM_STATUS2/3.of<math>i-2</math>.</p> <p>0: —</p> <p>1: An overflow has occurred.</p> <p>Note: Not indicated by the interrupt signal when SSI_SYSTEM_INT_ENABLE2/3.of<math>i-2</math>_ie = 0.</p>



Bit	Bit Name	Initial Value	R/W	Description
9	of_1	0	R	buf_over_flow <i>i</i> -1 (i = 0 to 2, 9) Indicates the state of SSI_SYSTEM_STATUS2/3.of <i>i</i> -1. 0: — 1: An overflow has occurred. Note: Not indicated by the interrupt signal when SSI_SYSTEM_INT_ENABLE2/3.of <i>i</i> -1_ie = 0.
8	of_0	0	R	buf_over_flow <i>i</i> -0 (i = 0 to 2, 9) Indicates the state of SSI_SYSTEM_STATUS2/3.of <i>i</i> -0. 0: — 1: An overflow has occurred. Note: Not indicated by the interrupt signal when SSI_SYSTEM_INT_ENABLE2/3.of <i>i</i> -0_ie = 0.
7 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

### 32.2.11 SSIR Status Register (SSIR\_STATUS)

Note:  $r = 3$  to 8

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: SSIR\_STATUS indicates the internal buffer state. When a bit in this register is set, its status is indicated by the corresponding interrupt signal. However, when the interrupt output is masked by the SSIR interrupt enable register, the interrupt signal is not output.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	FCST	DTST	UIRQ	OIRQ	IIRQ	DIRQ	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31, 30	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
29	FCST	0	R	SSIR <sub>i</sub> _FCST ( $i = 3$ to 8) Indicates the state of SSIFSR <sub>i</sub> _FCST. 0: — 1: The WS signal has stopped.
28	DTST	0	R	SSIR <sub>i</sub> _DTST ( $i = 3$ to 8) Indicates the state of SSIFSR <sub>i</sub> _DTST. 0: — 1: The frequency switching has been detected.
27	UIRQ	0	R	SSIR <sub>i</sub> _UIRQ ( $i = 3$ to 8) Indicates the state of SSISR <sub>i</sub> _UIRQ. 0: — 1: An underflow has occurred. Note: Not indicated by the interrupt signal when SSICR <sub>i</sub> .UIEN = 0.
26	OIRQ	0	R	SSIR <sub>i</sub> _OIRQ ( $i = 3$ to 8) Indicates the state of SSISR <sub>i</sub> _OIRQ. 0: — 1: An overflow has occurred. Note: Not indicated by the interrupt signal when SSICR <sub>i</sub> .OEN = 0.
25	IIRQ	0	R	SSIR <sub>i</sub> _IIRQ ( $i = 3$ to 8) Indicates the state of SSISR <sub>i</sub> _IIRQ. 0: — 1: Idle state Note: Not indicated by the interrupt signal when SSICR <sub>i</sub> .IEN = 0.

Bit	Bit Name	Initial Value	R/W	Description
24	DIRQ	0	R	<p>SSI<math>i</math>_DIRQ (<math>i = 3</math> to <math>8</math>)</p> <p>Indicates the state of SSISR<math>i</math>_DIRQ.</p> <p>0: —</p> <p>1: When SSICR<math>i</math>.TRMD is 0, DIRQ = 1 indicates that there are unread data in SSIRDR. When SSICR<math>i</math>.TRMD is 1, DIRQ = 1 indicates that data can be written to SSITDR.</p> <p>Note: Not indicated by the interrupt signal when SSICR<math>i</math>.DIEN = 0.</p>
23 to 0	—	All 0	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>

### 32.2.12 SSIq Interrupt Enable Register (SSIq\_INT\_ENABLE\_MAIN)

Note: q = 0-0, 1-0, 2-0, or 9-0

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: SSIq\_INT\_ENABLE\_MAIN enables or disables output of interrupts corresponding to the states indicated in the SSIq status register.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	FCST <sub>i</sub> <sub>e</sub>	DTST <sub>i</sub> <sub>e</sub>	UIRQ <sub>i</sub> <sub>e</sub>	OIRQ <sub>i</sub> <sub>e</sub>	IIRQ <sub>ie</sub>	DIRQ <sub>i</sub> <sub>e</sub>	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	uf <sub>3</sub> <sub>ie</sub>	uf <sub>2</sub> <sub>ie</sub>	uf <sub>1</sub> <sub>ie</sub>	uf <sub>0</sub> <sub>ie</sub>	of <sub>3</sub> <sub>ie</sub>	of <sub>2</sub> <sub>ie</sub>	of <sub>1</sub> <sub>ie</sub>	of <sub>0</sub> <sub>ie</sub>	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31, 30	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
29	FCST <sub>ie</sub>	0	R/W	SSI <sub>i</sub> _FCST_int_enable (i = 0 to 2,9) 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
28	DTST <sub>ie</sub>	0	R/W	SSI <sub>i</sub> _DTST_int_enable (i = 0 to 2,9) 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
27	UIRQ <sub>ie</sub>	0	R/W	SSI <sub>i</sub> _UIRQ_int_enable (i = 0 to 2,9) 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
26	OIRQ <sub>ie</sub>	0	R/W	SSI <sub>i</sub> _OIRQ_int_enable (i = 0 to 2,9) 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
25	IIRQ <sub>ie</sub>	0	R/W	SSI <sub>i</sub> _IIRQ_int_enable (i = 0 to 2,9) 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
24	DIRQ <sub>ie</sub>	0	R/W	SSI <sub>i</sub> _DIRQ_int_enable (i = 0 to 2,9) 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
23 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15	uf <sub>3</sub> <sub>ie</sub>	0	R/W	buf_under_flow <sub>i-3</sub> _int_enable (i = 0 to 2, 9) 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.

Bit	Bit Name	Initial Value	R/W	Description
14	uf_2_ie	0	R/W	buf_under_flow <i>i</i> -2_int_enable (i = 0 to 2, 9) 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
13	uf_1_ie	0	R/W	buf_under_flow <i>i</i> -1_int_enable (i = 0 to 2, 9) 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
12	uf_0_ie	0	R/W	buf_under_flow <i>i</i> -0_int_enable (i = 0 to 2, 9) 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
11	of_3_ie	0	R/W	buf_over_flow <i>i</i> -3_int_enable (i = 0 to 2, 9) 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
10	of_2_ie	0	R/W	buf_over_flow <i>i</i> -2_int_enable (i = 0 to 2, 9) 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
9	of_1_ie	0	R/W	buf_over_flow <i>i</i> -1_int_enable (i = 0 to 2, 9) 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
8	of_0_ie	0	R/W	buf_over_flow <i>i</i> -0_int_enable (i = 0 to 2, 9) 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
7 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

### 32.2.13 SSIr Interrupt Enable Register (SSIr\_INT\_ENABLE\_MAIN)

Note:  $r = 3$  to 8

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: SSIr\_INT\_ENABLE\_MAIN enables or disables output of interrupts corresponding to the states indicated in the SSIr status register.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	FCST <sub>i</sub> e	DTST <sub>i</sub> e	UIRQ <sub>i</sub> e	OIRQ <sub>i</sub> e	IIRQ <sub>ie</sub>	DIRQ <sub>i</sub> e	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	—	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31, 30	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
29	FCST <sub>i</sub> ie	0	R/W	SSI <sub>i</sub> _FCST_int_enable (i = 3 to 8) 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
28	DTST <sub>i</sub> ie	0	R/W	SSI <sub>i</sub> _DTST_int_enable (i = 3 to 8) 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
27	UIRQ <sub>i</sub> ie	0	R/W	SSI <sub>i</sub> _UIRQ_int_enable (i = 3 to 8) 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
26	OIRQ <sub>i</sub> ie	0	R/W	SSI <sub>i</sub> _OIRQ_int_enable (i = 3 to 8) 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
25	IIRQ <sub>ie</sub>	0	R/W	SSI <sub>i</sub> _IIRQ_int_enable (i = 3 to 8) 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
24	DIRQ <sub>i</sub> ie	0	R/W	SSI <sub>i</sub> _DIRQ_int_enable (i = 3 to 8) 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
23 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	—	—	R	Reserved The read value is undefined. The write value should always be 0.

---

Bit	Bit Name	Initial Value	R/W	Description
7 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

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### 32.2.14 SSI Mode Register 0 (SSI\_MODE0)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: SSI\_MODE0 specifies the independent SSI transfer.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	ind_word_swap9	ind_word_swap8	ind_word_swap7	ind_word_swap6	ind_word_swap5	ind_word_swap4	ind_word_swap3	ind_word_swap2	ind_word_swap1	ind_word_swap0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	ind9	ind8	ind7	ind6	ind5	ind4	ind3	ind2	ind1	ind0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 26	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
25	ind_word_swap9	0	R/W	ind_word_swap_en9 Swaps the word order (only for access to SSITDR or SSIRDR). 0: Word order is not swapped. 1: Word order is swapped. Note: Select this function only when the data length is 16 bits.
24	ind_word_swap8	0	R/W	ind_word_swap_en8 Swaps the word order (only for access to SSITDR or SSIRDR). 0: Word order is not swapped. 1: Word order is swapped. Note: Select this function only when the data length is 16 bits.
23	ind_word_swap7	0	R/W	ind_word_swap_en7 Swaps the word order (only for access to SSITDR or SSIRDR). 0: Word order is not swapped. 1: Word order is swapped. Note: Select this function only when the data length is 16 bits.
22	ind_word_swap6	0	R/W	ind_word_swap_en6 Swaps the word order (only for access to SSITDR or SSIRDR). 0: Word order is not swapped. 1: Word order is swapped. Note: Select this function only when the data length is 16 bits.
21	ind_word_swap5	0	R/W	ind_word_swap_en5 Swaps the word order (only for access to SSITDR or SSIRDR). 0: Word order is not swapped. 1: Word order is swapped. Note: Select this function only when the data length is 16 bits.



Bit	Bit Name	Initial Value	R/W	Description
20	ind_word_swap4	0	R/W	ind_word_swap_en4 Swaps the word order (only for access to SSITDR or SSIRDR). 0: Word order is not swapped. 1: Word order is swapped. Note: Select this function only when the data length is 16 bits.
19	ind_word_swap3	0	R/W	ind_word_swap_en3 Swaps the word order (only for access to SSITDR or SSIRDR). 0: Word order is not swapped. 1: Word order is swapped. Note: Select this function only when the data length is 16 bits.
18	ind_word_swap2	0	R/W	ind_word_swap_en2 Swaps the word order (only for access to SSITDR or SSIRDR). 0: Word order is not swapped. 1: Word order is swapped. Note: Select this function only when the data length is 16 bits.
17	ind_word_swap1	0	R/W	ind_word_swap_en1 Swaps the word order (only for access to SSITDR or SSIRDR). 0: Word order is not swapped. 1: Word order is swapped. Note: Select this function only when the data length is 16 bits.
16	ind_word_swap0	0	R/W	ind_word_swap_en0 Swaps the word order (only for access to SSITDR or SSIRDR). 0: Word order is not swapped. 1: Word order is swapped. Note: Select this function only when the data length is 16 bits.
15 to 10	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
9	ind9	0	R/W	Independent SSI9 transfer setting 0: Independent SSI9 transfer is not performed. 1: Independent SSI9 transfer is performed.
8	ind8	0	R/W	Independent SSI8 transfer setting 0: Independent SSI8 transfer is not performed. 1: Independent SSI8 transfer is performed.
7	ind7	0	R/W	Independent SSI7 transfer setting 0: Independent SSI7 transfer is not performed. 1: Independent SSI7 transfer is performed.
6	ind6	0	R/W	Independent SSI6 transfer setting 0: Independent SSI6 transfer is not performed. 1: Independent SSI6 transfer is performed.
5	ind5	0	R/W	Independent SSI5 transfer setting 0: Independent SSI5 transfer is not performed. 1: Independent SSI5 transfer is performed.

Bit	Bit Name	Initial Value	R/W	Description
4	ind4	0	R/W	Independent SSI transfer setting
3	ind3	0	R/W	0: Independent SSI transfer is not performed. 1: Independent SSI transfer is performed. These bits correspond to the SSI modules as follows. SSI3 = ssi_ind3 SSI4 = ssi_ind4
2	ind2	0	R/W	Independent SSI2 transfer setting 0: Independent SSI2 transfer is not performed. 1: Independent SSI2 transfer is performed.
1	ind1	0	R/W	Independent SSI1 transfer setting 0: Independent SSI1 transfer is not performed. 1: Independent SSI1 transfer is performed.
0	ind0	0	R/W	Independent SSI0 transfer setting 0: Independent SSI0 transfer is not performed. 1: Independent SSI0 transfer is performed.

### 32.2.15 SSI Mode Register 1 (SSI\_MODE1)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: SSI\_MODE1 specifies the SSI pin modes.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	ssi34_s ync	—	—	ssi4_pin	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	ssi012_ 3mod	ssi2_pin		ssi1_pin	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 21	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
20	ssi34_sync	0	R/W	ssi34_sync_mode Selects whether to synchronize SSI3 and SSI4. 0: SSI3 and SSI4 are not synchronized. 1: SSI3 and SSI4 are synchronized. This bit can be set to 1 only when the ssi4_pin_mode bits are set to 01 or 10.
19, 18	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
17, 16	ssi4_pin	00	R/W	ssi4_pin_mode Select the connections of the SSI_SCK4 and SSI_WS4 pins. 00: SSI3 and SSI4 use their own pins independently. 01: The SSI3 pins are used in common by SSI3 and SSI4. Both modules work as slaves. The SSI_WS and SSI_SCK pins of SSI3 are used. 10: The SSI3 pins are used in common by SSI3 and SSI4. SSI3 works as the master and SSI4 works as a slave. The SSI_WS and SSI_SCK pins of SSI3 are used. 11: Setting prohibited
15 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
4	ssi012_3module_mode	0	R/W	<p>ssi012_3module_mode</p> <p>Selects whether to use three modules (SSI0, SSI1, and SSI2) together as six channels.</p> <p>0: SSI0, SSI1, and SSI2 are not used as six channels.</p> <p>1: SSI0, SSI1, and SSI2 are used as six channels.</p> <p>This bit should be cleared to 0 when the ssi1_pin_mode or ssi2_pin_mode bits are set to 00.</p> <p>It can be set to 1 only when the ssi1_pin_mode and ssi2_pin_mode bits are set to 01 or when the ssi1_pin_mode and ssi2_pin_mode bits are set to 10.</p> <p>Either ssi012_3module_mode or ssi0129_4module_mode must be set to 1.</p>
3, 2	ssi2_pin	00	R/W	<p>ssi2_pin_mode</p> <p>Select the connections of the SSI_SCK2 and SSI_WS2 pins.</p> <p>00: SSI0 and SSI2 use their own pins independently.</p> <p>01: The SSI0 pins are used in common by SSI0 and SSI2. Both modules work as slaves. The SSI_WS and SSI_SCK pins of SSI0 are used.</p> <p>10: The SSI0 pins are used in common by SSI0 and SSI2. SSI0 works as the master and SSI2 works as a slave. The SSI_WS and SSI_SCK pins of SSI0 are used.</p> <p>11: Setting prohibited</p>
1, 0	ssi1_pin	00	R/W	<p>ssi1_pin_mode</p> <p>Select the connections of the SSI_SCK1 and SSI_WS1 pins.</p> <p>00: SSI0 and SSI1 use their own pins independently.</p> <p>01: The SSI0 pins are used in common by SSI0 and SSI1. Both modules work as slaves. The SSI_WS and SSI_SCK pins of SSI0 are used.</p> <p>10: The SSI0 pins are used in common by SSI0 and SSI1. SSI0 works as the master and SSI1 works as a slave. The SSI_WS and SSI_SCK pins of SSI0 are used.</p> <p>11: Setting prohibited</p>

**32.2.16 SSI Mode Register 2 (SSI\_MODE2)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: SSI\_MODE2 specifies the SSI pin modes.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	ssi0129_4mod	—	ssi9_pin		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	ssi0129_4mod	0	R/W	ssi0129_4module_mode Selects whether to use four modules (SSI0, SSI1, SSI2, and SSI9) together as eight channels. 0: SSI0, SSI1, SSI2, and SSI9 are not used as eight channels. 1: SSI0, SSI1, SSI2, and SSI9 are used as eight channels. This bit should be cleared to 0 when the ssi1_pin_mode or ssi2_pin_mode bits are set to 00, or when ssi9_pin_mode bits are set to 000. It can be set to 1 only when the ssi1_pin_mode and ssi2_pin_mode bits are set to 01 and the ssi9_pin_mode bits are set to 001, or when the ssi1_pin_mode and ssi2_pin_mode bits are set to 10 and the ssi9_pin_mode bits are set to 010. Either ssi0129_4module_mode or ssi012_3module_mode must be set to 1.
3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
2 to 0	ssi9_pin	000	R/W	<p>ssi9_pin_mode</p> <p>Selects the connections of the SSI_SCK9 and SSI_WS9 pins.</p> <p>000: SSI0 and SSI9 use their own pins independently.</p> <p>001: The SSI0 pins are used in common by SSI0 and SSI9. Both modules work as slaves. The SSI_WS and SSI_SCK pins of SSI0 are used.</p> <p>010: The SSI0 pins are used in common by SSI0 and SSI9. SSI0 works as the master and SSI9 works as a slave. The SSI_WS and SSI_SCK pins of SSI0 are used.</p> <p>011: Setting prohibited</p> <p>100: Setting prohibited</p> <p>101: The SSI3 pins are used in common by SSI3 and SSI9. Both modules work as slaves. The SSI_WS and SSI_SCK pins of SSI3 are used.</p> <p>110: The SSI3 pins are used in common by SSI3 and SSI9. SSI3 works as the master and SSI9 works as a slave. The SSI_WS and SSI_SCK pins of SSI3 are used.</p> <p>111: Setting prohibited</p>

**32.2.17 SSI Mode Register 3 (SSI\_MODE3)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: SSI\_MODE3 specifies the SSI pin modes.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ssi3_pin
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1, 0	ssi3_pin	00	R/W	ssi3_pin_mode Select the connections of the SSI_SCK3 and SSI_WS3 pins. 00: SSI0 and SSI3 use their own pins independently. 01: The SSI0 pins are used in common by SSI0 and SSI3. Both modules work as slaves. The SSI_WS and SSI_SCK pins of SSI0 are used. 10: The SSI0 pins are used in common by SSI0 and SSI3. SSI0 works as the master and SSI3 works as a slave. The SSI_WS and SSI_SCK pins of SSI0 are used. 11: Setting prohibited When setting these bits to use the pins in common by SSI0 and SSI3, ssi4_pin_mode should be 00 and ssi9_pin_mode should be 000, 001, or 010 (selection of the SSI3 pins is prohibited).

### 32.2.18 SSI Control Register (SSI\_CONTROL)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: SSI\_CONTROL controls the startup of the SSI modules when multiple SSI modules are used at the same time.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	ssi34	—	—	—	ssi0129
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	ssi34	0	R/W	ssi34_enable Starts or stops data transfer through two SSI modules (SSI3 and SSI4) at the same time. 0: Transfer through SSI3 and SSI4 is stopped. 1: Transfer through SSI3 and SSI4 is started.
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	ssi0129	0	R/W	ssi0129_enable <ul style="list-style-type: none"> <li>When ssi0129_4module_mode is 0 Starts or stops data transfer through three SSI modules (SSI0, SSI1, and SSI2) at the same time. 0: Transfer through SSI0, SSI1, and SSI2 is stopped. 1: Transfer through SSI0, SSI1, and SSI2 is started.</li> <li>When ssi0129_4module_mode is 1 Starts or stops data transfer through four SSI modules (SSI0, SSI1, SSI2, and SSI9) at the same time. 0: Transfer through SSI0, SSI1, SSI2, and SSI9 is stopped. 1: Transfer through SSI0, SSI1, SSI2, and SSI9 is started.</li> </ul>

Note: This function should be used only when data is transferred through multiple SSI modules in synchronization. When using each SSI module independently, use the EN bit of SSICRn (n = 0 to 4 and 9) for the SSI module to control the transfer.



**32.2.19 SSI SYSTEM Status Register 0 (SSI\_SYSTEM\_STATUS0)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: SSI\_SYSTEM\_STATUS0 indicates the internal buffer state. When a bit in this register is set, its status is indicated by the corresponding interrupt signal. However, when the interrupt output is masked by the SSI\_SYSTEM interrupt enable register 0, the interrupt signal is not output.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	of2-3	of2-2	of2-1	of2-0	of1-3	of1-2	of1-1	of1-0	of0-3	of0-2	of0-1	of0-0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1

Bit	Bit Name	Initial Value	R/W	Description
31 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11	of2-3	0	R/WC1	buf_over_flow2-3 Indicates the state of the SSI2-3_BUSIF buffer. 0: Normal operation 1: An overflow has occurred.
10	of2-2	0	R/WC1	buf_over_flow2-2 Indicates the state of the SSI2-2_BUSIF buffer. 0: Normal operation 1: An overflow has occurred.
9	of2-1	0	R/WC1	buf_over_flow2-1 Indicates the state of the SSI2-1_BUSIF buffer. 0: Normal operation 1: An overflow has occurred.
8	of2-0	0	R/WC1	buf_over_flow2-0 Indicates the state of the SSI2-0_BUSIF buffer. 0: Normal operation 1: An overflow has occurred.
7	of1-3	0	R/WC1	buf_over_flow1-3 Indicates the state of the SSI1-3_BUSIF buffer. 0: Normal operation 1: An overflow has occurred.
6	of1-2	0	R/WC1	buf_over_flow1-2 Indicates the state of the SSI1-2_BUSIF buffer. 0: Normal operation 1: An overflow has occurred.

Bit	Bit Name	Initial Value	R/W	Description
5	of1-1	0	R/WC1	buf_over_flow1-1 Indicates the state of the SSI1-1_BUSIF buffer. 0: Normal operation 1: An overflow has occurred.
4	of1-0	0	R/WC1	buf_over_flow2-0 Indicates the state of the SSI1-0_BUSIF buffer. 0: Normal operation 1: An overflow has occurred.
3	of0-3	0	R/WC1	buf_over_flow0-3 Indicates the state of the SSI0-3_BUSIF buffer. 0: Normal operation 1: An overflow has occurred.
2	of0-2	0	R/WC1	buf_over_flow0-2 Indicates the state of the SSI0-2_BUSIF buffer. 0: Normal operation 1: An overflow has occurred.
1	of0-1	0	R/WC1	buf_over_flow0-1 Indicates the state of the SSI0-1_BUSIF buffer. 0: Normal operation 1: An overflow has occurred.
0	of0-0	0	R/WC1	buf_over_flow0-0 Indicates the state of the SSI0-0_BUSIF buffer. 0: Normal operation 1: An overflow has occurred.

### 32.2.20 SSI SYSTEM Status Register 1 (SSI\_SYSTEM\_STATUS1)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: SSI\_SYSTEM\_STATUS1 indicates the internal buffer state. When a bit in this register is set, its status is indicated by the corresponding interrupt signal. However, when the interrupt output is masked by the SSI\_SYSTEM interrupt enable register 1, the interrupt signal is not output.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	of9-3	of9-2	of9-1	of9-0	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/WC1	R/WC1	R/WC1	R/WC1	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7	of9-3	0	R/WC1	buf_over_flow9-3 Indicates the state of the SSI9-3_BUSIF buffer. 0: Normal operation 1: An overflow has occurred.
6	of9-2	0	R/WC1	buf_over_flow9-2 Indicates the state of the SSI9-2_BUSIF buffer. 0: Normal operation 1: An overflow has occurred.
5	of9-1	0	R/WC1	buf_over_flow9-1 Indicates the state of the SSI9-1_BUSIF buffer. 0: Normal operation 1: An overflow has occurred.
4	of9-0	0	R/WC1	buf_over_flow9-0 Indicates the state of the SSI9-0_BUSIF buffer. 0: Normal operation 1: An overflow has occurred.
3 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

**32.2.21 SSI SYSTEM Status Register 2 (SSI\_SYSTEM\_STATUS2)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: SSI\_SYSTEM\_STATUS2 indicates the internal buffer state. When a bit in this register is set, its status is indicated by the corresponding interrupt signal. However, when the interrupt output is masked by the SSI\_SYSTEM interrupt enable register 2, the interrupt signal is not output.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	uf2-3	uf2-2	uf2-1	uf2-0	uf1-3	uf1-2	uf1-1	uf1-0	uf0-3	uf0-2	uf0-1	uf0-0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1

Bit	Bit Name	Initial Value	R/W	Description
31 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11	uf2-3	0	R/WC1	buf_under_flow2-3 Indicates the state of the SSI2-3_BUSIF buffer. 0: Normal operation 1: An underflow has occurred.
10	uf2-2	0	R/WC1	buf_under_flow2-2 Indicates the state of the SSI2-2_BUSIF buffer. 0: Normal operation 1: An underflow has occurred.
9	uf2-1	0	R/WC1	buf_under_flow2-1 Indicates the state of the SSI2-1_BUSIF buffer. 0: Normal operation 1: An underflow has occurred.
8	uf2-0	0	R/WC1	buf_under_flow2-0 Indicates the state of the SSI2-0_BUSIF buffer. 0: Normal operation 1: An underflow has occurred.
7	uf1-3	0	R/WC1	buf_under_flow1-3 Indicates the state of the SSI1-3_BUSIF buffer. 0: Normal operation 1: An underflow has occurred.
6	uf1-2	0	R/WC1	buf_under_flow1-2 Indicates the state of the SSI1-2_BUSIF buffer. 0: Normal operation 1: An underflow has occurred.

Bit	Bit Name	Initial Value	R/W	Description
5	uf1-1	0	R/WC1	buf_under_flow1-1 Indicates the state of the SSI1-1_BUSIF buffer. 0: Normal operation 1: An underflow has occurred.
4	uf1-0	0	R/WC1	buf_under_flow1-0 Indicates the state of the SSI1-0_BUSIF buffer. 0: Normal operation 1: An underflow has occurred.
3	uf0-3	0	R/WC1	buf_under_flow0-3 Indicates the state of the SSI0-3_BUSIF buffer. 0: Normal operation 1: An underflow has occurred.
2	uf0-2	0	R/WC1	buf_under_flow0-2 Indicates the state of the SSI0-2_BUSIF buffer. 0: Normal operation 1: An underflow has occurred.
1	uf0-1	0	R/WC1	buf_under_flow0-1 Indicates the state of the SSI0-1_BUSIF buffer. 0: Normal operation 1: An underflow has occurred.
0	uf0-0	0	R/WC1	buf_under_flow0-0 Indicates the state of the SSI0-0_BUSIF buffer. 0: Normal operation 1: An underflow has occurred.

**32.2.22 SSI SYSTEM Status Register 3 (SSI\_SYSTEM\_STATUS3)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: SSI\_SYSTEM\_STATUS3 indicates the internal buffer state. When a bit in this register is set, its status is indicated by the corresponding interrupt signal. However, when the interrupt output is masked by the SSI\_SYSTEM interrupt enable register 3, the interrupt signal is not output.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	uf9-3	uf9-2	uf9-1	uf9-0	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/WC1	R/WC1	R/WC1	R/WC1	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7	uf9-3	0	R/WC1	buf_under_flow9-3 Indicates the state of the SSI9-3_BUSIF buffer. 0: Normal operation 1: An underflow has occurred.
6	uf9-2	0	R/WC1	buf_under_flow9-2 Indicates the state of the SSI9-2_BUSIF buffer. 0: Normal operation 1: An underflow has occurred.
5	uf9-1	0	R/WC1	buf_under_flow9-1 Indicates the state of the SSI9-1_BUSIF buffer. 0: Normal operation 1: An underflow has occurred.
4	uf9-0	0	R/WC1	buf_under_flow9-0 Indicates the state of the SSI9-0_BUSIF buffer. 0: Normal operation 1: An underflow has occurred.
3 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

**32.2.23 SSI SYSTEM Interrupt Enable Register 0 (SSI\_SYSTEM\_INT\_ENABLE0)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: SSI\_SYSTEM\_INT\_ENABLE0 enables or disables output of interrupts corresponding to the states indicated in the SSI SYSTEM status register 0.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	of2-3 _ie	of2-2 _ie	of2-1 _ie	of2-0 _ie	of1-3 _ie	of1-2 _ie	of1-1 _ie	of1-0 _ie	of0-3 _ie	of0-2 _ie	of0-1 _ie	of0-0 _ie
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11	of2-3_ie	0	R/W	buf_over_flow2-3_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
10	of2-2_ie	0	R/W	buf_over_flow2-2_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
9	of2-1_ie	0	R/W	buf_over_flow2-1_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
8	of2-0_ie	0	R/W	buf_over_flow2-0_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
7	of1-3_ie	0	R/W	buf_over_flow1-3_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
6	of1-2_ie	0	R/W	buf_over_flow1-2_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
5	of1-1_ie	0	R/W	buf_over_flow1-1_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
4	of1-0_ie	0	R/W	buf_over_flow1-0_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.

Bit	Bit Name	Initial Value	R/W	Description
3	of0-3_ie	0	R/W	buf_over_flow0-3_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
2	of0-2_ie	0	R/W	buf_over_flow0-2_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
1	of0-1_ie	0	R/W	buf_over_flow0-1_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
0	of0-0_ie	0	R/W	buf_over_flow0-0_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.



### 32.2.24 SSI SYSTEM Interrupt Enable Register 1 (SSI\_SYSTEM\_INT\_ENABLE1)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: SSI\_SYSTEM\_INT\_ENABLE1 enables or disables output of interrupts corresponding to the states indicated in the SSI SYSTEM status register 1.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	of9-3 _ie	of9-2 _ie	of9-1 _ie	of9-0 _ie	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7	of9-3_ie	0	R/W	buf_over_flow9-3_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
6	of9-2_ie	0	R/W	buf_over_flow9-2_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
5	of9-1_ie	0	R/W	buf_over_flow9-1_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
4	of9-0_ie	0	R/W	buf_over_flow9-0_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
3 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

### 32.2.25 SSI SYSTEM Interrupt Enable Register 2 (SSI\_SYSTEM\_INT\_ENABLE2)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: SSI\_SYSTEM\_INT\_ENABLE2 enables or disables output of interrupts corresponding to the states indicated in the SSI SYSTEM status register 2.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	uf2-3 _ie	uf2-2 _ie	uf2-1 _ie	uf2-0 _ie	uf1-3 _ie	uf1-2 _ie	uf1-1 _ie	uf1-0 _ie	uf0-3 _ie	uf0-2 _ie	uf0-1 _ie	uf0-0 _ie
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11	uf2-3_ie	0	R/W	buf_under_flow2-3_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
10	uf2-2_ie	0	R/W	buf_under_flow2-2_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
9	uf2-1_ie	0	R/W	buf_under_flow2-1_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
8	uf2-0_ie	0	R/W	buf_under_flow2-0_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
7	uf1-3_ie	0	R/W	buf_under_flow1-3_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
6	uf1-2_ie	0	R/W	buf_under_flow1-2_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
5	uf1-1_ie	0	R/W	buf_under_flow1-1_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
4	uf1-0_ie	0	R/W	buf_under_flow1-0_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.

Bit	Bit Name	Initial Value	R/W	Description
3	uf0-3_ie	0	R/W	buf_under_flow0-3_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
2	uf0-2_ie	0	R/W	buf_under_flow0-2_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
1	uf0-1_ie	0	R/W	buf_under_flow0-1_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
0	uf0-0_ie	0	R/W	buf_under_flow0-0_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.

**32.2.26 SSI SYSTEM Interrupt Enable Register 3 (SSI\_SYSTEM\_INT\_ENABLE3)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: SSI\_SYSTEM\_INT\_ENABLE3 enables or disables output of interrupts corresponding to the states indicated in the SSI SYSTEM status register 3.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	uf9-3 _ie	uf9-2 _ie	uf9-1 _ie	uf9-0 _ie	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R	R	R	R

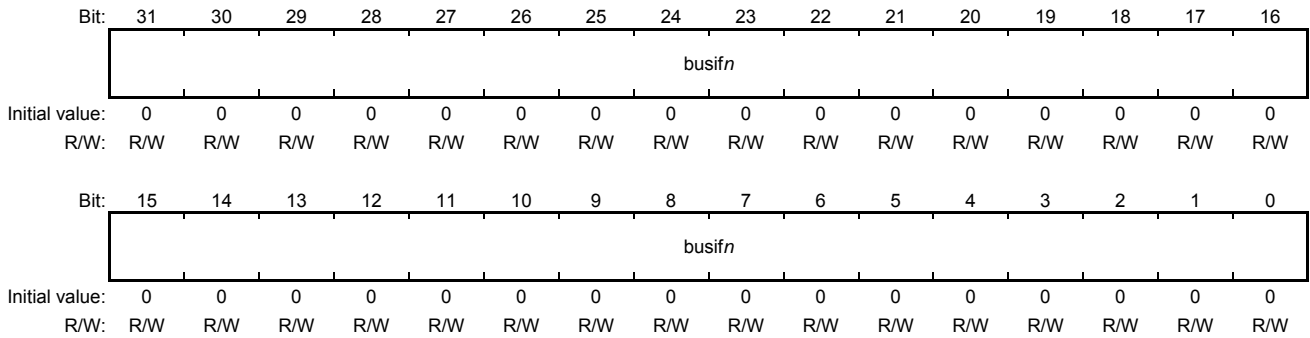
Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7	uf9-3_ie	0	R/W	buf_under_flow9-3_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
6	uf9-2_ie	0	R/W	buf_under_flow9-2_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
5	uf9-1_ie	0	R/W	buf_under_flow9-1_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
4	uf9-0_ie	0	R/W	buf_under_flow9-0_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
3 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

### 32.2.27 SSIn\_BUSIF Data Registers (SSIn\_BUSIF)

Note: n = 0-0 to 0-3, 1-0 to 1-3, 2-0 to 2-3, 3 to 8, or 9-0 to 9-3

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: SSIn\_BUSIF is a window register in which data is stored during data transfer via SSIn\_BUSIF. These registers are used for both transmission and reception.



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	busifn	H'00000000	R/W	These bits are used to hold the data during data transfer via SSIn_BUSIFn. This register is used for both transmission and reception. This register can only be written to during transmission and only be read from during reception.

## 32.3 SSIU Operation

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

### 32.3.1 Module Specifications

Table 32.3 shows the correspondences between the modules and functions.

**Table 32.3 Function Correspondences**

		External Interface	Format		
			Normal	TDM Extend Mode	TDM Split Mode
1	SSI0 SSI1 SSI2 SSI9	I2S	Supported	Not supported	Not supported
2	SSI0 SSI1 SSI2 SSI9	TDM	Supported	Supported	Supported
3	SSI0 SSI1 SSI2	I2S × 3 (multichannel)	Supported	Not supported	Not supported
4	SSI0 SSI1 SSI2 SSI9	I2S × 4 (multichannel)	Supported	Not supported	Not supported
5	SSI3 SSI4	I2S	Supported	Not supported	Not supported
6	SSI3 SSI4	TDM	Supported	Supported	Not supported
7	SSI5 SSI6 SSI7 SSI8	I2S	Supported	Not supported	Not supported
8	SSI5 SSI6 SSI7 SSI8	TDM	Not supported	Not supported	Not supported

### 32.3.2 Basic Configuration

Data transfer is performed between the SSIU and other audio modules or external memories via BUSIF connected to the audio local bus and the audio DMA bus. Figure 32.3 shows the data transfer of SSI0. As shown in Figure 32.3, SSI0\_1\_BUSIF, SSI0\_2\_BUSIF, and SSI0\_3\_BUSIF are not used. This basic configuration is also applied to SSI1, SSI2, and SSI9. Figure 32.4 shows the data transfer of SSI3, which is also applied to SSI4 to SSI8.

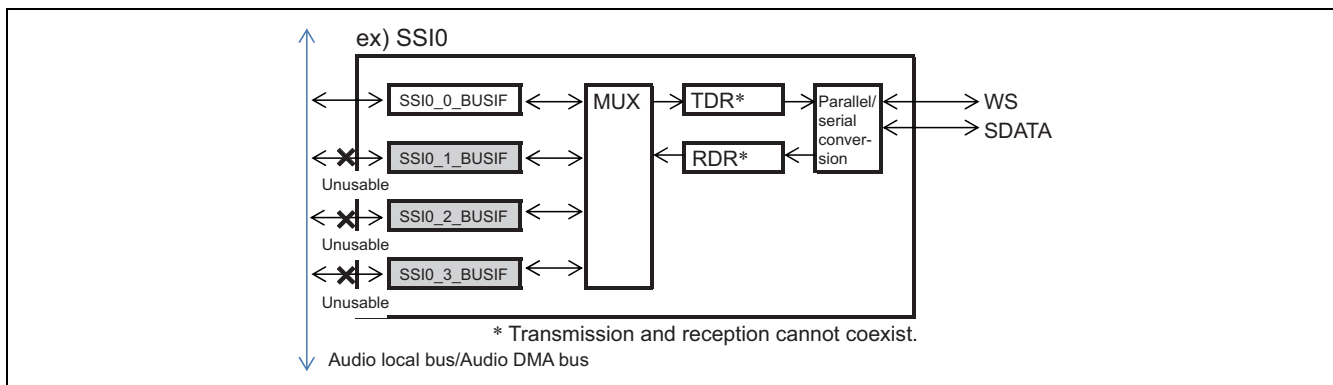


Figure 32.3 Basic Configuration (SSI0)

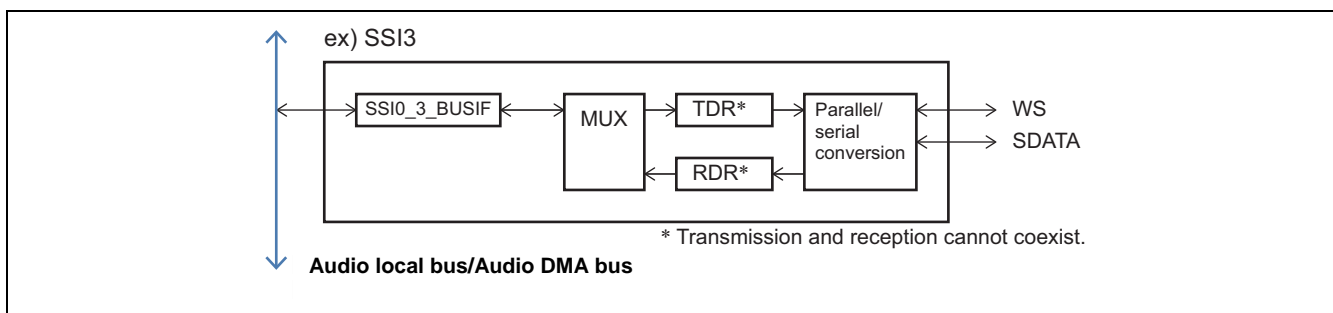
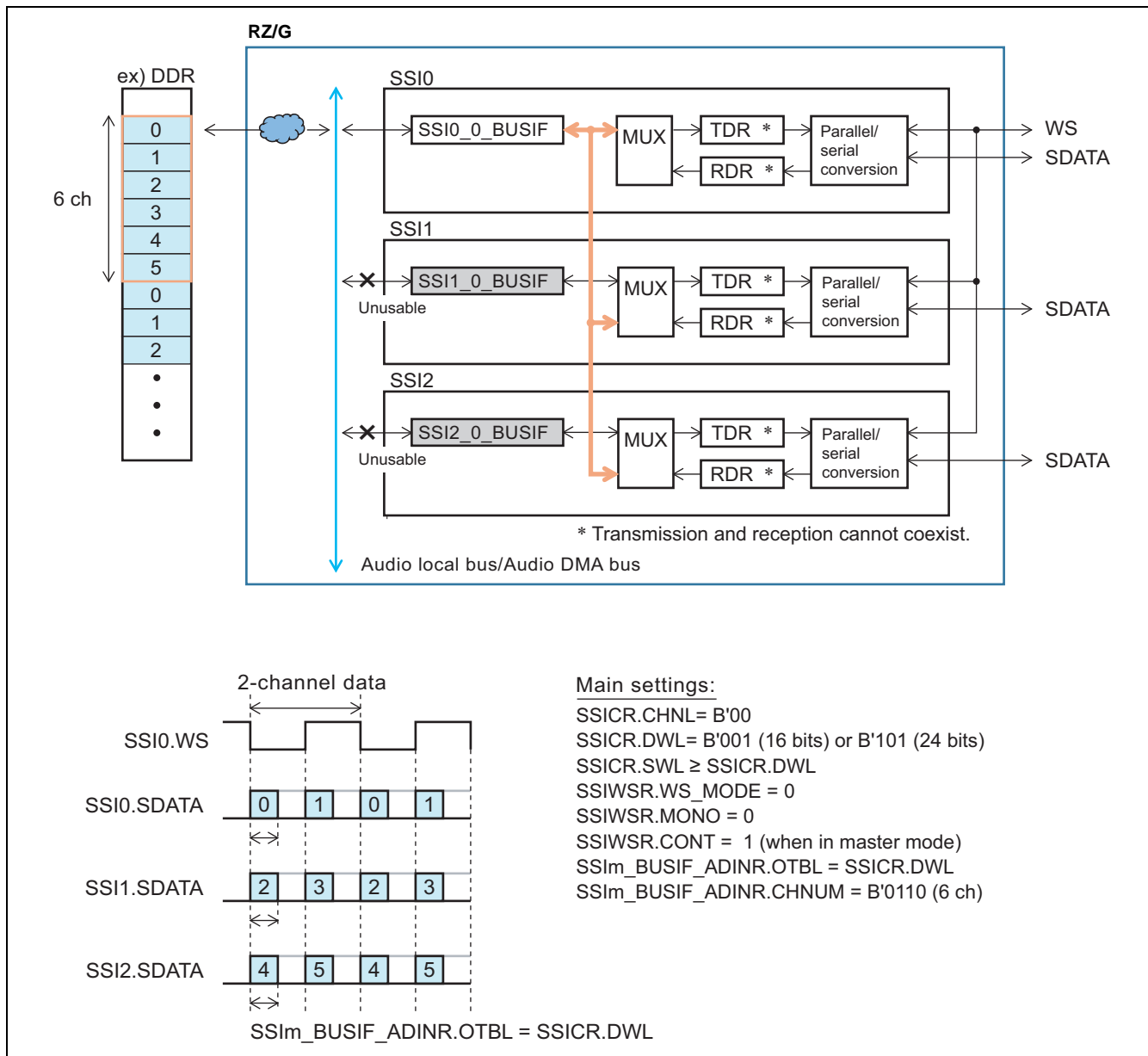


Figure 32.4 Basic Configuration (SSI3)

### 32.3.3 Configuration with Multiple SSI Modules

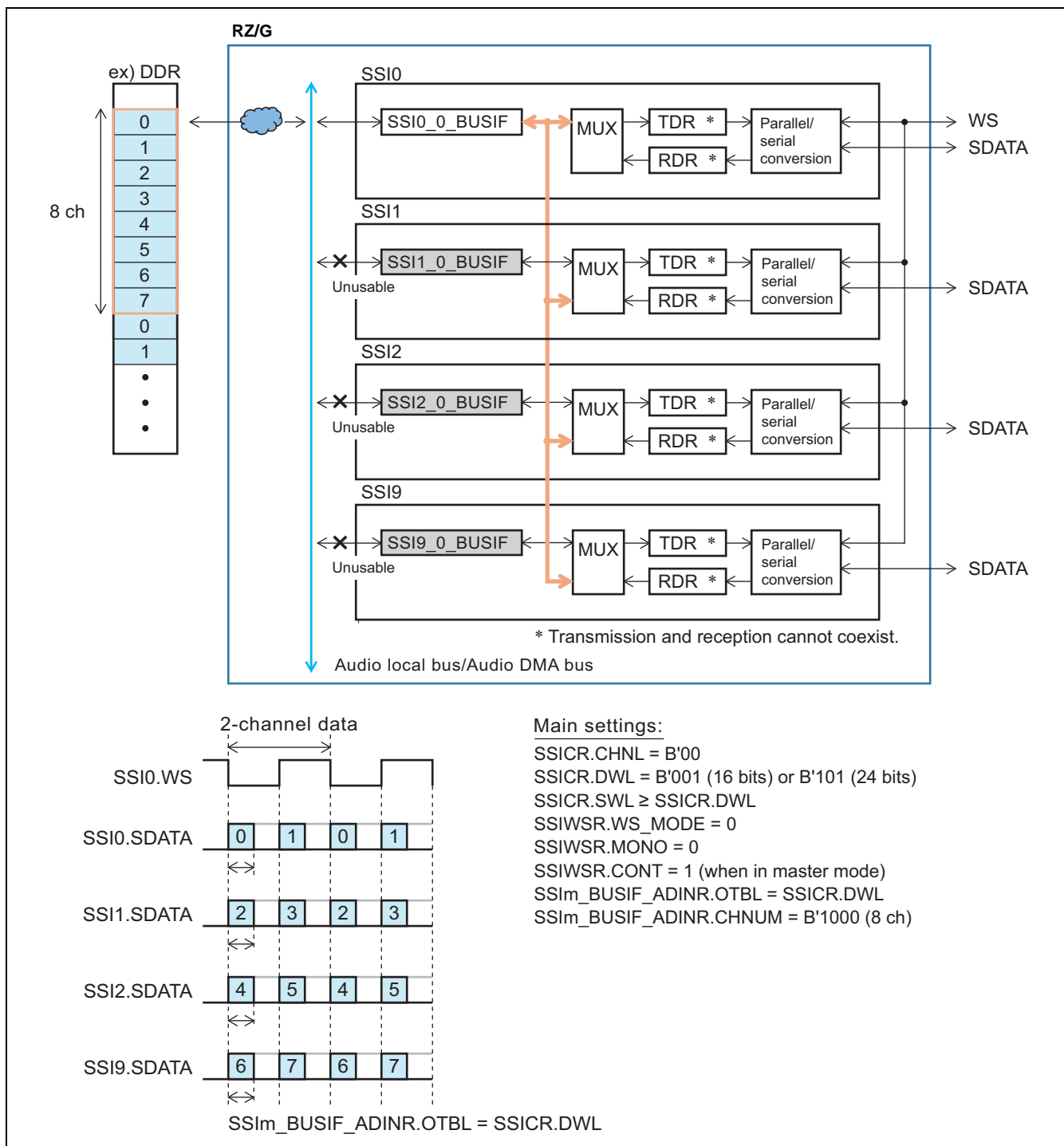
Multichannel data transfer can be performed by using multiple SSI modules. The available combination of modules is SSI0, SSI1, and SSI2 or SSI0, SSI1, SSI2, and SSI9.



**Figure 32.5 Multichannel Data Transfer (Using SSI0, SSI1 and SSI2)**

Note: When the above configuration is used, SSI0\_1\_BUSIF, SSI0\_2\_BUSIF, SSI0\_3\_BUSIF, all the BUSIFs of SSI1 and SSI2 cannot be used.



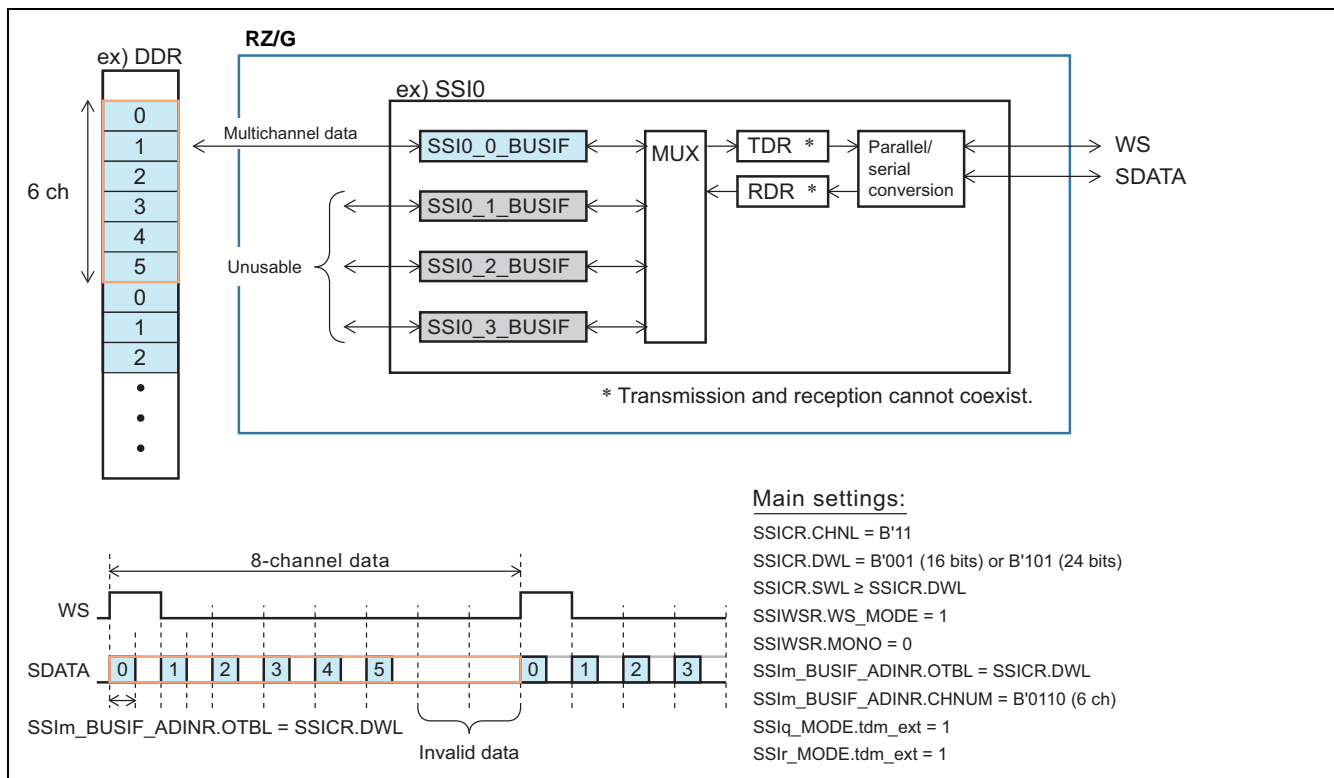


**Figure 32.6 Multichannel Data Transfer (Using SSI0, SSI1, SSI2 and SSI9)**

Note: When the above configuration is used, SSI0\_1\_BUSIF, SSI0\_2\_BUSIF, SSI0\_3\_BUSIF, all the BUSIFs of SSI1, SSI2, and SSI9 cannot be used.

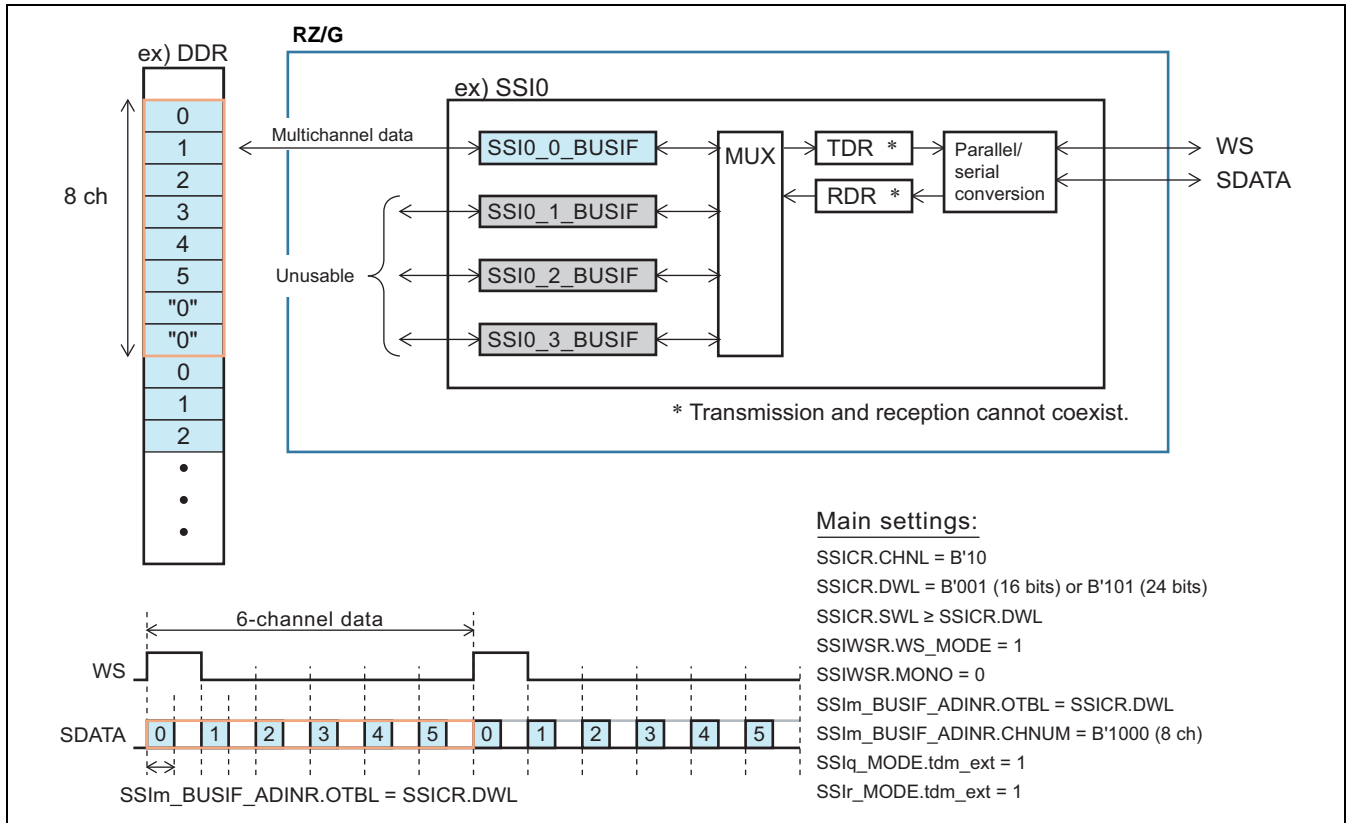
### 32.3.4 TDM Format Extension Function (TDM Extend Mode)

The TDM format extension function allows operation with 8-channel data in the serial bus and 6-channel data inside the RZ/G, or operation with 6-channel data in the serial bus and 8-channel data inside the RZ/G. This function is supported by SSI0, SSI1, SSI2, SSI3, SSI4, and SSI9.



**Figure 32.7 TDM Extend Mode Operation with 8-channel Data in Serial Bus and 6-channel Data Inside the RZ/G (SSI0)**

Note: When the above configuration is used, SSI0\_1\_BUSIF, SSI0\_2\_BUSIF, and SSI0\_3\_BUSIF cannot be used.



**Figure 32.8 TDM Extend Mode Operation with 6-channel Data in Serial Bus and 8-channel Data Inside the RZ/G (SSI0)**

Note: When the above configuration is used, SSI0\_1\_BUSIF, SSI0\_2\_BUSIF, and SSI0\_3\_BUSIF cannot be used.

### 32.3.5 TDM Format Split Function (TDM Split Mode)

The TDM format split function (TDM split mode) allows connecting four independent monaural or stereo data inside the RZ/G and outputting the data in the TDM format, and splitting TDM format input data into four independent monaural or stereo data and distributing the data inside the RZ/G. This function is supported by SSI0, SSI1, SSI2, and SSI9.

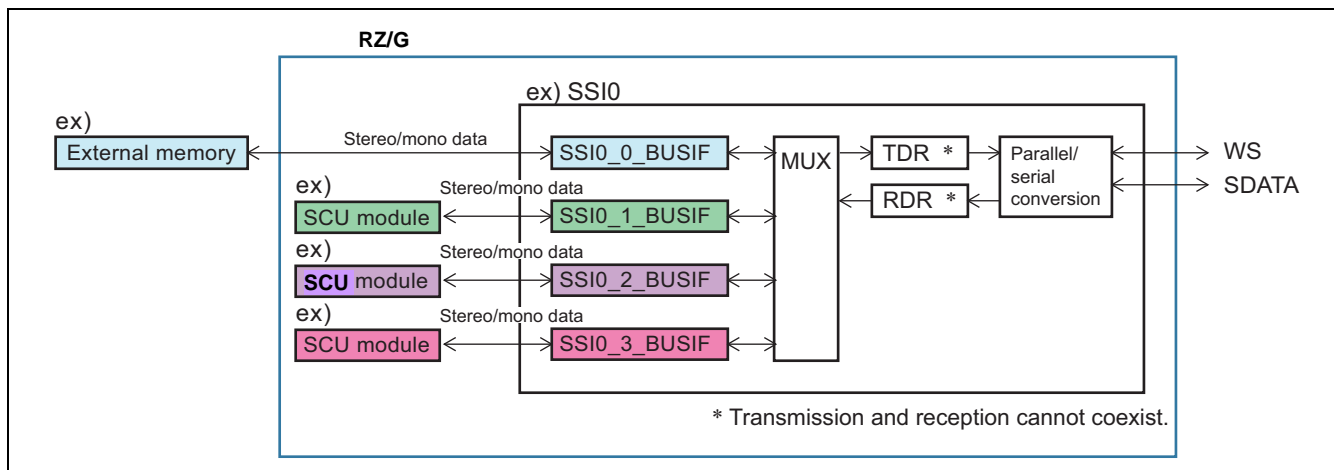


Figure 32.9 TDM Split Mode

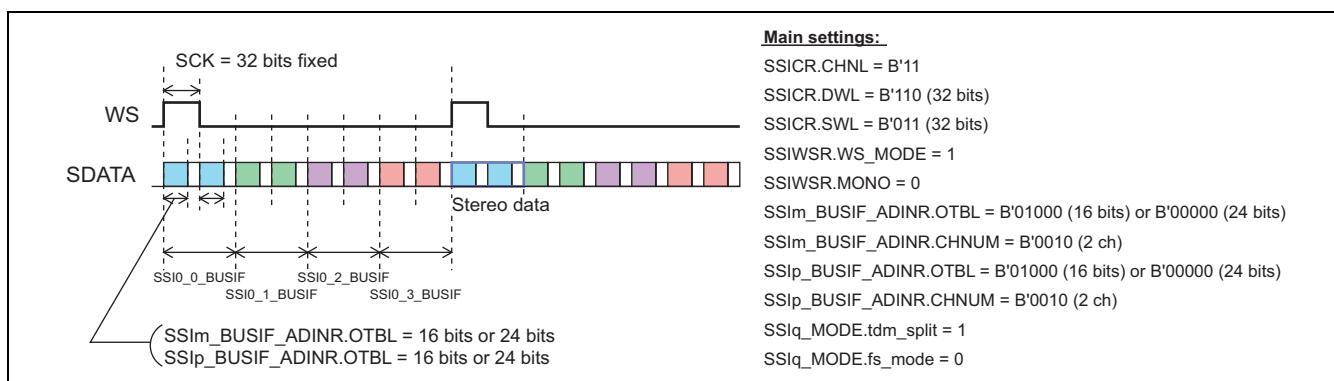
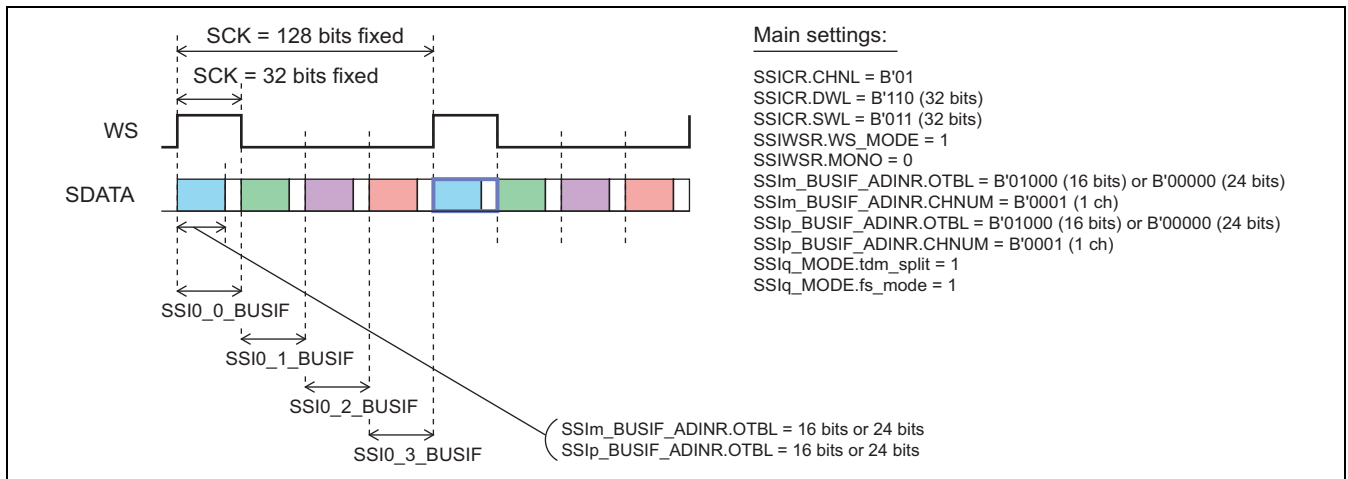


Figure 32.10 TDM Split Mode (Stereo x 4)

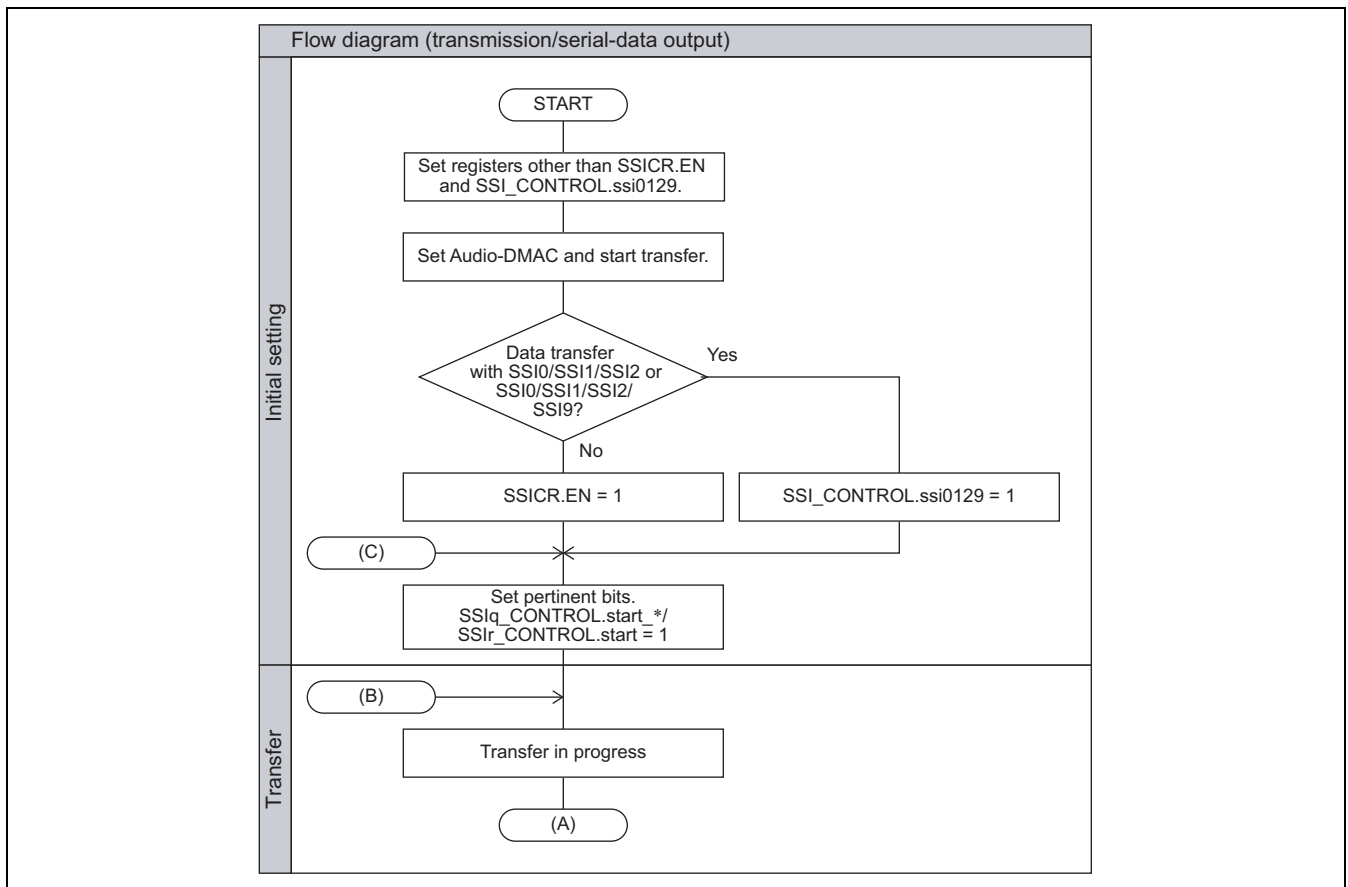


**Figure 32.11 TDM Split Mode (Monaural x 4)**

- Notes:
1. The SWL and DWL bits in SSICR should be fixed at 32-bit setting.
  2. Transmission and reception cannot coexist.
  3. Data input to BUSIFn 0 to 3 (n = 0, 1, 2, 3) should be operated synchronously with the SSI sampling frequency (WS signal cycle).

**32.3.6 Procedure of SSIU Transfer**

Figures 32.12 to 32.15 show the operation flow.



**Figure 32.12 Transmission (1)**

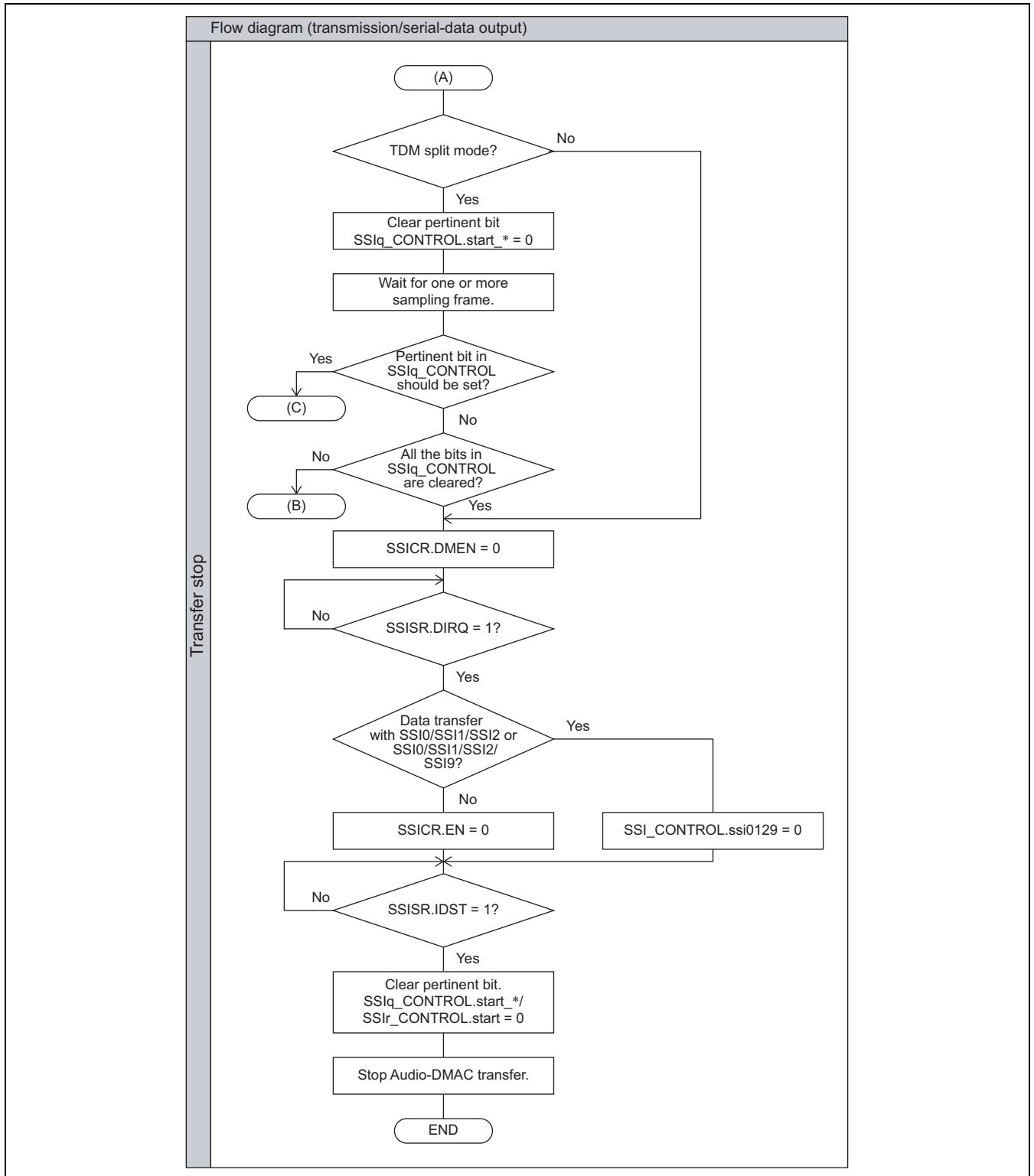


Figure 32.13 Transmission (2)

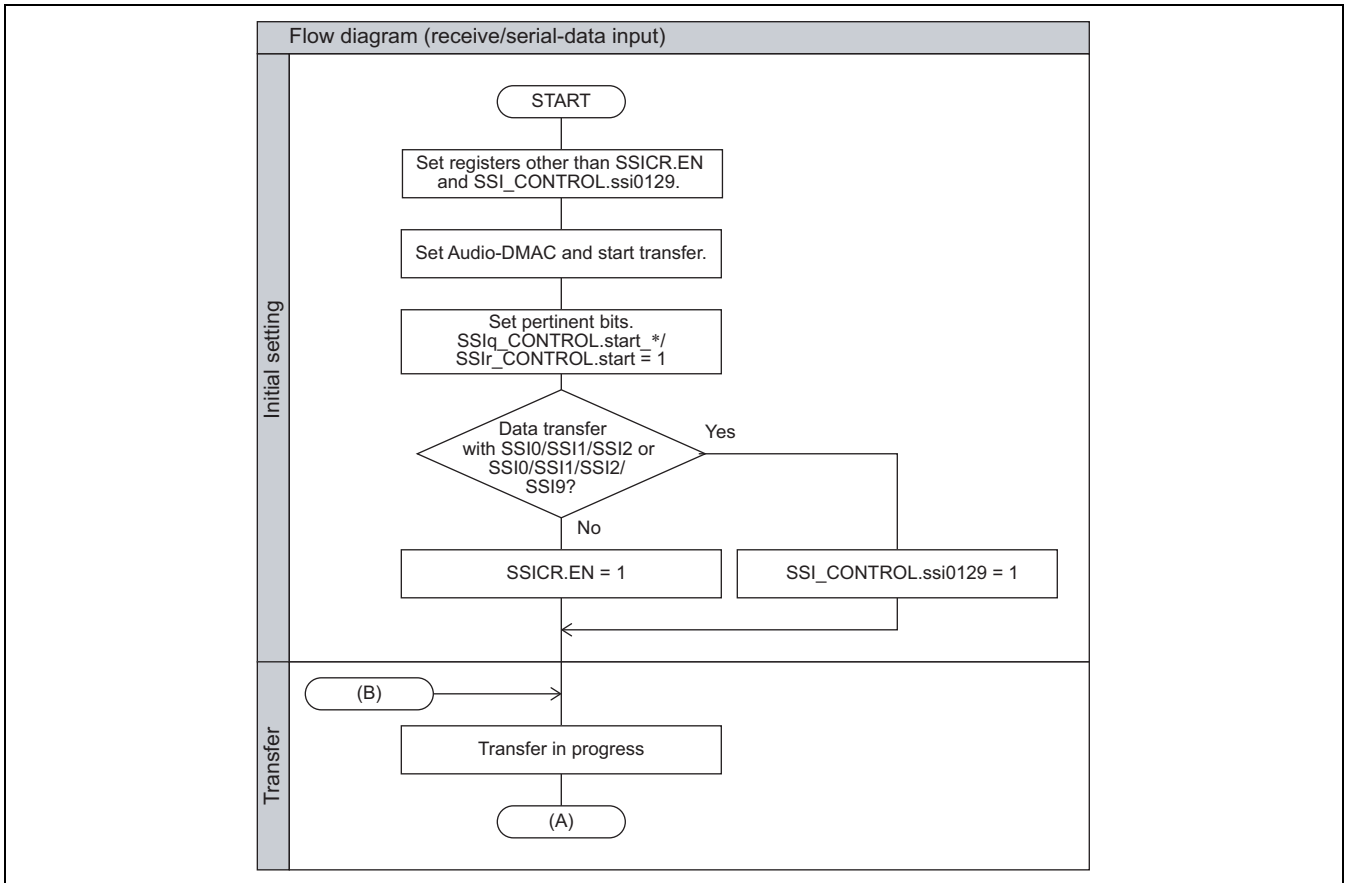


Figure 32.14 Reception (1)



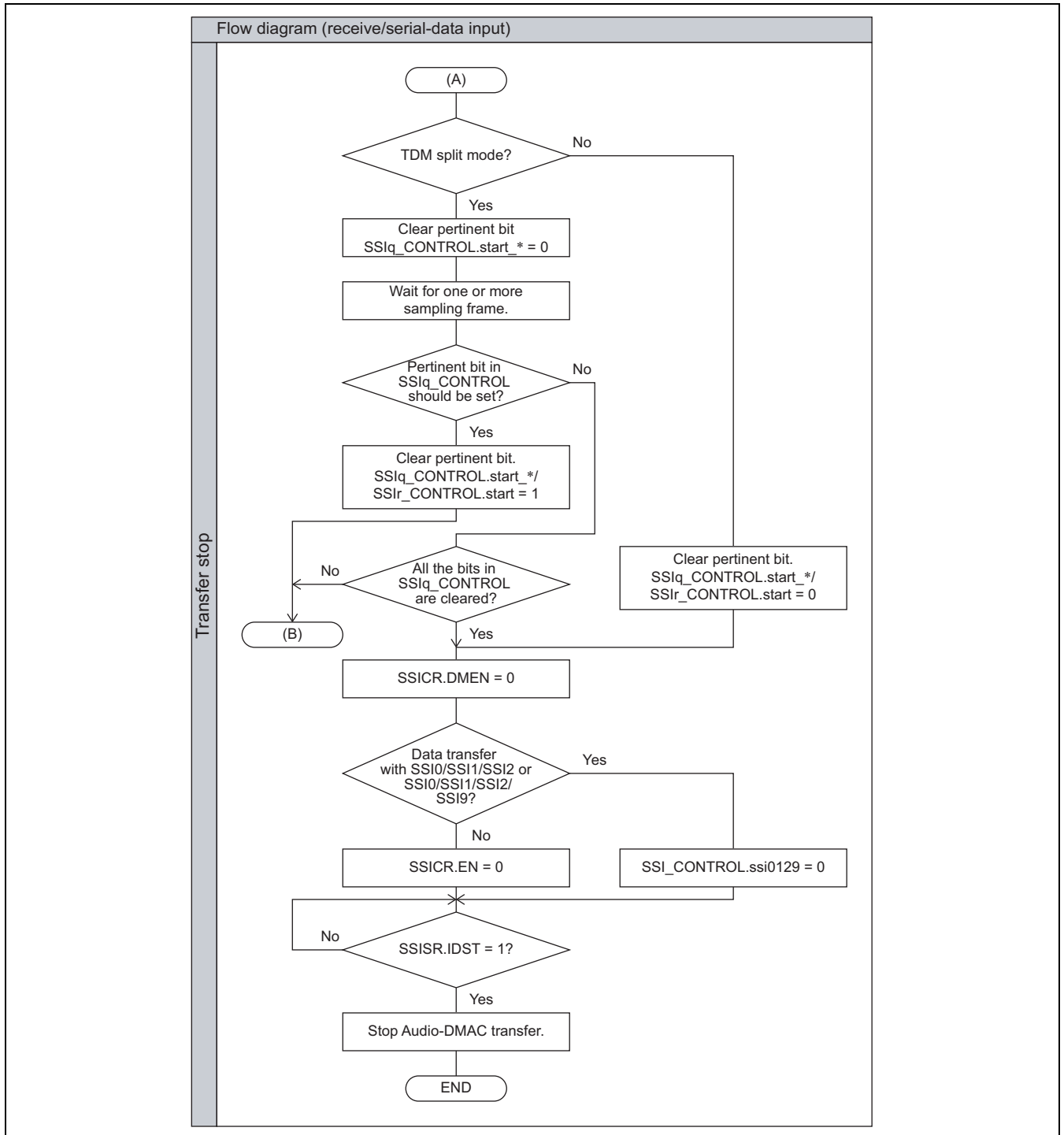
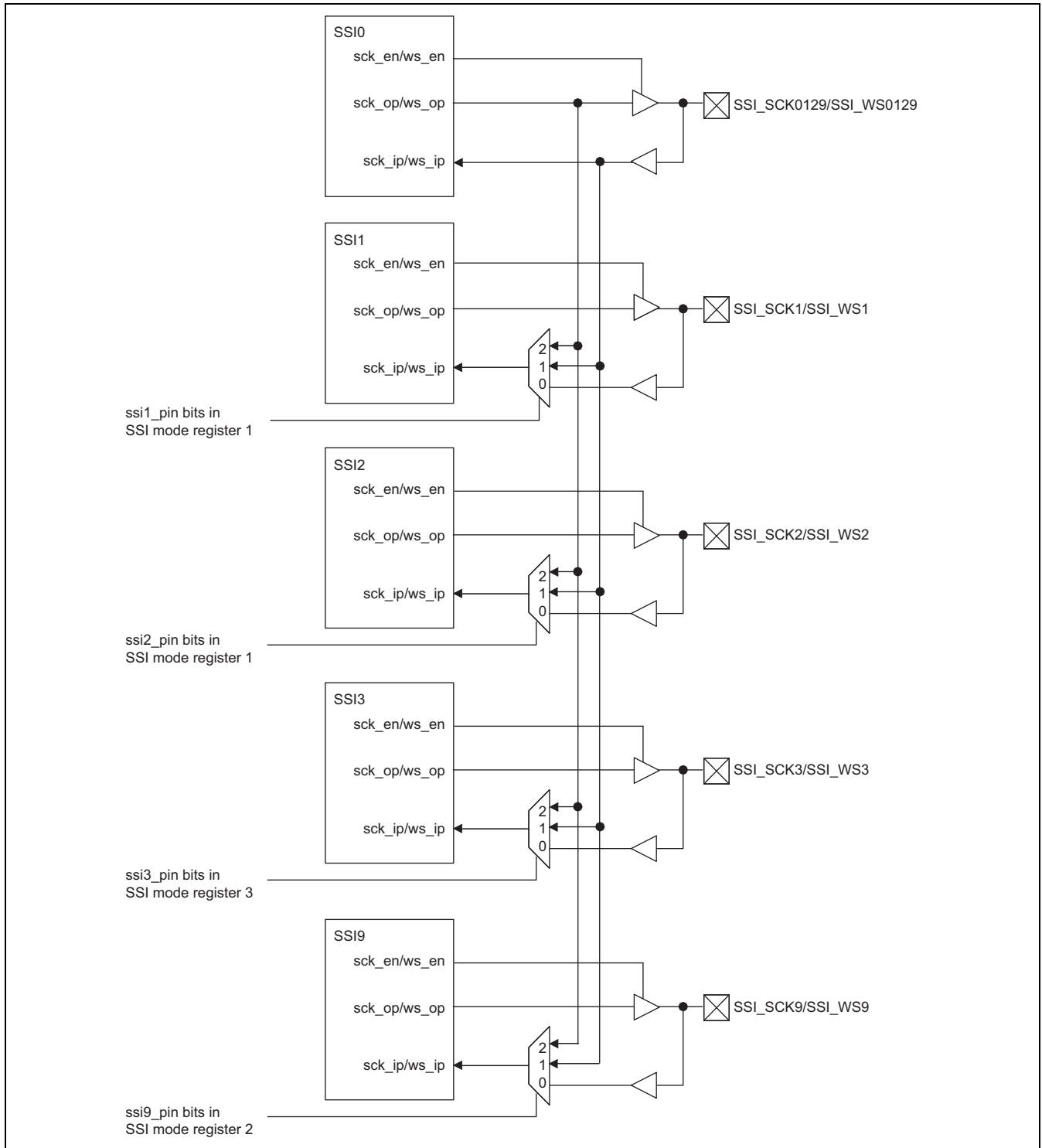


Figure 32.15 Reception (2)

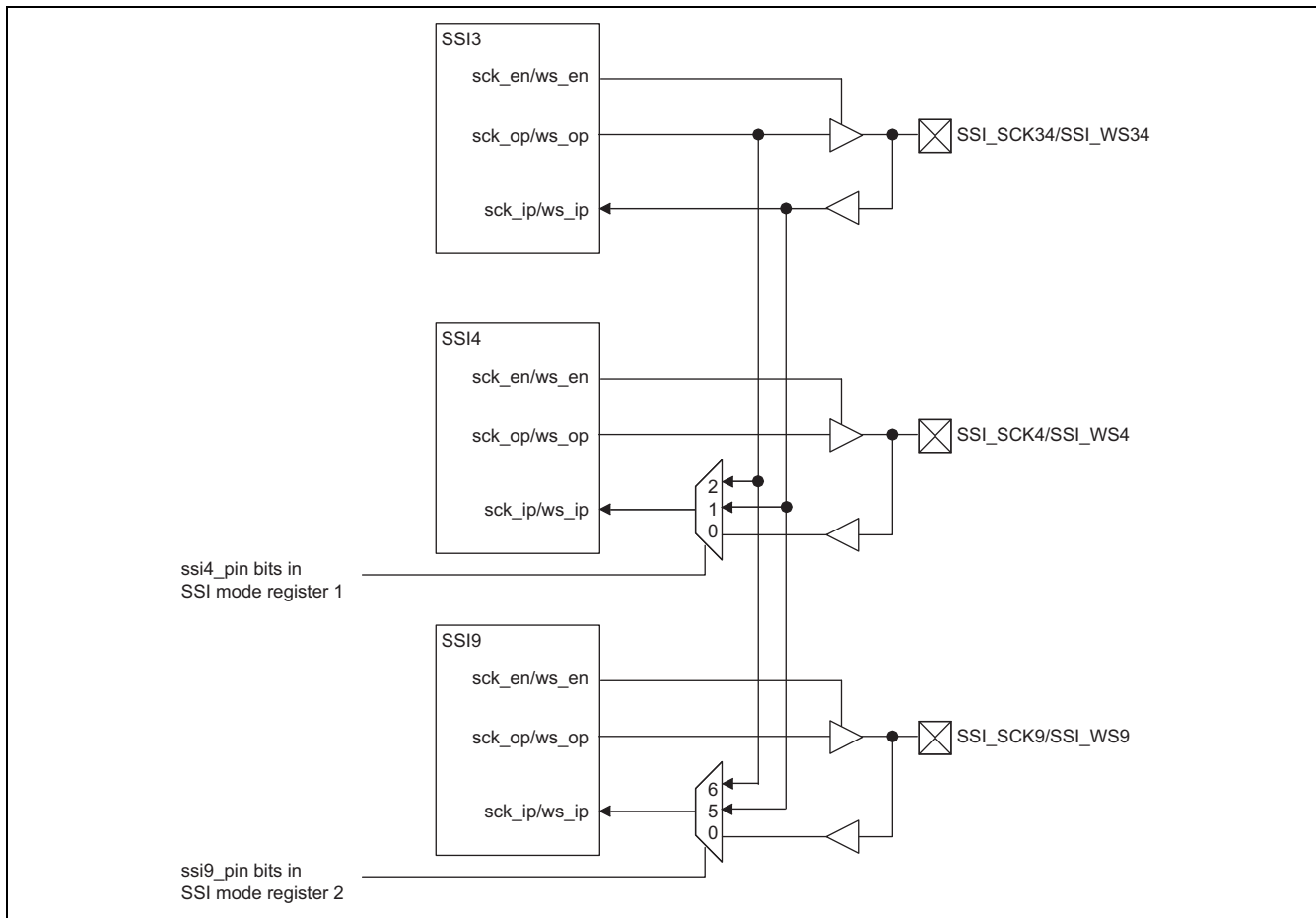
### 32.3.7 SSI Pin Connections

Multiple SSI modules (in combinations of SSI0, SSI1, SSI2, SSI3, and SSI9, SSI3, SSI4, and SSI9, and SSI7 and SSI8) can operate in synchronization with sharing of the same SSI\_SCK and SSI\_WS signals. Figures 32.16 to 32.18 show how to connect the pins for each combination of SSIs.

In the case of the combination of SSI0, SSI1, SSI2, SSI3, and SSI9, SSI0 as the master should start transfer first thus allowing output on SSI\_WS0129 and SSI\_SCK0129, after which SSI1, SSI2, SSI3, and SSI9 as the slaves should be used. If the master-side transfer is stopped by setting the CONT bit in SSIWSR to 0, the slave-side SSI1, SSI2, SSI3, and SSI9 should be stopped because output through SSI\_WS0129 is not possible. This also applies to the master and slaves in the combination of SSI3, SSI4, and SSI9, and to the master and slave in the combination of SSI7 and SSI8.

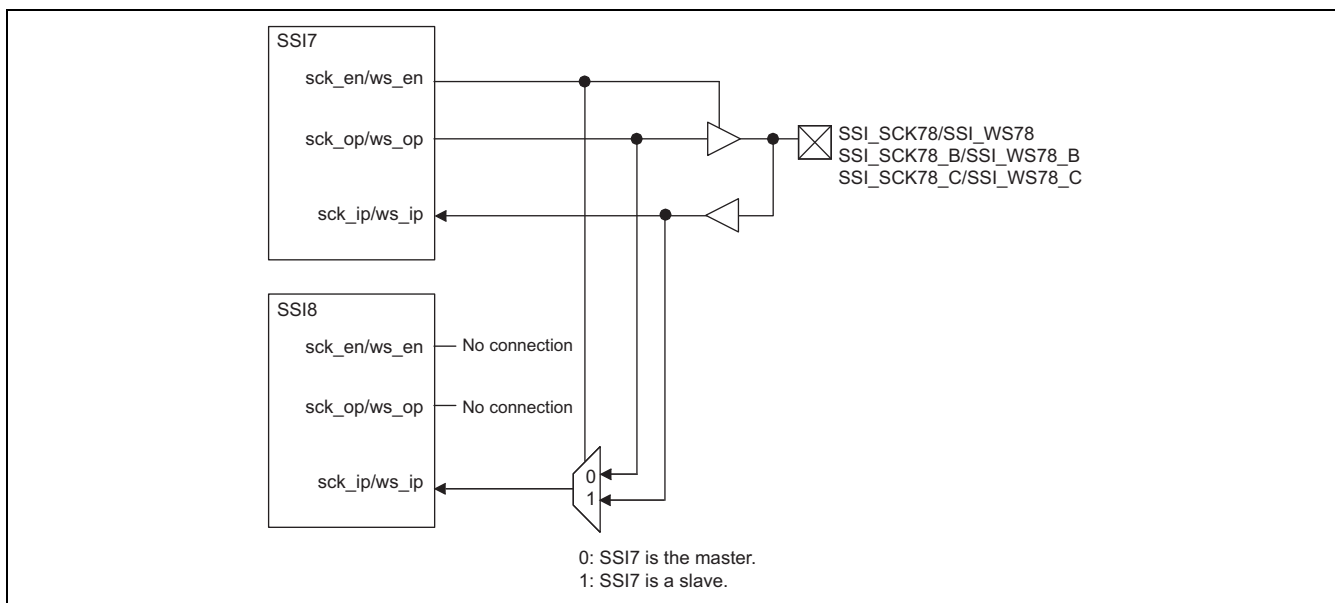


**Figure 32.16 Pin Connections for Combination of SSI0, SSI1, SSI2, SSI3, and SSI9**



**Figure 32.17 Pin Connections for Combination of SSI3, SSI4, and SSI9**

Note: The above configuration is prohibited if SSI0 SCK/WS is selected for SSI3 as shown in Figure 32.16.



**Figure 32.18 Pin Connections for Combination of SSI7 and SSI8**

## 32.4 Usage Note

RZ/G1H	RZ/G1N
RZ/G1M	RZ/G1E

### 32.4.1 Note on Transfer

If an underflow or overflow occurs, stop the transfer and restart it.

Do not stop serial clock (SCK) and word select (WS) signals during data transfer. Confirm that SSISR.IDST = 1 before stopping SCK and WS signals.

## 32A. Serial Sound Interface (SSI)

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

The serial sound interface (hereinafter referred to as the "SSI") is a transceiver module designed to send or receive audio data interfacing with a variety of devices offering I2S format. It also supports multi-channel mode in addition to other common formats.

### 32A.1 Features

The SSI has the following features:

- Number of channels: Maximum of four (when a multichannel format is specified)
- Operating mode: Non-compressed mode  
The non-compressed mode supports serial audio streams divided by channels.
- The SSI module can serve as both a transmitter and a receiver.
- Asynchronous transfer takes place between the data buffer and the shift register.
- Only the MSB first data alignment is supported.
- A value as the dividing ratio for the clock used by the serial bus interface is selectable.
- Controlling of data transmission or reception with DMAC or interrupt requests is possible.
- TDM format is supported.
- TDM format operation is performed at a 44.1- or 48-kHz sampling rate.
- The WS continue function by which operation can be performed without stopping WS signal is supported.
- Monaural mode (8 bits or 16 bits) is supported.
- In monaural mode, WS signal pulse width can be changed (short or long frame).
- If the sampling clock frequency is switched during transfer, it will be notified of the CPU with interrupts (a function to detect switching frequency).

Figure 32A.1 shows a block diagram of a single SSI module.

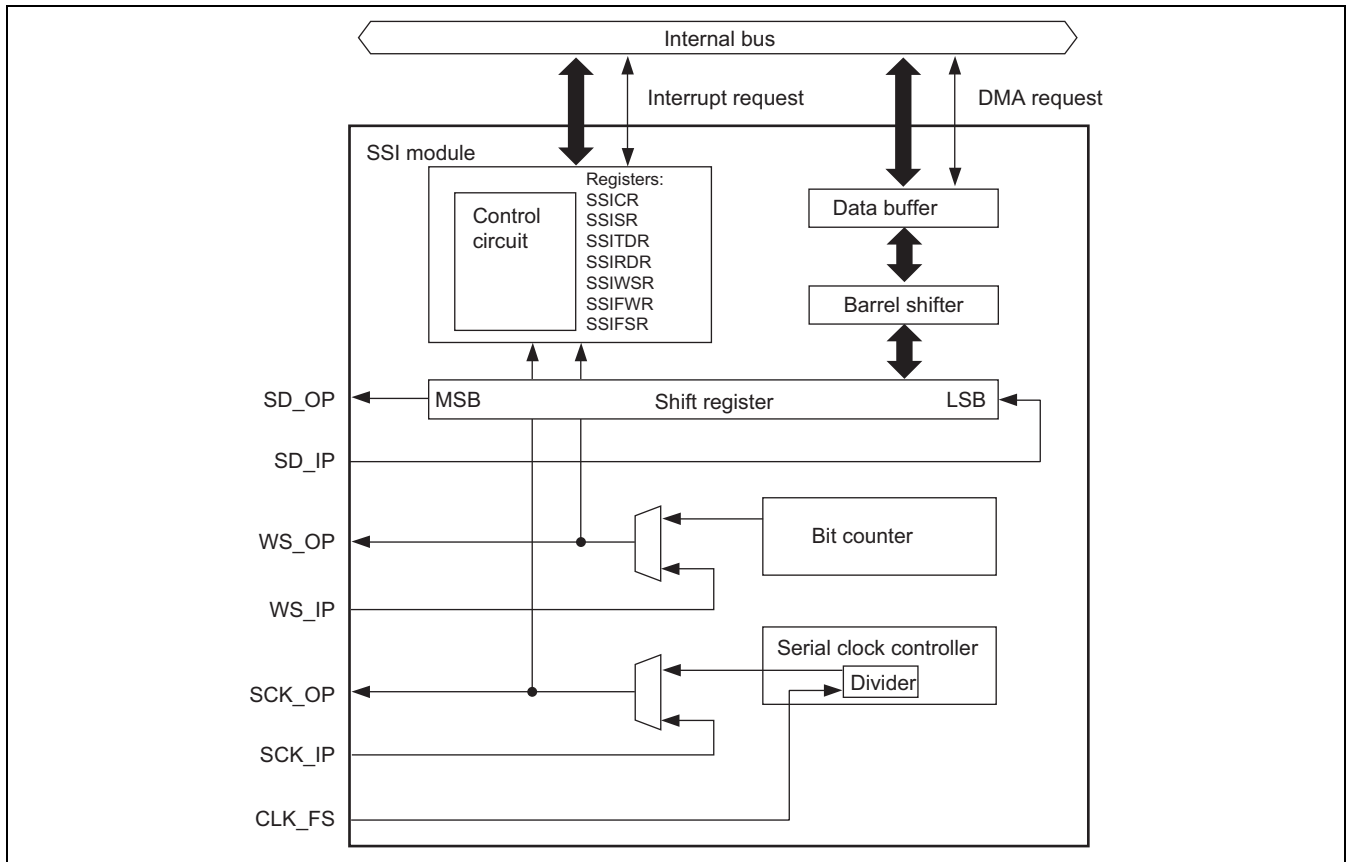


Figure 32A.1 Block Diagram of SSI

## 32A.2 Register Descriptions

The SSI has the following registers. Note that the module numbers are basically omitted from the register names in the text.

**Table 32A.1 Register Descriptions**

Module	Register Name	Abbreviation	R/W	Address	Access Size	RZ/G Series Products			
						RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
0	Control register 0	SSICR0	R/W	H'EC54 1000	32	√	√	√	√
	Status register 0	SSISR0	R/W*1	H'EC54 1004	32	√	√	√	√
	Transmit data register 0	SSITDR0	R/W	H'EC54 1008/ H'EC24 1008*3	32	√	√	√	√
	Receive data register 0	SSIRDR0	R	H'EC54 100C/ H'EC24 100C*3	32	√	√	√	√
	WS mode register 0	SSIWSR0	R/W	H'EC54 1020	32	√	√	√	√
	FS mode register 0	SSIFMR0	R/W	H'EC54 1024	32	√	√	√	√
	FS status register 0	SSIFSR0	R/W*2	H'EC54 1028	32	√	√	√	√
1	Control register 1	SSICR1	R/W	H'EC54 1040	32	√	√	√	√
	Status register 1	SSISR1	R/W*1	H'EC54 1044	32	√	√	√	√
	Transmit data register 1	SSITDR1	R/W	H'EC54 1048/ H'EC24 1048*3	32	√	√	√	√
	Receive data register 1	SSIRDR1	R	H'EC54 104C/ H'EC24 104C*3	32	√	√	√	√
	WS mode register 1	SSIWSR1	R/W	H'EC54 1060	32	√	√	√	√
	FS mode register 1	SSIFMR0	R/W	H'EC54 1064	32	√	√	√	√
	FS status register 1	SSIFSR0	R/W*2	H'EC54 1068	32	√	√	√	√
2	Control register 2	SSICR2	R/W	H'EC54 1080	32	√	√	√	√
	Status register 2	SSISR2	R/W*1	H'EC54 1084	32	√	√	√	√
	Transmit data register 2	SSITDR2	R/W	H'EC54 1088/ H'EC24 1088*3	32	√	√	√	√
	Receive data register 2	SSIRDR2	R	H'EC54 108C/ H'EC24 108C*3	32	√	√	√	√
	WS mode register 2	SSIWSR2	R/W	H'EC54 10A0	32	√	√	√	√
	FS mode register 2	SSIFMR2	R/W	H'EC54 10A4	32	√	√	√	√
	FS status register 2	SSIFSR2	R/W*2	H'EC54 10A8	32	√	√	√	√
3	Control register 3	SSICR3	R/W	H'EC54 10C0	32	√	√	√	√
	Status register 3	SSISR3	R/W*1	H'EC54 10C4	32	√	√	√	√
	Transmit data register 3	SSITDR3	R/W	H'EC54 10C8/ H'EC24 10C8*3	32	√	√	√	√
	Receive data register 3	SSIRDR3	R	H'EC54 10CC/ H'EC24 10CC*3	32	√	√	√	√
	WS mode register 3	SSIWSR3	R/W	H'EC54 10E0	32	√	√	√	√
	FS mode register 3	SSIFMR3	R/W	H'EC54 10E4	32	√	√	√	√
	FS status register 3	SSIFSR3	R/W*2	H'EC54 10E8	32	√	√	√	√



Module	Register Name	Abbreviation	R/W	Address	Access Size	RZ/G Series Products			
						RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
4	Control register 4	SSICR4	R/W	H'EC54 1100	32	√	√	√	√
	Status register 4	SSISR4	R/W*1	H'EC54 1104	32	√	√	√	√
	Transmit data register 4	SSITDR4	R/W	H'EC54 1108/ H'EC24 1108*3	32	√	√	√	√
	Receive data register 4	SSIRDR4	R	H'EC54 110C/ H'EC24 110C*3	32	√	√	√	√
	WS mode register 4	SSIWSR4	R/W	H'EC54 1120	32	√	√	√	√
	FS mode register 4	SSIFMR4	R/W	H'EC54 1124	32	√	√	√	√
	FS status register 4	SSIFSR4	R/W*2	H'EC54 1128	32	√	√	√	√
5	Control register 5	SSICR5	R/W	H'EC54 1140	32	√	√	√	√
	Status register 5	SSISR5	R/W*1	H'EC54 1144	32	√	√	√	√
	Transmit data register 5	SSITDR5	R/W	H'EC54 1148/ H'EC24 1148*3	32	√	√	√	√
	Receive data register 5	SSIRDR5	R	H'EC54 114C/ H'EC24 114C*3	32	√	√	√	√
	WS mode register 5	SSIWSR5	R/W	H'EC54 1160	32	√	√	√	√
	FS mode register 5	SSIFMR5	R/W	H'EC54 1164	32	√	√	√	√
	FS status register 5	SSIFSR5	R/W*2	H'EC54 1168	32	√	√	√	√
6	Control register 6	SSICR6	R/W	H'EC54 1180	32	√	√	√	√
	Status register 6	SSISR6	R/W*1	H'EC54 1184	32	√	√	√	√
	Transmit data register 6	SSITDR6	R/W	H'EC54 1188/ H'EC24 1188*3	32	√	√	√	√
	Receive data register 6	SSIRDR6	R	H'EC54 118C/ H'EC24 118C*3	32	√	√	√	√
	WS mode register 6	SSIWSR6	R/W	H'EC54 11A0	32	√	√	√	√
	FS mode register 6	SSIFMR6	R/W	H'EC54 11A4	32	√	√	√	√
	FS status register 6	SSIFSR6	R/W*2	H'EC54 11A8	32	√	√	√	√
7	Control register 7	SSICR7	R/W	H'EC54 11C0	32	√	√	√	√
	Status register 7	SSISR7	R/W*1	H'EC54 11C4	32	√	√	√	√
	Transmit data register 7	SSITDR7	R/W	H'EC54 11C8/ H'EC24 11C8*3	32	√	√	√	√
	Receive data register 7	SSIRDR7	R	H'EC54 11CC/ H'EC24 11CC*3	32	√	√	√	√
	WS mode register 7	SSIWSR7	R/W	H'EC54 11E0	32	√	√	√	√
	FS mode register 7	SSIFMR7	R/W	H'EC54 11E4	32	√	√	√	√
	FS status register 7	SSIFSR7	R/W*2	H'EC54 11E8	32	√	√	√	√

Module	Register Name	Abbreviation	R/W	Address	Access Size	RZ/G Series Products			
						RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
8	Control register 8	SSICR8	R/W	H'EC54 1200	32	√	√	√	√
	Status register 8	SSISR8	R/W* <sup>1</sup>	H'EC54 1204	32	√	√	√	√
	Transmit data register 8	SSITDR8	R/W	H'EC54 1208/ H'EC24 1208* <sup>3</sup>	32	√	√	√	√
	Receive data register 8	SSIRDR8	R	H'EC54 120C/ H'EC24 120C* <sup>3</sup>	32	√	√	√	√
	WS mode register 8	SSIWSR8	R/W	H'EC54 1220	32	√	√	√	√
	FS mode register 8	SSIFMR8	R/W	H'EC54 1224	32	√	√	√	√
	FS status register 8	SSIFSR8	R/W* <sup>2</sup>	H'EC54 1228	32	√	√	√	√
9	Control register 9	SSICR9	R/W	H'EC54 1240	32	√	√	√	√
	Status register 9	SSISR9	R/W* <sup>1</sup>	H'EC54 1244	32	√	√	√	√
	Transmit data register 9	SSITDR9	R/W	H'EC54 1248/ H'EC24 1248* <sup>3</sup>	32	√	√	√	√
	Receive data register 9	SSIRDR9	R	H'EC54 124C/ H'EC24 124C* <sup>3</sup>	32	√	√	√	√
	WS mode register 9	SSIWSR9	R/W	H'EC54 1260	32	√	√	√	√
	FS mode register 9	SSIFMR9	R/W	H'EC54 1264	32	√	√	√	√
	FS status register 9	SSIFSR9	R/W* <sup>2</sup>	H'EC54 1268	32	√	√	√	√

Notes: Do not write to any addresses other than listed above. Operations cannot be guaranteed if writing is attempted. Values read from addresses other than those listed above are undefined.

1. For this register, bits 26 and 27 are readable/writable bits, although the others are read-only bits. For details, refer to section 32A.2.2, Status Register (SSISR<sub>n</sub>) (n = 0 to 9).
2. For this register, bits 14 and 15 are readable/writable bits, although the others are read-only bits. For details, refer to section 32A.2.7, FS Status Register (SSIFSR<sub>n</sub>) (n = 0 to 9).
3. H'EC54 1XXX and H'EC24 1XXX are used with PIO access and audio-DMAC, respectively.

[Legend for Register Descriptions]

Initial value: Register value after a reset

—: Undefined value

R/W: Readable/writable. The written value can be read.

R/WC0: Readable/writable. Writing 0 initializes the bit. Writing 1 is ignored.

R: Read-only. The write value should always be 0.

### 32A.2.1 Control Register (SSICRn) (n = 0 to 9)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SSICR is a readable/writable 32-bit register that controls the IRQ, selects the polarity status, and sets operating mode.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	FORCE	—	FIEN	DMEN	UIEN	OIEN	IIEN	DIEN	CHNL[1:0]		DWL[2:0]		SWL[2:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SCKD	SWSD	SCKP	SWSP	SPDP	SDTA	PDTA	DEL	—	CKDV[2:0]		MUEN	—	TRMD	EN	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	FORCE	0	R/W	Fixed The bit should always be set to 1.
30	—	0	R	Reserved The read value is 0. The write value should always be 0.
29	FIEN	0	R/W	Frequency Switching Detection Interrupt Enable 0: Frequency switching detection interrupt is disabled. 1: Frequency switching detection interrupt is enabled.
28	DMEN	0	R/W	DMA Enable Enables or disables the DMA request. 0: DMA request is disabled. 1: DMA request is enabled.
27	UIEN	0	R/W	Underflow Interrupt Enable 0: Underflow interrupt is disabled. 1: Underflow Interrupt is enabled.
26	OIEN	0	R/W	Overflow Interrupt Enable 0: Overflow interrupt is disabled. 1: Overflow interrupt is enabled.
25	IIEN	0	R/W	Idle Mode Interrupt Enable 0: Idle mode interrupt is disabled. 1: Idle mode interrupt is enabled.
24	DIEN	0	R/W	Data Interrupt Enable 0: Data interrupt is disabled. 1: Data interrupt is enabled.

Bit	Bit Name	Initial Value	R/W	Description
23, 22	CHNL[1:0]	00	R/W	<p><b>Channels</b></p> <p>These bits set the number of channels in each system word.</p> <p>When the stereo format or multi-channel format is used (<math>WS\_MODE = 0</math>, <math>MONO = 0</math>, and <math>WIDTH = B'00000</math> in the WS mode register):</p> <p>00: A system word has one channel.  01: A system word has two channels.  10: A system word has three channels.  11: A system word has four channels.</p> <p>When the TDM format is used (<math>WS\_MODE = 1</math>, <math>MONO = 0</math>, and <math>WIDTH = B'00000</math> in the WS mode register):</p> <p>00: Setting prohibited  01: A TDM frame consists of four system words.  10: A TDM frame consists of six system words.  11: A TDM frame consists of eight system words.</p> <p>When the monaural format is used (<math>WS\_MODE = 1</math>, <math>MONO = 1</math>, and <math>WIDTH = B'00001</math> to <math>B'11111</math> in the WS mode register):</p> <p>00: A monaural frame consists of one system word.  01: Setting prohibited  10: Setting prohibited  11: Setting prohibited</p>
21 to 19	DWL[2:0]	000	R/W	<p><b>Data Word Length</b></p> <p>These bits set the number of bits in a data word.</p> <p>When the stereo format or multi-channel format (<math>WS\_MODE = 0</math>, <math>MONO = 0</math>, and <math>WIDTH = B'00000</math> in the WS mode register) or TDM format (<math>WS\_MODE = 1</math>, <math>MONO = 0</math>, and <math>WIDTH = B'00000</math> in the WS mode register) is used:</p> <p>000: 8 bits  001: 16 bits  010: 18 bits  011: 20 bits  100: 22 bits  101: 24 bits  110: 32 bits  111: Setting prohibited</p> <p>When the monaural format is used (<math>WS\_MODE = 1</math>, <math>MONO = 1</math>, and <math>WIDTH = B'00001</math> to <math>B'11111</math> in the WS mode register):</p> <p>000: 8 bits  001: 16 bits  Other than above: Setting prohibited</p>

Bit	Bit Name	Initial Value	R/W	Description
18 to 16	SWL[2:0]	000	R/W	<p>System Word Length</p> <p>These bits set the number of bits in a system word.</p> <p>When the stereo format or multi-channel format (WS_MODE = 0, MONO = 0, and WIDTH = B'00000 in the WS mode register) or TDM format (WS_MODE = 1, MONO = 0, and WIDTH = B'00000 in the WS mode register) is used:</p> <p>000: 8 bits            001: 16 bits            010: 24 bits            011: 32 bits            100: 48 bits            101: 64 bits            110: 128 bits            111: 256 bits</p> <p>When the monaural format is used (WS_MODE = 1, MONO = 1, and WIDTH = B'00001 to B'11111 in the WS mode register):</p> <p>000: 16 bits            001: 32 bits            010: 48 bits            011: 64 bits            100: 96 bits            101: 128 bits            110: 256 bits            111: 512 bits</p>
15	SCKD	0	R/W	<p>Serial Bit Clock Direction</p> <p>0: Serial bit clock is input, slave mode.            1: Serial bit clock is output, master mode.</p> <p>Note: (SCKD, SWSD) = (0,0) or (1,1) can be set to SSI0 to SSI7 and SSI9. To SSI8, only (SCKD, SWSD) = (0,0) can be set. Other settings are prohibited.</p>
14	SWSD	0	R/W	<p>Serial WS Direction</p> <p>0: Serial word select is input, slave mode.            1: Serial word select is output, master mode.</p> <p>Note: (SCKD, SWSD) = (0,0) or (1,1) can be set to SSI0 to SSI7 and SSI9. To SSI8, only (SCKD, SWSD) = (0,0) can be set. Other settings are prohibited.</p>

Bit	Bit Name	Initial Value	R/W	Description															
13	SCKP	0	R/W	<p>Serial Bit Clock Polarity</p> <p>0: SSI_WS and SSI_SDATA change at the SSI_SCK falling edge (sampled at the SCK rising edge).</p> <p>1: SSI_WS and SSI_SDATA change at the SSI_SCK rising edge (sampled at the SCK falling edge).</p> <table border="1"> <thead> <tr> <th></th> <th>SCKP = 0</th> <th>SCKP = 1</th> </tr> </thead> <tbody> <tr> <td>SSI_SDATA input sampling timing at the time of reception (TRMD = 0)</td> <td>SSI_SCK rising edge</td> <td>SSI_SCK falling edge</td> </tr> <tr> <td>SSI_SDATA output change timing at the time of transmission (TRMD = 1)</td> <td>SSI_SCK falling edge</td> <td>SSI_SCK rising edge</td> </tr> <tr> <td>SSI_WS input sampling timing at the time of slave mode (SWSD = 0)</td> <td>SSI_SCK rising edge</td> <td>SSI_SCK falling edge</td> </tr> <tr> <td>SSI_WS output change timing at the time of master mode (SWSD = 1)</td> <td>SSI_SCK falling edge</td> <td>SSI_SCK rising edge</td> </tr> </tbody> </table>		SCKP = 0	SCKP = 1	SSI_SDATA input sampling timing at the time of reception (TRMD = 0)	SSI_SCK rising edge	SSI_SCK falling edge	SSI_SDATA output change timing at the time of transmission (TRMD = 1)	SSI_SCK falling edge	SSI_SCK rising edge	SSI_WS input sampling timing at the time of slave mode (SWSD = 0)	SSI_SCK rising edge	SSI_SCK falling edge	SSI_WS output change timing at the time of master mode (SWSD = 1)	SSI_SCK falling edge	SSI_SCK rising edge
	SCKP = 0	SCKP = 1																	
SSI_SDATA input sampling timing at the time of reception (TRMD = 0)	SSI_SCK rising edge	SSI_SCK falling edge																	
SSI_SDATA output change timing at the time of transmission (TRMD = 1)	SSI_SCK falling edge	SSI_SCK rising edge																	
SSI_WS input sampling timing at the time of slave mode (SWSD = 0)	SSI_SCK rising edge	SSI_SCK falling edge																	
SSI_WS output change timing at the time of master mode (SWSD = 1)	SSI_SCK falling edge	SSI_SCK rising edge																	
12	SWSP	0	R/W	<p>Serial WS Polarity</p> <p>The value of this bit must not be changed when the SSI module enable (EN) bit in this register is set to 1.</p> <ul style="list-style-type: none"> <li>When the stereo format or multi-channel format is used (WS_MODE = 0, MONO = 0, and WIDTH = B'00000 in the WS mode register): <p>0: SSI_WS is low for 1st channel, high for 2nd channel.</p> <p>1: SSI_WS is high for 1st channel, low for 2nd channel.</p> </li> <li>When the TDM format is used (WS_MODE = 1, MONO = 0, and WIDTH = B'00000 in the WS mode register): <p>0: The SYNC pulse is high over the period of system word 1, and low otherwise.</p> <p>1: The SYNC pulse is low for over the period of system word 1, and high otherwise.</p> </li> <li>When the monaural format is used (WS_MODE = 1, MONO = 1, and WIDTH = B'00001 to B'11111 in the WS mode register): <p>0: WS pulse is high over the period specified with the WIDTH bits in the WS mode register, and low otherwise.</p> <p>1: WS pulse is low over the period specified with the WIDTH bits in the WS mode register, and high otherwise.</p> </li> </ul>															
11	SPDP	0	R/W	<p>Serial Padding Polarity</p> <p>0: Padding bits are low.</p> <p>1: Padding bits are high.</p> <p>Padding bits are low when MUEN = 1. (The mute function takes priority.)</p>															
10	SDTA	0	R/W	<p>Serial Data Alignment</p> <p>This bit should be set to 0 when the monaural format is used (WS_MODE = 1, MONO = 1, and WIDTH = B'00001 to B'11111 in the WS mode register).</p> <p>0: Transmitting and receiving in the order of serial data and padding bits.</p> <p>1: Transmitting and receiving in the order of padding bits and serial data.</p>															

Bit	Bit Name	Initial Value	R/W	Description
9	PDTA	0	R/W	<p><b>Parallel Data Alignment</b></p> <p>When the length of data word is 32, 16 or 8 bits, this configuration field has no meaning. This bit should be set to 0 when the monaural format is used (WS_MODE = 1, MONO = 1, and WIDTH = B'00001 to B'11111 in the WS mode register).</p> <p>This bit applies to SSIRDR in receive mode and SSITDR in transmit mode.</p> <p>0: Parallel data (SSITDR, SSIRDR) is left-aligned. 1: Parallel data (SSITDR, SSIRDR) is right-aligned.</p> <p>DWL = 000 (with a data word length of 8 bits), the PDTA setting is ignored.</p> <p>All data bits in SSIRDR or SSITDR are used on the audio serial bus. Four data words are transmitted or received at each 32-bit access. The first data word is derived from bits 7 to 0, the second from bits 15 to 8, the third from bits 23 to 16 and the last data word is derived from bits 31 to 24.</p> <p>DWL = 001 (with a data word length of 16 bits), the PDTA setting is ignored.</p> <p>All data bits in SSIRDR or SSITDR are used on the audio serial bus. Two data words are transmitted or received at each 32-bit access. The first data word is derived from bits 15 to 0 and the second data word is derived from bits 31 to 16.</p> <p>DWL = 010, 011, 100, 101 (with a data word length of 18, 20, 22 or 24 bits), PDTA = 0 (left-aligned)</p> <p>The data bits used in SSIRDR or SSITDR are the following: Bits 31 down to (32 minus the number of bits in the data word length specified by DWL).</p> <p>That is, if DWL = 011, the data word length is 20 bits; therefore, bits 31 to 12 in either SSIRDR or SSITDR are used. All other bits are ignored or reserved.</p> <p>DWL = 010, 011, 100, 101 (with a data word length of 18, 20, 22 or 24 bits), PDTA = 1 (right-aligned)</p> <p>The data bits used in SSIRDR or SSITDR are the following: Bits (the number of bits in the data word length specified by DWL minus 1) to 0 i.e. if DWL = 011, then DWL = 20 and bits 19 to 0 are used in either SSIRDR or SSITDR. All other bits are ignored or reserved.</p> <p>DWL = 110 (with a data word length of 32 bits), the PDTA setting is ignored.</p> <p>All data bits in SSIRDR or SSITDR are used on the audio serial bus.</p>
8	DEL	0	R/W	<p><b>Serial Data Delay</b></p> <p>0: One clock cycle delay between SSI_WS and SSI_SDATA 1: No delay between SSI_WS and SSI_SDATA</p>
7	—	0	R	<p><b>Reserved</b></p> <p>The read value is 0. The write value should always be 0.</p>

Bit	Bit Name	Initial Value	R/W	Description
6 to 4	CKDV[2:0]	000	R/W	<p>Serial Oversampling Clock Division Ratio</p> <p>Set the ratio between oversampling clock, CLK_FS, and the serial bit clock.</p> <p>These bits are ignored if SCKD = 0.</p> <p>The serial bit clock is used in the shift register and is provided on the SSI_SCK module pin.</p> <p>000: Serial bit clock frequency = oversampling clock frequency/1            001: Serial bit clock frequency = oversampling clock frequency/2            010: Serial bit clock frequency = oversampling clock frequency/4            011: Serial bit clock frequency = oversampling clock frequency/8            100: Serial bit clock frequency = oversampling clock frequency/16            101: Serial bit clock frequency = oversampling clock frequency/6            110: Serial bit clock frequency = oversampling clock frequency/12            111: Setting prohibited</p> <p>CKDV = 000 is invalid when WS_MODE = 1 or CONT = 1 in the WS mode register.</p>
3	MUEN	0	R/W	<p>Serial Data Output Disable</p> <p>0: Module is not muted.            1: Module is muted.</p> <p>Note: This bit can be used to stop output (low output) or to enable output. However, the operation is not synchronized with the change of SSI_WS.</p>
2	—	0	R	<p>Reserved</p> <p>The read value is 0. The write value should always be 0.</p>
1	TRMD	0	R/W	<p>Transmit/Receive Mode Select</p> <p>0: Module is in receive mode.            1: Module is in transmit mode.</p>
0	EN	0	R/W	<p>SSI Module Enable</p> <p>0: Module is disabled.            1: Module is enabled.</p>



### 32A.2.2 Status Register (SSISRn) (n = 0 to 9)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SSISR consists of status flags indicating the operational status of the SSI module and bits indicating the current channel numbers and word numbers.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	DMRQ	UIRQ	OIRQ	IIRQ	DIRQ	—	—	—	—	—	—	—	—
Initial value:	—	—	—	0	0	0	—	0	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R/WC0	R/WC0	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	CHNO[1:0]	SWNO	IDST	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	0	0	1	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	Undefined	R	Reserved The read value is not guaranteed. The write value should always be 0.
28	DMRQ	0	R	DMA Request Status Flag This status flag allows the CPU to recognize the value of the DMA request pin on the SSI module. <ul style="list-style-type: none"> <li>TRMD = 0 (receive mode) If DMRQ = 1, the SSIRDR has unread data. If SSIRDR is read, DMRQ = 0 until there is new unread data.</li> <li>TRMD = 1 (transmit mode) If DMRQ = 1, SSITDR requires data to be written to continue the transmission to the audio serial bus. Once data is written to SSITDR, DMRQ = 0 until it requires further transmit data.</li> </ul>

Bit	Bit Name	Initial Value	R/W	Description
27	UIRQ	0	R/WC0	<p><b>Underflow Error Interrupt Status Flag</b></p> <p>This status flag indicates that data was supplied at a lower rate than was required.</p> <p>In either case, this bit is set to 1 regardless of the value of the UIEN bit and can be cleared by writing 0 to this bit.</p> <p>If UIRQ = 1 and UIEN = 1, an interrupt occurs.</p> <ul style="list-style-type: none"> <li>• TRMD = 0 (receive mode) If UIRQ = 1, SSIRDR was read before there was new unread data indicated by the DMRQ or DIRQ bit. This can lead to the same received data being stored twice by the host leading to potential corruption of multi-channel data.</li> <li>• TRMD = 1 (transmit mode) If UIRQ = 1, SSITDR did not have data written to it before it was required for transmission. This will lead to the same data being transmitted once more and a potential corruption of multi-channel data. This is more serious error than a receive mode underflow as the output SSI data results in error.</li> </ul> <p>Note: When underflow error occurs, the current data in the data buffer of this module is transmitted until the next data is filled.</p>
26	OIRQ	0	R/WC0	<p><b>Overflow Error Interrupt Status Flag</b></p> <p>This status flag indicates that data was supplied at a higher rate than was required.</p> <p>In either case this bit is set to 1 regardless of the value of the OIEN bit and can be cleared by writing 0 to this bit.</p> <p>If OIRQ = 1 and OIEN = 1, an interrupt occurs.</p> <ul style="list-style-type: none"> <li>• TRMD = 0 (receive mode) If OIRQ = 1, SSIRDR was not read before there was new unread data written to it. This will lead to the loss of a data and a potential corruption of multi-channel data.</li> <li>• TRMD = 1 (transmit mode) If OIRQ = 1, SSITDR had data written to it before it was transferred to the shift register. This will lead to the loss of a data and a potential corruption of multi-channel data.</li> </ul> <p>Note: When overflow error occurs, the current data in the data buffer of this module is overwritten by the next incoming data from the SSI interface.</p>
25	IIRQ	Undefined	R	<p><b>Idle Mode Interrupt Status Flag</b></p> <p>This interrupt status flag indicates whether the SSI module is in idle state.</p> <p>This bit is set regardless of the value of the IIEN bit to allow polling.</p> <p>“Idle state” refers to the state where the serial bus has been stopped after activation of the SSI.</p> <p>The interrupt can be masked by clearing IIEN, but cannot be cleared by writing to this bit.</p> <p>If IIRQ = 1 and IIEN = 1, an interrupt occurs.</p> <p>0: The SSI module is not in idle state. 1: The SSI module is in idle state.</p>

Bit	Bit Name	Initial Value	R/W	Description
24	DIRQ	0	R	<p>Data Interrupt Status Flag</p> <p>This status flag indicates that the module has data to be read or requires data to be written.</p> <p>In either case this bit is set to 1 regardless of the value of the DIEN bit to allow polling.</p> <p>The interrupt can be masked by clearing DIEN, but cannot be cleared by writing to this bit.</p> <p>If DIRQ= 1 and DIEN = 1, an interrupt occurs.</p> <ul style="list-style-type: none"> <li>• TRMD = 0 (receive mode) <ul style="list-style-type: none"> <li>0: No unread data in SSIRDR</li> <li>1: Unread data in SSIRDR</li> </ul> </li> <li>• TRMD = 1 (transmit mode) <ul style="list-style-type: none"> <li>0: Transmit buffer is full.</li> <li>1: Transmit buffer is empty and requires data to be written to SSITDR.</li> </ul> </li> </ul>
23 to 4	—	—	R	<p>Reserved</p> <p>The read value is not guaranteed. The write value should always be 0.</p>
3, 2	CHNO[1:0]	00	R	<p>Channel Number</p> <p>These bits indicate the current channel number. However, if the length of data words is 8 or 16 bits, the value of these bits is meaningless.</p> <p>00: 1st channel 01: 2nd channel 10: 3rd channel 11: 4th channel</p> <ul style="list-style-type: none"> <li>• TRMD = 0 (receive mode) <p>CHNO indicates which channel the data in SSIRDR currently represents. This value will change as the data in SSIRDR is updated from the shift register.</p> </li> <li>• TRMD = 1 (transmit mode) <p>CHNO indicates which channel is required to be written to SSITDR. This value will change as the data is copied to the shift register, regardless of whether the data is written to SSITDR.</p> <p>These bits cannot be used when WS_MODE = 1 or CONT = 1 in the WS mode register.</p> </li> </ul>

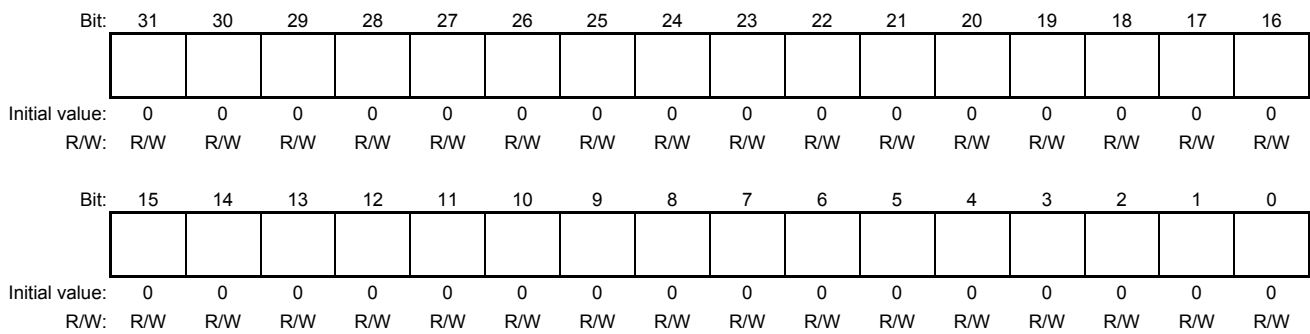
Bit	Bit Name	Initial Value	R/W	Description
1	SWNO	1	R	<p>System Word Number</p> <p>This status bit indicates the current word number. However, if the length of data words is 8 or 16 bits, the value of this bit is meaningless.</p> <ul style="list-style-type: none"> <li>• TRMD = 0 (receive mode) SWNO indicates which system word the data in SSIRDR currently represents. This value will change as the data in SSIRDR is updated from the shift register, regardless of whether SSIRDR has been read.</li> <li>• TRMD = 1 (transmit mode) SWNO indicates which system word is required to be written to SSITDR. This value will change as the data is copied to the shift register, regardless of whether the data is written to SSITDR. This bit cannot be used when WS_MODE = 1 or CONT = 1 in the WS mode register.</li> </ul>
0	IDST	Undefined	R	<p>Idle Mode Status Flag</p> <p>This status flag indicates that the serial bus activity has stopped. This bit is cleared if EN = 1 and the serial bus are currently active. This bit is automatically set to 1 under the following conditions.</p> <ul style="list-style-type: none"> <li>• SSI = Master transmitter (SWSD = 1 and TRMD = 1) This bit is set to 1 when the EN bit is cleared and data written in SSITDR has been output from the serial data input/output pin (SSI_SDATA).</li> <li>• SSI = Master receiver (SWSD = 1 and TRMD = 0) This bit is set to 1 when the EN bit is cleared and transfer of the current system word is completed.</li> <li>• SSI = Slave transmitter/receiver (SWSD = 0) This bit is set to 1 when the EN bit is cleared and transfer of the current system word is completed.</li> </ul> <p>Note: If an external device stops the serial bus clock before transfer of the current system word is completed, this bit is not set.</p>

### 32A.2.3 Transmit Data Register (SSITDRn) (n = 0 to 9)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SSITDR is a 32-bit register that holds data to be transmitted.

Data written to this register is transferred to the shift register upon transmission request. If the data word length is less than 32 bits, the alignment is determined by the setting of the PDTA control bit in SSICR. The data in the buffer can be accessed by reading this register.

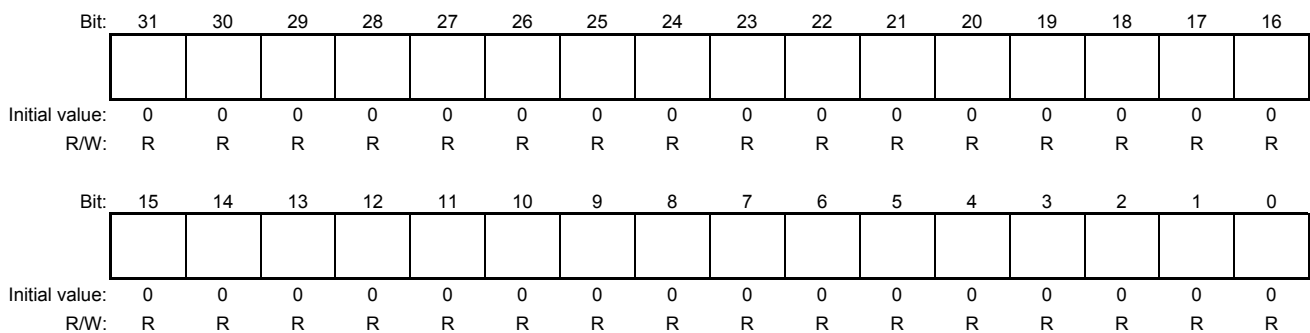


### 32A.2.4 Receive Data Register (SSIRDRn) (n = 0 to 9)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SSIRDR is a 32-bit register that stores receive messages.

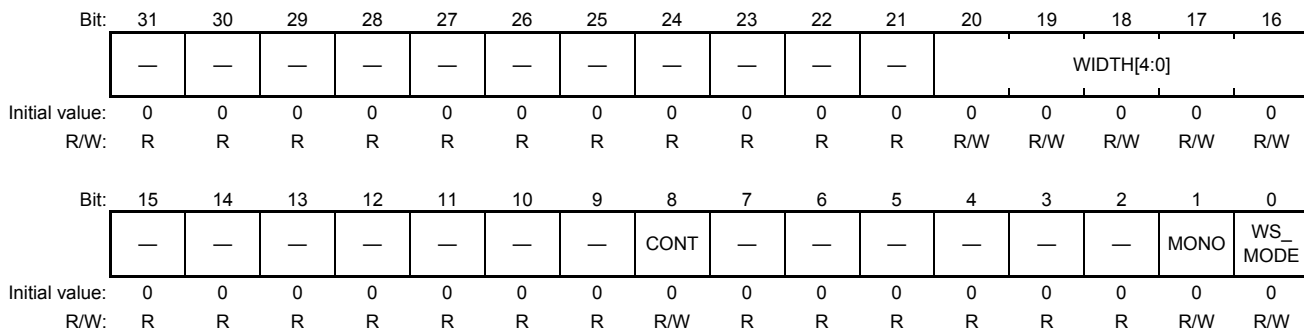
Data in this register is transferred from the shift register each time data word is received. If the data word length is less than 32 bits, the alignment is determined by the setting of the PDTA control bit in SSICR.



**32A.2.5 WS Mode Register (SSIWSRn) (n = 0 to 9)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SSIWSR is a 32-bit readable/writable register that sets the TDM format, monaural format, and WS continue function.



Bit	Bit Name	Initial Value	R/W	Description
31 to 21	—	All 0	R	Reserved The read value is 0. The write value should always be 0.
20 to 16	WIDTH[4:0]	00000	R/W	SYNC Pulse Width Change <ul style="list-style-type: none"> <li>When the TDM format is used (WS_MODE = 1 and MONO = 0 in this register):                             <ul style="list-style-type: none"> <li>00000: TDM format</li> <li>Other than 00000: Setting prohibited</li> </ul> </li> <li>When the monaural format is used (WS_MODE = 1 and MONO = 1 in this register):                             <ul style="list-style-type: none"> <li>00000: Setting prohibited</li> <li>00001: Pulse width is equivalent to one cycle of SCK.</li> <li>00010: Pulse width is equivalent to two cycles of SCK.</li> <li>...</li> <li>11111: Pulse width is equivalent to 31 cycles of SCK.</li> </ul> </li> </ul> Note that the set value of the system word length bits (SWL) in SSICR should be greater than that of the SYNC pulse width bits (WIDTH) when the monaural format is used.
15 to 9	—	All 0	R	Reserved The read value is 0. The write value should always be 0.
8	CONT	0	R/W	WS Continue Function <ul style="list-style-type: none"> <li>0: WS continue function is disabled.</li> <li>1: WS continue function is enabled.</li> </ul> Note: This bit can only be set in master mode (SSICR.SCKD = 1, SSICR.SWSD = 1).
7 to 2	—	All 0	R	Reserved The read value is 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
1	MONO	0	R/W	TDM Format/Monaural Format Selects the TDM format or monaural format. When the normal stereo format, multi-channel format, this bit should be 0. 0: TDM format 1: Monaural format
0	WS_MODE	0	R/W	WS Mode 0: Stereo format, multi-channel format 1: TDM format, monaural format

### 32A.2.6 FS Mode Register (SSIFMRn) (n = 0 to 9)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SSIFMR is used to set the frequency switching detection function.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
	—	—	—	—	—	—	—	—	—	—	DTCT[5:0]						
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	—	—	—	—	—	—	—	—	—	—	CTDV[1:0]		—	—	—	FSEN	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R	R	R	R/W	

Bit	Bit Name	Initial Value	R/W	Description
31 to 22	—	All 0	R	Reserved The read value is 0. The write value should always be 0.
20 to 16	DTCT[5:0]	000000	R/W	Frequency Switching Detection Range Set 000100: Set the value in the range as 5.
15 to 6	—	All 0	R	Reserved The read value is 0. The write value should always be 0.
5, 4	CTDV[1:0]	00	R/W	Bus Clock Division Ratio Sets the bus clock division ratio used for the frequency switching detection function. 11: Set the switching detection clock frequency = bus clock frequency/8.
3 to 1	—	All 0	R	Reserved The read value is 0. The write value should always be 0.
0	FSEN	0	R/W	Frequency Switching Detection Function Enable 0: The frequency switching detection function is disabled. 1: The frequency switching detection function is enabled. Note: This bit must be enabled after the desired settings have been made for SWSP in SSICR and WS_MODE in SSIWSR.



**32A.2.7 FS Status Register (SSIFSRn) (n = 0 to 9)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SSIFSR is used to read the frequency switching detection status and information on the frequency counter.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FCST	DTST	—	—	FCNT[11:0]											
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/WC0	R/WC0	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved The read value is 0. The write value should always be 0.
15	FCST	0	R/WC0	WS Stopped Status Flag In the frequency switching detection function, this status flag reflects the state that the WS signal is stopped. When FCST = 1, this bit indicates that the WS signal has stopped (the state is detected only when FSEN in SSIFMR = 1). Write 0 if this bit is cleared to 0.
14	DTST	0	R/WC0	Frequency Switching Detection Status Flag In the frequency switching detection function, this status flag reflects the state that frequency switching has been detected. When DTST = 1, this bit indicates that the switching has been detected (the state is detected only when FSEN in SSIFMR = 1). Write 0 if this bit is cleared to 0.
13, 12	—	0	R	Reserved The read value is 0. The write value should always be 0.
11 to 0	FCNT[11:0]	H'000	R	Frequency Count Monitor When the frequency switching detection function is enabled, the count value between WS signal edges is reflected according to the setting of the operating mode and the serial WS polarity (SWSP in SSICR). This value is updated when the frequency is switched and the WS signal has been detected.

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

## 32A.3 Operation

### 32A.3.1 Bus Format

The SSI module can operate as a transmitter or a receiver and can be configured into many serial bus formats in either mode.

The bus format can be selected from one of the four major modes shown in Table 32A.2.

**Table 32A.2 Bus Format for SSI Module**

	SSICR																SSIWSR				
	TRMD	SCKD	SWSD	EN	MUEN	DIEN	IEN	OIEN	UIEN	DEL	PDTA	SDTA	SPDP	SWSP	SCKP	SWL[2:0]	DWL[2:0]	CHNL	WS_MODE	MONO	CONT
Non-compressed slave receiver	0	0	0	Control bits						Configuration bits									WS mode bits		
Non-compressed slave transmitter	1	0	0																		
Non-compressed master receiver	0	1	1																		
Non-compressed master transmitter	1	1	1																		

### 32A.3.2 Non-compressed Modes

The non-compressed modes support all serial audio streams split into channels. They support I2S, left-aligned, and right-aligned formats as well as many more variants on these modes.

#### (1) Slave receiver

This mode allows the module to receive serial data from another device. The clock and word select signal used for the serial data stream is also supplied from an external device. If these signals do not conform to the format specified in the configuration fields of the SSI module, operation is not guaranteed.

#### (2) Slave transmitter

This mode allows the module to transmit serial data to another device. The clock and word select signal used for the serial data stream is also supplied from an external device. If these signals do not conform to the format specified in the configuration fields of the SSI module, operation is not guaranteed.

#### (3) Master receiver

This mode allows the module to receive serial data from another device. The clock and word select signals are internally derived from the CLK\_FS input clock. The format of these signals is defined in the configuration fields of the SSI module. If the incoming data does not follow the configured format, operation is not guaranteed.

#### (4) Master transmitter

This mode allows the module to transmit serial data to another device. The clock and word select signals are internally derived from the CLK\_FS input clock. The format of these signals is defined in the configuration fields of the SSI module.

(5) Setting for each format

Table 32A.3 shows the setting for each format:

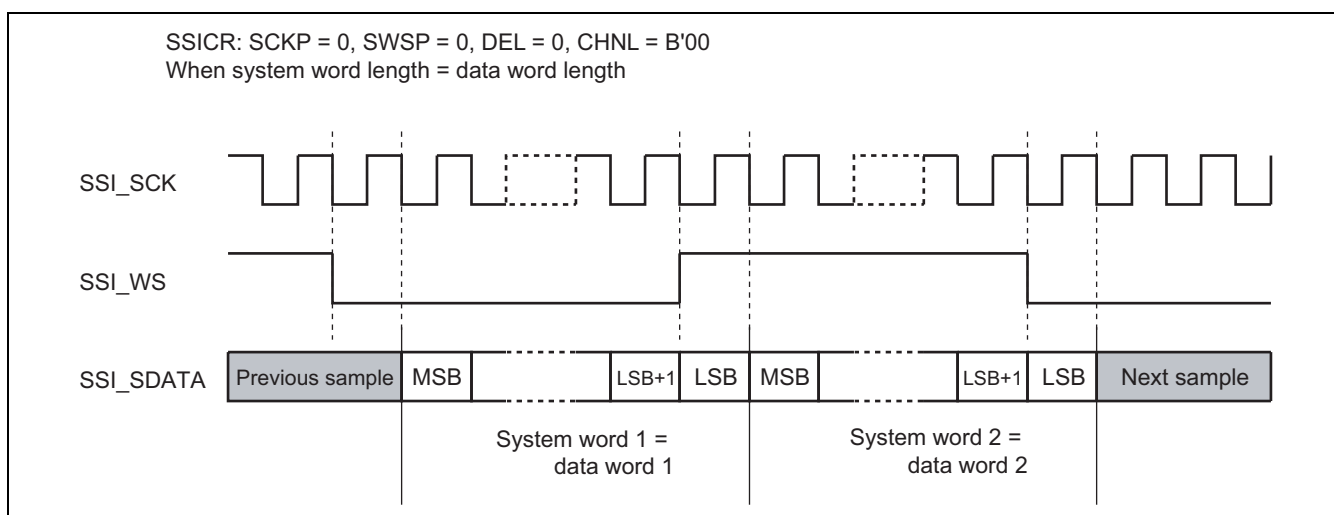
**Table 32A.3 Setting for Each Format**

Format	SSICR	SSIWSR		
	CHNL[1:0]	WS_MODE	MONO	WIDTH[4:0]
Stereo format	B'00	0	0	B'00000
Multi-channel format	B'01/B'10/B'11	0	0	B'00000
Monaural format	B'00	1	1	B'00001 to B'11111
TDM format	B'01/B'10/B'11	1	0	B'00000

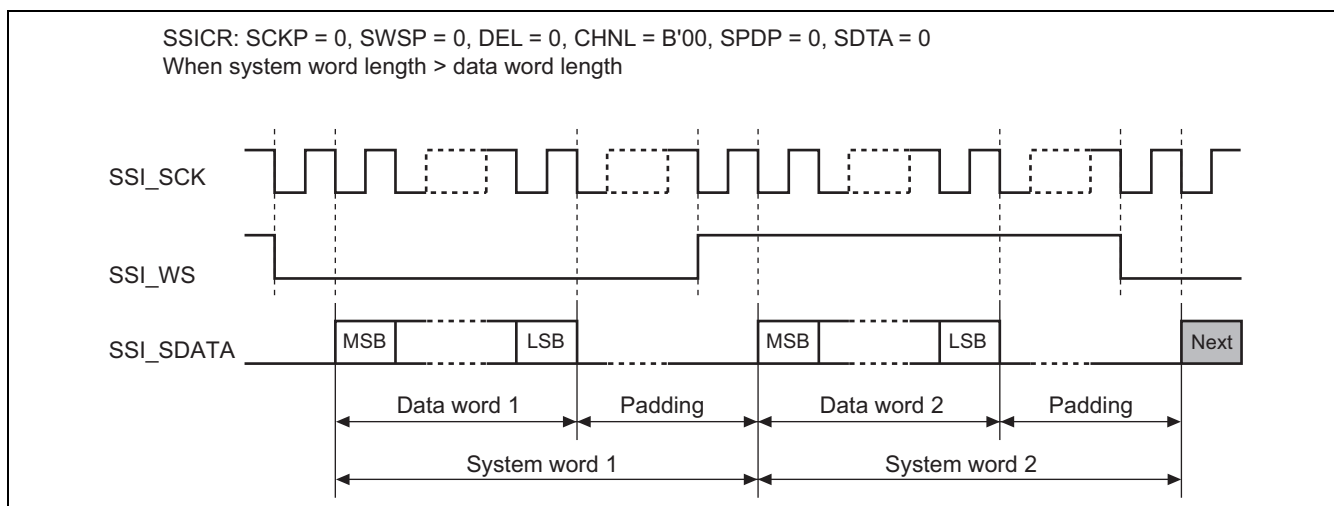
(6) Configuration bits (related to word length)

All bits related to the SSICR's word length are valid in non-compressed modes. There are many configurations the SSI module supports, but only some of the combinations are shown below for the I2S, left-aligned, and right-aligned formats.

Figures 32A.2 and 32A.3 demonstrate the supported I2S format both with and without padding. Padding occurs when the data word length is smaller than the system word length.

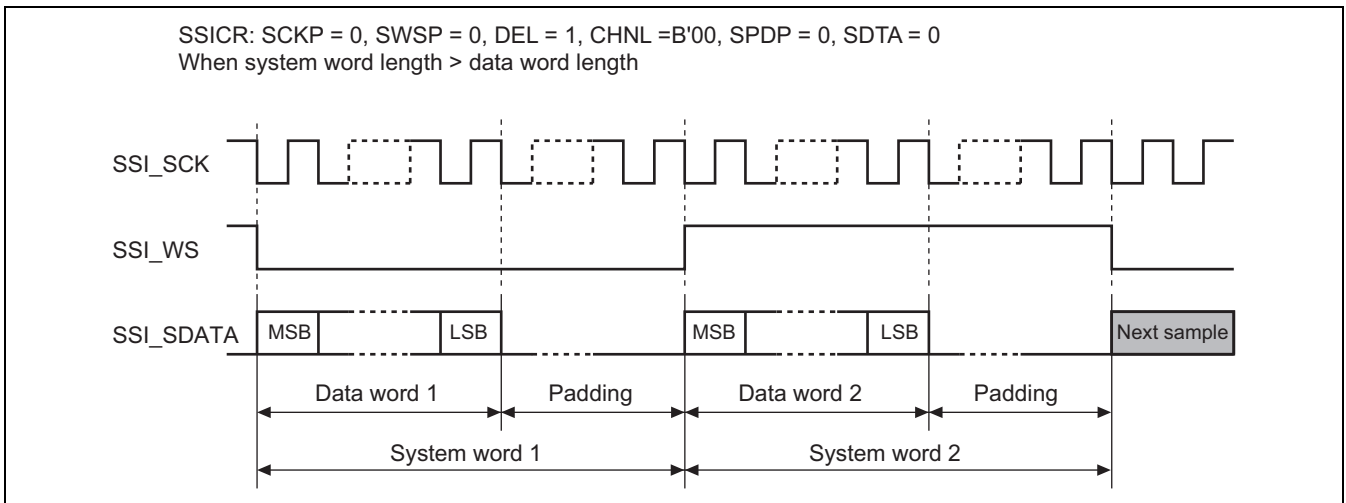


**Figure 32A.2 I2S Format (without Padding)**

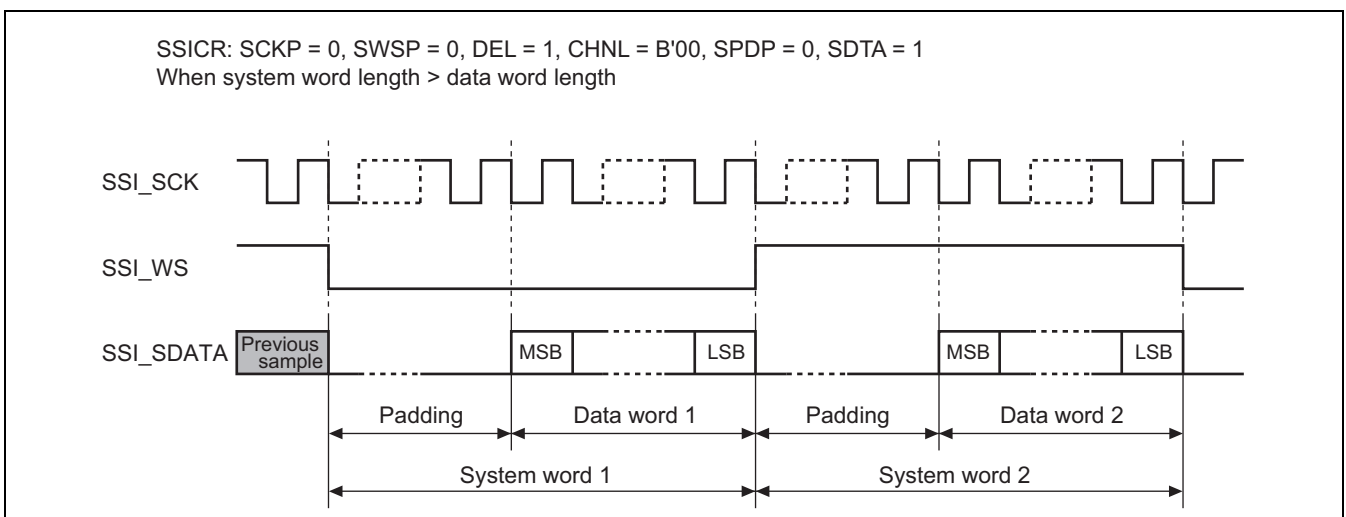


**Figure 32A.3 I2S Format (with Padding)**

Figure 32A.4 shows the left-aligned format and Figure 32A.5 shows the right-aligned format. Padding is assumed in both cases, but may not be present in a final implementation if the system word length equals the data word length.



**Figure 32A.4 Left-Aligned Format**  
**(Transmitting and Receiving in the Order of Serial Data and Padding Bits)**



**Figure 32A.5 Right-Aligned Format**  
**(Transmitting and Receiving in the Order of Padding Bits and Serial Data)**

**(7) Multi-channel formats**

Some devices extend the definition of the I2S format and allow more than two channels to be transferred within two system words.

The SSI module supports the transfer of two, three, and four channels by using the CHNL, SWL and DWL bits only when the system word length (SWL) is greater than or equal to the data word length (DWL) multiplied by channels (CHNL).

Table 32A.4 shows the number of padding bits for each of the valid setting. If setting is not valid, "—" is indicated instead of a number.

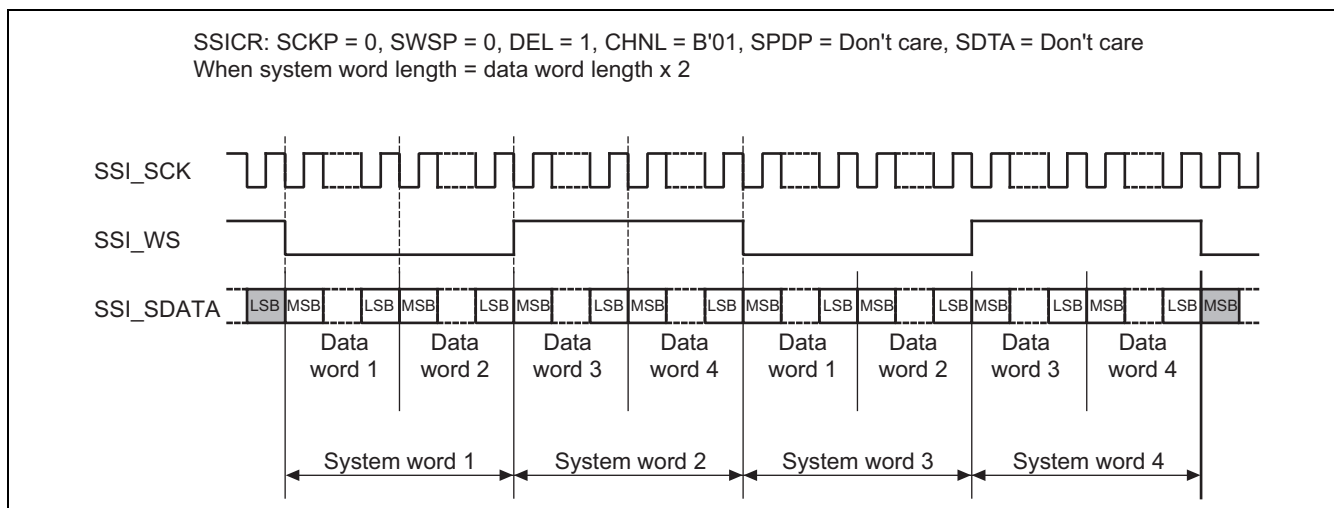
**Table 32A.4 The Number of Padding Bits for Each Valid Setting**

Padding Bits Per System Word		DWL[2:0]	B'000	B'001	B'010	B'011	B'100	B'101	B'110	
CHNL [1:0]	Decoded Channels per System Word	SWL [2:0]	Decoded Word Length	8	16	18	20	22	24	32
B'00	1	B'000	8	0	—	—	—	—	—	—
		B'001	16	8	0	—	—	—	—	—
		B'010	24	16	8	6	4	2	0	—
		B'011	32	24	16	14	12	10	8	0
		B'100	48	40	32	30	28	26	24	16
		B'101	64	56	48	46	44	42	40	32
		B'110	128	120	112	110	108	106	104	96
		B'111	256	248	240	238	236	234	232	224
B'01	2	B'000	8	—	—	—	—	—	—	—
		B'001	16	0	—	—	—	—	—	—
		B'010	24	8	—	—	—	—	—	—
		B'011	32	16	0	—	—	—	—	—
		B'100	48	32	16	12	8	4	0	—
		B'101	64	48	32	28	24	20	16	0
		B'110	128	112	96	92	88	84	80	64
		B'111	256	240	224	220	216	212	208	192

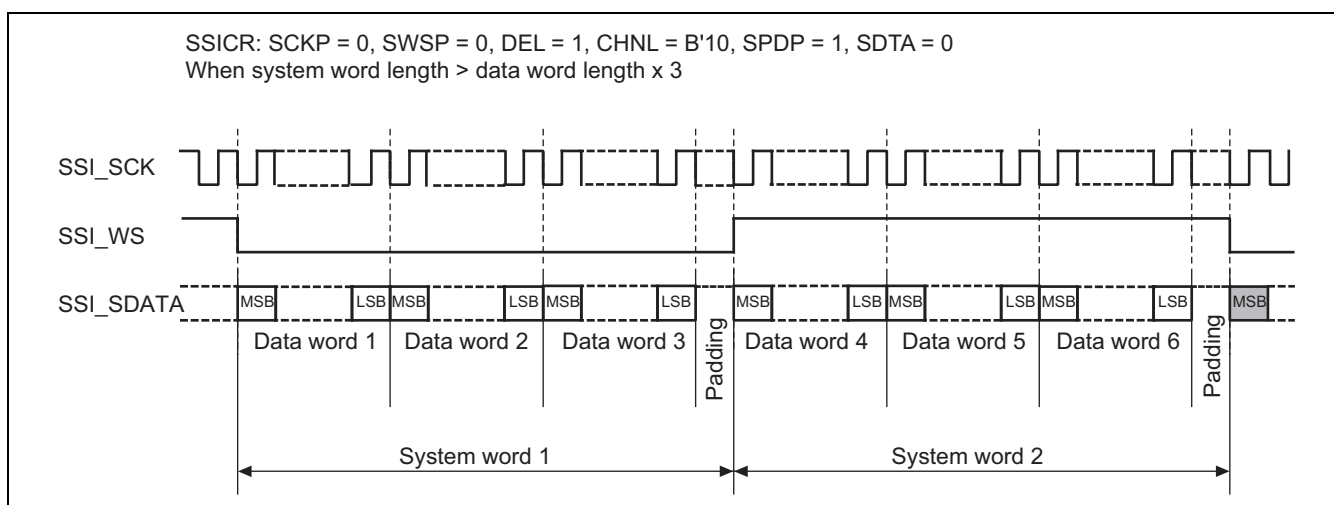
Padding Bits Per System Word			DWL[2:0]	B'000	B'001	B'010	B'011	B'100	B'101	B'110
CHNL [1:0]	Decoded Channels per System Word	SWL [2:0]	Decoded Word Length	8	16	18	20	22	24	32
B'10	3	B'000	8	—	—	—	—	—	—	—
		B'001	16	—	—	—	—	—	—	—
		B'010	24	0	—	—	—	—	—	—
		B'011	32	8	—	—	—	—	—	—
		B'100	48	24	0	—	—	—	—	—
		B'101	64	40	16	10	4	—	—	—
		B'110	128	104	80	74	68	62	56	32
		B'111	256	232	208	202	196	190	184	160
B'11	4	B'000	8	—	—	—	—	—	—	—
		B'001	16	—	—	—	—	—	—	—
		B'010	24	—	—	—	—	—	—	—
		B'011	32	0	—	—	—	—	—	—
		B'100	48	16	—	—	—	—	—	—
		B'101	64	32	0	—	—	—	—	—
		B'110	128	96	64	56	48	40	32	0
		B'111	256	224	192	184	176	168	160	128

When the SSI module acts as a transmitter, each word written to SSITDR is transmitted to the serial audio bus in the order they are written. When the SSI module acts as a receiver, each word received by the serial audio bus is read in the order received from SSIRDR.

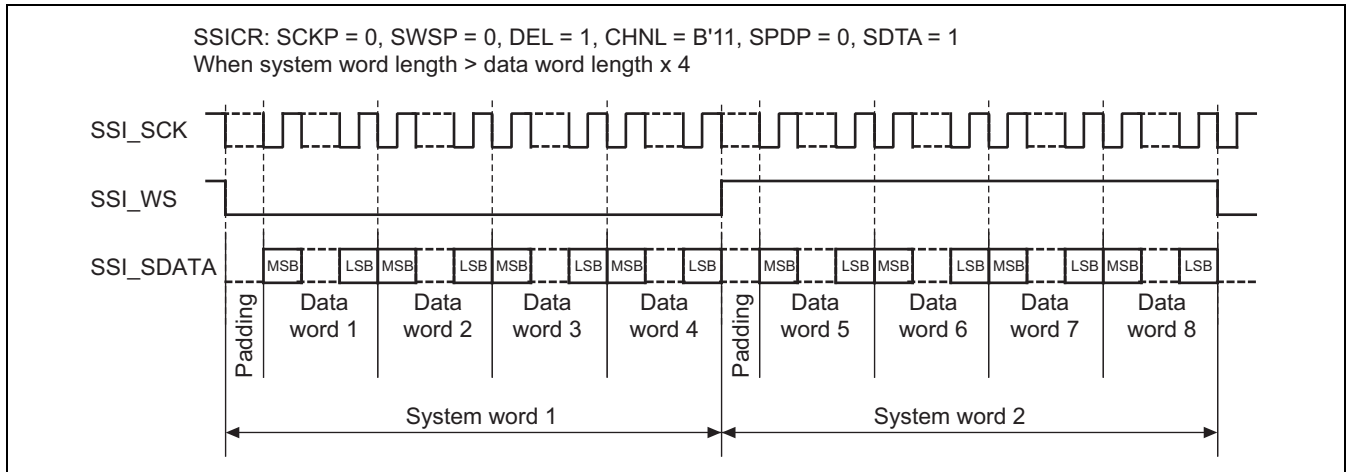
Figures 32A.6 to 32A.8 show how two, three and four channels are transferred to the serial audio bus. Note that there are no padding bits in the first example, the second example is left-aligned and the third is right-aligned. This selection is arbitrary and is just for demonstration purposes only.



**Figure 32A.6 Multi-Channel Format (Two Channels without Padding)**



**Figure 32A.7 Multi-Channel Format (Three Channels with High Padding)**



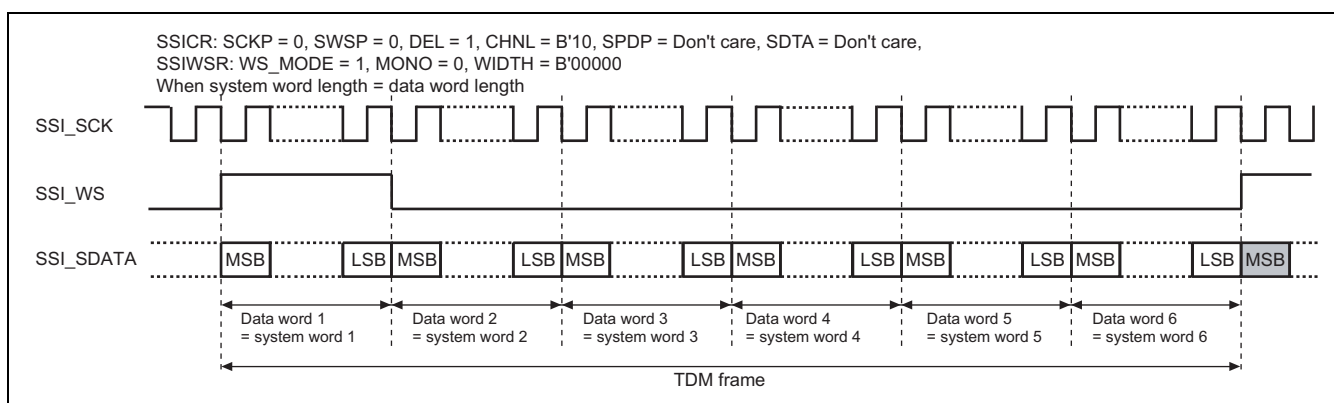
**Figure 32A.8 Multi-Channel Format (Four Channels; Transmitting and Receiving in the Order of Padding Bits and Serial Data; with Padding)**



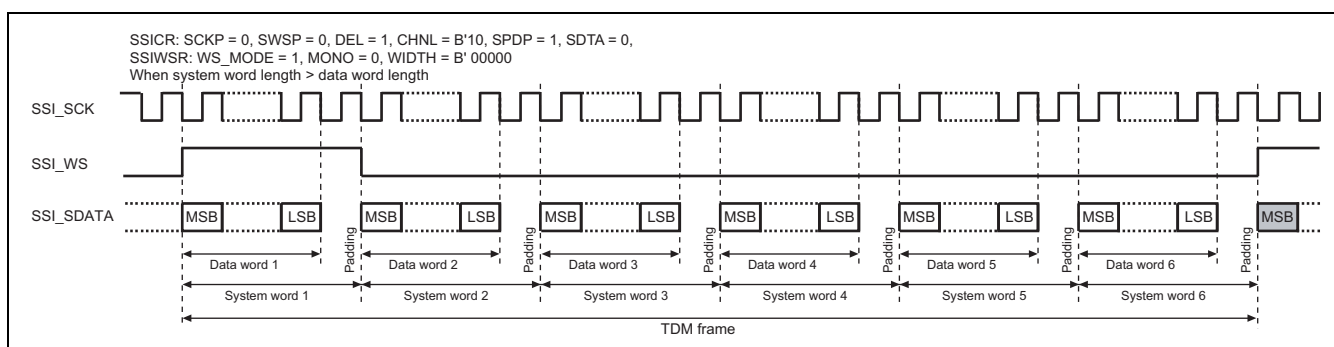
### (8) TDM formats

The TDM format is used for connecting the SSI with a multi-channel device which supports TDM. The TDM format is set by using the WS\_MODE and MONO bits in SSIWSR. When the SWSP bit in SSICR is 0 with the TDM format, SSI\_WS is driven high over the period of system word 1, and pulled low otherwise. When the SWSP bit is 1, SSI\_WS is pulled low over the period of system word 1, and driven high otherwise. The pulses generated on the SSI\_WS signal are referred to as SYNC pulses.

Figures 32A.9 and 32A.10 show the TDM formats without padding and with padding.



**Figure 32A.9 TDM Format (Six System Words, without Padding)**



**Figure 32A.10 TDM Format (Six System Words, with Padding)**

The following describes operation in each mode:

#### (a) Master transmitter

By a transfer start trigger (setting the EN bit in the control register to 1), a transfer of system word 1 begins synchronously with the SYNC pulses.

By a transfer stop trigger (setting the EN bit in the control register to 0), a transfer is stopped at the end of the currently-transferred system word and the SDATA signal is output according to the SPDP setting in SSICR (when SPDP = 0, a low-level signal is output).

If transmit data is not ready in the SSI module during transmission, an underflow will occur. When an underflow occurs, data to be output for the SYNC pulses cannot be determined. Therefore, stop and reconfigure the transfer.

#### (b) Master receiver

By a transfer start trigger (setting the EN bit in the control register to 1), a reception of system word 1 data begins at the point where the SSI module recognizes a SYNC pulse.

By a transfer stop trigger (setting the EN bit in the control register to 0), a reception is stopped at the end of the currently-transferred system word.

The receive data register should not be read when it does not have data. If read, an underflow will occur. When an underflow occurs, stop and reconfigure the transfer.

The receive data should not be written to before read. If written to, an overflow will occur. When an overflow occurs, stop and reconfigure the transfer.

**(c) Slave transmitter**

By a transfer start trigger (setting the EN bit in the control register to 1), a transfer of system word 1 begins synchronously with the SYNC pulses.

By a transfer stop trigger (setting the EN bit in the control register to 0), a transfer is stopped at the end of the currently-transferred system word and the SDATA signal is output according to the SPDP setting in SSICR (when SPDP = 0, a low-level signal is output).

If transmit data is not ready in the SSI module during transmission, an underflow will occur. When an underflow occurs, data to be output for SYNC pulses cannot be determined. Therefore, stop and re-set the transfer.

Transfers cannot be performed if the SCK signal and SYNC pulses are not provided to the SSI module during transfer.

**(d) Slave receiver**

By a transfer start trigger (setting the EN bit in the control register to 1), a reception of system word 1 data begins at the point where the SSI module recognizes a SYNC pulse.

By a transfer stop trigger (setting the EN bit in the control register to 0), a reception is stopped at the end of the currently-transferred system word.

The receive data should not be read when it does not have data. If read, an underflow will occur. When an underflow occurs, stop and reconfigure the transfer.

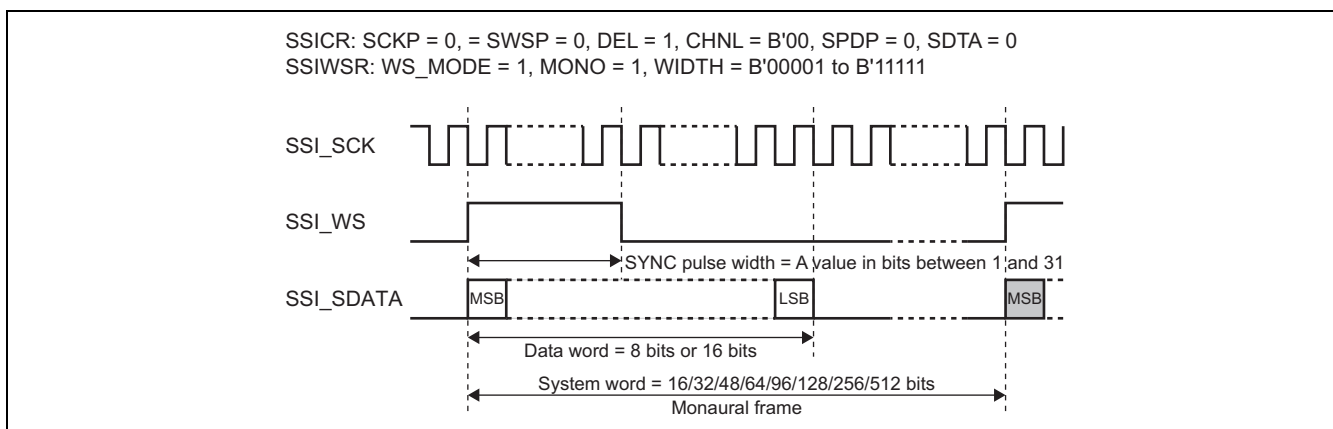
The receive data register should not be written to before read. If written to, an overflow will occur. When an overflow occurs, stop and reconfigure the transfer.

Transfer cannot proceed if the SCK signal and SYNC pulses are not being provided to the SSI module during transfer.

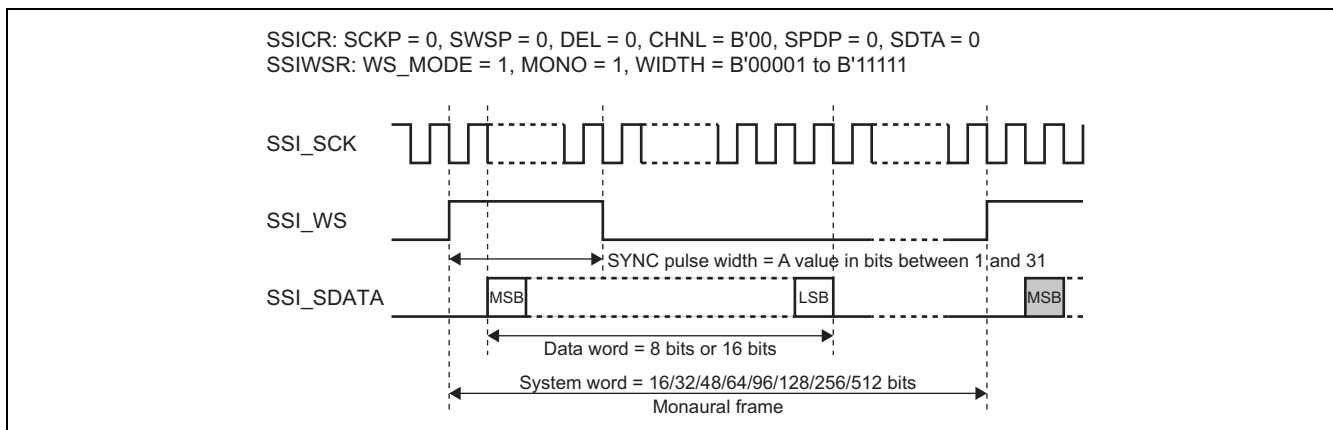
**(9) Monaural format**

The monaural format is set by using the WS\_MODE and MONO bits in SSIWSR. The available data lengths are 8 bits and 16 bits. When the SWSP bit in SSICR is 0 and the monaural format is selected, SSI\_WS is driven high over the period from bit 1 to bit 31, and pulled low otherwise. When the SWSP bit is 1, SSI\_WS is pulled low over the period from bit 1 to bit 31, and driven high otherwise. The pulses generated as the SSI\_WS signal are referred to as SYNC pulses. The width of the SYNC pulses can be set to a value in bits between 1 and 31 by using the WIDTH bits in SSIWSR. The setting must be smaller than the system word length (SSICR.SWL). In the monaural format, the system word length is equal to one monaural frame period.

Figure 32A.11 shows the left-aligned monaural format and Figure 32A.12 shows the monaural format with a delay of one bit-period.



**Figure 32A.11 Monaural Format (Left-Aligned)**

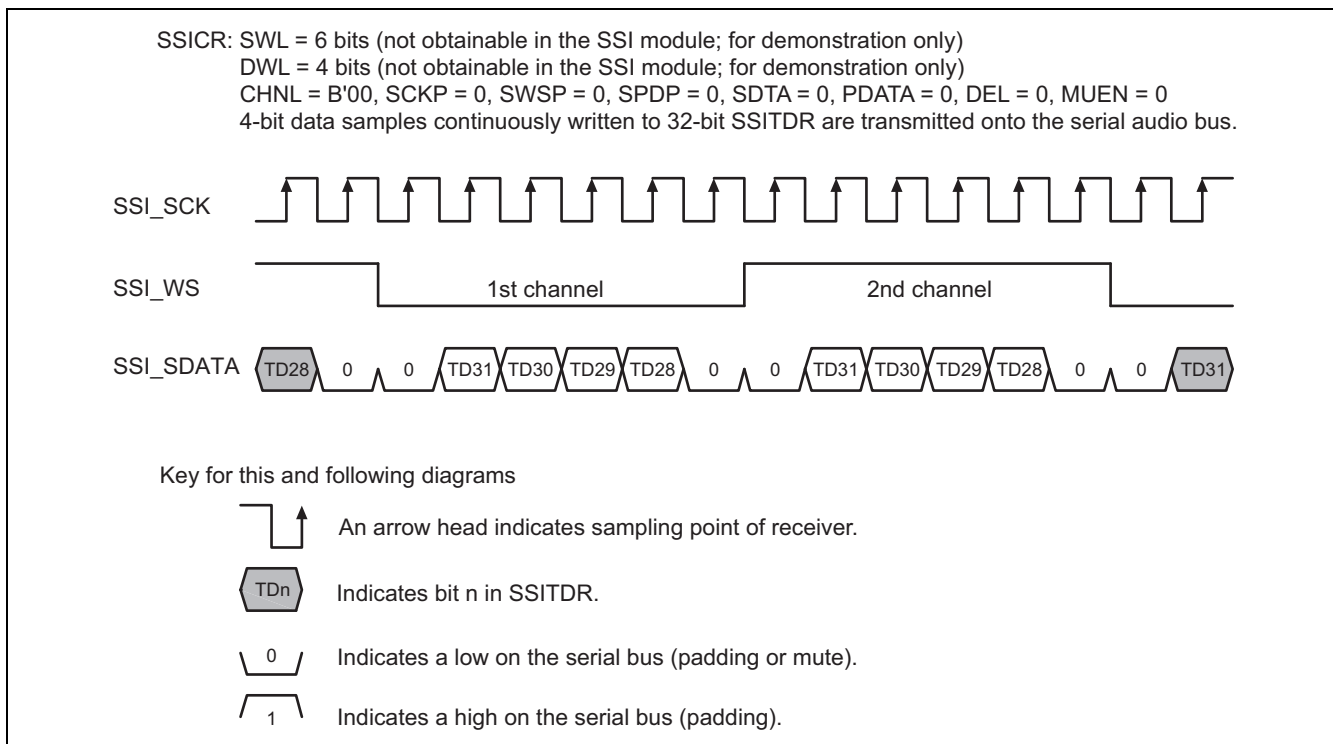


**Figure 32A.12 Monaural Format (with 1-bit Delay)**

**(10) Configuration bits**

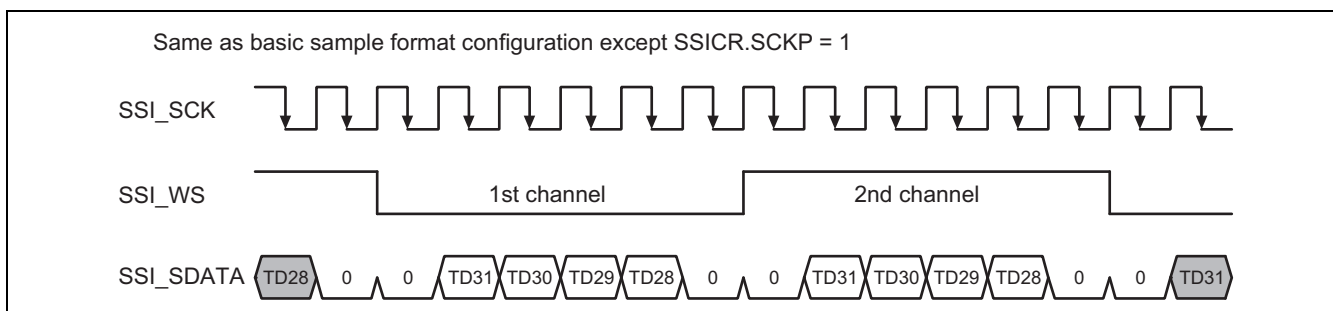
Several more configuration bits in non-compressed mode are shown below. These bits are not mutually exclusive, but some combinations may not be useful for any other device.

These configuration bits are described below with reference to Figure 32A.13, Basic Sample Format.

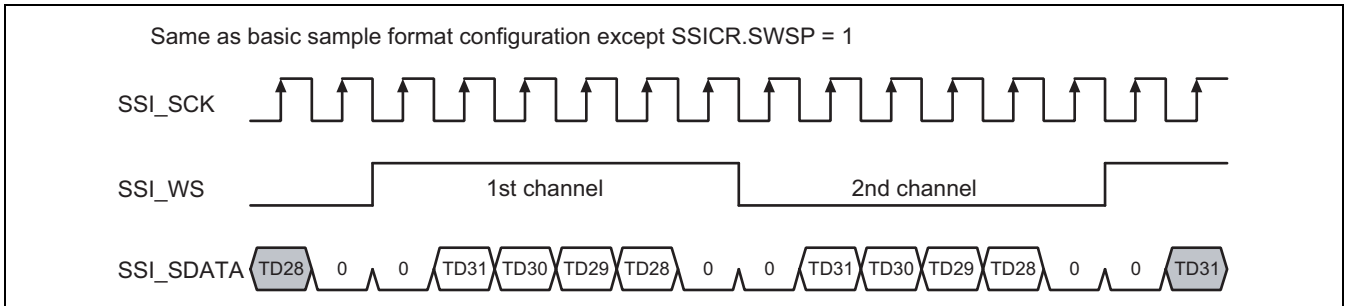


**Figure 32A.13 Basic Sample Format  
(Transmit Mode with Example System/Data Word Length)**

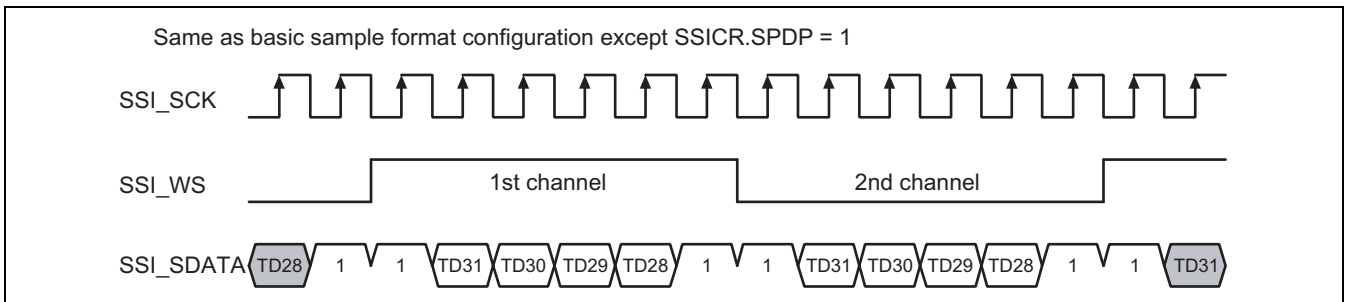
Figure 32A.13 uses a system word length of 6 bits and a data word length of 4 bits. These settings are not possible with the SSI module but are used only for clarification of the other configuration bits.



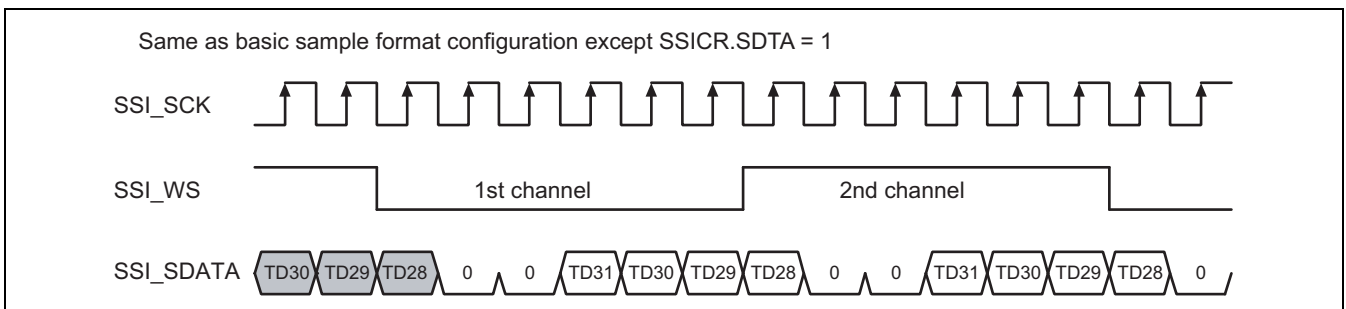
**Figure 32A.14 Inverted Clock**



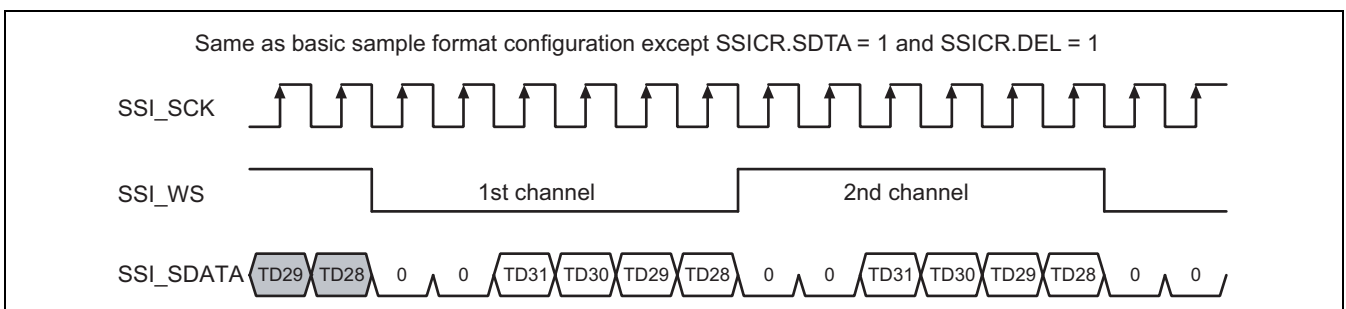
**Figure 32A.15 Inverted Word Select**



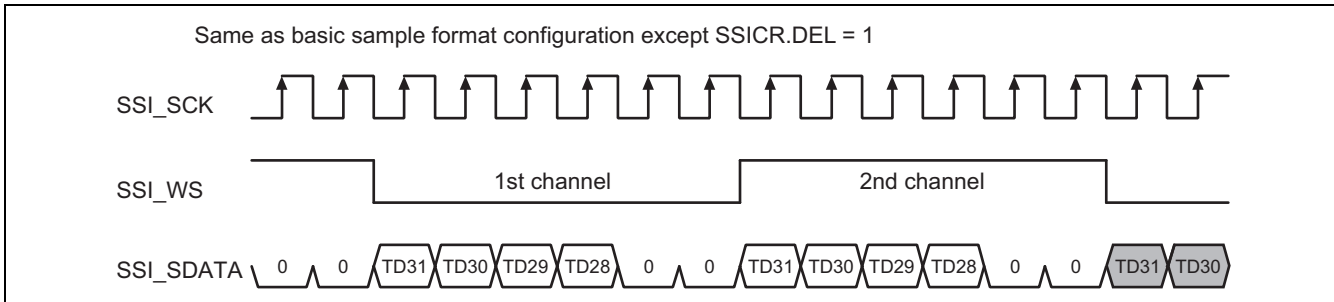
**Figure 32A.16 Inverted Padding Polarity**



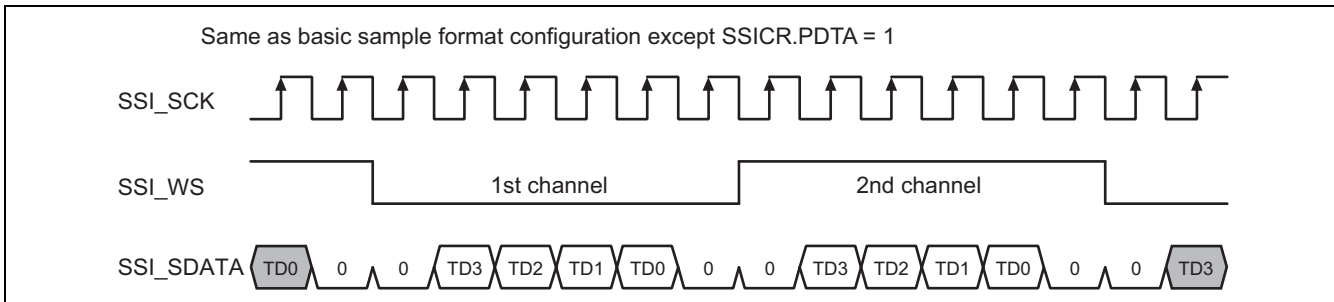
**Figure 32A.17 Transmitting and Receiving in the Order of Padding Bits and Serial Data; with Delay**



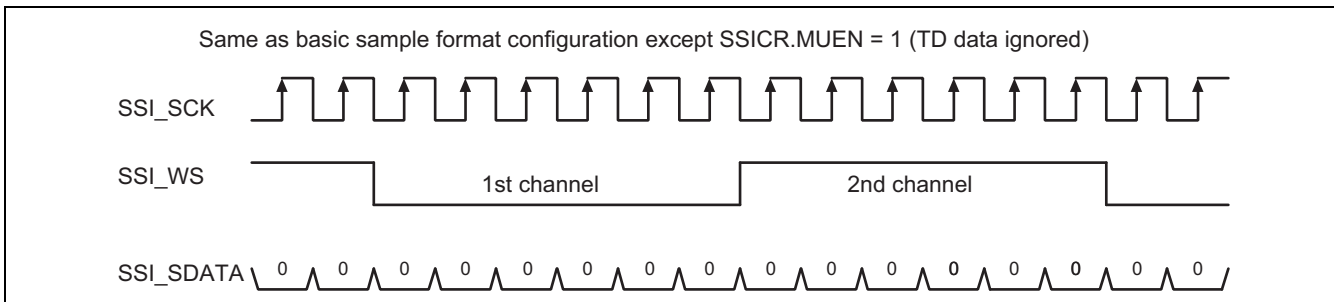
**Figure 32A.18 Transmitting and Receiving in the Order of Padding Bits and Serial Data; without Delay**



**Figure 32A.19 Transmitting and Receiving in the Order of Serial Data and Padding Bits; without Delay**



**Figure 32A.20 Parallel Right-Aligned with Delay**

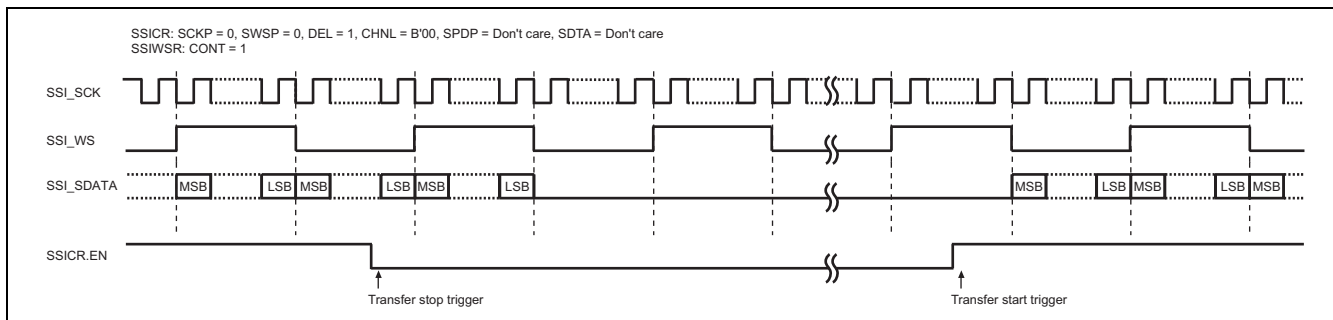


**Figure 32A.21 Mute Enabled**

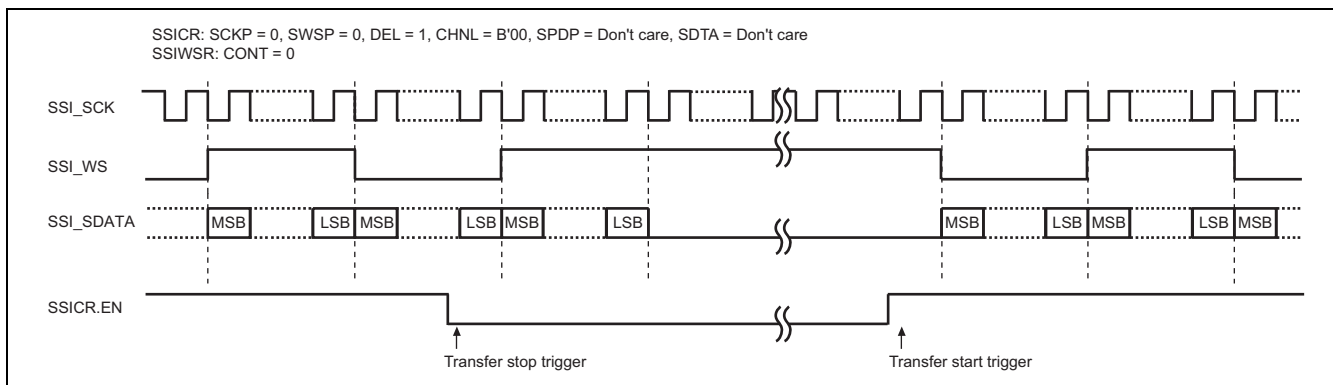
**(11) WS continue function**

The WS continue function is used to output SSI\_WS signal continuously regardless of whether data transfer is enabled or disabled. The WS continue function can be set by using the CONT bit in SSIWSR. This function can be combined with non-compressed mode and master mode only. When this function is enabled, the SSI\_WS signal continues to operate even if the EN bit in SSICR is cleared to 0 (stopping a transfer). When this function is disabled, the SSI\_WS signal operates synchronously with the EN bit.

Figures 32A.22 and 32A.23 show operations when the WS continue function is enabled and disabled, respectively.



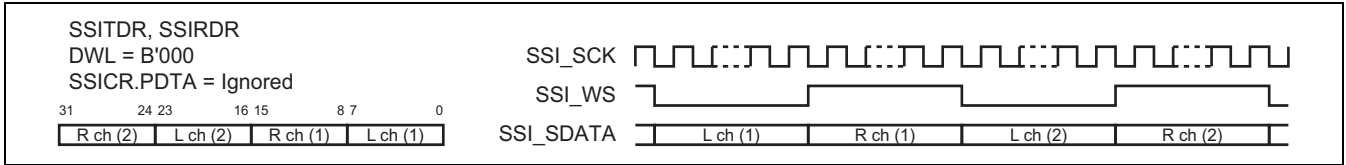
**Figure 32A.22 WS Continue Function Operation (When the Function is Enabled)**



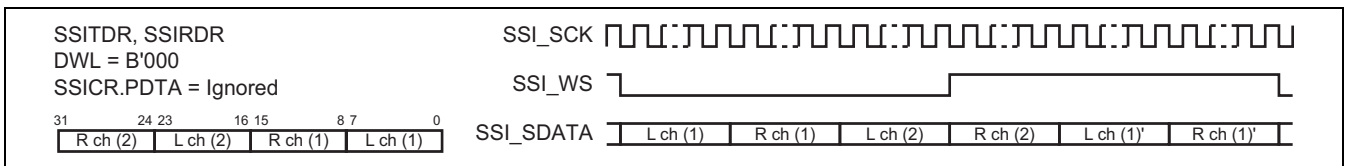
**Figure 32A.23 WS Continue Function Operation (When the Function is Disabled)**

**(12) Bit alignment in transferred data**

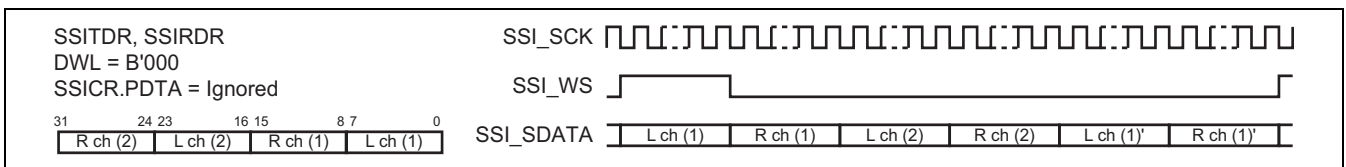
Figures 32A.24 to 32A.36 show the bit alignment in transmit or receive data. Only the MSB first alignment is available. The waveforms in Figures 32A.24 to 32A.36 are setting examples without delay (SSICR.DEL is set to 1, the number of bits specified with SSICR.DWL is the same as that specified with SSICR.SWL).



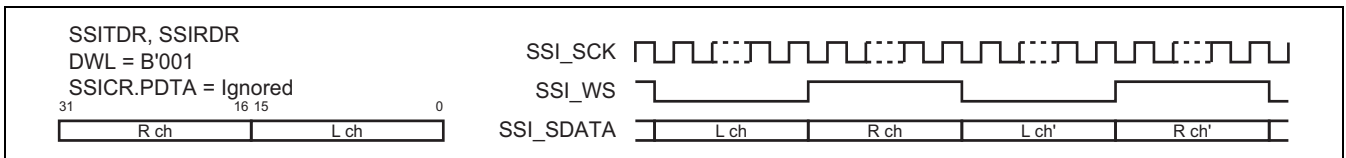
**Figure 32A.24 Bit Alignment in 8-Bit Stereo Format**



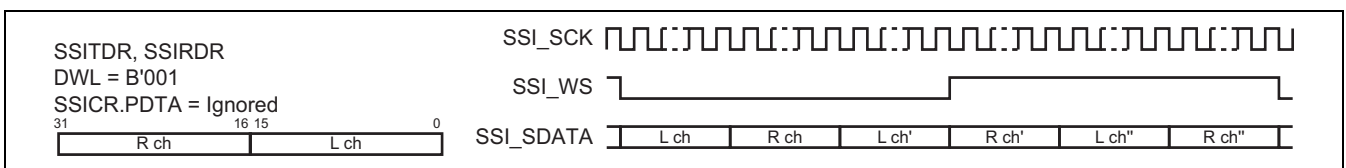
**Figure 32A.25 Bit Alignment in 8-Bit Multi-Channel Format (Three Channels)**



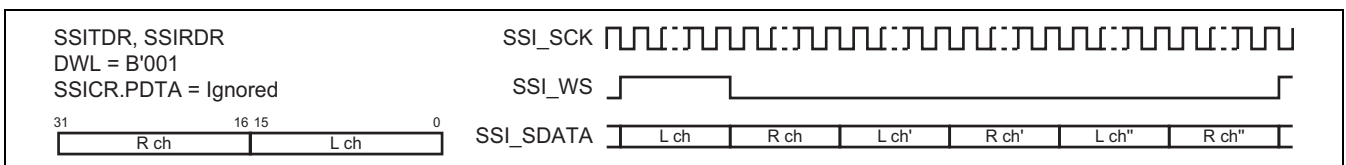
**Figure 32A.26 Bit Alignment in 8-Bit TDM Format (Six System Words)**



**Figure 32A.27 Bit Alignment in 16-Bit Stereo Format**



**Figure 32A.28 Bit Alignment in 16-Bit Multi-Channel Format (Three Channels)**

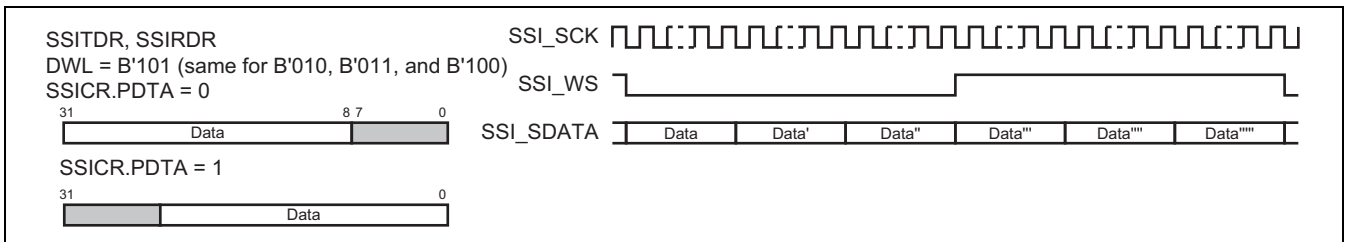


**Figure 32A.29 Bit Alignment in 16-Bit TDM Format (Six System Words)**

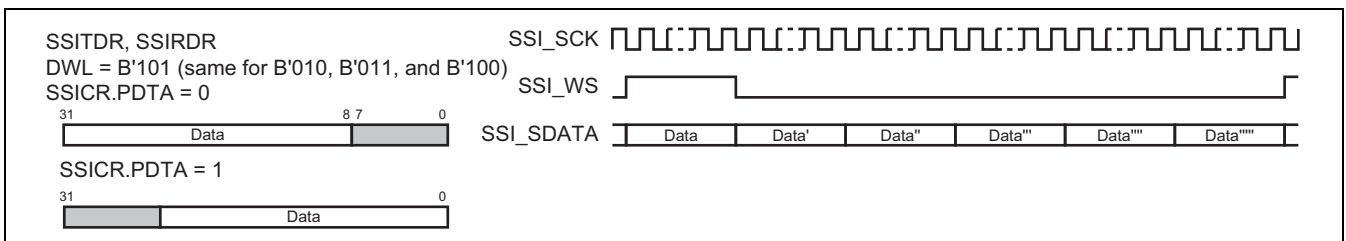




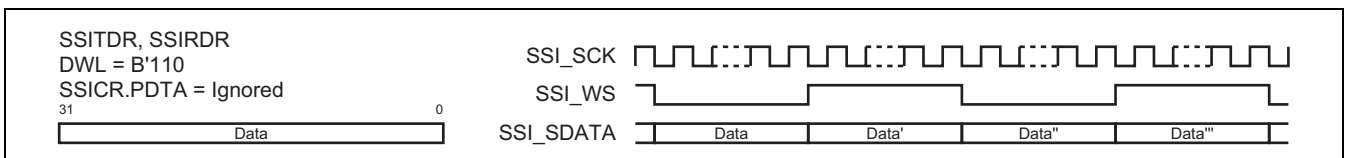
**Figure 32A.30 Bit Alignment in 18-/20-/22-/24-Bit Stereo Format**



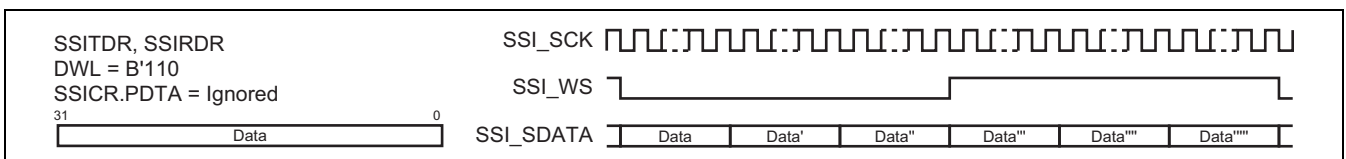
**Figure 32A.31 Bit Alignment in 18-/20-/22-/24-Bit Multi-Channel Format (Three Channels)**



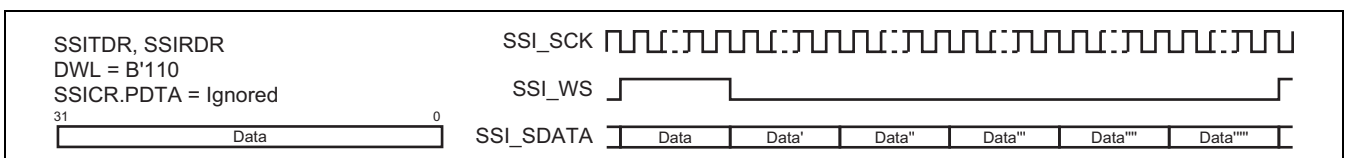
**Figure 32A.32 Bit Alignment in 18-/20-/22-/24-Bit TDM Format (Six System Words)**



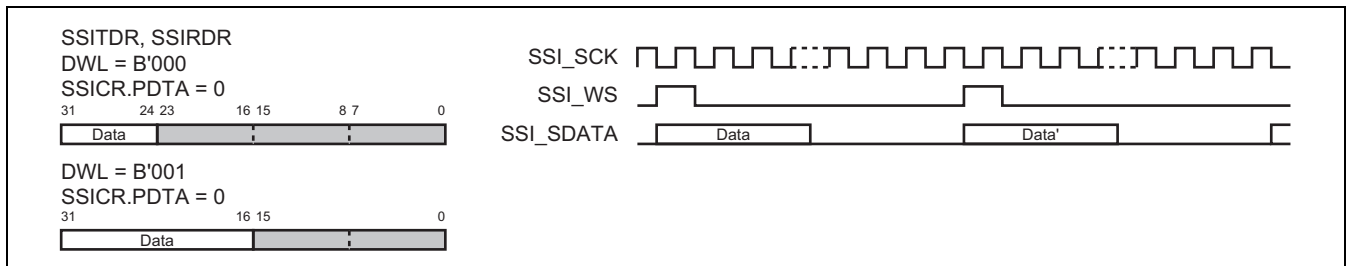
**Figure 32A.33 Bit Alignment in 32-Bit Stereo Format**



**Figure 32A.34 Bit Alignment in 32-Bit Multi-Channel Format (Three Channels)**



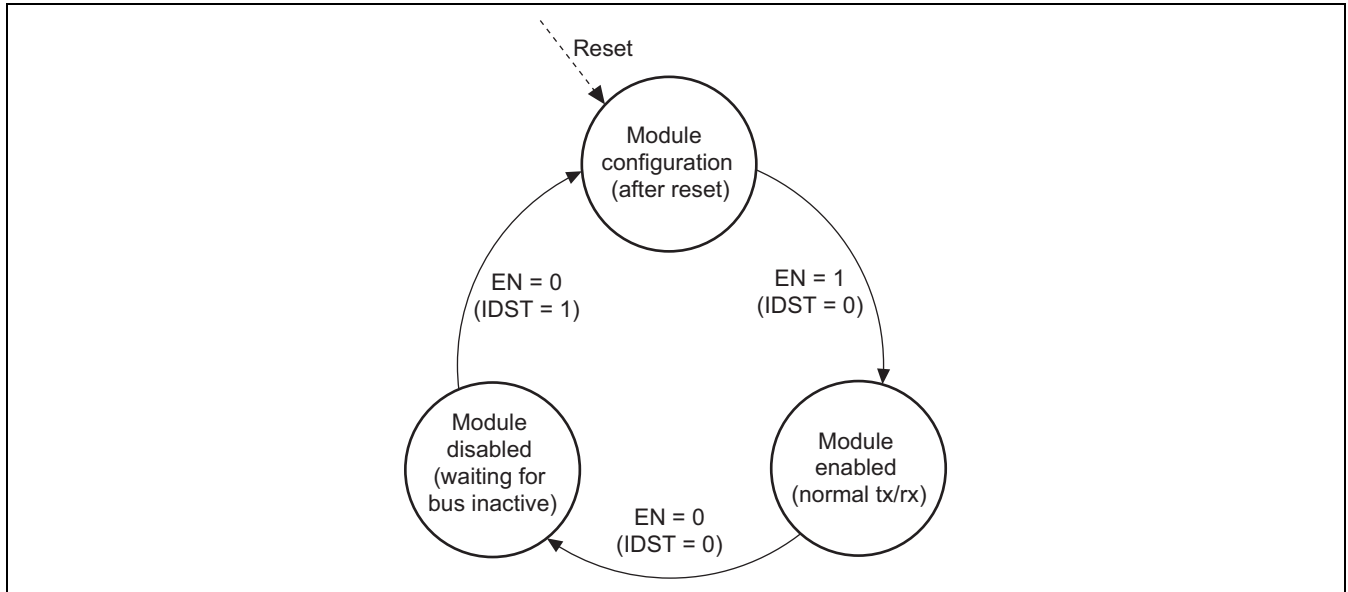
**Figure 32A.35 Bit Alignment in 32-Bit TDM Format (Six System Words)**



**Figure 32A.36 Bit Alignment in 8-/16-Bit Monaural Format**

### 32A.3.3 Operating Modes

There are three modes of operation: configuration, module enabled and module disabled. Figure 32A.37 shows how the module enters each of these modes.



**Figure 32A.37 Operating Modes**

#### (1) Configuration mode

This mode is entered after the module is released from reset. All required configuration fields in the control register should be defined in this mode, before the SSI module is enabled by setting the EN bit.

Setting the EN bit causes the module to enter the module enabled mode.

#### (2) Module enabled mode

Operation of the module in this mode is dependent on the operating mode selected. For details, refer to section 32A.3.4, Transmit Operation and section 32A.3.5, Receive Operation, below.

### 32A.3.4 Transmit Operation

Transmission can be controlled either by DMA or interrupt.

DMA control is preferred to reduce the processor load. In DMA control mode, the processor will only receive interrupts if there is an underflow or overflow of data or the DMAC has finished its transfer.

The alternative method is using the interrupts that the SSI module generates to supply data as required. This mode has a higher interrupt load as the module is only double buffered and will require data to be written at least every system word period.

When disabling the module, the SSI clock\* must remain present until the SSI module is in idle state, indicated by the SSISR.IIRQ bit.

Figure 32A.38 shows the transmit operation in DMA control mode, and Figure 32A.39 shows the transmit operation in interrupt control mode.

Note: \* Input clock from the SSI\_SCK pin when SCKD = 0.  
Input clock from the CLK\_FS pin when SCKD = 1.

Use the flowcharts in Figures 32A.38 and 32A.39 when bits ind9 to ind0, which are covered in the description of SSI mode register 0 (SSI\_MODE0) in section 32, Serial Sound Interface Unit (SSIU), are set to 1 (independent SSI transfer).

(1) Transmission using DMA controller

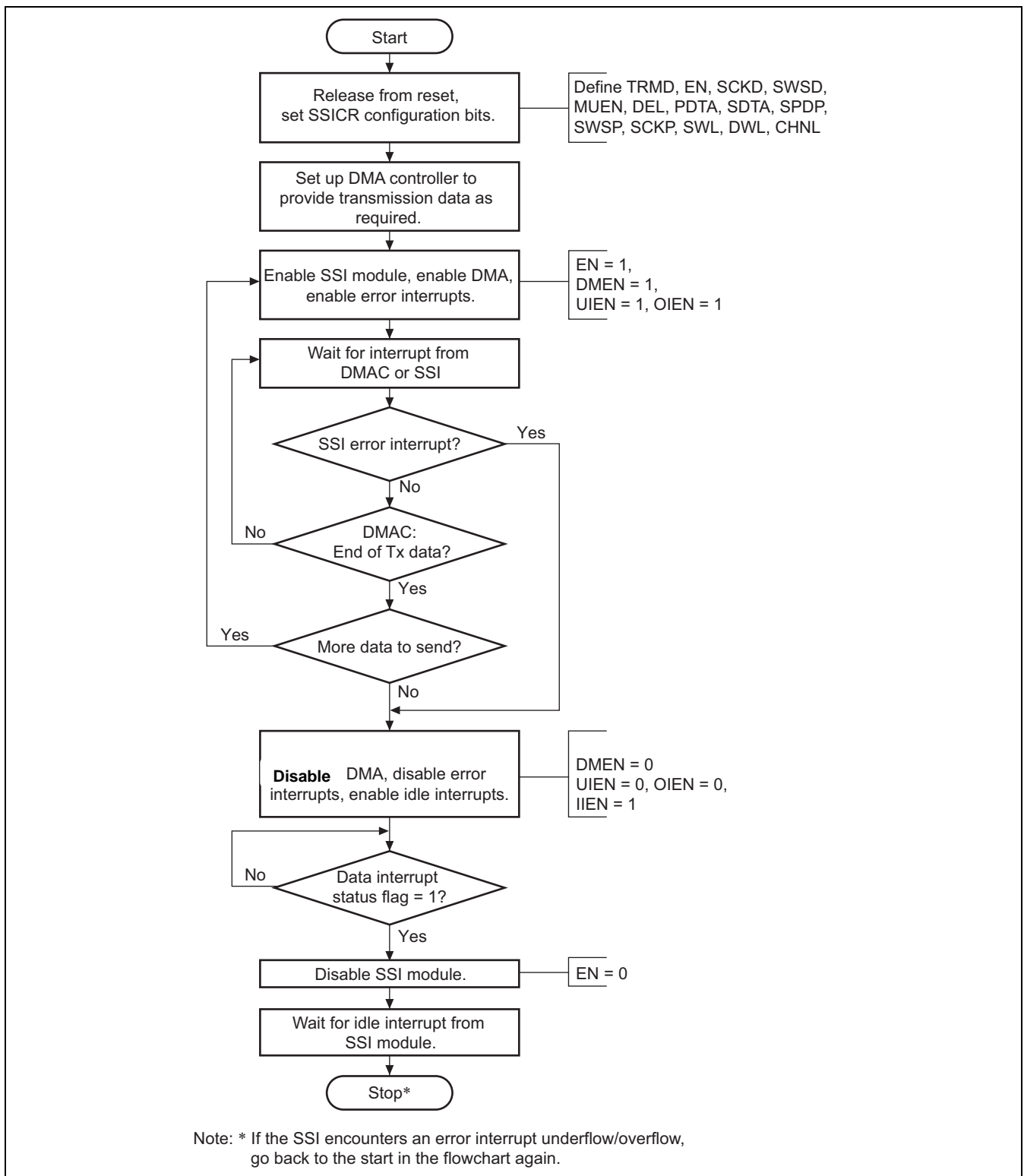


Figure 32A.38 Transmission Using DMA Controller

(2) Transmission using interrupt data flow control

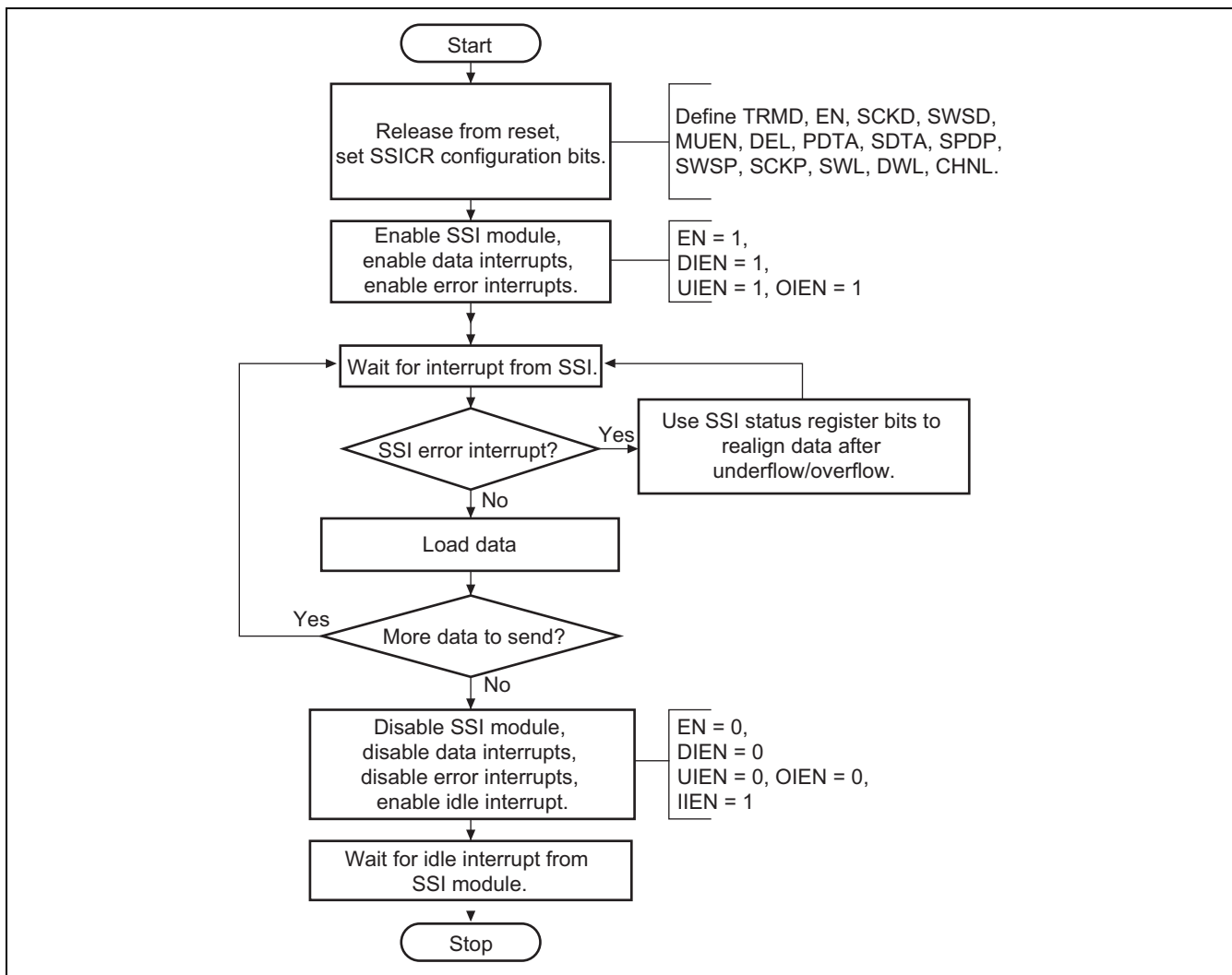


Figure 32A.39 Transmission Using Interrupt Data Flow Control

### 32A.3.5 Receive Operation

Like transmission, reception can be controlled either by DMA or interrupt.

Figures 32A.40 and 32A.41 show the flow of operation.

When disabling the SSI module, the SSI clock\* must be kept supplied until the SSISR.IIRQ bit is in idle state.

Note: \* Input clock from the SSI\_SCK pin when SCKD = 0.  
Input clock from the CLK\_FS pin when SCKD = 1.

Use the flowcharts in Figures 32A.40 and 32A.41 when bits ind9 to ind0, which are covered in the description of SSI mode register 0 (SSI\_MODE0) in section 32, Serial Sound Interface Unit (SSIU), are set to 1 (independent SSI transfer).

(1) Reception using DMA controller

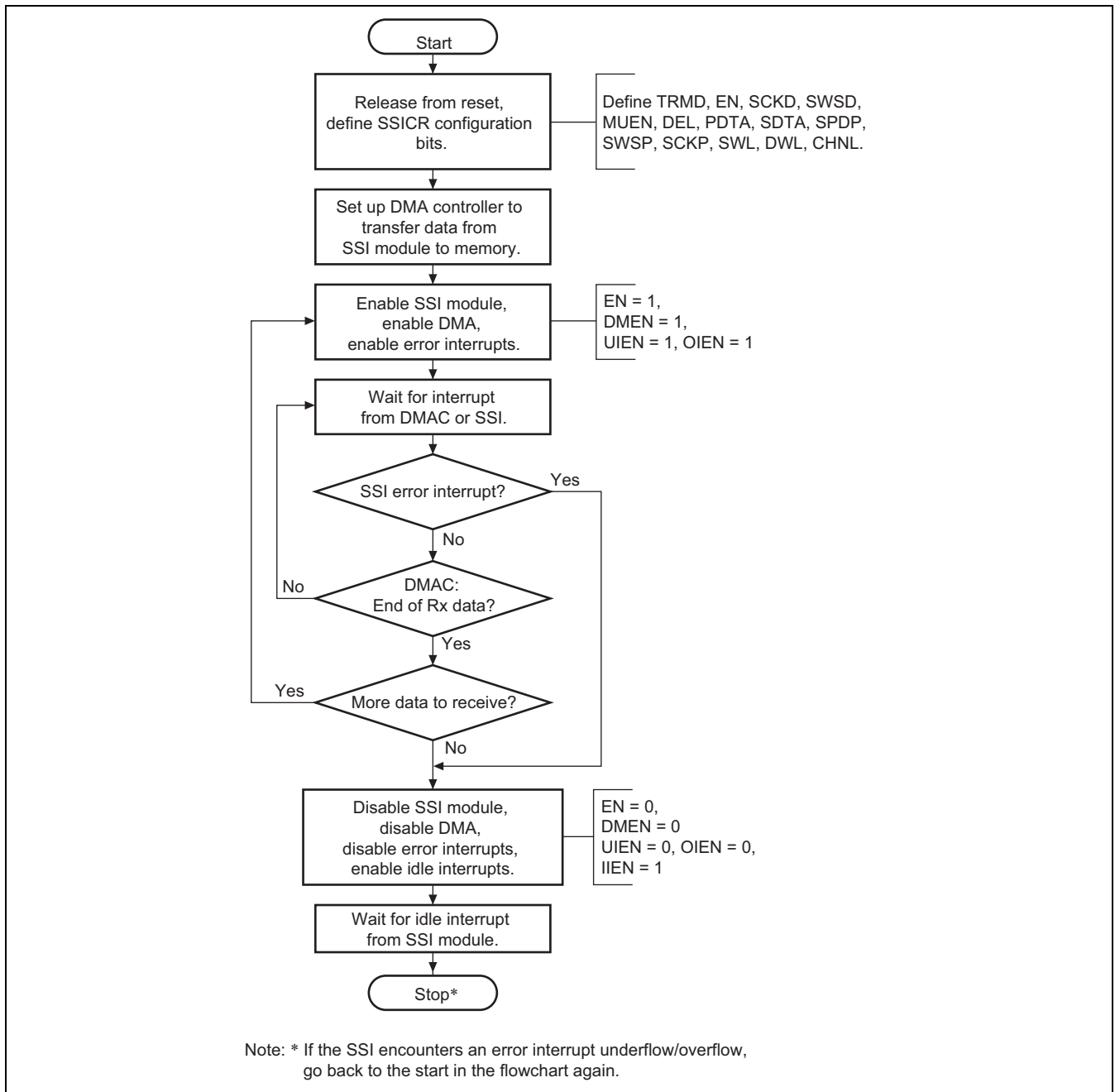


Figure 32A.40 Reception Using DMA Controller



(2) Reception using interrupt data flow control

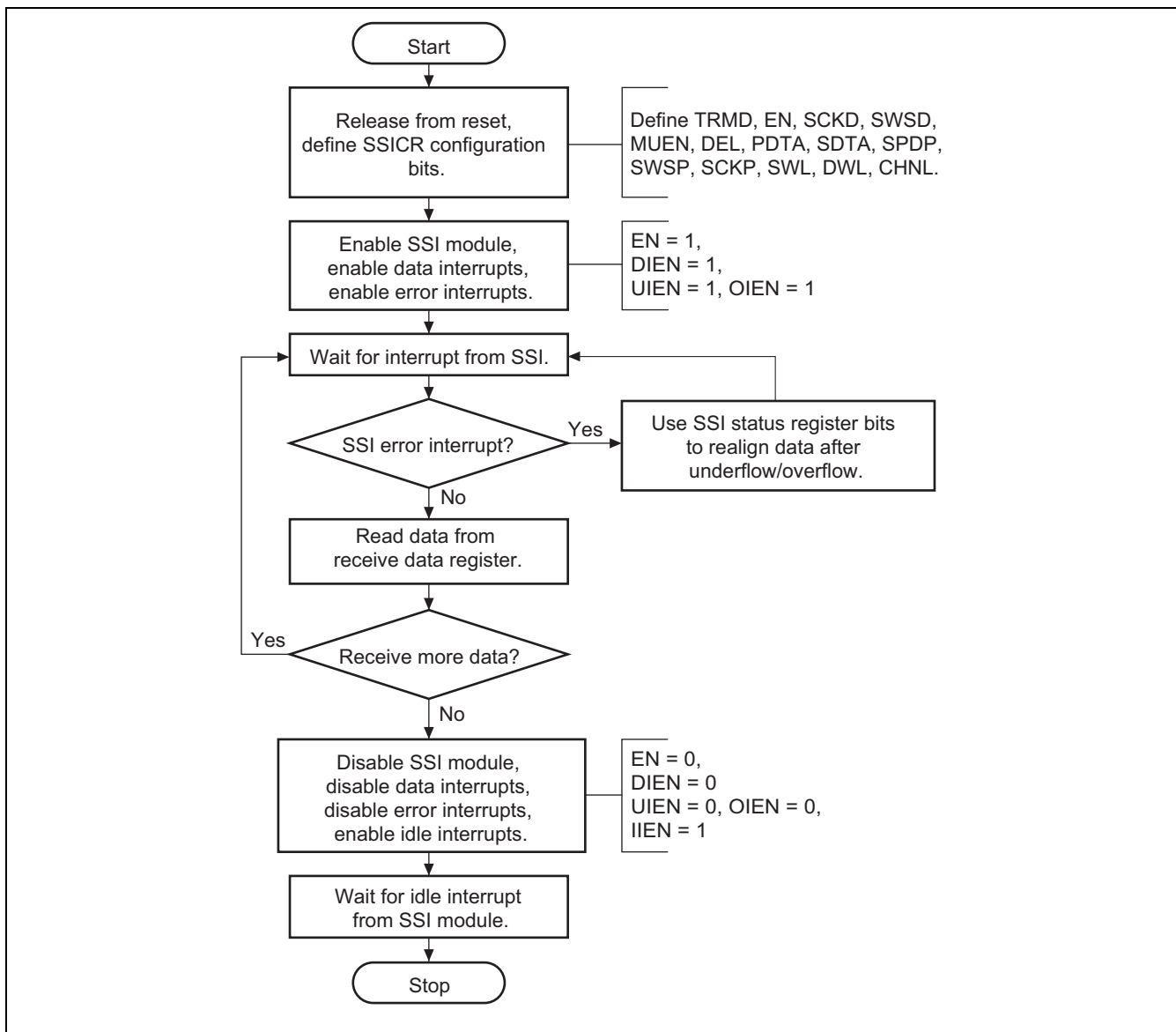


Figure 32A.41 Reception Using Interrupt Data Flow Control

### 32A.3.6 Serial Bit Clock Control

This function is used to control and select which clock is used for the serial bus interface.

If the serial clock direction is set to input (SSICR.SCKD = 0), the SSI module is in clock slave mode and the shift register uses the bit clock that was input to the SSI\_SCK pin.

If the serial clock direction is set to output (SSICR.SCKD = 1), the SSI module is in clock master mode, and the shift register uses the bit clock that is input from the CLK\_FS pin or the bit clock that is obtained by dividing the input from the CLK\_FS pin. In the latter case, the clock input from the CLK\_FS pin is divided by the ratio in the serial oversampling clock divide ratio (CKDV) in SSICR and used as the bit clock in the shift register.

In either case, the SSI\_SCK pin output is the same as the bit clock.

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

## 32A.4 Usage Notes

### 32A.4.1 Limitations from Overflow during Receive DMA Operation

If an overflow occurs while the receive DMA is in operation, the module should be restarted. The receive buffer in the SSI consists of 32-bit registers that share the L and R channels. Therefore, data to be received at the L channel may sometimes be received at the R channel if an overflow occurs, for example, under the following condition: the control register (SSICR) has a 32-bit setting for both data word length (DWL2 to DWL0) and system word length (SWL2 to SWL).

If an overflow is confirmed with the overflow error interrupt or overflow error status flag (SSISR.OIRQ), write 0 to the EN and DMEN bits in SSICR to disable DMA in the SSI module, thus stopping the operation (In this case, the controller setting should also be stopped). After this, write 0 to the OIRQ bit in SSISR to clear the overflow status, set DMA again and restart the transfer.

### 32A.4.2 Limitations on Combinations of Modes Related to Common Pins to SSI7 and SSI8

Table 32A.5 shows the available combinations of operating modes for SSI7 and SSI8. Operating modes can be set with the control registers for the SSI7 and SSI8 (SSICR).

**Table 32A.5 Usable Operating Mode Combinations for SSI7 and SSI8**

No.	Operating Mode		Operating Mode of External Device		Function
	SSI7	SSI8	SSI7 Side	SSI8 Side	
1	Slave	Slave	Master	Slave	SSI7 and SSI8 operate synchronously with SSI_WS78 and SSI_SCK78 input.
			Slave	Master	
			Slave	Slave	
2	Master	Slave	Slave	Slave	SSI8 and an external device operate synchronously with WS and SCK of SSI7.
3	Slave	Master	—	—	Setting prohibited
4	Master	Master	—	—	Setting prohibited

There are the following limitations on the operating mode combinations shown in Table 32A.5.

For No. 1, SSI\_WS78 and SSI\_SCK78 should be input before either of SSI7 or SSI8 starts data transfer.

For No. 2, the SSI7 as the master should start transfer first thus allowing SSI\_WS78 and SSI\_SCK78 to be output, and then the SSI8 as the slave should be used. If the master-side transfer is stopped with the CONT bit in SSIWSR being 0, the slave-side SSI8 should be stopped because SSI\_WS78 is not output.

### 32A.4.3 Limitations on Slave Mode Operation

When this LSI is used in slave mode, in ending a data transfer process, data transfer on this LSI should be stopped (SSICR.EN = 0) before the input word selection signal (SSI\_WS) is stopped.

In slave mode, data transfer is stopped by clearing the EN bit in SSICR (setting to stop transfer) and detecting the falling edge of the word selection signal (SSI\_WS). If the input word selection signal is stopped first, the falling edge of the word selection signal cannot be detected and data transfer cannot be ended successfully.

#### 32A.4.4 Limitations on Changes to Settings

The SSI\_SCK and SSI\_WS signals are not guaranteed immediately after changes of the WS mode bit in the WS mode register (SSIWSR) and configuration bits in the control register (SSICR). Settings must not be changed dynamically if this would affect any connected device.

#### 32A.4.5 Stopping or Resuming Transmission

Follow the procedure below to stop or resume transmission.

##### Stopping transmission:

1. Set the DMEN bit in SSICR to 0 for stopping transmission.
2. Wait for SSISR.DIRQ = 1 by using polling or interrupts.
3. Set the EN bit in SSICR to 0 to stop transmission.
4. Check that SSISR.IDST is 1.

##### Resuming transmission:

Set DMEN and EN bits in SSICR to 1 for resuming transmission (The DMEN bit should be set to 1 at the same time of or before the EN bit).

## 33. Audio Clock Generator (ADG)

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

### 33.1 Overview

The audio clock generator (ADG) selects and supplies the necessary clock for the SSI, or SCU module. It also divides the frequency of the selected clock and sends it outside the chip.

#### 33.1.1 Features

- Selects the clock signal from the AUDIO\_CLKA, AUDIO\_CLKB, or AUDIO\_CLKC pin or the internal clock and supplies it to the SSI, or SCU module.
- The frequency of the clock signals from the AUDIO\_CLKA, AUDIO\_CLKB, and AUDIO\_CLKC pins and the internal clock can be divided before use.
- The divided clock can be output through the AUDIO\_CLKOUT pin.

Note: The presence or absence of pins depends on the product. For details, see Table 33.1.

33.1.2 Block Diagram

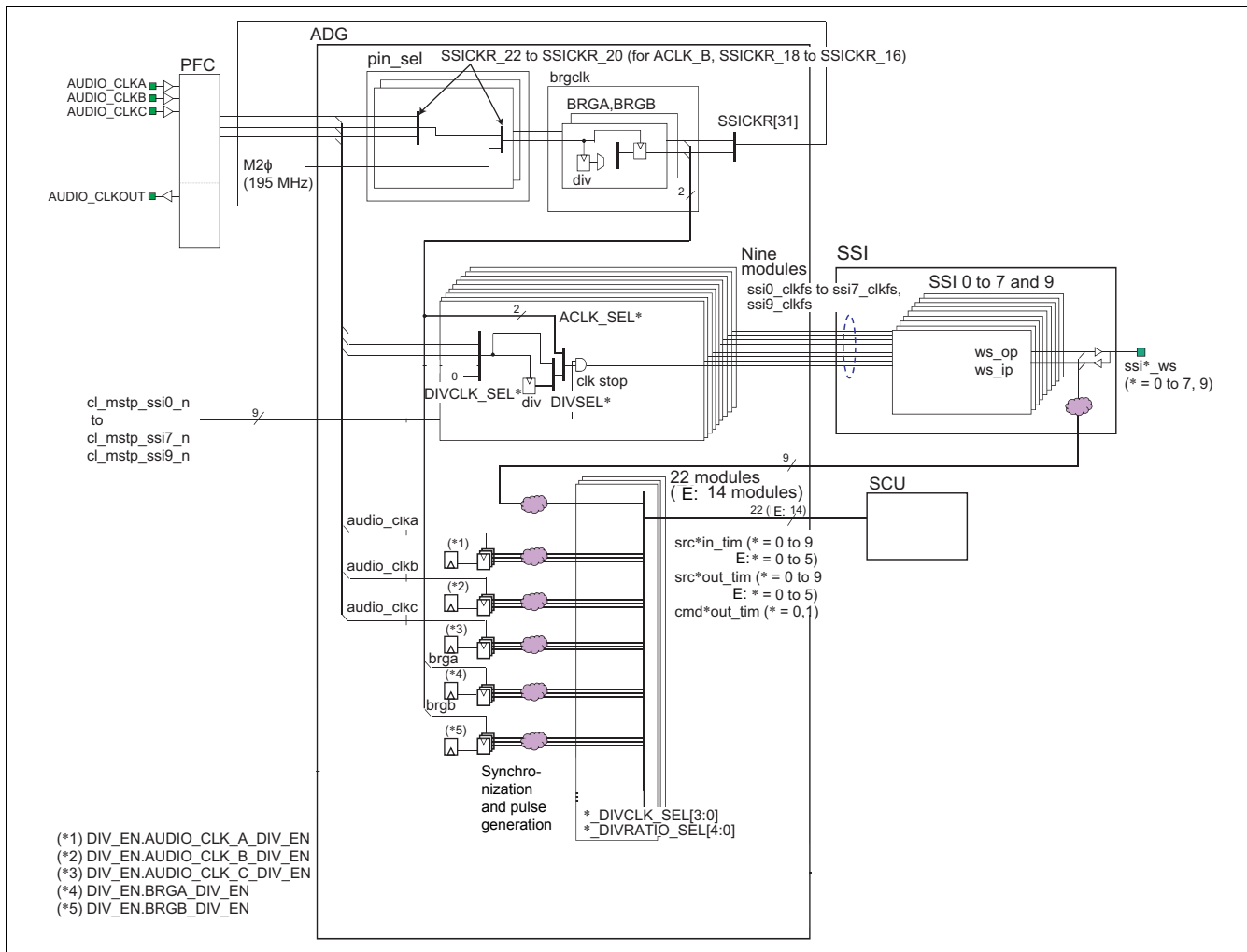


Figure 33.1 Block Diagram

### 33.1.3 External Pins

**Table 33.1 Pin Configuration**

Pin Name	I/O	Function	RZ/G Series Products			
			RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
AUDIO_CLKA	Input	AUDIO CLOCK A	√	√	√	√
AUDIO_CLKB	Input	AUDIO CLOCK B	√	√	√	√
AUDIO_CLKC	Input	AUDIO CLOCK C	√	√	√	√
AUDIO_CLKOUT	Output	AUDIO CLOCK OUT	√	√	√	√
		AUDIO CLOCK OUT_B	√	—	—	√
		AUDIO CLOCK OUT_C	√	—	—	√
		AUDIO CLOCK OUT_D	√	—	—	—

### 33.1.4 Register Configuration

Table 33.2 shows the register configuration. The base address is H'EC5A\_0000. Do not write to any addresses other than listed below. Operations cannot be guaranteed if writing is attempted. Values read from addresses other than those listed below are undefined.

**Table 33.2 Register Configuration**

Name	Abbreviation	R/W	Address	Initial Value	Access size	RZ/G Series Products			
						RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
BRGA baud rate setting register	BARRA	R/W	H'000	H'0000_00FF	32	√	√	√	√
BRGB baud rate setting register	BRRB	R/W	H'004	H'0000_00FF	32	√	√	√	√
Clock select register	SSICKR	R/W	H'008	H'2300_0000	32	√	√	√	√
Audio clock select register 0	AUDIO_CLK_SEL0	R/W	H'00C	H'0000_0000	32	√	√	√	√
Audio clock select register 1	AUDIO_CLK_SEL1	R/W	H'010	H'0000_0000	32	√	√	√	√
Audio clock select register 2	AUDIO_CLK_SEL2	R/W	H'014	H'0000_0000	32	√	√	√	√
Audio clock frequency division enable register	DIV_EN	R/W	H'030	H'0000_0000	32	√	√	√	√
SRC input timing select register 0	SRCIN_TIMSEL0	R/W	H'034	H'0000_0000	32	√	√	√	√*
SRC input timing select register 1	SRCIN_TIMSEL1	R/W	H'038	H'0000_0000	32	√	√	√	√
SRC input timing select register 2	SRCIN_TIMSEL2	R/W	H'03C	H'0000_0000	32	√	√	√	√
SRC input timing select register 3	SRCIN_TIMSEL3	R/W	H'040	H'0000_0000	32	√	√	√	√*
SRC input timing select register 4	SRCIN_TIMSEL4	R/W	H'044	H'0000_0000	32	√	√	√	√*
SRC output timing select register 0	SRCOUT_TIMSEL0	R/W	H'048	H'0000_0000	32	√	√	√	√*
SRC output timing select register 1	SRCOUT_TIMSEL1	R/W	H'04C	H'0000_0000	32	√	√	√	√
SRC output timing select register 2	SRCOUT_TIMSEL2	R/W	H'050	H'0000_0000	32	√	√	√	√
SRC output timing select register 3	SRCOUT_TIMSEL3	R/W	H'054	H'0000_0000	32	√	√	√	√*
SRC output timing select register 4	SRCOUT_TIMSEL4	R/W	H'058	H'0000_0000	32	√	√	√	√*
CMD output timing select register	CMDOUT_TIMSEL	R/W	H'05C	H'0000_0000	32	√	√	√	√



Note: \* Some restrictions apply.

## 33.2 Register Descriptions

[Legend for Register Description]

Initial value: Register value after a reset.

—: Undefined value

R/W: Bit or field is readable and writable. The written value can be read.

All registers are accessed in longword units.

### 33.2.1 BRGA Baud Rate Setting Register (BARR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

**Function:** BARR is a 32-bit readable/writable register that specifies the baud rate for ACLK\_A (see Table 33.3).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	CKS[1:0]		BARR[7:0]							
Initial value:	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
R/W:	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 10	—	All 0	R	Reserved The initial value is always read from these bits. The write value should always be the initial value.
9, 8	CKS[1:0]	00	R/W	These bits specify the clock source for the on-chip baud rate generator. 00: ACLK_A 01: ACLK_A/4 10: ACLK_A/16 11: ACLK_A/64
7 to 0	BARR[7:0]	H'FF	R/W	These bits specify the division ratio. For details, see Table 33.3. Note: Although a 5.951-kHz to 97.5-MHz clock can be generated from the internal clock, set the division ratio here so that a maximum of 25-MHz clock should be obtained.

**Table 33.3 Division Ratio for BRGA**

<b>BRGA Operating Clock (CKS[1], CKS[0])</b>	<b>Division Ratio BRGA (N = 0 to 255)</b>	<b>Calculating Formula</b>
ACLK_A	1/2, 1/4, 1/6, ..., 1/512	$1 / (2(N + 1))$
ACLK_A/4	1/8, 1/16, 1/24, ..., 1/2048	$1 / (8(N + 1))$
ACLK_A/16	1/32, 1/64, 1/96, ..., 1/8192	$1 / (32(N + 1))$
ACLK_A/64	1/128, 1/256, 1/384, ..., 1/32768	$1 / (128(N + 1))$

### 33.2.2 BRGB Baud Rate Setting Register (BRRB)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

**Function:** BRRB is a 32-bit readable/writable register that specifies the baud rate for ACLK\_B (see Table 33.4).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	CKS[1:0]	BRRB[7:0]								
Initial value:	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
R/W:	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 10	—	All 0	R	Reserved The initial value is always read from these bits. The write value should always be the initial value.
9, 8	CKS[1:0]	00	R/W	These bits specify the clock source for the on-chip baud rate generator. 00: ACLK_B 01: ACLK_B/4 10: ACLK_B/16 11: ACLK_B/64
7 to 0	BRRB[7:0]	H'FF	R/W	These bits specify the division ratio. For details, see Table 33.4. Note: Although a 5.951-kHz to 97.5-MHz clock can be generated from the internal clock, set the division ratio here so that a maximum of 25-MHz clock should be obtained.

**Table 33.4 Division Ratio for BRGB**

BRGB Operating Clock (CKS[1], CKS[0])	Division Ratio BRRB (N = 0 to 255)	Calculating Formula
ACLK_B	1/2, 1/4, 1/6, ..., 1/512	1 / (2(N + 1))
ACLK_B/4	1/8, 1/16, 1/24, ..., 1/2048	1 / (8(N + 1))
ACLK_B/16	1/32, 1/64, 1/96, ..., 1/8192	1 / (32(N + 1))
ACLK_B/64	1/128, 1/256, 1/384, ..., 1/32768	1 / (128(N + 1))

### 33.2.3 Clock Select Register (SSICKR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Note: \* Some restrictions apply.

**Function:** SSICKR selects the clocks input to and output from the ADG.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SSICKR_31	—	—	—	—	—	—	—	—	SSICKR_22	SSICKR_21	SSICKR_20	—	SSICKR_18	SSICKR_17	SSICKR_16
Initial value:	0	0	1	0	0	0	1	1	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31	SSICKR_31	0	R/W	<p>This bit selects the clock signal output to the AUDIO_CLKOUT, AUDIO_CLKOUT_B, AUDIO_CLKOUT_C, or AUDIO_CLKOUT_D external pin.</p> <ul style="list-style-type: none"> <li>AUDIO_CLKOUT, AUDIO_CLKOUT_B, AUDIO_CLKOUT_C, AUDIO_CLKOUT_D [For RZ/G1H]</li> <li>AUDIO_CLKOUT [For RZ/G1M, N]</li> <li>AUDIO_CLKOUT, AUDIO_CLKOUT_B, AUDIO_CLKOUT_C [For RZ/G1E]</li> </ul> <p>0: BRGA output clock 1: BRGB output clock</p>
30 to 23	—	H'46	R	<p>Reserved</p> <p>The initial value is always read from these bits. The write value should always be the initial value.</p>
22	SSICKR_22	0	R/W	These bits select the clock signal input to the BRGA.
21	SSICKR_21	0		000: AUDIO_CLKA
20	SSICKR_20	0		001: AUDIO_CLKB
				01x: M2 $\phi$ (195 MHz)
				100: AUDIO_CLKC
				101: Fixed at 0
				11x: Fixed at 0
				x = Don't care
19	—	0	R	<p>Reserved</p> <p>The initial value is always read from this bit. The write value should always be the initial value.</p>

Bit	Bit Name	Initial Value	R/W	Description
18	SSICKR_18	0	R/W	These bits select the clock signal input to the BRGB.
17	SSICKR_17	0		000: AUDIO_CLKA
16	SSICKR_16	0		001: AUDIO_CLKB 01x: M2 $\phi$ (195 MHz) 100: AUDIO_CLKC 101: Fixed at 0 11x: Fixed at 0 x = Don't care
15 to 0	—	All 0	R	Reserved The initial value is always read from these bits. The write value should always be the initial value.

### 33.2.4 Audio Clock Select Register 0 (AUDIO\_CLK\_SEL0)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Note: \* Some restrictions apply.

**Function:** AUDIO\_CLK\_SEL0 selects the clocks for the SRU (for SSI0 to SSI3).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DIVSEL_SSI3 [1:0]		ACLK_SEL_SSI3 [1:0]		DIVSEL2_SSI3		DIVCLK_SEL_SSI3 [2:0]		DIVSEL_SSI2 [1:0]		ACLK_SEL_SSI2 [1:0]		DIVSEL2_SSI2		DIVCLK_SEL_SSI2 [2:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DIVSEL_SSI1 [1:0]		ACLK_SEL_SSI1 [1:0]		DIVSEL2_SSI1		DIVCLK_SEL_SSI1 [2:0]		DIVSEL_SSI0 [1:0]		ACLK_SEL_SSI0 [1:0]		DIVSEL2_SSI0		DIVCLK_SEL_SSI0 [2:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31, 30	DIVSEL_SSI3 [1:0]	00	R/W	SSI3 Frequency Divider Select
27	DIVSEL2_SSI3	0	R/W	[27], [31:30]: 000: Not divided 001: Divided by 2 010: Divided by 4 011: Divided by 8 100: Divided by 16 101: Divided by 32 110, 111: Fixed at 0
29, 28	ACLK_SEL_SSI3 [1:0]	00	R/W	SSI3 Clock Select 00: DIVCLK 01: BRGA output clock 10: BRGB output clock 11: Setting prohibited

Bit	Bit Name	Initial Value	R/W	Description
26 to 24	DIVCLK_SEL_SSI3 [2:0]	000	R/W	SSI3 Clock Select 000: Fixed at 0 001: AUDIO_CLKA 010: AUDIO_CLKB 011: AUDIO_CLKC Others: Setting prohibited
23, 22	DIVSEL_SSI2[1:0]	00	R/W	SSI2 Frequency Divider Select
19	DIVSEL2_SSI2	0	R/W	[19], [23:22]: 000: Not divided 001: Divided by 2 010: Divided by 4 011: Divided by 8 100: Divided by 16 101: Divided by 32 110, 111: Fixed at 0
21, 20	ACLK_SEL_SSI2[1:0]	00	R/W	SSI2 Clock Select 00: DIVCLK 01: BRGA output clock 10: BRGB output clock 11: Setting prohibited
18 to 16	DIVCLK_SEL_SSI2 [2:0]	000	R/W	SSI2 Clock Select 000: Fixed at 0 001: AUDIO_CLKA 010: AUDIO_CLKB 011: AUDIO_CLKC Others: Setting Prohibited
15, 14	DIVSEL_SSI1[1:0]	00	R/W	SSI1 Frequency Divider Select
11	DIVSEL2_SSI1	0	R/W	[11], [15:14]: 000: Not divided 001: Divided by 2 010: Divided by 4 011: Divided by 8 100: Divided by 16 101: Divided by 32 110, 111: Fixed at 0
13, 12	ACLK_SEL_SSI1[1:0]	00	R/W	SSI1 Clock Select 00: DIVCLK 01: BRGA output clock 10: BRGB output clock 11: Setting prohibited

Bit	Bit Name	Initial Value	R/W	Description
10 to 8	DIVCLK_SEL_SSI1 [2:0]	000	R/W	SSI1 Clock Select 000: Fixed at 0 001: AUDIO_CLKA 010: AUDIO_CLKB 011: AUDIO_CLKC Others: Setting Prohibited
7, 6	DIVSEL_SSI0[1:0]	00	R/W	SSI0 Frequency Divider Select
3	DIVSEL2_SSI0	0	R/W	[3], [7:6]: 000: Not divided 001: Divided by 2 010: Divided by 4 011: Divided by 8 100: Divided by 16 101: Divided by 32 110, 111: Fixed at 0
5, 4	ACLK_SEL_SSI0[1:0]	00	R/W	SSI0 Clock Select 00: DIVCLK 01: BRGA output clock 10: BRGB output clock 11: Setting prohibited
2 to 0	DIVCLK_SEL_SSI0 [2:0]	000	R/W	SSI0 Clock Select 000: Fixed at 0 001: AUDIO_CLKA 010: AUDIO_CLKB 011: AUDIO_CLKC Others: Setting Prohibited



### 33.2.5 Audio Clock Select Register 1 (AUDIO\_CLK\_SEL1)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Note: \* Some restrictions apply.

**Function:** AUDIO\_CLK\_SEL1 selects the clocks for the SRU (for SSI4 to SSI7).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DIVSEL_SSI7 [1:0]		ACLK_SEL_SSI7 [1:0]		DIVSEL2_SSI7		DIVCLK_SEL_SSI7 [2:0]		DIVSEL_SSI6 [1:0]		ACLK_SEL_SSI6 [1:0]		DIVSEL2_SSI6		DIVCLK_SEL_SSI6 [1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DIVSEL_SSI5 [1:0]		ACLK_SEL_SSI5 [1:0]		DIVSEL2_SSI5		DIVCLK_SEL_SSI5 [2:0]		DIVSEL_SSI4 [1:0]		ACLK_SEL_SSI4 [1:0]		DIVSEL2_SSI4		DIVCLK_SEL_SSI4 [1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31, 30	DIVSEL_SSI7[1:0]	00	R/W	SSI7 Frequency Divider Select
27	DIVSEL2_SSI7	0	R/W	[27], [31:30]: 000: Not divided 001: Divided by 2 010: Divided by 4 011: Divided by 8 100: Divided by 16 101: Divided by 32 110, 111: Fixed at 0
29, 28	ACLK_SEL_SSI7[1:0]	00	R/W	SSI7 Clock Select 00: DIVCLK 01: BRGA output clock 10: BRGB output clock 11: Setting prohibited
26 to 24	DIVCLK_SEL_SSI7 [2:0]	000	R/W	SSI7 Clock Select 000: Fixed at 0 001: AUDIO_CLKA 010: AUDIO_CLKB 011: AUDIO_CLKC Others: Setting Prohibited

Bit	Bit Name	Initial Value	R/W	Description
23, 22	DIVSEL_SSI6[1:0]	00	R/W	SSI6 Frequency Divider Select
19	DIVSEL2_SSI6	0	R/W	[19], [23:22]: 000: Not divided 001: Divided by 2 010: Divided by 4 011: Divided by 8 100: Divided by 16 101: Divided by 32 110, 111: Fixed at 0
21, 20	ACLK_SEL_SSI6[1:0]	00	R/W	SSI6 Clock Select 00: DIVCLK 01: BRGA output clock 10: BRGB output clock 11: Setting prohibited
18 to 16	DIVCLK_SEL_SSI6 [2:0]	000	R/W	SSI6 Clock Select 000: Fixed at 0 001: AUDIO_CLKA 010: AUDIO_CLKB 011: AUDIO_CLKC Others: Setting Prohibited
15, 14	DIVSEL_SSI5[1:0]	00	R/W	SSI5 Frequency Divider Select
11	DIVSEL2_SSI5	0	R/W	[11], [15:14]: 000: Not divided 001: Divided by 2 010: Divided by 4 011: Divided by 8 100: Divided by 16 101: Divided by 32 110, 111: Fixed at 0
13, 12	ACLK_SEL_SSI5[1:0]	00	R/W	SSI5 Clock Select 00: DIVCLK 01: BRGA output clock 10: BRGB output clock 11: Setting prohibited
10 to 8	DIVCLK_SEL_SSI5 [2:0]	000	R/W	SSI5 Clock Select 000: Fixed at 0 001: AUDIO_CLKA 010: AUDIO_CLKB 011: AUDIO_CLKC Others: Setting Prohibited

Bit	Bit Name	Initial Value	R/W	Description
7, 6	DIVSEL_SSI4[1:0]	00	R/W	SSI4 Frequency Divider Select
3	DIVSEL2_SSI4	0	R/W	[3], [7:6]: 000: Not divided 001: Divided by 2 010: Divided by 4 011: Divided by 8 100: Divided by 16 101: Divided by 32 110, 111: Fixed at 0
5, 4	ACLK_SEL_SSI4[1:0]	00	R/W	SSI4 Clock Select 00: DIVCLK 01: BRGA output clock 10: BRGB output clock 11: Setting prohibited
2 to 0	DIVCLK_SEL_SSI4 [2:0]	000	R/W	SSI4 Clock Select 000: Fixed at 0 001: AUDIO_CLKA 010: AUDIO_CLKB 011: AUDIO_CLKC Others: Setting Prohibited

### 33.2.6 Audio Clock Select Register 2 (AUDIO\_CLK\_SEL2)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

**Function:** AUDIO\_CLK\_SEL2 selects the clocks for the SRU (for SSI9).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DIVSEL_SSI9 [1:0]	ACLK_SEL_SSI9 [1:0]	DIVSEL2_SSI9	DIVCLK_SEL_SSI9 [2:0]	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved The initial value is always read from these bits. The write value should always be the initial value.
15, 14	DIVSEL_SSI9[1:0]	00	R/W	SSI9 Frequency Divider Select
11	DIVSEL2_SSI9	0	R/W	[11], [15:14] 000: Not divided 001: Divided by 2 010: Divided by 4 011: Divided by 8 100: Divided by 16 101: Divided by 32 110, 111: Fixed at 0
13, 12	ACLK_SEL_SSI9[1:0]	00	R/W	SSI9 Clock Select 00: DIVCLK 01: BRGA output clock 10: BRGB output clock 11: Setting prohibited
10 to 8	DIVCLK_SEL_SSI9[2:0]	000	R/W	SSI9 Clock Select 000: Fixed at 0 001: AUDIO_CLKA 010: AUDIO_CLKB 011: AUDIO_CLKC Others: Setting Prohibited
7 to 0	—	All 0	R	Reserved The initial value is always read from these bits. The write value should always be the initial value.

### 33.2.7 Audio Clock Frequency Division Enable Register (DIV\_EN)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

**Function:** DIV\_EN enables or disables the AUDIO\_CLK\_A, AUDIO\_CLK\_B, AUDIO\_CLK\_C, BRGA, and BRGB frequency dividers.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	BRGB_DIV_EN	BRGA_DIV_EN	AUDIO_CLK_C_DIV_EN	AUDIO_CLK_B_DIV_EN	AUDIO_CLK_A_DIV_EN	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R

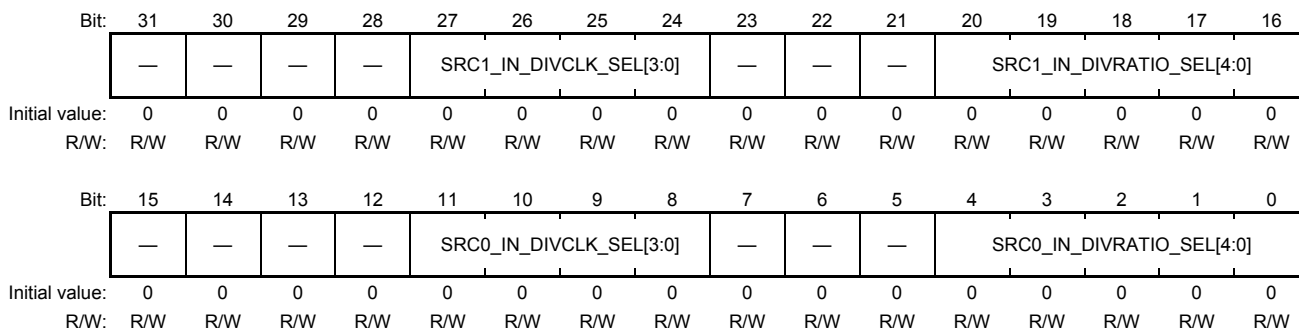
Bit	Bit Name	Initial Value	R/W	Description
31 to 6	—	All 0	R	Reserved The initial value is always read from this bit. The write value should always be the initial value.
5	BRGB_DIV_EN	0	R/W	This bit enables the BRGB frequency divider. 0: Disables frequency division. 1: Divides BRGB into the specified frequency.
4	BRGA_DIV_EN	0	R/W	This bit enables the BRGA frequency divider. 0: Disables frequency division. 1: Divides BRGA into the specified frequency.
3	AUDIO_CLK_C_DIV_EN	0	R/W	This bit enables the AUDIO_CLK_C frequency divider. 0: Disables frequency division. 1: Divides AUDIO_CLK_C into the specified frequency.
2	AUDIO_CLK_B_DIV_EN	0	R/W	This bit enables the AUDIO_CLK_B frequency divider. 0: Disables frequency division. 1: Divides AUDIO_CLK_B into the specified frequency.
1	AUDIO_CLK_A_DIV_EN	0	R/W	This bit enables the AUDIO_CLK_A frequency divider. 0: Disables frequency division. 1: Divides AUDIO_CLK_A into the specified frequency.
0	—	0	R	Reserved The initial value is always read from this bit. The write value should always be the initial value.

### 33.2.8 SRC Input Timing Select Register 0 (SRCIN\_TIMSEL0)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√*

Note: \* Some restrictions apply.

Function: SRCIN\_TIMSEL0 selects the input timing signals for SRC0 and SRC1.



Bit	Bit Name	Initial Value	R/W	Description
31 to 28	—	All 0	R/W	Reserved The write value should always be the initial value.
27 to 24	SRC1_IN_DIVCLK_SEL [3:0]	0000	R/W	SRC1 Input Timing Signal Select 0000: Divided AUDIO_CLK_A 0001: Divided AUDIO_CLK_B 0010: Divided AUDIO_CLK_C 0011: Divided BRGA 0100: Divided BRGB 0101: Setting prohibited 0110: ssi_ws0 0111: ssi_ws1 1000: ssi_ws2 1001: ssi_ws3 1010: ssi_ws4 1011: ssi_ws5 1100: ssi_ws6 1101: ssi_ws7 1110: ssi_ws9 1111: Setting prohibited
23 to 21	—	All 0	R/W	Reserved The write value should always be the initial value.

Bit	Bit Name	Initial Value	R/W	Description
20 to 16	SRC1_IN_DIVRATIO_SEL [4:0]	0_0000	R/W	<p>SRC1 Input Timing Signal Frequency Division Ratio Select</p> <p>These bits select the frequency division ratio for the clock signal selected using SRC1_IN_DIVCLK_SEL[3:0]. Note that ssi_ws signals cannot be divided.</p> <p>0_0000: Divided by 2            0_0001: Divided by 4            0_0010: Divided by 6            0_0011: Divided by 8            0_0100: Divided by 12            0_0101: Divided by 16            0_0110: Divided by 24            0_0111: Divided by 32            0_1000: Divided by 48            0_1001: Divided by 64            0_1010: Divided by 96            0_1011: Divided by 128            0_1100: Divided by 192            0_1101: Divided by 256            0_1110: Divided by 384            0_1111: Divided by 512            1_0000: Divided by 768            1_0001: Divided by 1024            1_0010: Divided by 1536            1_0011: Divided by 2048            1_0100: Divided by 3072            1_0101: Divided by 4096            1_0110: Divided by 6144            1_0111: Divided by 8192            1_1000: Divided by 12288            1_1001: Divided by 16384            1_1010: Divided by 24576            1_1011: Divided by 32768            1_1100: Divided by 49152            1_1101: Divided by 98304            Others: Setting prohibited</p>
15 to 12	—	All 0	R/W	<p>Reserved</p> <p>The write value should always be the initial value.</p>

Bit	Bit Name	Initial Value	R/W	Description
11 to 8	SRC0_IN_DIVCLK_SEL [3:0]	0000	R/W	[RZ/G1H, M, N] SRC0 Input Timing Signal Select 0000: Divided AUDIO_CLK_A 0001: Divided AUDIO_CLK_B 0010: Divided AUDIO_CLK_C 0011: Divided BRGA 0100: Divided BRGB 0101: Setting prohibited 0110: ssi_ws0 0111: ssi_ws1 1000: ssi_ws2 1001: ssi_ws3 1010: ssi_ws4 1011: ssi_ws5 1100: ssi_ws6 1101: ssi_ws7 1110: ssi_ws9 1111: Setting prohibited [RZ/G1E] Reserved
7 to 5	—	All 0	R/W	Reserved The write value should always be the initial value.

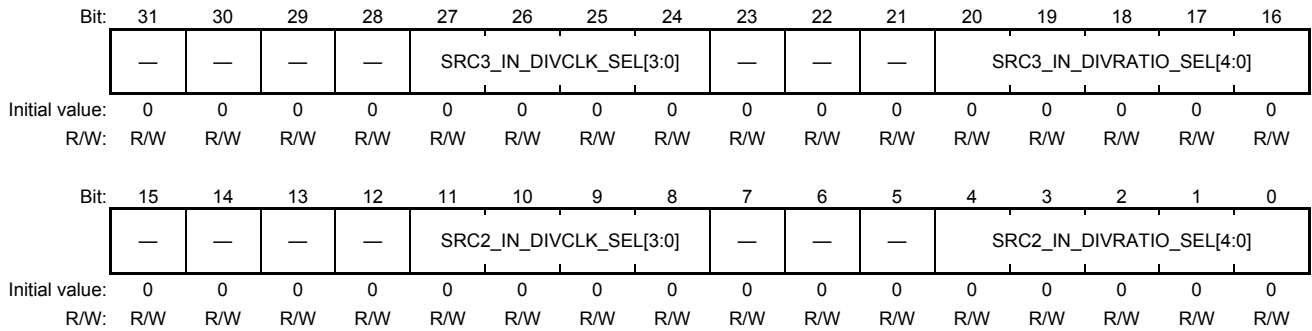


Bit	Bit Name	Initial Value	R/W	Description
4 to 0	SRC0_IN_DIVRATIO_SEL [4:0]	0_0000	R/W	<p>[RZ/G1H, M, N]</p> <p>SRC0 Input Timing Signal Frequency Division Ratio Select</p> <p>These bits select the frequency division ratio for the clock signal selected using SRC0_IN_DIVCLK_SEL[3:0]. Note that ssi_ws signals cannot be divided.</p> <p>0_0000: Divided by 2</p> <p>0_0001: Divided by 4</p> <p>0_0010: Divided by 6</p> <p>0_0011: Divided by 8</p> <p>0_0100: Divided by 12</p> <p>0_0101: Divided by 16</p> <p>0_0110: Divided by 24</p> <p>0_0111: Divided by 32</p> <p>0_1000: Divided by 48</p> <p>0_1001: Divided by 64</p> <p>0_1010: Divided by 96</p> <p>0_1011: Divided by 128</p> <p>0_1100: Divided by 192</p> <p>0_1101: Divided by 256</p> <p>0_1110: Divided by 384</p> <p>0_1111: Divided by 512</p> <p>1_0000: Divided by 768</p> <p>1_0001: Divided by 1024</p> <p>1_0010: Divided by 1536</p> <p>1_0011: Divided by 2048</p> <p>1_0100: Divided by 3072</p> <p>1_0101: Divided by 4096</p> <p>1_0110: Divided by 6144</p> <p>1_0111: Divided by 8192</p> <p>1_1000: Divided by 12288</p> <p>1_1001: Divided by 16384</p> <p>1_1010: Divided by 24576</p> <p>1_1011: Divided by 32768</p> <p>1_1100: Divided by 49152</p> <p>1_1101: Divided by 98304</p> <p>Others: Setting prohibited</p> <hr/> <p>[RZ/G1E] Reserved</p>

### 33.2.9 SRC Input Timing Select Register 1 (SRCIN\_TIMSEL1)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

**Function:** SRCIN\_TIMSEL1 selects the input timing signals for SRC2 and SRC3.



Bit	Bit Name	Initial Value	R/W	Description
31 to 28	—	All 0	R/W	Reserved The write value should always be the initial value.
27 to 24	SRC3_IN_DIVCLK_SEL [3:0]	0000	R/W	SRC3 Input Timing Signal Select 0000: Divided AUDIO_CLK_A 0001: Divided AUDIO_CLK_B 0010: Divided AUDIO_CLK_C 0011: Divided BRGA 0100: Divided BRGB 0101: Setting prohibited 0110: ssi_ws0 0111: ssi_ws1 1000: ssi_ws2 1001: ssi_ws3 1010: ssi_ws4 1011: ssi_ws5 1100: ssi_ws6 1101: ssi_ws7 1110: ssi_ws9 1111: Setting prohibited
23 to 21	—	All 0	R/W	Reserved The write value should always be the initial value.

Bit	Bit Name	Initial Value	R/W	Description
20 to 16	SRC3_IN_DIVRATIO_SE L [4:0]	0_0000	R/W	<p>SRC3 Input Timing Signal Frequency Division Ratio Select</p> <p>These bits select the frequency division ratio for the clock signal selected using SRC3_IN_DIVCLK_SEL[3:0]. Note that ssi_ws signals cannot be divided.</p> <p>0_0000: Divided by 2  0_0001: Divided by 4  0_0010: Divided by 6  0_0011: Divided by 8  0_0100: Divided by 12  0_0101: Divided by 16  0_0110: Divided by 24  0_0111: Divided by 32  0_1000: Divided by 48  0_1001: Divided by 64  0_1010: Divided by 96  0_1011: Divided by 128  0_1100: Divided by 192  0_1101: Divided by 256  0_1110: Divided by 384  0_1111: Divided by 512  1_0000: Divided by 768  1_0001: Divided by 1024  1_0010: Divided by 1536  1_0011: Divided by 2048  1_0100: Divided by 3072  1_0101: Divided by 4096  1_0110: Divided by 6144  1_0111: Divided by 8192  1_1000: Divided by 12288  1_1001: Divided by 16384  1_1010: Divided by 24576  1_1011: Divided by 32768  1_1100: Divided by 49152  1_1101: Divided by 98304  Others: Setting prohibited</p>
15 to 12	—	All 0	R/W	<p>Reserved</p> <p>The write value should always be the initial value.</p>

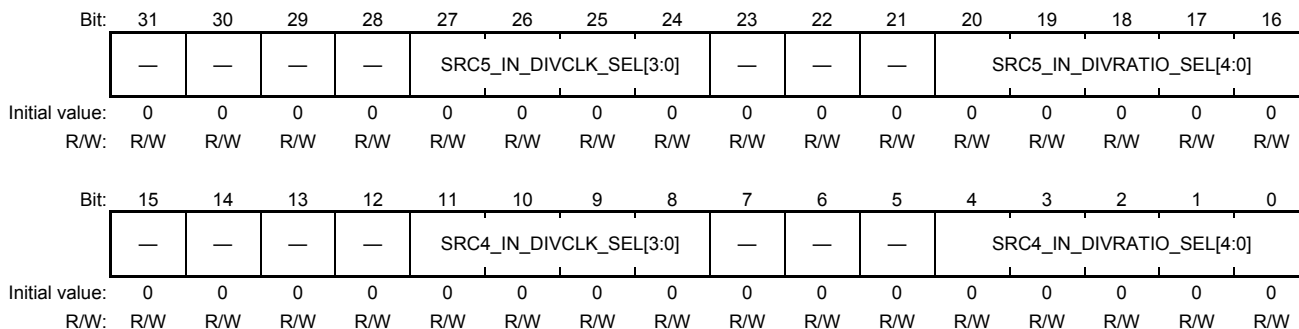
Bit	Bit Name	Initial Value	R/W	Description
11 to 8	SRC2_IN_DIVCLK_SEL[3:0]	0000	R/W	SRC2 Input Timing Signal Select 0000: Divided AUDIO_CLK_A 0001: Divided AUDIO_CLK_B 0010: Divided AUDIO_CLK_C 0011: Divided BRGA 0100: Divided BRGB 0101: Setting prohibited 0110: ssi_ws0 0111: ssi_ws1 1000: ssi_ws2 1001: ssi_ws3 1010: ssi_ws4 1011: ssi_ws5 1100: ssi_ws6 1101: ssi_ws7 1110: ssi_ws9 1111: Setting prohibited
7 to 5	—	All 0	R/W	Reserved The write value should always be the initial value.

Bit	Bit Name	Initial Value	R/W	Description
4 to 0	SRC2_IN_DIVRATIO_SE L [4:0]	0_0000	R/W	<p>SRC2 Input Timing Signal Frequency Division Ratio Select</p> <p>These bits select the frequency division ratio for the clock signal selected using SRC2_IN_DIVCLK_SEL[3:0]. Note that ssi_ws signals cannot be divided.</p> <p>0_0000: Divided by 2</p> <p>0_0001: Divided by 4</p> <p>0_0010: Divided by 6</p> <p>0_0011: Divided by 8</p> <p>0_0100: Divided by 12</p> <p>0_0101: Divided by 16</p> <p>0_0110: Divided by 24</p> <p>0_0111: Divided by 32</p> <p>0_1000: Divided by 48</p> <p>0_1001: Divided by 64</p> <p>0_1010: Divided by 96</p> <p>0_1011: Divided by 128</p> <p>0_1100: Divided by 192</p> <p>0_1101: Divided by 256</p> <p>0_1110: Divided by 384</p> <p>0_1111: Divided by 512</p> <p>1_0000: Divided by 768</p> <p>1_0001: Divided by 1024</p> <p>1_0010: Divided by 1536</p> <p>1_0011: Divided by 2048</p> <p>1_0100: Divided by 3072</p> <p>1_0101: Divided by 4096</p> <p>1_0110: Divided by 6144</p> <p>1_0111: Divided by 8192</p> <p>1_1000: Divided by 12288</p> <p>1_1001: Divided by 16384</p> <p>1_1010: Divided by 24576</p> <p>1_1011: Divided by 32768</p> <p>1_1100: Divided by 49152</p> <p>1_1101: Divided by 98304</p> <p>Others: Setting prohibited</p>

### 33.2.10 SRC Input Timing Select Register 2 (SRCIN\_TIMSEL2)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

**Function:** SRCIN\_TIMSEL2 selects the input timing signals for SRC4 and SRC5.



Bit	Bit Name	Initial Value	R/W	Description
31 to 28	—	All 0	R/W	Reserved The write value should always be the initial value.
27 to 24	SRC5_IN_DIVCLK_SEL [3:0]	0000	R/W	SRC5 Input Timing Signal Select 0000: Divided AUDIO_CLK_A 0001: Divided AUDIO_CLK_B 0010: Divided AUDIO_CLK_C 0011: Divided BRGA 0100: Divided BRGB 0101: Setting prohibited 0110: ssi_ws0 0111: ssi_ws1 1000: ssi_ws2 1001: ssi_ws3 1010: ssi_ws4 1011: ssi_ws5 1100: ssi_ws6 1101: ssi_ws7 1110: ssi_ws9 1111: Setting prohibited
23 to 21	—	All 0	R/W	Reserved The write value should always be the initial value.

Bit	Bit Name	Initial Value	R/W	Description
20 to 16	SRC5_IN_DIVRATIO_SEL[4:0]	0_0000	R/W	<p>SRC5 Input Timing Signal Frequency Division Ratio Select</p> <p>These bits select the frequency division ratio for the clock signal selected using SRC5_IN_DIVCLK_SEL[3:0]. Note that ssi_ws signals cannot be divided.</p> <p>0_0000: Divided by 2            0_0001: Divided by 4            0_0010: Divided by 6            0_0011: Divided by 8            0_0100: Divided by 12            0_0101: Divided by 16            0_0110: Divided by 24            0_0111: Divided by 32            0_1000: Divided by 48            0_1001: Divided by 64            0_1010: Divided by 96            0_1011: Divided by 128            0_1100: Divided by 192            0_1101: Divided by 256            0_1110: Divided by 384            0_1111: Divided by 512            1_0000: Divided by 768            1_0001: Divided by 1024            1_0010: Divided by 1536            1_0011: Divided by 2048            1_0100: Divided by 3072            1_0101: Divided by 4096            1_0110: Divided by 6144            1_0111: Divided by 8192            1_1000: Divided by 12288            1_1001: Divided by 16384            1_1010: Divided by 24576            1_1011: Divided by 32768            1_1100: Divided by 49152            1_1101: Divided by 98304            Others: Setting prohibited</p>
15 to 12	—	All 0	R/W	<p>Reserved</p> <p>The write value should always be the initial value.</p>

Bit	Bit Name	Initial Value	R/W	Description
11 to 8	SRC4_IN_DIVCLK_SEL [3:0]	0000	R/W	SRC4 Input Timing Signal Select 0000: Divided AUDIO_CLK_A 0001: Divided AUDIO_CLK_B 0010: Divided AUDIO_CLK_C 0011: Divided BRGA 0100: Divided BRGB 0101: Setting prohibited 0110: ssi_ws0 0111: ssi_ws1 1000: ssi_ws2 1001: ssi_ws3 1010: ssi_ws4 1011: ssi_ws5 1100: ssi_ws6 1101: ssi_ws7 1110: ssi_ws9 1111: Setting prohibited
7 to 5	—	All 0	R/W	Reserved The write value should always be the initial value.



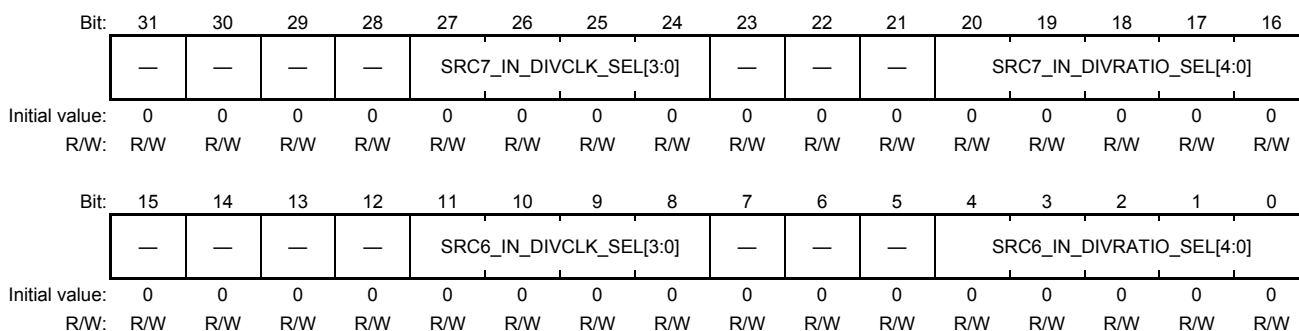
Bit	Bit Name	Initial Value	R/W	Description
4 to 0	SRC4_IN_DIVRATIO_SEL[4:0]	0_0000	R/W	<p>SRC4 Input Timing Signal Frequency Division Ratio Select</p> <p>These bits select the frequency division ratio for the clock signal selected using SRC4_IN_DIVCLK_SEL[3:0]. Note that ssi_ws signals cannot be divided.</p> <p>0_0000: Divided by 2  0_0001: Divided by 4  0_0010: Divided by 6  0_0011: Divided by 8  0_0100: Divided by 12  0_0101: Divided by 16  0_0110: Divided by 24  0_0111: Divided by 32  0_1000: Divided by 48  0_1001: Divided by 64  0_1010: Divided by 96  0_1011: Divided by 128  0_1100: Divided by 192  0_1101: Divided by 256  0_1110: Divided by 384  0_1111: Divided by 512  1_0000: Divided by 768  1_0001: Divided by 1024  1_0010: Divided by 1536  1_0011: Divided by 2048  1_0100: Divided by 3072  1_0101: Divided by 4096  1_0110: Divided by 6144  1_0111: Divided by 8192  1_1000: Divided by 12288  1_1001: Divided by 16384  1_1010: Divided by 24576  1_1011: Divided by 32768  1_1100: Divided by 49152  1_1101: Divided by 98304  11101: Divided by 98304  Others: Setting prohibited</p>

### 33.2.11 SRC Input Timing Select Register 3 (SRCIN\_TIMSEL3)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√*

Note: \* Some restrictions apply.

Function: SRCIN\_TIMSEL3 selects the input timing signals for SRC6 and SRC7.



Bit	Bit Name	Initial Value	R/W	Description
31 to 28	—	All 0	R/W	Reserved The write value should always be the initial value.
27 to 24	SRC7_IN_DIVCLK_SEL [3:0]	0000	R/W	[RZ/G1H, M, N] SRC7 Input Timing Signal Select 0000: Divided AUDIO_CLK_A 0001: Divided AUDIO_CLK_B 0010: Divided AUDIO_CLK_C 0011: Divided BRGA 0100: Divided BRGB 0101: Setting prohibited 0110: ssi_ws0 0111: ssi_ws1 1000: ssi_ws2 1001: ssi_ws3 1010: ssi_ws4 1011: ssi_ws5 1100: ssi_ws6 1101: ssi_ws7 1110: ssi_ws9 1111: Setting prohibited
				[RZ/G1E] Reserved
23 to 21	—	All 0	R/W	Reserved The write value should always be the initial value.

Bit	Bit Name	Initial Value	R/W	Description
20 to 16	SRC7_IN_DIVRATIO_SEL[4:0]	0_0000	R/W	<p>[RZ/G1H, M, N]</p> <p>SRC7 Input Timing Signal Frequency Division Ratio Select</p> <p>These bits select the frequency division ratio for the clock signal selected using SRC7_IN_DIVCLK_SEL[3:0]. Note that ssi_ws signals cannot be divided.</p> <p>0_0000: Divided by 2</p> <p>0_0001: Divided by 4</p> <p>0_0010: Divided by 6</p> <p>0_0011: Divided by 8</p> <p>0_0100: Divided by 12</p> <p>0_0101: Divided by 16</p> <p>0_0110: Divided by 24</p> <p>0_0111: Divided by 32</p> <p>0_1000: Divided by 48</p> <p>0_1001: Divided by 64</p> <p>0_1010: Divided by 96</p> <p>0_1011: Divided by 128</p> <p>0_1100: Divided by 192</p> <p>0_1101: Divided by 256</p> <p>0_1110: Divided by 384</p> <p>0_1111: Divided by 512</p> <p>1_0000: Divided by 768</p> <p>1_0001: Divided by 1024</p> <p>1_0010: Divided by 1536</p> <p>1_0011: Divided by 2048</p> <p>1_0100: Divided by 3072</p> <p>1_0101: Divided by 4096</p> <p>1_0110: Divided by 6144</p> <p>1_0111: Divided by 8192</p> <p>1_1000: Divided by 12288</p> <p>1_1001: Divided by 16384</p> <p>1_1010: Divided by 24576</p> <p>1_1011: Divided by 32768</p> <p>1_1100: Divided by 49152</p> <p>1_1101: Divided by 98304</p> <p>Others: Setting prohibited</p> <hr/> <p>[RZ/G1E] Reserved</p>
15 to 12	—	All 0	R/W	<p>Reserved</p> <p>The write value should always be the initial value.</p>

Bit	Bit Name	Initial Value	R/W	Description
11 to 8	SRC6_IN_DIVCLK_SEL [3:0]	0000	R/W	SRC6 Input Timing Signal Select 0000: Divided AUDIO_CLK_A 0001: Divided AUDIO_CLK_B 0010: Divided AUDIO_CLK_C 0011: Divided BRGA 0100: Divided BRGB 0101: Setting prohibited 0110: ssi_ws0 0111: ssi_ws1 1000: ssi_ws2 1001: ssi_ws3 1010: ssi_ws4 1011: ssi_ws5 1100: ssi_ws6 1101: ssi_ws7 1110: ssi_ws9 1111: Setting prohibited
7 to 5	—	All 0	R/W	Reserved The write value should always be the initial value.

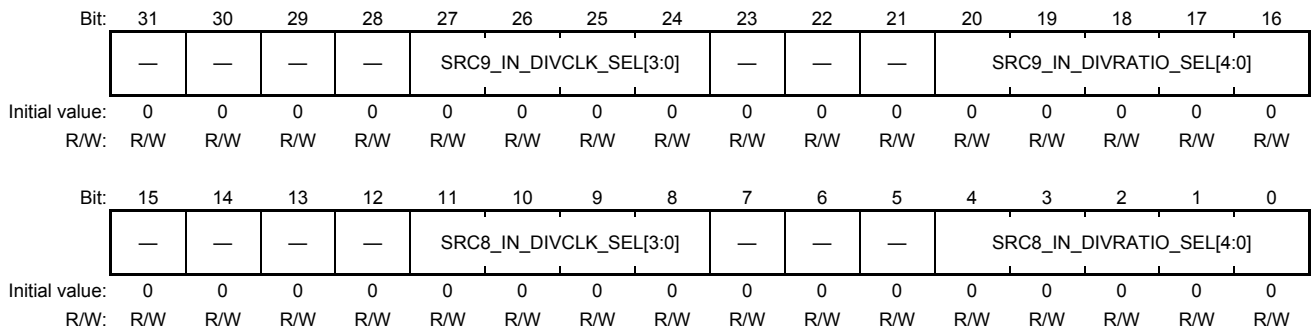
Bit	Bit Name	Initial Value	R/W	Description
4 to 0	SRC6_IN_DIVRATIO_SEL[4:0]	0_0000	R/W	<p>SRC6 Input Timing Signal Frequency Division Ratio Select</p> <p>These bits select the frequency division ratio for the clock signal selected using SRC6_IN_DIVCLK_SEL[3:0]. Note that ssi_ws signals cannot be divided.</p> <p>0_0000: Divided by 2</p> <p>0_0001: Divided by 4</p> <p>0_0010: Divided by 6</p> <p>0_0011: Divided by 8</p> <p>0_0100: Divided by 12</p> <p>0_0101: Divided by 16</p> <p>0_0110: Divided by 24</p> <p>0_0111: Divided by 32</p> <p>0_1000: Divided by 48</p> <p>0_1001: Divided by 64</p> <p>0_1010: Divided by 96</p> <p>0_1011: Divided by 128</p> <p>0_1100: Divided by 192</p> <p>0_1101: Divided by 256</p> <p>0_1110: Divided by 384</p> <p>0_1111: Divided by 512</p> <p>1_0000: Divided by 768</p> <p>1_0001: Divided by 1024</p> <p>1_0010: Divided by 1536</p> <p>1_0011: Divided by 2048</p> <p>1_0100: Divided by 3072</p> <p>1_0101: Divided by 4096</p> <p>1_0110: Divided by 6144</p> <p>1_0111: Divided by 8192</p> <p>1_1000: Divided by 12288</p> <p>1_1001: Divided by 16384</p> <p>1_1010: Divided by 24576</p> <p>1_1011: Divided by 32768</p> <p>1_1100: Divided by 49152</p> <p>1_1101: Divided by 98304</p> <p>Others: Setting prohibited</p>

### 33.2.12 SRC Input Timing Select Register 4 (SRCIN\_TIMSEL4)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√*

Note: \* Some restrictions apply.

**Function:** SRCIN\_TIMSEL4 selects the input timing signals for SRC8 and SRC9.



Bit	Bit Name	Initial Value	R/W	Description
31 to 28	—	All 0	R/W	Reserved The write value should always be the initial value.
27 to 24	SRC9_IN_DIVCLK_SEL [3:0]	0000	R/W	[RZ/G1H, M, N] SRC9 Input Timing Signal Select 0000: Divided AUDIO_CLK_A 0001: Divided AUDIO_CLK_B 0010: Divided AUDIO_CLK_C 0011: Divided BRGA 0100: Divided BRGB 0101: Setting prohibited 0110: ssi_ws0 0111: ssi_ws1 1000: ssi_ws2 1001: ssi_ws3 1010: ssi_ws4 1011: ssi_ws5 1100: ssi_ws6 1101: ssi_ws7 1110: ssi_ws9 1111: Setting prohibited
				[RZ/G1E] Reserved
23 to 21	—	All 0	R/W	Reserved The write value should always be the initial value.

Bit	Bit Name	Initial Value	R/W	Description
20 to 16	SRC9_IN_DIVRATIO_SEL[4:0]	0_0000	R/W	<p>[RZ/G1H, M, N]</p> <p>SRC9 Input Timing Signal Frequency Division Ratio Select</p> <p>These bits select the frequency division ratio for the clock signal selected using SRC9_IN_DIVCLK_SEL[3:0]. Note that ssi_ws signals cannot be divided.</p> <p>0_0000: Divided by 2</p> <p>0_0001: Divided by 4</p> <p>0_0010: Divided by 6</p> <p>0_0011: Divided by 8</p> <p>0_0100: Divided by 12</p> <p>0_0101: Divided by 16</p> <p>0_0110: Divided by 24</p> <p>0_0111: Divided by 32</p> <p>0_1000: Divided by 48</p> <p>0_1001: Divided by 64</p> <p>0_1010: Divided by 96</p> <p>0_1011: Divided by 128</p> <p>0_1100: Divided by 192</p> <p>0_1101: Divided by 256</p> <p>0_1110: Divided by 384</p> <p>0_1111: Divided by 512</p> <p>1_0000: Divided by 768</p> <p>1_0001: Divided by 1024</p> <p>1_0010: Divided by 1536</p> <p>1_0011: Divided by 2048</p> <p>1_0100: Divided by 3072</p> <p>1_0101: Divided by 4096</p> <p>1_0110: Divided by 6144</p> <p>1_0111: Divided by 8192</p> <p>1_1000: Divided by 12288</p> <p>1_1001: Divided by 16384</p> <p>1_1010: Divided by 24576</p> <p>1_1011: Divided by 32768</p> <p>1_1100: Divided by 49152</p> <p>1_1101: Divided by 98304</p> <p>Others: Setting prohibited</p> <hr/> <p>[RZ/G1E] Reserved</p>
15 to 12	—	All 0	R/W	<p>Reserved</p> <p>The write value should always be the initial value.</p>

Bit	Bit Name	Initial Value	R/W	Description
11 to 8	SRC8_IN_DIVCLK_SEL [3:0]	0000	R/W	<p>[RZ/G1H, M, N] SRC8 Input Timing Signal Select</p> <p>0000: Divided AUDIO_CLK_A 0001: Divided AUDIO_CLK_B 0010: Divided AUDIO_CLK_C 0011: Divided BRGA 0100: Divided BRGB 0101: Setting prohibited 0110: ssi_ws0 0111: ssi_ws1 1000: ssi_ws2 1001: ssi_ws3 1010: ssi_ws4 1011: ssi_ws5 1100: ssi_ws6 1101: ssi_ws7 1110: ssi_ws9 1111: Setting prohibited</p> <hr/> <p>[RZ/G1E] Reserved</p>
7 to 5	—	All 0	R/W	<p>Reserved</p> <p>The write value should always be the initial value.</p>



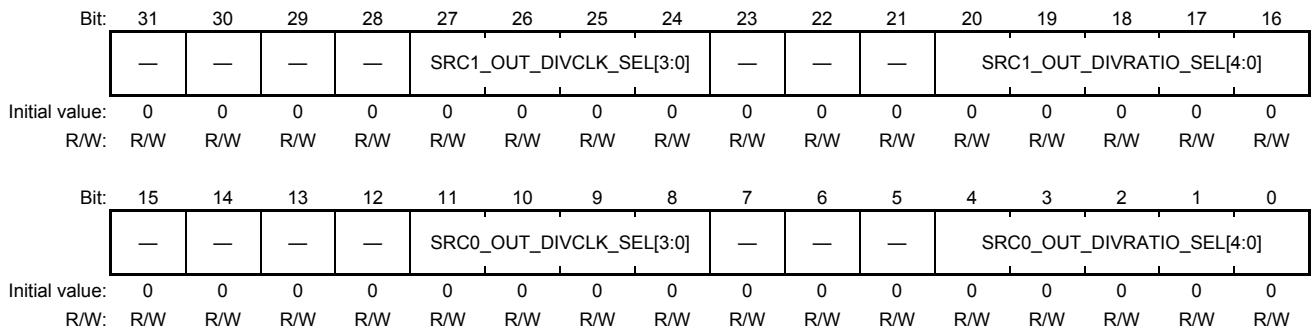
Bit	Bit Name	Initial Value	R/W	Description
4 to 0	SRC8_IN_DIVRATIO_SEL[4:0]	0_0000	R/W	<p>[RZ/G1H, M, N]</p> <p>SRC8 Input Timing Signal Frequency Division Ratio Select</p> <p>These bits select the frequency division ratio for the clock signal selected using SRC8_IN_DIVCLK_SEL[3:0]. Note that ssi_ws signals cannot be divided.</p> <p>0_0000: Divided by 2</p> <p>0_0001: Divided by 4</p> <p>0_0010: Divided by 6</p> <p>0_0011: Divided by 8</p> <p>0_0100: Divided by 12</p> <p>0_0101: Divided by 16</p> <p>0_0110: Divided by 24</p> <p>0_0111: Divided by 32</p> <p>0_1000: Divided by 48</p> <p>0_1001: Divided by 64</p> <p>0_1010: Divided by 96</p> <p>0_1011: Divided by 128</p> <p>0_1100: Divided by 192</p> <p>0_1101: Divided by 256</p> <p>0_1110: Divided by 384</p> <p>0_1111: Divided by 512</p> <p>1_0000: Divided by 768</p> <p>1_0001: Divided by 1024</p> <p>1_0010: Divided by 1536</p> <p>1_0011: Divided by 2048</p> <p>1_0100: Divided by 3072</p> <p>1_0101: Divided by 4096</p> <p>1_0110: Divided by 6144</p> <p>1_0111: Divided by 8192</p> <p>1_1000: Divided by 12288</p> <p>1_1001: Divided by 16384</p> <p>1_1010: Divided by 24576</p> <p>1_1011: Divided by 32768</p> <p>1_1100: Divided by 49152</p> <p>1_1101: Divided by 98304</p> <p>Others: Setting prohibited</p> <hr/> <p>[RZ/G1E] Reserved</p>

**33.2.13 SRC Output Timing Select Register 0 (SRCOUT\_TIMSEL0)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√*

Note: \* Some restrictions apply.

Function: SRCOUT\_TIMSEL0 selects the output timing signals for SRC0 and SRC1.



Bit	Bit Name	Initial Value	R/W	Description
31 to 28	—	All 0	R/W	Reserved The write value should always be the initial value.
27 to 24	SRC1_OUT_DIVCLK_SEL [3:0]	0000	R/W	SRC1 Output Timing Signal Select 0000: Divided AUDIO_CLK_A 0001: Divided AUDIO_CLK_B 0010: Divided AUDIO_CLK_C 0011: Divided BRGA 0100: Divided BRGB 0101: Setting prohibited 0110: ssi_ws0 0111: ssi_ws1 1000: ssi_ws2 1001: ssi_ws3 1010: ssi_ws4 1011: ssi_ws5 1100: ssi_ws6 1101: ssi_ws7 1110: ssi_ws9 1111: Setting prohibited
23 to 21	—	All 0	R/W	Reserved The write value should always be the initial value.

Bit	Bit Name	Initial Value	R/W	Description
20 to 16	SRC1_OUT_DIVRATIO_SEL[4:0]	0_0000	R/W	<p>SRC1 Output Timing Signal Frequency Division Ratio Select</p> <p>These bits select the frequency division ratio for the clock signal selected using SRC1_OUT_DIVCLK_SEL[3:0]. Note that ssi_ws signals cannot be divided.</p> <p>0_0000: Divided by 2  0_0001: Divided by 4  0_0010: Divided by 6  0_0011: Divided by 8  0_0100: Divided by 12  0_0101: Divided by 16  0_0110: Divided by 24  0_0111: Divided by 32  0_1000: Divided by 48  0_1001: Divided by 64  0_1010: Divided by 96  0_1011: Divided by 128  0_1100: Divided by 192  0_1101: Divided by 256  0_1110: Divided by 384  0_1111: Divided by 512  1_0000: Divided by 768  1_0001: Divided by 1024  1_0010: Divided by 1536  1_0011: Divided by 2048  1_0100: Divided by 3072  1_0101: Divided by 4096  1_0110: Divided by 6144  1_0111: Divided by 8192  1_1000: Divided by 12288  1_1001: Divided by 16384  1_1010: Divided by 24576  1_1011: Divided by 32768  1_1100: Divided by 49152  1_1101: Divided by 98304  Others: Setting prohibited</p>
15 to 12	—	All 0	R/W	<p>Reserved</p> <p>The write value should always be the initial value.</p>

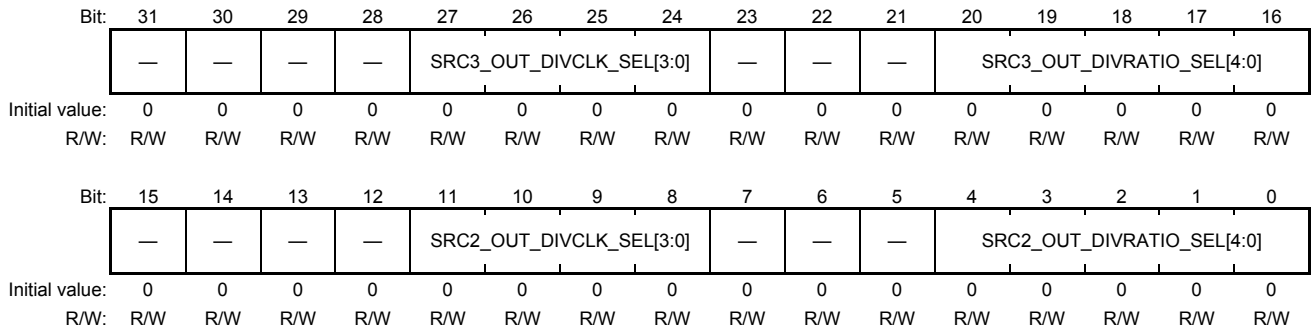
Bit	Bit Name	Initial Value	R/W	Description
11 to 8	SRC0_OUT_DIVCLK_SEL [3:0]	0000	R/W	[RZ/G1H, M, N] SRC0 Output Timing Signal Select 0000: Divided AUDIO_CLK_A 0001: Divided AUDIO_CLK_B 0010: Divided AUDIO_CLK_C 0011: Divided BRGA 0100: Divided BRGB 0101: Setting prohibited 0110: ssi_ws0 0111: ssi_ws1 1000: ssi_ws2 1001: ssi_ws3 1010: ssi_ws4 1011: ssi_ws5 1100: ssi_ws6 1101: ssi_ws7 1110: ssi_ws9 1111: Setting prohibited [RZ/G1E] Reserved
7 to 5	—	All 0	R/W	Reserved The write value should always be the initial value.

Bit	Bit Name	Initial Value	R/W	Description
4 to 0	SRC0_OUT_DIVRATIO_SEL[4:0]	0_0000	R/W	<p>[RZ/G1H, M, N]</p> <p>SRC0 Output Timing Signal Frequency Division Ratio Select</p> <p>These bits select the frequency division ratio for the clock signal selected using SRC0_OUT_DIVCLK_SEL[3:0]. Note that ssi_ws signals cannot be divided.</p> <p>0_0000: Divided by 2  0_0001: Divided by 4  0_0010: Divided by 6  0_0011: Divided by 8  0_0100: Divided by 12  0_0101: Divided by 16  0_0110: Divided by 24  0_0111: Divided by 32  0_1000: Divided by 48  0_1001: Divided by 64  0_1010: Divided by 96  0_1011: Divided by 128  0_1100: Divided by 192  0_1101: Divided by 256  0_1110: Divided by 384  0_1111: Divided by 512  1_0000: Divided by 768  1_0001: Divided by 1024  1_0010: Divided by 1536  1_0011: Divided by 2048  1_0100: Divided by 3072  1_0101: Divided by 4096  1_0110: Divided by 6144  1_0111: Divided by 8192  1_1000: Divided by 12288  1_1001: Divided by 16384  1_1010: Divided by 24576  1_1011: Divided by 32768  1_1100: Divided by 49152  1_1101: Divided by 98304  Others: Setting prohibited</p> <hr/> <p>[RZ/G1E] Reserved</p>

**33.2.14 SRC Output Timing Select Register 1 (SRCOUT\_TIMSEL1)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: SRCOUT\_TIMSEL1 selects the output timing signals for SRC2 and SRC3.



Bit	Bit Name	Initial Value	R/W	Description
31 to 28	—	All 0	R/W	Reserved The write value should always be the initial value.
27 to 24	SRC3_OUT_DIVCLK_SEL [3:0]	0000	R/W	SRC3 Output Timing Signal Select 0000: Divided AUDIO_CLK_A 0001: Divided AUDIO_CLK_B 0010: Divided AUDIO_CLK_C 0011: Divided BRGA 0100: Divided BRGB 0101: Setting prohibited 0110: ssi_ws0 0111: ssi_ws1 1000: ssi_ws2 1001: ssi_ws3 1010: ssi_ws4 1011: ssi_ws5 1100: ssi_ws6 1101: ssi_ws7 1110: ssi_ws9 1111: Setting prohibited
23 to 21	—	All 0	R/W	Reserved The write value should always be the initial value.

Bit	Bit Name	Initial Value	R/W	Description
20 to 16	SRC3_OUT_DIVRATIO_SEL[4:0]	0_0000	R/W	<p>SRC3 Output Timing Signal Frequency Division Ratio Select</p> <p>These bits select the frequency division ratio for the clock signal selected using SRC3_OUT_DIVCLK_SEL[3:0]. Note that ssi_ws signals cannot be divided.</p> <p>0_0000: Divided by 2                      0_0001: Divided by 4                      0_0010: Divided by 6                      0_0011: Divided by 8                      0_0100: Divided by 12                      0_0101: Divided by 16                      0_0110: Divided by 24                      0_0111: Divided by 32                      0_1000: Divided by 48                      0_1001: Divided by 64                      0_1010: Divided by 96                      0_1011: Divided by 128                      0_1100: Divided by 192                      0_1101: Divided by 256                      0_1110: Divided by 384                      0_1111: Divided by 512                      1_0000: Divided by 768                      1_0001: Divided by 1024                      1_0010: Divided by 1536                      1_0011: Divided by 2048                      1_0100: Divided by 3072                      1_0101: Divided by 4096                      1_0110: Divided by 6144                      1_0111: Divided by 8192                      1_1000: Divided by 12288                      1_1001: Divided by 16384                      1_1010: Divided by 24576                      1_1011: Divided by 32768                      1_1100: Divided by 49152                      1_1101: Divided by 98304                      Others: Setting prohibited</p>
15 to 12	—	All 0	R/W	<p>Reserved</p> <p>The write value should always be the initial value.</p>

Bit	Bit Name	Initial Value	R/W	Description
11 to 8	SRC2_OUT_DIVCLK_SEL [3:0]	0000	R/W	SRC2 Output Timing Signal Select 0000: Divided AUDIO_CLK_A 0001: Divided AUDIO_CLK_B 0010: Divided AUDIO_CLK_C 0011: Divided BRGA 0100: Divided BRGB 0101: Setting prohibited 0110: ssi_ws0 0111: ssi_ws1 1000: ssi_ws2 1001: ssi_ws3 1010: ssi_ws4 1011: ssi_ws5 1100: ssi_ws6 1101: ssi_ws7 1110: ssi_ws9 1111: Setting prohibited
7 to 5	—	All 0	R/W	Reserved The write value should always be the initial value.

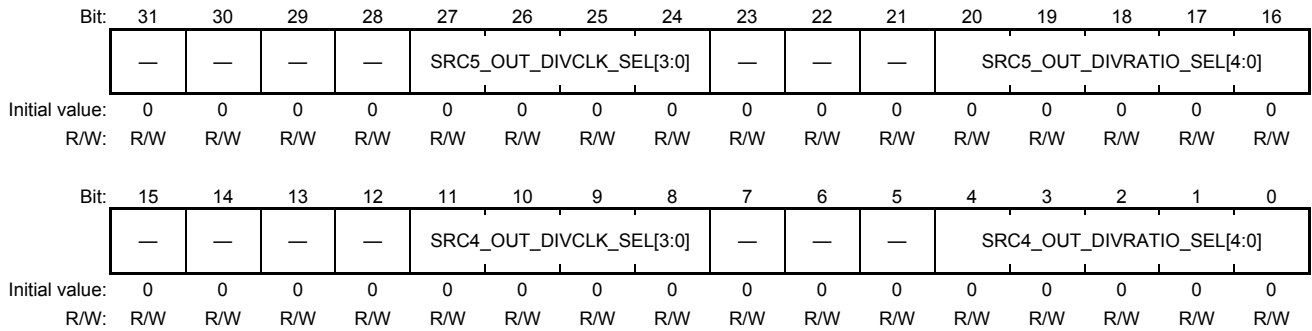


Bit	Bit Name	Initial Value	R/W	Description
4 to 0	SRC2_OUT_DIVRATIO_SEL[4:0]	0_0000	R/W	<p>SRC2 Output Timing Signal Frequency Division Ratio Select</p> <p>These bits select the frequency division ratio for the clock signal selected using SRC2_OUT_DIVCLK_SEL[3:0]. Note that ssi_ws signals cannot be divided.</p> <p>0_0000: Divided by 2  0_0001: Divided by 4  0_0010: Divided by 6  0_0011: Divided by 8  0_0100: Divided by 12  0_0101: Divided by 16  0_0110: Divided by 24  0_0111: Divided by 32  0_1000: Divided by 48  0_1001: Divided by 64  0_1010: Divided by 96  0_1011: Divided by 128  0_1100: Divided by 192  0_1101: Divided by 256  0_1110: Divided by 384  0_1111: Divided by 512  1_0000: Divided by 768  1_0001: Divided by 1024  1_0010: Divided by 1536  1_0011: Divided by 2048  1_0100: Divided by 3072  1_0101: Divided by 4096  1_0110: Divided by 6144  1_0111: Divided by 8192  1_1000: Divided by 12288  1_1001: Divided by 16384  1_1010: Divided by 24576  1_1011: Divided by 32768  1_1100: Divided by 49152  1_1101: Divided by 98304  Others: Setting prohibited</p>

### 33.2.15 SRC Output Timing Select Register 2 (SRCOUT\_TIMSEL2)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

**Function:** SRCOUT\_TIMSEL2 selects the output timing signals for SRC4 and SRC5.



Bit	Bit Name	Initial Value	R/W	Description
31 to 28	—	All 0	R/W	Reserved The write value should always be the initial value.
27 to 24	SRC5_OUT_DIVCLK_SEL [3:0]	0000	R/W	SRC5 Output Timing Signal Select 0000: Divided AUDIO_CLK_A 0001: Divided AUDIO_CLK_B 0010: Divided AUDIO_CLK_C 0011: Divided BRGA 0100: Divided BRGB 0101: Setting prohibited 0110: ssi_ws0 0111: ssi_ws1 1000: ssi_ws2 1001: ssi_ws3 1010: ssi_ws4 1011: ssi_ws5 1100: ssi_ws6 1101: ssi_ws7 1110: ssi_ws9 1111: Setting prohibited
23 to 21	—	All 0	R/W	Reserved The write value should always be the initial value.

Bit	Bit Name	Initial Value	R/W	Description
20 to 16	SRC5_OUT_DIVRATIO_SEL[4:0]	0_0000	R/W	<p>SRC5 Output Timing Signal Frequency Division Ratio Select</p> <p>These bits select the frequency division ratio for the clock signal selected using SRC5_OUT_DIVCLK_SEL[3:0]. Note that ssi_ws signals cannot be divided.</p> <p>0_0000: Divided by 2            0_0001: Divided by 4            0_0010: Divided by 6            0_0011: Divided by 8            0_0100: Divided by 12            0_0101: Divided by 16            0_0110: Divided by 24            0_0111: Divided by 32            0_1000: Divided by 48            0_1001: Divided by 64            0_1010: Divided by 96            0_1011: Divided by 128            0_1100: Divided by 192            0_1101: Divided by 256            0_1110: Divided by 384            0_1111: Divided by 512            1_0000: Divided by 768            1_0001: Divided by 1024            1_0010: Divided by 1536            1_0011: Divided by 2048            1_0100: Divided by 3072            1_0101: Divided by 4096            1_0110: Divided by 6144            1_0111: Divided by 8192            1_1000: Divided by 12288            1_1001: Divided by 16384            1_1010: Divided by 24576            1_1011: Divided by 32768            1_1100: Divided by 49152            1_1101: Divided by 98304            Others: Setting prohibited</p>
15 to 12	—	All 0	R/W	<p>Reserved</p> <p>The write value should always be the initial value.</p>

Bit	Bit Name	Initial Value	R/W	Description
11 to 8	SRC4_OUT_DIVCLK_SEL [3:0]	0000	R/W	SRC4 Output Timing Signal Select 0000: Divided AUDIO_CLK_A 0001: Divided AUDIO_CLK_B 0010: Divided AUDIO_CLK_C 0011: Divided BRGA 0100: Divided BRGB 0101: Setting prohibited 0110: ssi_ws0 0111: ssi_ws1 1000: ssi_ws2 1001: ssi_ws3 1010: ssi_ws4 1011: ssi_ws5 1100: ssi_ws6 1101: ssi_ws7 1110: ssi_ws9 1111: Setting prohibited
7 to 5	—	All 0	R/W	Reserved The write value should always be the initial value.

Bit	Bit Name	Initial Value	R/W	Description
4 to 0	SRC4_OUT_DIVRATIO_SEL[4:0]	0_0000	R/W	<p>SRC4 Output Timing Signal Frequency Division Ratio Select</p> <p>These bits select the frequency division ratio for the clock signal selected using SRC4_OUT_DIVCLK_SEL[3:0]. Note that ssi_ws signals cannot be divided.</p> <p>0_0000: Divided by 2            0_0001: Divided by 4            0_0010: Divided by 6            0_0011: Divided by 8            0_0100: Divided by 12            0_0101: Divided by 16            0_0110: Divided by 24            0_0111: Divided by 32            0_1000: Divided by 48            0_1001: Divided by 64            0_1010: Divided by 96            0_1011: Divided by 128            0_1100: Divided by 192            0_1101: Divided by 256            0_1110: Divided by 384            0_1111: Divided by 512            1_0000: Divided by 768            1_0001: Divided by 1024            1_0010: Divided by 1536            1_0011: Divided by 2048            1_0100: Divided by 3072            1_0101: Divided by 4096            1_0110: Divided by 6144            1_0111: Divided by 8192            1_1000: Divided by 12288            1_1001: Divided by 16384            1_1010: Divided by 24576            1_1011: Divided by 32768            1_1100: Divided by 49152            1_1101: Divided by 98304            Others: Setting prohibited</p>

### 33.2.16 SRC Output Timing Select Register 3 (SRCOUT\_TIMSEL3)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√*

Note: \* Some restrictions apply.

**Function:** SRCOUT\_TIMSEL3 selects the output timing signals for SRC6 and SRC7.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	SRC7_OUT_DIVCLK_SEL[3:0]				—	—	—	SRC7_OUT_DIVRATIO_SEL[4:0]				
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	SRC6_OUT_DIVCLK_SEL[3:0]				—	—	—	SRC6_OUT_DIVRATIO_SEL[4:0]				
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 28	—	All 0	R/W	Reserved The write value should always be the initial value.
27 to 24	SRC7_OUT_DIVCLK_SEL [3:0]	0000	R/W	[RZ/G1H, M, N] SRC7 Output Timing Signal Select 0000: Divided AUDIO_CLK_A 0001: Divided AUDIO_CLK_B 0010: Divided AUDIO_CLK_C 0011: Divided BRGA 0100: Divided BRGB 0101: Setting prohibited 0110: ssi_ws0 0111: ssi_ws1 1000: ssi_ws2 1001: ssi_ws3 1010: ssi_ws4 1011: ssi_ws5 1100: ssi_ws6 1101: ssi_ws7 1110: ssi_ws9 1111: Setting prohibited
				[RZ/G1E] Reserved
23 to 21	—	All 0	R/W	Reserved The write value should always be the initial value.

Bit	Bit Name	Initial Value	R/W	Description
20 to 16	SRC7_OUT_DIVRATIO_SEL[4:0]	0_0000	R/W	<p>[RZ/G1H, M, N]</p> <p>SRC7 Output Timing Signal Frequency Division Ratio Select</p> <p>These bits select the frequency division ratio for the clock signal selected using SRC7_OUT_DIVCLK_SEL[3:0]. Note that ssi_ws signals cannot be divided.</p> <p>0_0000: Divided by 2  0_0001: Divided by 4  0_0010: Divided by 6  0_0011: Divided by 8  0_0100: Divided by 12  0_0101: Divided by 16  0_0110: Divided by 24  0_0111: Divided by 32  0_1000: Divided by 48  0_1001: Divided by 64  0_1010: Divided by 96  0_1011: Divided by 128  0_1100: Divided by 192  0_1101: Divided by 256  0_1110: Divided by 384  0_1111: Divided by 512  1_0000: Divided by 768  1_0001: Divided by 1024  1_0010: Divided by 1536  1_0011: Divided by 2048  1_0100: Divided by 3072  1_0101: Divided by 4096  1_0110: Divided by 6144  1_0111: Divided by 8192  1_1000: Divided by 12288  1_1001: Divided by 16384  1_1010: Divided by 24576  1_1011: Divided by 32768  1_1100: Divided by 49152  1_1101: Divided by 98304  Others: Setting prohibited</p> <hr/> <p>[RZ/G1E] Reserved</p>
15 to 12	—	All 0	R/W	<p>Reserved</p> <p>The write value should always be the initial value.</p>

Bit	Bit Name	Initial Value	R/W	Description
11 to 8	SRC6_OUT_DIVCLK_SEL [3:0]	0000	R/W	SRC6 Output Timing Signal Select 0000: Divided AUDIO_CLK_A 0001: Divided AUDIO_CLK_B 0010: Divided AUDIO_CLK_C 0011: Divided BRGA 0100: Divided BRGB 0101: Setting prohibited 0110: ssi_ws0 0111: ssi_ws1 1000: ssi_ws2 1001: ssi_ws3 1010: ssi_ws4 1011: ssi_ws5 1100: ssi_ws6 1101: ssi_ws7 1110: ssi_ws9 1111: Setting prohibited
7 to 5	—	All 0	R/W	Reserved The write value should always be the initial value.



Bit	Bit Name	Initial Value	R/W	Description
4 to 0	SRC6_OUT_DIVRATIO_SEL[4:0]	0_0000	R/W	<p>SRC6 Output Timing Signal Frequency Division Ratio Select</p> <p>These bits select the frequency division ratio for the clock signal selected using SRC6_OUT_DIVCLK_SEL[3:0]. Note that ssi_ws signals cannot be divided.</p> <p>0_0000: Divided by 2  0_0001: Divided by 4  0_0010: Divided by 6  0_0011: Divided by 8  0_0100: Divided by 12  0_0101: Divided by 16  0_0110: Divided by 24  0_0111: Divided by 32  0_1000: Divided by 48  0_1001: Divided by 64  0_1010: Divided by 96  0_1011: Divided by 128  0_1100: Divided by 192  0_1101: Divided by 256  0_1110: Divided by 384  0_1111: Divided by 512  1_0000: Divided by 768  1_0001: Divided by 1024  1_0010: Divided by 1536  1_0011: Divided by 2048  1_0100: Divided by 3072  1_0101: Divided by 4096  1_0110: Divided by 6144  1_0111: Divided by 8192  1_1000: Divided by 12288  1_1001: Divided by 16384  1_1010: Divided by 24576  1_1011: Divided by 32768  1_1100: Divided by 49152  1_1101: Divided by 98304  Others: Setting prohibited</p>

### 33.2.17 SRC Output Timing Select Register 4 (SRCOUT\_TIMSEL4)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√*

Note: \* Some restrictions apply.

**Function:** SRCOUT\_TIMSEL4 selects the output timing signals for SRC8 and SRC9.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	SRC9_OUT_DIVCLK_SEL[3:0]				—	—	—	SRC9_OUT_DIVRATIO_SEL[4:0]				
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	SRC8_OUT_DIVCLK_SEL[3:0]				—	—	—	SRC8_OUT_DIVRATIO_SEL[4:0]				
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 28	—	All 0	R/W	Reserved The write value should always be the initial value.
27 to 24	SRC9_OUT_DIVCLK_SEL [3:0]	0000	R/W	[RZ/G1H, M, N] SRC9 Output Timing Signal Select 0000: Divided AUDIO_CLK_A 0001: Divided AUDIO_CLK_B 0010: Divided AUDIO_CLK_C 0011: Divided BRGA 0100: Divided BRGB 0101: Setting prohibited 0110: ssi_ws0 0111: ssi_ws1 1000: ssi_ws2 1001: ssi_ws3 1010: ssi_ws4 1011: ssi_ws5 1100: ssi_ws6 1101: ssi_ws7 1110: ssi_ws9 1111: Setting prohibited
				[RZ/G1E] Reserved
23 to 21	—	All 0	R/W	Reserved The write value should always be the initial value.

Bit	Bit Name	Initial Value	R/W	Description
20 to 16	SRC9_OUT_DIVRATIO_SEL[4:0]	0_0000	R/W	<p>[RZ/G1H, M, N]</p> <p>SRC9 Output Timing Signal Frequency Division Ratio Select</p> <p>These bits select the frequency division ratio for the clock signal selected using SRC9_OUT_DIVCLK_SEL[3:0]. Note that ssi_ws signals cannot be divided.</p> <p>0_0000: Divided by 2  0_0001: Divided by 4  0_0010: Divided by 6  0_0011: Divided by 8  0_0100: Divided by 12  0_0101: Divided by 16  0_0110: Divided by 24  0_0111: Divided by 32  0_1000: Divided by 48  0_1001: Divided by 64  0_1010: Divided by 96  0_1011: Divided by 128  0_1100: Divided by 192  0_1101: Divided by 256  0_1110: Divided by 384  0_1111: Divided by 512  1_0000: Divided by 768  1_0001: Divided by 1024  1_0010: Divided by 1536  1_0011: Divided by 2048  1_0100: Divided by 3072  1_0101: Divided by 4096  1_0110: Divided by 6144  1_0111: Divided by 8192  1_1000: Divided by 12288  1_1001: Divided by 16384  1_1010: Divided by 24576  1_1011: Divided by 32768  1_1100: Divided by 49152  1_1101: Divided by 98304  Others: Setting prohibited</p> <hr/> <p>[RZ/G1E] Reserved</p>
15 to 12	—	All 0	R/W	<p>Reserved</p> <p>The write value should always be the initial value.</p>

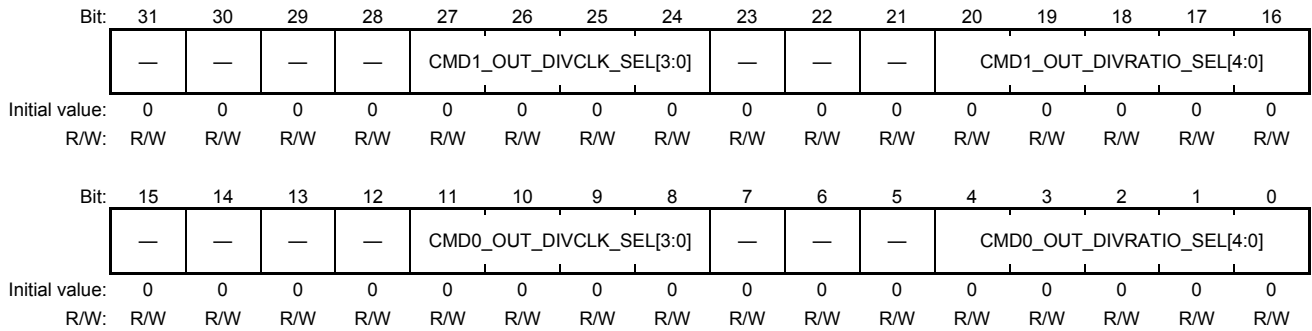
Bit	Bit Name	Initial Value	R/W	Description
11 to 8	SRC8_OUT_DIVCLK_SEL [3:0]	0000	R/W	[RZ/G1H, M, N] SRC8 Output Timing Signal Select 0000: Divided AUDIO_CLK_A 0001: Divided AUDIO_CLK_B 0010: Divided AUDIO_CLK_C 0011: Divided BRGA 0100: Divided BRGB 0101: Setting prohibited 0110: ssi_ws0 0111: ssi_ws1 1000: ssi_ws2 1001: ssi_ws3 1010: ssi_ws4 1011: ssi_ws5 1100: ssi_ws6 1101: ssi_ws7 1110: ssi_ws9 1111: Setting prohibited [RZ/G1E] Reserved
7 to 5	—	All 0	R/W	Reserved The write value should always be the initial value.

Bit	Bit Name	Initial Value	R/W	Description
4 to 0	SRC8_OUT_DIVRATIO_SEL[4:0]	0_0000	R/W	<p>[RZ/G1H, M, N]</p> <p>SRC8 Output Timing Signal Frequency Division Ratio Select</p> <p>These bits select the frequency division ratio for the clock signal selected using SRC8_OUT_DIVCLK_SEL[3:0]. Note that ssi_ws signals cannot be divided.</p> <p>0_0000: Divided by 2  0_0001: Divided by 4  0_0010: Divided by 6  0_0011: Divided by 8  0_0100: Divided by 12  0_0101: Divided by 16  0_0110: Divided by 24  0_0111: Divided by 32  0_1000: Divided by 48  0_1001: Divided by 64  0_1010: Divided by 96  0_1011: Divided by 128  0_1100: Divided by 192  0_1101: Divided by 256  0_1110: Divided by 384  0_1111: Divided by 512  1_0000: Divided by 768  1_0001: Divided by 1024  1_0010: Divided by 1536  1_0011: Divided by 2048  1_0100: Divided by 3072  1_0101: Divided by 4096  1_0110: Divided by 6144  1_0111: Divided by 8192  1_1000: Divided by 12288  1_1001: Divided by 16384  1_1010: Divided by 24576  1_1011: Divided by 32768  1_1100: Divided by 49152  1_1101: Divided by 98304  Others: Setting prohibited</p> <hr/> <p>[RZ/G1E] Reserved</p>

**33.2.18 CMD Output Timing Select Register (CMDOUT\_TIMSEL)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: CMDOUT\_TIMSEL selects the output timing signals for CMD0 and CMD1.



Bit	Bit Name	Initial Value	R/W	Description
31 to 28	—	All 0	R/W	Reserved The write value should always be the initial value.
27 to 24	CMD1_OUT_DIVCLK_SEL [3:0]	0000	R/W	CMD1 Output Timing Signal Select 0000: Divided AUDIO_CLK_A 0001: Divided AUDIO_CLK_B 0010: Divided AUDIO_CLK_C 0011: Divided BRGA 0100: Divided BRGB 0101: Setting prohibited 0110: ssi_ws0 0111: ssi_ws1 1000: ssi_ws2 1001: ssi_ws3 1010: ssi_ws4 1011: ssi_ws5 1100: ssi_ws6 1101: ssi_ws7 1110: ssi_ws9 1111: Setting prohibited
23 to 21	—	All 0	R/W	Reserved The write value should always be the initial value.

Bit	Bit Name	Initial Value	R/W	Description
20 to 16	CMD1_OUT_DIVRATIO_SEL[4:0]	0_0000	R/W	<p>CMD1 Output Timing Signal Frequency Division Ratio Select</p> <p>These bits select the frequency division ratio for the clock signal selected using CMD1_OUT_DIVCLK_SEL[3:0]. Note that ssi_ws signals cannot be divided.</p> <p>0_0000: Divided by 2            0_0001: Divided by 4            0_0010: Divided by 6            0_0011: Divided by 8            0_0100: Divided by 12            0_0101: Divided by 16            0_0110: Divided by 24            0_0111: Divided by 32            0_1000: Divided by 48            0_1001: Divided by 64            0_1010: Divided by 96            0_1011: Divided by 128            0_1100: Divided by 192            0_1101: Divided by 256            0_1110: Divided by 384            0_1111: Divided by 512            1_0000: Divided by 768            1_0001: Divided by 1024            1_0010: Divided by 1536            1_0011: Divided by 2048            1_0100: Divided by 3072            1_0101: Divided by 4096            1_0110: Divided by 6144            1_0111: Divided by 8192            1_1000: Divided by 12288            1_1001: Divided by 16384            1_1010: Divided by 24576            1_1011: Divided by 32768            1_1100: Divided by 49152            1_1101: Divided by 98304            Others: Setting prohibited</p>
15 to 12	—	All 0	R/W	<p>Reserved</p> <p>The write value should always be the initial value.</p>

Bit	Bit Name	Initial Value	R/W	Description
11 to 8	CMD0_OUT_DIVCLK_SEL [3:0]	0000	R/W	CMD0 Output Timing Signal Select 0000: Divided AUDIO_CLK_A 0001: Divided AUDIO_CLK_B 0010: Divided AUDIO_CLK_C 0011: Divided BRGA 0100: Divided BRGB 0101: Setting prohibited 0110: ssi_ws0 0111: ssi_ws1 1000: ssi_ws2 1001: ssi_ws3 1010: ssi_ws4 1011: ssi_ws5 1100: ssi_ws6 1101: ssi_ws7 1110: ssi_ws9 1111: Setting prohibited
7 to 5	—	All 0	R/W	Reserved The write value should always be the initial value.



Bit	Bit Name	Initial Value	R/W	Description
4 to 0	CMD0_OUT_DIVRATIO_SEL[4:0]	0_0000	R/W	<p>CMD0 Output Timing Signal Frequency Division Ratio Select</p> <p>These bits select the frequency division ratio for the clock signal selected using CMD0_OUT_DIVCLK_SEL[3:0]. Note that ssi_ws signals cannot be divided.</p> <p>0_0000: Divided by 2</p> <p>0_0001: Divided by 4</p> <p>0_0010: Divided by 6</p> <p>0_0011: Divided by 8</p> <p>0_0100: Divided by 12</p> <p>0_0101: Divided by 16</p> <p>0_0110: Divided by 24</p> <p>0_0111: Divided by 32</p> <p>0_1000: Divided by 48</p> <p>0_1001: Divided by 64</p> <p>0_1010: Divided by 96</p> <p>0_1011: Divided by 128</p> <p>0_1100: Divided by 192</p> <p>0_1101: Divided by 256</p> <p>0_1110: Divided by 384</p> <p>0_1111: Divided by 512</p> <p>1_0000: Divided by 768</p> <p>1_0001: Divided by 1024</p> <p>1_0010: Divided by 1536</p> <p>1_0011: Divided by 2048</p> <p>1_0100: Divided by 3072</p> <p>1_0101: Divided by 4096</p> <p>1_0110: Divided by 6144</p> <p>1_0111: Divided by 8192</p> <p>1_1000: Divided by 12288</p> <p>1_1001: Divided by 16384</p> <p>1_1010: Divided by 24576</p> <p>1_1011: Divided by 32768</p> <p>1_1100: Divided by 49152</p> <p>1_1101: Divided by 98304</p> <p>Others: Setting prohibited</p>

### 33.3 Operation

RZ/G1H	RZ/G1N
RZ/G1M	RZ/G1E

The following sections give examples of setting the ADG registers.

#### (1) Supplying SSI3 with Audio Clock

The following procedure can be used to divide the internal clock (195-MHz) by 18 and supply the resulting BRGB clock (10.833-MHz) to SSI3. (If the procedure is applied before starting SSI3, steps 1 to 5 can be executed in any order.)

1. Set BRRB so that the frequency division ratio should be 18.
2. Select internal clock (M2 $\phi$ ) as the clock to be input to BRGB using SSICKR.
3. Select the BRGB output clock as SSI3 clock using AUDIO\_CLK\_SEL0.
4. Release the ADG (M2 $\phi$ ) from the module standby state using SMSTPCR1 of the CPG module.
5. Release SSI3 from the module standby state using SMSTPCR10 of the CPG module.

**Table 33.5 Setting Example 1**

Register Name	Address	Setting Value	Description
BRRB	H'EC5A_0004	H'0000_0008	Divided by 18
SSICKR	H'EC5A_0008	H'2302_0000	Selects M2 $\phi$ as the clock to be input to BRGB.
AUDIO_CLK_SEL0	H'EC5A_000C	H'2000_0000	Selects the BRGB output clock as the clock to be output to SSI3.
SMSTPCR1	H'E615_0134	Set bit 6 to 0.	Releases the ADG (M2 $\phi$ ) from the module standby state.
SMSTPCR10	H'E615_0998	Set bits 12 to 0.	Releases the SSI3 from the module standby state.

## 34. Sampling Rate Converter Unit (SCU)

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

### 34.1 Overview

The SCU has ten (six)\* SRC modules (six (four\*) for high-sound-quality type; four (two\*) for general-sound-quality type) that are useful for synchronization of asynchronous data, which is necessary for data transfer with external memory or external devices. It also provides the functions to change the number of channels, perform mixing, and control the volume.

Notes: When the SRCs are not in use, configure the system with the same clock sources for AUDIO CLOCK that is input to ADG, and INIC or devices for I2S that are connected to external modules, and all thus operate at the same sampling frequency.

\* Applicable to the RZ/G1E.

#### 34.1.1 Features

##### (1) Sampling Rate Converter (SRC)

- Asynchronous sampling rate conversion is available
- Supports resolutions up to 24 bits
- High-sound-quality type (THD + N\*<sup>1</sup> is -132 dB) and general-sound-quality type (THD + N\*<sup>1</sup> is -96 dB)
- Automatically generates antialiasing filter coefficients
- Four (three)\*<sup>2</sup> modules support one, two, four, six, or eight channels, and six (three)\*<sup>2</sup> modules support one or two channels.

Notes: 1. Total harmonic distortion plus noise

2. Applicable to the RZ/G1E.

##### (2) Channel Transfer Unit (CTU)

- Downmixing and splitter functions
  - Conversion of eight input channels into two output channels
  - Conversion of six input channels into two output channels
  - Conversion of two input channels into four sets of two output channels
  - Conversion of one input channel into eight sets of one output channel
  - No conversion

##### (3) Mixer (MIX)

- Mixing (adds) two to four sources into one
- Ratio for adding sources is selectable
- Ratio is dynamically changeable
- Mixing with volume ramp is available (ramp period is selectable)

##### (4) Digital Volume and Mute Function (DVC)

- Volume control function including digital volume, volume ramp, and zero-crossing mute
- The digital volume function is specified by a 24-bit fixed-point value within the range from 0 to 8 times (mute or -120 to 18 dB)
- The volume ramp function can be used for soft mute, fade-in, fade-out, or desired volume adjustment
- The volume ramp period can be changed within the sampling range from the 0th to 23rd power of 2
- The zero-crossing mute function silences the sound at the zero-crossing point of the audio data

The CTU, MIX, and DVC functional blocks are collectively called "CMD".

### 34.1.2 Block Diagram

Figure 34.1 shows the SCU block diagram.

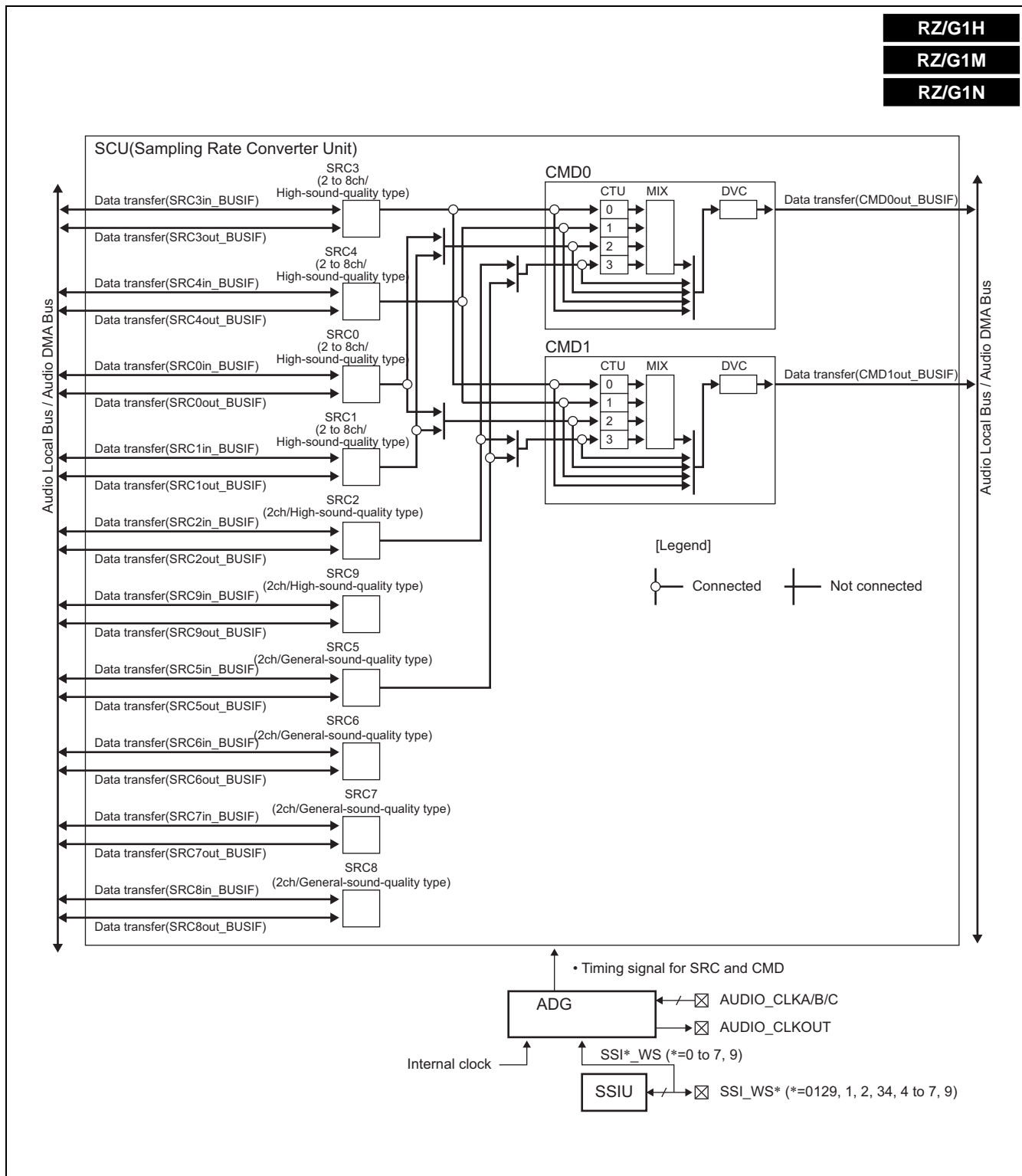


Figure 34.1a Block Diagram of SCU [for RZ/G1H, RZ/G1M, and RZ/G1N]

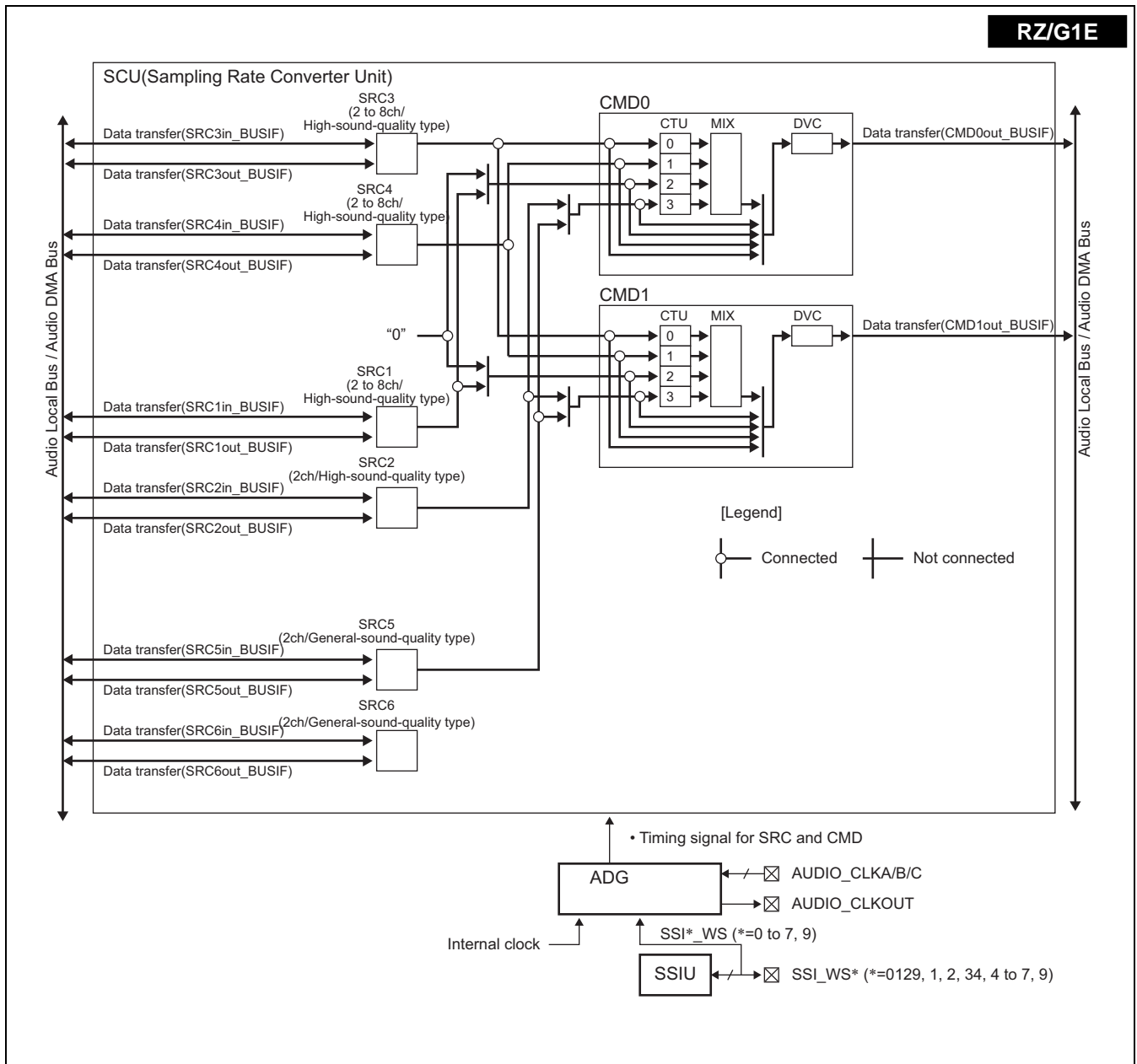


Figure 34.1b Block Diagram of SCU [for RZ/G1E]

### 34.1.3 Input/Output Pins

Table 34.1 shows the pin configuration.

**Table 34.1 Pin Configuration**

<b>Name</b>	<b>Pin Name</b>	<b>I/O</b>	<b>Function</b>
DVC_MUTE pin	DVC_MUTE	Input	DVCEN

### 34.1.4 Register Configuration

Table 34.2 shows the register configuration. Do not write to any addresses other than listed below. Operations cannot be guaranteed if writing is attempted. Values read from addresses other than those listed below are undefined. Access the register as a longword (32 bits). Operation cannot be guaranteed if the register is not accessed as a longword.

**Table 34.2 Register Configuration**

Name	Abbreviation	R/W	Address	Initial Value	Access Size	RZ/G Series Products			
						RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
SRC0in_BUSIF_MODE register	SRC0in_BUSIF_MODE	R/W	H'EC50 0000	H'00000001	32	√	√	√	—
SRC0out_BUSIF_MODE register	SRC0out_BUSIF_MODE	R/W	H'EC50 0004	H'00000001	32	√	√	√	—
SRC0_BUSIF_DALIGN register	SRC0_BUSIF_DALIGN	R/W	H'EC50 0008	H'76543210	32	√	√	√	—
SRC0_MODE register	SRC0_MODE	R/W	H'EC50 000C	H'00000000	32	√	√	√	—
SRC0 control register	SRC0_CONTROL	R/W	H'EC50 0010	H'00000000	32	√	√	√	—
SRC0 status register	SRC0_STATUS	R	H'EC50 0014	H'00000000	32	√	√	√	—
SRC0 interrupt enable register 0	SRC0_INT_ENABLE0	R/W	H'EC50 0018	H'00000000	32	√	√	√	—
SRC1in_BUSIF_MODE register	SRC1in_BUSIF_MODE	R/W	H'EC50 0020	H'00000001	32	√	√	√	√
SRC1out_BUSIF_MODE register	SRC1out_BUSIF_MODE	R/W	H'EC50 0024	H'00000001	32	√	√	√	√
SRC1_BUSIF_DALIGN register	SRC1_BUSIF_DALIGN	R/W	H'EC50 0028	H'76543210	32	√	√	√	√
SRC1_MODE register	SRC1_MODE	R/W	H'EC50 002C	H'00000000	32	√	√	√	√
SRC1 control register	SRC1_CONTROL	R/W	H'EC50 0030	H'00000000	32	√	√	√	√
SRC1 status register	SRC1_STATUS	R	H'EC50 0034	H'00000000	32	√	√	√	√
SRC1 interrupt enable register 0	SRC1_INT_ENABLE0	R/W	H'EC50 0038	H'00000000	32	√	√	√	√
SRC2in_BUSIF_MODE register	SRC2in_BUSIF_MODE	R/W	H'EC50 0040	H'00000001	32	√	√	√	√
SRC2out_BUSIF_MODE register	SRC2out_BUSIF_MODE	R/W	H'EC50 0044	H'00000001	32	√	√	√	√
SRC2_BUSIF_DALIGN register	SRC2_BUSIF_DALIGN	R/W	H'EC50 0048	H'00000010	32	√	√	√	√
SRC2_MODE register	SRC2_MODE	R/W	H'EC50 004C	H'00000000	32	√	√	√	√
SRC2 control register	SRC2_CONTROL	R/W	H'EC50 0050	H'00000000	32	√	√	√	√
SRC2 status register	SRC2_STATUS	R	H'EC50 0054	H'00000000	32	√	√	√	√
SRC2 interrupt enable register 0	SRC2_INT_ENABLE0	R/W	H'EC50 0058	H'00000000	32	√	√	√	√
SRC3in_BUSIF_MODE register	SRC3in_BUSIF_MODE	R/W	H'EC50 0060	H'00000001	32	√	√	√	√
SRC3out_BUSIF_MODE register	SRC3out_BUSIF_MODE	R/W	H'EC50 0064	H'00000001	32	√	√	√	√

						RZ/G Series Products			
Name	Abbreviation	R/W	Address	Initial Value	Access Size	RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
SRC3_BUSIF_DALIGN register	SRC3_BUSIF_DALIGN	R/W	H'EC50 0068	H'76543210	32	√	√	√	√
SRC3_MODE register	SRC3_MODE	R/W	H'EC50 006C	H'00000000	32	√	√	√	√
SRC3 control register	SRC3_CONTROL	R/W	H'EC50 0070	H'00000000	32	√	√	√	√
SRC3 status register	SRC3_STATUS	R	H'EC50 0074	H'00000000	32	√	√	√	√
SRC3 interrupt enable register 0	SRC3_INT_ENABLE0	R/W	H'EC50 0078	H'00000000	32	√	√	√	√
SRC4in_BUSIF_MODE register	SRC4in_BUSIF_MODE	R/W	H'EC50 0080	H'00000001	32	√	√	√	√
SRC4out_BUSIF_MODE register	SRC4out_BUSIF_MODE	R/W	H'EC50 0084	H'00000001	32	√	√	√	√
SRC4_BUSIF_DALIGN register	SRC4_BUSIF_DALIGN	R/W	H'EC50 0088	H'76543210	32	√	√	√	√
SRC4_MODE register	SRC4_MODE	R/W	H'EC50 008C	H'00000000	32	√	√	√	√
SRC4 control register	SRC4_CONTROL	R/W	H'EC50 0090	H'00000000	32	√	√	√	√
SRC4 status register	SRC4_STATUS	R	H'EC50 0094	H'00000000	32	√	√	√	√
SRC4 interrupt enable register 0	SRC4_INT_ENABLE0	R/W	H'EC50 0098	H'00000000	32	√	√	√	√
SRC5in_BUSIF_MODE register	SRC5in_BUSIF_MODE	R/W	H'EC50 00A0	H'00000001	32	√	√	√	√
SRC5out_BUSIF_MODE register	SRC5out_BUSIF_MODE	R/W	H'EC50 00A4	H'00000001	32	√	√	√	√
SRC5_BUSIF_DALIGN register	SRC5_BUSIF_DALIGN	R/W	H'EC50 00A8	H'00000010	32	√	√	√	√
SRC5_MODE register	SRC5_MODE	R/W	H'EC50 00AC	H'00000000	32	√	√	√	√
SRC5 control register	SRC5_CONTROL	R/W	H'EC50 00B0	H'00000000	32	√	√	√	√
SRC5 status register	SRC5_STATUS	R	H'EC50 00B4	H'00000000	32	√	√	√	√
SRC5 interrupt enable register 0	SRC5_INT_ENABLE0	R/W	H'EC50 00B8	H'00000000	32	√	√	√	√
SRC6in_BUSIF_MODE register	SRC6in_BUSIF_MODE	R/W	H'EC50 00C0	H'00000001	32	√	√	√	√
SRC6out_BUSIF_MODE register	SRC6out_BUSIF_MODE	R/W	H'EC50 00C4	H'00000001	32	√	√	√	√
SRC6_BUSIF_DALIGN register	SRC6_BUSIF_DALIGN	R/W	H'EC50 00C8	H'00000010	32	√	√	√	√
SRC6_MODE register	SRC6_MODE	R/W	H'EC50 00CC	H'00000000	32	√	√	√	√
SRC6 control register	SRC6_CONTROL	R/W	H'EC50 00D0	H'00000000	32	√	√	√	√
SRC6 status register	SRC6_STATUS	R	H'EC50 00D4	H'00000000	32	√	√	√	√
SRC6 interrupt enable register 0	SRC6_INT_ENABLE0	R/W	H'EC50 00D8	H'00000000	32	√	√	√	√
SRC7in_BUSIF_MODE register	SRC7in_BUSIF_MODE	R/W	H'EC50 00E0	H'00000001	32	√	√	√	—
SRC7out_BUSIF_MODE register	SRC7out_BUSIF_MODE	R/W	H'EC50 00E4	H'00000001	32	√	√	√	—



Name	Abbreviation	R/W	Address	Initial Value	Access Size	RZ/G Series Products			
						RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
SRC7_BUSIF_DALIGN register	SRC7_BUSIF_DALIGN	R/W	H'EC50 00E8	H'00000010	32	√	√	√	—
SRC7_MODE register	SRC7_MODE	R/W	H'EC50 00EC	H'00000000	32	√	√	√	—
SRC7 control register	SRC7_CONTROL	R/W	H'EC50 00F0	H'00000000	32	√	√	√	—
SRC7 status register	SRC7_STATUS	R	H'EC50 00F4	H'00000000	32	√	√	√	—
SRC7 interrupt enable register 0	SRC7_INT_ENABLE0	R/W	H'EC50 00F8	H'00000000	32	√	√	√	—
SRC8in_BUSIF_MODE register	SRC8in_BUSIF_MODE	R/W	H'EC50 0100	H'00000001	32	√	√	√	—
SRC8out_BUSIF_MODE register	SRC8out_BUSIF_MODE	R/W	H'EC50 0104	H'00000001	32	√	√	√	—
SRC8_BUSIF_DALIGN register	SRC8_BUSIF_DALIGN	R/W	H'EC50 0108	H'00000010	32	√	√	√	—
SRC8_MODE register	SRC8_MODE	R/W	H'EC50 010C	H'00000000	32	√	√	√	—
SRC8 control register	SRC8_CONTROL	R/W	H'EC50 0110	H'00000000	32	√	√	√	—
SRC8 status register	SRC8_STATUS	R	H'EC50 0114	H'00000000	32	√	√	√	—
SRC8 interrupt enable register 0	SRC8_INT_ENABLE0	R/W	H'EC50 0118	H'00000000	32	√	√	√	—
SRC9in_BUSIF_MODE register	SRC9in_BUSIF_MODE	R/W	H'EC50 0120	H'00000001	32	√	√	√	—
SRC9out_BUSIF_MODE register	SRC9out_BUSIF_MODE	R/W	H'EC50 0124	H'00000001	32	√	√	√	—
SRC9_BUSIF_DALIGN register	SRC9_BUSIF_DALIGN	R/W	H'EC50 0128	H'00000010	32	√	√	√	—
SRC9_MODE register	SRC9_MODE	R/W	H'EC50 012C	H'00000000	32	√	√	√	—
SRC9 control register	SRC9_CONTROL	R/W	H'EC50 0130	H'00000000	32	√	√	√	—
SRC9 status register	SRC9_STATUS	R	H'EC50 0134	H'00000000	32	√	√	√	—
SRC9 interrupt enable register 0	SRC9_INT_ENABLE0	R/W	H'EC50 0138	H'00000000	32	√	√	√	—
CMD0out_BUSIF_MODE register	CMD0out_BUSIF_MODE	R/W	H'EC50 0184	H'00000001	32	√	√	√	√
CMD0_BUSIF_DALIGN register	CMD0_BUSIF_DALIGN	R/W	H'EC50 0188	H'76543210	32	√	√	√	√
CMD0_ROUTE_SELECT register	CMD0_ROUTE_SELECT	R/W	H'EC50 018C	H'00000000	32	√	√	√	√
CMD0 control register	CMD0_CONTROL	R/W	H'EC50 0190	H'00000000	32	√	√	√	√
CMD1out_BUSIF_MODE register	CMD1out_BUSIF_MODE	R/W	H'EC50 01A4	H'00000001	32	√	√	√	√
CMD1_BUSIF_DALIGN register	CMD1_BUSIF_DALIGN	R/W	H'EC50 01A8	H'76543210	32	√	√	√	√
CMD1_ROUTE_SELECT register	CMD1_ROUTE_SELECT	R/W	H'EC50 01AC	H'00000000	32	√	√	√	√
CMD1 control register	CMD1_CONTROL	R/W	H'EC50 01B0	H'00000000	32	√	√	√	√
SCU SYSTEM status register 0	SCU_SYSTEM_STATUS 0	R/WC1	H'EC5001C8	H'00000000	32	√	√	√	√

						RZ/G Series Products			
Name	Abbreviation	R/W	Address	Initial Value	Access Size	RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
SCU SYSTEM interrupt enable register 0	SCU_SYSTEM_INT_ENABLE0	R/W	H'EC5001CC	H'00000000	32	√	√	√	√
SCU SYSTEM status register 1	SCU_SYSTEM_STATUS1	R/WC1	H'EC5001D0	H'00000000	32	√	√	√	√
SCU SYSTEM interrupt enable register 1	SCU_SYSTEM_INT_ENABLE1	R/W	H'EC5001D4	H'00000000	32	√	√	√	√
SRC registers			SRC0_BASE: H'EC50 0200			√	√	√	—
			SRC1_BASE: H'EC50 0240			√	√	√	√
			SRC2_BASE: H'EC50 0280			√	√	√	√
			SRC3_BASE: H'EC50 02C0			√	√	√	√
			SRC4_BASE: H'EC50 0300			√	√	√	√
			SRC5_BASE: H'EC50 0340			√	√	√	√
			SRC6_BASE: H'EC50 0380			√	√	√	√
			SRC7_BASE: H'EC50 03C0			√	√	√	—
			SRC8_BASE: H'EC50 0400			√	√	√	—
			SRC9_BASE: H'EC50 0440			√	√	√	—
SRCm software reset register	SRCm_SWRSR	R/W	SRCm_BASE + H'00	H'00000001	32	√	√	√	√
SRCm SRC initialization register	SRCm_SRCIR	R/W	SRCm_BASE + H'04	H'00000001	32	√	√	√	√
SRCm audio information register	SRCm_ADINR	R/W	SRCm_BASE + H'14	H'00000000	32	√	√	√	√
SRCm IFS control register	SRCm_IFSCR	R/W	SRCm_BASE + H'1C	H'00000000	32	√	√	√	√
SRCm IFS value setting register	SRCm_IFSVR	R/W	SRCm_BASE + H'20	H'00000000	32	√	√	√	√
SRCm SRC control register	SRCm_SRCCR	R/W	SRCm_BASE + H'24	H'00000000	32	√	√	√	√
SRCm buffer size DATA RAM setting register	SRCm_BSDSR	R/W	SRCm_BASE + H'2C	H'00000000	32	√	√	√	√
SRCm buffer size IJEC RAM setting register	SRCm_BSISR	R/W	SRCm_BASE + H'38	H'00000000	32	√	√	√	√

Name	Abbreviation	R/W	Address	Initial Value	Access Size	RZ/G Series Products			
						RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
CTU registers			CTU00_BASE: H'EC50 0500			√	√	√	√
			CTU01_BASE: H'EC50 0600						
			CTU02_BASE: H'EC50 0700						
			CTU03_BASE: H'EC50 0800						
			CTU10_BASE: H'EC50 0900						
			CTU11_BASE: H'EC50 0A00						
			CTU12_BASE: H'EC50 0B00						
			CTU13_BASE: H'EC50 0C00						
CTUn software reset register	CTUn_SWRSR	R/W	CTUn_BASE + H'00	H'00000001	32	√	√	√	√
CTUn CTU initialization register	CTUn_CTUIR	R/W	CTUn_BASE + H'04	H'00000001	32	√	√	√	√
CTUn audio information register	CTUn_ADINR	R/W	CTUn_BASE + H'08	H'00000000	32	√	√	√	√
CTUn CTU pass mode register	CTUn_CPMDR	R/W	CTUn_BASE + H'10	H'00000000	32	√	√	√	√
CTUn scale mode register	CTUn_SCMDR	R/W	CTUn_BASE + H'14	H'00000000	32	√	√	√	√
CTUn scale value e00 register	CTUn_SV00R	R/W	CTUn_BASE + H'18	H'00000000	32	√	√	√	√
CTUn scale value e01 register	CTUn_SV01R	R/W	CTUn_BASE + H'1C	H'00000000	32	√	√	√	√
CTUn scale value e02 register	CTUn_SV02R	R/W	CTUn_BASE + H'20	H'00000000	32	√	√	√	√
CTUn scale value e03 register	CTUn_SV03R	R/W	CTUn_BASE + H'24	H'00000000	32	√	√	√	√
CTUn scale value e04 register	CTUn_SV04R	R/W	CTUn_BASE + H'28	H'00000000	32	√	√	√	√
CTUn scale value e05 register	CTUn_SV05R	R/W	CTUn_BASE + H'2C	H'00000000	32	√	√	√	√
CTUn scale value e06 register	CTUn_SV06R	R/W	CTUn_BASE + H'30	H'00000000	32	√	√	√	√
CTUn scale value e07 register	CTUn_SV07R	R/W	CTUn_BASE + H'34	H'00000000	32	√	√	√	√
CTUn scale value e10 register	CTUn_SV10R	R/W	CTUn_BASE + H'38	H'00000000	32	√	√	√	√
CTUn scale value e11 register	CTUn_SV11R	R/W	CTUn_BASE + H'3C	H'00000000	32	√	√	√	√

Name	Abbreviation	R/W	Address	Initial Value	Access Size	RZ/G Series Products			
						RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
CTUn scale value e12 register	CTUn_SV12R	R/W	CTUn_BASE + H'40	H'00000000	32	√	√	√	√
CTUn scale value e13 register	CTUn_SV13R	R/W	CTUn_BASE + H'44	H'00000000	32	√	√	√	√
CTUn scale value e14 register	CTUn_SV14R	R/W	CTUn_BASE + H'48	H'00000000	32	√	√	√	√
CTUn scale value e15 register	CTUn_SV15R	R/W	CTUn_BASE + H'4C	H'00000000	32	√	√	√	√
CTUn scale value e16 register	CTUn_SV16R	R/W	CTUn_BASE + H'50	H'00000000	32	√	√	√	√
CTUn scale value e17 register	CTUn_SV17R	R/W	CTUn_BASE + H'54	H'00000000	32	√	√	√	√
CTUn scale value e20 register	CTUn_SV20R	R/W	CTUn_BASE + H'58	H'00000000	32	√	√	√	√
CTUn scale value e21 register	CTUn_SV21R	R/W	CTUn_BASE + H'5C	H'00000000	32	√	√	√	√
CTUn scale value e22 register	CTUn_SV22R	R/W	CTUn_BASE + H'60	H'00000000	32	√	√	√	√
CTUn scale value e23 register	CTUn_SV23R	R/W	CTUn_BASE + H'64	H'00000000	32	√	√	√	√
CTUn scale value e24 register	CTUn_SV24R	R/W	CTUn_BASE + H'68	H'00000000	32	√	√	√	√
CTUn scale value e25 register	CTUn_SV25R	R/W	CTUn_BASE + H'6C	H'00000000	32	√	√	√	√
CTUn scale value e26 register	CTUn_SV26R	R/W	CTUn_BASE + H'70	H'00000000	32	√	√	√	√
CTUn scale value e27 register	CTUn_SV27R	R/W	CTUn_BASE + H'74	H'00000000	32	√	√	√	√
CTUn scale value e30 register	CTUn_SV30R	R/W	CTUn_BASE + H'78	H'00000000	32	√	√	√	√
CTUn scale value e31 register	CTUn_SV31R	R/W	CTUn_BASE + H'7C	H'00000000	32	√	√	√	√
CTUn scale value e32 register	CTUn_SV32R	R/W	CTUn_BASE + H'80	H'00000000	32	√	√	√	√
CTUn scale value e33 register	CTUn_SV33R	R/W	CTUn_BASE + H'84	H'00000000	32	√	√	√	√
CTUn scale value e34 register	CTUn_SV34R	R/W	CTUn_BASE + H'88	H'00000000	32	√	√	√	√
CTUn scale value e35 register	CTUn_SV35R	R/W	CTUn_BASE + H'8C	H'00000000	32	√	√	√	√
CTUn scale value e36 register	CTUn_SV36R	R/W	CTUn_BASE + H'90	H'00000000	32	√	√	√	√
CTUn scale value e37 register	CTUn_SV37R	R/W	CTUn_BASE + H'94	H'00000000	32	√	√	√	√

Name	Abbreviation	R/W	Address	Initial Value	Access Size	RZ/G Series Products			
						RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
MIX registers			MIX0_BASE: H'EC50 0D00  MIX1_BASE: H'EC50 0D40			√	√	√	√
MIXp software reset register	MIXp_SWRSR	R/W	MIXp_BASE + H'00	H'00000001	32	√	√	√	√
MIXp MIX initialization register	MIXp_MIXIR	R/W	MIXp_BASE + H'04	H'00000001	32	√	√	√	√
MIXp audio information register	MIXp_ADINR	R/W	MIXp_BASE + H'08	H'00000000	32	√	√	√	√
MIXp MIX mode register	MIXp_MIXMR	R/W	MIXp_BASE + H'10	H'00000000	32	√	√	√	√
MIXp MIX volume period register	MIXp_MVPDR	R/W	MIXp_BASE + H'14	H'00000000	32	√	√	√	√
MIXp MIX decibel A register	MIXp_MDBAR	R/W	MIXp_BASE + H'18	H'00000000	32	√	√	√	√
MIXp MIX decibel B register	MIXp_MDBBR	R/W	MIXp_BASE + H'1C	H'00000000	32	√	√	√	√
MIXp MIX decibel C register	MIXp_MDBCR	R/W	MIXp_BASE + H'20	H'00000000	32	√	√	√	√
MIXp MIX decibel D register	MIXp_MDBDR	R/W	MIXp_BASE + H'24	H'00000000	32	√	√	√	√
MIXp MIX decibel enable register	MIXp_MDBER	R/W	MIXp_BASE + H'28	H'00000000	32	√	√	√	√
MIXp MIX Status register	MIXp_MIXSR	R	MIXp_BASE + H'2C	H'00000000	32	√	√	√	√
DVC registers			DVC0_BASE: H'EC50 0E00  DVC1_BASE: H'EC50 0F00			√	√	√	√
DVCp software reset register	DVCp_SWRSR	R/W	DVCp_BASE + H'00	H'00000001	32	√	√	√	√
DVCp DVU initialization register	DVCp_DVUIR	R/W	DVCp_BASE + H'04	H'00000001	32	√	√	√	√
DVCp audio information register	DVCp_ADINR	R/W	DVCp_BASE + H'08	H'00000000	32	√	√	√	√
DVCp DVU control register	DVCp_DVUCR	R/W	DVCp_BASE + H'10	H'00000000	32	√	√	√	√
DVCp zero cross mute control register	DVCp_ZCMCR	R/W	DVCp_BASE + H'14	H'00000000	32	√	√	√	√
DVCp volume ramp control register	DVCp_VRCTR	R/W	DVCp_BASE + H'18	H'00000000	32	√	√	√	√
DVCp volume ramp Period register	DVCp_VRPDR	R/W	DVCp_BASE + H'1C	H'00000000	32	√	√	√	√
DVCp volume ramp decibel register	DVCp_VRDBR	R/W	DVCp_BASE + H'20	H'00000000	32	√	√	√	√

Name	Abbreviation	R/W	Address	Initial Value	Access Size	RZ/G Series Products			
						RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
DVCp volume ramp wait time register	DVCp_VRWTR	R/W	DVCp_BASE + H'24	H'00000000	32	√	√	√	√
DVCp volume value setting 0 register	DVCp_VOL0R	R/W	DVCp_BASE + H'28	H'00000000	32	√	√	√	√
DVCp volume value setting 1 register	DVCp_VOL1R	R/W	DVCp_BASE + H'2C	H'00000000	32	√	√	√	√
DVCp volume value setting 2 register	DVCp_VOL2R	R/W	DVCp_BASE + H'30	H'00000000	32	√	√	√	√
DVCp volume value setting 3 register	DVCp_VOL3R	R/W	DVCp_BASE + H'34	H'00000000	32	√	√	√	√
DVCp volume value setting 4 register	DVCp_VOL4R	R/W	DVCp_BASE + H'38	H'00000000	32	√	√	√	√
DVCp volume value setting 5 register	DVCp_VOL5R	R/W	DVCp_BASE + H'3C	H'00000000	32	√	√	√	√
DVCp volume value setting 6 register	DVCp_VOL6R	R/W	DVCp_BASE + H'40	H'00000000	32	√	√	√	√
DVCp volume value setting 7 register	DVCp_VOL7R	R/W	DVCp_BASE + H'44	H'00000000	32	√	√	√	√
DVCp DVU enable register	DVCp_DVUER	R/W	DVCp_BASE + H'48	H'00000000	32	√	√	√	√
DVCp DVU status register	DVCp_DVUSR	R	DVCp_BASE + H'4C	H'00000008	32	√	√	√	√
DVCp interrupt enable register	DVCp_DVIER	R/W	DVCp_BASE + H'50	H'00000000	32	√	√	√	√
SRC0in write data register	SRC0in_BUSIF	-/W	H'EC00 0000/ H'EC30 0000*	H'00000000	32	√	√	√	—
SRC1in write data register	SRC1in_BUSIF	-/W	H'EC00 0400/ H'EC30 0400*	H'00000000	32	√	√	√	√
SRC2in write data register	SRC2in_BUSIF	-/W	H'EC00 0800/ H'EC30 0800*	H'00000000	32	√	√	√	√
SRC3in write data register	SRC3in_BUSIF	-/W	H'EC00 0C00/ H'EC30 0C00*	H'00000000	32	√	√	√	√
SRC4in write data register	SRC4in_BUSIF	-/W	H'EC00 1000/ H'EC30 1000*	H'00000000	32	√	√	√	√
SRC5in write data register	SRC5in_BUSIF	-/W	H'EC00 1400/ H'EC30 1400*	H'00000000	32	√	√	√	√
SRC6in write data register	SRC6in_BUSIF	-/W	H'EC00 1800/ H'EC30 1800*	H'00000000	32	√	√	√	√
SRC7in write data register	SRC7in_BUSIF	-/W	H'EC00 1C00/ H'EC30 1C00*	H'00000000	32	√	√	√	—
SRC8in write data register	SRC8in_BUSIF	-/W	H'EC00 2000/ H'EC30 2000*	H'00000000	32	√	√	√	—

Name	Abbreviation	R/W	Address	Initial Value	Access Size	RZ/G Series Products			
						RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
SRC9in write data register	SRC9in_BUSIF	-W	H'EC00 2400/ H'EC30 2400*	H'00000000	32	√	√	√	—
SRC0out read data register	SRC0out_BUSIF	R	H'EC00 4000/ H'EC30 4000*	H'00000000	32	√	√	√	—
SRC1out read data register	SRC1out_BUSIF	R	H'EC00 4400/ H'EC30 4400*	H'00000000	32	√	√	√	√
SRC2out read data register	SRC2out_BUSIF	R	H'EC00 4800/ H'EC30 4800*	H'00000000	32	√	√	√	√
SRC3out read data register	SRC3out_BUSIF	R	H'EC00 4C00/ H'EC30 4C00*	H'00000000	32	√	√	√	√
SRC4out read data register	SRC4out_BUSIF	R	H'EC00 5000/ H'EC30 5000*	H'00000000	32	√	√	√	√
SRC5out read data register	SRC5out_BUSIF	R	H'EC00 5400/ H'EC30 5400*	H'00000000	32	√	√	√	√
SRC6out read data register	SRC6out_BUSIF	R	H'EC00 5800/ H'EC30 5800*	H'00000000	32	√	√	√	√
SRC7out read data register	SRC7out_BUSIF	R	H'EC00 5C00/ H'EC30 5C00*	H'00000000	32	√	√	√	—
SRC8out read data register	SRC8out_BUSIF	R	H'EC00 6000/ H'EC30 6000*	H'00000000	32	√	√	√	—
SRC9out read data register	SRC9out_BUSIF	R	H'EC00 6400/ H'EC30 6400*	H'00000000	32	√	√	√	—
CMD0out read data register	CMD0out_BUSIF	R	H'EC00 8000/ H'EC30 8000*	H'00000000	32	√	√	√	√
CMD1out read data register	CMD1out_BUSIF	R	H'EC00 8400/ H'EC30 8400*	H'00000000	32	√	√	√	√

Notes: [RZ/G1H, RZ/G1M, RZ/G1N]

m = 0 to 9; n = 00, 01, 02, 03, 10, 11, 12, or 13; p = 0 or 1

[RZ/G1E]

m = 1 to 6; n = 00, 01, 02, 03, 10, 11, 12, or 13; p = 0 or 1

\* H'EC00 XXXX is the address for transferring by Audio-DMAC. H'EC30 XXXX is the address for transferring by Audio-DMAC (Peripheral-Peripheral).

## 34.2 Register Description

### Legend for Register Description

Initial value: Register value after a reset. H'xxxx represents a hexadecimal number. Others are represented in binary numbers.

—: Undefined value

R/W: Readable/writable. The written value can be read.

R: Read-only. The write value should always be 0.

R/WC0: Readable/writable. Writing 0 initializes the bit. Writing 1 is ignored.

R/WC1: Readable/writable. Writing 1 initializes the bit. Writing 0 is ignored.

W: Write-only. Reading this bit is prohibited. When the bit is reserved, the write value should always be 0.

—/W: Write-only. The read value is undefined.

All access to registers is made in longword units.



### 34.2.1 SRCm(in/out)\_BUSIF\_MODE Register (SRCm(in/out)\_BUSIF\_MODE)

Note: RZ/G1H, M and N: m = 0 to 9, RZ/G1E: m = 1 to 6

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: SRCm (in/out)\_BUSIF\_MODE sets the initial setting for the bus interface.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	sft_dir	sft_num			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	dma
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 21	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
20	sft_dir	0	R/W	srcm(in/out)_busif_shift_dir Selects the bit-shift direction for position adjustment of the valid SRCm(in/out)_BUSIF input and output data. 0: Shift to left. 1: Shift to right.
19 to 16	sft_num	0000	R/W	srcm(in/out)_busif_shift_num Selects the bit-shift count for position adjustment of the valid SRCm(in/out)_BUSIF input and output data. 0000: 0 bit 0001: 1 bit 0010: 2 bits 0011: 3 bits 0100: 4 bits 0101: 5 bits 0110: 6 bits 0111: 7 bits 1000: 8 bits 1001: 9 bits 1010: 10 bits 1011: 11 bits 1100: 12 bits 1101: 13 bits 1110: 14 bits 1111: 15 bits
15 to 1	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.

---

Bit	Bit Name	Initial Value	R/W	Description
0	dma	1	R/W	<i>srcm</i> (in/out)_busif_dma Selects the access type for SRC <i>m</i> (in/out)_BUSIF. 0: PIO access (setting prohibited) 1: DMA access Be sure to specify the DMA access.

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### 34.2.2 SRCm\_BUSIF\_DALIGN Register (SRCm\_BUSIF\_DALIGN)

Note: RZ/G1H, M and N: m = 0, 1, 3, or 4, RZ/G1E: m = 1, 3, or 4

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: SRCm\_BUSIF\_DALIGN determines the initial settings of the SRCm route.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	place7			—	place6			—	place5			—	place4		
Initial value:	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	0
R/W:	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	place3			—	place2			—	place1			—	place0		
Initial value:	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0
R/W:	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
30 to 28	place7	111	R/W	Changes the stream data order. These bits are used for the 8-channel setting. <b>For the 6- or less-channel setting, the initial value should not be changed.</b> The data order is changed before input to the SRC. Selects the input-side data to be output to place 7 on the output side. 000: Data at input-side place 0 is sent to output-side place 7. 001: Data at input-side place 1 is sent to output-side place 7. 010: Data at input-side place 2 is sent to output-side place 7. 011: Data at input-side place 3 is sent to output-side place 7. 100: Data at input-side place 4 is sent to output-side place 7. 101: Data at input-side place 5 is sent to output-side place 7. 110: Data at input-side place 6 is sent to output-side place 7. 111: Data at input-side place 7 is sent to output-side place 7.
27	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
26 to 24	place6	110	R/W	<p>Changes the stream data order. These bits are used for the 8-channel setting. <b>For the 6- or less-channel setting, the initial value should not be changed.</b></p> <p>The data order is changed before input to the SRC.</p> <p>Selects the input-side data to be output to place 6 on the output side.</p> <p>000: Data at input-side place 0 is sent to output-side place 6.            001: Data at input-side place 1 is sent to output-side place 6.            010: Data at input-side place 2 is sent to output-side place 6.            011: Data at input-side place 3 is sent to output-side place 6.            100: Data at input-side place 4 is sent to output-side place 6.            101: Data at input-side place 5 is sent to output-side place 6.            110: Data at input-side place 6 is sent to output-side place 6.            111: Data at input-side place 7 is sent to output-side place 6.</p>
23	—	0	R	<p>Reserved</p> <p>This bit is always read as 0. The write value should always be 0.</p>
22 to 20	place5	101	R/W	<p>Changes the stream data order. These bits are used for the 6- or more-channel setting. <b>For the 4- or less-channel setting, the initial value should not be changed.</b></p> <p>The data order is changed before input to the SRC.</p> <p>Selects the input-side data to be output to place 5 on the output side.</p> <p>000: Data at input-side place 0 is sent to output-side place 5.            001: Data at input-side place 1 is sent to output-side place 5.            010: Data at input-side place 2 is sent to output-side place 5.            011: Data at input-side place 3 is sent to output-side place 5.            100: Data at input-side place 4 is sent to output-side place 5.            101: Data at input-side place 5 is sent to output-side place 5.            110: Data at input-side place 6 is sent to output-side place 5.            111: Data at input-side place 7 is sent to output-side place 5.</p>
19	—	0	R	<p>Reserved</p> <p>This bit is always read as 0. The write value should always be 0.</p>
18 to 16	place4	100	R/W	<p>Changes the stream data order. These bits are used for the 6- or more-channel setting. <b>For the 4- or less-channel setting, the initial value should not be changed.</b></p> <p>The data order is changed before input to the SRC.</p> <p>Selects the input-side data to be output to place 4 on the output side.</p> <p>000: Data at input-side place 0 is sent to output-side place 4.            001: Data at input-side place 1 is sent to output-side place 4.            010: Data at input-side place 2 is sent to output-side place 4.            011: Data at input-side place 3 is sent to output-side place 4.            100: Data at input-side place 4 is sent to output-side place 4.            101: Data at input-side place 5 is sent to output-side place 4.            110: Data at input-side place 6 is sent to output-side place 4.            111: Data at input-side place 7 is sent to output-side place 4.</p>
15	—	0	R	<p>Reserved</p> <p>This bit is always read as 0. The write value should always be 0.</p>

Bit	Bit Name	Initial Value	R/W	Description
14 to 12	place3	011	R/W	<p>Changes the stream data order. These bits are used for the 4- or more-channel setting. <b>For the 2- or less-channel setting, the initial value should not be changed.</b></p> <p>The data order is changed before input to the SRC.</p> <p>Selects the input-side data to be output to place 3 on the output side.</p> <p>000: Data at input-side place 0 is sent to output-side place 3.            001: Data at input-side place 1 is sent to output-side place 3.            010: Data at input-side place 2 is sent to output-side place 3.            011: Data at input-side place 3 is sent to output-side place 3.            100: Data at input-side place 4 is sent to output-side place 3.            101: Data at input-side place 5 is sent to output-side place 3.            110: Data at input-side place 6 is sent to output-side place 3.            111: Data at input-side place 7 is sent to output-side place 3.</p>
11	—	0	R	<p>Reserved</p> <p>This bit is always read as 0. The write value should always be 0.</p>
10 to 8	place2	010	R/W	<p>Changes the stream data order. These bits are used for the 4- or more-channel setting. <b>For the 2- or less-channel setting, the initial value should not be changed.</b></p> <p>The data order is changed before input to the SRC.</p> <p>Selects the input-side data to be output to place 2 on the output side.</p> <p>000: Data at input-side place 0 is sent to output-side place 2.            001: Data at input-side place 1 is sent to output-side place 2.            010: Data at input-side place 2 is sent to output-side place 2.            011: Data at input-side place 3 is sent to output-side place 2.            100: Data at input-side place 4 is sent to output-side place 2.            101: Data at input-side place 5 is sent to output-side place 2.            110: Data at input-side place 6 is sent to output-side place 2.            111: Data at input-side place 7 is sent to output-side place 2.</p>
7	—	0	R	<p>Reserved</p> <p>This bit is always read as 0. The write value should always be 0.</p>
6 to 4	place1	001	R/W	<p>Changes the stream data order.</p> <p>The data order is changed before input to the SRC.</p> <p>Selects the input-side data to be output to place 1 on the output side.</p> <p>000: Data at input-side place 0 is sent to output-side place 1.            001: Data at input-side place 1 is sent to output-side place 1.            010: Data at input-side place 2 is sent to output-side place 1.            011: Data at input-side place 3 is sent to output-side place 1.            100: Data at input-side place 4 is sent to output-side place 1.            101: Data at input-side place 5 is sent to output-side place 1.            110: Data at input-side place 6 is sent to output-side place 1.            111: Data at input-side place 7 is sent to output-side place 1.</p>
3	—	0	R	<p>Reserved</p> <p>This bit is always read as 0. The write value should always be 0.</p>

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Bit	Bit Name	Initial Value	R/W	Description
2 to 0	place0	000	R/W	<p>Changes the stream data order.</p> <p>The data order is changed before input to the SRC.</p> <p>Selects the input-side data to be output to place 0 on the output side.</p> <p>000: Data at input-side place 0 is sent to output-side place 0.</p> <p>001: Data at input-side place 1 is sent to output-side place 0.</p> <p>010: Data at input-side place 2 is sent to output-side place 0.</p> <p>011: Data at input-side place 3 is sent to output-side place 0.</p> <p>100: Data at input-side place 4 is sent to output-side place 0.</p> <p>101: Data at input-side place 5 is sent to output-side place 0.</p> <p>110: Data at input-side place 6 is sent to output-side place 0.</p> <p>111: Data at input-side place 7 is sent to output-side place 0.</p>

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**34.2.3 SRCn\_BUSIF\_DALIGN Register (SRCn\_BUSIF\_DALIGN)**

Note: RZ/G1H, M and N: n = 2, 5, 6, 7, 8, or 9, RZ/G1E: n = 2, 5, or 6

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: SRCn\_BUSIF\_DALIGN determines the initial settings of the SRCn route.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	place1	—	—	—	place0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	place1	1	R/W	Changes the stream data order. The data order is changed before input to the SRC. Selects the input-side data to be output to place 1 on the output side. 0: Data at input-side place 0 is sent to output-side place 1. 1: Data at input-side place 1 is sent to output-side place 1.
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	place0	0	R/W	Changes the stream data order. The data order is changed before input to the SRC. Selects the input-side data to be output to place 0 on the output side. 0: Data at input-side place 0 is sent to output-side place 0. 1: Data at input-side place 1 is sent to output-side place 0.

### 34.2.4 SRCm\_MODE Register (SRCm\_MODE)

Note: RZ/G1H, M and N: m = 0 to 9, RZ/G1E: m = 1 to 6

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: SRCm\_MODE determines the initial settings of the SRCm route.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	sync_out	sync_in	—	—	—	—	—	—	—	uf_data
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R	R	R	R	R	R	R	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	src
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 26	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
25	sync_out	0	R/W	srcmout_sync Selects how to treat data in the SRC output buffer. 0: Asynchronous SRC 1: Synchronous SRC
24	sync_in	0	R/W	srcmin_sync Selects how to treat data in the SRC input buffer. 0: Asynchronous SRC 1: Synchronous SRC
23 to 17	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
16	uf_data	0	R/W	srcm_uf_data_sel Selects how to treat data when an underflow occurs in the SRC input buffer. 0: Data before the underflow occurs is output. 1: All 0s are output.
15 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	src	0	R/W	srcm_src Selects whether to use SRCm. 0: SRCm is not used. 1: SRCm is used.

- Notes: 1. Please set one of sync\_in and sync\_out bits, when SRCm is used in synchronous mode by setting SRCMD bit in SRCm\_SRCCR register.
2. If sync\_out is set in synchronous mode, data should directly transmit to memory. (Data should not transmit throughout CMD.)



### 34.2.5 SRCm Control Register (SRCm\_CONTROL)

Note: RZ/G1H, M and N: m = 0 to 9, RZ/G1E: m = 1 to 6

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: SRCm\_CONTROL starts or stops transfer.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	start_out	—	—	—	start_in
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	start_out	0	R/W	SRCmout_start_flag Starts or stops transfer via SRCm. 0: Stops transfer. 1: Starts transfer.
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	start_in	0	R/W	SRCmin_start_flag Starts or stops transfer via SRCm. 0: Stops transfer. 1: Starts transfer.

Note: [RZ/G1H, M, N]:

When CMD is used with route SRC0, SRC1, SRC2, SRC3, SRC4, or SRC5, SRCmout\_start\_flag should be set to 0 to stop transfer. When CMD is not used with route SRC0, SRC1, SRC2, SRC3, SRC4, or SRC5, or when route SRC6, SRC7, SRC8, or SRC9 is used, SRCmin\_start\_flag and SRCmout\_start\_flag should be set simultaneously.

[RZ/G1E]:

When CMD is used with route SRC1, SRC2, SRC3, SRC4, or SRC5, SRCmout\_start\_flag should be set to 0 to stop transfer. When CMD is not used with route SRC1, SRC2, SRC3, SRC4, or SRC5, SRCmin\_start\_flag and SRCmout\_start\_flag should be set simultaneously.

[RZ/G1H, M, N, E]:

When CMD is used and the sync\_in bit in the SRCm\_MODE register is set for synchronous mode, SRCmout\_start\_flag should be set to 1 to start transfer. However, in this case, use of the output data SRCm\_out\_BUSIF is prohibited and ignore the value of over\_flow\_srcout in the SRCm\_STATUS register.

### 34.2.6 SRCm Status Register (SRCm\_STATUS)

Note: RZ/G1H, M and N: m = 0 to 5, RZ/G1E: m = 1 to 5

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: SRCm\_STATUS indicates the state of each SRC. When a register bit is set, the corresponding interrupt signal is output. However, if interrupt outputs are masked by the SRCm interrupt enable register, interrupt signals are not output.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	dvc1	—	—	—	dvc0	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	uf_src0	of_src0	—	—	of_src1	uf_src1	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28	dvc1	0	R	dvc1 Indicates the state of the DVC1_DVUSR register collectively. The state information is used only for the interrupt signal that is enabled by DVC1_DVIER.
27 to 25	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
24	dvc0	0	R	dvc0 Indicates the state of the DVC0_DVUSR register collectively. The state information is used only for the interrupt signal that is enabled by DVC0_DVIER.
23 to 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13	uf_src0	0	R	under_flow_srcout Indicates the state of the output buffer of SRCout in the SCU_SYSTEM_STATUS1 register. The state information is used when the interrupt signal is enabled by SCU_SYSTEM_INT_ENABLE1.
12	of_src0	0	R	over_flow_srcout Indicates the state of the output buffer of SRCout in the SCU_SYSTEM_STATUS0 register. The state information is used when the interrupt signal is enabled by SCU_SYSTEM_INT_ENABLE0.
11, 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
9	of_srcin	0	R	over_flow_srcin Indicates the state of the output buffer of SRCin in the SCU_SYSTEM_STATUS1 register. The state information is used when the interrupt signal is enabled by SCU_SYSTEM_INT_ENABLE1.
8	uf_srcin	0	R	under_flow_srcin Indicates the state of the output buffer of SRCin in the SCU_SYSTEM_STATUS0 register. The state information is used when the interrupt signal is enabled by SCU_SYSTEM_INT_ENABLE0.
7 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

### 34.2.7 SRCn Status Register (SRCn\_STATUS)

Note: RZ/G1H, M and N: n = 6 to 9, RZ/G1E: n = 6

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: SRCn\_STATUS indicates the state of each SRC. When a register bit is set, the corresponding interrupt signal is output. However, if interrupt outputs are masked by the SRCn interrupt enable register, interrupt signals are not output.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	uf_src0	of_src0	—	—	of_src1	uf_src1	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13	uf_src0	0	R	under_flow_srcout Indicates the state of the output buffer of SRCout in the SCU_SYSTEM_STATUS1 register. The state information is used when the interrupt signal is enabled by SCU_SYSTEM_INT_ENABLE1.
12	of_src0	0	R	over_flow_srcout Indicates the state of the output buffer of SRCout in the SCU_SYSTEM_STATUS0 register. The state information is used when the interrupt signal is enabled by SCU_SYSTEM_INT_ENABLE0.
11, 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9	of_src1	0	R	over_flow_srcin Indicates the state of the output buffer of SRCin in the SCU_SYSTEM_STATUS1 register. The state information is used when the interrupt signal is enabled by SCU_SYSTEM_INT_ENABLE1.
8	uf_src1	0	R	under_flow_srcin Indicates the state of the output buffer of SRCin in the SCU_SYSTEM_STATUS0 register. The state information is used when the interrupt signal is enabled by SCU_SYSTEM_INT_ENABLE0.
7 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

### 34.2.8 SRCm Interrupt Enable Register 0 (SRCm\_INT\_ENABLE0)

Note: RZ/G1H, M and N: m = 0 to 5, RZ/G1E: m = 1 to 5

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: SRCm\_INT\_ENABLE0 enables or disables output of interrupts corresponding to the states indicated in the SRCm status register.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	dvc1_ie	—	—	—	dvc0_ie	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R	R	R	R/W	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	uf_srco_ie	of_srco_ie	—	—	of_srci_ie	uf_srci_ie	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R	R	R/W	R/W	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28	dvc1_ie	0	R/W	dvc1_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
27 to 25	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
24	dvc0_ie	0	R/W	dvc0_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
23 to 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13	uf_srco_ie	0	R/W	under_flow_srcout_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
12	of_srco_ie	0	R/W	over_flow_srcout_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
11, 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9	of_srci_ie	0	R/W	over_flow_srcin_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.

Bit	Bit Name	Initial Value	R/W	Description
8	uf_srcie	0	R/W	under_flow_srcin_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
7 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

### 34.2.9 SRCn Interrupt Enable Register 0 (SRCn\_INT\_ENABLE0)

Note: RZ/G1H, M and N: n = 6 to 9, RZ/G1E: n = 6

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: SRCn\_INT\_ENABLE0 enables or disables output of interrupts corresponding to the states indicated in the SRCn status register.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	uf_srco_ie	of_srco_ie	—	—	of_srcie	uf_srcie	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R	R	R/W	R/W	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13	uf_srco_ie	0	R/W	under_flow_srcout_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
12	of_srco_ie	0	R/W	over_flow_srcout_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
11, 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9	of_srcie	0	R/W	over_flow_srcin_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
8	uf_srcie	0	R/W	under_flow_srcin_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
7 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

### 34.2.10 CMDn out\_BUSIF\_MODE Register (CMDn out\_BUSIF\_MODE)

Note: n = 0, 1

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: CMDn out\_BUSIF\_MODE sets the initial setting for the bus interface

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	sft_dir	sft_num			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	dma
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 21	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
20	sft_dir	0	R/W	cmdnout_busif_shift_dir Selects the bit-shift direction for position adjustment of the valid CMDnout_BUSIF input and output data. 0: Shift to left. 1: Shift to right.
19 to 16	sft_num	0000	R/W	cmdnout_busif_shift_num Selects the bit-shift count for position adjustment of the valid CMDnout_BUSIF input and output data. 0000: 0 bit 0001: 1 bit 0010: 2 bits 0011: 3 bits 0100: 4 bits 0101: 5 bits 0110: 6 bits 0111: 7 bits 1000: 8 bits 1001: 9 bits 1010: 10 bits 1011: 11 bits 1100: 12 bits 1101: 13 bits 1110: 14 bits 1111: 15 bits
15 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.



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Bit	Bit Name	Initial Value	R/W	Description
0	dma	1	R/W	CMDnout_busif_dma Selects the access type for CMDnout_BUSIF. 0: PIO access (setting prohibited) 1: DMA access Be sure to specify the DMA access.

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**34.2.11 CMDn\_BUSIF\_DALIGN Register (CMDn\_BUSIF\_DALIGN)**

Note: n = 0, 1

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: CMDn\_BUSIF\_DALIGN determines the initial settings of the CMDn route.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	place7			—	place6			—	place5			—	place4		
Initial value:	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	0
R/W:	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	place3			—	place2			—	place1			—	place0		
Initial value:	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0
R/W:	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
30 to 28	place7	111	R/W	Changes the stream data order. These bits are used for the 8-channel setting. <b>For the 6- or less-channel setting, the initial value should not be changed.</b> The data order is changed after output from the CMD. Selects the input-side data to be output to place 7 on the output side. 000: Data at input-side place 0 is sent to output-side place 7. 001: Data at input-side place 1 is sent to output-side place 7. 010: Data at input-side place 2 is sent to output-side place 7. 011: Data at input-side place 3 is sent to output-side place 7. 100: Data at input-side place 4 is sent to output-side place 7. 101: Data at input-side place 5 is sent to output-side place 7. 110: Data at input-side place 6 is sent to output-side place 7. 111: Data at input-side place 7 is sent to output-side place 7.
27	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
26 to 24	place6	110	R/W	<p>Changes the stream data order. These bits are used for the 8-channel setting. <b>For the 6- or less-channel setting, the initial value should not be changed.</b></p> <p>The data order is changed after output from the CMD.</p> <p>Selects the input-side data to be output to place 6 on the output side.</p> <p>000: Data at input-side place 0 is sent to output-side place 6.            001: Data at input-side place 1 is sent to output-side place 6.            010: Data at input-side place 2 is sent to output-side place 6.            011: Data at input-side place 3 is sent to output-side place 6.            100: Data at input-side place 4 is sent to output-side place 6.            101: Data at input-side place 5 is sent to output-side place 6.            110: Data at input-side place 6 is sent to output-side place 6.            111: Data at input-side place 7 is sent to output-side place 6.</p>
23	—	0	R	<p>Reserved</p> <p>This bit is always read as 0. The write value should always be 0.</p>
22 to 20	place5	101	R/W	<p>Changes the stream data order. These bits are used for the 6- or more-channel setting. <b>For the 4- or less-channel setting, the initial value should not be changed.</b></p> <p>The data order is changed after output from the CMD.</p> <p>Selects the input-side data to be output to place 5 on the output side.</p> <p>000: Data at input-side place 0 is sent to output-side place 5.            001: Data at input-side place 1 is sent to output-side place 5.            010: Data at input-side place 2 is sent to output-side place 5.            011: Data at input-side place 3 is sent to output-side place 5.            100: Data at input-side place 4 is sent to output-side place 5.            101: Data at input-side place 5 is sent to output-side place 5.            110: Data at input-side place 6 is sent to output-side place 5.            111: Data at input-side place 7 is sent to output-side place 5.</p>
19	—	0	R	<p>Reserved</p> <p>This bit is always read as 0. The write value should always be 0.</p>
18 to 16	place4	100	R/W	<p>Changes the stream data order. These bits are used for the 6- or more-channel setting. <b>For the 4- or less-channel setting, the initial value should not be changed.</b></p> <p>The data order is changed after output from the CMD.</p> <p>Selects the input-side data to be output to place 4 on the output side.</p> <p>000: Data at input-side place 0 is sent to output-side place 4.            001: Data at input-side place 1 is sent to output-side place 4.            010: Data at input-side place 2 is sent to output-side place 4.            011: Data at input-side place 3 is sent to output-side place 4.            100: Data at input-side place 4 is sent to output-side place 4.            101: Data at input-side place 5 is sent to output-side place 4.            110: Data at input-side place 6 is sent to output-side place 4.            111: Data at input-side place 7 is sent to output-side place 4.</p>
15	—	0	R	<p>Reserved</p> <p>This bit is always read as 0. The write value should always be 0.</p>

Bit	Bit Name	Initial Value	R/W	Description
14 to 12	place3	011	R/W	<p>Changes the stream data order. These bits are used for the 4- or more-channel setting. <b>For the 2- or less-channel setting, the initial value should not be changed.</b></p> <p>The data order is changed after output from the CMD.</p> <p>Selects the input-side data to be output to place 3 on the output side.</p> <p>000: Data at input-side place 0 is sent to output-side place 3.            001: Data at input-side place 1 is sent to output-side place 3.            010: Data at input-side place 2 is sent to output-side place 3.            011: Data at input-side place 3 is sent to output-side place 3.            100: Data at input-side place 4 is sent to output-side place 3.            101: Data at input-side place 5 is sent to output-side place 3.            110: Data at input-side place 6 is sent to output-side place 3.            111: Data at input-side place 7 is sent to output-side place 3.</p>
11	—	0	R	<p>Reserved</p> <p>This bit is always read as 0. The write value should always be 0.</p>
10 to 8	place2	010	R/W	<p>Changes the stream data order. These bits are used for the 4- or more-channel setting. <b>For the 2- or less-channel setting, the initial value should not be changed.</b></p> <p>The data order is changed after output from the CMD.</p> <p>Selects the input-side data to be output to place 2 on the output side.</p> <p>000: Data at input-side place 0 is sent to output-side place 2.            001: Data at input-side place 1 is sent to output-side place 2.            010: Data at input-side place 2 is sent to output-side place 2.            011: Data at input-side place 3 is sent to output-side place 2.            100: Data at input-side place 4 is sent to output-side place 2.            101: Data at input-side place 5 is sent to output-side place 2.            110: Data at input-side place 6 is sent to output-side place 2.            111: Data at input-side place 7 is sent to output-side place 2.</p>
7	—	0	R	<p>Reserved</p> <p>This bit is always read as 0. The write value should always be 0.</p>
6 to 4	place1	001	R/W	<p>Changes the stream data order.</p> <p>The data order is changed after output from the CMD.</p> <p>Selects the input-side data to be output to place 1 on the output side.</p> <p>000: Data at input-side place 0 is sent to output-side place 1.            001: Data at input-side place 1 is sent to output-side place 1.            010: Data at input-side place 2 is sent to output-side place 1.            011: Data at input-side place 3 is sent to output-side place 1.            100: Data at input-side place 4 is sent to output-side place 1.            101: Data at input-side place 5 is sent to output-side place 1.            110: Data at input-side place 6 is sent to output-side place 1.            111: Data at input-side place 7 is sent to output-side place 1.</p>
3	—	0	R	<p>Reserved</p> <p>This bit is always read as 0. The write value should always be 0.</p>

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Bit	Bit Name	Initial Value	R/W	Description
2 to 0	place0	000	R/W	<p>Changes the stream data order.</p> <p>The data order is changed after output from the CMD.</p> <p>Selects the input-side data to be output to place 0 on the output side.</p> <p>000: Data at input-side place 0 is sent to output-side place 0.</p> <p>001: Data at input-side place 1 is sent to output-side place 0.</p> <p>010: Data at input-side place 2 is sent to output-side place 0.</p> <p>011: Data at input-side place 3 is sent to output-side place 0.</p> <p>100: Data at input-side place 4 is sent to output-side place 0.</p> <p>101: Data at input-side place 5 is sent to output-side place 0.</p> <p>110: Data at input-side place 6 is sent to output-side place 0.</p> <p>111: Data at input-side place 7 is sent to output-side place 0.</p>

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**34.2.12 CMDn\_ROUTE\_SELECT Register (CMDn\_ROUTE\_SELECT)**

Note: n = 0, 1

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: CMDn\_ROUTE\_SELECT selects the sound route for each CMD (CTU, MIX, and DVC). Refer to Figures 34.1 and 34.11 for the sound routes.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	cmd_case		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	cmdin_ctu3	—	—	—	—	—	—	—	cmdin_ctu2
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 19	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
18 to 16	cmd_case	000	R/W	cmdn_case_sel Selects the route in CMDn. 000: Input audio data0 to 3 → CTU → MIX → DVC route is used. 001: Input audio data0 (from SRC3) → DVC route is used. 010: Input audio data1 (from SRC4) → DVC route is used. 011: Input audio data2 [RZ/G1H, M, N] (from SRC0 or SRC1) → DVC route is used. [RZ/G1E] (from SRC1) → DVC route is used. 100: Input audio data3 (from SRC2 or SRC5) → DVC route is used. Others: Setting prohibited.
15 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	cmdin_ctu3	0	R/W	cmdnin_ctu3_sel Selects SRC for Input audio data3 of CMDn. 0: SRC2 route is used. 1: SRC5 route is used.
7 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
0	cmdin_ctu2	0	R/W	cmdrin_ctu2_sel Selects SRC for Input audio data2 of CMDn. [RZ/G1H, M, N] 0: SRC0 route is used. 1: SRC1 route is used. [RZ/G1E] 0: Setting prohibited 1: SRC1 route is used.

### 34.2.13 CMDn Control Register (CMDn\_CONTROL)

Note: n = 0, 1

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: CMDn\_CONTROL starts or stops transfer.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	start_out	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	start_out	0	R/W	CMDnout_start_flag Starts or stops transfer via CMDn. 0: Stops transfer. 1: Starts transfer.
3 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

### 34.2.14 SCU\_SYSTEM Status Register 0 (SCU\_SYSTEM\_STATUS0)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

#### [RZ/G1H, M, N]

Function: SCU\_SYSTEM\_STATUS0 indicates the internal buffer state. When a register bit is set, the corresponding interrupt signal is output. However, if interrupt outputs are masked by the SYSTEM interrupt enable register 0, interrupt signals are not output.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	of_cmd1o	of_cmd0o	—	—	of_src9o	of_src8o	of_src7o	of_src6o	of_src5o	of_src4o	of_src3o	of_src2o	of_src1o	of_src0o
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/WC1	R/WC1	R	R	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	uf_src9i	uf_src8i	uf_src7i	uf_src6i	uf_src5i	uf_src4i	uf_src3i	uf_src2i	uf_src1i	uf_src0i
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1

Bit	Bit Name	Initial Value	R/W	Description
31, 30	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
29	of_cmd1o	0	R/WC1	over_flow_cmd1out Indicates the state of the CMD1out output buffer. 0: Normal operation 1: An overflow has occurred.
28	of_cmd0o	0	R/WC1	over_flow_cmd0out Indicates the state of the CMD0out output buffer. 0: Normal operation 1: An overflow has occurred.
27, 26	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
25	of_src9o	0	R/WC1	over_flow_src9out Indicates the state of the SRC9out output buffer. 0: Normal operation 1: An overflow has occurred.
24	of_src8o	0	R/WC1	over_flow_src8out Indicates the state of the SRC8out output buffer. 0: Normal operation 1: An overflow has occurred.
23	of_src7o	0	R/WC1	over_flow_src7out Indicates the state of the SRC7out output buffer. 0: Normal operation 1: An overflow has occurred.



Bit	Bit Name	Initial Value	R/W	Description
22	of_src6o	0	R/WC1	over_flow_src6out Indicates the state of the SRC6out output buffer. 0: Normal operation 1: An overflow has occurred.
21	of_src5o	0	R/WC1	over_flow_src5out Indicates the state of the SRC5out output buffer. 0: Normal operation 1: An overflow has occurred.
20	of_src4o	0	R/WC1	over_flow_src4out Indicates the state of the SRC4out output buffer. 0: Normal operation 1: An overflow has occurred.
19	of_src3o	0	R/WC1	over_flow_src3out Indicates the state of the SRC3out output buffer. 0: Normal operation 1: An overflow has occurred.
18	of_src2o	0	R/WC1	over_flow_src2out Indicates the state of the SRC6out output buffer. 0: Normal operation 1: An overflow has occurred.
17	of_src1o	0	R/WC1	over_flow_src1out Indicates the state of the SRC7out output buffer. 0: Normal operation 1: An overflow has occurred.
16	of_src0o	0	R/WC1	over_flow_src0out Indicates the state of the SRC0out output buffer. 0: Normal operation 1: An overflow has occurred.
15 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9	uf_src9i	0	R/WC1	under_flow_src9in Indicates the state of the SRC9in input buffer. 0: Normal operation 1: An underflow has occurred.
8	uf_src8i	0	R/WC1	under_flow_src8in Indicates the state of the SRC8in input buffer. 0: Normal operation 1: An underflow has occurred.
7	uf_src7i	0	R/WC1	under_flow_src7in Indicates the state of the SRC7in input buffer. 0: Normal operation 1: An underflow has occurred.

Bit	Bit Name	Initial Value	R/W	Description
6	uf_src6i	0	R/WC1	under_flow_src6in Indicates the state of the SRC6in input buffer. 0: Normal operation 1: An underflow has occurred.
5	uf_src5i	0	R/WC1	under_flow_src5in Indicates the state of the SRC5in input buffer. 0: Normal operation 1: An underflow has occurred.
4	uf_src4i	0	R/WC1	under_flow_src4in Indicates the state of the SRC4in input buffer. 0: Normal operation 1: An underflow has occurred.
3	uf_src3i	0	R/WC1	under_flow_src3in Indicates the state of the SRC3in input buffer. 0: Normal operation 1: An underflow has occurred.
2	uf_src2i	0	R/WC1	under_flow_src2in Indicates the state of the SRC2in input buffer. 0: Normal operation 1: An underflow has occurred.
1	uf_src1i	0	R/WC1	under_flow_src1in Indicates the state of the SRC1in input buffer. 0: Normal operation 1: An underflow has occurred.
0	uf_src0i	0	R/WC1	under_flow_src0in Indicates the state of the SRC0in input buffer. 0: Normal operation 1: An underflow has occurred.

[RZ/G1E]

Function: SCU\_SYSTEM\_STATUS0 indicates the internal buffer state. When a register bit is set, the corresponding interrupt signal is output. However, if interrupt outputs are masked by the SYSTEM interrupt enable register 0, interrupt signals are not output.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	of_cmd 1o	of_cmd 0o	—	—	—	—	—	of_src6 o	of_src5 o	of_src4 o	of_src3 o	of_src2 o	of_src1 o	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/WC1	R/WC1	R	R	R	R	R	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	uf_src6i	uf_src5i	uf_src4i	uf_src3i	uf_src2i	uf_src1i	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R

Bit	Bit Name	Initial Value	R/W	Description
31, 30	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
29	of_cmd1o	0	R/WC1	over_flow_cmd1out Indicates the state of the CMD1out output buffer. 0: Normal operation 1: An overflow has occurred.
28	of_cmd0o	0	R/WC1	over_flow_cmd0out Indicates the state of the CMD0out output buffer. 0: Normal operation 1: An overflow has occurred.
27 to 23	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
22	of_src6o	0	R/WC1	over_flow_src6out Indicates the state of the SRC6out output buffer. 0: Normal operation 1: An overflow has occurred.
21	of_src5o	0	R/WC1	over_flow_src5out Indicates the state of the SRC5out output buffer. 0: Normal operation 1: An overflow has occurred.
20	of_src4o	0	R/WC1	over_flow_src4out Indicates the state of the SRC4out output buffer. 0: Normal operation 1: An overflow has occurred.
19	of_src3o	0	R/WC1	over_flow_src3out Indicates the state of the SRC3out output buffer. 0: Normal operation 1: An overflow has occurred.
18	of_src2o	0	R/WC1	over_flow_src2out Indicates the state of the SRC6out output buffer. 0: Normal operation 1: An overflow has occurred.
17	of_src1o	0	R/WC1	over_flow_src1out Indicates the state of the SRC7out output buffer. 0: Normal operation 1: An overflow has occurred.
16 to 7	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
6	uf_src6i	0	R/WC1	under_flow_src6in Indicates the state of the SRC6in input buffer. 0: Normal operation 1: An underflow has occurred.

Bit	Bit Name	Initial Value	R/W	Description
5	uf_src5i	0	R/WC1	under_flow_src5in Indicates the state of the SRC5in input buffer. 0: Normal operation 1: An underflow has occurred.
4	uf_src4i	0	R/WC1	under_flow_src4in Indicates the state of the SRC4in input buffer. 0: Normal operation 1: An underflow has occurred.
3	uf_src3i	0	R/WC1	under_flow_src3in Indicates the state of the SRC3in input buffer. 0: Normal operation 1: An underflow has occurred.
2	uf_src2i	0	R/WC1	under_flow_src2in Indicates the state of the SRC2in input buffer. 0: Normal operation 1: An underflow has occurred.
1	uf_src1i	0	R/WC1	under_flow_src1in Indicates the state of the SRC1in input buffer. 0: Normal operation 1: An underflow has occurred.
0	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.

### 34.2.15 SCU\_SYSTEM Interrupt Enable Register 0 (SCU\_SYSTEM\_INT\_ENABLE0)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

[RZ/G1H, M, N]

Function: SCU\_SYSTEM\_INT\_ENABLE0 enables or disables output of interrupts corresponding to the states indicated in the SCU\_SYSTEM status register 0.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	of_cmd1o_ie	of_cmd0o_ie	—	—	of_src9o_ie	of_src8o_ie	of_src7o_ie	of_src6o_ie	of_src5o_ie	of_src4o_ie	of_src3o_ie	of_src2o_ie	of_src1o_ie	of_src0o_ie
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	uf_src9i_ie	uf_src8i_ie	uf_src7i_ie	uf_src6i_ie	uf_src5i_ie	uf_src4i_ie	uf_src3i_ie	uf_src2i_ie	uf_src1i_ie	uf_src0i_ie
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31, 30	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
29	of_cmd1o_ie	0	R/W	over_flow_cmd1out_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
28	of_cmd0o_ie	0	R/W	over_flow_cmd0out_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
27, 26	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
25	of_src9o_ie	0	R/W	over_flow_src9out_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
24	of_src8o_ie	0	R/W	over_flow_src8out_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
23	of_src7o_ie	0	R/W	over_flow_src7out_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
22	of_src6o_ie	0	R/W	over_flow_src6out_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
21	of_src5o_ie	0	R/W	over_flow_src5out_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.

Bit	Bit Name	Initial Value	R/W	Description
20	of_src4o_ie	0	R/W	over_flow_src4out_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
19	of_src3o_ie	0	R/W	over_flow_src3out_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
18	of_src2o_ie	0	R/W	over_flow_src2out_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
17	of_src1o_ie	0	R/W	over_flow_src1out_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
16	of_src0o_ie	0	R/W	over_flow_src0out_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
15 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9	uf_src9i_ie	0	R/W	under_flow_src9in_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
8	uf_src8i_ie	0	R/W	under_flow_src8in_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
7	uf_src7i_ie	0	R/W	under_flow_src7in_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
6	uf_src6i_ie	0	R/W	under_flow_src6in_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
5	uf_src5i_ie	0	R/W	under_flow_src5in_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
4	uf_src4i_ie	0	R/W	under_flow_src4in_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
3	uf_src3i_ie	0	R/W	under_flow_src3in_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
2	uf_src2i_ie	0	R/W	under_flow_src2in_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
1	uf_src1i_ie	0	R/W	under_flow_src1in_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.

Bit	Bit Name	Initial Value	R/W	Description
0	uf_src0i_ie	0	R/W	under_flow_src0in_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.

**[RZ/G1E]**

Function: SCU\_SYSTEM\_INT\_ENABLE0 enables or disables output of interrupts corresponding to the states indicated in the SCU\_SYSTEM status register 0.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	of_cmd1o_ie	of_cmd0o_ie	—	—	—	—	—	of_src6o_ie	of_src5o_ie	of_src4o_ie	of_src3o_ie	of_src2o_ie	of_src1o_ie	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	uf_src6i_ie	uf_src5i_ie	uf_src4i_ie	uf_src3i_ie	f_src2i_ie	uf_src1i_ie	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R

Bit	Bit Name	Initial Value	R/W	Description
31, 30	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
29	of_cmd1o_ie	0	R/W	over_flow_cmd1out_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
28	of_cmd0o_ie	0	R/W	over_flow_cmd0out_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
27 to 23	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
22	of_src6o_ie	0	R/W	over_flow_src6out_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
21	of_src5o_ie	0	R/W	over_flow_src5out_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
20	of_src4o_ie	0	R/W	over_flow_src4out_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
19	of_src3o_ie	0	R/W	over_flow_src3out_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
18	of_src2o_ie	0	R/W	over_flow_src2out_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.

Bit	Bit Name	Initial Value	R/W	Description
17	of_src1o_ie	0	R/W	over_flow_src1out_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
16 to 7	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
6	uf_src6i_ie	0	R/W	under_flow_src6in_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
5	uf_src5i_ie	0	R/W	under_flow_src5in_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
4	uf_src4i_ie	0	R/W	under_flow_src4in_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
3	uf_src3i_ie	0	R/W	under_flow_src3in_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
2	uf_src2i_ie	0	R/W	under_flow_src2in_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
1	uf_src1i_ie	0	R/W	under_flow_src1in_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.



### 34.2.16 SCU\_SYSTEM Status Register 1 (SCU\_SYSTEM\_STATUS1)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

[RZ/G1H, M, N]

Function: SCU\_SYSTEM\_STATUS1 indicates the internal buffer state in synchronous mode. When a register bit is set, the corresponding interrupt signal is output. However, if interrupt outputs are masked by the SYSTEM interrupt enable register 1, interrupt signals are not output.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	uf_src9 0	uf_src8 0	uf_src7 0	uf_src6 0	uf_src5 0	uf_src4 0	uf_src3 0	uf_src2 0	uf_src1 0	uf_src0 0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	of_src9i 0	of_src8i 0	of_src7i 0	of_src6i 0	of_src5i 0	of_src4i 0	of_src3i 0	of_src2i 0	of_src1i 0	of_src0i 0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1

Bit	Bit Name	Initial Value	R/W	Description
31 to 26	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
25	uf_src9o	0	R/WC1	under_flow_src9out Indicates the state of the SRC9out output buffer. 0: Normal operation 1: An underflow has occurred.
24	uf_src8o	0	R/WC1	under_flow_src8out Indicates the state of the SRC8out output buffer. 0: Normal operation 1: An underflow has occurred.
23	uf_src7o	0	R/WC1	under_flow_src7out Indicates the state of the SRC7out output buffer. 0: Normal operation 1: An underflow has occurred.
22	uf_src6o	0	R/WC1	under_flow_src6out Indicates the state of the SRC6out output buffer. 0: Normal operation 1: An underflow has occurred.
21	uf_src5o	0	R/WC1	under_flow_src5out Indicates the state of the SRC5out output buffer. 0: Normal operation 1: An underflow has occurred.
20	uf_src4o	0	R/WC1	under_flow_src4out Indicates the state of the SRC4out output buffer. 0: Normal operation 1: An underflow has occurred.

Bit	Bit Name	Initial Value	R/W	Description
19	uf_src3o	0	R/WC1	under_flow_src3out Indicates the state of the SRC3out output buffer. 0: Normal operation 1: An underflow has occurred.
18	uf_src2o	0	R/WC1	under_flow_src2out Indicates the state of the SRC6out output buffer. 0: Normal operation 1: An underflow has occurred.
17	uf_src1o	0	R/WC1	under_flow_src1out Indicates the state of the SRC7out output buffer. 0: Normal operation 1: An underflow has occurred.
16	uf_src0o	0	R/WC1	under_flow_src0out Indicates the state of the SRC0out output buffer. 0: Normal operation 1: An underflow has occurred.
15 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9	of_src9i	0	R/WC1	over_flow_src9in Indicates the state of the SRC9in input buffer. 0: Normal operation 1: An overflow has occurred.
8	of_src8i	0	R/WC1	over_flow_src8in Indicates the state of the SRC8in input buffer. 0: Normal operation 1: An overflow has occurred.
7	of_src7i	0	R/WC1	over_flow_src7in Indicates the state of the SRC7in input buffer. 0: Normal operation 1: An overflow has occurred.
6	of_src6i	0	R/WC1	over_flow_src6in Indicates the state of the SRC6in input buffer. 0: Normal operation 1: An overflow has occurred.
5	of_src5i	0	R/WC1	over_flow_src5in Indicates the state of the SRC5in input buffer. 0: Normal operation 1: An overflow has occurred.
4	of_src4i	0	R/WC1	over_flow_src4in Indicates the state of the SRC4in input buffer. 0: Normal operation 1: An overflow has occurred.

Bit	Bit Name	Initial Value	R/W	Description
3	of_src3i	0	R/WC1	over_flow_src3in Indicates the state of the SRC3in input buffer. 0: Normal operation 1: An overflow has occurred.
2	of_src2i	0	R/WC1	over_flow_src2in Indicates the state of the SRC2in input buffer. 0: Normal operation 1: An overflow has occurred.
1	of_src1i	0	R/WC1	over_flow_src1in Indicates the state of the SRC1in input buffer. 0: Normal operation 1: An overflow has occurred.
0	of_src0i	0	R/WC1	over_flow_src0in Indicates the state of the SRC0in input buffer. 0: Normal operation 1: An overflow has occurred.

**[RZ/G1E]**

Function: SCU\_SYSTEM\_STATUS1 indicates the internal buffer state in synchronous mode. When a register bit is set, the corresponding interrupt signal is output. However, if interrupt outputs are masked by the SYSTEM interrupt enable register 1, interrupt signals are not output.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	uf_src6 o	uf_src5 o	uf_src4 o	uf_src3 o	uf_src2 o	uf_src1 o	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	of_src6i	of_src5i	of_src4i	of_src3i	of_src2i	of_src1i	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 23	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
22	uf_src6o	0	R/WC1	under_flow_src6out Indicates the state of the SRC6out output buffer. 0: Normal operation 1: An underflow has occurred.
21	uf_src5o	0	R/WC1	under_flow_src5out Indicates the state of the SRC5out output buffer. 0: Normal operation 1: An underflow has occurred.

Bit	Bit Name	Initial Value	R/W	Description
20	uf_src4o	0	R/WC1	under_flow_src4out Indicates the state of the SRC4out output buffer. 0: Normal operation 1: An underflow has occurred.
19	uf_src3o	0	R/WC1	under_flow_src3out Indicates the state of the SRC3out output buffer. 0: Normal operation 1: An underflow has occurred.
18	uf_src2o	0	R/WC1	under_flow_src2out Indicates the state of the SRC6out output buffer. 0: Normal operation 1: An underflow has occurred.
17	uf_src1o	0	R/WC1	under_flow_src1out Indicates the state of the SRC7out output buffer. 0: Normal operation 1: An underflow has occurred.
16 to 7	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
6	of_src6i	0	R/WC1	over_flow_src6in Indicates the state of the SRC6in input buffer. 0: Normal operation 1: An overflow has occurred.
5	of_src5i	0	R/WC1	over_flow_src5in Indicates the state of the SRC5in input buffer. 0: Normal operation 1: An overflow has occurred.
4	of_src4i	0	R/WC1	over_flow_src4in Indicates the state of the SRC4in input buffer. 0: Normal operation 1: An overflow has occurred.
3	of_src3i	0	R/WC1	over_flow_src3in Indicates the state of the SRC3in input buffer. 0: Normal operation 1: An overflow has occurred.
2	of_src2i	0	R/WC1	over_flow_src2in Indicates the state of the SRC2in input buffer. 0: Normal operation 1: An overflow has occurred.
1	of_src1i	0	R/WC1	over_flow_src1in Indicates the state of the SRC1in input buffer. 0: Normal operation 1: An overflow has occurred.
0	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.

### 34.2.17 SCU\_SYSTEM Interrupt Enable Register 1 (SCU\_SYSTEM\_INT\_ENABLE1)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

[RZ/G1H, M, N]

Function: SCU\_SYSTEM\_INT\_ENABLE1 enables or disables output of interrupts corresponding to the states indicated in the SCU\_SYSTEM status register 1.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	uf_src9_o_ie	uf_src8_o_ie	uf_src7_o_ie	uf_src6_o_ie	uf_src5_o_ie	uf_src4_o_ie	uf_src3_o_ie	uf_src2_o_ie	uf_src1_o_ie	uf_src0_o_ie
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	of_src9i_ie	of_src8i_ie	of_src7i_ie	of_src6i_ie	of_src5i_ie	of_src4i_ie	of_src3i_ie	of_src2i_ie	of_src1i_ie	of_src0i_ie
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 26	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
25	uf_src9o_ie	0	R/W	under_flow_src9out_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
24	uf_src8o_ie	0	R/W	under_flow_src8out_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
23	uf_src7o_ie	0	R/W	under_flow_src7out_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
22	uf_src6o_ie	0	R/W	under_flow_src6out_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
21	uf_src5o_ie	0	R/W	under_flow_src5out_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
20	uf_src4o_ie	0	R/W	under_flow_src4out_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
19	uf_src3o_ie	0	R/W	under_flow_src3out_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
18	uf_src2o_ie	0	R/W	under_flow_src2out_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.

Bit	Bit Name	Initial Value	R/W	Description
17	uf_src1o_ie	0	R/W	under_flow_src1out_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
16	uf_src0o_ie	0	R/W	under_flow_src0out_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
15 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9	of_src9i_ie	0	R/W	over_flow_src9in_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
8	of_src8i_ie	0	R/W	over_flow_src8in_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
7	of_src7i_ie	0	R/W	over_flow_src7in_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
6	of_src6i_ie	0	R/W	over_flow_src6in_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
5	of_src5i_ie	0	R/W	over_flow_src5in_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
4	of_src4i_ie	0	R/W	over_flow_src4in_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
3	of_src3i_ie	0	R/W	over_flow_src3in_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
2	of_src2i_ie	0	R/W	over_flow_src2in_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
1	of_src1i_ie	0	R/W	over_flow_src1in_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
0	of_src0i_ie	0	R/W	over_flow_src0in_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.

**[RZ/G1E]**

Function: SCU\_SYSTEM\_INT\_ENABLE1 enables or disables output of interrupts corresponding to the states indicated in the SCU\_SYSTEM status register 1.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	uf_src6_o_ie	uf_src5_o_ie	uf_src4_o_ie	uf_src3_o_ie	uf_src2_o_ie	uf_src1_o_ie	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	of_src6i_ie	of_src5i_ie	of_src4i_ie	of_src3i_ie	of_src2i_ie	of_src1i_ie	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 23	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
22	uf_src6o_ie	0	R/W	under_flow_src6out_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
21	uf_src5o_ie	0	R/W	under_flow_src5out_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
20	uf_src4o_ie	0	R/W	under_flow_src4out_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
19	uf_src3o_ie	0	R/W	under_flow_src3out_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
18	uf_src2o_ie	0	R/W	under_flow_src2out_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
17	uf_src1o_ie	0	R/W	under_flow_src1out_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
16 to 7	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
6	of_src6i_ie	0	R/W	over_flow_src6in_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
5	of_src5i_ie	0	R/W	over_flow_src5in_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
4	of_src4i_ie	0	R/W	over_flow_src4in_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.

Bit	Bit Name	Initial Value	R/W	Description
3	of_src3i_ie	0	R/W	over_flow_src3in_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
2	of_src2i_ie	0	R/W	over_flow_src2in_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
1	of_src1i_ie	0	R/W	over_flow_src1in_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
0	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.



**34.2.18 SRCm Software Reset Register (SRCm\_SWRSR)**

Note: RZ/G1H, M and N: m = 0 to 9, RZ/G1E: m = 1 to 6

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: SRCm\_SWRSR is a 32-bit readable/writable register that controls operation/reset of the SRC internal circuits.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SWRST
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	SWRST	1	R/W	Software Reset While this bit is 0, the SRC internal circuits are put in the reset state. SRCm_* registers except this register are reset. Therefore, they should be set again after the reset is canceled. 0: Resets the SRC 1: SRC enters the operating state

**34.2.19 SRCm SRC Initialization Register (SRCm\_SRCIR)**

Note: RZ/G1H, M and N: m = 0 to 9, RZ/G1E: m = 1 to 6

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: SRCm\_SRCIR is a 32-bit readable/writable register that initializes the operation of the SRC internal circuits.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	INIT
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

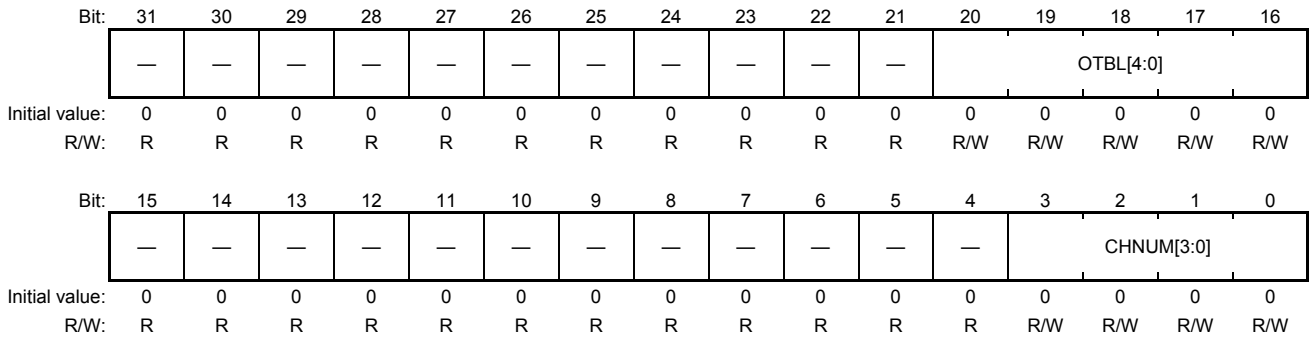
Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	INIT	1	R/W	Initialization of Processing When this bit is set to 1, the SRC processing is initialized. This bit should be cleared to 0 after it was set to 1. 0: Processing State 1: Initialization (sets the initial setting of other registers)

**34.2.20 SRCm Audio Information Register (SRCm\_ADINR)**

Note: RZ/G1H, M and N: m = 0 to 9, RZ/G1E: m = 1 to 6

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: SRCm\_ADINR is a 32-bit readable/writable register that selects channel number and bit length of output audio data.



Bit	Bit Name	Initial Value	R/W	Description
31 to 21	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
20 to 16	OTBL[4:0]	00000	R/W	Bit Length of Output Audio Data. These bits set the bit length of output audio data. 00000: 24 bits 00001: Reserved 00010: 22 bits 00011: Reserved 00100: 20 bits 00101: Reserved 00110: 18 bits 00111: Reserved 01000: 16 bits 01001 to 01111: Reserved 10000: 8 bits 10001 to 11111: Reversed
15 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
3 to 0	CHNUM[3:0]	0000	R/W	<p>Channel Number (For m = 0, 1, 3, or 4 / (m = 1, 3, or 4)*)</p> <p>These bits set the channel number.</p> <p>0000: 0 (None)</p> <p>0001: 1 channel</p> <p>0010: 2 channels</p> <p>0011: Reserved</p> <p>0100: 4 channels</p> <p>0101: Reserved</p> <p>0110: 6 channels</p> <p>0111: Reserved</p> <p>1000: 8 channels</p> <p>1001 to 1111: Reserved</p> <p>Channel Number (For m = 2, 5 to 9 / (m = 2, 5, or 6)*)</p> <p>These bits set the channel number.</p> <p>0000: 0 (None)</p> <p>0001: 1 channel</p> <p>0010: 2 channels</p> <p>0011 to 1111: Reserved</p> <p>Note: * Applicable to the RZ/G1E.</p>

### 34.2.21 SRCm IFS Control Register (SRCm\_IFSCR)

Note: RZ/G1H, M and N: m = 0 to 9, RZ/G1E: m = 1 to 6

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: SRCm\_IFSCR is a 32-bit readable/writable register that controls INTIFS value.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	INTIFS EN
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	INTIFSEN	0	R/W	INTIFS Value Setting Enable This bit controls the INTIFS bit of SRCm_IFSVR register. This bit is effective only in asynchronous SRC Mode (bit SRCMD in SRCm_SRCCR register is 0) 0: Disables INTIFS bit of SRCm_IFSVR register 1: Enables INTIFS bit of SRCm_IFSVR register Basically, this bit should be set to 1.

### 34.2.22 SRCm IFS Value Setting Register (SRCm\_IFSVR)

Note: RZ/G1H, M and N: m = 0 to 9, RZ/G1E: m = 1 to 6

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

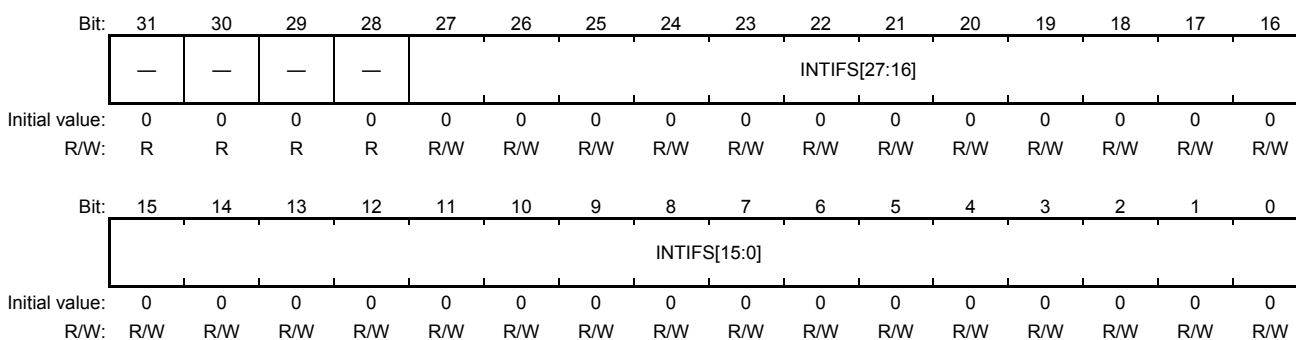
Function: SRCm\_IFSVR is a 32-bit readable/writable register that sets the value of INTIFS. The INTIFS is the initial value of FSI of sampling rate conversion function. SRC detects input sampling rate and output sampling rate automatically. By doing this, it calculates the FSI value so that the below formula is satisfied.

$$F_{in}/F_{out} \approx FSI/FSO$$

The INTIFS value is used for the initial value of FSI. If this setting is disabled (INTIFSEN bit of SRCm\_IFSCR register is 0), SRC will use FSO for initial value of FSI.

$$INTIFS = F_{in} \times FSO/F_{out}$$

- Note:  $F_{in}$ : Input sampling frequency  
 $F_{out}$ : Output sampling frequency  
 FSI: Input sampling rate  
 FSO: Output sampling rate (Fixed value:  $2^{22} = H'040\ 0000$ )



Bit	Bit Name	Initial Value	R/W	Description
31 to 28	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
27 to 0	INTIFS[27:0]	H'000 0000	R/W	Initial Value of FSI These bits set initial value of FSI. These bits should be set the ratio of input and output sampling-rate within the range of the restriction decided from channel number. Example: $F_{in} = 32\text{ kHz}$ $F_{out} = 44.1\text{ kHz}$ $FSI = 2^{22} \times 32000 / 44100 = 3043485 = H'02E709D$ For the setting value examples, see Table 34.8.

Note: When SRCm is used in synchronous mode (SRCMD bit in SRCm\_SRCCR register is 1), INTIFS can change without SRC initialization. On the operating state, INTIFS can change within 1%. However, the change of the SRC conversion rate means that it will set jitter by manual operation. Please evaluate sound quality, and use this function as far as you judged sound quality is no problem. If on the occasion of the change more than 1%, it should do SRC initialization (cf. section 34.3.5 (1) (d)) after changing INTIFS.

### 34.2.23 SRCm SRC Control Register (SRCm\_SRCCR)

Note: RZ/G1H, M and N: m = 0 to 9, RZ/G1E: m = 1 to 6

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: SRCm\_SRCCR is a 32-bit readable/writable register that controls the operation of sampling rate converter.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SRCM D
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R	R	R	R/W	R	R	R	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 17	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
16	—	0	R/W	This bit should be set to 1.
15 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12	—	0	R/W	This bit should be set to 1.
11 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	—	0	R/W	This bit should be set to 1.
7 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	—	0	R/W	This bit should be set to 1.
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	SRCMD	0	R/W	Select SRC Mode 0: Asynchronous SRC 1: Synchronous SRC

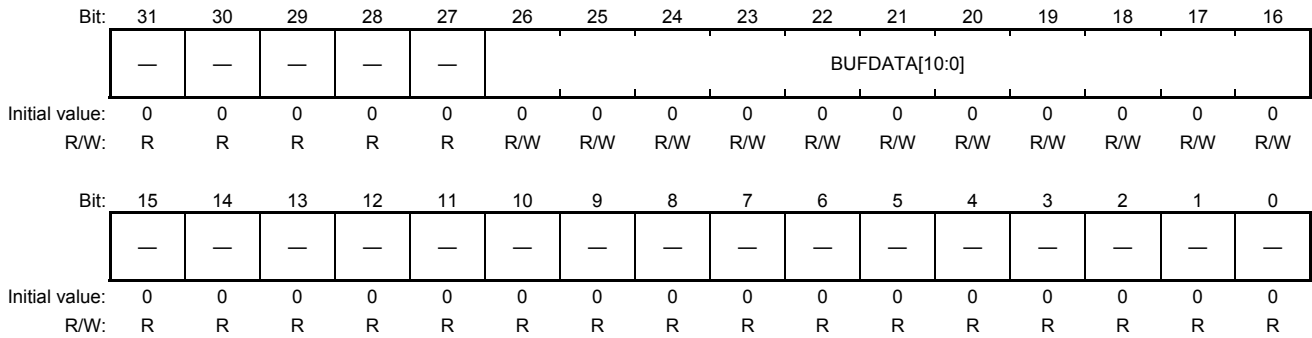
Note: Set sync\_in or sync\_out bit in SRCm\_MODE register, when SRCm is used in synchronous mode by setting SRCMD=1.

**34.2.24 SRCm Buffer Size DATA RAM Setting Register (SRCm\_BSDSR)**

Note: RZ/G1H, M and N: m = 0 to 4, 9, RZ/G1E: m = 1 to 4

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: SRCm\_BSDSR is a 32-bit readable/writable register that controls the buffer size of DATA RAM. This register should set with SRCm\_BSISR register. See Table 34.7 for the combination of settings.



Bit	Bit Name	Initial Value	R/W	Description														
31 to 27	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.														
26 to 16	BUFDATA [10:0]	All 0	R/W	These bits should be set appropriately according to the following table. Refer to Table 34.7 for the combination of FSO/FSI ratio, channel number, and latency.														
				<table border="1"> <thead> <tr> <th>FSO/FSI Ratio</th> <th>Value</th> </tr> </thead> <tbody> <tr> <td>6 - 1/6</td> <td>H'180</td> </tr> <tr> <td>6 - 1/4</td> <td>H'100</td> </tr> <tr> <td>6 - 1/3</td> <td>H'0C0</td> </tr> <tr> <td>6 - 1/2</td> <td>H'080</td> </tr> <tr> <td>6 - 2/3</td> <td>H'060</td> </tr> <tr> <td>6 - 1</td> <td>H'040</td> </tr> </tbody> </table>	FSO/FSI Ratio	Value	6 - 1/6	H'180	6 - 1/4	H'100	6 - 1/3	H'0C0	6 - 1/2	H'080	6 - 2/3	H'060	6 - 1	H'040
FSO/FSI Ratio	Value																	
6 - 1/6	H'180																	
6 - 1/4	H'100																	
6 - 1/3	H'0C0																	
6 - 1/2	H'080																	
6 - 2/3	H'060																	
6 - 1	H'040																	
15 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.														

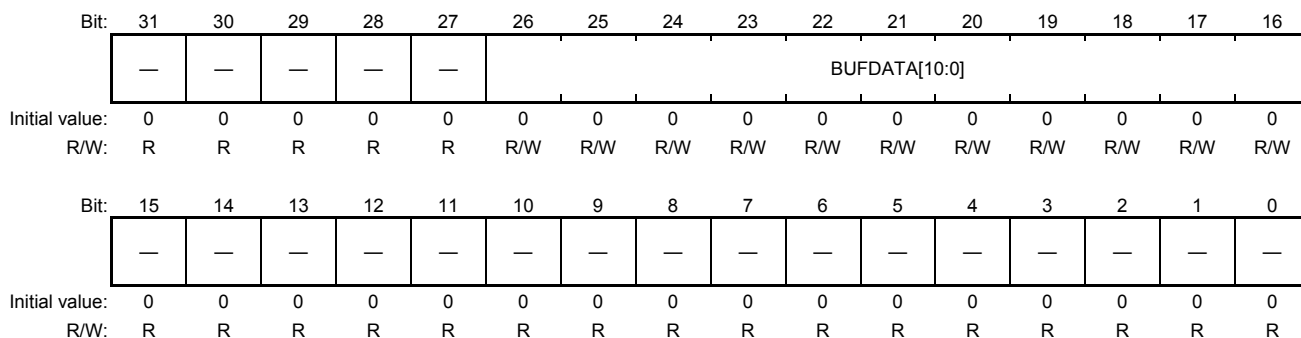


### 34.2.25 SRCn Buffer Size DATA RAM Setting Register (SRCn\_BSISR)

Note: RZ/G1H, M and N: n = 5 to 8, RZ/G1E: n = 5 or 6

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: SRCn\_BSISR is a 32-bit readable/writable register that controls the buffer size of DATA RAM. This register should set with SRCm\_BSISR register. See Table 34.7 for the combination of settings.



Bit	Bit Name	Initial Value	R/W	Description														
31 to 27	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.														
26 to 16	BUFDATA [10:0]	All 0	R/W	These bits should be set appropriately according to the following table. Refer to Table 34.7 for the combination of FSO/FSI ratio, channel number, and latency.														
				<table border="1"> <thead> <tr> <th>FSO/FSI Ratio</th> <th>Value</th> </tr> </thead> <tbody> <tr> <td>6 - 1/6</td> <td>H'240</td> </tr> <tr> <td>6 - 1/4</td> <td>H'180</td> </tr> <tr> <td>6 - 1/3</td> <td>H'120</td> </tr> <tr> <td>6 - 1/2</td> <td>H'0C0</td> </tr> <tr> <td>6 - 2/3</td> <td>H'090</td> </tr> <tr> <td>6 - 1</td> <td>H'060</td> </tr> </tbody> </table>	FSO/FSI Ratio	Value	6 - 1/6	H'240	6 - 1/4	H'180	6 - 1/3	H'120	6 - 1/2	H'0C0	6 - 2/3	H'090	6 - 1	H'060
FSO/FSI Ratio	Value																	
6 - 1/6	H'240																	
6 - 1/4	H'180																	
6 - 1/3	H'120																	
6 - 1/2	H'0C0																	
6 - 2/3	H'090																	
6 - 1	H'060																	
15 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.														

### 34.2.26 SRCm Buffer Size IJEC RAM Setting Register (SRCm\_BSISR)

Note: RZ/G1H, M and N: m = 0 to 9, RZ/G1E: m = 1 to 6

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: SRCm\_BSISR is a 32-bit readable/writable register that controls the precision value and buffer size of IJEC RAM. This register should set with SRCm\_BSDSR/SRCn\_BSDSR register. See Table 34.7 for the combination of settings.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
	—	—	—	—	—	—	—	—	—	—	IJEPREC[5:0]						
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	—	—	—	—	—	—	—	IJECSIZE[8:0]									
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
R/W:	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Bit	Bit Name	Initial Value	R/W	Description
31 to 22	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
21 to 16	IJEPREC[5:0]	All 0	R/W	These bits should be set to H'10.
15 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8 to 0	IJECSIZE[8:0]	All 0	R/W	These bits should be set appropriately according to the following table.

Refer to Table 34.7 for the combination of FSO/FSI ratio, channel number, and latency.

FSO/FSI Ratio	Value
6 - 1/6	H'60
6 - 1/4	H'40
6 - 1/3	H'30
6 - 1/2	H'20
6 - 2/3	H'20
6 - 1	H'20

**34.2.27 CTUn Software Reset Register (CTUn\_SWRSR)**

Note: n = 00, 01, 02, 03, 10, 11, 12, or 13

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: CTUn\_SWRSR is a 32-bit readable/writable register that controls operation/reset of the CTU internal circuits.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SWRST
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	SWRST	1	R/W	Software Reset While this bit is 0, the CTU internal circuits are put in the reset state. CTUn_* registers except this register are reset. Therefore, they should be set again after the reset is canceled. 0: Resets the CTU 1: Operating state

**34.2.28 CTUn CTU Initialization Register (CTUn\_CTUIR)**

Note: n = 00, 01, 02, 03, 10, 11, 12, or 13

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: CTUn\_CTUIR is a 32-bit readable/writable register that initializes the operation of the CTU internal circuits.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	INIT
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	INIT	1	R/W	Initialization of Processing When this bit is set to 1, the CTU processing is initialized. This bit should be cleared to 0 after it was set to 1. 0: Processing State 1: Initialization (sets the initial setting of other registers)

**34.2.29 CTUn Audio Information Register (CTUn\_ADINR)**

Note: n = 00, 01, 02, 03, 10, 11, 12, or 13

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: CTUn\_ADINR is a 32-bit readable/writable register that selects channel number.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	CHNUM[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

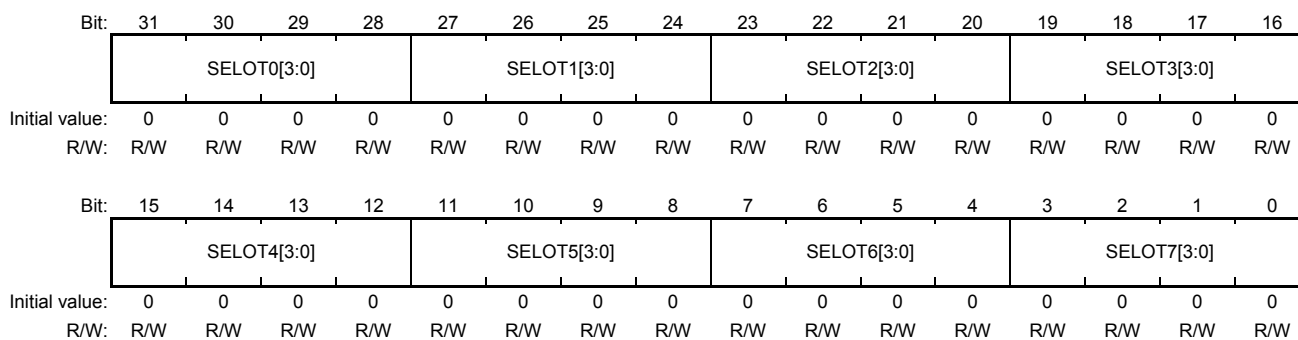
Bit	Bit Name	Initial Value	R/W	Description
31 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3 to 0	CHNUM[3:0]	0000	R/W	Channel Number These bits set the channel number 0000: 0 (None) 0001: 1 channel 0010: 2 channels 0011: Reserved 0100: 4 channels 0101: Reserved 0110: 6 channels 0111: Reserved 1000: 8 channels 1001 to 1111: Reserved

### 34.2.30 CTUn CTU Pass Mode Register (CTUn\_CPMDR)

Note: n = 00, 01, 02, 03, 10, 11, 12, or 13

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: CTUn\_CPMDR is a 32-bit readable/writable register that controls the pass of channel data for each output.



Bit	Bit Name	Initial Value	R/W	Description
31 to 28	SELOT0[3:0]	0000	R/W	Select output data for channel 0 These bits select the output data for channel 0. 0000: Connect input data of channel 0 0001: Connect input data of channel 0 0010: Connect input data of channel 1 0011: Connect input data of channel 2 0100: Connect input data of channel 3 0101: Connect input data of channel 4 0110: Connect input data of channel 5 0111: Connect input data of channel 6 1000: Connect input data of channel 7 1001: Connect calculated data by scale values of matrix row 0 1010: Connect calculated data by scale values of matrix row 1 1011: Connect calculated data by scale values of matrix row 2 1100: Connect calculated data by scale values of matrix row 3

Bit	Bit Name	Initial Value	R/W	Description
27 to 24	SELOT1[3:0]	0000	R/W	<p>Select output data for channel 1</p> <p>These bits select the output data for channel 1.</p> <p>0000: Connect input data of channel 1</p> <p>0001: Connect input data of channel 0</p> <p>0010: Connect input data of channel 1</p> <p>0011: Connect input data of channel 2</p> <p>0100: Connect input data of channel 3</p> <p>0101: Connect input data of channel 4</p> <p>0110: Connect input data of channel 5</p> <p>0111: Connect input data of channel 6</p> <p>1000: Connect input data of channel 7</p> <p>1001: Connect calculated data by scale values of matrix row 0</p> <p>1010: Connect calculated data by scale values of matrix row 1</p> <p>1011: Connect calculated data by scale values of matrix row 2</p> <p>1100: Connect calculated data by scale values of matrix row 3</p>
23 to 20	SELOT2[3:0]	0000	R/W	<p>Select output data for channel 2</p> <p>These bits select the output data for channel 2.</p> <p>0000: Connect input data of channel 2</p> <p>0001: Connect input data of channel 0</p> <p>0010: Connect input data of channel 1</p> <p>0011: Connect input data of channel 2</p> <p>0100: Connect input data of channel 3</p> <p>0101: Connect input data of channel 4</p> <p>0110: Connect input data of channel 5</p> <p>0111: Connect input data of channel 6</p> <p>1000: Connect input data of channel 7</p> <p>1001: Connect calculated data by scale values of matrix row 0</p> <p>1010: Connect calculated data by scale values of matrix row 1</p> <p>1011: Connect calculated data by scale values of matrix row 2</p> <p>1100: Connect calculated data by scale values of matrix row 3</p>

Bit	Bit Name	Initial Value	R/W	Description
19 to 16	SELOT3[3:0]	0000	R/W	<p>Select output data for channel 3</p> <p>These bits select the output data for channel 3.</p> <p>0000: Connect input data of channel 3</p> <p>0001: Connect input data of channel 0</p> <p>0010: Connect input data of channel 1</p> <p>0011: Connect input data of channel 2</p> <p>0100: Connect input data of channel 3</p> <p>0101: Connect input data of channel 4</p> <p>0110: Connect input data of channel 5</p> <p>0111: Connect input data of channel 6</p> <p>1000: Connect input data of channel 7</p> <p>1001: Connect calculated data by scale values of matrix row 0</p> <p>1010: Connect calculated data by scale values of matrix row 1</p> <p>1011: Connect calculated data by scale values of matrix row 2</p> <p>1100: Connect calculated data by scale values of matrix row 3</p>
15 to 12	SELOT4[3:0]	0000	R/W	<p>Select output data for channel 4</p> <p>These bits select the output data for channel 4.</p> <p>0000: Connect input data of channel 4</p> <p>0001: Connect input data of channel 0</p> <p>0010: Connect input data of channel 1</p> <p>0011: Connect input data of channel 2</p> <p>0100: Connect input data of channel 3</p> <p>0101: Connect input data of channel 4</p> <p>0110: Connect input data of channel 5</p> <p>0111: Connect input data of channel 6</p> <p>1000: Connect input data of channel 7</p> <p>1001: Connect calculated data by scale values of matrix row 0</p> <p>1010: Connect calculated data by scale values of matrix row 1</p> <p>1011: Connect calculated data by scale values of matrix row 2</p> <p>1100: Connect calculated data by scale values of matrix row 3</p>



Bit	Bit Name	Initial Value	R/W	Description
11 to 8	SELOT5[3:0]	0000	R/W	<p>Select output data for channel 5</p> <p>These bits select the output data for channel 5.</p> <p>0000: Connect input data of channel 5</p> <p>0001: Connect input data of channel 0</p> <p>0010: Connect input data of channel 1</p> <p>0011: Connect input data of channel 2</p> <p>0100: Connect input data of channel 3</p> <p>0101: Connect input data of channel 4</p> <p>0110: Connect input data of channel 5</p> <p>0111: Connect input data of channel 6</p> <p>1000: Connect input data of channel 7</p> <p>1001: Connect calculated data by scale values of matrix row 0</p> <p>1010: Connect calculated data by scale values of matrix row 1</p> <p>1011: Connect calculated data by scale values of matrix row 2</p> <p>1100: Connect calculated data by scale values of matrix row 3</p>
7 to 4	SELOT6[3:0]	0000	R/W	<p>Select output data for channel 6</p> <p>These bits select the output data for channel 6.</p> <p>0000: Connect input data of channel 6</p> <p>0001: Connect input data of channel 0</p> <p>0010: Connect input data of channel 1</p> <p>0011: Connect input data of channel 2</p> <p>0100: Connect input data of channel 3</p> <p>0101: Connect input data of channel 4</p> <p>0110: Connect input data of channel 5</p> <p>0111: Connect input data of channel 6</p> <p>1000: Connect input data of channel 7</p> <p>1001: Connect calculated data by scale values of matrix row 0</p> <p>1010: Connect calculated data by scale values of matrix row 1</p> <p>1011: Connect calculated data by scale values of matrix row 2</p> <p>1100: Connect calculated data by scale values of matrix row 3</p>

Bit	Bit Name	Initial Value	R/W	Description
3 to 0	SELOT7[3:0]	0000	R/W	Select output data for channel 7 These bits select the output data for channel 7. 0000: Connect input data of channel 7 0001: Connect input data of channel 0 0010: Connect input data of channel 1 0011: Connect input data of channel 2 0100: Connect input data of channel 3 0101: Connect input data of channel 4 0110: Connect input data of channel 5 0111: Connect input data of channel 6 1000: Connect input data of channel 7 1001: Connect calculated data by scale values of matrix row 0 1010: Connect calculated data by scale values of matrix row 1 1011: Connect calculated data by scale values of matrix row 2 1100: Connect calculated data by scale values of matrix row 3

**34.2.31 CTUn Scale Mode Register (CTUn\_SCMDR)**

Note: n = 00, 01, 02, 03, 10, 11, 12, or 13

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: CTUn\_SCMDR is a 32-bit readable/writable register that selects the number of rows calculated by matrix.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	SCMD[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W

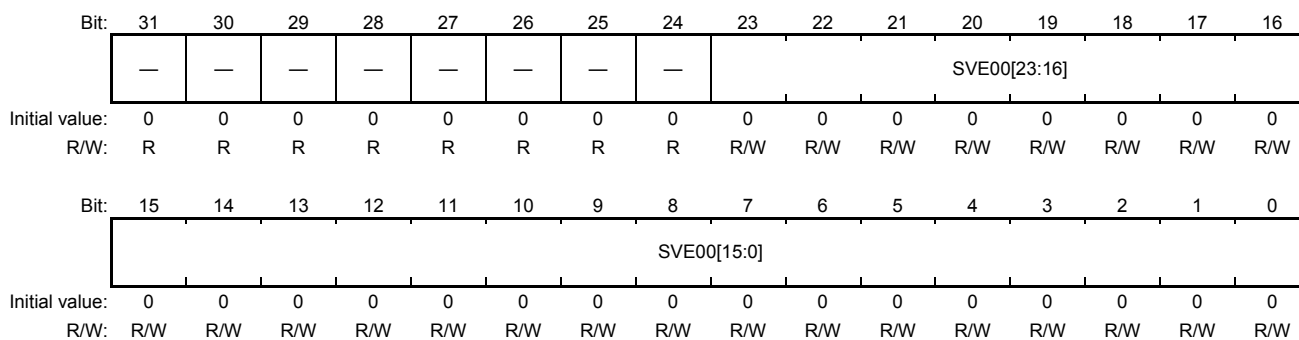
Bit	Bit Name	Initial Value	R/W	Description
31 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2 to 0	SCMD[2:0]	000	R/W	The number of rows calculated by matrix These bits select the number of rows calculated by matrix by the scale values. 000: No operation 001: Calculate matrix row 0 by scale values. 010: Calculate matrix row 0 and 1 by scale values. 011: Calculate matrix row 0 and 1 and 2 by scale values. 100: Calculate matrix row 0 and 1 and 2 and 3 by scale values.

### 34.2.32 CTUn Scale Value e00 Register (CTUn\_SV00R)

Note: n = 00, 01, 02, 03, 10, 11, 12, or 13

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: CTUn\_SV00R is a 32-bit readable/writable register that sets the scale value for channel 0 of matrix row 0.



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	SVE00[23:0]	H'00_0000	R/W	Scale Value e00 for Input Channel 0 of Matrix Row 0 These bits set the scale value for input data of channel 0 of matrix row 0. SVE00[23]: Sign bit SVE00[22]: Integer bit SVE00[21:0]: Decimal bits

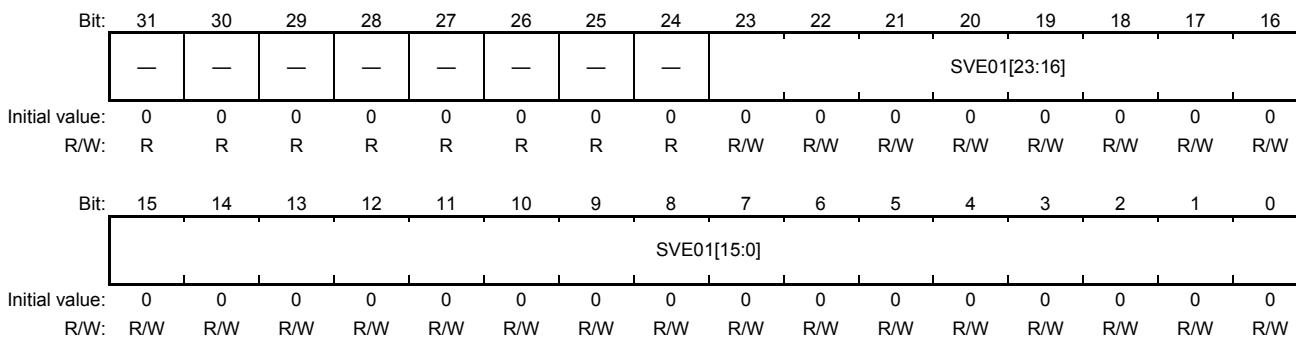
plus			minus		
Value	[time]	[dB]	Value	[time]	[dB]
H'7F_FFFF	2	6	H'80_0000	2	6
.....	.....	.....	.....	.....	.....
H'40_0000	1	0	H'C0_0000	1	0
.....	.....	.....	.....	.....	.....
H'00_0001	$2.38 \times 10^{-7}$	-132	.....	.....	.....
H'00_0000	0 (Mute)	$-\infty$	H'FF_FFFF	$2.38 \times 10^{-7}$	-132

### 34.2.33 CTUn Scale Value e01 Register (CTUn\_SV01R)

Note: n = 00, 01, 02, 03, 10, 11, 12, or 13

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: CTUn\_SV01R is a 32-bit readable/writable register that sets the scale value for channel 1 of matrix row 0.



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	SVE01[23:0]	H'00 0000	R/W	Scale Value e01 for Input Channel 1 of Matrix Row 0 These bits set the scale value for input data of channel 1 of matrix row 0. SVE01[23]: Sign bit SVE01[22]: Integer bit SVE01[21:0]: Decimal bits

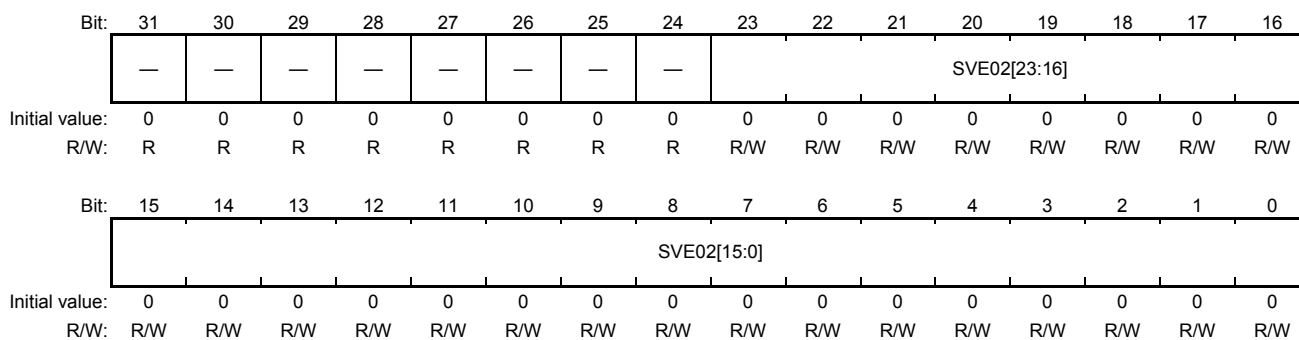
plus			minus		
Value	[time]	[dB]	Value	[time]	[dB]
H'7F_FFFF	2	6	H'80_0000	2	6
.....	.....	.....	.....	.....	.....
H'40_0000	1	0	H'C0_0000	1	0
.....	.....	.....	.....	.....	.....
H'00_0001	$2.38 \times 10^{-7}$	-132	.....	.....	.....
H'00_0000	0 (Mute)	$-\infty$	H'FF_FFFF	$2.38 \times 10^{-7}$	-132

### 34.2.34 CTUn Scale Value e02 Register (CTUn\_SV02R)

Note: n = 00, 01, 02, 03, 10, 11, 12, or 13

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: CTUn\_SV02R is a 32-bit readable/writable register that sets the scale value for channel 2 of matrix row 0.



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	SVE02[23:0]	H'00_0000	R/W	Scale Value e02 for Input Channel 2 of Matrix Row 0 These bits set the scale value for input data of channel 2 of matrix row 0. SVE02[23]: Sign bit SVE02[22]: Integer bit SVE02[21:0]: Decimal bits

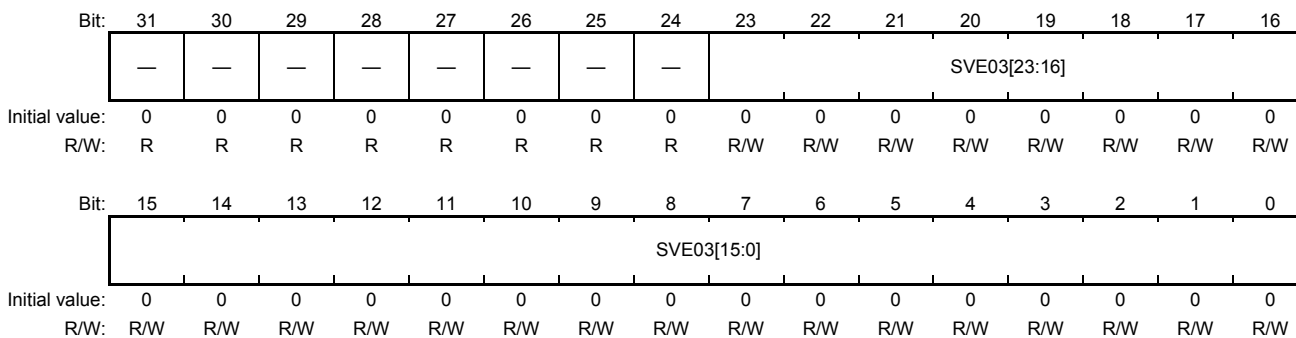
plus			minus		
Value	[time]	[dB]	Value	[time]	[dB]
H'7F_FFFF	2	6	H'80_0000	2	6
.....	.....	.....	.....	.....	.....
H'40_0000	1	0	H'C0_0000	1	0
.....	.....	.....	.....	.....	.....
H'00_0001	$2.38 \times 10^{-7}$	-132	.....	.....	.....
H'00_0000	0 (Mute)	$-\infty$	H'FF_FFFF	$2.38 \times 10^{-7}$	-132

### 34.2.35 CTUn Scale Value e03 Register (CTUn\_SV03R)

Note: n = 00, 01, 02, 03, 10, 11, 12, or 13

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: CTUn\_SV03R is a 32-bit readable/writable register that sets the scale value for channel 3 of matrix row 0.



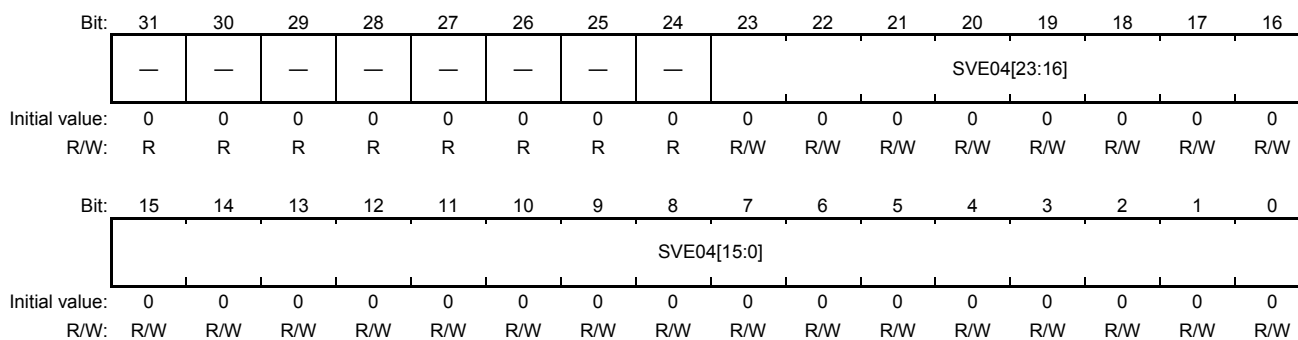
Bit	Bit Name	Initial Value	R/W	Description																																																
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.																																																
23 to 0	SVE03[23:0]	H'00 0000	R/W	Scale Value e03 for Input Channel 3 of Matrix Row 0 These bits set the scale value for input data of channel 3 of matrix row 0. SVE03[23]: Sign bit SVE03[22]: Integer bit SVE03[21:0]: Decimal bits																																																
		<table border="1"> <thead> <tr> <th colspan="3">plus</th> <th colspan="3">minus</th> </tr> <tr> <th>Value</th> <th>[time]</th> <th>[dB]</th> <th>Value</th> <th>[time]</th> <th>[dB]</th> </tr> </thead> <tbody> <tr> <td>H'7F_FFFF</td> <td>2</td> <td>6</td> <td>H'80_0000</td> <td>2</td> <td>6</td> </tr> <tr> <td>.....</td> <td>.....</td> <td>.....</td> <td>.....</td> <td>.....</td> <td>.....</td> </tr> <tr> <td>H'40_0000</td> <td>1</td> <td>0</td> <td>H'C0_0000</td> <td>1</td> <td>0</td> </tr> <tr> <td>.....</td> <td>.....</td> <td>.....</td> <td>.....</td> <td>.....</td> <td>.....</td> </tr> <tr> <td>H'00_0001</td> <td><math>2.38 \times 10^{-7}</math></td> <td>-132</td> <td>.....</td> <td>.....</td> <td>.....</td> </tr> <tr> <td>H'00_0000</td> <td>0 (Mute)</td> <td><math>-\infty</math></td> <td>H'FF_FFFF</td> <td><math>2.38 \times 10^{-7}</math></td> <td>-132</td> </tr> </tbody> </table>			plus			minus			Value	[time]	[dB]	Value	[time]	[dB]	H'7F_FFFF	2	6	H'80_0000	2	6	.....	.....	.....	.....	.....	.....	H'40_0000	1	0	H'C0_0000	1	0	.....	.....	.....	.....	.....	.....	H'00_0001	$2.38 \times 10^{-7}$	-132	.....	.....	.....	H'00_0000	0 (Mute)	$-\infty$	H'FF_FFFF	$2.38 \times 10^{-7}$	-132
plus			minus																																																	
Value	[time]	[dB]	Value	[time]	[dB]																																															
H'7F_FFFF	2	6	H'80_0000	2	6																																															
.....	.....	.....	.....	.....	.....																																															
H'40_0000	1	0	H'C0_0000	1	0																																															
.....	.....	.....	.....	.....	.....																																															
H'00_0001	$2.38 \times 10^{-7}$	-132	.....	.....	.....																																															
H'00_0000	0 (Mute)	$-\infty$	H'FF_FFFF	$2.38 \times 10^{-7}$	-132																																															

### 34.2.36 CTUn Scale Value e04 Register (CTUn\_SV04R)

Note: n = 00, 01, 02, 03, 10, 11, 12, or 13

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: CTUn\_SV04R is a 32-bit readable/writable register that sets the scale value for channel 4 of matrix row 0.



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	SVE04[23:0]	H'00 0000	R/W	Scale Value e04 for Input Channel 4 of Matrix Row 0 These bits set the scale value for input data of channel 4 of matrix row 0. SVE04[23]: Sign bit SVE04[22]: Integer bit SVE04[21:0]: Decimal bits

plus			minus		
Value	[time]	[dB]	Value	[time]	[dB]
H'7F_FFFF	2	6	H'80_0000	2	6
.....	.....	.....	.....	.....	.....
H'40_0000	1	0	H'C0_0000	1	0
.....	.....	.....	.....	.....	.....
H'00_0001	$2.38 \times 10^{-7}$	-132	.....	.....	.....
H'00_0000	0 (Mute)	$-\infty$	H'FF_FFFF	$2.38 \times 10^{-7}$	-132

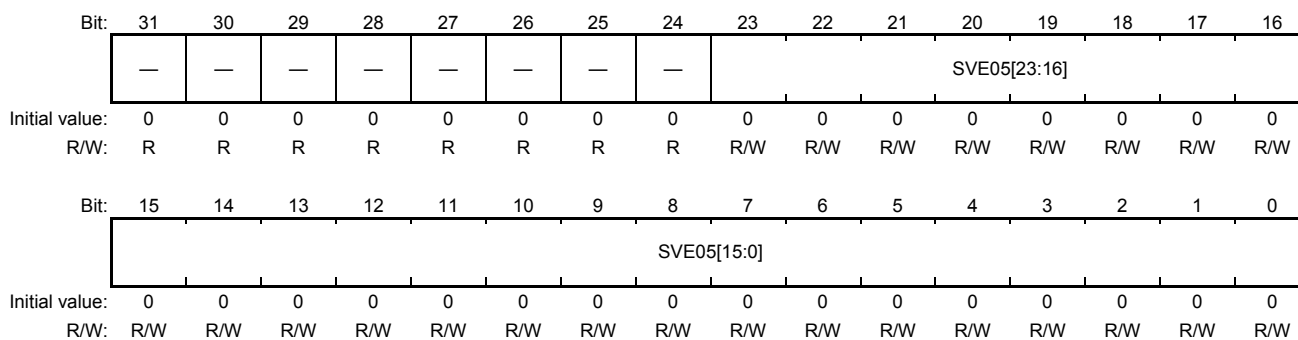


### 34.2.37 CTUn Scale Value e05 Register (CTUn\_SV05R)

Note: n = 00, 01, 02, 03, 10, 11, 12, or 13

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: CTUn\_SV05R is a 32-bit readable/writable register that sets the scale value for channel 5 of matrix row 0.



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	SVE05[23:0]	H'00 0000	R/W	Scale Value e05 for Input Channel 5 of Matrix Row 0 These bits set the scale value for input data of channel 5 of matrix row 0. SVE05[23]: Sign bit SVE05[22]: Integer bit SVE05[21:0]: Decimal bits

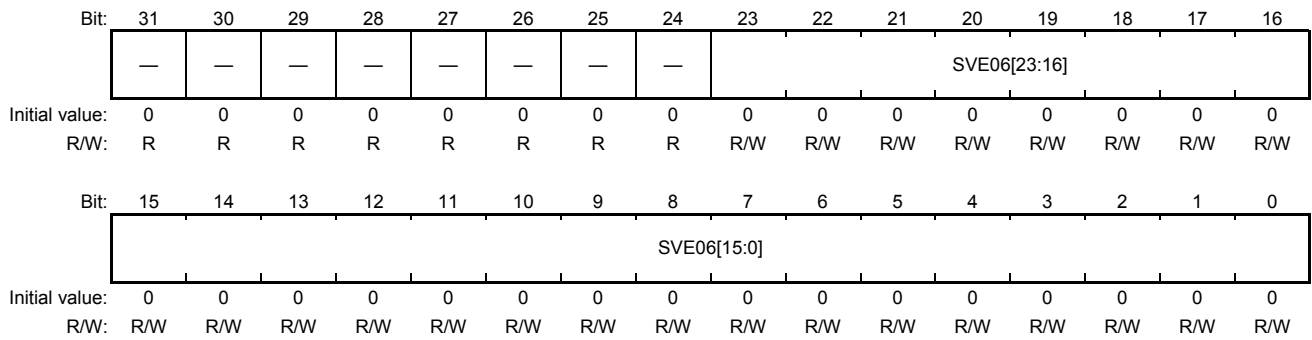
plus			minus		
Value	[time]	[dB]	Value	[time]	[dB]
H'7F_FFFF	2	6	H'80_0000	2	6
.....	.....	.....	.....	.....	.....
H'40_0000	1	0	H'C0_0000	1	0
.....	.....	.....	.....	.....	.....
H'00_0001	$2.38 \times 10^{-7}$	-132	.....	.....	.....
H'00_0000	0 (Mute)	$-\infty$	H'FF_FFFF	$2.38 \times 10^{-7}$	-132

**34.2.38 CTUn Scale Value e06 Register (CTUn\_SV06R)**

Note: n = 00, 01, 02, 03, 10, 11, 12, or 13

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: CTUn\_SV06R is a 32-bit readable/writable register that sets the scale value for channel 6 of matrix row 0.



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	SVE06[23:0]	H'00 0000	R/W	Scale Value e06 for Input Channel 6 of Matrix Row 0 These bits set the scale value for input data of channel 6 of matrix row 0. SVE06[23]: Sign bit SVE06[22]: Integer bit SVE06[21:0]: Decimal bits

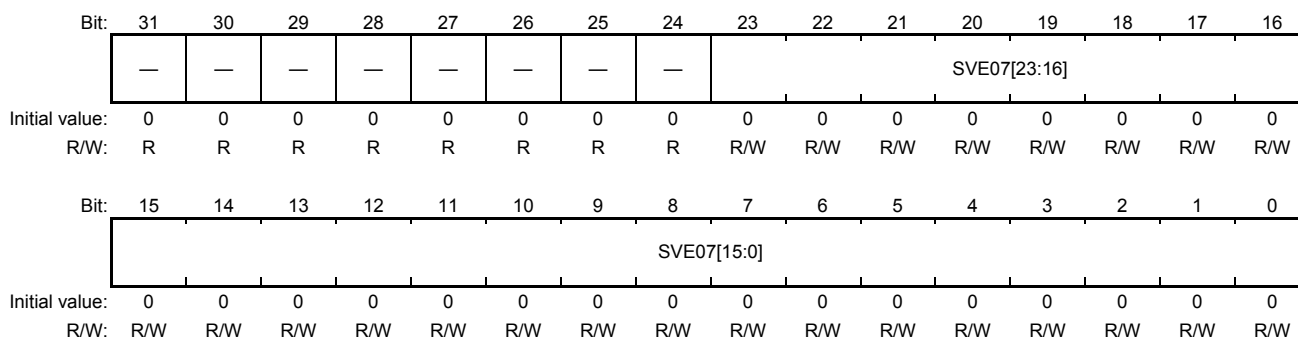
plus			minus		
Value	[time]	[dB]	Value	[time]	[dB]
H'7F_FFFF	2	6	H'80_0000	2	6
.....	.....	.....	.....	.....	.....
H'40_0000	1	0	H'C0_0000	1	0
.....	.....	.....	.....	.....	.....
H'00_0001	$2.38 \times 10^{-7}$	-132	.....	.....	.....
H'00_0000	0 (Mute)	$-\infty$	H'FF_FFFF	$2.38 \times 10^{-7}$	-132

### 34.2.39 CTUn Scale Value e07 Register (CTUn\_SV07R)

Note: n = 00, 01, 02, 03, 10, 11, 12, or 13

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: CTUn\_SV07R is a 32-bit readable/writable register that sets the scale value for channel 7 of matrix row 0.



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	SVE07[23:0]	H'00 0000	R/W	Scale Value e07 for Input Channel 7 of Matrix Row 0 These bits set the scale value for input data of channel 7 of matrix row 0. SVE07[23]: Sign bit SVE07[22]: Integer bit SVE07[21:0]: Decimal bits

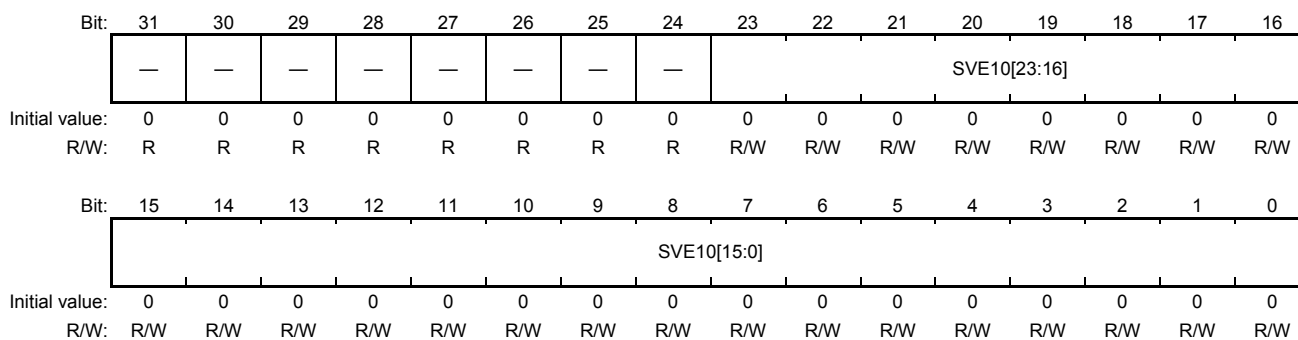
plus			minus		
Value	[time]	[dB]	Value	[time]	[dB]
H'7F_FFFF	2	6	H'80_0000	2	6
.....	.....	.....	.....	.....	.....
H'40_0000	1	0	H'C0_0000	1	0
.....	.....	.....	.....	.....	.....
H'00_0001	$2.38 \times 10^{-7}$	-132	.....	.....	.....
H'00_0000	0 (Mute)	$-\infty$	H'FF_FFFF	$2.38 \times 10^{-7}$	-132

### 34.2.40 CTUn Scale Value e10 Register (CTUn\_SV10R)

Note: n = 00, 01, 02, 03, 10, 11, 12, or 13

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: CTUn\_SV10R is a 32-bit readable/writable register that sets the scale value for channel 0 of matrix row 1.



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	SVE10[23:0]	H'00_0000	R/W	Scale Value e10 for Input Channel 0 of Matrix Row 1 These bits set the scale value for input data of channel 0 of matrix row 1. SVE10[23]: Sign bit SVE10[22]: Integer bit SVE10[21:0]: Decimal bits

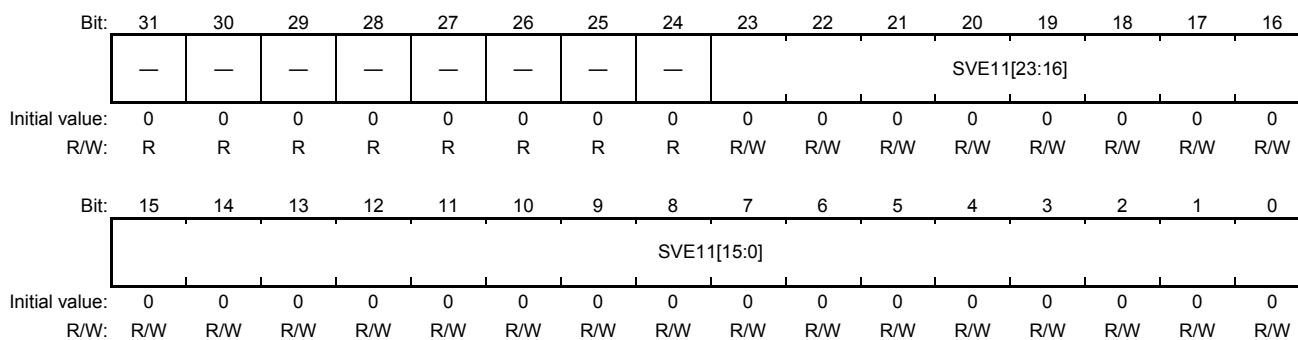
plus			minus		
Value	[time]	[dB]	Value	[time]	[dB]
H'7F_FFFF	2	6	H'80_0000	2	6
.....	.....	.....	.....	.....	.....
H'40_0000	1	0	H'C0_0000	1	0
.....	.....	.....	.....	.....	.....
H'00_0001	$2.38 \times 10^{-7}$	-132	.....	.....	.....
H'00_0000	0 (Mute)	$-\infty$	H'FF_FFFF	$2.38 \times 10^{-7}$	-132

### 34.2.41 CTUn Scale Value e11 Register (CTUn\_SV11R)

Note: n = 00, 01, 02, 03, 10, 11, 12, or 13

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: CTUn\_SV11R is a 32-bit readable/writable register that sets the scale value for channel 1 of matrix row 1.



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	SVE11[23:0]	H'00_0000	R/W	Scale Value e11 for Input Channel 1 of Matrix Row 1 These bits set the scale value for input data of channel 1 of matrix row 1. SVE11[23]: Sign bit SVE11[22]: Integer bit SVE11[21:0]: Decimal bits

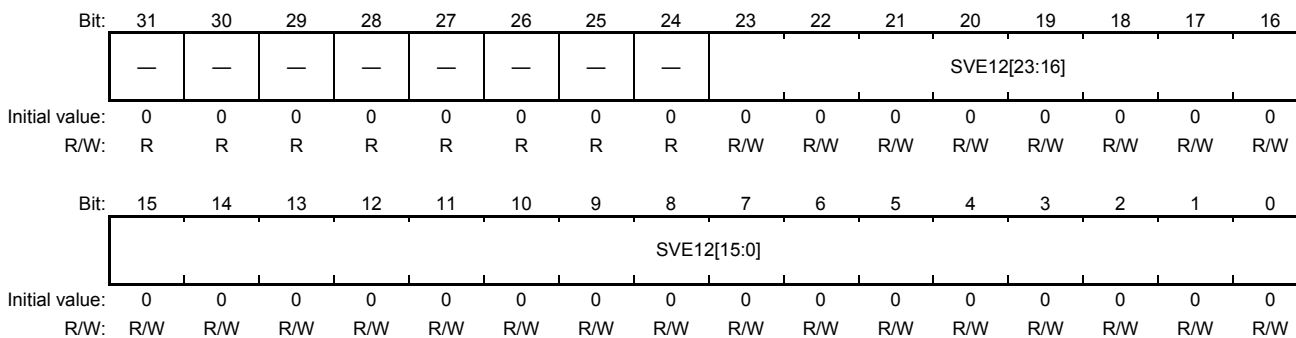
plus			minus		
Value	[time]	[dB]	Value	[time]	[dB]
H'7F_FFFF	2	6	H'80_0000	2	6
.....	.....	.....	.....	.....	.....
H'40_0000	1	0	H'C0_0000	1	0
.....	.....	.....	.....	.....	.....
H'00_0001	$2.38 \times 10^{-7}$	-132	.....	.....	.....
H'00_0000	0 (Mute)	$-\infty$	H'FF_FFFF	$2.38 \times 10^{-7}$	-132

**34.2.42 CTUn Scale Value e12 Register (CTUn\_SV12R)**

Note: n = 00, 01, 02, 03, 10, 11, 12, or 13

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: CTUn\_SV12R is a 32-bit readable/writable register that sets the scale value for channel 2 of matrix row 1.



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	SVE12[23:0]	H'00_0000	R/W	Scale Value e12 for Input Channel 2 of Matrix Row 1 These bits set the scale value for input data of channel 2 of matrix row 1. SVE12[23]: Sign bit SVE12[22]: Integer bit SVE12[21:0]: Decimal bits

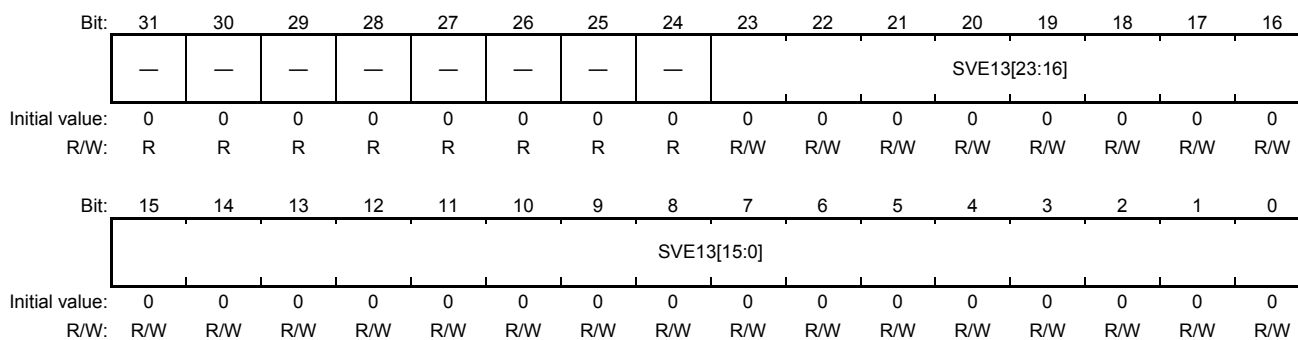
plus			minus		
Value	[time]	[dB]	Value	[time]	[dB]
H'7F_FFFF	2	6	H'80_0000	2	6
.....	.....	.....	.....	.....	.....
H'40_0000	1	0	H'C0_0000	1	0
.....	.....	.....	.....	.....	.....
H'00_0001	$2.38 \times 10^{-7}$	-132	.....	.....	.....
H'00_0000	0 (Mute)	$-\infty$	H'FF_FFFF	$2.38 \times 10^{-7}$	-132

### 34.2.43 CTUn Scale Value e13 Register (CTUn\_SV13R)

Note: n = 00, 01, 02, 03, 10, 11, 12, or 13

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: CTUn\_SV13R is a 32-bit readable/writable register that sets the scale value for channel 3 of matrix row 1.



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	SVE13[23:0]	H'00 0000	R/W	Scale Value e13 for Input Channel 3 of Matrix Row 1 These bits set the scale value for input data of channel 3 of matrix row 1. SVE13[23]: Sign bit SVE13[22]: Integer bit SVE13[21:0]: Decimal bits

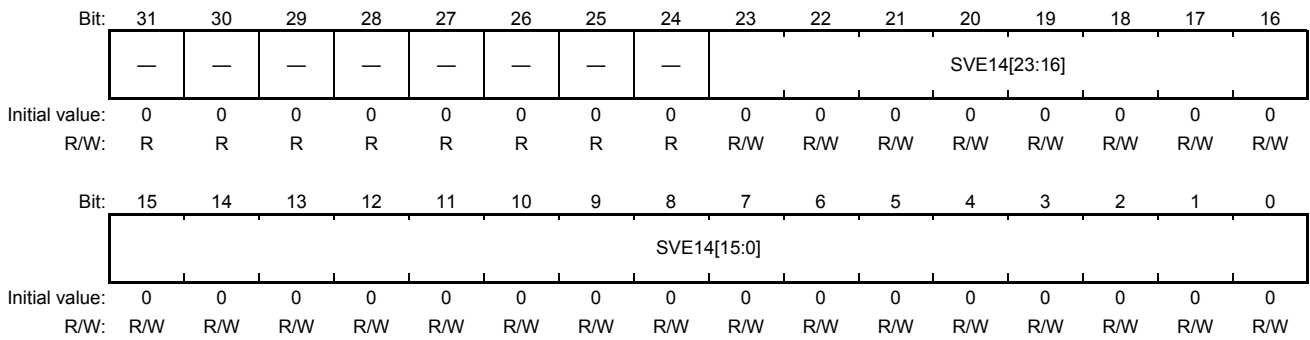
plus			minus		
Value	[time]	[dB]	Value	[time]	[dB]
H'7F_FFFF	2	6	H'80_0000	2	6
.....	.....	.....	.....	.....	.....
H'40_0000	1	0	H'C0_0000	1	0
.....	.....	.....	.....	.....	.....
H'00_0001	$2.38 \times 10^{-7}$	-132	.....	.....	.....
H'00_0000	0 (Mute)	$-\infty$	H'FF_FFFF	$2.38 \times 10^{-7}$	-132

**34.2.44 CTUn Scale Value e14 Register (CTUn\_SV14R)**

Note: n = 00, 01, 02, 03, 10, 11, 12, or 13

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: CTUn\_SV14R is a 32-bit readable/writable register that sets the scale value for channel 4 of matrix row 1.



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	SVE14[23:0]	H'00 0000	R/W	Scale Value e14 for Input Channel 4 of Matrix Row 1 These bits set the scale value for input data of channel 4 of matrix row 1. SVE14[23]: Sign bit SVE14[22]: Integer bit SVE14[21:0]: Decimal bits

plus			minus		
Value	[time]	[dB]	Value	[time]	[dB]
H'7F_FFFF	2	6	H'80_0000	2	6
.....	.....	.....	.....	.....	.....
H'40_0000	1	0	H'C0_0000	1	0
.....	.....	.....	.....	.....	.....
H'00_0001	$2.38 \times 10^{-7}$	-132	.....	.....	.....
H'00_0000	0 (Mute)	$-\infty$	H'FF_FFFF	$2.38 \times 10^{-7}$	-132

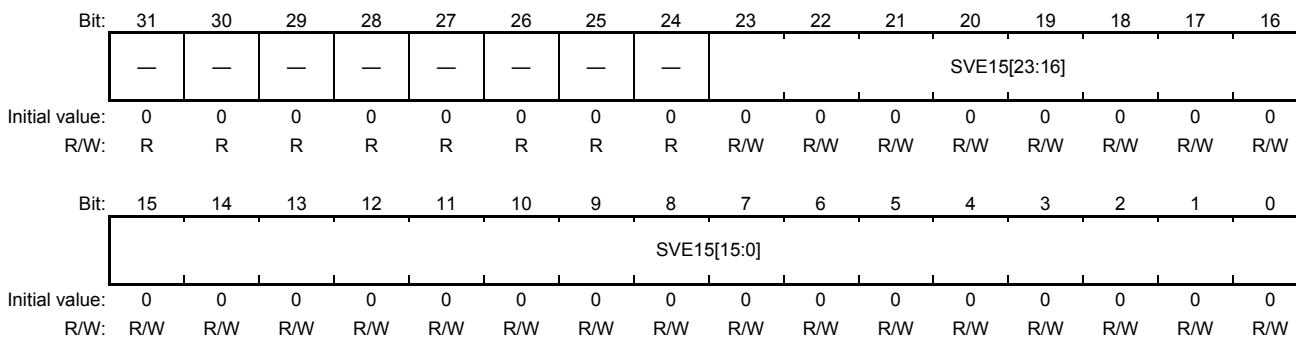


### 34.2.45 CTUn Scale Value e15 Register (CTUn\_SV15R)

Note: n = 00, 01, 02, 03, 10, 11, 12, or 13

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: CTUn\_SV15R is a 32-bit readable/writable register that sets the scale value for channel 5 of matrix row 1.



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	SVE15[23:0]	H'00 0000	R/W	Scale Value e15 for Input Channel 5 of Matrix Row 1 These bits set the scale value for input data of channel 5 of matrix row 1. SVE15[23]: Sign bit SVE15[22]: Integer bit SVE15[21:0]: Decimal bits

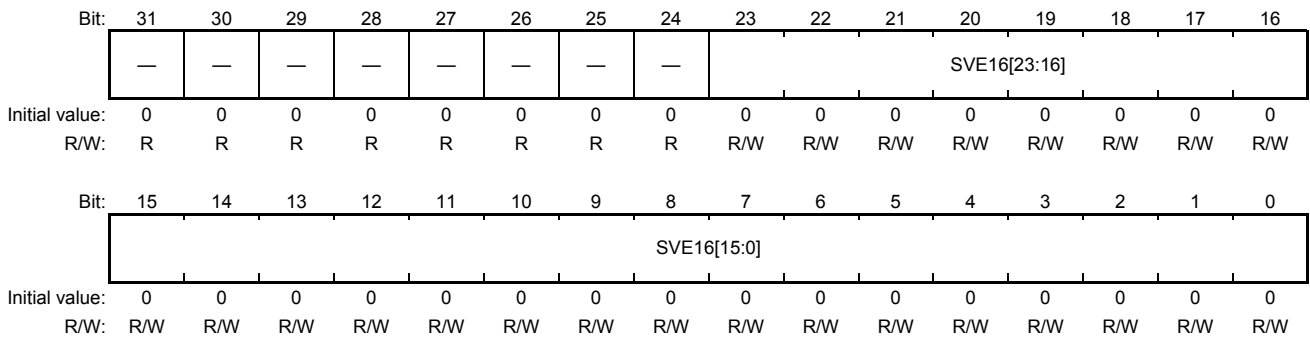
plus			minus		
Value	[time]	[dB]	Value	[time]	[dB]
H'7F_FFFF	2	6	H'80_0000	2	6
.....	.....	.....	.....	.....	.....
H'40_0000	1	0	H'C0_0000	1	0
.....	.....	.....	.....	.....	.....
H'00_0001	$2.38 \times 10^{-7}$	-132	.....	.....	.....
H'00_0000	0 (Mute)	$-\infty$	H'FF_FFFF	$2.38 \times 10^{-7}$	-132

**34.2.46 CTUn Scale Value e16 Register (CTUn\_SV16R)**

Note: n = 00, 01, 02, 03, 10, 11, 12, or 13

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: CTUn\_SV16R is a 32-bit readable/writable register that sets the scale value for channel 6 of matrix row 1.



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	SVE16[23:0]	H'00 0000	R/W	Scale Value e16 for Input Channel 6 of Matrix Row 1 These bits set the scale value for input data of channel 6 of matrix row 1. SVE16[23]: Sign bit SVE16[22]: Integer bit SVE16[21:0]: Decimal bits

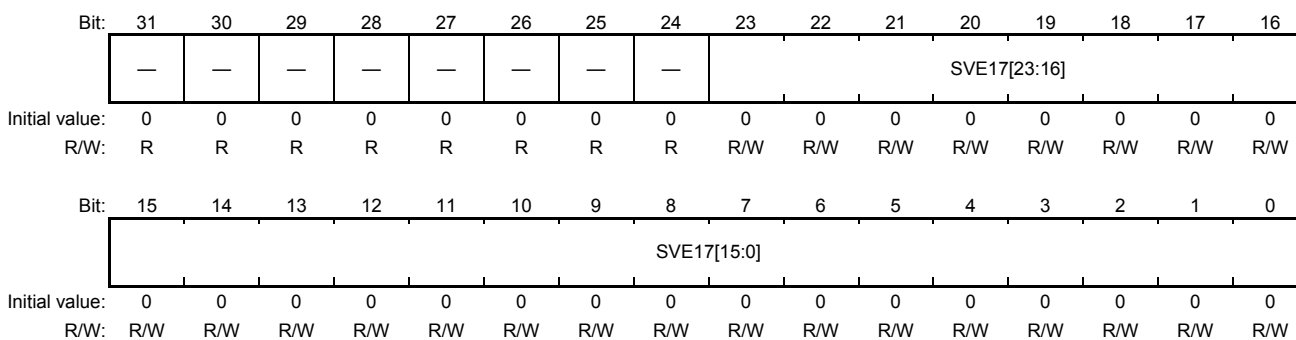
plus			minus		
Value	[time]	[dB]	Value	[time]	[dB]
H'7F_FFFF	2	6	H'80_0000	2	6
.....	.....	.....	.....	.....	.....
H'40_0000	1	0	H'C0_0000	1	0
.....	.....	.....	.....	.....	.....
H'00_0001	$2.38 \times 10^{-7}$	-132	.....	.....	.....
H'00_0000	0 (Mute)	$-\infty$	H'FF_FFFF	$2.38 \times 10^{-7}$	-132

### 34.2.47 CTUn Scale Value e17 Register (CTUn\_SV17R)

Note: n = 00, 01, 02, 03, 10, 11, 12, or 13

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: CTUn\_SV17R is a 32-bit readable/writable register that sets the scale value for channel 7 of matrix row 1.



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	SVE17[23:0]	H'00_0000	R/W	Scale Value e17 for Input Channel 7 of Matrix Row 1 These bits set the scale value for input data of channel 7 of matrix row 1. SVE17[23]: Sign bit SVE17[22]: Integer bit SVE17[21:0]: Decimal bits

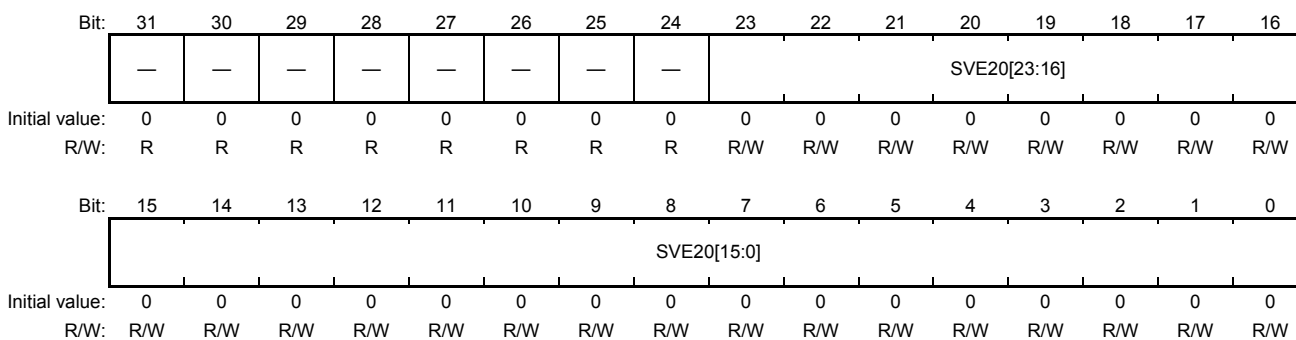
plus			minus		
Value	[time]	[dB]	Value	[time]	[dB]
H'7F_FFFF	2	6	H'80_0000	2	6
.....	.....	.....	.....	.....	.....
H'40_0000	1	0	H'C0_0000	1	0
.....	.....	.....	.....	.....	.....
H'00_0001	$2.38 \times 10^{-7}$	-132	.....	.....	.....
H'00_0000	0 (Mute)	$-\infty$	H'FF_FFFF	$2.38 \times 10^{-7}$	-132

**34.2.48 CTUn Scale Value e20 Register (CTUn\_SV20R)**

Note: n = 00, 01, 02, 03, 10, 11, 12, or 13

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: CTUn\_SV20R is a 32-bit readable/writable register that sets the scale value for channel 0 of matrix row 2.



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	SVE20[23:0]	H'00_0000	R/W	Scale Value e20 for Input Channel 0 of Matrix Row 2 These bits set the scale value for input data of channel 0 of matrix row 2. SVE20[23]: Sign bit SVE20[22]: Integer bit SVE20[21:0]: Decimal bits

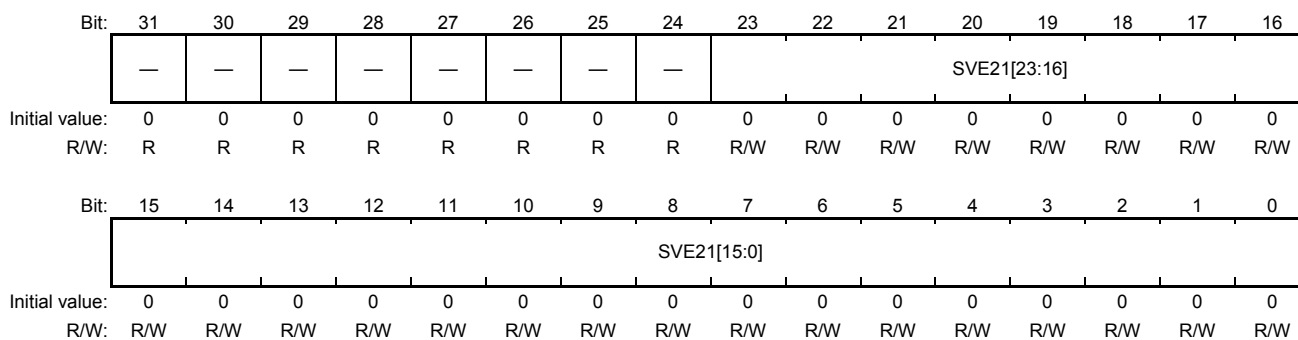
plus			minus		
Value	[time]	[dB]	Value	[time]	[dB]
H'7F_FFFF	2	6	H'80_0000	2	6
.....	.....	.....	.....	.....	.....
H'40_0000	1	0	H'C0_0000	1	0
.....	.....	.....	.....	.....	.....
H'00_0001	$2.38 \times 10^{-7}$	-132	.....	.....	.....
H'00_0000	0 (Mute)	$-\infty$	H'FF_FFFF	$2.38 \times 10^{-7}$	-132

### 34.2.49 CTUn Scale Value e21 Register (CTUn\_SV21R)

Note: n = 00, 01, 02, 03, 10, 11, 12, or 13

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: CTUn\_SV21R is a 32-bit readable/writable register that sets the scale value for channel 1 of matrix row 2.



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	SVE21[23:0]	H'00_0000	R/W	Scale Value e21 for Input Channel 1 of Matrix Row 2 These bits set the scale value for input data of channel 1 of matrix row 2. SVE21[23]: Sign bit SVE21[22]: Integer bit SVE21[21:0]: Decimal bits

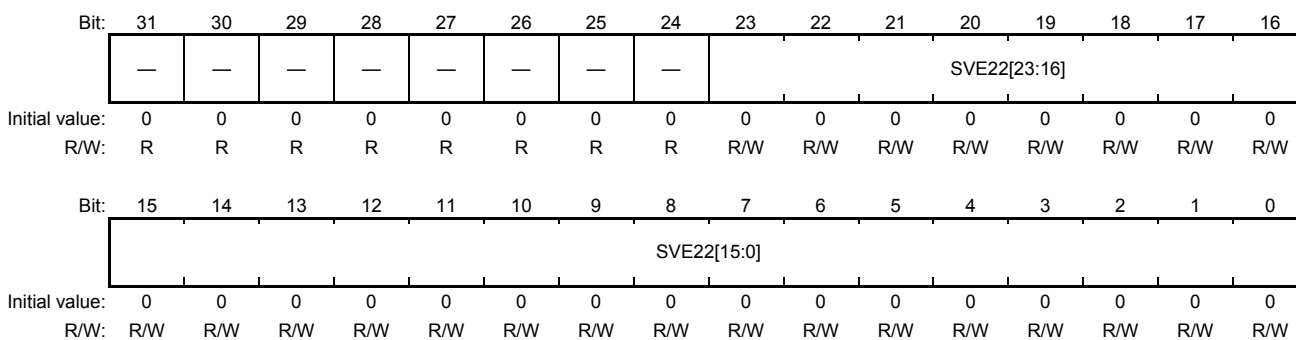
plus			minus		
Value	[time]	[dB]	Value	[time]	[dB]
H'7F_FFFF	2	6	H'80_0000	2	6
.....	.....	.....	.....	.....	.....
H'40_0000	1	0	H'C0_0000	1	0
.....	.....	.....	.....	.....	.....
H'00_0001	$2.38 \times 10^{-7}$	-132	.....	.....	.....
H'00_0000	0 (Mute)	$-\infty$	H'FF_FFFF	$2.38 \times 10^{-7}$	-132

### 34.2.50 CTUn Scale Value e22 Register (CTUn\_SV22R)

Note: n = 00, 01, 02, 03, 10, 11, 12, or 13

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: CTUn\_SV22R is a 32-bit readable/writable register that sets the scale value for channel 2 of matrix row 2.



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	SVE22[23:0]	H'00_0000	R/W	Scale Value e22 for Input Channel 2 of Matrix Row 2 These bits set the scale value for input data of channel 2 of matrix row 2. SVE22[23]: Sign bit SVE22[22]: Integer bit SVE22[21:0]: Decimal bits

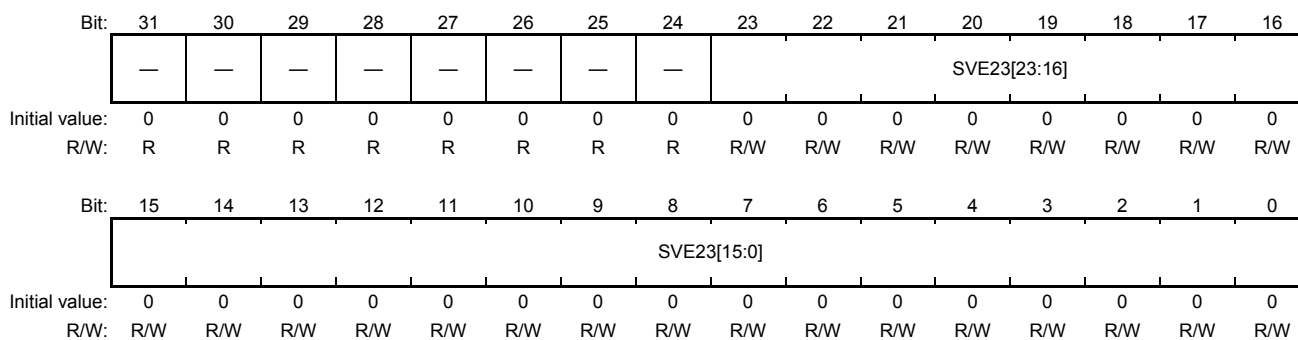
plus			minus		
Value	[time]	[dB]	Value	[time]	[dB]
H'7F_FFFF	2	6	H'80_0000	2	6
.....	.....	.....	.....	.....	.....
H'40_0000	1	0	H'C0_0000	1	0
.....	.....	.....	.....	.....	.....
H'00_0001	$2.38 \times 10^{-7}$	-132	.....	.....	.....
H'00_0000	0 (Mute)	$-\infty$	H'FF_FFFF	$2.38 \times 10^{-7}$	-132

### 34.2.51 CTUn Scale Value e23 Register (CTUn\_SV23R)

Note: n = 00, 01, 02, 03, 10, 11, 12, or 13

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: CTUn\_SV23R is a 32-bit readable/writable register that sets the scale value for channel 3 of matrix row 2.



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	SVE23[23:0]	H'00_0000	R/W	Scale Value e23 for Input Channel 3 of Matrix Row 2 These bits set the scale value for input data of channel 3 of matrix row 2. SVE23[23]: Sign bit SVE23[22]: Integer bit SVE23[21:0]: Decimal bits

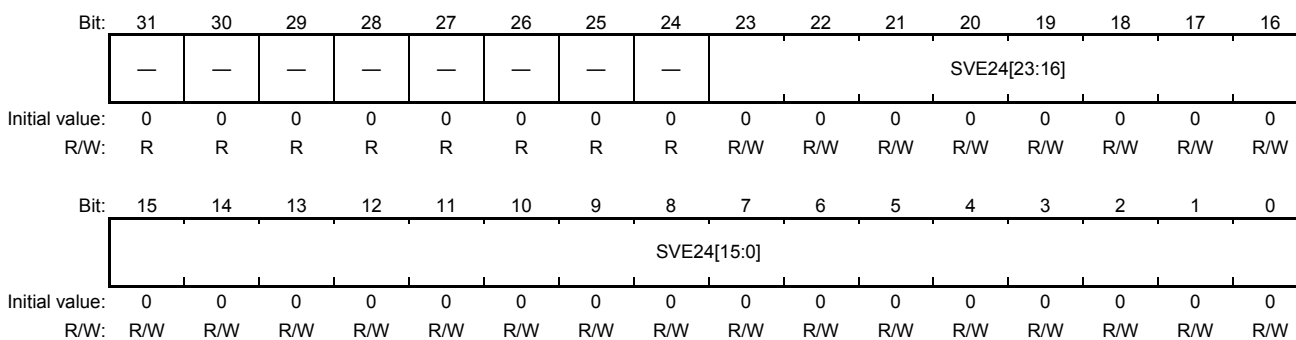
plus			minus		
Value	[time]	[dB]	Value	[time]	[dB]
H'7F_FFFF	2	6	H'80_0000	2	6
.....	.....	.....	.....	.....	.....
H'40_0000	1	0	H'C0_0000	1	0
.....	.....	.....	.....	.....	.....
H'00_0001	$2.38 \times 10^{-7}$	-132	.....	.....	.....
H'00_0000	0 (Mute)	$-\infty$	H'FF_FFFF	$2.38 \times 10^{-7}$	-132

### 34.2.52 CTUn Scale Value e24 Register (CTUn\_SV24R)

Note: n = 00, 01, 02, 03, 10, 11, 12, or 13

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: CTUn\_SV24R is a 32-bit readable/writable register that sets the scale value for channel 4 of matrix row 2.



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	SVE24[23:0]	H'00 0000	R/W	Scale Value e24 for Input Channel 4 of Matrix Row 2 These bits set the scale value for input data of channel 4 of matrix row 2. SVE24[23]: Sign bit SVE24[22]: Integer bit SVE24[21:0]: Decimal bits

plus			minus		
Value	[time]	[dB]	Value	[time]	[dB]
H'7F_FFFF	2	6	H'80_0000	2	6
.....	.....	.....	.....	.....	.....
H'40_0000	1	0	H'C0_0000	1	0
.....	.....	.....	.....	.....	.....
H'00_0001	$2.38 \times 10^{-7}$	-132	.....	.....	.....
H'00_0000	0 (Mute)	$-\infty$	H'FF_FFFF	$2.38 \times 10^{-7}$	-132

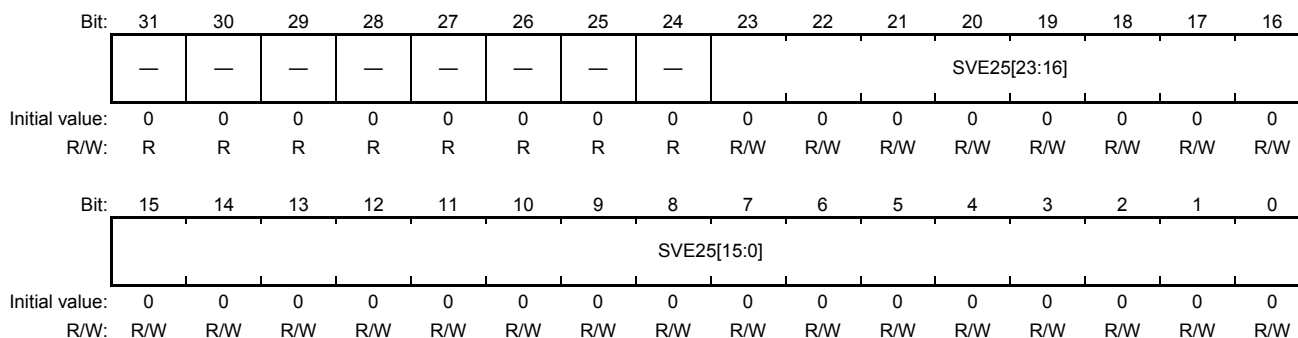


### 34.2.53 CTUn Scale Value e25 Register (CTUn\_SV25R)

Note: n = 00, 01, 02, 03, 10, 11, 12, or 13

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: CTUn\_SV25R is a 32-bit readable/writable register that sets the scale value for channel 5 of matrix row 2.



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	SVE25[23:0]	H'00 0000	R/W	Scale Value e25 for Input Channel 5 of Matrix Row 2 These bits set the scale value for input data of channel 5 of matrix row 2. SVE25[23]: Sign bit SVE25[22]: Integer bit SVE25[21:0]: Decimal bits

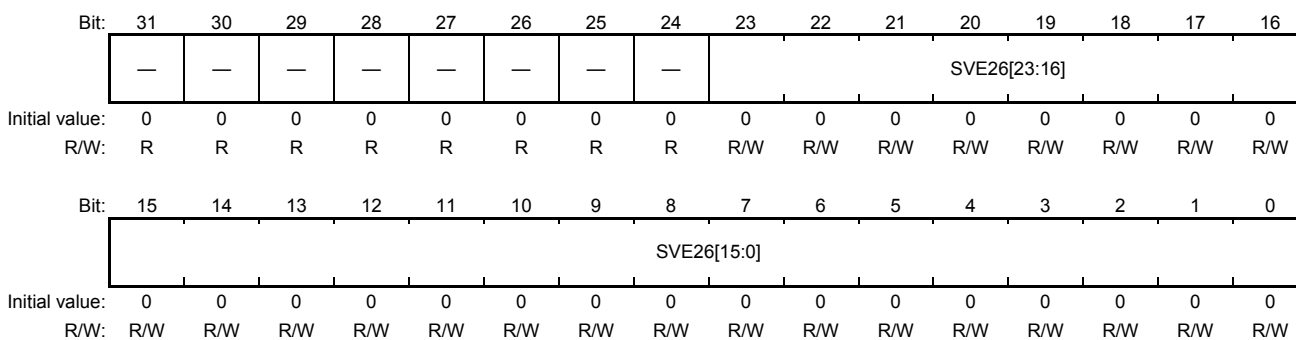
plus			minus		
Value	[time]	[dB]	Value	[time]	[dB]
H'7F_FFFF	2	6	H'80_0000	2	6
.....	.....	.....	.....	.....	.....
H'40_0000	1	0	H'C0_0000	1	0
.....	.....	.....	.....	.....	.....
H'00_0001	$2.38 \times 10^{-7}$	-132	.....	.....	.....
H'00_0000	0 (Mute)	$-\infty$	H'FF_FFFF	$2.38 \times 10^{-7}$	-132

### 34.2.54 CTUn Scale Value e26 Register (CTUn\_SV26R)

Note: n = 00, 01, 02, 03, 10, 11, 12, or 13

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: CTUn\_SV26R is a 32-bit readable/writable register that sets the scale value for channel 6 of matrix row 2.



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	SVE26[23:0]	H'00_0000	R/W	Scale Value e26 for Input Channel 6 of Matrix Row 2 These bits set the scale value for input data of channel 6 of matrix row 2. SVE26[23]: Sign bit SVE26[22]: Integer bit SVE26[21:0]: Decimal bits

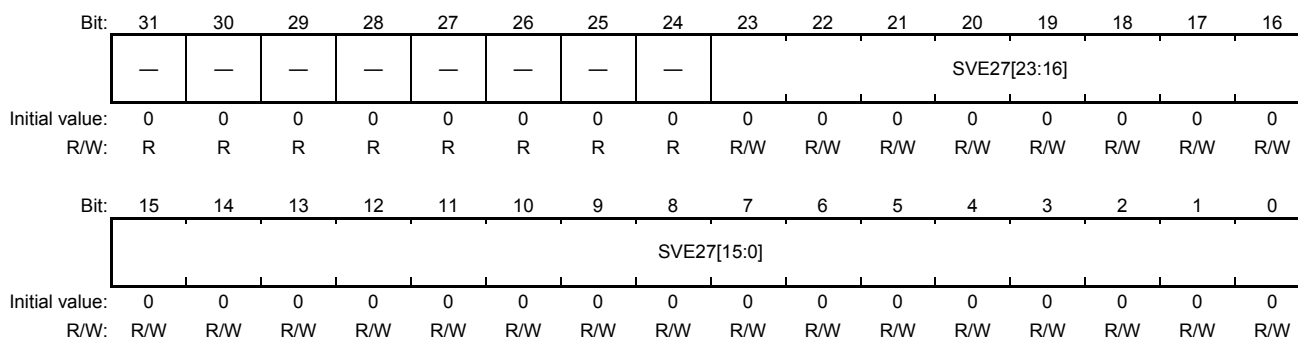
plus			minus		
Value	[time]	[dB]	Value	[time]	[dB]
H'7F_FFFF	2	6	H'80_0000	2	6
.....	.....	.....	.....	.....	.....
H'40_0000	1	0	H'C0_0000	1	0
.....	.....	.....	.....	.....	.....
H'00_0001	$2.38 \times 10^{-7}$	-132	.....	.....	.....
H'00_0000	0 (Mute)	$-\infty$	H'FF_FFFF	$2.38 \times 10^{-7}$	-132

### 34.2.55 CTUn Scale Value e27 Register (CTUn\_SV27R)

Note: n = 00, 01, 02, 03, 10, 11, 12, or 13

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: CTUn\_SV27R is a 32-bit readable/writable register that sets the scale value for channel 7 of matrix row 2.



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	SVE27[23:0]	H'00 0000	R/W	Scale Value e27 for Input Channel 7 of Matrix Row 2 These bits set the scale value for input data of channel 7 of matrix row 2. SVE27[23]: Sign bit SVE27[22]: Integer bit SVE27[21:0]: Decimal bits

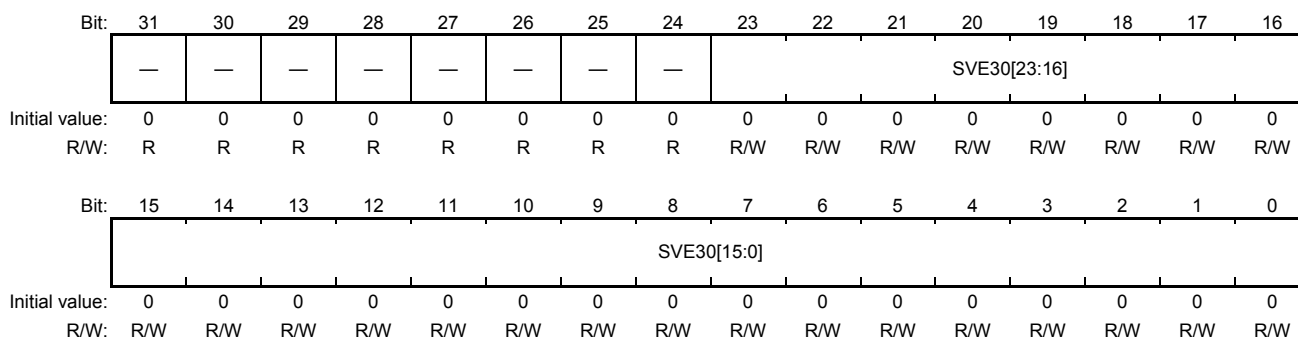
plus			minus		
Value	[time]	[dB]	Value	[time]	[dB]
H'7F_FFFF	2	6	H'80_0000	2	6
.....	.....	.....	.....	.....	.....
H'40_0000	1	0	H'C0_0000	1	0
.....	.....	.....	.....	.....	.....
H'00_0001	$2.38 \times 10^{-7}$	-132	.....	.....	.....
H'00_0000	0 (Mute)	$-\infty$	H'FF_FFFF	$2.38 \times 10^{-7}$	-132

### 34.2.56 CTUn Scale Value e30 Register (CTUn\_SV30R)

Note: n = 00, 01, 02, 03, 10, 11, 12, or 13

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: CTUn\_SV30R is a 32-bit readable/writable register that sets the scale value for channel 0 of matrix row 3.



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	SVE30[23:0]	H'00_0000	R/W	Scale Value e30 for Input Channel 0 of Matrix Row 3 These bits set the scale value for input data of channel 0 of matrix row 3. SVE30[23]: Sign bit SVE30[22]: Integer bit SVE30[21:0]: Decimal bits

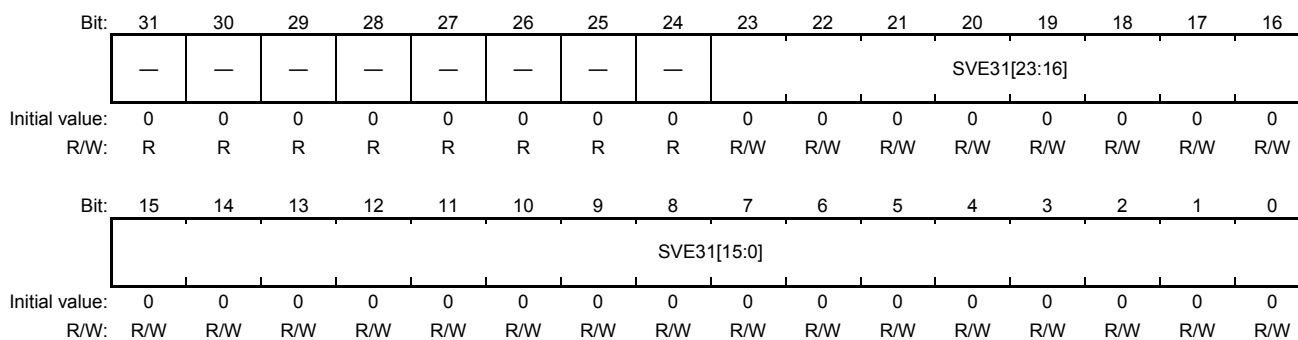
plus			minus		
Value	[time]	[dB]	Value	[time]	[dB]
H'7F_FFFF	2	6	H'80_0000	2	6
.....	.....	.....	.....	.....	.....
H'40_0000	1	0	H'C0_0000	1	0
.....	.....	.....	.....	.....	.....
H'00_0001	$2.38 \times 10^{-7}$	-132	.....	.....	.....
H'00_0000	0 (Mute)	$-\infty$	H'FF_FFFF	$2.38 \times 10^{-7}$	-132

### 34.2.57 CTUn Scale Value e31 Register (CTUn\_SV31R)

Note: n = 00, 01, 02, 03, 10, 11, 12, or 13

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: CTUn\_SV31R is a 32-bit readable/writable register that sets the scale value for channel 1 of matrix row 3.



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	SVE31[23:0]	H'00_0000	R/W	Scale Value e31 for Input Channel 1 of Matrix Row 3 These bits set the scale value for input data of channel 1 of matrix row 3. SVE31[23]: Sign bit SVE31[22]: Integer bit SVE31[21:0]: Decimal bits

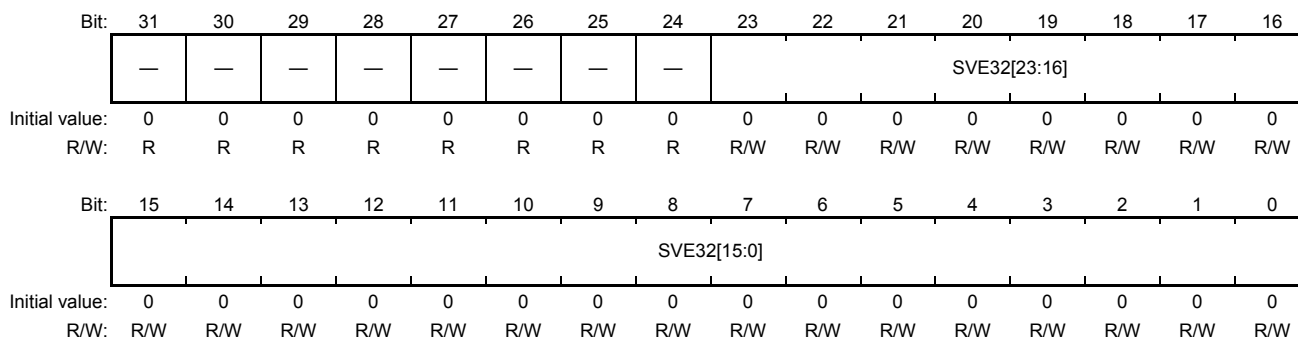
plus			minus		
Value	[time]	[dB]	Value	[time]	[dB]
H'7F_FFFF	2	6	H'80_0000	2	6
.....	.....	.....	.....	.....	.....
H'40_0000	1	0	H'C0_0000	1	0
.....	.....	.....	.....	.....	.....
H'00_0001	$2.38 \times 10^{-7}$	-132	.....	.....	.....
H'00_0000	0 (Mute)	$-\infty$	H'FF_FFFF	$2.38 \times 10^{-7}$	-132

### 34.2.58 CTUn Scale Value e32 Register (CTUn\_SV32R)

Note: n = 00, 01, 02, 03, 10, 11, 12, or 13

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: CTUn\_SV32R is a 32-bit readable/writable register that sets the scale value for channel 2 of matrix row 3.



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	SVE32[23:0]	H'00 0000	R/W	Scale Value e32 for Input Channel 2 of Matrix Row 3 These bits set the scale value for input data of channel 2 of matrix row 3. SVE32[23]: Sign bit SVE32[22]: Integer bit SVE32[21:0]: Decimal bits

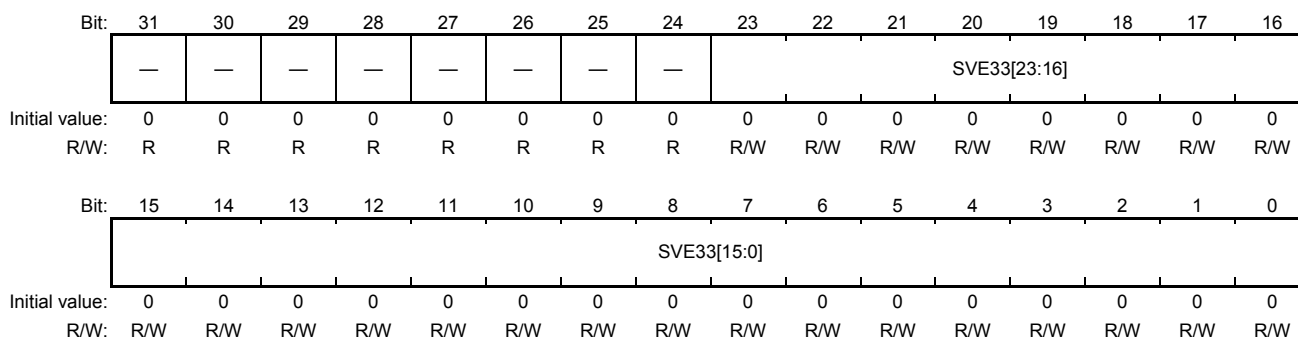
plus			minus		
Value	[time]	[dB]	Value	[time]	[dB]
H'7F_FFFF	2	6	H'80_0000	2	6
.....	.....	.....	.....	.....	.....
H'40_0000	1	0	H'C0_0000	1	0
.....	.....	.....	.....	.....	.....
H'00_0001	$2.38 \times 10^{-7}$	-132	.....	.....	.....
H'00_0000	0 (Mute)	$-\infty$	H'FF_FFFF	$2.38 \times 10^{-7}$	-132

### 34.2.59 CTUn Scale Value e33 Register (CTUn\_SV33R)

Note: n = 00, 01, 02, 03, 10, 11, 12, or 13

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: CTUn\_SV33R is a 32-bit readable/writable register that sets the scale value for channel 3 of matrix row 3.



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	SVE33[23:0]	H'00_0000	R/W	Scale Value e33 for Input Channel 3 of Matrix Row 3 These bits set the scale value for input data of channel 3 of matrix row 3. SVE33[23]: Sign bit SVE33[22]: Integer bit SVE33[21:0]: Decimal bits

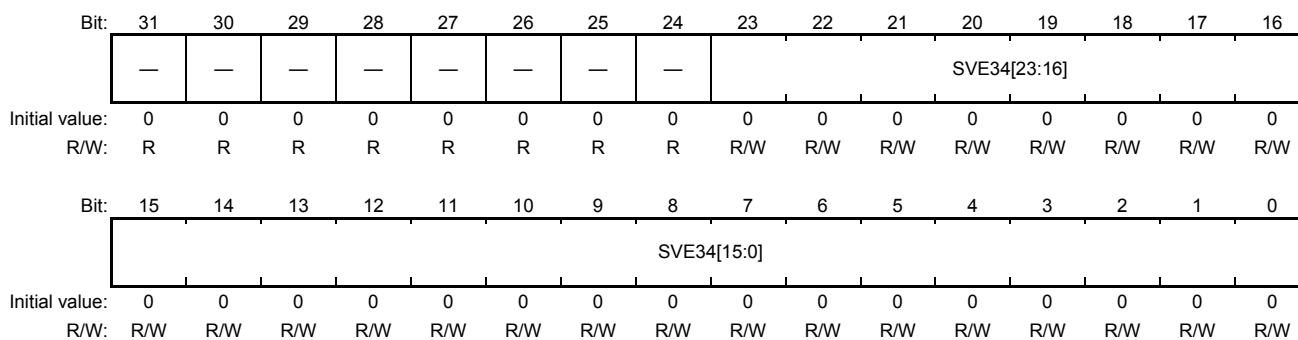
plus			minus		
Value	[time]	[dB]	Value	[time]	[dB]
H'7F_FFFF	2	6	H'80_0000	2	6
.....	.....	.....	.....	.....	.....
H'40_0000	1	0	H'C0_0000	1	0
.....	.....	.....	.....	.....	.....
H'00_0001	$2.38 \times 10^{-7}$	-132	.....	.....	.....
H'00_0000	0 (Mute)	$-\infty$	H'FF_FFFF	$2.38 \times 10^{-7}$	-132

### 34.2.60 CTUn Scale Value e34 Register (CTUn\_SV34R)

Note: n = 00, 01, 02, 03, 10, 11, 12, or 13

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: CTUn\_SV34R is a 32-bit readable/writable register that sets the scale value for channel 4 of matrix row 3.



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	SVE34[23:0]	H'00 0000	R/W	Scale Value e34 for Input Channel 4 of Matrix Row 3 These bits set the scale value for input data of channel 4 of matrix row 3. SVE34[23]: Sign bit SVE34[22]: Integer bit SVE34[21:0]: Decimal bits

plus			minus		
Value	[time]	[dB]	Value	[time]	[dB]
H'7F_FFFF	2	6	H'80_0000	2	6
.....	.....	.....	.....	.....	.....
H'40_0000	1	0	H'C0_0000	1	0
.....	.....	.....	.....	.....	.....
H'00_0001	$2.38 \times 10^{-7}$	-132	.....	.....	.....
H'00_0000	0 (Mute)	$-\infty$	H'FF_FFFF	$2.38 \times 10^{-7}$	-132

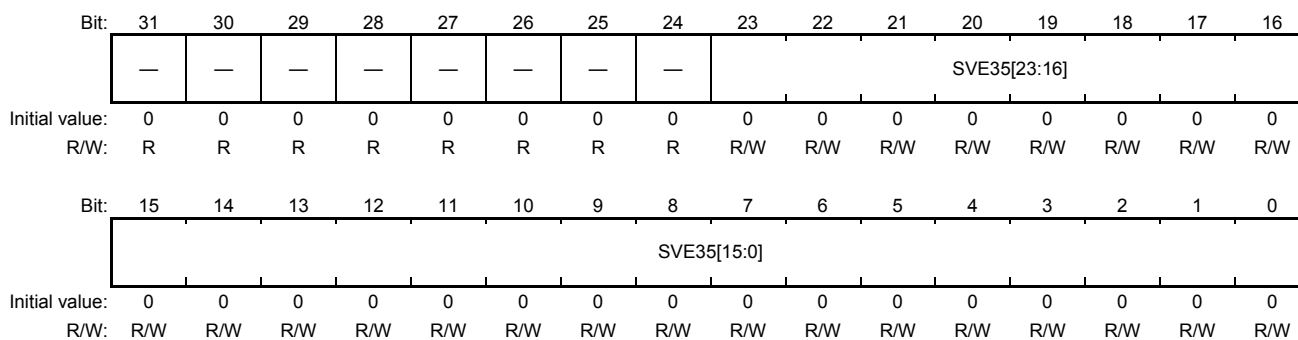


### 34.2.61 CTUn Scale Value e35 Register (CTUn\_SV35R)

Note: n = 00, 01, 02, 03, 10, 11, 12, or 13

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: CTUn\_SV35R is a 32-bit readable/writable register that sets the scale value for channel 5 of matrix row 3.



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	SVE35[23:0]	H'00_0000	R/W	Scale Value e35 for Input Channel 5 of Matrix Row 3 These bits set the scale value for input data of channel 5 of matrix row 3. SVE35[23]: Sign bit SVE35[22]: Integer bit SVE35[21:0]: Decimal bits

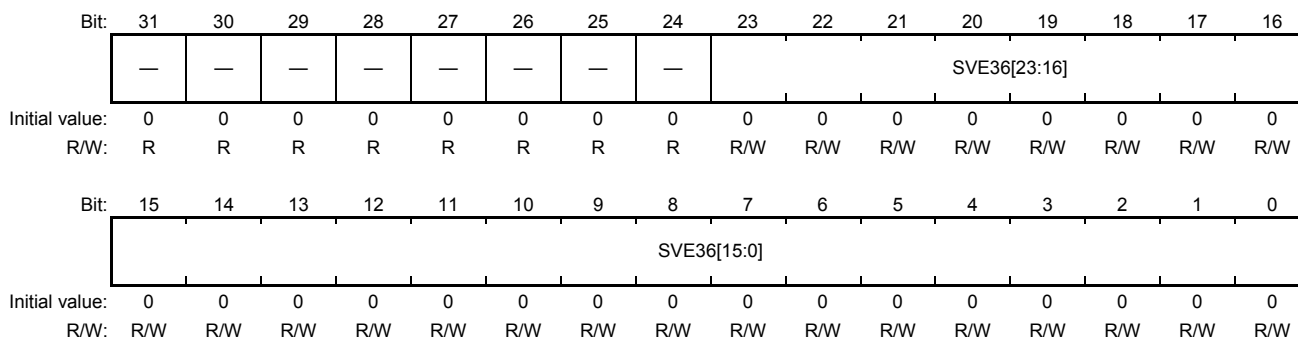
plus			minus		
Value	[time]	[dB]	Value	[time]	[dB]
H'7F_FFFF	2	6	H'80_0000	2	6
.....	.....	.....	.....	.....	.....
H'40_0000	1	0	H'C0_0000	1	0
.....	.....	.....	.....	.....	.....
H'00_0001	$2.38 \times 10^{-7}$	-132	.....	.....	.....
H'00_0000	0 (Mute)	$-\infty$	H'FF_FFFF	$2.38 \times 10^{-7}$	-132

### 34.2.62 CTUn Scale Value e36 Register (CTUn\_SV36R)

Note: n = 00, 01, 02, 03, 10, 11, 12, or 13

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: CTUn\_SV36R is a 32-bit readable/writable register that sets the scale value for channel 6 of matrix row 3.



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	SVE36[23:0]	H'00 0000	R/W	Scale Value e36 for Input Channel 6 of Matrix Row 3 These bits set the scale value for input data of channel 6 of matrix row 3. SVE36[23]: Sign bit SVE36[22]: Integer bit SVE36[21:0]: Decimal bits

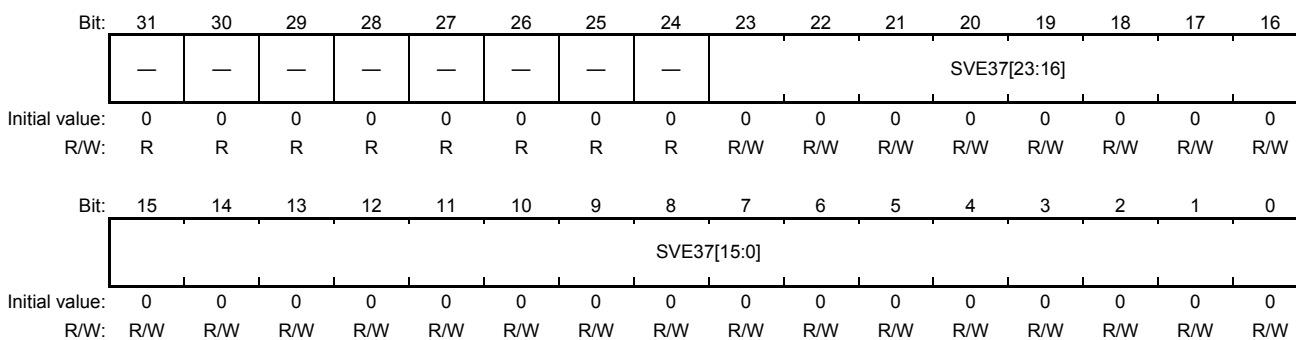
plus			minus		
Value	[time]	[dB]	Value	[time]	[dB]
H'7F_FFFF	2	6	H'80_0000	2	6
.....	.....	.....	.....	.....	.....
H'40_0000	1	0	H'C0_0000	1	0
.....	.....	.....	.....	.....	.....
H'00_0001	$2.38 \times 10^{-7}$	-132	.....	.....	.....
H'00_0000	0 (Mute)	$-\infty$	H'FF_FFFF	$2.38 \times 10^{-7}$	-132

**34.2.63 CTUn Scale Value e37 Register (CTUn\_SV37R)**

Note: n = 00, 01, 02, 03, 10, 11, 12, or 13

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: CTUn\_SV37R is a 32-bit readable/writable register that sets the scale value for channel 7 of matrix row 3.



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	SVE37[23:0]	H'00_0000	R/W	Scale Value e37 for Input Channel 7 of Matrix Row 3 These bits set the scale value for input data of channel 7 of matrix row 3. SVE37[23]: Sign bit SVE37[22]: Integer bit SVE37[21:0]: Decimal bits

plus			minus		
Value	[time]	[dB]	Value	[time]	[dB]
H'7F_FFFF	2	6	H'80_0000	2	6
.....	.....	.....	.....	.....	.....
H'40_0000	1	0	H'C0_0000	1	0
.....	.....	.....	.....	.....	.....
H'00_0001	$2.38 \times 10^{-7}$	-132	.....	.....	.....
H'00_0000	0 (Mute)	$-\infty$	H'FF_FFFF	$2.38 \times 10^{-7}$	-132

**34.2.64 MIXp Software Reset Register (MIXp\_SWRSR)**

Note: p = 0 or 1

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: MIXp\_SWRSR is a 32-bit readable/writable register that controls operation/reset of the MIX internal circuits.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SWRST
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	SWRST	1	R/W	Software Reset While this bit is 0, the MIX internal circuits are put in the reset state. MIXp_* registers except this register are reset. Therefore, they should be set again after the reset is canceled. 0: Resets the MIX 1: Operating state

**34.2.65 MIXp MIX Initialization Register (MIXp\_MIXIR)**

Note: p = 0 or 1

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: MIXp\_MIXIR is a 32-bit readable/writable register that initializes the operation of the MIX internal circuits.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	INIT
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	INIT	1	R/W	Initialization of Processing When this bit is set to 1, the MIX processing is initialized. This bit should be cleared to 0 after it was set to 1. 0: Processing State 1: Initialization (sets the initial setting of other registers)

**34.2.66 MIXp Audio Information Register (MIXp\_ADINR)**

Note: p = 0 or 1

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: MIXp\_ADINR is a 32-bit readable/writable register that selects channel number.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	CHNUM[3:0]				
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3 to 0	CHNUM[3:0]	0000	R/W	Channel Number These bits set the channel number 0000: 0 (None) 0001: 1 channel 0010: 2 channels 0011: Reserved 0100: 4 channels 0101: Reserved 0110: 6 channels 0111: Reserved 1000: 8 channels 1001 to 1111: Reserved

**34.2.67 MIXp MIX Mode Register (MIXp\_MIXMR)**

Note: p = 0 or 1

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: MIXp\_MIXMR is a 32-bit readable/writable register that controls the mix mode.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	MIX MODE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	MIXMODE	0	R/W	MIX Mode This bit controls the mix mode. 0: Selects volume step mixer 1: Selects volume ramp mixer

**34.2.68 MIXp MIX Volume Period Register (MIXp\_MVPDR)**

Note: p = 0 or 1

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: MIXp\_MVPDR is a 32-bit readable/writable register that sets the value of the change of the volume a sample.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	MXPDU[3:0]				—	—	—	—	MXPDDW[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11 to 8	MXPDU[3:0]	0000	R/W	MIX Period for Volume Up These bits set the decibel value that changed by one sample for volume down. And when MIXMODE bit of MIXp_MIXMR register is 1, this setting can be used. 0000: 128 dB / 1 sample 0001: 64 dB / 1 sample 0010: 32 dB / 1 sample 0011: 16 dB / 1 sample 0100: 8 dB / 1 sample 0101: 4 dB / 1 sample 0110: 2 dB / 1 sample 0111: 1 dB / 1 sample 1000: 0.5 dB / 1 sample 1001: 0.25 dB / 1 sample 1010: 0.125 dB / 1 sample 1011 to 1111: Reserved
7 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.



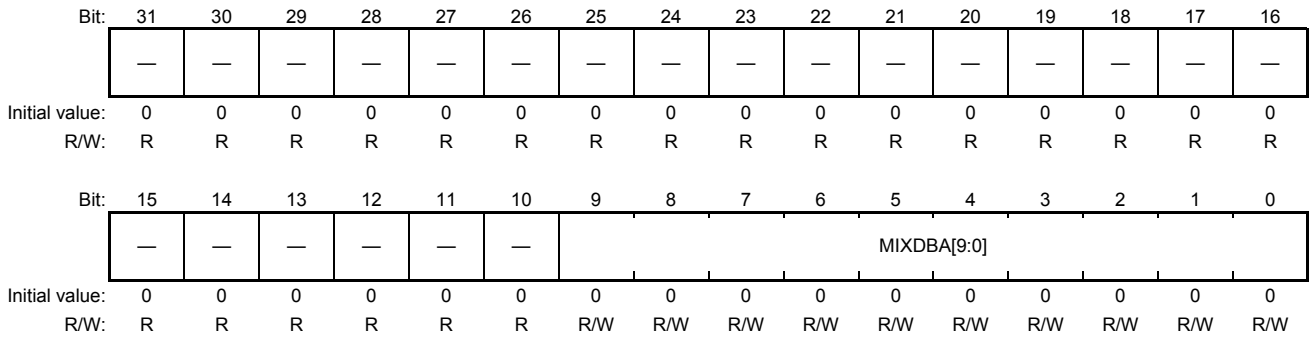
Bit	Bit Name	Initial Value	R/W	Description
3 to 0	MXPDDW[3:0]	0000	R/W	<p>MIX Period for Volume Down</p> <p>These bits set the decibel value that changed by one sample for volume up. And when MIXMODE bit of MIXp_MIXMR register is 1, this setting can be used.</p> <p>0000: -128 dB / 1 sample            0001: -64 dB / 1 sample            0010: -32 dB / 1 sample            0011: -16 dB / 1 sample            0100: -8 dB / 1 sample            0101: -4 dB / 1 sample            0110: -2 dB / 1 sample            0111: -1 dB / 1 sample            1000: -0.5 dB / 1 sample            1001: -0.25 dB / 1 sample            1010: -0.125 dB / 1 sample            1011 to 1111: Reserved</p>

**34.2.69 MIXp MIX Decibel A Register (MIXp\_MDBAR)**

Note: p = 0 or 1

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: MIXp\_MDBAR is a 32-bit readable/writable register that sets the decibel (gain level) of system A.



Bit	Bit Name	Initial Value	R/W	Description
31 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9 to 0	MIXDBA[9:0]	All 0	R/W	dB of System A These bits control the decibel (gain level) of system A. The value can select 1024 points from 0 dB to $-\infty$ dB at intervals of 0.125 dB.

Value	[time]	[dB]	Value	[time]	[dB]
H'000	1	0	.....	.....	.....
.....	.....	.....	H'091	0.125	-18.125
H'031	0.5	-6.125	.....	.....	.....
.....	.....	.....	H'3FE	$4.1 \times 10^{-7}$	-127.75
H'061	0.25	-12.125	H'3FF	0 (Mute)	$-\infty$

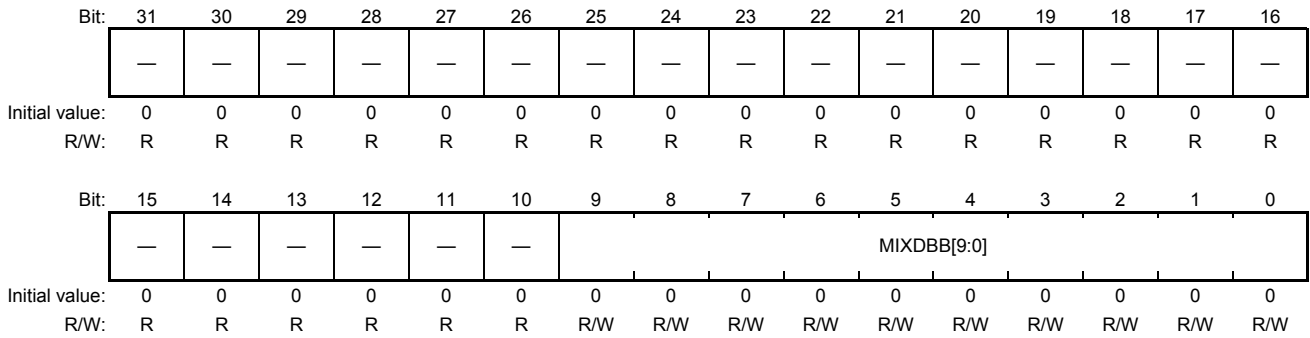
The relation between the setting value and the decibel is shown in Tables 34.9, 34.10, 34.11 and 34.12.

**34.2.70 MIXp MIX Decibel B Register (MIXp\_MDBBR)**

Note: p = 0 or 1

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: MIXp\_MDBBR is a 32-bit readable/writable register that sets the decibel (gain level) of system B.



Bit	Bit Name	Initial Value	R/W	Description
31 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9 to 0	MIXDBB[9:0]	All 0	R/W	dB of System B These bits control the decibel (gain level) of system B. The value can select 1024 points from 0 dB to $-\infty$ dB at intervals of 0.125 dB.

Value	[time]	[dB]	Value	[time]	[dB]
H'000	1	0	.....	.....	.....
.....	.....	.....	H'091	0.125	-18.125
H'031	0.5	-6.125	.....	.....	.....
.....	.....	.....	H'3FE	$4.1 \times 10^{-7}$	-127.75
H'061	0.25	-12.125	H'3FF	0 (Mute)	$-\infty$

The relation between the setting value and the decibel is shown in Tables 34.9, 34.10, 34.11 and 34.12.

### 34.2.71 MIXp MIX Decibel C Register (MIXp\_MDBCR)

Note: p = 0 or 1

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: MIXp\_MDBCR is a 32-bit readable/writable register that sets the decibel (gain level) of system C.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	MIXDBC[9:0]									
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

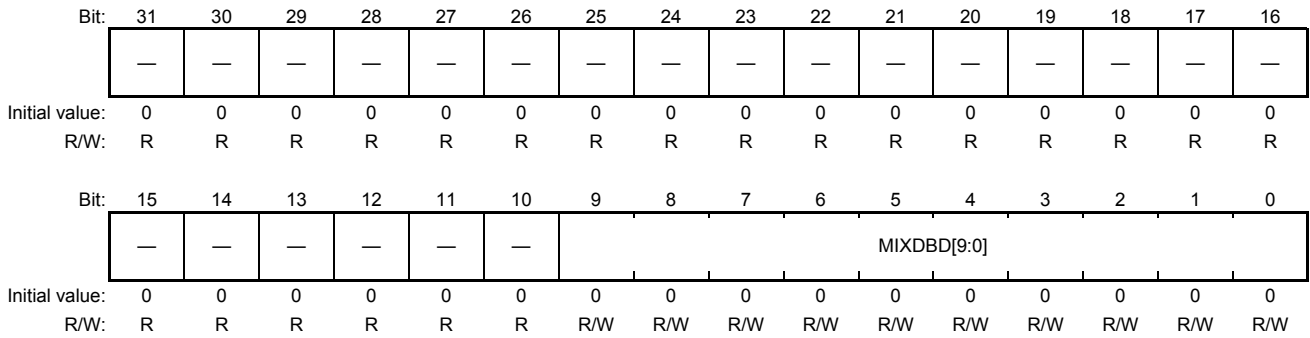
Bit	Bit Name	Initial Value	R/W	Description																																				
31 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.																																				
9 to 0	MIXDBC[9:0]	All 0	R/W	dB of System C These bits control the decibel (gain level) of system C. The value can select 1024 points from 0 dB to $-\infty$ dB at intervals of 0.125 dB.																																				
<table border="1"> <thead> <tr> <th>Value</th> <th>[time]</th> <th>[dB]</th> <th>Value</th> <th>[time]</th> <th>[dB]</th> </tr> </thead> <tbody> <tr> <td>H'000</td> <td>1</td> <td>0</td> <td>.....</td> <td>.....</td> <td>.....</td> </tr> <tr> <td>.....</td> <td>.....</td> <td>.....</td> <td>H'091</td> <td>0.125</td> <td>-18.125</td> </tr> <tr> <td>H'031</td> <td>0.5</td> <td>-6.125</td> <td>.....</td> <td>.....</td> <td>.....</td> </tr> <tr> <td>.....</td> <td>.....</td> <td>.....</td> <td>H'3FE</td> <td><math>4.1 \times 10^{-7}</math></td> <td>-127.75</td> </tr> <tr> <td>H'061</td> <td>0.25</td> <td>-12.125</td> <td>H'3FF</td> <td>0 (Mute)</td> <td><math>-\infty</math></td> </tr> </tbody> </table>					Value	[time]	[dB]	Value	[time]	[dB]	H'000	1	0	.....	.....	.....	.....	.....	.....	H'091	0.125	-18.125	H'031	0.5	-6.125	.....	.....	.....	.....	.....	.....	H'3FE	$4.1 \times 10^{-7}$	-127.75	H'061	0.25	-12.125	H'3FF	0 (Mute)	$-\infty$
Value	[time]	[dB]	Value	[time]	[dB]																																			
H'000	1	0	.....	.....	.....																																			
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.....	.....	.....	H'3FE	$4.1 \times 10^{-7}$	-127.75																																			
H'061	0.25	-12.125	H'3FF	0 (Mute)	$-\infty$																																			
The relation between the setting value and the decibel is shown in Tables 34.9, 34.10, 34.11 and 34.12.																																								

**34.2.72 MIXp MIX Decibel D Register (MIXp\_MDBDR)**

Note: p = 0 or 1

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: MIXp\_MDBDR is a 32-bit readable/writable register that sets the decibel (gain level) of system D.



Bit	Bit Name	Initial Value	R/W	Description
31 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9 to 0	MIXDBD[9:0]	All 0	R/W	dB of System D These bits control the decibel (gain level) of system D. The value can select 1024 points from 0 dB to $-\infty$ dB at intervals of 0.125 dB.

Value	[time]	[dB]	Value	[time]	[dB]
H'000	1	0	.....	.....	.....
.....	.....	.....	H'091	0.125	-18.125
H'031	0.5	-6.125	.....	.....	.....
.....	.....	.....	H'3FE	$4.1 \times 10^{-7}$	-127.75
H'061	0.25	-12.125	H'3FF	0 (Mute)	$-\infty$

The relation between the setting value and the decibel is shown in Tables 34.9, 34.10, 34.11 and 34.12.

**34.2.73 MIXp MIX Decibel Enable Register (MIXp\_MDBER)**

Note: p = 0 or 1

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: MIXp\_MDBER is a 32-bit readable/writable register that controls the dB value.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	MIX DBEN
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	MIXDBEN	0	R/W	MIX dB Enable This bit controls the dB value that sets in MIXp_MDBAR, MIXp_MDBBR, MIXp_MDBCR and MIXp_MDBDR registers. 0: Disables the setting of dB 1: Enables the setting of dB

**34.2.74 MIXp MIX Status Register (MIXp\_MIXSR)**

Note: p = 0 or 1

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: MIXp\_MIXSR is a 32-bit readable register that indicates the status of the volume ramp.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	MRPSTS
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1, 0	MRPSTS	00	R	MIX Volume Ramp Status These bits indicate the volume ramp status of mix operation. 00: Level of volume ramp is stable 01: Volume ramp down 10: Volume ramp up

**34.2.75 DVCp Software Reset Register (DVCp\_SWRSR)**

Note: p = 0 or 1

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: DVCp\_SWRSR is a 32-bit readable/writable register that controls operation/reset of the DVC internal circuits.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SWRST
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	SWRST	1	R/W	Software Reset While this bit is 0, the DVC internal circuits are put in the reset state. DVCp_* registers except this register are reset. Therefore, they should be set again after the reset is canceled. 0: Resets the DVC 1: Operating state



**34.2.76 DVCp DVU Initialization Register (DVCp\_DVUIR)**

Note: p = 0 or 1

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: DVCp\_DVUIR is a 32-bit readable/writable register that initializes the operation of the DVC internal circuits.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	INIT
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

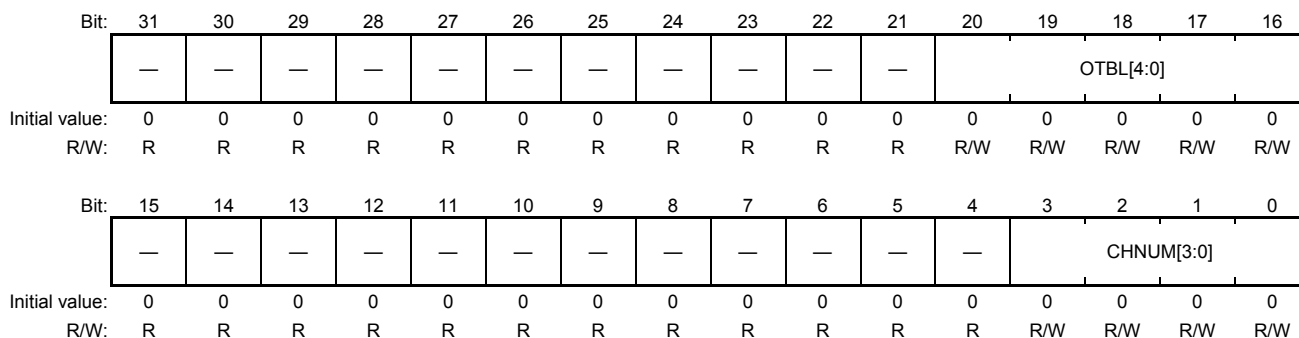
Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	INIT	1	R/W	Initialization of Processing When this bit is set to 1, the DVC processing is initialized. This bit should be cleared to 0 after it was set to 1. 0: Processing State 1: Initialization (sets the initial setting of other registers)

### 34.2.77 DVCp Audio Information Register (DVCp\_ADINR)

Note: p = 0 or 1

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: DVCp\_ADINR is a 32-bit readable/writable register that selects channel number and bit length of output audio data.



Bit	Bit Name	Initial Value	R/W	Description
31 to 21	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
20 to 16	OTBL[4:0]	00000	R/W	Bit Length of Output Audio Data. These bits set the bit length of output audio data. 00000: 24 bits 00001: Reserved 00010: 22 bits 00011: Reserved 00100: 20 bits 00101: Reserved 00110: 18 bits 00111: Reserved 01000: 16 bits 01001 to 01111: Reserved 10000: 8 bits 10001 to 11111: Reversed
15 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

---

Bit	Bit Name	Initial Value	R/W	Description
3 to 0	CHNUM[3:0]	0000	R/W	Channel Number
				These bits set the channel number
				0000: 0 (None)
				0001: 1 channel
				0010: 2 channels
				0011: Reserved
				0100: 4 channels
				0101: Reserved
				0110: 6 channels
				0111: Reserved
				1000: 8 channels
				1001 to 1111: Reserved

---

**34.2.78 DVCp DVU Control Register (DVCp\_DVUCR)**

Note: p = 0 or 1

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: DVCp\_DVUCR is a 32-bit readable/writable register that selects the mode of function to operate.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	HWMD
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	VVMD	—	—	—	VRMD	—	—	—	ZCMD
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R	R	R	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 17	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
16	HWMD	0	R/W	Enable the DVC_MUTE pin This bit enables DVC_MUTE pin for the setting of DVCEN bit of DVCp_DVUER register. (Set enable only. To set disable, write 0 DVCEN bit) 0: Disables the DVC_MUTE pin 1: Enables the DVC_MUTE pin
15 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	VVMD	0	R/W	Select Digital Volume Value Mode This bit selects the digital volume value function. 0: Sleep the digital volume value function 1: Use the digital volume value function
7 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	VRMD	0	R/W	Select Volume Ramp Mode This bit selects the volume ramp function. 0: Sleep the volume ramp function 1: Use the volume ramp function
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	ZCMD	0	R/W	Select Zero Cross Mute Mode This bit selects the zero cross mute function. 0: Sleep the zero cross mute function 1: Use the zero cross mute function

### 34.2.79 DVCp Zero Cross Mute Control Register (DVCp\_ZCMCR)

Note: p = 0 or 1

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: DVCp\_ZCMCR is a 32-bit readable/writable register that controls the operation of the zero cross mute function for each channel.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	ZCEN7	ZCEN6	ZCEN5	ZCEN4	ZCEN3	ZCEN2	ZCEN1	ZCEN0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7	ZCEN7	0	R/W	Zero Cross Mute Enable for Channel 7 This bit controls the operation of the zero cross mute function for channel 7. 0: Disables the operation of the zero cross mute function 1: Enables the operation of the zero cross mute function
6	ZCEN6	0	R/W	Zero Cross Mute Enable for Channel 6 This bit controls the operation of the zero cross mute function for channel 6. 0: Disables the operation of the zero cross mute function 1: Enables the operation of the zero cross mute function
5	ZCEN5	0	R/W	Zero Cross Mute Enable for Channel 5 This bit controls the operation of the zero cross mute function for channel 5. 0: Disables the operation of the zero cross mute function 1: Enables the operation of the zero cross mute function
4	ZCEN4	0	R/W	Zero Cross Mute Enable for Channel 4 This bit controls the operation of the zero cross mute function for channel 4. 0: Disables the operation of the zero cross mute function 1: Enables the operation of the zero cross mute function
3	ZCEN3	0	R/W	Zero Cross Mute Enable for Channel 3 This bit controls the operation of the zero cross mute function for channel 3. 0: Disables the operation of the zero cross mute function 1: Enables the operation of the zero cross mute function

Bit	Bit Name	Initial Value	R/W	Description
2	ZCEN2	0	R/W	Zero Cross Mute Enable for Channel 2 This bit controls the operation of the zero cross mute function for channel 2. 0: Disables the operation of the zero cross mute function 1: Enables the operation of the zero cross mute function
1	ZCEN1	0	R/W	Zero Cross Mute Enable for Channel 1 This bit controls the operation of the zero cross mute function for channel 1. 0: Disables the operation of the zero cross mute function 1: Enables the operation of the zero cross mute function
0	ZCEN0	0	R/W	Zero Cross Mute Enable for Channel 0 This bit controls the operation of the zero cross mute function for channel 0. 0: Disables the operation of the zero cross mute function 1: Enables the operation of the zero cross mute function

### 34.2.80 DVCp Volume Ramp Control Register (DVCp\_VRCTR)

Note: p = 0 or 1

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: DVCp\_VRCTR is a 32-bit readable/writable register that controls the operation of the volume ramp function for each channel.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	VREN7	VREN6	VREN5	VREN4	VREN3	VREN2	VREN1	VREN0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7	VREN7	0	R/W	Volume Ramp Enable for Channel 7 This bit controls the operation of the volume ramp function for channel 7. 0: Disables the operation of the volume ramp function 1: Enables the operation of the volume ramp function
6	VREN6	0	R/W	Volume Ramp Enable for Channel 6 This bit controls the operation of the volume ramp function for channel 6. 0: Disables the operation of the volume ramp function 1: Enables the operation of the volume ramp function
5	VREN5	0	R/W	Volume Ramp Enable for Channel 5 This bit controls the operation of the volume ramp function for channel 5. 0: Disables the operation of the volume ramp function 1: Enables the operation of the volume ramp function
4	VREN4	0	R/W	Volume Ramp Enable for Channel 4 This bit controls the operation of the volume ramp function for channel 4. 0: Disables the operation of the volume ramp function 1: Enables the operation of the volume ramp function
3	VREN3	0	R/W	Volume Ramp Enable for Channel 3 This bit controls the operation of the volume ramp function for channel 3. 0: Disables the operation of the volume ramp function 1: Enables the operation of the volume ramp function
2	VREN2	0	R/W	Volume Ramp Enable for Channel 2 This bit controls the operation of the volume ramp function for channel 2. 0: Disables the operation of the volume ramp function 1: Enables the operation of the volume ramp function

Bit	Bit Name	Initial Value	R/W	Description
1	VREN1	0	R/W	Volume Ramp Enable for Channel 1 This bit controls the operation of the volume ramp function for channel 1. 0: Disables the operation of the volume ramp function 1: Enables the operation of the volume ramp function
0	VREN0	0	R/W	Volume Ramp Enable for Channel 0 This bit controls the operation of the volume ramp function for channel 0. 0: Disables the operation of the volume ramp function 1: Enables the operation of the volume ramp function

Note: All of these bits should be set to 1 when VRMD bit of DVCp\_DVUCR register is 1.



**34.2.81 DVCp Volume Ramp Period Register (DVCp\_VRPDR)**

Note: p = 0 or 1

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: DVCp\_VRPDR is a 32-bit readable/writable register that controls.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	VRPDUP[4:0]				—	—	—	VRPDDW[4:0]					
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
12 to 8	VRPDUP[4:0]	00000	R/W	Volume Ramp Period for Volume Up 00000: 1 [sample] (128 dB/1 step) 00001: 2 [sample] (64 dB/1 step) 00010: 4 [sample] (32 dB/1 step) 00011: 8 [sample] (16 dB/1 step) 00100: 16 [sample] (8 dB/1 step) 00101: 32 [sample] (4 dB/1 step) 00110: 64 [sample] (2 dB/1 step) 00111: 128 [sample] (1 dB/1 step) 01000: 256 [sample] (0.5 dB/1 step) 01001: 512 [sample] (0.25 dB/1 step) 01010: 1024 [sample] (0.125 dB/1 step) 01011: 2048 [sample] (0.125 dB/2 steps) 01100: 4096 [sample] (0.125 dB/4 steps) 01101: 8192 [sample] (0.125 dB/8 steps) 01110: 16384 [sample] (0.125 dB/16 steps) 01111: 32768 [sample] (0.125 dB/32 steps) 10000: 65536 [sample] (0.125 dB/64 steps) 10001: 131072 [sample] (0.125 dB/128 steps) 10010: 262144 [sample] (0.125 dB/256 steps) 10011: 524288 [sample] (0.125 dB/512 steps) 10100: 1048576 [sample] (0.125 dB/1024 steps) 10101: 2097152 [sample] (0.125 dB/2048 steps) 10110: 4194304 [sample] (0.125 dB/4096 steps) 10111: 8388608 [sample] (0.125 dB/8192 steps) 11000 to 11111: Reserved
7 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

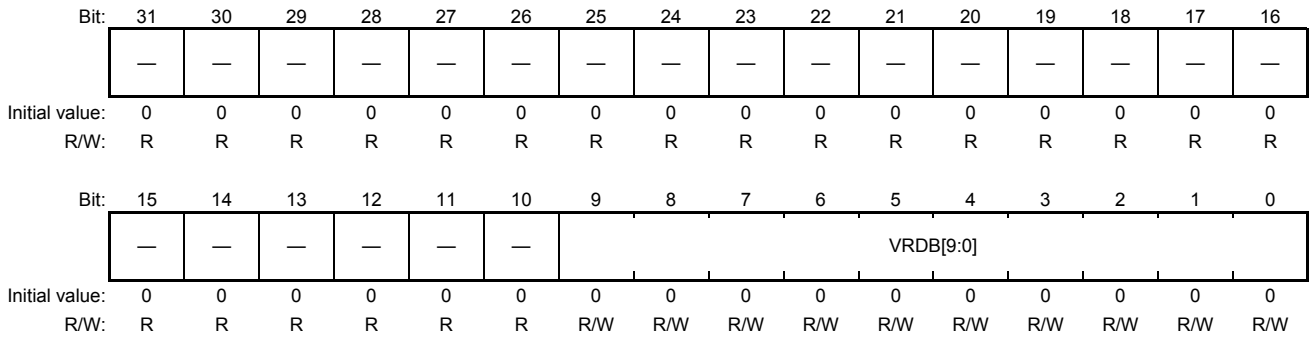
Bit	Bit Name	Initial Value	R/W	Description
4 to 0	VRPDDW[4:0]	00000	R/W	Volume Ramp Period for Volume Down
				00000: 1 [sample] (-128 dB/1 step)
				00001: 2 [sample] (-64 dB/1 step)
				00010: 4 [sample] (-32 dB/1 step)
				00011: 8 [sample] (-16 dB/1 step)
				00100: 16 [sample] (-8 dB/1 step)
				00101: 32 [sample] (-4 dB/1 step)
				00110: 64 [sample] (-2 dB/1 step)
				00111: 128 [sample] (-1 dB/1 step)
				01000: 256 [sample] (-0.5 dB/1 step)
				01001: 512 [sample] (-0.25 dB/1 step)
				01010: 1024 [sample] (-0.125 dB/1 step)
				01011: 2048 [sample] (-0.125 dB/2 steps)
				01100: 4096 [sample] (-0.125 dB/4 steps)
				01101: 8192 [sample] (-0.125 dB/8 steps)
				01110: 16384 [sample] (-0.125 dB/16 steps)
				01111: 32768 [sample] (-0.125 dB/32 steps)
				10000: 65536 [sample] (-0.125 dB/64 steps)
				10001: 131072 [sample] (-0.125 dB/128 steps)
				10010: 262144 [sample] (-0.125 dB/256 steps)
				10011: 524288 [sample] (-0.125 dB/512 steps)
				10100: 1048576 [sample] (-0.125 dB/1024 steps)
				10101: 2097152 [sample] (-0.125 dB/2048 steps)
				10110: 4194304 [sample] (-0.125 dB/4096 steps)
				10111: 8388608 [sample] (-0.125 dB/8192 steps)
				11000 to 11111: Reserved

**34.2.82 DVCp Volume Ramp Decibel Register (DVCp\_VRDBR)**

Note: p = 0 or 1

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: DVCp\_VRDBR is a 32-bit readable/writable register that sets the decibel (gain level) of volume ramp.



Bit	Bit Name	Initial Value	R/W	Description
31 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9 to 0	VRDB[9:0]	All 0	R/W	dB of Volume Ramp These bits control the decibel (gain level) of volume ramp. The value can select 1024 points from 0 dB to $-\infty$ dB at intervals of 0.125 dB.

Value	[time]	[dB]	Value	[time]	[dB]
H'000	1	0	.....	.....	.....
.....	.....	.....	H'091	0.125	-18.125
H'031	0.5	-6.125	.....	.....	.....
.....	.....	.....	H'3FE	$4.1 \times 10^{-7}$	-127.75
H'061	0.25	-12.125	H'3FF	0 (Mute)	$-\infty$

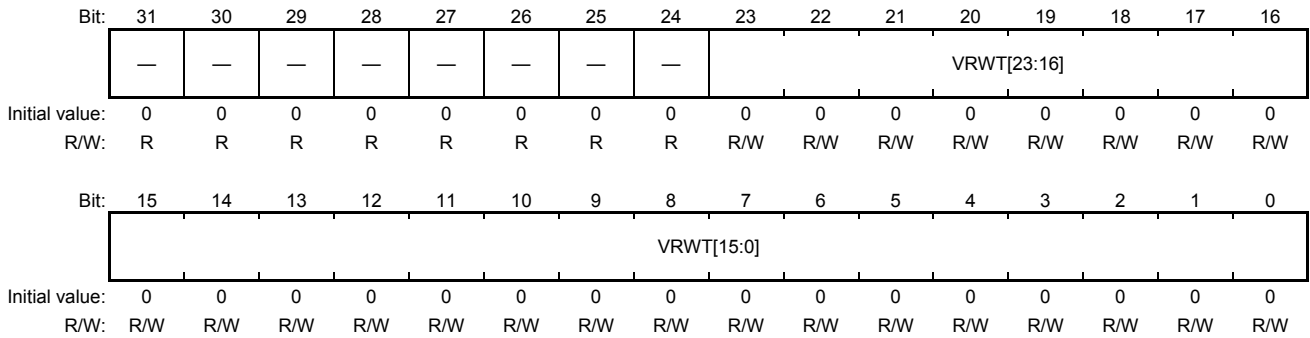
The relation between the setting value and the decibel is shown in Tables 34.9, 34.10, 34.11 and 34.12.

**34.2.83 DVCp Volume Ramp Wait Time Register (DVCp\_VRWTR)**

Note: p = 0 or 1

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: DVCp\_VRWTR is a 32-bit readable/writable register that sets the standby time to start the operation of the volume ramp function.



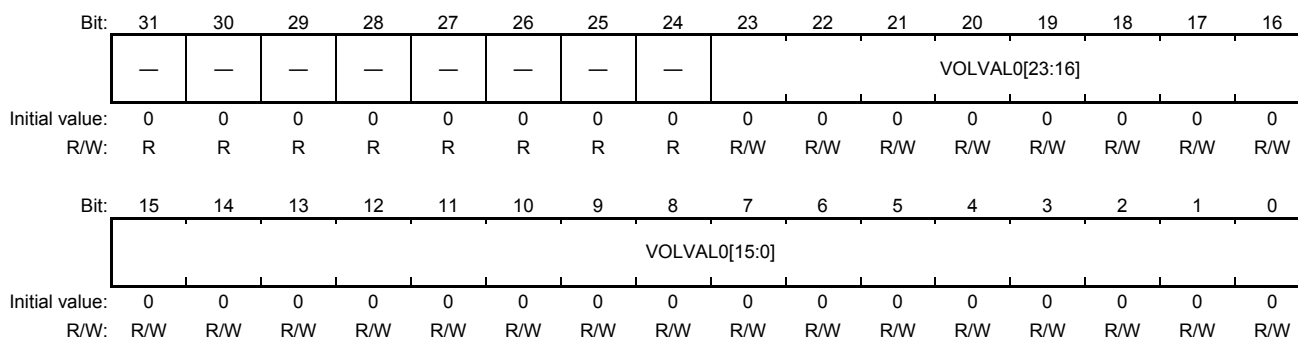
Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	VRWT[23:0]	H'00 0000	R/W	Volume Ramp Wait Time These bits set the standby time to adjust the start timing of operation of the volume ramp function when the setting of DVCp_VRDBR register is changed. If the internal counter of the DVC logic reached to the value of these bits, the volume ramp function starts to operate to change the volume to target volume of DVCp_VRDBR register.

### 34.2.84 DVCp Volume Value Setting 0 Register (DVCp\_VOL0R)

Note: p = 0 or 1

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: DVCp\_VOL0R is a 32-bit readable/writable register that sets digital volume value for channel 0.



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	VOLVAL0 [23:0]	H'00_0000	R/W	Digital Volume Value for Channel 0 These bits set the digital volume of channel 0. The maximum value is 8-time (18 dB) and the minimum value is 0 (-∞ dB). VOLVAL0[23]: Sign bit (The write value should be 0.) VOLVAL0[22:20]: Integer bits VOLVAL0[19:0]: Decimal bits

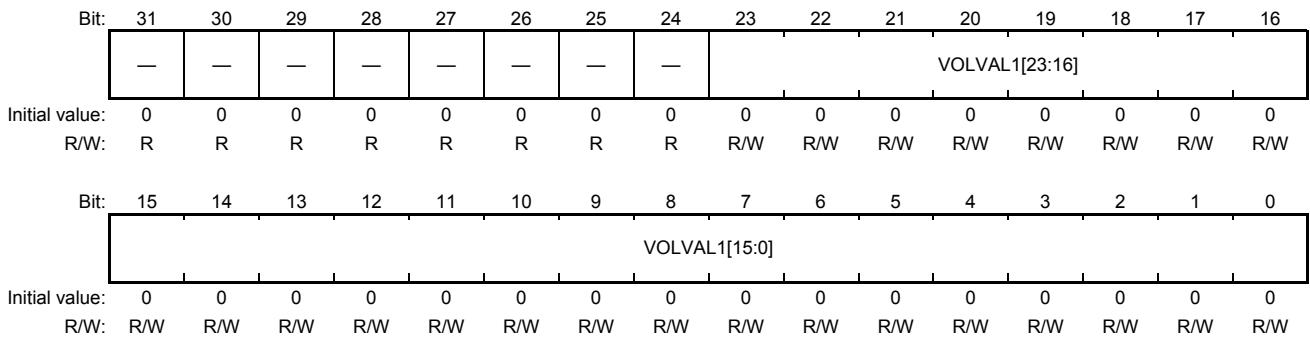
Value	[time]	[dB]	Value	[time]	[dB]
H'7F_FFFF	8	18	H'08_0000	0.5	-6
...	...	...	...	...	...
H'10_0000	1	0	H'00_0001	$9.5 \times 10^{-7}$	-120
...	...	...	H'00_0000	0	-∞

**34.2.85 DVCp Volume Value Setting 1 Register (DVCp\_VOL1R)**

Note: p = 0 or 1

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: DVCp\_VOL1R is a 32-bit readable/writable register that sets digital volume value for channel 1.



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	VOLVAL1 [23:0]	H'00 0000	R/W	Digital Volume Value for Channel 1 These bits set the digital volume of channel 1. The maximum value is 8-time (18 dB) and the minimum value is 0 (-∞ dB). VOLVAL1[23]: Sign bit (The write value should be 0.) VOLVAL1[22:20]: Integer bits VOLVAL1[19:0]: Decimal bits

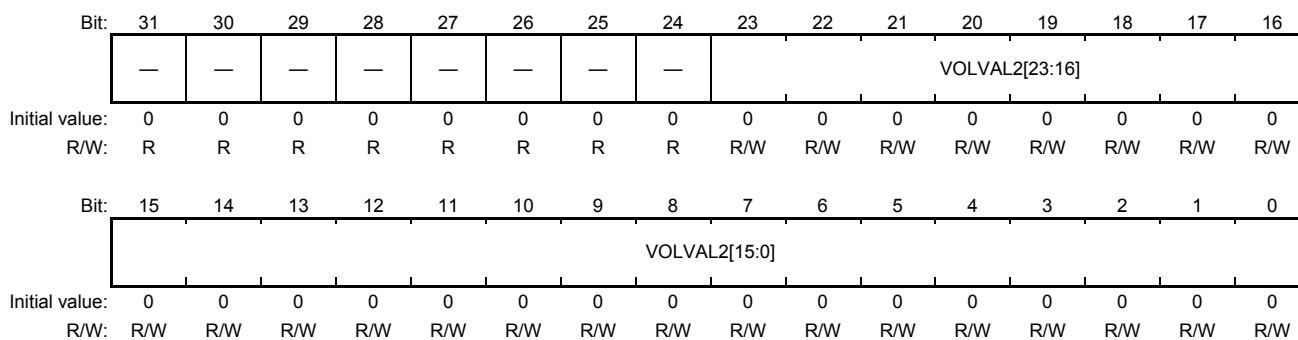
Value	[time]	[dB]	Value	[time]	[dB]
H'7F_FFFF	8	18	H'08_0000	0.5	-6
...	...	...	...	...	...
H'10_0000	1	0	H'00_0001	$9.5 \times 10^{-7}$	-120
...	...	...	H'00_0000	0	-∞

### 34.2.86 DVCp Volume Value Setting 2 Register (DVCp\_VOL2R)

Note: p = 0 or 1

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: DVCp\_VOL2R is a 32-bit readable/writable register that sets digital volume value for channel 2.



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	VOLVAL2 [23:0]	H'00 0000	R/W	Digital Volume Value for Channel 2 These bits set the digital volume of channel 2. The maximum value is 8-time (18 dB) and the minimum value is 0 (-∞ dB). VOLVAL2[23]: Sign bit (The write value should be 0.) VOLVAL2[22:20]: Integer bits VOLVAL2[19:0]: Decimal bits

Value	[time]	[dB]	Value	[time]	[dB]
H'7F_FFFF	8	18	H'08_0000	0.5	-6
...	...	...	...	...	...
H'10_0000	1	0	H'00_0001	$9.5 \times 10^{-7}$	-120
...	...	...	H'00_0000	0	-∞

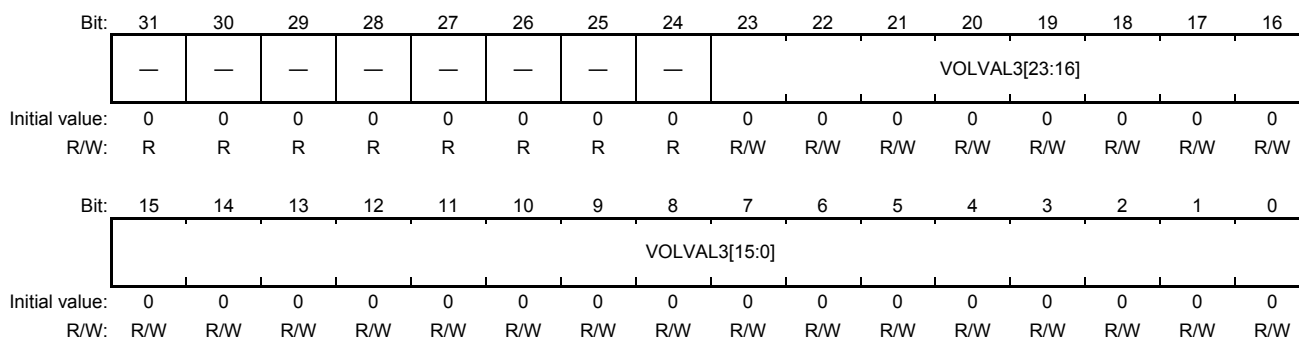


### 34.2.87 DVCp Volume Value Setting 3 Register (DVCp\_VOL3R)

Note: p = 0 or 1

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: DVCp\_VOL3R is a 32-bit readable/writable register that sets digital volume value for channel 3.



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	VOLVAL3 [23:0]	H'00 0000	R/W	Digital Volume Value for Channel 3 These bits set the digital volume of channel 3. The maximum value is 8-time (18 dB) and the minimum value is 0 (-∞ dB). VOLVAL3[23]: Sign bit (The write value should be 0.) VOLVAL3[22:20]: Integer bits VOLVAL3[19:0]: Decimal bits

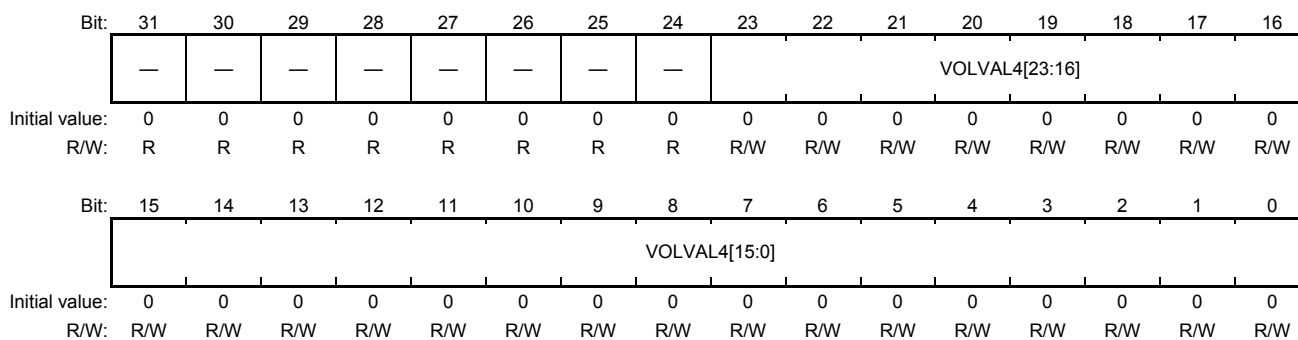
Value	[time]	[dB]	Value	[time]	[dB]
H'7F_FFFF	8	18	H'08_0000	0.5	-6
...	...	...	...	...	...
H'10_0000	1	0	H'00_0001	$9.5 \times 10^{-7}$	-120
...	...	...	H'00_0000	0	-∞

### 34.2.88 DVCp Volume Value Setting 4 Register (DVCp\_VOL4R)

Note: p = 0 or 1

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: DVCp\_VOL4R is a 32-bit readable/writable register that sets digital volume value for channel 4.



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	VOLVAL4 [23:0]	H'00 0000	R/W	Digital Volume Value for Channel 4 These bits set the digital volume of channel 4. The maximum value is 8-time (18 dB) and the minimum value is 0 (-∞ dB). VOLVAL4[23]: Sign bit (The write value should be 0.) VOLVAL4[22:20]: Integer bits VOLVAL4[19:0]: Decimal bits

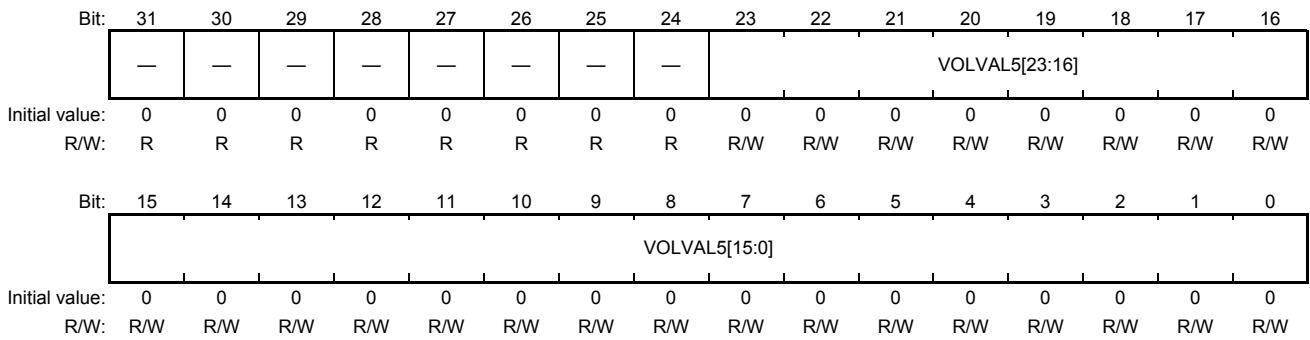
Value	[time]	[dB]	Value	[time]	[dB]
H'7F_FFFF	8	18	H'08_0000	0.5	-6
...	...	...	...	...	...
H'10_0000	1	0	H'00_0001	$9.5 \times 10^{-7}$	-120
...	...	...	H'00_0000	0	-∞

**34.2.89 DVCp Volume Value Setting 5 Register (DVCp\_VOL5R)**

Note: p = 0 or 1

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: DVCp\_VOL5R is a 32-bit readable/writable register that sets digital volume value for channel 5.



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	VOLVAL5 [23:0]	H'00 0000	R/W	Digital Volume Value for Channel 5 These bits set the digital volume of channel 5. The maximum value is 8-time (18 dB) and the minimum value is 0 (-∞ dB). VOLVAL5[23]: Sign bit (The write value should be 0.) VOLVAL5[22:20]: Integer bits VOLVAL5[19:0]: Decimal bits

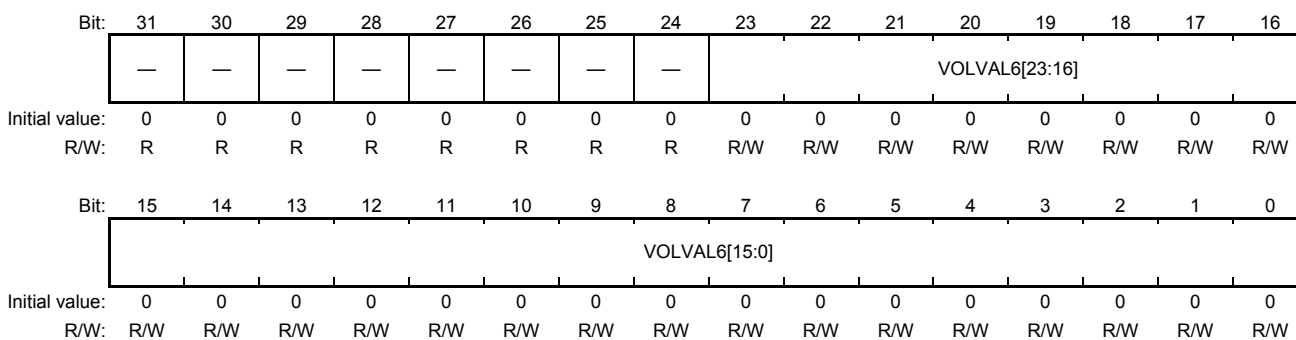
Value	[time]	[dB]	Value	[time]	[dB]
H'7F_FFFF	8	18	H'08_0000	0.5	-6
...	...	...	...	...	...
H'10_0000	1	0	H'00_0001	$9.5 \times 10^{-7}$	-120
...	...	...	H'00_0000	0	-∞

### 34.2.90 DVCp Volume Value Setting 6 Register (DVCp\_VOL6R)

Note: p = 0 or 1

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: DVCp\_VOL6R is a 32-bit readable/writable register that sets digital volume value for channel 6.



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	VOLVAL6 [23:0]	H'00 0000	R/W	Digital Volume Value for Channel 6 These bits set the digital volume of channel 6. The maximum value is 8-time (18 dB) and the minimum value is 0 (-∞ dB). VOLVAL6[23]: Sign bit (The write value should be 0.) VOLVAL6[22:20]: Integer bits VOLVAL6[19:0]: Decimal bits

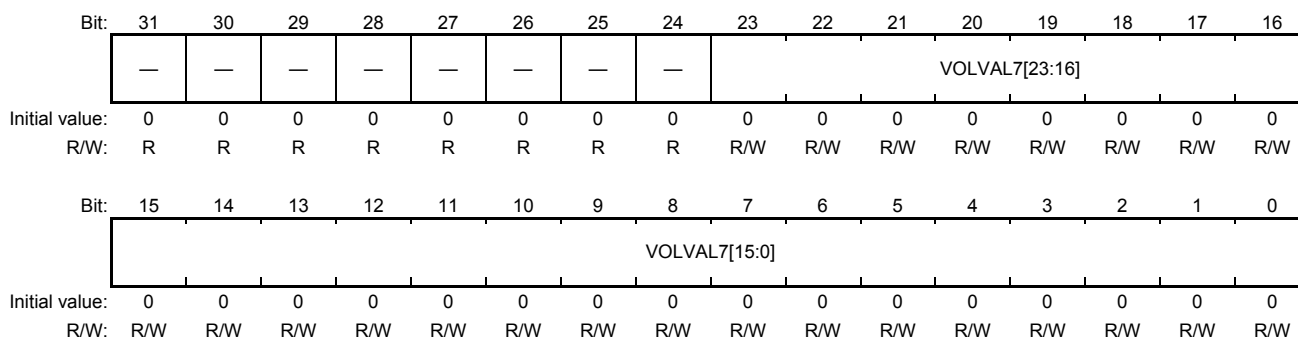
Value	[time]	[dB]	Value	[time]	[dB]
H'7F_FFFF	8	18	H'08_0000	0.5	-6
...	...	...	...	...	...
H'10_0000	1	0	H'00_0001	$9.5 \times 10^{-7}$	-120
...	...	...	H'00_0000	0	-∞

### 34.2.91 DVCp Volume Value Setting 7 Register (DVCp\_VOL7R)

Note: p = 0 or 1

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: DVCp\_VOL7R is a 32-bit readable/writable register that sets digital volume value for channel 7.



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	VOLVAL7 [23:0]	H'00 0000	R/W	Digital Volume Value for Channel 7 These bits set the digital volume of channel 7. The maximum value is 8-time (18 dB) and the minimum value is 0 (-∞ dB). VOLVAL7[23]: Sign bit (The write value should be 0.) VOLVAL7[22:20]: Integer bits VOLVAL7[19:0]: Decimal bits

Value	[time]	[dB]	Value	[time]	[dB]
H'7F_FFFF	8	18	H'08_0000	0.5	-6
...	...	...	...	...	...
H'10_0000	1	0	H'00_0001	$9.5 \times 10^{-7}$	-120
...	...	...	H'00_0000	0	-∞

**34.2.92 DVCp DVU Enable Register (DVCp\_DVUER)**

Note: p = 0 or 1

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: DVCp\_DVUER is a 32-bit readable/writable register that controls the setting of DVC registers.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DVCEN
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	DVCEN	0	R/W	DVC Register Setting Enable This bit controls the setting of DVC registers (DVCp_ZCMCR, DVCp_VRCTR, DVCp_VRPDR, DVCp_VRDBR, DVCp_VOL0R, DVCp_VOL1R, DVCp_VOL2R, DVCp_VOL3R, DVCp_VOL4R, DVCp_VOL5R, DVCp_VOL6R, DVCp_VOL7R ). 0: Disables the setting of dvc registers to DVC logic 1: Enables the setting of dvc registers to DVC logic

**34.2.93 DVCp DVU Status Register (DVCp\_DVUSR)**

Note: p = 0, 1

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: DVCp\_DVUSR is a 32-bit readable register that indicates the status of the zero cross mute and the volume ramp. This register is used for debug.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	ALLZS TS	ZSTS7	ZSTS6	ZSTS5	ZSTS4	ZSTS3	ZSTS2	ZSTS1	ZSTS0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	VRSTS_ LEVEL	VRSTS_ MUTE	VRSTS[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 25	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
24	ALLZSTS	0	R	All-Channel Zero Cross Mute Status 0: Not all-channel zero cross mute state 1: All-channel zero cross mute state Note: The state is determined only based on the channels for which the zero cross mute function is set.
23	ZSTS7	0	R	Zero Cross Mute Status of Channel 7 This bit indicates the zero cross mute status of channel 7. 0: Not mute status 1: Mute status
22	ZSTS6	0	R	Zero Cross Mute Status of Channel 6 This bit indicates the zero cross mute status of channel 6. 0: Not mute status 1: Mute status
21	ZSTS5	0	R	Zero Cross Mute Status of Channel 5 This bit indicates the zero cross mute status of channel 5. 0: Not mute status 1: Mute status
20	ZSTS4	0	R	Zero Cross Mute Status of Channel 4 This bit indicates the zero cross mute status of channel 4. 0: Not mute status 1: Mute status
19	ZSTS3	0	R	Zero Cross Mute Status of Channel 3 This bit indicates the zero cross mute status of channel 3. 0: Not mute status 1: Mute status

Bit	Bit Name	Initial Value	R/W	Description
18	ZSTS2	0	R	Zero Cross Mute Status of Channel 2 This bit indicates the zero cross mute status of channel 2. 0: Not mute status 1: Mute status
17	ZSTS1	0	R	Zero Cross Mute Status of Channel 1 This bit indicates the zero cross mute status of channel 1. 0: Not mute status 1: Mute status
16	ZSTS0	0	R	Zero Cross Mute Status of Channel 0 This bit indicates the zero cross mute status of channel 0. 0: Not mute status 1: Mute status
15 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	VRSTS_LEVEL	0	R	Volume Ramp Level Status 0: The volume ramp level is not the level specified by the DVCp_VRDBR register. (VRSTS is not 011.) 1: The volume ramp level is the level specified by the DVCp_VRDBR register. (VRSTS is 011.)
3	VRSTS_MUTE	1	R	Volume Ramp Mute Status 0: Not mute status 1: Mute status
2 to 0	VRSTS[2:0]	000	R	Volume Ramp Status These bits indicate the volume ramp status. 000: Mute status 001: Volume ramp down 010: Volume ramp up 011: The volume ramp level is not the level specified by the DVCp_VRDBR register. 100: Volume of input data is maintained (Volume is 1-time) 101~111: Reserved bits



### 34.2.94 DVCp Interrupt Enable Register (DVCp\_DVIER)

Note: p = 0, 1

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: DVCp\_DVIER enables or disables output of interrupts corresponding to the states indicated in the DVCp\_DVUSR register.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	ALLZS TS_ie	ZSTS7 _ie	ZSTS6 _ie	ZSTS5 _ie	ZSTS4 _ie	ZSTS3 _ie	ZSTS2 _ie	ZSTS1 _ie	ZSTS0 _ie
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	VRSTS_L EVEL_ie	VRSTS_M UTE_ie	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 25	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
24	ALLZSTS_ie	0	R/W	allzsts_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
23	ZSTS7_ie	0	R/W	zsts7_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
22	ZSTS6_ie	0	R/W	zsts6_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
21	ZSTS5_ie	0	R/W	zsts5_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
20	ZSTS4_ie	0	R/W	zsts4_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
19	ZSTS3_ie	0	R/W	zsts3_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
18	ZSTS2_ie	0	R/W	zsts2_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
17	ZSTS1_ie	0	R/W	zsts1_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.

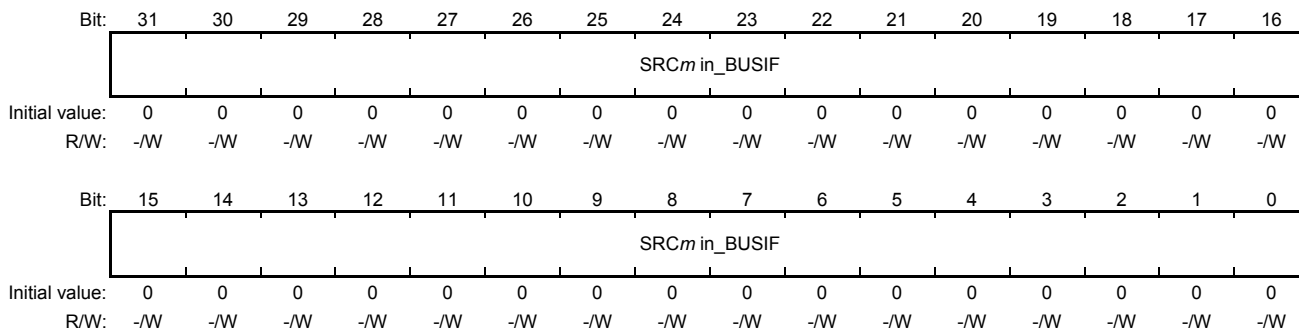
Bit	Bit Name	Initial Value	R/W	Description
16	ZSTS0_ie	0	R/W	zsts0_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
15 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	VRSTS_LEVEL_ie	0	R/W	vrsts_level_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
3	VRSTS_MUTE_ie	0	R/W	vrsts_mute_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
2 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

**34.2.95 SRCm in Write Data Register (SRCm in\_BUSIF)**

Note: RZ/G1H, M and N: m = 0 to 9, RZ/G1E: m = 1 to 6

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: SRCm in\_BUSIF are window registers in which data is stored during data transfer via SRCm in\_BUSIF. These registers are used for transmission.



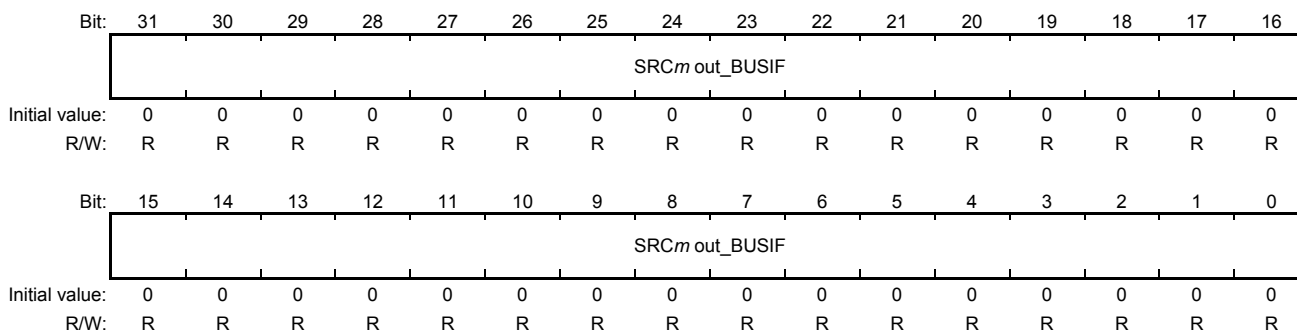
Bit	Bit Name	Initial Value	R/W	Description
31 to 0	SRCm in_BUSIF	All 0	-W	These bits are a window register in which data is stored during data transfer via SRCm in_BUSIF. This register is used for transmission.

### 34.2.96 SRCm out Read Data Register (SRCm out\_BUSIF)

Note: RZ/G1H, M and N: m = 0 to 9, RZ/G1E: m = 1 to 6

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: SRCm out\_BUSIF are window registers in which data is stored during data transfer via SRCm out\_BUSIF. These registers are used for reception.



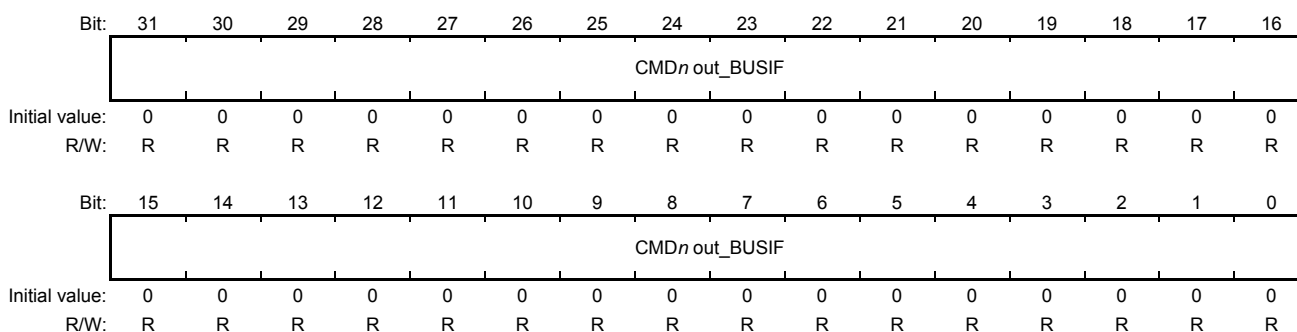
Bit	Bit Name	Initial Value	R/W	Description
31 to 0	SRCm out_BUSIF	All 0	R	These bits are a window register in which data is stored during data transfer via SRCm out_BUSIF. This register is used for reception.

### 34.2.97 CMDn out Read Data Register (CMDn out\_BUSIF)

Note: n = 0 or 1

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: CMDn out\_BUSIF are window registers in which data is stored during data transfer via CMDn out\_BUSIF. These registers are used for reception.



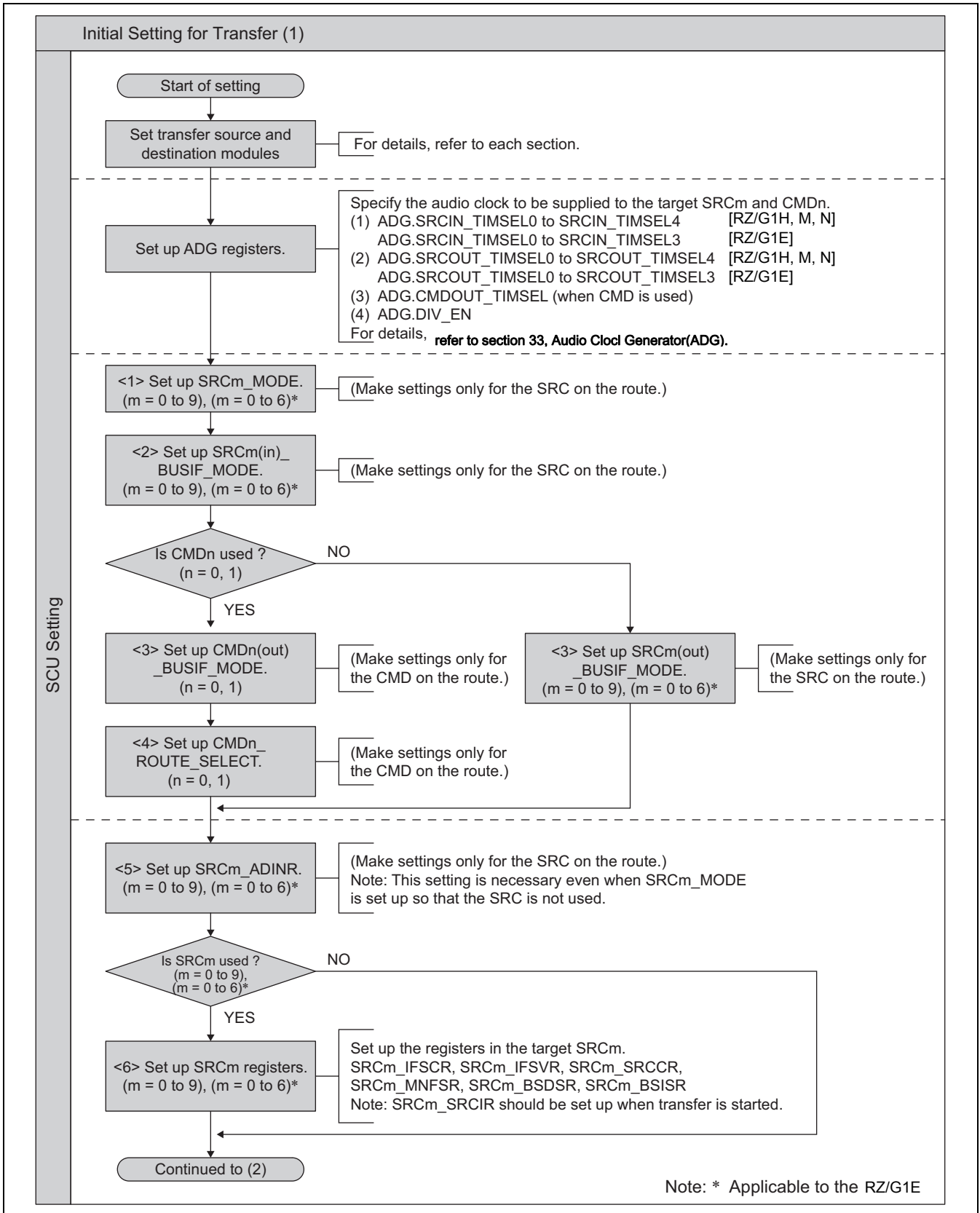
Bit	Bit Name	Initial Value	R/W	Description
31 to 0	CMDn out_BUSIF	All 0	R	These bits are a window register in which data is stored during data transfer via CMDn out_BUSIF. This register is used for reception.

### 34.3 SCU Operation

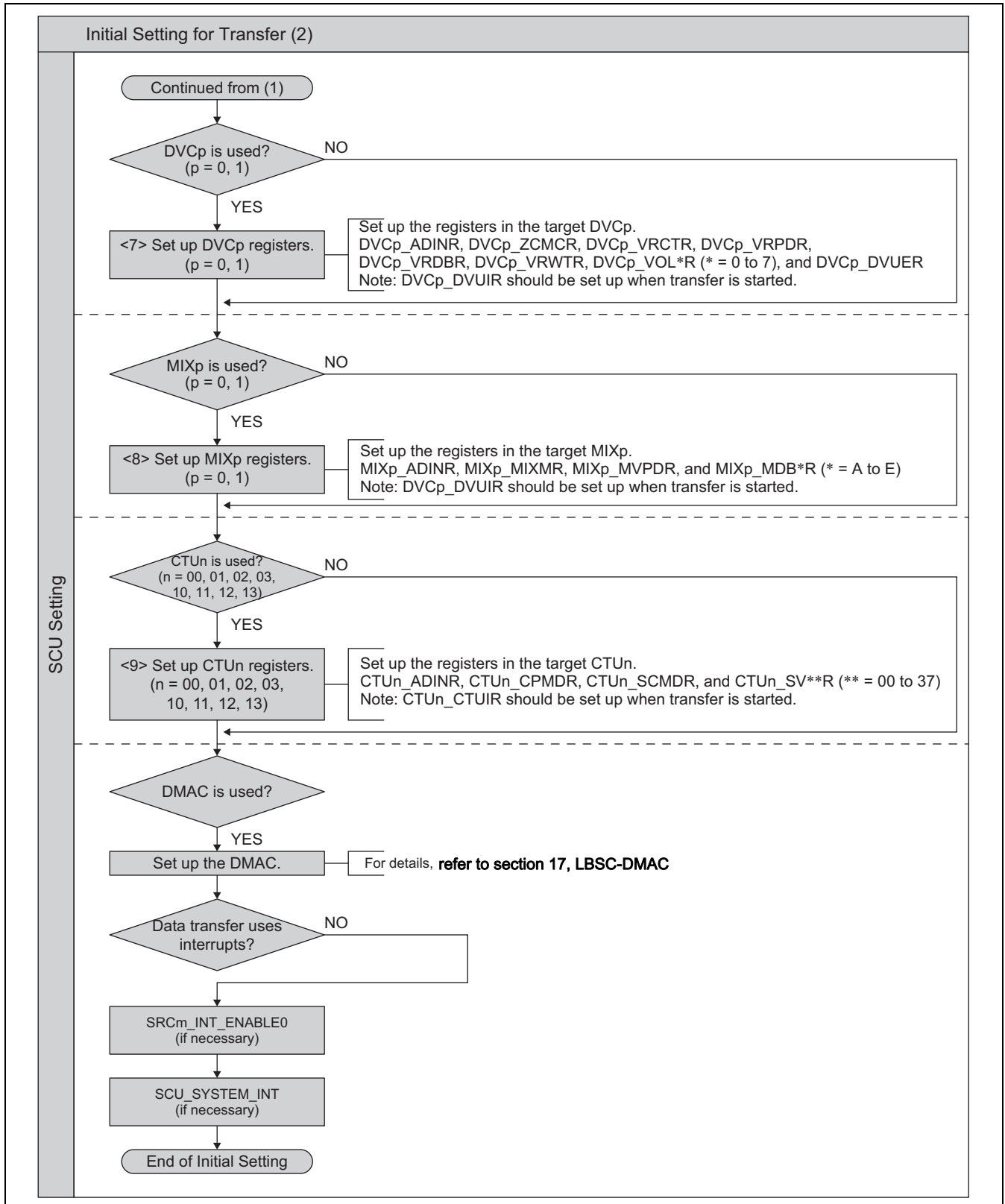
RZ/G1H	RZ/G1N
RZ/G1M	RZ/G1E

#### 34.3.1 Procedure for Initializing the SCU

Figures 34.2 and 34.3 show the procedure for initializing the SCU. For details on the register settings, refer to section 34.2, Register Description.



**Figure 34.2 Procedure for Initializing the SCU (1)**



**Figure 34.3 Procedure for Initializing the SCU (2)**

### 34.3.2 Procedure for Starting and Stopping Transfer by the SCU

Figure 34.4 shows the procedure for starting and stopping the transfer by the SCU. For details on the register settings, refer to section 34.2, Register Description.

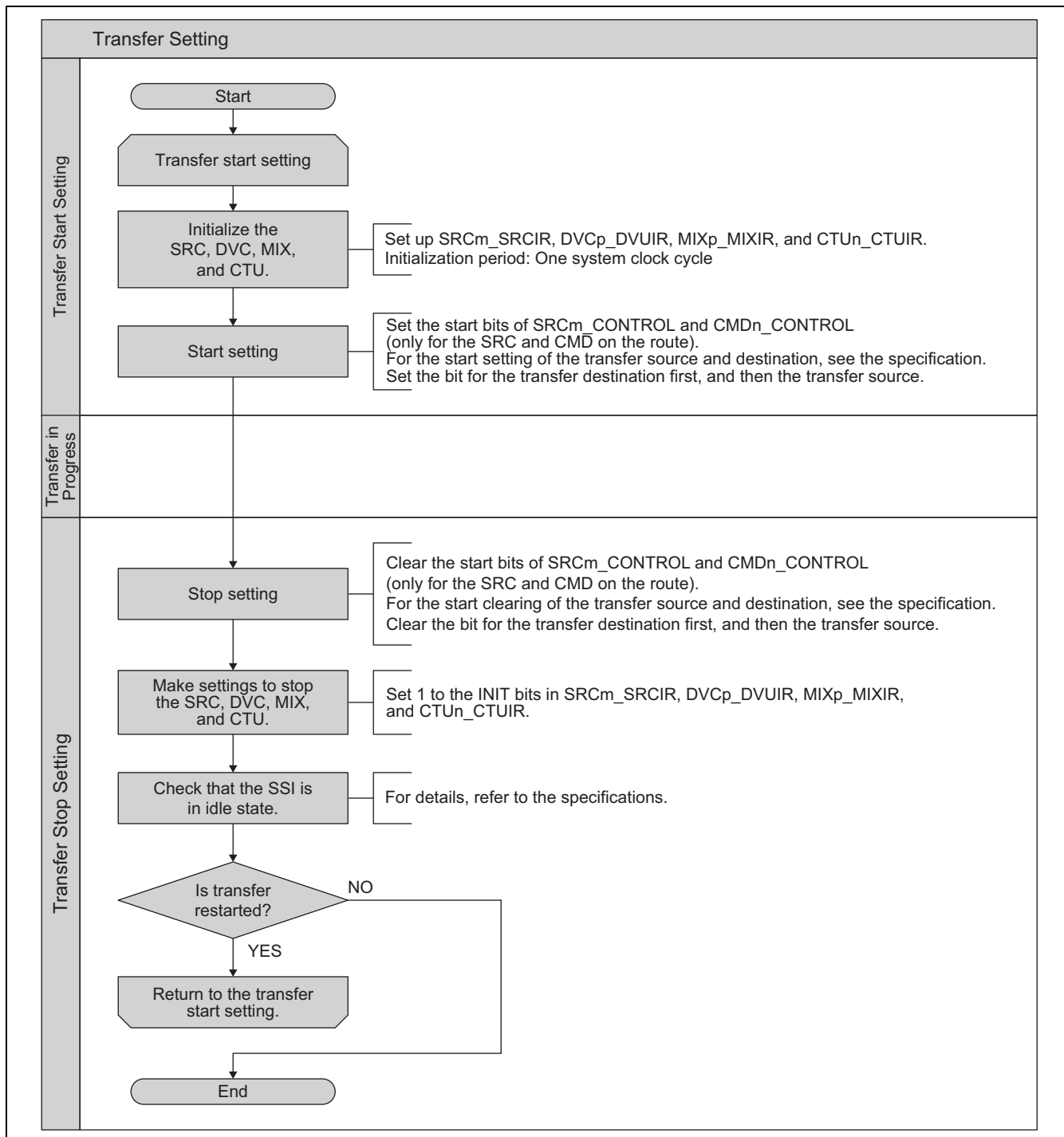


Figure 34.4 Procedure for Starting and Stopping Transfer by the SCU

### 34.3.3 Data Format for Data Transfer BUSIF

Table 34.3 shows the data formats handled in the SCU. When writing or reading data through the data transfer BUSIF (SRCm in\_BUSIF, SRCm out\_BUSIF, or CMDn out\_BUSIF), align data to match the appropriate data format from those in Table 34.3. Data alignment can be changed through the SRCm(in/out)\_BUSIF\_MODE, SRCm\_MODE register or CMDnout\_BUSIF\_MODE register (see section 34.2.4, SRCm\_MODE Register (SRCm\_MODE) or section 34.2.10, CMDn out\_BUSIF\_MODE Register (CMDn out\_BUSIF\_MODE)).

**Table 34.3 Data Formats Handled in the SCU**

24-bit stereo data, multichannel data	<div style="text-align: center;"> <span style="float: left;">31</span> <span style="float: right;">8 7 0</span>   <div style="border: 1px solid black; padding: 2px; width: 100%; display: flex; justify-content: space-between;"> <span>MSB</span> <span>LSB</span> <span style="background-color: #cccccc; padding: 0 5px;">x</span> <span style="background-color: #cccccc; padding: 0 5px;">x</span> <span style="background-color: #cccccc; padding: 0 5px;">x</span> <span style="background-color: #cccccc; padding: 0 5px;">x</span> </div> </div>
17- to 23-bit stereo data, multichannel data	<div style="text-align: center;"> <span style="float: left;">31</span> <span style="float: right;">? 0</span>   <div style="border: 1px solid black; padding: 2px; width: 100%; display: flex; justify-content: space-between;"> <span>MSB</span> <span>LSB</span> <span style="background-color: #cccccc; padding: 0 5px;">x</span> <span style="background-color: #cccccc; padding: 0 5px;">x</span> <span style="background-color: #cccccc; padding: 0 5px;">x</span> <span style="background-color: #cccccc; padding: 0 5px;">x</span> <span style="background-color: #cccccc; padding: 0 5px;">x</span> <span style="background-color: #cccccc; padding: 0 5px;">x</span> </div> </div>
16-bit stereo data, multichannel data	<div style="text-align: center;"> <span style="float: left;">31</span> <span style="float: right;">16 15 0</span>   <div style="border: 1px solid black; padding: 2px; width: 100%; display: flex; justify-content: space-between;"> <span>MSB</span> <span>LSB</span> <span>MSB</span> <span>LSB</span> </div> <div style="display: flex; justify-content: space-around; margin-top: 5px;"> <span>(Lch)</span> <span>(Rch)</span> </div> </div>
9- to 15-bit stereo data, multichannel data	<div style="text-align: center;"> <span style="float: left;">31</span> <span style="float: right;">? 16 15 ? 0</span>   <div style="border: 1px solid black; padding: 2px; width: 100%; display: flex; justify-content: space-between;"> <span>MSB</span> <span>LSB</span> <span style="background-color: #cccccc; padding: 0 5px;">x</span> <span style="background-color: #cccccc; padding: 0 5px;">x</span> <span>MSB</span> <span>LSB</span> <span style="background-color: #cccccc; padding: 0 5px;">x</span> <span style="background-color: #cccccc; padding: 0 5px;">x</span> </div> <div style="display: flex; justify-content: space-around; margin-top: 5px;"> <span>(Lch)</span> <span>(Rch)</span> </div> </div>
8-bit stereo data	<div style="text-align: center;"> <span style="float: left;">31</span> <span style="float: right;">24 23 16 15 8 7 0</span>   <div style="border: 1px solid black; padding: 2px; width: 100%; display: flex; justify-content: space-between;"> <span>MSB</span> <span>MSB</span> <span>MSB</span> <span>MSB</span> <span>MSB</span> <span>MSB</span> <span>MSB</span> <span>MSB</span> </div> <div style="display: flex; justify-content: space-around; margin-top: 5px;"> <span>(Rch/2)</span> <span>(Lch/2)</span> <span>(Rch/1)</span> <span>(Lch/1)</span> </div> </div>
16-bit monaural data	<div style="text-align: center;"> <span style="float: left;">31</span> <span style="float: right;">16 15 0</span>   <div style="border: 1px solid black; padding: 2px; width: 100%; display: flex; justify-content: space-between;"> <span>MSB</span> <span>MSB</span> <span style="background-color: #cccccc; padding: 0 5px;">x</span> <span style="background-color: #cccccc; padding: 0 5px;">x</span> <span style="background-color: #cccccc; padding: 0 5px;">x</span> <span style="background-color: #cccccc; padding: 0 5px;">x</span> <span style="background-color: #cccccc; padding: 0 5px;">x</span> <span style="background-color: #cccccc; padding: 0 5px;">x</span> <span style="background-color: #cccccc; padding: 0 5px;">x</span> <span style="background-color: #cccccc; padding: 0 5px;">x</span> <span style="background-color: #cccccc; padding: 0 5px;">x</span> </div> </div>
8-bit monaural data	<div style="text-align: center;"> <span style="float: left;">31</span> <span style="float: right;">24 23 16 15 0</span>   <div style="border: 1px solid black; padding: 2px; width: 100%; display: flex; justify-content: space-between;"> <span>MSB</span> <span>MSB</span> <span style="background-color: #cccccc; padding: 0 5px;">x</span> <span style="background-color: #cccccc; padding: 0 5px;">x</span> <span style="background-color: #cccccc; padding: 0 5px;">x</span> <span style="background-color: #cccccc; padding: 0 5px;">x</span> <span style="background-color: #cccccc; padding: 0 5px;">x</span> <span style="background-color: #cccccc; padding: 0 5px;">x</span> <span style="background-color: #cccccc; padding: 0 5px;">x</span> <span style="background-color: #cccccc; padding: 0 5px;">x</span> <span style="background-color: #cccccc; padding: 0 5px;">x</span> <span style="background-color: #cccccc; padding: 0 5px;">x</span> <span style="background-color: #cccccc; padding: 0 5px;">x</span> </div> </div>

- Notes:
1. Write 0 to the "x" bits in the table when writing data through the data transfer SRCm in\_BUSIF. When reading data through the SRCm out\_BUSIF or CMDn out\_BUSIF, ignore the values read from these bits.
  2. In the 8-bit stereo data format, (Lch/1) and (Rch/1) indicate the data pair to be processed first and (Lch/2) and (Rch/2) indicate the next data pair to be processed.
  3. Only the MSB-first data formats can be used in the SRU.



#### 34.3.4 Changing Data Order in Channel Units

The data order can be changed in channel units in the SCU immediately before input to the SRC and immediately after output from the CMD. Tables 34.3 and 34.4 show the data places in each data format. Use SRCm\_BUSIF\_DALIGN or SRCn\_BUSIF\_DALIGN to change the order before input to the SRC (see section 34.2.2, SRCm\_BUSIF\_DALIGN Register (SRCm\_BUSIF\_DALIGN) or section 34.2.3, SRCn\_BUSIF\_DALIGN Register (SRCn\_BUSIF\_DALIGN)). Use CMDn\_BUSIF\_DALIGN to change the order immediately after output from the CMD (see section 34.2.11, CMDn\_BUSIF\_DALIGN Register (CMDn\_BUSIF\_DALIGN)). Tables 34.3 and 34.4 show the data places when these registers are set to the initial values.

**Table 34.4 Data Places in Each Data Format (1)**

<p>BUSIF</p> <ul style="list-style-type: none"> <li>· Stereo (2 channels)</li> <li>· 24 bits</li> </ul>	<p>External memory image</p> <table style="margin-left: auto; margin-right: auto;"> <tr> <td></td> <td style="text-align: center;">31</td> <td></td> <td style="text-align: center;">0</td> </tr> <tr> <td>H'00</td> <td style="border: 1px solid black; text-align: center;">Place 0</td> <td style="border: 1px solid black; text-align: center;">*</td> <td></td> </tr> <tr> <td>H'04</td> <td style="border: 1px solid black; text-align: center;">Place 1</td> <td style="border: 1px solid black; text-align: center;">*</td> <td></td> </tr> <tr> <td>H'08</td> <td style="border: 1px solid black; text-align: center;">Place 0</td> <td style="border: 1px solid black; text-align: center;">*</td> <td></td> </tr> <tr> <td>H'0C</td> <td style="border: 1px solid black; text-align: center;">Place 1</td> <td style="border: 1px solid black; text-align: center;">*</td> <td></td> </tr> <tr> <td>...</td> <td style="border: 1px solid black; text-align: center;">...</td> <td style="border: 1px solid black; text-align: center;">*</td> <td></td> </tr> </table>		31		0	H'00	Place 0	*		H'04	Place 1	*		H'08	Place 0	*		H'0C	Place 1	*		...	...	*																	
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<p>BUSIF</p> <ul style="list-style-type: none"> <li>· Stereo (2 channels)</li> <li>· 16 bits</li> </ul>	<p>External memory image</p> <table style="margin-left: auto; margin-right: auto;"> <tr> <td></td> <td style="text-align: center;">31</td> <td></td> <td style="text-align: center;">0</td> </tr> <tr> <td>H'00</td> <td style="border: 1px solid black; text-align: center;">Place 0</td> <td style="border: 1px solid black; text-align: center;">Place 1</td> <td></td> </tr> <tr> <td>H'04</td> <td style="border: 1px solid black; text-align: center;">Place 0</td> <td style="border: 1px solid black; text-align: center;">Place 1</td> <td></td> </tr> <tr> <td>H'08</td> <td style="border: 1px solid black; text-align: center;">Place 0</td> <td style="border: 1px solid black; text-align: center;">Place 1</td> <td></td> </tr> <tr> <td>H'0C</td> <td style="border: 1px solid black; text-align: center;">Place 0</td> <td style="border: 1px solid black; text-align: center;">Place 1</td> <td></td> </tr> <tr> <td>...</td> <td style="border: 1px solid black; text-align: center;">...</td> <td style="border: 1px solid black; text-align: center;">...</td> <td></td> </tr> </table>		31		0	H'00	Place 0	Place 1		H'04	Place 0	Place 1		H'08	Place 0	Place 1		H'0C	Place 0	Place 1		...	...	...																	
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<p>BUSIF</p> <ul style="list-style-type: none"> <li>· Stereo (2 channels)</li> <li>· 8 bits</li> </ul>	<p>External memory image</p> <table style="margin-left: auto; margin-right: auto;"> <tr> <td></td> <td style="text-align: center;">31</td> <td></td> <td></td> <td style="text-align: center;">0</td> </tr> <tr> <td>H'00</td> <td style="border: 1px solid black; text-align: center;">Place 1</td> <td style="border: 1px solid black; text-align: center;">Place 0</td> <td style="border: 1px solid black; text-align: center;">Place 1</td> <td style="border: 1px solid black; text-align: center;">Place 0</td> </tr> <tr> <td>H'04</td> <td style="border: 1px solid black; text-align: center;">Place 1</td> <td style="border: 1px solid black; text-align: center;">Place 0</td> <td style="border: 1px solid black; text-align: center;">Place 1</td> <td style="border: 1px solid black; text-align: center;">Place 0</td> </tr> <tr> <td>...</td> <td style="border: 1px solid black; text-align: center;">...</td> <td style="border: 1px solid black; text-align: center;">...</td> <td style="border: 1px solid black; text-align: center;">...</td> <td style="border: 1px solid black; text-align: center;">...</td> </tr> </table>		31			0	H'00	Place 1	Place 0	Place 1	Place 0	H'04	Place 1	Place 0	Place 1	Place 0	...	...	...	...	...																				
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<p>BUSIF</p> <ul style="list-style-type: none"> <li>· Monaural (1 channel)</li> <li>· 8/16 bits</li> </ul>	<p>External memory image</p> <table style="margin-left: auto; margin-right: auto;"> <tr> <td></td> <td style="text-align: center;">31</td> <td></td> <td style="text-align: center;">0</td> </tr> <tr> <td>H'00</td> <td style="border: 1px solid black; text-align: center;">Place 0</td> <td style="border: 1px solid black; text-align: center;">*</td> <td></td> </tr> <tr> <td>H'04</td> <td style="border: 1px solid black; text-align: center;">Place 0</td> <td style="border: 1px solid black; text-align: center;">*</td> <td></td> </tr> <tr> <td>H'08</td> <td style="border: 1px solid black; text-align: center;">Place 0</td> <td style="border: 1px solid black; text-align: center;">*</td> <td></td> </tr> <tr> <td>H'0C</td> <td style="border: 1px solid black; text-align: center;">Place 0</td> <td style="border: 1px solid black; text-align: center;">*</td> <td></td> </tr> <tr> <td>...</td> <td style="border: 1px solid black; text-align: center;">...</td> <td style="border: 1px solid black; text-align: center;">*</td> <td></td> </tr> </table>		31		0	H'00	Place 0	*		H'04	Place 0	*		H'08	Place 0	*		H'0C	Place 0	*		...	...	*																	
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<p>BUSIF</p> <ul style="list-style-type: none"> <li>· Multichannel (4 channels)</li> <li>· 16 bits</li> </ul>	<p>External memory image</p> <table style="margin-left: auto; margin-right: auto;"> <tr> <td></td> <td style="text-align: center;">31</td> <td></td> <td style="text-align: center;">0</td> </tr> <tr> <td>H'00</td> <td style="border: 1px solid black; text-align: center;">Place 0</td> <td style="border: 1px solid black; text-align: center;">Place 1</td> <td></td> </tr> <tr> <td>H'04</td> <td style="border: 1px solid black; text-align: center;">Place 2</td> <td style="border: 1px solid black; text-align: center;">Place 3</td> <td></td> </tr> <tr> <td>H'08</td> <td style="border: 1px solid black; text-align: center;">Place 0</td> <td style="border: 1px solid black; text-align: center;">Place 1</td> <td></td> </tr> <tr> <td>H'0C</td> <td style="border: 1px solid black; text-align: center;">Place 2</td> <td style="border: 1px solid black; text-align: center;">Place 3</td> <td></td> </tr> <tr> <td>...</td> <td style="border: 1px solid black; text-align: center;">...</td> <td style="border: 1px solid black; text-align: center;">...</td> <td></td> </tr> </table>		31		0	H'00	Place 0	Place 1		H'04	Place 2	Place 3		H'08	Place 0	Place 1		H'0C	Place 2	Place 3		...	...	...																	
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**Table 34.5 Data Places in Each Data Format (2)**

<p>BUSIF</p> <ul style="list-style-type: none"> <li>· Multichannel (6 channels)</li> <li>· 24 bits</li> </ul>	<p>External memory image</p> <table style="margin-left: auto; margin-right: auto;"> <tr> <td></td> <td style="text-align: center;">31</td> <td style="text-align: center;">0</td> </tr> <tr> <td>H'00</td> <td style="border: 1px solid black; text-align: center;">Place 0</td> <td style="border: 1px solid black; text-align: center;">*</td> </tr> <tr> <td>H'04</td> <td style="border: 1px solid black; text-align: center;">Place 1</td> <td style="border: 1px solid black; text-align: center;">*</td> </tr> <tr> <td>H'08</td> <td style="border: 1px solid black; text-align: center;">Place 2</td> <td style="border: 1px solid black; text-align: center;">*</td> </tr> <tr> <td>H'0C</td> <td style="border: 1px solid black; text-align: center;">Place 3</td> <td style="border: 1px solid black; text-align: center;">*</td> </tr> <tr> <td>H'10</td> <td style="border: 1px solid black; text-align: center;">Place 4</td> <td style="border: 1px solid black; text-align: center;">*</td> </tr> <tr> <td>H'14</td> <td style="border: 1px solid black; text-align: center;">Place 5</td> <td style="border: 1px solid black; text-align: center;">*</td> </tr> <tr> <td>H'18</td> <td style="border: 1px solid black; text-align: center;">Place 0</td> <td style="border: 1px solid black; text-align: center;">*</td> </tr> <tr> <td>H'1C</td> <td style="border: 1px solid black; text-align: center;">Place 1</td> <td style="border: 1px solid black; text-align: center;">*</td> </tr> <tr> <td>...</td> <td style="border: 1px solid black; text-align: center;">...</td> <td style="border: 1px solid black; text-align: center;">...</td> </tr> </table>		31	0	H'00	Place 0	*	H'04	Place 1	*	H'08	Place 2	*	H'0C	Place 3	*	H'10	Place 4	*	H'14	Place 5	*	H'18	Place 0	*	H'1C	Place 1	*	...	...	...			
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<p>BUSIF</p> <ul style="list-style-type: none"> <li>· Multichannel (6 channels)</li> <li>· 16 bits</li> </ul>	<p>External memory image</p> <table style="margin-left: auto; margin-right: auto;"> <tr> <td></td> <td style="text-align: center;">31</td> <td style="text-align: center;">0</td> </tr> <tr> <td>H'00</td> <td style="border: 1px solid black; text-align: center;">Place 0</td> <td style="border: 1px solid black; text-align: center;">Place 1</td> </tr> <tr> <td>H'04</td> <td style="border: 1px solid black; text-align: center;">Place 2</td> <td style="border: 1px solid black; text-align: center;">Place 3</td> </tr> <tr> <td>H'08</td> <td style="border: 1px solid black; text-align: center;">Place 4</td> <td style="border: 1px solid black; text-align: center;">Place 5</td> </tr> <tr> <td>H'0C</td> <td style="border: 1px solid black; text-align: center;">Place 0</td> <td style="border: 1px solid black; text-align: center;">Place 1</td> </tr> <tr> <td>...</td> <td style="border: 1px solid black; text-align: center;">...</td> <td style="border: 1px solid black; text-align: center;">...</td> </tr> </table>		31	0	H'00	Place 0	Place 1	H'04	Place 2	Place 3	H'08	Place 4	Place 5	H'0C	Place 0	Place 1	...	...	...															
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<p>BUSIF</p> <ul style="list-style-type: none"> <li>· Multichannel (8 channels)</li> <li>· 24 bits</li> </ul>	<p>External memory image</p> <table style="margin-left: auto; margin-right: auto;"> <tr> <td></td> <td style="text-align: center;">31</td> <td style="text-align: center;">0</td> </tr> <tr> <td>H'00</td> <td style="border: 1px solid black; text-align: center;">Place 0</td> <td style="border: 1px solid black; text-align: center;">*</td> </tr> <tr> <td>H'04</td> <td style="border: 1px solid black; text-align: center;">Place 1</td> <td style="border: 1px solid black; text-align: center;">*</td> </tr> <tr> <td>H'08</td> <td style="border: 1px solid black; text-align: center;">Place 2</td> <td style="border: 1px solid black; text-align: center;">*</td> </tr> <tr> <td>H'0C</td> <td style="border: 1px solid black; text-align: center;">Place 3</td> <td style="border: 1px solid black; text-align: center;">*</td> </tr> <tr> <td>H'10</td> <td style="border: 1px solid black; text-align: center;">Place 4</td> <td style="border: 1px solid black; text-align: center;">*</td> </tr> <tr> <td>H'14</td> <td style="border: 1px solid black; text-align: center;">Place 5</td> <td style="border: 1px solid black; text-align: center;">*</td> </tr> <tr> <td>H'18</td> <td style="border: 1px solid black; text-align: center;">Place 6</td> <td style="border: 1px solid black; text-align: center;">*</td> </tr> <tr> <td>H'1C</td> <td style="border: 1px solid black; text-align: center;">Place 7</td> <td style="border: 1px solid black; text-align: center;">*</td> </tr> <tr> <td>H'20</td> <td style="border: 1px solid black; text-align: center;">Place 0</td> <td style="border: 1px solid black; text-align: center;">*</td> </tr> <tr> <td>...</td> <td style="border: 1px solid black; text-align: center;">...</td> <td style="border: 1px solid black; text-align: center;">*</td> </tr> </table>		31	0	H'00	Place 0	*	H'04	Place 1	*	H'08	Place 2	*	H'0C	Place 3	*	H'10	Place 4	*	H'14	Place 5	*	H'18	Place 6	*	H'1C	Place 7	*	H'20	Place 0	*	...	...	*
	31	0																																
H'00	Place 0	*																																
H'04	Place 1	*																																
H'08	Place 2	*																																
H'0C	Place 3	*																																
H'10	Place 4	*																																
H'14	Place 5	*																																
H'18	Place 6	*																																
H'1C	Place 7	*																																
H'20	Place 0	*																																
...	...	*																																
<p>BUSIF</p> <ul style="list-style-type: none"> <li>· Multichannel (8 channels)</li> <li>· 16 bits</li> </ul>	<p>External memory image</p> <table style="margin-left: auto; margin-right: auto;"> <tr> <td></td> <td style="text-align: center;">31</td> <td style="text-align: center;">0</td> </tr> <tr> <td>H'00</td> <td style="border: 1px solid black; text-align: center;">Place 0</td> <td style="border: 1px solid black; text-align: center;">Place 1</td> </tr> <tr> <td>H'04</td> <td style="border: 1px solid black; text-align: center;">Place 2</td> <td style="border: 1px solid black; text-align: center;">Place 3</td> </tr> <tr> <td>H'08</td> <td style="border: 1px solid black; text-align: center;">Place 4</td> <td style="border: 1px solid black; text-align: center;">Place 5</td> </tr> <tr> <td>H'0C</td> <td style="border: 1px solid black; text-align: center;">Place 6</td> <td style="border: 1px solid black; text-align: center;">Place 7</td> </tr> <tr> <td>H'10</td> <td style="border: 1px solid black; text-align: center;">Place 0</td> <td style="border: 1px solid black; text-align: center;">Place 1</td> </tr> <tr> <td>...</td> <td style="border: 1px solid black; text-align: center;">...</td> <td style="border: 1px solid black; text-align: center;">...</td> </tr> </table>		31	0	H'00	Place 0	Place 1	H'04	Place 2	Place 3	H'08	Place 4	Place 5	H'0C	Place 6	Place 7	H'10	Place 0	Place 1	...	...	...												
	31	0																																
H'00	Place 0	Place 1																																
H'04	Place 2	Place 3																																
H'08	Place 4	Place 5																																
H'0C	Place 6	Place 7																																
H'10	Place 0	Place 1																																
...	...	...																																

### 34.3.5 SRC Block

The SRC is a block for implementing the sampling rate conversion function, which can convert asynchronous sampling rates.

- Asynchronous sampling rate conversion is available
- Supports resolutions up to 24 bits
- High-sound-quality type (THD+N is -132 dB) and general-sound-quality type (THD+N is -96 dB)
- Automatically generates antialiasing filter coefficients
- Four (three)\* modules support one, two, four, six, or eight channels, and six (three)\* modules support one or two channels.

Figure 34.5 shows the SRC block diagram.

The "Input audio data" in the figure indicates the data before SRC processing is applied. The "Output audio data" indicates the data after SRC processing is applied.

The "Input data timing" is a signal to show the sampling period for the input audio data. The "Output data timing" is a signal to show the sampling period for the output audio data. When CMD is used in the route, the output data timing signal is the same signal as the output data timing signal used in the CMD.

In synchronous mode specified by setting the SRCMD bit in the SRCm\_SRCCR register, when the sync\_in bit in the SRCm\_MODE register is set to 1, the SRCm doesn't need the input data timing signal, and when the sync\_out bit in the SRCm\_MODE register is set to 1, the SRCm doesn't need the output data timing signal.

Before using the SRC function, be sure to specify the sampling rate through the SRCm\_IFS value setting register (see section 34.2.22, SRCm\_IFS Value Setting Register (SRCm\_IFSVR)).

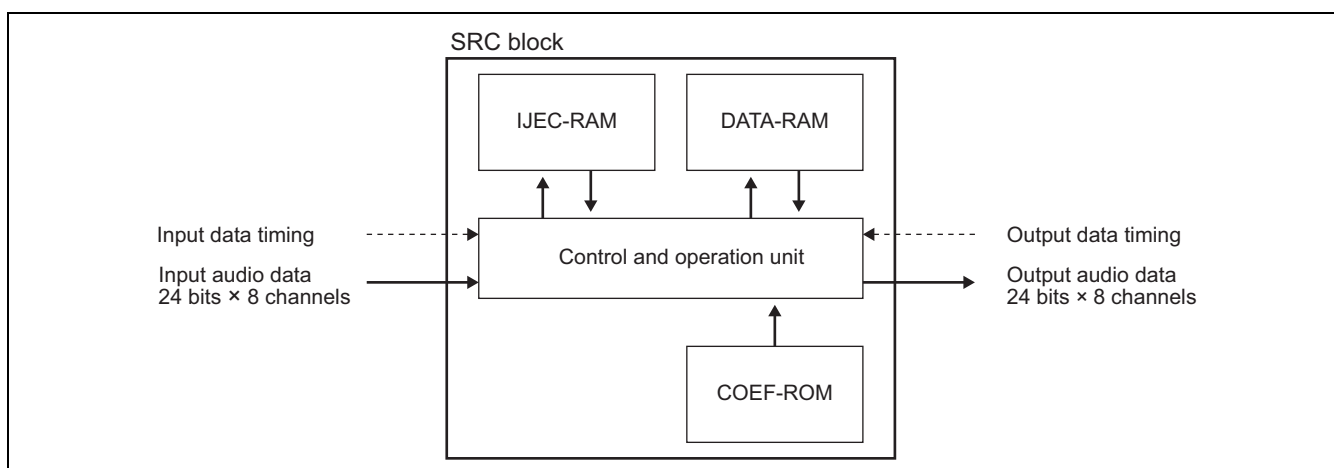


Figure 34.5 SRC Block Diagram

Table 34.6 shows the SRC functions.

**Table 34.6 SRC Functions**

**[RZ/G1H, RZ/G1M, and RZ/G1N]**

Item		Performance			
Type of SRC		Asynchronous/ Synchronous SRC			
Operation frequency		130 MHz			
Channel number		1 or 2	4	6	8
Sampling rate of input source	SRC0	8k to 192k [Hz]	8k to 192k [Hz]	8k to 192k [Hz]	8k to 192k [Hz]
	SRC1, SRC3, SRC4	8k to 192k [Hz]	8k to 192k [Hz]	8k to 128k [Hz]	8k to 96k [Hz]
	SRC2, SRC9	8k to 192k [Hz]	—	—	—
	SRC5 to SRC8	8k to 192k [Hz]	—	—	—
Sampling rate of output source	SRC0	8k to 192k [Hz]	8k to 192k [Hz]	8k to 192k [Hz]	8k to 192k [Hz]
	SRC1, SRC3, SRC4	8k to 192k [Hz]	8k to 192k [Hz]	8k to 128k [Hz]	8k to 96k [Hz]
	SRC2, SRC9	8k to 192k [Hz]	—	—	—
	SRC5 to SRC8	8k to 192k [Hz]	—	—	—
Ratio of input and output sampling rates (FSO/FSI ratio)	SRC0	6 to 1/6 [times]	6 to 0.25 [times]	6 to 0.25 [times]	6 to 0.25 [times]
	SRC1, SRC3, SRC4	6 to 1/6 [times]	6 to 0.25 [times]	6 to 0.5 [times]	6 to 0.5 [times]
	SRC2, SRC9	6 to 1/6 [times]	—	—	—
	SRC5 to SRC8	6 to 1/6 [times]	—	—	—
Sound quality (THD+N)	SRC0 to SRC4, SRC9	-132 dB (for high-quality type)			
	SRC5 to SRC8	-96 dB (for general-quality type)			

**[RZ/G1E]**

Item		Performance			
Type of SRC		Asynchronous/ Synchronous SRC			
Operation frequency		130 MHz			
Channel number		1 or 2	4	6	8
Sampling rate of input source	SRC1, SRC3, SRC4	8k to 192k [Hz]	8k to 192k [Hz]	8k to 128k [Hz]	8k to 96k [Hz]
	SRC2	8k to 192k [Hz]	—	—	—
	SRC5, SRC6	8k to 192k [Hz]	—	—	—
Sampling rate of output source	SRC1, SRC3, SRC4	8k to 192k [Hz]	8k to 192k [Hz]	8k to 128k [Hz]	8k to 96k [Hz]
	SRC2	8k to 192k [Hz]	—	—	—
	SRC5, SRC6	8k to 192k [Hz]	—	—	—
Ratio of input and output sampling rates (FSO/FSI ratio)	SRC1, SRC3, SRC4	6 to 1/6 [times]	6 to 0.25 [times]	6 to 0.5 [times]	6 to 0.5 [times]
	SRC2	6 to 1/6 [times]	—	—	—
	SRC5, SRC6	6 to 1/6 [times]	—	—	—
Sound quality (THD+N)	SRC1 to SRC4	-132 dB (for high-quality type)			
	SRC5, SRC6	-96 dB (for general-quality type)			

Table 34.7 shows the IJEC RAM and DATA RAM buffer size settings and the latencies.

Latency is different by setting of channel number.

Select the combination of settings BUFDATA[10:0] bits in SRCm\_BSDSR/ SRCn\_BSDSR register and IJECSIZE[8:0] bits in SRCm\_BSISR register from Table 34.7. Operation cannot be guaranteed if the register is not set as specified combination.

Output delay depends on FSO/FSI ratio and it is calculated from following formula.

$$\text{Output delay [sample]} = (\text{Processing delay}) \times (\text{FSO/FSI ratio}) + (\text{Logic delay})$$

**Table 34.7 Combination of Register Setting Related to FSO/FSI Ratio and Channel, Latency**

[RZ/G1H, RZ/G1M, RZ/G1N]

Item	Setting Range		Register Setting			Latency (Example case calculated by formula, Logic delay = 3)										Note
	FSO/FSI Ratio	Channel Number	IJEC SIZE [8:0]	BUF DATA [10:0]	Processing Delay [sample]	6	4	3	2	1	2/3	1/2	1/3	1/4	1/6	
SRC0	6 to 1/6	1 to 2	H'60	H'180	241	1449	967	726	485	244	164	124	83	63	43	*
	6 to 1/4	1 to 8	H'40	H'100	161	969	647	486	325	164	110	84	57	43		
	6 to 1/3	1 to 8	H'30	H'0C0	121	729	487	366	245	124	84	64	43			
	6 to 1/2	1 to 8	H'20	H'080	81	489	327	246	165	84	57	44				
	6 to 2/3	1 to 8	H'20	H'060	65	393	263	198	133	68	46					
	6 to 1	1 to 8	H'20	H'040	49	297	199	150	101	52						
SRC1	6 to 1/6	1 to 2	H'60	H'180	241	1449	967	726	485	244	164	124	83	63	43	*
SRC3	6 to 1/4	1 to 4	H'40	H'100	161	969	647	486	325	164	110	84	57	43		
SRC4	6 to 1/3	1 to 4	H'30	H'0C0	121	729	487	366	245	124	84	64	43			
	6 to 1/2	1 to 8	H'20	H'080	81	489	327	246	165	84	57	44				
	6 to 2/3	1 to 8	H'20	H'060	65	393	263	198	133	68	46					
	6 to 1	1 to 8	H'20	H'040	49	297	199	150	101	52						
SRC2	6 to 1/6	1 to 2	H'60	H'180	241	1449	967	726	485	244	164	124	83	63	43	*
SRC9	6 to 1/4	1 to 2	H'40	H'100	161	969	647	486	325	164	110	84	57	43		
	6 to 1/3	1 to 2	H'30	H'0C0	121	729	487	366	245	124	84	64	43			
	6 to 1/2	1 to 2	H'20	H'080	81	489	327	246	165	84	57	44				
	6 to 2/3	1 to 2	H'20	H'060	65	393	263	198	133	68	46					
	6 to 1	1 to 2	H'20	H'040	49	297	199	150	101	52						
SRC5 to SRC8	6 to 1/6	1 to 2	H'60	H'240	337	2025	1351	1014	677	340	228	172	115	87	59	*
	6 to 1/4	1 to 2	H'40	H'180	225	1353	903	678	453	228	153	116	78	59		
	6 to 1/3	1 to 2	H'30	H'120	169	1017	679	510	341	172	116	88	59			
	6 to 1/2	1 to 2	H'20	H'0C0	113	681	455	342	229	116	78	60				
	6 to 2/3	1 to 2	H'20	H'090	89	537	359	270	181	92	62					
	6 to 1	1 to 2	H'20	H'060	65	393	263	198	133	68						

Note: Please set up "\*" case by common setting, if there are no problem for the latency.

## [RZ/G1E]

Item	Setting Range		Register Setting			Latency (Example case calculated by formula, Logic delay = 3)											Note
	FSO/FSI Ratio	Channel Number	IJEC SIZE [8:0]	BUF DATA [10:0]	Processing Delay [sample]	6	4	3	2	1	2/3	1/2	1/3	1/4	1/6		
SRC1	6 to 1/6	1 to 2	H'60	H'180	241	1449	967	726	485	244	164	124	83	63	43	*	
SRC3	6 to 1/4	1 to 4	H'40	H'100	161	969	647	486	325	164	110	84	57	43			
SRC4	6 to 1/3	1 to 4	H'30	H'0C0	121	729	487	366	245	124	84	64	43				
	6 to 1/2	1 to 8	H'20	H'080	81	489	327	246	165	84	57	44					
	6 to 2/3	1 to 8	H'20	H'060	65	393	263	198	133	68	46						
	6 to 1	1 to 8	H'20	H'040	49	297	199	150	101	52							
	SRC2	6 to 1/6	1 to 2	H'60	H'180	241	1449	967	726	485	244	164	124	83	63	43	*
	6 to 1/4	1 to 2	H'40	H'100	161	969	647	486	325	164	110	84	57	43			
	6 to 1/3	1 to 2	H'30	H'0C0	121	729	487	366	245	124	84	64	43				
	6 to 1/2	1 to 2	H'20	H'080	81	489	327	246	165	84	57	44					
	6 to 2/3	1 to 2	H'20	H'060	65	393	263	198	133	68	46						
	6 to 1	1 to 2	H'20	H'040	49	297	199	150	101	52							
SRC5 to SRC6	6 to 1/6	1 to 2	H'60	H'240	337	2025	1351	1014	677	340	228	172	115	87	59	*	
	6 to 1/4	1 to 2	H'40	H'180	225	1353	903	678	453	228	153	116	78	59			
	6 to 1/3	1 to 2	H'30	H'120	169	1017	679	510	341	172	116	88	59				
	6 to 1/2	1 to 2	H'20	H'0C0	113	681	455	342	229	116	78	60					
	6 to 2/3	1 to 2	H'20	H'090	89	537	359	270	181	92	62						
	6 to 1	1 to 2	H'20	H'060	65	393	263	198	133	68							

Note: Please set up "\*" case by common setting, if there are no problem for the latency.

Table 34.8 shows the INTIFS setting examples in the SRC block.

**Table 34.8 INTIFS Values in SRCm\_IFSVR Register for Some Specific Cases**

INTIFS[27:0]							
Input sampling rate [kHz]	Output sampling rate [kHz]						
	8	16	32	44.1	48	96	192
8	H'0400000	H'0200000	H'0100000	H'00B9C27	H'00AAAAA	—	—
11.025	H'0583333	H'02C1999	H'0160CCC	H'0100000	H'00EB333	—	—
12	H'0600000	H'0300000	H'0180000	H'0116A3B	H'0100000	—	—
16	H'0800000	H'0400000	H'0200000	H'017384E	H'0155555	H'00AAAAA	—
22.05	H'0B06666	H'0583333	H'02C1999	H'0200000	H'01D6666	H'00EB333	—
24	H'0C00000	H'0600000	H'0300000	H'022D476	H'0200000	H'0100000	—
32	H'1000000	H'0800000	H'0400000	H'02E709D	H'02AAAAA	H'0155555	H'00AAAAA
44.1	H'160CCCC	H'0B06666	H'0583333	H'0400000	H'03ACCCC	H'01D6666	H'00EB333
48	H'1800000	H'0C00000	H'0600000	H'045A8EC	H'0400000	H'0200000	H'0100000
64	—	H'1000000	H'0800000	H'05CE13B	H'0555555	H'02AAAAA	H'0155555
88.2	—	H'160CCCC	H'0B06666	H'0800000	H'0759999	H'03ACCCC	H'01D6666
96	—	H'1800000	H'0C00000	H'08B51D9	H'0800000	H'0400000	H'0200000
176.4	—	H'2C19999	H'160CCCC	H'1000000	H'0EB3333	H'0759999	H'03ACCCC
192	—	—	H'1800000	H'116A3B3	H'1000000	H'0800000	H'0400000

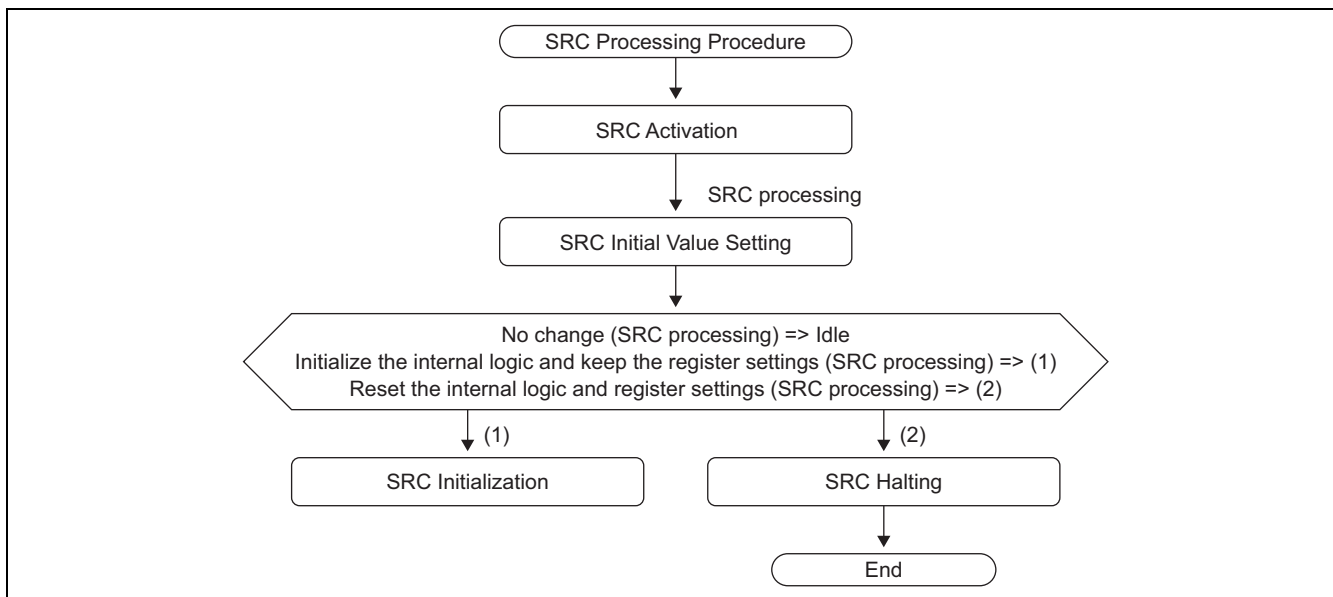


**(1) Register Setting Procedure**

The following describes the SRC register setting procedures. The register should be used according to the following procedures.

**(a) SRC Processing Procedure**

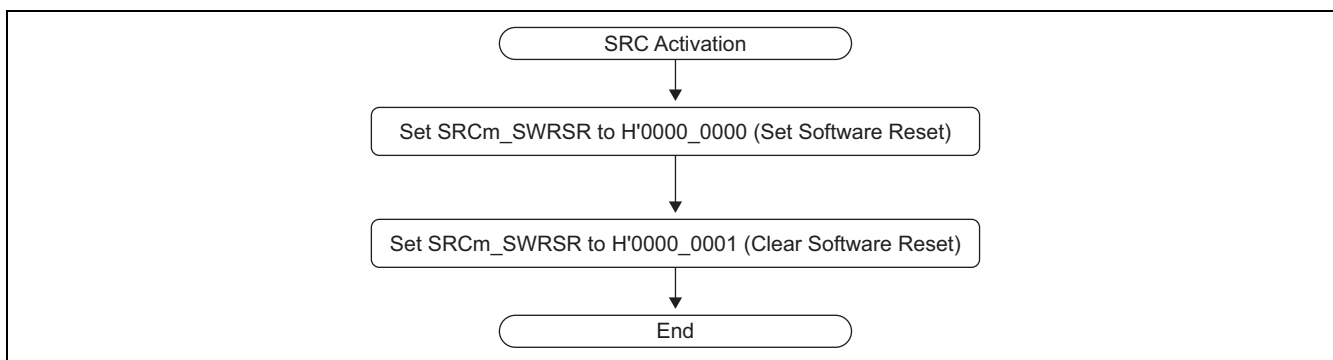
Figure 34.6 shows the processing procedure of SRC.



**Figure 34.6 SRC Processing Procedure**

**(b) SRC Activation**

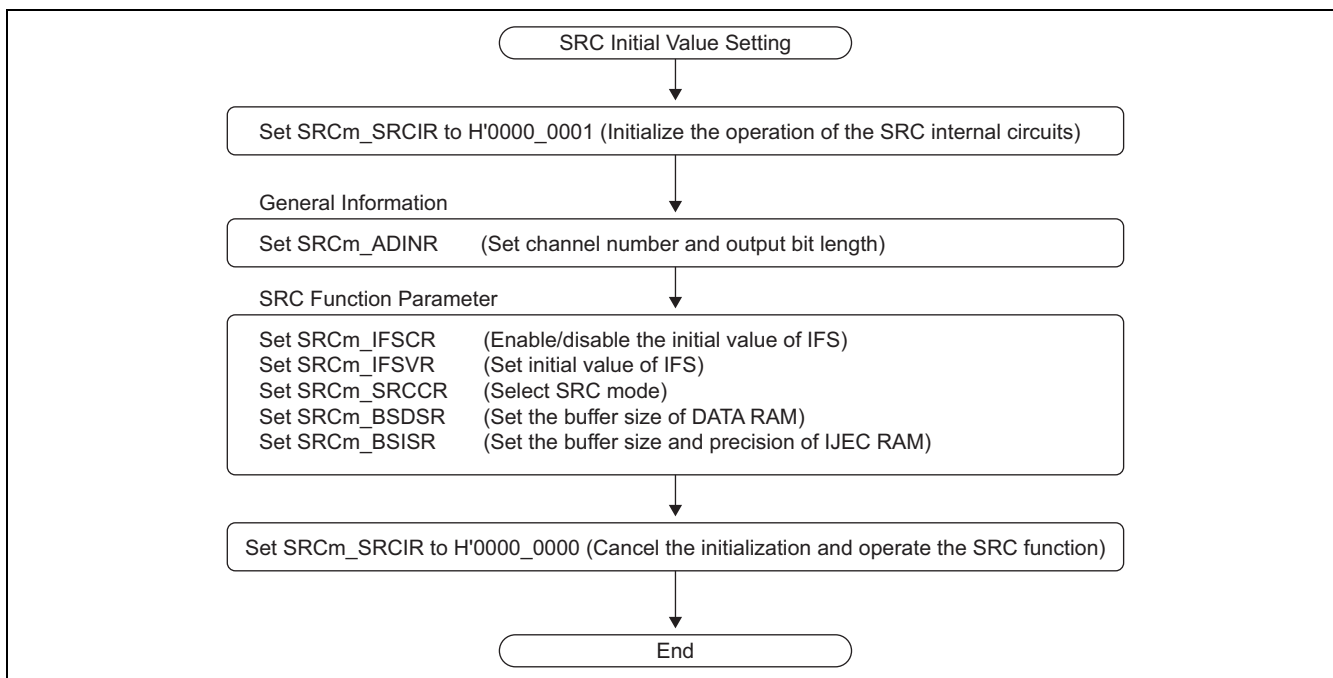
Figure 34.7 shows the SRC activation flowchart. When the SRC is activated, a software reset should be set to initialize logic and register setting. Then, the software reset should be cleared and ready to operate SRC. When reset the SRC function, all registers are initialized. If the SRC function was initialized by a hardware reset, it doesn't need to initialize the SRC function by software reset.



**Figure 34.7 SRC Activation Flowchart**

**(c) SRC Initial Value Setting**

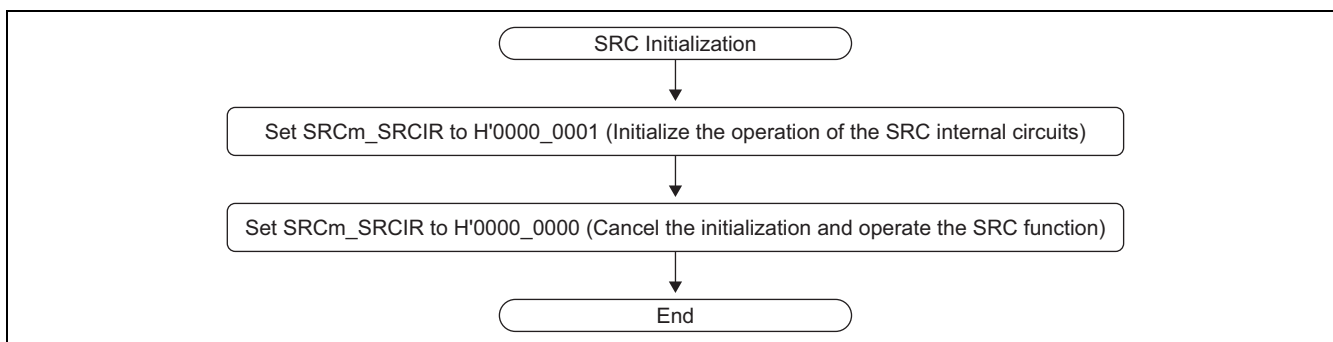
Figure 34.8 shows the flowchart of the SRC initial value setting. Before operate SRC function, the initial values should be set.



**Figure 34.8 SRC Initial Value Setting Flowchart**

**(d) SRC Initialization**

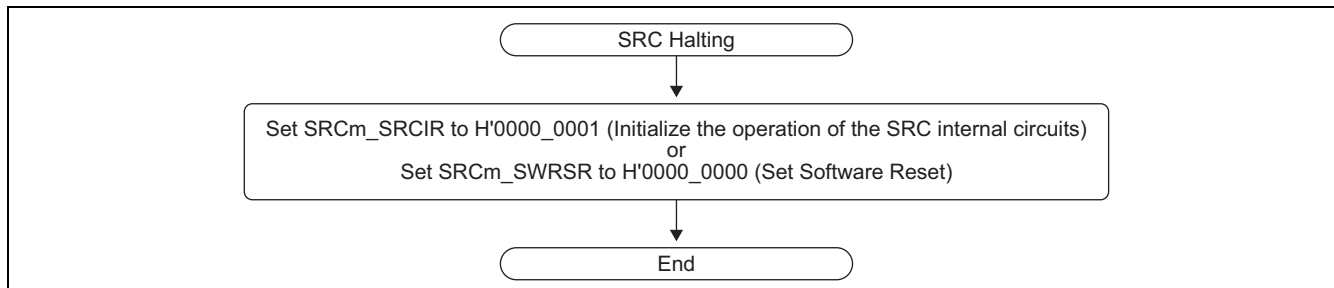
Figure 34.9 shows the SRC initialization flowchart. SRCm\_SRCIR register doesn't initialize the register settings and these values are maintained. Before cancel the initialization, it is necessary to set or check the register settings of peripheral IP. And also it is necessary to provide the input and output timing signal.



**Figure 34.9 SRC Initialization Flowchart**

**(e) SRC Halting**

Figure 34.10 shows the flowchart of SRC halting. When SRC is halting, it should be initialize or reset by software reset or hardware reset. Before initialize or reset the SRC function, it is necessary to confirm the register settings and operation of peripheral IP.



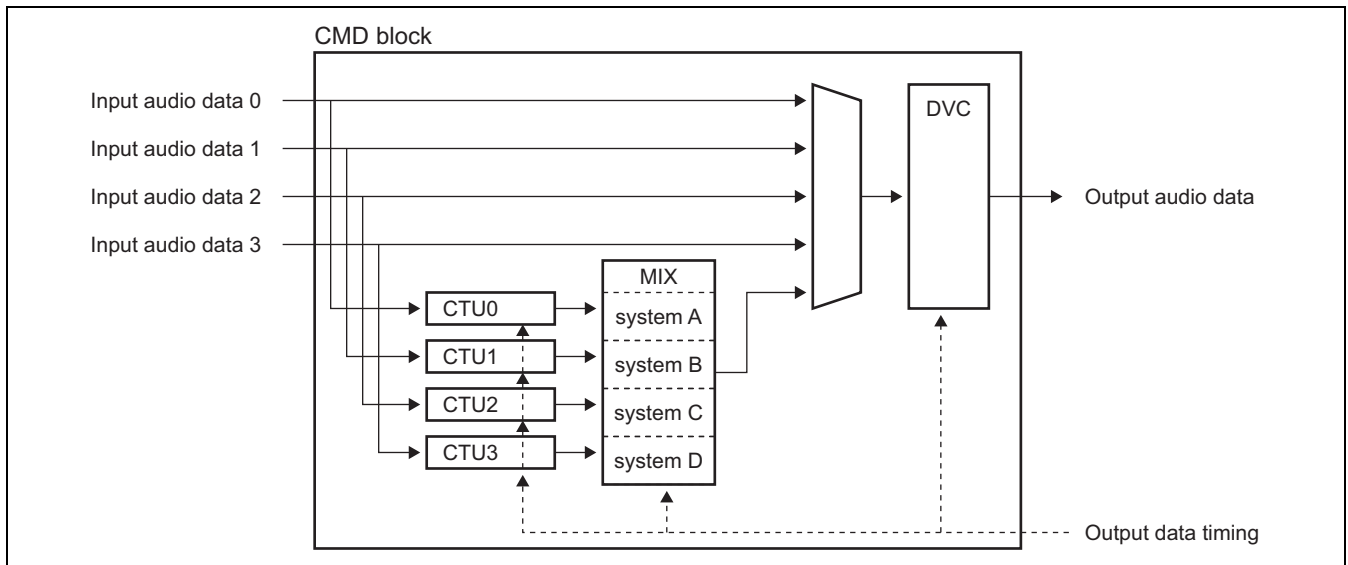
**Figure 34.10 SRC Halting Flowchart**

**34.3.6 CMD Block**

The CMD is a block for implementing the channel transfer unit (CTU block), mixing (MIX block), and digital volume and mute (DVC block) functions. Figure 34.11 shows the CMD block diagram.

The "Input audio data 0" to "Input audio data 3" in the figure indicate the data before the CMD function is applied. The "Output audio data" indicates the data after the CMD function is applied.

The "Output data timing" is a signal to show the sampling period for the output audio data. In addition, please give the same signals to CMD output timing signal and output data timing signal used in the SRC.



**Figure 34.11 CMD Block Diagram**

### 34.3.7 Functional Blocks in CMD

#### (1) CTU Block

The CTU is a block for implementing channel transfer unit functions such as downmixing and splitter functions.

- Conversion of eight input channels into two output channels
- Conversion of six input channels into two output channels
- Conversion of two input channels into four sets of two output channels
- Conversion of one input channel into eight sets of one output channel
- No conversion

The settings of the Scale Value e00 to Scale Value e37 registers are calculated by using the following formula (signed bits are excluded):

$$\text{Setting (decimal)} = 10^X \times 4194304$$

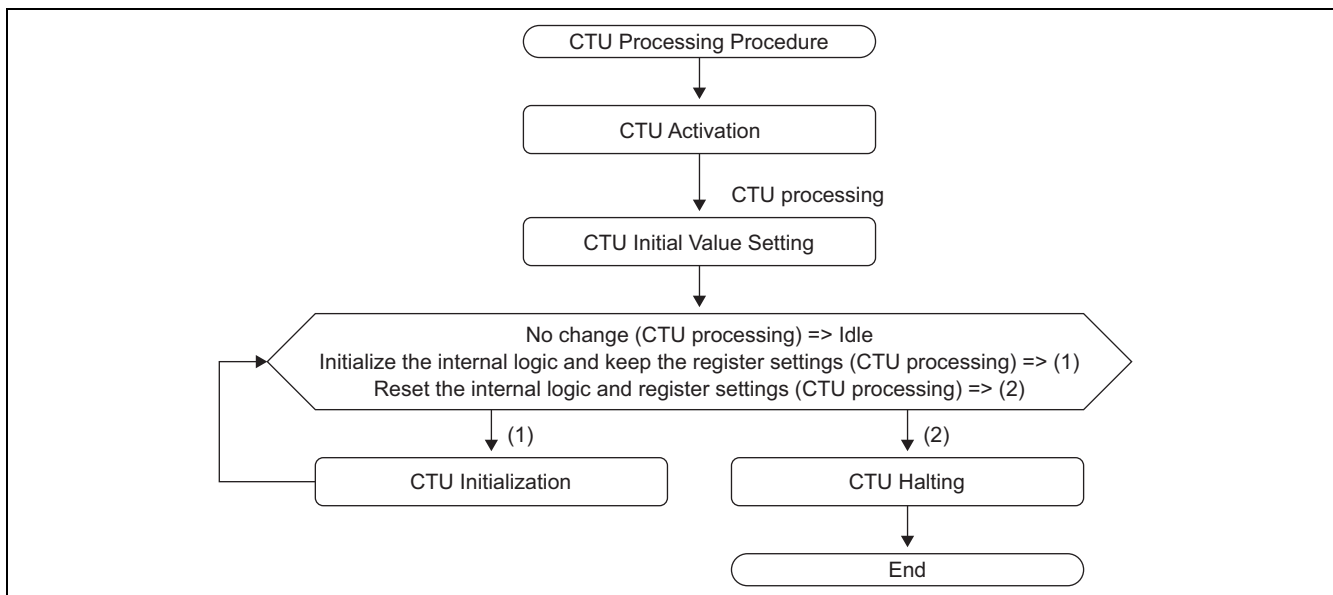
$$X = (\text{value in dB}) / 20$$

**(a) Register Setting Procedure**

The following describes the CTU register setting procedures. The register should be used according to the following procedures.

- CTU Processing Procedure

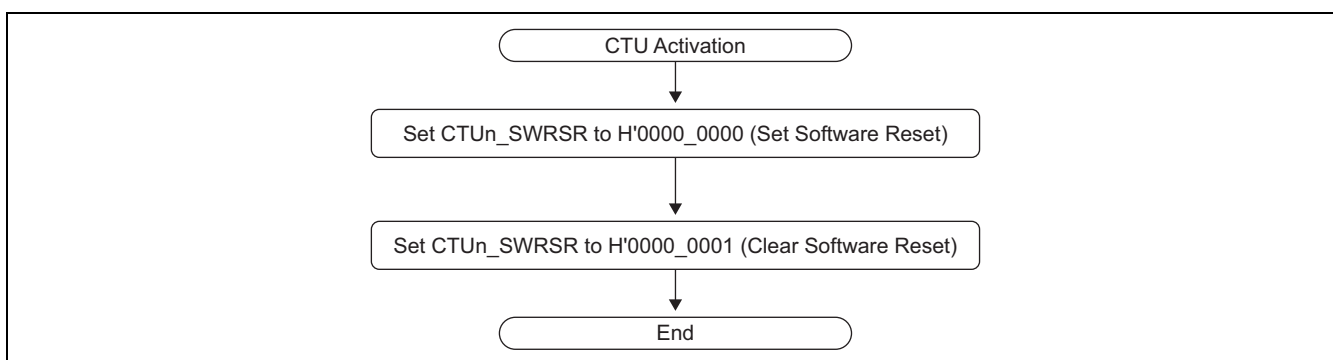
Figure 34.12 shows the processing procedure of CTU.



**Figure 34.12 CTU Processing Procedure**

- CTU Activation

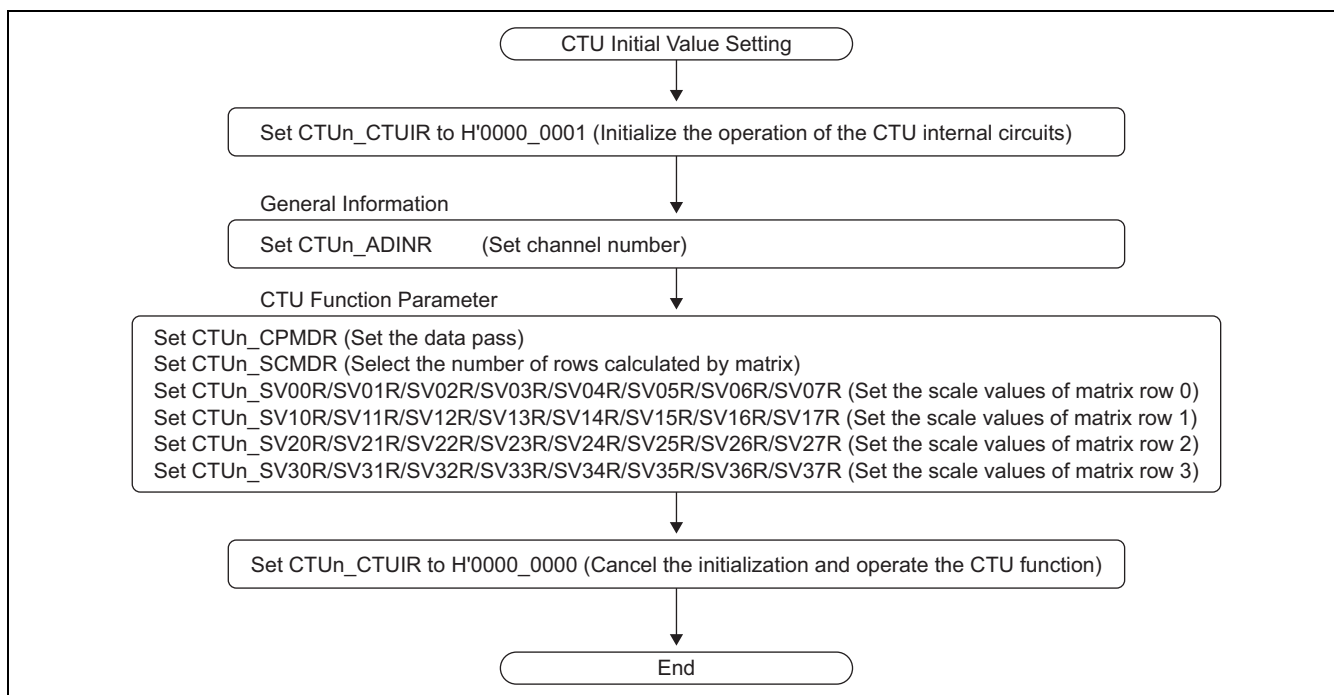
Figure 34.13 shows the CTU activation flowchart. When the CTU is activated, a software reset should be set to initialize logic and register setting. Then, the software reset should be cleared and ready to operate CTU. When reset the CTU function, all registers are initialized. If the CTU function was initialized by a hardware reset, it doesn't need to initialize the CTU function by software reset.



**Figure 34.13 CTU Activation Flowchart**

- CTU Initial Value Setting

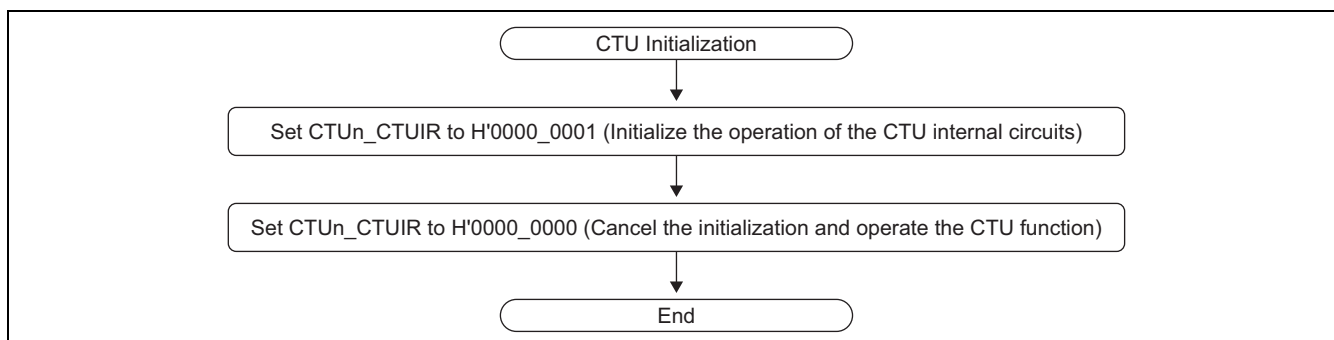
Figure 34.14 shows the flowchart of the CTU initial value setting. Before operate CTU function, the initial values should be set. After set the register setting and cancel the initialization, CTU module starts the operation.



**Figure 34.14 CTU Initial Value Setting Flowchart**

- CTU Initialization

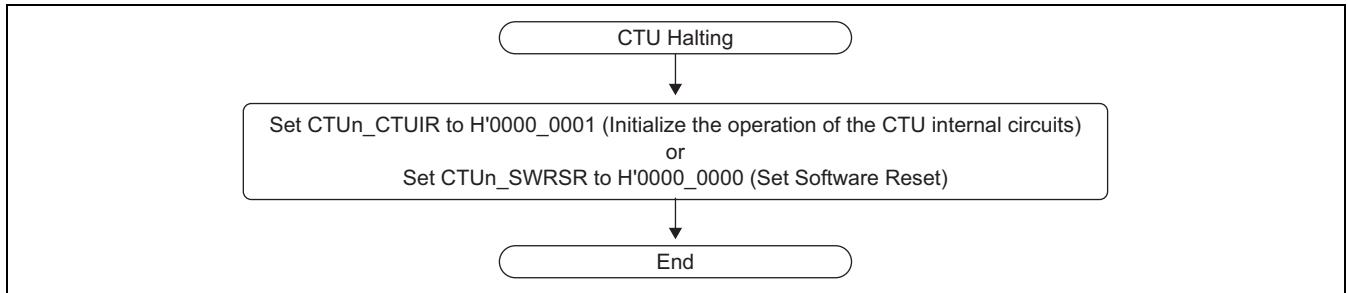
Figure 34.15 shows the CTU initialization flowchart. CTUn\_CTUIR register doesn't initialize the register settings and these values are maintained. Before cancel the initialization, it is necessary to set or check the register settings of peripheral IP.



**Figure 34.15 CTU Initialization Flowchart**

- CTU Halting

Figure 34.16 shows the flowchart of CTU halting. When CTU is halting, it should be initialize or reset by software reset or hardware reset. Before initialize or reset the CTU function, it is necessary to confirm the register settings and operation of peripheral IP.



**Figure 34.16 CTU Halting Flowchart**

- CTU – Example

The channel conversion executes the linear transformation (matrix operation) as follows.

$$\begin{pmatrix} y_0 \\ y_1 \\ y_2 \\ y_3 \\ y_4 \\ y_5 \\ y_6 \\ y_7 \end{pmatrix} = \begin{pmatrix} e_{00} & e_{01} & e_{02} & e_{03} & e_{04} & e_{05} & e_{06} & e_{07} \\ e_{10} & e_{11} & e_{12} & e_{13} & e_{14} & e_{15} & e_{16} & e_{17} \\ e_{20} & e_{21} & e_{22} & e_{23} & e_{24} & e_{25} & e_{26} & e_{27} \\ e_{30} & e_{31} & e_{32} & e_{33} & e_{34} & e_{35} & e_{36} & e_{37} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{pmatrix} \times \begin{pmatrix} x_0 \\ x_1 \\ x_2 \\ x_3 \\ x_4 \\ x_5 \\ x_6 \\ x_7 \end{pmatrix}$$

$x_i$ : Input data of channel  $i$  ( $i = 0$  to  $7$ )

$y_i$ : Output data of channel  $i$  ( $i = 0$  to  $7$ )

$e_j$ : CTUn\_SVjR.SVEj ( $j = 00, 01, 02, 03, 04, 05, 06, 07,$   
 $10, 11, 12, 13, 14, 15, 16, 17,$   
 $20, 21, 22, 23, 24, 25, 26, 27,$   
 $30, 31, 32, 33, 34, 35, 36, 37)$



Figure 34.17 shows 2 channels fold-down.

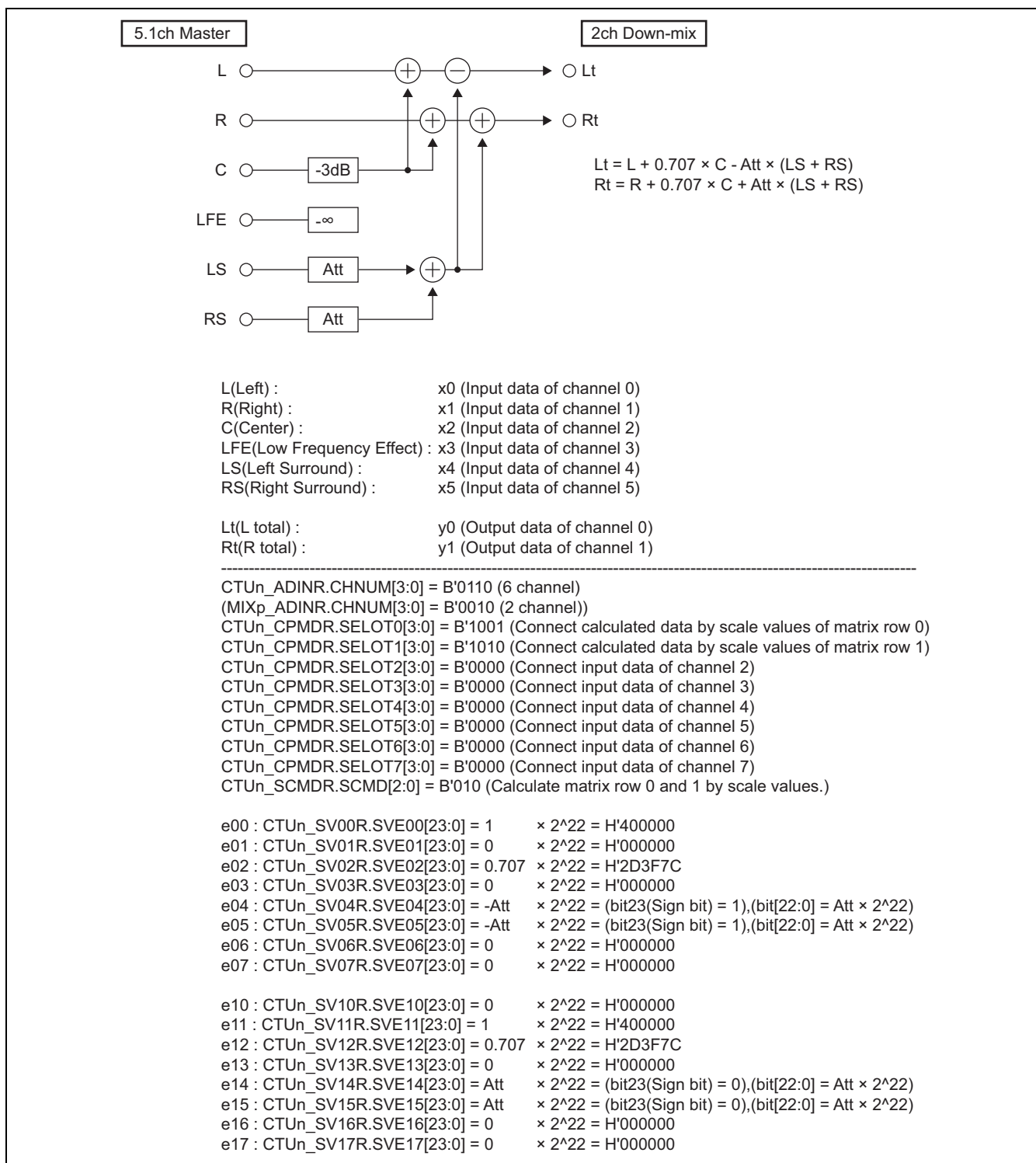
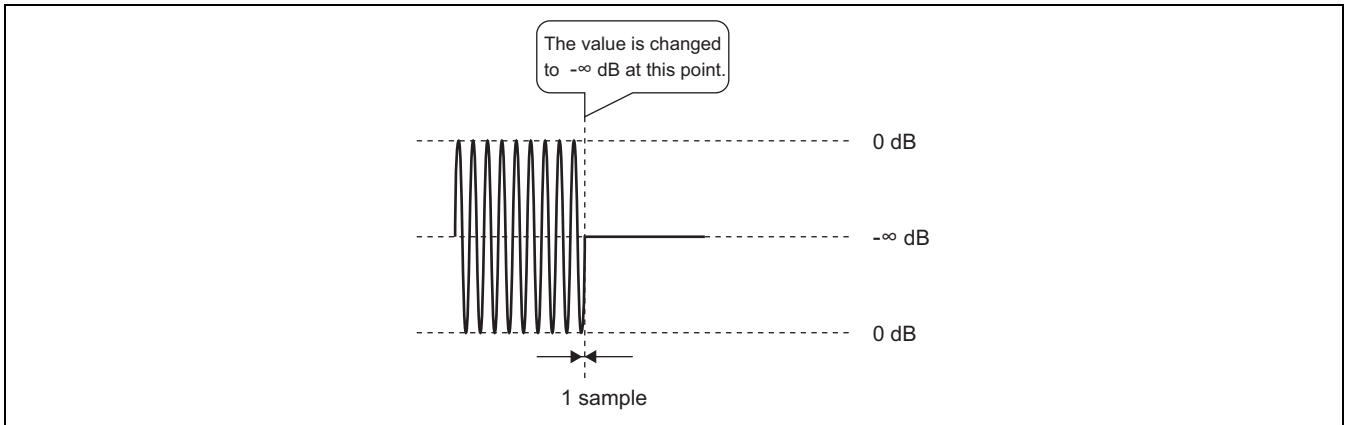


Figure 34.17 2 channels fold-down (Lt/Rt Downmix)

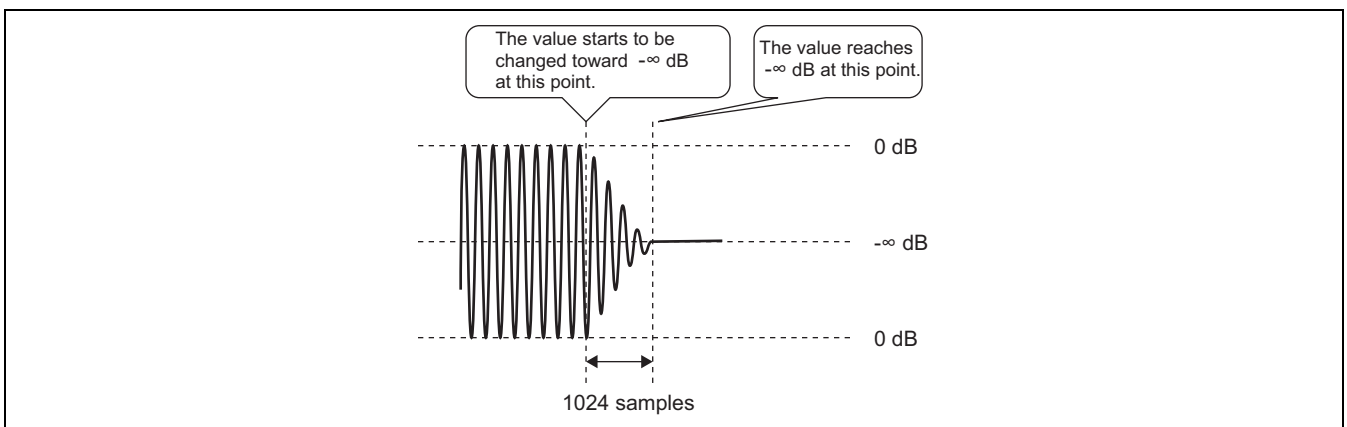
**(2) MIX Block**

The MIX block is for mixing (adding) streams from two to four audio data sources into a single stream.

- Ratio for adding sources is selectable
- Ratio is dynamically changeable
- Mixing with volume ramp is available (ramp period is selectable)



**Figure 34.18 Step Processing**



**Figure 34.19 Ramp Processing**

Tables 34.9 to 34.12 show the settings of the MIX decibel register and the corresponding levels in decibels.

**Table 34.9 Settings of MIXp\_MDBAR, MIXp\_MDBBR, MIXp\_MDBCR, and MIXp\_MDBDR and Corresponding Values in Decibels (No. 0 to 255)**

No	Value (HEX)	dB	No	Value (HEX)	dB	No	Value (HEX)	dB	No	Value (HEX)	dB
0	000	0	39	027	-4.875	78	04E	-9.75	117	075	-14.625
1	001	-0.125	40	028	-5	79	04F	-9.875	118	076	-14.75
2	002	-0.25	41	029	-5.125	80	050	-10	119	077	-14.875
3	003	-0.375	42	02A	-5.25	81	051	-10.125	120	078	-15
4	004	-0.5	43	02B	-5.375	82	052	-10.25	121	079	-15.125
5	005	-0.625	44	02C	-5.5	83	053	-10.375	122	07A	-15.25
6	006	-0.75	45	02D	-5.625	84	054	-10.5	123	07B	-15.375
7	007	-0.875	46	02E	-5.75	85	055	-10.625	124	07C	-15.5
8	008	-1	47	02F	-5.875	86	056	-10.75	125	07D	-15.625
9	009	-1.125	48	030	-6	87	057	-10.875	126	07E	-15.75
10	00A	-1.25	49	031	-6.125	88	058	-11	127	07F	-15.875
11	00B	-1.375	50	032	-6.25	89	059	-11.125	128	080	-16
12	00C	-1.5	51	033	-6.375	90	05A	-11.25	129	081	-16.125
13	00D	-1.625	52	034	-6.5	91	05B	-11.375	130	082	-16.25
14	00E	-1.75	53	035	-6.625	92	05C	-11.5	131	083	-16.375
15	00F	-1.875	54	036	-6.75	93	05D	-11.625	132	084	-16.5
16	010	-2	55	037	-6.875	94	05E	-11.75	133	085	-16.625
17	011	-2.125	56	038	-7	95	05F	-11.875	134	086	-16.75
18	012	-2.25	57	039	-7.125	96	060	-12	135	087	-16.875
19	013	-2.375	58	03A	-7.25	97	061	-12.125	136	088	-17
20	014	-2.5	59	03B	-7.375	98	062	-12.25	137	089	-17.125
21	015	-2.625	60	03C	-7.5	99	063	-12.375	138	08A	-17.25
22	016	-2.75	61	03D	-7.625	100	064	-12.5	139	08B	-17.375
23	017	-2.875	62	03E	-7.75	101	065	-12.625	140	08C	-17.5
24	018	-3	63	03F	-7.875	102	066	-12.75	141	08D	-17.625
25	019	-3.125	64	040	-8	103	067	-12.875	142	08E	-17.75
26	01A	-3.25	65	041	-8.125	104	068	-13	143	08F	-17.875
27	01B	-3.375	66	042	-8.25	105	069	-13.125	144	090	-18
28	01C	-3.5	67	043	-8.375	106	06A	-13.25	145	091	-18.125
29	01D	-3.625	68	044	-8.5	107	06B	-13.375	146	092	-18.25
30	01E	-3.75	69	045	-8.625	108	06C	-13.5	147	093	-18.375
31	01F	-3.875	70	046	-8.75	109	06D	-13.625	148	094	-18.5
32	020	-4	71	047	-8.875	110	06E	-13.75	149	095	-18.625
33	021	-4.125	72	048	-9	111	06F	-13.875	150	096	-18.75
34	022	-4.25	73	049	-9.125	112	070	-14	151	097	-18.875
35	023	-4.375	74	04A	-9.25	113	071	-14.125	152	098	-19
36	024	-4.5	75	04B	-9.375	114	072	-14.25	153	099	-19.125
37	025	-4.625	76	04C	-9.5	115	073	-14.375	154	09A	-19.25
38	026	-4.75	77	04D	-9.625	116	074	-14.5	155	09B	-19.375

No	Value (HEX)	dB	No	Value (HEX)	dB	No	Value (HEX)	dB	No	Value (HEX)	dB
156	09C	-19.5	181	0B5	-22.625	206	0CE	-25.75	231	0E7	-28.875
157	09D	-19.625	182	0B6	-22.75	207	0CF	-25.875	232	0E8	-29
158	09E	-19.75	183	0B7	-22.875	208	0D0	-26	233	0E9	-29.125
159	09F	-19.875	184	0B8	-23	209	0D1	-26.125	234	0EA	-29.25
160	0A0	-20	185	0B9	-23.125	210	0D2	-26.25	235	0EB	-29.375
161	0A1	-20.125	186	0BA	-23.25	211	0D3	-26.375	236	0EC	-29.5
162	0A2	-20.25	187	0BB	-23.375	212	0D4	-26.5	237	0ED	-29.625
163	0A3	-20.375	188	0BC	-23.5	213	0D5	-26.625	238	0EE	-29.75
164	0A4	-20.5	189	0BD	-23.625	214	0D6	-26.75	239	0EF	-29.875
165	0A5	-20.625	190	0BE	-23.75	215	0D7	-26.875	240	0F0	-30
166	0A6	-20.75	191	0BF	-23.875	216	0D8	-27	241	0F1	-30.125
167	0A7	-20.875	192	0C0	-24	217	0D9	-27.125	242	0F2	-30.25
168	0A8	-21	193	0C1	-24.125	218	0DA	-27.25	243	0F3	-30.375
169	0A9	-21.125	194	0C2	-24.25	219	0DB	-27.375	244	0F4	-30.5
170	0AA	-21.25	195	0C3	-24.375	220	0DC	-27.5	245	0F5	-30.625
171	0AB	-21.375	196	0C4	-24.5	221	0DD	-27.625	246	0F6	-30.75
172	0AC	-21.5	197	0C5	-24.625	222	0DE	-27.75	247	0F7	-30.875
173	0AD	-21.625	198	0C6	-24.75	223	0DF	-27.875	248	0F8	-31
174	0AE	-21.75	199	0C7	-24.875	224	0E0	-28	249	0F9	-31.125
175	0AF	-21.875	200	0C8	-25	225	0E1	-28.125	250	0FA	-31.25
176	0B0	-22	201	0C9	-25.125	226	0E2	-28.25	251	0FB	-31.375
177	0B1	-22.125	202	0CA	-25.25	227	0E3	-28.375	252	0FC	-31.5
178	0B2	-22.25	203	0CB	-25.375	228	0E4	-28.5	253	0FD	-31.625
179	0B3	-22.375	204	0CC	-25.5	229	0E5	-28.625	254	0FE	-31.75
180	0B4	-22.5	205	0CD	-25.625	230	0E6	-28.75	255	0FF	-31.875

**Table 34.10 Settings of MIXp\_MDBAR, MIXp\_MDBBR, MIXp\_MDBCR, and MIXp\_MDBDR and Corresponding Values in Decibels (No. 256 to 511)**

No	Value (HEX)	dB	No	Value (HEX)	dB	No	Value (HEX)	dB	No	Value (HEX)	dB
256	100	-32	297	129	-37.125	338	152	-42.25	379	17B	-47.375
257	101	-32.125	298	12A	-37.25	339	153	-42.375	380	17C	-47.5
258	102	-32.25	299	12B	-37.375	340	154	-42.5	381	17D	-47.625
259	103	-32.375	300	12C	-37.5	341	155	-42.625	382	17E	-47.75
260	104	-32.5	301	12D	-37.625	342	156	-42.75	383	17F	-47.875
261	105	-32.625	302	12E	-37.75	343	157	-42.875	384	180	-48
262	106	-32.75	303	12F	-37.875	344	158	-43	385	181	-48.125
263	107	-32.875	304	130	-38	345	159	-43.125	386	182	-48.25
264	108	-33	305	131	-38.125	346	15A	-43.25	387	183	-48.375
265	109	-33.125	306	132	-38.25	347	15B	-43.375	388	184	-48.5
266	10A	-33.25	307	133	-38.375	348	15C	-43.5	389	185	-48.625
267	10B	-33.375	308	134	-38.5	349	15D	-43.625	390	186	-48.75
268	10C	-33.5	309	135	-38.625	350	15E	-43.75	391	187	-48.875
269	10D	-33.625	310	136	-38.75	351	15F	-43.875	392	188	-49
270	10E	-33.75	311	137	-38.875	352	160	-44	393	189	-49.125
271	10F	-33.875	312	138	-39	353	161	-44.125	394	18A	-49.25
272	110	-34	313	139	-39.125	354	162	-44.25	395	18B	-49.375
273	111	-34.125	314	13A	-39.25	355	163	-44.375	396	18C	-49.5
274	112	-34.25	315	13B	-39.375	356	164	-44.5	397	18D	-49.625
275	113	-34.375	316	13C	-39.5	357	165	-44.625	398	18E	-49.75
276	114	-34.5	317	13D	-39.625	358	166	-44.75	399	18F	-49.875
277	115	-34.625	318	13E	-39.75	359	167	-44.875	400	190	-50
278	116	-34.75	319	13F	-39.875	360	168	-45	401	191	-50.125
279	117	-34.875	320	140	-40	361	169	-45.125	402	192	-50.25
280	118	-35	321	141	-40.125	362	16A	-45.25	403	193	-50.375
281	119	-35.125	322	142	-40.25	363	16B	-45.375	404	194	-50.5
282	11A	-35.25	323	143	-40.375	364	16C	-45.5	405	195	-50.625
283	11B	-35.375	324	144	-40.5	365	16D	-45.625	406	196	-50.75
284	11C	-35.5	325	145	-40.625	366	16E	-45.75	407	197	-50.875
285	11D	-35.625	326	146	-40.75	367	16F	-45.875	408	198	-51
286	11E	-35.75	327	147	-40.875	368	170	-46	409	199	-51.125
287	11F	-35.875	328	148	-41	369	171	-46.125	410	19A	-51.25
288	120	-36	329	149	-41.125	370	172	-46.25	411	19B	-51.375
289	121	-36.125	330	14A	-41.25	371	173	-46.375	412	19C	-51.5
290	122	-36.25	331	14B	-41.375	372	174	-46.5	413	19D	-51.625
291	123	-36.375	332	14C	-41.5	373	175	-46.625	414	19E	-51.75
292	124	-36.5	333	14D	-41.625	374	176	-46.75	415	19F	-51.875
293	125	-36.625	334	14E	-41.75	375	177	-46.875	416	1A0	-52
294	126	-36.75	335	14F	-41.875	376	178	-47	417	1A1	-52.125
295	127	-36.875	336	150	-42	377	179	-47.125	418	1A2	-52.25
296	128	-37	337	151	-42.125	378	17A	-47.25	419	1A3	-52.375

No	Value (HEX)	dB	No	Value (HEX)	dB	No	Value (HEX)	dB	No	Value (HEX)	dB
420	1A4	-52.5	443	1BB	-55.375	466	1D2	-58.25	489	1E9	-61.125
421	1A5	-52.625	444	1BC	-55.5	467	1D3	-58.375	490	1EA	-61.25
422	1A6	-52.75	445	1BD	-55.625	468	1D4	-58.5	491	1EB	-61.375
423	1A7	-52.875	446	1BE	-55.75	469	1D5	-58.625	492	1EC	-61.5
424	1A8	-53	447	1BF	-55.875	470	1D6	-58.75	493	1ED	-61.625
425	1A9	-53.125	448	1C0	-56	471	1D7	-58.875	494	1EE	-61.75
426	1AA	-53.25	449	1C1	-56.125	472	1D8	-59	495	1EF	-61.875
427	1AB	-53.375	450	1C2	-56.25	473	1D9	-59.125	496	1F0	-62
428	1AC	-53.5	451	1C3	-56.375	474	1DA	-59.25	497	1F1	-62.125
429	1AD	-53.625	452	1C4	-56.5	475	1DB	-59.375	498	1F2	-62.25
430	1AE	-53.75	453	1C5	-56.625	476	1DC	-59.5	499	1F3	-62.375
431	1AF	-53.875	454	1C6	-56.75	477	1DD	-59.625	500	1F4	-62.5
432	1B0	-54	455	1C7	-56.875	478	1DE	-59.75	501	1F5	-62.625
433	1B1	-54.125	456	1C8	-57	479	1DF	-59.875	502	1F6	-62.75
434	1B2	-54.25	457	1C9	-57.125	480	1E0	-60	503	1F7	-62.875
435	1B3	-54.375	458	1CA	-57.25	481	1E1	-60.125	504	1F8	-63
436	1B4	-54.5	459	1CB	-57.375	482	1E2	-60.25	505	1F9	-63.125
437	1B5	-54.625	460	1CC	-57.5	483	1E3	-60.375	506	1FA	-63.25
438	1B6	-54.75	461	1CD	-57.625	484	1E4	-60.5	507	1FB	-63.375
439	1B7	-54.875	462	1CE	-57.75	485	1E5	-60.625	508	1FC	-63.5
440	1B8	-55	463	1CF	-57.875	486	1E6	-60.75	509	1FD	-63.625
441	1B9	-55.125	464	1D0	-58	487	1E7	-60.875	510	1FE	-63.75
442	1BA	-55.25	465	1D1	-58.125	488	1E8	-61	511	1FF	-63.875

**Table 34.11 Settings of MIXp\_MDBAR, MIXp\_MDBBR, MIXp\_MDBCR, and MIXp\_MDBDR and Corresponding Values in Decibels (No. 512 to 767)**

No	Value (HEX)	dB	No	Value (HEX)	dB	No	Value (HEX)	dB	No	Value (HEX)	dB
512	200	-64	553	229	-69.125	594	252	-74.25	635	27B	-79.375
513	201	-64.125	554	22A	-69.25	595	253	-74.375	636	27C	-79.5
514	202	-64.25	555	22B	-69.375	596	254	-74.5	637	27D	-79.625
515	203	-64.375	556	22C	-69.5	597	255	-74.625	638	27E	-79.75
516	204	-64.5	557	22D	-69.625	598	256	-74.75	639	27F	-79.875
517	205	-64.625	558	22E	-69.75	599	257	-74.875	640	280	-80
518	206	-64.75	559	22F	-69.875	600	258	-75	641	281	-80.125
519	207	-64.875	560	230	-70	601	259	-75.125	642	282	-80.25
520	208	-65	561	231	-70.125	602	25A	-75.25	643	283	-80.375
521	209	-65.125	562	232	-70.25	603	25B	-75.375	644	284	-80.5
522	20A	-65.25	563	233	-70.375	604	25C	-75.5	645	285	-80.625
523	20B	-65.375	564	234	-70.5	605	25D	-75.625	646	286	-80.75
524	20C	-65.5	565	235	-70.625	606	25E	-75.75	647	287	-80.875
525	20D	-65.625	566	236	-70.75	607	25F	-75.875	648	288	-81
526	20E	-65.75	567	237	-70.875	608	260	-76	649	289	-81.125
527	20F	-65.875	568	238	-71	609	261	-76.125	650	28A	-81.25
528	210	-66	569	239	-71.125	610	262	-76.25	651	28B	-81.375
529	211	-66.125	570	23A	-71.25	611	263	-76.375	652	28C	-81.5
530	212	-66.25	571	23B	-71.375	612	264	-76.5	653	28D	-81.625
531	213	-66.375	572	23C	-71.5	613	265	-76.625	654	28E	-81.75
532	214	-66.5	573	23D	-71.625	614	266	-76.75	655	28F	-81.875
533	215	-66.625	574	23E	-71.75	615	267	-76.875	656	290	-82
534	216	-66.75	575	23F	-71.875	616	268	-77	657	291	-82.125
535	217	-66.875	576	240	-72	617	269	-77.125	658	292	-82.25
536	218	-67	577	241	-72.125	618	26A	-77.25	659	293	-82.375
537	219	-67.125	578	242	-72.25	619	26B	-77.375	660	294	-82.5
538	21A	-67.25	579	243	-72.375	620	26C	-77.5	661	295	-82.625
539	21B	-67.375	580	244	-72.5	621	26D	-77.625	662	296	-82.75
540	21C	-67.5	581	245	-72.625	622	26E	-77.75	663	297	-82.875
541	21D	-67.625	582	246	-72.75	623	26F	-77.875	664	298	-83
542	21E	-67.75	583	247	-72.875	624	270	-78	665	299	-83.125
543	21F	-67.875	584	248	-73	625	271	-78.125	666	29A	-83.25
544	220	-68	585	249	-73.125	626	272	-78.25	667	29B	-83.375
545	221	-68.125	586	24A	-73.25	627	273	-78.375	668	29C	-83.5
546	222	-68.25	587	24B	-73.375	628	274	-78.5	669	29D	-83.625
547	223	-68.375	588	24C	-73.5	629	275	-78.625	670	29E	-83.75
548	224	-68.5	589	24D	-73.625	630	276	-78.75	671	29F	-83.875
549	225	-68.625	590	24E	-73.75	631	277	-78.875	672	2A0	-84
550	226	-68.75	591	24F	-73.875	632	278	-79	673	2A1	-84.125
551	227	-68.875	592	250	-74	633	279	-79.125	674	2A2	-84.25
552	228	-69	593	251	-74.125	634	27A	-79.25	675	2A3	-84.375

No	Value (HEX)	dB	No	Value (HEX)	dB	No	Value (HEX)	dB	No	Value (HEX)	dB
676	2A4	-84.5	699	2BB	-87.375	722	2D2	-90.25	745	2E9	-93.125
677	2A5	-84.625	700	2BC	-87.5	723	2D3	-90.375	746	2EA	-93.25
678	2A6	-84.75	701	2BD	-87.625	724	2D4	-90.5	747	2EB	-93.375
679	2A7	-84.875	702	2BE	-87.75	725	2D5	-90.625	748	2EC	-93.5
680	2A8	-85	703	2BF	-87.875	726	2D6	-90.75	749	2ED	-93.625
681	2A9	-85.125	704	2C0	-88	727	2D7	-90.875	750	2EE	-93.75
682	2AA	-85.25	705	2C1	-88.125	728	2D8	-91	751	2EF	-93.875
683	2AB	-85.375	706	2C2	-88.25	729	2D9	-91.125	752	2F0	-94
684	2AC	-85.5	707	2C3	-88.375	730	2DA	-91.25	753	2F1	-94.125
685	2AD	-85.625	708	2C4	-88.5	731	2DB	-91.375	754	2F2	-94.25
686	2AE	-85.75	709	2C5	-88.625	732	2DC	-91.5	755	2F3	-94.375
687	2AF	-85.875	710	2C6	-88.75	733	2DD	-91.625	756	2F4	-94.5
688	2B0	-86	711	2C7	-88.875	734	2DE	-91.75	757	2F5	-94.625
689	2B1	-86.125	712	2C8	-89	735	2DF	-91.875	758	2F6	-94.75
690	2B2	-86.25	713	2C9	-89.125	736	2E0	-92	759	2F7	-94.875
691	2B3	-86.375	714	2CA	-89.25	737	2E1	-92.125	760	2F8	-95
692	2B4	-86.5	715	2CB	-89.375	738	2E2	-92.25	761	2F9	-95.125
693	2B5	-86.625	716	2CC	-89.5	739	2E3	-92.375	762	2FA	-95.25
694	2B6	-86.75	717	2CD	-89.625	740	2E4	-92.5	763	2FB	-95.375
695	2B7	-86.875	718	2CE	-89.75	741	2E5	-92.625	764	2FC	-95.5
696	2B8	-87	719	2CF	-89.875	742	2E6	-92.75	765	2FD	-95.625
697	2B9	-87.125	720	2D0	-90	743	2E7	-92.875	766	2FE	-95.75
698	2BA	-87.25	721	2D1	-90.125	744	2E8	-93	767	2FF	-95.875



**Table 34.12 Settings of MIXp\_MDBAR, MIXp\_MDBBR, MIXp\_MDBCR, and MIXp\_MDBDR and Corresponding Values in Decibels (No. 768 to 1023)**

No	Value (HEX)	dB	No	Value (HEX)	dB	No	Value (HEX)	dB	No	Value (HEX)	dB
768	300	-96	809	329	-101.125	850	352	-106.25	891	37B	-111.375
769	301	-96.125	810	32A	-101.25	851	353	-106.375	892	37C	-111.5
770	302	-96.25	811	32B	-101.375	852	354	-106.5	893	37D	-111.625
771	303	-96.375	812	32C	-101.5	853	355	-106.625	894	37E	-111.75
772	304	-96.5	813	32D	-101.625	854	356	-106.75	895	37F	-111.875
773	305	-96.625	814	32E	-101.75	855	357	-106.875	896	380	-112
774	306	-96.75	815	32F	-101.875	856	358	-107	897	381	-112.125
775	307	-96.875	816	330	-102	857	359	-107.125	898	382	-112.25
776	308	-97	817	331	-102.125	858	35A	-107.25	899	383	-112.375
777	309	-97.125	818	332	-102.25	859	35B	-107.375	900	384	-112.5
778	30A	-97.25	819	333	-102.375	860	35C	-107.5	901	385	-112.625
779	30B	-97.375	820	334	-102.5	861	35D	-107.625	902	386	-112.75
780	30C	-97.5	821	335	-102.625	862	35E	-107.75	903	387	-112.875
781	30D	-97.625	822	336	-102.75	863	35F	-107.875	904	388	-113
782	30E	-97.75	823	337	-102.875	864	360	-108	905	389	-113.125
783	30F	-97.875	824	338	-103	865	361	-108.125	906	38A	-113.25
784	310	-98	825	339	-103.125	866	362	-108.25	907	38B	-113.375
785	311	-98.125	826	33A	-103.25	867	363	-108.375	908	38C	-113.5
786	312	-98.25	827	33B	-103.375	868	364	-108.5	909	38D	-113.625
787	313	-98.375	828	33C	-103.5	869	365	-108.625	910	38E	-113.75
788	314	-98.5	829	33D	-103.625	870	366	-108.75	911	38F	-113.875
789	315	-98.625	830	33E	-103.75	871	367	-108.875	912	390	-114
790	316	-98.75	831	33F	-103.875	872	368	-109	913	391	-114.125
791	317	-98.875	832	340	-104	873	369	-109.125	914	392	-114.25
792	318	-99	833	341	-104.125	874	36A	-109.25	915	393	-114.375
793	319	-99.125	834	342	-104.25	875	36B	-109.375	916	394	-114.5
794	31A	-99.25	835	343	-104.375	876	36C	-109.5	917	395	-114.625
795	31B	-99.375	836	344	-104.5	877	36D	-109.625	918	396	-114.75
796	31C	-99.5	837	345	-104.625	878	36E	-109.75	919	397	-114.875
797	31D	-99.625	838	346	-104.75	879	36F	-109.875	920	398	-115
798	31E	-99.75	839	347	-104.875	880	370	-110	921	399	-115.125
799	31F	-99.875	840	348	-105	881	371	-110.125	922	39A	-115.25
800	320	-100	841	349	-105.125	882	372	-110.25	923	39B	-115.375
801	321	-100.125	842	34A	-105.25	883	373	-110.375	924	39C	-115.5
802	322	-100.25	843	34B	-105.375	884	374	-110.5	925	39D	-115.625
803	323	-100.375	844	34C	-105.5	885	375	-110.625	926	39E	-115.75
804	324	-100.5	845	34D	-105.625	886	376	-110.75	927	39F	-115.875
805	325	-100.625	846	34E	-105.75	887	377	-110.875	928	3A0	-116
806	326	-100.75	847	34F	-105.875	888	378	-111	929	3A1	-116.125
807	327	-100.875	848	350	-106	889	379	-111.125	930	3A2	-116.25
808	328	-101	849	351	-106.125	890	37A	-111.25	931	3A3	-116.375

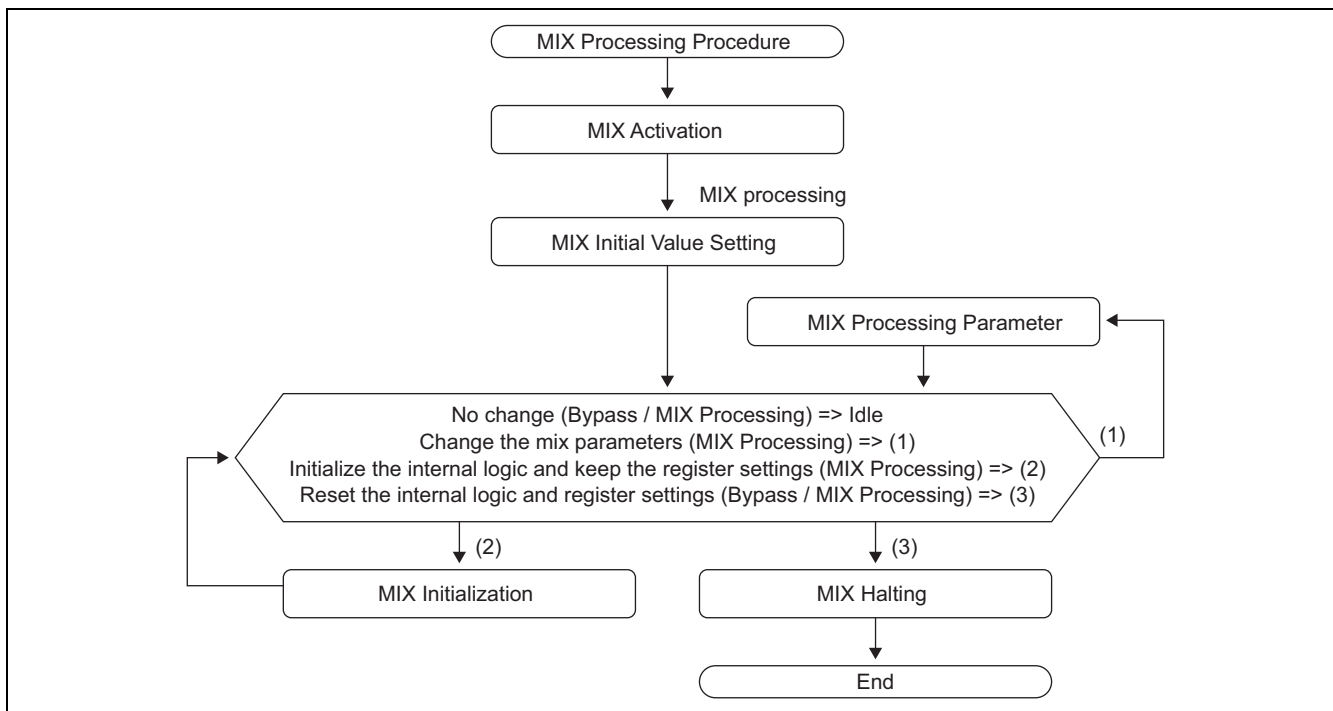
No	Value (HEX)	dB	No	Value (HEX)	dB	No	Value (HEX)	dB	No	Value (HEX)	dB
932	3A4	-116.5	955	3BB	-119.375	978	3D2	-122.25	1001	3E9	-125.125
933	3A5	-116.625	956	3BC	-119.5	979	3D3	-122.375	1002	3EA	-125.25
934	3A6	-116.75	957	3BD	-119.625	980	3D4	-122.5	1003	3EB	-125.375
935	3A7	-116.875	958	3BE	-119.75	981	3D5	-122.625	1004	3EC	-125.5
936	3A8	-117	959	3BF	-119.875	982	3D6	-122.75	1005	3ED	-125.625
937	3A9	-117.125	960	3C0	-120	983	3D7	-122.875	1006	3EE	-125.75
938	3AA	-117.25	961	3C1	-120.125	984	3D8	-123	1007	3EF	-125.875
939	3AB	-117.375	962	3C2	-120.25	985	3D9	-123.125	1008	3F0	-126
940	3AC	-117.5	963	3C3	-120.375	986	3DA	-123.25	1009	3F1	-126.125
941	3AD	-117.625	964	3C4	-120.5	987	3DB	-123.375	1010	3F2	-126.25
942	3AE	-117.75	965	3C5	-120.625	988	3DC	-123.5	1011	3F3	-126.375
943	3AF	-117.875	966	3C6	-120.75	989	3DD	-123.625	1012	3F4	-126.5
944	3B0	-118	967	3C7	-120.875	990	3DE	-123.75	1013	3F5	-126.625
945	3B1	-118.125	968	3C8	-121	991	3DF	-123.875	1014	3F6	-126.75
946	3B2	-118.25	969	3C9	-121.125	992	3E0	-124	1015	3F7	-126.875
947	3B3	-118.375	970	3CA	-121.25	993	3E1	-124.125	1016	3F8	-127
948	3B4	-118.5	971	3CB	-121.375	994	3E2	-124.25	1017	3F9	-127.125
949	3B5	-118.625	972	3CC	-121.5	995	3E3	-124.375	1018	3FA	-127.25
950	3B6	-118.75	973	3CD	-121.625	996	3E4	-124.5	1019	3FB	-127.375
951	3B7	-118.875	974	3CE	-121.75	997	3E5	-124.625	1020	3FC	-127.5
952	3B8	-119	975	3CF	-121.875	998	3E6	-124.75	1021	3FD	-127.625
953	3B9	-119.125	976	3D0	-122	999	3E7	-124.875	1022	3FE	-127.75
954	3BA	-119.25	977	3D1	-122.125	1000	3E8	-125	1023	3FF	-∞

**(a) Register Setting Procedure**

The following describes the MIX register setting procedures. The register should be used according to the following procedures.

- MIX Processing Procedure

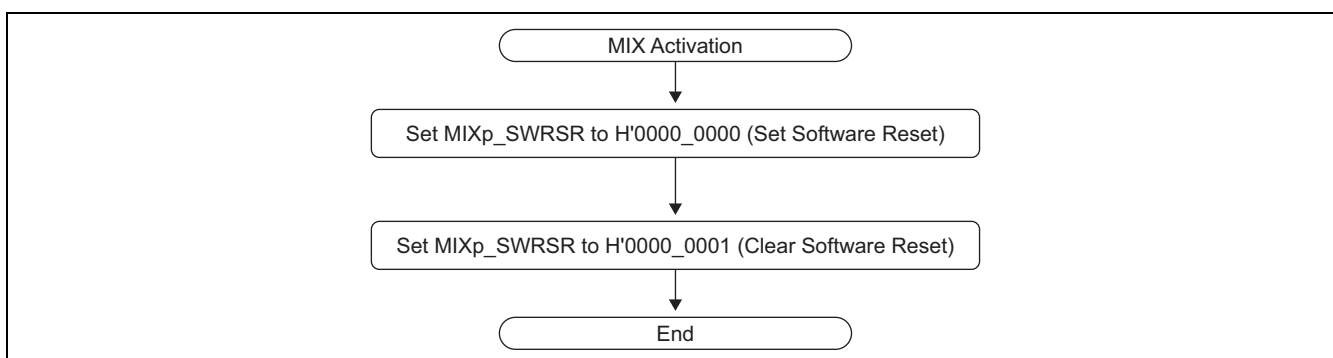
Figure 34.20 shows the processing procedure of MIX.



**Figure 34.20 MIX Processing Procedure**

- MIX Activation

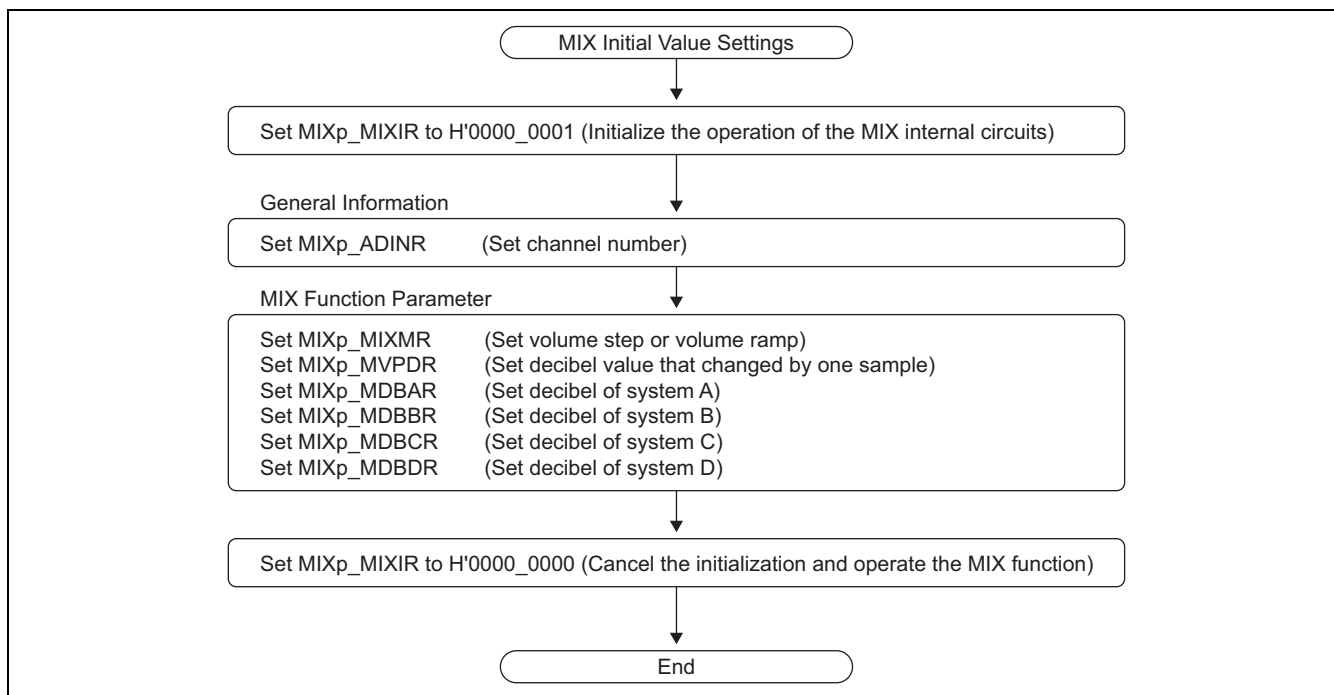
Figure 34.21 shows the MIX activation flowchart. When the MIX is activated, a software reset should be set to initialize logic and register setting. Then, the software reset should be cleared and ready to operate MIX. When reset the MIX function, all registers are initialized. If the MIX function was initialized by a hardware reset, it doesn't need to initialize the MIX function by software reset.



**Figure 34.21 MIX Activation Flowchart**

- MIX Initial Value Setting

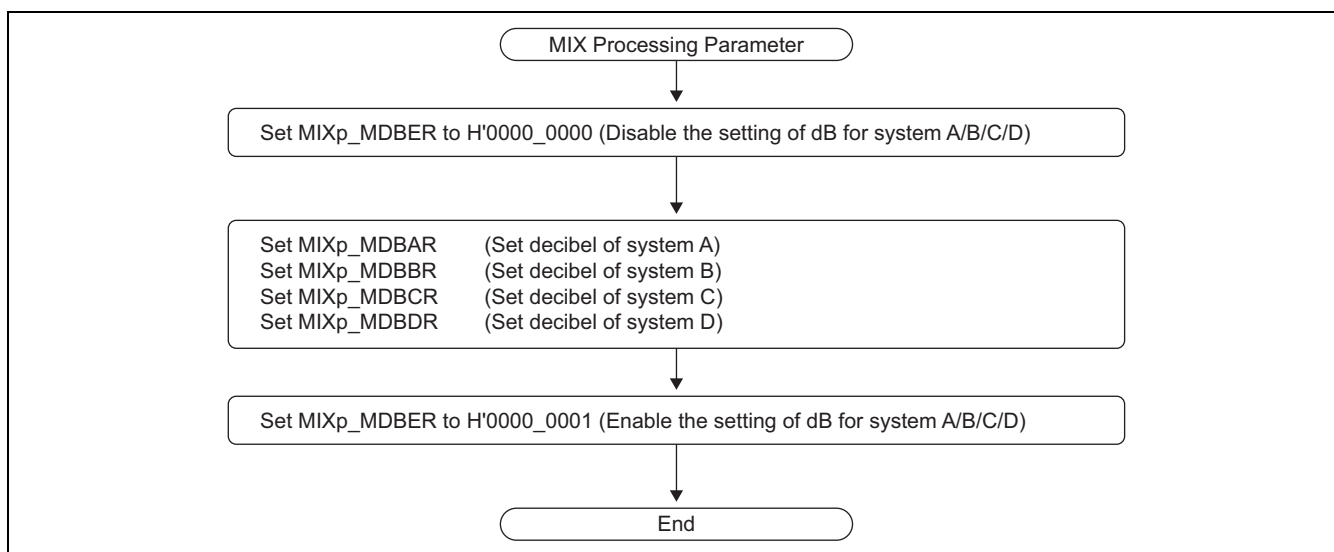
Figure 34.22 shows the flowchart of the MIX initial value setting. Before operate MIX function, the initial values should be set. After set the register setting and cancel the initialization, MIX module changes the volume of each system by volume step to the dB value of MIXp\_MDBAR and MIXp\_MDBBR and MIXp\_MDBCR and MIXp\_MDBDR regardless of MIXp\_MIXMR setting.



**Figure 34.22 MIX Initial Value Setting Flowchart**

- MIX Processing Parameter

Figure 34.23 shows the MIX processing parameter flowchart. Before change the parameter of decibel for each system, the setting of the MIXp\_MDBER should be disables. After that set the decibels of MIXp\_MDBAR and MIXp\_MDBBR and MIXp\_MDBCR and MIXp\_MDBDR and enables the MIXp\_MDBER for reflect the decibel setting to the MIX processing.



**Figure 34.23 MIX Processing Parameter Flowchart**

- MIX Initialization

Figure 34.24 shows the MIX initialization flowchart. MIXp\_MIXIR register doesn't initialize the register settings and these values are maintained. Before cancel the initialization, it is necessary to set or check the register settings of peripheral IP.

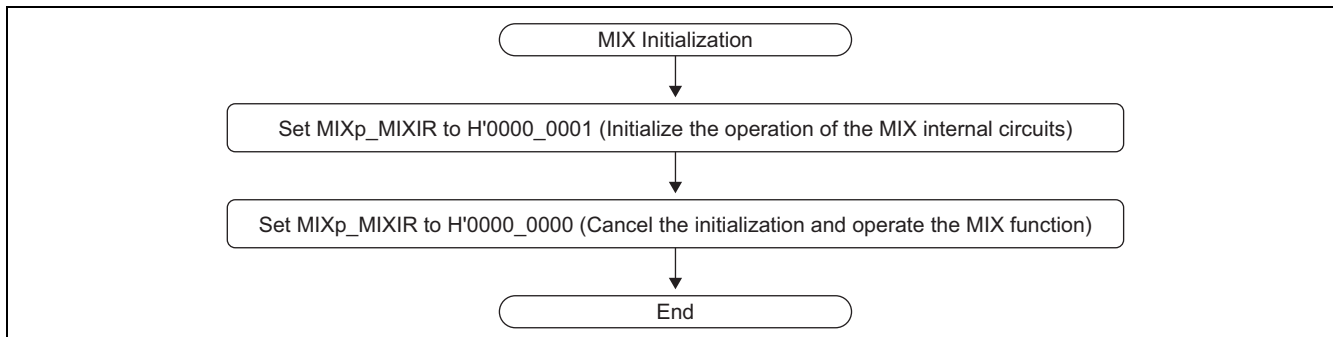


Figure 34.24 MIX Initialization Flowchart

- MIX Halting

Figure 34.25 shows the flowchart of MIX halting. When MIX is halting, it should be initialize or reset by software reset or hardware reset. Before initialize or reset the MIX function, it is necessary to confirm the register settings and operation of peripheral IP.

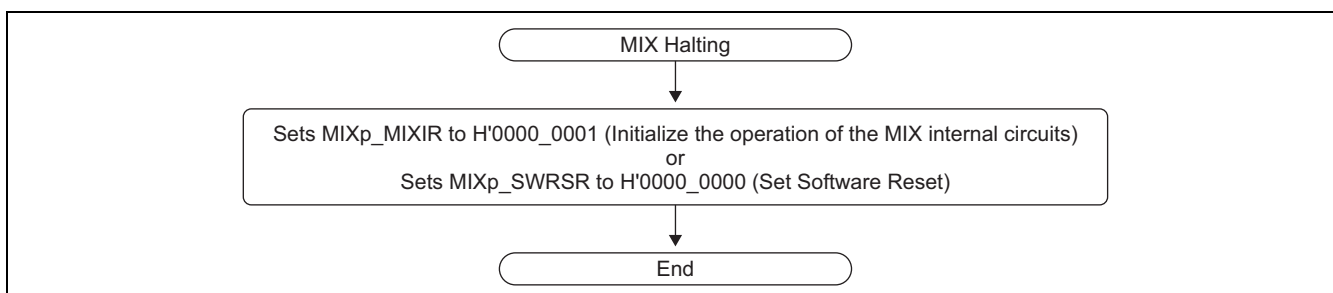


Figure 34.25 MIX Halting Flowchart

**(3) DVC Block**

The DVC is a block for implementing the volume and mute functions.

- Volume control function including digital volume, volume ramp, and zero-crossing mute
- The digital volume function is specified by a 24-bit fixed-point value within the range from 0 to 8 times (mute or -120 to 18 dB)
- The volume ramp function can be used for soft mute, fade-in, fade-out, or desired volume adjustment
- The volume ramp period can be changed within the sampling range from the 0th to 23rd power of 2
- The zero-crossing mute function silences the sound at the zero-crossing point of the audio data

Table 34.13 shows the DVC functions.

**Table 34.13 DVC Functions**

Item	Performance
Digital volume	Range: -120 dB to 18 dB ( $9.5 \times 10^{-7}$ times to 8 times)
Volume ramp	Volume ramp is used for many kinds of operation (soft mute, fade-in, fade-out, and volume adjustment by ramp) Ramp period: $2^0/f_{so}$ to $2^{23}/f_{so}$ Examples: (1/ $f_{so}$ ): -128 dB/1 step (2/ $f_{so}$ ): -64 dB/1 step (4/ $f_{so}$ ): -32 dB/1 step : (128/ $f_{so}$ ): -1 dB/1 step (256/ $f_{so}$ ): -0.5 dB/1 step (512/ $f_{so}$ ): -0.25 dB/1 step (1024/ $f_{so}$ ): -0.125 dB/1 step (2048/ $f_{so}$ ): -0.125 dB/2 steps (4096/ $f_{so}$ ): -0.125 dB/4 steps : (8388608/ $f_{so}$ ): -0.125 dB/8192 steps)
Zero-crossing mute	Mute the signal at zero-crossing point

The settings and corresponding values for the volume ramp are the same as those listed in Tables 34.9 to 34.12.

The settings and corresponding values for the digital volume are calculated by using the following formula:

$$\text{Setting (decimal)} = 10^X \times 1048576$$

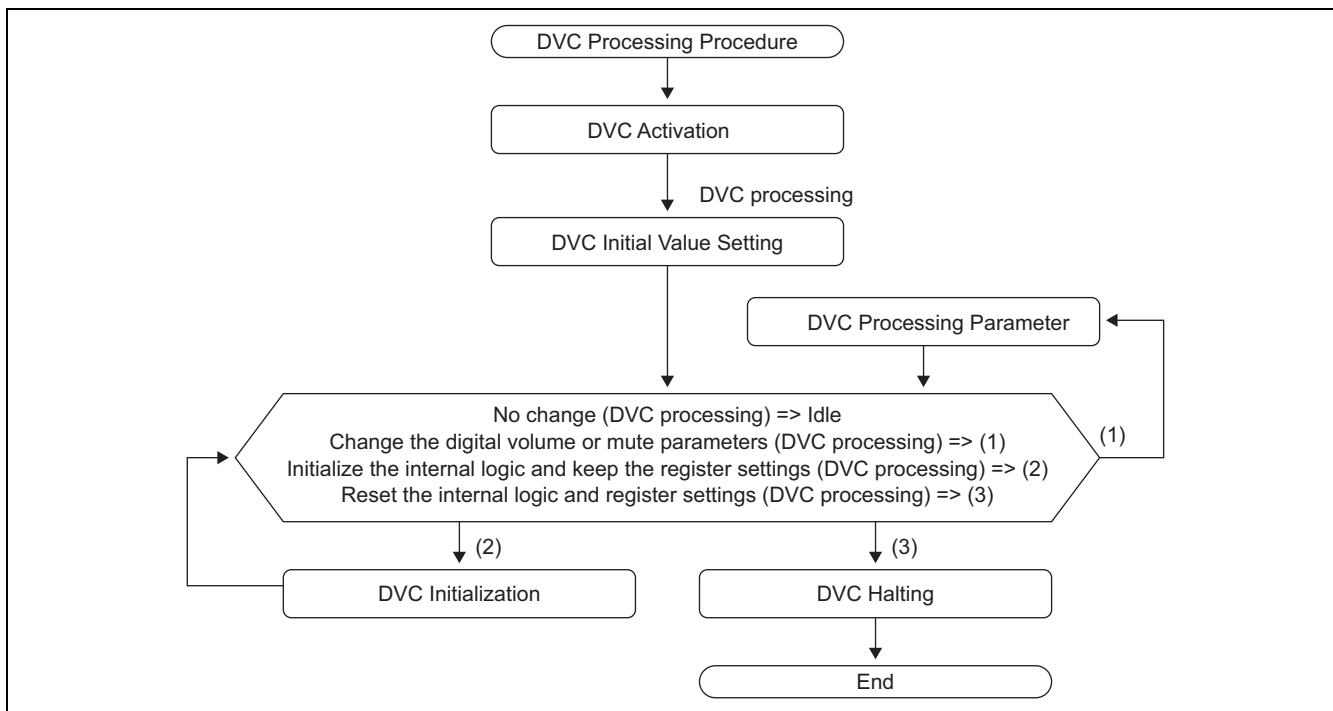
$$X = (\text{value in dB}) / 20$$

**(a) Register Setting Procedure**

The following describes the DVC register setting procedures. The register should be used according to the following procedures.

- DVC Processing Procedure

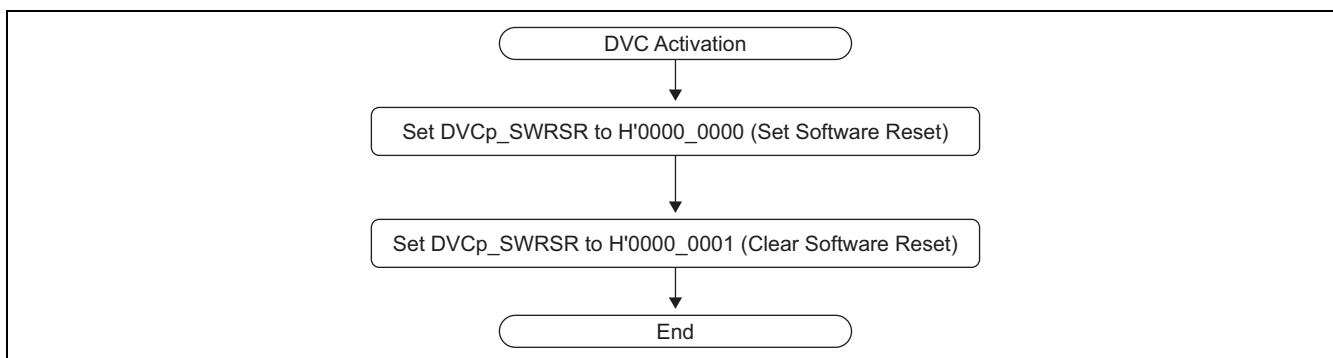
Figure 34.26 shows the processing procedure of DVC.



**Figure 34.26 DVC Processing Procedure**

- DVC Activation

Figure 34.27 shows the DVC activation flowchart. When the DVC is activated, a software reset should be set to initialize logic and register setting. Then, the software reset should be cleared and ready to operate DVC. When reset the DVC function, all registers are initialized. If the DVC function was initialized by a hardware reset, it doesn't need to initialize the DVC function by software reset.



**Figure 34.27 DVC Activation Flowchart**

- DVC Initial Value Setting

Figure 34.28 shows the flowchart of the DVC initial value setting. Before operate DVC function, the initial values should be set.

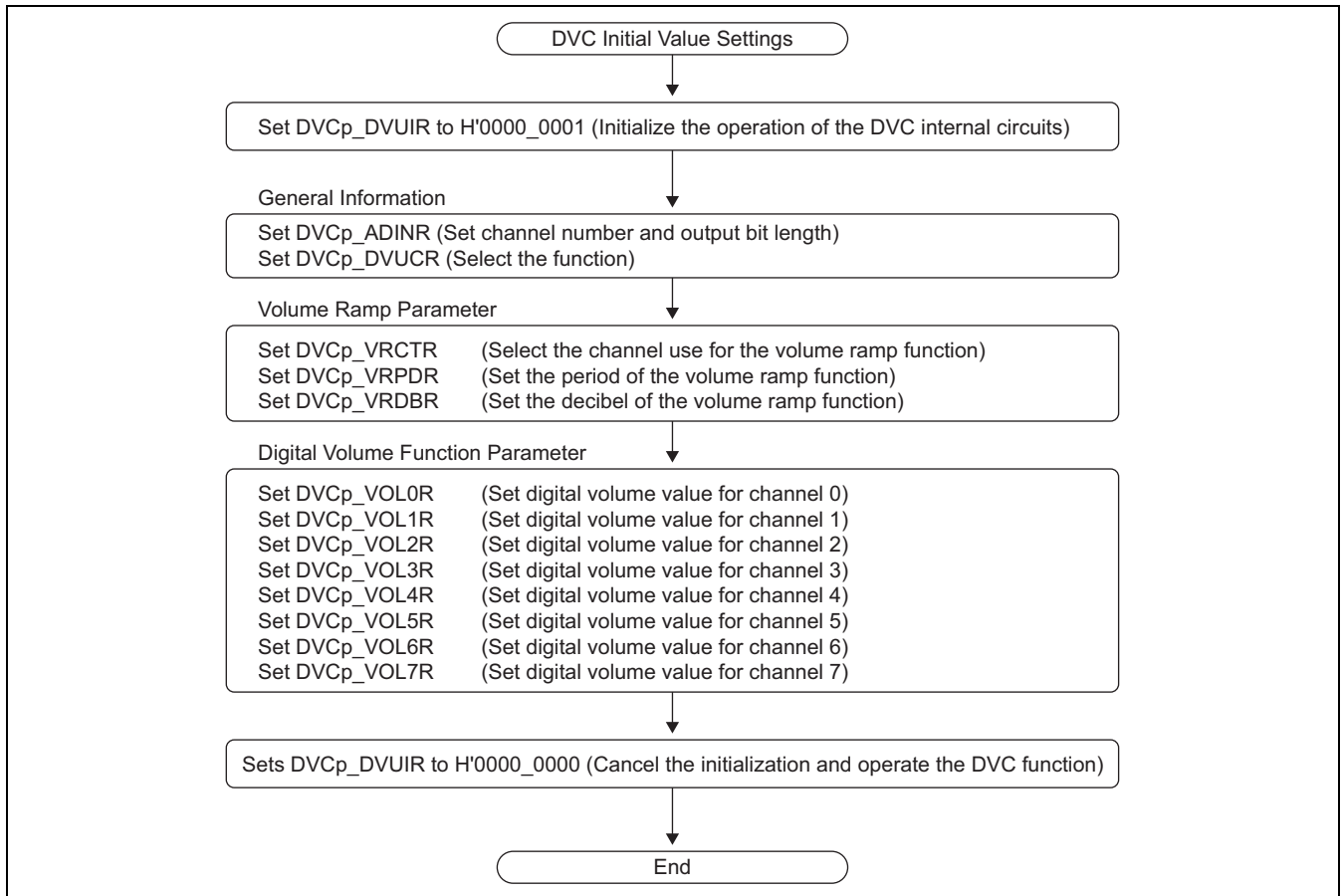


Figure 34.28 DVC Initial Value Setting Flowchart



- DVC Processing Parameter

Figure 34.29 shows the DVC processing parameter flowchart. When DVC is processing, user can control the zero cross mute and the volume ramp and the digital volume value or by changing the setting value of registers. Before change the parameter of each function, the setting of DVCp\_DVUER should be disables. After that set the setting of each function and enables the DVCp\_DVUER for reflect the register setting to the DVC processing.

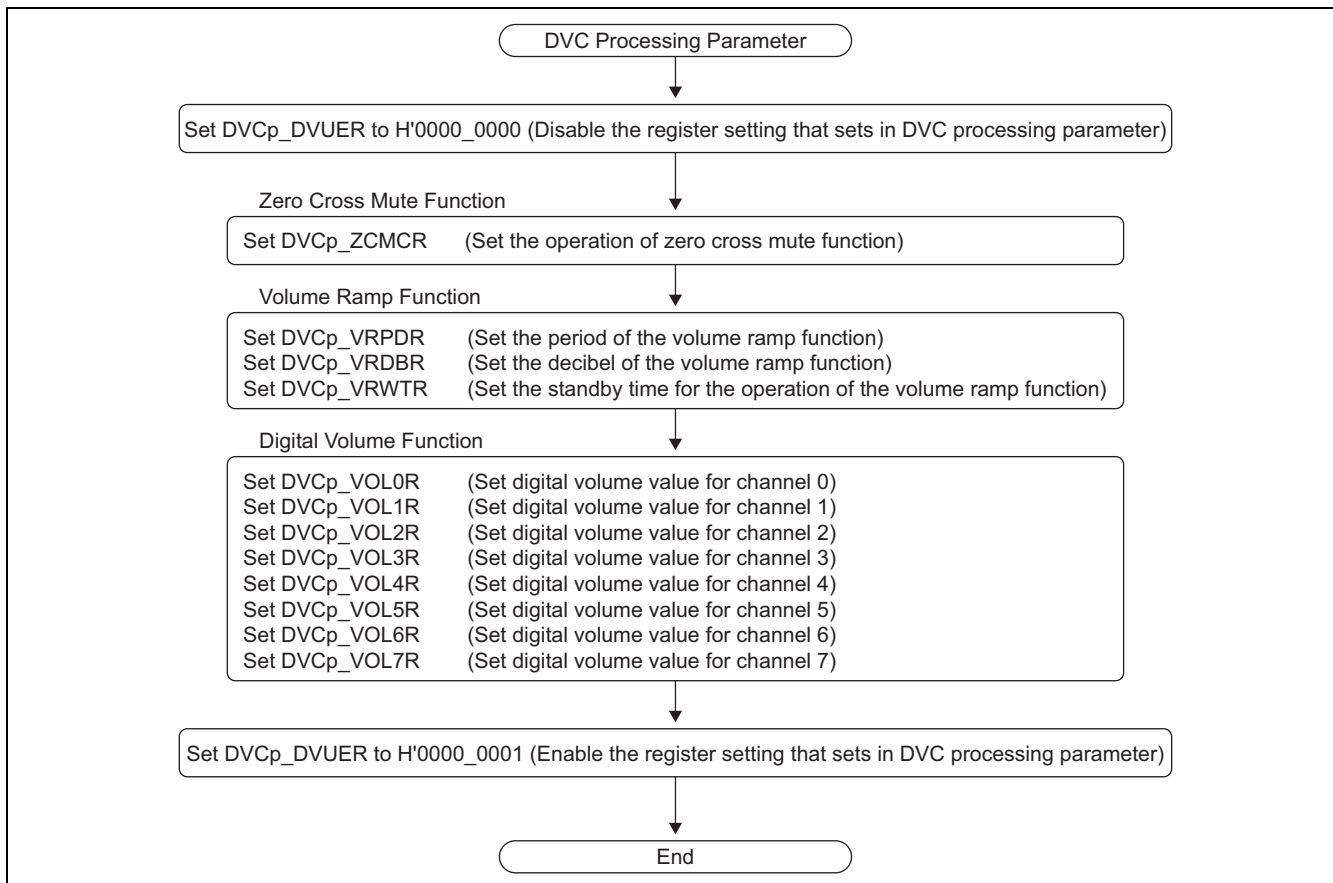
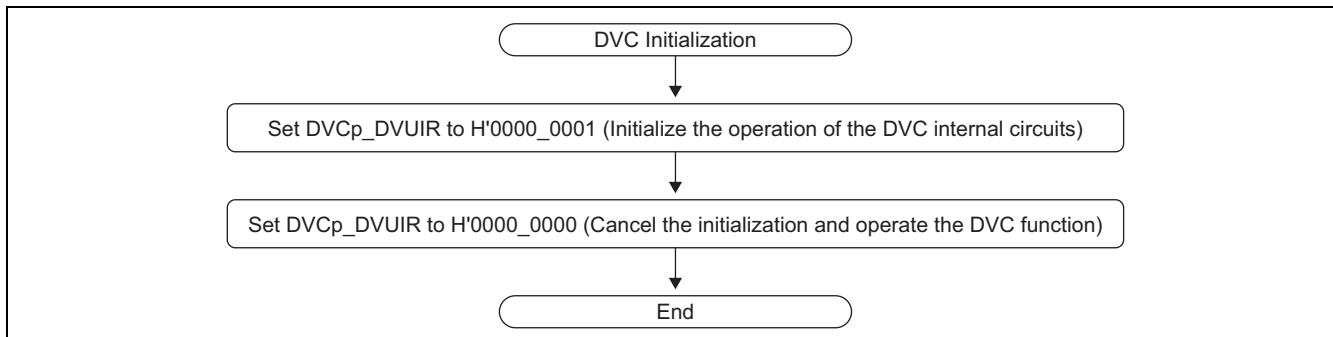


Figure 34.29 DVC Processing Parameter Flowchart

- DVC Initialization

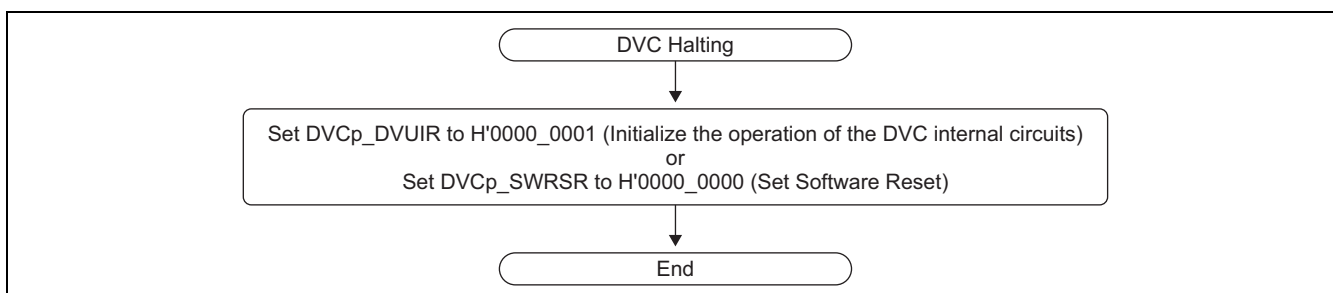
Figure 34.30 shows the flowchart of DVC Initialization. DVCp\_DVUIR register doesn't initialize the register settings and these values are maintained. Before cancel the initialization, it is necessary to set or check the register settings of peripheral IP.



**Figure 34.30 DVC Initialization Flowchart**

- DVC Halting

Figure 34.31 shows the flowchart of DVC halting. When DVC is halting, it should be initialize or reset by software reset or hardware reset. Before initialize or reset the DVC function, it is necessary to confirm the register settings and operation of peripheral IP.



**Figure 34.31 DVC Halting Flowchart**

### 34.3.8 Input Data Timing and Output Data Timing

When using the SRC or CMD, the input data timing and output data timing should be specified. For details of the settings, refer to section 33, Audio Clock Generator (ADG).

## 35. Direct Memory Access Controller for Audio (Audio-DMAC)

RZ/G1H

RZ/G1N

RZ/G1M

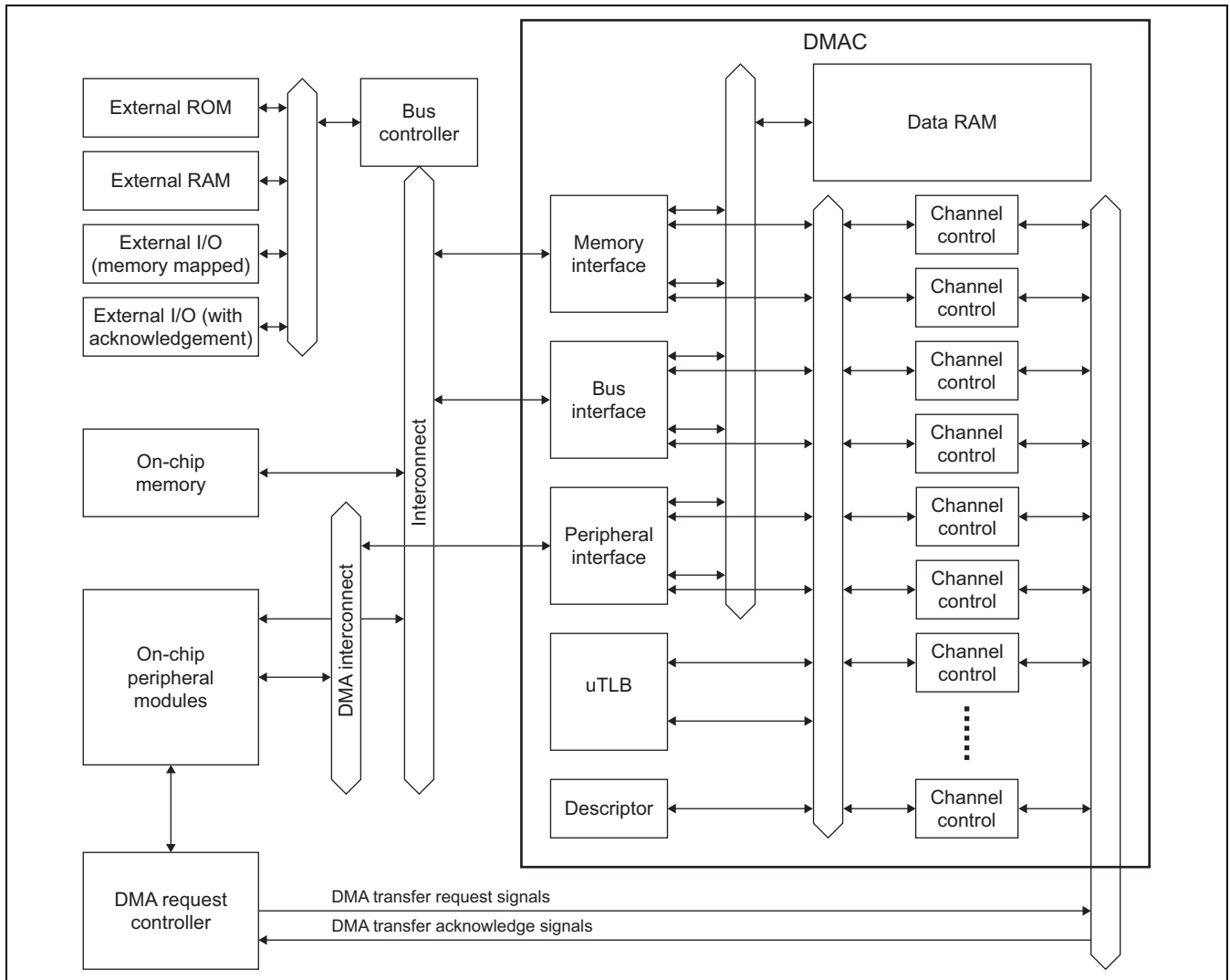
RZ/G1E

This LSI includes a direct memory access controller for audio (audio-DMAC). The audio-DMAC can be used in place of the CPU to handle high-speed data transfer to and from an external memory, the on-chip memory, memory-mapped external devices, or on-chip peripheral modules.

### 35.1 Features

- Up to 26 channels are available.  
RZ/G1H/M/N: 26 channels (channels 0 to 25)  
RZ/G1E: 13 channels (channels 0 to 12)
- 4-Gbyte physical address space
- Transfer data length: Byte, word (2 bytes), longword (4 bytes), 8 bytes, 16 bytes, 32 bytes, and 64 bytes
- Maximum number of transfer times: 16,777,216
- Address mode: Dual address mode
- Transfer requests:  
Requests from on-chip peripheral modules or auto requests can be selected. The following modules can issue on-chip peripheral module requests.  
SSI0 to SSI9, SCU0 to SCU9
- Selectable bus modes:  
Normal speed mode or slow mode can be selected for each channel.
- Either fixed priority or round-robin arbitration can be selected for use in arbitration among the transfer channels.
- Interrupt request:  
The audio-DMAC can be set up to generate an interrupt request for the CPU upon completion of transfer under the control of one stage of the descriptor memory, at the end of the data transfer, in response to an MMU error, and in response to an address error.
- Descriptor memory function:  
Up to 128 sets of the settings for the source address register, destination address register, and transfer count register are available (if use of the descriptor memory is only enabled for one channel) for use in setting up consecutive DMA transfers (the memory can hold register values for up to 256 stages of transfer when the external memory is selected). An infinite repeat mode is also available.

Figure 35.1 shows the block diagram of the audio-DMAC.



**Figure 35.1 Block Diagram of the Audio-DMAC**

### 35.2 Input/Output Pins

There are no external pins relevant to the audio-DMAC.

### 35.3 Register Descriptions

Table 35.1 lists the registers of the audio-DMAC. Table 35.2 shows the register states of the audio-DMAC in each operating mode.

Note: The number of the audio-DMAC channels and the registers in use depend on the product:  
 26 channels for the RZ/G1H and RZ/G1M/N (registers for both the higher- and lower-numbered sets of channels 0 to 12 and 13 to 25 are in use)  
 13 channels for the RZ/G1E (only the registers for the higher-numbered channels 0 to 12 are in use)

**Table 35.1 Register Configuration of the Audio-DMAC**

Name	Abbreviation	R/W	Address	Access Size	RZ/G Series Products			
					RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
DMA interrupt status register (for lower-numbered channels)	DMAISTA_L	R	H'EC70 0020	32	√	√	√	√
DMA secure control register (for lower-numbered channels)	DMASEC_L	R/W	H'EC70 0030	32	√	√	√	√
DMA operation register (for lower-numbered channels)	DMAOR_L	R/W	H'EC70 0060	16	√	√	√	√
DMA channel clear register (for lower-numbered channels)	DMACHCLR_L	W	H'EC70 0080	32	√	√	√	√
DPRAM secure control register (for lower-numbered channels)	DMADPSEC_L	R/W	H'EC70 00A0	32	√	√	√	√
DMA source address register_0	DMASAR_0	R/W	H'EC70 8000 H'EC70 8020*	32	√	√	√	√
DMA destination address register_0	DMADAR_0	R/W	H'EC70 8004 H'EC70 8024*	32	√	√	√	√
DMA transfer count register_0	DMATCR_0	R/W	H'EC70 8008	32	√	√	√	√
DMA transfer size register_0	DMATSR_0	R/W	H'EC70 8028*	32	√	√	√	√
DMA channel control register_0	DMACHCR_0	R/W	H'EC70 800C H'EC70 802C*	32	√	√	√	√
DMA transfer count register B_0	DMATCRB_0	R/W	H'EC70 8018	32	√	√	√	√
DMA transfer size register B_0	DMATSRB_0	R/W	H'EC70 8038	32	√	√	√	√
DMA channel control register B_0	DMACHCRB_0	R/W	H'EC70 801C	32	√	√	√	√
DMA extended resource selector_0	DMARS_0	R/W	H'EC70 8040	16	√	√	√	√
DMA buffer control register_0	DMABUFCR_0	R/W	H'EC70 8048	32	√	√	√	√
DMA descriptor base address register_0	DMADPBASE_0	R/W	H'EC70 8050	32	√	√	√	√
DMA descriptor control register_0	DMADPCR_0	R/W	H'EC70 8054	32	√	√	√	√
DMA fixed source address register_0	DMAFIXSAR_0	R/W	H'EC70 8010	32	√	√	√	√
DMA fixed destination address register_0	DMAFIXDAR_0	R/W	H'EC70 8014	32	√	√	√	√
DMA fixed descriptor base address register_0	DMAFIXDP BASE_0	R/W	H'EC70 8060	32	√	√	√	√
DMA source address register_1	DMASAR_1	R/W	H'EC70 8080 H'EC70 80A0*	32	√	√	√	√

Name	Abbreviation	R/W	Address	Access Size	RZ/G Series Products			
					RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
DMA destination address register_1	DMADAR_1	R/W	H'EC70 8084 H'EC70 80A4*	32	√	√	√	√
DMA transfer count register_1	DMATCR_1	R/W	H'EC70 8088	32	√	√	√	√
DMA transfer size register_1	DMATSR_1	R/W	H'EC70 80A8*	32	√	√	√	√
DMA channel control register_1	DMACHCR_1	R/W	H'EC70 808C H'EC70 80AC*	32	√	√	√	√
DMA transfer count register B_1	DMATCRB_1	R/W	H'EC70 8098	32	√	√	√	√
DMA transfer size register B_1	DMATSRB_1	R/W	H'EC70 80B8*	32	√	√	√	√
DMA channel control register B_1	DMACHCRB_1	R/W	H'EC70 809C	32	√	√	√	√
DMA extended resource selector_1	DMARS_1	R/W	H'EC70 80C0	16	√	√	√	√
DMA buffer control register_1	DMABUFCR_1	R/W	H'EC70 80C8	32	√	√	√	√
DMA descriptor base address register_1	DMADPBASE_1	R/W	H'EC70 80D0	32	√	√	√	√
DMA descriptor control register_1	DMADPCR_1	R/W	H'EC70 80D4	32	√	√	√	√
DMA fixed descriptor base address register_1	DMAFIXDPBASE_1	R/W	H'EC70 80E0	32	√	√	√	√
DMA fixed source address register_1	DMAFIXSAR_1	R/W	H'EC70 8090	32	√	√	√	√
DMA fixed destination address register_1	DMAFIXDAR_1	R/W	H'EC70 8094	32	√	√	√	√
DMA source address register_2	DMASAR_2	R/W	H'EC70 8100 H'EC70 8120*	32	√	√	√	√
DMA destination address register_2	DMADAR_2	R/W	H'EC70 8104 H'EC70 8124*	32	√	√	√	√
DMA transfer count register_2	DMATCR_2	R/W	H'EC70 8108	32	√	√	√	√
DMA transfer size register_2	DMATSR_2	R/W	H'EC70 8128*	32	√	√	√	√
DMA channel control register_2	DMACHCR_2	R/W	H'EC70 810C H'EC70 812C*	32	√	√	√	√
DMA transfer count register B_2	DMATCRB_2	R/W	H'EC70 8118	32	√	√	√	√
DMA transfer size register B_2	DMATSRB_2	R/W	H'EC70 8138*	32	√	√	√	√
DMA channel control register B_2	DMACHCRB_2	R/W	H'EC70 811C	32	√	√	√	√
DMA extended resource selector_2	DMARS_2	R/W	H'EC70 8140	16	√	√	√	√
DMA buffer control register_2	DMABUFCR_2	R/W	H'EC70 8148	32	√	√	√	√
DMA descriptor base address register_2	DMADPBASE_2	R/W	H'EC70 8150	32	√	√	√	√
DMA descriptor control register_2	DMADPCR_2	R/W	H'EC70 8154	32	√	√	√	√
DMA fixed source address register_2	DMAFIXSAR_2	R/W	H'EC70 8110	32	√	√	√	√
DMA fixed destination address register_2	DMAFIXDAR_2	R/W	H'EC70 8114	32	√	√	√	√
DMA fixed descriptor base address register_2	DMAFIXDPBASE_2	R/W	H'EC70 8160	32	√	√	√	√
DMA source address register_3	DMASAR_3	R/W	H'EC70 8180 H'EC70 81A0*	32	√	√	√	√
DMA destination address register_3	DMADAR_3	R/W	H'EC70 8184 H'EC70 81A4*	32	√	√	√	√

Name	Abbreviation	R/W	Address	Access Size	RZ/G Series Products			
					RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
DMA transfer count register_3	DMATCR_3	R/W	H'EC70 8188	32	√	√	√	√
DMA transfer size register_3	DMATSR_3	R/W	H'EC70 81A8*	32	√	√	√	√
DMA channel control register_3	DMACHCR_3	R/W	H'EC70 818C H'EC70 81AC*	32	√	√	√	√
DMA transfer count register B_3	DMATCRB_3	R/W	H'EC70 8198	32	√	√	√	√
DMA transfer size register B_3	DMATSRB_3	R/W	H'EC70 81B8*	32	√	√	√	√
DMA channel control register B_3	DMACHCRB_3	R/W	H'EC70 819C	32	√	√	√	√
DMA extended resource selector_3	DMARS_3	R/W	H'EC70 81C0	16	√	√	√	√
DMA buffer control register_3	DMABUFCR_3	R/W	H'EC70 81C8	32	√	√	√	√
DMA descriptor base address register_3	DMADPBASE_3	R/W	H'EC70 81D0	32	√	√	√	√
DMA descriptor control register_3	DMADPCR_3	R/W	H'EC70 81D4	32	√	√	√	√
DMA fixed source address register_3	DMAFIXSAR_3	R/W	H'EC70 8190	32	√	√	√	√
DMA fixed destination address register_3	DMAFIXDAR_3	R/W	H'EC70 8194	32	√	√	√	√
DMA fixed descriptor base address register_3	DMAFIXDPBASE_3	R/W	H'EC70 81E0	32	√	√	√	√
DMA source address register_4	DMASAR_4	R/W	H'EC70 8200 H'EC70 8220*	32	√	√	√	√
DMA destination address register_4	DMADAR_4	R/W	H'EC70 8204 H'EC70 8224*	32	√	√	√	√
DMA transfer count register_4	DMATCR_4	R/W	H'EC70 8208	32	√	√	√	√
DMA transfer size register_4	DMATSR_4	R/W	H'EC70 8228*	32	√	√	√	√
DMA channel control register_4	DMACHCR_4	R/W	H'EC70 820C H'EC70 822C*	32	√	√	√	√
DMA transfer count register B_4	DMATCRB_4	R/W	H'EC70 8218	32	√	√	√	√
DMA transfer size register B_4	DMATSRB_4	R/W	H'EC70 8238*	32	√	√	√	√
DMA channel control register B_4	DMACHCRB_4	R/W	H'EC70 821C	32	√	√	√	√
DMA extended resource selector_4	DMARS_4	R/W	H'EC70 8240	16	√	√	√	√
DMA buffer control register_4	DMABUFCR_4	R/W	H'EC70 8248	32	√	√	√	√
DMA descriptor base address register_4	DMADPBASE_4	R/W	H'EC70 8250	32	√	√	√	√
DMA descriptor control register_4	DMADPCR_4	R/W	H'EC70 8254	32	√	√	√	√
DMA fixed source address register_4	DMAFIXSAR_4	R/W	H'EC70 8210	32	√	√	√	√
DMA fixed destination address register_4	DMAFIXDAR_4	R/W	H'EC70 8214	32	√	√	√	√
DMA fixed descriptor base address register_4	DMAFIXDPBASE_4	R/W	H'EC70 8260	32	√	√	√	√
DMA source address register_5	DMASAR_5	R/W	H'EC70 8280 H'EC70 82A0*	32	√	√	√	√
DMA destination address register_5	DMADAR_5	R/W	H'EC70 8284 H'EC70 82A4*	32	√	√	√	√
DMA transfer count register_5	DMATCR_5	R/W	H'EC70 8288	32	√	√	√	√
DMA transfer size register_5	DMATSR_5	R/W	H'EC70 82A8*	32	√	√	√	√

Name	Abbreviation	R/W	Address	Access Size	RZ/G Series Products			
					RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
DMA channel control register_5	DMACHCR_5	R/W	H'EC70 828C H'EC70 82AC*	32	√	√	√	√
DMA transfer count register B_5	DMATCRB_5	R/W	H'EC70 8298	32	√	√	√	√
DMA transfer size register B_5	DMATSRB_5	R/W	H'EC70 82B8*	32	√	√	√	√
DMA channel control register B_5	DMACHCRB_5	R/W	H'EC70 829C	32	√	√	√	√
DMA extended resource selector_5	DMARS_5	R/W	H'EC70 82C0	16	√	√	√	√
DMA buffer control register_5	DMABUFCR_5	R/W	H'EC70 82C8	32	√	√	√	√
DMA descriptor base address register_5	DMADPBASE_5	R/W	H'EC70 82D0	32	√	√	√	√
DMA descriptor control register_5	DMADPCR_5	R/W	H'EC70 82D4	32	√	√	√	√
DMA fixed source address register_5	DMAFIXSAR_5	R/W	H'EC70 8290	32	√	√	√	√
DMA fixed destination address register_5	DMAFIXDAR_5	R/W	H'EC70 8294	32	√	√	√	√
DMA fixed descriptor base address register_5	DMAFIXDPBASE_5	R/W	H'EC70 82E0	32	√	√	√	√
DMA source address register_6	DMASAR_6	R/W	H'EC70 8300 H'EC70 8320*	32	√	√	√	√
DMA destination address register_6	DMADAR_6	R/W	H'EC70 8304 H'EC70 8324*	32	√	√	√	√
DMA transfer count register_6	DMATCR_6	R/W	H'EC70 8308	32	√	√	√	√
DMA transfer size register_6	DMATSR_6	R/W	H'EC70 8328*	32	√	√	√	√
DMA channel control register_6	DMACHCR_6	R/W	H'EC70 830C H'EC70 832C*	32	√	√	√	√
DMA transfer count register B_6	DMATCRB_6	R/W	H'EC70 8318	32	√	√	√	√
DMA transfer size register B_6	DMATSRB_6	R/W	H'EC70 8338*	32	√	√	√	√
DMA channel control register B_6	DMACHCRB_6	R/W	H'EC70 831C	32	√	√	√	√
DMA extended resource selector_6	DMARS_6	R/W	H'EC70 8340	16	√	√	√	√
DMA buffer control register_6	DMABUFCR_6	R/W	H'EC70 8348	32	√	√	√	√
DMA descriptor base address register_6	DMADPBASE_6	R/W	H'EC70 8350	32	√	√	√	√
DMA descriptor control register_6	DMADPCR_6	R/W	H'EC70 8354	32	√	√	√	√
DMA fixed source address register_6	DMAFIXSAR_6	R/W	H'EC70 8310	32	√	√	√	√
DMA fixed destination address register_6	DMAFIXDAR_6	R/W	H'EC70 8314	32	√	√	√	√
DMA fixed descriptor base address register_6	DMAFIXDPBASE_6	R/W	H'EC70 8360	32	√	√	√	√
DMA source address register_7	DMASAR_7	R/W	H'EC70 8380 H'EC70 83A0*	32	√	√	√	√
DMA destination address register_7	DMADAR_7	R/W	H'EC70 8384 H'EC70 83A4*	32	√	√	√	√
DMA transfer count register_7	DMATCR_7	R/W	H'EC70 8388	32	√	√	√	√
DMA transfer size register_7	DMATSR_7	R/W	H'EC70 83A8*	32	√	√	√	√
DMA channel control register_7	DMACHCR_7	R/W	H'EC70 838C H'EC70 83AC*	32	√	√	√	√



Name	Abbreviation	R/W	Address	Access Size	RZ/G Series Products			
					RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
DMA transfer count register B_7	DMATCRB_7	R/W	H'EC70 8398	32	√	√	√	√
DMA transfer size register B_7	DMATSRB_7	R/W	H'EC70 83B8*	32	√	√	√	√
DMA channel control register B_7	DMACHCRB_7	R/W	H'EC70 839C	32	√	√	√	√
DMA extended resource selector_7	DMARS_7	R/W	H'EC70 83C0	16	√	√	√	√
DMA buffer control register_7	DMABUFCR_7	R/W	H'EC70 83C8	32	√	√	√	√
DMA descriptor base address register_7	DMADPBASE_7	R/W	H'EC70 83D0	32	√	√	√	√
DMA descriptor control register_7	DMADPCR_7	R/W	H'EC70 83D4	32	√	√	√	√
DMA fixed source address register_7	DMAFIXSAR_7	R/W	H'EC70 8390	32	√	√	√	√
DMA fixed destination address register_7	DMAFIXDAR_7	R/W	H'EC70 8394	32	√	√	√	√
DMA fixed descriptor base address register_7	DMAFIXDPBASE_7	R/W	H'EC70 83E0	32	√	√	√	√
DMA source address register_8	DMASAR_8	R/W	H'EC70 8400 H'EC70 8420*	32	√	√	√	√
DMA destination address register_8	DMADAR_8	R/W	H'EC70 8404 H'EC70 8424*	32	√	√	√	√
DMA transfer count register_8	DMATCR_8	R/W	H'EC70 8408	32	√	√	√	√
DMA transfer size register_8	DMATSR_8	R/W	H'EC70 8428*	32	√	√	√	√
DMA channel control register_8	DMACHCR_8	R/W	H'EC70 840C H'EC70 842C*	32	√	√	√	√
DMA transfer count register B_8	DMATCRB_8	R/W	H'EC70 8418	32	√	√	√	√
DMA transfer size register B_8	DMATSRB_8	R/W	H'EC70 8438*	32	√	√	√	√
DMA channel control register B_8	DMACHCRB_8	R/W	H'EC70 841C	32	√	√	√	√
DMA extended resource selector_8	DMARS_8	R/W	H'EC70 8440	16	√	√	√	√
DMA buffer control register_8	DMABUFCR_8	R/W	H'EC70 8448	32	√	√	√	√
DMA descriptor base address register_8	DMADPBASE_8	R/W	H'EC70 8450	32	√	√	√	√
DMA descriptor control register_8	DMADPCR_8	R/W	H'EC70 8454	32	√	√	√	√
DMA fixed source address register_8	DMAFIXSAR_8	R/W	H'EC70 8410	32	√	√	√	√
DMA fixed destination address register_8	DMAFIXDAR_8	R/W	H'EC70 8414	32	√	√	√	√
DMA fixed descriptor base address register_8	DMAFIXDPBASE_8	R/W	H'EC70 8460	32	√	√	√	√
DMA source address register_9	DMASAR_9	R/W	H'EC70 8480 H'EC70 84A0*	32	√	√	√	√
DMA destination address register_9	DMADAR_9	R/W	H'EC70 8484 H'EC70 84A4*	32	√	√	√	√
DMA transfer count register_9	DMATCR_9	R/W	H'EC70 8488	32	√	√	√	√
DMA transfer size register_9	DMATSR_9	R/W	H'EC70 84A8*	32	√	√	√	√
DMA channel control register_9	DMACHCR_9	R/W	H'EC70 848C H'EC70 84AC*	32	√	√	√	√
DMA transfer count register B_9	DMATCRB_9	R/W	H'EC70 8498	32	√	√	√	√
DMA transfer size register B_9	DMATSRB_9	R/W	H'EC70 84B8*	32	√	√	√	√

Name	Abbreviation	R/W	Address	Access Size	RZ/G Series Products			
					RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
DMA channel control register B_9	DMACHCRB_9	R/W	H'EC70 849C	32	√	√	√	√
DMA extended resource selector_9	DMARS_9	R/W	H'EC70 84C0	16	√	√	√	√
DMA buffer control register_9	DMABUFCR_9	R/W	H'EC70 84C8	32	√	√	√	√
DMA descriptor base address register_9	DMADPBASE_9	R/W	H'EC70 84D0	32	√	√	√	√
DMA descriptor control register_9	DMADPCR_9	R/W	H'EC70 84D4	32	√	√	√	√
DMA fixed source address register_9	DMAFIXSAR_9	R/W	H'EC70 8490	32	√	√	√	√
DMA fixed destination address register_9	DMAFIXDAR_9	R/W	H'EC70 8494	32	√	√	√	√
DMA fixed descriptor base address register_9	DMAFIXDPBASE_9	R/W	H'EC70 84E0	32	√	√	√	√
DMA source address register_10	DMASAR_10	R/W	H'EC70 8500 H'EC70 8520*	32	√	√	√	√
DMA destination address register_10	DMADAR_10	R/W	H'EC70 8504 H'EC70 8524*	32	√	√	√	√
DMA transfer count register_10	DMATCR_10	R/W	H'EC70 8508	32	√	√	√	√
DMA transfer size register_10	DMATSR_10	R/W	H'EC70 8528*	32	√	√	√	√
DMA channel control register_10	DMACHCR_10	R/W	H'EC70 850C H'EC70 852C*	32	√	√	√	√
DMA transfer count register B_10	DMATCRB_10	R/W	H'EC70 8518	32	√	√	√	√
DMA transfer size register B_10	DMATSRB_10	R/W	H'EC70 8538*	32	√	√	√	√
DMA channel control register B_10	DMACHCRB_10	R/W	H'EC70 851C	32	√	√	√	√
DMA extended resource selector_10	DMARS_10	R/W	H'EC70 8540	16	√	√	√	√
DMA buffer control register_10	DMABUFCR_10	R/W	H'EC70 8548	32	√	√	√	√
DMA descriptor base address register_10	DMADPBASE_10	R/W	H'EC70 8550	32	√	√	√	√
DMA descriptor control register_10	DMADPCR_10	R/W	H'EC70 8554	32	√	√	√	√
DMA fixed source address register_10	DMAFIXSAR_10	R/W	H'EC70 8510	32	√	√	√	√
DMA fixed destination address register_10	DMAFIXDAR_10	R/W	H'EC70 8514	32	√	√	√	√
DMA fixed descriptor base address register_10	DMAFIXDPBASE_10	R/W	H'EC70 8560	32	√	√	√	√
DMA source address register_11	DMASAR_11	R/W	H'EC70 8580 H'EC70 85A0*	32	√	√	√	√
DMA destination address register_11	DMADAR_11	R/W	H'EC70 8584 H'EC70 85A4*	32	√	√	√	√
DMA transfer count register_11	DMATCR_11	R/W	H'EC70 8588	32	√	√	√	√
DMA transfer size register_11	DMATSR_11	R/W	H'EC70 85A8*	32	√	√	√	√
DMA channel control register_11	DMACHCR_11	R/W	H'EC70 858C H'EC70 85AC*	32	√	√	√	√
DMA transfer count register B_11	DMATCRB_11	R/W	H'EC70 8598	32	√	√	√	√
DMA transfer size register B_11	DMATSRB_11	R/W	H'EC70 85B8*	32	√	√	√	√
DMA channel control register B_11	DMACHCRB_11	R/W	H'EC70 859C	32	√	√	√	√
DMA extended resource selector_11	DMARS_11	R/W	H'EC70 85C0	16	√	√	√	√

Name	Abbreviation	R/W	Address	Access Size	RZ/G Series Products			
					RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
DMA buffer control register_11	DMABUFCR_11	R/W	H'EC70 85C8	32	√	√	√	√
DMA descriptor base address register_11	DMADPBASE_11	R/W	H'EC70 85D0	32	√	√	√	√
DMA descriptor control register_11	DMADPCR_11	R/W	H'EC70 85D4	32	√	√	√	√
DMA fixed source address register_11	DMAFIXSAR_11	R/W	H'EC70 8590	32	√	√	√	√
DMA fixed destination address register_11	DMAFIXDAR_11	R/W	H'EC70 8594	32	√	√	√	√
DMA fixed descriptor base address register_11	DMAFIXDPBASE_11	R/W	H'EC70 85E0	32	√	√	√	√
DMA source address register_12	DMASAR_12	R/W	H'EC70 8600 H'EC70 8620*	32	√	√	√	√
DMA destination address register_12	DMADAR_12	R/W	H'EC70 8604 H'EC70 8624*	32	√	√	√	√
DMA transfer count register_12	DMATCR_12	R/W	H'EC70 8608	32	√	√	√	√
DMA transfer size register_12	DMATSR_12	R/W	H'EC70 8628*	32	√	√	√	√
DMA channel control register_12	DMACHCR_12	R/W	H'EC70 860C H'EC70 862C*	32	√	√	√	√
DMA transfer count register B_12	DMATCRB_12	R/W	H'EC70 8618	32	√	√	√	√
DMA transfer size register B_12	DMATSRB_12	R/W	H'EC70 8638*	32	√	√	√	√
DMA channel control register B_12	DMACHCRB_12	R/W	H'EC70 861C	32	√	√	√	√
DMA extended resource selector_12	DMARS_12	R/W	H'EC70 8640	16	√	√	√	√
DMA buffer control register_12	DMABUFCR_12	R/W	H'EC70 8648	32	√	√	√	√
DMA descriptor base address register_12	DMADPBASE_12	R/W	H'EC70 8650	32	√	√	√	√
DMA descriptor control register_12	DMADPCR_12	R/W	H'EC70 8654	32	√	√	√	√
DMA fixed source address register_12	DMAFIXSAR_12	R/W	H'EC70 8610	32	√	√	√	√
DMA fixed destination address register_12	DMAFIXDAR_12	R/W	H'EC70 8614	32	√	√	√	√
DMA fixed descriptor base address register_12	DMAFIXDPBASE_12	R/W	H'EC70 8660	32	√	√	√	√
Descriptor memory (for lower-numbered channels)	DescriptorMEM	R/W	H'EC70 A000 to H'EC70 A7FC	32	√	√	√	√
DMA interrupt status register (for higher-numbered channels)	DMAISTA_U	R	H'EC72 0020	32	√	√	√	—
DMA secure control register (for higher-numbered channels)	DMASEC_U	R/W	H'EC72 0030	32	√	√	√	—
DMA operation register (for higher-numbered channels)	DMAOR_U	R/W	H'EC72 0060	16	√	√	√	—
DMA channel clear register (for higher-numbered channels)	DMACHCLR_U	W	H'EC72 0080	32	√	√	√	—
DPRAM secure control register (for higher-numbered channels)	DMADPSEC_U	R/W	H'EC72 00A0	32	√	√	√	—
DMA source address register_13	DMASAR_13	R/W	H'EC72 8000 H'EC72 8020*	32	√	√	√	—
DMA destination address register_13	DMADAR_13	R/W	H'EC72 8004 H'EC72 8024*	32	√	√	√	—

Name	Abbreviation	R/W	Address	Access Size	RZ/G Series Products			
					RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
DMA transfer count register_13	DMATCR_13	R/W	H'EC72 8008	32	√	√	√	—
DMA transfer size register_13	DMATSR_13	R/W	H'EC72 8028*	32	√	√	√	—
DMA channel control register_13	DMACHCR_13	R/W	H'EC72 800C H'EC72 802C*	32	√	√	√	—
DMA transfer count register B_13	DMATCRB_13	R/W	H'EC72 8018	32	√	√	√	—
DMA transfer size register B_13	DMATSRB_13	R/W	H'EC72 8038	32	√	√	√	—
DMA channel control register B_13	DMACHCRB_13	R/W	H'EC72 801C	32	√	√	√	—
DMA extended resource selector_13	DMARS_13	R/W	H'EC72 8040	16	√	√	√	—
DMA buffer control register_13	DMABUFCR_13	R/W	H'EC72 8048	32	√	√	√	—
DMA descriptor base address register_13	DMADPBASE_13	R/W	H'EC72 8050	32	√	√	√	—
DMA descriptor control register_13	DMADPCR_13	R/W	H'EC72 8054	32	√	√	√	—
DMA fixed source address register_13	DMAFIXSAR_13	R/W	H'EC72 8010	32	√	√	√	—
DMA fixed destination address register_13	DMAFIXDAR_13	R/W	H'EC72 8014	32	√	√	√	—
DMA fixed descriptor base address register_13	DMAFIXDPBASE_13	R/W	H'EC72 8060	32	√	√	√	—
DMA source address register_14	DMASAR_14	R/W	H'EC72 8080 H'EC72 80A0*	32	√	√	√	—
DMA destination address register_14	DMADAR_14	R/W	H'EC72 8084 H'EC72 80A4*	32	√	√	√	—
DMA transfer count register_14	DMATCR_14	R/W	H'EC72 8088	32	√	√	√	—
DMA transfer size register_14	DMATSR_14	R/W	H'EC72 80A8*	32	√	√	√	—
DMA channel control register_14	DMACHCR_14	R/W	H'EC72 808C H'EC72 80AC*	32	√	√	√	—
DMA transfer count register B_14	DMATCRB_14	R/W	H'EC72 8098	32	√	√	√	—
DMA transfer size register B_14	DMATSRB_14	R/W	H'EC72 80B8*	32	√	√	√	—
DMA channel control register B_14	DMACHCRB_14	R/W	H'EC72 809C	32	√	√	√	—
DMA extended resource selector_14	DMARS_14	R/W	H'EC72 80C0	16	√	√	√	—
DMA buffer control register_14	DMABUFCR_14	R/W	H'EC72 80C8	32	√	√	√	—
DMA descriptor base address register_14	DMADPBASE_14	R/W	H'EC72 80D0	32	√	√	√	—
DMA descriptor control register_14	DMADPCR_14	R/W	H'EC72 80D4	32	√	√	√	—
DMA fixed descriptor base address register_14	DMAFIXDPBASE_14	R/W	H'EC72 80E0	32	√	√	√	—
DMA fixed source address register_14	DMAFIXSAR_14	R/W	H'EC72 8090	32	√	√	√	—
DMA fixed destination address register_14	DMAFIXDAR_14	R/W	H'EC72 8094	32	√	√	√	—
DMA source address register_15	DMASAR_15	R/W	H'EC72 8100 H'EC72 8120*	32	√	√	√	—
DMA destination address register_15	DMADAR_15	R/W	H'EC72 8104 H'EC72 8124*	32	√	√	√	—
DMA transfer count register_15	DMATCR_15	R/W	H'EC72 8108	32	√	√	√	—
DMA transfer size register_15	DMATSR_15	R/W	H'EC72 8128*	32	√	√	√	—

Name	Abbreviation	R/W	Address	Access Size	RZ/G Series Products			
					RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
DMA channel control register_15	DMACHCR_15	R/W	H'EC72 810C H'EC72 812C*	32	√	√	√	—
DMA transfer count register B_15	DMATCRB_15	R/W	H'EC72 8118	32	√	√	√	—
DMA transfer size register B_15	DMATSRB_15	R/W	H'EC72 8138*	32	√	√	√	—
DMA channel control register B_15	DMACHCRB_15	R/W	H'EC72 811C	32	√	√	√	—
DMA extended resource selector_15	DMARS_15	R/W	H'EC72 8140	16	√	√	√	—
DMA buffer control register_15	DMABUFCR_15	R/W	H'EC72 8148	32	√	√	√	—
DMA descriptor base address register_15	DMADPBASE_15	R/W	H'EC72 8150	32	√	√	√	—
DMA descriptor control register_15	DMADPCR_15	R/W	H'EC72 8154	32	√	√	√	—
DMA fixed source address register_15	DMAFIXSAR_15	R/W	H'EC72 8110	32	√	√	√	—
DMA fixed destination address register_15	DMAFIXDAR_15	R/W	H'EC72 8114	32	√	√	√	—
DMA fixed descriptor base address register_15	DMAFIXDPBASE_15	R/W	H'EC72 8160	32	√	√	√	—
DMA source address register_16	DMASAR_16	R/W	H'EC72 8180 H'EC72 81A0*	32	√	√	√	—
DMA destination address register_16	DMADAR_16	R/W	H'EC72 8184 H'EC72 81A4*	32	√	√	√	—
DMA transfer count register_16	DMATCR_16	R/W	H'EC72 8188	32	√	√	√	—
DMA transfer size register_16	DMATSR_16	R/W	H'EC72 81A8*	32	√	√	√	—
DMA channel control register_16	DMACHCR_16	R/W	H'EC72 818C H'EC72 81AC*	32	√	√	√	—
DMA transfer count register B_16	DMATCRB_16	R/W	H'EC72 8198	32	√	√	√	—
DMA transfer size register B_16	DMATSRB_16	R/W	H'EC72 81B8*	32	√	√	√	—
DMA channel control register B_16	DMACHCRB_16	R/W	H'EC72 819C	32	√	√	√	—
DMA extended resource selector_16	DMARS_16	R/W	H'EC72 81C0	16	√	√	√	—
DMA buffer control register_16	DMABUFCR_16	R/W	H'EC72 81C8	32	√	√	√	—
DMA descriptor base address register_16	DMADPBASE_16	R/W	H'EC72 81D0	32	√	√	√	—
DMA descriptor control register_16	DMADPCR_16	R/W	H'EC72 81D4	32	√	√	√	—
DMA fixed source address register_16	DMAFIXSAR_16	R/W	H'EC72 8190	32	√	√	√	—
DMA fixed destination address register_16	DMAFIXDAR_16	R/W	H'EC72 8194	32	√	√	√	—
DMA fixed descriptor base address register_16	DMAFIXDPBASE_16	R/W	H'EC72 81E0	32	√	√	√	—
DMA source address register_17	DMASAR_17	R/W	H'EC72 8200 H'EC72 8220*	32	√	√	√	—
DMA destination address register_17	DMADAR_17	R/W	H'EC72 8204 H'EC72 8224*	32	√	√	√	—
DMA transfer count register_17	DMATCR_17	R/W	H'EC72 8208	32	√	√	√	—
DMA transfer size register_17	DMATSR_17	R/W	H'EC72 8228*	32	√	√	√	—
DMA channel control register_17	DMACHCR_17	R/W	H'EC72 820C H'EC72 822C*	32	√	√	√	—

Name	Abbreviation	R/W	Address	Access Size	RZ/G Series Products			
					RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
DMA transfer count register B_17	DMATCRB_17	R/W	H'EC72 8218	32	√	√	√	—
DMA transfer size register B_17	DMATSRB_17	R/W	H'EC72 8238*	32	√	√	√	—
DMA channel control register B_17	DMACHCRB_17	R/W	H'EC72 821C	32	√	√	√	—
DMA extended resource selector_17	DMARS_17	R/W	H'EC72 8240	16	√	√	√	—
DMA buffer control register_17	DMABUFCR_17	R/W	H'EC72 8248	32	√	√	√	—
DMA descriptor base address register_17	DMADPBASE_17	R/W	H'EC72 8250	32	√	√	√	—
DMA descriptor control register_17	DMADPCR_17	R/W	H'EC72 8254	32	√	√	√	—
DMA fixed source address register_17	DMAFIXSAR_17	R/W	H'EC72 8210	32	√	√	√	—
DMA fixed destination address register_17	DMAFIXDAR_17	R/W	H'EC72 8214	32	√	√	√	—
DMA fixed descriptor base address register_17	DMAFIXDPBASE_17	R/W	H'EC72 8260	32	√	√	√	—
DMA source address register_18	DMASAR_18	R/W	H'EC72 8280 H'EC72 82A0*	32	√	√	√	—
DMA destination address register_18	DMADAR_18	R/W	H'EC72 8284 H'EC72 82A4*	32	√	√	√	—
DMA transfer count register_18	DMATCR_18	R/W	H'EC72 8288	32	√	√	√	—
DMA transfer size register_18	DMATSR_18	R/W	H'EC72 82A8*	32	√	√	√	—
DMA channel control register_18	DMACHCR_18	R/W	H'EC72 828C H'EC72 82AC*	32	√	√	√	—
DMA transfer count register B_18	DMATCRB_18	R/W	H'EC72 8298	32	√	√	√	—
DMA transfer size register B_18	DMATSRB_18	R/W	H'EC72 82B8*	32	√	√	√	—
DMA channel control register B_18	DMACHCRB_18	R/W	H'EC72 829C	32	√	√	√	—
DMA extended resource selector_18	DMARS_18	R/W	H'EC72 82C0	16	√	√	√	—
DMA buffer control register_18	DMABUFCR_18	R/W	H'EC72 82C8	32	√	√	√	—
DMA descriptor base address register_18	DMADPBASE_18	R/W	H'EC72 82D0	32	√	√	√	—
DMA descriptor control register_18	DMADPCR_18	R/W	H'EC72 82D4	32	√	√	√	—
DMA fixed source address register_18	DMAFIXSAR_18	R/W	H'EC72 8290	32	√	√	√	—
DMA fixed destination address register_18	DMAFIXDAR_18	R/W	H'EC72 8294	32	√	√	√	—
DMA fixed descriptor base address register_18	DMAFIXDPBASE_18	R/W	H'EC72 82E0	32	√	√	√	—
DMA source address register_19	DMASAR_19	R/W	H'EC72 8300 H'EC72 8320*	32	√	√	√	—
DMA destination address register_19	DMADAR_19	R/W	H'EC72 8304 H'EC72 8324*	32	√	√	√	—
DMA transfer count register_19	DMATCR_19	R/W	H'EC72 8308	32	√	√	√	—
DMA transfer size register_19	DMATSR_19	R/W	H'EC72 8328*	32	√	√	√	—
DMA channel control register_19	DMACHCR_19	R/W	H'EC72 830C H'EC72 832C*	32	√	√	√	—
DMA transfer count register B_19	DMATCRB_19	R/W	H'EC72 8318	32	√	√	√	—
DMA transfer size register B_19	DMATSRB_19	R/W	H'EC72 8338*	32	√	√	√	—

Name	Abbreviation	R/W	Address	Access Size	RZ/G Series Products			
					RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
DMA channel control register B_19	DMACHCRB_19	R/W	H'EC72 831C	32	√	√	√	—
DMA extended resource selector_19	DMARS_19	R/W	H'EC72 8340	16	√	√	√	—
DMA buffer control register_19	DMABUFCR_19	R/W	H'EC72 8348	32	√	√	√	—
DMA descriptor base address register_19	DMADPBASE_19	R/W	H'EC72 8350	32	√	√	√	—
DMA descriptor control register_19	DMADPCR_19	R/W	H'EC72 8354	32	√	√	√	—
DMA fixed source address register_19	DMAFIXSAR_19	R/W	H'EC72 8310	32	√	√	√	—
DMA fixed destination address register_19	DMAFIXDAR_19	R/W	H'EC72 8314	32	√	√	√	—
DMA fixed descriptor base address register_19	DMAFIXDPBASE_19	R/W	H'EC72 8360	32	√	√	√	—
DMA source address register_20	DMASAR_20	R/W	H'EC72 8380 H'EC72 83A0*	32	√	√	√	—
DMA destination address register_20	DMADAR_20	R/W	H'EC72 8384 H'EC72 83A4*	32	√	√	√	—
DMA transfer count register_20	DMATCR_20	R/W	H'EC72 8388	32	√	√	√	—
DMA transfer size register_20	DMATSR_20	R/W	H'EC72 83A8*	32	√	√	√	—
DMA channel control register_20	DMACHCR_20	R/W	H'EC72 838C H'EC72 83AC*	32	√	√	√	—
DMA transfer count register B_20	DMATCRB_20	R/W	H'EC72 8398	32	√	√	√	—
DMA transfer size register B_20	DMATSRB_20	R/W	H'EC72 83B8*	32	√	√	√	—
DMA channel control register B_20	DMACHCRB_20	R/W	H'EC72 839C	32	√	√	√	—
DMA extended resource selector_20	DMARS_20	R/W	H'EC72 83C0	16	√	√	√	—
DMA buffer control register_20	DMABUFCR_20	R/W	H'EC72 83C8	32	√	√	√	—
DMA descriptor base address register_20	DMADPBASE_20	R/W	H'EC72 83D0	32	√	√	√	—
DMA descriptor control register_20	DMADPCR_20	R/W	H'EC72 83D4	32	√	√	√	—
DMA fixed source address register_20	DMAFIXSAR_20	R/W	H'EC72 8390	32	√	√	√	—
DMA fixed destination address register_20	DMAFIXDAR_20	R/W	H'EC72 8394	32	√	√	√	—
DMA fixed descriptor base address register_20	DMAFIXDPBASE_20	R/W	H'EC72 83E0	32	√	√	√	—
DMA source address register_21	DMASAR_21	R/W	H'EC72 8400 H'EC72 8420*	32	√	√	√	—
DMA destination address register_21	DMADAR_21	R/W	H'EC72 8404 H'EC72 8424*	32	√	√	√	—
DMA transfer count register_21	DMATCR_21	R/W	H'EC72 8408	32	√	√	√	—
DMA transfer size register_21	DMATSR_21	R/W	H'EC72 8428*	32	√	√	√	—
DMA channel control register_21	DMACHCR_21	R/W	H'EC72 840C H'EC72 842C*	32	√	√	√	—
DMA transfer count register B_21	DMATCRB_21	R/W	H'EC72 8418	32	√	√	√	—
DMA transfer size register B_21	DMATSRB_21	R/W	H'EC72 8438*	32	√	√	√	—
DMA channel control register B_21	DMACHCRB_21	R/W	H'EC72 841C	32	√	√	√	—
DMA extended resource selector_21	DMARS_21	R/W	H'EC72 8440	16	√	√	√	—

Name	Abbreviation	R/W	Address	Access Size	RZ/G Series Products			
					RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
DMA buffer control register_21	DMABUFCR_21	R/W	H'EC72 8448	32	√	√	√	—
DMA descriptor base address register_21	DMADPBASE_21	R/W	H'EC72 8450	32	√	√	√	—
DMA descriptor control register_21	DMADPCR_21	R/W	H'EC72 8454	32	√	√	√	—
DMA fixed source address register_21	DMAFIXSAR_21	R/W	H'EC72 8410	32	√	√	√	—
DMA fixed destination address register_21	DMAFIXDAR_21	R/W	H'EC72 8414	32	√	√	√	—
DMA fixed descriptor base address register_21	DMAFIXDPBASE_21	R/W	H'EC72 8460	32	√	√	√	—
DMA source address register_22	DMASAR_22	R/W	H'EC72 8480 H'EC72 84A0*	32	√	√	√	—
DMA destination address register_22	DMADAR_22	R/W	H'EC72 8484 H'EC72 84A4*	32	√	√	√	—
DMA transfer count register_22	DMATCR_22	R/W	H'EC72 8488	32	√	√	√	—
DMA transfer size register_22	DMATSR_22	R/W	H'EC72 84A8*	32	√	√	√	—
DMA channel control register_22	DMACHCR_22	R/W	H'EC72 848C H'EC72 84AC*	32	√	√	√	—
DMA transfer count register B_22	DMATCRB_22	R/W	H'EC72 8498	32	√	√	√	—
DMA transfer size register B_22	DMATSRB_22	R/W	H'EC72 84B8*	32	√	√	√	—
DMA channel control register B_22	DMACHCRB_22	R/W	H'EC72 849C	32	√	√	√	—
DMA extended resource selector_22	DMARS_22	R/W	H'EC72 84C0	16	√	√	√	—
DMA buffer control register_22	DMABUFCR_22	R/W	H'EC72 84C8	32	√	√	√	—
DMA descriptor base address register_22	DMADPBASE_22	R/W	H'EC72 84D0	32	√	√	√	—
DMA descriptor control register_22	DMADPCR_22	R/W	H'EC72 84D4	32	√	√	√	—
DMA fixed source address register_22	DMAFIXSAR_22	R/W	H'EC72 8490	32	√	√	√	—
DMA fixed destination address register_22	DMAFIXDAR_22	R/W	H'EC72 8494	32	√	√	√	—
DMA fixed descriptor base address register_22	DMAFIXDPBASE_22	R/W	H'EC72 84E0	32	√	√	√	—
DMA source address register_23	DMASAR_23	R/W	H'EC72 8500 H'EC72 8520*	32	√	√	√	—
DMA destination address register_23	DMADAR_23	R/W	H'EC72 8504 H'EC72 8524*	32	√	√	√	—
DMA transfer count register_23	DMATCR_23	R/W	H'EC72 8508	32	√	√	√	—
DMA transfer size register_23	DMATSR_23	R/W	H'EC72 8528*	32	√	√	√	—
DMA channel control register_23	DMACHCR_23	R/W	H'EC72 850C H'EC72 852C*	32	√	√	√	—
DMA transfer count register B_23	DMATCRB_23	R/W	H'EC72 8518	32	√	√	√	—
DMA transfer size register B_23	DMATSRB_23	R/W	H'EC72 8538*	32	√	√	√	—
DMA channel control register B_23	DMACHCRB_23	R/W	H'EC72 851C	32	√	√	√	—
DMA extended resource selector_23	DMARS_23	R/W	H'EC72 8540	16	√	√	√	—
DMA buffer control register_23	DMABUFCR_23	R/W	H'EC72 8548	32	√	√	√	—
DMA descriptor base address register_23	DMADPBASE_23	R/W	H'EC72 8550	32	√	√	√	—



Name	Abbreviation	R/W	Address	Access Size	RZ/G Series Products			
					RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
DMA descriptor control register_23	DMADPCR_23	R/W	H'EC72 8554	32	√	√	√	—
DMA fixed source address register_23	DMAFIXSAR_23	R/W	H'EC72 8510	32	√	√	√	—
DMA fixed destination address register_23	DMAFIXDAR_23	R/W	H'EC72 8514	32	√	√	√	—
DMA fixed descriptor base address register_23	DMAFIXDPBASE_23	R/W	H'EC72 8560	32	√	√	√	—
DMA source address register_24	DMASAR_24	R/W	H'EC72 8580 H'EC72 85A0*	32	√	√	√	—
DMA destination address register_24	DMADAR_24	R/W	H'EC72 8584 H'EC72 85A4*	32	√	√	√	—
DMA transfer count register_24	DMATCR_24	R/W	H'EC72 8588	32	√	√	√	—
DMA transfer size register_24	DMATSR_24	R/W	H'EC72 85A8*	32	√	√	√	—
DMA channel control register_24	DMACHCR_24	R/W	H'EC72 858C H'EC72 85AC*	32	√	√	√	—
DMA transfer count register B_24	DMATCRB_24	R/W	H'EC72 8598	32	√	√	√	—
DMA transfer size register B_24	DMATSRB_24	R/W	H'EC72 85B8*	32	√	√	√	—
DMA channel control register B_24	DMACHCRB_24	R/W	H'EC72 859C	32	√	√	√	—
DMA extended resource selector_24	DMARS_24	R/W	H'EC72 85C0	16	√	√	√	—
DMA buffer control register_24	DMABUFCR_24	R/W	H'EC72 85C8	32	√	√	√	—
DMA descriptor base address register_24	DMADPBASE_24	R/W	H'EC72 85D0	32	√	√	√	—
DMA descriptor control register_24	DMADPCR_24	R/W	H'EC72 85D4	32	√	√	√	—
DMA fixed source address register_24	DMAFIXSAR_24	R/W	H'EC72 8590	32	√	√	√	—
DMA fixed destination address register_24	DMAFIXDAR_24	R/W	H'EC72 8594	32	√	√	√	—
DMA fixed descriptor base address register_24	DMAFIXDPBASE_24	R/W	H'EC72 85E0	32	√	√	√	—
DMA source address register_25	DMASAR_25	R/W	H'EC72 8600 H'EC72 8620*	32	√	√	√	—
DMA destination address register_25	DMADAR_25	R/W	H'EC72 8604 H'EC72 8624*	32	√	√	√	—
DMA transfer count register_25	DMATCR_25	R/W	H'EC72 8608	32	√	√	√	—
DMA transfer size register_25	DMATSR_25	R/W	H'EC72 8628*	32	√	√	√	—
DMA channel control register_25	DMACHCR_25	R/W	H'EC72 860C H'EC72 862C*	32	√	√	√	—
DMA transfer count register B_25	DMATCRB_25	R/W	H'EC72 8618	32	√	√	√	—
DMA transfer size register B_25	DMATSRB_25	R/W	H'EC72 8638*	32	√	√	√	—
DMA channel control register B_25	DMACHCRB_25	R/W	H'EC72 861C	32	√	√	√	—
DMA extended resource selector_25	DMARS_25	R/W	H'EC72 8640	16	√	√	√	—
DMA buffer control register_25	DMABUFCR_25	R/W	H'EC72 8648	32	√	√	√	—
DMA descriptor base address register_25	DMADPBASE_25	R/W	H'EC72 8650	32	√	√	√	—
DMA descriptor control register_25	DMADPCR_25	R/W	H'EC72 8654	32	√	√	√	—
DMA fixed source address register_25	DMAFIXSAR_25	R/W	H'EC72 8610	32	√	√	√	—

Name	Abbreviation	R/W	Address	Access Size	RZ/G Series Products			
					RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
DMA fixed destination address register_25	DMAFIXDAR_25	R/W	H'EC72 8614	32	√	√	√	—
DMA fixed descriptor base address register_25	DMAFIXDPBASE_25	R/W	H'EC72 8660	32	√	√	√	—
Descriptor memory (for higher-numbered channels)	DescriptorMEM	R/W	H'EC72 A000 to H'EC72 A7FC	32	√	√	√	—

Note: The base address of registers for the lower-numbered channels (0 to 12) is H'EC70 0000.

The base address of registers for the higher-numbered channels (13 to 25) is H'EC72 0000.

\* This address is used in total size transmission (see section 35.4.6, Total Size Transmission).

**Table 35.2 States of Audio-DMAC Registers in each Operating Mode**

<b>Abbreviation</b>	<b>Power-On Reset</b>	<b>Module Standby</b>
DMAISTA_L/ DMAISTA_U	Initialized	Retained
DMASEC_L/ DMASEC_U	Initialized	Retained
DMAOR_L/ DMAOR_U	Initialized	Retained
DMACHCLR_L/ DMACHCLR_U	Initialized	Retained
DMADPSEC_L/ DMADPSEC_U	Initialized	Retained
DMASAR_0 to DMASAR_25	Initialized	Retained
DMADAR_0 to DMADAR_25	Initialized	Retained
DMATCR_0 to DMATCR_25	Initialized	Retained
DMATSR_0 to DMATSR_25	Initialized	Retained
DMACHCR_0 to DMACHCR_25	Initialized	Retained
DMATCRB_0 DMATCRB_25	Initialized	Retained
DMATSRB_0 to DMATSRB_25	Initialized	Retained
DMACHCRB_0 to DMACHCRB_25	Initialized	Retained
DMABUFCR_0 to DMABUFCR_25	Initialized	Retained
DMARS_0 to DMARS_25	Initialized	Retained
DMADPBASE_0 to DMADPBASE_25	Initialized	Retained
DMADPCR_0 DMADPCR_25	Initialized	Retained
DMAFIXSAR_0 to DMAFIXSAR_25	Initialized	Retained
DMAFIXDAR_0 to DMAFIXDAR_25	Initialized	Retained
DMAFIXDPBASE_0 to DMAFIXDPBASE_25	Initialized	Retained
DescriptorMEM	Undefined	Retained

### 35.3.1 DMA Interrupt Status Register for Lower-Numbered Channels (DMAISTA\_L)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

DMAISTA\_L is a 32-bit readable register that indicates the states of the interrupt signals for each of the lower-numbered channels.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12	I12	0	R	Interrupt State in Channel 12 0: An interrupt is not present. 1: An interrupt is present.
11	I11	0	R	Interrupt State in Channel 11 0: An interrupt is not present. 1: An interrupt is present.
10	I10	0	R	Interrupt State in Channel 10 0: An interrupt is not present. 1: An interrupt is present.
9	I9	0	R	Interrupt State in Channel 9 0: An interrupt is not present. 1: An interrupt is present.
8	I8	0	R	Interrupt State in Channel 8 0: An interrupt is not present. 1: An interrupt is present.

Bit	Bit Name	Initial Value	R/W	Descriptions
7	I7	0	R	Interrupt State in Channel 7 0: An interrupt is not present. 1: An interrupt is present.
6	I6	0	R	Interrupt State in Channel 6 0: An interrupt is not present. 1: An interrupt is present.
5	I5	0	R	Interrupt State in Channel 5 0: An interrupt is not present. 1: An interrupt is present.
4	I4	0	R	Interrupt State in Channel 4 0: An interrupt is not present. 1: An interrupt is present.
3	I3	0	R	Interrupt State in Channel 3 0: An interrupt is not present. 1: An interrupt is present.
2	I2	0	R	Interrupt State in Channel 2 0: An interrupt is not present. 1: An interrupt is present.
1	I1	0	R	Interrupt State in Channel 1 0: An interrupt is not present. 1: An interrupt is present.
0	I0	0	R	Interrupt State in Channel 0 0: An interrupt is not present. 1: An interrupt is present.

### 35.3.2 DMA Interrupt Status Register for Higher-Numbered Channels (DMAISTA\_U)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

DMAISTA\_U is a 32-bit readable register that indicates the states of the interrupt signals for each of the higher-numbered channels.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	I25	I24	I23	I22	I21	I20	I19	I18	I17	I16	I15	I14	I13
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12	I25	0	R	Interrupt State in Channel 25 0: An interrupt is not present. 1: An interrupt is present.
11	I24	0	R	Interrupt State in Channel 24 0: An interrupt is not present. 1: An interrupt is present.
10	I23	0	R	Interrupt State in Channel 23 0: An interrupt is not present. 1: An interrupt is present.
9	I22	0	R	Interrupt State in Channel 22 0: An interrupt is not present. 1: An interrupt is present.
8	I21	0	R	Interrupt State in Channel 21 0: An interrupt is not present. 1: An interrupt is present.
7	I20	0	R	Interrupt State in Channel 20 0: An interrupt is not present. 1: An interrupt is present.
6	I19	0	R	Interrupt State in Channel 19 0: An interrupt is not present. 1: An interrupt is present.
5	I18	0	R	Interrupt State in Channel 18 0: An interrupt is not present. 1: An interrupt is present.

Bit	Bit Name	Initial Value	R/W	Descriptions
4	I17	0	R	Interrupt State in Channel 17 0: An interrupt is not present. 1: An interrupt is present.
3	I16	0	R	Interrupt State in Channel 16 0: An interrupt is not present. 1: An interrupt is present.
2	I15	0	R	Interrupt State in Channel 15 0: An interrupt is not present. 1: An interrupt is present.
1	I14	0	R	Interrupt State in Channel 14 0: An interrupt is not present. 1: An interrupt is present.
0	I13	0	R	Interrupt State in Channel 13 0: An interrupt is not present. 1: An interrupt is present.

### 35.3.3 DMA Secure Control Register for Lower-Numbered Channels (DMASEC\_L)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

DMASEC\_L is a 32-bit readable/writeable register that controls the security attribute of each of the lower-numbered channels. Only the initiator in the secure mode can change the setting of this register.

Only secure access is allowed to registers of channels with the secure mode setting. The following registers are protected by the secure mode.

DMASAR, DMADAR, DMATCR, DMATSR, DMACHCR, DMATCRB, DMATSRB, DMACHCRB, DMARS, DMABUFCR, DMADPBASE, DMADPCR, DMAFIXSAR, DMAFIXDAR, and DMAFIXDPBASE

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	S0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12	S12	0	R/W	Secure Mode Setting for Channel 12 0: Non-secure mode 1: Secure mode
11	S11	0	R/W	Secure Mode Setting for Channel 11 0: Non-secure mode 1: Secure mode
10	S10	0	R/W	Secure Mode Setting for Channel 10 0: Non-secure mode 1: Secure mode
9	S9	0	R/W	Secure Mode Setting for Channel 9 0: Non-secure mode 1: Secure mode



Bit	Bit Name	Initial Value	R/W	Descriptions
8	S8	0	R/W	Secure Mode Setting for Channel 8 0: Non-secure mode 1: Secure mode
7	S7	0	R/W	Secure Mode Setting for Channel 7 0: Non-secure mode 1: Secure mode
6	S6	0	R/W	Secure Mode Setting for Channel 6 0: Non-secure mode 1: Secure mode
5	S5	0	R/W	Secure Mode Setting for Channel 5 0: Non-secure mode 1: Secure mode
4	S4	0	R/W	Secure Mode Setting for Channel 4 0: Non-secure mode 1: Secure mode
3	S3	0	R/W	Secure Mode Setting for Channel 3 0: Non-secure mode 1: Secure mode
2	S2	0	R/W	Secure Mode Setting for Channel 2 0: Non-secure mode 1: Secure mode
1	S1	0	R/W	Secure Mode Setting for Channel 1 0: Non-secure mode 1: Secure mode
0	S0	0	R/W	Secure Mode Setting for Channel 0 0: Non-secure mode 1: Secure mode

### 35.3.4 DMA Secure Control Register Higher-Numbered Channels (DMASEC\_U)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

DMASEC\_U is a 32-bit readable/writable register that controls the security attribute of each of the higher-numbered channels. Only the initiator in the secure mode can change the setting of this register.

Only secure access is allowed to registers of channels with the secure mode setting. The following registers are protected by the secure mode.

DMASAR, DMADAR, DMATCR, DMATSR, DMACHCR, DMATCRB, DMATSRB, DMACHCRB, DMARS, DMABUFCR, DMADPBASE, DMADPCR, DMAFIXSAR, DMAFIXDAR, and DMAFIXDPBASE

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	S25	S24	S23	S22	S21	S20	S19	S18	S17	S16	S15	S14	S13
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12	S25	0	R/W	Secure Mode Setting for Channel 25 0: Non-secure mode 1: Secure mode
11	S24	0	R/W	Secure Mode Setting for Channel 24 0: Non-secure mode 1: Secure mode
10	S23	0	R/W	Secure Mode Setting for Channel 23 0: Non-secure mode 1: Secure mode
9	S22	0	R/W	Secure Mode Setting for Channel 22 0: Non-secure mode 1: Secure mode
8	S21	0	R/W	Secure Mode Setting for Channel 21 0: Non-secure mode 1: Secure mode
7	S20	0	R/W	Secure Mode Setting for Channel 20 0: Non-secure mode 1: Secure mode

Bit	Bit Name	Initial Value	R/W	Descriptions
6	S19	0	R/W	Secure Mode Setting for Channel 19 0: Non-secure mode 1: Secure mode
5	S18	0	R/W	Secure Mode Setting for Channel 18 0: Non-secure mode 1: Secure mode
4	S17	0	R/W	Secure Mode Setting for Channel 17 0: Non-secure mode 1: Secure mode
3	S16	0	R/W	Secure Mode Setting for Channel 16 0: Non-secure mode 1: Secure mode
2	S15	0	R/W	Secure Mode Setting for Channel 15 0: Non-secure mode 1: Secure mode
1	S14	0	R/W	Secure Mode Setting for Channel 14 0: Non-secure mode 1: Secure mode
0	S13	0	R/W	Secure Mode Setting for Channel 13 0: Non-secure mode 1: Secure mode

### 35.3.5 DMA Operation Register for Lower-Numbered Channels (DMAOR\_L)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

DMAOR\_L is a 16-bit readable/writable register that enables DMA transfer on all lower-numbered channels and specifies the method used to determine the priority levels for all lower-numbered DMA channels. This register also indicates address errors.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	PR[1:0]	—	—	—	—	—	—	AE	—	DME
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R	R	R	R	R	R/(W)*	R	R/W

Bit	Bit Name	Initial Value	R/W	Descriptions
15 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9, 8	PR[1:0]	00	R/W	Priority Mode Select the method for setting the order of priority of channels when transfer requests for multiple channels arrive simultaneously. 00: Fixed CH0 > CH1 > ... > CH11 > CH12 11: Round-robin priority Other than above: Setting prohibited
7 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2	AE	0	R/(W)*	Address Error Flag Indicates that an address error interrupt occurred during DMA transfer. This bit is set under the following conditions: The value set in DMASAR or DMADAR does not fall on a boundary corresponding to the transfer size. The source or destination for transfer is in an invalid space. The source or destination for transfer is in module stop mode. If this bit is set, DMA transfer through the channel is not possible even if the DE bit is set to 1. To clear the AE bit, write 0 to the AE bit after reading 1 from it or clear the CAE bit for each channel for which it is set. Clearing the AE bit clears the channel address error bits for all channels. 0: An audio-DMAC address error interrupt is not present. [Clearing condition] Writing CAE = 0 after reading CAE = 1 1: An audio-DMAC address error interrupt being generated during DMA transfer.
1	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

---

Bit	Bit Name	Initial Value	R/W	Descriptions
0	DME	0	R/W	<p>DMA Master Enable</p> <p>Enables or disables DMA transfer on all channels. If the DME bit and the DE bit in DMACHCR are both set to 1, DMA transfer is enabled. At this time all AE bits in DMAOR_L must have the value 0. For DMA transfer on a channel to then proceed, the TE bit in DMACHCR for the channel must also have the value 0. Clearing this bit during transfer aborts transfer on all channels.</p> <p>0: Disables DMA transfers on all channels</p> <p>1: Enables DMA transfers on all channels</p>

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### 35.3.6 DMA Operation Register for Higher-Numbered Channels (DMAOR\_U)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

DMAOR\_U is a 16-bit readable/writable register that enables DMA transfer on all higher-numbered channels and specifies the method used to determine the priority levels for all higher-numbered DMA channels. This register also indicates address errors.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	PR[1:0]		—	—	—	—	—	AE	—	DME
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R	R	R	R	R	R/(W)*	R	R/W

Bit	Bit Name	Initial Value	R/W	Descriptions
15 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9, 8	PR[1:0]	00	R/W	Priority Mode Select the method for setting the order of priority of channels when transfer requests for multiple channels arrive simultaneously. 00: Fixed CH13 > CH14 > ... > CH24 > CH25 11: Round-robin priority Other than above: Setting prohibited
7 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2	AE	0	R/(W)*	Address Error Flag Indicates that an address error interrupt occurred during DMA transfer. This bit is set under the following conditions: The value set in DMASAR or DMADAR does not fall on a boundary corresponding to the transfer size. The source or destination for transfer is in an invalid space. The source or destination for transfer is in module stop mode. If this bit is set, DMA transfer through the channel is not possible even if the DE bit is set to 1. To clear the AE bit, write 0 to the AE bit after reading 1 from it or clear the CAE bit for each channel for which it is set. Clearing the AE bit clears the channel address error bits for all channels. 0: An audio-DMAC address error interrupt is not present. [Clearing condition] Writing CAE = 0 after reading CAE = 1 1: An audio-DMAC address error interrupt being generated during DMA transfer.
1	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

---

<b>Bit</b>	<b>Bit Name</b>	<b>Initial Value</b>	<b>R/W</b>	<b>Descriptions</b>
0	DME	0	R/W	<p>DMA Master Enable</p> <p>Enables or disables DMA transfer on all channels. If the DME bit and the DE bit in DMACHCR are both set to 1, DMA transfer is enabled. At this time all AE bits in DMAOR_U must have the value 0. For DMA transfer on a channel to then proceed, the TE bit in DMACHCR for the channel must also have the value 0. Clearing this bit during transfer aborts transfer on all channels.</p> <p>0: Disables DMA transfers on all channels</p> <p>1: Enables DMA transfers on all channels</p>

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### 35.3.7 DMA Channel Clear Register for Lower-Numbered Channels (DMACHCLR\_L)

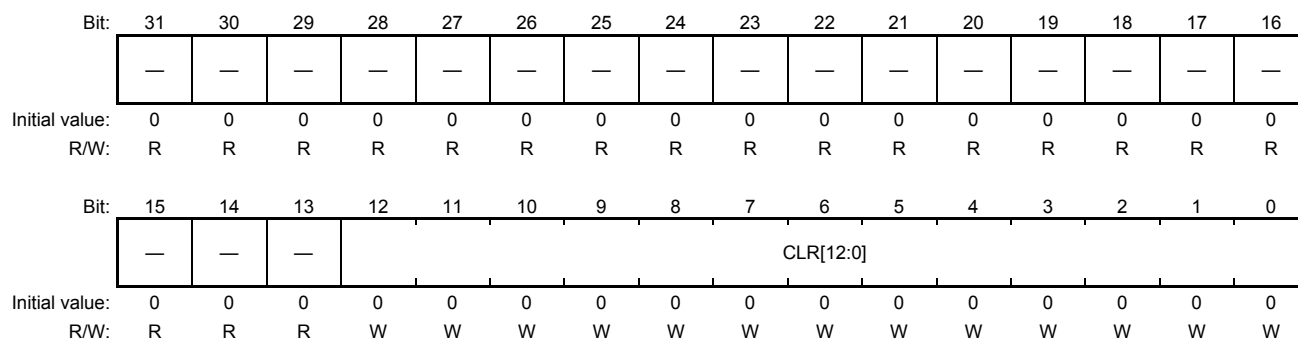
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

DMACHCLR\_L is a 32-bit writable register that initializes each of the lower-numbered channels.

When a bit of this register is set, the state of the corresponding channel is completely initialized.

This includes initialization of the following registers.

DMASAR, DMADAR, DMATCR, DMATSR, DMACHCR, DMATCRB, DMATSRB, DMACHCRB, DMARS, DMABUFGR, DMADPBASE, DMADPCR, DMAFIXSAR, DMAFIXDAR, and DMAFIXDPBASE



Bit	Bit Name	Initial Value	R/W	Description
31 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12 to 0	CLR[12:0]	All 0	W	Writing to a bit leads to clearing of all registers for the corresponding channel. CLR[0] 0: Ignored 1: All registers for channel 0 are cleared. CLR[1] 0: Ignored 1: All registers for channel 1 are cleared. CLR[2] 0: Ignored 1: All registers for channel 2 are cleared. ... CLR[12] 0: Ignored 1: All registers for channel 12 are cleared. When writing to this register, confirm that the DE bit is set to 0.



### 35.3.8 DMA Channel Clear Register for Higher-Numbered Channels (DMACHCLR\_U)

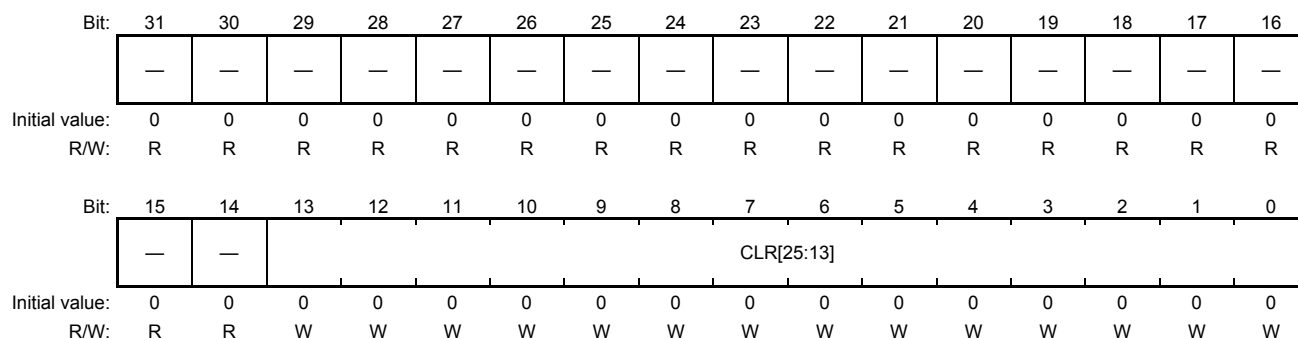
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

DMACHCLR\_U is a 32-bit writable register that initializes each of the higher-numbered channels.

When a bit of this register is set, the state of the corresponding channel is completely initialized.

This includes initialization of the following registers.

DMASAR, DMADAR, DMATCR, DMATSR, DMACHCR, DMATCRB, DMATSRB, DMACHCRB, DMARS, DMABUFCR, DMADPBASE, DMADPCR, DMAFIXSAR, DMAFIXDAR, and DMAFIXDPBASE



Bit	Bit Name	Initial Value	R/W	Description
31 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12 to 0	CLR[25:13]	All 0	W	Writing to a bit leads to clearing of all registers for the corresponding channel. CLR[13] 0: Ignored 1: All registers for channel 13 are cleared. CLR[14] 0: Ignored 1: All registers for channel 14 are cleared. ... CLR[25] 0: Ignored 1: All registers for channel 25 are cleared. When writing to this register, confirm that the DE bit is set to 0.

### 35.3.9 DPRAM Secure Control Register for Lower-Numbered Channels (DMADPSEC\_L)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

DMADPSEC\_L is a 32-bit readable/writable register that controls the security attribute of the descriptor memory. Only the initiator in the secure mode can change the setting of this register.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16			
	SEC	—	—	—	—	—	—	SA[8:0]											
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
R/W:	R/W	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
	—	—	—	—	—	—	—	SM[8:0]											
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
R/W:	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			

Bit	Bit Name	Initial Value	R/W	Description
31	SEC	0	R/W	Security Attribute Setting for Descriptor Memory Specifies the security attribute of the address space used for the descriptor memory. 0: Non-secure 1: Secure
30 to 25	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
24 to 16	SA[8:0]	H'000	R/W	Security Attribute Setting for Base Address of Descriptor Memory Specify the base address of the descriptor memory to be assigned the security attribute. H'000: H'A000 H'001: H'A004 ... H'1FF: H'A7FC
15 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8 to 0	SM[8:0]	H'000	R/W	Security Attribute Setting for Base Address Mask of Descriptor Memory Specify the security attribute base address mask of the descriptor memory. The range of memory to be assigned the security attribute is specified by this register. See Figure 35.4.

### 35.3.10 DPRAM Secure Control Register for Higher-Numbered Channels (DMADPSEC\_U)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

DMADPSEC\_U is a 32-bit readable/writeable register that controls the security attribute of the descriptor memory. Only the initiator in the secure mode can change the setting of this register.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16			
	SEC	—	—	—	—	—	—	SA[8:0]											
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
R/W:	R/W	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
	—	—	—	—	—	—	—	SM[8:0]											
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
R/W:	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			

Bit	Bit Name	Initial Value	R/W	Description
31	SEC	0	R/W	Security Attribute Setting for Descriptor Memory Specifies the security attribute of the address space used for the descriptor memory. 0: Non-secure 1: Secure
30 to 25	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
24 to 16	SA[8:0]	H'000	R/W	Security Attribute Setting for Base Address of Descriptor Memory Specify the base address of the descriptor memory to be assigned the security attribute. H'000: H'A000 H'001: H'A004 ... H'1FF: H'A7FC
15 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8 to 0	SM[8:0]	H'000	R/W	Security Attribute Setting for Base Address Mask of Descriptor Memory Specify the security attribute base address mask of the descriptor memory. The range of memory to be assigned the security attribute is specified by this register. See Figure 35.4.

### 35.3.11 DMA Source Address Registers 0 to 25 (DMASAR\_0 to DMASAR\_25)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

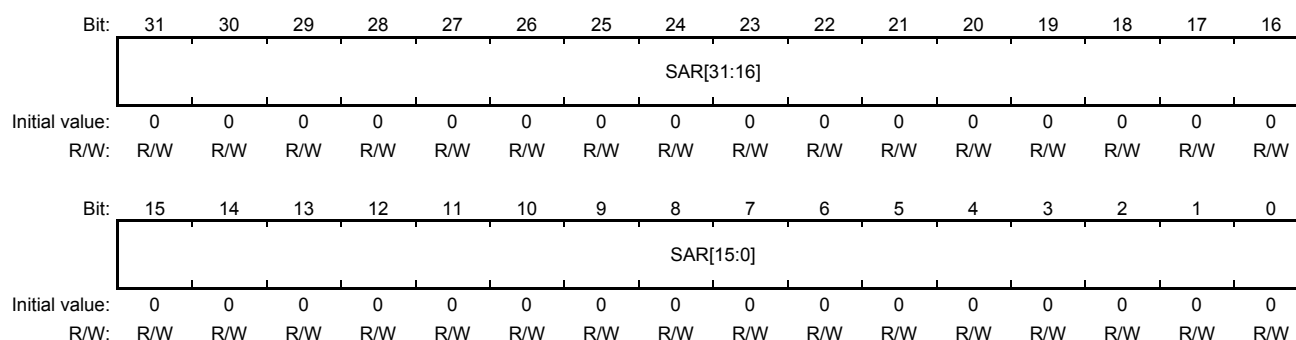
Note: The availability of channels depends on the product as follows.

RZ/G1H and M/N: 26 channels (channels 0 to 25)

RZ/G1E: 13 channels (channels 0 to 12)

DMASAR is a 32-bit readable/writable register that specifies the source address of a DMA transfer. While a DMA transfer is in progress, this register indicates the next source address.

When the address mode is incrementation, sources in memory only have byte boundaries. For details, refer to Table 35.3.



### 35.3.12 DMA Destination Address Registers 0 to 25 (DMADAR\_0 to DMADAR\_25)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

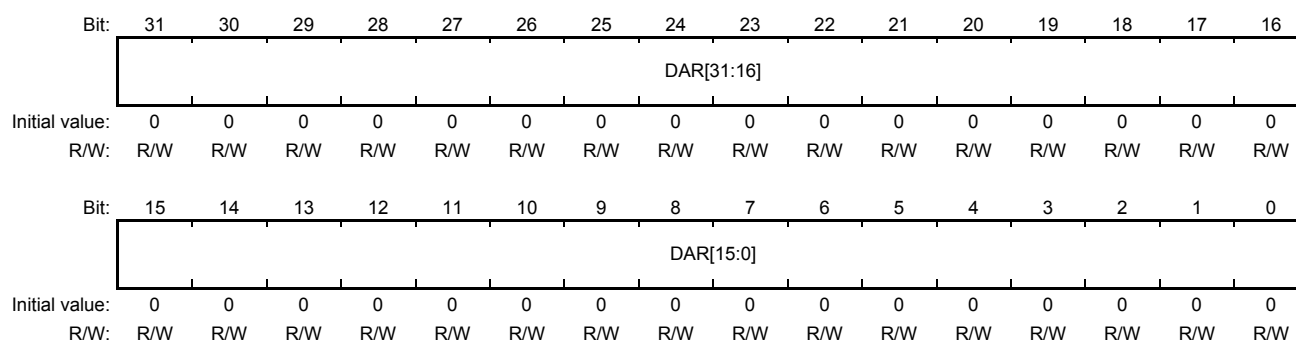
Note: The availability of channels depends on the product as follows.

RZ/G1H and M/N: 26 channels (channels 0 to 25)

RZ/G1E: 13 channels (channels 0 to 12)

DMADAR is 32-bit readable/writable register that specify the destination address of a DMA transfer. While a DMA transfer is in progress, this register indicates the next destination address.

When the address mode is incrementation, destinations in memory only have byte boundaries. For details, refer to Table 35.3.



**Table 35.3 SAR/DAR Address Restriction**

Resource Selection	Address Mode	Restriction
Auto request	Incrementation	No restriction (byte boundaries)
	Others	Boundary corresponding to the DMA transfer size
On-chip peripheral module request Transmission/DAR, Reception/SAR	All	Boundary corresponding to the DMA transfer size
On-chip peripheral module request Transmission/SAR, Reception/DAR	Incrementation	No restriction (byte boundaries)
	Others	Boundary corresponding to the DMA transfer size

**35.3.13 DMA Transfer Count Registers 0 to 25 (DMATCR\_0 to DMATCR\_25)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Note: The availability of channels depends on the product as follows.

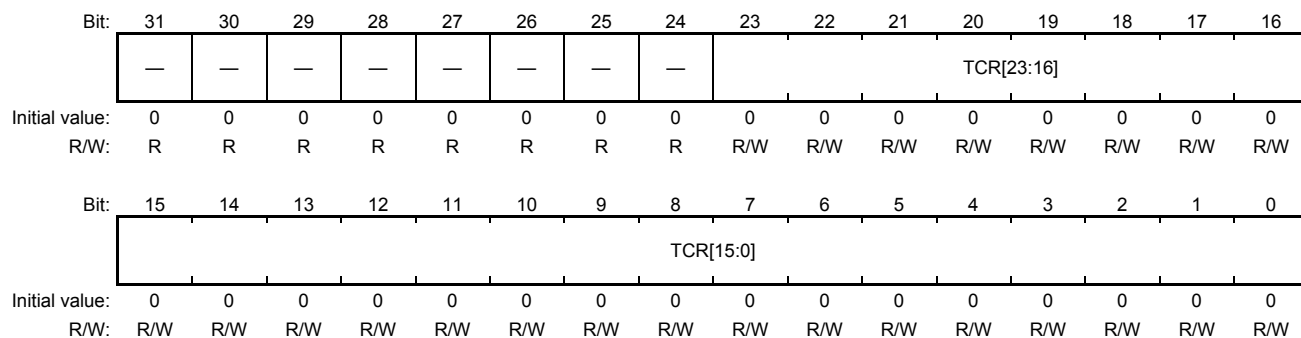
RZ/G1H and M/N: 26 channels (channels 0 to 25)

RZ/G1E: 13 channels (channels 0 to 12)

DMATCR is a 32-bit readable/writable register that specifies the number of rounds of DMA transfer. The number of rounds of DMA transfer is 1 when the setting is H'00000001, 16,777,215 when the setting is H'00FFFFFF, and 16,777,216 (the maximum) when the setting is H'00000000. During a DMA transfer, this register indicates the remaining number of rounds of transfer.

The audio-DMAC includes independent data buffers for reading and writing. Therefore, the read transfer counter and write transfer counter have different values. This register indicates the counter value used in reading.

The eight higher-order bits of DMATCR are always read as 0, and the write value should always be 0.



### 35.3.14 DMA Transfer Count Registers B\_0 to 25 (DMATCRB\_0 to DMATCRB\_25)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Note: The availability of channels depends on the product as follows.

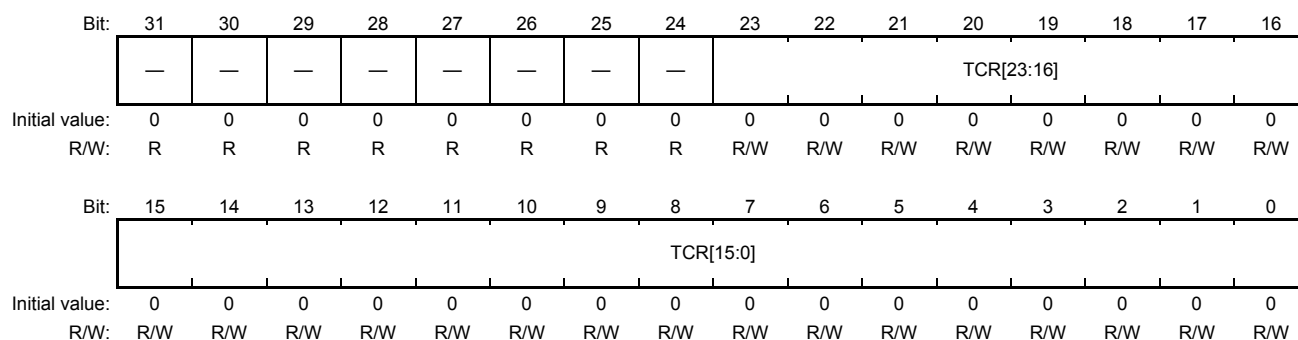
RZ/G1H and M/N: 26 channels (channel 0 to 25)

RZ/G1E: 13 channels (channel 0 to 12)

DMATCRB is a 32-bit readable/writable register that specifies the number of rounds of DMA transfer. The number of rounds of DMA transfer is 1 when the setting is H'00000001, 16,777,215 when the setting is H'00FFFFFF, and 16,777,216 (the maximum) when the setting is H'00000000. During a DMA transfer, this register indicates the remaining number of rounds of transfer.

The audio-DMAC includes independent data buffers for reading and writing. Therefore, the read transfer counter and write transfer counter have different values. This register indicates the counter value used in writing.

The eight higher-order bits of DMATCRB are always read as 0, and the write value should always be 0.



**35.3.15 DMA Transfer Size Registers 0 to 25 (DMATSR\_0 to DMATSR\_25)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

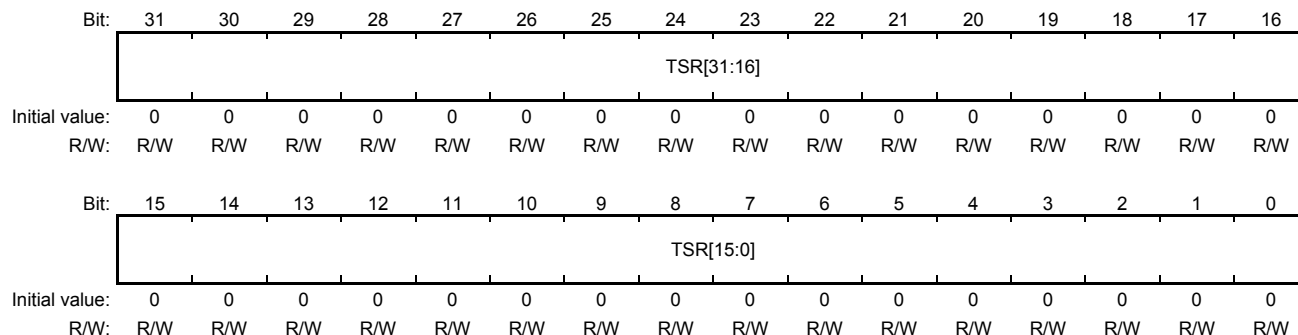
Note: The availability of channels depends on the product as follows.

RZ/G1H and M/N: 26 channels (channel 0 to 25)

RZ/G1E: 13 channels (channel 0 to 12)

DMATSR is a 32-bit readable/writable register that specifies a total amount of memory to be transferred. The total size of DMA transfer is 1 byte when the setting is H'00000001, 4,294,967,295 bytes when the setting is H'FFFFFFF, and 4,294,967,296 bytes (the maximum) when the setting is H'00000000. During a DMA transfer, this register indicates the remaining amount of memory to be transferred. This register is used in total size transmission.

The audio-DMAC includes independent data buffers for reading and writing. Therefore, reading and writing will have different transfer sizes. This register indicates the value of the read transfer size.



**35.3.16 DMA Transfer Size Registers B\_0 to 25 (DMATSRB\_0 to DMATSRB\_25)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

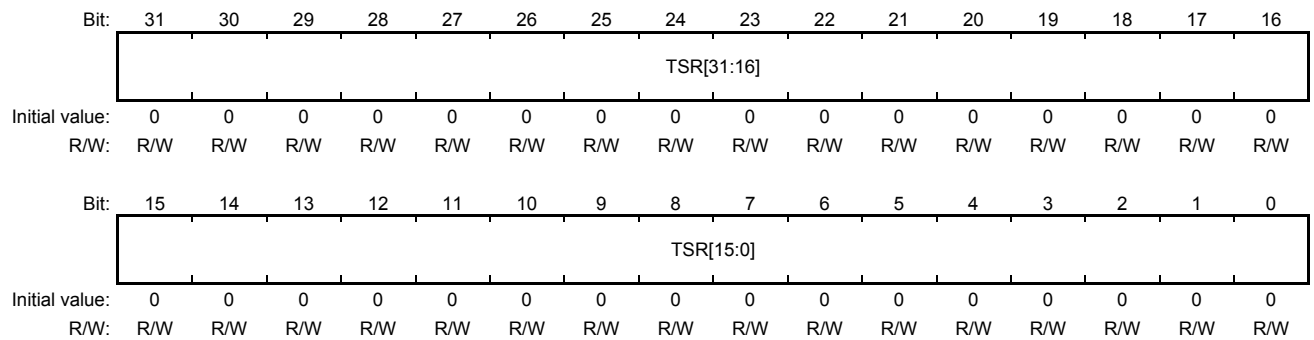
Note: The availability of channels depends on the product as follows.

RZ/G1H and M/N: 26 channels (channels 0 to25)

RZ/G1E: 13 channels (channels 0 to 12)

DMATSRB is a 32-bit readable/writable register that specifies a total amount of memory to be transferred. The total size of DMA transfer is 1 byte when the setting is H'00000001, 4,294,967295 bytes when the setting is H'FFFFFFF, and 4,294,967,296 bytes (the maximum) when the setting is H'00000000. During a DMA transfer, this register indicates the remaining amount of memory to be transferred. This register is used in total size transmission.

The audio-DMAC includes independent data buffers for reading and writing. Therefore, reading and writing will have different transfer sizes. This register indicates the value of the write transfer size.





### 35.3.17 DMA Channel Control Registers 0 to 25 (DMACHCR\_0 to DMACHCR\_25)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Note: The availability of channels depends on the product as follows.

RZ/G1H, M/N: 26 channels (channels 0 to 25)

RZ/G1E: 13 channels (channels 0 to 12)

DMACHCR is a 32-bit readable/writable register that controls the DMA transfer mode.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CAE	CAIE	DPM[1:0]		RPT[2:0]			—	—	DPB	TS[3:2]		DSE	DSIE	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/(W)*	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/(W)*	R/W	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DM[1:0]		SM[1:0]		RS[3:0]			—	—	—	TS[1:0]		IE	TE	DE	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R/W	R/W	R/W	R/(W)*	R/W

Bit	Bit Name	Initial Value	R/W	Descriptions
31	CAE	0	R/(W)*	<p>Channel Address Error Flag</p> <p>Indicates that an address error interrupt occurred during DMA transfer.</p> <p>This bit is set under the following conditions:</p> <ul style="list-style-type: none"> <li>The value set in DMASAR or DMADAR does not fall on a boundary corresponding to the transfer size.</li> <li>The source or destination for transfer is in an invalid space.</li> <li>The source or destination for transfer is in module stop mode.</li> </ul> <p>If this bit is set, DMA transfer through the channel is not possible even if the DE bit is set to 1.</p> <p>To clear the CAE bit, write 0 to the CAE bit after reading 1 from it or clear the AE bit in DMAOR.</p> <p>Clearing the CAE bit clears the channel address error bits for all channels.</p> <p>0: An audio-DMAC address error interrupt is not present.            [Clearing condition] Writing CAE = 0 after reading CAE = 1</p> <p>1: An audio-DMAC address error interrupt being generated during DMA transfer.</p>
30	CAIE	0	R/W	<p>Channel Address Error Interrupt Enable</p> <p>Enables or disables the generation of interrupt requests for the CPU when address errors occur. When the CAIE bit is set to 1, if the CAE bit is also set, an interrupt (DEI 0 to 25) from the corresponding channel will be generated for the CPU in response to address errors.</p> <p>Note: An address error interrupt (DADERR) is also asserted simultaneously. See section 11, Interrupt Controller for AP-System Core (INTC-SYS) for more details.</p> <p>0: Interrupt requests are disabled.            1: Interrupt requests are enabled.</p>

Bit	Bit Name	Initial Value	R/W	Descriptions
29, 28	DPM[1:0]	00	R/W	<p>Operating Mode of Descriptor Memory</p> <p>Enable or disable the descriptor memory and specify its operating mode.</p> <p>00: Disabled (normal use)</p> <p>01: Enabled (normal mode)</p> <p>10: Enabled (repeat mode)</p> <p>11: Enabled (read-out interrupt mode, infinite repeat mode)</p>
27 to 25	RPT[2:0]	000	R/W	<p>Descriptor Setting Update</p> <p>Specify the parameters to be updated from the descriptor memory.</p> <p>RPT[2]: Enables or disables updating of the source address register</p> <p>RPT[1]: Enables or disables updating of the destination address register</p> <p>RPT[0]: Enables or disables updating of the transfer count register</p> <p>0: Disabled</p> <p>1: Enabled</p>
24, 23	—	All 0	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>
22	DPB	0	R/W	<p>Descriptor Start</p> <p>Specifies configuration to be loaded when transfer under control of the descriptor memory begins.</p> <p>This bit is cleared after the descriptor memory is read.</p> <p>0: Processing starts with the values in DMASAR, DMADAR, and DMATCR.</p> <p>1: Processing starts after the first set of descriptors is read out.</p>
21, 20	TS[3:2]	00	R/W	<p>DMA Transfer Size</p> <p>In combination with TS[1:0], these bits specify the DMA transfer size. When the transfer source or transfer destination is a register of an on-chip peripheral module for which a transfer size is specified, be sure to select the specified transfer size. For the transfer source or destination address specified by DMASAR or DMADAR, an appropriate boundary address should be set according to the transfer data size.</p> <p>TS[3:2] + TS[1:0] (“+” here indicates concatenation, not addition)</p> <p>0000: Transfer is in byte units.</p> <p>0001: Transfer is in word (2-byte) units.</p> <p>0010: Transfer is in longword (4-byte) units.</p> <p>0011: Transfer is in 16-byte units.</p> <p>0100: Transfer is in 32-byte units.</p> <p>0101: Transfer is in 64-byte units.</p> <p>0111: Transfer is in 8-byte units.</p> <p>Other than above: Setting prohibited</p> <p>Note: Transfer size must be specified to satisfy both source and destination access sizes.</p>

Bit	Bit Name	Initial Value	R/W	Descriptions
19	DSE	0	R/(W)*	<p>Descriptor Stage End</p> <p>When the DSIE bit is set to 1 and the descriptor memory is enabled, the DSE bit is set to 1 on completion of the DMA transfer. This bit is not set when the DPM bit is set to 0 (descriptors are disabled). To clear the DSE bit, start by reading it as 1, and then write 0 to the bit.</p> <p>0: DMA transfer is still running or has been aborted. 1: Transfer under the control of one stage of the descriptor memory has been completed.</p>
18	DSIE	0	R/W	<p>Descriptor Stage End Interrupt Enable</p> <p>Specifies whether an interrupt request is generated for the CPU on completion of transfer under the control of one stage of the descriptor memory. When this bit is set to 1, an interrupt (DEI) is generated for the CPU whenever the DSE is set to 1.</p> <p>0: Interrupt requests are disabled. 1: Interrupt requests are enabled.</p>
17, 16	—	All 0	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>
15, 14	DM[1:0]	00	R/W	<p>Destination Address Mode</p> <p>Specify whether the DMA destination address is incremented, fixed, or decremented. The unit of transfer (transfer size) determines the size of the increment.</p> <p>00: Destination address is fixed. 01: Destination addresses are incremented.  <ul style="list-style-type: none"> <li>+ 1 when transfer is in byte units.</li> <li>+ 2 when transfer is in word units.</li> <li>+ 4 when transfer is in longword units.</li> <li>+ 8 when transfer is in 8-byte units.</li> <li>+ 16 when transfer is in 16-byte units.</li> <li>+ 32 when transfer is in 32-byte units.</li> <li>+ 64 when transfer is in 64-byte units.</li> </ul> 10: Destination addresses are decremented.  <ul style="list-style-type: none"> <li>– 1 when transfer is in byte units.</li> <li>– 2 when transfer is in word units.</li> <li>– 4 when transfer is in longword units.</li> </ul> Setting prohibited when transfer is in 8-, 16-, 32-, or 64-byte units. 11: Setting Prohibited</p>

Bit	Bit Name	Initial Value	R/W	Descriptions
13, 12	SM[1:0]	00	R/W	<p>Source Address Mode</p> <p>Specify whether the DMA source address is incremented, fixed, or decremented. The unit of transfer (transfer size) determines the size of the increment.</p> <p>00: Source address is fixed.</p> <p>01: Source addresses are incremented.</p> <ul style="list-style-type: none"> <li>+ 1 when transfer is in byte units.</li> <li>+ 2 when transfer is in word units.</li> <li>+ 4 when transfer is in longword units.</li> <li>+ 8 when transfer is in 8-byte units.</li> <li>+ 16 when transfer is in 16-byte units.</li> <li>+ 32 when transfer is in 32-byte units.</li> <li>+ 64 when transfer is in 64-byte units.</li> </ul> <p>10: Source addresses are decremented.</p> <ul style="list-style-type: none"> <li>– 1 when transfer is in byte units.</li> <li>– 2 when transfer is in word units.</li> <li>– 4 when transfer is in longword units.</li> </ul> <p>Setting prohibited when transfer is in 8-, 16-, 32-, or 64-byte units.</p> <p>11: Setting Prohibited</p>
11 to 8	RS[3:0]	0000	R/W	<p>Resource Selection</p> <p>Specify the source of transfer requests. Only change the transfer request source while the DMA enable bit (DE) is set to 0.</p> <p>0100: Auto request</p> <p>1000: Source is selected by the DMA extended resource selector.</p> <p>Other than above: Settings prohibited</p>
7 to 5	—	All 0	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>
4, 3	TS[1:0]	00	R/W	<p>DMA Transfer Size</p> <p>See the description of TS[3:2] (bits 21 and 20).</p>
2	IE	0	R/W	<p>Interrupt Enable</p> <p>Specifies whether or not an interrupt request is generated for the CPU on completion of DMA transfer. When this bit is set to 1, an interrupt request (DEI) for the CPU is generated whenever the TE bit is set to 1.</p> <p>0: Interrupt request is disabled.</p> <p>1: Interrupt request is enabled.</p>

Bit	Bit Name	Initial Value	R/W	Descriptions
1	TE	0	R/(W)*	<p>Transfer End Flag</p> <p>When the descriptor memory is not in use, the TE bit is set to 1 when DMATCR becomes 0 on completion of the DMA transfer.</p> <p>When the descriptor memory is in use, the TE bit is set to 1 on completion of all transfers set up in the descriptor memory. The TE bit is not set to 1 in the following cases.</p> <ul style="list-style-type: none"> <li>• DMA transfer ends due to a DMA address error before DMATCR becomes 0.</li> <li>• DMA transfer is aborted by clearing the DE and DME bits in DMAOR.</li> </ul> <p>To clear the TE bit, start by reading it as 1, and then write 0 to it.</p> <p>When the TE bit is set to 1, transfer is not possible even if the DE bit is set to 1.</p> <p>0: DMA transfer is in progress or was aborted            [Clearing condition] Writing of 0 after reading of 1            1: DMA transfer ended on the specified count (TCR = 0)</p>
0	DE	0	R/W	<p>DMA Enable</p> <p>Enables or disables DMA transfer. In the auto request mode, a DMA transfer is started by setting the DE and DME bits in DMAOR to 1. At this time, the setting of both the AE and TE bits in DMAOR must be 0. In a peripheral module request, a DMA transfer starts if the transfer request is generated by the selected device or on-chip peripheral module after setting the DE and DME bits to 1. In this case too, the settings of both the TE and AE bits must be 0. Clearing the DE bit to 0 aborts all DMA transfer.</p> <p>Note: Ensure that the setting of the DE bit is actually 0 after clearing it.</p> <p>0: DMA transfer is disabled.            1: DMA transfer is enabled.</p>

Note: \* Writing 0 is possible to clear the flag.

### 35.3.18 DMA Channel Control Register B\_0 to 25 (DMACHCRB\_0 to DMACHCRB\_25)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Note: The availability of channels depends on the product as follows.

RZ/G1H and M/N: 26 channels (channels 0 to 25)

RZ/G1E: 13 channels (channels 0 to 12)

DMACHCRB is a 32-bit readable/writable register that controls the DMA transfer mode.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DCNT[7:0]								DPTR[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DRST	—	—	—	—	—	—	DTS	SLM[3:0]			PRI[3:0]				
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	W	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 24	DCNT[7:0]	H'00	R/W	Number of Stages of Descriptor Memory Specify the number of stages of the descriptor memory as DCNT + 1. When the descriptor memory is enabled, a transfer end (TE) interrupt is only generated for the CPU on completion of transfer under control of the specified number of stages.
23 to 16	DPTR[7:0]	H'00	R	Descriptor Pointer This bit indicates the pointer to the next descriptor to be read. It is cleared to 0 when the last descriptor of the number of stages specified by DCNT[7:0] is read. It is also cleared to 0 when 1 is written to DRST.
15	DRST	0	W	Descriptor Reset Resets the descriptor pointer. Before the descriptor memory is used, the pointer must be reset by writing 1 to this bit. This bit is always read as 0.
14 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	DTS	0	R/W	Total Size Transmission under Descriptor Control This bit is only effective when total size transmission is selected. 0: The TCR fields of the descriptors are used as transfer count settings. 1: The TCR fields of the descriptors are used as total size settings.

Bit	Bit Name	Initial Value	R/W	Descriptions
7 to 4	SLM[3:0]	0000	R/W	<p>DMA Transfer Low-Speed Mode</p> <p>Specify the number of cycles of the clock (ZS<math>\phi</math>) for the DMA transfer. One round of DMA transfer is executed in the number of cycles of the clock specified by this bit.</p> <p>0000: Normal mode</p> <p>1000: On round in 256 cycles of the clock.</p> <p>1001: On round in 512 cycles of the clock.</p> <p>1010: On round in 1024 cycles of the clock.</p> <p>:</p> <p>1111: On round in 32768 cycles of the clock.</p> <p>Other than above: Setting prohibited</p>
3 to 0	PRI[3:0]	0000	R/W	<p>Channel Request Priority Setting</p> <p>These bits set the priority of requests for transfer on the given channel.</p> <p>1111: Highest priority</p> <p>:</p> <p>0111 to 0000: Lowest priority</p>

### 35.3.19 DMA Buffer Control Registers 0 to 25 (DMABUFCR\_0 to DMABUFCR\_25)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Note: The availability of channels depends on the product as follows.

RZ/G1H and M/N: 26 channels (channels 0 to 25)

RZ/G1E: 13 channels (channels 0 to 12)

DMABUFCR is a 32-bit readable/writable register that controls the upper limit on buffer size in and burst unit for the SDRAM.

Use this register when the upper limit on buffering requires control.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16				
	—	—	—	—	—	—	—	MBU[8:0]									—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0				
R/W:	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W				
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
	—	—	—	—	—	—	ULB[9:0]									—	—	—	—	
Initial value:	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0				
R/W:	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W				

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 25	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
24 to 16	MBU[8:0]	H'080	R/W	Maximum Burst Unit for SDRAM This register is only effective for SDRAM access, and everything other than that is under control of the transfer size (unit). Settings bigger than UBL are prohibited. Power-of-two settings are recommended. Maximum value is 256 (bytes).
15 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9 to 0	ULB[9:0]	H'100	R/W	Upper Limit on Buffer Size This register controls the upper limit value for buffering. Power-of-two settings are recommended. Maximum value is 512 (bytes).



### 35.3.20 DMA Extended Resource Selectors 0 to 25 (DMARS\_0 to DMARS\_25)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Note: The availability of channels depends on the product as follows.

RZ/G1H and M/N: 26 channels (channels 0 to 25)

RZ/G1E: 13 channels (channels 0 to 12)

DMARS is a 16-bit readable/writable register that specifies the on-chip peripheral module to be the source of the DMA transfer request for the given channel. DMARS\_0 specifies the source for channel 0, DMARS\_1 specifies the source for channel 1 and so on.

When bits MID and RID are set to a value other than the values listed in Table 35.4, the operation of this LSI is not guaranteed. Transfer requests from the source selected in DMARS are only valid when the resource selection bits (RS[3:0]) in DMACHCR have been set to B'1000. Otherwise, even if DMARS has been set, requests from the corresponding transfer request source are not accepted.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	MID[5:0]					RID[1:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Descriptions
15 to 8	—	—	R	Reserved These bits are always read as 0. The write value should always be 0.
7 to 2	MID[5:0]	000000	R/W	DMA Request Source Adoption ID5 to ID0 (MID) See Table 35.4.
1, 0	RID[1:0]	00	R/W	DMA Request Source Adoption ID1 and ID0 (RID) See Table 35.4.

**35.3.21 DMA Descriptor Base Address Registers 0 to 25 (DMADPBASE\_0 to DMADPBASE\_25)**

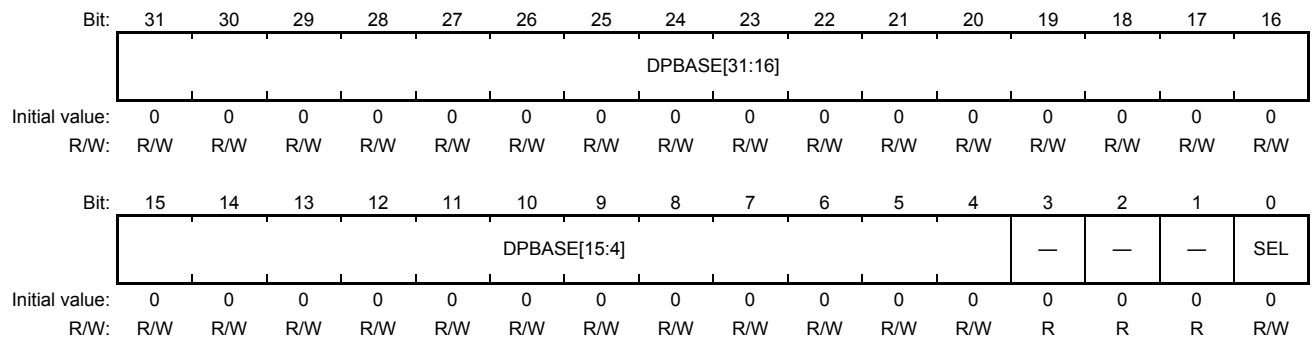
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Note: The availability of channels depends on the product as follows.

RZ/G1H and M/N: 26 channels (channels 0 to 25)

RZ/G1E: 13 channels (channels 0 to 12)

DMADPBASE specifies the base address of the descriptor memory. The address range of the descriptor memory is specified by setting this register.



Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 4	DPBASE[31:4]	All 0	R/W	Base Address of Descriptor Memory Place each stage of the descriptor memory on a 16-byte boundary. Setting example When Built-in memory is used, [Audio-DMAC Lower]: H'EC70 A000 to H'EC70 A7FC [Audio-DMAC Higher]: H'EC72 A000 to H'EC72 A7FC When External memory is used, Other memory area on a 16-byte boundary
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	SEL	0	R/W	Descriptor Memory Selection Select the memory to be used as descriptor memory. 0: Setting Prohibited 1: Built-in memory or External memory is used.

**35.3.22 DMA Descriptor Control Registers 0 to 25 (DMADPCR\_0 to DMADPCR\_25)**

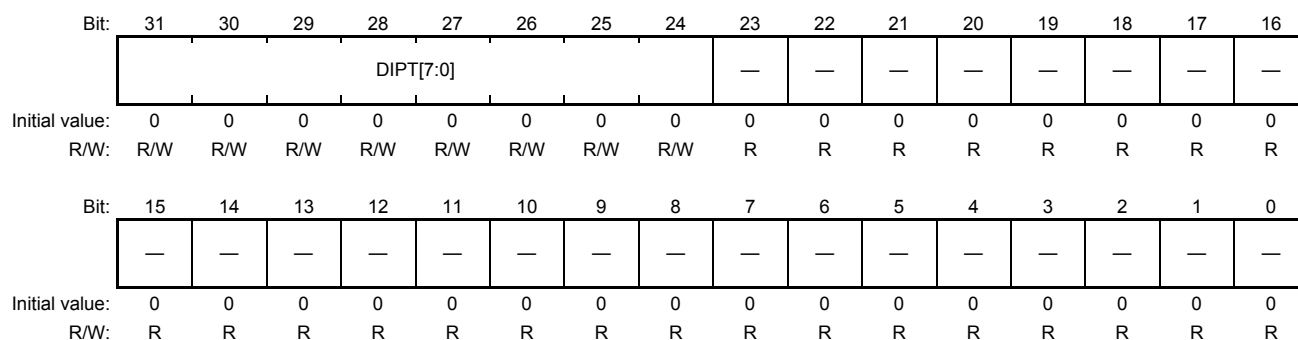
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Note: The availability of channels depends on the product as follows.

RZ/G1H and M/N: 26 channels (channels 0 to 25)

RZ/G1E: 13 channels (channels 0 to 12)

DMADPCR is a 32-bit readable/writable register that controls the timing with which interrupts are output in read-out interrupt mode (descriptor mode 3).



Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 24	DIPT[7:0]	H'00	R/W	Descriptor Read-out Interrupt Pointer The number of stages for which descriptor read-out interrupts are generated in descriptor mode 3. DIPT + 1 specifies the number of descriptor stages.
23 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

**35.3.23 DMA Fixed Source Address Registers 0 to 25 (DMAFIXSAR\_0 to DMAFIXSAR\_25)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

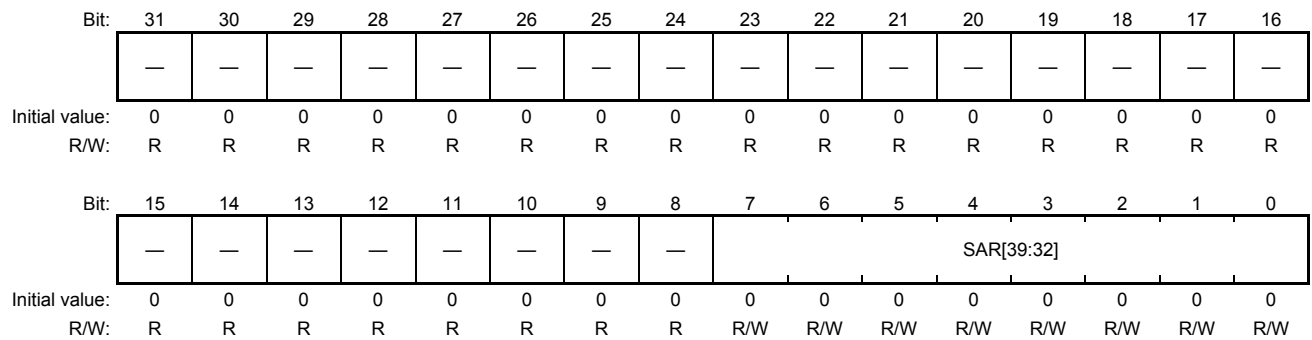
Note: The availability of channels depends on the product as follows.

RZ/G1H and M/N: 26 channels (channels 0 to 25)

RZ/G1E: 13 channels (channels 0 to 12)

DMAFIXSAR is a 32-bit readable/writable register that specifies the most significant 8 bits of the 40-bit source address for a DMA transfer.

This register is not incremented by carrying when DMASAR overflows.



**35.3.24 DMA Fixed Destination Address Registers 0 to 25 (DMAFIXDAR\_0 to DMAFIXDAR\_25)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

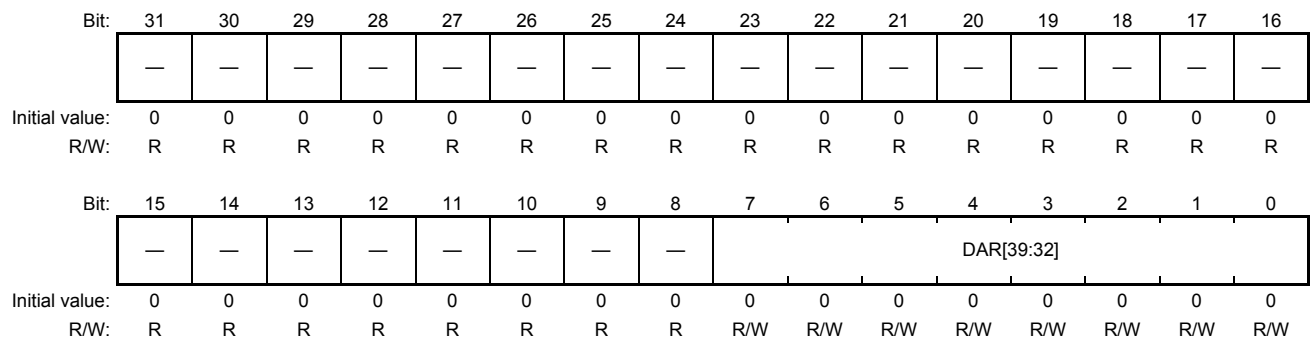
Note: The availability of channels depends on the product as follows.

RZ/G1H and M/N: 26 channels (channels 0 to 25)

RZ/G1E: 13 channels (channels 0 to 12)

DMAFIXDAR is a 32-bit readable/writable register that specifies the most significant 8 bits of the 40-bit destination address for a DMA transfer.

This register is not incremented by carrying when DMADAR overflows.



**35.3.25 DMA Fixed Descriptor Base Address Registers 0 to 25 (DMAFIXDPBASE\_0 to DMAFIXDPBASE\_25)**

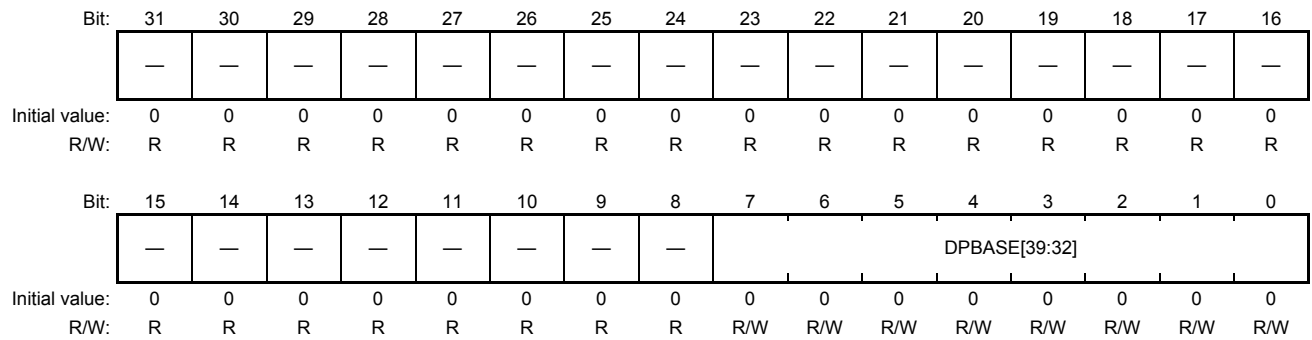
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Note: The availability of channels depends on the product as follows.

RZ/G1H and M/N: 26 channels (channels 0 to25)

RZ/G1E: 13 channels (channels 0 to 12)

DMAFIXDPBASE is a 32-bit readable/writable register that specifies the most significant 8 bits of the 40-bit descriptor base address for a DMA transfer.



**35.3.26 Descriptor Memory (DescriptorMEM)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

See section 35.4.4, Descriptor Memory for the descriptor memory.

## 35.4 Operation

RZ/G1H	RZ/G1N
RZ/G1M	RZ/G1E

When there is a DMA transfer request, the DMAC starts the transfer according to the predetermined channel priority; when the transfer end conditions are satisfied, it ends the transfer. Transfers can be requested in two modes: auto request and on-chip peripheral module request. The bus mode can be selected from normal speed mode and slow speed mode).

### 35.4.1 DMA Transfer Requests

Most commonly, DMA transfer requests are generated by either the source or destination for transfer, but they can also be generated by on-chip peripheral modules that are neither the source nor the destination. Transfers can be requested in two modes: auto request, and on-chip peripheral module request. The request mode is selected for each channel by DMARS.

#### (1) Auto-Request Mode

When there is no transfer request signal from an external source, as in a memory-to-memory transfer or a transfer between memory and an on-chip peripheral module unable to request a transfer, auto-request mode allows the audio-DMAC to automatically generate a transfer request signal internally. When the DE bit in DMACHCR and the DME bit in DMAOR are set to 1 for the target channel, the transfer begins so long as the CAE bit in DMACHCR is 0.

#### (2) On-Chip Peripheral Module Request Mode

In this mode, a transfer is performed at the transfer request signal of an on-chip peripheral module. The source (on-chip peripheral module) of the DMA transfer request is specified by DMARS.

When this mode is selected, if the DMA transfer is enabled (DE = 1, DME = 1, TE = 0, CAE = 0), a transfer is performed upon the input of a transfer request signal.

When a transmit data empty transfer request of the SCIF is set as the transfer request, the transfer destination must be the SCIF's transmit data register. Likewise, when receive data full transfer request of the SCIF is set as the transfer request, the transfer source must be the SCIF's receive data register. These conditions also apply to the other on-chip peripheral modules.

The number of the receive FIFO triggers can be set as a transfer request depending on an on-chip peripheral module. Data needs to be read after the DMA transfer is ended, because data may be left in the receive FIFO when the receive FIFO trigger condition is not satisfied.

Table 35.4 Selecting On-Chip Peripheral Module Request Modes

DMARS MID + RID	DMA Transfer Request Source	DMA Transfer Request Signal	Source	Destination	RZ/G Series Products			
					RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
H'85	SCU0	Transmit	Arbitrary		√	√	√	√
H'87	SCU1	Transmit	Arbitrary		√	√	√	√
H'89	SCU2	Transmit	Arbitrary		√	√	√	√
H'8B	SCU3	Transmit	Arbitrary		√	√	√	√
H'8D	SCU4	Transmit	Arbitrary		√	√	√	√
H'8F	SCU5	Transmit	Arbitrary		√	√	√	√
H'91	SCU6	Transmit	Arbitrary		√	√	√	-
H'93	SCU7	Transmit	Arbitrary		√	√	√	-
H'95	SCU8	Transmit	Arbitrary		√	√	√	-
H'97	SCU9	Transmit	Arbitrary		√	√	√	-
H'BC	SCUCMD0	Receive		Arbitrary	√	√	√	√
H'BE	SCUCMD1	Receive		Arbitrary	√	√	√	√
H'9A	SCUOUT0	Receive		Arbitrary	√	√	√	√
H'9C	SCUOUT1	Receive		Arbitrary	√	√	√	√
H'9E	SCUOUT2	Receive		Arbitrary	√	√	√	√
H'A0	SCUOUT3	Receive		Arbitrary	√	√	√	√
H'B0	SCUOUT4	Receive		Arbitrary	√	√	√	√
H'B2	SCUOUT5	Receive		Arbitrary	√	√	√	√
H'B4	SCUOUT6	Receive		Arbitrary	√	√	√	-
H'B6	SCUOUT7	Receive		Arbitrary	√	√	√	-
H'B8	SCUOUT8	Receive		Arbitrary	√	√	√	-
H'BA	SCUOUT9	Receive		Arbitrary	√	√	√	-
H'15	SSI0_0 transmitter	TXI (Transmit data request)	Arbitrary	ssip00	√	√	√	√
H'16	SSI0_0 receiver	RXI (Receive data request)	ssip00	Arbitrary	√	√	√	√
H'35	SSI0_1 transmitter	TXI (Transmit data request)	Arbitrary	ssip01	√	√	√	√
H'36	SSI0_1 receiver	RXI (Receive data request)	ssip01	Arbitrary	√	√	√	√
H'37	SSI0_2 transmitter	TXI (Transmit data request)	Arbitrary	ssip02	√	√	√	√
H'38	SSI0_2 receiver	RXI (Receive data request)	ssip02	Arbitrary	√	√	√	√
H'47	SSI0_3 transmitter	TXI (Transmit data request)	Arbitrary	ssip03	√	√	√	√
H'48	SSI0_3 receiver	RXI (Receive data request)	ssip03	Arbitrary	√	√	√	√
H'49	SSI1_0 transmitter	TXI (Transmit data request)	Arbitrary	ssip10	√	√	√	√
H'4A	SSI1_0 receiver	RXI (Receive data request)	ssip10	Arbitrary	√	√	√	√
H'4B	SSI1_1 transmitter	TXI (Transmit data request)	Arbitrary	ssip11	√	√	√	√
H'4C	SSI1_1 receiver	RXI (Receive data request)	ssip11	Arbitrary	√	√	√	√

DMARS MID + RID	DMA Transfer Request Source	DMA Transfer Request Signal	Source	Destination	RZ/G Series Products			
					RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
H'57	SSI1_2 transmitter	TXI (Transmit data request)	Arbitrary	ssip12	√	√	√	√
H'58	SSI1_2 receiver	RXI (Receive data request)	ssip12	Arbitrary	√	√	√	√
H'59	SSI1_3 transmitter	TXI (Transmit data request)	Arbitrary	ssip13	√	√	√	√
H'5A	SSI1_3 receiver	RXI (Receive data request)	ssip13	Arbitrary	√	√	√	√
H'63	SSI2_0 transmitter	TXI (Transmit data request)	Arbitrary	ssip20	√	√	√	√
H'64	SSI2_0 receiver	RXI (Receive data request)	ssip20	Arbitrary	√	√	√	√
H'67	SSI2_1 transmitter	TXI (Transmit data request)	Arbitrary	ssip21	√	√	√	√
H'68	SSI2_1 receiver	RXI (Receive data request)	ssip21	Arbitrary	√	√	√	√
H'6B	SSI2_2 transmitter	TXI (Transmit data request)	Arbitrary	ssip22	√	√	√	√
H'6C	SSI2_2 receiver	RXI (Receive data request)	ssip22	Arbitrary	√	√	√	√
H'6D	SSI2_3 transmitter	TXI (Transmit data request)	Arbitrary	ssip23	√	√	√	√
H'6E	SSI2_3 receiver	RXI (Receive data request)	ssip23	Arbitrary	√	√	√	√
H'6F	SSI3 transmitter	TXI (Transmit data request)	Arbitrary	ssip3	√	√	√	√
H'70	SSI3 receiver	RXI (Receive data request)	ssip3	Arbitrary	√	√	√	√
H'71	SSI4 transmitter	TXI (Transmit data request)	Arbitrary	ssip4	√	√	√	√
H'72	SSI4 receiver	RXI (Receive data request)	ssip4	Arbitrary	√	√	√	√
H'73	SSI5 transmitter	TXI (Transmit data request)	Arbitrary	ssip5	√	√	√	√
H'74	SSI5 receiver	RXI (Receive data request)	ssip5	Arbitrary	√	√	√	√
H'75	SSI6 transmitter	TXI (Transmit data request)	Arbitrary	ssip6	√	√	√	√
H'76	SSI6 receiver	RXI (Receive data request)	ssip6	Arbitrary	√	√	√	√
H'79	SSI7 transmitter	TXI (Transmit data request)	Arbitrary	ssip7	√	√	√	√
H'7A	SSI7 receiver	RXI (Receive data request)	ssip7	Arbitrary	√	√	√	√
H'7B	SSI8 transmitter	TXI (Transmit data request)	Arbitrary	ssip8	√	√	√	√
H'7C	SSI8 receiver	RXI (Receive data request)	ssip8	Arbitrary	√	√	√	√
H'7D	SSI9_0 transmitter	TXI (Transmit data request)	Arbitrary	ssip90	√	√	√	√
H'7E	SSI9_0 receiver	RXI (Receive data request)	ssip90	Arbitrary	√	√	√	√
H'7F	SSI9_1 transmitter	TXI (Transmit data request)	Arbitrary	ssip91	√	√	√	√
H'80	SSI9_1 receiver	RXI (Receive data request)	ssip91	Arbitrary	√	√	√	√
H'81	SSI9_2 transmitter	TXI (Transmit data request)	Arbitrary	ssip92	√	√	√	√
H'82	SSI9_2 receiver	RXI (Receive data request)	ssip92	Arbitrary	√	√	√	√
H'83	SSI9_3 transmitter	TXI (Transmit data request)	Arbitrary	ssip93	√	√	√	√
H'84	SSI9_3 receiver	RXI (Receive data request)	ssip93	Arbitrary	√	√	√	√



DMARS MID + RID	DMA Transfer Request Source	DMA Transfer Request Signal	Source	Destination	RZ/G Series Products			
					RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
H'01	SSIND0 transmitter	TXI (Transmit data request)	Arbitrary	ssindd0	√	√	√	√
H'02	SSIND0 receiver	RXI (Receive data request)	ssindd0	Arbitrary	√	√	√	√
H'03	SSIND1 transmitter	TXI (Transmit data request)	Arbitrary	ssindd1	√	√	√	√
H'04	SSIND1 receiver	RXI (Receive data request)	ssindd1	Arbitrary	√	√	√	√
H'05	SSIND2 transmitter	TXI (Transmit data request)	Arbitrary	ssindd2	√	√	√	√
H'06	SSIND2 receiver	RXI (Receive data request)	ssindd2	Arbitrary	√	√	√	√
H'07	SSIND3 transmitter	TXI (Transmit data request)	Arbitrary	ssindd3	√	√	√	√
H'08	SSIND3 receiver	RXI (Receive data request)	ssindd3	Arbitrary	√	√	√	√
H'09	SSIND4 transmitter	TXI (Transmit data request)	Arbitrary	ssindd4	√	√	√	√
H'0A	SSIND4 receiver	RXI (Receive data request)	ssindd4	Arbitrary	√	√	√	√
H'0B	SSIND5 transmitter	TXI (Transmit data request)	Arbitrary	ssindd5	√	√	√	√
H'0C	SSIND5 receiver	RXI (Receive data request)	ssindd5	Arbitrary	√	√	√	√
H'0D	SSIND6 transmitter	TXI (Transmit data request)	Arbitrary	ssindd6	√	√	√	√
H'0E	SSIND6 receiver	RXI (Receive data request)	ssindd6	Arbitrary	√	√	√	√
H'0F	SSIND7 transmitter	TXI (Transmit data request)	Arbitrary	ssindd7	√	√	√	√
H'10	SSIND7 receiver	RXI (Receive data request)	ssindd7	Arbitrary	√	√	√	√
H'11	SSIND8 transmitter	TXI (Transmit data request)	Arbitrary	ssindd8	√	√	√	√
H'12	SSIND8 receiver	RXI (Receive data request)	ssindd8	Arbitrary	√	√	√	√
H'13	SSIND9 transmitter	TXI (Transmit data request)	Arbitrary	ssindd9	√	√	√	√
H'14	SSIND9 receiver	RXI (Receive data request)	ssindd9	Arbitrary	√	√	√	√

**Table 35.5 Data Length of DMA Transfer for Each of the On-Chip Peripheral Modules**

Module	1 Byte	2 Bytes	4 Bytes	8 Bytes	16 Bytes	32 Bytes	RZ/G Series Products			
							RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
SCU0/SCU1/SCU2/ SCU3/SCU4/SCU5/ SCU6/SCU7/SCU8/ SCU9			✓				✓	✓	✓	✓
SCUCMD0/SCUCMD1			✓				✓	✓	✓	✓
SCUOUT0/SCUOUT1/ SCUOUT2/SCUOUT3/ SCUOUT4/SCUOUT5/ SCUOUT6/SCUOUT7/ SCUOUT8/SCUOUT9			✓				✓	✓	✓	✓
SSI0_0/SSI0_1/SSI0_2/ SSI0_3/SSI1_0/SSI1_1/ SSI1_2/SSI1_3/SSI2_0/ SSI2_1/SSI2_2/SSI2_3/ SSI3/SSI4/SSI5/SSI6/ SSI7/SSI8/SSI9_0/ SSI9_1/SSI9_2/SSI9_3			✓				✓	✓	✓	✓
SSIND0/1/2/3/4/5/6/7/8/ 9			✓				✓	✓	✓	✓

### 35.4.2 Channel Priority

When the audio-DMAC receives simultaneous transfer requests on two or more channels, it transfers data according to a predetermined priority. Two modes (fixed mode and round-robin mode) are selected by the PR[1:0] bits in DMAOR.

#### (a) Fixed Mode

In this mode, the priority levels among the channels remain fixed.

CH0 > CH1 > ... > CH11 > CH12, CH13 > CH14 > ... > CH24 > CH25

#### (b) Round-Robin Mode

In round-robin mode, each time data of one transfer unit (byte, word, longword, 8-byte or 16-byte units) is transferred on one channel, the priority is rotated. The channel on which the transfer was just finished rotates to the bottom of the priority. The priority of round-robin mode is CH0 > CH1 > ... > CH11 > CH12 and CH13 > CH14 > ... > CH24 > CH25 immediately after reset.

### 35.4.3 Slow Speed Mode

In the low-speed mode, a single round of DMA transfer is performed every time the number of clock cycles specified by the SLM bits in DMACHCRB elapse. This mode can be selected per DMA channel. Transfer on other channels can proceed after each round of transfer for a channel in the low-speed mode is completed.

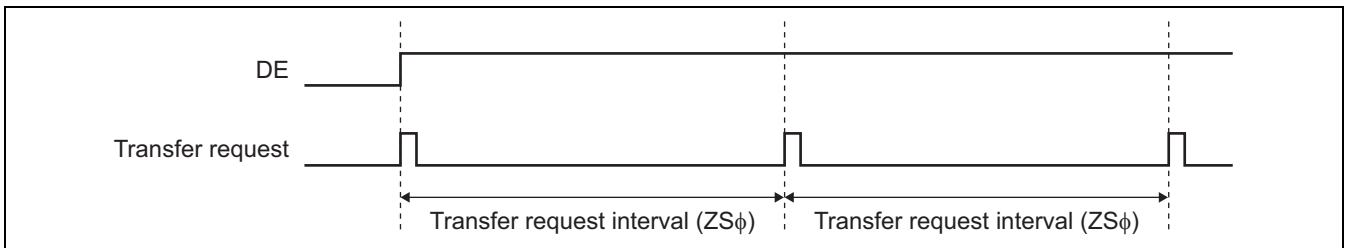


Figure 35.2 Slow Speed Mode

### 35.4.4 Descriptor Memory

The descriptor memory function is selected by setting the DPM[1:0] bits in DMACHCR to B'01, B'10, or B'11. When DMATCR is set to 0 and the DMA transfer is completed, the next set of settings is read, and if only a single channel is enabled, the contents defined by up to 128 stages of descriptor memory can be consecutively transferred when the built-in descriptor memory is used. External memory can also be used as the descriptor memory. In that case, the contents defined by up to 256 stages of descriptor memory can be transferred.

The following initial settings are required to use the descriptor memory.

- Set the base address of the descriptor memory for the DMA transfer in DMADPBASE.
- Set the DRST bit in DMACHCRB to reset the descriptor memory.
- Set the number of stages of the descriptor memory in the DCNT bits of DMACHCRB.

The descriptor memory is shared between all channels. Ensure that the areas of descriptor memory for use by each of the channels do not overlap. It is necessary to arrange each stage of the descriptor memory on a 16-byte boundary.

There are two methods to activate the descriptor memory as follows.

- Specify the first DMA transfer settings in DMASAR, DMADAR, and DMATCR, and specify the subsequent settings in the descriptor memory. Then, set the DPB bit in DMACHCR to 0 to activate the descriptor memory. In this case, after completion of the transfer specified in DMASAR, DMADAR, and DMATCR, transfer continues after new settings are read from the descriptor memory. Note, however, that, when the operating mode of the descriptor memory is set to the repeat mode, the values specified in DMASAR, DMADAR, and DMATCR are not read, and the transfer starts and is repeated from the head of the descriptor memory.
- Write the DMA transfer settings to the descriptor memory, and write 1 to the DPB bit in DMACHCR to activate the descriptor memory. In this case, the DMA transfer starts from the first settings in the descriptor memory.

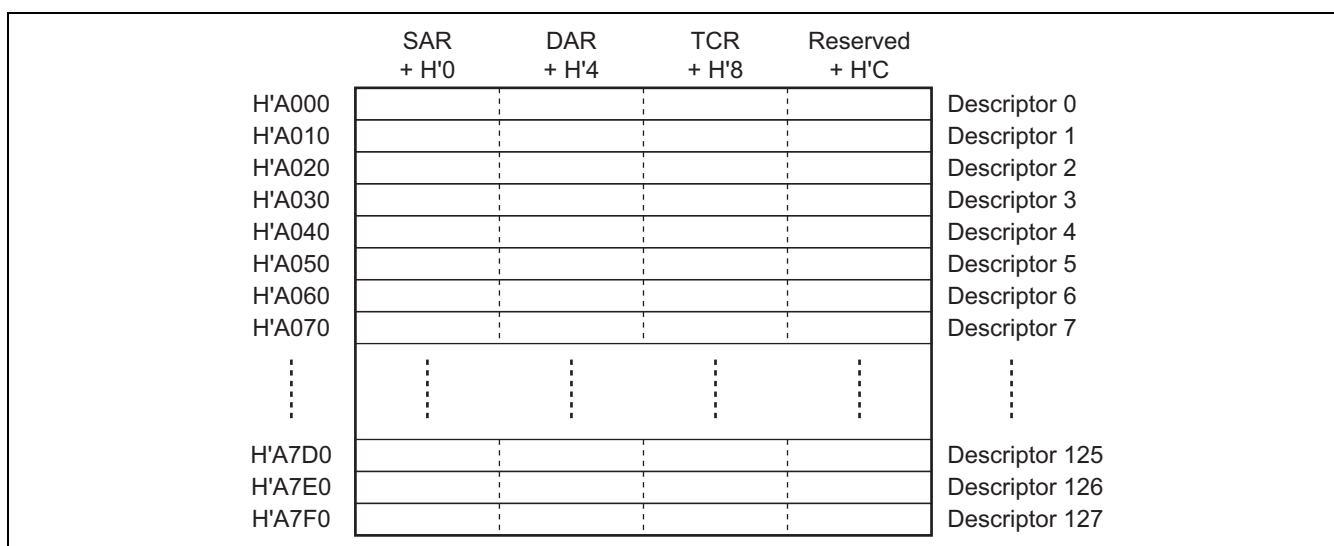
There are three operating modes of the descriptor memory, which can be selected by setting the DPM bits in DMACHCR.

For details on these operating modes, see the descriptions of each operating mode in this section.

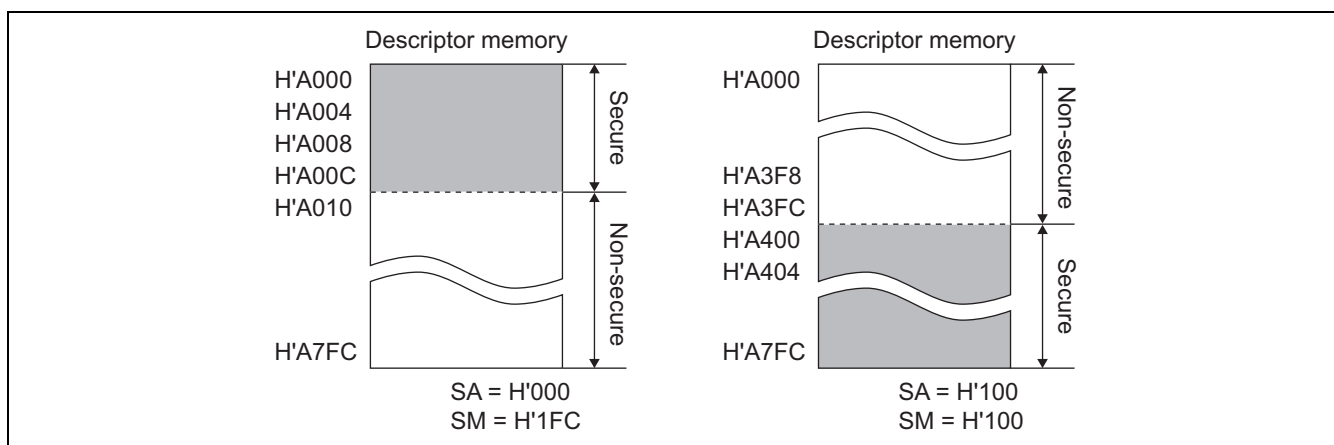
**(1) Configuration of Descriptor Memory**

Figure 35.3 shows the configuration of the built-in descriptor memory.

The capacity of the built-in descriptor memory is 16 bytes per stage × 128 stages.



**Figure 35.3 Configuration of Built-in Descriptor Memory**



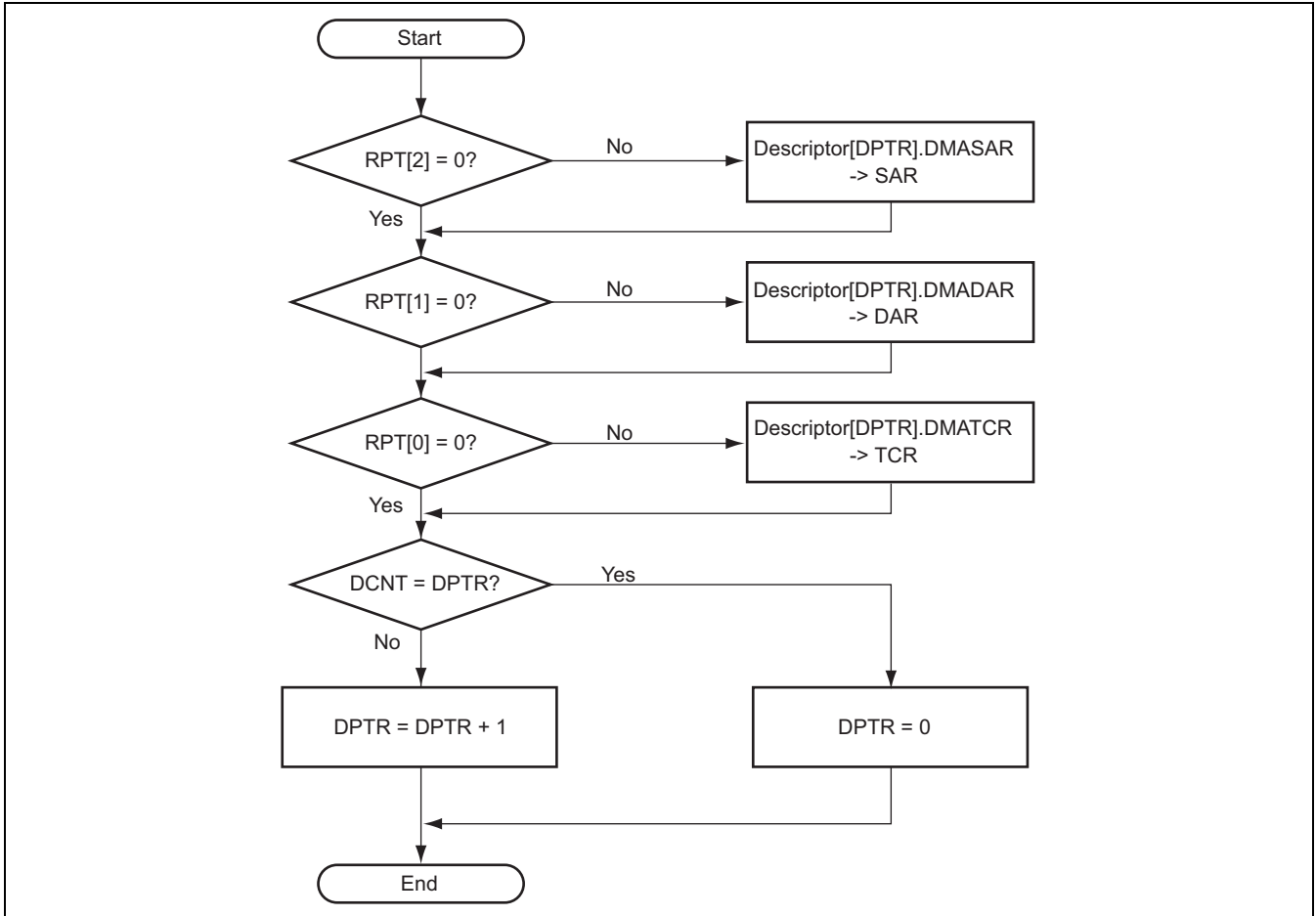
**Figure 35.4 Example of DMADPSEC Setting**

**(2) Flow of Updating from Descriptor Memory**

The RPT bits in DMACHCR can be used to specify which registers are to be updated from the descriptor memory.

The DPTR bits in DMACHCRB are incremented when updating from the descriptor memory is completed. If the DPTR value matches the DCNT value, the DPTR value is reset to 0.

This flow is automatically processed by hardware.



**Figure 35.5 Flow of Updating from Descriptor Memory**

**(3) Operating Mode 1 of Descriptor Memory**

Set the DPM bits in DMACHCR to B'01 to select operating mode 1 (normal mode). This mode allows consecutive transfer under control of the descriptor memory.

In this mode, the DMA transfer is complete when the TE bit in DMACHCR is set to 1 after transfer under control of the number of stages of the descriptor memory specified in the DCNT bits in DMACHCRB.

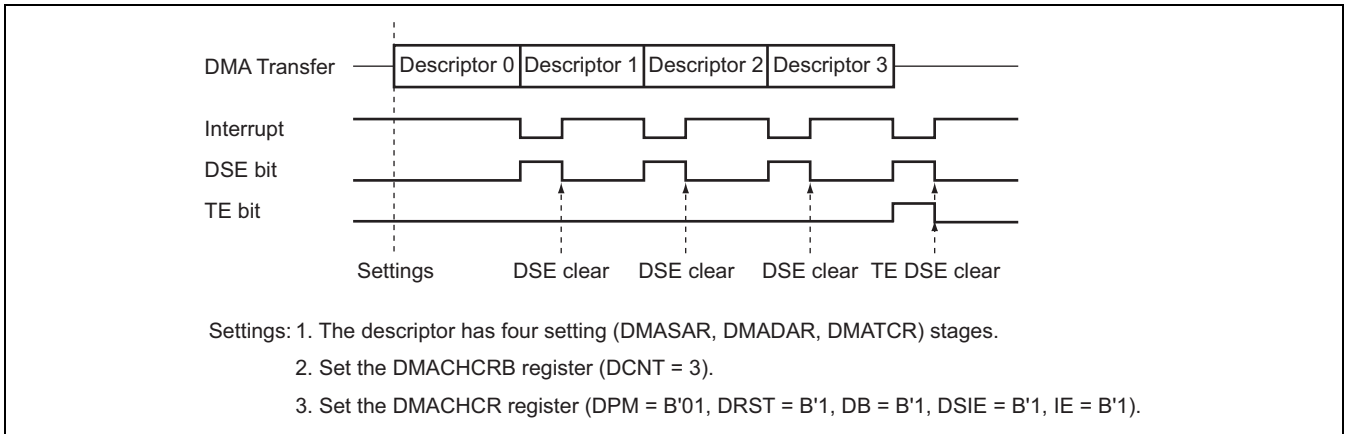
When the DSIE bit in DMACHCR is set to 1, a DSE interrupt is generated every time transfer under the control of one stage of descriptor memory is complete. If a first DSE interrupt has not been processed when a further DSE interrupt is generated, the contents of the next stage of the descriptor memory are not read and the DMA transfer is aborted. Clearing the DSE bit only causes clearing of the first interrupt and reading of the next stage of the descriptor memory.

Figure 35.6 is an example of transfer when operating mode 1 is selected and the TE and DSE bits are set to 1.

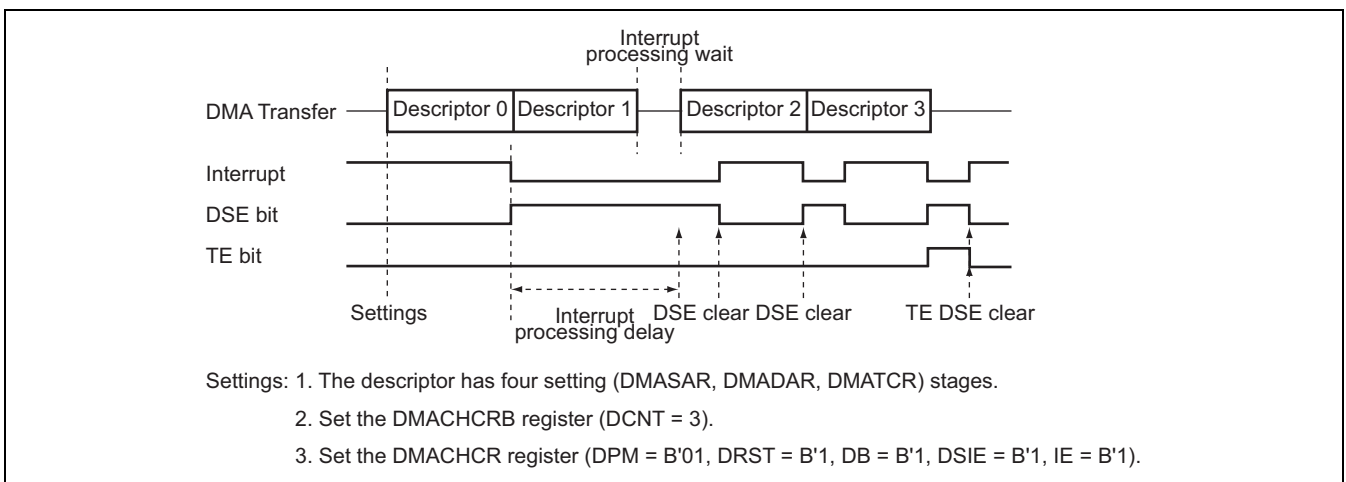
Figure 35.7 is an example of transfer when there is a delay in processing of the DSE interrupt when operating mode 1 is selected and the TE and DSE bits are set to 1.

Figure 35.8 is an example of transfer when operating mode 1 is selected and the TE bit is set to 1.

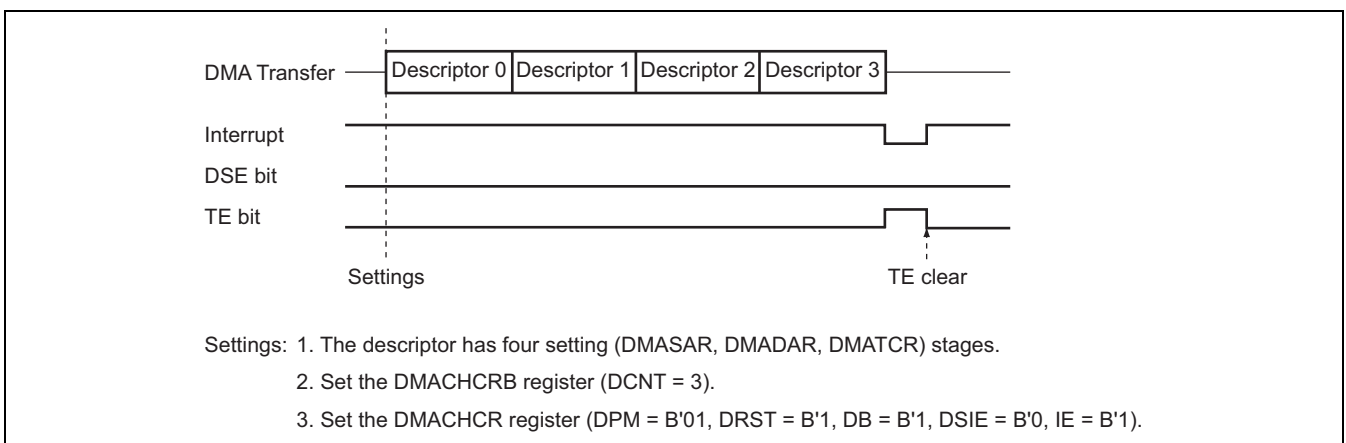
In each example, there are four descriptor stages.



**Figure 35.6 Operating Mode 1 (Example 1)**



**Figure 35.7 Operating Mode 1 (Example 2)**



**Figure 35.8 Operating Mode 1 (Example 3)**

#### (4) Operating Mode 2 of Descriptor Memory

Set the DPM bits in DMACHCR to B'10 to select operating mode 2 (repeat mode). This mode allows consecutive transfer under control of the descriptor memory.

In this mode, after transfer under control of the number of stages of descriptor memory specified in the DCNT bits in DMACHCRB, the TE bit in DMACHCR is set to 1. This operation is then repeated from the head of the descriptor memory.

When the DSIE bit in DMACHCR is set to 1, a DSE interrupt is generated every time transfer under the control of one stage of descriptor memory is complete. If a first DSE interrupt has not been processed when a further DSE interrupt is generated, the contents of the next stage of the descriptor memory are not read and the DMA transfer is aborted. Clearing the DSE bit only causes clearing of the first interrupt and reading of the next stage of the descriptor memory.

When the DSIE bit in DMACHCR is set to 0, after transfer under control of all stages of the descriptor memory is complete, the TE bit in DMACHCR is set to 1 and a TE interrupt is generated. If a TE interrupt has not been processed when a further interrupt is generated, the contents of the next stage of the descriptor memory are not read and the DMA transfer is aborted. Clearing the TE bit only causes clearing of the first interrupt and reading of the next stage of the descriptor memory.

To end operation in mode 2, change the mode to mode 1 by using the TE interrupt processing. When the mode is changed to mode 1, the DMA transfer is completed when the next TE interrupt is generated.

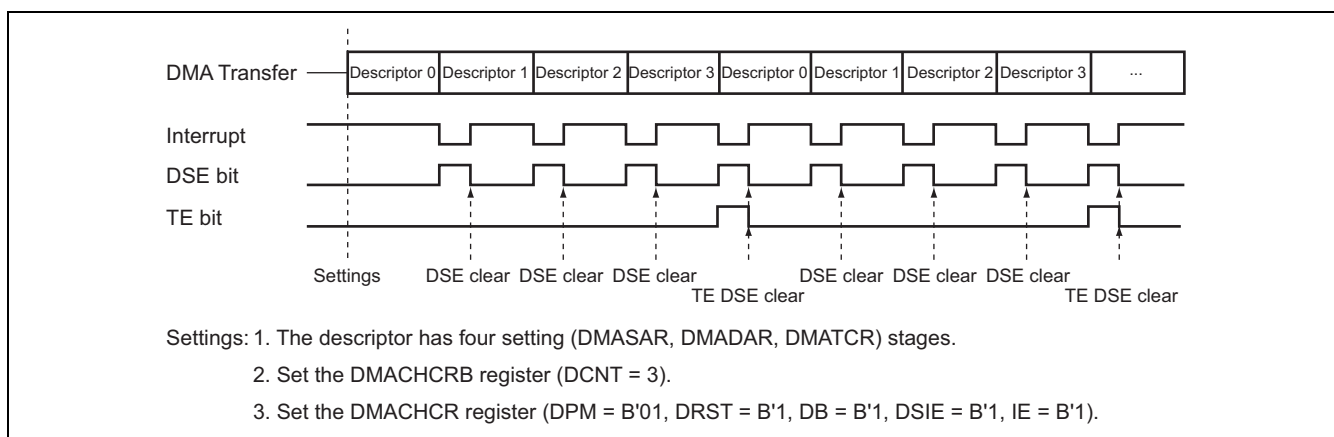
Figure 35.9 is an example of transfer when operating mode 2 is selected and the TE and DSE bits are set to 1.

Figure 35.10 is an example of transfer when there is a delay in processing of the DSE interrupt when operating mode 2 is selected and the TE and DSE bits are set to 1.

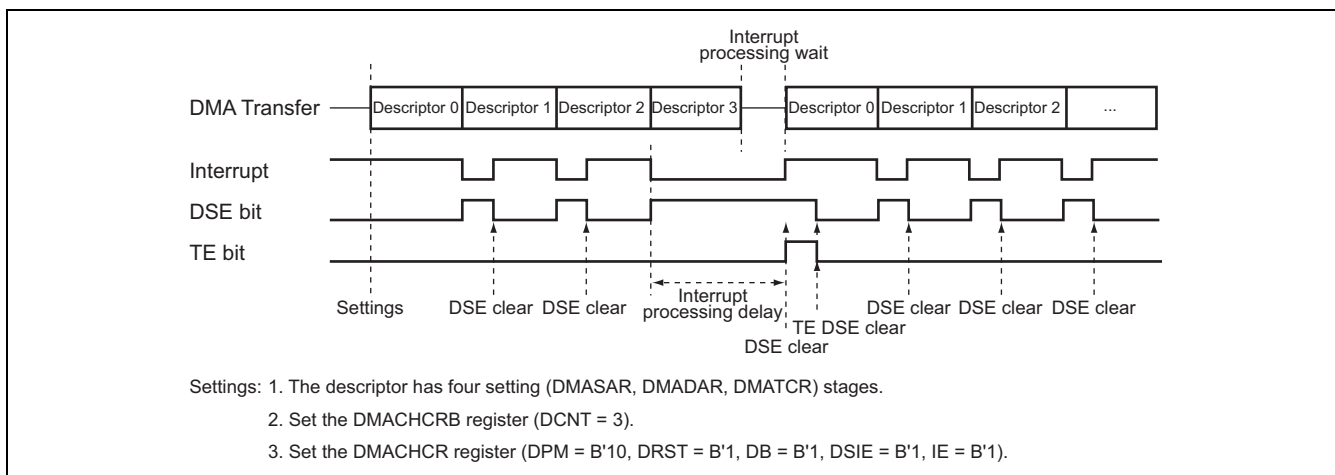
Figure 35.11 is an example of transfer when operating mode 2 is selected and the TE bit is set to 1.

Figure 35.12 is an example of transfer when there is a delay in processing of the DSE interrupt when operating mode 2 is selected and the TE is set to 1.

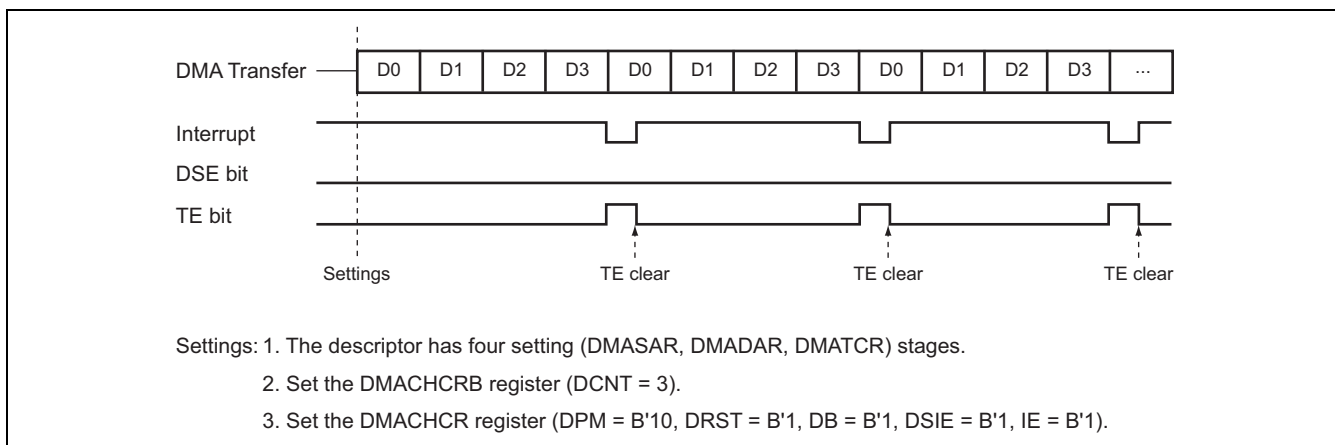
In each example, there are four descriptor stages.



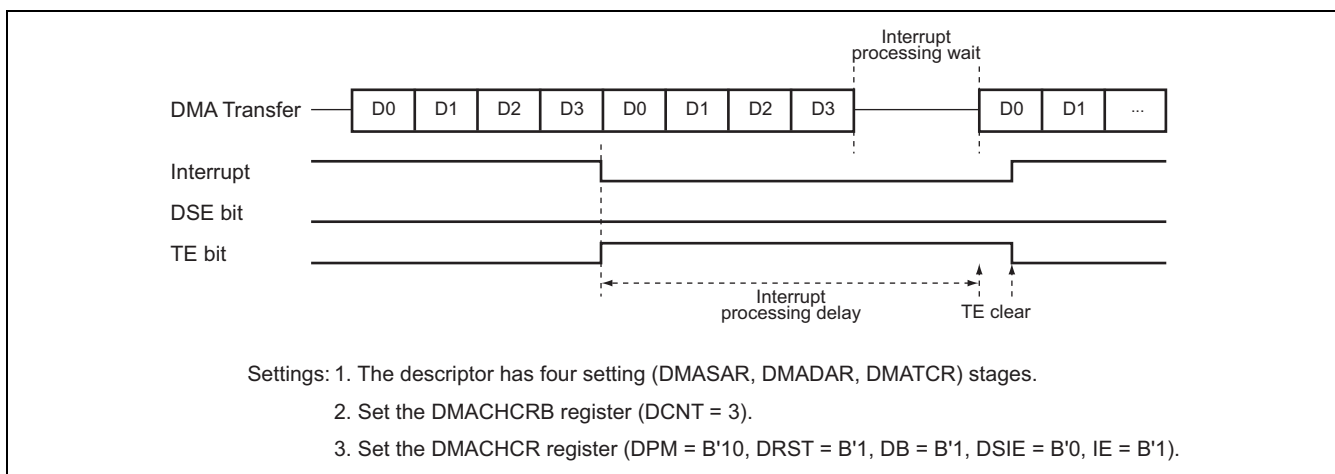
**Figure 35.9 Operating Mode 2 (Example 1)**



**Figure 35.10 Operating Mode 2 (Example 2)**



**Figure 35.11 Operating Mode 2 (Example 3)**



**Figure 35.12 Operating Mode 2 (Example 4)**



### (5) Operating Mode 3 of Descriptor Memory

Set the DPM bits in DMACHCR to B'11 to select operating mode 3 (infinite repeat mode). This mode allows consecutive transfer under control of the descriptor memory.

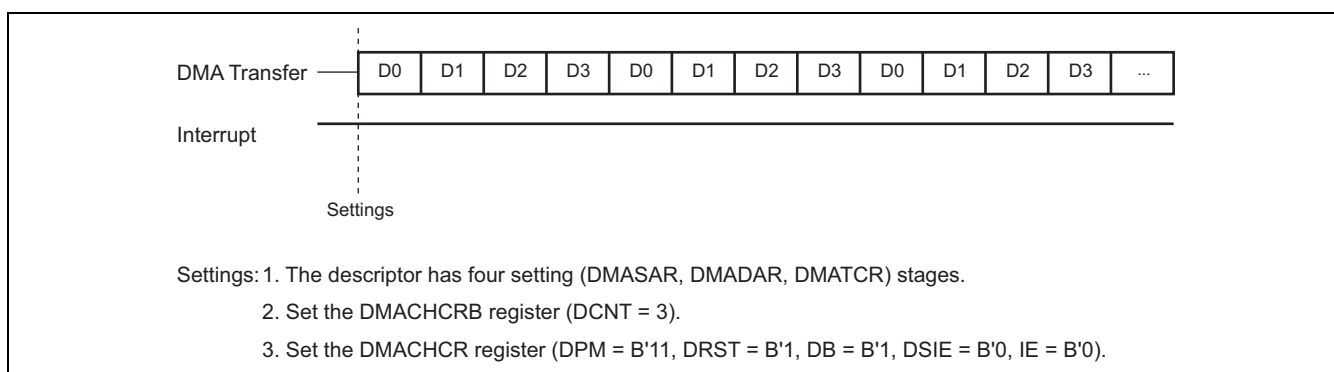
In this mode, after transfer under control of the number of stages of descriptor memory specified in the DCNT bits in DMACHCRB, the TE bit in DMACHCR is set to 1. This operation is then repeated from the head of the descriptor memory.

When the DSIE bit in DMACHCR is set to 1, a DSE interrupt is generated every time transfer under the control of one stage of descriptor memory is complete. Even if a first DSE interrupt has not been processed when a further DSE interrupt is generated, the DMA transfer is not aborted. Regardless of the number of DSE interrupts that have been generated, the DSE bit can be cleared by writing to it once. Similarly, even if a first TE interrupt has not been processed when a further TE interrupt is generated, the DMA transfer is not aborted. Regardless of the number of TE interrupts that have been generated, the TE bit can be cleared by writing to it once.

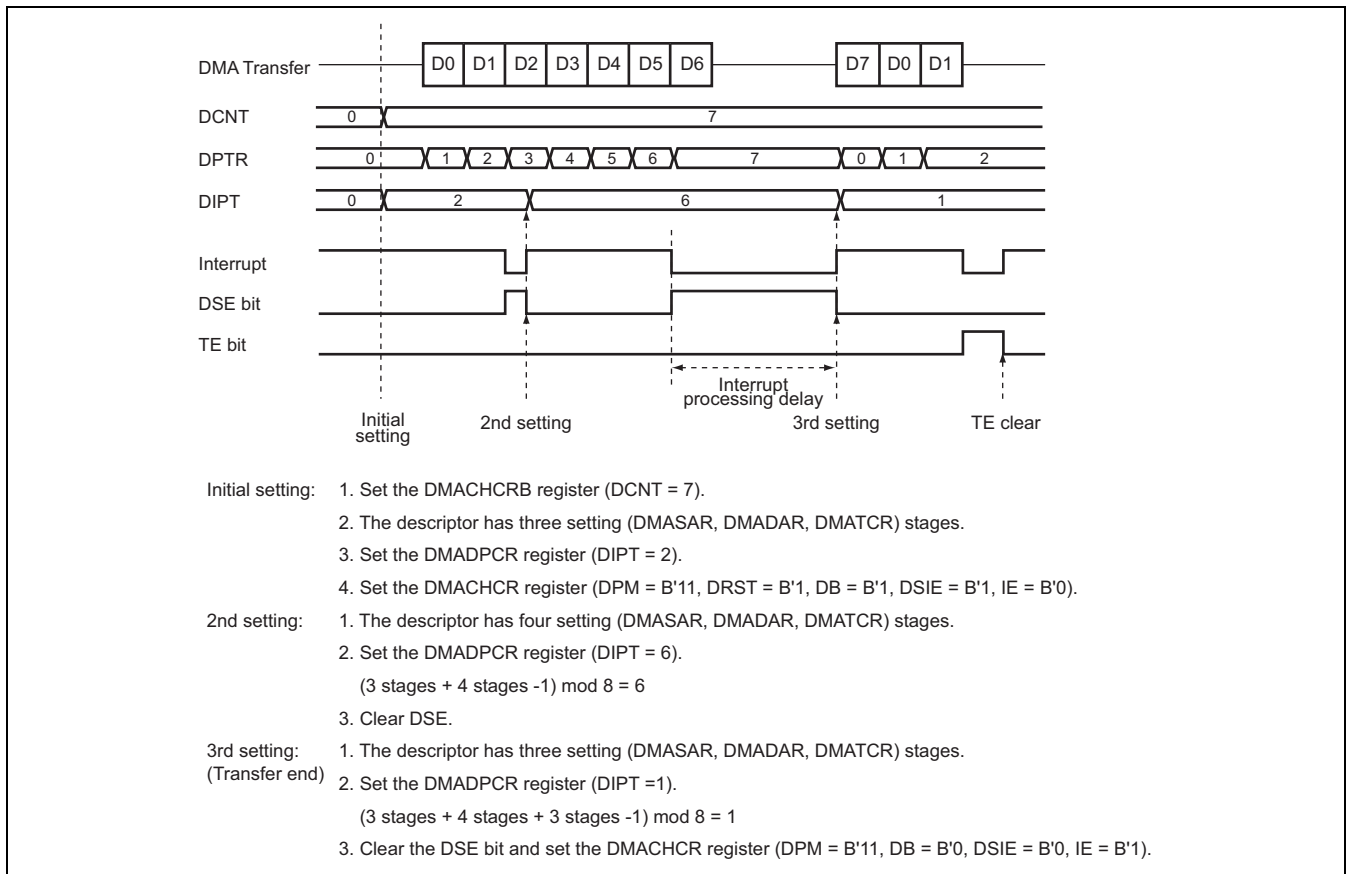
Figure 35.13 is an example of transfer when infinite repeat mode is selected.

Figure 35.14 is an example of transfer when read-out interrupt mode is selected.

In each example, there are four descriptor stages.



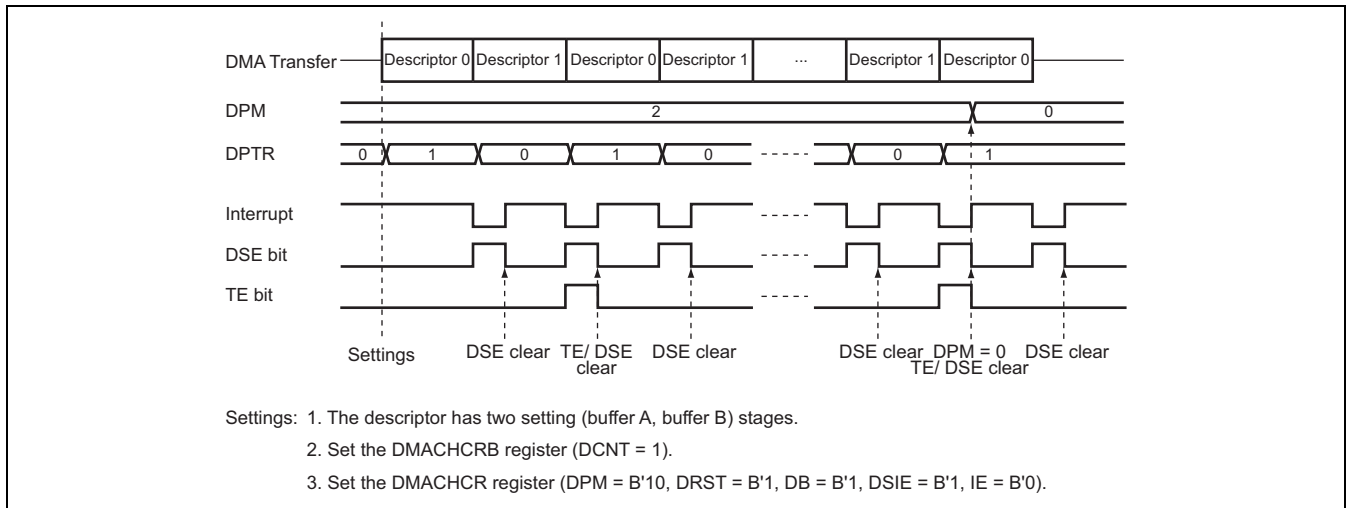
**Figure 35.13 Operating Mode 3 (Infinite Repeat Mode)**



**Figure 35.14 Operating Mode 3 (Read-Out Interrupt Mode)**

**(6) Using the Descriptor Memory for Double Buffering**

To use the descriptor memory for double buffering, set the number of stages of descriptor memory to 2, set the buffer configuration to the descriptor memory, and activate the memory in operating mode 2. The DSE interrupt is used in double buffering. To end the use of double buffering, disable the descriptor operating mode, which stops the transfer on completion of the transfer currently in progress.



**Figure 35.15 Using the Descriptor Memory for Double Buffering**

### 35.4.5 Transmission Flow

Set the transfer conditions as required in the following registers:

DMA source address register (DMASAR), DMA destination address register (DMADAR), DMA transfer count register (DMATCR), DMA Channel control register (DMACHCR), DMA operation register (DMAOR) and DMA extended resource selector (DMARS)

The DMAC then transmits data in the following order.

- A transfer request is generated and the controller checks whether the transfer is allowed (DE = 1, DME = 1, TE = 0, DSE = 0, CAE = 0). When a channel is in the auto request mode, the transfer starts automatically.
- The controller checks whether updating from the descriptor memory is required.  
Updating from the descriptor memory proceeds when the DPB bit in DMACHCR is set to 1 or the descriptor memory is enabled, if DMATCR is set to 0.  
For updating by using the descriptor memory, see section 35.4.4, Descriptor Memory.
- Check whether address translation by the IPMMU is required.  
Address translation by the IPMMU proceeds if the address exceeds the effective size for address translation when the DE bit in DMACHCR is enabled and updating of transfer settings from the descriptor memory is executed.
- Each time a transfer request is generated, the amount of data for a single round of transfer (specified by the TS[3:0] bits) is transmitted. The value in DMATCR is decremented by 1 every time the DMA transfer is completed.
- When the specified number of rounds of transfer are completed (the value in DMATCR is set to 0), the transfer ends normally. A TE interrupt is generated for the CPU upon the end of the transfer if the IE bit in DMACHCR is set to 1. If the descriptor memory is enabled, the processing differs with the mode of the descriptor memory. For more details, see section 35.4.4, Descriptor Memory.
- Transfer is aborted when the DMAC encounters an address error. Transfer is also aborted when the DE bit in DMACHCR or the DME bit in DMAOR is set to 0.

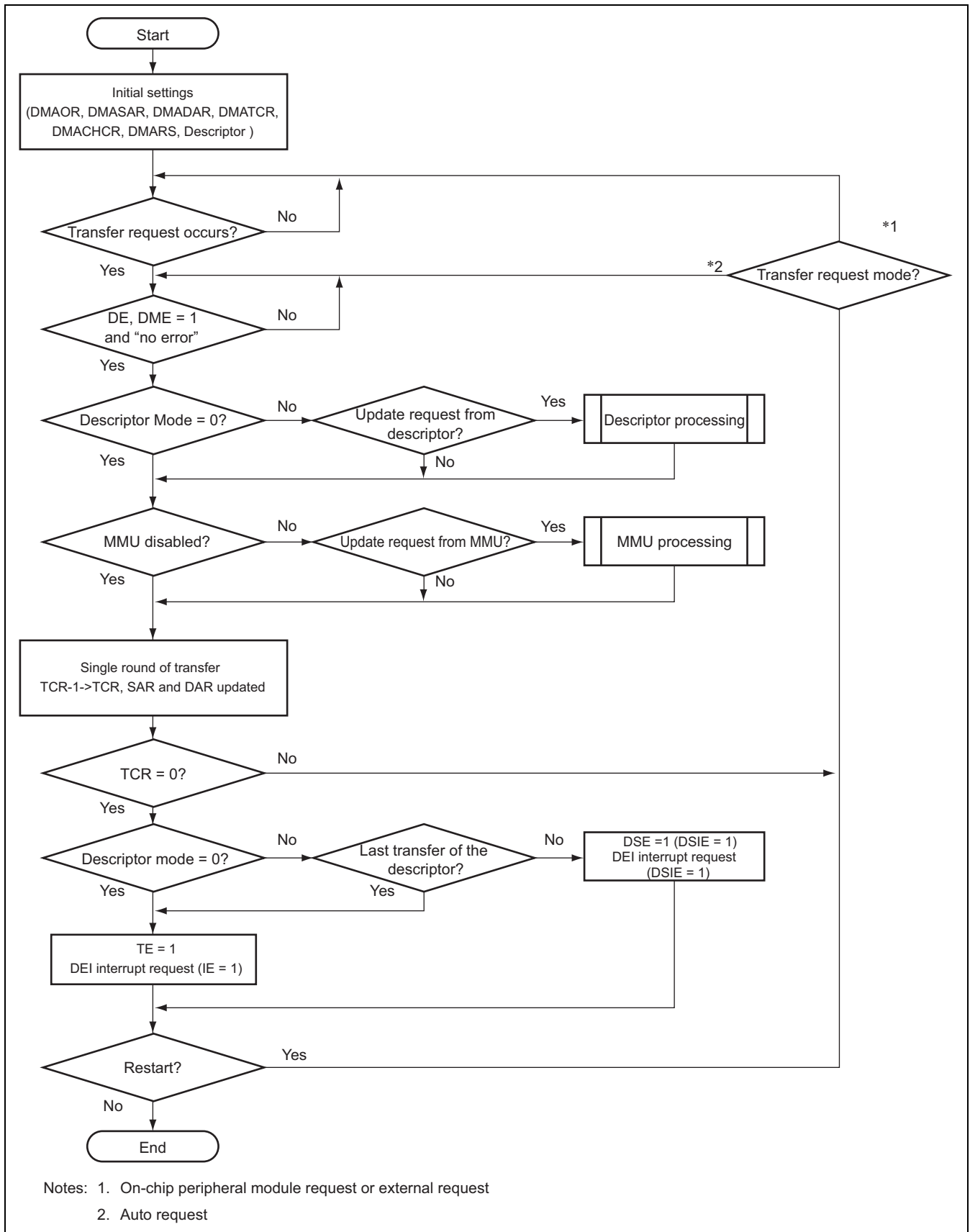


Figure 35.16 Transmission Flow

### 35.4.6 Total Size Transmission

The amount of data for total size transmission can be set in DMATSR (in bytes), and this setting is effective regardless of the size specified in the TS bits in DMACHCR. Thereby, the desired size can be transmitted in a single round of DMA transfer.

To use this function, make the settings for total size transmission in DMASAR, DMADAR, DMATSR, DMATSRB and DMACHCR.

Total size is set in the TCR (TSR) field of descriptors and 1 is set in DMACHCRB.DTS when total size transmission and descriptors are in use.

## 35.5 Usage Notes

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

Pay attention to the following notes when using the audio-DMAC.

### (1) DMA Transfer for Peripheral Modules

When executing DMA transfer for an on-chip peripheral module, set addresses on the appropriate boundary (in terms of the amount of data for each round of transfer) for the transfer source and destination addresses. Otherwise, an address error may occur.

### (2) Module Stop

While the audio-DMAC is operating, the module stop register (MSTPCR5) should not be set to stop the audio-DMAC. If the audio-DMAC is stopped in this way, results of the transfer that was in progress cannot be guaranteed.

### (3) Address Error

When a DMA address error is generated, reset the registers of the channel on which the error has occurred and then start transfer anew.

### (4) Aborting DMA Transfer

To abort a DMA transfer, disable the interrupt signal and set the DE bit in the DMA channel control register (DMACHCR) to 0 to disable the DMA transfer. If the TE and DSE bits are set when DMA transfer is aborted, these bits should be initialized. There is a possibility that TE and DSE will not be set with synchronized timing after transmission, so it's necessary to recognize the following three possibilities and take measures accordingly.

1. The DSE and TE bits are set to 1 before initialization of DMACHCR, but after the interrupt was disabled.  
The TE and DSE bits are initialized within the DMA transfer initialization sequence.
2. The DSE and TE bits are set to 1 and the controller fails to abort the transfer, after the interrupt was disabled.  
When the DE bit has become 0 after DMA transfer initialization, check the TE and DSE bits. If the TE or DSE bit is 1, go through the DMA transfer initialization process.
3. The TE and DSE bits are not cleared to 0 but the transfer is aborted, after the interrupt is disabled.  
The TE or DSE bits are not set because data for transfer still remain after transfer is aborted.

Note: Initialization of DMA transfer during execution of the last transfer leads to a delay in setting of the TE and DSE bits, so include a dummy read.

Figure 35.17 shows an example of processing to abort DMA transfer.

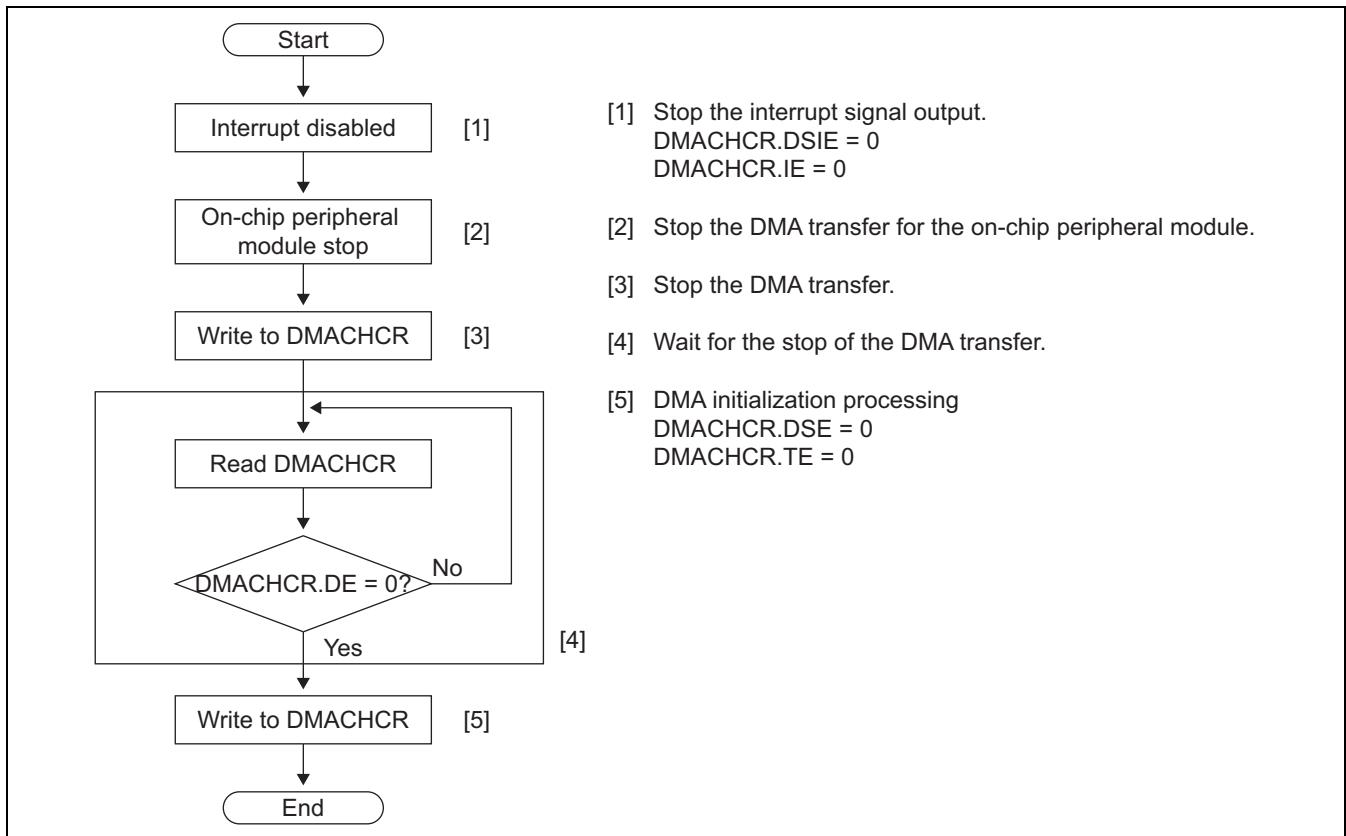


Figure 35.17 Example of Processing to Abort DMA Transfer

### (5) Descriptor Transfer

When using the descriptor transfer in cases where both conditions 1) and 2) apply, an incorrect DMA transfer proceeds before the correct transfer starts.

- Conditions

- The timing of the start of transfer is specified as being after the descriptor information is loaded, i.e. DPB = 1.  
Audio-DMAC: DMACHCR\_n.DPB = 1 (refer to the description of bit 22 in section 35.3.17)
- Address translation by the uTLB is enabled.

- Problem

When both conditions 1) and 2) apply, an incorrect DMA read transfer to the address formerly stored in DAR proceeds after DMA is enabled (DE = 1). Furthermore, if the address is undefined in the IPMMU, the DMA transfer may stop and operation of the DMAC may hang up without any indication of the error.

[Workarounds]

- Use the descriptor transfer with DPB = 0.
- Use the descriptor transfer with DPB = 1 and address translation by the uTLB disabled.
- When using the descriptor transfer with DBP = 1 and address translation by the uTLB enabled, write the same destination address as the first address in the descriptor to the corresponding DAR before enabling DMA (DE = 1). While the incorrect DMA read transfer still proceeds, the descriptor transfer is executed correctly as long as the address written to the corresponding DAR is a defined address.



## 36. Audio DMAC-Peripheral-Peripheral

RZ/G1H	RZ/G1N
RZ/G1M	RZ/G1E

### 36.1 Overview

The Audio DMAC-Peripheral-Peripheral module controls data transfer between the audio modules connected to the audio local bus.

#### 36.1.1 Features

- Number of channels: 29 channels
- Data transfer size: Longwords (4 bytes)
- Addressing mode: Dual addressing; fixed access size
- Transfer count: Not programmable
- Interrupt processing: None

#### 36.1.2 Block Diagram

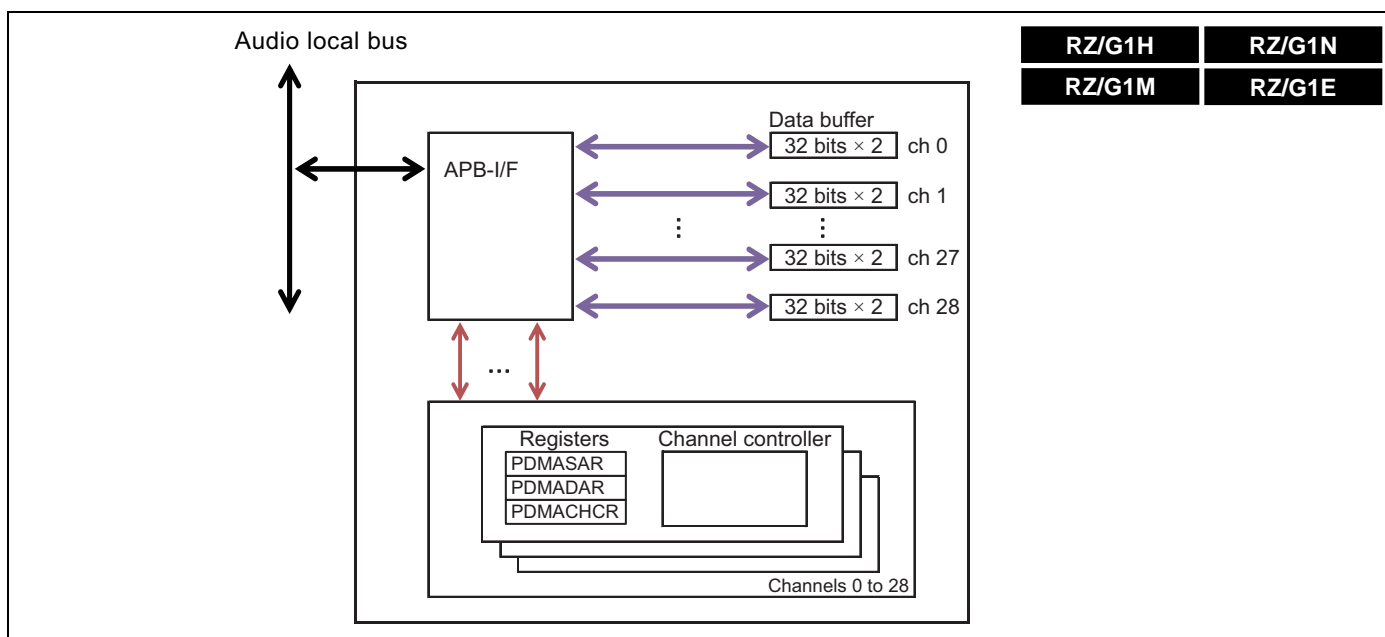


Figure 36.1 Block Diagram

#### 36.1.3 Input/Output Pins

No external pins are provided.

### 36.1.4 Register Configuration

**Table 36.1 List of Registers**

Register Name	Abbreviation	Access Type	Initial Value	Address	Access Size	RZ/G Series Products			
						RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
PDMA source address register	PDMASAR	R/W	H'0000_0000	H'EC740020 + H'10 × [n]	32	√	√	√	√
PDMA destination address register	PDMADAR	R/W	H'0000_0000	H'EC740024 + H'10 × [n]	32	√	√	√	√
PDMA channel control register	PDMACHCR	R/W	H'0000_0000	H'EC74002C + H'10 × [n]	32	√	√	√	√

- Notes:
1. n indicates the DMAC channel number (n = 0 to 28).
  2. Access the listed registers from the CPU in longword (32-bit) units; byte or word access is prohibited.
  3. Do not write to any addresses other than listed above. Operations cannot be guaranteed if writing is attempted. Values read from addresses other than those listed above are undefined.

## 36.2 Register Description

### [Legend]

Initial value: Register value after a reset

—: Undefined value

R/W: Readable/writable. The written value can be read.

R/WC1: Readable/writable. Writing 1 initializes the bit, and writing 0 is ignored.

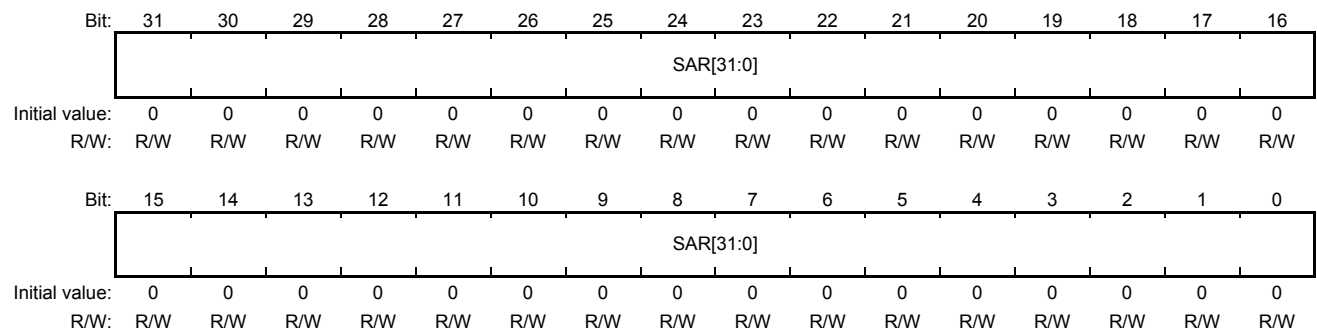
R: Read-only. The write value should always be 0.

—/W: Write-only. The read value is undefined.

### 36.2.1 PDMA Source Address Register (PDMASAR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

**Function:** Sets the DMA transfer source address.

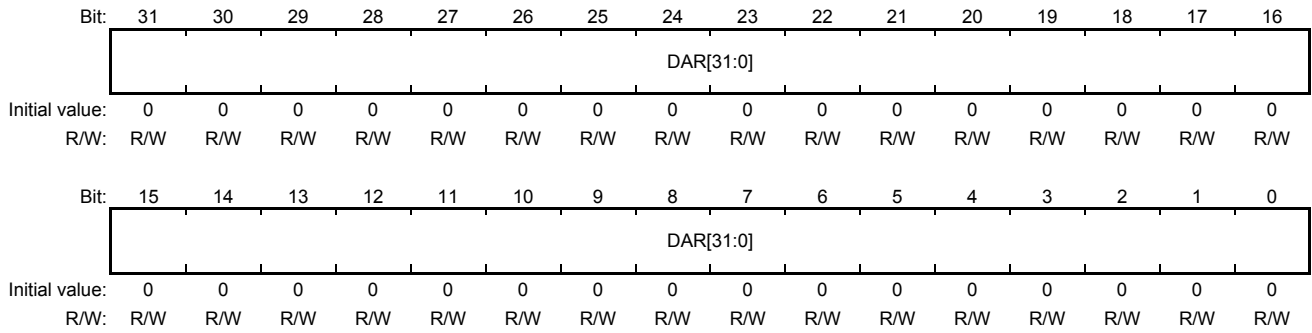


Bit	Bit Name	Initial Value	R/W	Description
31 to 0	SAR	All 0	R/W	Sets the DMA transfer source address.

**36.2.2 PDMA Destination Address Register (PDMADAR)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Function: Sets the DMA transfer destination address.

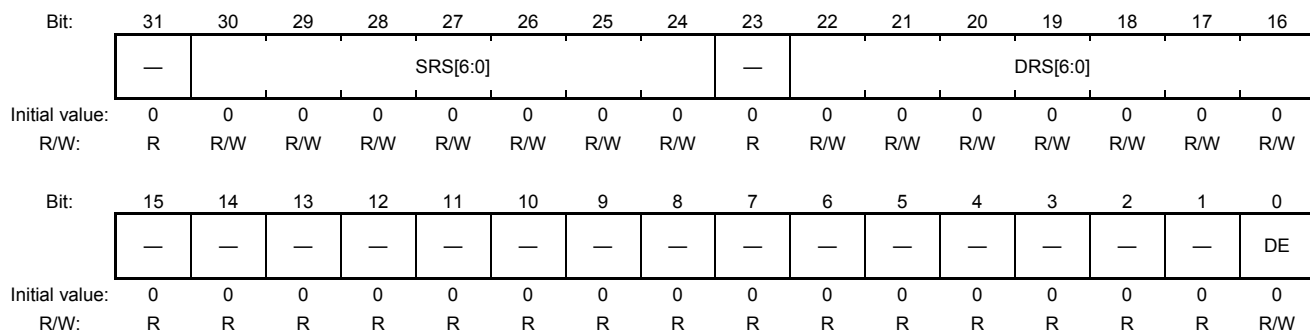


Bit	Bit Name	Initial Value	R/W	Description
31 to 0	DAR	All 0	R/W	Sets the DMA transfer destination address.

### 36.2.3 PDMA Channel Control Register (PDMACHCR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

**Function:** Selects the request sources of DMA transfer source and destination, and also starts or stops DMA.



Bit	Bit Name	Initial Value	R/W	Description
-----	----------	---------------	-----	-------------

31 — 0 R Reserved  
This bit is always read as 0. The write value should always be 0.

30 to 24 SRS H'00 R/W Transfer Source Request Source Select  
(setting H'00 to H'38 and the values with — are prohibited)

Set Value (H'xx)	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15
Transfer Source Request Source	SS100	SS101	SS102	SS103	SS110	SS111	SS112	SS113	SS120	SS121	SS122	SS123	SS13	SS14	SS15	SS16	SS17	SS18	SS190	SS191	SS192	SS193
Transfer Source Request Source	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Transfer Source Request Source	—	—	—	—	—	—	—	—	2D	2E	2F	30	31	32	33	34	35	36	37	38	—	—
Transfer Source Request Source	—	—	—	—	—	—	—	—	SCU_SRC00*	SCU_SRC01	SCU_SRC02	SCU_SRC03	SCU_SRC04	SCU_SRC05	SCU_SRC06	SCU_SRC07*	SCU_SRC08*	SCU_SRC09*	SCU_CMD0	SCU_CMD1	—	—

Note: \* Setting prohibited in the RZ/G1E (setting the value has no effect)

23 — 0 R Reserved  
This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description																																																																																																																																										
22 to 16	DRS	H'00	R/W	Transfer Destination Request Source Select (setting H'00 to H'36 and the values with — are prohibited)																																																																																																																																										
<table border="1"> <tr> <td>Set Value (H'xx)</td> <td>00</td><td>01</td><td>02</td><td>03</td><td>04</td><td>05</td><td>06</td><td>07</td><td>08</td><td>09</td><td>0A</td><td>0B</td><td>0C</td><td>0D</td><td>0E</td><td>0F</td><td>10</td><td>11</td><td>12</td><td>13</td><td>14</td><td>15</td> </tr> <tr> <td>Transfer Destination Request Source</td> <td>SSI00</td><td>SSI01</td><td>SSI02</td><td>SSI03</td><td>SSI10</td><td>SSI11</td><td>SSI12</td><td>SSI13</td><td>SSI20</td><td>SSI21</td><td>SSI22</td><td>SSI23</td><td>SSI3</td><td>SSI4</td><td>SSI5</td><td>SSI6</td><td>SSI7</td><td>SSI8</td><td>SSI90</td><td>SSI91</td><td>SSI92</td><td>SSI93</td> </tr> <tr> <td>Set Value (H'xx)</td> <td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td> </tr> <tr> <td>Transfer Destination Request Source</td> <td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td> </tr> <tr> <td>Set Value (H'xx)</td> <td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>2D</td><td>2E</td><td>2F</td><td>30</td><td>31</td><td>32</td><td>33</td><td>34</td><td>35</td><td>36</td><td>—</td><td>—</td><td>—</td><td>—</td> </tr> <tr> <td>Transfer Destination Request Source</td> <td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>SCU_SRC10*</td><td>SCU_SRC11</td><td>SCU_SRC12</td><td>SCU_SRC13</td><td>SCU_SRC14</td><td>SCU_SRC15</td><td>SCU_SRC16</td><td>SCU_SRC17*</td><td>SCU_SRC18*</td><td>SCU_SRC19*</td><td>—</td><td>—</td><td>—</td><td>—</td> </tr> </table>					Set Value (H'xx)	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	Transfer Destination Request Source	SSI00	SSI01	SSI02	SSI03	SSI10	SSI11	SSI12	SSI13	SSI20	SSI21	SSI22	SSI23	SSI3	SSI4	SSI5	SSI6	SSI7	SSI8	SSI90	SSI91	SSI92	SSI93	Set Value (H'xx)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	Transfer Destination Request Source	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	Set Value (H'xx)	—	—	—	—	—	—	—	—	2D	2E	2F	30	31	32	33	34	35	36	—	—	—	—	Transfer Destination Request Source	—	—	—	—	—	—	—	—	SCU_SRC10*	SCU_SRC11	SCU_SRC12	SCU_SRC13	SCU_SRC14	SCU_SRC15	SCU_SRC16	SCU_SRC17*	SCU_SRC18*	SCU_SRC19*	—	—	—	—
Set Value (H'xx)	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15																																																																																																																								
Transfer Destination Request Source	SSI00	SSI01	SSI02	SSI03	SSI10	SSI11	SSI12	SSI13	SSI20	SSI21	SSI22	SSI23	SSI3	SSI4	SSI5	SSI6	SSI7	SSI8	SSI90	SSI91	SSI92	SSI93																																																																																																																								
Set Value (H'xx)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—																																																																																																																								
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Set Value (H'xx)	—	—	—	—	—	—	—	—	2D	2E	2F	30	31	32	33	34	35	36	—	—	—	—																																																																																																																								
Transfer Destination Request Source	—	—	—	—	—	—	—	—	SCU_SRC10*	SCU_SRC11	SCU_SRC12	SCU_SRC13	SCU_SRC14	SCU_SRC15	SCU_SRC16	SCU_SRC17*	SCU_SRC18*	SCU_SRC19*	—	—	—	—																																																																																																																								
Note: * RZ/G1E is prohibition. (A setup is invalid.)																																																																																																																																														
15 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.																																																																																																																																										
0	DE	0	R/W	DMA Enable To enable DMA transfer function, set this bit to 1. Clearing this bit to 0 stops transfer. Note: Even if 0 is written to this bit while it is 1, 1 is read out until the transfer is completed.																																																																																																																																										

## 36.3 Operation

RZ/G1H	RZ/G1N
RZ/G1M	RZ/G1E

### 36.3.1 PDMASAR and PDMADAR Register Settings

Table 36.2 PDMASAR and PDMADAR Register Settings

Request Source	PDMASAR or PDMADAR	RZ/G Series Products			
		RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
SSI00	H'EC40_ 0000	√	√	√	√
SSI01	0400	√	√	√	√
SSI02	0800	√	√	√	√
SSI03	0C00	√	√	√	√
SSI10	1000	√	√	√	√
SSI11	1400	√	√	√	√
SSI12	1800	√	√	√	√
SSI13	1C00	√	√	√	√
SSI20	2000	√	√	√	√
SSI21	2400	√	√	√	√
SSI22	2800	√	√	√	√
SSI23	2C00	√	√	√	√
SSI3	3000	√	√	√	√
SSI4	4000	√	√	√	√
SSI5	5000	√	√	√	√
SSI6	6000	√	√	√	√
SSI7	7000	√	√	√	√
SSI8	8000	√	√	√	√
SSI90	9000	√	√	√	√
SSI91	9400	√	√	√	√
SSI92	9800	√	√	√	√
SSI93	9C00	√	√	√	√

Request Source	PDMASAR or PDMADAR	RZ/G Series Products			
		RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
SCU_SRCI0 **	H'EC30_ 0000	√	√	√	—
SCU_SRCI1 **	0400	√	√	√	√
SCU_SRCI2 **	0800	√	√	√	√
SCU_SRCI3 **	0C00	√	√	√	√
SCU_SRCI4 **	1000	√	√	√	√
SCU_SRCI5 **	1400	√	√	√	√
SCU_SRCI6 **	1800	√	√	√	√
SCU_SRCI7 **	1C00	√	√	√	—
SCU_SRCI8 **	2000	√	√	√	—
SCU_SRCI9 **	2400	√	√	√	—
SCU_SRCO0 *	4000	√	√	√	—
SCU_SRCO1 *	4400	√	√	√	√
SCU_SRCO2 *	4800	√	√	√	√
SCU_SRCO3 *	4C00	√	√	√	√
SCU_SRCO4 *	5000	√	√	√	√
SCU_SRCO5 *	5400	√	√	√	√
SCU_SRCO6 *	5800	√	√	√	√
SCU_SRCO7 *	5C00	√	√	√	—
SCU_SRCO8 *	6000	√	√	√	—
SCU_SRCO9 *	6400	√	√	√	—
SCU_CMD0 *	8000	√	√	√	√
SCU_CMD1 *	8400	√	√	√	√

Notes: \* Only PDMASAR is used.

\*\* Only PDMADAR is used.



### 36.3.2 Setting Flow

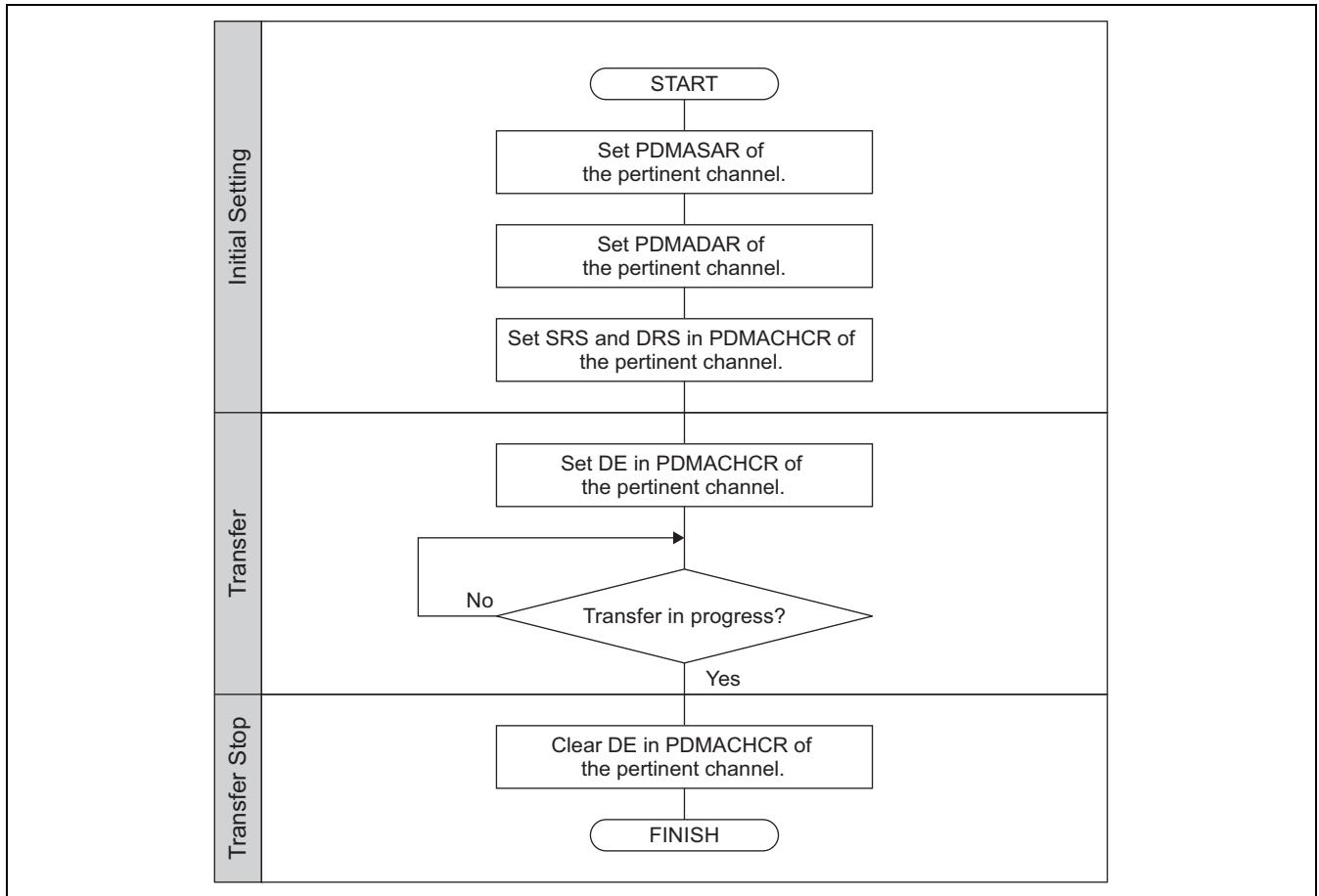


Figure 36.2 Setting Flow

# 37. Ethernet MAC Controller (Ether)

RZ/G1H	RZ/G1N
RZ/G1M	RZ/G1E

## 37.1 Overview

The Ether is a control unit which incorporates a function core conforming to the IEEE802.3u MAC (media access control) layer standard.

### 37.1.1 Features

- IEEE802.3u MAC (Ether) function
- Transmits and receives data frames
- Supports transfer at 10 and 100 Mbps
- Conforms to IEEE802.3u
- Reduced media independent interface (RMII)
- Magic packet detection
- Flow control conforming to IEEE802.3x or back pressure system
- On-chip DMA controller

Figure 37.1 shows a block diagram of the Ether. Table 37.1 lists the functions of each block.

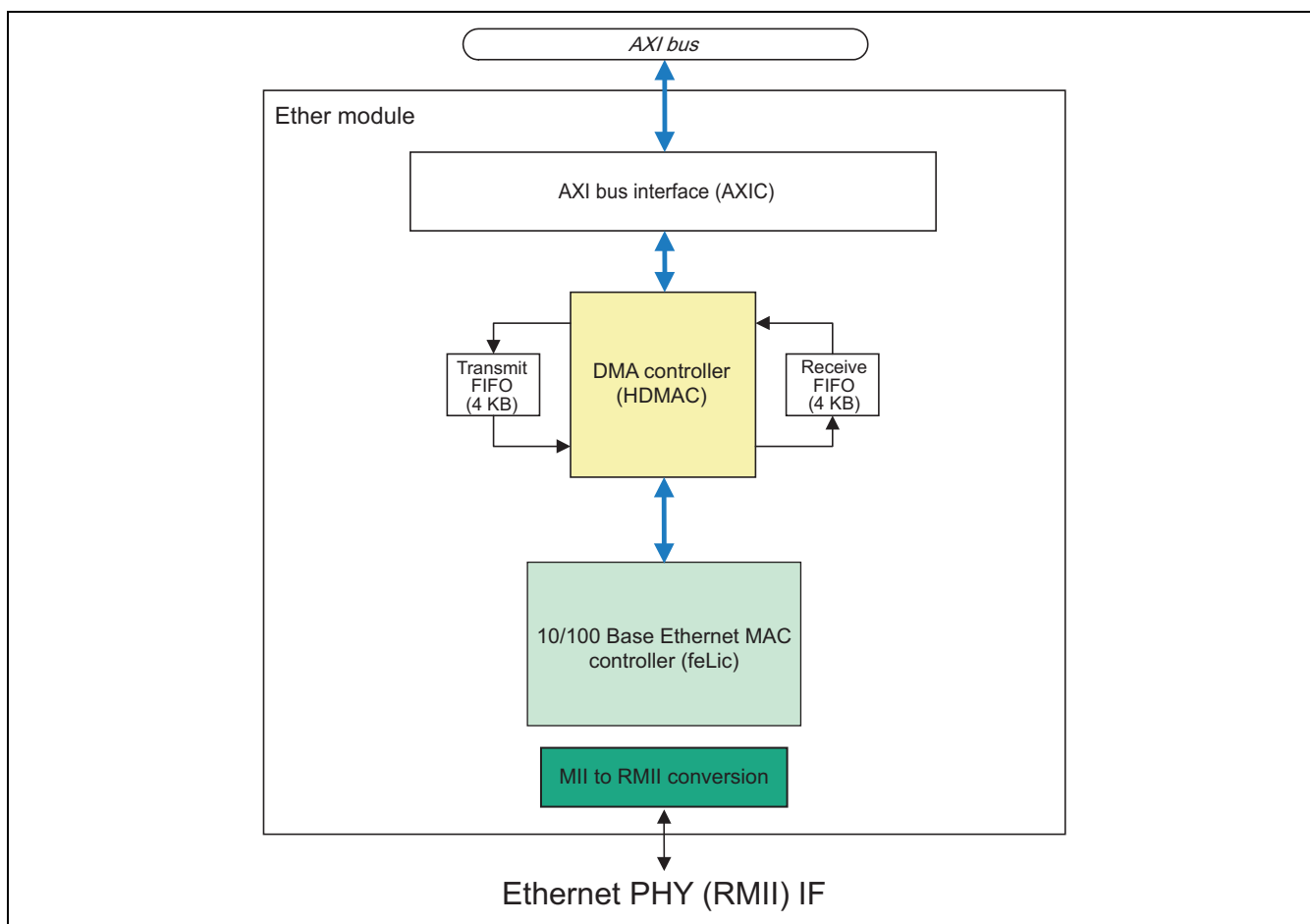


Figure 37.1 Block Diagram of Ether

**Table 37.1 Functions of Each Block**

<b>Block</b>	<b>Function</b>
AXI bus interface (AXIC)	<ul style="list-style-type: none"> <li>• Controls AXI bus interface.</li> </ul>
DMA controller (HDMAC)	<ul style="list-style-type: none"> <li>• DMA transfer of data transmitted from and received in the 10/100 Base Ethernet MAC controller between the transmit/receive buffer on memory and internal FIFOs For details, see section 37.8, HDMAC Function Specifications.</li> </ul>
10/100 Base Ethernet MAC controller (feLic)	<ul style="list-style-type: none"> <li>• Conforms to the IEEE802.3u MAC layer standard.</li> <li>• Transmits and receives data frames.</li> <li>• Supports transfer at 10/100 Mbps.</li> <li>• Magic packet detection</li> <li>• Flow control conforming to IEEE802.3x or back pressure system For details, see section 37.9, feLic Function Specifications.</li> </ul>
MII to RMI conversion	<ul style="list-style-type: none"> <li>• MII to RMI interface conversion</li> </ul>
Transmit/receive FIFO (TFIFO/RFIFO)	<ul style="list-style-type: none"> <li>• Transmit/receive FIFO for DMA controller Transmit FIFO depth: 4 Kbytes Receive FIFO depth: 4 Kbytes</li> </ul>

## 37.2 Input/Output Pins

Table 37.2 lists the external pin functions.

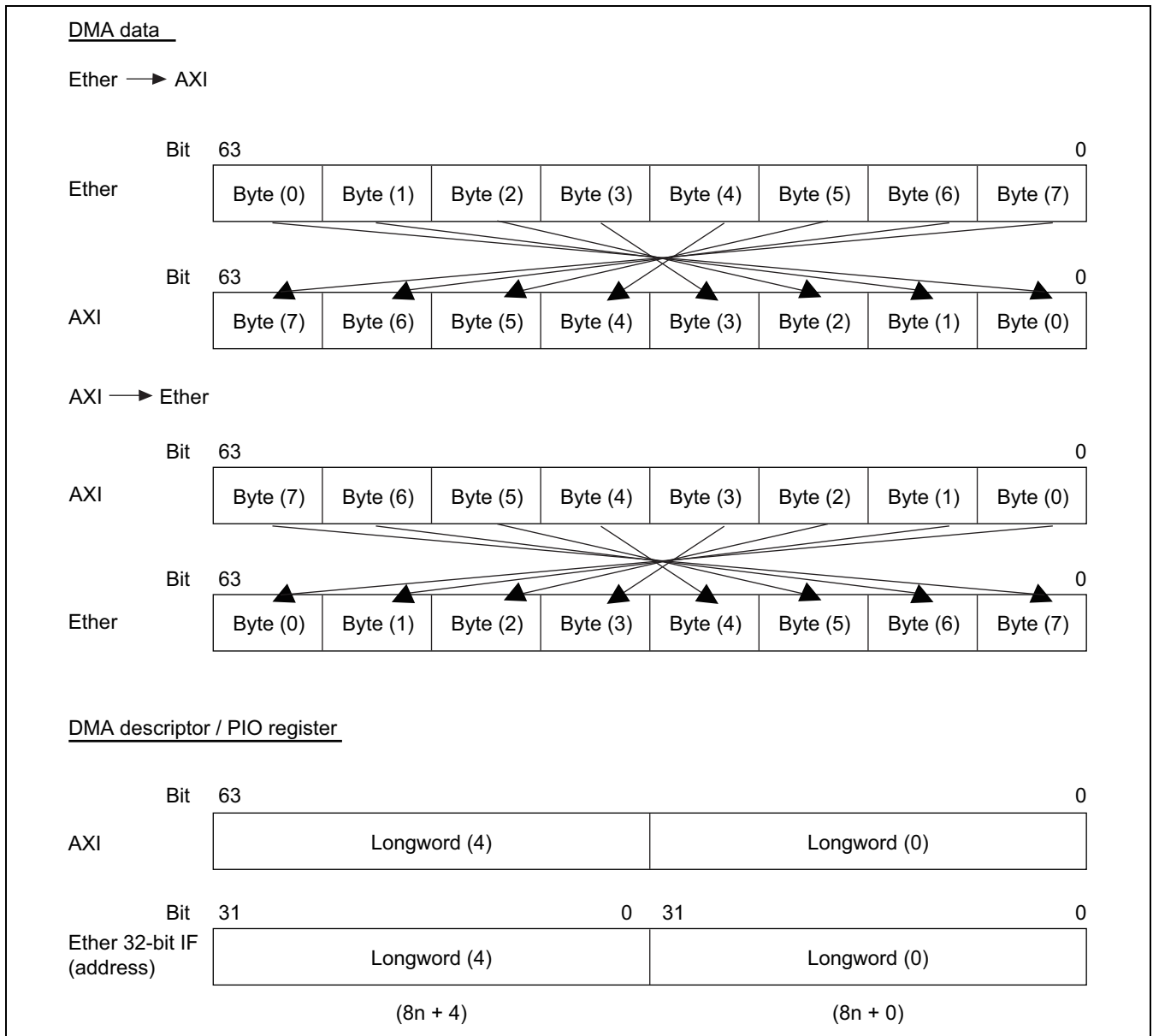
**Table 37.2 External Pin Function**

Pin Name	I/O	Function	RZ/G Series Products			
			RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
ETH_REF_CLK	Input	Reference input clock	√	√	√	√
ETH_TXD0	Output	Transmit data	√	√	√	√
ETH_TXD1						
ETH_TX_EN	Output	Transmit data enable	√	√	√	√
ETH_CRSDV	Input	Carrier sense	√	√	√	√
ETH_RX_ER	Input	Receive error	√	√	√	√
ETH_RXD0	Input	Receive data	√	√	√	√
ETH_RXD1						
ETH_MDC	Output	Management data clock	√	√	√	√
ETH_MDIO	I/O	Management data	√	√	√	√
ETH_LINK	Input	PHY output LINK signal	√	√	√	√
ETH_MAGIC	Output	Magic packet detection	√	√	√	√

### 37.3 Endian

<b>RZ/G1H</b>	<b>RZ/G1N</b>
<b>RZ/G1M</b>	<b>RZ/G1E</b>

The Ether has a 32-bit interface. Figure 37.2 shows data arrangement. The Ether allows endian conversion for DMA data through the setting of the CXR0 register of the HDMAC.



**Figure 37.2 Data Arrangement**

## 37.4 Register Descriptions

### (1) Notes on Register Access

To access the registers, the following restrictions and notes should be obeyed.

1. For the register bits not defined implicitly in this specifications document, the write value should always be 0, and the read value should always be handled as undefined.
2. Even when there are no restrictions on writing to each register, the undefined bits should be written to as described in the above restriction.
3. Each register is a 32-bit long and should be accessed in 32-bit units. Accordingly, any register cannot be partially read from or written to.

### (2) Register Configuration

Table 37.3 shows the configuration of HDMAC registers. Table 37.4 shows the configuration of feLic registers.

**Table 37.3 HDMAC Register Configuration**

Name	Abbreviation	R/W	Address	Access Size	Initial Value	RZ/G Series Products			
						RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
HDMAC operating mode setting register	CXR0	R/W*	H'EE70 0200	32	H'0000 0000	√	√	√	√
Transmit activation register	CXR1	R/W*	H'EE70 0208	32	H'0000 0000	√	√	√	√
Receive activation register	CXR2	R/W	H'EE70 0210	32	H'0000 0000	√	√	√	√
Transmit descriptor start address setting register	CXR3	R/W*	H'EE70 0218	32	H'0000 0000	√	√	√	√
Receive descriptor start address setting register	CXR4	R/W*	H'EE70 0220	32	H'0000 0000	√	√	√	√
Status register	CXR5	R/W	H'EE70 0228	32	H'0000 0000	√	√	√	√
Interrupt mask setting register	CXR6	R/W	H'EE70 0230	32	H'0000 0000	√	√	√	√
Error mask setting register	CXR7	R/W	H'EE70 0238	32	H'0000 0000	√	√	√	√
Discarded frame counter register	CXR8	R/W	H'EE70 0240	32	H'0000 0000	√	√	√	√
Transmit FIFO threshold setting register	CXR9	R/W*	H'EE70 0248	32	H'0000 0000	√	√	√	√
External FIFO depth setting register	CXR10	R/W*	H'EE70 0250	32	H'0000 0000	√	√	√	√
Receive activation reset method setting register	CXR11	R/W*	H'EE70 0258	32	H'0000 0000	√	√	√	√
Transmit FIFO underflow counter register	CXR13	R/W	H'EE70 0264	32	H'0000 0000	√	√	√	√
Receive FIFO overflow counter register	CXR14	R/W	H'EE70 0268	32	H'0000 0000	√	√	√	√
RMII mode register	CXR15	R/W	H'EE70 026C	32	H'0000 0000	√	√	√	√
Receive FIFO busy transmit threshold setting register	CXR16	R/W	H'EE70 0270	32	H'0007 0007	√	√	√	√
Transmit interrupt mode setting register	CXR18	R/W	H'EE70 027C	32	H'0000 0000	√	√	√	√

Note: \* There are restrictions on write access.

**Table 37.4 feLic Register Configuration**

						<u>RZ/G Series Products</u>			
Name	Abbreviation	R/W	Address	Access Size	Initial Value	RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
feLic operating mode setting register	CXR20	R/W*	H'EE70 0300	32	H'0000 0000	√	√	√	√
Long frame length check value setting register	CXR2A	R/W*	H'EE70 0308	32	H'0000 0000	√	√	√	√
Status register	CXR21	R/W	H'EE70 0310	32	H'0000 0000	√	√	√	√
interrupt mask setting register	CXR22	R/W	H'EE70 0318	32	H'0000 0000	√	√	√	√
MII control register	CXR23	R/W	H'EE70 0320	32	H'0000 000x	√	√	√	√
PHY status register	CXR2B	R	H'EE70 0328	32	H'0000 000x	√	√	√	√
Random number generating counter upper limit setting register	CXR30	R/W	H'EE70 0340	32	H'0000 0000	√	√	√	√
IPG counter setting register	CXR70	R/W*	H'EE70 0350	32	H'0000 0014	√	√	√	√
Automatic PAUSE parameter setting register	CXR71	R/W	H'EE70 0354	32	H'0000 0000	√	√	√	√
Manual PAUSE parameter setting register	CXR72	W	H'EE70 0358	32	H'0000 0000	√	√	√	√
Receive PAUSE frame counter register	CXR80	R	H'EE70 0360	32	H'0000 0000	√	√	√	√
PAUSE frame retransmit count setting register	CXR81	R/W*	H'EE70 0364	32	H'0000 0000	√	√	√	√
PAUSE frame retransmit counter register	CXR82	R	H'EE70 0368	32	H'0000 0000	√	√	√	√
MAC address high register	CXR24	R/W*	H'EE70 03C0	32	H'0000 0000	√	√	√	√
MAC address low register	CXR25	R/W*	H'EE70 03C8	32	H'0000 0000	√	√	√	√
TINT1 count register	CXR40	R/W	H'EE70 03D0	32	H'0000 0000	√	√	√	√
TINT2 count register	CXR41	R/W	H'EE70 03D4	32	H'0000 0000	√	√	√	√
TINT3 count register	CXR42	R/W	H'EE70 03D8	32	H'0000 0000	√	√	√	√
TINT4 count register	CXR43	R/W	H'EE70 03DC	32	H'0000 0000	√	√	√	√
RINT1 count register	CXR50	R/W	H'EE70 03E4	32	H'0000 0000	√	√	√	√
RINT2 count register	CXR51	R/W	H'EE70 03E8	32	H'0000 0000	√	√	√	√
RINT3 count register	CXR52	R/W	H'EE70 03EC	32	H'0000 0000	√	√	√	√
RINT4 count register	CXR53	R/W	H'EE70 03F0	32	H'0000 0000	√	√	√	√
RINT5 count register	CXR54	R/W	H'EE70 03F4	32	H'0000 0000	√	√	√	√
RINT8 count register	CXR55	R/W	H'EE70 03F8	32	H'0000 0000	√	√	√	√

Note: \* There are restrictions on write access.



### 37.4.1 HDMAC Operating Mode Setting Register (CXR0)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CXR0 is used for specifying the operating mode of the HDMAC.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	DE	DL1	DL0	—	—	—	SWR
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value*	R/W	Description
31 to 7	—	All 0	R	Reserved
6	DE	0	R/W	DMA Data Endian Conversion 0: Does not perform endian conversion for DMA data. 1: Performs endian conversion for DMA data. Endian conversion for descriptors and registers is not performed. Note: Be sure to set this bit to 1 before operating the Ethernet MAC controller (Ether).
5, 4	DL1 and DL0	00	R/W	Transmit/Receive Descriptor Length Setting    Descriptor length 00:        16 bytes 01:        32 bytes 10:        64 bytes 11:        Reserved
3 to 1	—	All 0	R	Reserved
0	SWR	0	R/W	HDMAC/feLic Software Reset Writing 1 resets the HDMAC/feLic module except for CXR3, CXR4, CXR8, CXR13 and CXR14. Note: Registers should not be accessed until 64 clock cycles have elapsed after the SWR bit is set to 1. When writing to registers (except for the SWR bit), the transmitting and receiving function should be disabled.

Note: \* This register is initialized by an HDMAC/feLic software reset.

### 37.4.2 Transmit Activation Register (CXR1)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CXR1 initiates transmission by the HDMAC.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TRNS
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value*	R/W	Description
31 to 1	—	All 0	R	Reserved
0	TRNS	0	R/W	Transmit Activation If 1 is written to this bit, the HDMAC accesses the transmit descriptor ring and transmits frames for all the valid descriptors. This bit is automatically cleared when transmission of all the valid frames has been completed, or the transmit descriptor depletion occurs. Note: Writing 0 is disabled.

Note: \* This register is initialized by an HDMAC/feLic software reset.

**37.4.3 Receive Activation Register (CXR2)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CXR2 initiates reception by the HDMAC.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	R
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value*	R/W	Description
31 to 1	—	All 0	R	Reserved
0	R	0	R/W	<p>Receive Ready</p> <p>If 1 is written to this bit, the HDMAC accesses the receive descriptor ring and enters the receive wait state. For operation of this bit after completion of reception, which depends on the CXR11 settings, see section 37.4.12, Receive Activation Reset Method Setting Register (CXR11).</p> <p>If 0 is written to this bit, the HDMAC completes reception of the frame being processed, and then disables the receiving function.</p> <p>This bit is reset to 0 when the RACT bit of the fetched descriptor is 0 (when the receive descriptor depletion occurs).</p>

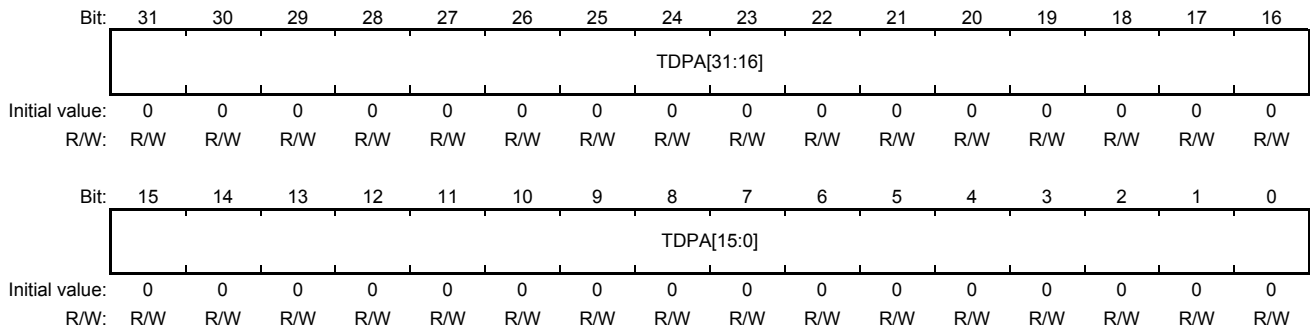
Note: \* This register is initialized by an HDMAC/feLic software reset.

### 37.4.4 Transmit Descriptor Start Address Setting Register (CXR3)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CXR3 specifies the start address of the transmit descriptor ring. The start address of the descriptor ring should be aligned to the boundary consistent with the descriptor length specified by the DL bits in CXR0.

Writing to CXR3 should be performed before transmission is started. Writing to CXR3 after transmission has been started is prohibited and operation according to the written value cannot be guaranteed.



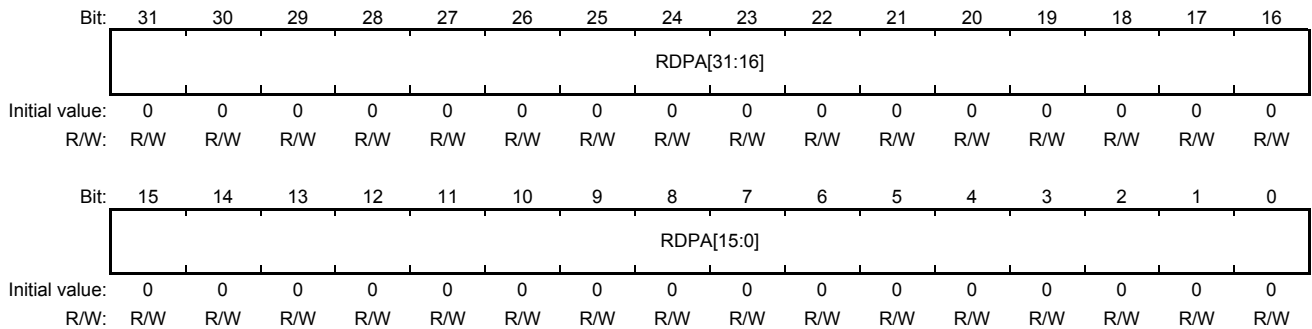
Bit	Bit Name	Initial Value	R/W	Description
31 to 0	TDPA [31:0]	All 0	R/W	Transmit Descriptor Start Address Bits 3 to 0 should be set to 0 for alignment of the descriptor. Note: A value other than 0 must not be set to bits 3 to 0. Writing is prohibited after transmission has been started.

### 37.4.5 Receive Descriptor Start Address Setting Register (CXR4)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CXR4 specifies the start address of the receive descriptor ring. The start address of the descriptor ring should be aligned to the boundary consistent with the descriptor length specified by the DL bits in CXR0.

Writing to CXR4 should be performed before reception is started. Writing to CXR4 after reception has been started is prohibited and operation according to the written value cannot be guaranteed.



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	RDPA [31:0]	All 0	R/W	Transmit Descriptor Start Address Bits 3 to 0 should be set to 0 for alignment of the descriptor. Note: A value other than 0 must not be set to bits 3 to 0. Writing is prohibited after transmission has been started.

### 37.4.6 Status Register (CX5)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CX5 is a register that indicates HDMAC interrupt sources.

The status sources are output to the INTC module by a signal of each source.

Each bit is cleared by writing 1 to the corresponding bit. The MINT bit is set to 0 by clearing CX21. Generation of interrupts can be masked by the corresponding bits in CX6.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	TWB	BINT	AIN	LKON	TABT	RABT	RFRMER	BER	MINT	FTC	TDE	TFE	FRC	RDE	RFE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TINT8	TINT7	TINT6	TINT5	TINT4	TINT3	TINT2	TINT1	RINT8	RINT7	RINT6	RINT5	RINT4	RINT3	RINT2	RINT1
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1

Bit	Bit Name	Initial Value*2	R/W	Description
31	—	0	R	Reserved
30	TWB	0	R/W*1	Indicates that write-back to the transmit descriptor whose TWBI bit is set has been performed. The interrupt can be generated every frame by so setting CX18. <Interrupt source>
29	BINT	0	R/W*1	Not used.
28	AIN	0	R/W*1	Not used.
27	LKON	0	R/W*1	Not used.
26	TABT	0	R/W*1	Transmit Abort Detect <Interrupt source>
25	RABT	0	R/W*1	Receive Abort Detect <Interrupt source>
24	RFRMER	0	R/W*1	Receive Frame Count Overflow Occurrence <Interrupt source>
23	BER	0	R/W*1	Indicates that a DMA error is input.
22	MINT	0	R	M Port Interrupt Occurrence <Interrupt source> Indicates that an interrupt signal from the feLic is asserted.
21	FTC	0	R/W*1	Frame Transmit Completion <Interrupt source> Indicates that transmission of all the frames specified by the transmit descriptor has been completed. This bit is not set for each frame.
20	TDE	0	R/W*1	Not used.
19	TFE	0	R/W*1	Transmit FIFO Underflow Error Occurrence <Interrupt source> Indicates that the transmit FIFO becomes empty during frame transmission.

Bit	Bit Name	Initial Value*2	R/W	Description
18	FRC	0	R/W*1	Frame Receive Completion <Interrupt source> Indicates that the receive descriptor is updated by frame reception. This bit is set when reception of one frame has been completed regardless of the setting of the RR bit in CXR11.
17	RDE	0	R/W*1	Receive Descriptor Depletion <Interrupt source> Indicates that the fetched receive descriptor is invalid. Occurrence of this source resets the R bit in CXR2 to 0.
16	RFE	0	R/W*1	Receive FIFO Overflow Error Occurrence <Interrupt source>
15 to 8	TINT8 to TINT1	All 0	R/W*1	Transmit Port Interrupt
7 to 0	RINT8 to RINT1	All 0	R/W*1	Receive Port Interrupt

- Notes: 1. These bits are cleared by writing 1 to the corresponding bits. Writing 0 has no meaning.  
2. This register is initialized by an HDMAC/feLic software reset.

### 37.4.7 Interrupt Mask Setting Register (CXR6)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CXR6 is a register that masks the interrupts indicated by CXR5.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	TWB	BINT	AINT	LKON	TABT	RABT	RFRMER	BER	MINT	FTC	TDE	TFE	FRC	RDE	RFE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TINT8	TINT7	TINT6	TINT5	TINT4	TINT3	TINT2	TINT1	RINT8	RINT7	RINT6	RINT5	RINT4	RINT3	RINT2	RINT1
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value*	R/W	Description
31	—	0	R	Reserved
30	TWB	0	R/W	Interrupt Enable
29	BINT	0	R/W	0: Disables an interrupt indicated by the corresponding bit in CXR5.
28	AINT	0	R/W	1: Enables an interrupt indicated by the corresponding bit in CXR5.
27	LKON	0	R/W	Note: Bits 29 to 27 should always be set to 0.
26	TABT	0	R/W	
25	RABT	0	R/W	
24	RFRMER	0	R/W	
23	BER	0	R/W	
22	MINT	0	R/W	
21	FTC	0	R/W	
20	TDE	0	R/W	
19	TFE	0	R/W	
18	FRC	0	R/W	
17	RDE	0	R/W	
16	RFE	0	R/W	
15 to 8	TINT8 to TINT1	All 0	R/W	
7 to 0	RINT8 to RINT0	All 0	R/W	

Note: \* This register is initialized by an HDMAC/feLic software reset.



### 37.4.8 Error Mask Setting Register (CX7)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CX7 is a register that specifies whether or not to allow the status of the descriptor information (indicated by the RFS7 bit in RD0) to be reflected in the RFE bit in the receive descriptor 0 (RD0) as a summary.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	RINT8	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R	R	R	R	R	R	R

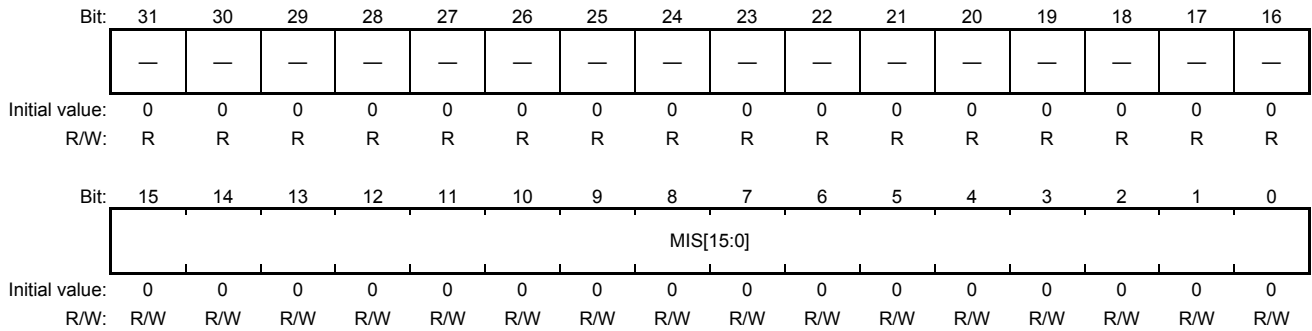
Bit	Bit Name	Initial Value*	R/W	Description
31 to 8	—	All 0	R	Reserved
7	RINT8	All 0	R/W	Receive Descriptor Error Flag (RFE) Mask 0: Allows RINT8 (RFS7 bit in RD0) to be reflected in RFE. 1: Does not allow RINT8 (RFS7 bit in RD0) to be reflected in RFE.
6 to 0	—	All 0	R	Reserved

Note: \* This register is initialized by an HDMAC/feLic software reset.

**37.4.9 Discarded Frame Counter Register (CXR8)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CXR8 is a register that indicates the number of discarded frames.

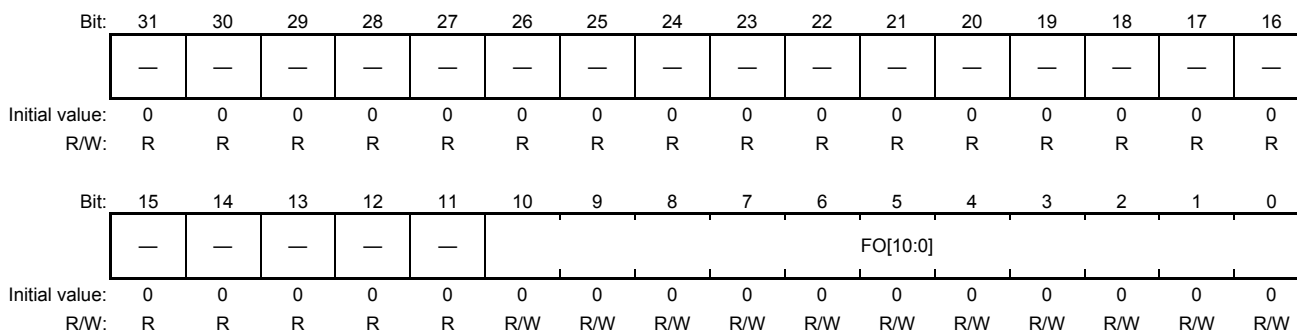


Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved
15 to 0	MIS[15:0]	H'0000	R/W	Discarded Frame Counter These bits indicate the number of frames which are discarded because the receive descriptor is disabled, for example. The counter stops counting when all bits are set to 1 (H'FFFF). Note: Writing any data clears these bits.

**37.4.10 Transmit FIFO Threshold Setting Register (CXR9)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CXR9 is a register that specifies the threshold for the transmit FIFO.



Bit	Bit Name	Initial Value*	R/W	Description
31 to 11	—	All 0	R	Reserved
10 to 0	FO[10:0]	H'000	R/W	Transmit FIFO Threshold Setting            Threshold H'000:            Store and forward H'001:            4 bytes H'002:            8 bytes :                    : H'0FE:            1016 bytes H'0FF:            1020 bytes H'100:            1024 bytes :                    : H'1FE:            1040 bytes H'1FF:            2044 bytes H'200:            2048 bytes :                    : H'3FE:            4088 bytes 3 H'FF:            4092 bytes H'400 to H'7FF    Setting prohibited

Reading (transmission) is started when one frame data has been written to the FIFO or when data in the FIFO exceeds the above setting.

Using on the initial value (store and forward) is recommended to prevent from occurring underflow error on sending.

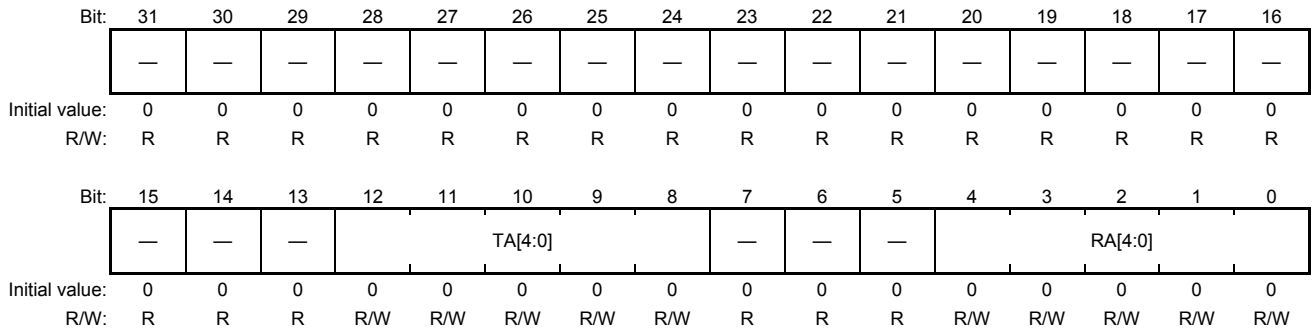
Note: Writing is disabled when the TRNS bit in CXR1 = 1.

Note: \* This register is initialized by an HDMAC/feLic software reset.

**37.4.11 External FIFO Depth Setting Register (CXR10)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CXR10 is a register that specifies the depth of the transmit and receive FIFOs.



Bit	Bit Name	Initial Value*	R/W	Description
31 to 13	—	All 0	R	Reserved
12 to 8	TA[4:0]	H'00	R/W	Transmit FIFO Depth Setting      Depth H'00:          256 bytes H'01:          512 bytes H'02:          768 bytes H'03:          1024 bytes :                : H'07:          2048 bytes :                : H'0F:          4096 bytes H'10 to H'1F: Setting prohibited Note: Writing to bits 12 to 8 is disabled when the TRNS bit in CXR1 = 1.
7 to 5	—	All 0	R	Reserved
4 to 0	RA[4:0]	H'00	R/W	Receive FIFO Depth Setting      Depth H'00:          256 bytes H'01:          512 bytes H'02:          768 bytes H'03:          1024 bytes :                : H'07:          2048 bytes :                : H'0F:          4096 bytes H'10 to H'1F: Setting prohibited Note: Writing to bits 4 to 0 is disabled when the R bit in CXR2 = 1.

Note: \* This register is initialized by an HDMAC/feLic software reset.

**37.4.12 Receive Activation Reset Method Setting Register (CXR11)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CXR11 is a register that specifies a method for resetting the receive ready bit (R bit in CXR2).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RNR	RR
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

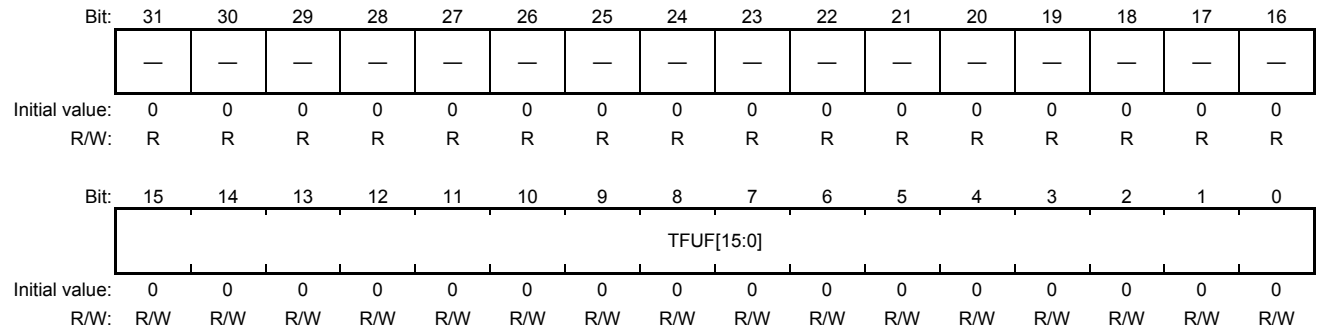
Bit	Bit Name	Initial Value*	R/W	Description
31 to 2	—	All 0	R	Reserved
1	RNR	0	R/W	Not used. This bit should always be set to 0.
0	RR	0	R/W	Receive Ready Reset 0: (initial value) Automatically clears the receive ready bit (R bit in CXR2) by hardware. The receive ready bit (R bit in CXR2) is automatically cleared by receiving one frame, thus disabling reception of the following frames. In this mode, interrupt control for each frame is possible. 1: Normal operating mode Resets the receive ready bit (R bit in CXR2) by software. After 1 is written to the receive ready bit (R bit in CXR2), the HDMAC automatically fetches the receive descriptor and receives frames until 0 is written to the receive ready bit (R bit in CXR2). Continuous reception of multiple frames is possible. Note that the receive ready bit (R bit in CXR2) is reset to 0 when the RACT bit in the fetched descriptor is 0. Note: Writing to this bit is disabled when the R bit in CXR2 = 1.

Note: \* This register is initialized by an HDMAC/feLic software reset.

### 37.4.13 Transmit FIFO Underflow Counter Register (CXR13)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CXR13 is a register that indicates the number of times the transmit FIFO underflow occurs.

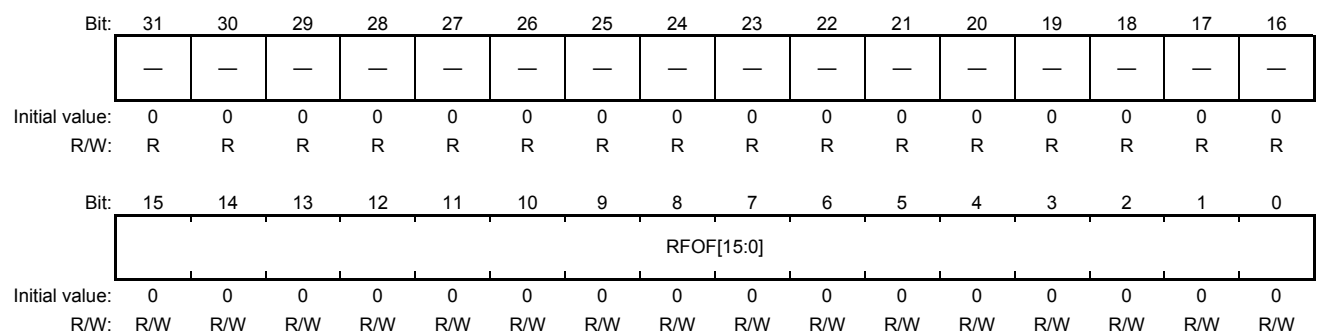


Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved
15 to 0	TFUF[15:0]	H'0000	R/W	Transmit FIFO Underflow Counter The counter stops counting when all bits are set to 1 (H'FFFF). Note: Writing any data clears these bits.

### 37.4.14 Receive FIFO Overflow Counter Register (CXR14)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CXR14 is a register that indicates the number of times the receive FIFO overflow occurs.



Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved
15 to 0	RFOF[15:0]	H'0000	R/W	Receive FIFO Overflow Counter The counter stops counting when all bits are set to 1 (H'FFFF). Note: Writing any data clears these bits.

**37.4.15 RMI Mode Register (CXR15)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CXR15 sets the RMI mode.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RMI
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value*	R/W	Description
31 to 1	—	All 0	R	Reserved
0	RMI	0	R/W	RMI Mode Specification 0: (initial value) 1: RMI mode Be sure to set this bit to 1 before operating the Ethernet MAC controller (Ether).

Note: \* This register is initialized by an HDMAC/feLic software reset.

**37.4.16 Receive FIFO Busy Transmit Threshold Setting Register (CXR16)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CXR16 is a register that specifies the threshold value for sending the receive FIFO busy to the feLic based on the number of frames and number of data bytes stored in the receive FIFO.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	RFF[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	RFD[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value*	R/W	Description
31 to 19	—	All 0	R	Reserved
18 to 16	RFF[2:0]	111	R/W	Busy Transmit Threshold based on the Number of Receive Frames Setting Threshold 000: Transmits the busy when two frames have been stored. 001: Transmits the busy when four frames have been stored. 010: Transmits the busy when six frames have been stored. : 110: Transmits the busy when 14 frames have been stored. 111: Transmits the busy when 16 frames have been stored.
15 to 3	—	All 0	R	Reserved
2 to 0	RFD[2:0]	111	R/W	Busy Transmit Threshold based on the Amount of Data in the Receive FIFO Setting Threshold 000: Transmits the busy when 224 (256 – 32) bytes have been stored. 001: Transmits the busy when 480 (512 – 32) bytes have been stored. 010: Transmits the busy when 736 (768 – 32) bytes have been stored. 011: Transmits the busy when 992 (1024 – 32) bytes have been stored. : 110: Transmits the busy when 1760 (1792 – 32) bytes have been stored. 111: See the following note. Note: The set value to these bits should be smaller than the set value to the RA bits in CXR10. If the former and latter values are equal, the busy will be sent out when (receive FIFO depth – 64 bytes) have been stored in the receive FIFO, not when (receive FIFO depth – 32 bytes) have been stored. For example, when the RA bits in CXR10 and RFD bits in CXR16 are both 7, the busy will be sent out when 1984 (= 2048 – 64) bytes have been stored in the receive FIFO.

Note: \* This register is initialized by an HDMAC/feLic software reset.



**37.4.17 Transmit Interrupt Mode Setting Register (CXR18)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CXR18 is used for setting transmit interrupt operating mode for the HDMAC.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	TIM	—	—	—	TIS
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value*	R/W	Description
31 to 5	—	All 0	R	Reserved
4	TIM	0	R/W	Transmit Interrupt Mode 0: Mode in which the interrupt is issued each time a frame has been transmitted. 1: Mode in which the interrupt is issued when write-back to the descriptor whose TWBI bit is set has been completed.
3 to 1	—	All 0	R	Reserved
0	TIS	0	R/W	Interrupt Mode Enable 0: TIM setting is disabled. 1: TIM setting is enabled.

Note: \* This register is initialized by an HDMAC/feLic software reset.

## 37.4.18 feLic Operating Mode Setting Register (CXR20)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CXR20 is a register that specifies the operating mode of the feLic. Some mode bits in this register should not be modified while the transmitting and receiving functions are enabled.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	TPC	ZPF	PFR	RXF	TXF
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	CER	—	—	MPM	—	—	RPE	TPE	—	ILB	OLB	DPM	PRM
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R	R	R/W	R	R	R/W	R/W	R	R/W*1	R/W*1	R/W*1	R/W*1

Bit	Bit Name	Initial Value*2	R/W	Description
31 to 21	—	All 0	R	Reserved
20	TPC	0	R/W	PAUSE Frame Transmission 0: Transmission of a PAUSE frame is enabled even during a PAUSE period. 1: Transmission of a PAUSE frame is disabled during PAUSE period.
19	ZPF	0	R/W	PAUSE Frame Enable with TIME = 0 0: Control of a PAUSE frame whose TIME parameter value is 0 is disabled. 1: Control of a PAUSE frame whose TIME parameter value is 0 is enabled.
18	PFR	0	R/W	PAUSE Frame Receive Mode 0: PAUSE frame is not transferred to the upper module. 1: PAUSE frame is transferred to the upper module.
17	RXF	0	R/W	Operating Mode for Reception Flow Control 0: Reception flow control is disabled. 1: Reception flow control is enabled.
16	TXF	0	R/W	Operating Mode for Transmission Flow Control 0: Transmission flow control is disabled. 1: Transmission flow control is enabled.
15 to 13	—	All 0	R	Reserved
12	CER	0	R/W	CRC Error Frame Receive Mode 0: Normal mode (an error frame is regarded as an error). 1: Mode in which the received frame with a CRC error is not regarded as an error.
11, 10	—	All 0	R	Reserved
9	MPM	0	R/W	Magic Packet Detection Enable 0: Magic packet detection is disabled. 1: Magic packet detection is enabled.
8, 7	—	All 0	R	Reserved

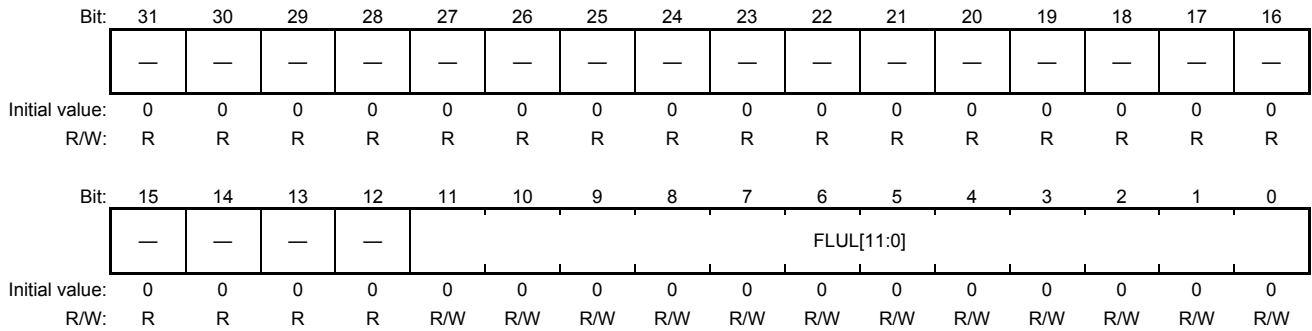
Bit	Bit Name	Initial Value*2	R/W	Description
6	RPE	0	R/W	<p>Reception Enable</p> <p>0: Receiving function is disabled after completion of current frame reception.</p> <p>1: Frame receiving function is enabled and receive data is transferred to the HDMAC.</p>
5	TPE	0	R/W	<p>Transmission Enable</p> <p>0: Transmitting function is disabled after completion of current frame transmission.</p> <p>1: A frame transmit request from the HDMAC is enabled.</p>
4	—	0	R	Reserved
3	ILB	0	R/W*1	<p>feLic Loopback Mode</p> <p>0: The feLic enters normal mode.</p> <p>1: The feLic enters loopback mode.</p>
2	OLB	0	R/W*1	<p>10-Base T or 100-Base TX Transfer Setting (Transfer at 10 or 100 Mbps)</p> <p>0: Transfer is 10-base T (i.e. at 10 Mbps).</p> <p>1: Transfer is 100-base TX (i.e. at 100 Mbps).</p>
1	DPM	0	R/W*1	<p>Duplex Mode</p> <p>0: The feLic enters half-duplex mode. Note that feLic loopback mode should not be specified during this mode.</p> <p>1: The feLic enters full-duplex mode.</p>
0	PRM	0	R/W*1	<p>Promiscuous Mode</p> <p>0: The feLic enters normal mode. (When the MPM bit is set, the feLic operates in normal mode regardless of the status of this bit.)</p> <p>1: The feLic enters promiscuous mode.</p>

Notes: 1. Bits 3 to 0 should not be modified while the transmitting and receiving functions are enabled.  
2. This register is initialized by an HDMAC/feLic software reset.

**37.4.19 Long Frame Length Check Value Setting Register (CXR2A)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CXR2A is a register that specifies the upper limit of the receive frame length used for checking the length.



Bit	Bit Name	Initial Value*	R/W	Description
31 to 12	—	All 0	R	Reserved
11 to 0	FLUL[11:0]	H'000	R/W	Frame Length Upper Limit The specified value is used as the frame length check value. When the received frame length value exceeds this value, it is regarded as RINT4 (frame length error). (See below.) Setting Check Value H'000 to H'5EE: 1518 bytes H'5EF: 1519 bytes : : H'7FF: 2047 bytes H'800 to H'FFF: 2048 bytes Note: The CXR20 register should not be modified while the receiving function is enabled.

Note: \* This register is initialized by an HDMAC/feLic software reset.

**37.4.20 Status Register (CXR21)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CXR21 is a register that indicates the feLic status.

The status sources are output to the INTC module by a signal of each source.

Each bit is cleared by writing 1 to the corresponding bit. Generation of interrupts can be masked by the corresponding bits in CXR22.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	BCR	PRO	—	LNK	MPR	FCD
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R/W*1	R/W*1	R	R/W*1	R/W*1	R/W*1

Bit	Bit Name	Initial Value*2	R/W	Description
31 to 6	—	All 0	R	Reserved
5	BCR	0	R/W*1	Reserved
4	PRO	0	R/W*1	PAUSE Frame Retransmit Retry Over <Interrupt Source> Indicates that the PAUSE frame retransmission count has reached the upper limit of retransmission set in the CXR81 register.
3	—	0	R	Reserved
2	LNK	0	R/W*1	LINK Signal Change Interrupt <Interrupt Source> Indicates that the LINK signal output from the PHY has changed from high to low or low to high.
1	MPR	0	R/W*1	Magic Packet Receive Interrupt <Interrupt Source> Indicates that a magic packet has been received. (This bit is cleared by writing 1 to the bit; however, the MAGIC signal is not cleared because it is an external output signal.)
0	FCD	0	R/W*1	Illegal Carrier Detection Interrupt <Interrupt Source> Indicates that an illegal carrier is detected on the line.

- Notes: 1. These bits are cleared by writing 1 to the corresponding bits. Writing 0 has no meaning.  
2. This register is initialized by an HDMAC/feLic software reset.

### 37.4.21 Interrupt Mask Setting Register (CXR22)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CXR22 is a register that masks the interrupts indicated by CXR21.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	BCRE	PROE	—	LNKE	MPRE	FCDE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value*	R/W	Description
31 to 6	—	All 0	R	Reserved
5	BCRE	0	R/W	Reserved
4	PROE	0	R/W	PAUSE Frame Retransmit Retry Over Interrupt Enable 0: Disables an interrupt indicated by the corresponding bit in CXR21. 1: Enables an interrupt indicated by the corresponding bit in CXR21.
3	—	0	R	Reserved
2	LKNE	0	R/W	LINK Signal Change Interrupt Enable 0: Disables an interrupt indicated by the corresponding bit in CXR21. 1: Enables an interrupt indicated by the corresponding bit in CXR21.
1	MPRE	0	R/W	Magic Packet Receive Interrupt Enable 0: Disables an interrupt indicated by the corresponding bit in CXR21. 1: Enables an interrupt indicated by the corresponding bit in CXR21.
0	FCDE	0	R/W	Illegal Carrier Detection Interrupt Enable 0: Disables an interrupt indicated by the corresponding bit in CXR21. 1: Enables an interrupt indicated by the corresponding bit in CXR21.

Note: \* This register is initialized by an HDMAC/feLic software reset.

**37.4.22 MII Control Register (CXR23)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CXR23 is a register that controls the MII interface to access the PHY register.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	MDI	MDO	MMD	MDC
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	—	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value*	R/W	Description
31 to 4	—	All 0	R	Reserved
3	MDI	—	R	MII Management Data In Read data from MII
2	MDO	0	R/W	MII Management Data Out Write data to MII
1	MMD	0	R/W	MII Management Mode 1: Data is written to MII. 0: Data is read from MII.
0	MDC	0	R/W	MII Management Clock Clock for MII

Note: \* This register is initialized by an HDMAC/feLic software reset.

**37.4.23 PHY Status Register (CXR2B)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CXR2B is a register that can monitor the PHY status signal.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	LINK
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value*	R/W	Description
31 to 1	—	All 0	R	Reserved
0	LINK	—	R	The status of the PHY output LINK signal can be monitored. See the specifications of the PHY to be connected.

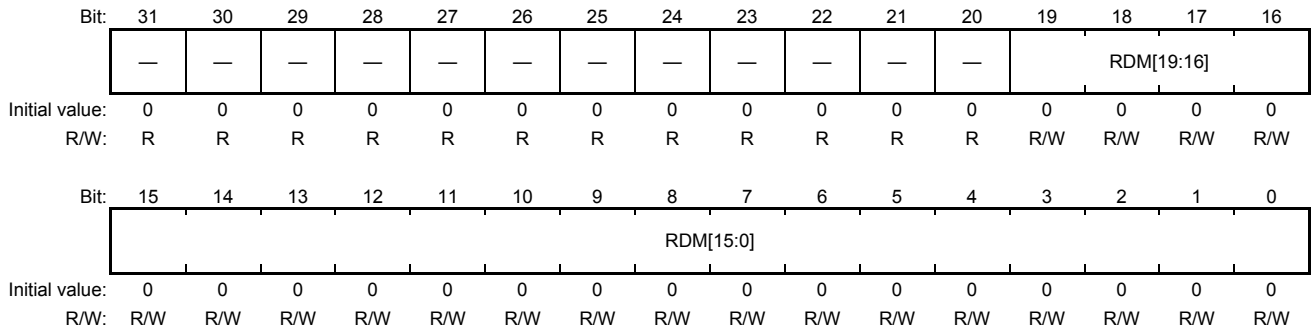
Note: \* This register is initialized by an HDMAC/feLic software reset.



**37.4.24 Random Number Generating Counter Upper Limit Setting Register (CXR30)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CXR30 is a register that can set the upper limit of the counter used for the random number generator.



Bit	Bit Name	Initial Value*	R/W	Description
31 to 20	—	All 0	R	Reserved
19 to 0	RDM[19:0]	H'00000	R/W	Upper limit of the Counter used for the Random Number Generator H'00000: Setting for normal operation H'00001 to H'FFFFE: Counter upper limit Note: Since the operation of the feLic random number generator depends on the value set to this register, take care when setting a value other than 0.

Note: \* This register is initialized by an HDMAC/feLic software reset.

**37.4.25 IPG Counter Setting Register (CXR70)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CXR70 is a register that specifies the IPG (inter packet gap) value.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	IPG[4:0]				
Initial value:	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value*	R/W	Description
31 to 5	—	All 0	R	Reserved
4 to 0	IPG[4:0]	H'14	R/W	These bits set the IPG value in 40 ns units. Setting      IPG value H'00 to H'06: 400 ns H'07:        440 ns :            : H'13:        920 ns H'14:        960 ns (default) :            : H'1F:        1440 ns

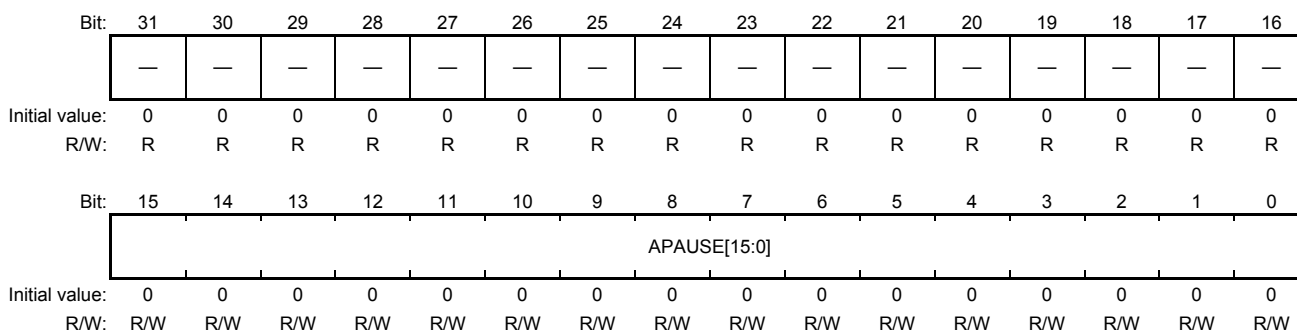
Note: The CXR20 register should not be modified while the transmitting and receiving functions are enabled.

Note: \* This register is initialized by an HDMAC/feLic software reset.

### 37.4.26 Automatic PAUSE Parameter Setting Register (CXR71)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CXR71 is used to set the TIME parameter value of an automatic PAUSE frame. When an automatic PAUSE frame is transmitted, the value set in this register is used as the TIME parameter of the PAUSE frame.



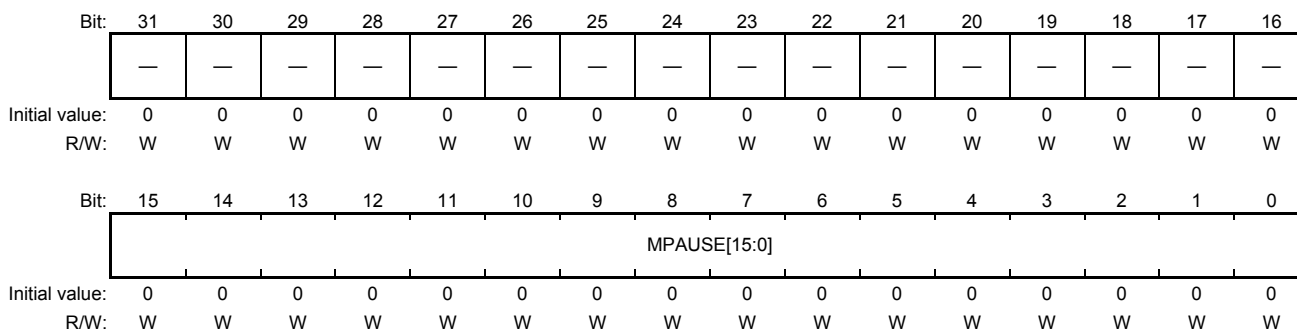
Bit	Bit Name	Initial Value*	R/W	Description
31 to 16	—	All 0	R	Reserved
15 to 0	APAUSE[15:0]	H'0000	R/W	TIME Parameter Value of an Automatic PAUSE Frame One bit is equivalent to 512 bit-time.

Note: \* This register is initialized by an HDMAC/feLic software reset.

### 37.4.27 Manual PAUSE Parameter Setting Register (CXR72)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CXR72 is used to set the TIME parameter value of a manual PAUSE frame. When a manual PAUSE frame is transmitted, the value set in this register is used as the TIME parameter of the PAUSE frame.



Bit	Bit Name	Initial Value*	R/W	Description
31 to 16	—	All 0	W	Reserved
15 to 0	MPAUSE[15:0]	H'0000	W	TIME Parameter Value of an Manual PAUSE Frame One bit is equivalent to 512 bit-time.

Notes: This register can't be read.

\* This register is initialized by an HDMAC/feLic software reset.

**37.4.28 Receive PAUSE Frame Counter Register (CXR80)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CXR80 is used to the counter of received the PAUSE frame.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	RPAUSE[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

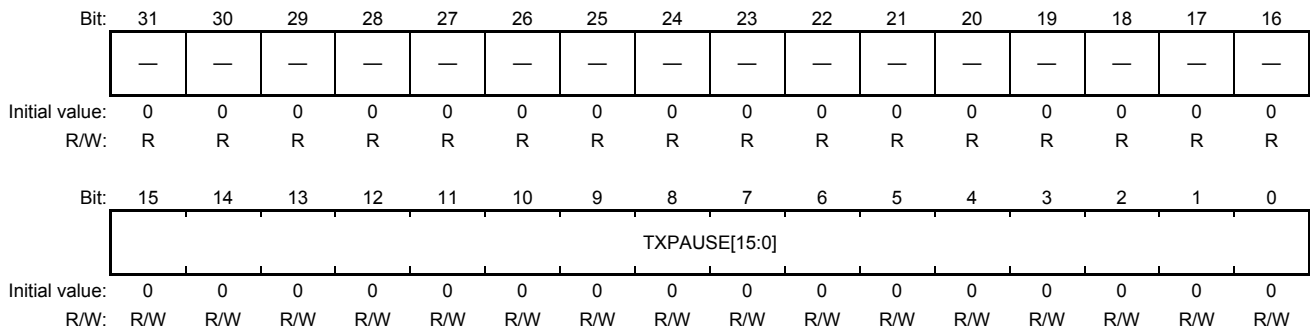
Bit	Bit Name	Initial Value*	R/W	Description
31 to 8	—	All 0	R	Reserved
7 to 0	RPAUSE[7:0]	H'00	R	Received PAUSE frame Counter

- Notes: Writing to this register has no meaning.  
 \* This register is initialized by an HDMAC/feLic software reset.

**37.4.29 PAUSE Frame Retransmit Count Setting Register (CXR81)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CXR81 is used to set the upper limit of the automatic PAUSE frame retransmission count. For details of this register, see section 37.9.2 (6), Flow Control Conforming to IEEE802.3.



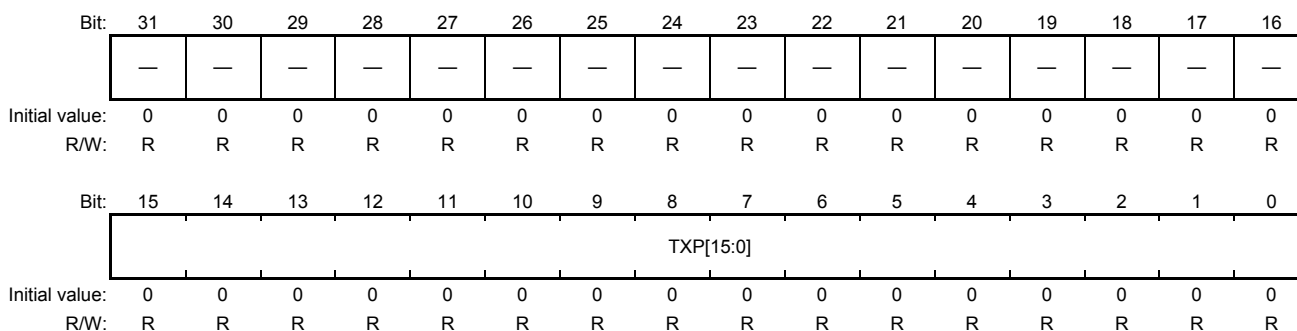
Bit	Bit Name	Initial Value*1	R/W	Description
31 to 16	—	All 0	R	Reserved
15 to 0	TXPAUSE[15:0]	H'0000	R/W	Upper Limit of PAUSE Frame Retransmission Setting Retransmit count H'0000: Unlimited*2 H'0001: 1 : : H'FFFF: 65535  Note: The CXR20 register should not be modified while the transmitting function is enabled.

- Notes: 1. This register is initialized by an HDMAC/feLic software reset.  
 2. When using in unlimited setting, the time parameter MPAUSE of CXR71 should be set other than zero.

### 37.4.30 PAUSE Frame Retransmit Counter Register (CXR82)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CXR82 is used to the counter of retransmitting of the PAUSE frame. For details of this register, see section 37.9.2 (6), Flow Control Conforming to IEEE802.3.



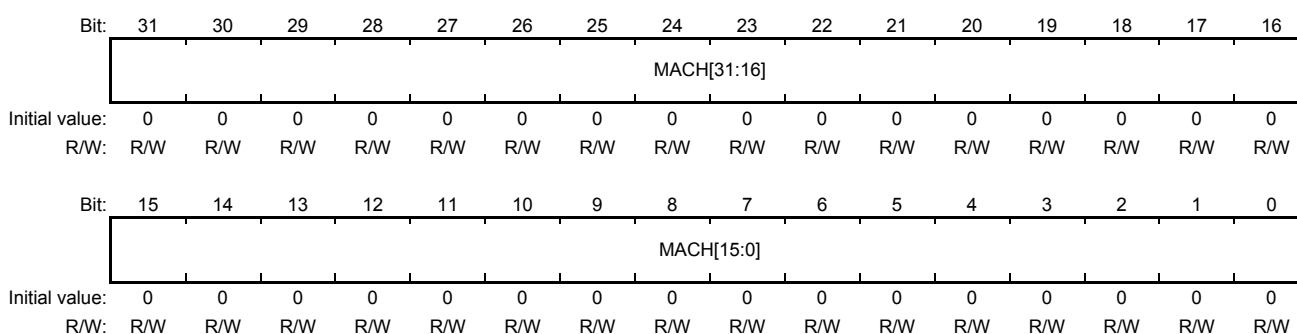
Bit	Bit Name	Initial Value*	R/W	Description
31 to 8	—	All 0	R	Reserved
15 to 0	TXP[15:0]	H'0000	R	PAUSE Frame Retransmit Counter

Notes: Writing to this register has no meaning.  
 \* This register is initialized by an HDMAC/feLic software reset.

### 37.4.31 MAC Address High Register (CXR24)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CXR24 is used to set the upper 32 bits of the universal MAC address.



Bit	Bit Name	Initial Value*	R/W	Description
31 to 0	MACH[31:0]	H'00000000	R/W	MAC Address Upper 32 Bits

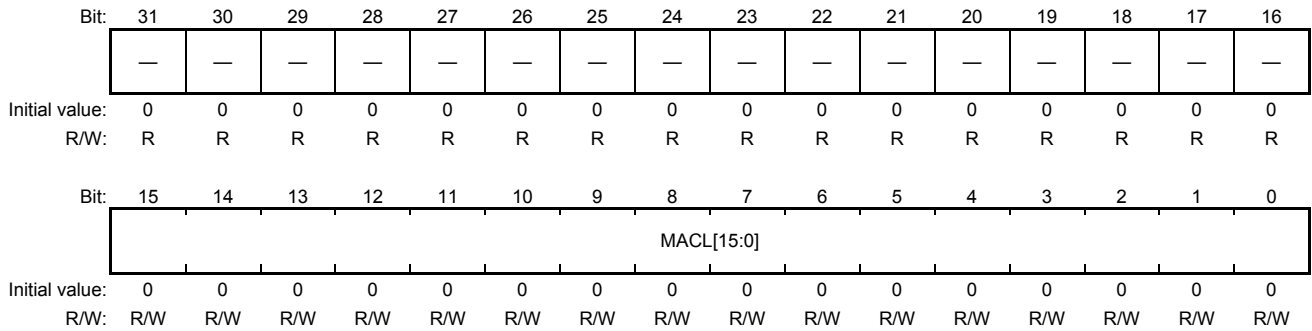
Note: These bits should not be written to while the transmission enable and reception enable bits in CXR20 are set.

Note: \* This register is initialized by an HDMAC/feLic software reset.

**37.4.32 MAC Address Low Register (CXR25)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CXR25 is used to set the lower 16 bits of the universal MAC address.



Bit	Bit Name	Initial Value*	R/W	Description
31 to 16	—	All 0	R	Reserved
15 to 0	MACL[15:0]	H'0000	R/W	MAC Address Lower 16 Bits

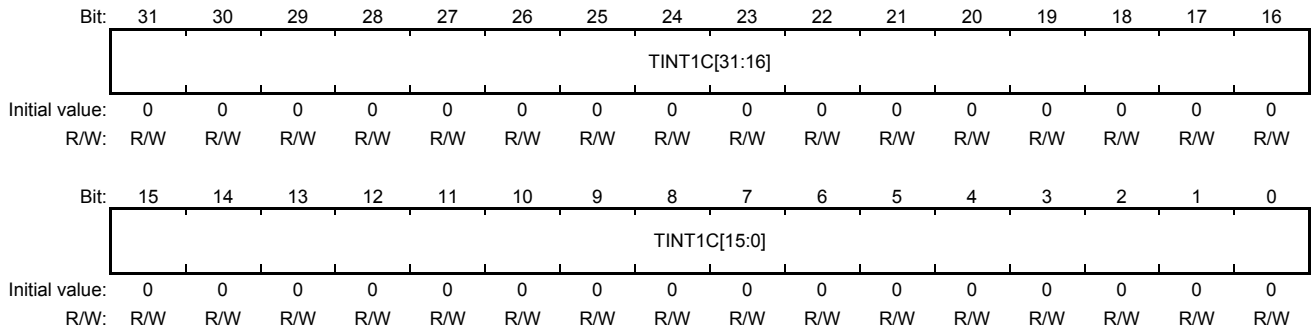
Note: These bits should not be written to while the transmission enable and reception enable bits in CXR20 are set.

Note: \* This register is initialized by an HDMAC/feLic software reset.

**37.4.33 TINT1 Count Register (CX40)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CXR40 is a register with which the TINT1 source signal count value can be read and referred to.



Bit	Bit Name	Initial Value*	R/W	Description
31 to 0	TINT1C[31:0]	H'00000000	R/W	TINT1 (Transmit Timeout) Counter This counter is not automatically updated after incremented to H'FFFFFFFF. To update the counter continuously and restart increment from H'00000000, write-access to the counter and clear it. Note: Cleared by write access.

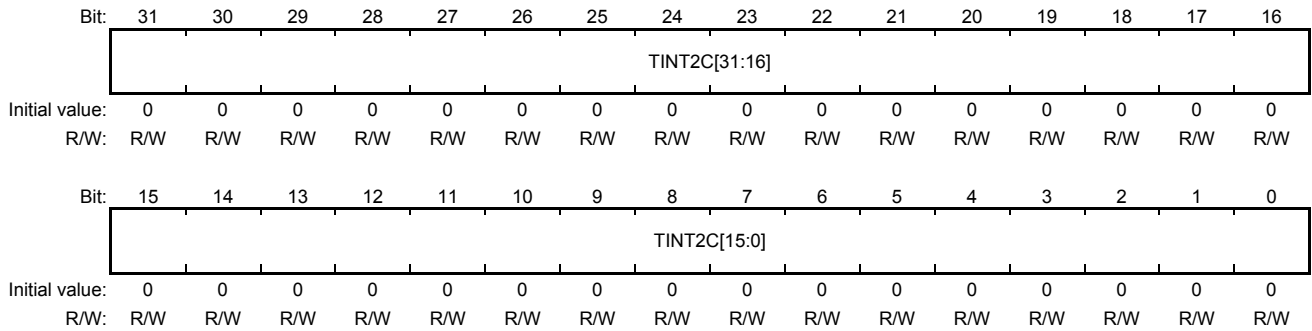
Note: \* This register is initialized by an HDMAC/feLic software reset.



**37.4.34 TINT2 Count Register (CX41)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CXR41 is a register with which the TINT2 source signal count value can be read and referred to.



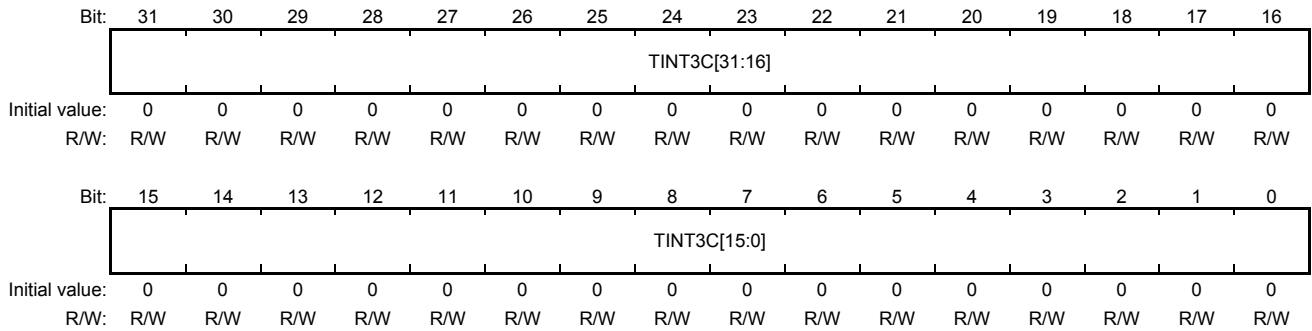
Bit	Bit Name	Initial Value*	R/W	Description
31 to 0	TINT2C[31:0]	H'00000000	R/W	TINT2 (Collision Detection during Frame Transmission) Counter This counter is not automatically updated after incremented to H'FFFFFFFF. To update the counter continuously and restart increment from H'00000000, write-access to the counter and clear it. Note: Cleared by write access.

Note: \* This register is initialized by an HDMAC/feLic software reset.

**37.4.35 TINT3 Count Register (CX42)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CXR42 is a register with which the TINT3 source signal count value can be read and referred to.



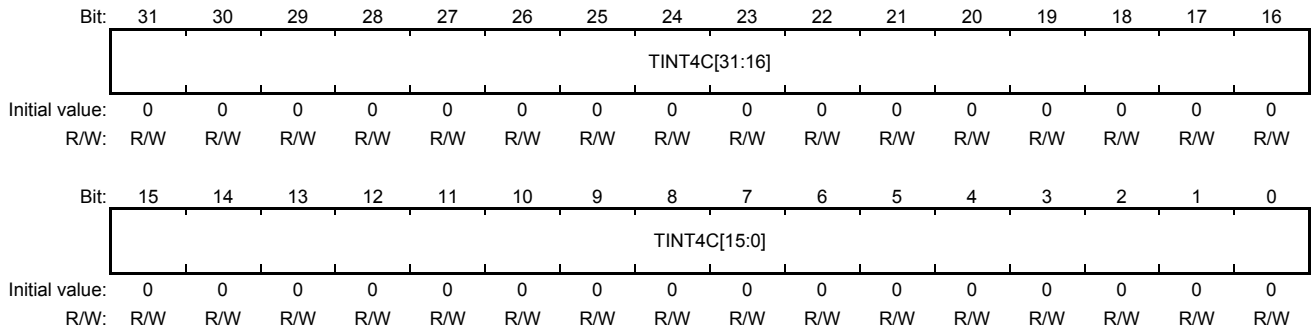
Bit	Bit Name	Initial Value*	R/W	Description
31 to 0	TINT3C[31:0]	H'00000000	R/W	<p>TINT3 (Carrier Loss during Frame Transmission) Counter</p> <p>This counter is not automatically updated after incremented to H'FFFFFFFF. To update the counter continuously and restart increment from H'00000000, write-access to the counter and clear it.</p> <p>Note: Cleared by write access.</p>

Note: \* This register is initialized by an HDMAC/feLic software reset.

**37.4.36 TINT4 Count Register (CX43)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CXR43 is a register with which the TINT4 source signal count value can be read and referred to.



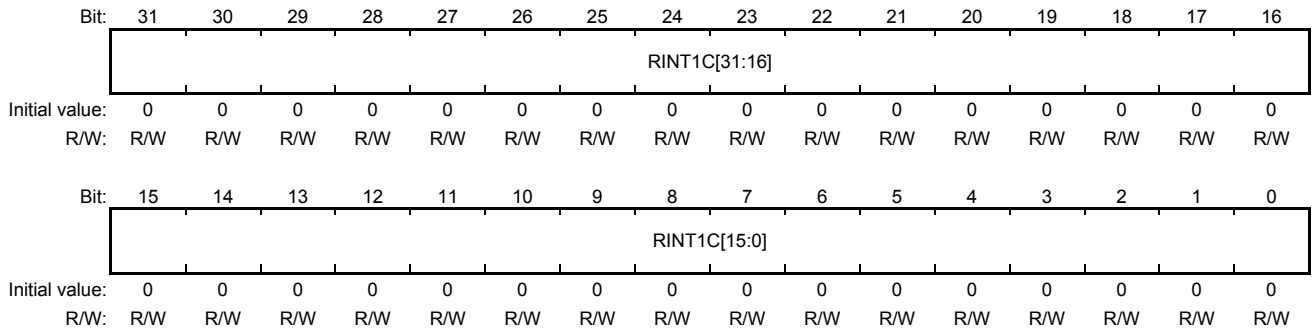
Bit	Bit Name	Initial Value*	R/W	Description
31 to 0	TINT4C[31:0]	H'00000000	R/W	TINT4 (Carrier not Detected) Counter  This counter is not automatically updated after incremented to H'FFFFFFF. To update the counter continuously and restart increment from H'00000000, write-access to the counter and clear it.  Note: Cleared by write access.

Note: \* This register is initialized by an HDMAC/feLic software reset.

**37.4.37 RINT1 Count Register (CX50)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CX50 is a register with which the RINT1 source signal count value can be read and referred to.



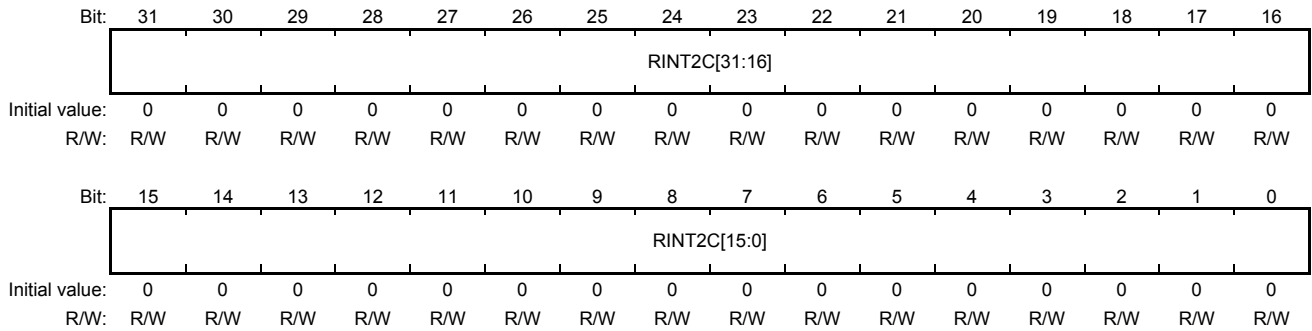
Bit	Bit Name	Initial Value*	R/W	Description
31 to 0	RINT1C[31:0]	H'00000000	R/W	RINT1 (CRC Error) Counter  This counter is not automatically updated after incremented to H'FFFFFFF. To update the counter continuously and restart increment from H'00000000, write-access to the counter and clear it.  Note: Cleared by write access.

Note: \* This register is initialized by an HDMAC/feLic software reset.

**37.4.38 RINT2 Count Register (CX51)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CXR51 is a register with which the RINT2 source signal count value can be read and referred to.



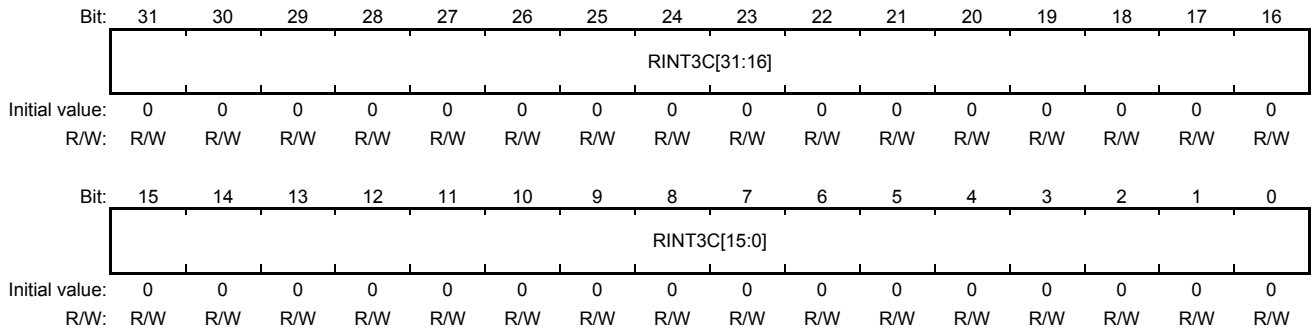
Bit	Bit Name	Initial Value*	R/W	Description
31 to 0	RINT2C[31:0]	H'00000000	R/W	RINT2 (Frame Receive Error) Counter  This counter is not automatically updated after incremented to H'FFFFFFF. To update the counter continuously and restart increment from H'00000000, write-access to the counter and clear it.  Note: Cleared by write access.

Note: \* This register is initialized by an HDMAC/feLic software reset.

**37.4.39 RINT3 Count Register (CX52)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CX52 is a register with which the RINT3 source signal count value can be read and referred to.



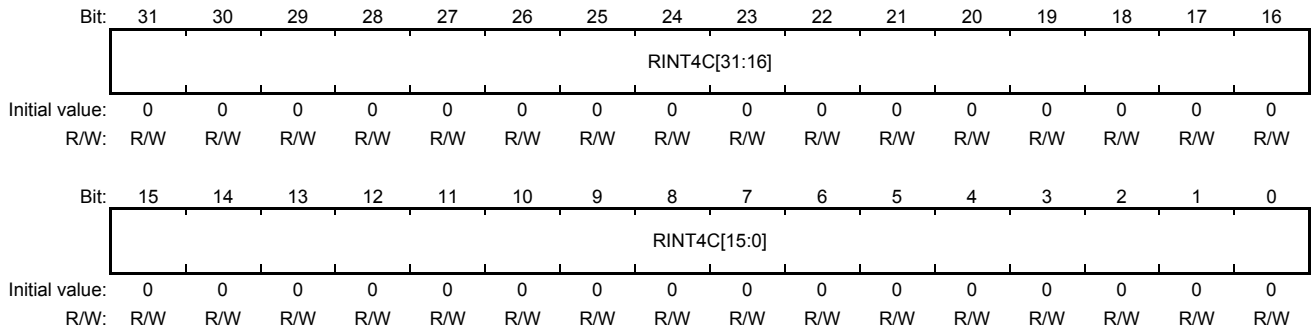
Bit	Bit Name	Initial Value*	R/W	Description
31 to 0	RINT3C[31:0]	H'00000000	R/W	RINT3 (Frame Length Error: less than 64 bytes) Counter  This counter is not automatically updated after incremented to H'FFFFFFF. To update the counter continuously and restart increment from H'00000000, write-access to the counter and clear it.  Note: Cleared by write access.

Note: \* This register is initialized by an HDMAC/feLic software reset.

**37.4.40 RINT4 Count Register (CX53)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CX53 is a register with which the RINT4 source signal count value can be read and referred to.



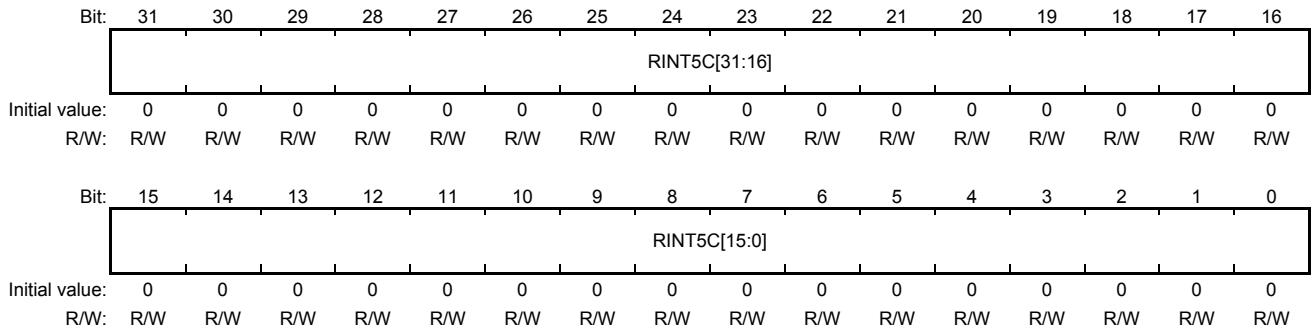
Bit	Bit Name	Initial Value*	R/W	Description
31 to 0	RINT4C[31:0]	H'00000000	R/W	RINT4 (Frame Length Error: 1518 bytes or more) Counter This counter is not automatically updated after incremented to H'FFFFFFFF. To update the counter continuously and restart increment from H'00000000, write-access to the counter and clear it. Note: Cleared by write access.

Note: \* This register is initialized by an HDMAC/feLic software reset.

**37.4.41 RINT5 Count Register (CX54)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CXR54 is a register with which the RINT5 source signal count value can be read and referred to.



Bit	Bit Name	Initial Value*	R/W	Description
31 to 0	RINT5C[31:0]	H'00000000	R/W	RINT5 (Fractional Number Bit Error) Counter  This counter is not automatically updated after incremented to H'FFFFFFFF. To update the counter continuously and restart increment from H'00000000, write-access to the counter and clear it.  Note: Cleared by write access.

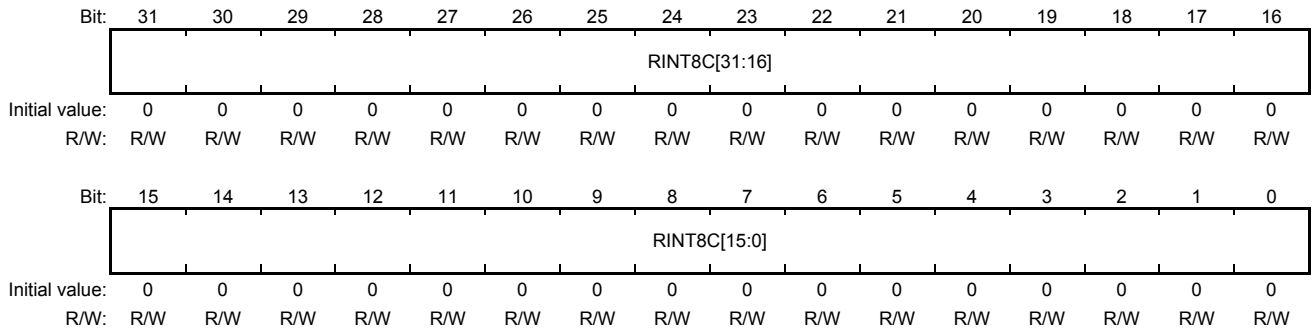
Note: \* This register is initialized by an HDMAC/feLic software reset.



**37.4.42 RINT8 Count Register (CX55)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CX55 is a register with which the RINT8 source signal count value can be read and referred to.



Bit	Bit Name	Initial Value*	R/W	Description
31 to 0	RINT8C[31:0]	H'00000000	R/W	RINT8 (Multicast Frame Reception) Counter  This counter is not automatically updated after incremented to H'FFFFFFF. To update the counter continuously and restart increment from H'00000000, write-access to the counter and clear it.  Note: Cleared by write access.

Note: \* This register is initialized by an HDMAC/feLic software reset.

## 37.5 Data Format

RZ/G1H

RZ/G1N

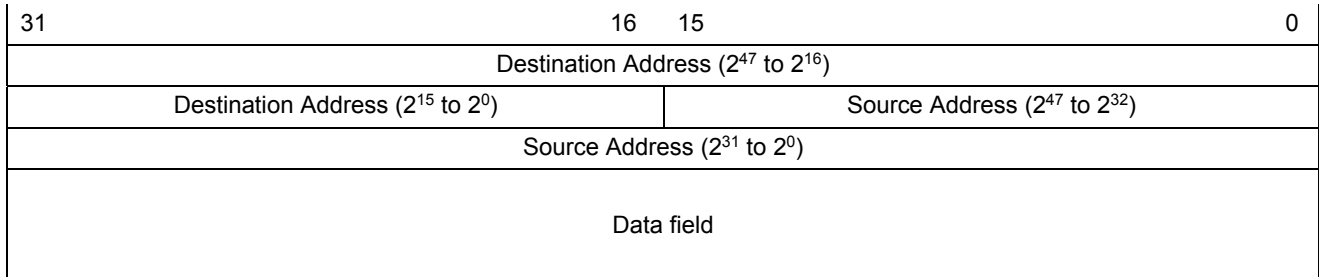
RZ/G1M

RZ/G1E

### 37.5.1 Ethernet Packet

#### (1) Transmit Packet

Figure 37.3 shows the data format of a transmit packet. Table 37.5 shows the field definition of a transmit packet.



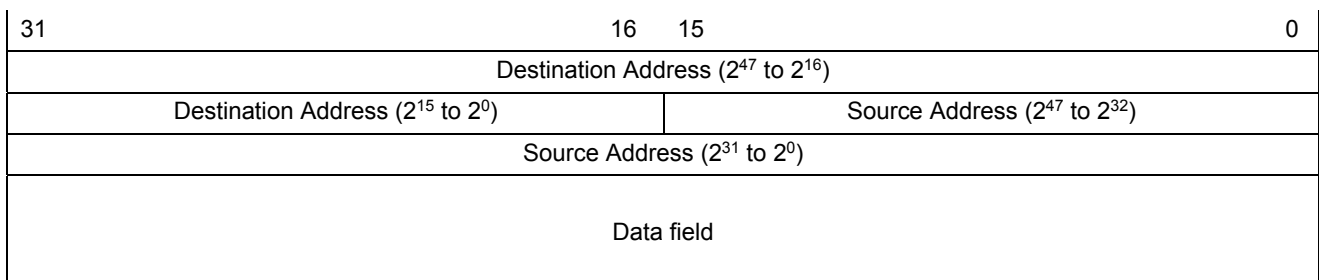
**Figure 37.3 Data Format of a Transmit Packet**

**Table 37.5 Field Definition of a Transmit Packet**

Field	Definition
Destination Address	See IEEE Std 802.3.
Source Address	See IEEE Std 802.3.
Data field	See IEEE Std 802.3.

#### (2) Receive Packet

Figure 37.4 shows the data format of a receive packet. Table 37.6 shows the field definition of a receive packet.



**Figure 37.4 Data Format of a Receive Packet**

**Table 37.6 Field Definition of a Receive Packet**

Field	Definition
Destination Address	See IEEE Std 802.3.
Source Address	See IEEE Std 802.3.
Data field	See IEEE Std 802.3.

RZ/G1H	RZ/G1N
RZ/G1M	RZ/G1E

## 37.6 Software Control Flow

### 37.6.1 Ether Software Control Flow

#### (1) Example of Ethernet Transmission and Reception Procedure

Figure 37.5 shows an example of initialization procedure for Ethernet transmission and reception. Figure 37.6 shows an example of Ethernet transmission and reception procedure.

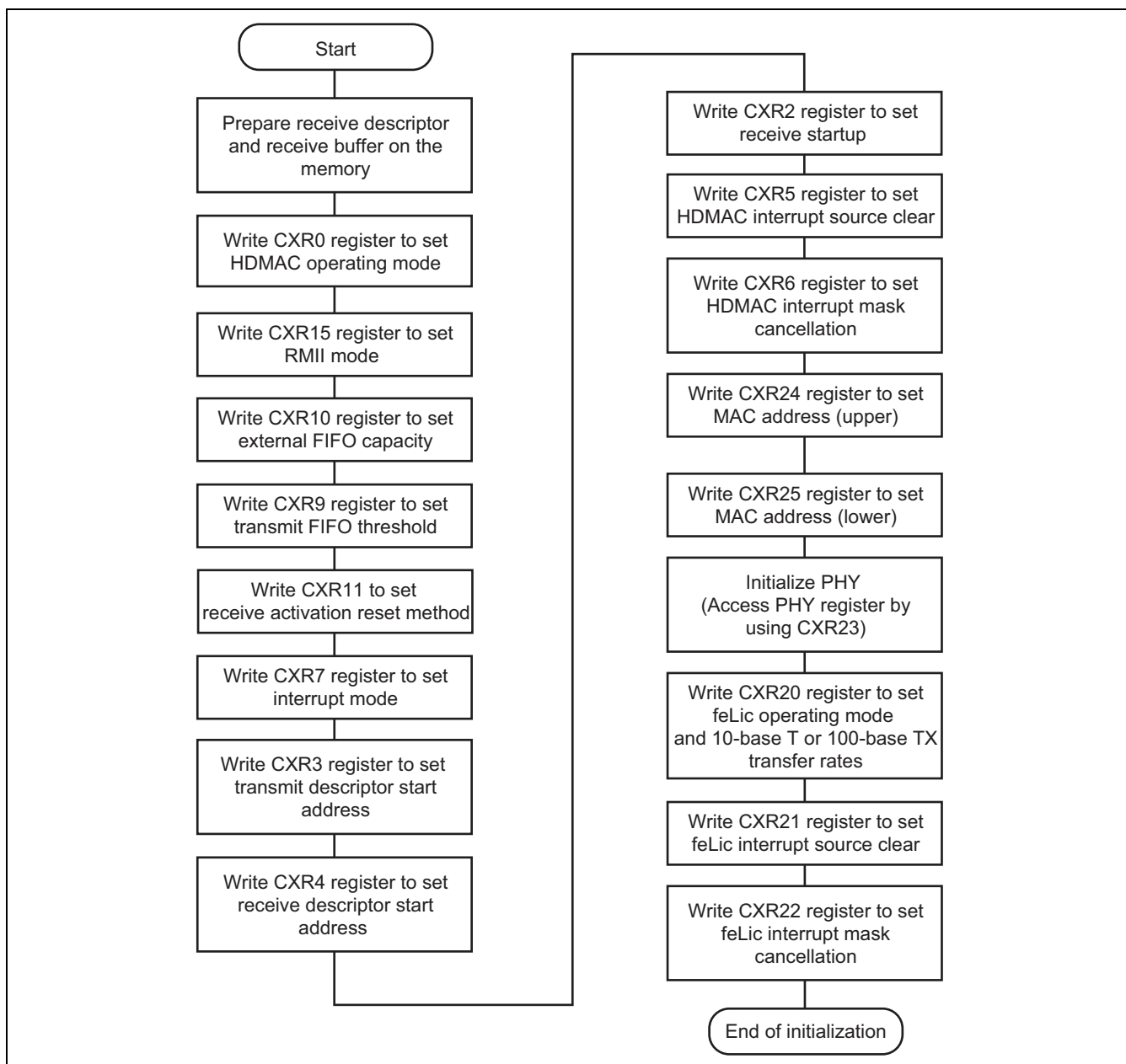


Figure 37.5 Initialization Procedure for Ethernet Transmission and Reception

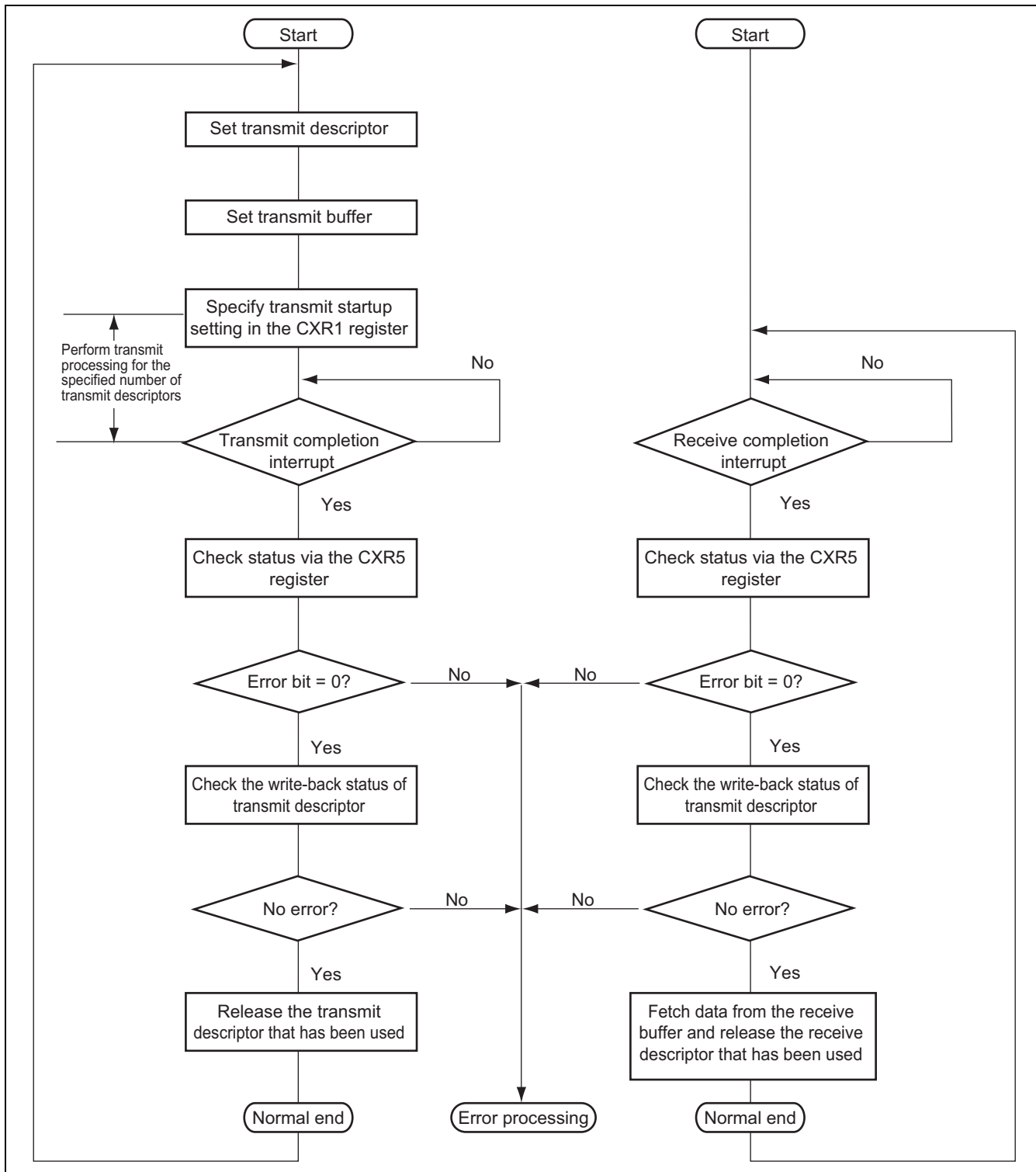


Figure 37.6 Ethernet Transmission and Reception Procedure

**(2) Example of PHY Register Accessing Procedure**

The PHY register is accessed by using the CXR23 register. This access should be performed using the MII management frame format as shown in Figure 37.7. Figure 37.8 shows an example of 1-bit data writing procedure to achieve the MII management frame. Figure 37.9 shows an example of bus releasing procedure. Figure 37.10 shows an example of 1-bit data reading procedure. Figure 37.11 shows an example of single bus releasing procedure.

Access Type	MII Management Frame							
Item	PRE	ST	OP	PHYAD	REGAD	TA	DATA	IDLE
Number of Bits	32	2	2	5	5	2	16	
Read	1..1	01	10	AAAAA	RRRRR	Z0	D...D	
Write	1..1	01	01	AAAAA	RRRRR	10	D...D	X

## Legend:

PRE: 32 consecutive 1s

ST: Write B'01 to indicate the start of a frame

OP: Write a code to indicate an access type

PHYAD: Write B'00001 if a PHY-LSI address is 1 (write sequentially from MSB). The values of these bits change according to the PHY-LSI address.

REGAD: Write B'00001 when a register address is 1 (write sequentially from MSB). The value of these bits change according to the PHY-LSI address.

TA: Data transmit source switch time on the MII interface.

(a) Write B'10 during write

(b) Release bus (indicated as Z0) during read

DATA: 16-bit data. Written to or read sequentially from MSB.

(a) Write 16-bit data during write

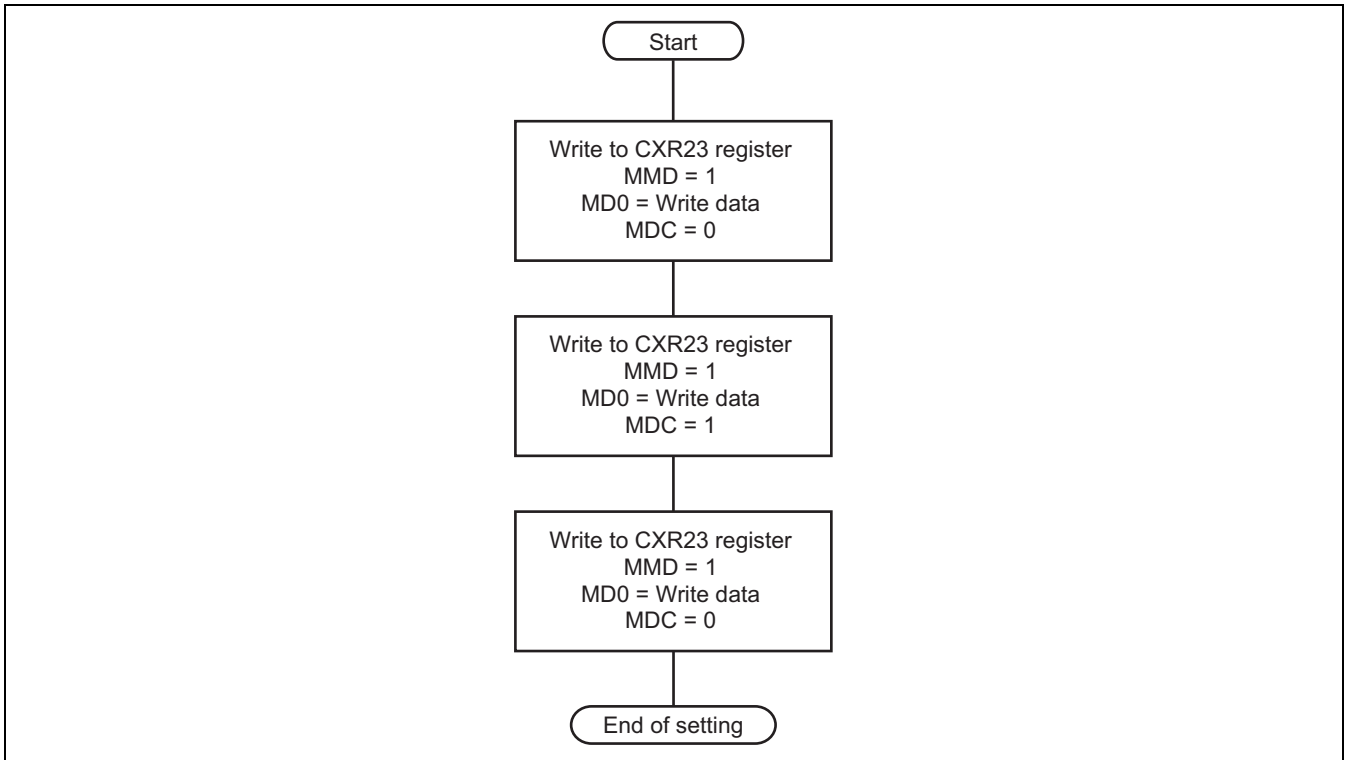
(b) Read 16-bit data during read

IDLE: Wait time until next MII management format is input

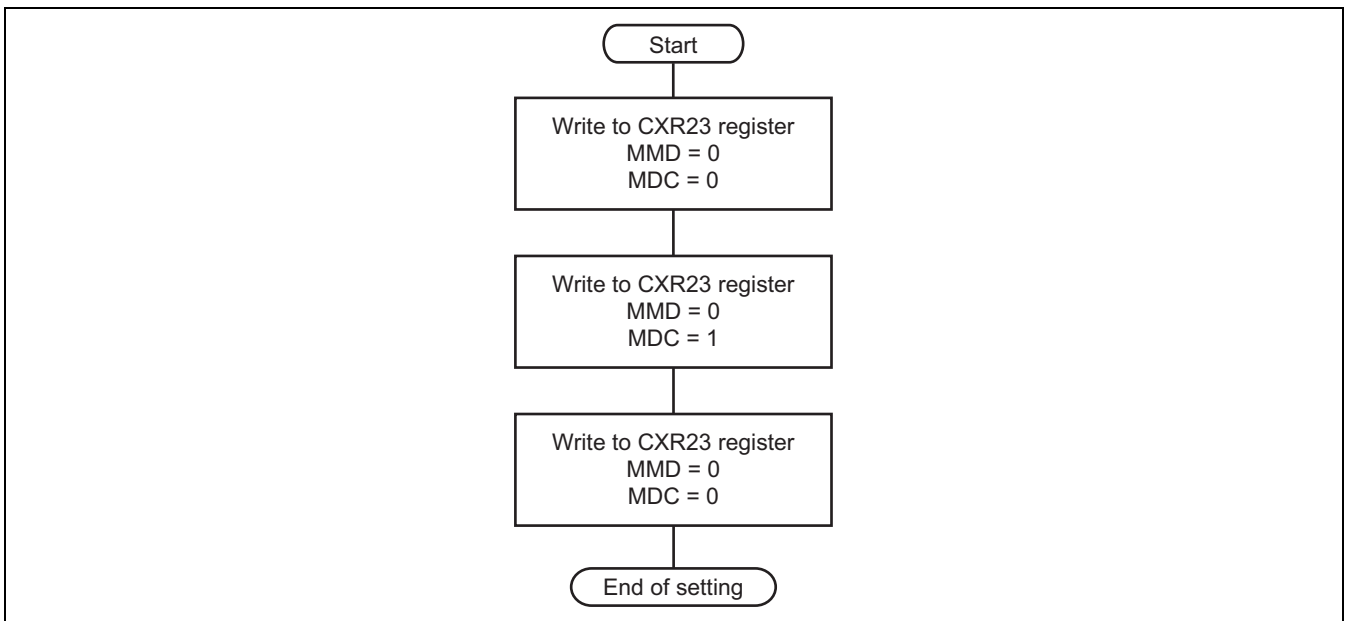
(a) Release a single bus (indicated as X) during write

(b) Control not required because a bus has been released using the TA bits during read

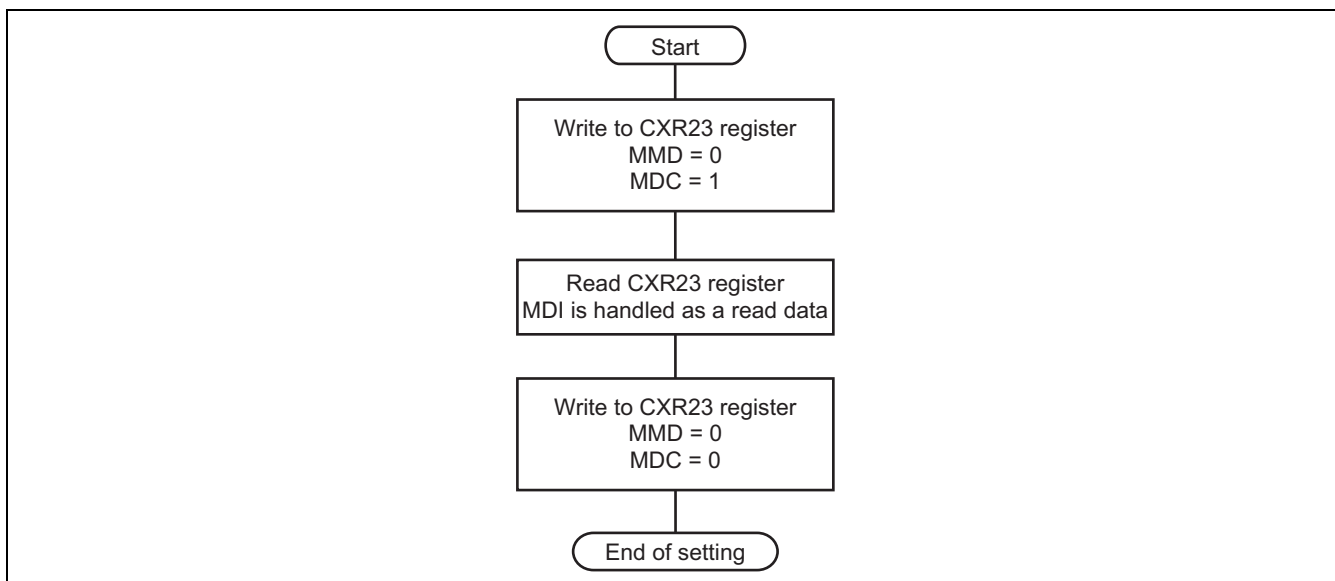
**Figure 37.7 MII Management Frame Format**



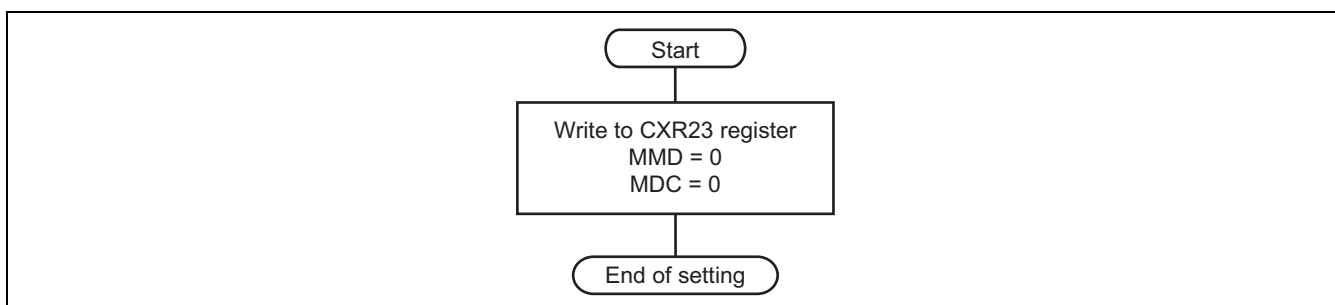
**Figure 37.8 1-Bit Data Writing Procedure**



**Figure 37.9 Bus Releasing Procedure**



**Figure 37.10 1-Bit Data Reading Procedure**



**Figure 37.11 Single Bus Releasing Procedure**

### (3) Example of the Procedure for Setting 10-Base T or 100-Base TX Transfer Rates

An example of the procedure for setting 10-base T and 100-base TX transfer rates is given below. Follow this procedure when setting the transfer rate.

This section describes the procedure during operation. For the initial settings, follow the flow in subsection (1), Example of Ethernet Transmission and Reception Procedure, above.

1. Detecting the PHY chip link being down  
Use the CXR2B or CXR21 register to detect the PHY chip link being down.
2. On finding the linking from the PHY chip down  
On detecting the link from the PHY chip being down, proceed with processing for that situation in accord with the PHY chip specification.
3. Transfer Rate Settings  
Make settings on the feLic side as required by the state of the PHY chip. Use the OLB bit in the CXR20 register to set the transfer rate.

## 37.7 Notes

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

### 37.7.1 Software Reset

The ether can be software-reset by setting the SWR bit in the CXR0 register of the HDMAC to 1. If software reset is applied during DMA transfer, the current DMA transfer can be completed but the data transferred by DMA transfer cannot be guaranteed.

### 37.7.2 Standby

If the ether is requested to enter the standby state, the ether first completes the current AXI bus operation, and then enters the standby state. After returning from the standby state, the ether should be reset and initialized.

### 37.7.3 Input Signal on the ETH\_RX\_ER Pin

If an error signal received from PHY is not at the active level for more than one cycle of the RMI reference clock at 50 MHz, the signal is not detected as an error signal.



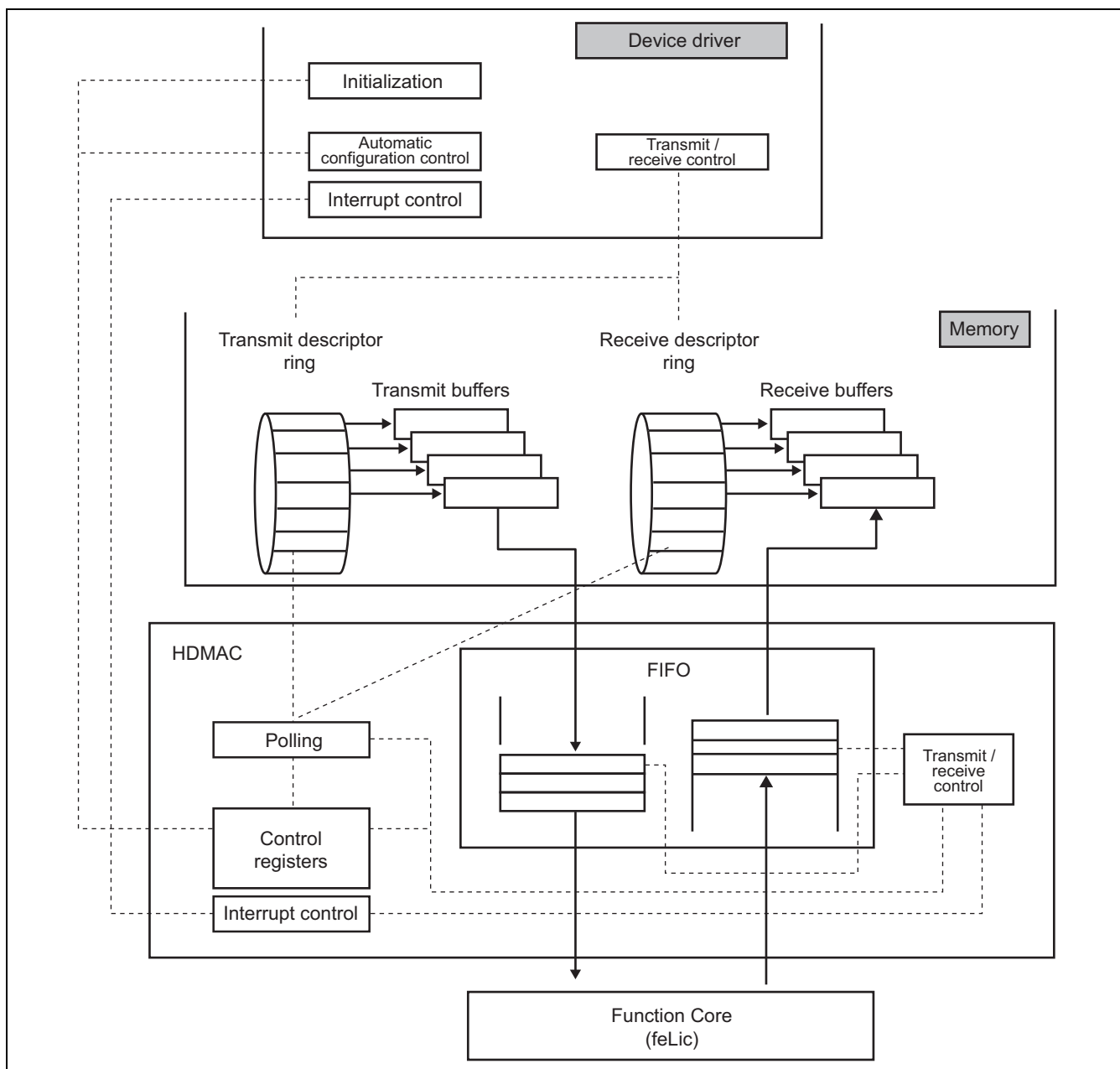
### 37.8 HDMAC Function Specifications

RZ/G1H	RZ/G1N
RZ/G1M	RZ/G1E

#### 37.8.1 Operation

##### (1) Basic Operation

Figure 37.12 shows an image of control between this logic core (HDMAC) and device driver (software).



**Figure 37.12 Image of Control between Device Driver and HDMAC**

The device driver should create the transmit and receive descriptor rings and their corresponding transmit and receive buffers on the memory.

During transmission, this logic core fetches the transmit descriptor to obtain the transmit buffer address and the number of transmit bytes, and transmits data from the transmit buffer to the function core via the transmit FIFO. During

reception, this logic core fetches the receive descriptor to obtain the receive buffer address and buffer size, and stores data received from the function core in the receive buffer via the receive FIFO.

## (2) Descriptor Rings

There is no restriction on the number of descriptors. It is recommended, however, that multiple descriptors are provided.

This logic core uses the descriptor from the start descriptor to the last descriptor sequentially. If it reaches the last descriptor, it returns to use the start descriptor.

The start descriptor address is specified by the start address setting registers (CXR3 and CXR4). The last descriptor is specified by the descriptor ring end bits (TDL, RDL) = 1 in the descriptor. The descriptor boundary is specified by the descriptor length bits (DL) in the operating mode setting register (CXR0).

There is no restriction on the number of receive descriptors in terms of a ring configuration. Note that if only one receive descriptor is used, a receive descriptor depletion occurs when one frame has been received. (For details, refer to section 37.8.1 (8) (g), Receive Descriptor Depletion.)

For details on the descriptor description format, refer to section 37.8.2, Transmit Descriptors, and section 37.8.3, Receive Descriptors.

## (3) Multiple Frames and Multiple Buffers

Multiple frames and multiple buffers enable consecutive frame transmission and reception.

In the receiver, a frame can be divided and stored in multiple buffers separately by specifying the frame in multiple descriptors.

In the transmitter, a frame is specified by a descriptor.

During transmission, after having transmitted data (frame) specified by a transmit descriptor, this logic core fetches the next descriptor. This logic core then determines that there is data (frame) to be transmitted next if the TACT bit in the fetched transmit descriptor is 1 and transmits the data (frame). If the TACT bit in the fetched transmit descriptor is 0, this logic core completes the transmit operation.

Note that bits 29 and 28 in the transmit descriptor TD0 should be set to 11. Otherwise, correct operation cannot be guaranteed.

During reception, after having received a frame, this logic core fetches the next receive descriptor. This logic core determines that the reception is ready if the RACT bit in the fetched receive descriptor is 1 and stores the received frame. If the RACT bit in the fetched receive descriptor is 0, this logic core determines that the receive descriptors have been depleted and completes the receive operation.

If this logic core receives a frame longer than the buffer length specified in the receive descriptor, it stores the frame up to the specified buffer length and then fetches the next receive descriptor. If this logic core further receives a frame longer than the buffer length specified in the fetched receive descriptor, it stores the frame up to the specified buffer length and then fetches the following descriptor. If this logic core receives a frame whose frame length is within the buffer size specified by the fetched receive descriptor, it stores the last byte of the frame and writes back the number of bytes so far stored in the receive buffer to the receive frame length (RFL) in the receive descriptor. The logic core then fetches the next descriptor to prepare for the next frame reception.

Note that correct operation cannot be guaranteed if the receive buffer length is specified as 0 in the receive descriptor.

#### **(4) DMA Operation**

##### **(a) Burst Operation**

This logic core accesses the descriptors and buffers in longword units via DMA transfer.

During descriptor (16 bytes as standard) fetch, 16-byte DMA transfer is performed per bus acquisition.

During transmit descriptor write back, 4-byte DMA transfer is performed per bus acquisition.

During receive descriptor write back, 8-byte DMA transfer is performed per bus acquisition.

During buffer data transfer, a maximum of 32-byte DMA transfer is performed per bus acquisition.

If the remaining data in a frame to be transferred is 17 to 32 bytes, 32-byte DMA transfer is performed per bus acquisition.

If the remaining data in a frame to be transferred is 9 to 16 bytes, 16-byte DMA transfer is performed per bus acquisition.

If the remaining data in a frame to be transferred is 5 to 8 bytes, 8-byte DMA transfer is performed per bus acquisition.

If the remaining data in a frame to be transferred is 1 to 4 bytes, 4-byte DMA transfer is performed per bus acquisition.

##### **(b) DMA Operation Error Report**

If a DMA error is detected during DMA operation, the BER bit in the status register (CXR5) is set to 1 to generate an interrupt. After interrupt, DMA operation should be restarted by a reset (system reset or software reset).

#### **(5) Transmit and Receive Buffers**

A transmit buffer address and transmit buffer length to be specified by a transmit descriptor can be set in byte units. However, if 1 to 16 bytes is specified as the transmit buffer length, the transmit buffer address should be aligned on a 32-byte boundary. Note that correct operation cannot be guaranteed if 0 byte is specified as the transfer buffer length.

A receive buffer address to be specified by a receive descriptor should be aligned on a 32-byte boundary to prevent the DMA burst operation from being performed beyond SDRAM boundary.

In addition, if the number of data bytes remaining in a frame to be transferred cannot be divided by DMA burst bytes (32 bytes), the receive buffer length to be specified by the receive descriptor should be specified on a 32-byte boundary since extra data is transmitted.

For example, if the number of last data bytes remaining in a receive frame is 17 bytes, invalid data is written in the 18th to 32nd bytes in the corresponding address of the receive buffer since 32-byte DMA burst transfer is performed.

#### **(6) Endian**

Endian conversion can be used for the data arrangement in the transmit and receive buffers according to the DE bit setting in the operating mode setting register (CXR0).

Note that only the endian of the data in the transmit and receive buffers can be changed. Endian of descriptors and registers cannot be changed.

Note: Be sure to set DE bit to 1 before operating the Ethernet MAC controller (Ether).

#### **(7) Transmit Operation**

##### **(a) Normal Transmit Operation**

This logic core starts the transmit processing when 1 is written to the TRNS bit in the transmit activation register (CXR1).

This logic core fetches a descriptor next to the previous descriptor from the transmit descriptor ring.

If the TACT bit in the fetched transmit descriptor is 1, data in the transmit buffer is read out and written in the transmit FIFO sequentially according to the specified transmit buffer address and the number of bytes.

If the TACT bit in the fetched transmit descriptor is 0, the TRNS bit in the transmit activation register (CXR1) is cleared to 0 and transmit processing is completed without any operation.

When data of the buffer length indicated by the descriptor has been transmitted to the function core via the transmit FIFO (normally completed or aborted), the transmit descriptor is written back to, and the next descriptor is fetched.

While the TACT bit in the fetched transmit descriptor is 1, the transmit descriptor fetch and DMA transfer are performed continuously.

If the TACT bit in the fetched transmit descriptor is 0, the FTC bit in the status register (CXR5) is set to 1 to indicate the completion of transmission thus requesting an interrupt to the CPU, and simultaneously the TRNS bit in the transmit activation register (CXR1) is cleared to 0 to stop transmit processing.

If data in the transmit FIFO exceeds the threshold (changes according to the register setting), if data of a frame has been stored, or if the transmit FIFO becomes full, the function core is activated and data in the transmit FIFO is transmitted to the function core synchronously with the RDY signal in the function core.

When a transmit completion signal or abort signal is input from the function core, the above transmit operation is ended.

#### **(b) Continuous Frame Transmit Operation**

Multiple frames can be specified in a transmit descriptor.

This logic core clears the TACT bit in the transmit descriptor to 0 when data transmission indicated in the transmit descriptor has been completed, and fetches the next transmit descriptor. While the TACT bit in the fetched descriptor is 1, the frame transmission is performed continuously. When the TACT bit in the transmit descriptor is 0, the FTC bit in the status register (CXR5) is set to 1 to indicate the transmission completion thus requesting an interrupt to the CPU, and the TRNS bit in the transmit activation register (CXR1) is cleared to 0 to stop transmit processing.

Generation of a transmit completion interrupt (the FTC bit in CXR1 is set to 1) informs the CPU that all the specified frames have been transmitted.

#### **(c) Transmit Abort**

If this logic core receives an abort signal (ATABT) from the function core during frame transmission, it aborts data transmission of the corresponding frame from transmit FIFO to the function core.

When the transmission is aborted, this logic core clears the TACT bit in the transmit descriptor to 0, sets bit 8 in the transmit frame status (TFS) to 1.

The following operations are the same as (1) Normal Transmit Operation or (2) Continuous Frame Transmit Operation described above.

When detected the TACT bit in the fetched transmit descriptor is 0, the FTC bit in the status register (CXR5) is set to 1 to indicate the transmission completion, and TABT bit is also set to 1 to indicate the transmission abort to requesting an interrupt to the CPU.

#### **(d) Transmit FIFO Underflow**

This logic core does not transmit data to the function core until data in the transmit FIFO exceeds the specified threshold (changes according to the register setting), data of a frame is stored in the transmit FIFO, or the transmit FIFO becomes full to prevent the transmit FIFO from underflow.

An underflow will occur if the transmit FIFO becomes empty (there is no data to be transmitted) because the bus mastership cannot be obtained.

In this case, the TFE bit in the status register (CXR5) is set to 1 to indicate transmit FIFO underflow and an interrupt is requested to the CPU.

The frame where an underflow occurred is transmitted to the function core in the same way as the normal frame. After the frame transmission, the TACT bit in the transmit descriptor is cleared to 0 and transmit frame status (TFS) is set to 1. The following operations are the same as (1) Normal Transmit Operation or (2) Continuous Frame Transmit Operation described above.

#### (e) Transmit Frame Retry

If this logic core receives an ATRTRY signal from the function core after having transmitted the last byte of a frame to the function core, this logic core fetches the start descriptor of the current frame again, and re-transmits the data of the current frame from the start to last bytes to the transmit FIFO.

### (8) Receive Operation

#### (a) Normal Receive Operation

This logic core starts receive processing when 1 is written to the R bit in the receive activation register (CXR2).

This logic core fetches the receive descriptor (Nth receive descriptor) next to the previous receive descriptor ((N - 1)th receive descriptor) from the receive descriptor ring, and enters the receive wait state.

In the receive wait state, if the receive FIFO contains data of 32 bytes or more or the last byte, data is transferred from the receive FIFO to the receive buffer.

When the receive buffer specified by the receive descriptor becomes full, this logic core writes 0 to the RACT bit in the receive descriptor and fetches the (N + 1)th receive descriptor. If the RACT bit in the (N + 1)th receive descriptor is 1, this logic core enters the receive wait state again.

If the last byte of a frame has been transferred, this logic core writes 0 and 1 in the RACT bit and the RFP[0] bit in the receive descriptor, respectively, sets the FRC bit in the status register (CXR5) to 1 to indicate the completion of frame reception, requests an interrupt to the CPU, and finally fetches the (N + 2)th receive descriptor.

If the RACT bit in the (N + 2)th receive descriptor is 1, this logic core enters the receive wait state. Contrarily, if the RACT bit in the (N + 2)th receive descriptor is 0, a receive descriptor depletion occurs. (For details, refer to section 37.8.1 (8) (g), Receive Descriptor Depletion.)

#### (b) Continuous Frame Receive Operation

As described in (1) Normal Receive Operation, when a frame has been received and the last byte of the frame has been transferred, this logic core writes 0 and 1 in the RACT bit and RFP[0] bit in the Nth receive descriptor, respectively, sets the FRC bit in the status register (CXR5) to 1 to indicate the completion of frame reception, generates an interrupt to the CPU, fetches the (N + 1)th receive descriptor, and enters the receive wait state.

When the last byte in the (N + 1)th receive descriptor has been transferred, this logic core writes 0 and 1 in the RACT bit and RFP[0] bit in the (N + 1)th receive descriptor, respectively, sets the FRC bit in the status register (CXR5) to 1 to indicate the completion of frame reception, generates an interrupt to the CPU, fetches the (N + 2)th receive descriptor, and enters the receive wait state.

This logic core then receives frames continuously until the RACT bit in the fetched descriptor is cleared to 0 (a receive descriptor depletion occurs).

**(c) Receive Operation of Multiple Frames and Multiple Buffers**

If the byte count of the received Mth frame is greater than the buffer length specified by the Nth receive descriptor, this logic core transfers data of the specified receive buffer length and then writes 0s in the RACT bit and RFP[0] bit in the Nth receive descriptor and fetches the (N + 1)th receive descriptor.

With the (N + 1)th receive descriptor, this logic core performs the data transfer of the same frame (Mth frame). If the byte count of the received Mth frame is greater than the buffer length specified by the (N + 1)th receive descriptor, this logic core transfers data of the specified receive buffer length and writes 0s in the RACT bit and RFP[0] bit in the (N + 1)th receive descriptor and fetches the (N + 2)th receive descriptor as described above. Contrarily, if the byte count of the received Mth frame is smaller than the buffer length specified by the (N + 1)th receive descriptor, this logic core, after having transferred the last byte, writes 0 and 1 in the RACT bit and RFP[0] bit in the (N + 1)th receive descriptor, sets the FRC bit in the status register (CRX5) to 1 to indicate the completion of frame reception, generates an interrupt to the CPU, fetches the (N + 2)th receive descriptor, and enters the receive wait state, as described in (1) Normal Receive Operation.

**(d) Receive Abort**

If this logic core receives a receive abort (ARABT) signal from the function core during frame reception, it aborts reception of the corresponding frame data from the function core.

This logic core transfers data stored in the receive FIFO before receive abortion to the receive buffer. When the last byte has been transferred, this logic core clears the RACT bit in the receive descriptor to 0, sets bit 8 of receive frame status in the receive descriptor to 1, sets the FRC and RABT bits in the status register (CRX5) to 1s to indicate the frame transmission completion and receive abort detection, respectively, and finally generates an interrupt to the CPU.

If this logic core receives an ARABT signal from the function core while the number of data bytes of the stored frame in the receive FIFO is less than 16 bytes, this logic core deletes the corresponding frame.

**(e) Receive FIFO Overflow**

If the receive FIFO becomes full because the bus mastership cannot be obtained, an overflow error occurs because the next data cannot be stored in the receive FIFO.

If an overflow error occurs, the receive FIFO terminates the data reception and sets the RFE bit in the status register (CXR5) to 1 to indicate the receive FIFO overflow, and generates an interrupt to the CPU. When the transfer of the byte immediately before the overflow has been completed, this logic core writes 0 and 1 to the RACT bit and bit 9 of receive frame status (RFS) in the receive descriptor, respectively, sets the FRC and RFE bits in the status register (CXR5) to 1s to indicate the frame reception completion and receive FIFO overflow, respectively, and finally generates an interrupt to the CPU.

While the receive FIFO is full, the next frame is received but discarded. Simultaneously, the discarded frame counter register (CXR8) is incremented.

If the receive FIFO becomes not full after data has been transferred from the receive FIFO to the receive buffer, this logic core restarts the reception from the start byte of the next receive frame.

The number of frames that can be simultaneously stored in the receive FIFO is limited to 16 frames due to the frame management restriction. Accordingly, this logic core cannot receive a frame if 16 frames have been stored in the receive FIFO. If this logic core receives the start data of the 17th frame, it sets the RFRMER bit in the status register (CXR5) to 1 to indicate the receive frame count overflow, and generates an interrupt to the CPU.

This logic core receives the next frame but discards it, and simultaneously increments the discarded frame counter register (CXR8).

If a space of 1 frame or more is produced in the receive FIFO after data has been transferred from the receive FIFO to the receive buffer, this logic core restarts the reception from the start byte of the next receive frame.

**(f) Flow Control Support**

This function core provides an ARBSY signal to inform the function core of the receive FIFO status. It can output the ARBSY signal based on the data amount stored in the receive FIFO according to the setting of the receive FIFO busy transmit threshold setting register (CXR16).

Accordingly, the flow can be controlled by sending "BUSY" to the function core before the receive FIFO overflows.

The BUSY status can be cancelled when the data byte count or the frame count in the receive FIFO become (the byte count value causing a transition to the BUSY state – 32 bytes) or smaller and (the frame count value causing a transition to the BUSY state – 1 frame) or smaller, respectively.

**(g) Receive Descriptor Depletion**

When this logic core has transferred data of the Mth frame to the receive buffer specified by the Nth receive descriptor, it fetches the (N + 1)th receive descriptor to prepare for the reception of the (M + 1)th frame.

If the RACT bit of the fetched descriptor ((N + 1)th descriptor) is 0, this logic core regards it as receive descriptor depletion, sets the RDE bit in the status register (CXR5) to 1 to indicate the receive descriptor depletion, and generates an interrupt to the CPU.

Simultaneously, this logic core clears the R bit in the receive activation register (CXR2) to 0 and terminates the receive processing. In this case, data transfer from the function core to the receive FIFO continues.

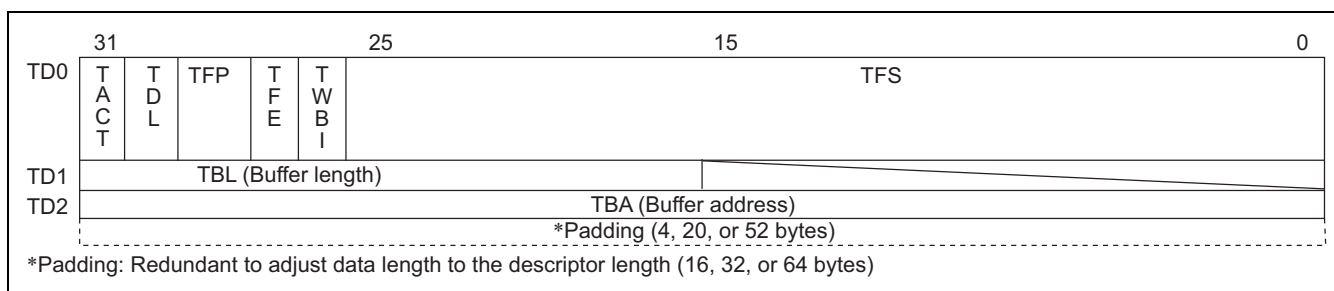
In this situation, the CPU should clear the interrupt source and reset the receive descriptor correctly.

If the valid receive descriptor is set before a receive FIFO overflow occurs, a frame reception can be continued without data loss.

**37.8.2 Transmit Descriptors**

Figure 37.13 shows a transmit descriptor format.

If 1 to 16 bytes is specified as the transmit buffer length, the transmit buffer address should be aligned on a 32-byte boundary. Note that correct operation cannot be guaranteed if 0 byte is specified as the transfer buffer length.



**Figure 37.13 Transmit Descriptor Format**

**(1) Transmit Descriptor 0 (TD0)**

Table 37.7 shows a definition of transmit descriptor 0. (A bit to be written back to is underlined.)

**Table 37.7 Definition of Transmit Descriptor 0**

Bit	Bit Name	Initial Value	R/W	Definition
<u>31</u>	TACT	Undefined	R/W	Descriptor Valid Indicates that the corresponding descriptor is valid. This bit is set to 1 by a driver, and reset (cleared to 0) by this logic core when a frame transmission has been completed or a frame transmission has been aborted for some reason.
30	TDL	Undefined	R/W	Descriptor Ring End Set to 1 to indicate that the corresponding descriptor is an end of the transmit descriptor ring.
29, 28	TFP	Undefined	R/W	Position in a Frame 11: Indicate that the information in this descriptor includes one whole frame. This field should be set to 11.
<u>27</u>	TFE	Undefined	R/W	Transmit Frame Error Set to 1 to indicate that an error occurs in TFS.
26	TWBI	Undefined	R/W	Write-Back Completion Interrupt Request (Enabled according to CXR18 settings) 0: nop 1: Requests an interrupt after a write-back to this descriptor has been completed.
<u>25 to 0</u>	TFS	Undefined	R/W	Transmit Frame Status Bit 8: Set to 1 to indicate that the underflow occurs shown as an abort signal is set to 1 during transmission of the frame, (TFE set source). Bits 7 to 0: Set to 1 to indicate that a corresponding bit among TINT8 to TINT1 is set to 1.

**(2) Transmit Descriptor 1 (TD1)**

Table 37.8 shows a definition of transmit descriptor 1.

**Table 37.8 Definition of Transmit Descriptor 1**

Bit	Bit Name	Initial Value	R/W	Definition
31 to 16	TBL	Undefined	R/W	Buffer length: Indicates the valid byte count in the target transmit buffer.
15 to 0	—	Undefined	R/W	Reserved

**(3) Transmit Descriptor 2 (TD2)**

Table 37.9 shows a definition of transmit descriptor 2.

**Table 37.9 Definition of Transmit Descriptor 2**

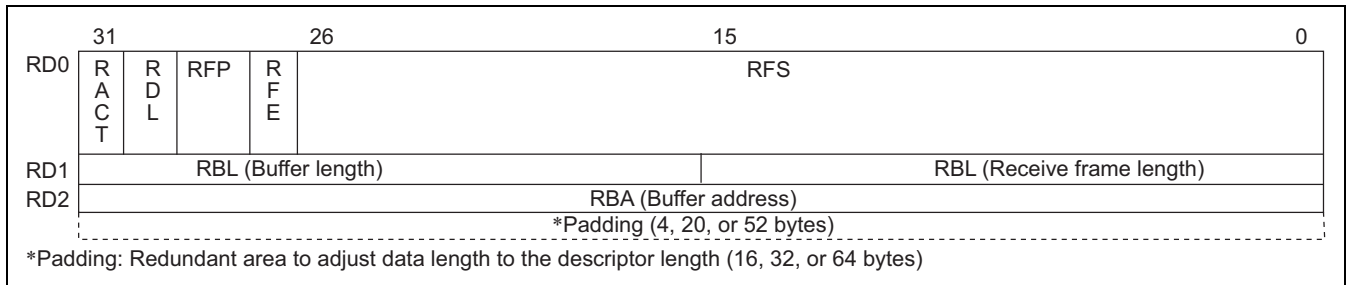
Bit	Bit Name	Initial Value	R/W	Definition
31 to 0	TBA	Undefined	R/W	Buffer address: Indicates the start address of the transmit buffer.



### 37.8.3 Receive Descriptors

Figure 37.14 shows a receive descriptor format.

A receive buffer address specified by a receive descriptor should be aligned on a 32-byte boundary. Note that correct operation cannot be guaranteed if 0 byte is specified as the receive buffer length (RBL).



**Figure 37.14 Receive Descriptor Format**

**(1) Receive Descriptor 0 (RD0)**

Table 37.10 shows a definition of receive descriptor 0. (A bit to be written back to is underlined.)

**Table 37.10 Definition of Receive Descriptor 0**

Bit	Bit Name	Initial Value	R/W	Definition
<u>31</u>	RACT	Undefined	R/W	Descriptor Valid Indicates that the corresponding descriptor is valid. This bit is set to 1 by a driver, and reset (cleared to 0) by this logic core when a frame transmission has been completed or the receive buffers have become full.
30	RDL	Undefined	R/W	Descriptor Ring End Set to 1 to indicate that the corresponding descriptor is an end of the receive descriptor ring.
<u>29, 28</u>	RFP	Undefined	R/W	Position in a Frame 10: Indicate that the information in this descriptor includes the start of a frame. 11: Indicate that the information in this descriptor includes one whole frame. 01: indicate that the information in this descriptor includes the end of a frame. 00: Indicate that the information in this descriptor is other than above.
<u>27</u>	RFE	Undefined	R/W	Receive Frame Error Set to 1 to indicate that an error occurs in RFS.
<u>26 to 0</u>	RFS	Undefined	R/W	Receive Frame Status Bit 9: Set to 1 to indicate that an aborted frame is written back due to a receive FIFO overflow (FRE setting source). Bit 8: Set to 1 to indicate that an abort signal is set to 1 during frame reception (RFE set source). Bits 7 to 0: Set to 1 to indicate that a corresponding bit among RINT8 to TINT1 is set to 1 (RFE setting sources specified by CXR7).

**(2) Receive Descriptor 1 (RD1)**

Table 37.11 shows a definition of receive descriptor 1. (A bit to be written back to is underlined.)

**Table 37.11 Definition of Receive Descriptor 1**

Bit	Bit Name	Initial Value	R/W	Definition
31 to 16	RBL	Undefined	R/W	Buffer length Indicate the byte count in the target receive buffer. The buffer length should be specified by 32 bytes x n.
<u>15 to 0</u>	RFL	Undefined	R/W	Receive Frame Length Indicate the receive frame length (bytes) stores in the receive buffer. This receive frame length does not include the number of bytes for padding specified in the CXRS5. This receive frame length is written back in the receive descriptor that includes the last of a frame.

**(3) Receive Descriptor 1 (RD2)**

Table 37.12 shows a definition of receive descriptor 2.

**Table 37.12 Definition of Receive Descriptor 2**

Bit	Bit Name	Initial Value	R/W	Definition
31 to 0	RBA	Undefined	R/W	Buffer Address These bits indicate the start address of a receive buffer. The buffer address should be aligned on a 32-byte boundary.

**37.8.4 Error Detection and Report**

The error sources are classified into two types: those detected by the HDMAC and those detected and reported by the feLic.

Each error is described below. If an error is detected, the detected error is indicated in the status register (CXR5) and an interrupt signal is output.

**(1) Error Sources Detected by the HDMAC****(a) Descriptor Depletion**

If no descriptor whose descriptor valid bit is set can be detected during frame reception, a receive descriptor depletion error occurs and the R bit in the receive activation register (CXR2) is reset to complete the receive processing.

**(b) External FIFO Underflow/Overflow**

If a transmit FIFO becomes empty during frame transmission, an underflow error occurs because there is no data to be transmitted.

If a receive FIFO becomes full during frame reception, an overflow error occurs because the next receive data cannot be stored in the receive FIFO.

If an underflow error in a transmit FIFO or an overflow error in a receive FIFO is detected, it is indicated in the status register (CXR5).

**(2) Error Sources Detected and Reported by the Function Core (feLic)****(a) Transmit Interrupt**

Interrupt sources detected by the function core (feLic) during frame transmission are reported to the transmit descriptor of the corresponding frame and status register (CXR5) as TINT1 to TINT8, or transmit abort detect (TABT).

**(b) Receive Interrupt**

Interrupt sources detected by the function core (feLic) during frame reception are reported to the receive descriptor of the corresponding frame and status register (CXR5) as RINT1 to RINT8, and receive abort detect (RABT).

**(c) MPORT Interrupt (MINT)**

If an error is detected other than during transmission or reception, it is reported as an MPORT interrupt.

For details on TINT, RINT, and MINT bits, see the Function Core Function Specifications.

**(3) Error Log Information**

This logic core provides the following log collection registers.

1. Discarded frame counter register (CXR8)
2. Transmit FIFO underflow counter register (CXR13)
3. Receive FIFO overflow counter register (CXR14)

### 37.8.5 Firmware/Software Interface

#### (1) Interrupts

Interrupts sources in this logic module are as follows.

1. RINT1 to RINT8
2. TINT1 to TINT8
3. Receive FIFO overflow
4. Receive descriptor depletion
5. Frame receive completion
6. Transmit FIFO underflow
7. Transmit descriptor depletion (not used)
8. Frame transmit completion
9. M port interrupt
10. DMA error
11. Receive frame count overflow
12. Receive abort detection
13. Transmit abort detection
14. External EXIN signal assertion detection (not used)
15. Transmit descriptor write-back

The above interrupt sources are indicated in the status register (CXR5). An interrupt source (other than M port interrupt signal (MINT) bit) can be reset by writing 1 to the corresponding bit in the CXR5 register. An M port interrupt signal (MINT) can be reset by resetting the corresponding source in the function core. The above interrupt sources can be separately masked by setting the interrupt mask register (CXR6).

### 37.9 feLic Function Specifications

RZ/G1H	RZ/G1N
RZ/G1M	RZ/G1E

#### 37.9.1 Configuration

Figure 37.15 shows a block diagram of feLic.

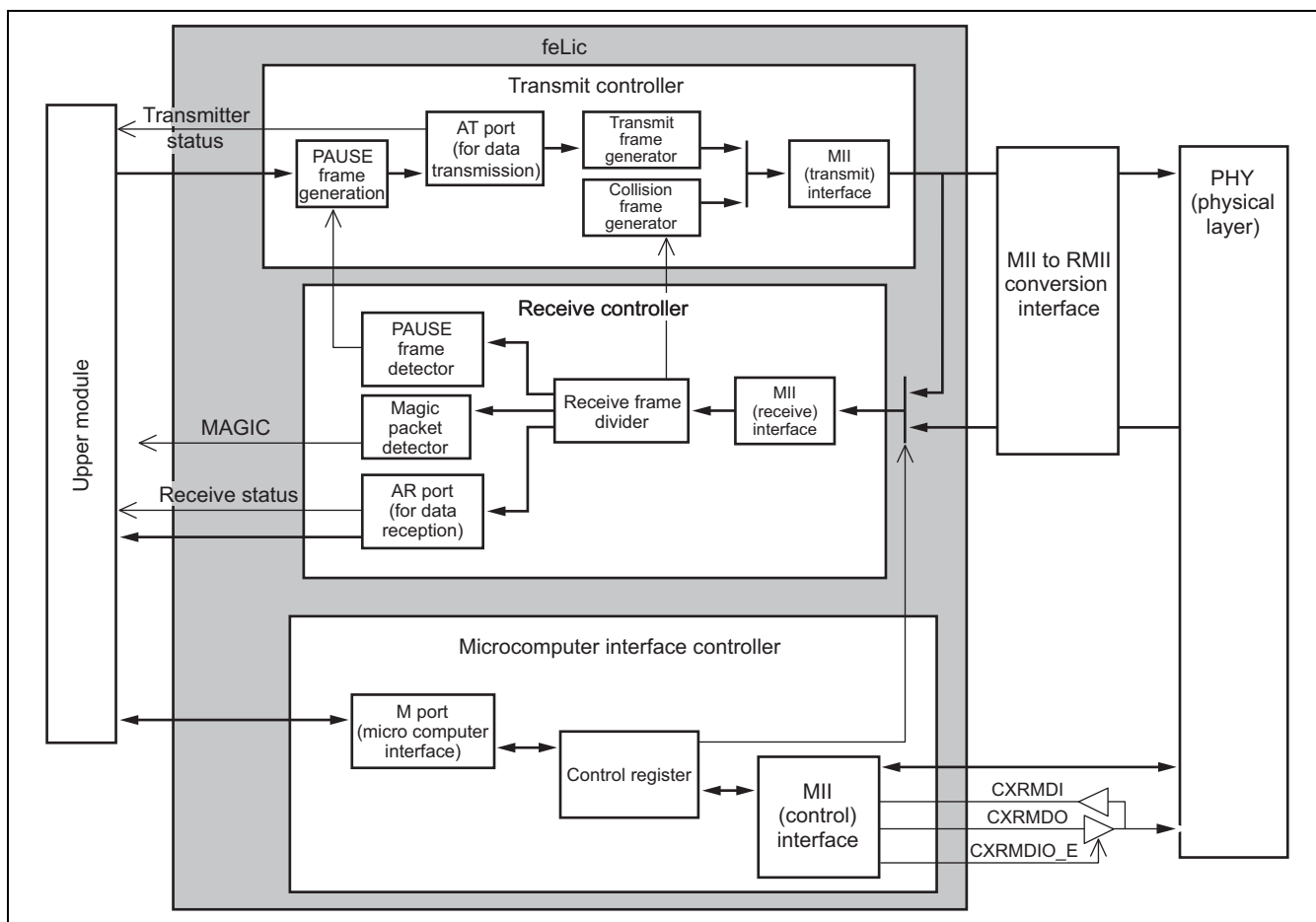


Figure 37.15 feLic Block Diagram

#### 37.9.2 feLic Function

##### (1) Transmit Controller

The transmit controller assembles data received from AT port into the IEEE802.3 format frames, and transmits them via the MII interface.

The main functions of the transmit controller are listed below.

1. Assembles data received from the AT port into the IEEE802.3 format frames and transmits them.
2. Performs CRC calculation and adds it to the frame.
3. Retransmits frames (up to 15 times) when a collision occurs.
4. Provides the MII interface function conforming to the IEEE802.3u.
5. Performs serial and parallel conversion according to the PHY chip speed.
6. Provides transmit frame data padding function.

7. Generates a PAUSE frame.

## (2) Receive Controller

Upon receiving a frame via the MII interface, the receive controller checks the frame address to see if the address matches the self-node; it also checks CRC and the frame length of the data and transfers the data to the AR port.

The main functions of the receive controller are listed below.

1. Checks the format of the received frame header.
2. Checks the CRC and frame length of the received frame data.
3. Transfers frames addressed to itself, multicast frames, and broadcast frames to the AR port.
4. Provides the MII interface function conforming to the IEEE802.3u.
5. Performs serial and parallel conversion according to the PHY chip speed.
6. Monitors a magic packet.
7. Analyzes a PAUSE frame.

## (3) Microcomputer Interface Controller

The microcomputer interface controller incorporates a function to interface to the upper microprocessor. The data width of the M port is 32 bits. The M port operates synchronously with the external clock. The upper microprocessor controls the registers in this microcomputer interface controller block and the registers in PHY via the MII interface.

The main functions of the microcomputer interface controller are listed below.

1. Controls the operation of transmitter and receiver.
2. Accesses the PHY registers via the serial bus.

## (4) Magic Packet Monitor Function

The receive controller monitors the magic packet and report the magic packet detection to an external device in magic packet monitor mode. This function becomes effective by the MPM bit in the CXR20 register. When the magic packet is detected, "ETH\_MAGIC" signal that is an output is asserted and the CXR21 register is updated. Their detecting functions are explained as follows.

### (a) Assertion by the ETH\_MAGIC signal

ETH\_MAGIC signal that is an output signal of the feLic is asserted synchronizing with the rising edge of the received clock from PHY. Detection of the magic packet can be informed to external circuits by using this signal. The ETH\_MAGIC signal is negated by the hardware reset and the software reset of the HDMAC/feLic using CXR0 register.

### (b) Assertion by the CXR21 register

Updating CXR21 can assert as software interruption. The detecting information is cleared by writing a 1 to the corresponding bit. Note that if a magic packet is received again, CXR21 register is not updated while the ETH\_MAGIC signal is asserting. Set the feLic again after clearing by the procedure described (1).

## (5) Transmit and Receive Status Statistical Function

The interrupt source signals (TINT/RINT) to be output to the upper modules can be counted and referenced as statistical information by accessing a register via the M port.

The interrupt source signal counting starts after reset (includes a soft reset by CXR0 register) and the count value can be cleared only by a write access.

## (6) Flow Control Conforming to IEEE802.3

As the flow control during full-duplex operation, the flow control conforming to IEEE802.3x is supported. Transmission of a PAUSE frame used in flow control is performed in the following methods. These methods can be used by mutually combining.

### (a) Automatic PAUSE Frame Transmission

A PAUSE frame is transmitted automatically by asserting the ARBSY signal. Note that as the Timer value included in the PAUSE frame, the value set in the automatic PAUSE parameter setting register (see CXR71) is used. If the ARBSY signal is not negated when the time indicated by the Timer value has passed after transmitting a PAUSE frame, a PAUSE frame is transmitted again. The number of PAUSE frame re-transmissions (upper limit) can be specified from 1 to 65535 times by setting the PAUSE frame retransmit count setting register (CXR81). If the number of PAUSE frame re-transmissions reaches the upper limit, the following PAUSE frame re-transmissions will not be performed.

Transmission can be restarted when ARBSY signal is negated once and then asserted again thus resetting the PAUSE frame re-transmission counter (CXR82). In addition, it is possible not to set the upper limit of the re-transmissions (unlimited).

### (b) Manual PAUSE Frame Transmission

This method can send the PAUSE frame by calling of software. Set the Timer value to the CXR72 register to sending the PAUSE frame. It is sent just one time (one frame) in this method.

### (c) PAUSE Timer Value

For the PAUSE frame whose Timer value is 0, it is possible to enable or disable the PAUSE frame control.

- During transmission
  - When control of a PAUSE frame whose Timer value is 0 is enabled, a PAUSE frame with Timer value 0 is transmitted if the ARBSY signal is negated before the time indicated by the Timer value has passed.
  - When control of a PAUSE frame whose Timer value is 0 is disabled, the next frame will not be transmitted until the time indicated by the Timer value has passed.
- During reception
  - When control of a PAUSE frame whose Timer value is 0 is enabled, a PAUSE frame is set in the receive wait counter even if the time indicated by Timer value is 0. (The receive wait state is cancelled.)
  - When control of a PAUSE frame whose Timer value is 0 is disabled, the PAUSE frame is discarded if the time indicated by Timer value is 0.

### (d) PAUSE Frame Reception

When a PAUSE frame is received, this logic function suspends transmission of the next frame until the time indicated by the Timer value has passed. However, transmission of the frame being transmitted continues. A number of the PAUSE frame receiving is counted to CXR80.

## (7) Back-Pressure Flow Control

As the flow control during half-duplex operation, the back-pressure flow control is supported. This method generates a pseudo collision (transmits a collision frame) to stop the frame reception if the remaining space in the FIFO is not sufficient when the frame is received. This method does not refer to the DA.

### 37.9.3 Detailed Description of Transmit and Receive Controllers

#### (1) Transmit Controller

The transmit controller assembles the transmit data from the AT port into the frames based on the appropriate format and transmits them via the MII interface. Here, an error may occur according to the status of the communication lines. If an error of TINT1 to RINT8 occurs, the transmission is aborted and the error source is reported to the upper block using the abort signal (ARABT). If the transmission is completed normally, it is reported via the transmit completion signal (ATCOMP).

The conditions of generating each error source and operation are described below.

- TINT1: Transmit timeout  
When a collision occurs (the COL signal assertion) during frame transmission, the transmission is retried after the back-off time has passed. A transmit timeout is generated if a collision occurs again during the 15th transmission retry.
- TINT2: Collision detection during frame transmission  
Generated if a delay collision described in the IEEE802.3 standard occurs.  
Description in the standard: It is regarded as a delay collision if a collision occurs after the collision window at 512-bit time from the transmission start.
- TINT3: Carrier loss during frame transmission  
Generated when a carrier is lost (the CRS signal is negated) during frame transmission.
- TINT4: Carrier not detected  
Generated when a carrier is not detected (the CRS signal is not asserted) during preamble field transmission.
- TINT5: Not assigned
- TINT6: Not assigned
- TINT7: Not assigned
- TINT8: Not assigned

If any transmit error described above occurs, the feLic enters the wait state for the next frame transmission request and starts the next frame transmission when the next frame transmission is requested.

#### (2) Receive Controller

The receive controller transfers a frame received via the MII interface to the AR port. Here, an error may occur according to the status of the communication lines. If an error of RINT1 to RINT4 occurs, the reception is aborted and the error source is reported to the upper block using the abort signal (ARABT). RINT5 indicates that a fractional number bit error has occurred. Note, however, that a frame with an RINT5 error but with no CRC error can be received normally. A frame with RINT8 can also be received normally. RINT8 is an error source allowing normal frame reception and is reported by using the receive completion signal (ARCOMP) when the frame destination address is a multicast address.

The conditions of generating each error source and operation are described below.

- RINT1: CRC error  
Generated when an error is detected in the FCS field in the receive frame.
- RINT2: Frame receive error  
Reported when the RX\_ER signal in the MII interface is asserted during frame reception. For details on the RX\_ER signal assertion, see the Data Book of the PHY to be connected.
- RINT3: Frame length error  
Reported when the receive frame length is less than 64 bytes.
- RINT4: Frame length error



Reported when the receive frame length exceeds the value specified in the CXR2A register. An excess of data field over the specified frame length is discarded in the feLic and will not be transferred to the upper block.

- RINT5: Fractional number bit error

Reported when the received frame length is not the multiple of an octet. In this case, the last 1 to 4 octets in the data field will not be transferred to the upper block.

- RINT6: Not assigned
- RINT7: Not assigned

- RINT8: Multicast frame reception

Reported when the frame destination address is a multicast address. This error source is reported with a receive completion signal only when other error source is not generated.

If any receive error described above occurs, the feLic enters the wait state for the next frame reception and starts the next frame reception when the next frame is received.

### 37.10 MII-RMII Interface Conversion

RZ/G1H	RZ/G1N
RZ/G1M	RZ/G1E

This LSI supports an RMII interface. The RMII signals are generated by converting the MII signals in the MII-RMII conversion circuit.

#### (1) Clock

ETH\_REFCLK (50 MHz) from the RMII interface is divided and ET\_TX-CLK/ET\_RX-CLK (25 MHz or 2.5 MHz) is output.

#### (2) Reception

Waveforms received from the RMII interface are converted to MII waveforms and output (10 Mbps or 100 Mbps). Illegal carrier detection signal received from the RMII interface is converted to MII signal and output. ETH\_RX\_ER signal received from the RMII interface is converted to MII interface signal and output.

Note: Illegal carrier detection is not generated from preamble detection to reception completion.

#### (3) Transmission

Transmit waveforms from the MII interface is converted to the RMII interface waveforms and output (10 Mbps or 100 Mbps). The collision signal, ET\_COL, is generated by AND operation of the ET\_CRS and ET\_TX-EN signals.

#### (4) Full-Duplex/Half-Duplex Selection

In full-duplex transfer mode, the assertion of the COL is suppressed. Figure 37.16 shows a schematic of the conversion circuit.

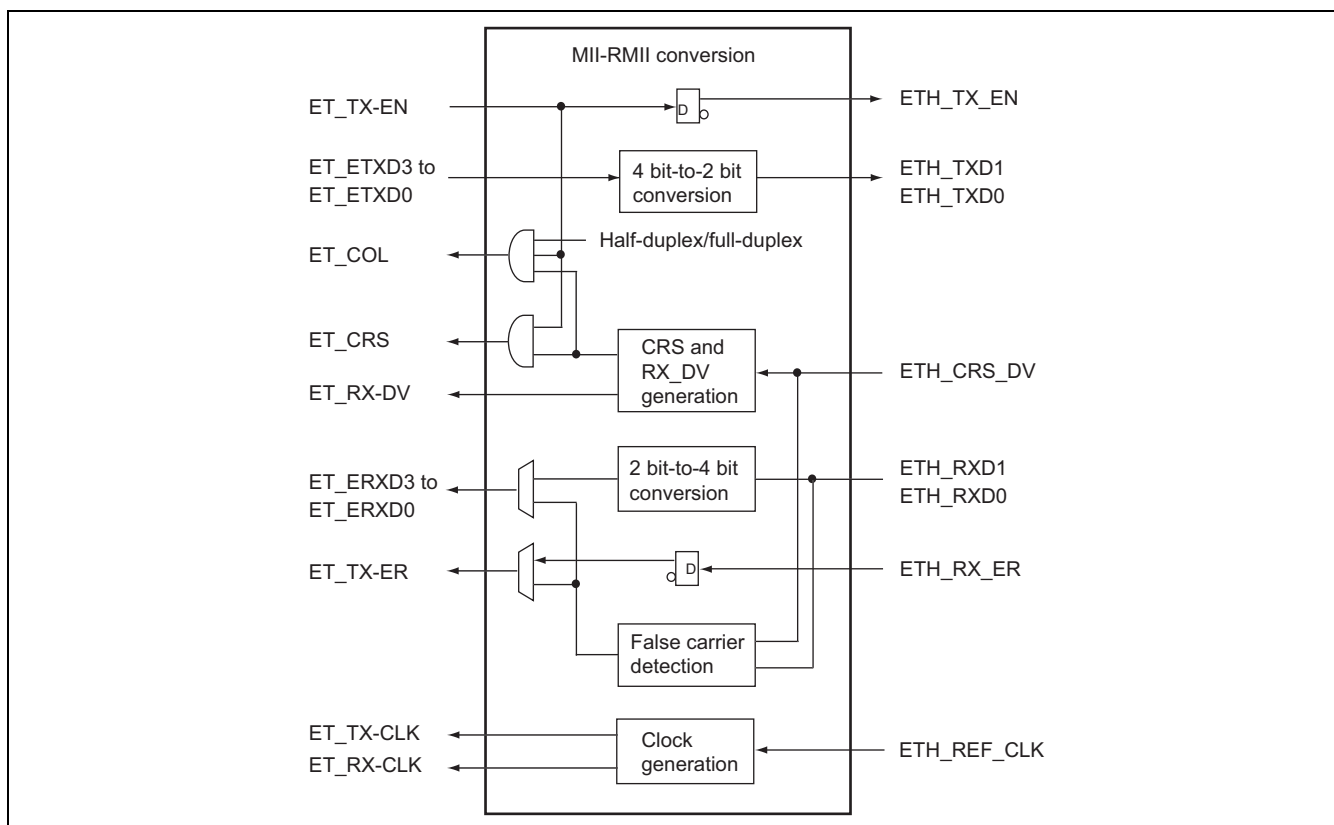


Figure 37.16 MII-RMII Conversion Circuit

## 37A. EthernetAVB

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

### 37A.1 Overview

The EthernetAVB includes an Ethernet controller (E-MAC) that conforms to the definition of the MAC (Media Access Control) layer for Ethernet in the IEEE 802.3 standard.

When connected with a physical-layer LSI chip (PHY-LSI) that complies with the standard, the E-MAC is able to transmit and receive Ethernet (IEEE 802.3) frames. The E-MAC has a single MAC layer interface.

The EthernetAVB has a dedicated direct memory access controller (AVB-DMAC) for transferring transmitted Ethernet frames to and received Ethernet frames from respective storage areas in the URAM at high speed.

The AVB-DMAC is compliant with the following three standards formulated for IEEE 802.1BA: the IEEE 802.1AS timing and synchronization protocol, the IEEE 802.1Qav real-time transfer, and the IEEE 802.1Qat stream reservation protocol.

In this section, URAM refers to the local RAM and external memory.

Descriptors are recommended to be located at addresses H'00 EE0E 8000 to H'00 EE0E BFFF.

#### 37A.1.1 Specifications (Functions)

Table 37A.1 lists the specifications of the EthernetAVB module.

**Table 37A.1 Specifications (Functions)**

Item	Description
Protocol	Flow control conforming with the IEEE 802.3x standard
Data transmission and reception	Transmission and reception of Ethernet (IEEE 802.3) frames
Transfer speed	Supports transfer at 100 and 1000 Mbps
Mode	Full-duplex mode
Interface	Supports the IEEE 802.3 standard MII (Media Independent Interface) and GMII (Gigabit Media Independent Interface)
Summary of the EthernetAVB function	An intelligent frame separation DMAC (AVB-DMAC) conforming with the following standards stipulated for IEEE 802.1BA: IEEE 802.1AS (time synchronization protocol) IEEE 802.1Qav (real-time transfer) IEEE 1722 (AVTP presentation timestamp) IEEE 802.1Qat is supported by software. Descriptor management system Identification and sorting of frame data, and extraction and gathering of valid data Controllable interrupt frequency (reducing the load on the CPU)
Magic Packet™	Detection of Magic Packets™* and output of a detected signal

Note: \* Magic Packet™ is a trademark of Advanced Micro Devices, Inc.

### 37A.1.2 Block Diagram

Figure 37A.1 is a block diagram of the EthernetAVB.

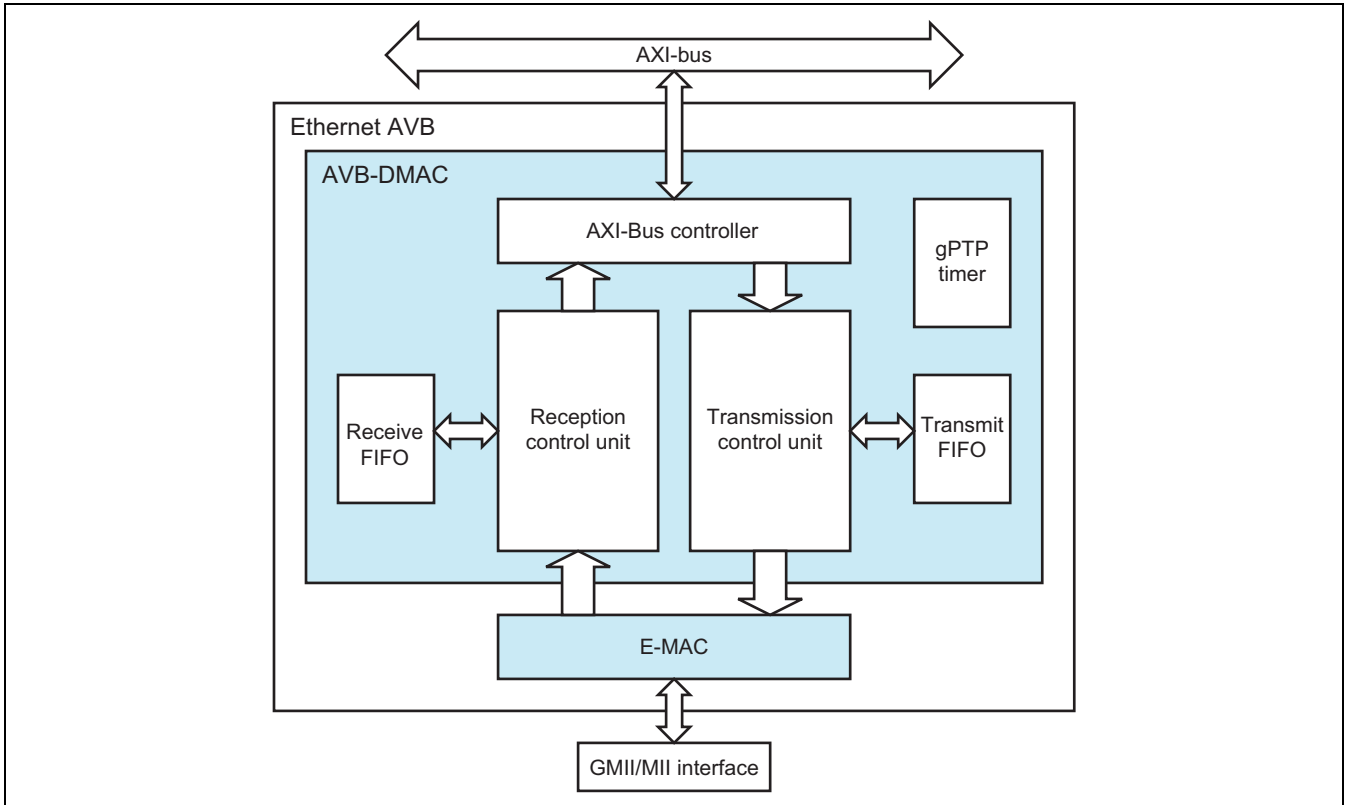


Figure 37A.1 Block Diagram of EthernetAVB

**37A.1.3 Input/Output Pins**

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

Table 37A.2 lists the pins for use by EthernetAVB.

**Table 37A.2 Pin Configuration**

Pin Name	I/O	Function
AVB_TXD[7:0]	O	Transmit data signal
AVB_TX_EN	O	Transmit data enable signal
AVB_RXD[7:0]	I	Receive data signal
AVB_RX_DV	I	Receive data enable signal
AVB_TX_CLK	I	Transmit clock signal
AVB_RX_CLK	I	Receive clock signal
AVB_TX_ER	O	Transmit error signal
AVB_RX_ER	I	Reception error signal
AVB_GTX_CLK	O	GMII transmit clock signal
AVB_GTXREFCLK	I	GMII reference clock signal
AVB_MDC	O	Management information transfer clock signal
AVB_MDIO	I/O	Management information transmit/receive data
AVB_CRD	I	Carrier detection signal
AVB_COL	I	Collision detection signal
AVB_LINK	I	Link status signal
AVB_MAGIC	O	Magic packet signal
AVB_PHY_INT	I	PHY interrupt signal

## 37A.2 Register Descriptions

RZ/G1H	RZ/G1N
RZ/G1M	RZ/G1E

Tables 37A.3 and 37A.4 lists the EthernetAVB related registers and their configurations.

**Table 37A.3 Configuration of AVB-DMAC-related Registers**

Name	Abbreviation	R/W	Address	Initial Value	Access Size	RZ/G Series Products			
						RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
AVB-DMAC mode register	CCC	R/W	H'E680 0000	H'0000 0000	32	√	√	√	√
Descriptor base address table register	DBAT	R/W	H'E680 0004	H'0000 0000	32	√	√	√	√
Descriptor base address load request register	DLR	R/W	H'E680 0008	H'003F FFFF	32	√	√	√	√
AVB-DMAC status register	CSR	R	H'E680 000C	H'0000 0001	32	√	√	√	√
Current descriptor address register q (q = 0 to 21)	CDARq	R	H'E680 0010 + q × 4	H'0000 0000	32	√	√	√	√
Error status register	ESR	R	H'E680 0088	H'0000 0000	32	√	√	√	√
Receive configuration register	RCR	R/W	H'E680 0090	H'1800 0000	32	√	√	√	√
Receive queue configuration register i (i = 0 to 4)	RQCi	R/W	H'E680 0094 + i × 4	H'0000 0000	32	√	√	√	√
Receive padding configuration register	RPC	R/W	H'E680 00B0	H'0000 0100	32	√	√	√	√
Unread frame counter warning level register	UFCW	R/W	H'E680 00BC	H'0000 0000	32	√	√	√	√
Unread frame counter stop level register	UFCS	R/W	H'E680 00C0	H'0000 0000	32	√	√	√	√
Unread frame counter register i (i = 0 to 4)	UFCVi	R	H'E680 00C4 + i × 4	H'0000 0000	32	√	√	√	√
Unread frame counter decrement register i (i = 0 to 4)	UFCDi	R/W	H'E680 00E0 + i × 4	H'0000 0000	32	√	√	√	√
Separation filter offset register	SFO	R/W	H'E680 00FC	H'0000 0000	32	√	√	√	√
Separation filter pattern register i (i = 0 to 31)	SFPi	R/W	H'E680 0100 + i × 4	H'0000 0000	32	√	√	√	√
Separation filter mask register i (i = 0, 1)	SFMi	R/W	H'E680 01C0 + i × 4	H'0000 0000	32	√	√	√	√
Transmit configuration register	TGC	R/W	H'E680 0300	H'0022 2200	32	√	√	√	√
Transmit configuration control register	TCCR	R/W	H'E680 0304	H'0000 0000	32	√	√	√	√
Transmit status register	TSR	R	H'E680 0308	H'0000 0000	32	√	√	√	√
Time stamp FIFO access register 0	TFA0	R	H'E680 0310	H'0000 0000	32	√	√	√	√
Time stamp FIFO access register 1	TFA1	R	H'E680 0314	H'0000 0000	32	√	√	√	√
Time stamp FIFO access register 2	TFA2	R	H'E680 0318	H'0000 0000	32	√	√	√	√
CBS increment value register c (c = 0, 1)	CIVRc	R/W	H'E680 0320 + c × 4	H'0000 0001	32	√	√	√	√
CBS decrement value register c (c = 0, 1)	CDVRc	R/W	H'E680 0328 + c × 4	H'FFFF FFFF	32	√	√	√	√

Name	Abbreviation	R/W	Address	Initial Value	Access Size	RZ/G Series Products			
						RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
CBS upper limit register c (c = 0, 1)	CULc	R/W	H'E680 0330 + c × 4	H'7FFF FFFF	32	√	√	√	√
CBS lower limit register c (c = 0, 1)	CLLc	R/W	H'E680 0338 + c × 4	H'8000 0001	32	√	√	√	√
Descriptor interrupt control register	DIC	R/W	H'E680 0350	H'0000 0000	32	√	√	√	√
Descriptor interrupt status register	DIS	R/W	H'E680 0354	H'0000 0000	32	√	√	√	√
Error interrupt control register	EIC	R/W	H'E680 0358	H'0000 0000	32	√	√	√	√
Error interrupt status register	EIS	R/W	H'E680 035C	H'0000 0000	32	√	√	√	√
Receive interrupt control register 0	RIC0	R/W	H'E680 0360	H'0000 0000	32	√	√	√	√
Receive interrupt status register 0	RIS0	R/W	H'E680 0364	H'0000 0000	32	√	√	√	√
Receive interrupt control register 1	RIC1	R/W	H'E680 0368	H'0000 0000	32	√	√	√	√
Receive interrupt status register 1	RIS1	R/W	H'E680 036C	H'0000 0000	32	√	√	√	√
Receive interrupt control register 2	RIC2	R/W	H'E680 0370	H'0000 0000	32	√	√	√	√
Receive interrupt status register 2	RIS2	R/W	H'E680 0374	H'0000 0000	32	√	√	√	√
Transmit interrupt control register	TIC	R/W	H'E680 0378	H'0000 0000	32	√	√	√	√
Transmit interrupt status register	TIS	R/W	H'E680 037C	H'0000 0000	32	√	√	√	√
Interrupt summary status register	ISS	R	H'E680 0380	H'0000 0000	32	√	√	√	√
gPTP configuration control register	GCCR	R/W	H'E680 0390	H'0000 003C	32	√	√	√	√
gPTP maximum transit time register	GMTT	R/W	H'E680 0394	H'0000 0000	32	√	√	√	√
gPTP presentation time comparison register	GPTC	R/W	H'E680 0398	H'0000 0000	32	√	√	√	√
gPTP timer increment register	GTI	R/W	H'E680 039C	H'0000 0001	32	√	√	√	√
gPTP timer offset register i (i = 0 to 2)	GTOi	R/W	H'E680 03A0 + i × 4	H'0000 0000	32	√	√	√	√
gPTP interrupt control register	GIC	R/W	H'E680 03AC	H'0000 0000	32	√	√	√	√
gPTP interrupt status register	GIS	R/W	H'E680 03B0	H'0000 0000	32	√	√	√	√
gPTP timer capture register i (i = 0 to 2)	GCTi	R/W	H'E680 03B8 + i × 4	H'0000 0000	32	√	√	√	√

**Table 37A.4 Configuration of E-MAC-related Registers**

Name	Abbreviation	R/W	Address	Initial Value	Access Size	RZ/G Series Products			
						RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
E-MAC mode register	ECMR	R/W	H'E680 0500	H'0000 0000	32	√	√	√	√
Receive frame length register	RFLR	R/W	H'E680 0508	H'0000 0000	32	√	√	√	√
E-MAC status register	ECSR	R/W	H'E680 0510	H'0000 0000	32	√	√	√	√
E-MAC interrupt permission register	ECSIPR	R/W	H'E680 0518	H'0000 0000	32	√	√	√	√
PHY interface register	PIR	R/W	H'E680 0520	H'0000 0000	32	√	√	√	√
PHY Status Register	PSR	R	H'E680 0528	H'0000 0000	32	√	√	√	√
PHY_INT Polarity Register	PIPR	R/W	H'E680 052C	H'0000 0000	32	√	√	√	√
Manual PAUSE frame register	MPR	R/W	H'E680 0558	H'0000 0000	32	√	√	√	√
PAUSE frame transmit counter	PFTCR	R	H'E680 055C	H'0000 0000	32	√	√	√	√
PAUSE frame receive counter	PFRCCR	R	H'E680 0560	H'0000 0000	32	√	√	√	√
EthernetAVB Mode Register	GECMR	R/W	H'E680 05B0	H'0000 0000	32	√	√	√	√
E-MAC address high register	MAHR	R/W	H'E680 05C0	H'0000 0000	32	√	√	√	√
E-MAC address low register	MALR	R/W	H'E680 05C8	H'0000 0000	32	√	√	√	√
CRC error frame receive counter register	CEFCR	R/W	H'E680 0740	H'0000 0000	32	√	√	√	√
Frame receive error counter register	FRECR	R/W	H'E680 0748	H'0000 0000	32	√	√	√	√
Too-short frame receive counter register	TSFRCR	R/W	H'E680 0750	H'0000 0000	32	√	√	√	√
Too-long frame receive counter register	TLFRCR	R/W	H'E680 0758	H'0000 0000	32	√	√	√	√
Residual-bit frame receive counter register	RFCR	R/W	H'E680 0760	H'0000 0000	32	√	√	√	√
Multicast address frame receive counter register	MAFCR	R/W	H'E680 0778	H'0000 0000	32	√	√	√	√



### 37A.2.1 AVB-DMAC Mode Register (CCC)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

The CCC register specifies the operating mode of the AVB-DMAC.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	LBME	—	—	—	—	—	—	CSEL[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	DTSR	—	—	—	—	—	—	OPC[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

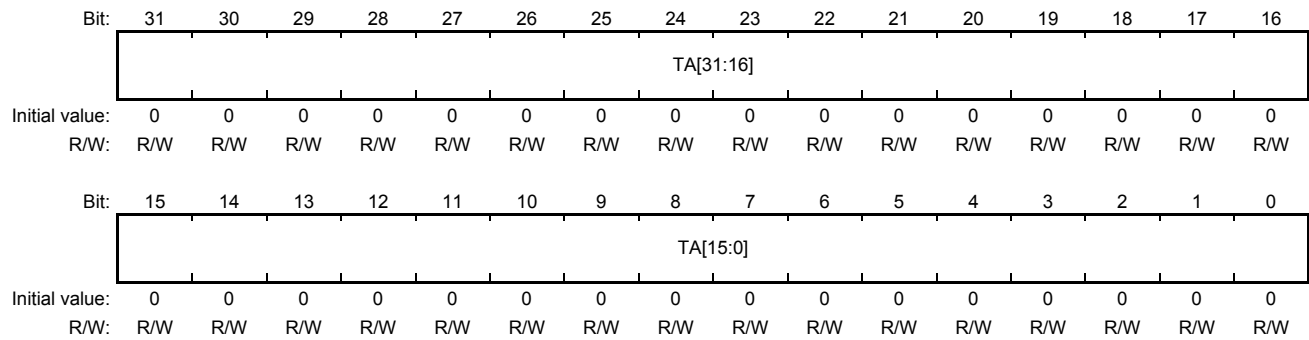
Bit	Bit Name	Initial Value	R/W	Description
31 to 25	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
24	LBME	0	R/W	Loopback Mode Enable This bit enables loopback mode. In loopback mode, the transmission lines are internally connected to the reception lines. When loopback mode is to be used, the Ethernet transmission clock must be supplied to the GMII or MII interface. A received clock signal is not required. Writing to this bit is only possible when the current operating mode is configuration mode. 0: Normal operation 1: Loopback mode is enabled. Note: Data for transmission are still output normally. To eliminate effects on external modules, pin control should be applied to block the output of data.
23 to 18	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
17, 16	CSEL[1:0]	00	R/W	gPTP Clock Select These bits select the clock source for the gPTP timer. Writing to these bits is only possible when the current operating mode is configuration mode. 00: Setting prohibited 01: High-speed peripheral bus clock 10: Ethernet transmission clock (125 MHz at 1000 Mbps, 25 MHz at 100 Mbps) 11: GMII reference clock (AVB_GTXREFCLK)
15 to 9	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.

Bit	Bit Name	Initial Value	R/W	Description
8	DTSR	0	R/W	<p>Data Transmission Suspend Request</p> <p>This bit can suspend access to the URAM.</p> <p>The access is suspended on completion of the transfer of the AXI transaction currently being transferred.</p> <p>This function disables access to the URAM without affecting normal operation of the AVB-DMAC. Use this bit when exclusive control over the contents of the URAM is necessary, for example, in checking its integrity.</p> <p>Note that the transmission and reception queues are not processed while access is suspended.</p> <p>Change neither the AVB-DMAC settings nor the mode while access is suspended.</p> <p>0: Normal operation 1: Requests suspension</p>
7 to 2	—	All 0	R/W	<p>Reserved</p> <p>These bits are read as 0. The write value should be 0.</p>
1, 0	OPC[1:0]	00	R/W	<p>Operating Mode Configuration</p> <p>These bits specify the operating mode.</p> <p>For the operating modes, see section 37A.3.1.1, Operating Modes.</p> <p>Writing to these bits is possible in any of the operating modes, but should not be done after the application system has issued a Power Off request.</p> <p>00: Reset mode 01: Configuration mode 10: Operation mode 11: Reserved</p>

### 37A.2.2 Descriptor Base Address Table Register (DBAT)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

The DBAT register specifies the base address of the descriptor table in the URAM. For the structure of this table, see section 37A.3.3, Descriptors. Writing to this bit is only possible when the current operating mode is configuration mode.



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	TA[31:0]	H'0000 0000	R/W	Descriptor Base Table Address Base address of the descriptor table in the URAM Note: The setting of this bit must be a multiple of four (i.e. bit 0 and bit 1 must be set to 0).

### 37A.2.3 Descriptor Base Address Load Request Register (DLR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

The DLR register is used to issue a request to load the values from the current descriptor address register q (CDARq) for each queue to the descriptor base address table register (DBAT).

Setting a bit to 1 issues a request for loading the descriptor base address for the queue q. If transfer is currently in progress, loading is executed on completion of transfer for the current frame. Completion of loading leads to automatic setting of the corresponding bit to 0.

For the transmission queues, base address load requests are executed even while fetching is in progress (the transmit start request bit in the transmit configuration control register (TCCR.TSRQt) is 1). Therefore, be sure to check that fetching is not in progress before issuing a request.

Writing to a bit of this register is only possible when the current operating mode is operation mode. Only 1 can be written to this bit.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	LBA21	LBA20	LBA19	LBA18	LBA17	LBA16
Initial value:	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LBA15	LBA14	LBA13	LBA12	LBA11	LBA10	LBA9	LBA8	LBA7	LBA6	LBA5	LBA4	LBA3	LBA2	LBA1	LBA0
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 22	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
21	LBA21	1	R/W	Base Address Load Request (Rx17: Stream 15) 0: No load request is issued. 1: When written: A request for loading the corresponding base address is issued. When read: The given base address is being loaded.
20	LBA20	1	R/W	Base Address Load Request (Rx16: Stream 14) 0: No load request is issued. 1: When written: A request for loading the corresponding base address is issued. When read: The given base address is being loaded.
19	LBA19	1	R/W	Base Address Load Request (Rx15: Stream 13) 0: No load request is issued. 1: When written: A request for loading the corresponding base address is issued. When read: The given base address is being loaded.

Bit	Bit Name	Initial Value	R/W	Description
18	LBA18	1	R/W	Base Address Load Request (Rx14: Stream 12) 0: No load request is issued. 1: When written: A request for loading the corresponding base address is issued. When read: The given base address is being loaded.
17	LBA17	1	R/W	Base Address Load Request (Rx13: Stream 11) 0: No load request is issued. 1: When written: A request for loading the corresponding base address is issued. When read: The given base address is being loaded.
16	LBA16	1	R/W	Base Address Load Request (Rx12: Stream 10) 0: No load request is issued. 1: When written: A request for loading the corresponding base address is issued. When read: The given base address is being loaded.
15	LBA15	1	R/W	Base Address Load Request (Rx11: Stream 9) 0: No load request is issued. 1: When written: A request for loading the corresponding base address is issued. When read: The given base address is being loaded.
14	LBA14	1	R/W	Base Address Load Request (Rx10: Stream 8) 0: No load request is issued. 1: When written: A request for loading the corresponding base address is issued. When read: The given base address is being loaded.
13	LBA13	1	R/W	Base Address Load Request (Rx9: Stream 7) 0: No load request is issued. 1: When written: A request for loading the corresponding base address is issued. When read: The given base address is being loaded.
12	LBA12	1	R/W	Base Address Load Request (Rx8: Stream 6) 0: No load request is issued. 1: When written: A request for loading the corresponding base address is issued. When read: The given base address is being loaded.
11	LBA11	1	R/W	Base Address Load Request (Rx7: Stream 5) 0: No load request is issued. 1: When written: A request for loading the corresponding base address is issued. When read: The given base address is being loaded.
10	LBA10	1	R/W	Base Address Load Request (Rx6: Stream 4) 0: No load request is issued. 1: When written: A request for loading the corresponding base address is issued. When read: The given base address is being loaded.
9	LBA9	1	R/W	Base Address Load Request (Rx5: Stream 3) 0: No load request is issued. 1: When written: A request for loading the corresponding base address is issued. When read: The given base address is being loaded.

Bit	Bit Name	Initial Value	R/W	Description
8	LBA8	1	R/W	Base Address Load Request (Rx4: Stream 2) 0: No load request is issued. 1: When written: A request for loading the corresponding base address is issued. When read: The given base address is being loaded.
7	LBA7	1	R/W	Base Address Load Request (Rx3: Stream 1) 0: No load request is issued. 1: When written: A request for loading the corresponding base address is issued. When read: The given base address is being loaded.
6	LBA6	1	R/W	Base Address Load Request (Rx2: Stream 0) 0: No load request is issued. 1: When written: A request for loading the corresponding base address is issued. When read: The given base address is being loaded.
5	LBA5	1	R/W	Base Address Load Request (Rx1: Network Control) 0: No load request is issued. 1: When written: A request for loading the corresponding base address is issued. When read: The given base address is being loaded.
4	LBA4	1	R/W	Base Address Load Request (Rx0: Best Effort) 0: No load request is issued. 1: When written: A request for loading the corresponding base address is issued. When read: The given base address is being loaded.
3	LBA3	1	R/W	Base Address Load Request (Tx3: Stream Class A) 0: No load request is issued. 1: When written: A request for loading the corresponding base address is issued. When read: The given base address is being loaded.
2	LBA2	1	R/W	Base Address Load Request (Tx2: Stream Class B) 0: No load request is issued. 1: When written: A request for loading the corresponding base address is issued. When read: The given base address is being loaded.
1	LBA1	1	R/W	Base Address Load Request (Tx1: Network Control) 0: No load request is issued. 1: When written: A request for loading the corresponding base address is issued. When read: The given base address is being loaded.
0	LBA0	1	R/W	Base Address Load Request (Tx0: Best Effort) 0: No load request is issued. 1: When written: A request for loading the corresponding base address is issued. When read: The given base address is being loaded.

### 37A.2.4 AVB-DMAC Status Register (CSR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

The CSR register is used to indicate the operating mode in which the AVB-DMAC is running and the individual communications states.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	RPO	TPO3	TPO2	TPO1	TPO0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	DTS	—	—	—	—	OPS[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 21	—	All 0	R	Reserved These bits are read as 0.
20	RPO	0	R	Receive Process Status This bit indicates whether a reception queue contains an unread received frame. This bit being set to 1 indicates that a received frame is yet to be stored in the URAM. 0: Normal operation [Clearing conditions] — The current operating mode is not operation mode. — Received frames in the reception FIFO all being stored in the URAM. 1: Reception is in progress. [Setting condition] — A received frame being stored in the reception FIFO (but not yet in the URAM).
19	TPO3	0	R	Transmit Process Status 3 (Stream Class A) This bit indicates whether a class A stream is being transmitted. This bit being set to 1 indicates that the AVB-DMAC is fetching data for transmission from the URAM, or the E-MAC is transmitting data. 0: Normal operation [Clearing conditions] — The current operating mode is not operation mode. — Completion of transfer of all frames for transmission from the transmission FIFO and TCCR.TSRQ3 is 0. 1: Transmission is in progress. [Setting condition] — Transmission being started (by writing 1 to the transmit start request bit in the transmit configuration control register (TCCR.TSRQ3)).

Bit	Bit Name	Initial Value	R/W	Description
18	TPO2	0	R	<p>Transmit Process Status 2 (Stream Class B)</p> <p>This bit indicates whether a class B stream is being transmitted.</p> <p>This bit being set to 1 indicates that the AVB-DMAC is fetching data for transmission from the URAM, or the E-MAC is transmitting data.</p> <p>0: Normal operation</p> <p>[Clearing conditions]</p> <ul style="list-style-type: none"> <li>— The current operating mode is not operation mode.</li> <li>— Completion of transfer of all frames for transmission from the transmission FIFO and TCCR.TSRQ2 is 0.</li> </ul> <p>1: Transmission is in progress.</p> <p>[Setting condition]</p> <ul style="list-style-type: none"> <li>— Transmission being started (by writing 1 to the transmit start request bit in the transmit configuration control register (TCCR.TSRQ2)).</li> </ul>
17	TPO1	0	R	<p>Transmit Process Status 1 (Network Control)</p> <p>This bit indicates whether a network control is being transmitted.</p> <p>This bit being set to 1 indicates that the AVB-DMAC is fetching data for transmission from the URAM, or the E-MAC is transmitting data.</p> <p>0: Normal operation</p> <p>[Clearing conditions]</p> <ul style="list-style-type: none"> <li>— The current operating mode is not operation mode.</li> <li>— Completion of transfer of all frames for transmission from the transmission FIFO and TCCR.TSRQ1 is 0.</li> </ul> <p>1: Transmission is in progress.</p> <p>[Setting condition]</p> <ul style="list-style-type: none"> <li>— Transmission being started (by writing 1 to the transmit start request bit in the transmit configuration control register (TCCR.TSRQ1)).</li> </ul>
16	TPO0	0	R	<p>Transmit Process Status 0 (Best Effort)</p> <p>This bit indicates whether a best effort is being transmitted.</p> <p>This bit being set to 1 indicates that the AVB-DMAC is fetching data for transmission from the URAM, or the E-MAC is transmitting data.</p> <p>0: Normal operation</p> <p>[Clearing conditions]</p> <ul style="list-style-type: none"> <li>— The current operating mode is not operation mode.</li> <li>— Completion of transfer of all frames for transmission from the transmission FIFO and TCCR.TSRQ0 is 0.</li> </ul> <p>1: Transmission is in progress.</p> <p>[Setting condition]</p> <ul style="list-style-type: none"> <li>— Transmission being started (by writing 1 to the transmit start request bit in the transmit configuration control register (TCCR.TSRQ0)).</li> </ul>
19 to 9	—	All 0	R	<p>Reserved</p> <p>These bits are read as 0.</p>



Bit	Bit Name	Initial Value	R/W	Description
8	DTS	0	R	<p>Data Transmission Suspended Status</p> <p>This bit indicates whether access to the URAM is enabled.</p> <p>0: Normal operation</p> <p>[Clearing conditions]</p> <ul style="list-style-type: none"> <li>— The data transmission suspend request bit in the AVB-DMAC mode register (CCC.DTSR) being 0.</li> </ul> <p>1: Transmission is in progress.</p> <p>[Setting condition]</p> <ul style="list-style-type: none"> <li>— Access to the URAM not proceeding while the data transmission suspend request bit (CCC.DTSR) in the AVB-DMAC mode register (CCC) is 1 (if the URAM is being accessed, this bit is set to 1 on completion of access).</li> </ul>
7 to 4	—	All 0	R	<p>Reserved</p> <p>These bits are read as 0.</p>
3 to 0	OPS[3:0]	0001	R	<p>Operating Mode Status</p> <p>These bits indicate the current operating mode.</p> <p>For the operating modes, see section 37A.3.1.1, Operating Modes.</p> <p>0001: Reset mode</p> <p>0010: Configuration mode</p> <p>0100: Operation mode</p> <p>1000: Reserved</p> <p>Other settings are reserved.</p>

**37A.2.5 Current Descriptor Address Register q (CDARq) (q = 0 to 21)**

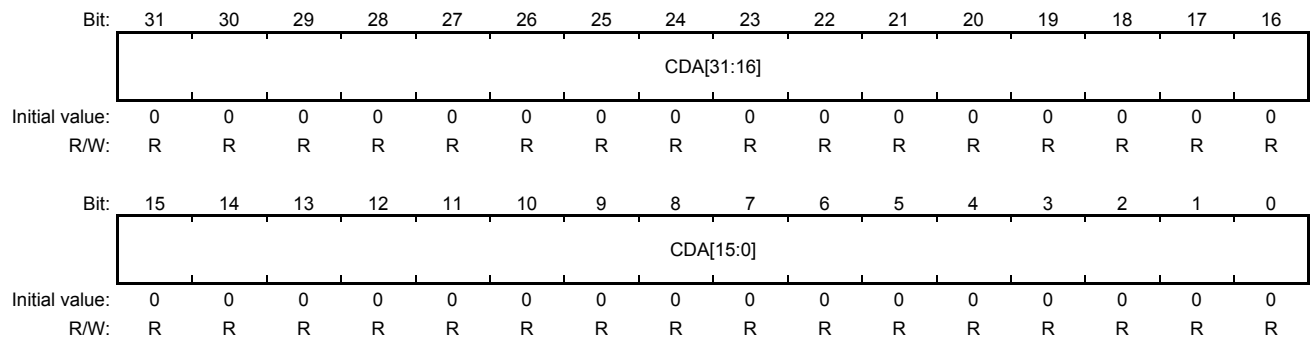
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

The CDARq register indicates the current descriptor address.

CDAR0 to CDAR3 indicate the addresses of the current descriptors for the corresponding transmission queues while CDAR4 to CDAR21 indicate the addresses of the current descriptors for the corresponding reception queues.

If the operating mode is changed to operation mode, the contents of the register for the queue to be used are set in the descriptor base address table register (DBAT).

Also, when the descriptor base address load request register (DLR) issues a load request, the contents of the descriptor base address table register (DBAT) are set in to the corresponding CDAR registers.



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	CDA[31:0]	H'0000 0000	R	<p>Current Descriptor Address</p> <p>The address of the current descriptors for the transmission queues.</p> <p>Conditions for updating:</p> <ul style="list-style-type: none"> <li>These bits are set to 0 when the operating mode is not operation mode. This register is updated in response to processing of the descriptor for a queue.</li> </ul>

**37A.2.6 Error Status Register (ESR)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	EIL	ET[3:0]			—	—	—	EQN[4:0]					
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 13	—	All 0	R	Reserved These bits are read as 0.
12	EIL	0	R	<p>Error Information Lost</p> <p>This bit indicates that error information detect by EthernetAVB is lost, because the previous reported error has not been processed by CPU.</p> <p>[Changing conditions]</p> <ul style="list-style-type: none"> <li>— This bit is set to 0 when leaving operation mode.</li> <li>— This bit is set to 0 when CPU writes 0 to EIS.QEF.</li> <li>— This bit is set to 1 when the set condition of EIS.QEF is fulfilled while EIS.QEF is 1.</li> </ul> <p>0: No loss of error information 1: Lost of error information detected</p>

Bit	Bit Name	Initial Value	R/W	Description
11 to 8	ET[3:0]	0000	R	<p><b>Error Type</b></p> <p>These bits indicate details about the transfer stage which was handled when EthernetAVB has detected an error.</p> <p>When the fault is related to the read descriptor (ESR.ET = B'0000 or B'0010), CPU needs to correct the faulty descriptor before the related queue can continue processing. Because the queue halts at the faulty descriptor CDARq.CDA (q = ESR.EQN) is identifying the faulty descriptor directly.</p> <p>When the fault is related to descriptor writing (ESR.ET = B'0001), CPU needs to recognize the not-updated or incorrectly updated descriptor in queue ESR.EQN. The write problem is not influencing how EthernetAVB processes the descriptor chain.</p> <p>When the fault is related to the Tx-buffer (ESR.ET = B'0011), CPU needs to clean-up the Tx-buffer to correct the buffer control structures.</p> <p>All other errors are transient in nature and may be corrected by continuation of hardware or software operation; so there is no strong demand on CPU interaction.</p> <p>Refer to section 37A.3.2.2, Checking Integrity for details of error handling.</p> <p>The CPU should only evaluate these bits when the EIS.QEF bit is 1.</p> <p>[Changing condition]</p> <ul style="list-style-type: none"> <li>— These bits are updated when the set condition of the EIS.QEF bit is fulfilled and the EIS.QEF bit is 0.</li> </ul> <p>0000: Read descriptor from URAM            0001: Write descriptor to URAM            0010: Interpret data descriptor            0011: Tx-buffer is corrupted            0100: Read data from URAM            0101: Write data or timestamp to URAM            0110: Reading from Rx-FIFO            0111: Rx-FIFO is corrupted            1000: Frame size error during reception detected            1001: Frame size error during transmission detected            1010: Tx-buffer overflow</p>
7 to 5	—	All 0	R	<p><b>Reserved</b></p> <p>These bits are read as 0.</p>

Bit	Bit Name	Initial Value	R/W	Description
4 to 0	EQN[4:0]	00000	R	<p>Error Queue Number</p> <p>These bits indicate the queue number which was handled when EthernetAVB has detected an error.</p> <p>A fault reported for ESR.EQN = 0 to 3 is related to transmit queue t (t = 0 to 3).</p> <p>From ESR.EQN = 4, the fault is related to receive queue r (r = ESR.EQN – 4).</p> <p>The CPU should only evaluate these bits when the EIS.QEF bit is 1. The CPU should not evaluate these bits when the ESR.ET bit is B'0011 or B'0111.</p> <p>[Changing condition]</p> <p>— These bits are updated when the set condition of the EIS.QEF bit is fulfilled and the EIS.QEF bit is 0.</p>

### 37A.2.7 Receive Configuration Register (RCR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

The RCR register is used to make settings related to reception for the AVB-DMAC.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	RFCL[12:0]												
Initial value:	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	ETS2	ETS0	ESF[1:0]	ENCF	EFFS	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
28 to 16	RFCL[12:0]	H'1800	R/W	Receive FIFO Caution Level These bits set the caution level for the reception FIFO and are used to maintain the priority order of the storage of received data and the fetching of data for transmission. If the reception FIFO contains less data than this level, processing of both transmission and reception queues becomes pending. If the reception FIFO contains more data than this level, only data in the reception queue are transferred, and processing of the transmission queue becomes pending. Writing to this bit is only possible when the current operating mode is configuration mode. Recommended value: H'1800 Notes: <ul style="list-style-type: none"> <li>The setting of this bit must be a multiple of four (i.e. set RFCL[1:0] = B'00).</li> <li>In the case of this LSI chip, set these bits to H'1800.</li> </ul>
15 to 6	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
5	ETS2	0	R/W	Time Stamp Enable (Stream) Enables the inclusion of time-stamp information in reception queues 2 to 17. Writing to this bit is only possible when the current operating mode is configuration mode. 0: Time stamping is disabled. 1: Time stamping is enabled. Recommended value: 0

Bit	Bit Name	Initial Value	R/W	Description
4	ETS0	0	R/W	<p>Time Stamp Enable (Best Effort)</p> <p>Enables the inclusion of time-stamp information in reception queue 0.</p> <p>Writing to this bit is only possible when the current operating mode is configuration mode.</p> <p>0: Time stamping is disabled.</p> <p>1: Time stamping is enabled.</p> <p>Recommended value: 0</p>
3, 2	ESF[1:0]	00	R/W	<p>Stream Filtering Select</p> <p>Settings for reception queues 2 to 17.</p> <p>These bits select separation filtering for reception queues 2 to 17.</p> <p>The queue-dependent separation filter can be used in combination with the identification of AVB stream frames.</p> <p>When the value is B'00, filtering is disabled and frames from streams are processed in reception queue 0 (best effort).</p> <p>When the value is B'01, the separation filter is enabled for both AVB stream frames and non-AVB stream frames; frames from non-matching streams are processed in reception queue 0 (best effort).</p> <p>When the value is B'10, the separation filter is enabled for AVB stream frames; frames from non-matching streams are discarded.</p> <p>When the value is B'11, the separation filter is enabled for AVB stream frames; frames from non-matching streams are processed in reception queue 0 (best effort).</p> <p>For separation filtering, see section 37A.3.4.1 (1), Separation Filtering.</p> <p>Writing to this bit is only possible when the current operating mode is configuration mode.</p> <p>00: Filtering is disabled. Frames are processed in queue 0 (best effort).</p> <p>01: The filter for both AVB stream frames and non-AVB stream frames is enabled; non-matching frames from the stream are processed in queue 0 (best effort).</p> <p>10: The filter for separating AVB stream frames from non-AVB stream frames is enabled; non-matching frames are discarded.</p> <p>11: The filter for separating AVB stream frames from non-AVB stream frames is enabled; non-matching frames from a stream are processed in queue 0 (best effort).</p> <p>Recommended value: B'10 or B'11</p>
1	ENCF	0	R/W	<p>Network Control Filtering Enable</p> <p>Setting for reception queue 1 (network control)</p> <p>Enables the AVB network control frame for reception queue 1.</p> <p>When reception queue 1 is disabled, a received frame is stored in reception queue 0 (best effort).</p> <p>Writing to this bit is only possible when the current operating mode is configuration mode.</p> <p>0: Network control is disabled.</p> <p>1: Network control is enabled.</p>

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Bit	Bit Name	Initial Value	R/W	Description
0	EFFS	0	R/W	<p>Error Frame Enable</p> <p>Enables or disables the reception of frames that have been classified as error frames by the E-MAC.</p> <p>Received error frames are stored in reception queue 0 (best effort).</p> <p>An indicator of error detection by the E-MAC during reception is stored in the descriptor (DESCR.MS).</p> <p>Writing to this bit is only possible when the current operating mode is configuration mode.</p> <p>0: Error frames are disabled.</p> <p>1: Error frames are enabled.</p> <p>Recommended value: 0</p>

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### 37A.2.8 Receive Queue Configuration Register i (RQCi) (i = 0 to 4)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

The RQC0 register is used to set up reception queues 0 to 3.

The RQC1 register is used to set up reception queues 4 to 7.

The RQC2 register is used to set up reception queues 8 to 11.

The RQC3 register is used to set up reception queues 12 to 15.

The RQC4 register is used to set up reception queues 16 to 17.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	UFCC3[1:0]		—	—	RSM3[1:0]		—	—	UFCC2[1:0]		—	—	RSM2[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	UFCC1[1:0]		—	—	RSM1[1:0]		—	—	UFCC0[1:0]		—	—	RSM0[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31, 30	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
29, 28	UFCC3[1:0]	00	R/W	Unread Frame Counter Configuration (Receive Queue 3+i×4) These bits set the unread frame counter used in reception queue 3+i×4. With the AVB-DMAC, four patterns of settings are available for the unread frame counter. Use the unread frame counter warning level configuration register (UFCW) and the unread frame counter stop level configuration register (UFCS) to set the warning level and stop level of the unread frame counter. Set the pattern number 3 set in the unread frame counter warning level configuration register (UFCW) and unread frame counter stop level configuration register (UFCS) in this bit. When the value is B'00, the stop function is disabled. Writing to the bits is only possible when the current operating mode is configuration mode.
27, 26	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.

Bit	Bit Name	Initial Value	R/W	Description
25, 24	RSM3[1:0]	00	R/W	<p>Receive Synchronous Mode (Receive Queue 3+i×4)</p> <p>These bits set receive synchronous mode.</p> <p>Set B'00 in this bit.</p> <p>For receive synchronous mode, see section 37A.3.4.3 (3), Mode with Write-Back. Writing to the bits is only possible when the current operating mode is configuration mode.</p> <p>00: Mode with write-back</p> <p>Other than 00: Setting prohibited</p>
23, 22	—	All 0	R/W	<p>Reserved</p> <p>These bits are read as 0. The write value should be 0.</p>
21, 20	UFCC2[1:0]	00	R/W	<p>Unread Frame Counter Configuration (Receive Queue 2+i×4)</p> <p>These bits set the unread frame counter used in reception queue 2+i×4.</p> <p>With the AVB-DMAC, four patterns of settings are available for the unread frame counter. Use the unread frame counter warning level configuration register (UFCW) and the unread frame counter stop level configuration register (UFCS) to set the warning level and stop level of the unread frame counter.</p> <p>Set the pattern number 2 set in the unread frame counter warning level configuration register (UFCW) and unread frame counter stop level configuration register (UFCS) in this bit.</p> <p>When the value is B'00, the stop function is disabled.</p> <p>Writing to the bits is only possible when the current operating mode is configuration mode.</p>
19, 18	—	All 0	R/W	<p>Reserved</p> <p>These bits are read as 0. The write value should be 0.</p>
17, 16	RSM2[1:0]	00	R/W	<p>Receive Synchronous Mode (Receive Queue 2+i×4)</p> <p>These bits set receive synchronous mode.</p> <p>Set B'00 in this bit.</p> <p>For receive synchronous mode, see section 37A.3.4.3 (3), Mode with Write-Back. Writing to the bits is only possible when the current operating mode is configuration mode.</p> <p>00: Mode with write-back</p> <p>Other than 00: Setting prohibited</p>
15, 14	—	All 0	R/W	<p>Reserved</p> <p>These bits are read as 0. The write value should be 0.</p>
13, 12	UFCC1[1:0]	00	R/W	<p>Unread Frame Counter Configuration (Receive Queue 1+i×4)</p> <p>These bits set the unread frame counter used in reception queue 1+i×4.</p> <p>With the AVB-DMAC, four patterns of settings are available for the unread frame counter. Use the unread frame counter warning level configuration register (UFCW) and the unread frame counter stop level configuration register (UFCS) to set the warning level and stop level of the unread frame counter.</p> <p>Set the pattern number 1 set in the unread frame counter warning level configuration register (UFCW) and unread frame counter stop level configuration register (UFCS) in this bit.</p> <p>When the value is B'00, the stop function is disabled.</p> <p>Writing to the bits is only possible when the current operating mode is configuration mode.</p>

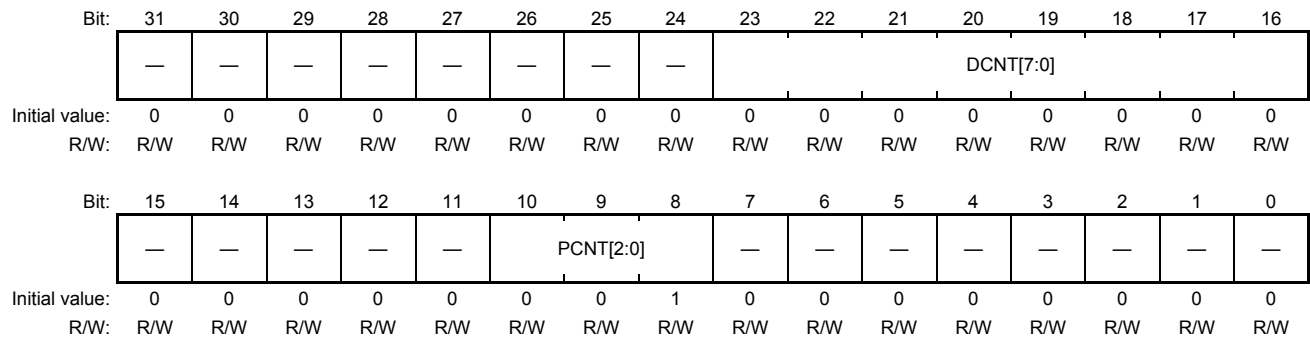
Bit	Bit Name	Initial Value	R/W	Description
11, 10	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
9, 8	RSM1[1:0]	00	R/W	Receive Synchronous Mode (Receive Queue 1+i×4) These bits set receive synchronous mode. Set B'00 in this bit. For receive synchronous mode, see section 37A.3.4.3 (3), Mode with Write-Back. Writing to the bits is only possible when the current operating mode is configuration mode. 00: Mode with write-back Other than 00: Setting prohibited
7, 6	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
5, 4	UFCC0[1:0]	00	R/W	Unread Frame Counter Configuration (Receive Queue 0+i×4) These bits set the unread frame counter used in reception queue 0+i×4. With the AVB-DMAC, four patterns of settings are available for the unread frame counter. Use the unread frame counter warning level configuration register (UFCW) and the unread frame counter stop level configuration register (UFCS) to set the warning level and stop level of the unread frame counter. Set the pattern number 0 set in the unread frame counter warning level configuration register (UFCW) and unread frame counter stop level configuration register (UFCS) in this bit. When the value is B'00, the stop function is disabled. Writing to the bits is only possible when the current operating mode is configuration mode.
3, 2	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
1, 0	RSM0[1:0]	00	R/W	Receive Synchronous Mode (Receive Queue 0+i×4) These bits set receive synchronous mode. Set B'00 in this bit. For receive synchronous mode, see section 37A.3.4.3 (3), Mode with Write-Back. Writing to the bits is only possible when the current operating mode is configuration mode. 00: Mode with write-back Other than 00: Setting prohibited

### 37A.2.9 Receive Padding Configuration Register (RPC)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

The RPC register is used to set padding for received frames.

Note: Padding can be used to extend frame lengths, but frame lengths should not exceed 4 Kbytes.



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
23 to 16	DCNT[7:0]	H'00	R/W	Stored Data Counter These bits specify the amount of the frame data (1 to 255) to be stored following the padding. Counting by one indicates one word (4 bytes). For example, when these bits are set to 47, the amount of data is 47 words (= 188 bytes). When these bits are 0, all received data have been stored following the initial padding. Writing to the bits is only possible when the current operating mode is configuration mode. For details on padding, see section 37A.3.4.3 (2) (c), Padding.
15 to 11	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
10 to 8	PCNT[2:0]	001	R/W	Stored Padding Counter These bits specify the amount of padding to be appended to the URAM. Counting by one indicates one word (4 bytes). For example, when these bits are set to 1, the amount of padding is one word (= 4 bytes). Writing to the bits is only possible when the current operating mode is configuration mode. For details on padding, see section 37A.3.4.3 (2) (c), Padding.
7 to 0	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.

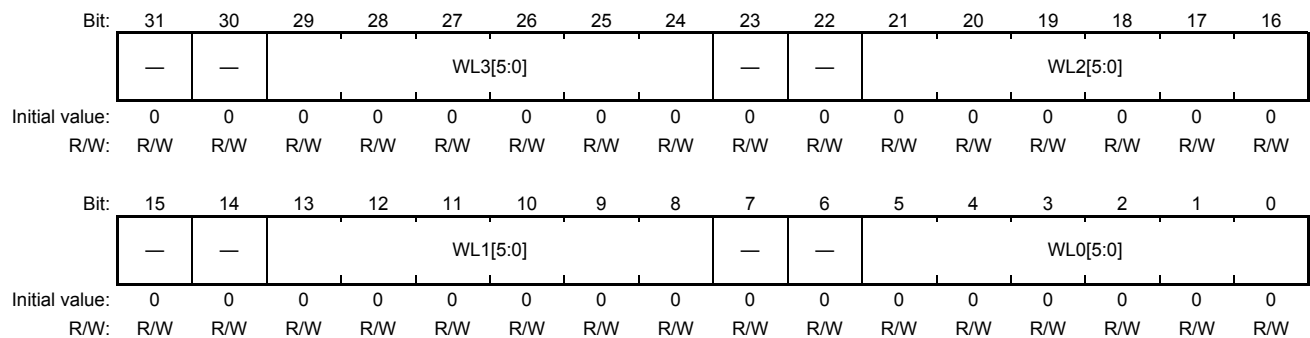
### 37A.2.10 Unread Frame Counter Warning Level Configuration Register (UFCW)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

The UFCW register sets the warning levels for the number of unread frames.

One of the four warning levels from 0 to 3 can be set for each reception queue. When these bits are set to 0, the stop function is disabled. The level to be used is specified by the receive queue configuration register  $i$  (RQCi) ( $i = 0$  to 4).

Writing to the bits is only possible when the current operating mode is configuration mode.



Bit	Bit Name	Initial Value	R/W	Description
31, 30	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
29 to 24	WL3[5:0]	000000	R/W	Warning Level 3 Unread frame count warning level 3
23, 22	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
21 to 16	WL2[5:0]	000000	R/W	Warning Level 2 Unread frame count warning level 2
15, 14	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
13 to 8	WL1[5:0]	000000	R/W	Warning Level 1 Unread frame count warning level 1
7, 6	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
5 to 0	WL0[5:0]	000000	R/W	Warning Level 0 Unread frame count warning level 0

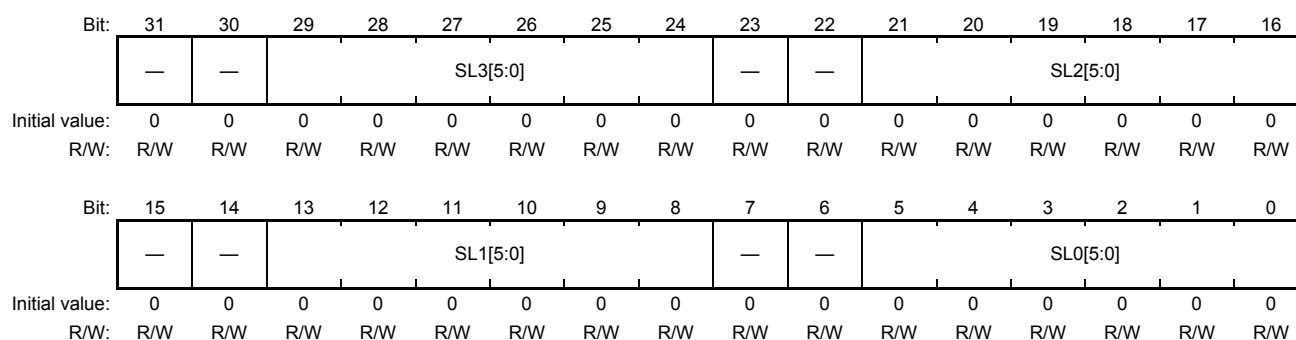
### 37A.2.11 Unread Frame Counter Stop Level Configuration Register (UFCS)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

The UFCS register sets the stop levels for unread frames.

One of the four stop levels from 0 to 3 can be set for each reception queue. When these bits are set to 0, the stop function is disabled. The level to be used is specified by the receive queue configuration register *i* (RQCi) (*i* = 0 to 4).

Writing to the bits is only possible when the current operating mode is configuration mode.



Bit	Bit Name	Initial Value	R/W	Description
31, 30	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
29 to 24	SL3[5:0]	000000	R/W	Stop Level 3 Unread frame count stop level 3
23, 22	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
21 to 16	SL2[5:0]	000000	R/W	Stop Level 2 Unread frame count stop level 2
15, 14	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
13 to 8	SL1[5:0]	000000	R/W	Stop Level 1 Unread frame count stop level 1
7, 6	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
5 to 0	SL0[5:0]	000000	R/W	Stop Level 0 Unread frame count stop level 0

### 37A.2.12 Unread Frame Counter Register i (UFCVi) (i = 0 to 4)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

The UFCV0 register indicates the number of unread frames in reception queues 0 to 3.

The UFCV1 register indicates the number of unread frames in reception queues 4 to 7.

The UFCV2 register indicates the number of unread frames in reception queues 8 to 11.

The UFCV3 register indicates the number of unread frames in reception queues 12 to 15.

The UFCV4 register indicates the number of unread frames in reception queues 16 and 17.

For a description of how to use unread frames, refer to section 37A.3.4.4, Unread Frame Counters.

#### Conditions for updating:

The bits are set to 0 when the operating mode is not operation mode and when the descriptor base address load request register (DLR) issues a base address load request.

The number is incremented when data received in reception queue r are stored normally. The maximum increment is H'3F. If the value exceeds H'3F, incrementation will not proceed.)

The number is decremented by the value written to the unread frame counter decrement register i (UFCDi).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	CV3[5:0]						—	—	CV2[5:0]					
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	CV1[5:0]						—	—	CV0[5:0]					
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31, 30	—	All 0	R	Reserved These bits are read as 0.
29 to 24	CV3[5:0]	000000	R	Unread Frame Count 3+4×i Number of unread frames in reception queue 3+4×i
23, 22	—	All 0	R	Reserved These bits are read as 0.
21 to 16	CV2[5:0]	000000	R	Unread Frame Count 2+4×i Number of unread frames in reception queue 2+4×i
15, 14	—	All 0	R	Reserved These bits are read as 0.
13 to 8	CV1[5:0]	000000	R	Unread Frame Count 1+4×i Number of unread frames in reception queue 1+4×i

Bit	Bit Name	Initial Value	R/W	Description
7, 6	—	All 0	R	Reserved These bits are read as 0.
5 to 0	CV0[5:0]	000000	R	Unread Frame Count $0+4 \times i$ Number of unread frames in reception queue $0+4 \times i$



**37A.2.13 Unread Frame Counter Decrement Register i (UFCDi) (i = 0 to 4)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

The UFCD0 register is used to decrement unread counters in reception queues 0 to 3.

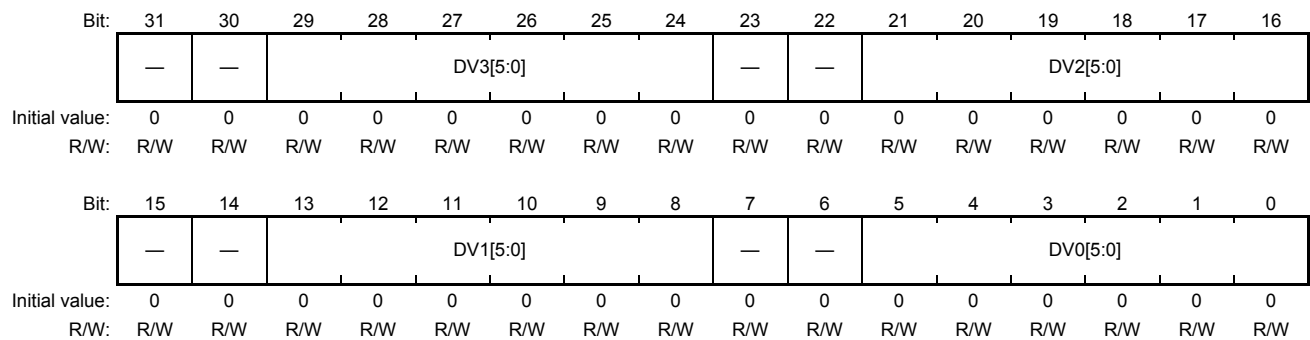
The UFCD1 register is used to decrement unread counters in reception queues 4 to 7.

The UFCD2 register is used to decrement unread counters in reception queues 8 to 11.

The UFCD3 register is used to decrement unread counters in reception queues 12 to 15.

The UFCD4 register is used to decrement unread counters in reception queues 16 and 17.

Write H'3F to these bits to reset the unread counters in reception queue r (r = 0 to 17). These bits are always read as 0.



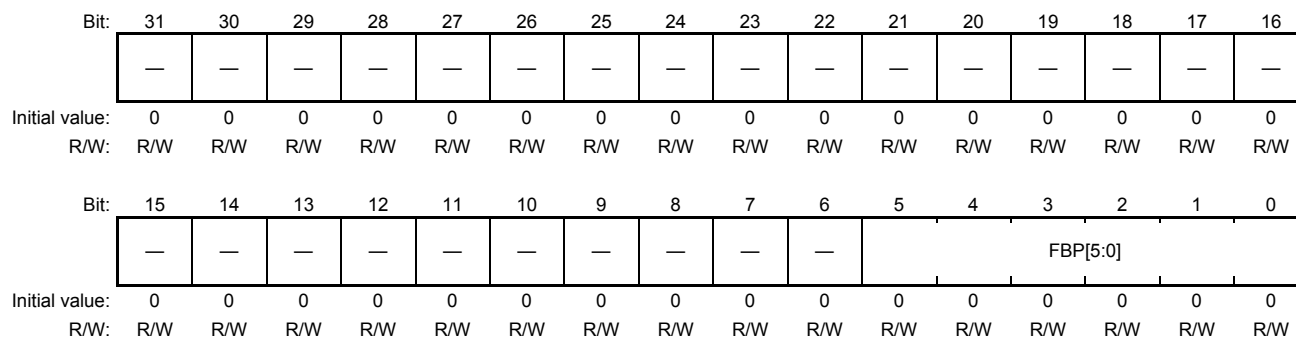
Bit	Bit Name	Initial Value	R/W	Description
31, 30	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
29 to 24	DV3[5:0]	000000	R/W	Unread Frame Decrement Value 3+4×i Unread frame decrement value for reception queue 3+4×i
23, 22	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
21 to 16	DV2[5:0]	000000	R/W	Unread Frame Decrement Value 2+4×i Unread frame decrement value for reception queue 2+4×i
15, 14	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
13 to 8	DV1[5:0]	000000	R/W	Unread Frame Decrement Value 1+4×i Unread frame decrement value for reception queue 1+4×i
7, 6	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
5 to 0	DV0[5:0]	000000	R/W	Unread Frame Decrement Value 0+4×i Unread frame decrement value for reception queue 0+4×i

### 37A.2.14 Separation Filter Offset Register (SFO)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

The SFO register sets an offset into frames for use by the separation filter.

Note: Received frames having fewer bytes than the setting of these bits + 8 bytes are judged to be non-matching by the separation filter. In this case, the data will either be sorted into a reception queue or discarded in accord with the setting of the separation filtering select bits in the receive configuration register (RCR.ESF).



Bit	Bit Name	Initial Value	R/W	Description
31 to 6	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
5 to 0	FBP[5:0]	000000	R/W	First Byte Position These bits set the position in Ethernet frames of the first byte of the bytes to be used by the separation filter. When these bits are 0, the separation filter starts from the start of each Ethernet frame (first byte of the destination address). For bytes in Ethernet frames, see Figure 37A.2, Operating Mode of AVB-DMAC, in section 37A.3.1, AVB-DMAC Operating Modes. Writing to the bits is only possible when the current operating mode is configuration mode. For separation filtering, see section 37A.3.4.1 (1), Separation Filtering.

### 37A.2.15 Separation Filter Pattern Register i (SFPi) (i = 0 to 31)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

A pair of SFPi registers set the pattern for the separation filters to be used by the corresponding reception queues 2 to 17 (for streams 0 to 15).

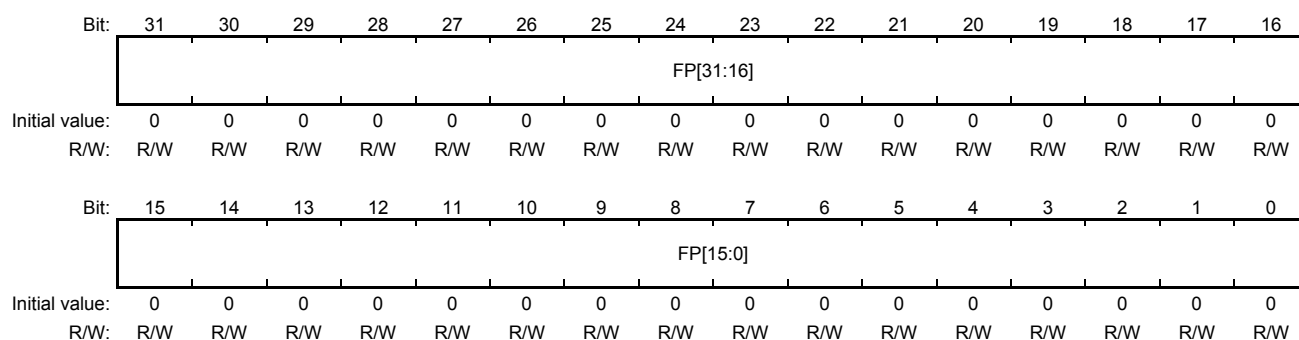
Each queue shares a 64-bit setting; reception queue 2 (for stream 0) uses SFP0 and SFP1, reception queue 17 (for stream 15) uses SFP30 and SFP31, and so on.

The separation filter passes a frame when, after masking by the mask value set in the separation filter mask register (SFMi), data from received frames match the value defined in these bits.

SFPi.FP[7:0] (where i is an even number) are used for the byte of Ethernet frame data specified by the separation filter offset register, while SFPi.FP[63:56] (where i is the corresponding odd number) are used for the byte at the address specified by the separation filter offset register (SFO) + 7.

Writing to the bits is only possible when the current operating mode is configuration mode.

For separation filtering, see section 37A.3.4.1 (1), Separation Filtering.



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	FP[31:0]	H'0000 0000	R/W	Separation Filter Pattern These bits set the pattern of the separation filter. The 64-bit filter pattern is set for each queue.

**37A.2.16 Separation Filter Mask Register i (SFMi) (i = 0 or 1)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

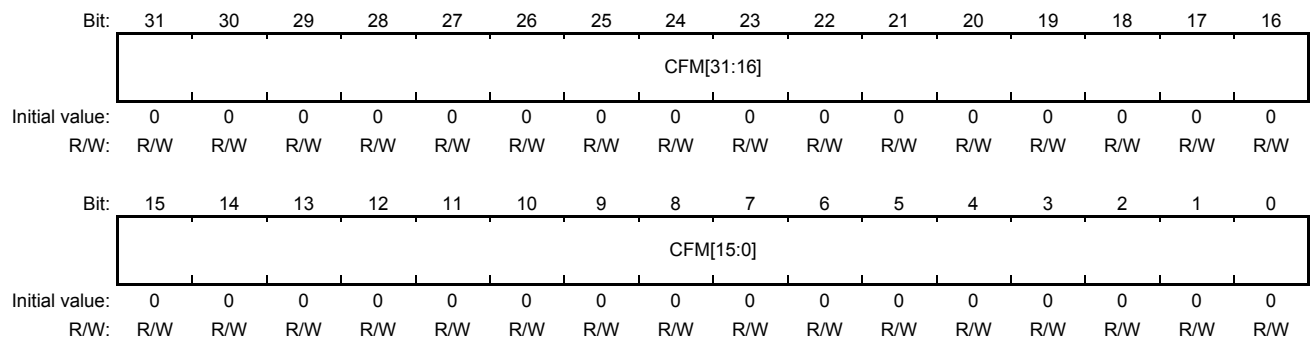
A pair of SFMi registers sets the mask value for the separation filter used by the corresponding reception queue 2 to 17 (stream 0 to 15).

SFM0.CFM[7:0] are used for bytes of Ethernet frame data specified by the separation filter offset register, while SFM1.CFM[63:56] are used for the separation filter offset register (SFO) + 7.

Frame data at the positions of mask bits that are set to 0 are masked; that is, they do not affect pattern-matching by the separation filter.

Writing to the bits is only possible when the current operating mode is configuration mode.

For separation filtering, see section 37A.3.4.1 (1), Separation Filtering.



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	CFM[31:0]	H'0000 0000	R/W	Separation Filter Mask These bits set the mask value for the separation filter.

### 37A.2.17 Transmit Configuration Register (TGC)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

The TGC register is used to make settings related to transmission for the AVB-DMAC.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	TBD3[1:0]		—	—	TBD2[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	TBD1[1:0]		—	—	TBD0[1:0]		—	—	TQP[1:0]		TSM3	TSM2	TSM1	TSM0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 22	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
21, 20	TBD3[1:0]	00	R/W	Transmit FIFO Size (Stream Class A) These bits set the sizes of the transmission FIFO buffers for use with each of the transmission queue 3 (for stream class A). Writing to these bits is only possible when the current operating mode is configuration mode. Set these bits to B'10.
19, 18	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
17, 16	TBD2[1:0]	00	R/W	Transmit FIFO Size (Stream Class B) These bits set the sizes of the transmission FIFO buffers for use with each of the transmission queue 2 (for stream class B). Writing to these bits is only possible when the current operating mode is configuration mode. Set these bits to B'10.
15, 14	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
13, 12	TBD1[1:0]	00	R/W	Transmit FIFO Size (Network Control) These bits set the sizes of the transmission FIFO buffers for use with each of the transmission queue 1 (for network control). Writing to these bits is only possible when the current operating mode is configuration mode.
11, 10	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
9, 8	TBD0[1:0]	00	R/W	Transmit FIFO Size (Best Effort) These bits set the sizes of the transmission FIFO buffers for use with each of the transmission queue 0 (for best effort). Writing to these bits is only possible when the current operating mode is configuration mode.

Bit	Bit Name	Initial Value	R/W	Description
7, 6	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
5, 4	TQP[1:0]	00	R/W	Transmit Queue Priority These bits set the priority of the transmission queues. 00: Non-AVB mode: Q3 → Q2 → Q1 → Q0 01: AVB mode 1: Q3 (CBS) → Q2 (CBS) → Q1 → Q0 10: Setting prohibited 11: AVB mode 2: Q1 → Q3 (CBS) → Q2 (CBS) → Q0 For the credit-based shaping (CBS) algorithm, see section 37A.3.6, CBS (Credit-Based Shaping). The CBS algorithm is not applied in non-AVB mode (i.e. when the value is B'00). Writing to the bits is only possible when the current operating mode is configuration mode.
3	TSM3	0	R/W	Transmit Synchronous Mode (Stream Class A) Set these bits to 0. 0: With write-back 1: Setting prohibited
2	TSM2	0	R/W	Transmit Synchronous Mode (Stream Class B) Set these bits to 0. 0: With write-back 1: Setting prohibited
1	TSM1	0	R/W	Transmit Synchronous Mode (Network Control) Set these bits to 0. 0: With write-back 1: Setting prohibited
0	TSM0	0	R/W	Transmit Synchronous Mode (Best Effort) Set these bits to 0. 0: With write-back 1: Setting prohibited

### 37A.2.18 Transmit Configuration Control Register (TCCR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

The TCCR register controls transmission by the AVB-DMAC and is used to make related settings.

#### Conditions for updating:

The bit is set to 0 when the operating mode is not operation mode, when a descriptor of type EEMPTY, FEMPTY or LEMPTY (no usable data) is processed, when an EOS descriptor is processed, and when a descriptor with defective data is processed.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	TFR	TFEN	—	—	—	—	TSRQ3	TSRQ2	TSRQ1	TSRQ0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 10	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
9	TFR	0	R/W	Time Stamp FIFO Release This bit releases the oldest entry in the time-stamp FIFO. For a description of how to use the time-stamp FIFO, see section 37A.3.5.4, Time Stamping in Transmission. 0: (Not operating) 1: Releases the oldest entry in the time-stamp FIFO.
8	TFEN	0	R/W	Time Stamp FIFO Enable This bit enables storage in the time-stamp FIFO. When it is set, time-stamp information is stored for descriptors with DESCR.TSR set to 1 (for DESCR.TSR, see section 37A.3.5.2 (2), Configuration of Transmission Frame Data Descriptors. When 0 is set in this bit, no entries are made in the time-stamp FIFO. For a description of how to use the time-stamp FIFO, see section 37A.3.5.4, Time Stamping in Transmission. 0: Recording of transmission time stamps in the time-stamp FIFO is disabled. 1: Recording of transmission time stamps in the time-stamp FIFO is enabled.
7 to 4	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.

Bit	Bit Name	Initial Value	R/W	Description
3	TSRQ3	0	R/W	<p>Transmit Start Request (Queue 3 (Stream Class A))</p> <p>This bit issues a request to start transmission for transmission queue 3.</p> <p>When read, this bit being set to 1 indicates that transmission queue t has a frame that has not yet been fetched to the transmission FIFO.</p> <p>Frame transmission by the E-MAC is processed independently from fetching to the transmission FIFO. The timing of transmission from a queue depends on the priority order of transmission.</p> <p>For the scheduling of transmission queues, see section 37A.3.5.1, Transmission Modes.</p> <p>Writing to this bit is only possible when the current operating mode is operation mode.</p> <p>Only 1 can be written to the bit. Writing 0 to the bit has no effect.</p> <p>0: Transmission queue is empty or stopped.</p> <p>1: When written: A transmission start request is issued.</p> <p>When read: Fetching of data for transmission is pending.</p>
2	TSRQ2	0	R/W	<p>Transmit Start Request (Queue 2 (Stream Class B))</p> <p>This bit issues a request to start transmission for transmission queue 2.</p> <p>When read, this bit being set to 1 indicates that transmission queue t has a frame that has not yet been fetched to the transmission FIFO.</p> <p>Frame transmission by the E-MAC is processed independently from fetching to the transmission FIFO. The timing of transmission from a queue depends on the priority order of transmission.</p> <p>For the scheduling of transmission queues, see section 37A.3.5.1, Transmission Modes.</p> <p>Writing to this bit is only possible when the current operating mode is operation mode.</p> <p>Only 1 can be written to the bit. Writing 0 to the bit has no effect.</p> <p>0: Transmission queue is empty or stopped.</p> <p>1: When written: A transmission start request is issued.</p> <p>When read: Fetching of data for transmission is pending.</p>
1	TSRQ1	0	R/W	<p>Transmit Start Request (Queue 1 (Network Control))</p> <p>This bit issues a request to start transmission for transmission queue 1.</p> <p>When read, this bit being set to 1 indicates that transmission queue t has a frame that has not yet been fetched to the transmission FIFO.</p> <p>Frame transmission by the E-MAC is processed independently from fetching to the transmission FIFO. The timing of transmission from a queue depends on the priority order of transmission.</p> <p>For the scheduling of transmission queues, see section 37A.3.5.1, Transmission Modes.</p> <p>Writing to this bit is only possible when the current operating mode is operation mode.</p> <p>Only 1 can be written to the bit. Writing 0 to the bit has no effect.</p> <p>0: Transmission queue is empty or stopped.</p> <p>1: When written: A transmission start request is issued.</p> <p>When read: Fetching of data for transmission is pending.</p>



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Bit	Bit Name	Initial Value	R/W	Description
0	TSRQ0	0	R/W	<p>Transmit Start Request (Queue 0 (Best Effort))</p> <p>This bit issues a request to start transmission for transmission queue 0.</p> <p>When read, this bit being set to 1 indicates that transmission queue t has a frame that has not yet been fetched to the transmission FIFO.</p> <p>Frame transmission by the E-MAC is processed independently from fetching to the transmission FIFO. The timing of transmission from a queue depends on the priority order of transmission.</p> <p>For the scheduling of transmission queues, see section 37A.3.5.1, Transmission Modes.</p> <p>Writing to this bit is only possible when the current operating mode is operation mode.</p> <p>Only 1 can be written to the bit. Writing 0 to the bit has no effect.</p> <p>0: Transmission queue is empty or stopped.</p> <p>1: When written: A transmission start request is issued.</p> <p>When read: Fetching of data for transmission is pending.</p>

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### 37A.2.19 Transmit Status Register (TSR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

The TSR register indicates the state of transmission by the AVB-DMAC.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	TFFL[2:0]			—	—	—	—	CCS1[1:0]		CCS0[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

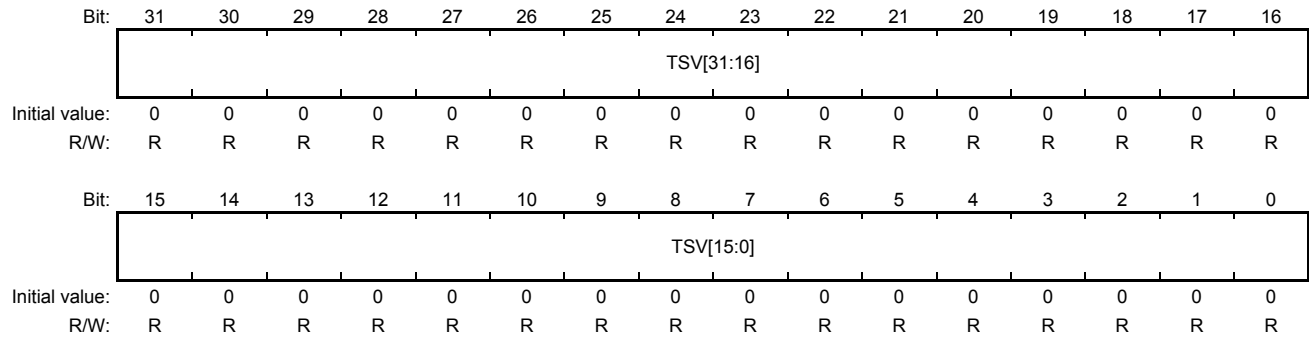
Bit	Bit Name	Initial Value	R/W	Description
31 to 11	—	All 0	R	Reserved These bits are read as 0. The write value should be 0.
10 to 8	TFFL[2:0]	00	R	Time Stamp FIFO Count These bits indicate the number of time stamps in the time-stamp FIFO. The values 0 and 2 indicate that the time-stamp FIFO is empty and full, respectively (values 3 to 7 are reserved). Conditions for updating: <ul style="list-style-type: none"> <li>The bits are set to 0 when the operating mode is not operation mode and when the time stamp FIFO enable bit in the transmit configuration control register (TCCR.TFEN) = 0.</li> <li>When the time stamp FIFO enable bit (TCCR.TFEN) is 1 and these bits are not 2, the value of these bits is incremented after a frame with DESCR.TSR set has been transmitted by the E-MAC (for DESCR.TSR, see section 37A.3.5.2 (2), Configuration of Transmission Frame Data Descriptors.</li> <li>The value of these bits is decremented if it is not 0 when 1 is written to the time stamp FIFO release bit in the transmit configuration control register (TCCR.TFR).</li> </ul>
7 to 4	—	All 0	R	Reserved These bits are read as 0. The write value should be 0.

Bit	Bit Name	Initial Value	R/W	Description
3, 2	CCS1[1:0]	00	R	<p>CBS Counter Status 1 (Class A)</p> <p>These bits indicate the CBS (credit-based shaping) state of stream data transmission queue 1. If the calculated credit value is outside the range specified by CBS upper limit register c (CULc) and CBS lower limit register c (CLLc), it falls outside the range for CBS.</p> <p>Conditions for updating:</p> <ul style="list-style-type: none"> <li>The bits are set to B'00 when the operating mode is not operation mode. The bits are set to B'00 when the CBS is inside the condition limits.</li> <li>The bits are set to B'01 if the credit value calculated by the CBS is lower than the value in CBS lower limit register c (CLLc).</li> <li>The bits are set to B'10 if the credit value calculated by the CBS is higher than the value in CBS upper limit register c (CULc).</li> </ul> <p>00: The current credit value is within the limit.            01: The current credit value is less than or equal to the lower limit.            10: The current credit value is greater than or equal to the upper limit.            11: (Reserved)</p>
1, 0	CCS0[1:0]	00	R	<p>CBS Counter Status 0 (Class B)</p> <p>These bits indicate the CBS (credit-based shaping) state of stream data transmission queue 0. If the calculated credit value is outside the range specified by CBS upper limit register c (CULc) and CBS lower limit register c (CLLc), it falls outside the range for CBS.</p> <p>Conditions for updating:</p> <ul style="list-style-type: none"> <li>The bits are set to B'00 when the operating mode is not operation mode. The bits are set to B'00 when the CBS is inside the condition limits.</li> <li>The bits are set to B'01 if the credit value calculated by the CBS is lower than the value in CBS lower limit register c (CLLc).</li> <li>The bits are set to B'10 if the credit value calculated by the CBS is higher than the value in CBS upper limit register c (CULc).</li> </ul> <p>00: The current credit value is within the limit.            01: The current credit value is less than or equal to the lower limit.            10: The current credit value is greater than or equal to the upper limit.            11: (Reserved)</p>

**37A.2.20 Time Stamp FIFO Access Register 0 (TFA0)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

TFA0 indicates the nanosecond portion of the timestamp value.

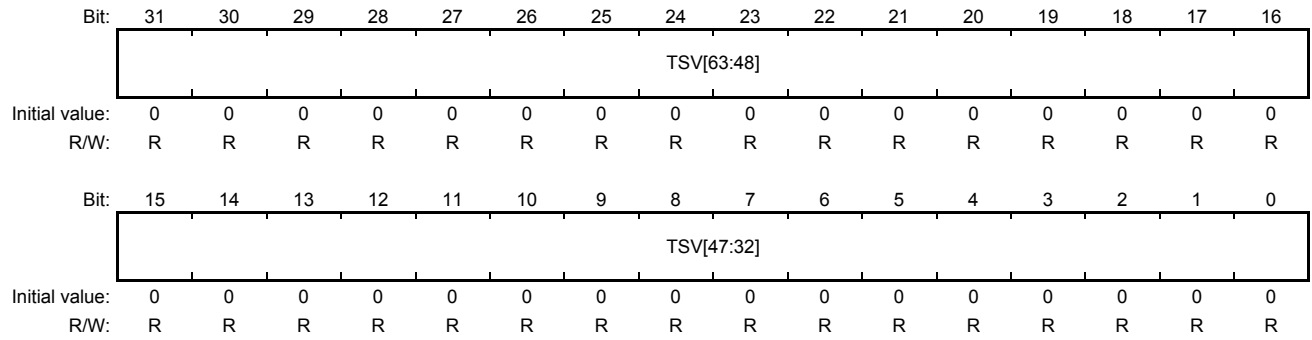


Bit	Bit Name	Initial Value	R/W	Description
31 to 0	TSV[31:0]	H'0000 0000	R	<p>Time Stamp Value</p> <p>These 80 bits consist of TFA0.TSV[31:0], TFA1.TSV[63:32], and TFA2.TSV[79:64], which together indicate the oldest time stamp value stored in the time-stamp FIFO.</p> <p>Once the time-stamp FIFO is full, no further time-stamp values are stored.</p> <p>Conditions for updating:</p> <ul style="list-style-type: none"> <li>The bits are set to H'0000 0000 when the operating mode is not operation mode.</li> <li>The register is updated whenever a value is stored in the time-stamp FIFO (when the time-stamp FIFO count bit in the transmit status register (TSR.TFFL) changes from 0 to 1).</li> <li>The register is updated when the oldest entry is released (when the time stamp FIFO release bit in the transmit configuration control register (TCCR.TFR) is set to 1).</li> </ul>

**37A.2.21 Time Stamp FIFO Access Register 1 (TFA1)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

The TFA1 register indicates the lower 32 bits of the second portion of the timestamp value.



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	TSV[63:32]	H'0000 0000	R	Time Stamp Value For details, see section 37A.2.20, Time Stamp FIFO Access Register 0 (TFA0).

### 37A.2.22 Time Stamp FIFO Access Register 2 (TFA2)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

The TFA2 register indicates the timestamp tag and higher 16 bits of the second portion of the timestamp value.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	TST[9:0]									
Initial value:	0	0	0	0	0	0	0									
R/W:	R	R	R	R	R	R	R									
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TSV[79:64]															
Initial value:	0															
R/W:	R															

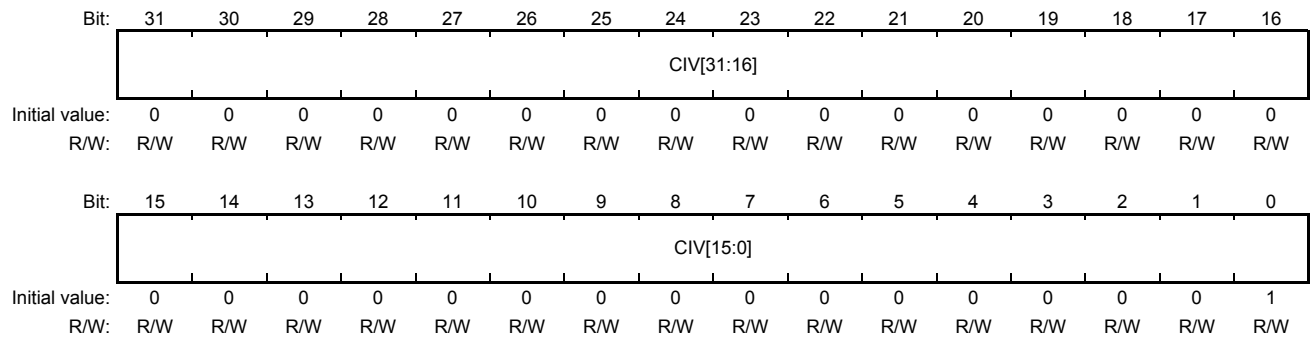
Bit	Bit Name	Initial Value	R/W	Description
31 to 26	—	All 0	R	Reserved These bits are read as 0.
25 to 16	TST[9:0]	H'000	R	<b>Time Stamp Tag</b> These bits indicate the contents of the DESCR.TAG bit within the descriptor for frame transmission. These values are used to check the correlation between frames within the transmission queue and the time-stamp values (accessible through time stamp FIFO access register i (TFAi)) which can be placed in the FIFO. For the tagging of frames in transmission, see section 37A.3.5.4, Time Stamping in Transmission. Conditions for updating: <ul style="list-style-type: none"> <li>• The bits are set to 000H when the operating mode is not operation mode.</li> <li>• Updated when a value is stored in the time-stamp FIFO (when the value of the time stamp FIFO count bit in the transmit status register (TSR.TFFL) changes from 0 to 1).</li> <li>• Updated when the oldest entry has been released (1 is set in the time stamp FIFO release bit in the transmit configuration control register (TCCR.TFR)).</li> </ul>
15 to 0	TSV[79:64]	H'0000	R	<b>Time Stamp Value</b> For details, see section 37A.2.20, Time Stamp FIFO Access Register 0 (TFA0).

**37A.2.23 CBS Increment Value Register c (CIVRc) (c = 0 or 1)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

The CIVR0 register sets the increment in the CBS algorithm for transmission queue 2 (for stream class B).

The CIVR1 register sets the increment in the CBS algorithm for transmission queue 3 (for stream class A).



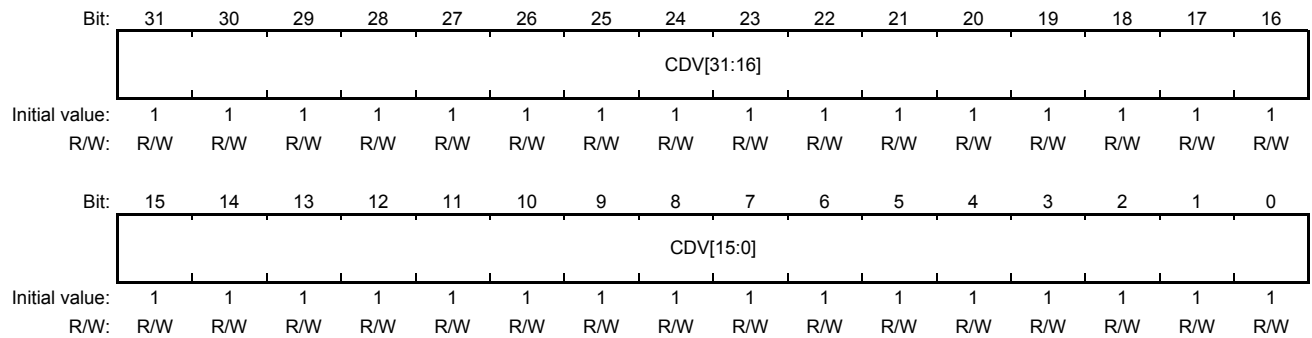
Bit	Bit Name	Initial Value	R/W	Description
31 to 0	CIV[31:0]	H'0000 0001	R/W	<p>CBS Increment Value</p> <p>CBS increment value (1 to H'FFFF)</p> <p>These bits define the increment value related to idleSlope for the CBS algorithm.</p> <p>Set a value in the range from H'0000 0001 to H'0000 FFFF.</p> <p>The value to be written to these bits depends on the Ethernet bit rate and HPφ (high-speed peripheral clock). For details, see section 37A.3.6, CBS (Credit-Based Shaping).</p>

**37A.2.24 CBS Decrement Value Register c (CDV<sub>Rc</sub>) (c = 0 or 1)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

The CDVR<sub>0</sub> register sets the decrement in the CBS algorithm for transmission queue 2 (for stream class B).

The CDVR<sub>1</sub> register sets the decrement in the CBS algorithm for transmission queue 3 (for stream class A).



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	CDV[31:0]	H'FFFF FFFF	R/W	<p>CBS Decrement Value</p> <p>Setting value: -1 to -65536 (H'FFFF FFFF to H'FFFF 0000)</p> <p>These bits set the decrement for the CBS algorithm.</p> <p>These bits define the decrement value related to sendSlope for CBS algorithm.</p> <p>The value to be written to these bits depends on the Ethernet bit rate and HP<math>\phi</math> (high-speed peripheral clock). For details, see section 37A.3.6, CBS (Credit-Based Shaping).</p>

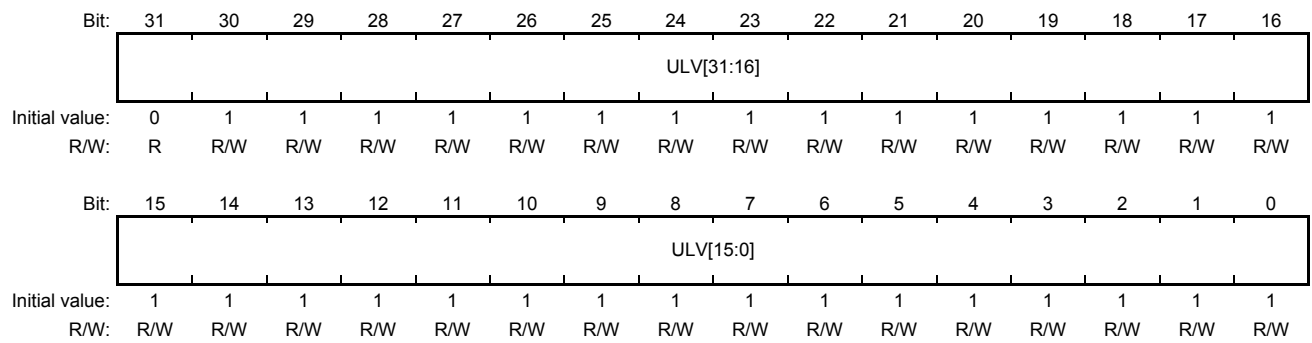


**37A.2.25 CBS Upper Limit Register c (CULc) (c = 0 or 1)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

The CUL0 register sets the upper limit for credit values calculated by using the CBS algorithm for transmission queue 2 (for stream class B).

The CUL1 register sets the upper limit for credit values calculated by using the CBS algorithm for transmission queue 3 (for stream class A).



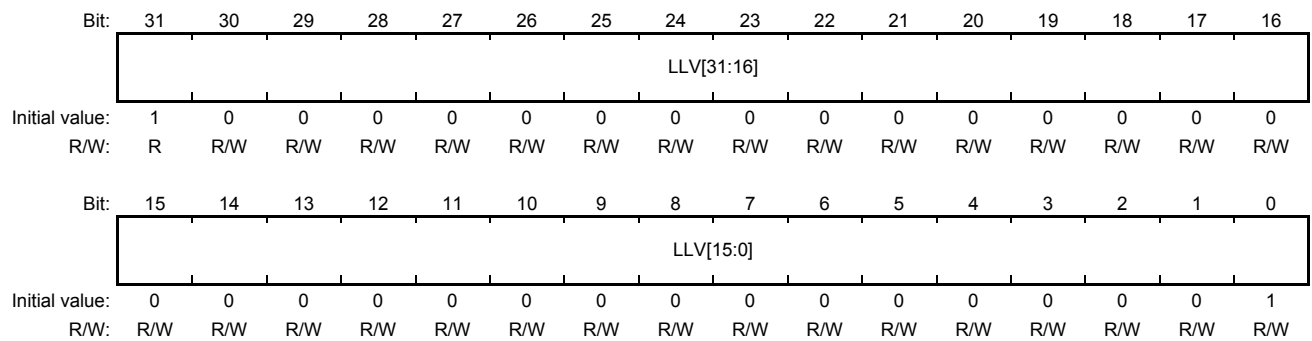
Bit	Bit Name	Initial Value	R/W	Description
31 to 0	ULV[31:0]	H'7FFF FFFF	R/W	<p>CBS Upper Limit</p> <p>These bits set the upper limit for credit values calculated by using the CBS algorithm.</p> <p>The setting is a limiting value for error detection and does not normally affect operation of the algorithm.</p> <p>Write a positive value to these bits.</p> <p>For details, see section 37A.3.6, CBS (Credit-Based Shaping).</p>

**37A.2.26 CBS Lower Limit Register c (CLLc) (c = 0 or 1)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

The CUL0 register sets the lower limit for credit values calculated by using the CBS algorithm for transmission queue 2 (for stream class B).

The CUL1 register sets the lower limit for credit values calculated by using the CBS algorithm for transmission queue 3 (for stream class A).



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	LLV[31:0]	H'8000 0001	R/W	<p>CBS Lower Limit</p> <p>These bits set the lower limit for credit values calculated by using the CBS algorithm.</p> <p>The setting is a limiting value for error detection and does not normally affect operation of the algorithm.</p> <p>Write a negative value to these bits.</p> <p>For details, see section 37A.3.6, CBS (Credit-Based Shaping).</p>

**37A.2.27 Descriptor Interrupt Control Register (DIC)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

The DIC register is used to control descriptor interrupts 1 to 15.

When an interrupt source flag is set (a bit from DPF1 to DPF15 bits in the descriptor interrupt status register (DIS) = 1) while the interrupt is enabled, the interrupt is issued.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DPE15	DPE14	DPE13	DPE12	DPE11	DPE10	DPE9	DPE8	DPE7	DPE6	DPE5	DPE4	DPE3	DPE2	DPE1	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
15	DPE15	0	R/W	Descriptor Interrupt Enable 15 0: Disabled 1: Enabled
14	DPE14	0	R/W	Descriptor Interrupt Enable 14 0: Disabled 1: Enabled
13	DPE13	0	R/W	Descriptor Interrupt Enable 13 0: Disabled 1: Enabled
12	DPE12	0	R/W	Descriptor Interrupt Enable 12 0: Disabled 1: Enabled
11	DPE11	0	R/W	Descriptor Interrupt Enable 11 0: Disabled 1: Enabled
10	DPE10	0	R/W	Descriptor Interrupt Enable 10 0: Disabled 1: Enabled
9	DPE9	0	R/W	Descriptor Interrupt Enable 9 0: Disabled 1: Enabled
8	DPE8	0	R/W	Descriptor Interrupt Enable 8 0: Disabled 1: Enabled

Bit	Bit Name	Initial Value	R/W	Description
7	DPE7	0	R/W	Descriptor Interrupt Enable 7 0: Disabled 1: Enabled
6	DPE6	0	R/W	Descriptor Interrupt Enable 6 0: Disabled 1: Enabled
5	DPE5	0	R/W	Descriptor Interrupt Enable 5 0: Disabled 1: Enabled
4	DPE4	0	R/W	Descriptor Interrupt Enable 4 0: Disabled 1: Enabled
3	DPE3	0	R/W	Descriptor Interrupt Enable 3 0: Disabled 1: Enabled
2	DPE2	0	R/W	Descriptor Interrupt Enable 2 0: Disabled 1: Enabled
1	DPE1	0	R/W	Descriptor Interrupt Enable 1 0: Disabled 1: Enabled
0	—	0	R/W	Reserved These bits are read as 0. The write value should be 0.

### 37A.2.28 Descriptor Interrupt Status Register (DIS)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

The DIS register indicates the state of descriptor interrupts.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DPF15	DPF14	DPF13	DPF12	DPF11	DPF10	DPF9	DPF8	DPF7	DPF6	DPF5	DPF4	DPF3	DPF2	DPF1	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
15	DPF15	0	R/W	Descriptor Interrupt Status15 0: The interrupt is not pending. 1: The interrupt is pending.
14	DPF14	0	R/W	Descriptor Interrupt Status14 0: The interrupt is not pending. 1: The interrupt is pending.
13	DPF13	0	R/W	Descriptor Interrupt Status13 0: The interrupt is not pending. 1: The interrupt is pending.
12	DPF12	0	R/W	Descriptor Interrupt Status12 0: The interrupt is not pending. 1: The interrupt is pending.
11	DPF11	0	R/W	Descriptor Interrupt Status11 0: The interrupt is not pending. 1: The interrupt is pending.
10	DPF10	0	R/W	Descriptor Interrupt Status10 0: The interrupt is not pending. 1: The interrupt is pending.
9	DPF9	0	R/W	Descriptor Interrupt Status9 0: The interrupt is not pending. 1: The interrupt is pending.
8	DPF8	0	R/W	Descriptor Interrupt Status8 0: The interrupt is not pending. 1: The interrupt is pending.
7	DPF7	0	R/W	Descriptor Interrupt Status7 0: The interrupt is not pending. 1: The interrupt is pending.

Bit	Bit Name	Initial Value	R/W	Description
6	DPF6	0	R/W	Descriptor Interrupt Status6 0: The interrupt is not pending. 1: The interrupt is pending.
5	DPF5	0	R/W	Descriptor Interrupt Status5 0: The interrupt is not pending. 1: The interrupt is pending.
4	DPF4	0	R/W	Descriptor Interrupt Status4 0: The interrupt is not pending. 1: The interrupt is pending.
3	DPF3	0	R/W	Descriptor Interrupt Status3 0: The interrupt is not pending. 1: The interrupt is pending.
2	DPF2	0	R/W	Descriptor Interrupt Status2 0: The interrupt is not pending. 1: The interrupt is pending.
1	DPF1	0	R/W	Descriptor Interrupt Status1 0: The interrupt is not pending. 1: The interrupt is pending.
0	—	0	R/W	Reserved These bits are read as 0. The write value should be 0.

#### DPF1 to DPF15 Descriptor Interrupt Status Bits:

When DESC.R.DIE is 1 to 15, the corresponding bit indicates completion of the processing of a descriptor within the reception or transmission queue.

When DESC.R.DIE is 0, the descriptor interrupt is not generated.

Only 0 can be written to these bits.

#### [Conditions for Changing]

- A bit is set to 0 when the operating mode is not operation mode.
- A bit is set to 1 when a descriptor with DESC.R.DIE set to the corresponding number from 1 to 15 is processed.

**37A.2.29 Error Interrupt Control Register (EIC)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

The EIC register controls the AVB-DMAC-related error interrupts.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	TFFE	CULE1	CULE0	CLLE1	CLLE0	SEE	QEE	MTEE	MREE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 9	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
8	TFFE	0	R/W	Time Stamp FIFO Full-Error Interrupt Enable When the time stamp FIFO is full (TFFF in the error interrupt status register (EIS) = 1) and the interrupt is enabled, the interrupt is issued. 0: Disabled 1: Enabled
7	CULE1	0	R/W	CBS Upper Limit Error Interrupt Enable (Class A) When the Class A CBS reaches its upper limit (CULF1 in the error interrupt status register (EIS) = 1), the interrupt is issued. 0: Disabled 1: Enabled
6	CULE0	0	R/W	CBS Upper Limit Error Interrupt Enable (Class B) When the Class B CBS reaches its upper limit (CULF0 in the error interrupt status register (EIS) = 1), the interrupt is issued. 0: Disabled 1: Enabled
5	CLLE1	0	R/W	CBS Lower Limit Error Interrupt Enable (Class A) When the Class A CBS reaches its lower limit (CLLF1 in the error interrupt status register (EIS) = 1), the interrupt is issued. 0: Disabled 1: Enabled
4	CLLE0	0	R/W	CBS Lower Limit Error Interrupt Enable (Class B) When the Class B CBS reaches its lower limit (CLLF0 in the error interrupt status register (EIS) = 1), the interrupt is issued. 0: Disabled 1: Enabled

Bit	Bit Name	Initial Value	R/W	Description
3	SEE	0	R/W	Separation Error Interrupt Enable While this bit is 1, an interrupt will be generated when the EIS.SEF bit is 1. 0: Disabled 1: Enabled
2	QEE	0	R/W	Queue Error Interrupt Enable While this bit is 1, an interrupt will be generated when the EIS.QEF bit is 1. 0: Disabled 1: Enabled
1	MTEE	0	R/W	E-MAC Transmission Error Interrupt Enable While this bit is 1, an interrupt will be generated when the EIS.MTEF bit is 1. 0: Disabled 1: Enabled
0	MREE	0	R/W	E-MAC Reception Error Interrupt Enable While this bit is 1, an interrupt will be generated when the EIS.MREF bit is 1. 0: Disabled 1: Enabled



**37A.2.30 Error Interrupt Status Register (EIS)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

The EIS register indicates the states of AVB-DMAC-related error interrupts.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	QFS
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	TFFF	CULF1	CULF0	CLLF1	CLLF0	SEF	QEF	MTEF	MREF
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 17	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
16	QFS	0	R/W	Queue Full Error Interrupt Status With the interrupts enabled, this bit indicates that a queue is full (the receive queue r full interrupt status bit (QFFr) or the receive FIFO full interrupt status bit (RFFF) in receive interrupt status register 2 (RIS2) = 1). [Conditions for Changing] — If the receive queue r full interrupt status bit (RIS2.QFFr) and/or the receive queue r full interrupt enable bit in the - receive interrupt control register 2 (RIC2.QFEr) are updated, this bit is also updated. — If the receive FIFO full interrupt status bit (RIS2.RFFF) and/or the receive FIFO full interrupt enable bit (RIC2.RFFE) are updated, this bit is also updated. 0: The interrupt is not pending. 1: The interrupt is pending.
15 to 9	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.

Bit	Bit Name	Initial Value	R/W	Description
8	TFFF	0	R/W	<p>Time Stamp FIFO Full Error Interrupt Status</p> <p>This bit indicates that a new transmission time stamp has been discarded due to the time-stamp FIFO being full (i.e. has reached the overflow state).</p> <p>Only 0 can be written to the bit.</p> <p>[Conditions for Changing]</p> <ul style="list-style-type: none"> <li>— The bit is set to 0 when the operating mode is not operation mode.</li> <li>— The bit is set to 1 when a frame with DESCR.TSR set is transmitted while the time stamp FIFO enable bit in the transmit configuration control register (TCCR.TFEN) is set to 1 and the time stamp FIFO count bit in the transmit status register (TSR.TFFL) is set to 2.</li> </ul> <p>0: The interrupt is not pending. 1: The interrupt is pending.</p>
7	CULF1	0	R/W	<p>CBS Upper Limit Error Interrupt Status (Class A)</p> <p>This bit indicates that CBS counter 1 has exceeded the set upper limit (CUL1.ULV in the CBS upper limit register c (CULc)).</p> <p>Only 0 can be written to the bit.</p> <p>[Conditions for Changing]</p> <ul style="list-style-type: none"> <li>— This bit is set to 0 when the operating mode is not operation mode.</li> <li>— This bit is set to 1 when the value of the CBS counter status 1 (Class A) bits in the transmit status register (TSR.CCS1) change from B'00 (indicating a value within the range between the limits) to B'10 (indicating a value over the upper limit).</li> </ul> <p>0: The interrupt is not pending. 1: The interrupt is pending.</p>
6	CULF0	0	R/W	<p>CBS Upper Limit Error Interrupt Status (Class B)</p> <p>This bit indicates that CBS counter 0 has exceeded the set upper limit (CUL0.ULV in the CBS upper limit register c (CULc)).</p> <p>Only 0 can be written to the bit.</p> <p>[Conditions for Changing]</p> <ul style="list-style-type: none"> <li>— The bit is set to 0 when the operating mode is not operation mode.</li> <li>— The bit is set to 1 when the value of the CBS counter status 0 (Class B) bit in the transmit status register changes from B'00 (indicating a value within the range between the limits) to B'10 (indicating a value over the upper limit).</li> </ul> <p>0: The interrupt is not pending. 1: The interrupt is pending.</p>

Bit	Bit Name	Initial Value	R/W	Description
5	CLLF1	0	R/W	<p>CBS Lower Limit Error Interrupt Status (Class A)</p> <p>This bit indicates that CBS counter 1 has fallen below the set lower limit (CLL1.LLV in CBS lower limit register c (CLLc)).</p> <p>Only 0 can be written to the bit.</p> <p>[Conditions for Changing]</p> <ul style="list-style-type: none"> <li>— The bit is set to 0 when the operating mode is not operation mode.</li> <li>— The bit is set to 1 when the value of the CBS counter status 1 (Class A) bit in the transmit status register (TSR.CCS1) changes from B'00 (indicating a value within the range between the limits) to B'01 (indicating a value less than the lower limit).</li> </ul> <p>0: The interrupt is not pending. 1: The interrupt is pending.</p>
4	CLLF0	0	R/W	<p>CBS Lower Limit Error Interrupt Status (Class B)</p> <p>This bit indicates that CBS counter 0 has fallen below the set lower limit (CLL0.LLV in the CBS lower limit register c (CLLc)).</p> <p>Only 0 can be written to the bit.</p> <p>[Conditions for Changing]</p> <ul style="list-style-type: none"> <li>— The bit is set to 0 when the operating mode is not operation mode.</li> <li>— The bit is set to 1 when the value of the CBS counter status 0 (Class B) bit in the transmit status register (TSR.CCS0) changes from B'00 (indicating a value within the range between the limits) to B'01 (indicating a value less than the lower limit).</li> </ul> <p>0: The interrupt is not pending. 1: The interrupt is pending.</p>
3	SEF	0	R/W	<p>Separation Error Flag</p> <p>This bit indicates that a received frame was discarded because it has not matched any configured separation filter for AVB stream data frames.</p> <p>The CPU can only write 0 to this bit.</p> <p>[Conditions for Changing]</p> <ul style="list-style-type: none"> <li>— This bit is set to 0 when leaving operation mode.</li> <li>— This bit is set to 1 when a valid AVB stream data frame was received by E-MAC but discarded because the RCR.ESF bits are B'10 and no separation filter has matched.</li> </ul> <p>0: No interrupt pending. 1: AVB stream data frame has discarded.</p>

Bit	Bit Name	Initial Value	R/W	Description
2	QEF	0	R/W	<p>Queue Error Flag</p> <p>This bit indicates that an error has been detected while processing reception or transmit queue.</p> <p>Details about the detected error is indicated by ESR.</p> <p>Section 7.3 gives an overview of detail error conditions and the required interaction.</p> <p>The CPU can only write 0 to this bit.</p> <p>[Conditions for Changing]</p> <ul style="list-style-type: none"> <li>— This bit is set to 0 when leaving operating mode.</li> <li>— This bit is set to 1 when an error condition is detected.</li> </ul> <p>0: No interrupt pending. 1: Interrupt pending.</p>
1	MTEF	0	R/W	<p>E-MAC Transmission Error Flag</p> <p>This bit indicates that the E-MAC has detected a fault during transmission.</p> <p>For detail, the E-MAC registers have to be checked.</p> <p>The CPU can only write 0 to this bit.</p> <p>[Conditions for Changing]</p> <ul style="list-style-type: none"> <li>— This bit is set to 0 when leaving operating mode.</li> <li>— This bit is set to 1 when E-MAC detects an error during frame transmission.</li> </ul> <p>0: No interrupt pending. 1: E-MAC has reported an error during transmission.</p>
0	MREF	0	R/W	<p>E-MAC Reception Error Flag</p> <p>This bit indicates that the E-MAC has detected a fault during reception.</p> <p>For detail, the E-MAC registers have to be checked.</p> <p>Note: When the storage of faulty received frames (RCR.EFFS) is enabled, the E-MAC error code (DESCR.MSC) is stored in the descriptor. By evaluating this information, CPU can identify corrupted frames in URAM.</p> <p>The CPU can only write 0 to this bit.</p> <p>[Conditions for Changing]</p> <ul style="list-style-type: none"> <li>— This bit is set to 0 when leaving operating mode.</li> <li>— This bit is set to 1 when E-MAC detects an error during frame reception.</li> </ul> <p>0: No interrupt pending. 1: E-MAC has reported an error during reception.</p>

### 37A.2.31 Receive Interrupt Control Register 0 (RIC0)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

The RIC0 register controls the AVB-DMAC receive interrupts.

When an interrupt source flag is set (a bit from among the receive interrupt status bits in the receive interrupt status register (RIS0.FR0 to 17) = 1) while the interrupt is enabled, the interrupt is issued.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FRE17	FRE16
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FRE15	FRE14	FRE13	FRE12	FRE11	FRE10	FRE9	FRE8	FRE7	FRE6	FRE5	FRE4	FRE3	FRE2	FRE1	FRE0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 18	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
17	FRE17	0	R/W	Receive Frame Enable 17 (Stream) 0: Disabled 1: Enabled
16	FRE16	0	R/W	Receive Frame Enable 16 (Stream) 0: Disabled 1: Enabled
15	FRE15	0	R/W	Receive Frame Enable 15 (Stream) 0: Disabled 1: Enabled
14	FRE14	0	R/W	Receive Frame Enable 14 (Stream) 0: Disabled 1: Enabled
13	FRE13	0	R/W	Receive Frame Enable 13 (Stream) 0: Disabled 1: Enabled
12	FRE12	0	R/W	Receive Frame Enable 12 (Stream) 0: Disabled 1: Enabled
11	FRE11	0	R/W	Receive Frame Enable 11 (Stream) 0: Disabled 1: Enabled
10	FRE10	0	R/W	Receive Frame Enable 10 (Stream) 0: Disabled 1: Enabled

Bit	Bit Name	Initial Value	R/W	Description
9	FRE9	0	R/W	Receive Frame Enable 9 (Stream) 0: Disabled 1: Enabled
8	FRE8	0	R/W	Receive Frame Enable 8 (Stream) 0: Disabled 1: Enabled
7	FRE7	0	R/W	Receive Frame Enable 7 (Stream) 0: Disabled 1: Enabled
6	FRE6	0	R/W	Receive Frame Enable 6 (Stream) 0: Disabled 1: Enabled
5	FRE5	0	R/W	Receive Frame Enable 5 (Stream) 0: Disabled 1: Enabled
4	FRE4	0	R/W	Receive Frame Enable 4 (Stream) 0: Disabled 1: Enabled
3	FRE3	0	R/W	Receive Frame Enable 3 (Stream) 0: Disabled 1: Enabled
2	FRE2	0	R/W	Receive Frame Enable 2 (Stream) 0: Disabled 1: Enabled
1	FRE1	0	R/W	Receive Frame Enable 1 (Network Control) 0: Disabled 1: Enabled
0	FRE0	0	R/W	Receive Frame Enable 0 (Best Effort) 0: Disabled 1: Enabled

### 37A.2.32 Receive Interrupt Status Register 0 (RIS0)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

The RIS0 register indicates the states of the AVB-DMAC receive interrupts.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FRF17	FRF16
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FRF15	FRF14	FRF13	FRF12	FRF11	FRF10	FRF9	FRF8	FRF7	FRF6	FRF5	FRF4	FRF3	FRF2	FRF1	FRF0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 18	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
17	FRF17	0	R/W	Receive Frame Interrupt Status 17 (Stream) 0: The interrupt is not pending. 1: The interrupt is pending.
16	FRF16	0	R/W	Receive Frame Interrupt Status 16 (Stream) 0: The interrupt is not pending. 1: The interrupt is pending.
15	FRF15	0	R/W	Receive Frame Interrupt Status 15 (Stream) 0: The interrupt is not pending. 1: The interrupt is pending.
14	FRF14	0	R/W	Receive Frame Interrupt Status 14 (Stream) 0: The interrupt is not pending. 1: The interrupt is pending.
13	FRF13	0	R/W	Receive Frame Interrupt Status 13 (Stream) 0: The interrupt is not pending. 1: The interrupt is pending.
12	FRF12	0	R/W	Receive Frame Interrupt Status 12 (Stream) 0: The interrupt is not pending. 1: The interrupt is pending.
11	FRF11	0	R/W	Receive Frame Interrupt Status 11 (Stream) 0: The interrupt is not pending. 1: The interrupt is pending.
10	FRF10	0	R/W	Receive Frame Interrupt Status 11 (Stream) 0: The interrupt is not pending. 1: The interrupt is pending.
9	FRF9	0	R/W	Receive Frame Interrupt Status 9 (Stream) 0: The interrupt is not pending. 1: The interrupt is pending.

Bit	Bit Name	Initial Value	R/W	Description
8	FRF8	0	R/W	Receive Frame Interrupt Status 8 (Stream) 0: The interrupt is not pending. 1: The interrupt is pending.
7	FRF7	0	R/W	Receive Frame Interrupt Status 7 (Stream) 0: The interrupt is not pending. 1: The interrupt is pending.
6	FRF6	0	R/W	Receive Frame Interrupt Status 6 (Stream) 0: The interrupt is not pending. 1: The interrupt is pending.
5	FRF5	0	R/W	Receive Frame Interrupt Status 5 (Stream) 0: The interrupt is not pending. 1: The interrupt is pending.
4	FRF4	0	R/W	Receive Frame Interrupt Status 4 (Stream) 0: The interrupt is not pending. 1: The interrupt is pending.
3	FRF3	0	R/W	Receive Frame Interrupt Status 3 (Stream) 0: The interrupt is not pending. 1: The interrupt is pending.
2	FRF2	0	R/W	Receive Frame Interrupt Status 2 (Stream) 0: The interrupt is not pending. 1: The interrupt is pending.
1	FRF1	0	R/W	Receive Frame Interrupt Status 1 (Network Control) 0: The interrupt is not pending. 1: The interrupt is pending.
0	FRF0	0	R/W	Receive Frame Interrupt Status 0 (Best Effort) 0: The interrupt is not pending. 1: The interrupt is pending.

#### FRF0 to FRF17 Receive Frame Interrupt Status Bits 0 to 17:

Each bit indicates that a corresponding frame has been stored normally in reception queues 0 to 17 and that data are ready for CPU processing.

Only 0 can be written to the bit.

#### [Conditions for Changing]

- A bit is set to 0 when the operating mode is not operation mode.
- A bit is set to 0 when a value is written to the unread frame counter decrement register  $i$  (UFCD $i$ ) ( $i = 0$  to 4), and this decrements the value of unread frame counter register  $i$  (UFCV $i$ ) ( $i = 0$  to 4) to 0.
- When a frame is stored normally in a reception queue, the corresponding bit is set to 1.



**37A.2.33 Receive Interrupt Control Register 1 (RIC1)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

The RIC1 register controls the AVB-DMAC receive interrupts.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	RFWE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	RFWE	0	R/W	Receive FIFO Warning Interrupt Enable If the reception FIFO reaches the caution level (the value set in the receive FIFO caution level bits in the receive configuration register (RCR.RFCL)) with the corresponding interrupt enabled, the interrupt is issued. 0: Disabled 1: Enabled
30 to 0	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.

**37A.2.34 Receive Interrupt Status Register 1 (RIS1)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

The RIS1 register indicates the states of the AVB-DMAC receive interrupts.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	RFWF	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	RFWF	0	R/W	<p>Receive FIFO Warning Interrupt Status</p> <p>This bit indicates that the reception FIFO has exceeded the set caution level (the value set in the receive FIFO caution level bits in the receive configuration register (RCR.RFCL)).</p> <p>Only 0 can be written to the bit.</p> <p>[Conditions for Changing]</p> <ul style="list-style-type: none"> <li>— The bit is set to 0 when the operating mode is not operation mode.</li> <li>— The bit is set to 1 when the reception FIFO exceeded the set caution level (the value set in the receive FIFO caution level bits in the receive configuration register (RCR.RFCL)).</li> </ul> <p>0: The interrupt is not pending. 1: The interrupt is pending.</p>
30 to 0	—	All 0	R/W	<p>Reserved</p> <p>These bits are read as 0. The write value should be 0.</p>

### 37A.2.35 Receive Interrupt Control Register 2 (RIC2)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

The RIC2 register controls the AVB-DMAC receive interrupts.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	RFFE	—	—	—	—	—	—	—	—	—	—	—	—	—	QFE17	QFE16
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	QFE15	QFE14	QFE13	QFE12	QFE11	QFE10	QFE9	QFE8	QFE7	QFE6	QFE5	QFE4	QFE3	QFE2	QFE1	QFE0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	RFFE	0	R/W	Receive FIFO Full Interrupt Enable When the reception FIFO is full and the interrupt is enabled, the interrupt is issued. 0: Disabled 1: Enabled
30 to 18	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
17	QFE17	0	R/W	Receive Queue 17 (Stream) Full Interrupt Enable When a reception queue is full and the interrupt is enabled, the interrupt is issued. 0: Disabled 1: Enabled
16	QFE16	0	R/W	Receive Queue 16 (Stream) Full Interrupt Enable When a reception queue is full and the interrupt is enabled, the interrupt is issued. 0: Disabled 1: Enabled
15	QFE15	0	R/W	Receive Queue 15 (Stream) Full Interrupt Enable When a reception queue is full and the interrupt is enabled, the interrupt is issued. 0: Disabled 1: Enabled
14	QFE14	0	R/W	Receive Queue 14 (Stream) Full Interrupt Enable When a reception queue is full and the interrupt is enabled, the interrupt is issued. 0: Disabled 1: Enabled

Bit	Bit Name	Initial Value	R/W	Description
13	QFE13	0	R/W	Receive Queue 13 (Stream) Full Interrupt Enable When a reception queue is full and the interrupt is enabled, the interrupt is issued. 0: Disabled 1: Enabled
12	QFE12	0	R/W	Receive Queue 12 (Stream) Full Interrupt Enable When a reception queue is full and the interrupt is enabled, the interrupt is issued. 0: Disabled 1: Enabled
11	QFE11	0	R/W	Receive Queue 11 (Stream) Full Interrupt Enable When a reception queue is full and the interrupt is enabled, the interrupt is issued. 0: Disabled 1: Enabled
10	QFE10	0	R/W	Receive Queue 10 (Stream) Full Interrupt Enable When a reception queue is full and the interrupt is enabled, the interrupt is issued. 0: Disabled 1: Enabled
9	QFE9	0	R/W	Receive Queue 9 (Stream) Full Interrupt Enable When a reception queue is full and the interrupt is enabled, the interrupt is issued. 0: Disabled 1: Enabled
8	QFE8	0	R/W	Receive Queue 8 (Stream) Full Interrupt Enable When a reception queue is full and the interrupt is enabled, the interrupt is issued. 0: Disabled 1: Enabled
7	QFE7	0	R/W	Receive Queue 7 (Stream) Full Interrupt Enable When a reception queue is full and the interrupt is enabled, the interrupt is issued. 0: Disabled 1: Enabled
6	QFE6	0	R/W	Receive Queue 6 (Stream) Full Interrupt Enable When a reception queue is full and the interrupt is enabled, the interrupt is issued. 0: Disabled 1: Enabled
5	QFE5	0	R/W	Receive Queue 5 (Stream) Full Interrupt Enable When a reception queue is full and the interrupt is enabled, the interrupt is issued. 0: Disabled 1: Enabled

Bit	Bit Name	Initial Value	R/W	Description
4	QFE4	0	R/W	Receive Queue 4 (Stream) Full Interrupt Enable When a reception queue is full and the interrupt is enabled, the interrupt is issued. 0: Disabled 1: Enabled
3	QFE3	0	R/W	Receive Queue 3 (Stream) Full Interrupt Enable When a reception queue is full and the interrupt is enabled, the interrupt is issued. 0: Disabled 1: Enabled
2	QFE2	0	R/W	Receive Queue 2 (Stream) Full Interrupt Enable When a reception queue is full and the interrupt is enabled, the interrupt is issued. 0: Disabled 1: Enabled
1	QFE1	0	R/W	Receive Queue 1 (Network Control) Full Interrupt Enable When a reception queue is full and the interrupt is enabled, the interrupt is issued. 0: Disabled 1: Enabled
0	QFE0	0	R/W	Receive Queue 0 (Best Effort) Full Interrupt Enable When a reception queue is full and the interrupt is enabled, the interrupt is issued. 0: Disabled 1: Enabled

### 37A.2.36 Receive Interrupt Status Register 2 (RIS2)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

The RIS2 register indicates the states of the AVB-DMAC receive interrupts.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	RFFF	—	—	—	—	—	—	—	—	—	—	—	—	—	QFF17	QFF16
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	QFF15	QFF14	QFF13	QFF12	QFF11	QFF10	QFF9	QFF8	QFF7	QFF6	QFF5	QFF4	QFF3	QFF2	QFF1	QFF0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	RFFF	0	R/W	<p>Receive FIFO Full Interrupt Status</p> <p>This bit indicates that a frame was received but storing it was not possible due to the reception FIFO being full.</p> <p>When receiving a frame is not possible, the frame will be discarded. Other information regarding discarded frames is not retained. Even if the frame is discarded, this bit may also be set to 1 if the E-MAC determines that the frame is an error frame</p> <p>Only 0 can be written to the bit.</p> <p>[Conditions for Changing]</p> <ul style="list-style-type: none"> <li>— The bit is set to 0 when the operating mode is not operation mode.</li> <li>— The bit is set to 1 when frame data provided by the E-MAC cannot be stored in the reception FIFO.</li> </ul> <p>0: The interrupt is not pending. 1: The interrupt is pending</p>
30 to 18	—	All 0	R/W	<p>Reserved</p> <p>These bits are read as 0. The write value should be 0.</p>
17	QFF17	0	R/W	<p>Receive Queue 17 (Stream) Full Interrupt Status</p> <p>0: The interrupt is not pending. 1: The interrupt is pending.</p>
16	QFF16	0	R/W	<p>Receive Queue 16 (Stream) Full Interrupt Status</p> <p>0: The interrupt is not pending. 1: The interrupt is pending.</p>
15	QFF15	0	R/W	<p>Receive Queue 15 (Stream) Full Interrupt Status</p> <p>0: The interrupt is not pending. 1: The interrupt is pending.</p>
14	QFF14	0	R/W	<p>Receive Queue 14 (Stream) Full Interrupt Status</p> <p>0: The interrupt is not pending. 1: The interrupt is pending.</p>

Bit	Bit Name	Initial Value	R/W	Description
13	QFF13	0	R/W	Receive Queue 13 (Stream) Full Interrupt Status 0: The interrupt is not pending. 1: The interrupt is pending.
12	QFF12	0	R/W	Receive Queue 12 (Stream) Full Interrupt Status 0: The interrupt is not pending. 1: The interrupt is pending.
11	QFF11	0	R/W	Receive Queue 11 (Stream) Full Interrupt Status 0: The interrupt is not pending. 1: The interrupt is pending.
10	QFF10	0	R/W	Receive Queue 10 (Stream) Full Interrupt Status 0: The interrupt is not pending. 1: The interrupt is pending.
9	QFF9	0	R/W	Receive Queue 9 (Stream) Full Interrupt Status 0: The interrupt is not pending. 1: The interrupt is pending.
8	QFF8	0	R/W	Receive Queue 8 (Stream) Full Interrupt Status 0: The interrupt is not pending. 1: The interrupt is pending.
7	QFF7	0	R/W	Receive Queue 7 (Stream) Full Interrupt Status 0: The interrupt is not pending. 1: The interrupt is pending.
6	QFF6	0	R/W	Receive Queue 6 (Stream) Full Interrupt Status 0: The interrupt is not pending. 1: The interrupt is pending.
5	QFF5	0	R/W	Receive Queue 5 (Stream) Full Interrupt Status 0: The interrupt is not pending. 1: The interrupt is pending.
4	QFF4	0	R/W	Receive Queue 4 (Stream) Full Interrupt Status 0: The interrupt is not pending. 1: The interrupt is pending.
3	QFF3	0	R/W	Receive Queue 3 (Stream) Full Interrupt Status 0: The interrupt is not pending. 1: The interrupt is pending.
2	QFF2	0	R/W	Receive Queue 2 (Stream) Full Interrupt Status 0: The interrupt is not pending. 1: The interrupt is pending.
1	QFF1	0	R/W	Receive Queue 1 (Network Control) Full Interrupt Status 0: The interrupt is not pending. 1: The interrupt is pending.
0	QFF0	0	R/W	Receive Queue 0 (Best Effort) Full Interrupt Status 0: The interrupt is not pending. 1: The interrupt is pending.

**QFF0 to 17 Receive 0 to 17 Full Interrupt Status Bits:**

These bits indicate that reception queue *r* did not have space for storing a received frame.

A reception queue is treated as full when it has no descriptors (descriptor type (DESCR.DT) = FEMPTY, FEMPTY\_IS, FEMPTY\_IC, or FEMPTY\_ND) available or reaches the set level for stopping.

Note: If no FEMPTY descriptors or no empty space for descriptors remains in the queue during storing of a divided frame (see section 37A.3.4.3 (1) (b) Storing Frame Data as Divided Frames, for storing a frame as a divided frame), an error frame is stored in the queue. Such error frames are treated as descriptor sequence errors.

**[Conditions for Changing]**

- A bit is set to 0 when the operating mode is not operation mode.
- A bit is set to 1 when reception queue *r* has no space available for storage.
- A bit is set to 1 when the unread frame counter (unread frame counter register *i* (UFCVi) (*i* = 0 to 4)) reaches the set level for stopping.



**37A.2.37 Transmit Interrupt Control Register (TIC)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

The TIC register controls the AVB-DMAC transmit interrupts.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	TFWE	TFUE	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 10	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
9	TFWE	0	R/W	Time Stamp FIFO Warning Interrupt Enable When the time-stamp FIFO reaches the warning level while the interrupt is enabled, the interrupt is issued. 0: Disabled 1: Enabled
8	TFUE	0	R/W	Time Stamp FIFO Update Interrupt Enable When the time-stamp FIFO is updated while the interrupt is enabled, the interrupt is issued. 0: Disabled 1: Enabled
7 to 0	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.

### 37A.2.38 Transmit Interrupt Status Register (TIS)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

The TIS register indicates the states of the AVB-DMAC transmit interrupts.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	TFWF	TFUF	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 10	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
9	TFWF	0	R/W	Time Stamp FIFO Warning Interrupt Status This bit indicates that the transmission time-stamp FIFO has reached the warning level. Only 0 can be written to the bit. [Conditions for Changing] <ul style="list-style-type: none"> <li>— The bit is set to 0 when the operating mode is not operation mode and when the time stamp FIFO enable bit in the transmit configuration control register (TCCR.TFEN) is 0.</li> <li>— The bit is set to 1 after a frame including DESCR.TSR set has been transmitted and one entry has already been stored in the time-stamp FIFO.</li> </ul> 0: The interrupt is not pending. 1: The time-stamp FIFO has reached the warning level.
8	TFUF	0	R/W	Time Stamp FIFO Update Interrupt Status This bit indicates that the transmission time-stamp FIFO has been updated. Only 0 can be written to the bit. [Conditions for Changing] <ul style="list-style-type: none"> <li>— The bit is set to 0 when the operating mode is not operation mode, when the time stamp FIFO enable bit in the transmit configuration control register (TCCR.TFEN) is 0, and when 1 is written to the time stamp FIFO release bit in the transmit configuration control register (TCCR.TFR).</li> <li>— The bit is set to 1 when the time stamp FIFO enable bit (TCCR.TFEN) is 1 after a frame including DESCR.TSR set has been transmitted.</li> </ul> 0: The interrupt is not pending. 1: The time-stamp FIFO has been updated.

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Bit	Bit Name	Initial Value	R/W	Description
7 to 0	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.

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### 37A.2.39 Interrupt Summary Status Register (ISS)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

The ISS register gives a summary of the states of AVB-DMAC-related interrupts.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DPS15	DPS14	DPS13	DPS12	DPS11	DPS10	DPS9	DPS8	DPS7	DPS6	DPS5	DPS4	DPS3	DPS2	DPS1	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	CGIS	RFWS	—	—	TFWS	TFUS	MS	ES	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31	DPS15	0	R/W	<p>Descriptor Interrupt 15 Summary</p> <p>This bit is set to 1 when the given descriptor interrupt enable bit (DIC.DPE15) and descriptor interrupt status flag (DIS.DPF15) are both 1.</p> <p>0: The interrupt is not pending. 1: The interrupt is pending.</p>
30	DPS14	0	R/W	<p>Descriptor Interrupt 14 Summary</p> <p>This bit is set to 1 when the given descriptor interrupt enable bit (DIC.DPE14) and descriptor interrupt status flag (DIS.DPF14) are both 1.</p> <p>0: The interrupt is not pending. 1: The interrupt is pending.</p>
29	DPS13	0	R/W	<p>Descriptor Interrupt 13 Summary</p> <p>This bit is set to 1 when the given descriptor interrupt enable bit (DIC.DPE13) and descriptor interrupt status flag (DIS.DPF13) are both 1.</p> <p>0: The interrupt is not pending. 1: The interrupt is pending.</p>
28	DPS12	0	R/W	<p>Descriptor Interrupt 12 Summary</p> <p>This bit is set to 1 when the given descriptor interrupt enable bit (DIC.DPE12) and descriptor interrupt status flag (DIS.DPF12) are both 1.</p> <p>0: The interrupt is not pending. 1: The interrupt is pending.</p>
27	DPS11	0	R/W	<p>Descriptor Interrupt 11 Summary</p> <p>This bit is set to 1 when the given descriptor interrupt enable bit (DIC.DPE11) and descriptor interrupt status flag (DIS.DPF11) are both 1.</p> <p>0: The interrupt is not pending. 1: The interrupt is pending.</p>

Bit	Bit Name	Initial Value	R/W	Description
26	DPS10	0	R/W	<p>Descriptor Interrupt 10 Summary</p> <p>This bit is set to 1 when the given descriptor interrupt enable bit (DIC.DPE10) and descriptor interrupt status flag (DIS.DPF10) are both 1.</p> <p>0: The interrupt is not pending. 1: The interrupt is pending.</p>
25	DPS9	0	R/W	<p>Descriptor Interrupt 9 Summary</p> <p>This bit is set to 1 when the given descriptor interrupt enable bit (DIC.DPE9) and descriptor interrupt status flag (DIS.DPF9) are both 1.</p> <p>0: The interrupt is not pending. 1: The interrupt is pending.</p>
24	DPS8	0	R/W	<p>Descriptor Interrupt 8 Summary</p> <p>This bit is set to 1 when the given descriptor interrupt enable bit (DIC.DPE8) and descriptor interrupt status flag (DIS.DPF8) are both 1.</p> <p>0: The interrupt is not pending. 1: The interrupt is pending.</p>
23	DPS7	0	R/W	<p>Descriptor Interrupt 7 Summary</p> <p>This bit is set to 1 when the given descriptor interrupt enable bit (DIC.DPE7) and descriptor interrupt status flag (DIS.DPF7) are both 1.</p> <p>0: The interrupt is not pending. 1: The interrupt is pending.</p>
22	DPS6	0	R/W	<p>Descriptor Interrupt 6 Summary</p> <p>This bit is set to 1 when the given descriptor interrupt enable bit (DIC.DPE6) and descriptor interrupt status flag (DIS.DPF6) are both 1.</p> <p>0: The interrupt is not pending. 1: The interrupt is pending.</p>
21	DPS5	0	R/W	<p>Descriptor Interrupt 5 Summary</p> <p>This bit is set to 1 when the given descriptor interrupt enable bit (DIC.DPE5) and descriptor interrupt status flag (DIS.DPF5) are both 1.</p> <p>0: The interrupt is not pending. 1: The interrupt is pending.</p>
20	DPS4	0	R/W	<p>Descriptor Interrupt 4 Summary</p> <p>This bit is set to 1 when the given descriptor interrupt enable bit (DIC.DPE4) and descriptor interrupt status flag (DIS.DPF4) are both 1.</p> <p>0: The interrupt is not pending. 1: The interrupt is pending.</p>
19	DPS3	0	R/W	<p>Descriptor Interrupt 3 Summary</p> <p>This bit is set to 1 when the given descriptor interrupt enable bit (DIC.DPE3) and descriptor interrupt status flag (DIS.DPF3) are both 1.</p> <p>0: The interrupt is not pending. 1: The interrupt is pending.</p>

Bit	Bit Name	Initial Value	R/W	Description
18	DPS2	0	R/W	<p>Descriptor Interrupt 2 Summary</p> <p>This bit is set to 1 when the given descriptor interrupt enable bit (DIC.DPE2) and descriptor interrupt status flag (DIS.DPF2) are both 1.</p> <p>0: The interrupt is not pending. 1: The interrupt is pending.</p>
17	DPS1	0	R/W	<p>Descriptor Interrupt 1 Summary</p> <p>This bit is set to 1 when the given descriptor interrupt enable bit (DIC.DPE1) and descriptor interrupt status flag (DIS.DPF1) are both 1.</p> <p>0: The interrupt is not pending. 1: The interrupt is pending.</p>
16 to 14	—	All 0	R/W	<p>Reserved</p> <p>These bits are read as 0. The write value should be 0.</p>
13	CGIS	0	R/W	<p>gPTP Interrupt Summary</p> <p>This bit is set to 1 when either interrupt-related bit in the two gPTP-related interrupt registers (GIC and GIS) is 1.</p> <p>0: The interrupt is not pending. 1: The interrupt is pending.</p>
12	RFWS	0	R/W	<p>Receive FIFO Warning Interrupt Summary</p> <p>This bit is set to 1 when the receive FIFO warning interrupt enable bit (RIC1.RFWE) and receive FIFO warning interrupt status flag (RIS1.RFWF) are both 1.</p> <p>0: The interrupt is not pending. 1: The interrupt is pending.</p>
11, 10	—	All 0	R/W	<p>Reserved</p> <p>These bits are read as 0. The write value should be 0.</p>
9	TFWS	0	R/W	<p>Time Stamp FIFO Warning Interrupt Summary</p> <p>This bit is set to 1 when the time stamp FIFO warning interrupt enable bit (TIC.TFWE) and time stamp FIFO warning interrupt status flag (TIS.TFWF) are both 1.</p> <p>0: The interrupt is not pending. 1: The interrupt is pending.</p>
8	TFUS	0	R/W	<p>Time Stamp FIFO Update Interrupt</p> <p>This bit is set to 1 when the time stamp FIFO update interrupt enable bit (TIC.TFUE) and time stamp FIFO update interrupt status flag (TIS.TFUF) are both 1.</p> <p>0: The interrupt is not pending. 1: The interrupt is pending.</p>
7	MS	0	R/W	<p>E-MAC Interrupt Summary</p> <p>This bit is set to 1 when an E-MAC interrupt is issued.</p> <p>0: The interrupt is not pending. 1: The interrupt is pending.</p>
6	ES	0	R/W	<p>Error Interrupt Summary</p> <p>This bit is set to 1 when an error interrupt is issued (both of a bit in EIS and corresponding to the bit in EIC are 1).</p> <p>0: The interrupt is not pending. 1: The interrupt is pending.</p>

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Bit	Bit Name	Initial Value	R/W	Description
5 to 0	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.

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### 37A.2.40 gPTP Configuration Control Register (GCCR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

The GCCR register is used to set and control the gPTP (generalized precision time protocol).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	TCSS[1:0]	—	—	LMTT	LPTC	LTI	LTO	TCR[1:0]	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 10	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
9, 8	TCSS[1:0]	00	R/W	Timer Capture Source Select These bits select the source used for updating the captured timer register (gPTP timer capture register (GCTi.CTV)). These bits should still be controlled when timer control is not being requested (GCCR.TCR = 0). 00: gPTP timer value 01: Adjusted gPTP timer value 10: AVTP presentation time 11: Setting prohibited
7, 6	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
5	LMTT	1	R/W	Maximum Transit Time Configuration Request This bit issues requests for configuring the gPTP maximum transit time configuration register (GMTT). Only 1 can be written to the bit. [Conditions for Changing] — The bit is set to 1 when the operating mode is not operation mode. — The bit is set to 0 when the value of the gPTP maximum transit time configuration register (GMTT) is loaded. 0: Setting completed 1: When written: Issue a configuration request. When read: Completion of settings is pending.



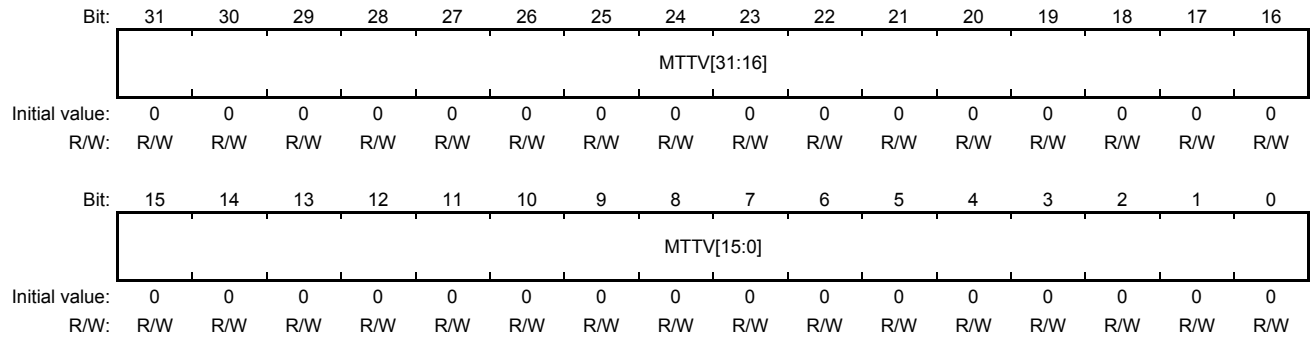
Bit	Bit Name	Initial Value	R/W	Description
4	LPTC	1	R/W	<p>Presentation Time Compare Value Configuration Request</p> <p>This bit issues requests for configuring the gPTP presentation time comparison register (GPTC).</p> <p>Only 1 can be written to the bit.</p> <p>[Conditions for Changing]</p> <ul style="list-style-type: none"> <li>— The bit is set to 1 when the operating mode is not operation mode.</li> <li>— The bit is set to 0 when the value of the gPTP presentation time comparison register (GPTC) is loaded.</li> </ul> <p>0: Setting completed 1: When written: Issue a configuration request. When read: Completion of settings is pending.</p>
3	LTI	1	R/W	<p>Timer Increment Value Configuration Request</p> <p>This bit issues requests for configuring the gPTP timer increment configuration register (GTI).</p> <p>Only 1 can be written to the bit.</p> <p>[Conditions for Changing]</p> <ul style="list-style-type: none"> <li>— The bit is set to 1 when the operating mode is not operation mode.</li> <li>— The bit is set to 0 when the value of the gPTP timer increment configuration register (GTI) is loaded.</li> </ul> <p>0: Setting completed 1: When written: Issue a configuration request. When read: Completion of settings is pending.</p>
2	LTO	1	R/W	<p>Timer Offset Value Configuration Request</p> <p>This bit issues requests for configuring gPTP timer offset configuration register i (GTOi).</p> <p>Only 1 can be written to the bit.</p> <p>[Conditions for Changing]</p> <ul style="list-style-type: none"> <li>— The bit is set to 1 when the operating mode is not operation mode.</li> <li>— The bit is set to 0 when the value of gPTP timer offset configuration register i (GTOi) is loaded.</li> </ul> <p>0: Setting completed 1: When written: Issue a configuration request. When read: Completion of settings is pending.</p>

Bit	Bit Name	Initial Value	R/W	Description
1, 0	TCR[1:0]	00	R/W	<p>Timer Control Request</p> <p>These bits issue requests for controlling the gPTP timer.</p> <p>Writing to the bits is only possible when the current operating mode is operation mode.</p> <p>Do not write to the bit when the gPTP timer clock select bit in the AVB-DMAC mode register is B'00. Write to these bits while GCCR.TCR is B'00.</p> <p>[Conditions for Changing]</p> <ul style="list-style-type: none"> <li>— The bits are set to B'00 when the operating mode is not operation mode.</li> <li>— The bits are also set to B'00 on completion of the requested processing.</li> </ul> <p>00: Timer control is not requested.            01: gPTP/AVTP presentation time reset            10: Setting prohibited            11: Captures the value set in the TCSS bit.</p>

**37A.2.41 gPTP Maximum Transit Time Configuration Register (GMTT)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

The GMTT register sets the maximum time for transitions of the gPTP timer.



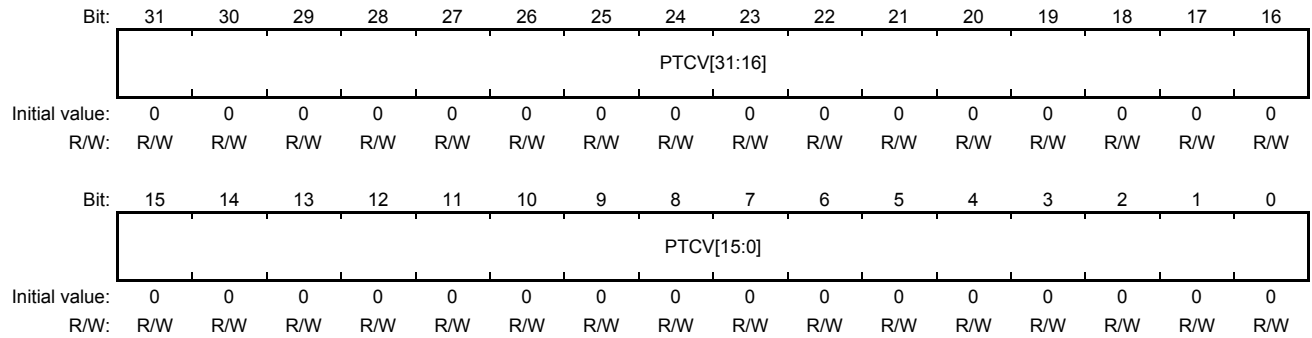
Bit	Bit Name	Initial Value	R/W	Description
31 to 0	MTTV[31:0]	H'0000 0000	R/W	<p>Maximum Transit Time</p> <p>These bits set the maximum transition time for use in calculating AVTP presentation time.</p> <p>Write the desired setting to the bits, then issue the configuration request by setting the maximum transit time configuration request bit in the gPTP configuration control register (GCCR.LMTT) to 1.</p>

Note: Do not write a value to these bits when the operating mode is operation mode and the maximum transit time configuration request bit (GCCR.LMTT) is 1.

**37A.2.42 gPTP Presentation Time Comparison Register (GPTC)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

The GPTC register sets a value for comparison with presentation times in the gPTP timer.



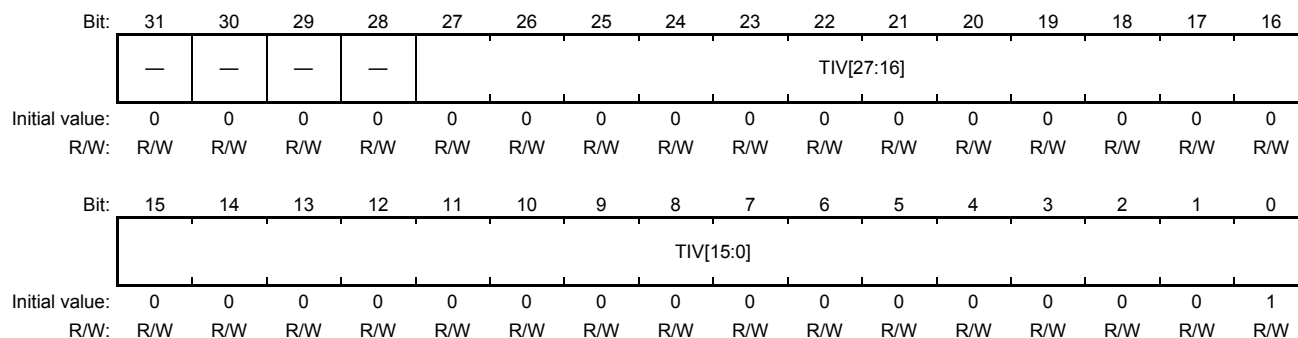
Bit	Bit Name	Initial Value	R/W	Description
31 to 0	PTCV[31:0]	H'0000 0000	R/W	<p>Presentation Time Comparison Value</p> <p>These bits set a value for comparison with AVTP timer values to which a maximum transit time is not appended.</p> <p>Write the desired setting to the bits, then issue the configuration request by setting the presentation time comparison value configuration request bit in the gPTP configuration control register (GCCR.LPTC) to 1.</p>

**Note:** Do not write a value to these bits when the operating mode is operation mode and the presentation time comparison value configuration request bit (GCCR.LPTC) is 1.

### 37A.2.43 gPTP Timer Increment Configuration Register (GTI)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

The GTI register sets the increment for the gPTP timer.



Bit	Bit Name	Initial Value	R/W	Description
31 to 28	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
27 to 0	TIV[27:0]	H'000 0001	R/W	gPTP Timer Increment Value When the gPTP clock select bits in the AVB-DMAC mode register (CCC.CSEL) are selecting a clock signal, these bits set the value by which the timer is incremented each time a cycle of that clock signal elapses. Write the desired setting to the bits, then issue the configuration request by setting the timer increment value configuration request bit in the gPTP configuration control register (GCCR.LTI) to 1.

Note: Do not write a value to these bits when the operating mode is operation mode and the timer increment value configuration request bit (GCCR.LTI) is 1.

Do not write 0 to the bits.

Keep comparison value in the following range

$$x \leq \text{comparison\_value} \leq 2^{32} - x$$

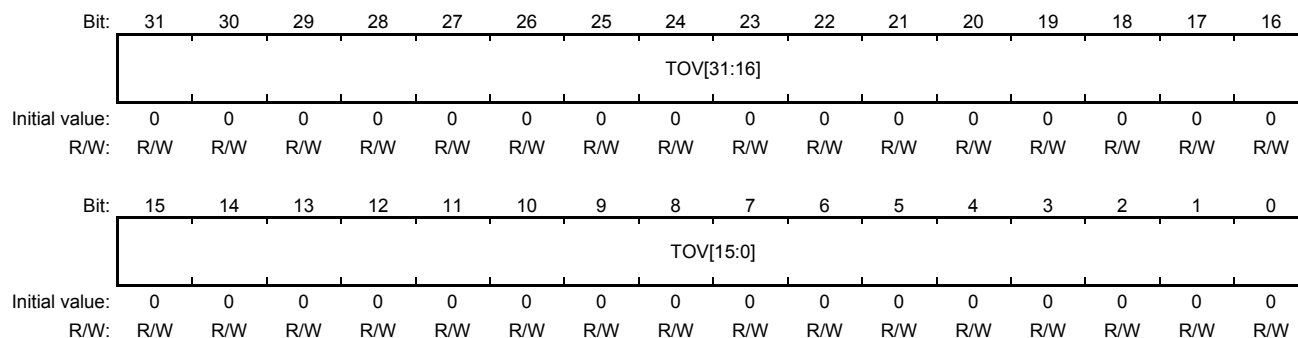
, where x is amount of nanoseconds of the configured increment value in GTI.TIV

**37A.2.44 gPTP Timer Offset Configuration Register i (GTOi) (i = 0 to 2)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

The GTOi register sets an offset value for the gPTP timer.

The offset value is added to the combination of bits 0 to 31 in GTO0, 32 to 63 in GTO1, and 64 to 79 in GTO2, which together make up the gPTP timer.



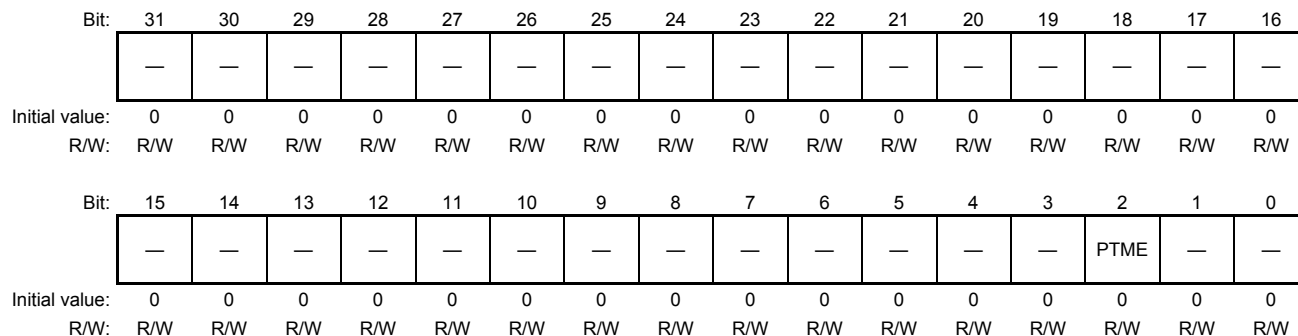
Bit	Bit Name	Initial Value	R/W	Description
31 to 0	TOV[31:0]	H'0000 0000	R/W	<p>Timer Offset Value</p> <p>This is an 80-bit value consisting of the settings in GTO0.TOV[31:0], GTO1.TOV[63:32], and GTO2.TOV[79:64], and is used to set an offset for adding to the value of the gPTP timer.</p> <p>Write the desired setting to the bits, then issue the configuration request by setting the timer offset value configuration request bit in the gPTP configuration control register (GCCR.LTO) to 1.</p>

Note: Do not write a value to these bits when the operating mode is operation mode and the timer offset value configuration request bit (GCCR.LTO) is 1. Write H'0000 to GTO2.TOV[95:80]. Set a value in the range from 0 to 10<sup>9</sup>-1 (H'0000 0000 to H'3B9A C9FF) in GTOi.TOV[31:0].

**37A.2.45 gPTP Interrupt Control Register (GIC)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

The GCI register is used to control gPTP-related interrupts.

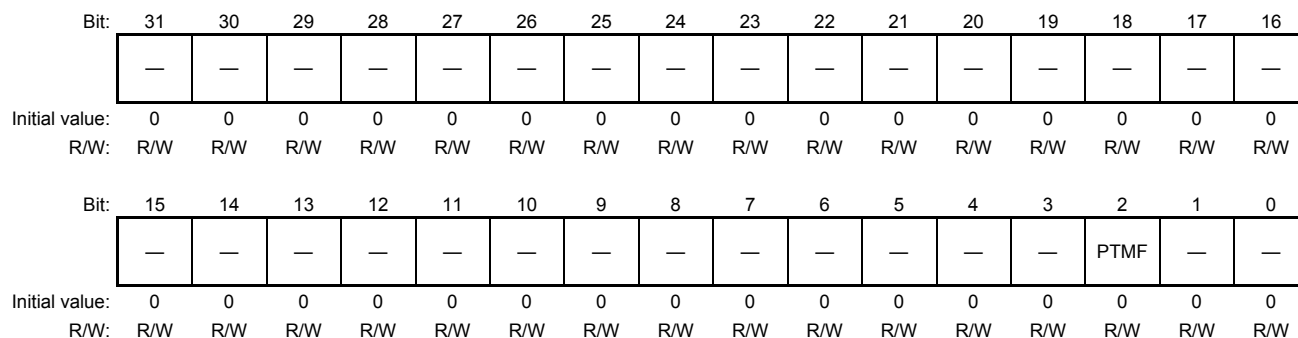


Bit	Bit Name	Initial Value	R/W	Description
31 to 3	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
2	PTME	0	R/W	Presentation Time Match Interrupt Enable When this bit is 1, setting of the presentation time match interrupt flag in the gPTP interrupt status register (GIS.PTMF) to 1 leads to generation of that interrupt. 0: Disabled 1: Enabled
1, 0	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.

### 37A.2.46 gPTP Interrupt Status Register (GIS)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

The GIC register indicates the state of the gPTP-related interrupt.



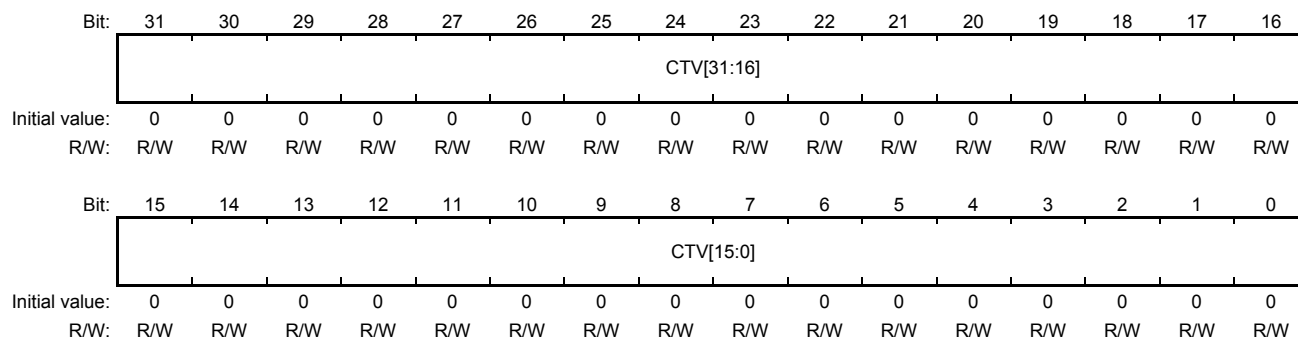
Bit	Bit Name	Initial Value	R/W	Description
31 to 3	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
2	PTMF	0	R/W	Presentation Time Match Interrupt Flag This bit indicates that the value of the AVTP timer exceeds the value of the gPTP presentation time comparison register (GPTC). Only 0 can be written to the bit. [Conditions for Changing] <ul style="list-style-type: none"> <li>— The bit is set to 0 when the operating mode is not operation mode.</li> <li>— The bit is set to 1 when the AVTP timer value is greater than or equal to the value of the gPTP presentation time comparison register (GPTC).</li> </ul> 0: The interrupt is not pending. 1: The interrupt is pending.
1, 0	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.



**37A.2.47 gPTP Timer Capture Register i (GCTi) (i = 0 to 2)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

The GCTi registers form an 80-bit register that captures the gPTP timer value.



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	CTV[31:0]	H'0000 0000	R/W	<p><b>gPTP Timer Capture Value</b></p> <p>These 80 bits consist of GCT0.CTV[31:0], GCT1.CTV[63:32 and GCT2.CTV[79:64], which together indicate captured timer values.</p> <p>When B'00 (value of the gPTP timer) or B'01 (adjusted gPTP timer value) is selected by the timer capture source select bits in the gPTP configuration control register, the corresponding 80-bit values are stored in these bits.</p> <p>When B'10 (AVTP presentation time) is selected by the timer capture source select bit, the corresponding 32-bit values are stored in these bits.</p> <p>Actual writing of the timer value specified by the timer capture source select bits (GCCR.TCSS) proceeds when B'11 (timer capture request) is written to the timer control request bits in the gPTP configuration control register (GCCR.TCR).</p> <p>Do not read the value while the value of the timer control request bits (GCCR.TCR) is B'11, because this indicates that storage is still in progress.</p>

### 37A.2.48 E-MAC Mode Register (ECMR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

ECMR is used to specify the operating mode of the E-MAC. The settings in this register are normally made in the initialization process following a reset.

The operating mode settings must not be changed while transmission or reception is enabled (i.e. while the RE or TE bit in this register is 1).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	TRCC M	—	—	RCSC	—	DPAD	RZPF	—	PFR	RXF	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	MPDE	—	—	RE	TE	—	—	—	DM	PRM
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 27	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
26	TRCCM	0	R/W	Counter Clear Mode This bit sets the method for clearing the counter register. Refer to the descriptions of the counter registers. 0: Writing to a counter register leads to the register being cleared to 0. 1: Reading from a counter register leads to the register being cleared to 0.
25, 24	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
23	RCSC	0	R/W	Checksum Calculation Setting this bit to 1 enables automatic calculation of checksums for data in received frames. Only the data field of an Ethernet frame without a VLAN field is in the scope of checksum calculation. Specifically, the checksum is calculated from the data field, which follows the length/type field and is followed by the CRC field. Calculation only involves 16-bit addition; it does not involve bit inversion. 0: Checksums are not automatically calculated. 1: Checksums are automatically calculated.
22	—	0	R/W	Reserved This bit is read as 0. The write value should be 0.

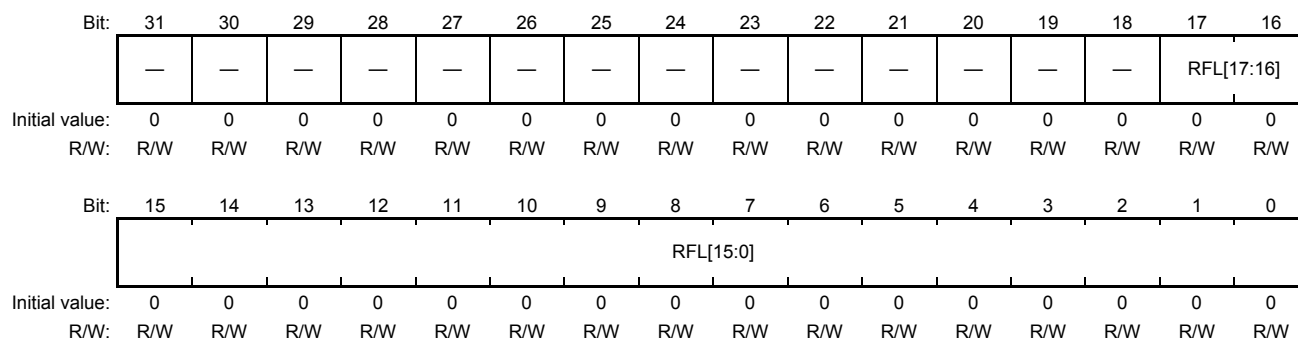
Bit	Bit Name	Initial Value	R/W	Description
21	DPAD	0	R/W	<p>Data Padding</p> <p>This bit specifies padding or non-padding of data when less than 60 bytes are to be transmitted.</p> <p>When this bit is set to 1, data are transmitted without padding; when it is set to 0, data are padded to make up 60-byte units for transmission.</p> <p>0: Padding to make up 60 bytes is inserted in data for transmission when fewer than 60 bytes are to be transmitted.</p> <p>1: Padding is not inserted in data for transmission when fewer than 60 bytes are to be transmitted and the data are transmitted without being changed.</p>
20	RZPF	0	R/W	<p>PAUSE Frame Reception with Time = 0</p> <p>When the RZPF bit is set to 0, received PAUSE frames with the Timer value 0 are discarded.</p> <p>When the RZPF bit is set to 1, release from the transmission wait state follows reception of a PAUSE frame with the Timer value 0.</p> <p>0: Reception of PAUSE frames with the TIME parameter value 0 is disabled.</p> <p>1: Reception of PAUSE frames with the TIME parameter value 0 is enabled.</p>
19	—	0	R/W	<p>Reserved</p> <p>This bit is read as 0. The write value should be 0.</p>
18	PFR	0	R/W	<p>PAUSE Frame Receive Mode</p> <p>This bit specifies whether PAUSE frames are transferred to the AVB-DMAC.</p> <p>0: PAUSE frames are not transferred to the AVB-DMAC.</p> <p>1: PAUSE frames are transferred to the AVB-DMAC.</p>
17	RXF	0	R/W	<p>Operating Mode for Flow Control in Reception</p> <p>When the RXF bit is set to 1 and a PAUSE frame is received, a next frame to be transmitted is not transmitted until the time indicated by the Timer value in the PAUSE frame has elapsed. However, the transmission of a current frame is continued. The number of received PAUSE frames is also counted. For details, see section 37A.2.57, PAUSE Frame Receive Counter (PFRCR).</p> <p>Setting this bit to 0 disables PAUSE frame detection.</p> <p>0: Detection of PAUSE frames is disabled.</p> <p>1: Flow control for the receiving port is enabled.</p>
16 to 10	—	All 0	R/W	<p>Reserved</p> <p>These bits are read as 0. The write value should be 0.</p>
9	MPDE	0	R/W	<p>Magic Packet™ Detection Enable</p> <p>The MPDE bit enables or disables Magic Packet™ detection by hardware to allow activation via the Ethernet connection.</p> <p>0: Magic Packet™ detection is not enabled.</p> <p>1: Magic Packet™ detection is enabled.</p>
8, 7	—	All 0	R/W	<p>Reserved</p> <p>These bits are read as 0. The write value should be 0.</p>

Bit	Bit Name	Initial Value	R/W	Description
6	RE	0	R/W	<p>Reception Enable</p> <p>If this bit is switched from reception being enabled (RE = 1) to reception being disabled (RE = 0) while a frame is being received, reception will continue until reception of the frame is completed.</p> <p>0: Reception is disabled. 1: Reception is enabled.</p>
5	TE	0	R/W	<p>Transmission Enable</p> <p>If this bit is switched from transmission being enabled (TE = 1) to transmission being disabled (TE = 0) while a frame is being transmitted, transmission will continue until transmission of that frame is completed.</p> <p>0: Transmission is disabled. 1: Transmission is enabled.</p>
4 to 2	—	All 0	R/W	<p>Reserved</p> <p>These bits are read as 0. The write value should be 0.</p>
1	DM	0	R/W	<p>Duplex Mode</p> <p>This bit should always be set to 1. The value after reset is 0.</p> <p>0: Value after reset 1: Full-duplex operation</p> <p>This bit should always be set to 1.</p>
0	PRM	0	R/W	<p>Promiscuous Mode</p> <p>Setting the PRM bit enables all Ethernet frames to be received. All Ethernet frames mean all receivable frames, irrespective of differences of destination address (exclude PAUSE frame).</p> <p>0: Normal operation 1: Promiscuous mode operation</p>

### 37A.2.49 Receive Frame Length Register (RFLR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

The RFLR register specifies the maximum length (in bytes) of frames that can be received by this LSI. Settings in this register must not be changed while reception is enabled (while the RE bit in the E-MAC mode register (EMCR) is 1).



Bit	Bit Name	Initial Value	R/W	Description
31 to 18	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
17 to 0	RFL[17:0]	H'0 0000	R/W	Receive Frame Length Frame data described here refers to all fields from the destination address up to the CRC data. Frame contents from the destination address up to the data are actually transferred to memory. CRC data are not included in the transfer. When more data than the specified number of bytes are received, the portion of data that exceeds the specified value and more 8 byte length is discarded. CAUTION: The prepared descriptor data size is just the specified value (RFLR.RFL). Therefore descriptor data size must be more than RFLR.RFL + 8 if you will receive such the long frame. H'00000 to H'005EE: 1,518 bytes H'005EF: 1,519 bytes H'005F0: 1,520 bytes : : H'007FF: 2,047 bytes H'00800: 2,048 bytes : : H'01000: 4,096 bytes : : H'10000: 65,535 bytes : : H'20000 to H'3FFFF: 131,072 bytes

### 37A.2.50 E-MAC Status Register (ECSR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

The ECSR register indicates the state of the E-MAC. The CPU can be notified of the state. For bits associated with interrupts, the interrupt can be enabled or disabled by the corresponding bit in the E-MAC Interrupt Permission Register (ECSIPR) described in section 37A.2.51.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	PHYI	LCHNG	MPD	ICD
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 4	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
3	PHYI	0	R/W	PHY interrupt terminal state bit This bit indicates the state of input to the PHY interrupt pin (AVB_PHY_INT) from the PHY-LSI. 0: PHY interrupt terminal (AVB_PHY_INT) is not asserted. 1: PHY interrupt terminal (AVB_PHY_INT) is asserted.
2	LCHNG	0	R/W	Link signal change bit This bit indicates a transition of the link status signal (AVB_LINK) input from the PHY-LSI from high to low or low to high. However, signal changes may also be detected at times when the link status signal (AVB_LINK) function is selected. To check the current link state, refer to the link status pin state bit in the PHY status register (PSR.LMON). 0: The change of Link status signal (AVB_LINK) is not detected. 1: The change of Link status signal (AVB_LINK) is detected.
1	MPD	0	R/W	Magic Packet™ Detection This bit indicates that a Magic Packet™ has been detected on the line. Writing 1 to this bit clears it to 0. 0: A Magic Packet™ has not been detected. 1: A Magic Packet™ has been detected.

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Bit	Bit Name	Initial Value	R/W	Description
0	ICD	0	R/W	<p>Illegal Carrier Detection</p> <p>This bit indicates that the PHY-LSI has detected an illegal carrier on the line. If a change in the signal input from the PHY-LSI occurs in a period shorter than the software recognition period, the correct information may not be obtained. Refer to the timing specification for the PHY-LSI used.</p> <p>Writing 1 to this bit clears it to 0.</p> <p>0: PHY-LSI has not detected an illegal carrier on the line.</p> <p>1: PHY-LSI has detected an illegal carrier on the line.</p>

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### 37A.2.51 E-MAC Interrupt Permission Register (ECSIPR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

The ECSIPR register enables or disables the states indicated by the ECSR register as interrupt sources. Each effective bit disables or enables interrupts corresponding to the bits in ECSR.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	MPDIP	ICDIP
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 2	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
1	MPDIP	0	R/W	Magic Packet™ Detect Interrupt Enable Setting this bit to 1 selects interrupt generation on setting of the Magic Packet™ detection bit (ECSR.MPD) in the E-MAC status register to 1. 0: Interrupts on setting of the MPD bit is disabled. 1: Interrupts on setting of the MPD bit is enabled.
0	ICDIP	0	R/W	Illegal Carrier Detect Interrupt Enable Setting this bit to 1 selects interrupt generation on setting of the illegal carrier detection bit (ECSR.ICD) in the E-MAC status register to 1. 0: Interrupts on setting of the ICD bit is disabled. 1: Interrupt on setting of the ICD bit is enabled.



### 37A.2.52 PHY Interface Register (PIR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

The PIR register provides a means of access to the PHY-LSI internal registers via the MII.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	MDI	MDO	MMD	MDC
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	—	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 4	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
3	MDI	—	R/W	MII Management Data-In This bit indicates the level of the AVB_MDIO pin.
2	MDO	0	R/W	MII Management Data-Out This bit holds data for output from the AVB_MDIO pin. The AVB_MDIO pin outputs data when the MMD bit is set to 1 (to specify writing as the direction). Data are not output while the MMD bit is set to 0 (to specify reading as the direction).
1	MMD	0	R/W	MII Management Mode This bit specifies the direction for data through MDIO (reading or writing). 0: Read direction is specified. 1: Write direction is specified.
0	MDC	0	R/W	MII Management Data Clock Values set in this bit are output on the AVB_MDC pin to supply the MII with the management data clock. For the method of access to the MII registers, see section 37A.3.13, Connection to PHY-LSI.

**37A.2.53 PHY Status Register (PSR)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

The PSR register is a read-only register that can read interface signals from the PHY-LSI.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	LMON
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are read as 0.
0	LMON	0	R	Link Status Pin State The Link state can be read by connecting the Link signal output from the PHY-LSI to the link status pin (AVB_LNK) pin. For the active sense, refer to the specifications of the PHY-LSI to be connected. 0: The link status signal (AVB_LNK) is at the low level. 1: The link status signal (AVB_LNK) is at the high level.

**37A.2.54 PHY\_INT Polarity Register (PIPR)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

The PIPR register is used to set the active sense of the AVB\_PHY-INT pin.

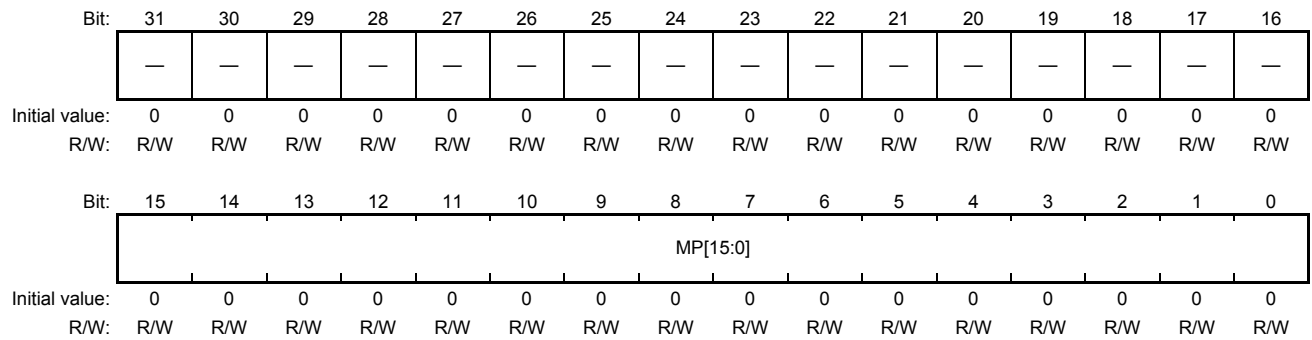
Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PHYIP
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
0	PHYIP	0	R/W	PHY Interrupt Input Pin Polarity This bit sets the active sense of the PHY interrupt pin (AVB_PHY-INT). For the active sense, refer to the specifications of the PHY-LSI to be connected. 0: PHY interrupt pin (AVB_PHY-INT) is active low (the low level triggers the interrupt state) 1: PHY interrupt pin (AVB_PHY-INT) is active high (the high level triggers the interrupt state)

**37A.2.55 Manual PAUSE Frame Register (MPR)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

The MPR register is used to set the value for the TIME parameter of manually generated PAUSE frames. When a PAUSE frame is manually transmitted, the value set in this register is used as its TIME parameter.

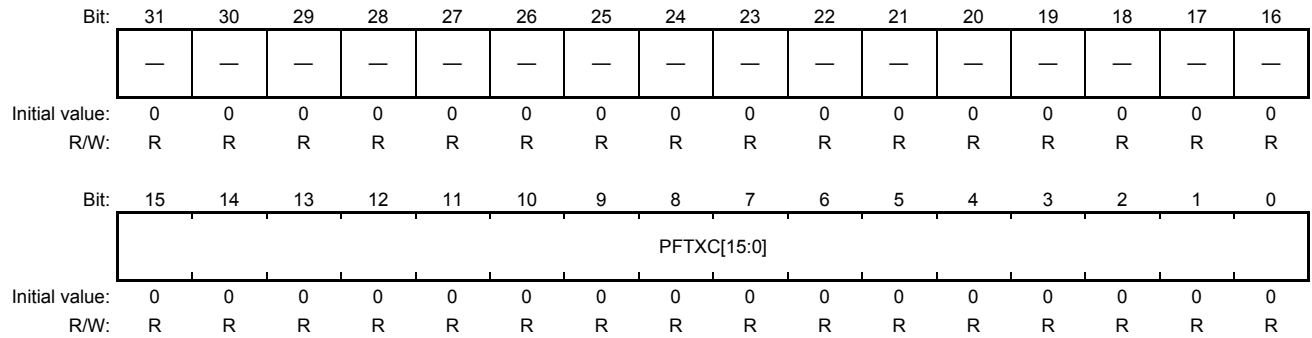


Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
15 to 0	MP[15:0]	H'0000	R/W	Manual PAUSE These bits set the value of the TIME parameter in manually generated PAUSE frames. The unit for the setting is 512 bit time. These bits set the TIME parameter value of a manual PAUSE frame. H'0000: — H'0001: 1 × 512 bit time H'0002: 2 × 512 bit time : : H'FFFF: 65535 × 512 bit time A bit time changes relative to the transfer speed as follows. 1000 Mbps: 1 bit time = 1 ns 100 Mbps: 1 bit time = 10 ns

**37A.2.56 PAUSE Frame Transmit Counter (PFTCR)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

The PFTCR register is a counter that indicates the number of times PAUSE frames have been transmitted.

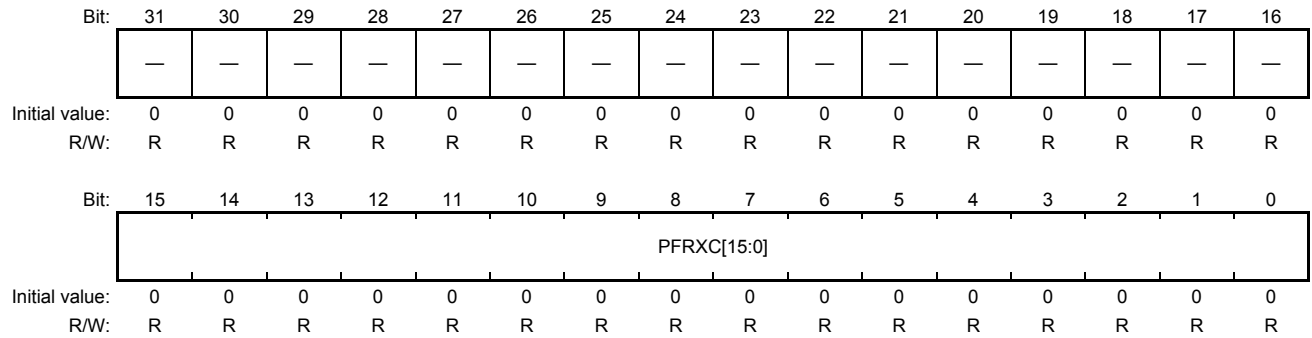


Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are read as 0. The write value should be 0.
15 to 0	PFTXC[15:0]	H'0000	R	PAUSE Frame Transmit Counter Counter for counting the number of transmitted PAUSE frames The bits are cleared to 0 when they are read. If counting up and clearing of the counter coincide, clearing the counter takes priority.

**37A.2.57 PAUSE Frame Receive Counter (PFRCR)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

The RFRCCR register is a counter that indicates the number of times PAUSE frames have been received.



Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are read as 0. The write value should be 0.
15 to 0	PFRXC[15:0]	H'0000	R	PAUSE Frame Receive Counter These bits indicate the number of PAUSE frames that have been received when flow control in reception is enabled (the RXF bit in ECMR = 1). The bits are cleared to 0 when they are read. If counting up and clearing the counter coincide, clearing the counter takes priority.

**37A.2.58 E-MAC Mode Register 2 (GECMR)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

The GECMR register specifies the operating mode for the E-MAC.

The setting in the GECMR register must not be changed while transmission or reception is enabled.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SPEED
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

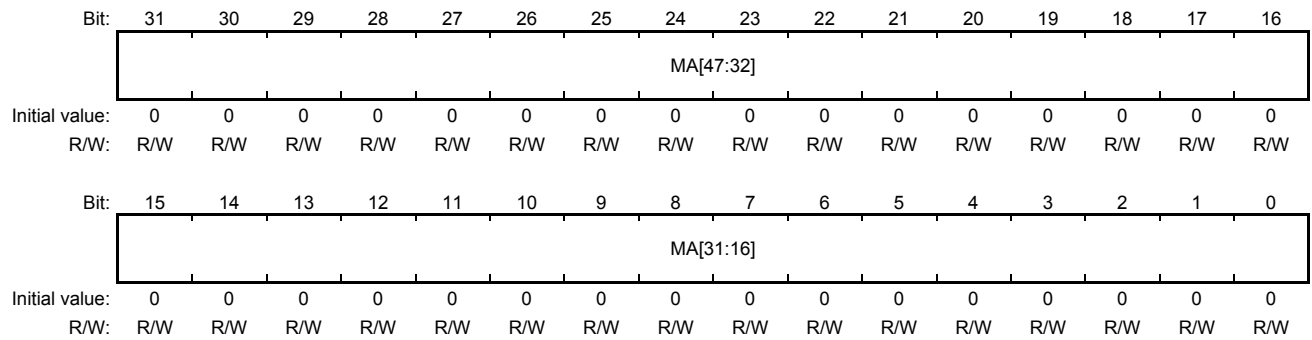
Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
0	SPEED	0	R/W	Transfer Speed Setting This bit sets the transfer rate. 0: Transfer is at 100 Mbps. 1: Transfer is at 1000 Mbps.

### 37A.2.59 E-MAC Address High Register (MAHR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

The MAHR register specifies the 32 higher-order bits of the 48-bit E-MAC address. The settings in this register are normally made in the initialization process after a reset.

The settings in this register must not be changed while transmission or reception is enabled.



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	MA[47:16]	H'0000 0000	R/W	E-MAC Address Bits 47 to 16 These bits are used to set the 32 higher-order bits of the E-MAC address. For example, if the E-MAC address is 01-23-45-67-89-AB (hexadecimal), set H'0123 4567 in the MAHR register.

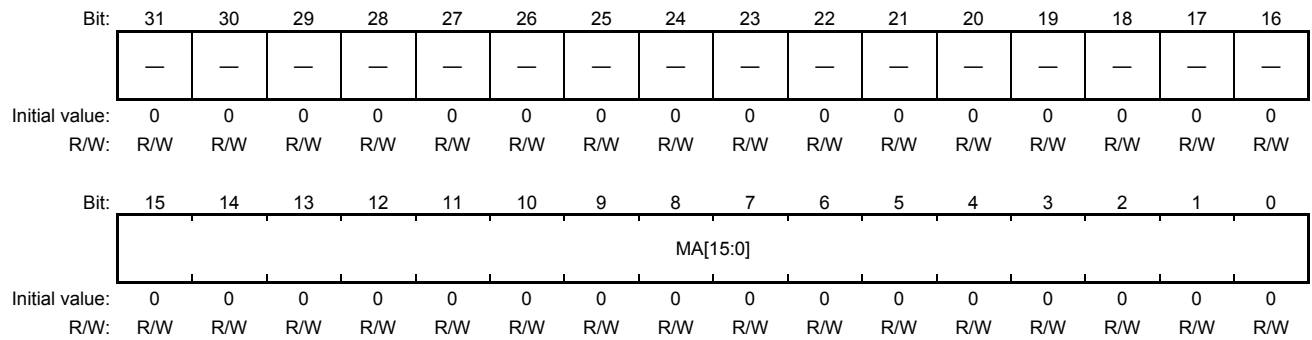


### 37A.2.60 E-MAC Address Low Register (MALR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

The MALR register specifies the 16 lower-order bits of the 48-bit E-MAC address. The settings in this register are normally made in the initialization process after a reset.

The settings in this register must not be changed while transmission or reception is enabled.

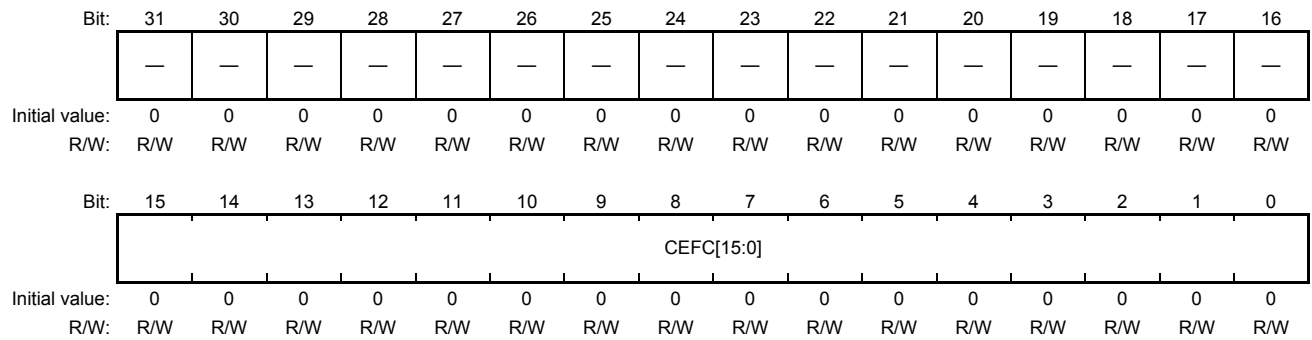


Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
15 to 0	MA[15:0]	H'0000	R/W	E-MAC Address Bits 15 to 0 These bits are used to set the 16 lower-order bits of the E-MAC address. For example, if the E-MAC address is 01-23-45-67-89-AB (hexadecimal), set H'89AB in the MALR register.

**37A.2.61 CRC Error Frame Receive Counter Register (CEFCR)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

The CEFCR register is a counter that indicates the number of times frames with CRC errors were received. Counting up stops when the value in this register reaches H'0000 FFFF.

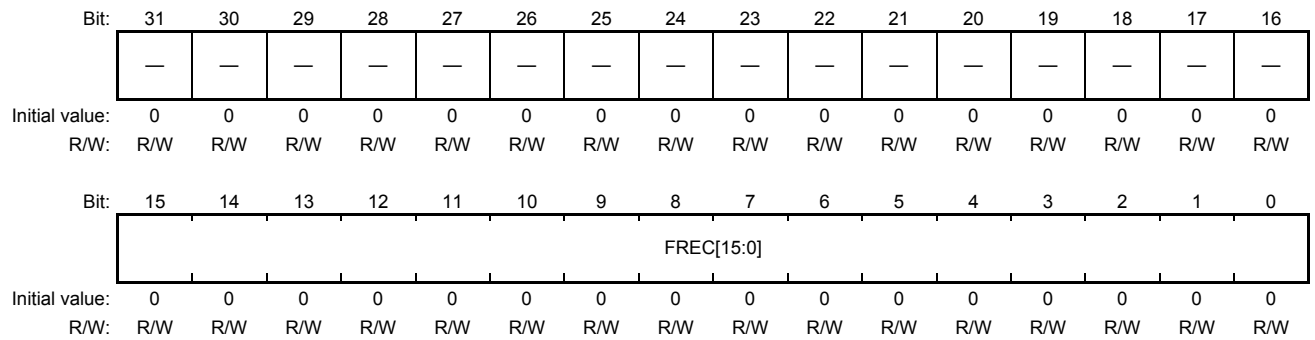


Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
15 to 0	CEFC[15:0]	H'0000	R/W	CRC Error Frame Counter These bits indicate the number of received frames having CRC errors. The bits are cleared to 0 when they are read while the counter clear mode bit (TRCCM) in the E-MAC mode register is set to 1. When TRCCM = 0, they are cleared to 0 by the writing of any value to this register.

**37A.2.62 Frame Receive Error Counter Register (FRECR)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

The FRECR register is a counter that indicates the number of frames for which receive errors were generated by input on the AVB\_RX\_ER pin from the PHY-LSI. Counting up stops when the value in this register reaches H'0000 FFFF.

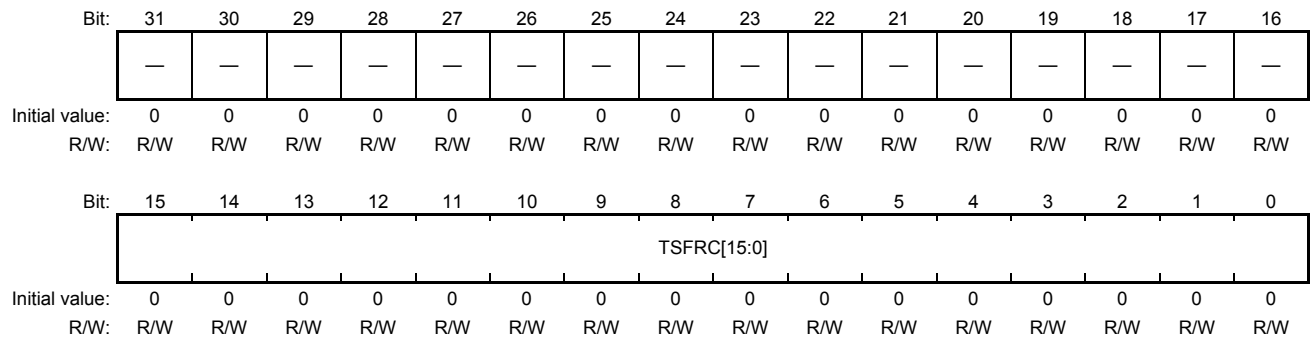


Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
15 to 0	FREC[15:0]	H'0000	R/W	Frame Receive Error Counter These bits indicate the number of errors during frame reception. The bits are cleared to 0 when they are read while the counter clear mode bit (TRCCM) in the E-MAC mode register is set to 1. When TRCCM = 0, they are cleared to 0 by the writing of any value to this register.

**37A.2.63 Too-Short Frame Receive Counter Register (TSFRCR)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

The TSFRCR register is a counter that indicates the number of received frames that were fewer than 64 bytes in length. Counting stops when the value in this register reaches H'0000 FFFF.

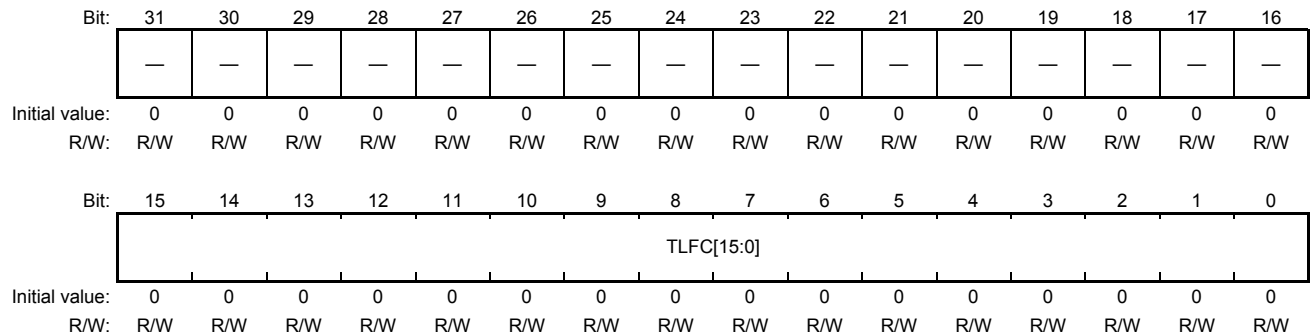


Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
15 to 0	TSFRC[15:0]	H'0000	R/W	Too-Short Frame Receive Counter These bits indicate the number of received frames that were fewer than 64 bytes in length. The bits are cleared to 0 when they are read while the counter clear mode bit (TRCCM) in the E-MAC mode register is set to 1. When TRCCM = 0, they are cleared to 0 by the writing of any value to this register.

**37A.2.64 Too-Long Frame Receive Counter Register (TLFRCR)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

The TLFRCR register is a counter that indicates the number of received frames that were longer than the value specified in the receive frame length register (RFLR). Counting up stops when the value in the TLFRCR register reaches H'0000 FFFF.

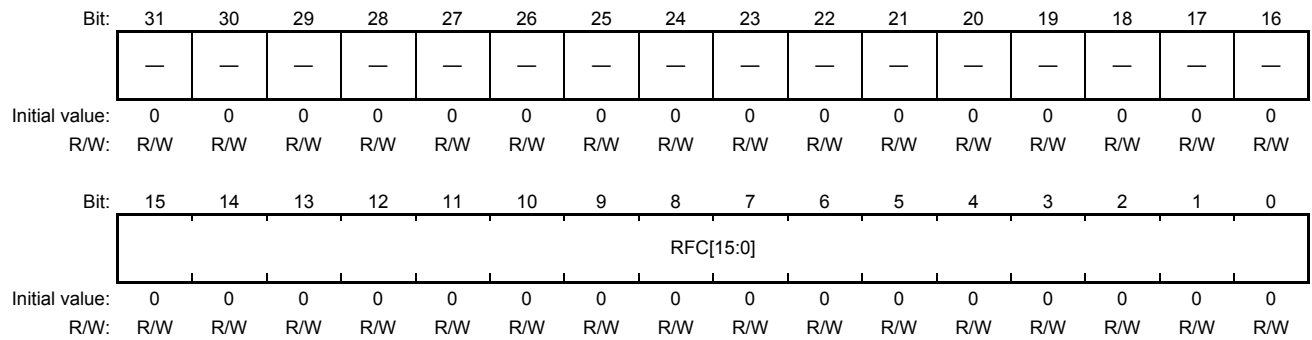


Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
15 to 0	TLFC[15:0]	H'0000	R/W	Too-Long Frame Receive Counter These bits indicate the number of received frames that were longer than the value in RFLR. The bits are cleared to 0 when they are read while the counter clear mode bit (TRCCM) in the E-MAC mode register is set to 1. When TRCCM = 0, they are cleared to 0 by the writing of any value to this register.

**37A.2.65 Residual-Bit Frame Receive Counter Register (RFCR)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

The RFCR register is a counter that indicates the number of received frames containing “residual bits” (trailing bits not making up an 8-bit unit). Counting up stops when the value in this register reaches H'0000 FFFF.

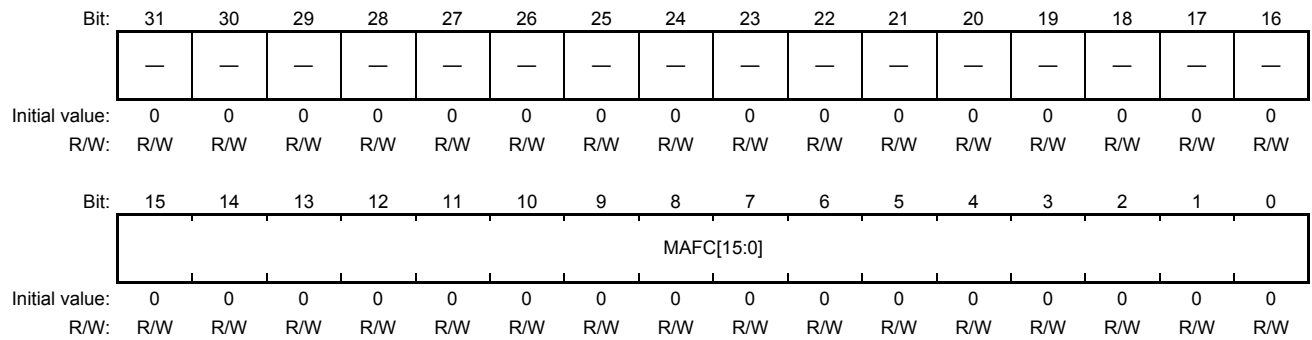


Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
15 to 0	RFC[15:0]	H'0000	R/W	Residual-Bit Frame Receive Counter These bits indicate the number of received frames containing residual bits. The bits are cleared to 0 when they are read while the counter clear mode bit (TRCCM) in the E-MAC mode register is set to 1. When TRCCM = 0, they are cleared to 0 by the writing of any value to this register.

**37A.2.66 Multicast Address Frame Receive Counter Register (MAFCR)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

The MAFCR register is a counter that indicates the number of received frames for which a multicast address was specified. Counting up stops when the value in this register reaches H'0000 FFFF.



Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
15 to 0	MAFC[15:0]	H'0000	R/W	Multicast Address Frame Counter These bits indicate the number of multicast frames that have been received. The bits are cleared to 0 when they are read while the counter clear mode bit (TRCCM) in the E-MAC mode register is set to 1. When TRCCM = 0, they are cleared to 0 by the writing of any value to this register.

### 37A.3 Operation

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

The EthernetAVB consists of the following functional units:

- DMA transfer controller (AVB-DMAC): Handles DMA transfer between the data storage areas for reception and transmission in the URAM and the reception and transmission FIFO buffers
- MAC controller (E-MAC): Handles transfer between the reception and transmission FIFO buffers and the GMII or MII

Using its direct memory access (DMA) function, the AVB-DMAC handles DMA transfer of frame data between the destinations for storing Ethernet frame data for transmission and reception in the URAM and the FIFO buffers for reception and transmission. Data cannot be directly read from or written to the FIFO buffers.

To handle DMA transfer, the AVB-DMAC requires information that includes the addresses for storage of data for transmission and received data. These data are referred to as descriptors. The AVB-DMAC reads data for transmission from the storage area for data to be transmitted according to the information in descriptors and writes received data to the storage area for received data accompanied by information in descriptors. The descriptors are placed in the URAM. Arranging multiple descriptors in descriptor lists allows the continuous reception or transmission of multiple Ethernet frames.

The E-MAC supports a GMII and MII, which provides an interface format for the externally connected PHY-LSI. The E-MAC constructs Ethernet frames from data written to the transmission FIFO and transmits these frames to the GMII or MII. It also performs CRC checking of Ethernet frames received from the GMII or MII and writes the frames to the reception FIFO.



### 37A.3.1 AVB-DMAC Operating Modes

Figure 37A.2 illustrates the operating modes of the AVB-DMAC.

Transitions of AVB-DMAC operating mode are under the control of the items listed below.

- CPU operating mode (hardware reset and power-down mode)
- Configuration of the operating mode configuration bits (CCC.OPC) in the AVB-DMAC mode register

The current operating mode can be confirmed by reading the operating mode status bits in the AVB-DMAC status register (CSR.OPS).

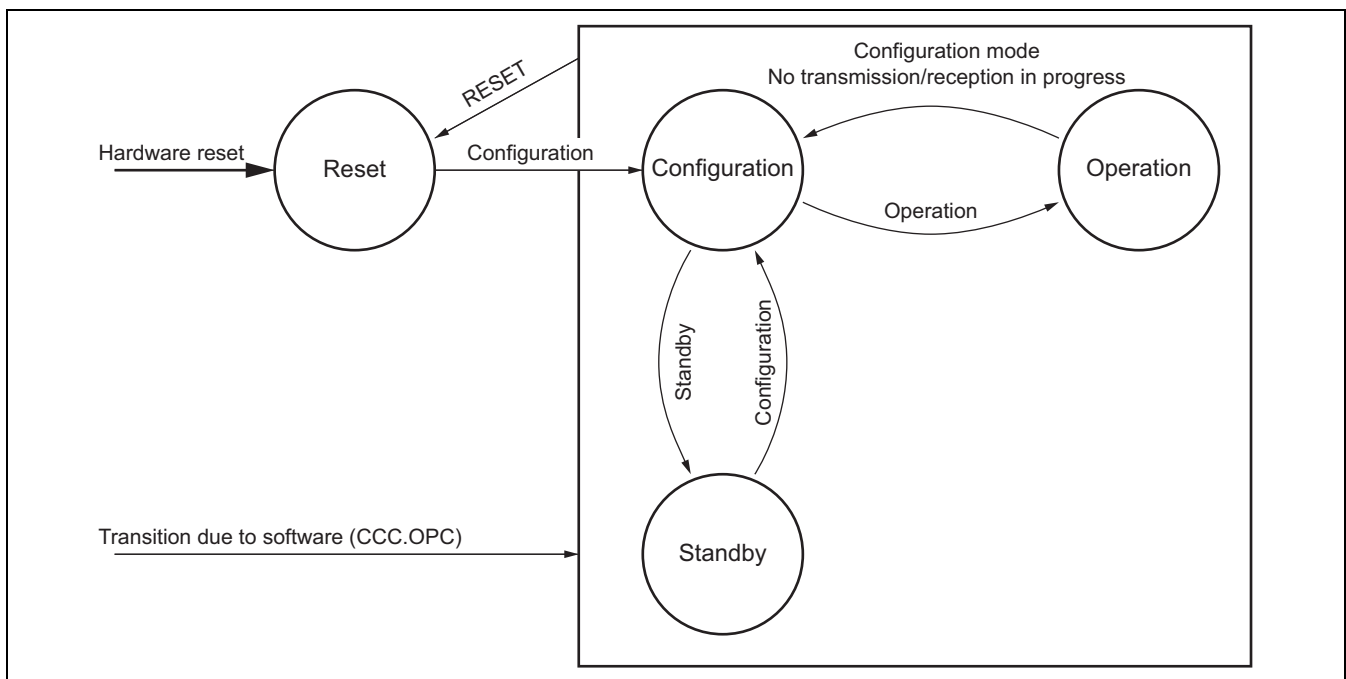


Figure 37A.2 Operating Mode of AVB-DMAC

#### 37A.3.1.1 Operating Modes

##### (1) Reset mode

After a hardware reset, the AVB-DMAC enters reset mode.

In reset mode, only the AVB-DMAC operating mode control function is controllable and other functions are all stopped. This mode is designed for reduced power when the Ethernet function is not necessary.

##### (2) Configuration mode

In configuration mode, various settings for the AVB-DMAC can be made.

The operation of most functions is stopped and all status registers are initialized to their reset values. The E-MAC functions in this mode.

##### (3) Operation mode

In operation mode, all functions of the AVB-DMAC can operate. Ethernet communications can only proceed in this mode.

##### (4) Standby mode

In standby mode, the E-MAC can only be used to control the operating mode. Other functions cannot be used.

### 37A.3.1.2 How to Set the Operating Mode

Set the operating mode configuration bits in the AVB-DMAC mode register (CCC.OPC) to select the operating mode. Furthermore, the current operating mode can be checked by reading the operating mode status bits in the AVB-DMAC status register (CSR.OPS).

Transitions other than from operation mode to configuration mode are made after the value is written to the operating mode configuration bits (CCC.OPC) (Figure 37A.3).

For transitions from operation mode to configuration mode, follow the procedure in Figure 37A.4 because any transmission and reception in progress will be executed before the transition to configuration mode.

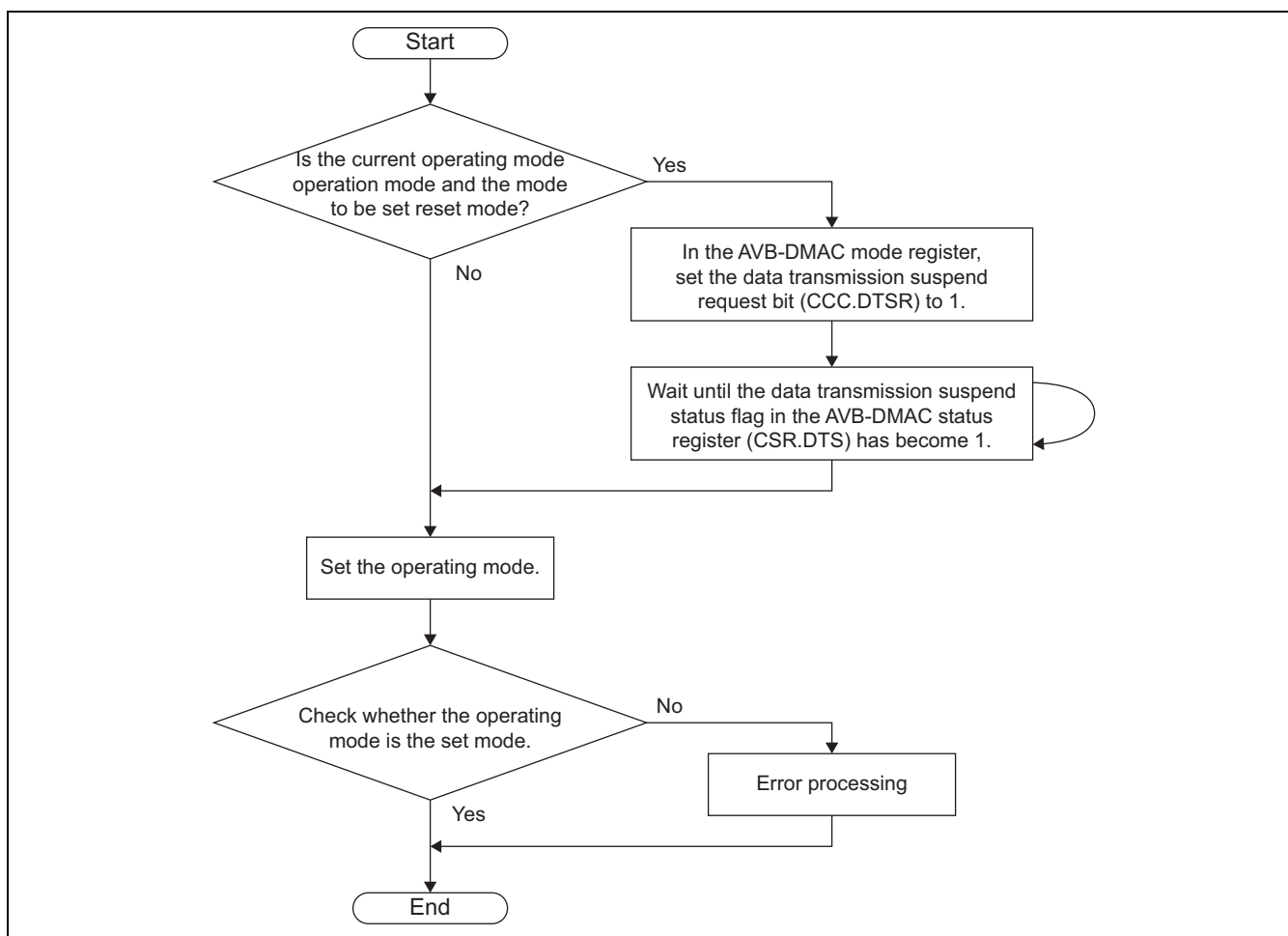
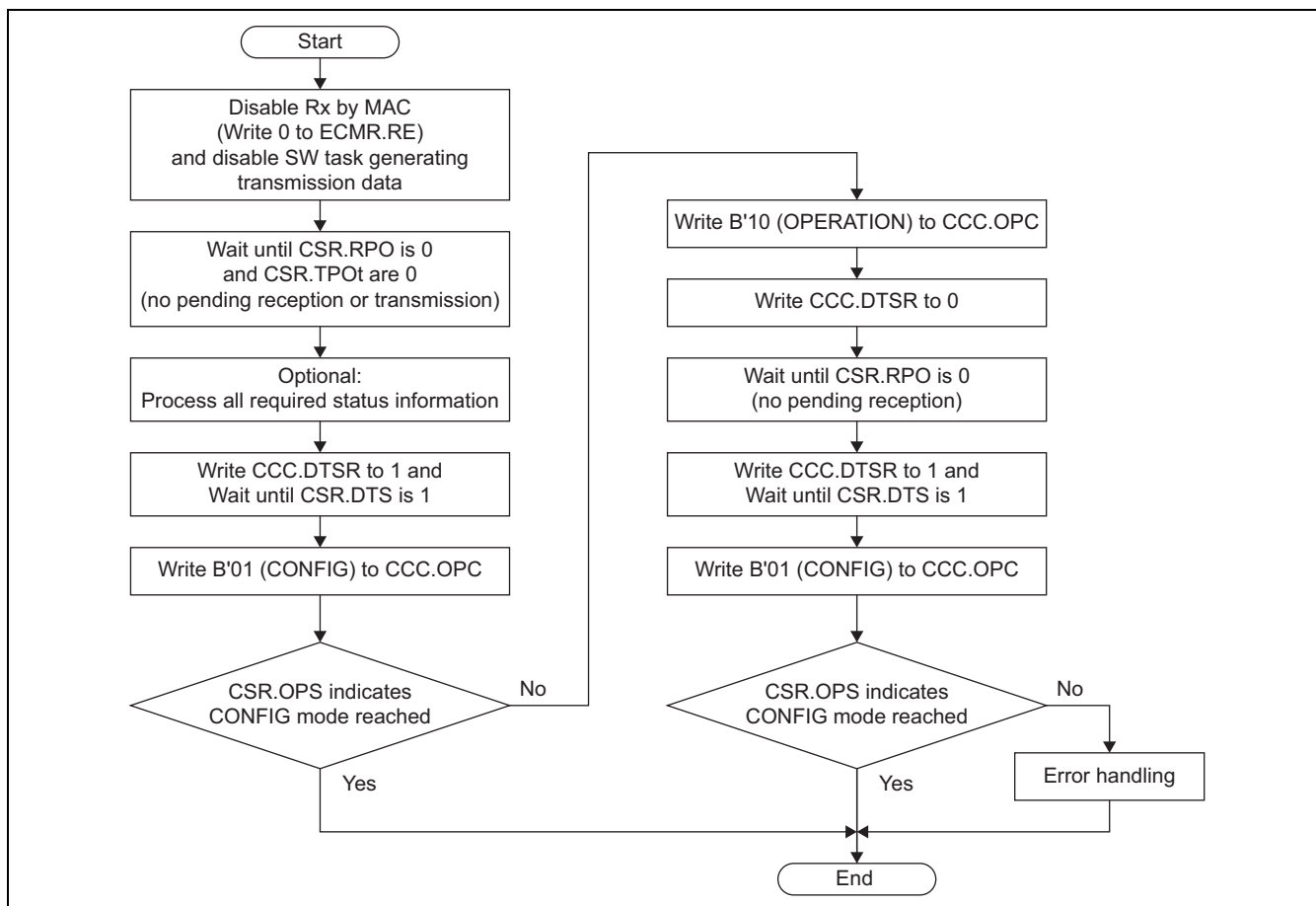


Figure 37A.3 Flow for Transitions of Operating Mode (Other than from Operation Mode to Configuration Mode)



**Figure 37A.4 Flow for Transitions of Operating Mode (from Operation Mode to Configuration Mode)**

In the transition from operation mode to configuration mode, the AVB-DMAC executes the following operations before the transition is completed. Read the operating mode status bits in the AVB-DMAC status register (CSR.OPS) to check that the transition to configuration mode has been completed.

- If the transfer of a frame between the reception FIFO and URAM is in progress, this is completed (other received frames remaining in the FIFO and any frames that are subsequently received by the E-MAC are discarded).
- If the transfer of a frame is in progress between the transmission FIFO and URAM, this is completed (frames for transmission remaining in the URAM will not be transmitted).
- All frames for transmission in the transmission FIFO are transferred to the E-MAC.

Notes: When the operating mode shifts to configuration mode, all status registers are cleared.

We recommend following the procedure below in the case of this transition.

1. Disable reception.
2. Since reception actually stopping after being disabled requires time, wait for an interval equivalent to that for reception of a maximum length packet.
3. Stop the software task that is generating data for transmission.
4. Wait until the receive process status bit (CSR.RPO) and the transmit process status bits (CSR.TPO0 to 3) in the AVB-DMAC status register are set to 0.
5. Capture all of the required status information.
6. Set the operating mode configuration bits in the AVB-DMAC mode register (CCC.OPC) to initiate the transition to configuration mode.

### 37A.3.1.3 Operating Mode Transitions Due to Hardware

The following hardware factors can also initiate transitions of the AVB-DMAC operating mode.

**(1) Hardware reset**

Resetting of the LSI chip leads to resetting of the entire EthernetAVB module. The operating mode shifts to reset mode.

**(2) Transition during power-off by module standby**

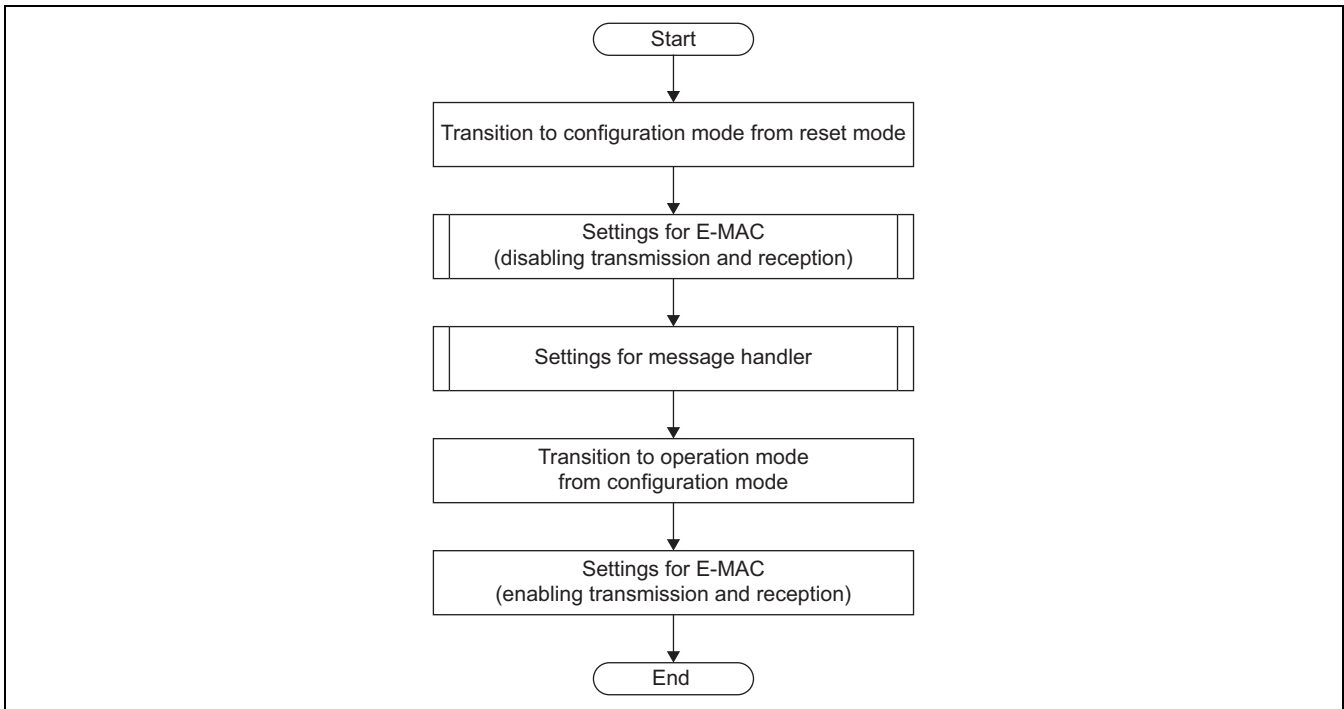
This transition is triggered by module standby of CPG during the power-off sequence.

The AVB-DMAC completes the bus master access in progress, and then shifts to reset mode. At this time, the operating mode configuration bits in the AVB-DMAC mode register (CCC.OPC) are set to B'00.

### 37A.3.2 Common Control for Transmission and Reception

#### 37A.3.2.1 Initialization Procedure

Figure 37A.5 shows the overall initialization procedure in outline.



**Figure 37A.5 Outline of the Initialization Procedure**

#### (1) Initializing the Receiver Section

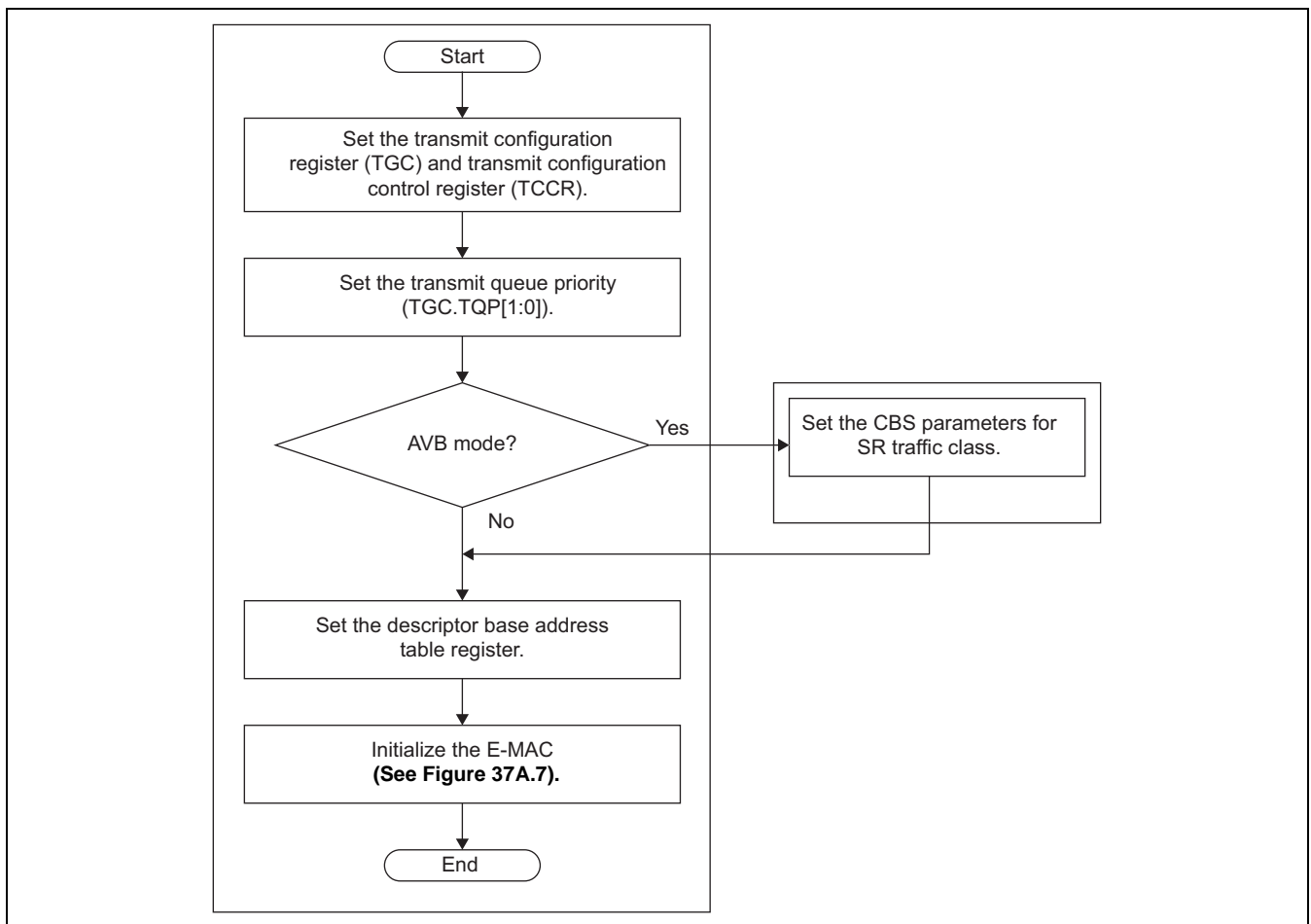
Before starting reception, follow the procedure below.

Keep the operating mode to configuration mode, and do not enable reception until the settings for the AVB-DMAC are completed.

- Set the operating mode to configuration mode.
- Set AVB filtering for network control frames and AVB stream frames to suit the specifications of the product the chip will be used in.
- Create a descriptor chain for each queue to be used.
- Set the base address for table address in the descriptor base address table register (DBAT).
- Specify the maximum frame length with the receive frame length upper limit register (RFLR).
- Specify whether padding is to be used with the receive padding configuration register (RPC).
- Set the unread frame counter for each queue with unread frame counter registers (UFCVs) 0 to 4.

## (2) Initializing the Transmitter Section

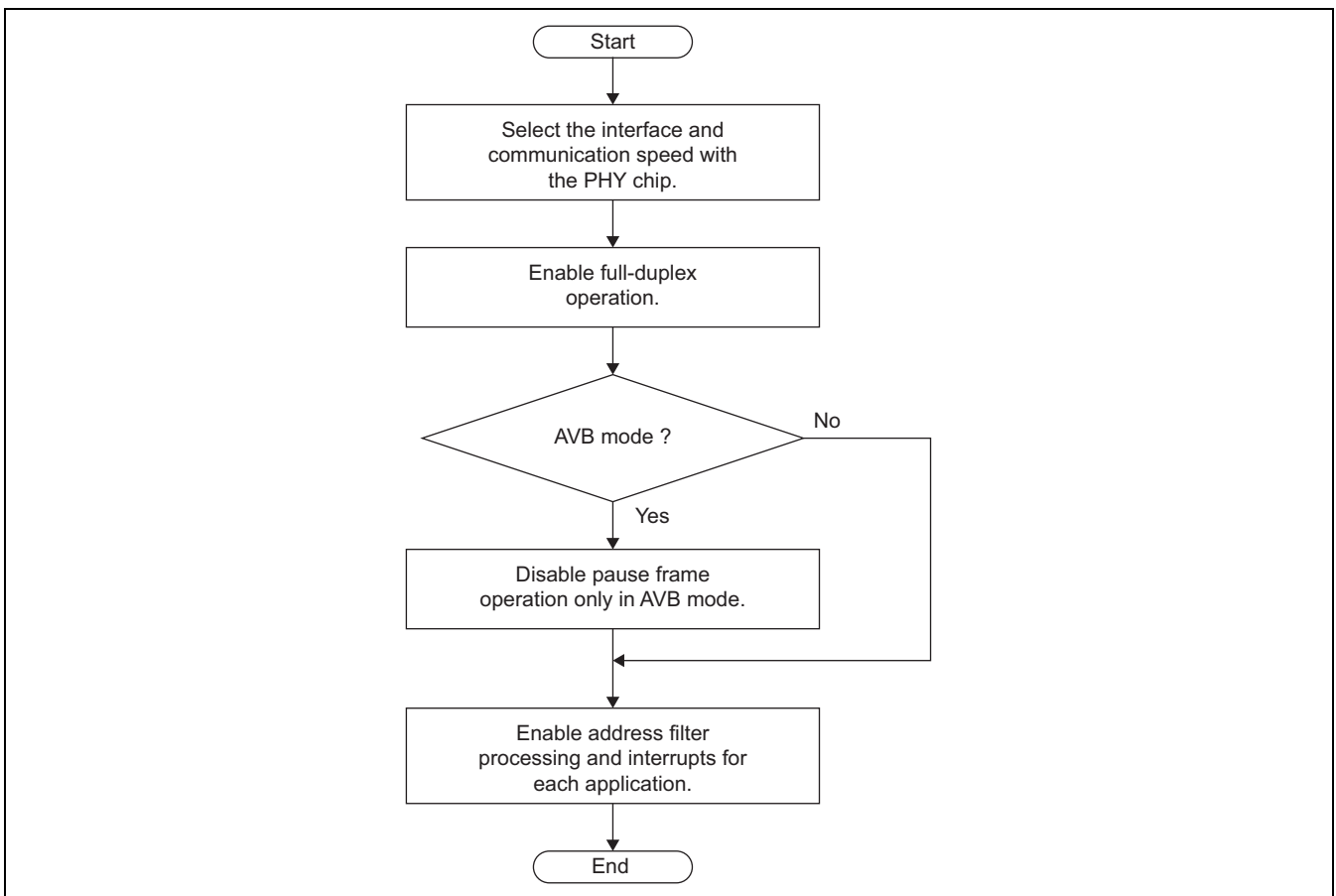
Figure 37A.6 illustrates initialization of the transmitter section.



**Figure 37A.6 Procedure for Initializing the Transmitter Section**

### (3) Initializing the E-MAC Section

Figure 37A.7 illustrates initialization of the E-MAC section.

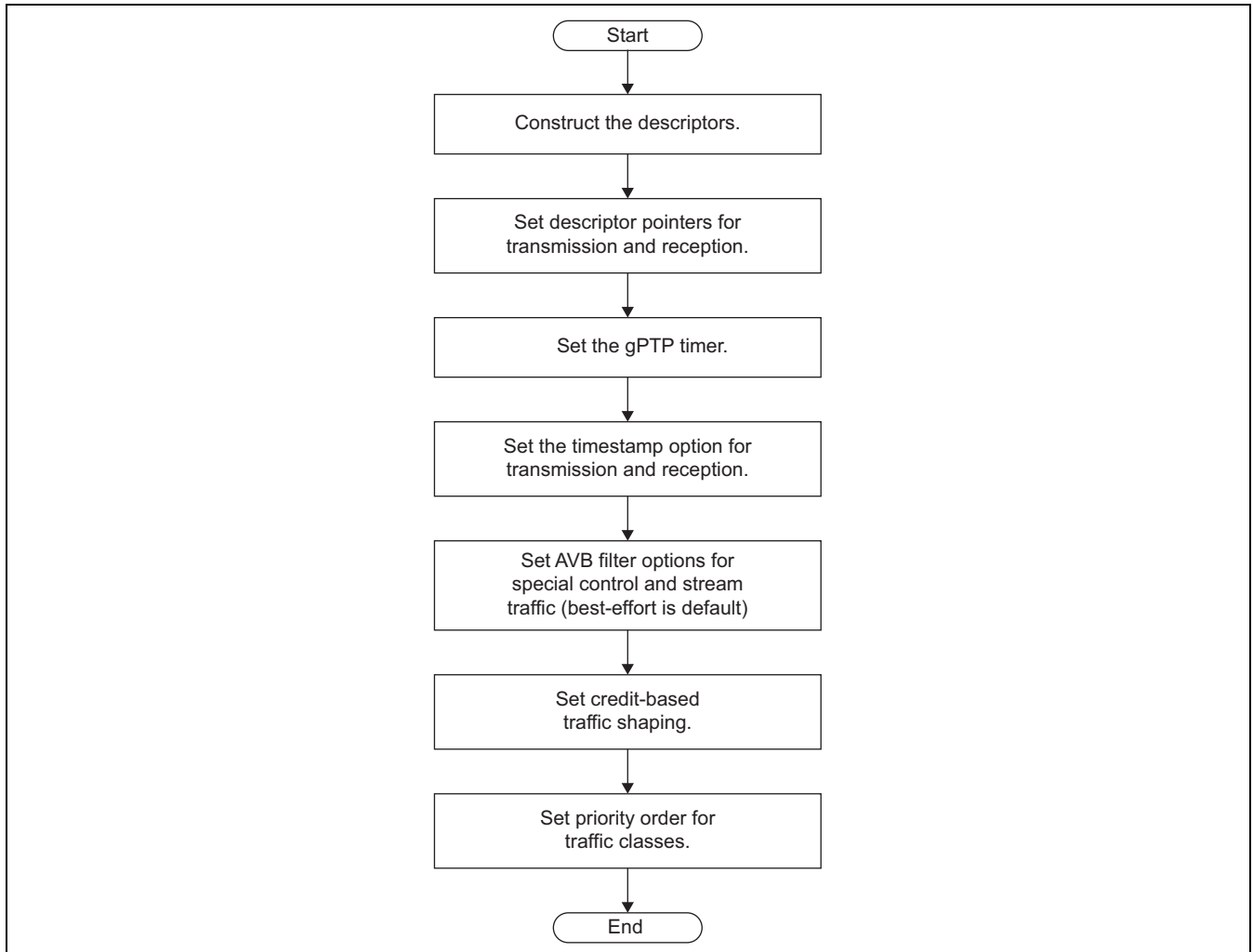


**Figure 37A.7 Procedure for Initializing the E-MAC Section**

#### (4) Initialization of the Application Unit

Figure 37A.8 illustrates initialization of the application unit.

For a description of how to set up the descriptors and the CBS traffic shaping parameters, see section 37A.3.3, Descriptors, and section 37A.3.6, CBS (Credit-Based Shaping).

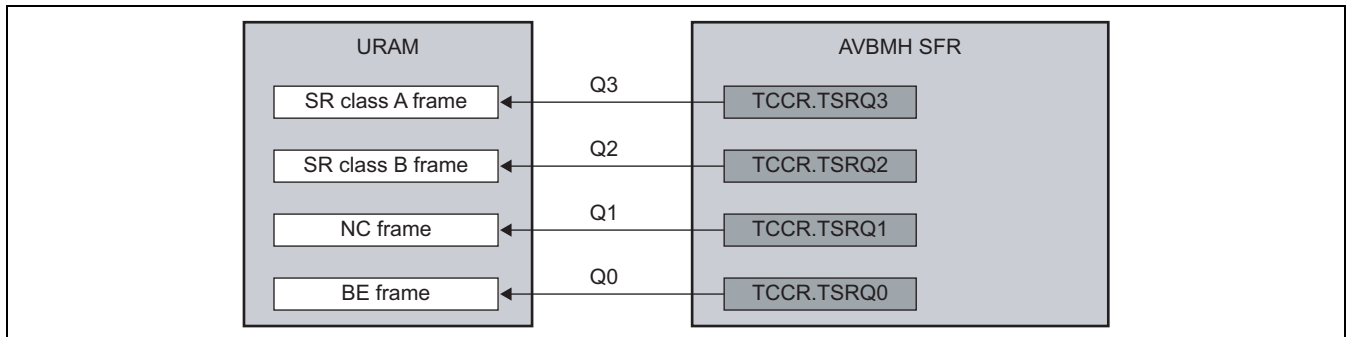


**Figure 37A.8 Initializing the Sections for Use by the Application**



### (5) Relationship between Transmission Queue Numbers and Traffic Classes

In fetching, the relationships between the transmission queues and traffic classes are fixed, so the priority specified by the transmit queue priority bits in the transmit configuration register (TGC.TQP) has no effect.



**Figure 37A.9 Class Associations of Queues for the Scheduler**

In fetching, the credit values for stream classes A and B are not taken into account. Behavior depends on the setting of the transfer FIFO size configuration bits in the transfer configuration registers (TGC.TBDt) and on the frame size that can be fetched to the transmission FIFO.

When the transmit queue priority bits in the transmit configuration register (TGC.TQP) are B'00 or B'01, the priority order is Q3 → Q2 → Q1 → Q0.

When the transmit queue priority bits in the transmit configuration register (TGC.TQP) are B'11, the priority order is Q1 → Q3 → Q2 → Q0.

### 37A.3.2.2 Checking Integrity

The AVB-DMAC is capable of detecting and identifying errors produced in the processing of Ethernet frames and in the transfer of frame data for transmission and reception.

#### (1) Concept of Integrity Checking in Reception

The aim of integrity checking in reception is preventing the storage of error frames in the URAM. If an error frame is stored in the URAM, software can get information to identify the frame as an error frame.

Note: If a special descriptor chain is to be used for separation of received headers from the associated data, an error that breaks the sequence may lead to storage space for synchronization running out. In such cases, software interaction or re-synchronization via the EOS descriptor is required.

#### (2) Concept of Integrity Checking in Transmission

The purpose of integrity checking in transmission is to prevent the transmission of broken frames.

Since transmission of a frame by the E-MAC can neither be stopped nor disabled once it has started, this check involves intensive monitoring for problems that can arise during fetching.

#### (3) Items for Monitoring in Both Reception and Transmission

##### (a) Errors in access to the URAM for reading of descriptors

The same descriptor may be processed again because the current descriptor address (CDARq.CDA) was not changed. If this problem occurs in a divided frame, the sequence may be broken.

##### In reception

- The received frame will be lost.
- The same problem will occur for the next frame of data received for the same queue.

##### In transmission

- The transmit start request bit in the transmit configuration control register (TCCR.TSRQt) is set to 0.
- The frame will be lost from the transmission FIFO.

Errors in access to read descriptors from the URAM are detected from the response signal of the AXI-Bus.

##### (b) Illegal configuration of a descriptor by an application

The same descriptor may be processed again because the current descriptor address (CDARq.CDA) was not changed. If this problem occurs in a divided frame, the sequence may be broken.

##### In reception

- The received frame will be lost.
- The same problem will occur for the next frame of data received for the same queue.

##### In transmission

- The transmit start request bit in the transmit configuration control register (TCCR.TSRQt) is set to 0.
- The frame will be lost from the transmission FIFO.

##### (c) Errors in access to the URAM for writing of descriptors

As in the case where no error occurs, the current descriptor address (CDARq.CDA) and the transmit start request bit in the transmit configuration control register (TCCR.TSRQt) are updated.

As DESCR.DT was not updated, hardware and software synchronization may have been destroyed.

Errors in access to write descriptors to the URAM are detected from the response signal of the AXI-Bus.

#### (4) Items for Monitoring in Reception

##### (a) Errors in access to the URAM for writing of data or time stamps

- As in the case where no error occurs, the current descriptor address (CDARq.CDA) is updated.
- DESC.R.EI is set to indicate incorrect contents.
- This problem occurring in a divided frame may break the descriptor sequence, making the queue unusable.

Errors in access to write data or descriptors to the URAM are detected from the response signal of the AXI-Bus.

##### (b) Error of the Reception FIFO

- Received frames are all invalidated.
- All frames stored as received frames are discarded. At this time, the number of frames and queue information cannot be captured.

If the reception FIFO RAM faults, AVB-DMAC detects the fault as error of the reception FIFO.

#### (5) Items for Monitoring in Transmission

##### (a) Errors in Access for Reading Data from the URAM

- Data that have already been fetched are discarded from the transmission FIFO.
- When an error of this type occurs during processing of an FSINGLE or FEND descriptor:  
As in the case where no error occurs, the current descriptor address (CDARq.CDA) and the transmit start bit in the transmit configuration control register (TCCR.TSRQt) are updated. Fetching resumes after the error frame.
- When an error of this type occurs during processing of an FSTART or FMID descriptor:  
The current descriptor address (CDARq.CDA) is not updated.  
The transmit start bit in the transmit configuration control register (TCCR.TSRQt) is set to 0.

Errors in access to read data from the URAM are detected from the response signal of the AXI-Bus.

##### (b) Overflow of the Transmission FIFO

- As in the case where no error occurs, the current descriptor address (CDARq.CDA) and the transmit start bit in the transmit configuration control register (TCCR.TSRQt) are updated. Fetching resumes after the error frame.
- The frame will be discarded from the FIFO.

##### (c) Frame size error during transmission

- As in the case where no error occurs, the current descriptor address (CDARq.CDA) and the transmit start bit in the transmit configuration control register (TCCR.TSRQt) are updated. Fetching resumes after the error frame.

A transmit frame size error is detected when the size setting in one or more (in the case of a divided frame) descriptors for frame transmission is 1966 or more bytes. Such frames are cut out and transmitted.

##### (d) Damaged Data in the Transmission FIFO

- Fetching is not affected by damaged data.
- Since damaged data from the FIFO is only detected during frame transmission, an error frame may be transmitted.

If damaged data in the transmission FIFO is an error due to the transmission FIFO, this is detected by the AVB-DMAC.

### 37A.3.3 Descriptors

#### 37A.3.3.1 Data Representation in URAM

The AVB-DMAC transfers data for transmission and received data to and from the application software via the URAM.

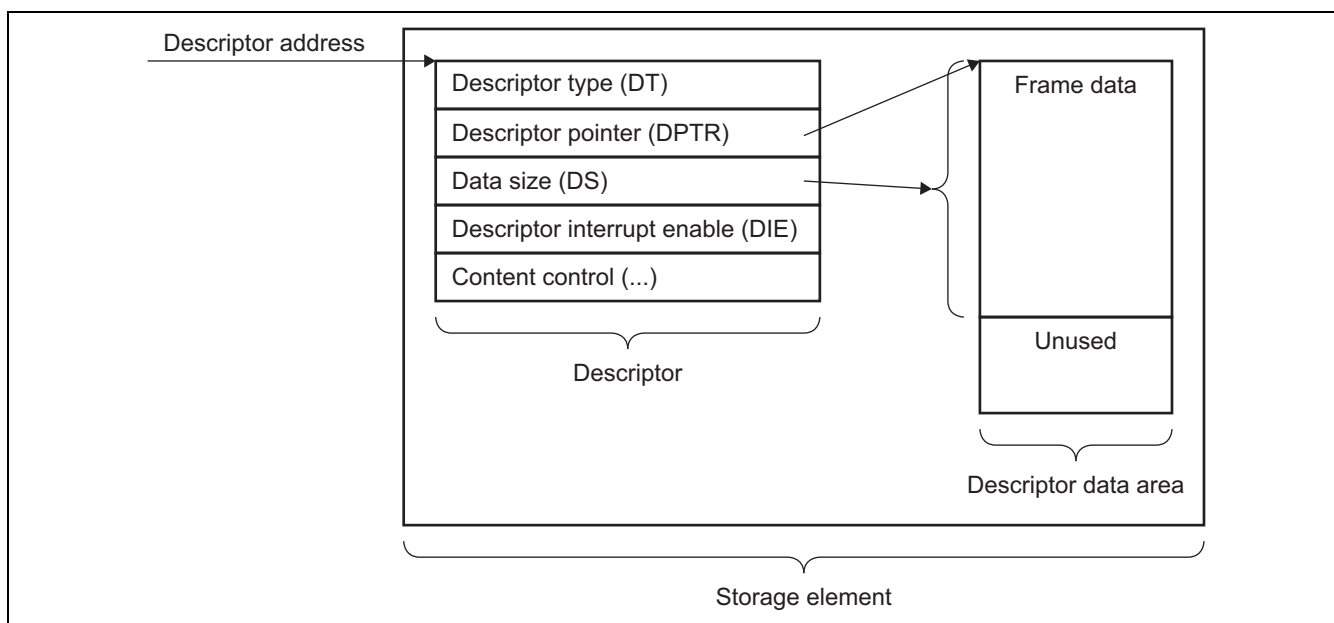
The memory in the URAM for use by the AVB-DMAC is configured with control structures referred to as descriptors and associated areas to which the frame data are allocated. Dividing the memory into a control area and data area allows the flexible allocation of frame data to the URAM. This enables sharing of the areas to which frame data are allocated and the use of non-contiguous areas. Frame data can be copied without using the CPU. Arbitration that ensures hardware and software access to the memory area is also available without access to registers of the AVB-DMAC.

Figure 37A.10 shows an example of the memory maps for descriptors and the descriptor data area in the URAM.

A descriptor consists of its type (DESCR.DT), which controls the descriptor functions, a descriptor pointer (DESCR.DPTR) indicating the start address for storage of the frame data in the descriptor area, and the data size field (DESCR.DS), indicating the amount of frame data. Post-processing interrupt generation can be set up for each descriptor. Enabling and disabling of the interrupt is controlled by the descriptor interrupt enable bits (DESCR.DIE).

The descriptor may also hold information related to content. This information does not affect general descriptor functions. It provides information other than the frame data proper, such as on the state of reception.

For details, see section 37A.3.4.2, Setting Up Reception Descriptors, and section 37A.3.5.2, Setting Up Transmission Descriptors.



**Figure 37A.10 Outline of Storage Element Used for Receive and Transmit Queues**

The descriptor must be aligned with a 32-bit boundary in the URAM.

Descriptors are generally configured of 64 bits, but are configured of 160 bits when reception and storage of gPTP time stamps is enabled.

The frame data must also be aligned with a 32-bit boundary in the URAM.

The amount of data in the frame is defined by the data size bits (DESCR.DS). In reception, these bits indicate the upper limit on the size of frames to be received. If the data size is not aligned with a 32-bit boundary, the bytes to the next 32-bit boundary in the data area will be an unused area.

### 37A.3.3.2 Using Descriptor Chains in Queues

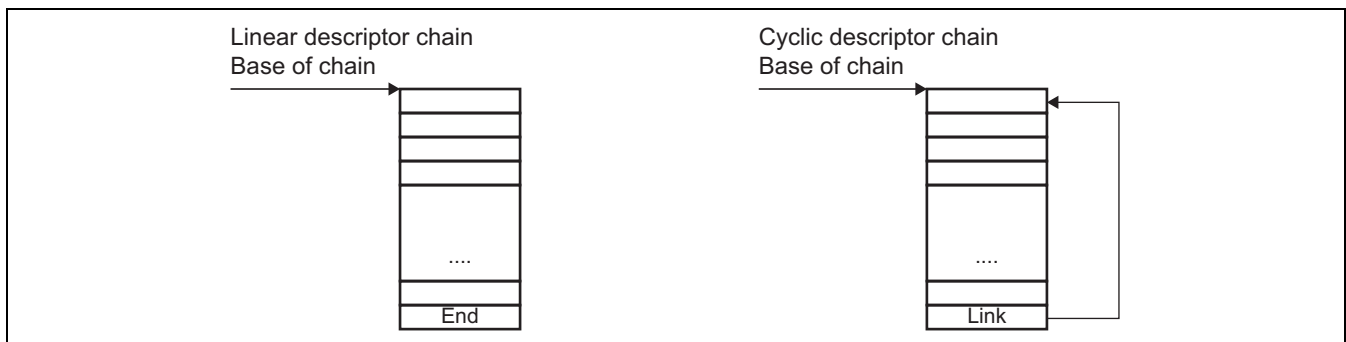
Transmission and reception descriptors in the URAM are grouped into queues. Each queue handles frames so that they are transmitted in order of priority and received separately. A queue is capable of controlling one or more frames. Accordingly, multiple descriptors can be assigned to one queue. A combination of multiple descriptors is referred to as a descriptor chain.

For a descriptor chain, the three general descriptor types listed below are defined. For details on these descriptor types, see section 37A.3.3.6, Descriptor Type.

- Descriptors that define frame data
- Descriptors that control the descriptor chain itself (e.g. LINK, EOS).
- Descriptors that arbitrate access by hardware or software

Figure 37A.11 shows the two basic topologies for descriptor chains. In the simplified examples in the figure, all descriptors allocated to the chain are stored in the array.

- For a linear descriptor chain, the last descriptor in the array is a control descriptor indicating the end of the descriptors (e.g. EEMPTY).
- For a cyclic descriptor chain, the last descriptor in the array is a control descriptor that returns to the first descriptor in the array (e.g. LINK).



**Figure 37A.11 Outline of the Basic Descriptor Chains**

The relationship between queues and descriptor chains is defined by the base addresses of chains. A queue is connected to one descriptor chain over one round of processing. There is also a method of switching to a different chain while in operation mode.

There are no restrictions on the number of link descriptors and their locations within the chain. The last descriptor of a designed chain determines the topology.

Which chain structure is to be used or which topology is suitable depends on the application. A description of how to design descriptor chains to suit various applications is given in section 37A.3.4 (2), Setting Up Reception Descriptors, and section 37A.3.5 (2), Setting Up Transmission Descriptors.

### 37A.3.3.3 Descriptor Base Address Table

The base address table in the URAM contains the address of the first descriptor of all chains to be handled by the respective queues.

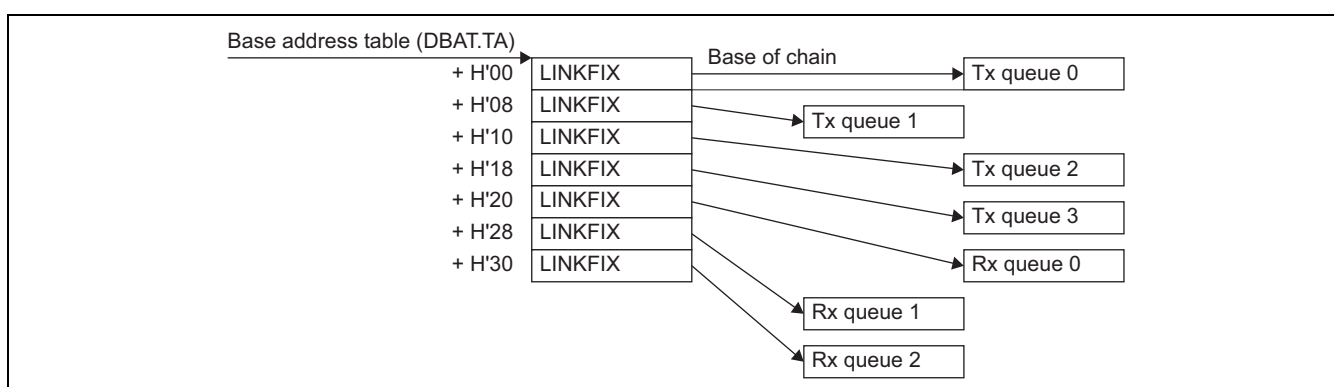
Entries 0 to 3 are used to access transmission queues 0 to 3. Subsequent entries are used to access reception queues. Entry 4 thus corresponds to reception queue 0.

The configuration of entries in the base address table is the same as the configuration of link descriptors. We recommend using the descriptor type (DESCR.DT) LINKFIX. Processing of this link descriptor does not change it, so it does not require updating. The first descriptor of a chain performs hardware and software synchronization. If the application requires hardware and software synchronization for the base addresses, use the descriptor type (DESCR.DT) LINK.

The CPU is only capable of using LINKFIX and LINK as descriptor types (DESCR.DT) of descriptors in the base address table.

Set the location of the base address table in the URAM in the descriptor base address table register (DBAT).

Figure 37A.12 shows an example of a base address table for controlling four transmission and three reception queues. The boxes to the right of the table represent descriptor chains with the desired topologies.



**Figure 37A.12 Example of a Base Address Table for Reception and Transmission Queues**

Note: The size of the descriptors in the base address table is always eight bytes even if the queue itself includes extended descriptors.

### 37A.3.3.4 Descriptor Chain Processing

The descriptor that is currently processed or will be processed when the related queue gets active is the current descriptor. The current descriptor address for use by a queue q can be checked in the current descriptor address register q (CDARq).

Current descriptors are stored in registers or in descriptors as described below in the given situations.

- In the descriptor base address table registers for all q queues (DBAT) (DBAT.TA+8\*q) when the operating mode shifts to operation mode.
- In the descriptor base address table register (DBAT) (DBAT.TA+8\*q) when a base address load request is issued for a queue q by setting the corresponding bit (DLR.LBAq) in the descriptor base address load request register (DLR).
- In DESC.RDPTR for a link descriptor (LINK, LINKFIX) to be processed.
- After a descriptor has been processed, the current descriptor for the same queue is incremented by the size of the descriptors being handled by the queue (8 bytes for normal descriptors and 20 bytes for extended descriptors). The AVB-DMAC updates the descriptor type and informs the CPU that the descriptor has been processed.

### 37A.3.3.5 Descriptor Interrupts

A descriptor is able to issue a descriptor interrupt on completion of its processing. The setting of the descriptor interrupt enable bits (DESCR.DIE) in each descriptor selects disabling or generation of the descriptor interrupt.

The descriptor interrupt is a common resource that is shared between reception and transmission queues. Software control of the descriptor interrupt provides a flexible method of application-specific flag processing.

Figure 37A.13 illustrates the way in which the AVB-DMAC generates descriptor interrupts (or sets bits in the descriptor interrupt status register (DIS.DPFi)). Processing of a descriptor with the value i in the descriptor interrupt enable bits (DESCR.DIE) leads to the corresponding bit in the descriptor interrupt status register (DIS.DPFi) being set.

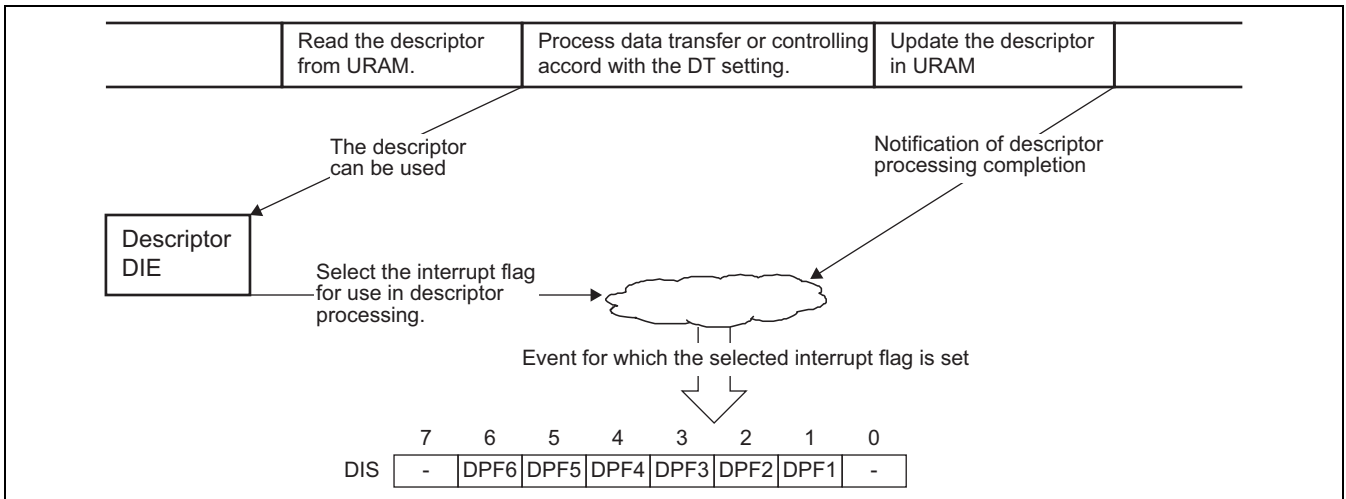


Figure 37A.13 Method of Descriptor Interrupt Generation

### 37A.3.3.6 Descriptor Type

The descriptor types (indicated by the DESCR.DT bits) supported by the AVB-DMAC fall into the following three categories.

- Definitions of frame data
- Control of descriptor chains
- Hardware and software arbitration

Table 37A.5 is a summary of the descriptor types available for the AVB-DMAC. Entries under “Name” are the names of the descriptor types and the values under “DT” are the corresponding values to be set in the descriptor type field (DESCR.DT). A given descriptor may be handled differently according to whether it is in a transmission or reception queue, so the transmission and reception columns list the scopes of control and processing of the descriptor types.

The abbreviations defined below are used in the transmission and reception columns.

#### Definition of SW:

- The descriptor is processed by software.
- Software has access to and may modify the descriptor and descriptor data area.
- This descriptor cannot be changed by hardware (AVB-DMAC).

#### Definition of HW:

- The descriptor is processed by hardware (AVB-DMAC).
- Software must modify neither the descriptor nor the descriptor data area.
- Hardware (AVB-DMAC) processes this descriptor and subsequently changes the descriptor type.

#### Invalid:

This descriptor type is not used in transfer in the given direction (transmission or reception).

Do not write this value to the descriptor type (DESCR.DT) field for transfer in the given direction.

Hardware does not process these descriptor types in the cases listed as invalid. The current descriptor address (CDARq.CDA) will not be changed when processing of a queue for the given direction arrives at a descriptor with this type setting.



**Table 37A.5 Summary of Descriptor Types**

Name	DT	Description	Reception	Transmission
Frame data				
FSTART	5	Frame Start The descriptor points to valid data for a frame. The frame starts with the given data and continues with that indicated by the next descriptor.	SW	HW
FMID	4	Frame Middle The descriptor points to valid data for a frame. The frame started with a previous descriptor and continues to the data indicated by the next descriptor.	SW	HW
FEND	6	Frame End The descriptor points to valid data for a frame. The frame continues from the previous descriptor and ends with the data indicated by in this descriptor.	SW	HW
FSINGLE	7	Frame Single The descriptor points to valid data for a complete frame.	SW	HW
Chain control				
LINK	8	Link Defines the next descriptor in the chain.	HW	HW
LINKFIX	9	Fixed Link Same as LINK, but not changed by AVB-DMAC after processing.	SW	SW
EOS	10	End Of Set Control element to split a descriptor chain. The chain stops and waits for user interaction.	HW	HW
HW/SW arbitration				
FEMPTY	12	Frame Empty A descriptor related to frame data but not containing valid data for a frame	HW	SW
FEMPTY_IS	13	Frame Empty Incremental Start A descriptor related to frame data but not containing valid data for a frame. DESCR.DPTR sets the base address of an "incremental data area" in the URAM.	HW	Invalid
FEMPTY_IC	14	Frame Empty Incremental Continue A descriptor related to frame data but not containing valid data for a frame. Data is stored to the incremental data area in the URAM.	HW	Invalid
FEMPTY_ND	15	Frame Empty No Data storage A descriptor related to frame data but not containing valid data for a frame. The descriptor is processed in the same way as FEMPTY but data are not stored in the URAM.	HW	Invalid
LEEMPTY	2	Link Empty A link descriptor for processing by the AVB-DMAC	SW	SW
EEMPTY	3	EOS Empty An EOS descriptor for processing by the AVB-DMAC	SW	SW
DT0	0	Reserved	Invalid	Invalid
DT1	1	Reserved	Invalid	Invalid
DT11	11	Reserved	Invalid	Invalid

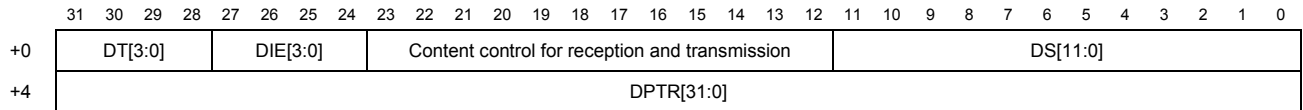
### 37A.3.3.7 Layout of General Descriptors in the URAM

The AVB-DMAC updates processed descriptors in the URAM. The field to be changed in the descriptor being updated depends upon whether the direction is transmission or reception and the queue mode. Other fields will not be changed. There are no restrictions on the values set in unused descriptor fields (indicated by “—” in the figure).

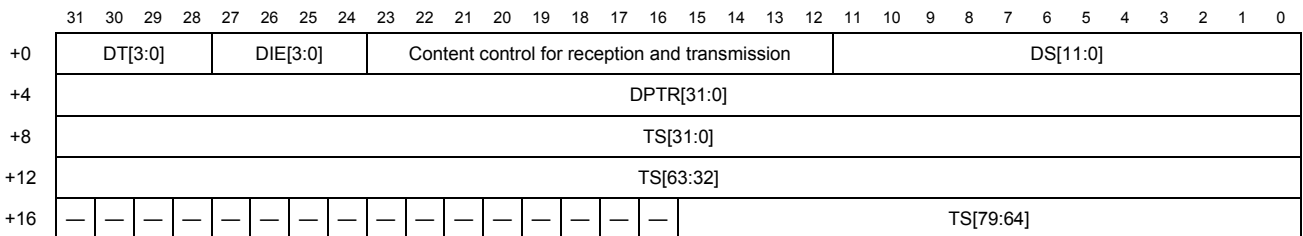
#### (1) Frame Data Descriptors

The allocation of bits in the frame data descriptors (FSTART, FMID, FEND, and FSINGLE) is shown below.

- Normal descriptor (usable in both reception and transmission)



- Extended descriptor (usable only in reception)



**Table 37A.6 Contents of Frame Data Descriptors (DESCR)**

Bit Name	Function
DT[3:0]	Descriptor Type 5: FSTART 4: FMID 6: FEND 7: FSINGLE For details, see section 37A.3.4.2, Setting Up Reception Descriptors, and section 37A.3.5.2, Setting Up Transmission Descriptors.
DIE[3:0]	Descriptor Interrupt Enable B'0000: Descriptor interrupt is disabled. B'0001 to B'1111: The corresponding descriptor interrupt is generated (DIS.DPFi).
—	Content Control For details, see section 37A.3.4.2, Setting Up Reception Descriptors, and section 37A.3.5.2, Setting Up Transmission Descriptors.
DS[11:0]	Data Size Size of the data area/frame data for the descriptor (in bytes)
DPTR[31:0]	Descriptor Pointer Pointer to the data area for the descriptor Register an address on a 32-bit boundary.
TS[79:0]	Time Stamp Time stamp of the received frame (only available in extended descriptors)

Note: Register an address aligned with a 32-bit boundary as the descriptor pointer (DESCR.DPTR).

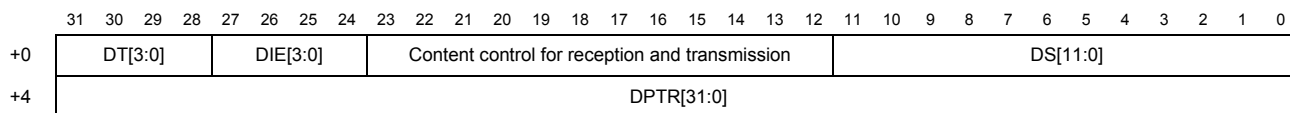
Some bits in extended descriptors are reserved (The reserved bits (above DESCR.TS[79:64]) in an extended descriptor are set to H'0000 after the time stamp is stored).

**(2) Hardware/Software Arbitration Descriptors (Only for Reception)**

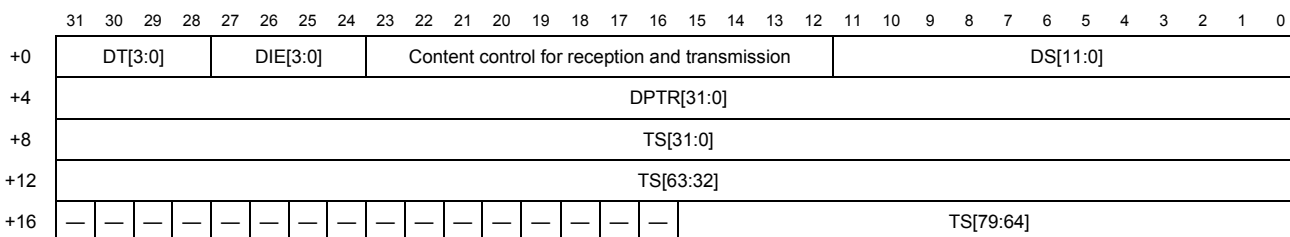
The allocation of bits in the descriptors for hardware/software arbitration (FEMPTY, FEMPTY\_IS, FEMPTY\_IC, and FEMPTY\_ND) is shown below.

The allocation of bits in the arbitration descriptors for use in reception is the same as in frame data descriptors.

- Normal descriptor



- Extended descriptor (usable only in reception)



**Table 37A.7 Contents of Hardware/Software Arbitration Descriptors (DESCR)**

Bit Name	Function
DT[3:0]	Descriptor Type 12: FEMPTY 13: FEMPTY_IS 14: FEMPTY_IC 15: FEMPTY_ND For details, see Table 37A.5, Summary of Descriptor Types.
DIE[3:0]	Descriptor Interrupt Enable B'0000: Descriptor interrupt is disabled. B'0001 to B'1111: The corresponding descriptor interrupt is generated (DIS.DPFi).
—	Content Control For details, see section 37A.3.4.2, Setting Up Reception Descriptors, and section 37A.3.5.2, Setting Up Transmission Descriptors.
DS[11:0]	Data Size Size of the data area/frame data for the descriptor (in bytes)
DPTR[31:0]	Descriptor Pointer Pointer to the data area for the descriptor Register an address on a 32-bit boundary.
TS[79:0]	Time Stamp Time stamp of the received frame (only available in extended descriptors)

Note: Register an address aligned with a 32-bit boundary as the descriptor pointer (DESCR.DPTR).  
When the descriptor is an extended descriptor, it has a 12-byte unused area.

In an FEMPTY descriptor, the descriptor type (DT), descriptor interrupt enable (DIE), data size (DS), and descriptor pointer (DPTR) fields are used.

In an FEMPTY\_IS descriptor, the descriptor type (DT), descriptor interrupt enable (DIE), and descriptor pointer (DPTR) fields are used.

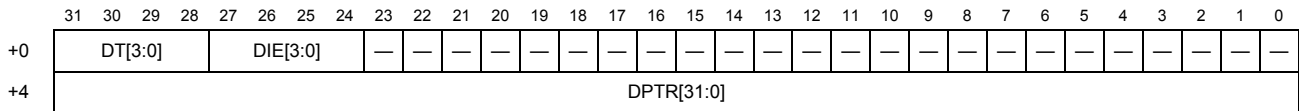
In an FEMPTY\_IC descriptor, the descriptor type (DT) and descriptor interrupt enable (DIE) are used.

In an FEMPTY\_ND descriptor, the descriptor type (DT), descriptor interrupt enable (DIE), and data size (DS) are used.

**(3) Link Descriptors**

The allocation of bits in the link descriptors (LINK and LINKFIX) is shown below.

- Normal descriptor



**Table 37A.8 Contents of Link Descriptors (DESCR)**

Bit Name	Function
DT[3:0]	Descriptor Type 8: LINK 9: LINKFIX For details, see Table 37A.5, Summary of Descriptor Types.
DIE[3:0]	Descriptor Interrupt Enable B'0000: Descriptor interrupt is disabled. B'0001 to B'1111: The corresponding descriptor interrupt is generated (DIS.DPFi).
DPTR[31:0]	Descriptor Pointer Pointer to the data area for the descriptor Register an address on a 32-bit boundary.

Note: Register an address aligned with a 32-bit boundary as the descriptor pointer (DESCR.DPTR).

**(4) Other Descriptors**

The allocation of bits in the other descriptors (EOS, FEMPTY (only for transmission), LEMPTY, and EEMPTY) is shown below.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
+0	DT[3:0]				DIE[3:0]				—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
+4	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

**Table 37A.9 Contents of Other Descriptors (DESCR)**

Bit Name	Function
DT[3:0]	Descriptor Type 10: EOS 12: FEMPTY (only for transmission) 2: LEMPTY 3: EEMPTY For details, see Table 37A.5, Summary of Descriptor Types.
DIE[3:0]	Descriptor Interrupt Enable B'0000: Descriptor interrupt is disabled. B'0001 to B'1111: The corresponding descriptor interrupt is generated (DIS.DPFi).

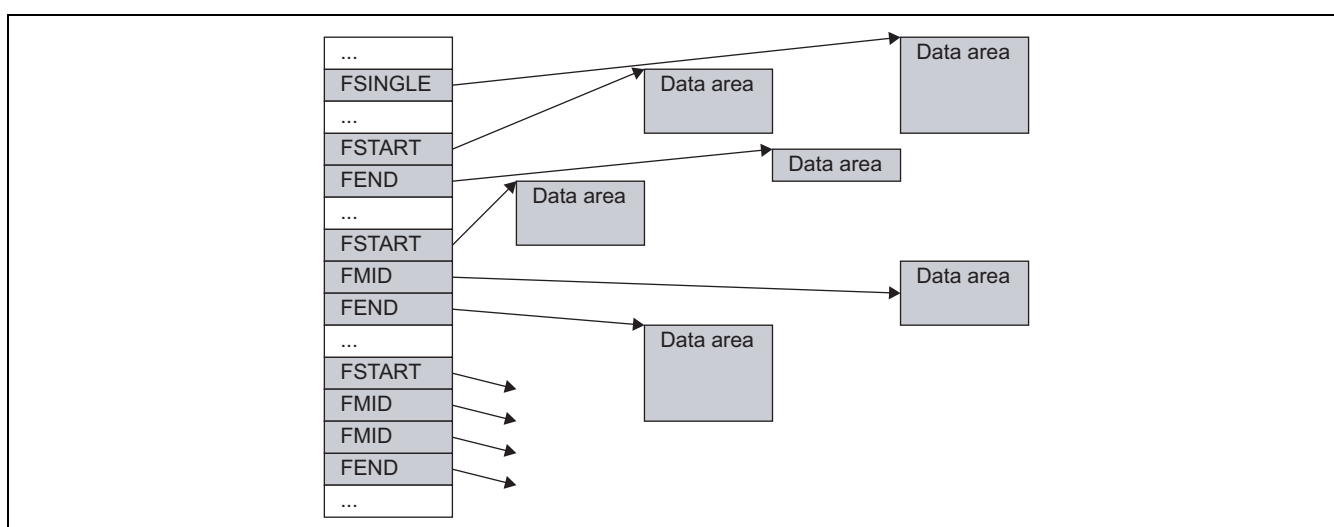
### 37A.3.3.8 How to Use Frame Data Descriptors

The descriptor data area size field (DESCR.DS) can specify up to 2048 bytes of Ethernet frame data per data area. Settings higher than 2048 (bytes) cannot be made.

In general, Ethernet frames are not of uniform length. The AVB-DMAC is capable of dividing frame data into multiple descriptors in order to minimize the memory capacity for frame data. This function allows processing of frames that are longer than the limit for descriptor data areas. Division can also be applied to frames on the basis of their data structures.

To handle frames and descriptors, four descriptor types (DESCR.DT) as FSTART, FEND, FMID and FSINGLE are defined.

Figure 37A.14 shows the mapping of frame data by frame data descriptors. The descriptor data areas are allocated to the URAM. For frames that require division into four or more data areas, additional FMID descriptors can be added as required.



**Figure 37A.14 Mapping of Frame Data**

For reception, set the descriptor data areas to the maximum size (i.e. give DESCR.DS its maximum value). The AVB-DMAC will store received frame data in the given area. If a received frame has more data than the maximum size, the AVB-DMAC will divide the data up.

For transmission, set the descriptor data area size field to the actual data size. The AVB-DMAC modifies the descriptor type (DESCR.DT) to FEMPTY after processing the relevant descriptor. The data size (DESCR.DS) and descriptor pointer (DESCR.PTR) fields retain their settings.

A descriptor data area including unused space produces an empty space between data areas. In reception, an “incremental data area” can be used to prevent empty spaces. For incremental data areas, see section 37A.3.4.3 (2), Incremental Data Areas.

As well as reducing the memory capacity taken up by the descriptor area in the URAM, division into frames can be used to identify different sections of data (e.g. for separating a header and data).

### 37A.3.3.9 How to Use Chain Control Descriptors

#### (a) Link Descriptors

The link descriptors can be used to set up cyclic descriptor chains (for details, see section 37A.3.3.2, Using Descriptor Chains in Queues)

After a LINK descriptor is processed, its descriptor type (DESCR.DT) is changed to LEMPTY. The descriptor pointer (DESCR.PTR) retains its setting.

After processing of a LINKFIX descriptor, the descriptor type (DESCR.DT) is not updated. Software can change the descriptor type (DESCR.DT), descriptor interrupt enable (DESCR.DIE), and descriptor pointer (DESCR.DPTR). However, DESCR.DT should not be modified by software. Take care to check the current descriptor address register (CDARq.CDA) before changing the descriptor pointer (DESCR.DPTR).

#### (b) EOS Descriptor

Use the EOS descriptor to divide a descriptor chain into various segments. The queue can continue even after an EOS descriptor.

In transmission, the response to an EOS descriptor is clearing of the transmit start request bit in the transmit configuration control register (TCCR.TSRQq) to 0.

In reception, the response is generation of a receive queue full interrupt (RIS2.QFFr), although if the frame currently being received is being divided for storage (received data such as those where some storage is in FMID- or FEND-type frames), the data are not completely stored.

### 37A.3.3.10 How to Use Hardware and Software Arbitration Descriptors

In hardware processing of descriptors, the empty descriptor types (FEMPTY, LEMPTY, and EEMPTY) are used to distinguish various descriptors. For software, they can be used to initiate checking for empty spaces, etc.

#### (a) FEMPTY, FEMPTY\_IS, FEMPTY\_IC, and FEMPTY\_ND

These descriptor types (DESCR.DT) are used for descriptors that do not contain effective data. Of these, only FEMPTY is used in transmission. The descriptor pointer of a FEMPTYxxx descriptor refers to a descriptor data area.

#### (b) LEMPTY

This descriptor type (DESCR.DT) is assigned to LINK descriptors after they have been processed. The descriptor pointer (DESCR.DPTR) of an LEMPTY descriptor still points to the linked descriptor.

#### (c) EEMPTY

This descriptor type (DESCR.DT) is assigned to EOS descriptors after they have been processed. The descriptor pointer (DESCR.DPTR) of an EEMPTY descriptor is not used.

### 37A.3.3.11 Synchronization between Descriptor Access by Hardware and Software

The allocation of descriptor types (DESCR.DT) to the URAM can be used to set up the primary synchronization between hardware and software. By this, the number of CPU accesses to registers of EthernetAVB can be minimized and performance can be increased.

Basic concepts of synchronization:

- Each descriptor type in the set is exclusively for processing by hardware or software, depending on the direction of transfer (see Table 37A.5, Summary of Descriptor Types).
- Software must not change a descriptor assigned to hardware processing (the hardware does not change descriptors assigned to software processing).

In the case of software processing, the software must process the information in the descriptor and the corresponding frame data before changing the descriptor type. If a descriptor type for hardware is set in DESCR.DT, the software should not change any part of the descriptor or of the corresponding frame data.

### 37A.3.3.12 Tips for Optimizing Performance in Handling Descriptors

The following items are recommended as ways to ensure the optimal use of data structures in the URAM.

They are not requirements, but using a different approach may increase the load on the system bus within the LSI chip.

- Register descriptors with 64-bit alignment (this does not apply to extended descriptors).
- While in operation mode, use LINKFIX instead of LINK whenever a descriptor need not be changed. Hardware modifies the descriptor type (DESCR.DT) fields of LINK descriptors.
- Frame data is accessed in blocks up to 128 bytes.
- The number of 128 byte borders (addresses H'xxx00 and H'xxx80) and frame data inside should be minimized.
- Design the descriptor chains in ways that minimize parallelism of processing. This helps in dividing the chains into segments allocated to different cache pages, and in arranging the different segments exclusively for access by software or hardware.
- Minimize the number of divided frames. This can reduce the overhead of descriptor handling.



### 37A.3.4 Control in Reception

The point of the AVB-DMAC is to transfer data between the E-MAC and URAM without intervention by the CPU.

AVB-DMAC needs descriptors that define the amounts of frame data to be stored and the locations. After the E-MAC receives a frame, it stores the received frame data and the conditions of reception as the E-MAC state. If the descriptor is extended, the time stamp is also stored. For a description of how to set up descriptors for use in reception, see section 37A.3.4.2, Setting Up Reception Descriptors.

The AVB-DMAC filters received frames to separate them into various classifications (separation filtering). More specifically, this is done to separate received frames into the various reception queues and to set the priorities of different classes of received frames. For more on separation filtering, see section 37A.3.4.1 (1), Separation Filtering.

Figure 37A.15 shows the reception data bus and the selection of queues for use in reception.

Each frame received from the E-MAC is stored in the reception FIFO; in parallel with this, the frame is analyzed to identify its type and the target queue number. After the E-MAC completes reception, the target queue number is generated and stored in the reception FIFO. Appending of a reception flag depends on the storage of one frame among the reception queues in the URAM, and the unread frame counter (UFC) is also associated with frame storage.

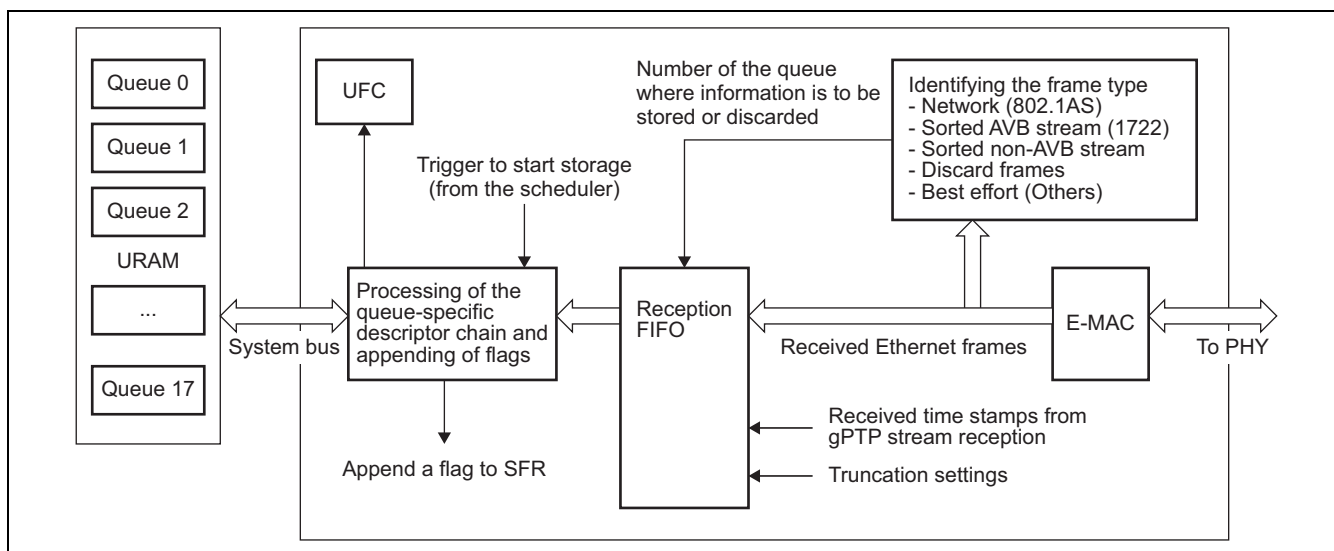


Figure 37A.15 Mechanism of General Reception Queue Selection

### 37A.3.4.1 Reception Queues

The AVB-DMAC applies its separation filtering mechanism to select the reception queue for storing a received frame. The AVB-DMAC stores all received frames in the URAM.

There are two conditions for the AVB-DMAC to discard a received frame.

- Detection of an error during reception by the E-MAC
  - Whether error frames are discarded or stored in reception queue 0 (best effort) depends on the setting of the error frame enable bit in the receive configuration register (RCR.EFFS). If error frames are to be stored (RCR.EFFS = 1), they are always stored in queue 0 (best effort). In this case, characteristics specific to the queue (e.g. truncation) will vary. If the storage of time stamps for reception queue 0 (best effort) is enabled (the time stamp enable bit in the receive configuration register RCR.ETS0 = 1), time stamps are stored even for error frames.
- Frame fails the separation filter
  - It depends on RCR.ESF if such frame is discarded or stored in receive queue 0 (best effort).

The flowchart in Figure 37A.16 shows how the AVB-DMAC selects the reception queue in accord with the frame type, including judgment by the separation filter. Selection of the queue starts when the E-MAC completes frame reception. The result is storage of the frame in the proper queue or the frame being discarded.

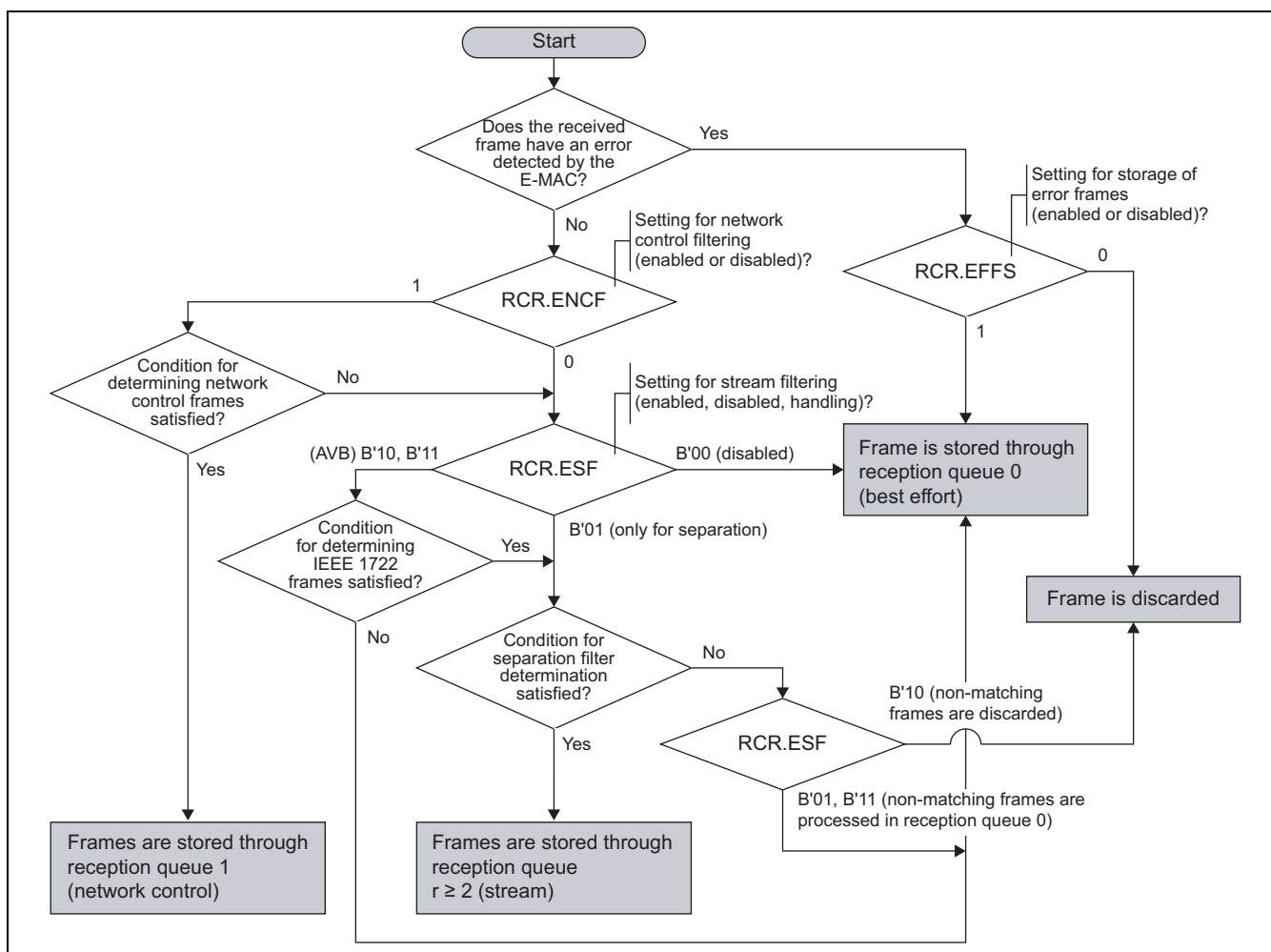


Figure 37A.16 Mechanism of Reception Queue Selection

Notes on the meanings of entries in the flowchart

- “Condition for determining network control frames”  
 The Ethernet destination address (DA) is 01:80:C2:00:00:0E.  
 The Ethernet type (ET) is 88:F7.
- “Condition for determining IEEE 1722 frames”  
 The Ethernet destination address (DA) is within the range from 91:E0:F0:00:00:00 to 91:E0:F0:00:FE:FF.  
 The VLAN tagged TPID (tag protocol identifier) field (VL) is 81:00.  
 The Ethernet type (ET) is 22:F0.
- “Condition for separation filter determination”  
 See section 37A.3.4.1 (1), Separation Filtering.

Figure 37A.17 shows the allocation of bits related to the network and stream types in Ethernet frames. The preambles of Ethernet frames are not taken into account.

Data bytes	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
Network type	DA1	DA2	DA3	DA4	DA5	DA6	SA1	SA2	SA3	SA4	SA5	SA6	ET1	ET2	...	...	...	...	...	...
Stream type	DA1	DA2	DA3	DA4	DA5	DA6	SA1	SA2	SA3	SA4	SA5	SA6	VL1	VL2	-	-	ET1	ET2	...	...

**Figure 37A.17 Data Bytes of Ethernet Frames Used in Classification**

**(1) Separation Filtering**

Separation filtering involves the checking of up to 64 bits (eight successive bytes) in received Ethernet frames. The setting for the first byte (i.e. the setting of the separation filter offset configuration register (SFO.FBP)), selects the part of frames to be used in separation filtering. There is also a common filter mask (set in the separation filter mask configuration register (SFMi.CFM)) that can be freely set to reduce the number of bytes used in separation filtering or to mask particular bits.

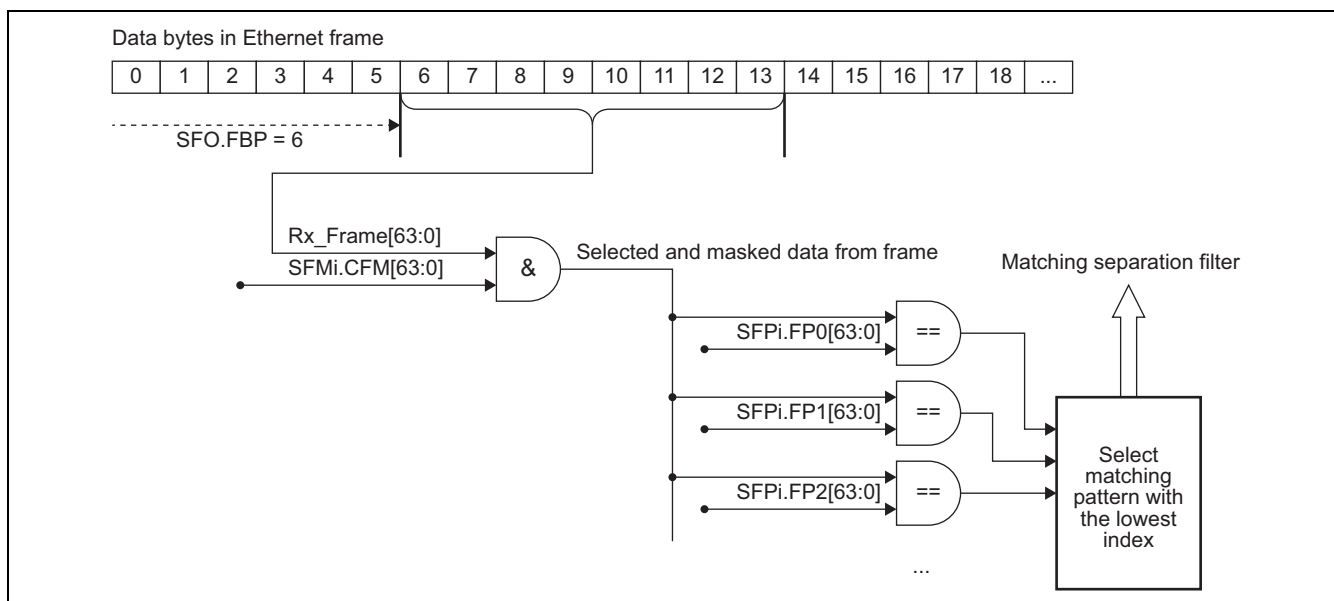
**Examples**

To use one byte in separation, set separation filter mask configuration register 0 (SFM0.CFM) to H'0000 00FF and separation filter mask configuration register 1 (SFM1.CFM) to H'0000 0000.

To use seven bytes in separation, set separation filter mask configuration register 0 (SFM0.CFM) to H'FFFF FFFF and separation filter mask configuration register 1 (SFM1.CFM) to H'00FF FFFF.

Note: If bits at some positions are set to 0 in the separation mask, in order to match with the pattern, the bits at the corresponding positions of the pattern must also be set to 0. Only those bits in which the separation filter pattern configuration register (SFPi.FPs) setting is equal to the separation filter mask configuration register (SFMi.CFM) are sorted by matching with received data.

Figure 37A.18 shows separation filtering. The selected data from a received frame (Rx\_Frame[63:0]) are masked by the common filter mask. As a result, the selected frame data can be obtained. This value is compared with all filter patterns. The separation filter circuit in the AVB-DMAC selects the filter pattern that matches the queue having the lowest index s or selects a flag to indicate that there is no matching separation pattern.



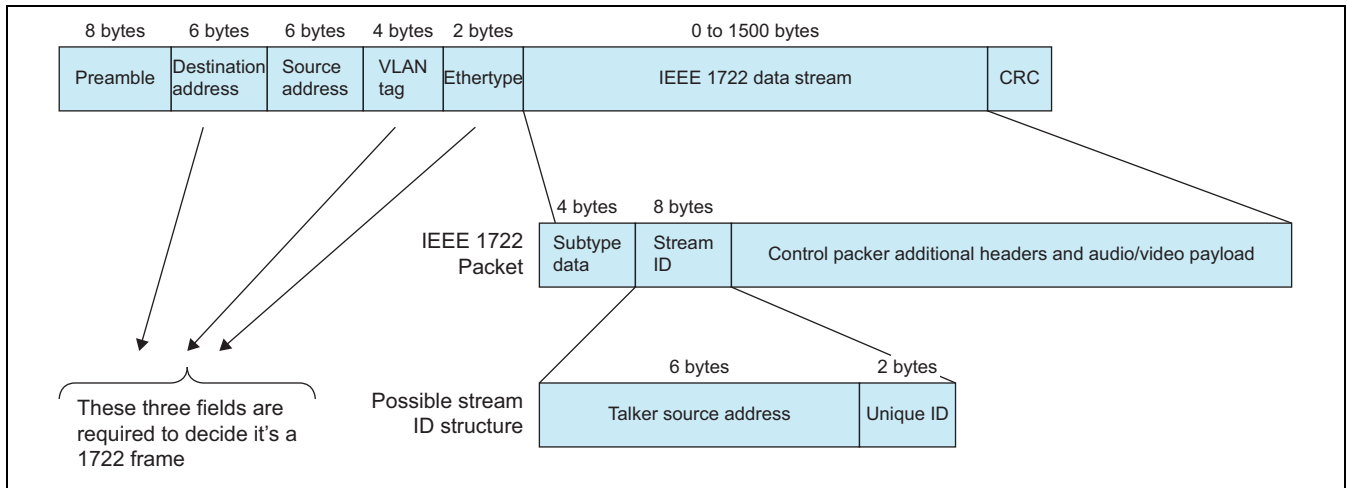
**Figure 37A.18 Separation Filtering**

**(2) Separating Streams**

The AVB-DMAC applies separation filtering to sort frames received in streams. An AVB network has a concept of “Talker” and “Listener”. A Talker is an end station that generates one or more streams. A Listener is an end station that has the role of being a sink for at least one stream. The various A/V streams are identified by 8-byte stream IDs.

The number of end stations within an AVB network and their roles differ with the application.

The stream ID is a general pattern of the AVB network for identifying one stream. Figure 37A.19 shows the bit allocation of bits in IEEE1722 Ethernet frames and stream ID fields.



**Figure 37A.19 IEEE 1722 Frame Layout and Stream ID**

The IEEE 1722 standard stipulates that the stream ID field starts from the 23rd byte (not counting the preamble). Accordingly, set the separation filter offset (SFO.FBP) to 22 in operations on IEEE 1722 streams. Set the separation filter mask (SFMi) and separation filter pattern (SFPi) in accord with the specification of the product in which the chip is being used.

Example: In the example of a stream ID shown in Figure 37A.19, the current application divides the field into the talker source address and the unique stream ID. The unique ID is used to differentiate between multiple streams from the same talker. Based on this, there are two settings for separation filter masking:

- To divide various streams into individual queues, set SFM0.CFM to H'FFFF FFFF and SFM1.CFM to H'FFFF FFFF.
- To divide streams from various talkers into individual queues, set SFM0.CFM to H'FFFF FFFF and SFM1.CFM to H'0000 FFFF. This excludes the unique ID from the filter condition.

### 37A.3.4.2 Setting Up Reception Descriptors

For reception, the descriptor mechanism is essentially as described in section 37A.3.3, Descriptors.

This section describes memory operations that are especially required in handling reception queues.

#### (1) Reception Descriptor Type

The type of a descriptor is defined by the descriptor type (DESCR.DT) field.

Table 37A.10 shows the descriptor types used in reception.

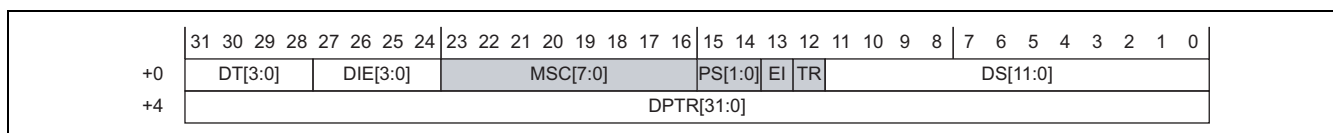
**Table 37A.10 Descriptor Types in Reception**

Descriptor Type (DESCR.DT)	Operation	Write-back
Frame Start (FSTART)	Condition for data not being stored in a reception queue: The RIS2.QFFr bit indicates that queue r is full and the received frame is not stored. Descriptor processing proceeds again in response to further reception.	Not changed
Frame Middle (FMID)	Same as FSTART	Not changed
Frame End (FEND)	Same as FSTART	Not changed
Frame Single (FSINGLE)	Same as FSTART	Not changed
Link (LINK)	Processing proceeds to the descriptor specified by DESCR.DPTR.	LEEMPTY
Fixed Link (LINKFIX)	Same as LINK	Not changed
End Of Set (EOS)	A stop point defined by software has been reached. A descriptor of this type within a divided frame (writing of FMID or FEND) stops the frame being stored and the frame is lost. RIS2.QFFr indicates that the frame has been lost. If this happens at the start of a frame (writing of FSTART or FSINGLE), storing of frames starts from the next descriptor. In either case, processing shifts to the next descriptor in the chain.	EEMPTY
Frame Empty (FEMPTY)	The descriptor can be used to store received data. Up to DESCR.DS bytes are stored in the descriptor data area. For details, see section 37A.3.4.3 (1), Storing Frame Data in the Descriptor Data Area.	FSTART, FMID, FEND, or FSINGLE
Frame Empty Incremental Start (FEMPTY_IS)	The descriptor can be used to store received data. All data for the frame are stored in the descriptor data area. DESCR.DPTR indicates the base address of the incremental data area. For details, see section 37A.3.4.3 (2), Incremental Data Areas.	FEND or FSINGLE
Frame Empty Incremental Continue (FEMPTY_IC)	The descriptor can be used to store received data. The remaining bytes of frame data are stored in the descriptor data area. DESCR.DPTR is undefined, but is written back at the start position within the incremental data area after processing. For details, see section 37A.3.4.3 (2), Incremental Data Areas.	FEND or FSINGLE
Frame Empty No Data storage (FEMPTY_ND)	The descriptor can be used to store received data. Up to DESCR.DS bytes are captured from the reception FIFO but not stored. After processing, DESCR.DS is written back as 0. For details, see section 37A.3.4.3 (2), Incremental Data Areas	FSTART, FMID, FEND or FSINGLE
Link Empty (LEEMPTY)	Same as FSTART	Not changed
EOS Empty (EEMPTY)	Same as FSTART	Not changed

## (2) Configuration of Reception Frame Data Descriptors

Figure 37A.20 shows the configuration of descriptors for use with reception queues. The reception-specific fields are the same whether the descriptor is normal or extended. The reception-specific fields (DESCR.MSC, DESCR.PS, DESCR.EI, and DESCR.TR) are described in Table 37A.11.

For the other fields and the descriptor types, see section 37A.3.3.6, Descriptor Type.



**Figure 37A.20 Configuration of Descriptor for a Received Frame**

**Table 37A.11 Configuration of a Received Descriptor**

Bit Name	Function
MSC	<p>E-MAC Status Code</p> <p>These bits indicate errors in reception detected by the E-MAC.</p> <p>In the case of a divided frame, these bits are set to the same value within all descriptors for the frame data. Details of the bits are as follows.</p> <p>MSC[7]: Received frame has a multicast address.</p> <p>MSC[6]: Carrier extend error</p> <p>MSC[5]: Carrier sense error</p> <p>MSC[4]: Received frame has alignment error.</p> <p>MSC[3]: Received frame is too long.</p> <p>MSC[2]: Received frame is too short</p> <p>MSC[1]: Error in frame reception (PHY detects an error)</p> <p>MSC[0]: Received frame has a CRC error.</p>
PS	<p>Padding Selection</p> <p>These bits specify whether frame data are to be padded when stored in the incremental data area.</p> <p>Insertion of padding data is in accord with the settings in the RPC register.</p> <p>B'00: Padding is not to be inserted.</p> <p>B'01: Padding data may be inserted. This depends on the RPC settings.</p> <p>Other settings are not effective.</p>
EI	<p>Error Indication</p> <p>This bit indicates the detection of an error in frame data while a frame was being stored.</p> <p>The bit is set to 1 for a descriptor in which an error has been detected. If the descriptor is for a divided frame, storage of the frame is aborted.</p> <p>0: No error</p> <p>1: Error is detected</p>
TR	<p>Truncation Indication</p> <p>This bit indicates whether frame data received from the E-MAC have been truncated before being stored.</p> <p>These bits are set to the same value within all frame data descriptors for a divided frame.</p> <p>0: Data have not been truncated.</p> <p>1: Data have been truncated.</p>

**Note:** The RCR.EFFS bit specifies whether or not frames with errors detected by the E-MAC are to be stored in the URAM. When the storing of error frames is disabled, error codes are not written to DESCR.MSC.

### 37A.3.4.3 Reception Processing

After initialization, the AVB-DMAC is able to select the proper reception queue and store received frames in the data area in the URAM as indicated by the descriptor. The AVB-DMAC continues to store received data in the URAM as long as space is available for descriptors and data areas.

Received frames are classified and stored in the reception FIFO in accord with the algorithm described in section 37A.3.4.1 (1), Separation Filtering.

If the reception FIFO contains even one frame, storing is executed to the reception queue.

If there is even one empty data descriptor in a queue for which reception has started, the storage of frame data starts. Received frames for a queue that is already full (there is no empty frame descriptor or the UFC stop level has been reached) are discarded from the reception FIFO. This ensures that one queue being full does not prevent the storage of data in the other queues.

#### (1) Storing Frame Data in the Descriptor Data Area

Frame data for storage are assumed to be in either of the two patterns described below.

- The data for an entire frame will fit in the descriptor data area.
  - In this case, the descriptor type (DESCR.DT) is FSINGLE.
- Frame data to be stored in the descriptor data area arrive in divided form.
  - In this case, FSTART is written to the descriptor type (DESCR.DT) bits of the first descriptor of the frame data to arrive and FMID and FEND are written to the type bits of descriptors for subsequent data.

The descriptor type is updated by the AVB-DMAC in the last step of descriptor processing, so software can always access the descriptor assigned to DESCR.DT.

When normal synchronization mode is used, the CPU can write FEMPTYxxx directly to the descriptor type field after processing the stored element. Do not change the descriptor or any part of the descriptor data area after FEMPTYxxx is written to DESCR.DT.

#### (a) Storing Frame Data for a Whole Single Frame

For a frame with an FSINGLE descriptor, all data for the frame are held at the position defined by DESCR.DPTR. DESCR.DS indicates the length of the received frame.

If DESCR.DS is bigger than the actual size of a received frame, the FSINGLE descriptor is stored in place of the FEMPTY or FEMPTY\_ND descriptor after processing.

Also, the FSINGLE descriptor is stored in place of the FEMPTY\_IS or FEMPTY\_IC descriptor, which always hold the descriptor data area greater than all frame data in Rx-FIFO after processing.

#### (b) Storing Frame Data as Divided Frames

Divided frames are handled in the same way as a single frame. A frame stored with divided descriptors must be recombined before use. DESCR.EI and DESCR.TS are only valid in the last descriptor of the sequence for a divided frame.

Note: If the data area size setting in DESCR.DS is not a multiple of four, the number of bytes set in DESCR.DS is fetched from the reception FIFO and the remaining bytes are used as the next storage area.

After a received frame is divided into different descriptors, each storage element is handled separately, and the descriptor type is assigned by software after processing. Accordingly, an error frame (FEMPTYxxx instead of FMID or FEND) may exist while a descriptor chain is being processed. In such a case, the CPU must postpone processing of the error frame to the next trigger point.



**(c) No Data are Stored**

The application specification may lead to some types of received frames being unimportant (for example, when the application only requires stream data from the Ethernet frames). Storing frames in divided form makes separating out the unnecessary parts of Ethernet frames possible.

If part of a divided frame is not required, use the FEMPTY\_ND descriptor for that part so that it is not stored in the URAM. Not storing the data negates the need for bandwidth on the data bus, improving the overall performance.

When an FEMPTY\_ND descriptor is processed, DESCR.DS is set to 0. This brings the frame data section of the descriptor into agreement with the FEMPTY type. DESCR.DS = 0 is for the unique identification of the descriptor after writing.

**(2) Incremental Data Areas**

Secure space in the URAM for storing received data. Even when data are placed in the URAM area such that all descriptor data areas of a chain are contiguous, a received frame being shorter than the descriptor data area will lead to an empty space. Figure 37A.21 shows an example of settings and the memory map.

Certain applications require that data areas be contiguous (e.g. when received data are to be processed other than by hardware as the A/V codec module). When the length of received frames differs (e.g. when payloads vary between having one or two A/V packages), the use of a static pointer in the descriptor produces empty spaces in the data area. This may necessitate direct additional processing to remove the empty spaces.

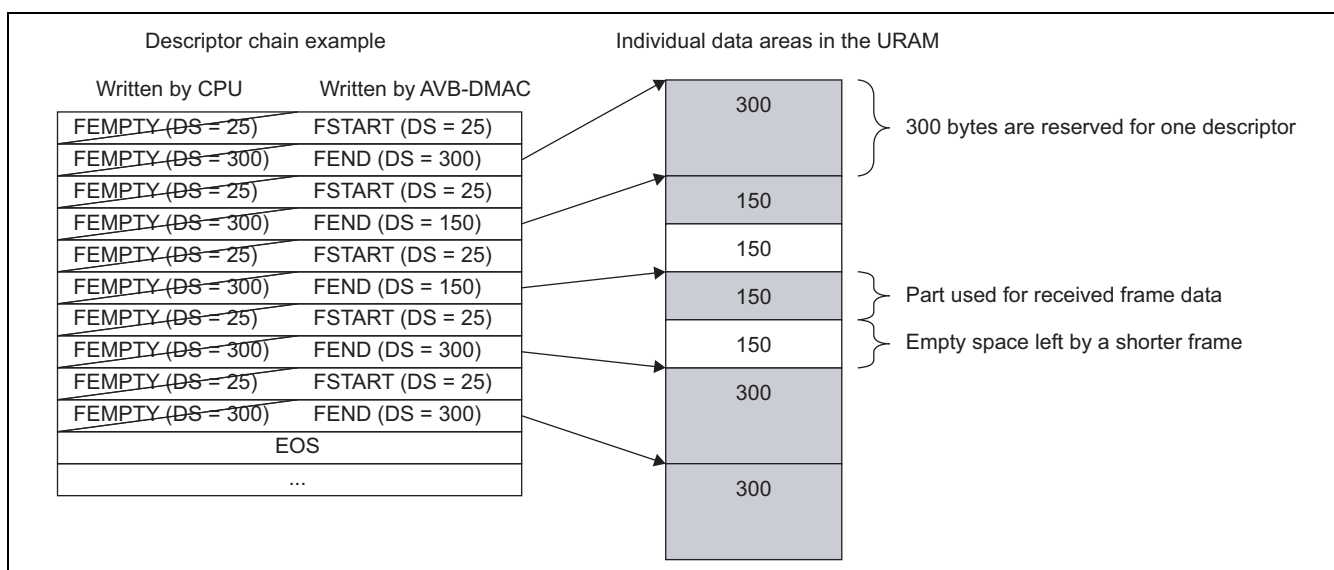
Accordingly, and to reduce the CPU load imposed by copying data, the AVB-DMAC supports an “incremental data area” function.

When incremental data areas are in use, all descriptors use a common data area for storage. One descriptor (FEMPTY\_IS) defines the base address of the incremental data area and the next descriptor (FEMPTY\_IC) within the descriptor chain holds received data. Figure 37A.22 shows an example of settings and the memory map.

Use of an incremental data area does not reduce the memory space in the individual descriptor data areas.

The hardware and software synchronization strategy and performance are also not changed.

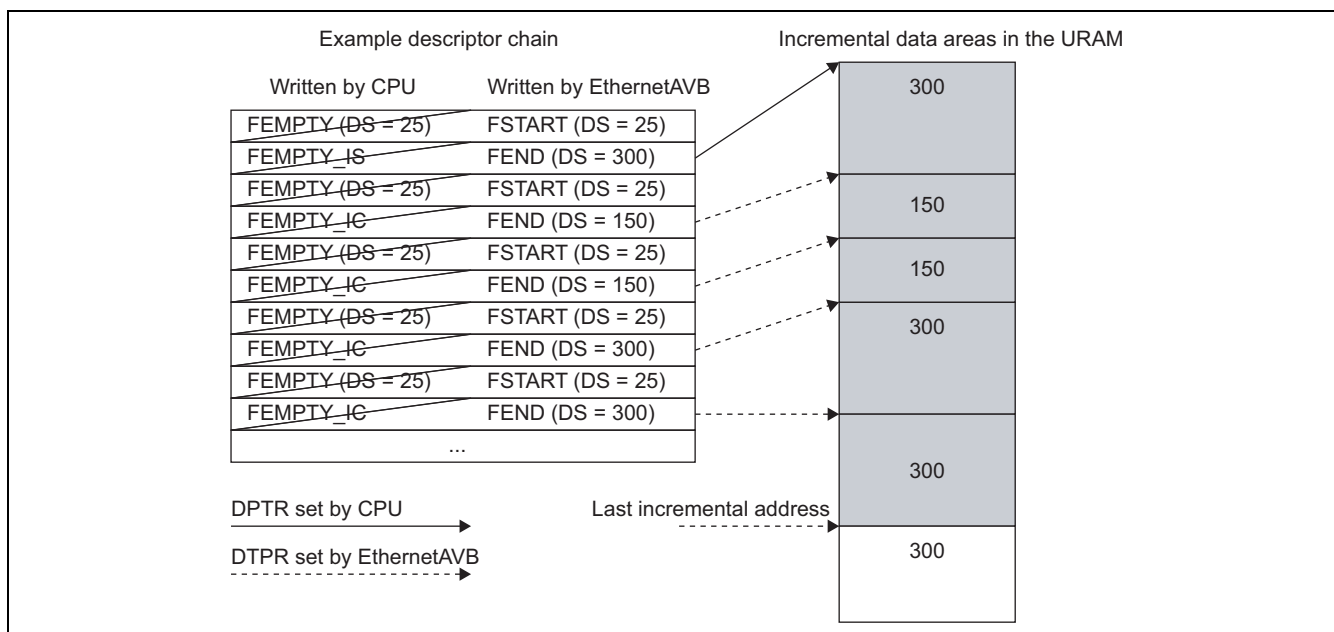
It is also possible to divide a frame up among various descriptors in a way that reflects its structure (e.g. one descriptor for the Ethernet header and one for the data payload).



**Figure 37A.21 A Reception Queue Using Individual Descriptor Data Areas**

Figures 37A.21 and 37A.22 show how control of the data storage areas by a descriptor chain varies according to whether individual or incremental data areas are in use. The chains are configured for storing received frames consisting of a 25-byte header (which is treated as one descriptor; and is outside the scope) and a 150- or 300-byte payload (whether one or two 150-byte payload packages are transmitted with one Ethernet frame depends on the data source).

In Figure 37A.21, the EOS descriptor is added as an example of a re-synchronization point. If the frame source transmits a frame containing more than 325 bytes, the frame will be divided among three descriptors, meaning that synchronization of the header and data sequences is lost. Despite this, however, the frame is not divided across the EOS descriptor, so recovery is automatic without software interaction. The EOS is not required with the incremental descriptors because all data being processed are always stored while an incremental data area is in use.



**Figure 37A.22 Reception Queue Using a Common Incremental Data Area**

As Figure 37A.22 shows, when data are stored in an incremental data area, the descriptor pointers in the FEMPTY\_IC descriptors (DESCR.DPTR) are updated. Accordingly, the resulting FEND or FSINGLE descriptor is in the same format as after writing to an FEMPTY descriptor.

Software captures received data from an incremental data area, which has no empty storage areas between frame data. The only empty space is that at the end of the incremental data area. The sizes of incremental data areas and of blocks of data for storage in incremental data areas must be multiples of four bytes. When the amount of data for storage in an incremental data area is not a multiple of four bytes, from one to three bytes of empty space will be produced. DESCR.DS can be read to check for such empty spaces.

CPU cannot restrict directly the amount of received data stored by an incremental descriptor (FEMPTY\_IS, FEMPTY\_IC) as this is possible for other descriptors (FEMPTY, FEMPTY\_ND) by DESCR.DS. Incremental descriptors store always all received data.

#### (a) Setting Up an Incremental Data Area

A descriptor chain in the incremental data area having N descriptors (one FEMPTY\_IS and N-1 FEMPTY\_IC) means that the incremental storage area of N times of maximum frame size is needed.

As Figure 37A.22 shows, DESCR.DPTR of an FEMPTY\_IS descriptor indicates the base address of the incremental data area. The next FEMPTY\_IS descriptor in the chain indicates the processing step where data must be stored in the incremental data area.

**(b) Processing an Incremental Data Area Based on Descriptors**

Since data processing by the CPU is the same regardless of how the AVB-DMAC stores the data, data stored in an incremental data area do not require any special handling.

**(c) Padding**

Use padding for received frame data that are not aligned correctly in the specified memory structure. Padding can be set individually for each descriptor. Accordingly, in the reception of divided frames, padding can be restricted to only those frames that require it (e.g. A/V payload data.)

Padding can also be used to optimize system performance in an incremental data area (e.g. to prevent inefficient access by aligning received data with 32-byte boundaries in the incremental data area), as well as to fulfill application-specific requirements for specified memory structures (e.g. formats required by other modules that will be processing the received data).

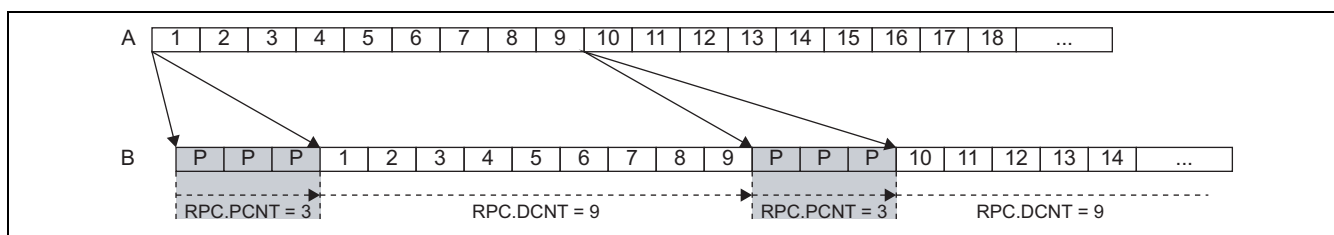
Padding can only be used in an incremental data area.

The value H'0000 0000 is always used in padding.

Padding is the addition of the number of words (from one to seven 32-bit words) set in the stored padding counter in the receive padding configuration register (RPC.PCNT). This padding is repeatedly inserted in accord with the value in the stored data counter (RPC.DCNT) (from one to 255 32-bit words). When the stored data counter (RPC.DCNT) reaches 0, however, padding is not repeated.

The first word of padding is always inserted at the position specified by DESCR.DPTR. When divided frames are in use, a padding word can be inserted at any byte position, and padding is handled on a 32-bit basis (e.g. an incremental data area where the first descriptor is for a 42-byte header data and the second descriptor holds padded payload data).

The next figure shows a general example of how padding is inserted and an example of setting up padding. A indicates frame data A received by the E-MAC, and B indicates the frame data stored in the descriptor data area (32-bit word units).



**Figure 37A.23 Example of a Padding Setting**

Both padding and received frame data are counted in the descriptor size (DESCR.DS).

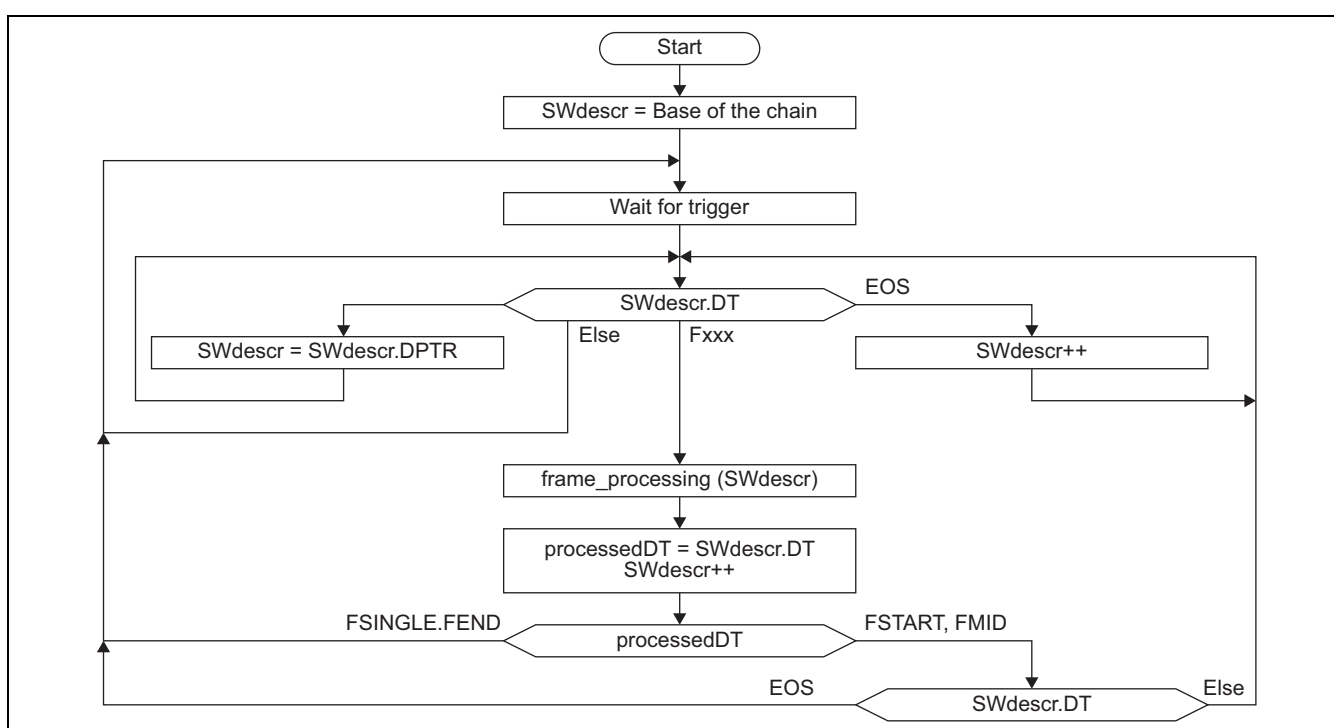
### (3) Mode with Write-Back

Constructing a descriptor chain requires software (see Figure 37A.24).

In the example in the figure, the variable SWdescr (software descriptor pointer) is a structure to identify a descriptor being processed. SWdescr must be initialized after operation mode is entered and a descriptor base address load request (DLR.LBAq) is executed (condition for starting the flow of software operations).

The frame\_processing() function processes the stored data. The function can use SWdescr.DT to check whether processing of a frame is completed. How frame data are processed differs with the application, so create functions that handle processing in accord with the specification.

The processing section is common to all modes of reception. The number of frames processed in response to each trigger can be restricted. When multiple frames have to be processed in a batch, waiting for individual trigger boxes must be skipped for these frames.



**Figure 37A.24 Flow of Reception Descriptor Processing (with Write-Back)**

### (4) Support for Reception Time Stamps

Capturing reception time stamps is essential for IEEE 802.1AS time synchronization. Other types of received frames may also require that a reception time stamp be appended; this depends on the application. The AVB-DMAC supports reception time stamps based on the gPTP timer by storing time stamps, which have been captured when Start Frame Delimiter (SFD) of a received frame is arrived, in the last frame data descriptor (FEND or FSINGLE). For the gPTP timer, see section 37A.3.7.1, gPTP Timer.

When time stamps are to be stored, use extended descriptors for the entire reception queue. Furthermore, time stamps are always stored for reception queue 1 (network control). Time stamps for reception queue 0 (best effort) and reception queue  $r$  ( $r \geq 2$ ; for stream data) can be selected by the time stamp enable bits in the receive configuration register (RCR.ETS0 or RCR.ETS2).

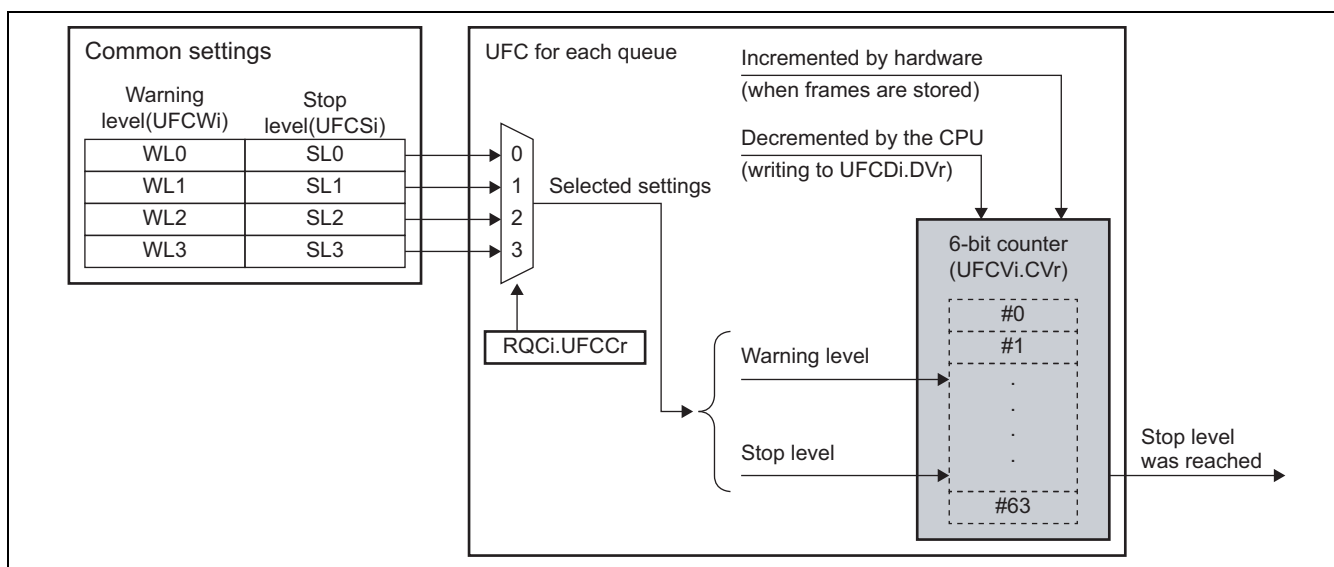
### 37A.3.4.4 Unread Frame Counters

Each reception queue has an unread frame counter (UFCVi). Use the unread frame counter configuration bits in the receive queue configuration register (RQCi.UFCCr) to select from among the four warning and stop levels for each unread frame counter. The 0 setting disables the stop and warning functions. For how to set this up, see Figure 37A.25.

Operations of the AVB-DMAC (hardware) and CPU (software) drive an unread frame counter (UFC) in the following ways.

- The hardware indicates that it has added a new frame to the descriptor chain for the queue (this increments the counter).
- Software indicates how many frames from the descriptor chain it has processed by writing to the corresponding bits of the unread frame counter decrement register for the queue (this decrements the register by the number written).

The unread frame counter is based on the number of frames stored in the URAM and is only incremented by one even when a received frame is divided into different descriptors. Failure in storing a descriptor chain requires care because this may unread frame counter may fail in synchronization as described in section 37A.3.4.4 (1), Unread Frame (UFC) Synchronization Failure.



**Figure 37A.25 Overview of an Unread Frame Counter**

Unless synchronization of hardware and software is lost, the current unread frame counter value (UFCVi.CVr) indicates the number of unread frames in the queue.

The indicator that the stop level has been reached prevents the storage of further received frames in the descriptor chain. Selecting 0 as the stop level disables this function. Otherwise, further received frames for the queue are discarded once its unread frame counter reaches the stop level. Activation of the unread frame counter stop function is indicating by setting of the receive queue full interrupt flag in the receive interrupt status register 2 (RIS2.QFFr).

Set the unread frame counter warning level configuration register (UFCW) and the unread frame counter stop level configuration register (UFCS) for each reception queue that will use the unread frame counter function while the current operating mode is configuration mode.

### (1) Unread Frame (UFC) Synchronization Failure

The unread frame counters do not recognize failure to store a frame in the URAM. In other words, the AVB-DMAC increments the counter for a queue each time it captures a frame for that queue from the reception FIFO whether or not it succeeds in storing the frame normally in the descriptor chain.

In general, synchronization of hardware and software fails under the following conditions.

- An unread frame counter reaching its maximum value  
When the value of a counter in an unread frame counter register  $i$  (UFCVi) ( $i = 0$  to  $4$ ) reaches 63, synchronization for the corresponding queue can fail.  
The CPU can only judge that a failure in synchronization has not occurred when the stop level is set to 63.
- A queue not having enough space for a descriptor  
In this case, the corresponding receive queue full interrupt flag (RIS2.QFFr) in receive interrupt status register 2 (RIS2) is set.  
If an unread frame counter reaches its stop level while synchronization remains normal, the receive queue full interrupt flag (RIS2.QFFr) in the receive interrupt status register 2 (RIS2) is set. Software must respond to this.
- A problem occurring during access to memory

The result of a failure in synchronization is the unread frame counter indicating that the corresponding descriptor chain may contain more available frames than it actually can. To retrieve the correct starting point for operations, use the descriptor base address load request (DLR.LBAq) for the given queue.

### 37A.3.5 Transmission Control

Areas in the URAM for storing transmission descriptors must also be secured (for descriptors, see section 37A.3.3, Descriptors).

The AVB-DMAC fetches data from the URAM in accord with the procedure the descriptor describes. The descriptor also retains tag information once the frame has been fetched for transmission. The tag information is used to maintain the relationships between status and time stamps for the software and the AVB-DMAC. The status and time stamp information for transmitted frames remains accessible after their transmission is completed.

#### 37A.3.5.1 Transmission Modes

The AVB-DMAC has two modes of transmission.

- AVB transmission mode  
This mode is selected by the priority level setting for the transmission queue in the transmit configuration register (setting of the TGC.TQP[1:0] bits) being B'01 or B'11.
- Non-AVB transmission mode  
This mode is selected by the priority level setting for the transmission queue in the transmit configuration register (setting of the TGC.TQP[1:0] bits) being B'00.

##### (1) AVB Transmission Mode

AVB transmission supports the control of traffic through the output port to implement various traffic classes.

##### (a) Support for Traffic Classes and Associated Priority

When transmission is in AVB transmission mode, streams of traffic are transmitted in accord with the part of the AVB specification called Forwarding and Queuing for Time Sensitive Streams (FQTSS; for details on this, see the IEEE 802.1Q standard).

In the AVB specification, at least one queue for a reserving stream under the Stream Reservation Protocol (SR stream) and at least one queue for a non-SR stream are present, and the queues for SR traffic is Highest priority queue.

The AVB-DMAC supports four traffic classes: SR class A, SR class B, network control (NC) traffic (gPTP frames), and best effort (BE) traffic. Allocating a specific queue to network control (NC) frames ensures the control of synchronization.

The AVB-DMAC realizes compliance with the AVB standards by handling queues with the following architecture (in terms of traffic classes).

- Four transmission queues (Q3, Q2, Q1, and Q0) are available.
- Q3 and Q2 are for SR streams (one each for class A and class B).
- Q1 is for low-bandwidth network control (NC) traffic (gPTP frames)
- Q0 is for other types of traffic (MSRPDU\*<sup>1</sup>, MVRPDU\*<sup>2</sup>, best effort (BE), etc.)

Notes: 1. MSRPDU: Multiple Stream Registration Protocol Data Unit  
2. MVRPDU: Multiple VLAN Registration Protocol Data Unit

Fetching from queues proceeds in order of priority of the above traffic types. Three systems of priority are available through the setting of the transmit queue priority bits in the transmit configuration register (TGC.TQP[1:0]). In the default priority scheme, which is called AVB mode 1 (selected by TGC.TQP[1:0] = B'01), operation of the AVB-DMAC is fully in accord with the AVB specification. AVB mode 2 (transmit queue priority bits (TGC.TQP[1:0] = B'11) is an alternative priority scheme and varies from the AVB specification. Using this scheme thus requires more care. The other setting is for non-AVB-mode transmission.

**Table 37A.12 Default and Alternative Priority Orders in AVB Transmission Mode**

Priority Schemes (AVB Mode)	Priority Order of Queues
Default	Q3 (SR class A) > Q2 (SR class B) > Q1 (NC) > Q0 (BE)
Alternative	Q1 (NC) > Q3 (SR class A) > Q2 (SR class B) > Q0 (BE)

**(b) Transmission Selecting Algorithm and CBS**

The algorithm the AVB-DMAC applies to select frames for transmission is in accord with the specifications under section 8.6.8, Transmission selection, of the IEEE 802.1Q standard. For AVB mode, the CBS (credit-based shaping) algorithm is applied to the class A and class B SR queues (Q3 and Q2). Use of the CBS enables correct handling of the priorities of transmission from the SR queues. For the CBS algorithm, see section 37A.3.6, CBS (Credit-Based Shaping).

When the following conditions both hold, transmission from an SR queue (Q3 or Q2) proceeds at the specified time.

- The queue contains at least one frame ready for transmission.
- The queue has available credit.
- Unless an SR queue satisfies the above conditions, a higher priority queue is not present (not ready for transmission).

A non-SR queue (Q1 or Q0) is selected if the conditions below both hold.

- The queue contains at least one frame ready for transmission.
- As well as the above condition, a higher priority queue is not present (not ready for transmission).

Figures 37A.26 and 37A.27 are flowcharts of selection for transmission in AVB mode 1 (default) and AVB mode 2 (alternative).



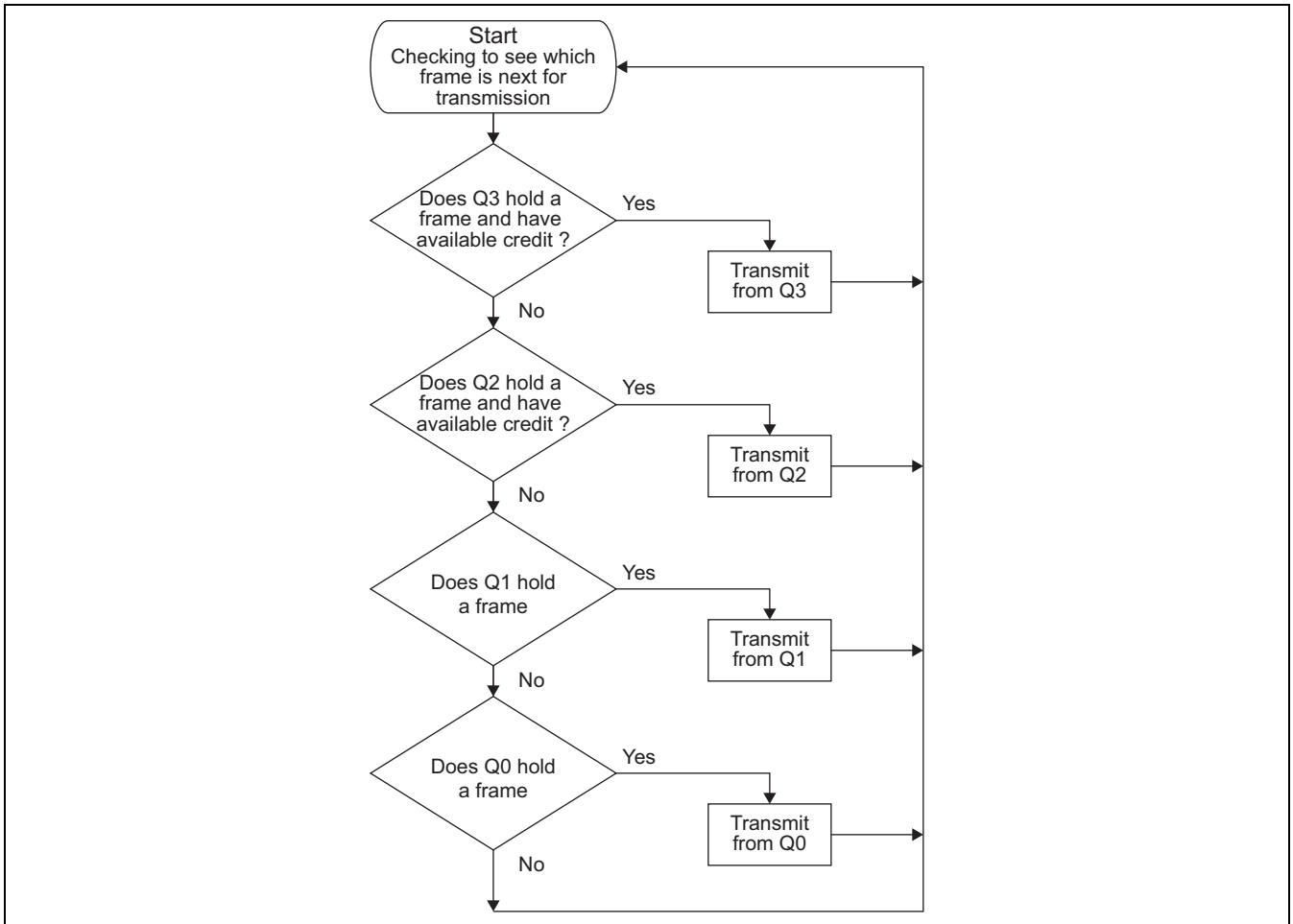


Figure 37A.26 Flow of Selection for Transmission in AVB Mode 1 (Default)

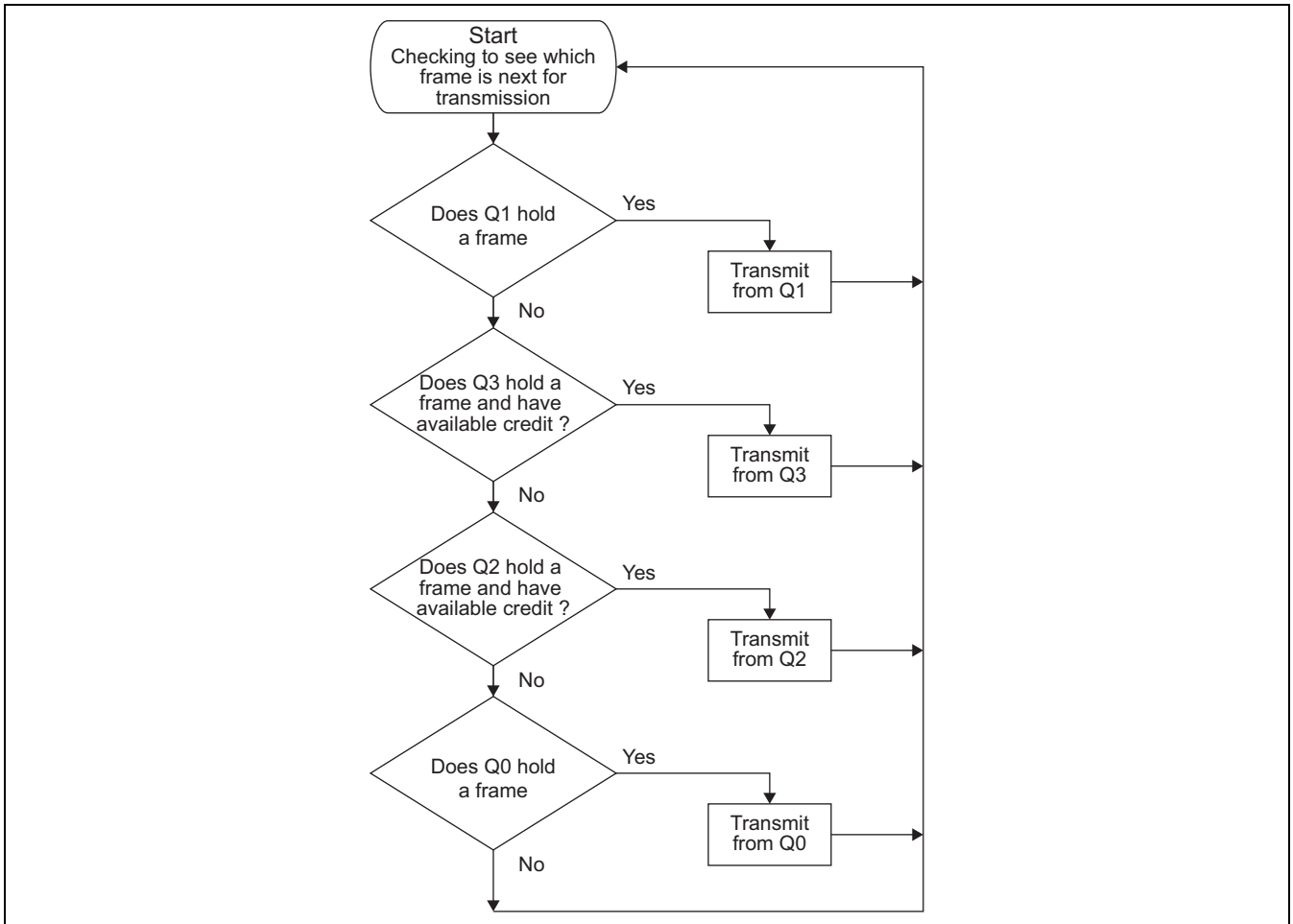


Figure 37A.27 Flow of Selection for Transmission in AVB Mode 2 (Alternative)

## (2) Non-AVB Transmission Mode

In non-AVB transmission mode, an absolute priority scheme is used. The SR class is not supported and the CBS algorithm is not used.

In non-AVB transmission mode (when the transmit queue priority bits in the transmit configuration register (TGC.TQP[1:0]) are B'00), data is fetched for transmission in a strict order of priority ( $Q3 > Q2 > Q1 > Q0$ ).

Figure 37A.28 shows the flow of selection in non-AVB transmission mode.

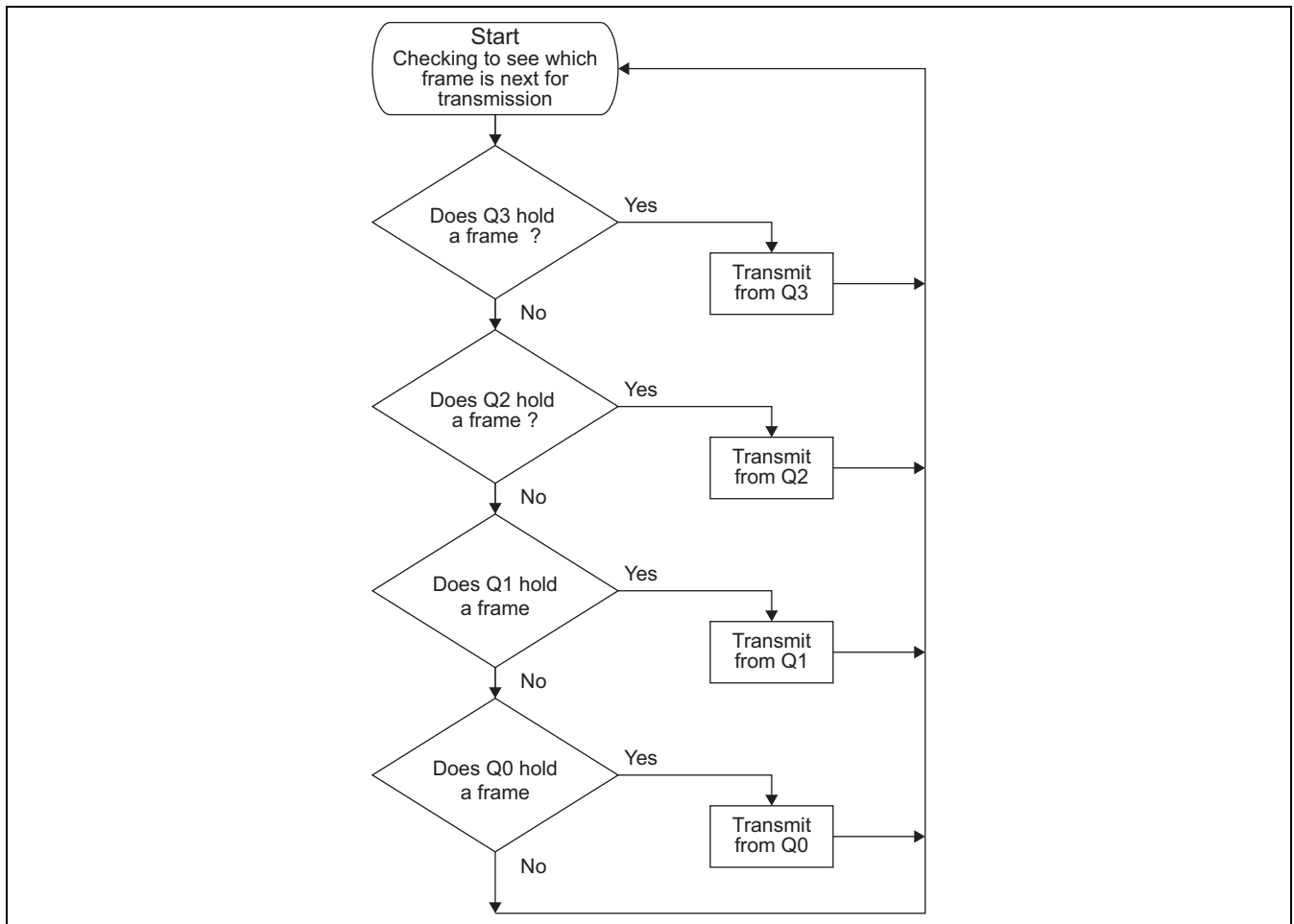


Figure 37A.28 Flow of Selection for Transmission in Non-AVB Mode

### (3) Setting the Size of the Transmission FIFO

The transmission FIFO is made up of 124 clusters. Each cluster can hold up to 128 bytes.

The size of the part of the transmission FIFO for use by each of the four transmission queues can be set by the corresponding transmit queue configuration q bits in the transmit control register (TGC.TBDq). The setting of TGC.TBDq is fixed to 2.

#### General Usage Examples:

Q0: Frames containing up to 1500 bytes  $\rightarrow 1500/128 = 11.7 \rightarrow 12$  clusters

Q1: Frames containing up to 1024 bytes  $\rightarrow 1024/128 = 8.0 \rightarrow 8$  clusters

Q3: Frames containing up to 1996 bytes  $\rightarrow 1996/128 = 15.6 \rightarrow 16$  clusters

Q4: Frames containing up to 1996 bytes  $\rightarrow 1996/128 = 15.6 \rightarrow 16$  clusters

When the depth of all transmission queues is 2, only the following number of clusters is required.

$$2 \times (12 + 8 + 16 + 16) + 16 = 2 \times 52 + 16 = 120$$

In the worst case (each of the transmission queues holds 1996 bytes),  $2 \times 64 + 16 = 144$  clusters are required, so the maximum length of transmission frames must be less than 1996 bytes for some queues.

### 37A.3.5.2 Setting Up Transmission Descriptors

#### (1) Transmission Descriptor Type

The type of a descriptor is defined by the descriptor type (DESCR.DT) field.

Table 37A.13 shows the descriptor types used in transmission.

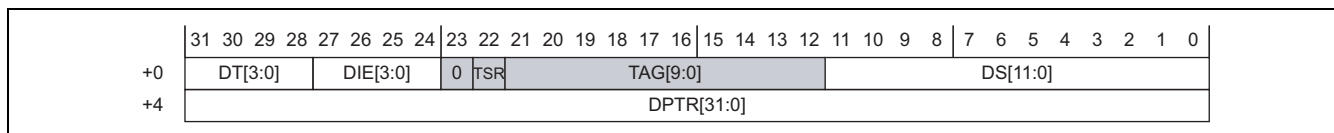
**Table 37A.13 Descriptor Types in Transmission**

Descriptor Type (DESCR.DT)	Operation	Write-back
Frame Start (FSTART)	The AVB-DMAC fetches the first of the data for the divided frame and proceeds to processing of the next descriptor.	FEMPTY
Frame Middle (FMID)	The AVB-DMAC fetches the second or subsequent data for the divided frame and proceeds to processing of the next descriptor.	FEMPTY
Frame End (FEND)	The AVB-DMAC fetches the last of the data for the divided frame. The frame of data that has been fetched to the transmission FIFO is ready for transmission by the E-MAC, and then the AVB-DMAC proceeds to processing of the next descriptor.	FEMPTY
Frame Single (FSINGLE)	The AVB-DMAC fetches the frame of data. The frame of data that has been fetched to the transmission FIFO is ready for transmission by the E-MAC, and then the AVB-DMAC proceeds to processing of the next descriptor.	FEMPTY
Link (LINK)	Processing proceeds to the descriptor specified by DESCR.DPTR.	LEEMPTY
Fixed Link (LINKFIX)	Same as LINK	Not changed
End Of Set (EOS)	This is a transmission stop point defined by software This leads to clearing of the transmit start request bit (TCCR.TSRQt), which stops transmission. When the TCCR.TSRQt is again set to 1 (a new transmission start request is issued), processing proceeds to the next descriptor.	EEMPTY
Frame Empty (FEMPTY)	No frame data are ready for transmission This leads to clearing of the transmit start request bit (TCCR.TSRQt), which stops transmission. When the TCCR.TSRQt is again set to 1 (a new transmission start request is issued), processing starts at this descriptor.	Not changed
Link Empty (LEEMPTY)	Same as FEMPTY	Not changed
EOS Empty (EEMPTY)	Same as FEMPTY	Not changed

**(2) Configuration of Transmission Frame Data Descriptors**

Figure 37A.29 shows the configuration of descriptors for use with transmission queues. The transmission-specific fields (DESCR.MSR, DESCR.TSR, and DESCR.TAG) are described in Table 37A.14.

For the other fields and the descriptor types, see section 37A.3.3.6, Descriptor Type.



**Figure 37A.29 Configuration of Descriptor for a Transmitted Frame**

**Table 37A.14 Configuration of a Transmission Descriptor**

Bit Name	Function
TSR	Time Stamp Store Request This bit specifies whether the transmission time stamp is to be stored within the EthernetAVB module. 0: The time stamp status FIFO within the EthernetAVB module does not retain a transmission time stamp. 1: The time stamp status FIFO within the EthernetAVB module retains a transmission time stamp. This bit is available while the current DESCR.DT is FEND or FSINGLE.
TAG	Frame Tag This TAG field is used to associate each frame data with a time stamp. Frame TAG is not required but is recommended. This bit is available while the current DESCR.DT is FEND or FSINGLE.

For the time stamp FIFO function, see section 37A.3.5.4, Time Stamping in Transmission.

### 37A.3.5.3 Transmission

#### (1) Transmitting Frames

Setting the transmit start request bit in the transmit configuration control register (TCCR.TSRQt) starts the transfer of frames from the corresponding transmission queue.

The descriptor in the current descriptor address (CDARq.CDA) for the queue t (with q = t) is read first.

If this descriptor is a descriptor for frame transmission (FSINGLE, etc.), the AVB-DMAC fetches the frame data from the data area indicated by the descriptor, writes FEMPTY back to the descriptor type (DESCR.DT) bits to indicate completion of this processing, then proceeds to processing of the next descriptor.

If the descriptor is not for transmission, processing is as dictated by the given descriptor (for these descriptors, see the descriptions in section 37A.3.3, Descriptors).

If a base address load request is issued for a descriptor chain while it is being processed (by setting 1 in the LBAq bit for transmission queue q that is currently being processed in the descriptor base address load request register, DLR), processing proceeds to the new descriptor chain. Changing the chain does not interrupt frame fetching, but note that frames that have not been fetched from the old chain remain where they are.

Figure 37A.30 shows descriptor processing during transmission.

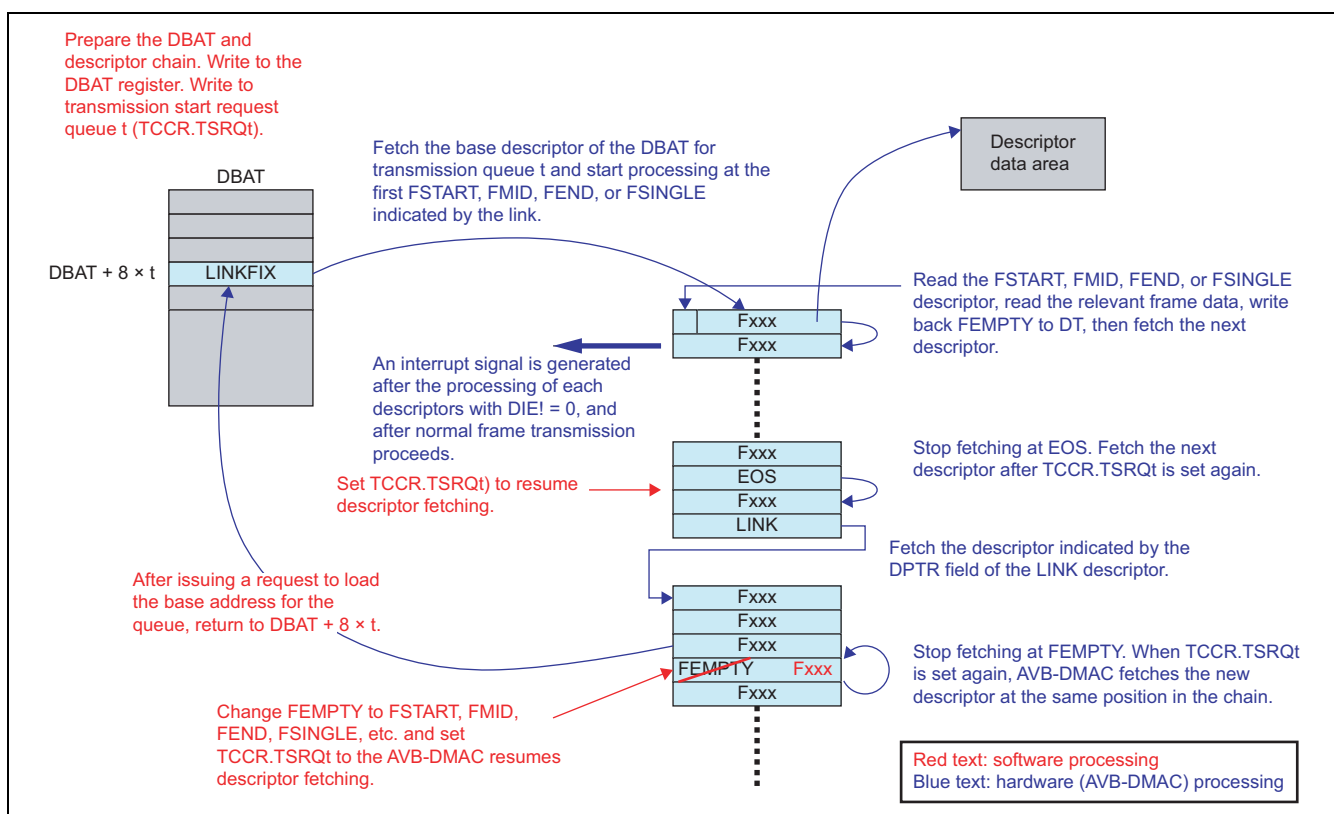


Figure 37A.30 Descriptor Processing During Transmission

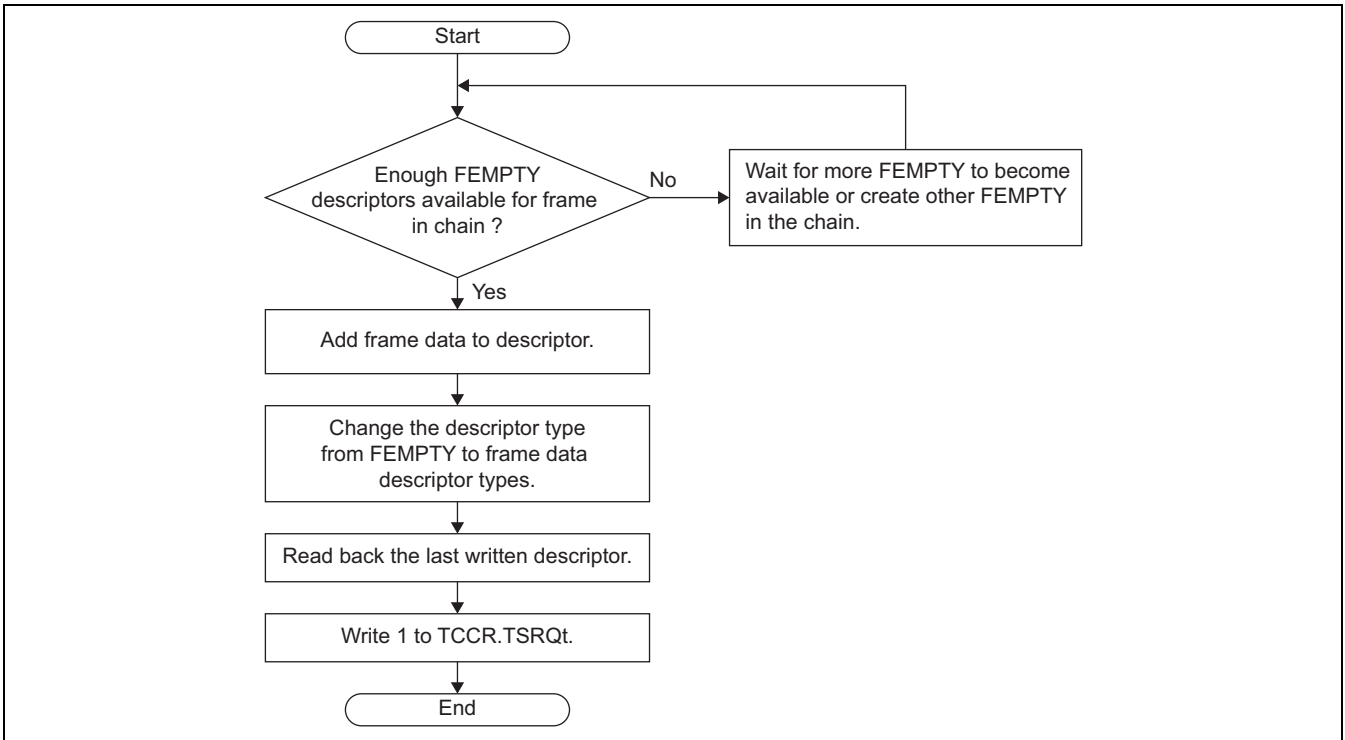
**(2) Examples of Descriptor Usage**

**(a) Immediate Frame Transmission**

Immediate frame transmission is a pattern in which fetching by the AVB-DMAC starts whenever software adds data to a queue. FEMPTY descriptors are used as stop points to keep the hardware and software in synchronization.

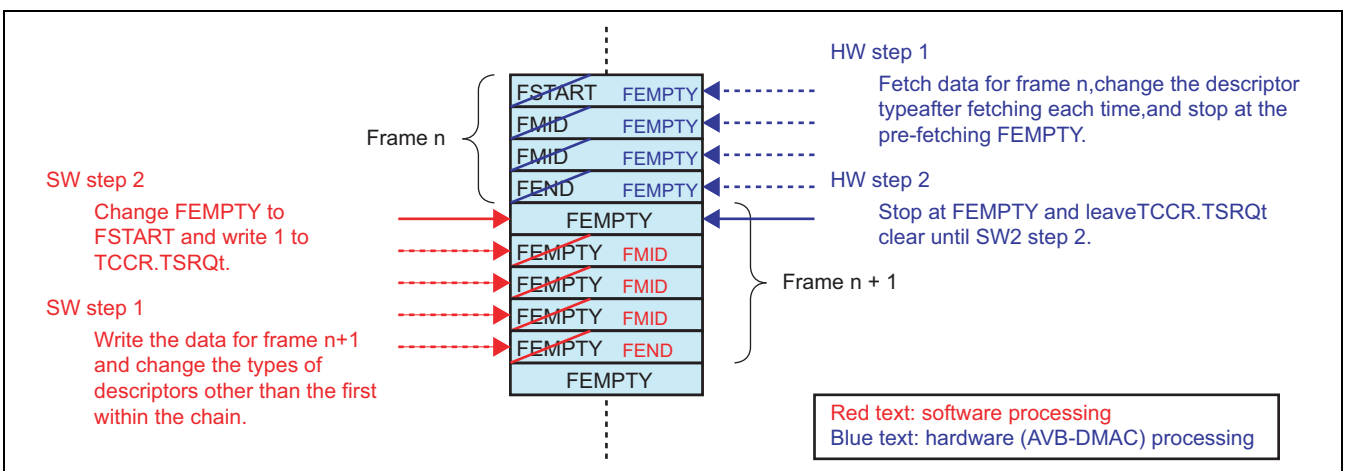
Create descriptor chains that have FEMPTY descriptors at the stop points.

Figure 37A.31 shows the flow for software implementing this pattern. SW should read back written descriptor between changing FEMPTY descriptor before writing to TCCR.TSRQt.



**Figure 37A.31 Software Flow for Immediate Frame Transmission**

Figure 37A.32 shows software and AVB-DMAC operations for immediate frame transmission.



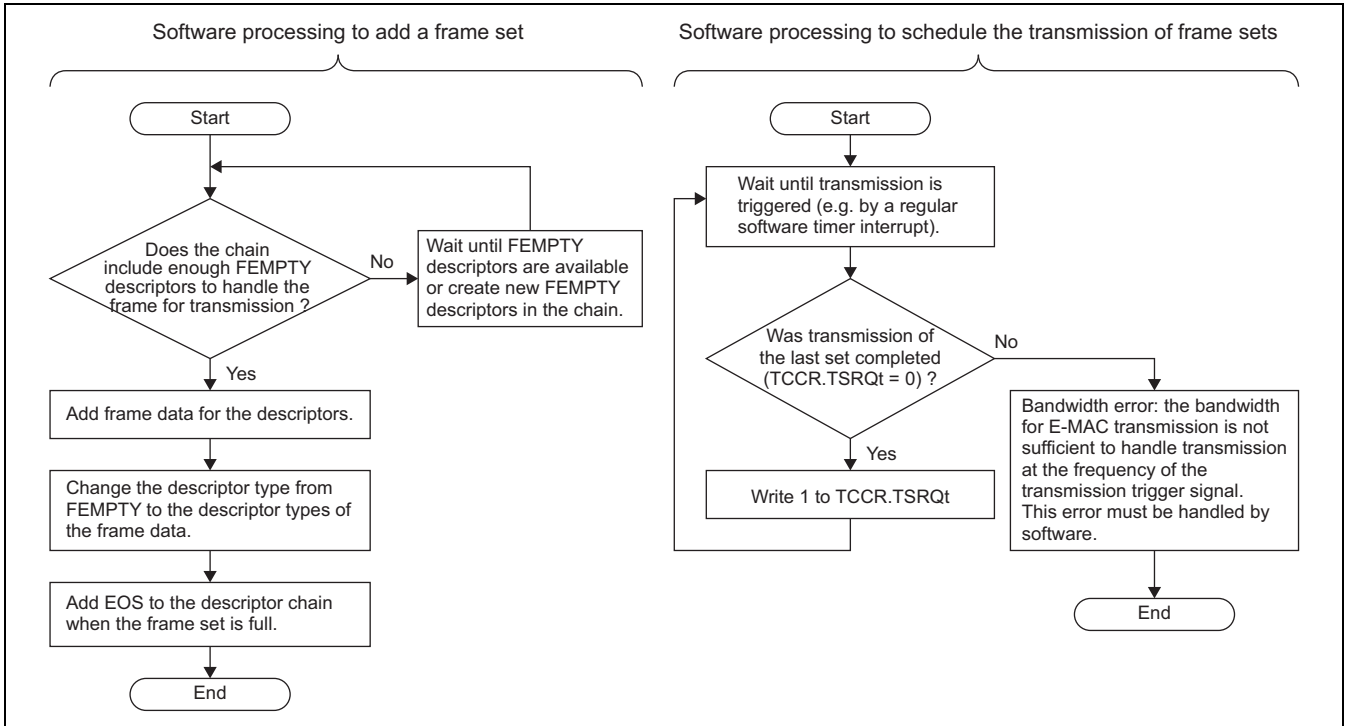
**Figure 37A.32 Software and AVB-DMAC Operations for Immediate Frame Transmission**



**(b) Frame Set Transmission with Changing of the Active Descriptor Chain**

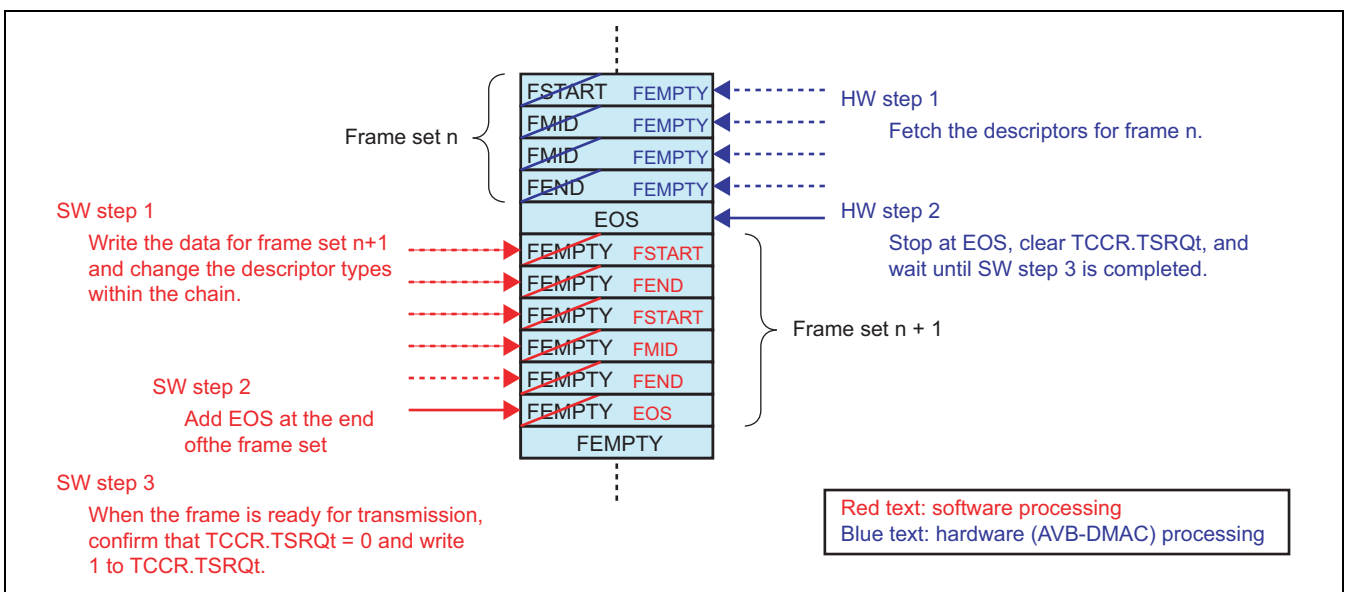
This pattern is used when data are transmitted with a delay for software control to secure bandwidth or for other reasons, rather than immediately transmitted. EOS descriptors are used for the stop points. Start by creating a descriptor chain that has a FEMPTY descriptor as its stop point.

Figure 37A.33 shows the software flow in this pattern.



**Figure 37A.33 Software Flow for Frame Set Transmission with Changing of the Active Descriptor Chain**

Figure 37A.34 shows software and AVB-DMAC operations for frame set transmission.



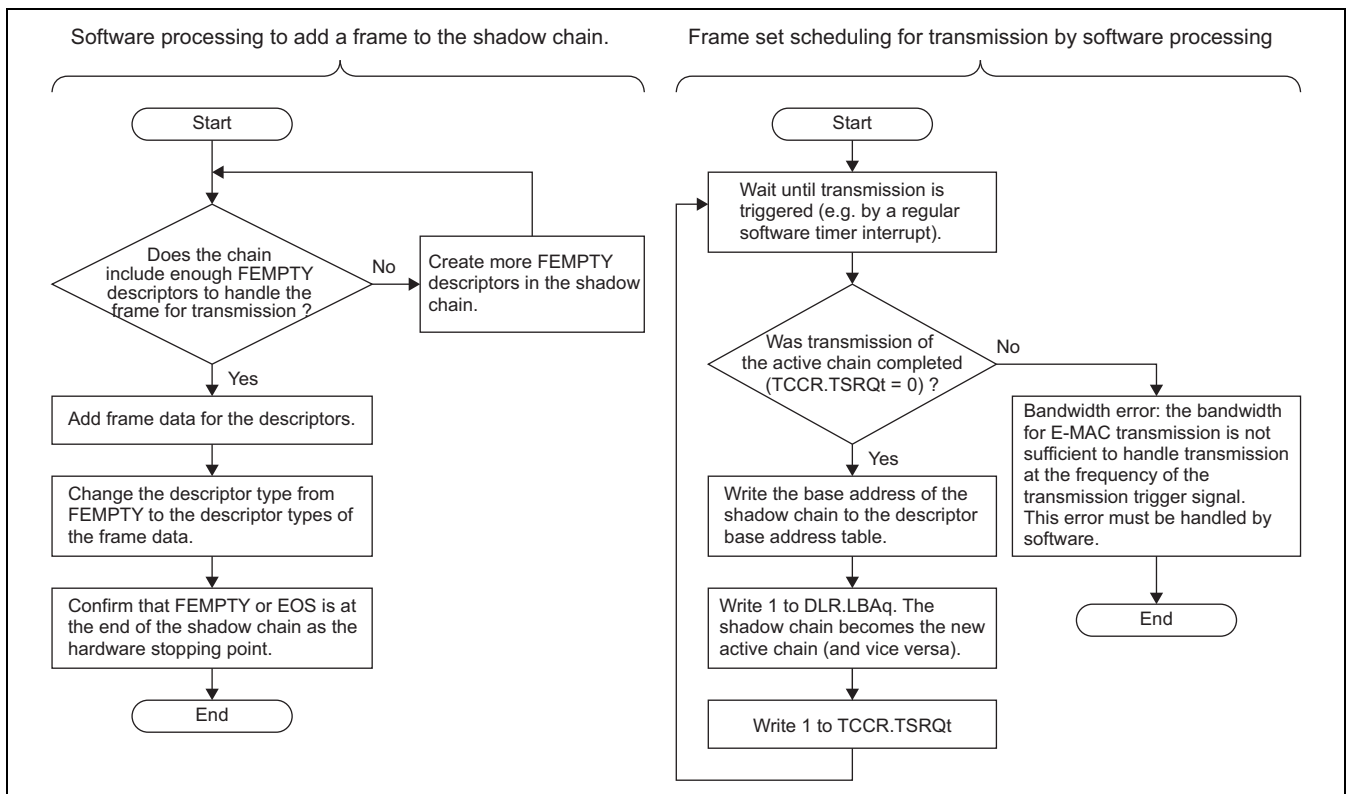
**Figure 37A.34 SW and AVB-DMAC Operations for Frame Set Transmission with Changing of the Active Descriptor Chain**

**(c) Frame Set Transmission Using a Shadow Descriptor Chain**

This pattern is used when data are transmitted with a delay for software control to secure bandwidth or for other reasons, rather than immediately transmitted. Two or more descriptor chains are used. The chains are classified as active or shadow chains. EOS descriptors are used for the stop points.

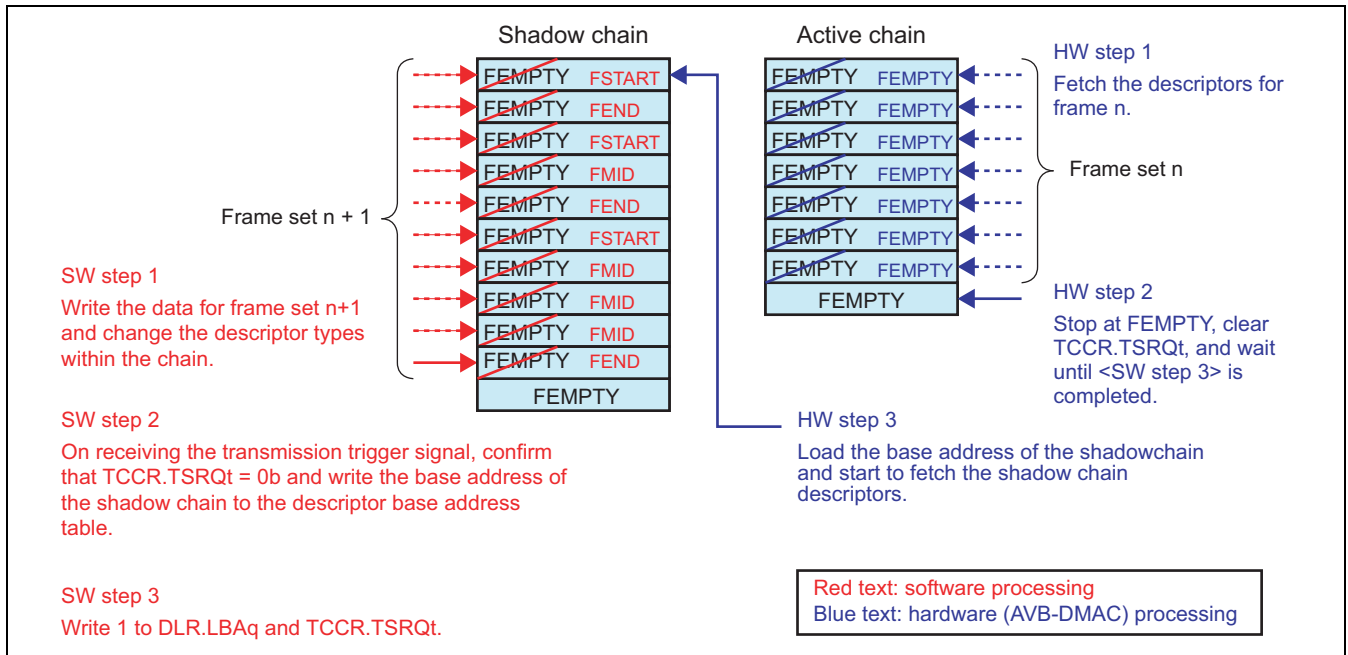
Create descriptor chains that have FEMPTY descriptors at the stop points.

Figure 37A.35 shows the flow for software implementing this pattern.



**Figure 37A.35 Software Flow for Frame Set Transmission Using the Shadow Descriptor Chain**

Figure 37A.36 shows software and AVB-DMAC operations for frame set transmission.



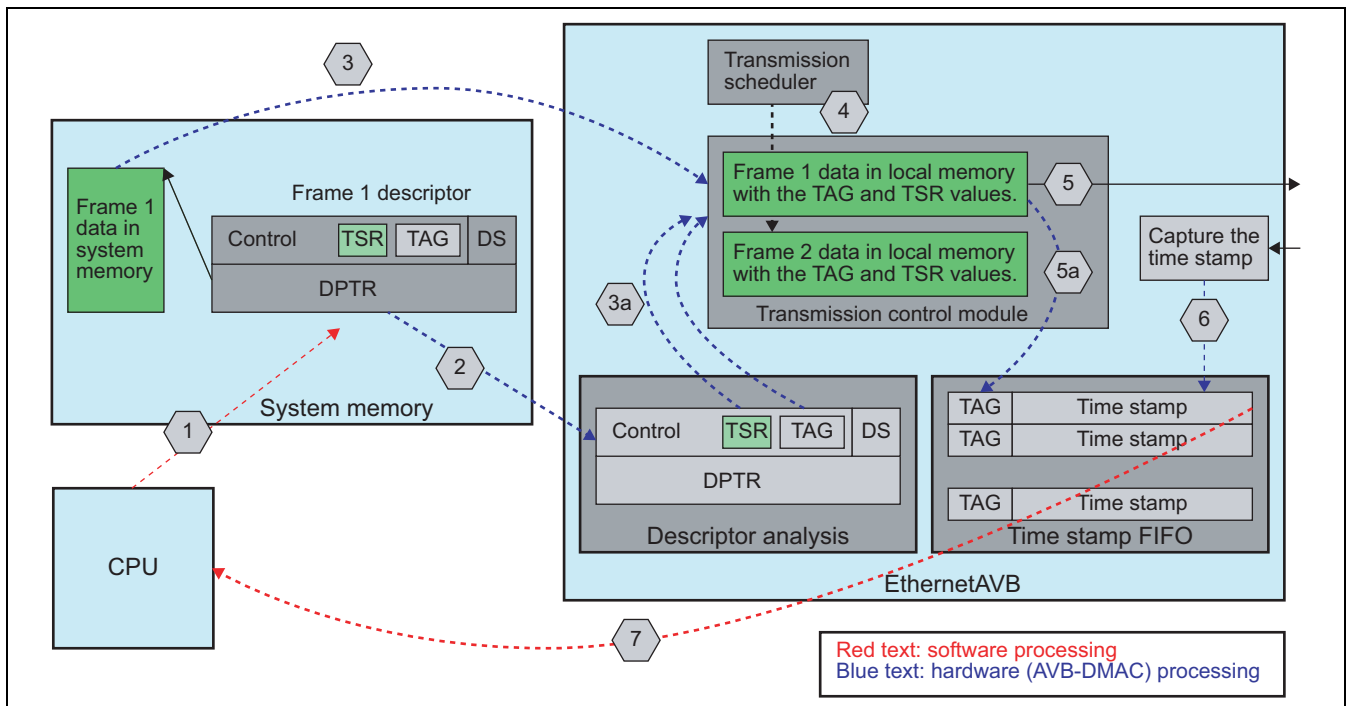
**Figure 37A.36 SW and AVB-DMAC Operations for Frame Set Transmission Using the Shadow Descriptor Chain**

### 37A.3.5.4 Time Stamping in Transmission

Transmission time stamps are important in satisfying the requirements for timing and synchronization of the IEEE 802.1AS standard. Reference to this information can also be useful to other applications and in testing. The AVB-DMAC supports the storage of time stamps for transmitted frames. The time-stamp values are based on the gPTP timer and are captured at the same time as sending of the Start of Frame Delimiter (SFD) for transmitted frames.

When the time stamp storage request field (DESCR.TSR) is set to 1, selecting storage of a time stamp, the tag number defined in the tag field (DESCR.TAG) of the last descriptor (FEND or FSINGLE) for the frame being transmitted is stored with the time stamp. This eases identification and association. The time-stamp FIFO is accessible at any time.

Figure 37A.37 shows the mechanism supporting transmission time stamping.



**Figure 37A.37 Mechanism to Support Transmission Time Stamps**

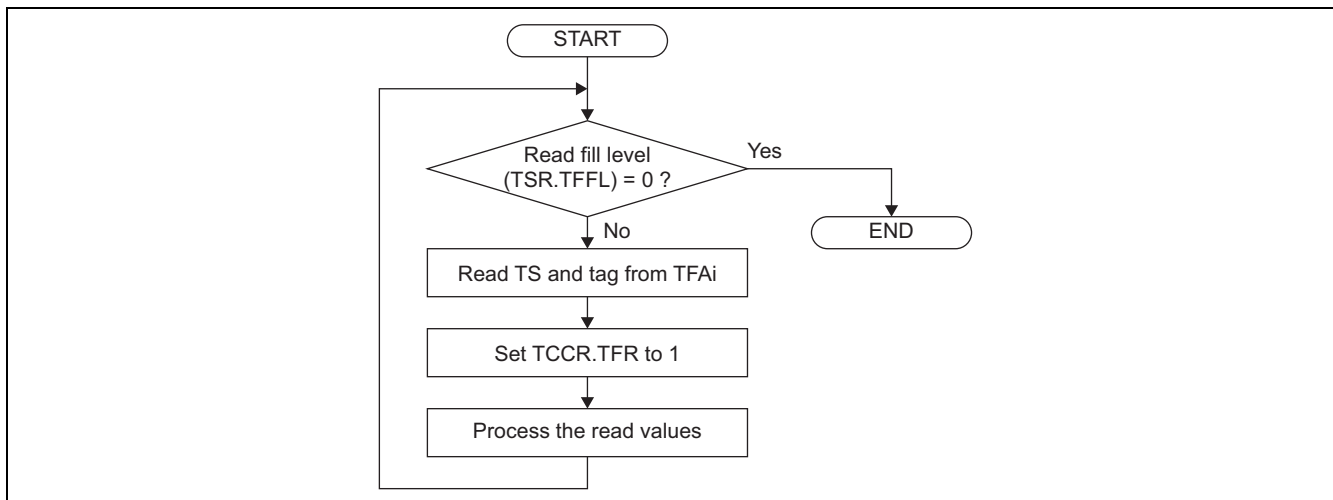
The method of using this function is described below:

- Secure space in the URAM for the frame requiring time stamping.  
Write the tag number of the frame to the frame tag field (DESCR.TAG) and set the time stamp storage request field (DESCR.TSR) to 1.
- The AVB-DMAC fetches and analyzes the descriptor. The time stamp storage request field (DESCR.TSR) is 1, so it recognizes that transmitting this frame also requires storage of the time stamp.
- The AVB-DMAC fetches the data for frame 1 and temporarily stores the frame in internal memory for scheduling.  
3a: The frame tag field (DESCR.TAG) and time stamp storage request field (DESCR.TSR) are stored with the fetched data.)
- Under the control of priority settings according to credit-based shaping (CBS) or another scheme, the transmission scheduler decides it is time to transmit frame 1.
- Transmission of frame 1 starts.  
5a: Frame 1's tag is stored in the time-stamp FIFO.
- The gPTP time stamp is captured at the start of frame delimiter (SFD) for transmission and stored with the tag in the time-stamp FIFO when the frame is completely transmitted. An interrupt is generated to indicate existence of new timestamp information. For this to happen, the descriptor interrupt control register (DIC) must be set beforehand.

7. The entry can now be read from the time-stamp FIFO.

Use the time-stamp FIFO for the timing and synchronization of frames with IEEE 802.1AS compliance.

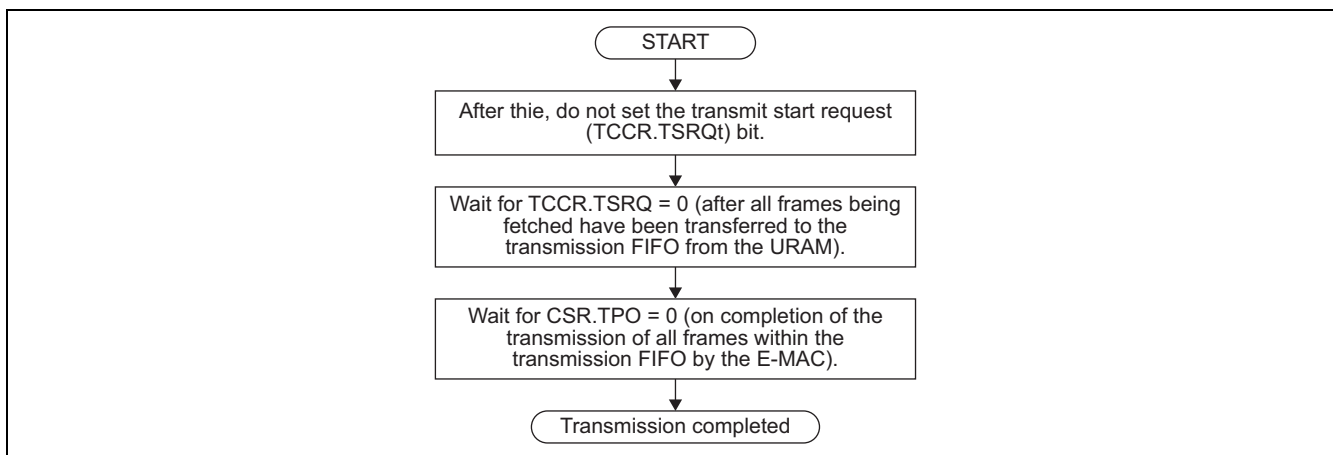
Time stamping can also be used with other frames, but take care not to allow the time-stamp FIFO to overflow. When the FIFO is full, further time stamps supplied to it are lost.



**Figure 37A.38 Flow of Transmission Time Stamping**

### 37A.3.5.5 Ending Transmission

Figure 37A.39 shows the procedure for ending transmission.



**Figure 37A.39 Procedures for Ending Transmission**

### 37A.3.6 CBS (Credit-Based Shaping)

In AVB transmission mode (i.e. when the transmit queue priority field in the transmit configuration register (TGC.TQP) is B'01 or B'11), transmission queues Q3 and Q2 are respectively assigned to class A and class B stream traffic and the CBS (Credit Based Shaping) algorithm is used to select the transmission queues in order to satisfy the Forwarding and Queuing for Time Sensitive Streams (FQTSS) specification (see section 8.6.8 or section 34 in IEEE 802.1Q).

The CBS algorithm is based on the concept of transmission credit for each queue. Credit can be thought of as the degree to which a queue has the “right” to transmit at a given time. Actually, in AVB transmission mode as specified in IEEE 802.1Q, queues that are subject to the CBS algorithm are able to transmit when the following conditions are met.

At least one frame is stored in the queue.

The credit for the queue is 0 or a positive value.

The credit for a transmission queue is incremented while one or more frames from the queue are present in the transmission FIFO but transmission of these frames is not proceeding. This state is indicated by the transmission process status bit for queue t in the AVB-DMAC status register (CSR.TPOt). The credit is decremented while transmission of a frame from the queue is in progress. This mechanism is used to control transmission so that the transmission of frames from the queues for each of the traffic classes does not exceed the specified maximum bandwidths.

IEEE 802.1Q defines the following parameters for queues under the control of the CBS algorithm.

**portTransmitRate:** Maximum transmission data rate of an external port. The E-MAC determines this parameter.

**bandwidthFraction:** Maximum fraction of portTransmitRate that can be used for a queue.

**idleSlope:** Rate of change of credit for a queue when transmission of frames from the queue is not proceeding so the credit value (in bits per second) is increasing. idleSlope is also equal to the maximum fraction of the total bandwidth (portTransmitRate) that is available to the given queue under a specified condition (frames from the queue can be placed in a continuous stream. See Annex L of IEEE 802.Q.  

$$\text{idleSlope} = \text{bandwidthFraction} \times \text{portTransmitRate}$$

**sendSlope:** Rate of change of credit for a queue while transmission of a frame from the queue is in progress so the credit value is decreasing.  
 The value of sendSlope is defined as follows:  

$$\text{sendSlope} = \text{idleSlope} - \text{portTransmitRate}$$

Furthermore, the values below are used to define individual traffic classes (or queues for the classes) under control of the algorithm. See Annex L of IEEE 802.Q.

**maxFrameSize:** Maximum size of frames (in bits) of the corresponding traffic class that can be transmitted from a port

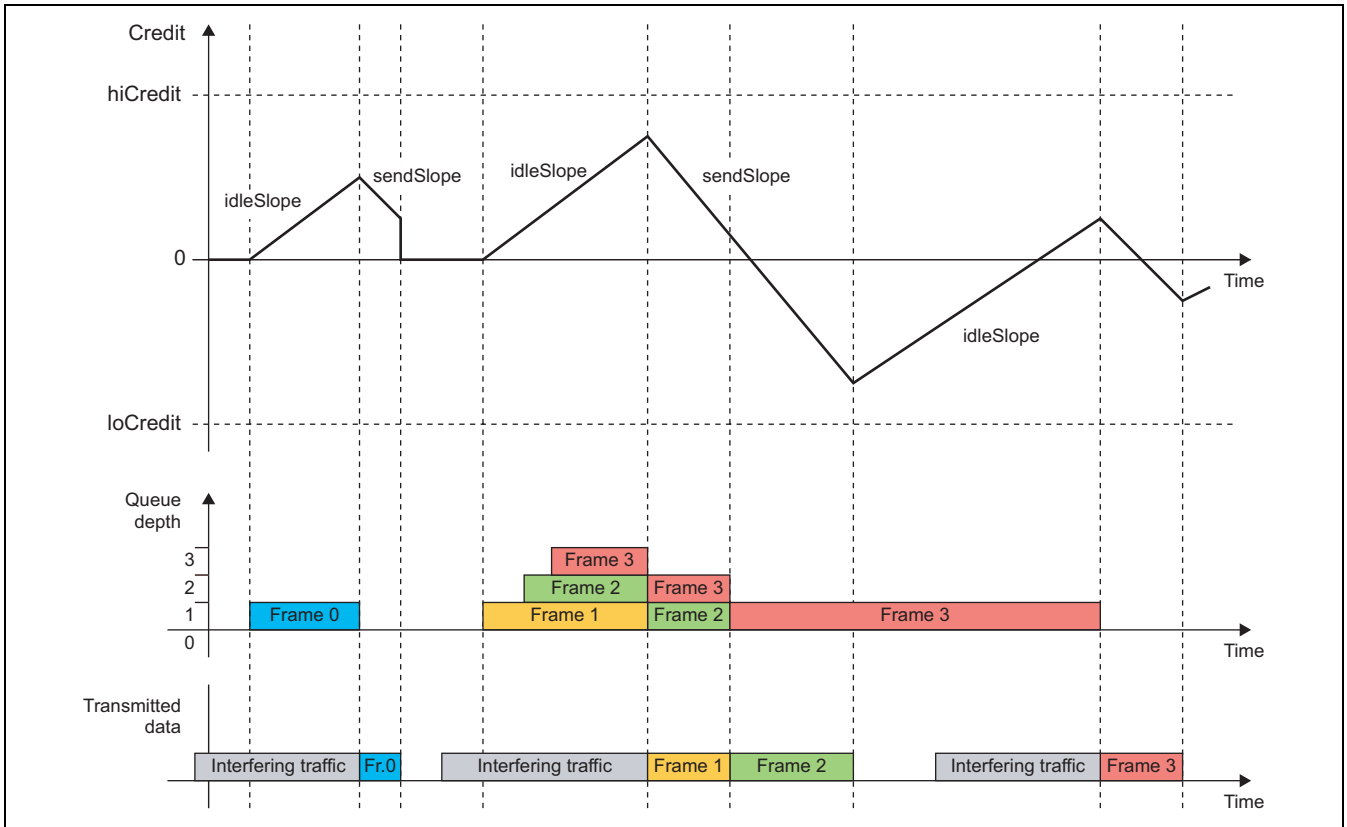
**maxInterferenceSize:** Maximum burst size (in bits) by which delays for the corresponding traffic class can be allowed

**hiCredit:** Maximum credit value (positive number). Can be calculated by using the following equation:  $\text{hiCredit} = \text{maxInterferenceSize} \times (\text{idleSlope} / \text{portTransmitRate})$

**loCredit:** Minimum credit value (negative number). Can be calculated by using the following equation:  

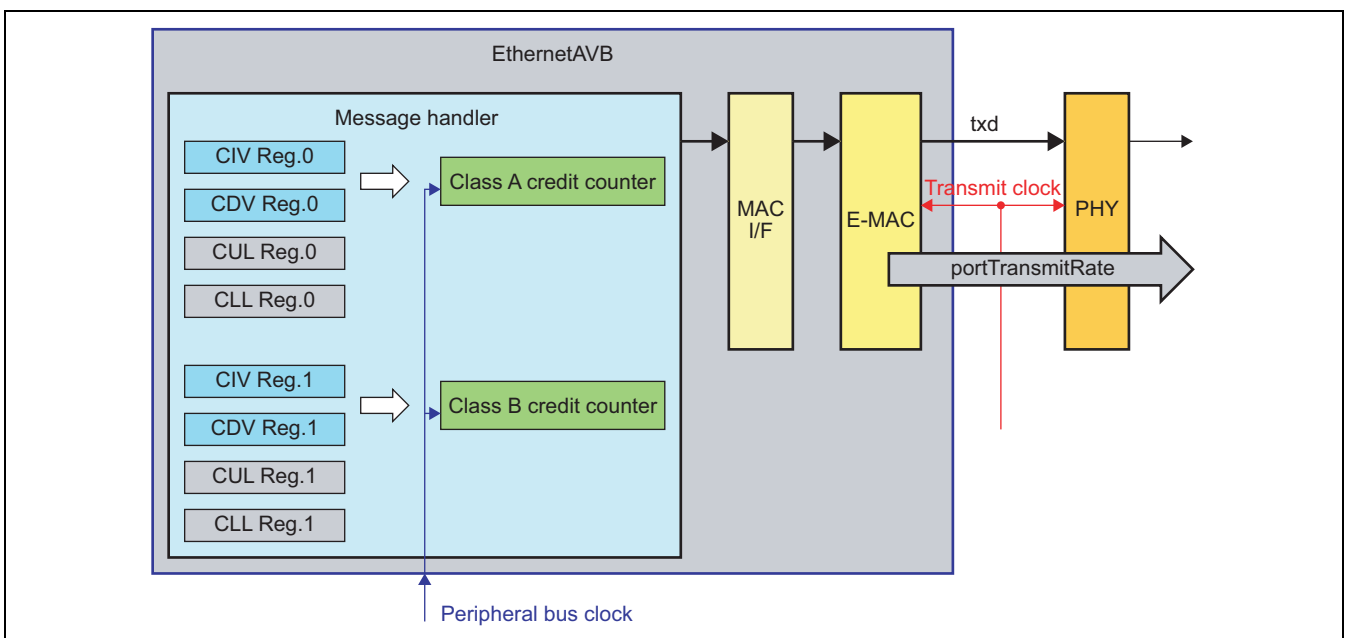
$$\text{loCredit} = \text{maxFrameSize} \times (\text{sendSlope} / \text{portTransmitRate})$$

Figure 37A.40 shows how the CBS algorithm works and the meaning of the above parameters.



**Figure 37A.40 CBS (Credit-Based Shaping) Operation**

Figure 37A.41 shows the implementation of CBS in the AVB-DMAC.



**Figure 37A.41 CBS (Credit-Based Shaping) Operation in the AVB-DMAC**

The above implementation is based on “credit counters” for the respective traffic classes (SR class A and class B). The following parameters apply for these classes.

CBS increment value (CIV): Signed positive number

The credit is incremented by this amount every high-speed peripheral bus clock cycle while a frame from the queue is pending but transmission has not started (idleSlope).

CBS decrement value (CDV): Signed negative number

The credit is decremented by this amount every high-speed peripheral bus clock cycle while transmission of a frame from the queue is proceeding (sendSlope).

The CBS increment value (CIV) and CBS decrement value (CDV) are defined as follows.

$$\text{CIV} = \text{idleSlope} \times \text{Mfactor}$$

$$\text{CDV} = \text{sendSlope} \times \text{Mfactor}$$

Mfactor is a multiplier factor to ensure accuracy for CIV and CDV. CIV and CDV are calculated by using the following equations.

$$\text{CIV} = (\text{portTransmitRate}/\text{HP}\phi) \times \text{bwFraction} \times \text{Mfactor}$$

$$\text{CDV} = (\text{portTransmitRate}/\text{HP}\phi) \times (\text{bwFraction} - 1) \times \text{Mfactor}$$

HP $\phi$  is the frequency of the high-speed peripheral bus clock. The credit counters are driven by the high-speed peripheral bus clock, so calculating the slope parameters for CBS requires (1/HP $\phi$ ).

Use software to prepare Mfactor for the CBS parameters. All queues for the same class must have the same Mfactor for all CBS parameters. Mfactor for a specified class c can be changed during operation, unless transmission is pending for that class (i.e. the transmit process status bit in the AVB-DMAC status register (CSR.TPOt) = 0). At that time, the credit counter values for class A and class B are 0. Note that the credit value will not match a new incrementation or decrementation parameter if Mfactor is changed while the credit counter value is non-zero. Mfactor is not present in the AVB-DMAC registers.

Set the CIV and CDV parameters in the CBS increment value registers (CIVRc) and the CBS decrement value registers (CDVRc). These are treated as dynamic settings since they should be updated when streams are registered and erased in accord with IEEE 802.1Qat.

The AVB-DMAC also has CBS upper limit registers (CULc) (the upper limit registers for classes A and B) and CBS lower limit registers (CLLc) (the lower limit registers for classes A and B). Set Mfactor to match the credit value and set the upper limit (hiCredit) and the lower limit (loCredit) for each class as defined above.

$$\text{CUL} = \text{hiCredit} \times \text{Mfactor} = \text{maxInterferenceSize} \times \text{bwFraction} \times \text{Mfactor}$$

$$\text{CLL} = \text{loCredit} \times \text{Mfactor} = \text{maxFrameSize} \times (\text{bwFraction} - 1) \times \text{Mfactor}$$

### Example:

Assume that portTransmitRate = 100 Mbps, HP $\phi$  = 130 MHz and bwFraction = 3%. Then idleSlope and sendSlope represented as one bit vs. cycles of the high-speed peripheral bus clock are as follows.

$$\text{idleSlope} = (\text{portTransmitRate}/\text{HP}\phi) \times \text{bwFraction} = 100/130 \text{ (Mbps/MHz)} \times 3\% = 0.023 \text{ bit per high-speed peripheral bus clock cycle}$$

$$\text{sendSlope} = \text{idleSlope} - (\text{portTransmitRate} / \text{HP}\phi) = -0.746 \text{ bits per high-speed peripheral bus clock cycle}$$

Let Mfactor be 100, then CIV and CDV parameters are determined as follows.

$$\text{CIV} = \text{idleSlope} \times \text{Mfactor} = 2.3$$

$$\text{CDV} = \text{sendSlope} \times \text{Mfactor} = -74.6$$



### 37A.3.6.1 Restrictions on CIV, CDV and Mfactor

The maximum value (the minimum value for negative numbers) up to which the credit counter will not overflow determines the maximum values of CIV and CDV that can be set in the CBS registers. This maximum credit value is equivalent to the worst case of the hiCredit value, and the maximum values for class A and class B are calculated as follows.

#### <Conditions>

- Class A maximum value (hiCredit\_max\_classA)

classA bwFraction  $\cong$  100%

Maintaining the proper relations in the transmission priority order requires waiting for a period equivalent to the maximum frame size.

hiCredit\_max\_classA  $\cong$  maxInterferenceSize for class A = Interference due to one max. sized frame = header + max. size payload + CRC (2000 bytes) + preamble (8 bytes) + IFG (12 bytes) + processing\_delay ( $\cong$  80 bytes)  $\cong$  2100 bytes

- Class B maximum value (hiCredit\_max\_classB)

classB bwFraction  $\cong$  100%

Maintaining the proper relations in the transmission priority order requires waiting for a period equivalent to the maximum size of frames in the class A transmission queue and other transmission queues.

hiCredit\_max\_classB  $\cong$  maxInterferenceSize for class B = Interference due to two max-size frames =  $2 \times$  hiCredit\_max\_classA  $\cong$  4200 bytes

hiCredit\_max\_classA = 16800

hiCredit\_max\_classB = 33600

The maximum values that can be selected with Mfactor for the 32-bit signed counter without overflow are:

Mfactor\_max\_classA =  $2^{31}-1$  / hiCredit\_max\_classA  $\cong$  127826 and

Mfactor\_max\_classB =  $2^{31}-1$  / hiCredit\_max\_classB  $\cong$  63913.

A high degree of accuracy can be achieved even with a low bandwidth. In class B, bandwidthFraction = 0.05% and the bandwidth error < 0.1%.

The maximum value of CIV is calculated from the following equation.

CIV = idleSlope x Mfactor = (portTransmitRate / HP $\phi$ )  $\times$  bandwidthFraction  $\times$  Mfactor

When Mfactor is the maximum value and bandwidthFraction is the maximum value (up to 100%):

CIV\_max\_classA = (portTransmitRate / HP $\phi$ )  $\times$  Mfactor\_max\_classA and

CIV\_max\_classB = (portTransmitRate / HP $\phi$ )  $\times$  Mfactor\_max\_classB.

The maximum values when portTransmitRate = 1000 Mbps and HP $\phi$  = 130 MHz are as follows:

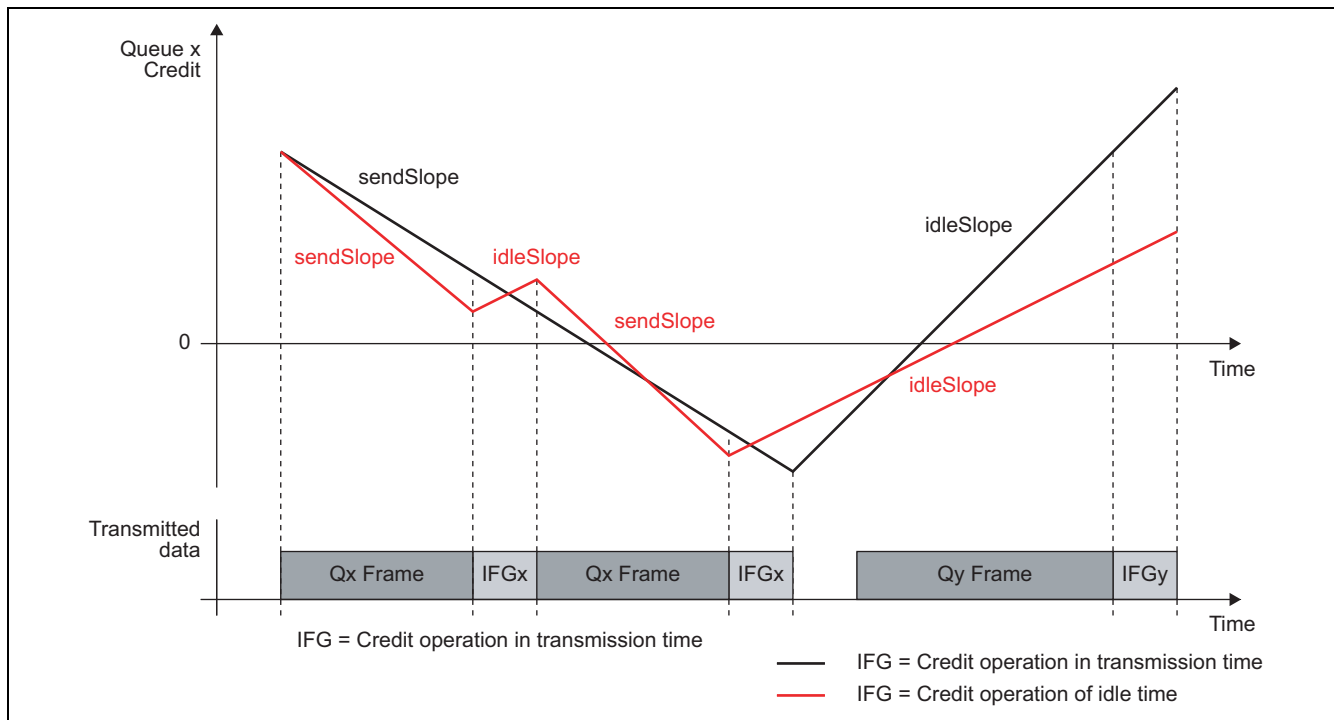
CIV\_max\_classA  $\cong$  983277

CIV\_max\_classB  $\cong$  491638

These values in the table are the limits of CIV up to which the 32-bit credit counter will not overflow. The CIV parameters are implemented as 16 bits + a sign bit, so a further limit of CIV  $\leq$  65535 applies to both class A and class B.

### 37A.3.6.2 Credit Incrementation during Inter-Frame Gaps (IFGs)

The inter-frame gap (IFG) after a frame is transmitted is not treated as part of frame transmission by the CBS credit counter. During an IFG, the credit is incremented for all SR queues that have pending frames or negative credit. Figure 37A.42 illustrates credit operations during IFGs.



**Figure 37A.42 Credit Operations during IFGs**

Accordingly, the IFG need not be included in calculation of the bandwidth requirements for the specified SR class when deciding the idleSlope, sendSlope, and CIV and CDV parameters. However, IFG must also be included in the calculation in order to confirm that the total bandwidth allocated to all SR classes does not exceed 100% of portTransmitRate. This is described in Section 35.2.2.8.4 of IEEE 802.1Q.

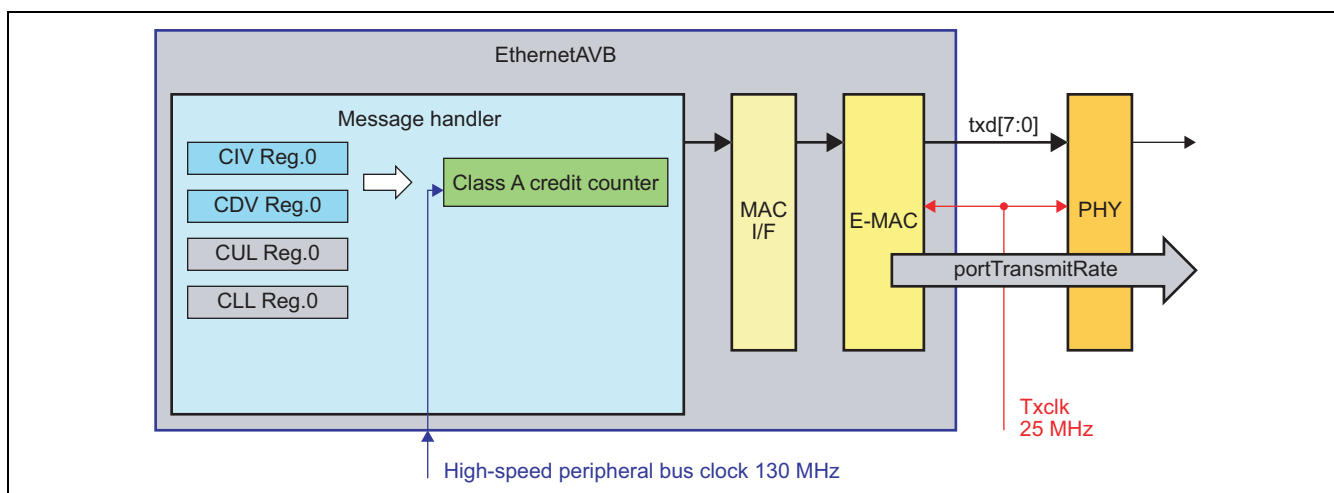
### 37A.3.6.3 Example

The case of a class A 48-kHz stereo audio stream among Ethernet frames is described as an example.

After every class A measurement interval (125  $\mu$ s), 80 octets consisting of two sets of six 32-bit samples plus a 32-octet header are stored as audio data within a frame. The IEEE 802.3 also imposes a 42-octet media-specific framing overhead (an 8-octet preamble, 14-octet IEEE 802.3 header, 4-octet IEEE 802.1Q priority/VID Tag, 4-octet CRC, and 12-octet IFG) are also added. Accordingly, the total frame size is  $80 + 42 = 122$ , and one such frame is transmitted after every class measurement interval.

This represents a total bandwidth of about 7.8 Mbits per second (122 octets  $\times$  8 bits per octet  $\times$  8000 frames per second) for this class. If the E-MAC is assumed to run at 1 Gbps (portTransmitRate), this is equivalent to the allocation of about 0.78% of the total bandwidth to each class A queue. If other traffic classes are to share the total transmission bandwidth, checking that this 0.78% allocation does not lead to the total allocation of bandwidth being greater than 100% of portTransmitRate is required.

To obtain the CIV and CDV parameters for a given class, the IFG must not be taken into account in calculation of the frame size must not include the IFG. For this case, therefore, we obtain an 80-bit payload + 30-bit overhead = 110-octet measurement interval for the class  $\rightarrow$  the total bandwidth for the class = 7.04 Mbps = 0.704% of portTransmitRate.



**Figure 37A.43 Example of CBS Settings**

Given that:

- the E-MAC runs at 100 Mbps, so portTransmitRate = 100 Mbps and
- high-speed peripheral bus clock (operating clock for the credit counter) frequency = 130 MHz, securing a bandwidth of 7.04 Mbits/sec for class A requires configuring the CBS parameters as follows.

$$\text{bandwidthFraction} = 0.704\%$$

$$\text{idleSlope} = (\text{portTransmitRate} / \text{HP}\phi) \times \text{bandwidthFraction} \cong 0.0176 \text{ bits per high-speed peripheral bus clock cycle}$$

$$\text{sendSlope} = \text{idleSlope} - (\text{portTransmitRate} / \text{HP}\phi) \cong -2.4824 \text{ bits per high-speed peripheral bus clock cycle}$$

When Mfactor = 100000, the parameters are as follows.

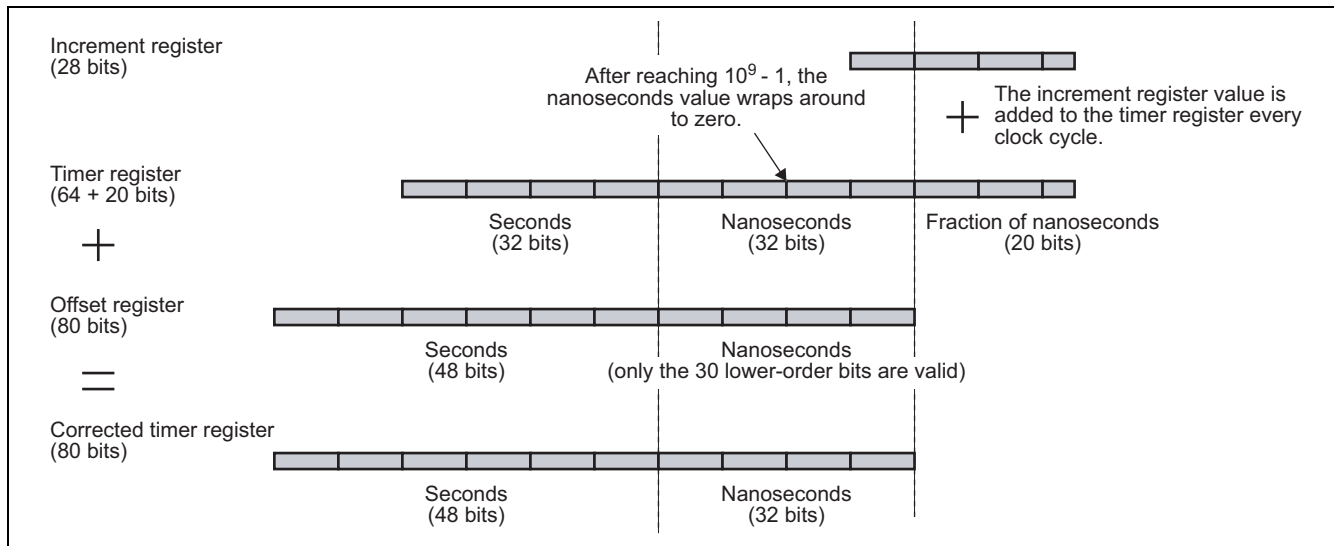
- CIV = idleSlope  $\times$  Mfactor = 1760 bits per high-speed peripheral bus clock cycle
- CDV = sendSlope  $\times$  Mfactor = 248240 bits per high-speed peripheral bus clock cycle

These are the final values for setting in the CIVR1 and CDVR1 registers.

### 37A.3.7 Time Synchronization

#### 37A.3.7.1 gPTP Timer

An 84-bit timer is provided to support the gPTP function. Figure 37A.44 shows the definitions of bits for the timer and in related registers.



**Figure 37A.44 Definitions of gPTP Timer Bits and Related Bits**

The higher-order 32 bits indicate seconds. For the next 32 bits, counting by one corresponds to the passage of 1 ns. The lower-order 20 bits are a fractional value (less than 1 ns). Software can only read the 32 higher-order bits, indicating seconds, and the subsequent 32-bits, indicating nanoseconds. The 20 lower-order 20 bits, representing less than 1 ns, are not readable. They are only used within the AVB-DMAC to maintain accuracy in time measurement.

The timer can be reset by setting the timer control request bits in the gPTP configuration control register (GCCR.TCR[1:0]) to B'01. These bits are set to B'00 on completion of normal resetting of the timer.

After the timer starts, the value in the gPTP timer increment register (GTI.TIV) is added to the value of the gPTP timer every clock cycle.

Before setting a value in the gPTP timer increment register (GTI.TIV), set the timer increment value setting request bit in the gPTP configuration control register (GCCR.LTI). If this bit is not set to 1, new values that are written will not be reflected in the register. This bit returns to 0 after the setting is completed.

An offset to the gPTP timer is also available. If this is required, set the value in the gPTP timer offset register (GTO.TOV). Before setting a value in this register, set the timer offset value setting request bit in the gPTP configuration control register (GCCR.LTO). If this bit is not set to 1, new values that are written will not be reflected in the register. This bit returns to 0 after the setting is completed. When adding an offset, take care that it does not exceed 80 bits.

The value of the gPTP timer can be read from the gPTP timer capture register (GCTi.CTV). Set the timer capture source select bits in the gPTP configuration control register (TCCR.TCSS) to select the timer value for capture as the value of the gPTP timer, the corrected value of the gPTP timer (value with the offset added), or the AVTP presentation time. Setting the timer control request bits in the gPTP configuration control register (GCCR.TCR[1:0]) to B'11 initiates the capture. Once normal capture of the timer is complete, the value of the timer control request bits in the gPTP configuration control register (GCCR.TCR[1:0]) returns to B'00.

The timer for gPTP operates as a free-running timer but can be synchronized with the Grandmaster clock.

### 37A.3.7.2 Free-Running Operation

The IEEE 802.1 AS standard for timing and synchronization does not prescribe the physical adjustment of local clocks to the Grandmaster clock. To avoid negative effects from the correction procedure, we recommend the use of a free-running timer.

As a free-running timer, the timer counts the local time in seconds or nanoseconds. The gPTP timer increment register (GTI.TIV) is set to 1 ns (the setting value = H'0010 0000) and the gPTP timer offset register (GTOi.TOV) is set to 0. The ratio information captured at the time of the gPTP delay measurement and synchronization procedures is used to correct the frequency ratio to that of the Grandmaster clock. The Grandmaster clock can be calculated from the local clock by using the information collected during the gPTP measurement and synchronization procedures.

### 37A.3.7.3 Synchronization with the Grandmaster Clock

In situations requiring physical synchronization of the local clock with the Grandmaster clock, the fractional nanoseconds value (the 20 lower-order bits of the gPTP timer) is used to make the adjustment. Specifically, the increment value is finely adjusted to correct for deviations of the clock frequency from that of the Grandmaster clock.

Use the timer offset value (in the gPTP timer offset registers, GTOi.TOV) to correct for offsets from the theoretical value (at start-up, etc.). The sum of the timer value and the offset register is the “corrected timer” value.

Note that for the nanoseconds part of the Offset register GTOi.TOV[31:0] should be below  $10^9$ .

The following equation gives a method of calculating the increment (GTI.TIV) from the frequency of the gPTP clock and its deviation from that of the Grandmaster clock. Variable  $d$  is the deviation ( $d = 10^{-6}$  for 1 ppm).

$$GTI.TIV = round\left(\frac{2^{20} \text{ GHz}}{f_{GPTP}} \times (1 + d)\right)$$

After adjusting for the current deviation of clock frequency, reset the gPTP timer increment register (GTI.TIV).

After calculating the new offset value, reset the gPTP timer offset register (GTOi.TOV).

### 37A.3.7.4 Support Provided by the gPTP Timer in Transmission and Reception

The timer value described above is used in the time-stamp values captured when start frame delimiters are detected in reception and generated in transmission at PHY interface.

Captured time stamp values for received frames are stored in the corresponding descriptors. Those for transmitted frames are stored with tag information in the time-stamp FIFO. The time stamp values are thus correlated with both transmitted and received frames.

Note that the use of corrected timer values can introduce an error due to the offset correction in the gPTP synchronization procedure.

Due to asynchronous interface between the SFD notification and the timer modules, errors must also be taken into account.

### 37A.3.8 Support for IEEE 1722

For IEEE 1722, the following two functions are supported.

- Output and capture of values in the IEEE 1722 AVTP (Audio/Video Transport Protocol) presentation time format
- Comparison of IEEE 1722 AVTP presentation time stamps

The 32-bit AVTP time stamp field of IEEE 1722 frames holds the AVTP presentation time when the AVTP time-stamp enable bit in the frame is 1. The AVTP time stamp field is generated from the gPTP timer and is given as seconds (gPTP\_seconds) and nanoseconds (gPTP\_nanoseconds) according to the following equation.

$$\text{AVTP time stamp} = (\text{gPTP\_seconds} \times 10^9 + \text{gPTP\_nanoseconds}) \text{ modulo } 2^{32}$$

The AVTP presentation time can be read from the gPTP timer capture register (GCTi.CTV). Set the timer capture source select bits in the gPTP configuration control register (GCCR.TCSS) to select the timer value for capture as the AVTP presentation time. Setting the timer control request bits in the gPTP configuration control register (GCCR.TCR[1:0]) to B'11 initiates the capture. The value is obtained by adding the maximum transit time defined in the gPTP maximum transit time register (GMTT.MTTV) to the corrected timer value. The AVTP presentation time wraps around approximately every four seconds.

Note: The AVTP presentation time captured in GCTi.CTV is only valid when the corrected timer value is in synchronization with the Grandmaster clock. That is, the timer increment and timer offset values for the corrected timer value must be adjusted during the synchronization procedure so that the corrected gPTP clock is physically adjusted to match the time kept by the Grandmaster clock.

### 37A.3.9 Flow Control

The EthernetAVB does not support flow control in the specification. Flow control is only effective when transmitting and receiving only normal (non-AVB) packets.

The E-MAC supports flow control for full-duplex operation in compliance with the IEEE 802.3 standards. This flow control is applicable to both reception and transmission. In regard to the transmission of PAUSE frames, flow control operates in the following ways.

#### (1) PAUSE Frame Transmission

PAUSE frames can also be transmitted in response to software operations. Writing a timer value to the manual PAUSE frame register (MPR) starts the transmission of a PAUSE frame. This only causes the transmission of one PAUSE frame.

#### (2) PAUSE Frame Reception

After reception of a PAUSE frame, transmission of the next frame does not proceed until the time indicated by the Timer value elapses. However, transmission of a frame currently being transmitted continues. PAUSE frames are only received while the RXF bit in the E-MAC mode register (ECMR) is set to 1. The number of received PAUSE frames is counted.

#### (3) PAUSE Frames with the Timer Value 0

The setting of the 0-time PAUSE frame enable bit (ECMR.ZPF) enables or disables the reception of PAUSE frames with the TIME parameter value 0.

- When control of PAUSE frames with the TIME parameter value 0 is disabled PAUSE frames with the TIME parameter value 0 are not transmitted. Received PAUSE frames with the TIME parameter value 0 are discarded.

### 37A.3.10 Magic Packet Detection

The E-MAC has a Magic Packet detection function. This function provides a facility for host devices and other sources to start other peripheral devices connected to a LAN. A peripheral device that handles Magic Packets starts itself in response to receiving a Magic Packet.

When a Magic Packet is detected, data from broadcast packets that were previously being received are stored in the FIFO and the E-MAC is notified of the receiving status. To return to normal operation from the associated interrupt processing, the E-MAC and AVB-DMAC must be initialized by using the operating mode configuration bit in the AVB-DMAC mode register (CCC.OPC) to set the operating mode to reset mode.

Magic Packets are received regardless of the destination address. As a result, the AVB\_MAGIC pin is only enabled in the case of a match with the destination address specified in the Magic Packet.

The procedure for using the Magic Packet detection function with this LSI chip is as follows.

1. Use the various interrupt enabling and masking registers to disable the output of interrupts from interrupt sources.
2. Set the Magic Packet detection enable bit in the E-MAC mode register (ECMR.MPDE).
3. Set the Magic Packet detection interrupt enable bit in the E-MAC interrupt enable register (ECSIPR.MPDIP) to enable the interrupt.
4. Place the CPU in sleep mode as required.
5. An interrupt is conveyed to the CPU on detection of a Magic Packet.
6. The AVB\_MAGIC pin notifies connected devices of Magic Packet detection.

Note: The Magic Packet detection interrupt status can be read in the E-MAC status register (ECSR.MPD). The bit can be cleared by setting the E-MAC status register Magic Packet TM detection bit (ECSR.MPD) to 1.

But EthernetAVB can't detect 2nd or later Magic Packet<sup>TM</sup> and the AVB\_MAGIC pin can be negated though the bit is cleared.

The AVB\_MAGIC pin can be negated and EthernetAVB can detect MAGIC Packet<sup>TM</sup> again according to below way.

- |                                   |   |
|-----------------------------------|---|
| 1) Hardware reset                 | set reset pin in the RZ/G series to reset signal.                                     |
| 2) Software reset                 | set mstp/srst register for EthernetAVB to software reset mode.                        |
| 3) Software reset register in AVB | set AVB DMAC mode register Operating Mode Configuration bits (CCC.OPC) to reset mode. |

### 37A.3.11 Interrupts

The EthernetAVB is capable of generating one interrupt.

For details, refer to the “Interrupt Controller” section in the manual.

The AVB-DMAC related interrupts include descriptor interrupts (15 sources), error interrupts (5 sources), reception interrupts (37 sources), transmission interrupts (2 sources), and gPTP interrupts (3 sources). From the CPU’s perspective, each appears as one of the above four interrupt sources.

The states of an AVB-DMAC-related interrupt sources can be checked in the following registers.

- Descriptor interrupt status register (DIS)
- Error interrupt status register (EIS)
- Receive interrupt status register (RISi)
- Transmit interrupt status register (TIS)
- gPTP interrupt status register (GIS)

The interrupts are controlled by the corresponding interrupt enable bits. However, the status flags operate independently of the settings of the enable bits.

The states of grouped interrupts can only be checked by reading the interrupt summary status register (ISS) and the queue full error interrupt status bit in the error interrupt status register (EIS.QFS). This reduces the load on the CPU.

#### 37A.3.11.1 Transmit/Receive Data Management Interrupt

The management interrupt for transmission and reception is conveyed when the interrupt conditions corresponding to the following sources are satisfied.

- Receive frame interrupt in the receive interrupt status register 0 (RIS0.FRFr)
- Descriptor interrupt in the descriptor interrupt status register (DIS.DPFi)

The general error interrupt state can be checked by reading the descriptor interrupt status bits in the interrupt summary status register (ISS.DPSi) or the receive FIFO warning interrupt summary bit (ISS.RFWS).

#### 37A.3.11.2 Error Management Interrupt

The error management interrupt is conveyed when interrupt conditions corresponding to the following sources are satisfied.

- Time stamp FIFO full interrupt in the error interrupt status register (EIS.TFFF)
- CBS limitation interrupts in the error interrupt status register (EIS.CULF1, EIS.CULF0, EIS.CLLF1, EIS.CLLF0)
- Receive FIFO full interrupt in the receive interrupt status register 2 (RIS2.RFFF)
- Receive queue full interrupt in the receive interrupt status register 2 (RIS2.QFFr)

The general error interrupt state can be checked by reading the error interrupt summary bit in the interrupt summary status register (ISS.ES).



### 37A.3.11.3 Other Management (FIFO Warning, etc.) Interrupts

The other management (FIFO warning, etc.) interrupt is conveyed when interrupt conditions corresponding to the following sources are satisfied.

(1) Reception related interrupt

Receive FIFO warning interrupt in the receive interrupt status register 1 (RIS1.RFWF)

(2) Transmission related interrupts

Time stamp FIFO warning interrupt in the transmit interrupt status register (TIS.TSWF)

Time stamp FIFO update interrupt in the transmit interrupt status register (TIS.TSUF)

(3) gPTP related interrupts

AVTP presentation target match interrupt in the gPTP interrupt status register (GIS.PTMF)

The general error interrupt state can be checked by reading the receive FIFO warning error interrupt status bit in the interrupt summary status register (ISS.RFWS), the time stamp FIFO warning interrupt status bit (ISS.TFWS), and the time stamp FIFO update interrupt status bit (ISS.TFUS).

### 37A.3.11.4 E-MAC Interrupt

The E-MAC interrupt is conveyed when the E-MAC interrupt source is generated.

The general error interrupt state can be checked by reading the E-MAC interrupt summary bit in the interrupt summary status register (ISS.MS).

### 37A.3.12 Flows of Operations

#### 37A.3.12.1 Flow of E-MAC Initialization

Figure 37A.45 shows the flow of E-MAC initialization (for AVB mode and full-duplex operation).

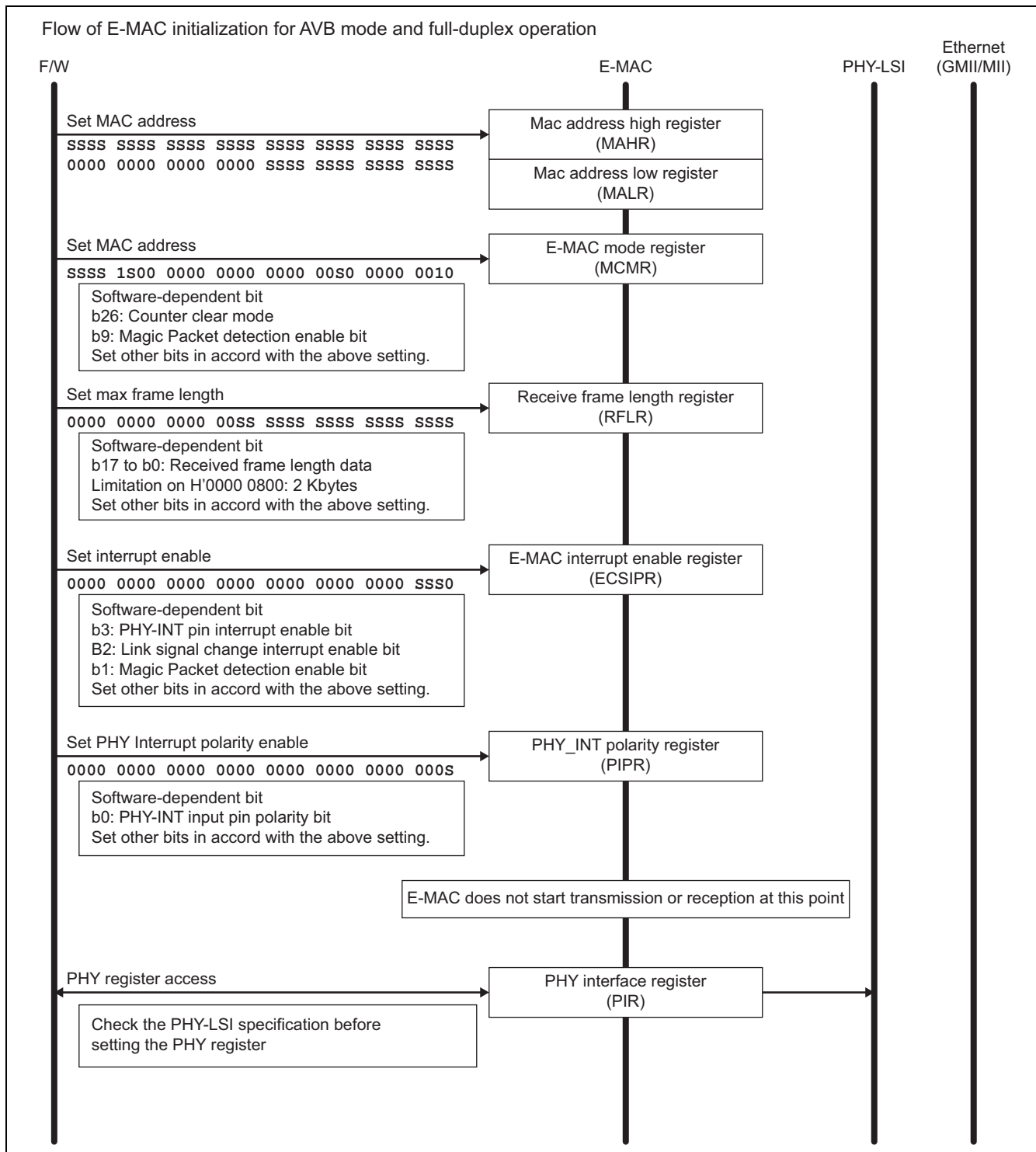


Figure 37A.45 Flow of E-MAC Initialization (for AVB Mode and Full-Duplex Operation)

### 37A.3.12.2 Flow of AVB-DMAC Initialization

Figure 37A.46 shows the flow of AVB-DMAC initialization (for AVB mode and full-duplex operation).

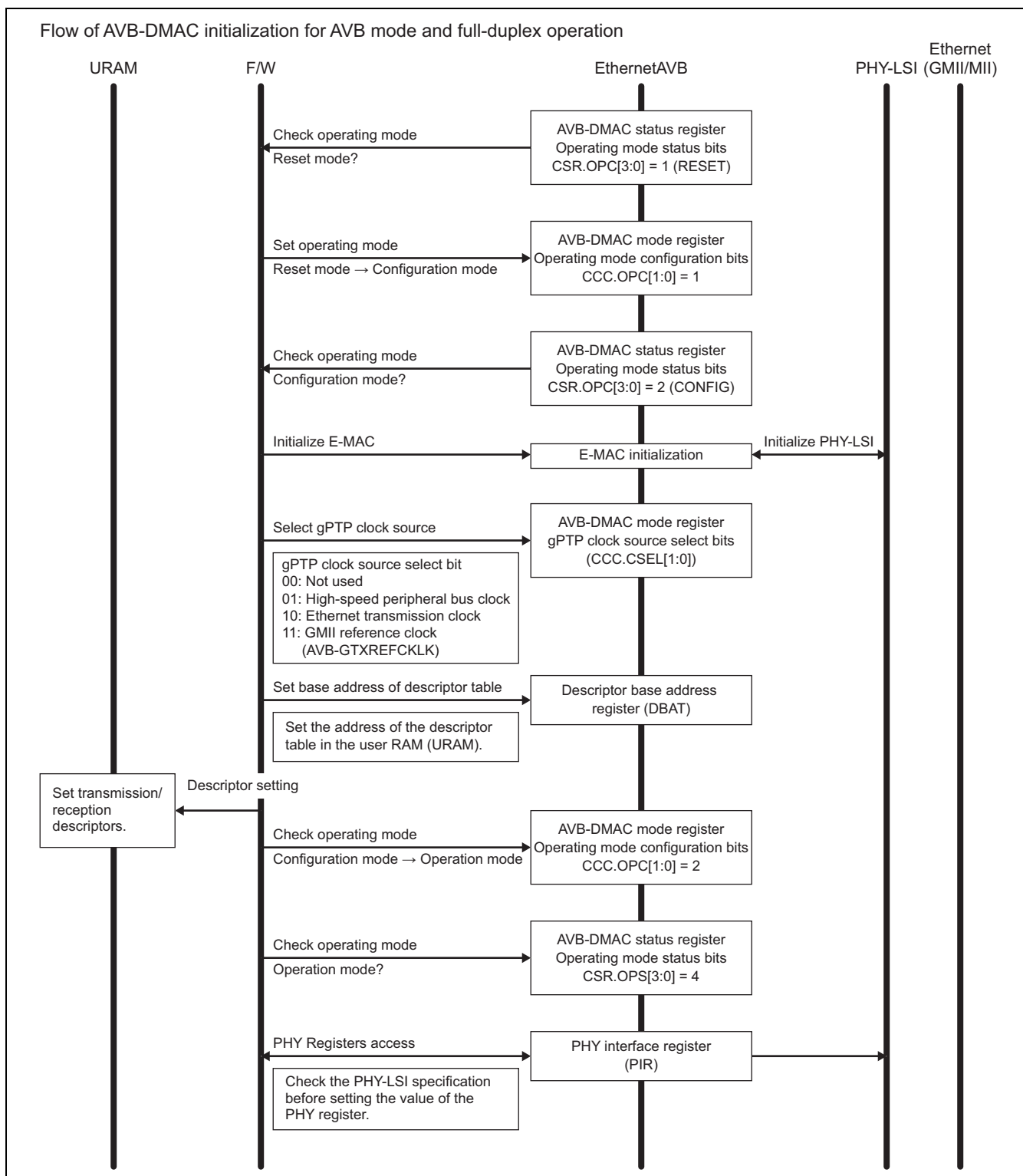


Figure 37A.46 Flow of AVB-DMAC Initialization (for AVB Mode and Full-Duplex Operation)

37A.3.12.3 Flow for the AVB-DMAC in Reception

Figure 37A.47 shows the flow for the AVB-DMAC in reception (in AVB mode and full-duplex operation).

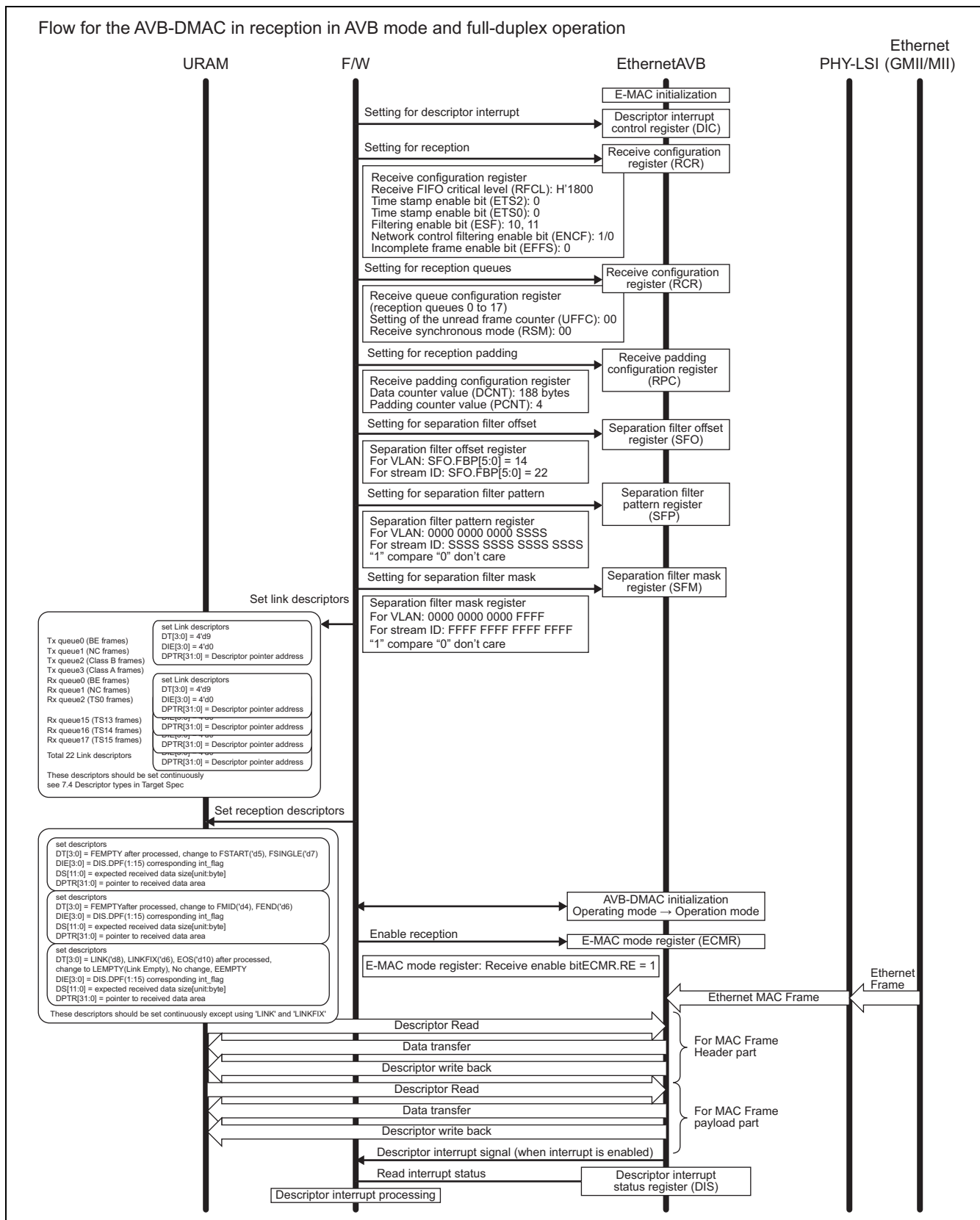


Figure 37A.47 Flow for the AVB-DMAC in Reception (in AVB Mode and Full-Duplex Operation)

37A.3.12.4 Flow for the AVB-DMAC in Transmission

Figure 37A.48 shows the flow for the AVB-DMAC in transmission (in AVB mode and full-duplex operation).

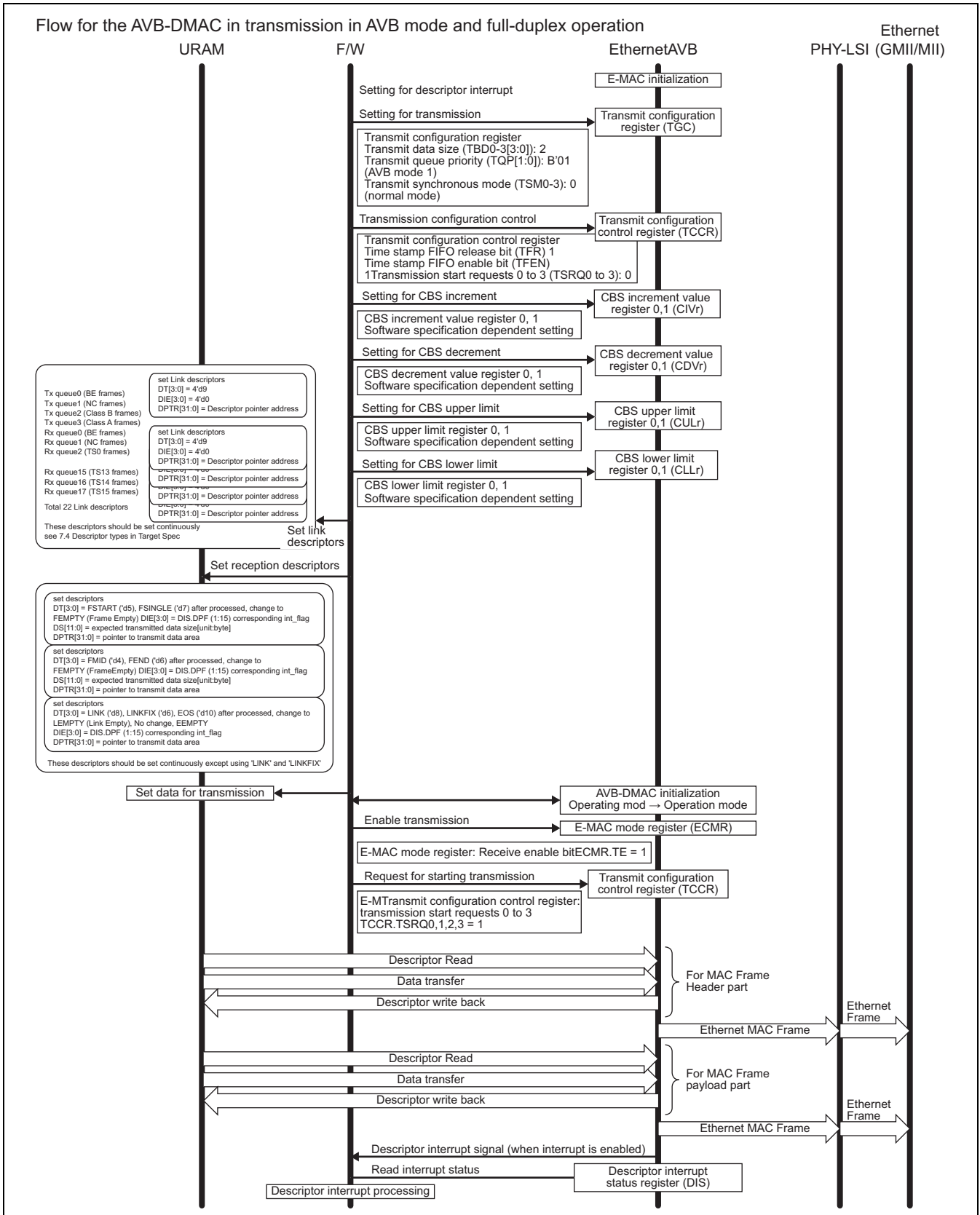


Figure 37A.48 Flow for the AVB-DMAC in Transmission (in AVB Mode and Full-Duplex Operation)

### 37A.3.12.5 Flow for Stopping AVB-DMAC Operation in Reception

Figure 37A.49 shows the flow for stopping AVB-DMAC operation in reception (normal, common to all modes).

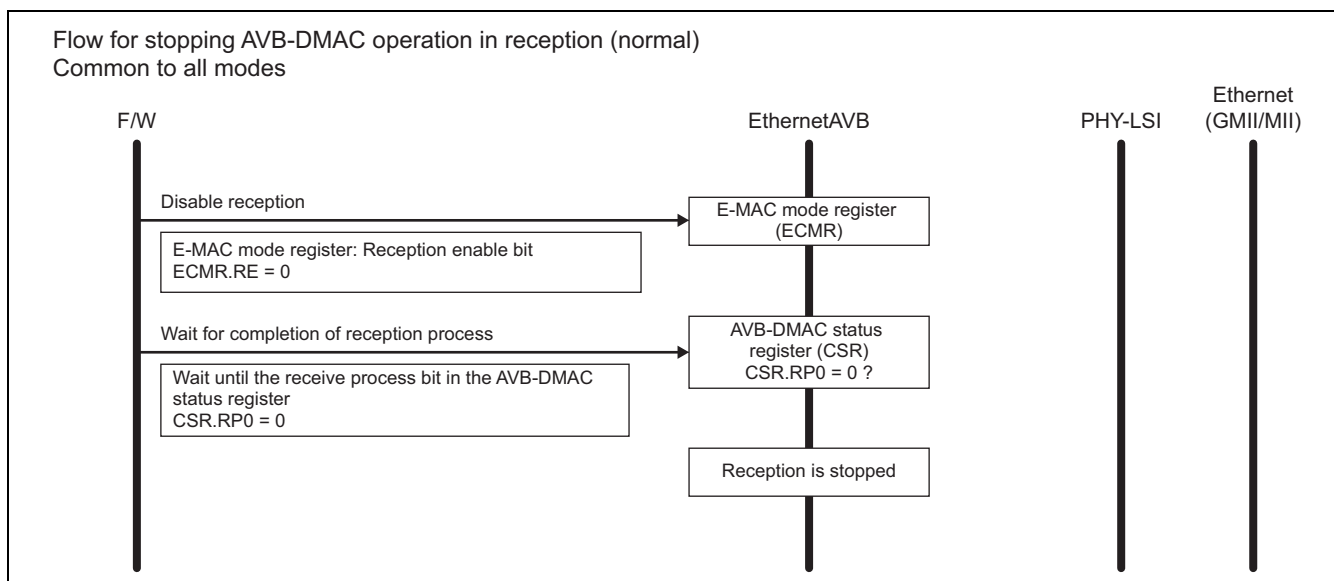


Figure 37A.49 Flow for Stopping AVB-DMAC Operation in Reception (Normal, Common to All Modes)

### 37A.3.12.6 Flow for Stopping AVB-DMAC Operation in Transmission

Figure 37A.50 shows the flow for stopping AVB-DMAC operation in transmission (normal, common to all modes).

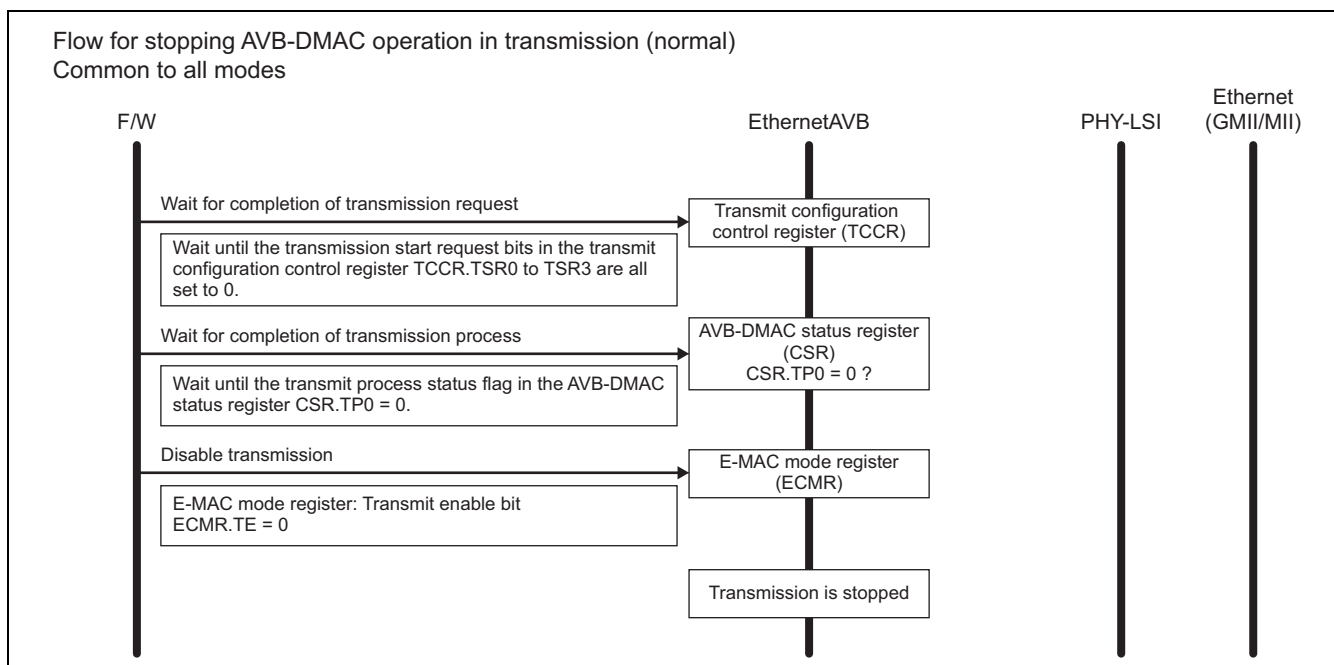
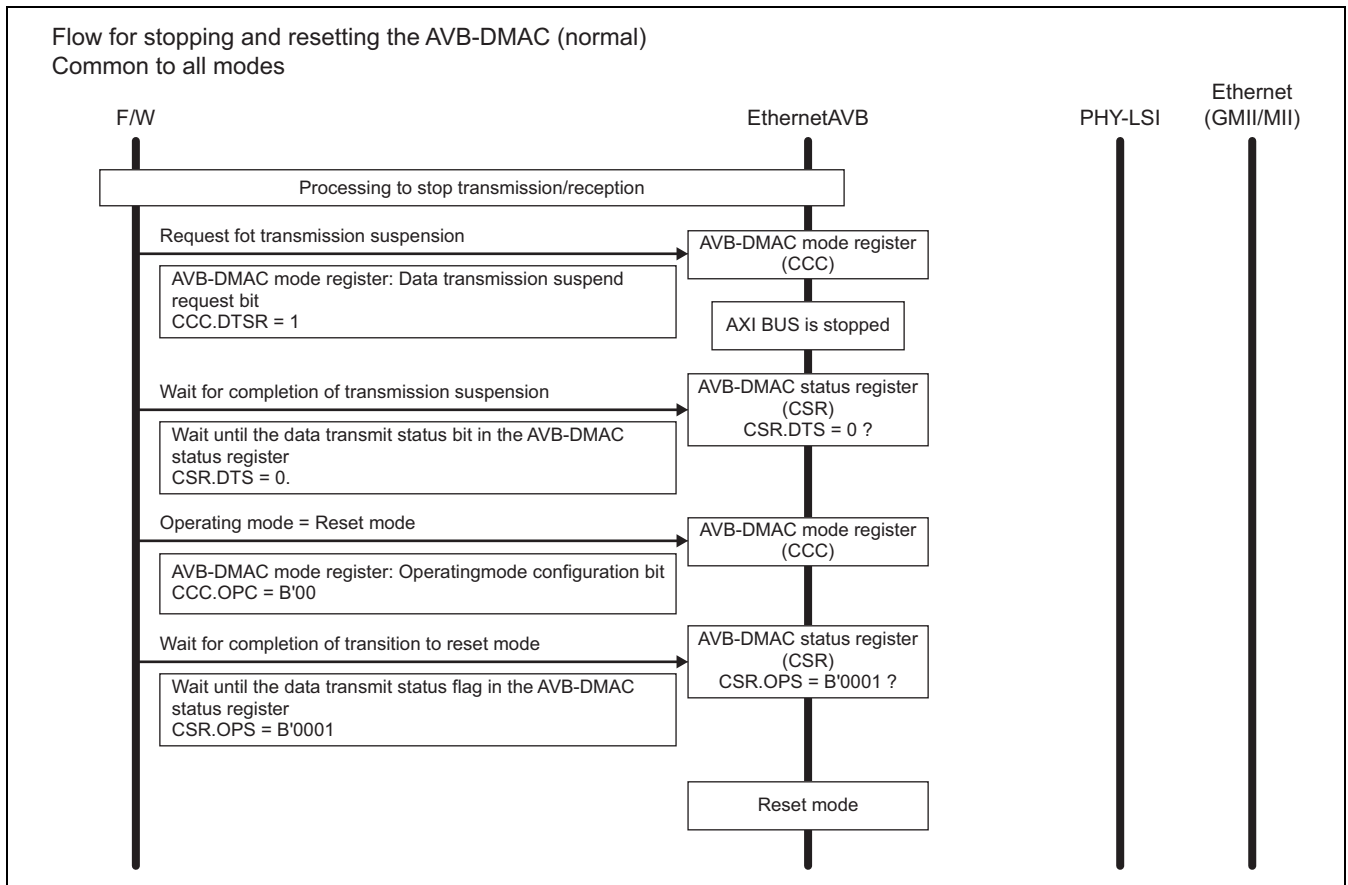


Figure 37A.50 Flow for Stopping AVB-DMAC Operation in Transmission (Normal, Common to All Modes)

**37A.3.12.7 Flow for Stopping and Resetting the AVB-DMAC**

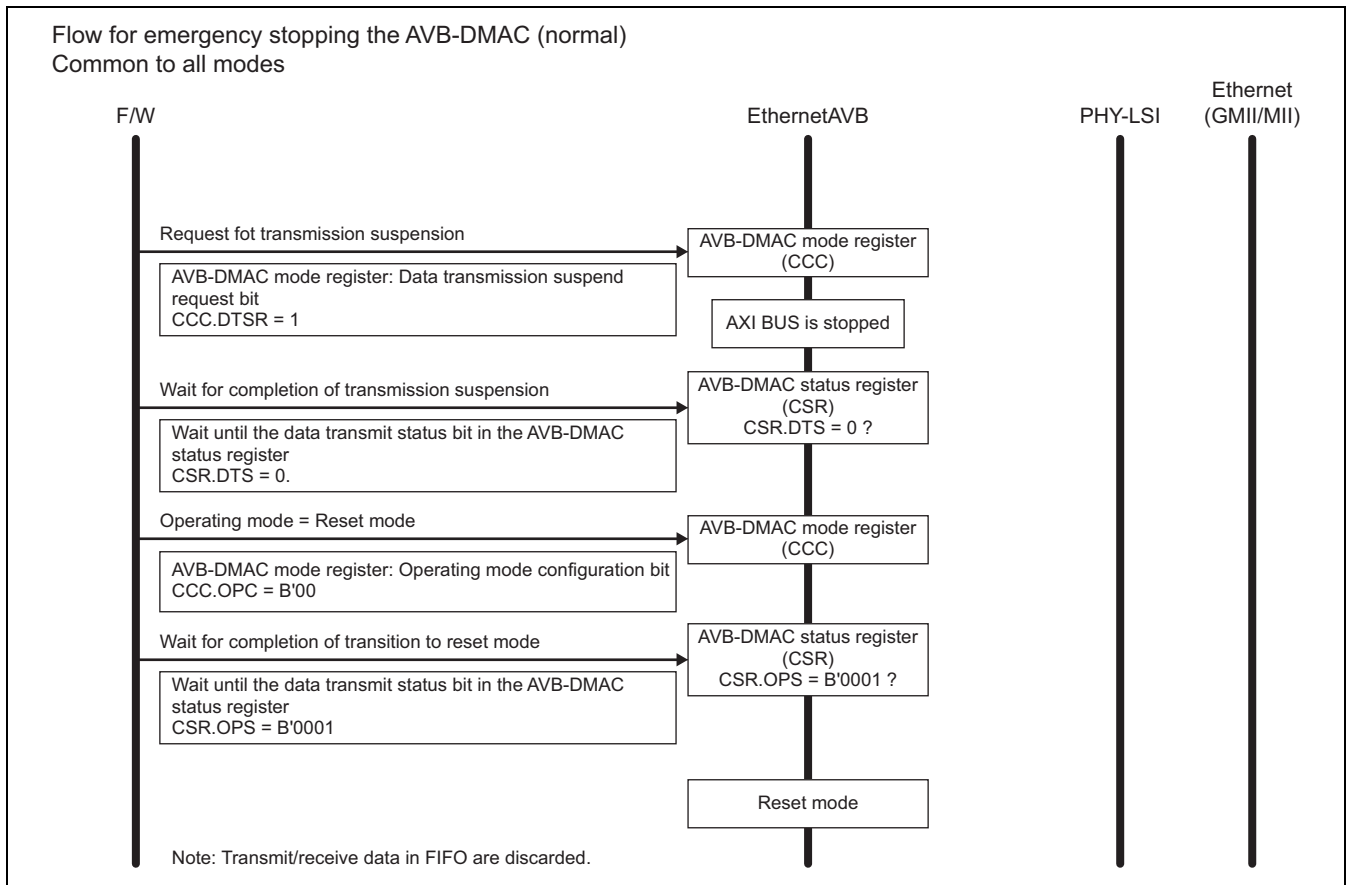
Figure 37A.51 shows the flow for stopping and resetting the AVB-DMAC (normal, common to all modes).



**Figure 37A.51 Flow for Stopping and Resetting the AVB-DMAC (Normal, Common to All Modes)**

### 37A.3.12.8 Flow for Emergency Stopping the AVB-DMAC

Figure 37A.52 shows the flow for emergency stopping the AVB-DMAC (normal, common to all modes).



**Figure 37A.52 Flow for Emergency Stopping the AVB-DMAC (Normal, Common to All Modes)**



### 37A.3.12.9 Flow of gPTP Initialization

Figure 37A.53 shows the flow of gPTP initialization (normal, common to all modes).

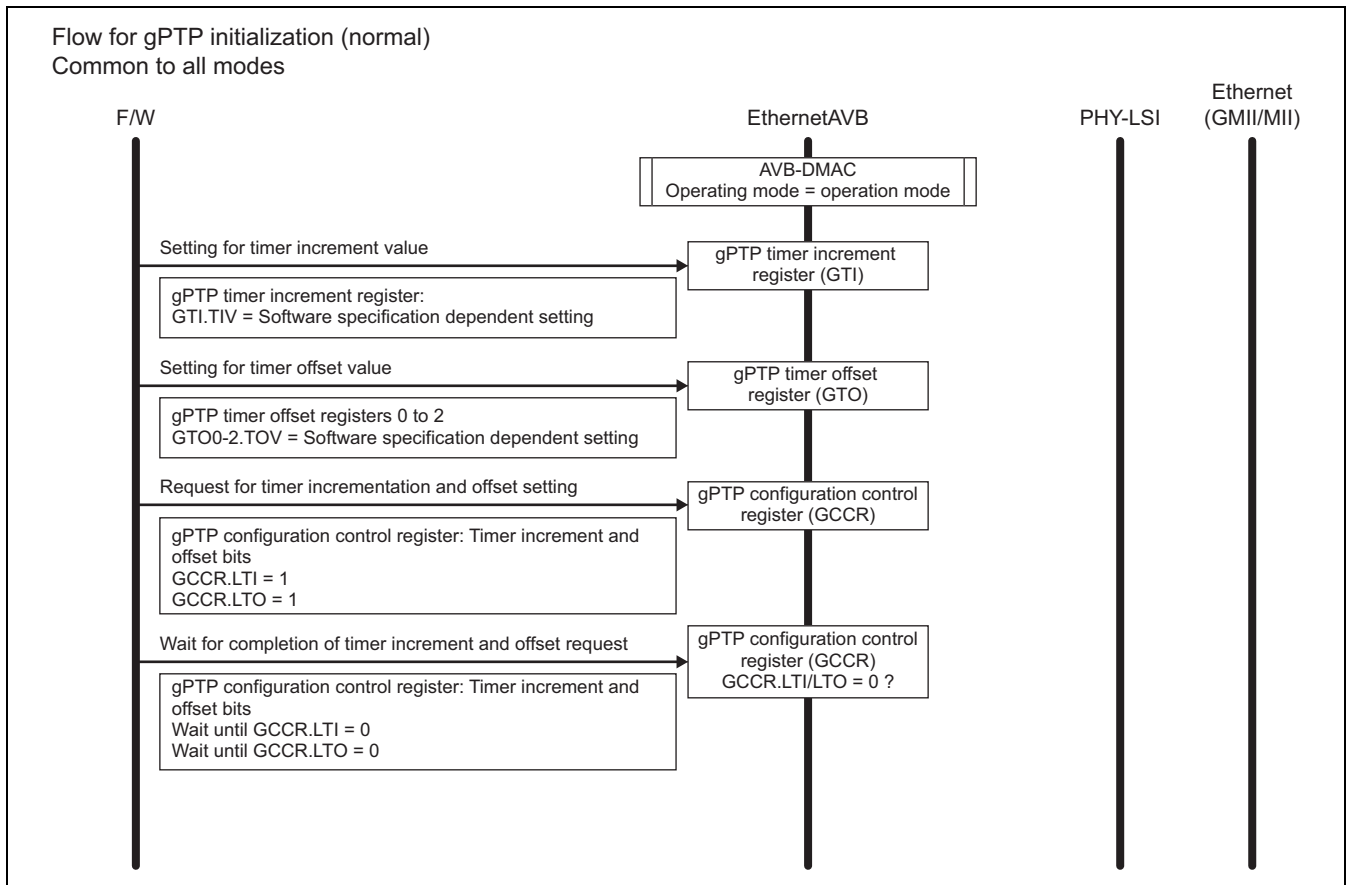


Figure 37A.53 Flow of gPTP Initialization (Normal, Common to All Modes)

### 37A.3.12.10 Flow of gPTP Time Stamping in Transmission

Figure 37A.54 shows the flow of gPTP time stamping in transmission (normal, common to all modes).

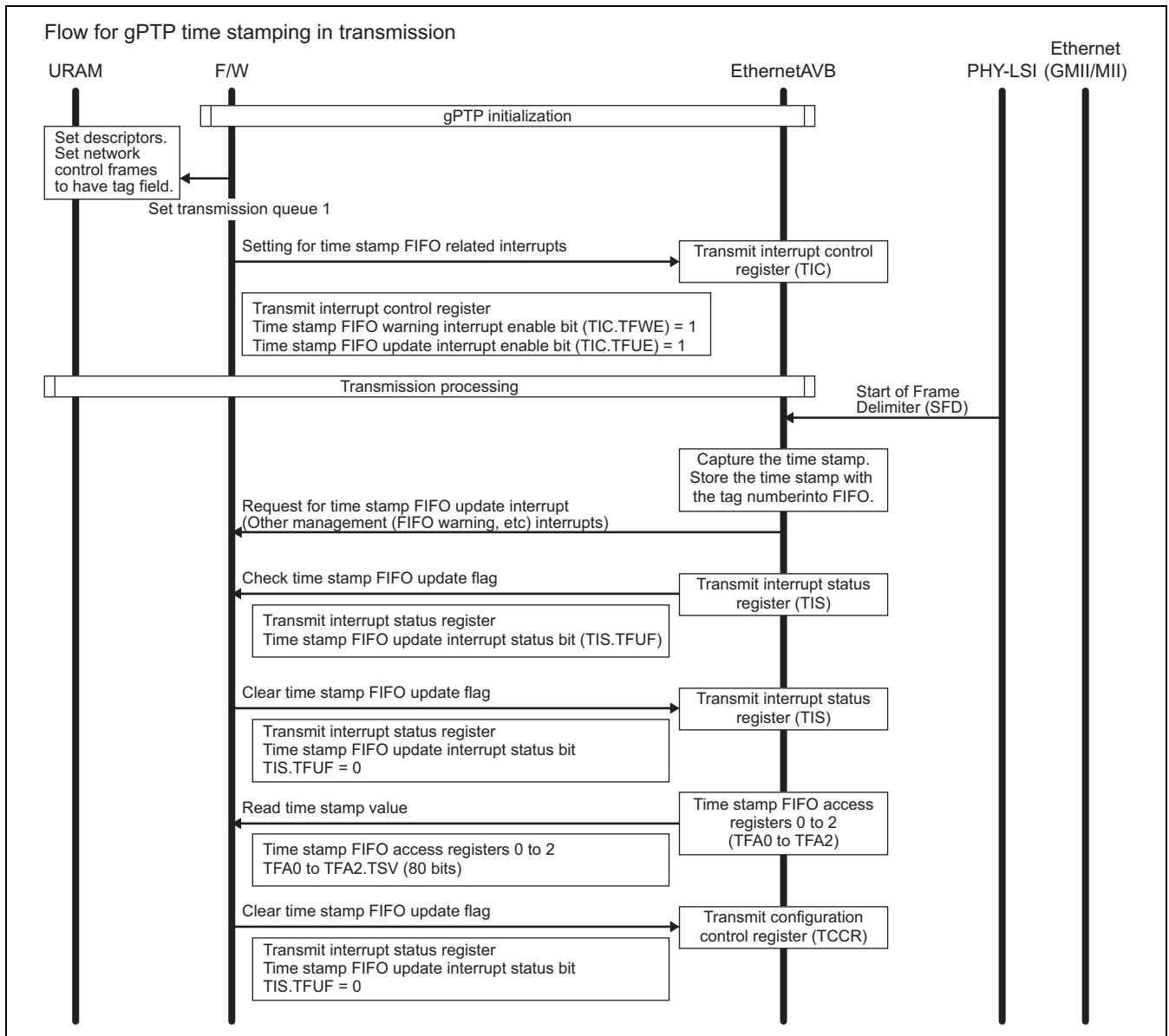
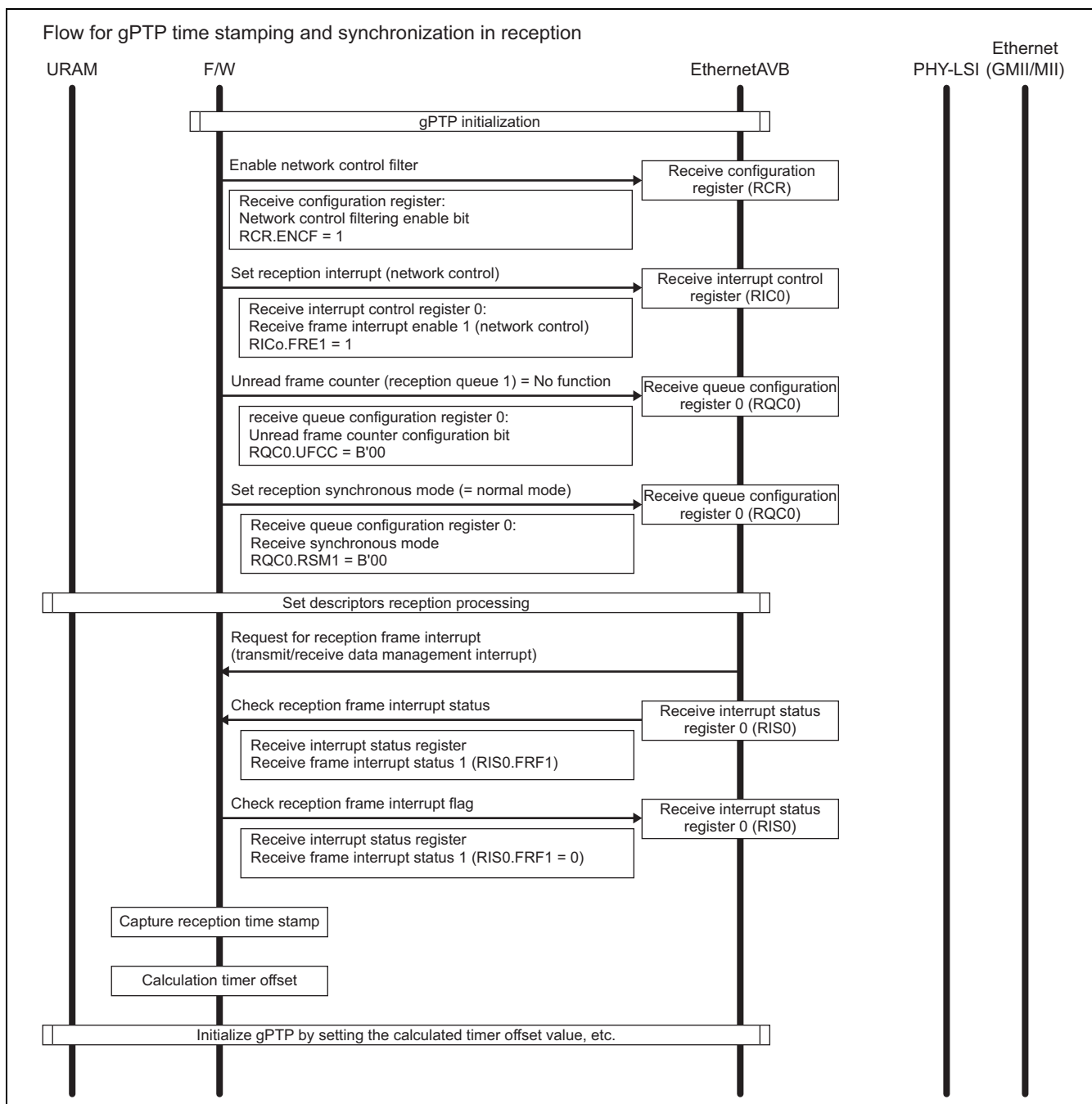


Figure 37A.54 Flow of gPTP Time Stamping in Transmission (Normal, Common to All Modes)

**37A.3.12.11 Flow of gPTP Time Stamping and Synchronization in Reception**

Figure 37A.55 shows the flow of gPTP time stamping and synchronization in reception (normal, common to all modes).



**Figure 37A.55 Flow of gPTP Time Stamping and Synchronization in Reception (Normal, Common to All Modes)**

### 37A.3.12.12 Flow of Capturing gPTP Presentation Times

Figure 37A.56 shows the flow of capturing gPTP presentation times (common to all modes).

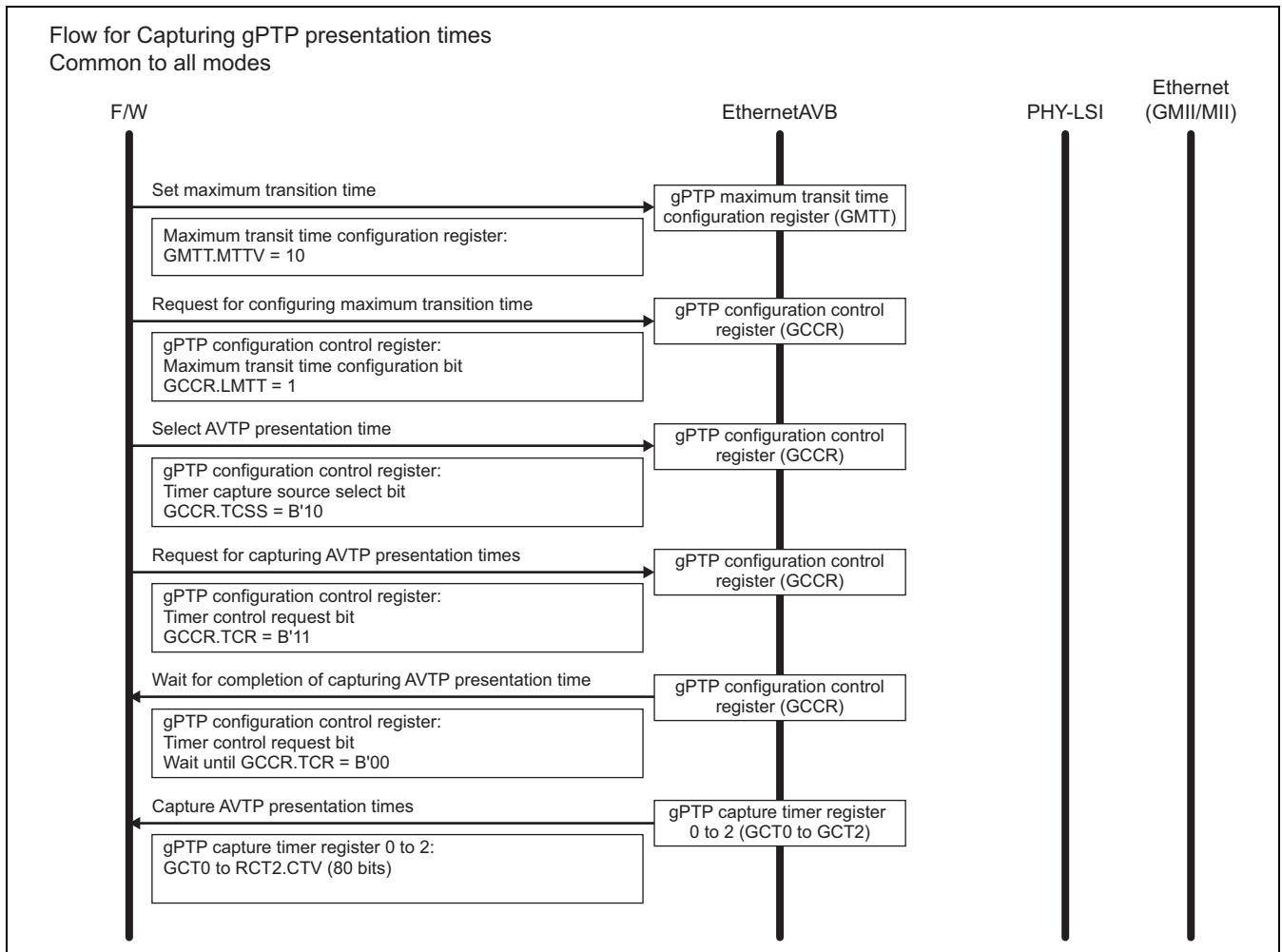


Figure 37A.56 Flow of Capturing gPTP Presentation Times (Common to All Modes)

### 37A.3.12.13 Flow of AVTP Presentation Time Comparison

Figure 37A.57 shows the flow of AVTP presentation time comparison (common to all modes).

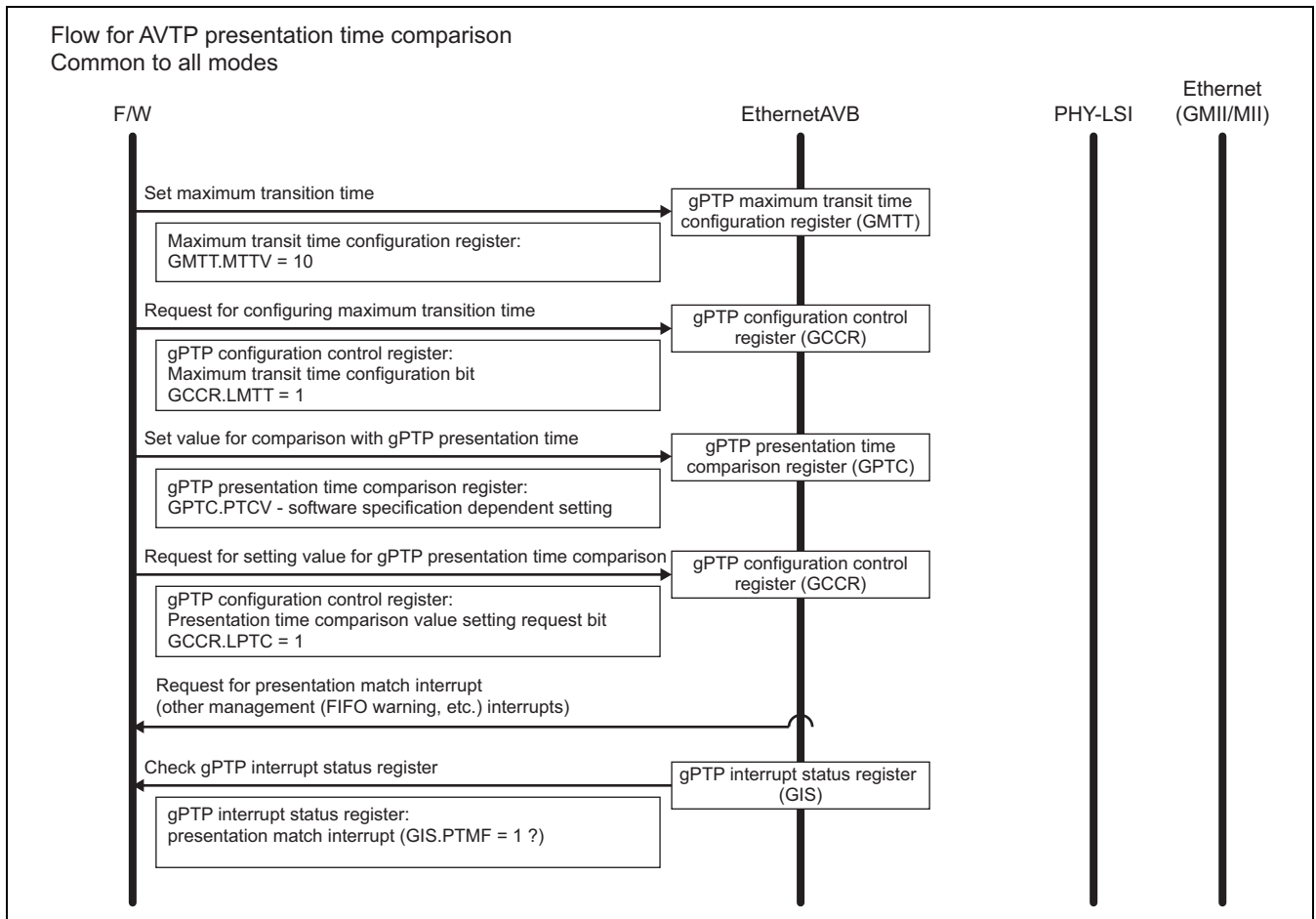


Figure 37A.57 Flow of AVTP Presentation Time Comparison (Common to All Modes)

### 37A.3.12.14 Flow of Loopback Mode Operation

Figure 37A.58 shows the flow of loopback mode operation.

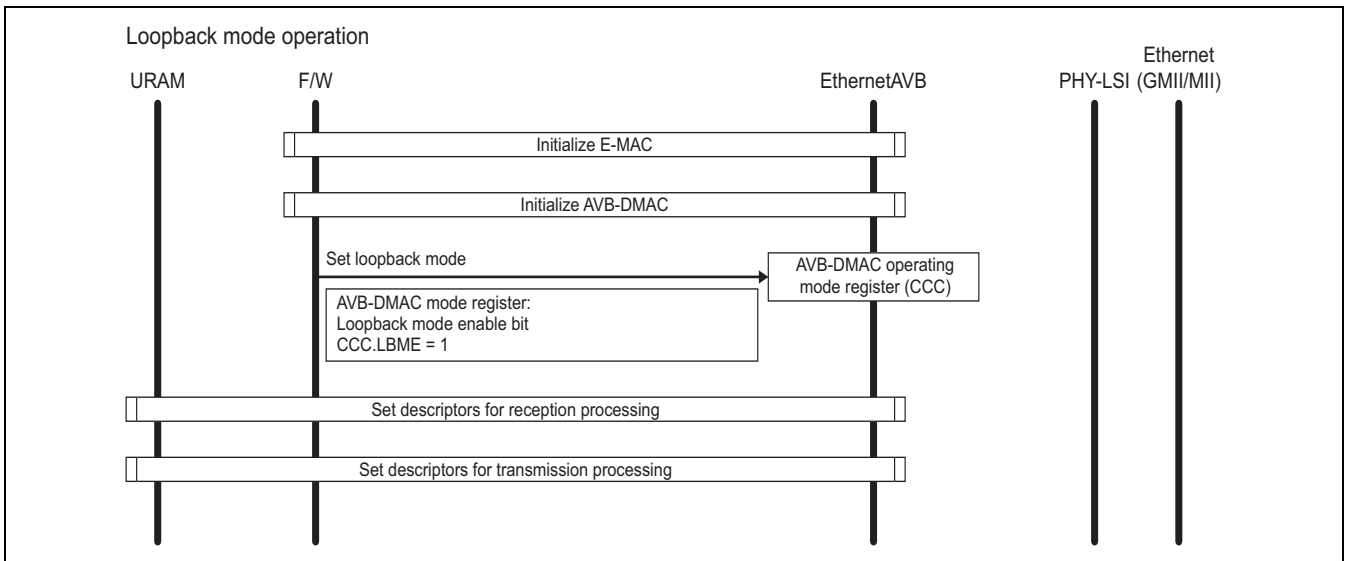
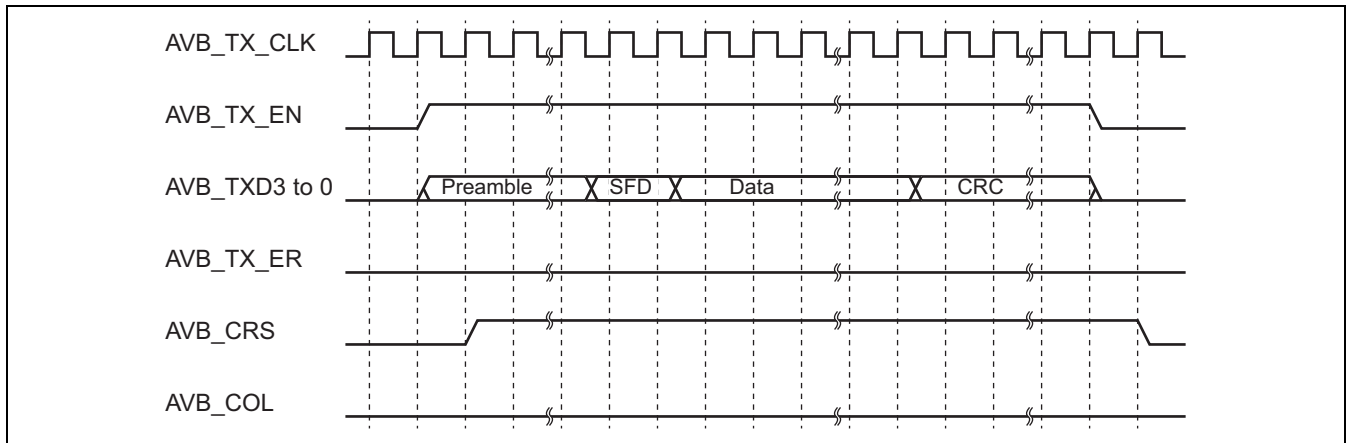


Figure 37A.58 Flow of Loopback Mode Operation

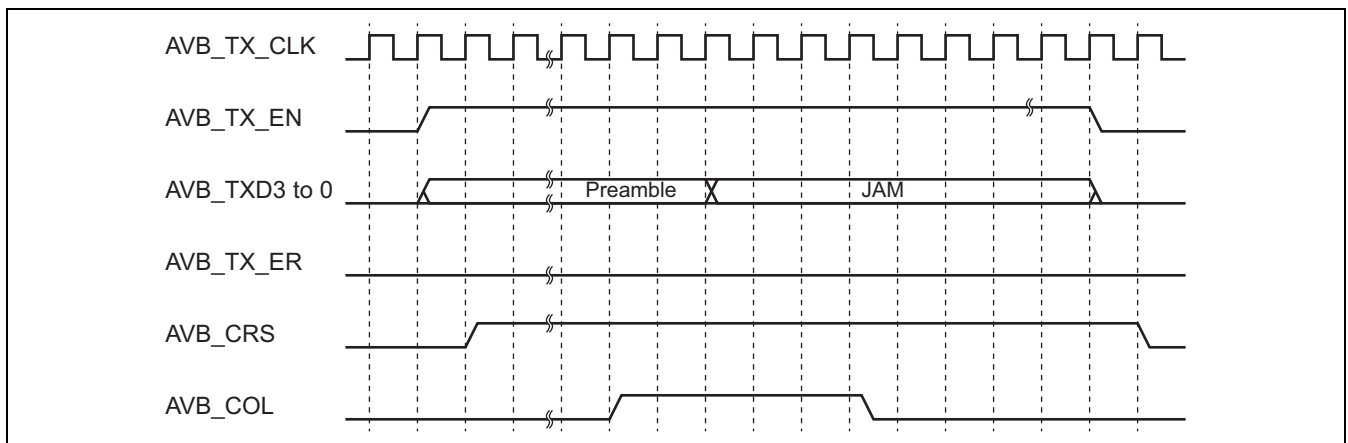
**37A.3.13 Connection to PHY-LSI**

**37A.3.13.1 MII Frame Transmission/Reception Timing**

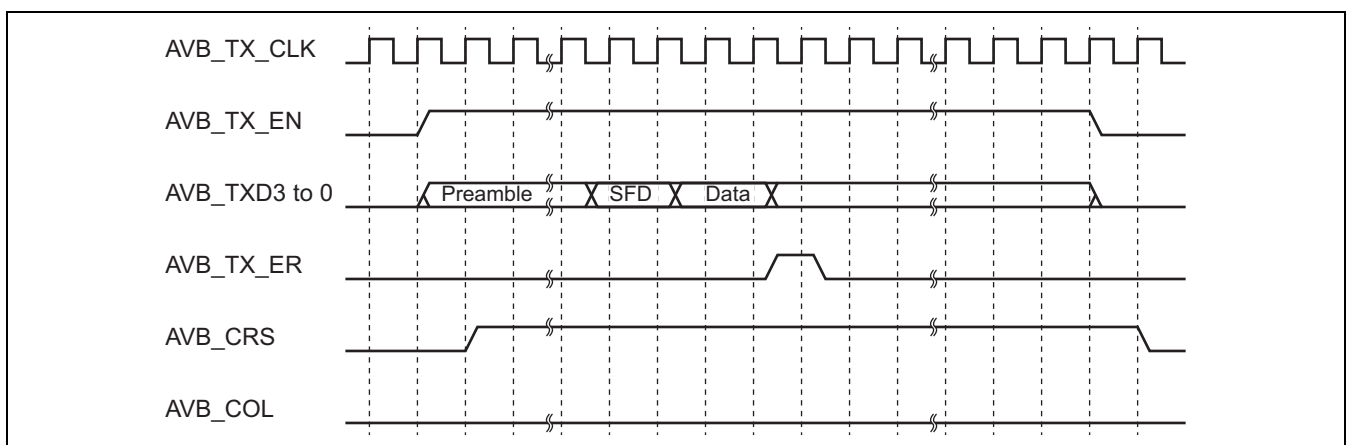
Each MII frame transmission/reception timing is shown in Figures 37A.59 to 37A.64.



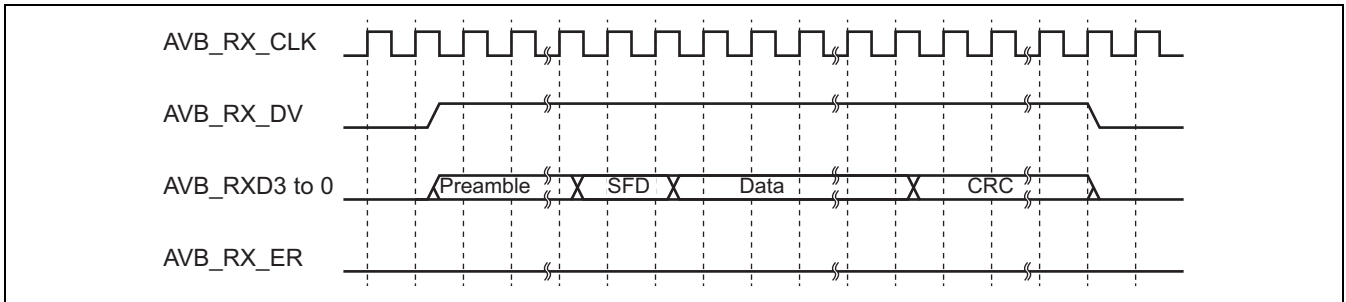
**Figure 37A.59 MII Frame Transmit Timing (Normal Transmission)**



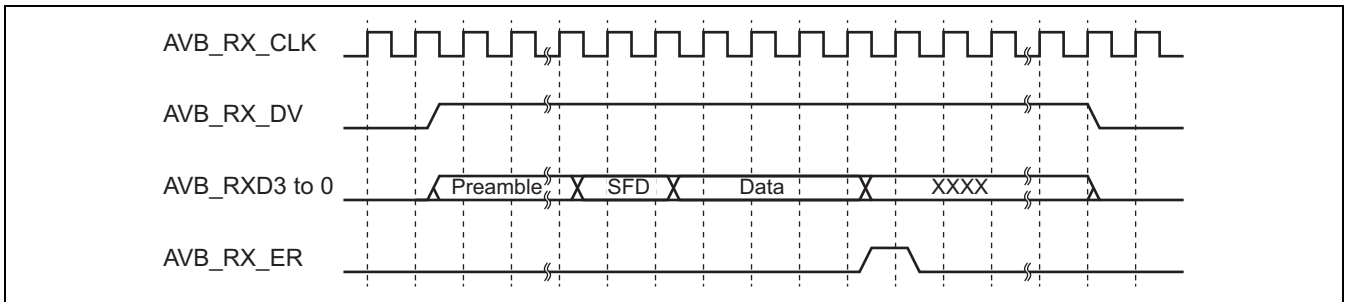
**Figure 37A.60 MII Frame Transmit Timing (Collision)**



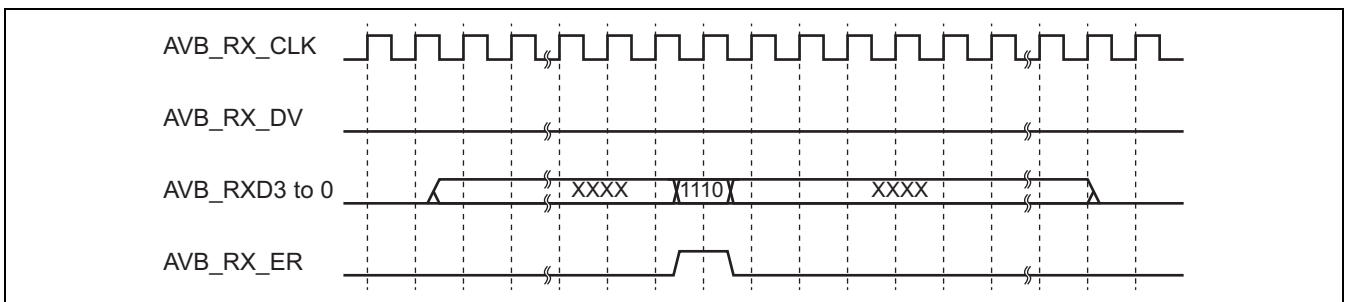
**Figure 37A.61 MII Frame Transmit Timing (Transmit Error)**



**Figure 37A.62 MII Frame Receive Timing (Normal Reception)**



**Figure 37A.63 MII Frame Receive Timing (Reception Error (1))**

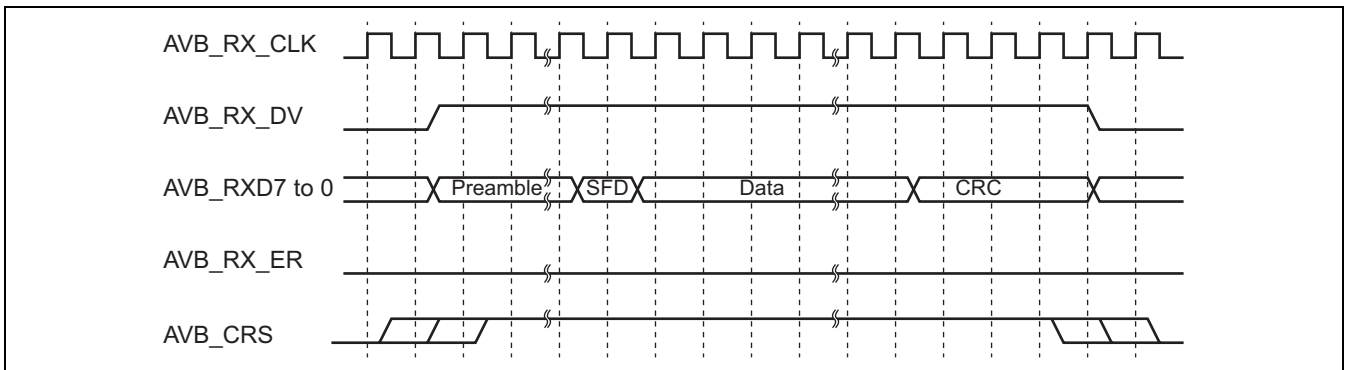


**Figure 37A.64 MII Frame Receive Timing (Reception Error (2))**

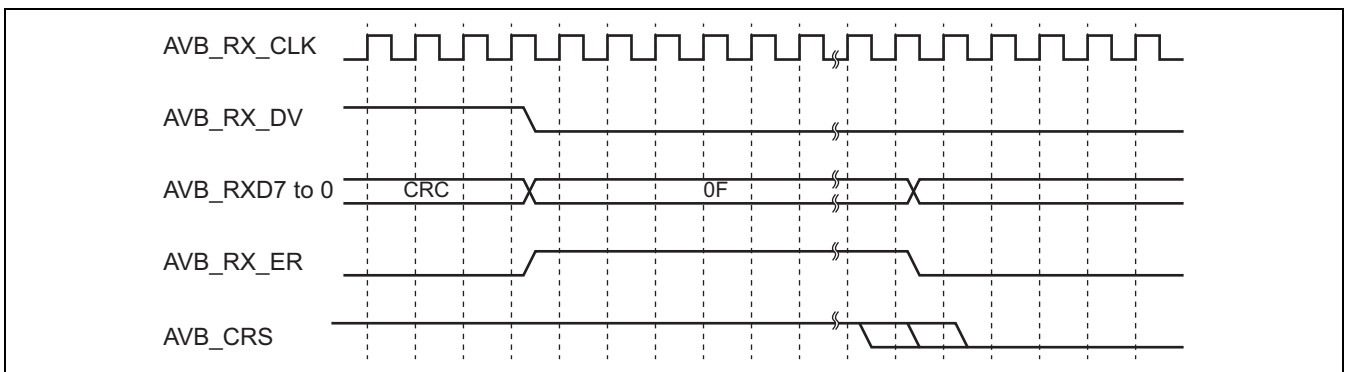


### 37A.3.13.2 GMII Frame Reception Timing

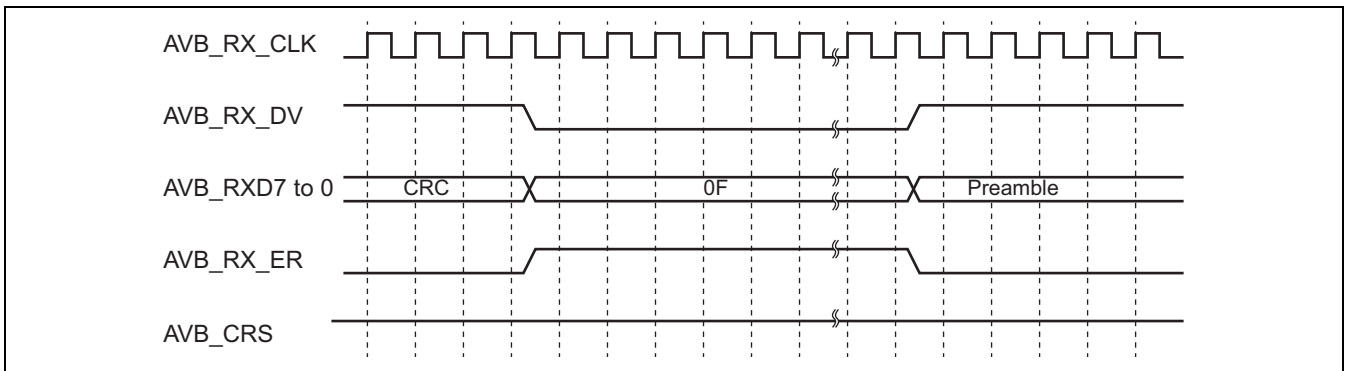
Each GMII frame reception timing is shown in Figures 37A.65 to 37A.70.



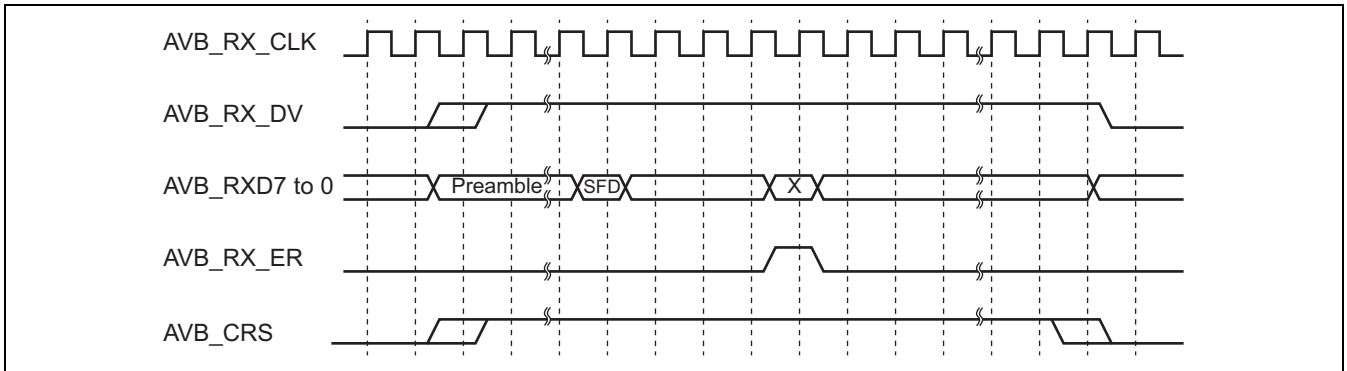
**Figure 37A.65 GMII Fame Receive Timing (Normal Reception)**



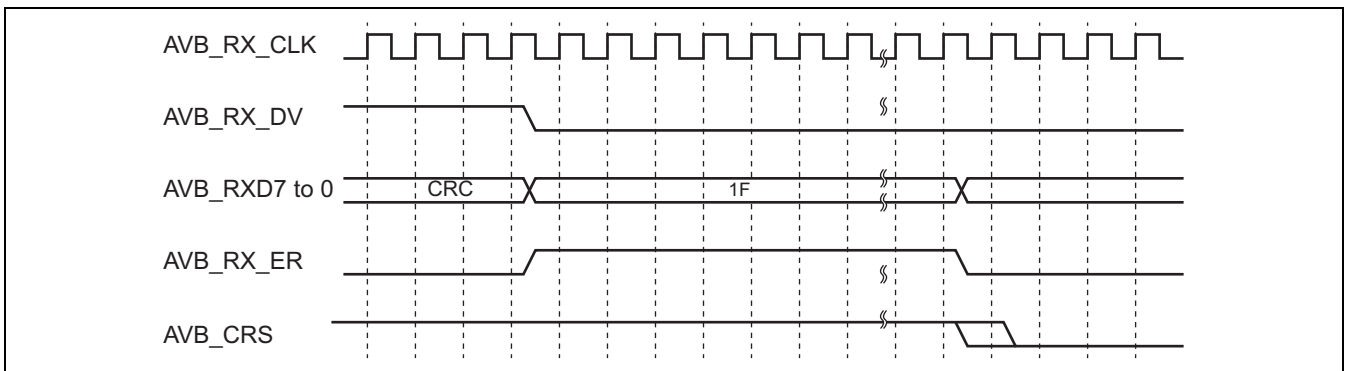
**Figure 37A.66 GMII Fame Receive Timing (with Carrier Extension)**



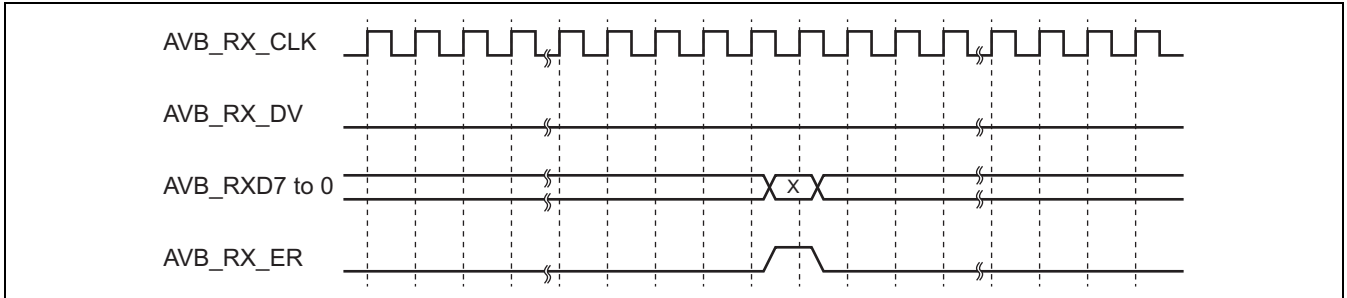
**Figure 37A.67 GMII Fame Receive Timing (Burst Reception)**



**Figure 37A.68 GMII Fame Receive Timing (Reception Error)**



**Figure 37A.69 GMII Fame Receive Timing (Error with Carrier Extension)**



**Figure 37A.70 GMII Fame Receive Timing (False Carrier Indication)**

### 37A.3.13.3 Accessing MII Management Registers

MII management registers in the PHY-LSI are accessed via PIR in this LSI. PIR is used as a serial interface conforming to the MII frame format specified in IEEE802.3u.

#### (1) MII Management Frame Format

Figure 37A.71 shows the format of an MII management frame. To access an MII management register, a management frame is implemented by the program in accordance with the procedures shown in MII Management Register Access Procedure.

Access Type	MII Management Frame							
Item	PRE	ST	OP	PHYAD	REGAD	TA	DATA	IDLE
Number of bits	32	2	2	5	5	2	16	
Read	1..1	01	10	00001	RRRRR	Z0	D...D	
Write	1..1	01	01	00001	RRRRR	10	D...D	X

[Legend]

PRE: 32 consecutive 1 s

ST: Write of B'01 indicating start of frame

OP: Write of code indicating access type

PHYAD: Write of B'00001 if the PHY-LSI address is 1 (sequential write starting with the MSB).  
This bit changes depending on the PHY-LSI address.

REGAD: Write of 000q if the register address is 1 (sequential write starting with the MSB).  
This bit changes depending on the PHY-LSI register address.

TA: Time for switching data transmission source on MII interface  
(a) Write: 10 written  
(b) Read: Bus release (notation: Z0) performed

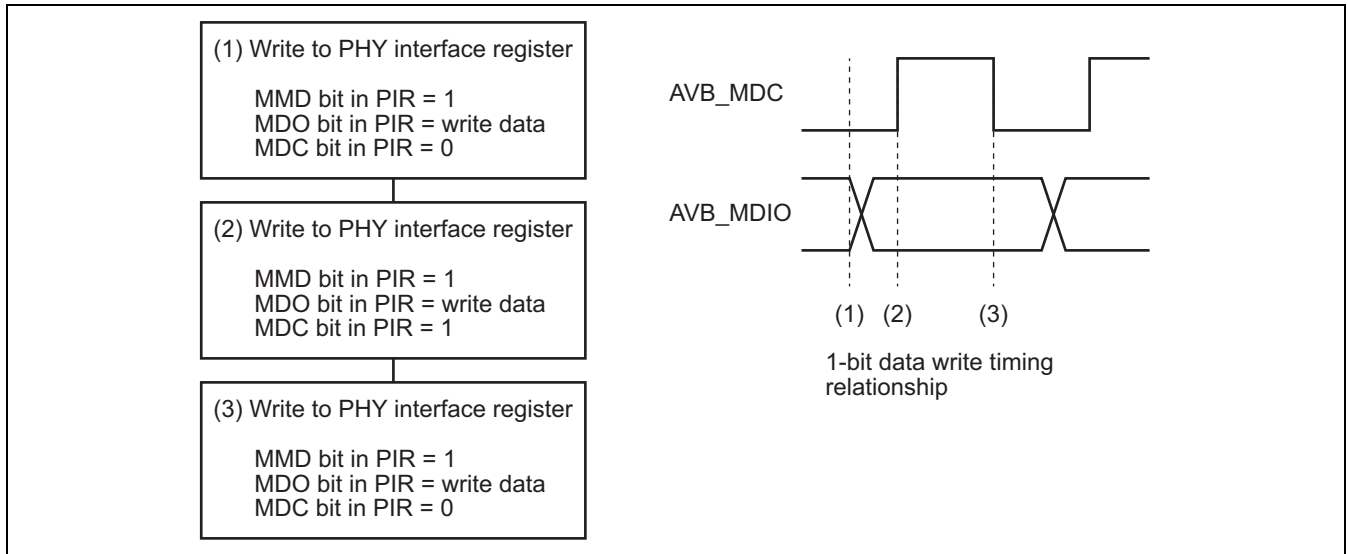
DATA: 16-bit data. Sequential write or read from MSB  
(a) Write: 16-bit data write  
(b) Read: 16-bit data read

IDLE: Wait time until next MII management format input  
(a) Write: Independent bus release (notation: X) performed  
(b) Read: Bus already released in TA: control unnecessary

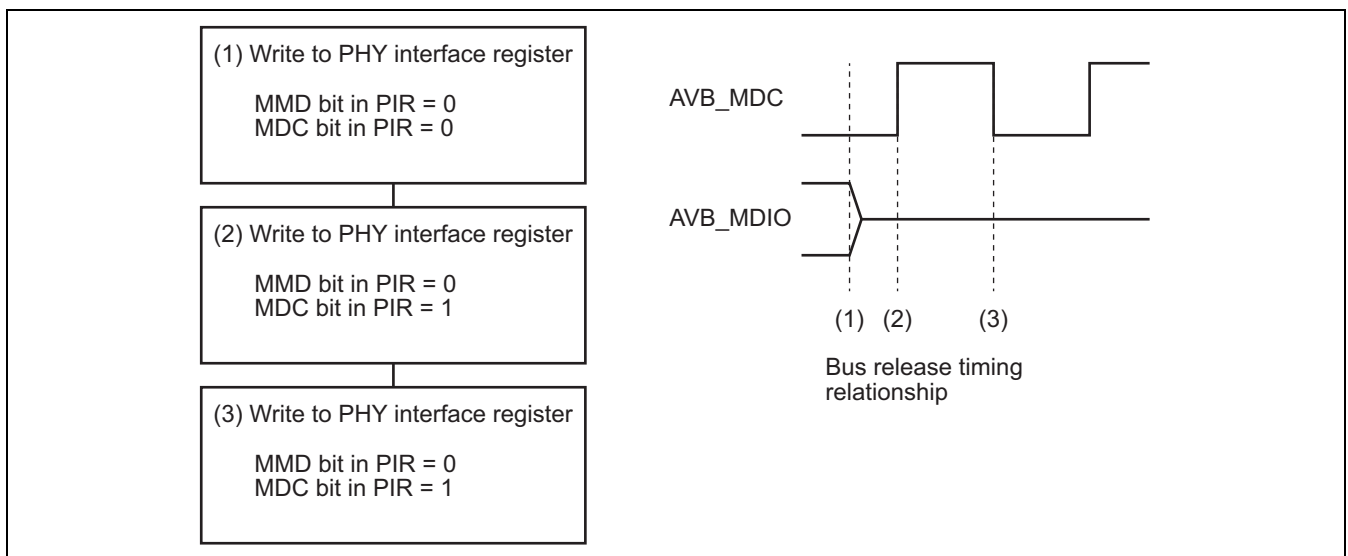
**Figure 37A.71 MII Management Frame Format**

#### (2) MII Management Register Access Procedure

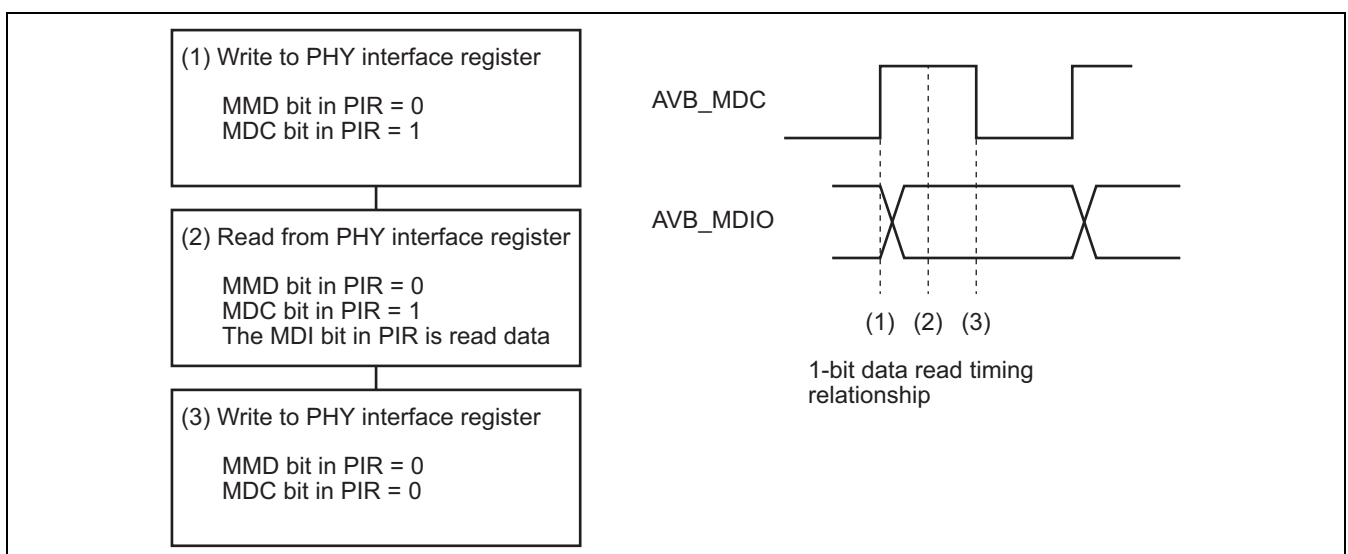
The program accesses MII management registers via PIR. Access is implemented by a combination of 1-bit-unit data write, 1-bit-unit data read, bus release, and independent bus release. Figures 37A.72 to 37A.75 show the MII management register timing. The timing will differ depending on the PHY-LSI type.



**Figure 37A.72 1-Bit Data Write Flowchart**



**Figure 37A.73 Bus Release Flowchart (TA in Read in Figure 37A.71)**



**Figure 37A.74 1-Bit Data Read Flowchart**

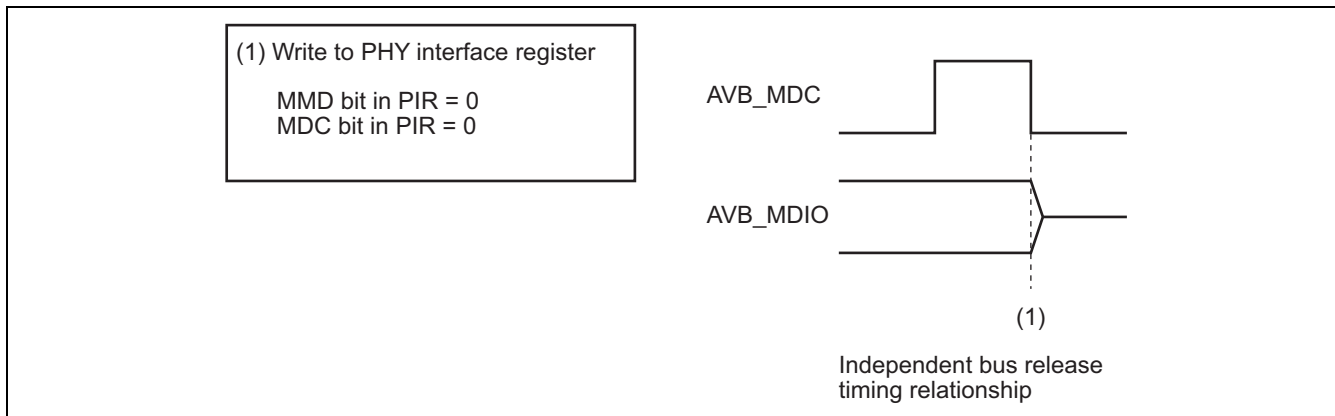


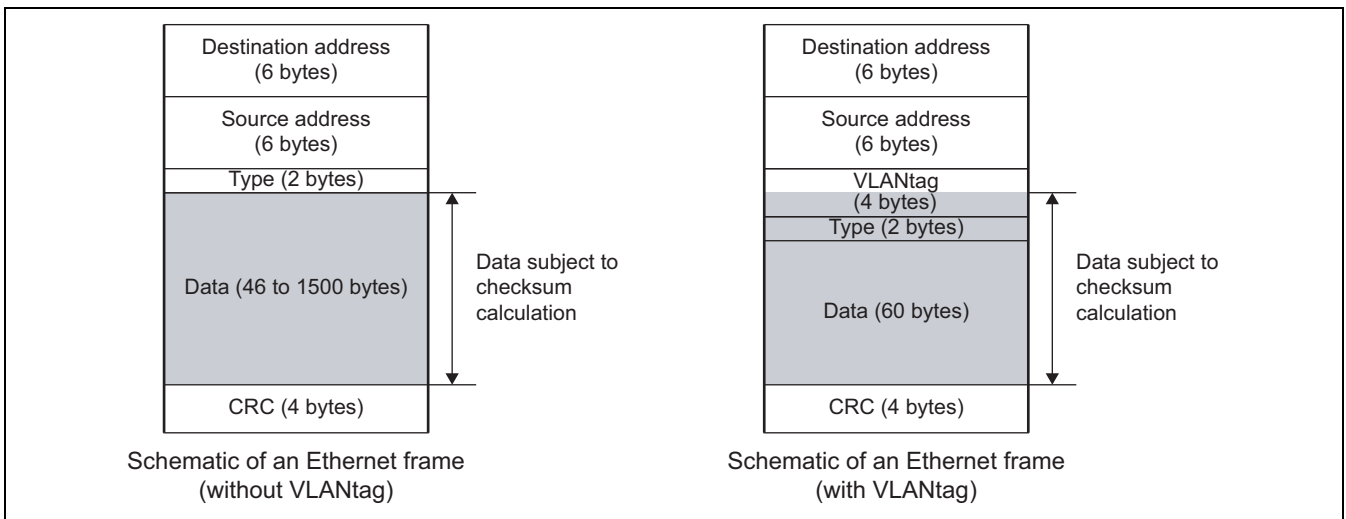
Figure 37A.75 Independent Bus Release Flowchart (IDLE in Write in Figure 37A.71)

**37A.3.14 Usage Notes**

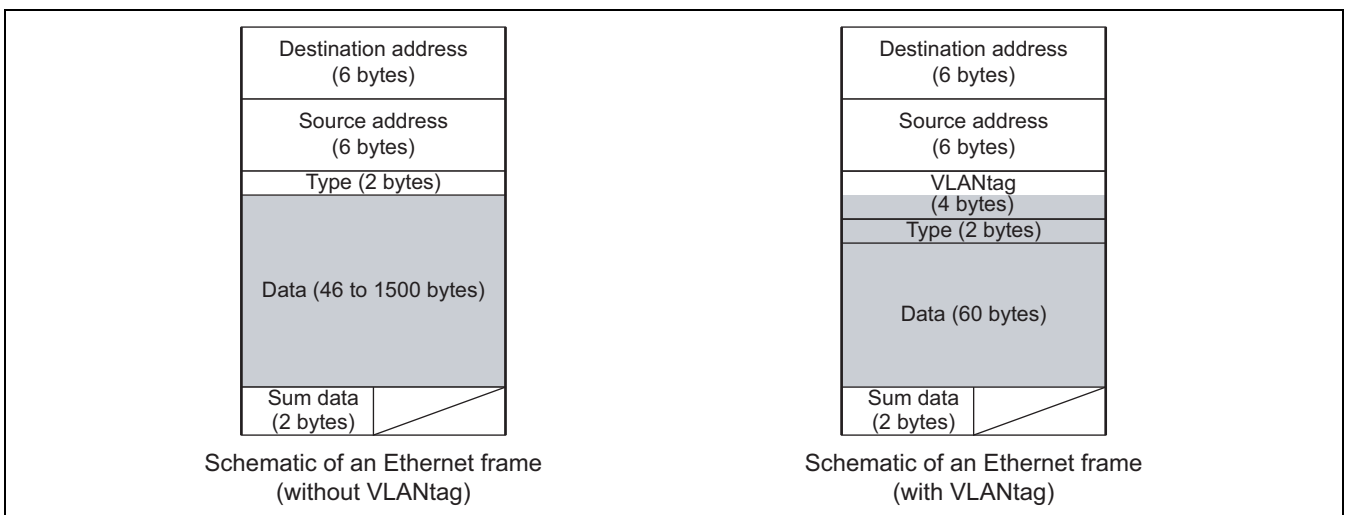
**37A.3.14.1 Checksum Calculation of Ethernet Frames**

This LSI is capable of calculating the checksum data of the received frames. Only the data fields of the Ethernet frames are subject to checksum calculation. Specifically, a data field follows the length/type field and is followed by the CRC field. Figure 37A.76 shows schematics indicating which parts of the Ethernet frames are calculated. Calculation involves 16-bit addition only; it does not involve bit inversion. Note that when the checksum data is valid, the CRC data (4 bytes) is not transferred as a receive frame, and the checksum data (sum data) is added automatically. Figure 37A.77 shows schematics of Ethernet frames to which the checksum data has been added.

Note: Also for the frames with VLANtag inserted, the 15th byte from the top and the following bytes before the CRC field are subject to calculation.



**Figure 37A.76 Data Subject to Checksum Calculation**



**Figure 37A.77 Data after Checksum Data Addition**

### 37A.3.14.2 Data Transfer Function Stops after Read Access Error

If EthernetAVB gets an access error when reading from work RAM, it may happen that no further work RAM accesses are issued. So transfer of receive/transmit frames is halted. By using the data transfer suspend function SW can observe if data transfer function is available or not.

Perform one of given SW flows which are triggered by this start condition: when AXI read access error has been flagged by EIS.QEF is 1, and ESR.ET is B'0000 or B'0100; additionally when ESR.EIL is 1 (this is an indication that an work RAM read error may be lost).

There are two possible SW flows given. Figure 37A.78 applies always the SW reset, independently if this is required or not. Figure 37A.79 checks in addition if SW reset is required; checking CSR.DTS after wait gives an indication that issue has been occurred.

Note that the wait after write of CCC.DTSR is mandatory to prevent cases where issue has not been occurred.

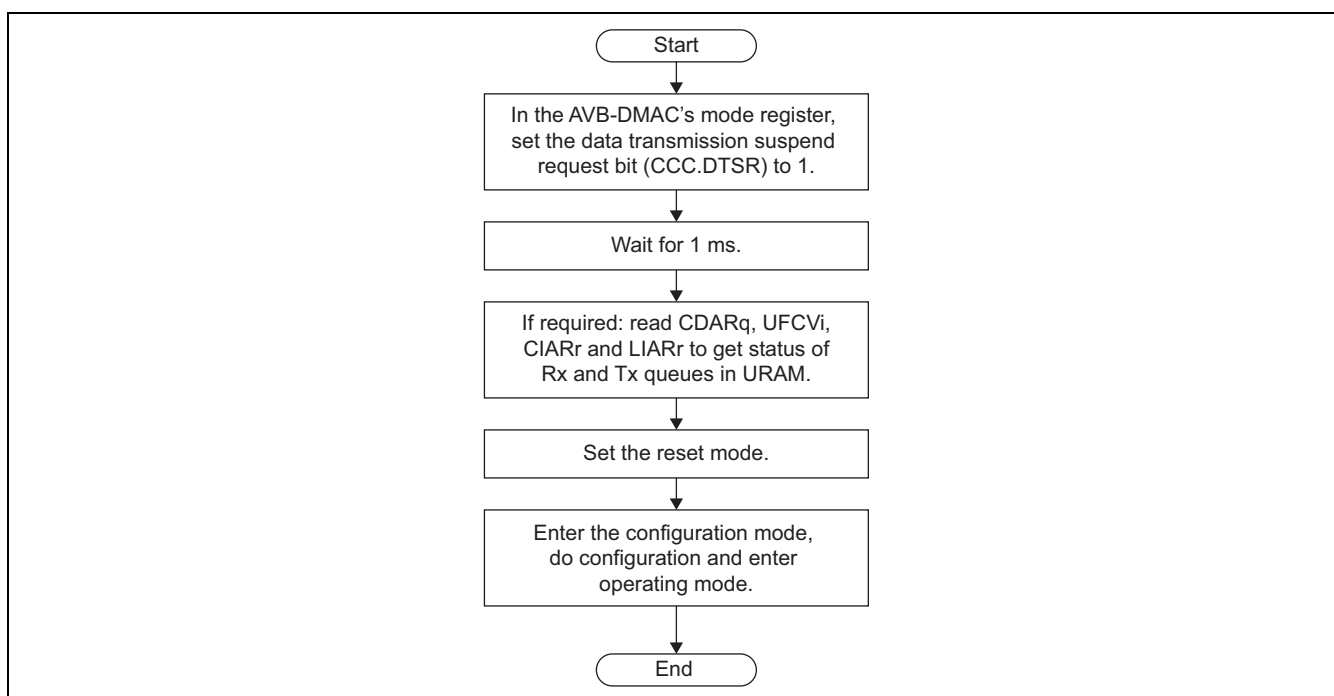
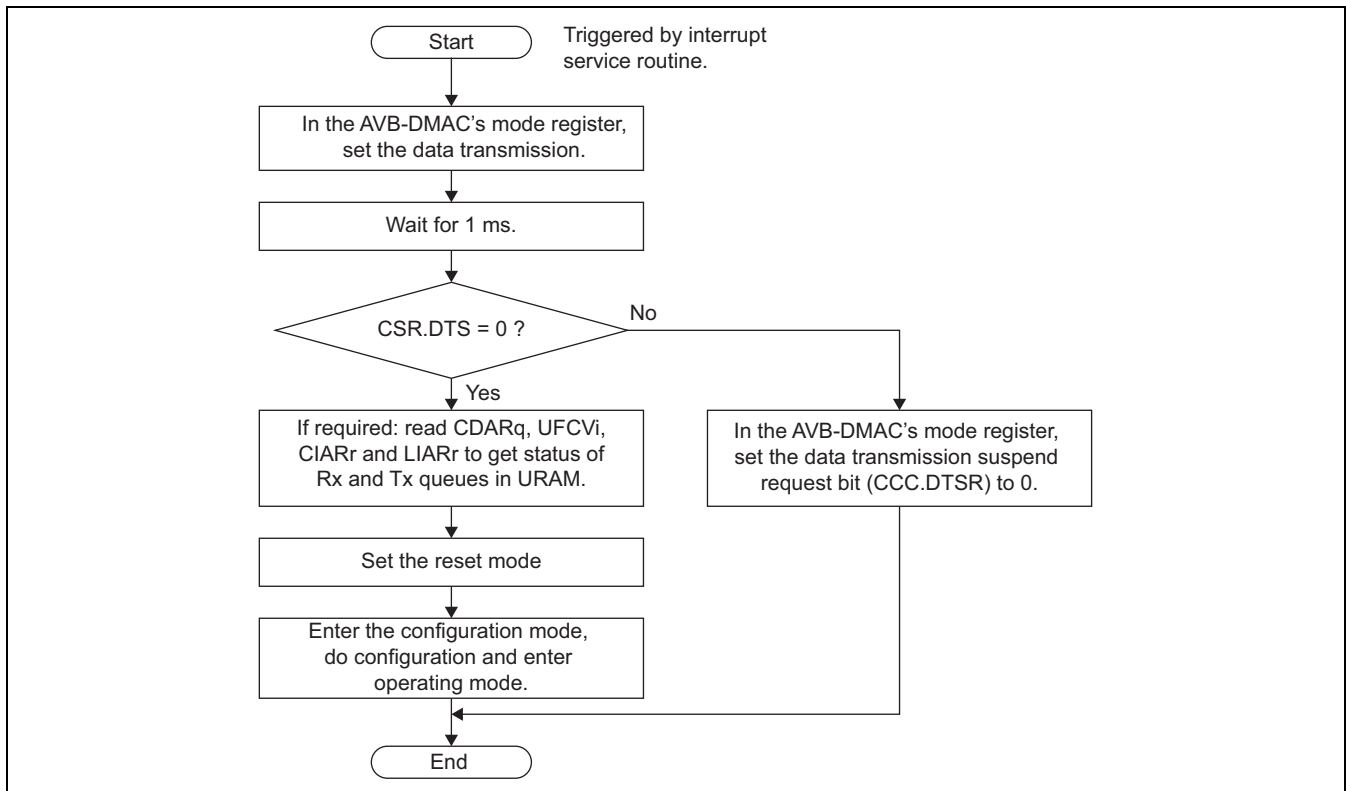


Figure 37A.78 Data Transfer Function Stop Flow1 after Read Access Error



**Figure 37A.79 Data Transfer Function Stop Flow2 after Read Access Error**

### 37A.3.14.3 Power Down Request

If EthernetAVB gets a power down request while writing to work RAM, it may happen that the request is not accepted even if the transfer is completed. Due to this the external power down module cannot complete the power down sequence.

A power down request is acceptable only when EthernetAVB is in RESET state.



### 37A.3.15 Notes

#### (1) Reception is Ignored when AVB\_RX\_ER from PHY is Flagged at 1st Data Byte

The issue is limited to reception of frames with physical faults. Flagging of occurrence in SFR is missing. When EthernetAVB is configured to store faulty frames in reception queue 0 (BE) by RCR.EFFS there is no storage.

#### (2) Unexpected Data are Exported when AVB\_RX\_ER is Flagged at 8th Data Byte

The issue is limited to reception of frames with physical faults.

Flagging of occurrence in SFR is invalid. When EthernetAVB is configured to store faulty frames in reception queue 0 (BE) by RCR.EFFS corrupted data is stored and MAC status code is wrong.

#### (3) Receive Frame Interrupt and Descriptor Interrupt may be Issued before Completion of Writing Data

When receive frame interrupt and descriptor interrupt are issued, whether writing data is completed by DESCR.DT in a descriptor can be confirmed.

And CDARq register has the descriptor address which EtherAVB is processing currently or is going to process at the next time.

The descriptors before one indicated by CDARq register are scope for receive frame interrupt and descriptor interrupt scope.

If there is a descriptor which wait for HW processing (ex. FEMPTY), it's delayed. Confirm the descriptor again after waiting for 1ms.

## 37B. Stream Buffer for EthernetAVB (STBE)

RZ/G1H	RZ/G1N
RZ/G1M	RZ/G1E

### 37B.1 Overview

The stream buffer for the EthernetAVB module (hereinafter referred to as STBE) incorporates a 16-Kbyte RAM for the EthernetAVB descriptors.

Using the STBE reduces the number of accesses to the DRAM and provides efficient access.

#### 37B.1.1 Features

- 1-, 2-, 4-, 8-, or 16-byte access is available for transfer.
- Transfer to/from the EthernetAVB is performed via the AXI bus using the following addresses:  
H'EE0E\_8000 to H'EE0E\_BFFF (16 Kbytes)

Note: For use of the EthernetAVB descriptors, refer to section 37A, EthernetAVB.

#### 37B.1.2 Block Diagram

Figure 37B.1 shows a block diagram of the STBE.

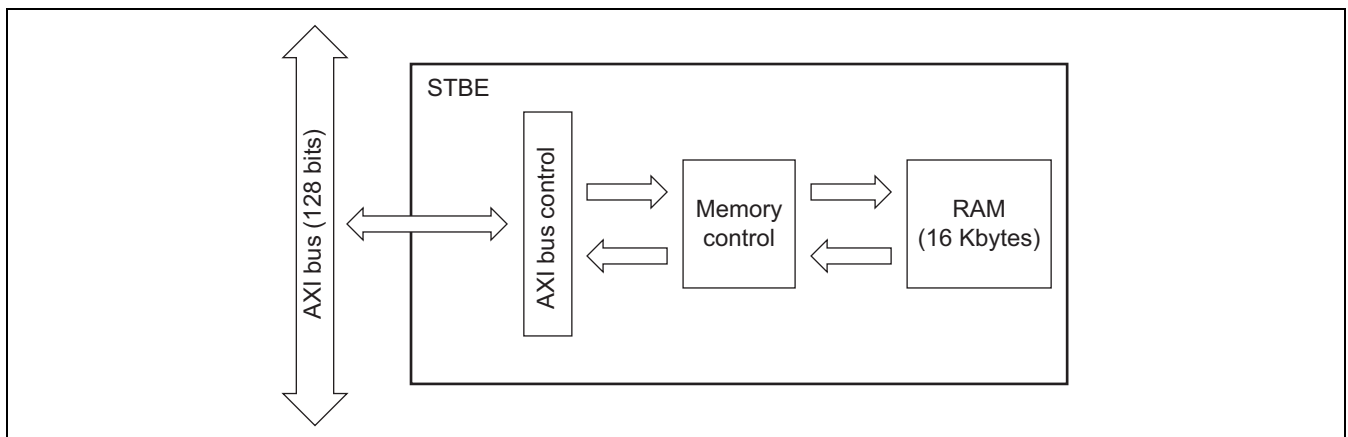


Figure 37B.1 Block Diagram

## 37B.2 Usage Notes

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

### 37B.2.1 Module Standby Mode

This module can be placed on module standby mode.

Ensure that this module is released from the module standby mode before using it.

### 37B.2.2 Transition to Module Standby Mode

1. Before stopping supply of the clock signal to this module, confirm that this module is not being accessed.
2. Set the relevant module stop control register in the clock pulse generator to stop supply of a clock signal to this module.

Note: Refer to section 7A, Module Standby and Software Reset, for the module stop control register.

### 37B.2.3 Release of Module Standby Mode and Restarting the STBE

Set the relevant module stop control register in the clock pulse generator to start supply of the clock signal to this module.

Note: Refer to section 7A, Module Standby and Software Reset, for the module stop control register.

## 38. Controller Area Network Interface (CAN interface)

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

### 38.1 Features

This MCU implements two channels (referred to as CAN0 and CAN1) of CAN (Controller Area Network) module that complies with the ISO11898-1 Specifications. The CAN module transmits and receives both formats of messages, namely the standard identifier (11 bits) (identifier hereafter referred to as ID) and extended ID (29 bits). Table 38.1 lists the CAN module overview and Figure 38.1 shows the CAN module block diagram. Connect the CAN bus transceiver externally.

**Table 38.1 CAN Module Overview**

Item	Overview
Protocol	<ul style="list-style-type: none"> <li>ISO11898-1 compliant</li> </ul>
Bit-rate	<ul style="list-style-type: none"> <li>Up to 1 Mbps</li> </ul>
Message box	<ul style="list-style-type: none"> <li>64 mailboxes: Two selectable mailbox mode Normal mailbox mode: Of the 64 mailboxes, 32 can be configured for either transmission or reception (and the other 32 are reception-only). FIFO mailbox mode: 24 mailboxes configurable as transmission or reception (and the other 32 are reception-only). 4 stages FIFO for transmission and 4 stages FIFO for reception</li> </ul>
Reception	<ul style="list-style-type: none"> <li>Data frame and remote frame can be received.</li> <li>Selectable receiving ID format (only standard ID, only extended ID or both ID)</li> <li>Programmable one-shot reception function</li> <li>Selectable overwrite mode (message overwritten) or overrun mode (message discarded)</li> <li>The reception complete interrupt can be enabled or disabled for each mailbox.</li> </ul>
Acceptance filter	<ul style="list-style-type: none"> <li>8 acceptance masks (one mask every 4 mailboxes)</li> <li>2 acceptance masks (one mask every 16 mailboxes)</li> <li>The mask can be enabled or disabled for each mailbox.</li> </ul>
Transmission	<ul style="list-style-type: none"> <li>Data frame and remote frame can be transmitted.</li> <li>Selectable transmitting ID format (only standard ID, only extended ID or both ID)</li> <li>Programmable one-shot transmission function (enable or disable)</li> <li>Selectable ID priority mode or mailbox number priority mode</li> <li>Transmission request can be aborted (The completion of abort can be confirmed with a flag.)</li> <li>The transmission complete interrupt can be enabled or disabled for each mailbox.</li> </ul>
Mode transition for bus-off recovery	<ul style="list-style-type: none"> <li>Mode transition for the recovery from the bus-off state can be selected: Automatic entry to CAN halt mode at bus-off entry Automatic entry to CAN halt mode at bus-off end Entry to CAN halt mode by a program Transition into error-active state by a program</li> </ul>
Error status monitoring	<ul style="list-style-type: none"> <li>CAN bus errors (stuff error, form error, ACK error, CRC error, bit error, and ACK delimiter error) can be monitored.</li> <li>Transition to error states can be detected (error-warning, error-passive, bus-off entry, and bus-off recovery).</li> <li>The error counters can be read.</li> </ul>

Item	Overview
Time stamp function	<ul style="list-style-type: none"> <li>• Time stamp function using a 16-bit counter</li> <li>• The reference clock can be selected from either 1-, 2-, 4- or 8-bit time periods.</li> </ul>
Interrupt sources	<ul style="list-style-type: none"> <li>• 5 types: <ul style="list-style-type: none"> <li>Reception complete</li> <li>Transmission complete</li> <li>Receive FIFO</li> <li>Transmit FIFO</li> <li>Error</li> </ul> </li> </ul>
CAN sleep mode	<ul style="list-style-type: none"> <li>• Current consumption can be reduced by stopping the CAN clock.</li> </ul>
Software support unit	<ul style="list-style-type: none"> <li>• 3 software support units: <ul style="list-style-type: none"> <li>Acceptance filter support</li> <li>Mailbox search support (receive mailbox search, transmit mailbox search and message lost search)</li> <li>Channel search support</li> </ul> </li> </ul>
CAN clock source (fCAN)	<ul style="list-style-type: none"> <li>• Peripheral clocks (clkp1 or clkp2) or externally input clock is selectable. clkp1 = P<math>\phi</math>, clkp2 =RCAN<math>\phi</math></li> </ul>
Test mode	<ul style="list-style-type: none"> <li>• 3 test modes available for user evaluation: <ul style="list-style-type: none"> <li>Listen-only mode</li> <li>Self-test mode 0 (external loop back)</li> <li>Self-test mode 1 (internal loop back)</li> </ul> </li> </ul>

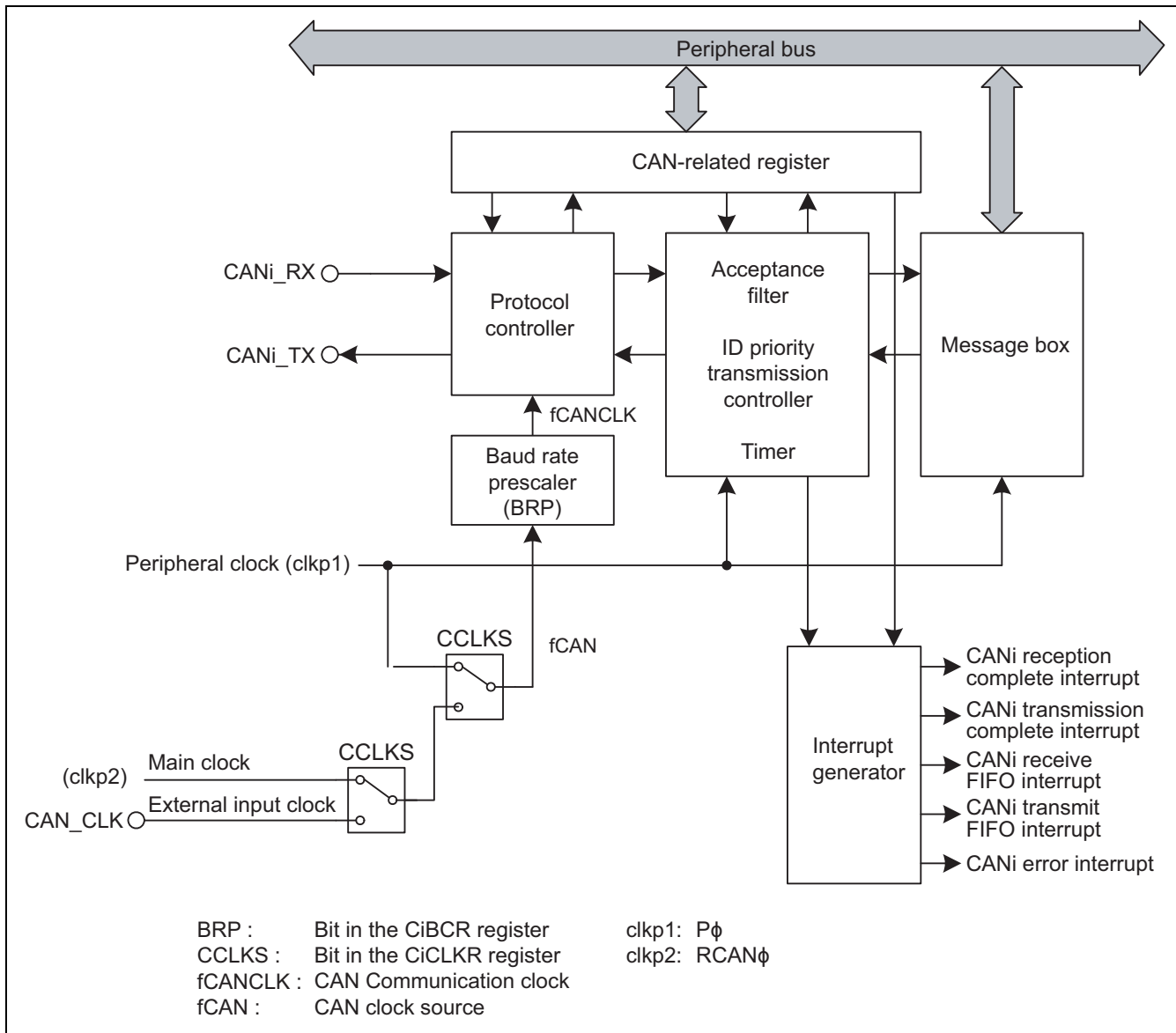


Figure 38.1 Block Diagram of CAN Module (i = 0, 1)

- CAN<sub>i</sub>\_RX/CAN<sub>i</sub>\_TX (i = 0 and 1):  
CAN input/output pins
- Protocol controller:  
Handles CAN protocol processing such as bus arbitration, bit timing at transmission and reception, stuffing, and error handling, etc.
- Message box:  
Consists of 64 mailboxes which can be configured as either transmit or receive mailboxes. Each mailbox has an individual ID, data length code, a data field (8 bytes), and a time stamp.
- Acceptance filter:  
Performs filtering of received messages. Registers CiMKR0 to CiMKR9 are used for the filtering process.
- Timer:  
Used for the time stamp function. The timer value when storing a message into the mailbox is written as the time stamp value.
- Interrupt generator:  
Generates the following five types of interrupts:  
CAN<sub>i</sub> reception complete interrupt  
CAN<sub>i</sub> transmission complete interrupt  
CAN<sub>i</sub> receive FIFO interrupt  
CAN<sub>i</sub> transmit FIFO interrupt  
CAN<sub>i</sub> error interrupt

## 38.2 Input/Output Pins

Table 38.2 shows the CAN module pin.

Pin switching is required for pins which are multiplexed with other functions. For details, see section 5, Pin Function Controller (PFC).

**Table 38.2 Pin Configuration**

Pin Name	I/O	Function	RZ/G Series Products			
			RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
CAN <sub>i</sub> _RX	Input	Pins for receiving data	√	√	√	√
CAN <sub>i</sub> _TX	Output	Pins for transmitting data	√	√	√	√
CAN_CLK	Input	Input pin used for external clock input.	√	√	√	√

Legend: i = 0 and 1

## 38.3 Register Descriptions

**Table 38.3 Register Configuration**

Register Name	Symbol	R/W	Value after Reset	Address	Access Size	RZ/G Series Products			
						RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
CAN0 Control Register	COCTRL	R/W	H'0500	H'E6E80840	8, 16	√	√	√	√

						RZ/G Series Products			
Register Name	Symbol	R/W	Value after Reset	Address	Access Size	RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
CAN0 Clock Select Register	C0CLKR	R/W	H'00	H'E6E80847	8	√	√	√	√
CAN0 Bit Configuration Register	C0BCR	R/W	H'00 0000	H'E6E80844	8, 16, 32	√	√	√	√
CAN0 Mask Register 0	C0MKR0	R/W	Undefined	H'E6E80430	8, 16, 32	√	√	√	√
CAN0 Mask Register 1	C0MKR1	R/W	Undefined	H'E6E80434	8, 16, 32	√	√	√	√
CAN0 Mask Register 2	C0MKR2	R/W	Undefined	H'E6E80400	8, 16, 32	√	√	√	√
CAN0 Mask Register 3	C0MKR3	R/W	Undefined	H'E6E80404	8, 16, 32	√	√	√	√
CAN0 Mask Register 4	C0MKR4	R/W	Undefined	H'E6E80408	8, 16, 32	√	√	√	√
CAN0 Mask Register 5	C0MKR5	R/W	Undefined	H'E6E8040C	8, 16, 32	√	√	√	√
CAN0 Mask Register 6	C0MKR6	R/W	Undefined	H'E6E80410	8, 16, 32	√	√	√	√
CAN0 Mask Register 7	C0MKR7	R/W	Undefined	H'E6E80414	8, 16, 32	√	√	√	√
CAN0 Mask Register 8	C0MKR8	R/W	Undefined	H'E6E80418	8, 16, 32	√	√	√	√
CAN0 Mask Register 9	C0MKR9	R/W	Undefined	H'E6E8041C	8, 16, 32	√	√	√	√
CAN0 FIFO Received ID Compare Register 0	C0FIDCR0	R/W	Undefined	H'E6E80420	8, 16, 32	√	√	√	√
CAN0 FIFO Received ID Compare Register 1	C0FIDCR1	R/W	Undefined	H'E6E80424	8, 16, 32	√	√	√	√
CAN0 Mask Invalid Register 0	C0MKIVLR0	R/W	Undefined	H'E6E80438	8, 16, 32	√	√	√	√
CAN0 Mask Invalid Register 1	C0MKIVLR1	R/W	Undefined	H'E6E80428	8, 16, 32	√	√	√	√
CAN0 Mailbox Register 0 to 63	C0MB0 to C0MB63	R/W	Undefined	H'E6E80000 to H'E6E803FF	8, 16, 32	√	√	√	√
CAN0 Mailbox Interrupt Enable Register 0	C0MIER0	R/W	Undefined	H'E6E8043C	8, 16, 32	√	√	√	√
CAN0 Mailbox Interrupt Enable Register 1	C0MIER1	R/W	Undefined	H'E6E8042C	8, 16, 32	√	√	√	√
CAN0 Message Control Register 0 to 63	C0MCTL0 to C0MCTL63	R/W	H'00	H'E6E80800 to H'E6E8083F	8	√	√	√	√
CAN0 Receive FIFO Control Register	C0RFCR	R/W	H'80	H'E6E80848	8	√	√	√	√
CAN0 Receive FIFO Pointer Control Register	C0RFPCR	R/W	Undefined	H'E6E80849	8	√	√	√	√
CAN0 Transmit FIFO Control Register	C0TFCR	R/W	H'80	H'E6E8084A	8	√	√	√	√
CAN0 Transmit FIFO Pointer Control Register	C0TFPCR	R/W	Undefined	H'E6E8084B	8	√	√	√	√
CAN0 Status Register	C0STR	R	H'0500	H'E6E80842	8, 16	√	√	√	√
CAN0 Mailbox Search Mode Register	C0MSMR	R/W	H'00	H'E6E80853	8	√	√	√	√
CAN0 Mailbox Search Status Register	C0MSSR	R	H'80	H'E6E80852	8	√	√	√	√
CAN0 Channel Search Support Register	C0CSSR	R/W	Undefined	H'E6E80851	8	√	√	√	√



						RZ/G Series Products			
Register Name	Symbol	R/W	Value after Reset	Address	Access Size	RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
CAN0 Acceptance Filter Support Register	C0AFSR	R/W	Undefined	H'E6E80856	8, 16	√	√	√	√
CAN0 Error Interrupt Enable Register	C0EIER	R/W	H'00	H'E6E8084C	8	√	√	√	√
CAN0 Error Interrupt Factor Judge Register	C0EIFR	R/W	H'00	H'E6E8084D	8	√	√	√	√
CAN0 Receive Error Count Register	C0RECR	R	H'00	H'E6E8084E	8	√	√	√	√
CAN0 Transmit Error Count Register	C0TECR	R	H'00	H'E6E8084F	8	√	√	√	√
CAN0 Error Code Store Register	C0ECSR	R/W	H'00	H'E6E80850	8	√	√	√	√
CAN0 Time Stamp Register	C0TSR	R	H'0000	H'E6E80854	8, 16	√	√	√	√
CAN0 Test Control Register	C0TCR	R/W	H'00	H'E6E80858	8	√	√	√	√
CAN0 Interrupt Enable Register	C0IER	R/W	H'00	H'E6E80860	8	√	√	√	√
CAN0 Interrupt Status Register	C0ISR	R/W	H'00	H'E6E80861	8	√	√	√	√
CAN0 Mailbox Search Mask Register	C0MBSMR	R/W	H'00	H'E6E80863	8	√	√	√	√
CAN1 Control Register	C1CTLR	R/W	H'0500	H'E6E88840	8, 16	√	√	√	√
CAN1 Clock Select Register	C1CLKR	R/W	H'00	H'E6E88847	8	√	√	√	√
CAN1 Bit Configuration Register	C1BCR	R/W	H'00 0000	H'E6E88844	8, 16, 32	√	√	√	√
CAN1 Mask Register 0	C1MKR0	R/W	Undefined	H'E6E88430	8, 16, 32	√	√	√	√
CAN1 Mask Register 1	C1MKR1	R/W	Undefined	H'E6E88434	8, 16, 32	√	√	√	√
CAN1 Mask Register 2	C1MKR2	R/W	Undefined	H'E6E88400	8, 16, 32	√	√	√	√
CAN1 Mask Register 3	C1MKR3	R/W	Undefined	H'E6E88404	8, 16, 32	√	√	√	√
CAN1 Mask Register 4	C1MKR4	R/W	Undefined	H'E6E88408	8, 16, 32	√	√	√	√
CAN1 Mask Register 5	C1MKR5	R/W	Undefined	H'E6E8840C	8, 16, 32	√	√	√	√
CAN1 Mask Register 6	C1MKR6	R/W	Undefined	H'E6E88410	8, 16, 32	√	√	√	√
CAN1 Mask Register 7	C1MKR7	R/W	Undefined	H'E6E88414	8, 16, 32	√	√	√	√
CAN1 Mask Register 8	C1MKR8	R/W	Undefined	H'E6E88418	8, 16, 32	√	√	√	√
CAN1 Mask Register 9	C1MKR9	R/W	Undefined	H'E6E8841C	8, 16, 32	√	√	√	√
CAN1 FIFO Received ID Compare Register 0	C1FIDCR0	R/W	Undefined	H'E6E88420	8, 16, 32	√	√	√	√
CAN1 FIFO Received ID Compare Register 1	C1FIDCR1	R/W	Undefined	H'E6E88424	8, 16, 32	√	√	√	√
CAN1 Mask Invalid Register 0	C1MKIVLR0	R/W	Undefined	H'E6E88438	8, 16, 32	√	√	√	√
CAN1 Mask Invalid Register 1	C1MKIVLR1	R/W	Undefined	H'E6E88428	8, 16, 32	√	√	√	√

						RZ/G Series Products			
Register Name	Symbol	R/W	Value after Reset	Address	Access Size	RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
CAN1 Mailbox Register 0 to 63	C1MB0 to C1MB63	R/W	Undefined	H'E6E88000 to H'E6E883FF	8, 16, 32	√	√	√	√
CAN1 Mailbox Interrupt Enable Register 0	C1MIER0	R/W	Undefined	H'E6E8843C	8, 16, 32	√	√	√	√
CAN1 Mailbox Interrupt Enable Register 1	C1MIER1	R/W	Undefined	H'E6E8842C	8, 16, 32	√	√	√	√
CAN1 Message Control Register 0 to 63	C1MCTL0 to C1MCTL63	R/W	H'00	H'E6E88800 to H'E6E8883F	8	√	√	√	√
CAN1 Receive FIFO Control Register	C1RFCR	R/W	H'80	H'E6E88848	8	√	√	√	√
CAN1 Receive FIFO Pointer Control Register	C1RFPCR	R/W	Undefined	H'E6E88849	8	√	√	√	√
CAN1 Transmit FIFO Control Register	C1TFCR	R/W	H'80	H'E6E8884A	8	√	√	√	√
CAN1 Transmit FIFO Pointer Control Register	C1TFPCR	R/W	Undefined	H'E6E8884B	8	√	√	√	√
CAN1 Status Register	C1STR	R	H'0500	H'E6E88842	8, 16	√	√	√	√
CAN1 Mailbox Search Mode Register	C1MSMR	R/W	H'00	H'E6E88853	8	√	√	√	√
CAN1 Mailbox Search Status Register	C1MSSR	R	H'80	H'E6E88852	8	√	√	√	√
CAN1 Channel Search Support Register	C1CSSR	R/W	Undefined	H'E6E88851	8	√	√	√	√
CAN1 Acceptance Filter Support Register	C1AFSR	R/W	Undefined	H'E6E88856	8, 16	√	√	√	√
CAN1 Error Interrupt Enable Register	C1EIER	R/W	H'00	H'E6E8884C	8	√	√	√	√
CAN1 Error Interrupt Factor Judge Register	C1EIFR	R/W	H'00	H'E6E8884D	8	√	√	√	√
CAN1 Receive Error Count Register	C1RECR	R	H'00	H'E6E8884E	8	√	√	√	√
CAN1 Transmit Error Count Register	C1TECR	R	H'00	H'E6E8884F	8	√	√	√	√
CAN1 Error Code Store Register	C1ECSR	R/W	H'00	H'E6E88850	8	√	√	√	√
CAN1 Time Stamp Register	C1TSR	R	H'0000	H'E6E88854	8, 16	√	√	√	√
CAN1 Test Control Register	C1TCR	R/W	H'00	H'E6E88858	8	√	√	√	√
CAN1 Interrupt Enable Register	C1IER	R/W	H'00	H'E6E88860	8	√	√	√	√
CAN1 Interrupt Status Register	C1ISR	R/W	H'00	H'E6E88861	8	√	√	√	√
CAN1 Mailbox Search Mask Register	C1MBSMR	R/W	H'00	H'E6E88863	8	√	√	√	√

**Legend:**

Initial value: Register value after a reset

—: Undefined value

R/W: Readable/writable. The written value can be read.

R/WC0: Readable/writable. Writing 0 initializes the bit. Writing 1 is ignored.

R: Read-only. When writing to the register, read out the value of these bits and write it back without alteration.

W: Write-only. The read value is undefined.

**38.3.1 CANi Control Register (CiCTLR) (i = 0, 1)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CAN0 Control Register (C0CTLR)

CAN1 Control Register (C1CTLR)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	RBOC	BOM	SLPM	CANM	TSPS	TSRC	TPM	MLM	IDFM	MBM				
Initial value:	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

<After Reset: H'0500>

Bit	Symbol	Initial Value	R/W	Description
15, 14	—	All 0	R	Reserved bits These bits are always read as 0. The write value should always be 0. Operation is not guaranteed if a value other than 0 is written to these bits.
13	RBOC	0	R/W	Forcible Return From Bus-OFF Bit*1 When the RBOC bit is set to "1" (forcible return from bus-off) in bus-off state, the CAN module forcibly returns from the bus-off state. This bit is automatically set to 0. The error state changes from bus-off to error-active. When the RBOC bit is set to "1", registers CiRECR and CiTECR are set to "H'00" and the BOST bit in the CiSTR register is set to "0" (the CAN module is not in bus-off state). The other registers remain unchanged. No bus-off recovery interrupt request is generated by this recovery from the bus-off state. Use the RBOC bit only when the BOM bit = "00" (normal mode). 0: Nothing occurred 1: Forcible return from bus-off*2

Bit	Symbol	Initial Value	R/W	Description
12, 11	BOM	All 0	R/W	<p>Bus-Off Recovery Mode Bit*<sup>3</sup></p> <p>The BOM bit is used to select bus-off recovery mode.</p> <p>When the BOM bit is "00", the recovery from bus-off is compliant with ISO11898-1, i.e. the CAN module re-enters CAN communication (error-active state) after detecting 11 consecutive recessive bits 128 times. A bus-off recovery interrupt request is generated when recovering from bus-off.</p> <p>When the BOM bit is "01", as soon as the CAN reaches the bus-off state, the CANM bit in the CiCTRL register is set to "10" (CAN halt mode) and the CAN enters CAN halt mode. No bus-off recovery interrupt request is generated when recovering from bus-off and registers CiTECR and CiRECR are set to "H'00".</p> <p>When the BOM bit is "10", the CANM bit is set to 10b as soon as the CAN module reaches the bus-off state. The CAN module enters CAN halt mode after the recovery from the bus-off state, i.e. after detecting 11 consecutive recessive bits 128 times. A bus-off recovery interrupt request is generated when recovering from bus-off and registers CiTECR and CiRECR are set to "H'00".</p> <p>When the BOM bit is "11", the CAN module enters CAN halt mode by setting the CANM bit to "10" while the CAN module is still in bus-off state. No bus-off recovery interrupt request is generated when recovering from bus-off and registers CiTECR and CiRECR are set to "H'00". However, if the CAN module recovers from bus-off after detecting 11 consecutive recessive bits 128 times before the CANM bit is set to "10", a bus-off recovery interrupt request is generated.</p> <p>If the CPU requests an entry to CAN reset mode at the same time as the CAN module attempts to enter CAN halt mode (at bus-off entry when the BOM bit is "01", or at bus-off end when the BOM bit is "10"), then the CPU request to enter CAN reset mode has higher priority.</p> <p>00: Normal mode (ISO11898-1 compliant)  01: Entry to CAN halt mode automatically at bus-off entry  10: Entry to CAN halt mode automatically at bus-off end  11: Entry to CAN halt mode (during bus-off recovery period) by a program request</p>
10	SLPM	1	R/W	<p>CAN Sleep Mode Bit*<sup>4,5</sup></p> <p>When the SLPM bit is set to "1", the CAN module enters CAN sleep mode.</p> <p>When the SLPM bit is set to "0", the CAN module exits CAN sleep mode. Refer to section 38.4, Operating Mode for detail.</p> <p>0: Other than CAN sleep mode  1: CAN sleep mode</p>
9, 8	CANM	01	R/W	<p>CAN Operating Mode Select Bit*<sup>4</sup></p> <p>The CANM bit selects one of the following modes for the CAN module: CAN operation mode, CAN reset mode or CAN halt mode. Refer to section 38.4, Operating Mode for detail. CAN sleep mode is set by the SLPM bit.</p> <p>When the CAN module enters CAN halt mode according to the setting of the BOM bit, the CANM bit is automatically set to "10".</p> <p>00: CAN operation mode  01: CAN reset mode  10: CAN halt mode  11: CAN reset mode (forcible transition)</p>

Bit	Symbol	Initial Value	R/W	Description
7, 6	TSPS	All 0	R/W	<p>Time Stamp Prescaler Select Bit*<sup>3</sup></p> <p>The TSPS bit selects the prescaler for the time stamp. The reference clock for the time stamp can be selected to be either 1-, 2-, 4- or 8-bit time periods.</p> <p>00: Every bit time 01: Every 2-bit time 10: Every 4-bit time 11: Every 8-bit time</p>
5	TSRC	0	R/W	<p>Time Stamp Counter Reset Command Bit*<sup>6</sup></p> <p>The TSRC bit is used to reset the time stamp counter. When the TSRC bit is set to "1", the CiTSR register is set to H'0000. It is automatically set to 0.</p> <p>0: Nothing occurred 1: Reset*<sup>2</sup></p>
4	TPM	0	R/W	<p>Transmission Priority Mode Select Bit*<sup>3</sup></p> <p>The TPM bit specifies the priority of modes when transmitting messages. ID priority transmit mode or mailbox number transmit mode can be selected.</p> <p>All mailboxes are set for either ID priority transmission or mailbox number priority transmission.</p> <p>When the TPM bit is 0, ID priority transmit mode is selected and transmission priority complies with the CAN bus arbitration rule, as defined in the ISO 11898-1 Specifications. In ID priority transmit mode, mailboxes [0] to [63] (in normal mailbox mode), and mailboxes [0] to [55] (in FIFO mailbox mode), and the transmit FIFO are compared for the IDs of mailboxes configured for transmission. If two or more mailbox IDs are the same, the mailbox with the smaller number has higher priority.</p> <p>Only the next message to be transmitted from the transmit FIFO is included in the transmission arbitration. If a transmit FIFO message is being transmitted, the next pending message within the transmit FIFO is included in the transmission arbitration.</p> <p>When the TPM bit is 1, mailbox number transmit mode is selected and the transmit mailbox with the smallest mailbox number has the highest priority. In FIFO mailbox mode, the transmit FIFO has lower priority than normal mailboxes (mailboxes [0] to [55]).</p> <p>0: ID priority transmit mode 1: Mailbox number priority transmit mode</p>
3	MLM	0	R/W	<p>Message Lost Mode Select Bit*<sup>3</sup></p> <p>The MLM bit specifies the operation when a new message is captured in the unread mailbox.</p> <p>Overwrite mode or overrun mode can be selected. All mailboxes (including the receive FIFO) are set to either overwrite mode or overrun mode.</p> <p>When the MLM bit is "0", all mailboxes are set to overwrite mode and the new message is overwriting the old message.</p> <p>When this bit is "1", all mailboxes are set to overrun mode and the new message is discarded.</p> <p>0: Overwrite mode 1: Overrun mode</p>

Bit	Symbol	Initial Value	R/W	Description
2, 1	IDFM	All 0	R/W	<p>ID Format Mode Select Bit*<sup>3</sup></p> <p>The IDFM bit specifies the ID format.</p> <p>00: Standard ID mode All mailboxes (including FIFO mailboxes) handle only standard IDs.</p> <p>01: Extended ID mode All mailboxes (including FIFO mailboxes) handle only extended IDs.</p> <p>10: Mixed ID mode All mailboxes (including FIFO mailboxes) handle both standard IDs and extended IDs. Standard IDs or extended IDs are specified by using the IDE bit in the corresponding mailbox in normal mail box mode. In FIFO mailbox mode, the IDE bit in the corresponding mailbox is used for mailboxes [0] to [55], the IDE bit in registers CiFIDCR0 and CiFIDCR1 is used for the receive FIFO, and the IDE bit in mailbox [56] is used for the transmit FIFO.</p> <p>11: Do not use this combination</p>
0	MBM	0	R/W	<p>CAN Mailbox Mode Select Bit*<sup>3</sup></p> <p>When the MBM bit is "0" (normal mailbox mode), mailboxes [0] to [63] are configured as transmit or receive mailboxes. When the MBM bit is "1" (FIFO mailbox mode), mailboxes [0] to [55] are configured as transmit or receive mailboxes. Mailboxes [56] to [59] are configured as a transmit FIFO and mailboxes [60] to [63] as a receive FIFO.</p> <p>Transmit data is written into mailbox [56] (mailbox [56] is a window mailbox for the transmit FIFO).</p> <p>Receive data is read from mailbox [60] (mailbox [60] is a window mailbox for the receive FIFO).</p> <p>Table 38.4 lists the Mailbox Configuration.</p> <p>0: Normal mailbox mode 1: FIFO mailbox mode</p>

- Notes:
1. Set the RBOC bit to "1" in bus-off state.
  2. Bits RBOC and TSRC are automatically set back to "0" after being set to "1". It should be read as "0".
  3. Write to bits BOM, MBM, IDFM, MLM, TPM, and TSPS in CAN reset mode.
  4. When bits CANM and SLPM are changed, check the CiSTR register to ensure that the mode has been switched.
  5. Write to the SLPM bit in CAN reset mode or CAN halt mode. When rewriting the SLPM bit, set only this bit to "0" or "1".
  6. Set the TSRC bit to "1" in CAN operation mode.

**Table 38.4 Mailbox Configuration**

Mailbox	MBM Bit = "0" (Normal mailbox mode)	MBM Bit = "1" (FIFO mailbox mode)
Mailboxes [0] to [55]	Normal mailbox	Normal mailbox
Mailboxes [56] to [59]		Transmit FIFO
Mailboxes [60] to [63]		Receive FIFO

Notes: Points 1 to 5 below should be considered when the MBM bit is set to "1".

1. Transmit FIFO is controlled by the CiTFCR register.  
The CiMCTLj register of mailboxes [56] to [59] are disabled.  
Registers CiMCTL56 to CiMCTL59 cannot be used.
2. Receive FIFO is controlled by the CiRFCR register.  
The CiMCTLj register of mailboxes [60] to [63] are disabled.  
Registers CiMCTL60 to CiMCTL63 cannot be used.
3. Refer to the CiMIER1 register about the FIFO interrupts.
4. The corresponding bits in the CiMKIVLR register for mailboxes [56] to [63] are disabled. Set 0 to these bits.
5. Transmit/receive FIFOs can be used for both data frames and remote frames.

### 38.3.2 CANi Clock Select Register (CiCLKR) (i = 0, 1)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CAN0 Clock Select Register (C0CLKR)

CAN1 Clock Select Register (C1CLKR)

Bit:	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	CCLKS	
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W

<After Reset: H'00>

Bit	Symbol	Initial Value	R/W	Description
7 to 2	—	All 0	R	Reserved bits These bits are always read as 0. The write value should always be 0. Operation is not guaranteed if a value other than 0 is written to these bits.
1, 0	CCLKS	0	R/W	CAN Clock Source Select Bits* The CCLKS bits select clock source from among the peripheral clock (clkp1 or clkp2) generated by the PLL frequency synthesizer, and an externally input clock. 00: Peripheral clock (clkp1) 01: Peripheral clock (clkp2) 10: Illegal value 11: Externally input clock

Note: \* Write to the CCLKS bit in CAN reset mode.



**38.3.3 CANi Bit Configuration Register (CiBCR) (i = 0, 1)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

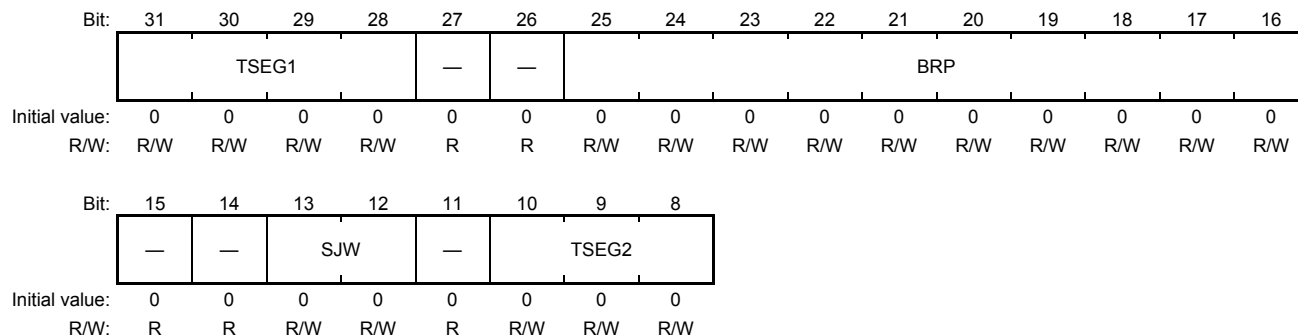
For the bit timing configuration rule, refer to section 38.5, CAN Communication Speed Configuration.

Set the CiBCR register before entering CAN halt mode from CAN reset mode or CAN operation mode from CAN reset mode. After the setting is made once, this register can be written to in CAN reset mode or CAN halt mode.

The CiBCR register consists of 24 bits. A 32-bit read/write access should be performed carefully not to rewrite the CiCLKR register.

CAN0 Bit Configuration Register (C0BCR)

CAN1 Bit Configuration Register (C1BCR)



<After Reset: H'000000>

Bit	Symbol	Initial Value	R/W	Description
31 to 28	TSEG1	All 0	R/W	<p>Time Segment 1 Control Bits</p> <p>The TSEG1 bit is used to specify the total length of the propagation time segment (PROP_SEG) and phase buffer segment 1 (PHASE_SEG1) with the value of Tq.</p> <p>A value from 4 to 16 time quanta can be set.</p> <p>0000: Do not use this combination</p> <p>0001: Do not use this combination</p> <p>0010: Do not use this combination</p> <p>0011: 4 Tq</p> <p>0100: 5 Tq</p> <p>0101: 6 Tq</p> <p>0110: 7 Tq</p> <p>0111: 8 Tq</p> <p>1000: 9 Tq</p> <p>1001: 10 Tq</p> <p>1010: 11 Tq</p> <p>1011: 12 Tq</p> <p>1100: 13 Tq</p> <p>1101: 14 Tq</p> <p>1110: 15 Tq</p> <p>1111: 16 Tq</p>

Bit	Symbol	Initial Value	R/W	Description
27, 26	—	All 0	R	Reserved bits These bits are always read as 0. The write value should always be 0. Operation is not guaranteed if a value other than 0 is written to these bits.
25 to 16	BRP	All 0	R/W	Prescaler Division Ratio Set Bits The BRP bit is used to set the peripheral bus clock periods contained in a Time Quantum. If the setting value is P (0 to 1023), the baud rate prescaler divides fCAN by P + 1.
15, 14	—	All 0	R	Reserved bits These bits are always read as 0. The write value should always be 0. Operation is not guaranteed if a value other than 0 is written to these bits.
13, 12	SJW	All 0	R/W	Resynchronization Jump Width Control Bits The SJW bit is used to specify the resynchronization jump width with the value of Tq. A value from 1 to 4 time quanta can be set. Set the value smaller than or equal to that of the TSEG2 bit. 00: 1 Tq 01: 2 Tq 10: 3 Tq 11: 4 Tq
11	—	0	R	Reserved bit This bit is always read as 0. The write value should always be 0. Operation is not guaranteed if a value other than 0 is written to this bit.
10 to 8	TSEG2	All 0	R/W	Time Segment 2 Control Bits The TSEG2 bit is used to specify the length of phase buffer segment 2 (PHASE_SEG2) with the value of Tq. A value from 2 to 8 time quanta can be set. Set the value smaller than that of the TSEG1 bit. 000: Do not use this combination 001: 2 Tq 010: 3 Tq 011: 4 Tq 100: 5 Tq 101: 6 Tq 110: 7 Tq 111: 8 Tq

### 38.3.4 CANi Mask Register k (CiMKRk) (i = 0, 1; k = 0 to 9)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

For masking the function in FIFO mailbox mode, refer to section 38.7, Acceptance Filtering and Masking Function.

Write to registers CiMKR0 to CiMKR9 in CAN reset mode or CAN halt mode.

CAN0 Mask Register 0 (C0MKR0)

CAN0 Mask Register 1 (C0MKR1)

CAN0 Mask Register 2 (C0MKR2)

:

CAN0 Mask Register 9 (C0MKR9)

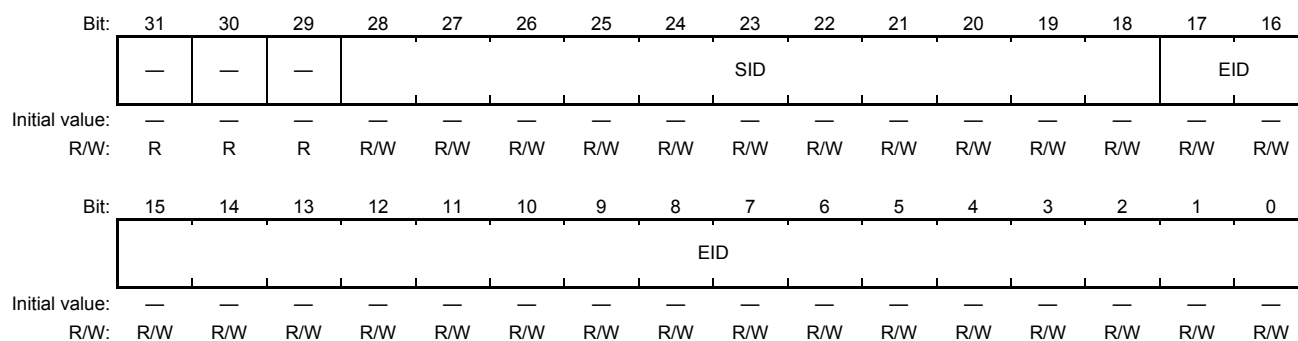
CAN1 Mask Register 0 (C1MKR0)

CAN1 Mask Register 1 (C1MKR1)

CAN1 Mask Register 2 (C1MKR2)

:

CAN1 Mask Register 9 (C1MKR9)



<After Reset: Undefined>

Bit	Symbol	Initial Value	R/W	Description
31 to 29	—	Undefined	R	Reserved bits The reset value is undefined. The write value should be "0". These bits are read as "0" after "0" is written to.
28 to 18	SID	Undefined	R/W	Standard ID Bits The SID bit is the filter mask bit corresponding to the CAN standard ID bit. The SID bit is used to receive both standard ID and extended ID messages. When the SID bit is set to "0", the corresponding SID bit is not compared for the received ID and the mailbox ID. When the SID bit is set to "1", corresponding SID bit compares received ID with mailbox ID. 0: Corresponding SID bit is not compared 1: Corresponding SID bit is compared

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Bit	Symbol	Initial Value	R/W	Description
17 to 0	EID	Undefined	R/W	<p>Extended ID Bits</p> <p>The EID bit is the filter mask bit for CAN extended ID bit.</p> <p>This bit is used to receive extended ID messages.</p> <p>When the EID bit is set to "0", corresponding EID bit does not compare received ID with mailbox ID.</p> <p>When the EID bit is set to "1", corresponding EID bit compares received ID with mailbox ID.</p> <p>0: Corresponding EID bit is not compared</p> <p>1: Corresponding EID bit is compared</p>

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### 38.3.5 CANi FIFO Received ID Compare Registers (CiFIDCR0 and CiFIDCR1) (i = 0, 1)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Registers CiFIDCR0 and CiFIDCR1 are enabled when the MBM bit in the CiCTLR register is set to "1" (FIFO mailbox mode). Bits EID, SID, RTR, and IDE in registers CiMB60 to CiMB63 are disabled.

For the usage of these registers, refer to section 38.7, Acceptance Filtering and Masking Function.

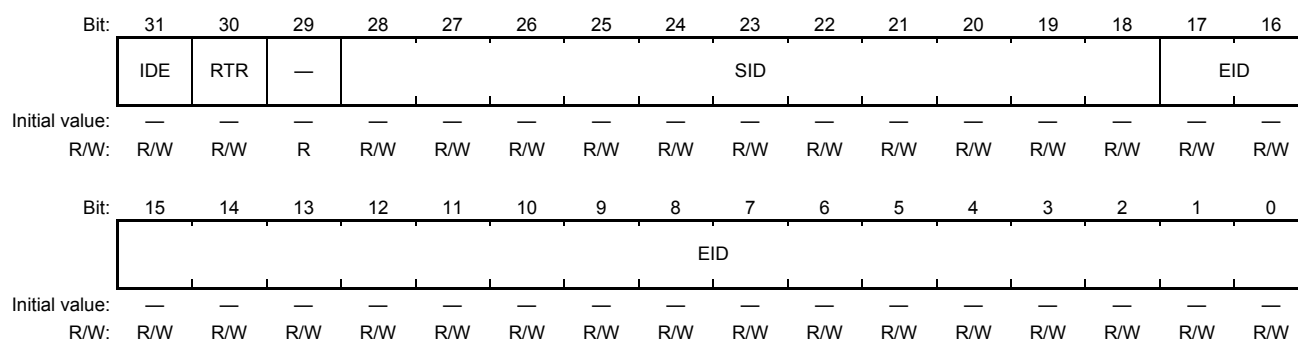
Write to registers CiFIDCR0 and CiFIDCR1 in CAN reset mode or CAN halt mode.

CAN0 FIFO Received ID Compare Register 0 (C0FIDCR0)

CAN0 FIFO Received ID Compare Register 1 (C0FIDCR1)

CAN1 FIFO Received ID Compare Register 0 (C1FIDCR0)

CAN1 FIFO Received ID Compare Register 1 (C1FIDCR1)



<After Reset: Undefined>

Bit	Symbol	Initial Value	R/W	Description
31	IDE	Undefined	R/W	<p>ID Extension Bit*</p> <p>The IDE bit sets the ID format to standard ID or extended ID. The IDE bit is enabled when the IDFM bit in the CiCTLR register is "10" (mixed ID mode). When the IDFM bit is "10", the IDE bit specifies the following operation.</p> <p>When both IDE bits in registers CiFIDCR0 and CiFIDCR1 are set to "0", only standard ID frames can be received.</p> <p>When both IDE bits in registers CiFIDCR0 and CiFIDCR1 are set to "1", only extended ID frames can be received.</p> <p>When the IDE bits in registers CiFIDCR0 and CiFIDCR1 are set to "0" or "1" individually, both standard ID and extended ID frames can be received.</p> <p>0: Standard ID 1: Extended ID</p>

Bit	Symbol	Initial Value	R/W	Description
30	RTR	Undefined	R/W	<p>Remote Transmission Request Bit</p> <p>The RTR bit sets the specified frames format of data frame or remote frames. The RTR bit specifies the following operation.</p> <p>When both RTR bits in registers CiFIDCR0 and CiFIDCR1 are set to "0", only data frames can be received.</p> <p>When both RTR bits in registers CiFIDCR0 and CiFIDCR1 are set to "1", only remote frames can be received.</p> <p>When the RTR bits in registers CiFIDCR0 and CiFIDCR1 are set to "0" or "1" individually, both data frames and remote frames can be received.</p> <p>0: Data frame 1: Remote frame</p>
29	—	Undefined	R	<p>Reserved bit</p> <p>The reset value is undefined. The write value should be "0". This bit is read as "0" after "0" is written to.</p>
28 to 18	SID	Undefined	R/W	<p>Standard ID Bits</p> <p>The SID bit sets the standard ID of data frames and remote frames. The SID bit is used to receive both standard ID and extended ID messages.</p> <p>0: Corresponding SID bit is "0" 1: Corresponding SID bit is "1"</p>
17 to 0	EID	Undefined	R/W	<p>Extended ID Bits</p> <p>The EID bit sets the extended ID of data frames and remote frames. The EID bit is used to receive extended ID messages.</p> <p>0: Corresponding EID bit is "0" 1: Corresponding EID bit is "1"</p>

Note: \* When the IDFM bit is not "10", the IDE bit should be written with "0".

### 38.3.6 CANi Mask Invalid Registers (CiMKIVLR0 and CiMKIVLR1) (i = 0, 1)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Each bit in registers CiMKIVLR0 and CiMKIVLR1 corresponds to a mailbox. The correspondence between the bits and mailboxes is as follows:

- Bit 0 in the CiMKIVLR0 register corresponds to mailbox 0 (MB0).
- Bit 31 in the CiMKIVLR0 register corresponds to mailbox 31 (MB31).
- Bit 0 in the CiMKIVLR1 register corresponds to mailbox 32 (MB32).
- Bit 31 in the CiMKIVLR1 register corresponds to mailbox 63 (MB63).

When each bit is "1", the acceptance mask for the mailbox corresponding to the bit number is disabled. In this case, a receiving message is stored into mailbox only its ID matches bits SID and EID in the CiMBj register.

Write to registers CiMKIVLR0 and CiMKIVLR1 either in CAN reset mode or CAN halt mode.

CAN0 Mask Invalid Register 0 (C0MKIVLR0)

CAN1 Mask Invalid Register 0 (C1MKIVLR0)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	MB31	MB30	MB29	MB28	MB27	MB26	MB25	MB24	MB23	MB22	MB21	MB20	MB19	MB18	MB17	MB16
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MB15	MB14	MB13	MB12	MB11	MB10	MB9	MB8	MB7	MB6	MB5	MB4	MB3	MB2	MB1	MB0
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

<After Reset: Undefined>

Bit	Symbol	Initial Value	R/W	Description
31 to 0	MB31 to 0	Undefined	R/W	Bit 31 corresponds to mailbox 31 (MB31), and bit 0 corresponds to mailbox 0 (MB0). 0: Mask valid 1: Mask invalid

CAN0 Mask Invalid Register 1 (C0MKIVLR1)

CAN1 Mask Invalid Register 1 (C1MKIVLR1)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	MB63	MB62	MB61	MB60	MB59	MB58	MB57	MB56	MB55	MB54	MB53	MB52	MB51	MB50	MB49	MB48
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MB47	MB46	MB45	MB44	MB43	MB42	MB41	MB40	MB39	MB38	MB37	MB36	MB35	MB34	MB33	MB32
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

&lt;After Reset: Undefined&gt;

Bit	Symbol	Initial Value	R/W	Description
31 to 0	MB63 to 32	Undefined	R/W	Bit 31 corresponds to mailbox 63 (MB63), and bit 0 corresponds to mailbox 32 (MB32). 0: Mask valid 1: Mask invalid

### 38.3.7 CANi Mailbox Register j (CiMBj) (i = 0, 1; j = 0 to 63)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Table 38.5 lists the CANi mailbox memory mapping and Table 38.6 lists the CAN data frame construction.

The value after reset of CANi Mailbox is undefined.

Write to the CiMBj register only when the associated CiMCTLj register is "H00" and the corresponding mailbox is not processing an abort request.

Refer to Table 38.5 for detailed addresses.

**Table 38.5 CANi Mailbox Memory Mapping (i = 0, 1)**

Address		Message Content
CAN0	CAN1	Memory Mapping
H'E6E80000 + 16 × j + 0	H'E6E88000 + 16 × j + 0	IDE, RTR, SID10 to SID6
H'E6E80000 + 16 × j + 1	H'E6E88000 + 16 × j + 1	SID5 to SID0, EID17, EID16
H'E6E80000 + 16 × j + 2	H'E6E88000 + 16 × j + 2	EID15 to EID8
H'E6E80000 + 16 × j + 3	H'E6E88000 + 16 × j + 3	EID7 to EID0
H'E6E80000 + 16 × j + 4	H'E6E88000 + 16 × j + 4	—
H'E6E80000 + 16 × j + 5	H'E6E88000 + 16 × j + 5	Data length code (DLC)
H'E6E80000 + 16 × j + 6	H'E6E88000 + 16 × j + 6	Data byte 0
H'E6E80000 + 16 × j + 7	H'E6E88000 + 16 × j + 7	Data byte 1
:	:	:
H'E6E80000 + 16 × j + 13	H'E6E88000 + 16 × j + 13	Data byte 7
H'E6E80000 + 16 × j + 14	H'E6E88000 + 16 × j + 14	Time stamp upper byte
H'E6E80000 + 16 × j + 15	H'E6E88000 + 16 × j + 15	Time stamp lower byte

**Table 38.6 CAN Data Frame Construction**

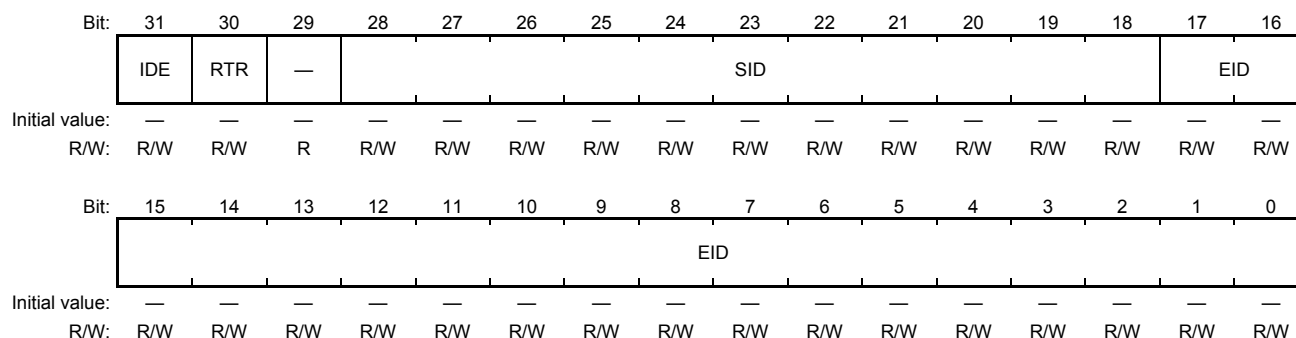
SID10 to SID6	SID5 to SID0	EID17 to EID16	EID15 to EID8	EID7 to EID0	DLC3 to DLC0	DATA0	DATA1	...	DATA7
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The previous value of each mailbox is retained unless a new message is received.



CAN0 Mailbox Register 0 to 63 (C0MB0 to 63)

CAN1 Mailbox Register 0 to 63 (C1MB0 to 63)



&lt;After Reset: Undefined&gt;

Bit	Symbol	Initial Value	R/W	Description
31	IDE	Undefined	R/W	<p>ID Extension Bit*1</p> <p>The IDE bit sets the ID format of standard IDs or extended IDs.</p> <p>The IDE bit is enabled when the IDFM bit in the CiCTLR register is "10" (mixed ID mode).</p> <p>When the IDFM bit is "10", the IDE bit specifies the following operation.</p> <p>Receive mailbox receives only ID format specified by the IDE bit.</p> <p>Transmit mailbox transmits with ID format specified by the IDE bit.</p> <p>Receive FIFO mailbox receives messages with the standard ID, extended ID, or both IDs specified by the IDE bit in registers CiFIDCR0 and CiFIDCR1.</p> <p>Transmit FIFO mailbox transmits messages with the standard ID or extended ID specified by the IDE bit in the relevant transmitting message.</p> <p>0: Standard ID 1: Extended ID</p>
30	RTR	Undefined	R/W	<p>Remote Frame Request Bit</p> <p>The RTR bit sets the frame format of data frames or remote frames.</p> <p>This bit specifies the following operation:</p> <p>Receive mailbox receives only frames with the format specified by the RTR bit.</p> <p>Transmit mailbox transmits according to the frame format specified by the RTR bit.</p> <p>Receive FIFO mailbox receives the data frame, remote frame, or both frames specified by the RTR bit in registers CiFIDCR0 and CiFIDCR1.</p> <p>Transmit FIFO mailbox transmits the data frame or remote frame specified by the RTR bit in the relevant transmitting message.</p> <p>0: Data frame 1: Remote frame</p>
29	—	Undefined	R	<p>Reserved bit</p> <p>The reset value is undefined. The write value should be "0". This bit is read as "0" after "0" is written to.</p>

Bit	Symbol	Initial Value	R/W	Description
28 to 18	SID	Undefined	R/W	<b>Standard ID Bits</b> The SID bit sets the standard ID of data frames and remote frames. The SID bit is used to transmit or receive both standard ID and extended ID messages. 0: Corresponding SID bit is "0" 1: Corresponding SID bit is "1"
17 to 0	EID	Undefined	R/W	<b>Extended ID Bits*2</b> The EID bit sets the extended ID of data frames and remote frames. The EID bit is used to transmit or receive extended ID messages. 0: Corresponding EID bit is "0" 1: Corresponding EID bit is "1"

Notes: 1. When the IDFM bit is not "10", it should be written with "0".  
 2. If the mailbox has received a standard ID message, the EID bit in the mailbox is undefined.

CAN0 Mailbox Register 0 to 63 (C0MB0 to 63)

CAN1 Mailbox Register 0 to 63 (C1MB0 to 63)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	DLC			
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

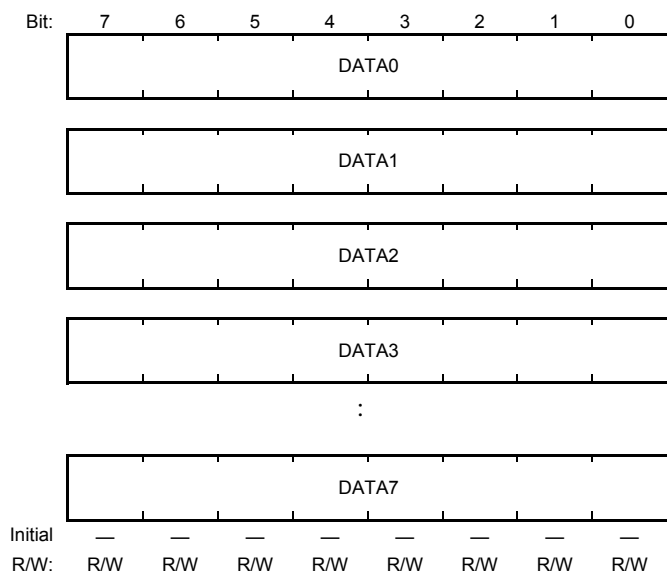
<After Reset: Undefined>

Bit	Symbol	Initial Value	R/W	Description
15 to 4	—	Undefined	R	<b>Reserved bits</b> The reset value is undefined. The write value should be "0". These bits are read as "0" after "0" is written to.
3 to 0	DLC	Undefined	R/W	<b>Data Length Code Bits*</b> The DLC is used to set the number of data bytes to be transmitted in a data frame. When data is requested using a remote frame, the number of data bytes to be requested is set. When a data frame is received, the number of received data bytes is stored. When a remote frame is received, the number of requested data bytes is stored. 0000: Data length = 0 byte 0001: Data length = 1 byte 0010: Data length = 2 bytes 0011: Data length = 3 bytes 0100: Data length = 4 bytes 0101: Data length = 5 bytes 0110: Data length = 6 bytes 0111: Data length = 7 bytes 1xxx: Data length = 8 bytes Legend: x represents any value.

Note: \* If the mailbox has received a message with n bytes less than 8 bytes, the values of DATA<sub>n</sub> to DATA<sub>7</sub> in the mailbox are undefined.

CAN0 Mailbox Register 0 to 63 (C0MB0 to 63)

CAN1 Mailbox Register 0 to 63 (C1MB0 to 63)



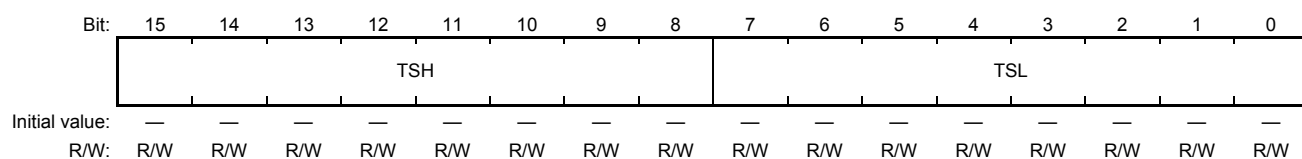
<After Reset: Undefined>

Bit	Symbol	Initial Value	R/W	Description
7 to 0	DATA0 to 7	Undefined	R/W	Data Bytes 0 to 7*1*2 DATA0 to DATA7 store the transmitted or received CAN message data. Transmission or reception starts from DATA0. The bit order on the CAN bus is MSB first, and transmission or reception starts from bit 7.

- Notes:
1. If the mailbox has received a message with n bytes less than 8 bytes, the values of DATAn to DATA7 in the mailbox are undefined.
  2. If the mailbox has received a remote frame, the previous values of DATA0 to DATA7 in the mailbox are retained.

CAN0 Mailbox Register 0 to 63 (C0MB0 to 63)

CAN1 Mailbox Register 0 to 63 (C1MB0 to 63)



<After Reset: Undefined>

Bit	Symbol	Initial Value	R/W	Description
15 to 8	TSH	Undefined	R/W	Time Stamp Higher Byte TSL and TSH store the counter value of the time stamp when received messages are stored in the mailbox.
7 to 0	TSL	Undefined	R/W	Time Stamp Lower Byte TSL and TSH store the counter value of the time stamp when received messages are stored in the mailbox.

### 38.3.8 CANi Mailbox Interrupt Enable Registers (CiMIER0 and CiMIER1) (i = 0, 1)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Interrupts can be enabled individually for each mailbox.

In normal mailbox mode (all bits) and in FIFO mailbox mode (bits 23 to 0 in the CiMIER1 register and all bits in the CiMIER0 register), each bit corresponds to the mailbox with the related number. These bits enable or disable transmission/reception complete interrupts for the corresponding mailboxes.

- Bit 0 in the CiMIER0 register corresponds to mailbox 0 (MB0).
- Bit 31 in the CiMIER0 register corresponds to mailbox 31 (MB31).
- Bit 0 in the CiMIER1 register corresponds to mailbox 32 (MB32).
- Bit 31 in the CiMIER1 register corresponds to mailbox 63 (MB63).

In FIFO mailbox mode, bits 29, 28, 25, and 24 of the CiMIER1 register specify whether transmit/receive FIFO interrupts are enabled/disabled and timing when interrupt requests are generated.

Write to registers CiMIER0 and CiMIER1 only when the associated CiMCTLj register (i = 0, 1) (j = 0 to 63) is "H'00" and the corresponding mailbox is not processing a transmission or reception abort request. In FIFO mailbox mode, change the bits in the CiMIER1 register for the associated FIFO only when:

- The TFE bit in the CiTFCR register is 0 and the TFEST bit is 1, and
- The RFE bit in the CiRFCR register is 0 and the RFEST bit is 1.

CAN0 Mailbox Interrupt Enable Register 1 (C0MIER1)

CAN1 Mailbox Interrupt Enable Register 1 (C1MIER1)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	MB63	MB62	MB61	MB60	MB59	MB58	MB57	MB56	MB55	MB54	MB53	MB52	MB51	MB50	MB49	MB48
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MB47	MB46	MB45	MB44	MB43	MB42	MB41	MB40	MB39	MB38	MB37	MB36	MB35	MB34	MB33	MB32
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Normal mailbox mode

<After Reset: Undefined>

Bit	Symbol	Initial Value	R/W	Description
31 to 0	MB63 to MB32	Undefined	R/W	Interrupt Enable Bits Bit 31 corresponds to mailbox 63 (MB63), and bit 0 corresponds to mailbox 32 (MB32). 0: Interrupt disabled 1: Interrupt enabled

- FIFO mailbox mode (CiMIER1 only)

&lt;After Reset: Undefined&gt;

Bit	Symbol	Initial Value	R/W	Description
31, 30	MB63 MB62	Undefined	R	Reserved bits The reset value is undefined. The write value should be "0". These bits are read as "0" after "0" is written to.
29	MB61	Undefined	R/W	Receive FIFO Interrupt Generation Timing Control Bit* Receive FIFO interrupt request is generated 0: Every time reception is completed 1: When receive FIFO becomes buffer warning by completion of reception
28	MB60	Undefined	R/W	Receive FIFO Interrupt Enable Bit 0: Interrupt disabled 1: Interrupt enabled
27, 26	MB59 MB58	Undefined	R	Reserved bits The reset value is undefined. The write value should be "0". These bits are read as "0" after "0" is written to.
25	MB57	Undefined	R/W	Transmit FIFO Interrupt Generation Timing Control Bit Transmit FIFO interrupt request is generated 0: Every time transmission is completed 1: When transmit FIFO becomes empty due to completion of transmission
24	MB56	Undefined	R/W	Transmit FIFO Interrupt Enable Bit 0: Interrupt disabled 1: Interrupt enabled
23 to 0	MB55 to MB32	Undefined	R/W	Interrupt Enable Bits Bit 23 corresponds to mailbox 55 (MB55), and bit 0 corresponds to mailbox 32 (MB32). 0: Interrupt disabled 1: Interrupt enabled

Note: \* No interrupt request is generated when the receive FIFO becomes buffer warning from full. "Buffer warning" indicates a state in which the third unread message is stored in the receive FIFO.

## CAN0 Mailbox Interrupt Enable Register 0 (C0MIER0)

## CAN1 Mailbox Interrupt Enable Register 0 (C1MIER0)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	MB31	MB30	MB29	MB28	MB27	MB26	MB25	MB24	MB23	MB22	MB21	MB20	MB19	MB18	MB17	MB16
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MB15	MB14	MB13	MB12	MB11	MB10	MB9	MB8	MB7	MB6	MB5	MB4	MB3	MB2	MB1	MB0
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

&lt;After Reset: Undefined&gt;

Bit	Symbol	Initial Value	R/W	Description
31 to 0	MB31 to MB0	Undefined	R/W	Interrupt Enable Bits Bit 31 corresponds to mailbox 31 (MB31), and bit 0 corresponds to mailbox 0 (MB0). 0: Interrupt disabled 1: Interrupt enabled

### 38.3.9 CANi Message Control Register j (CiMCTLj) (i = 0, 1; j = 0 to 63)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Write to the CiMCTLj register in CAN operation mode or CAN halt mode.

Do not use registers CiMCTL56 to CiMCTL63 in FIFO mailbox mode.

CAN0 Message Control Register 0 to 63 (C0MCTL0 to C0MCTL63)

CAN1 Message Control Register 0 to 63 (C1MCTL0 to C1MCTL63)

#### Registers CiMCTL32 to CiMCTL63

- Transmit mailbox setting enabled (When the TRMREQ bit is "1" and the RECREQ bit is "0")

Bit:	7	6	5	4	3	2	1	0
	TRM REQ	REC REQ	—	ONE SHOT	—	TRM ABT	TRMAC TIVE	SENTD ATA
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R	R/W	R	R/W	R	R/W

- Receive mailbox setting enabled (When the TRMREQ bit is "0" and the RECREQ bit is "1")

Bit:	7	6	5	4	3	2	1	0
	TRM REQ	REC REQ	—	ONE SHOT	—	MSG LOST	INVAL DATA	NEWD ATA
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R	R/W	R	R/W	R	R/W

#### Registers CiMCTL0 to CiMCTL31

Bit:	7	6	5	4	3	2	1	0
	—	REC REQ	—	—	—	MSG LOST	INVAL DATA	NEWD ATA
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R/W	R	R	R	R/W	R	R/W

&lt;After Reset: H'00&gt;

Bit	Symbol	Initial Value	R/W	Description
7	TRMREQ	0	R/W	<p>Transmit Mailbox Request Bit*2*4</p> <p>The TRMREQ bit selects transmit modes shown in Table 38.11.</p> <p>When TRMREQ bit is set to "1", the corresponding mailbox is configured for transmission of a data frame or a remote frame.</p> <p>When TRMREQ bit is set to "0", the corresponding mailbox is not configured for transmission of a data frame or a remote frame.</p> <p>If the TRMREQ bit is changed from "1" to "0" to cancel the corresponding transmission request, either the TRMABT or SENTDATA bit is set to "1".</p> <p>When setting the TRMREQ bit to "1", do not set the RECREQ bit to "1". To change the configuration of a mailbox from reception to transmission, first abort the reception and then set bits NEWDATA and MSGLOST to "0" before changing to transmission.</p> <p>0: Not configured for transmission 1: Configured for transmission</p>
—	—	0	R	<p>Reserved bit (Registers CiMCTL0 to CiMCTL31)</p> <p>This bit is always read as 0. The write value should always be 0. Operation is not guaranteed if a value other than 0 is written to this bit.</p>
6	RECREQ	0	R/W	<p>Receive Mailbox Request Bit*2*4*5</p> <p>The RECREQ bit selects receive modes shown in Table 38.11.</p> <p>When the RECREQ bit is set to "1", the corresponding mailbox is configured for reception of a data frame or a remote frame.</p> <p>When the RECREQ bit is set to "0", the corresponding mailbox is not configured for reception of a data frame or a remote frame.</p> <p>Due to hardware protection the RECREQ bit cannot be set to "0" by writing "0" by a program during the following period.</p> <p>Hardware protection is started From the acceptance filter procedure. (the beginning of CRC field) Hardware protection is released For the mailbox that is specified to receive the incoming message, after the received data is stored into the mailbox or a CAN bus error occurs. (i.e. a maximum period of hardware protection is from the beginning of CRC field to the end of the 7th bit of EOF.) For the other mailboxes, after the acceptance filter procedure.</p> <p>If no mailbox is specified to receive the message, after the acceptance filter procedure.</p> <p>When setting the RECREQ bit to "1", do not set "1" to the TRMREQ bit.</p> <p>To change the configuration of a mailbox from transmission to reception, first abort the transmission and then set bits SENTDATA and TRMABT to "0" before changing to reception.</p> <p>0: Not configured for reception 1: Configured for reception</p>
5	—	0	R	<p>Reserved bit</p> <p>This bit is always read as 0. The write value should always be 0. Operation is not guaranteed if a value other than 0 is written to this bit.</p>

Bit	Symbol	Initial Value	R/W	Description
4	ONESHOT	0	R/W	<p>One-shot Enable Bit*<sup>3</sup></p> <p>The ONESHOT bit can be used in the following two ways, receive mode and transmit mode:</p> <p>One-Shot Receive Mode</p> <p>When the ONESHOT bit is set to "1" in receive mode (RECREQ bit = "1" and TRMREQ bit = "0"), the mailbox receives a message only one time. The mailbox does not behave as a receive mailbox after having received a message one time. The behavior of bits NEWDATA and INVALIDDATA is the same as in normal reception mode. In one-shot receive mode, the MSGLOST bit is not set to "1".</p> <p>To set the ONESHOT bit to "0", first write "0" to the RECREQ bit and ensure that it has been set to "0".</p> <p>One-Shot Transmit Mode</p> <p>When the ONESHOT bit is set to "1" in transmit mode (RECREQ bit = "0" and TRMREQ bit = "1"), the CAN module transmits a message only one time.</p> <p>The CAN module does not transmit the message again if a CAN bus error or CAN bus arbitration lost occurs. When transmission is completed, the SENTDATA bit is set to "1". If transmission is not completed due to a CAN bus error or CAN bus arbitration lost, the TRMABT bit is set to "1".</p> <p>Set the ONESHOT bit to "0" after the SENTDATA or TRMABT bit is set to "1".</p> <p>0: One-shot reception or one-shot transmission disabled 1: One-shot reception or one-shot transmission enabled</p>
—	—	0	R	<p>Reserved bit (Registers CiMCTL0 to CiMCTL31)</p> <p>This bit is always read as 0. The write value should always be 0. Operation is not guaranteed if a value other than 0 is written to this bit.</p>
3	—	0	R	<p>Reserved bit</p> <p>This bit is always read as 0. The write value should always be 0. Operation is not guaranteed if a value other than 0 is written to this bit.</p>
2	TRMABT	0	R/W	<p>Transmission Abort Complete Flag (Transmit mailbox setting enabled)*<sup>1</sup>*<sup>2</sup></p> <p>The TRMABT bit is set to "1" in the following cases:</p> <p>Following a transmission abort request, when the transmission abort is completed before starting transmission.</p> <p>Following a transmission abort request, when the CAN module detects CAN bus arbitration lost or a CAN bus error.</p> <p>In one-shot transmission mode (RECREQ bit = "0", TRMREQ bit = "1", and ONESHOT bit = "1"), when the CAN module detects CAN bus arbitration lost or a CAN bus error.</p> <p>The TRMABT bit is not set to "1" when data transmission is completed. In this case, the SENTDATA bit is set to "1".</p> <p>The TRMABT bit is set to "0" by writing "0" by a program.</p> <p>0: Transmission has started, transmission abort failed because transmission is completed, or transmission abort is not requested 1: Transmission abort is completed</p>



Bit	Symbol	Initial Value	R/W	Description
	MSGLOST	0	R/W	<p>Message Lost Flag (Receive mailbox setting enabled)*1*2</p> <p>The MSGLOST bit is set to "1" when the mailbox is overwritten or overrun by a new received message while the NEWDATA bit is "1". The MSGLOST bit is set to "1" at the end of the 6th bit of EOF. The MSGLOST bit is set to "0" by writing "0" by a program.</p> <p>In both overwrite and overrun modes, the MSGLOST bit is not set to "0" by writing "0" by a program during the 5 peripheral clock (clkp1) cycles following the 6th bit of EOF.</p> <p>0: Message is not overwritten or overrun 1: Message is overwritten or overrun</p>
1	TRMACTIVE	0	R	<p>Transmission-in-Progress Status Flag (Transmit mailbox setting enabled)</p> <p>The TRMACTIVE bit is set to "1" when the corresponding mailbox of the CAN module begins transmitting a message.</p> <p>The TRMACTIVE is set to "0" when the CAN module has lost CAN bus arbitration, a CAN bus error occurs, or data transmission is completed.</p> <p>0: Transmission is pending or transmission is not requested 1: From acceptance of transmission request to completion of transmission, or error/arbitration lost</p>
	INVALIDDATA	0	R	<p>Reception-in-Progress Status Flag (Receive mailbox setting enabled)</p> <p>After the completion of a message reception, the INVALIDDATA bit is set to "1" while the received message is being updated into the corresponding mailbox.</p> <p>The INVALIDDATA bit is set to "0" immediately after the message has been stored. If the mailbox is read while the INVALIDDATA bit is "1", the data is undefined.</p> <p>0: Message valid 1: Message being updated</p>
0	SENTDATA	0	R/W	<p>Transmission Complete Flag (Transmit mailbox setting enabled)*1*2</p> <p>The SENTDATA bit is set to "1" when data transmission from the corresponding mailbox is completed.</p> <p>The SENTDATA bit is set to "0" by writing "0" by a program.</p> <p>To set the SENTDATA bit to "0", first set the TRMREQ bit to "0". Bits SENTDATA and TRMREQ cannot be set to "0" simultaneously.</p> <p>To transmit a new message from the corresponding mailbox, set the SENTDATA bit to "0".</p> <p>0: Transmission is not completed (pending) 1: Transmission is completed (success)</p>
	NEWDATA	0	R/W	<p>Reception Complete Flag (Receive mailbox setting enabled)*1*2</p> <p>The NEWDATA bit is set to "1" when a new message is being stored or has been stored to the mailbox. The timing for setting this bit to "1" is simultaneous with the INVALIDDATA bit.</p> <p>The NEWDATA bit is set to "0" by writing "0" by a program.</p> <p>The NEWDATA bit is not set to "0" by writing "0" by a program while the related INVALIDDATA bit is "1".</p> <p>0: No data has been received or "0" is written to the NEWDATA bit 1: A new message is being stored or has been stored to the mailbox</p>

- Notes:
1. Write "0" only. Writing "1" has no effect.
  2. When writing "0" to bits NEWDATA, SENTDATA, MSGLOST, TRMABT, RECREQ, and TRMREQ by a program, only the specified bit is set to "0" and the other bits are set to "1".
  3. To enter one-shot receive mode, write "1" to the ONESHOT bit at the same time as setting the RECREQ bit to "1".  
To exit one-shot receive mode, write "0" to the ONESHOT bit after writing "0" to the RECREQ bit and confirming it has been set to "0".  
To enter one-shot transmit mode, write "1" to the ONESHOT bit at the same time as setting the TRMREQ bit to "1".  
To exit one-shot transmit mode, write "0" to the ONESHOT bit after the message has been transmitted or aborted.
  4. Do not set both the RECREQ and TRMREQ bits to "1".
  5. When setting the RECREQ bit to "0", set bits MSGLOST, NEWDATA, RECREQ to "0" simultaneously.

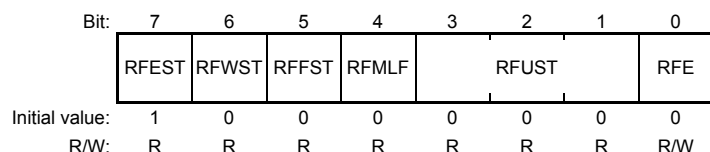
**38.3.10 CANi Receive FIFO Control Register (CiRFCR) (i = 0, 1)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Write to the CiRFCR registers in CAN operation mode or CAN halt mode.

CAN0 Receive FIFO Control Register (C0RFCR)

CAN1 Receive FIFO Control Register (C1RFCR)

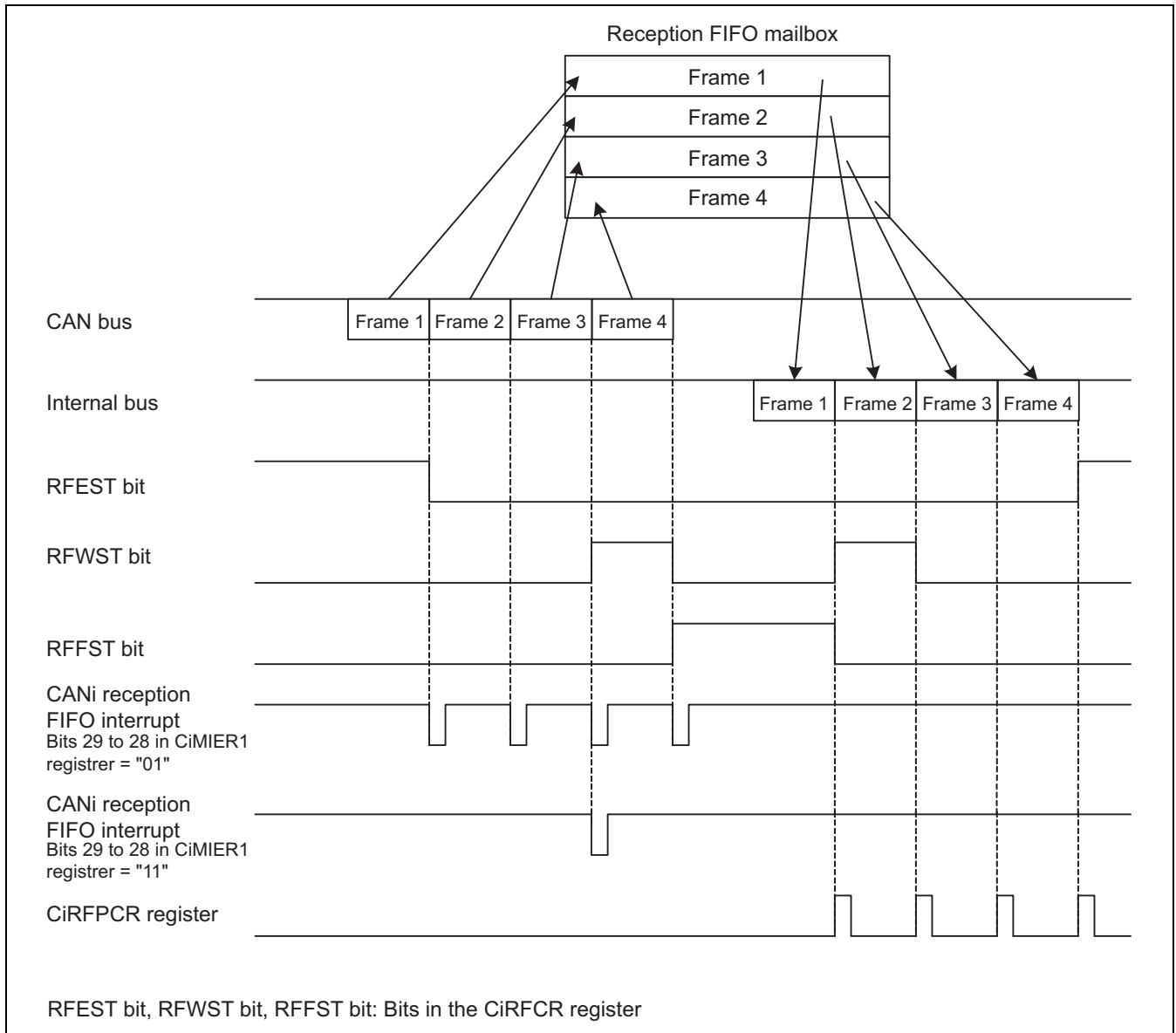


<After Reset: H'80>

Bit	Symbol	Initial Value	R/W	Description
7	RFEST	1	R	<p>Receive FIFO Empty Status Flag</p> <p>The RFEST bit is set to "1" (no unread message in receive FIFO) when the number of unread messages in the receive FIFO is "0". The RFEST bit is set to "1" when the RFE bit is set to "0". The RFEST bit is set to "0" (unread message in receive FIFO) when the number of unread messages in the receive FIFO is one or more.</p> <p>0: Unread message in receive FIFO 1: No unread message in receive FIFO</p>
6	RFWST	0	R	<p>Receive FIFO Buffer Warning Status Flag</p> <p>The RFWST bit is set to "1" (receive FIFO is buffer warning) when the number of unread messages in the receive FIFO is 3. The RFWST bit is "0" (receive FIFO is not buffer warning) when the number of unread messages in the receive FIFO is less than 3 or equal to 4. The RFWST bit is set to "0" when the RFE bit is "0".</p> <p>0: Receive FIFO is not buffer warning 1: Receive FIFO is buffer warning (3 unread messages)</p>
5	RFFST	0	R	<p>Receive FIFO Full Status Flag</p> <p>The RFFST bit is set to "1" (receive FIFO is full) when the number of unread messages in the receive FIFO is 4. The RFFST bit is "0" (receive FIFO is not full) when the number of unread messages in the receive FIFO is less than 4. The RFFST bit is set to "0" when the RFE bit is "0".</p> <p>0: Receive FIFO is not full 1: Receive FIFO full (4 unread messages)</p>

Bit	Symbol	Initial Value	R/W	Description
4	RFMLF	0	R	<p>Receive FIFO Message Lost Flag</p> <p>The RFMLF bit is set to "1" (receive FIFO message lost has occurred) when the receive FIFO receives a new message and the receive FIFO is full. The timing for setting this bit to "1" is at the end of the 6th bit of EOF.</p> <p>The RFMLF bit is set to "0" by writing "0" by a program (writing "1" has no effect). In both overwrite and overrun modes, the RFMLF bit cannot be set to "0" (receive FIFO message lost has not occurred) by writing "0" by a program due to hardware protection during the five cycles of peripheral clock (clkp1) following the 6th bit of EOF, if the receive FIFO is full and determined to receive the message.</p> <p>0: No receive FIFO message lost has occurred 1: Receive FIFO message lost has occurred</p>
3 to 1	RFUST	All 0	R	<p>Receive FIFO Unread Message Number Status Flag</p> <p>The RFUST bit indicates the number of unread messages in the receive FIFO.</p> <p>The value of the RFUST bit is initialized to "000" when the RFE bit is set to "0".</p> <p>000: No unread message 001: 1 unread message 010: 2 unread messages 011: 3 unread messages 100: 4 unread messages 101: Reserved 110: Reserved 111: Reserved</p>
0	RFE	0	R/W	<p>Receive FIFO Enable Bit</p> <p>When the RFE bit is set to "1", the receive FIFO is enabled.</p> <p>When this bit is set to "0", the receive FIFO is disabled for reception and becomes empty (RFEST bit = "1").</p> <p>Do not set this bit to "1" in normal mailbox mode (MBM bit in the CiCTLR register = "0").</p> <p>Due to hardware protection, the RFE bit is not set to "0" by writing "0" by a program during the following period:</p> <p>The hardware protection is started From the acceptance filter procedure (the beginning of CRC field) The hardware protection is released</p> <p>If the receive FIFO is specified to receive the incoming message, after the received data is stored into the receive FIFO or a CAN bus error occurs. (i.e. maximum period of hardware protection is from the beginning of CRC field to the end of 7th bit of EOF.)</p> <p>If the receive FIFO is not specified to receive the message, after the acceptance filter procedure.</p> <p>0: Receive FIFO disabled 1: Receive FIFO enabled</p>

Figure 38.2 shows the receive FIFO mailbox operation.



**Figure 38.2 Receive FIFO Mailbox Operation**  
**(Bits 29 and 28 in CiMIER1 Register = "01" and "11") (i = 0, 1)**

**38.3.11 CANi Receive FIFO Pointer Control Register (CiRFPCR) (i = 0, 1)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

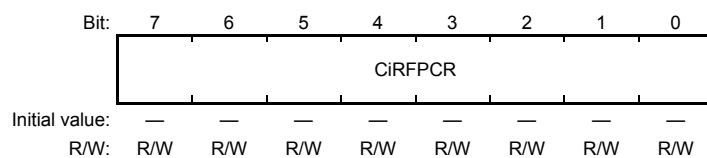
When the receive FIFO is not empty, write "H'FF" to the CiRFPCR register by a program to increment the CPU-side pointer for the receive FIFO to the next mailbox location.

Do not write to the CiRFPCR register when the RFE bit in the CiRFCR register is "0" (receive FIFO disabled).

Both the CAN-side pointer and the CPU-side pointer are incremented when a new message is received and the RFFST bit is "1" (receive FIFO is full) in overwrite mode. When the RFMLF bit is "1" in this condition, the CPU-side pointer cannot be incremented by writing to the CiRFPCR register by a program.

CAN0 Receive FIFO Pointer Control Register (C0RFPCR)

CAN1 Receive FIFO Pointer Control Register (C1RFPCR)



<After Reset: Undefined>

Bit	Symbol	Initial Value	R/W	Description
7 to 0	CiRFPCR	Undefined	R/W	The CPU-side pointer for the receive FIFO is incremented by writing "H'FF"

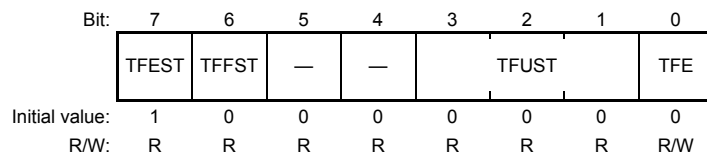
**38.3.12 CANi Transmit FIFO Control Register (CiTFCR) (i = 0, 1)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Write to the CiTFCR register in CAN operation mode or CAN halt mode.

CAN0 Transmit FIFO Control Register (C0TFCR)

CAN1 Transmit FIFO Control Register (C1TFCR)



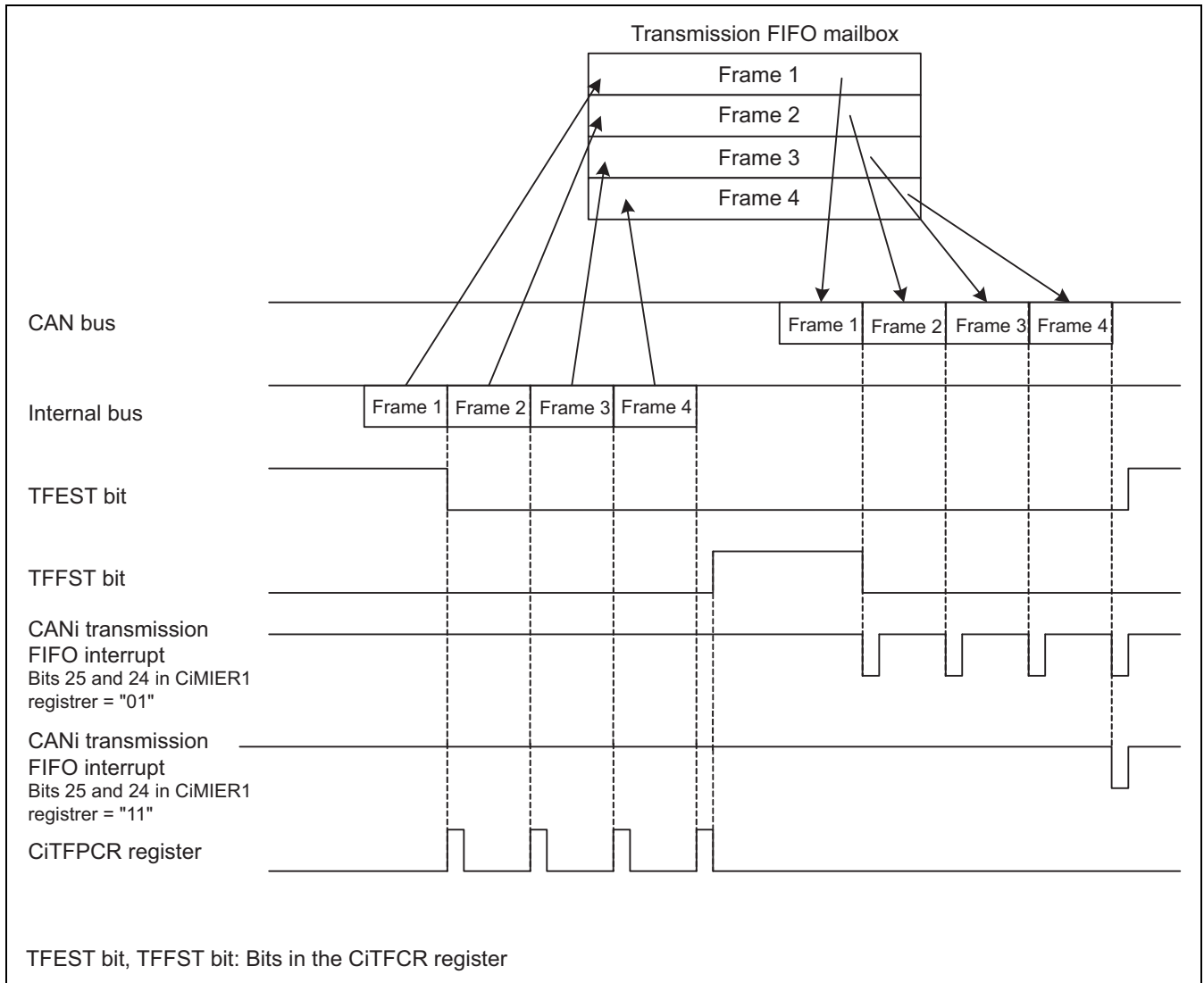
&lt;After Reset: H'80&gt;

Bit	Symbol	Initial Value	R/W	Description
7	TFEST	1	R	<p>Transmit FIFO Empty Status Bit</p> <p>The TFEST bit is set to "1" (no message in transmit FIFO) when the number of unsent messages in the transmit FIFO is "0". The TFEST bit is set to "1" when transmission from the transmit FIFO has been aborted.</p> <p>The TFEST bit is set to "0" (message in transmit FIFO) when the number of unsent messages in the transmit FIFO is not "0".</p> <p>0: Unsent message in transmit FIFO 1: No unsent message in transmit FIFO</p>
6	TFFST	0	R	<p>Transmit FIFO Full Status Bit</p> <p>The TFFST bit is set to "1" (transmit FIFO is full) when the number of unsent messages in the transmit FIFO is 4. The TFFST bit is set to "0" (transmit FIFO is not full) when the number of unsent messages in the transmit FIFO is less than 4. The TFFST bit is set to "0" when transmission from the transmit FIFO has been aborted.</p> <p>0: Transmit FIFO is not full 1: Transmit FIFO is full (4 unsent messages)</p>
5, 4	—	All 0	R	<p>Reserved bits</p> <p>These bits are always read as 0. The write value should always be 0. Operation is not guaranteed if a value other than 0 is written to these bits.</p>
3 to 1	TFUST	000	R	<p>Transmit FIFO Unsent Message Number Status Bits</p> <p>The TFUST bit indicates the number of unsent messages in the transmit FIFO.</p> <p>After the TFE bit is set to "0", the value of the TFUST bit is initialized to "000" when transmission abort or transmission is completed.</p> <p>000: No unsent message 001: 1 unsent message 010: 2 unsent messages 011: 3 unsent messages 100: 4 unsent messages 101: Reserved 110: Reserved 111: Reserved</p>

Bit	Symbol	Initial Value	R/W	Description
0	TFE	0	R/W	<p>Transmit FIFO Enable Bit</p> <p>When the TFE bit is set to "1", the transmit FIFO is enabled.</p> <p>When the TFE bit is set to "0", the transmit FIFO becomes empty (TFEST bit = "1") and then unsent messages from the transmit FIFO are lost as described below:</p> <p>If a message from the transmit FIFO is not scheduled for the next transmission or during transmission.</p> <p>Following the completion of transmission, a CAN bus error, CAN bus arbitration lost, or entry to CAN halt mode if a message from the transmit FIFO is scheduled for the next transmission or already during transmission.</p> <p>Before setting the TFE bit to set to "1" again, ensure that the TFEST bit has been set to "1".</p> <p>After setting the TFE bit to "1", write transmit data into the CiMB56 register.</p> <p>Do not set the TFE bit to "1" in normal mailbox mode (MBM bit in the CiCTLR register = "0").</p> <p>0: Transmit FIFO disabled 1: Transmit FIFO enabled</p>



Figure 38.3 shows the transmit FIFO mailbox operation.



**Figure 38.3 Transmit FIFO Mailbox Operation**  
**(Bits 25 and 24 in CiMIER1 Register = "01" and "11") (i = 0, 1)**

**38.3.13 CANi Transmit FIFO Pointer Control Register (CiTFPCR) (i = 0, 1)**

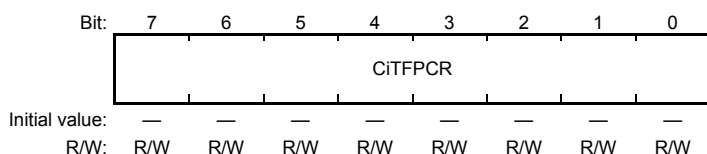
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

When the transmit FIFO is not full, write "H'FF" to the CiTFPCR register by a program to increment the CPU-side pointer for the transmit FIFO to the next mailbox location.

Do not write to the CiTFPCR register when the TFE bit in the CiTFPCR register is "0" (transmit FIFO disabled).

CAN0 Transmit FIFO Pointer Control Register (C0TFPCR)

CAN1 Transmit FIFO Pointer Control Register (C1TFPCR)



<After Reset: Undefined>

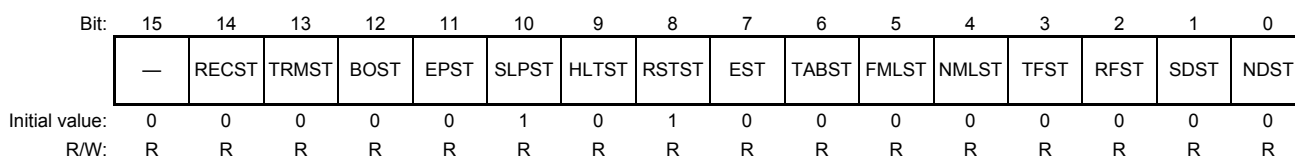
Bit	Symbol	Initial Value	R/W	Description
7 to 0	CiTFPCR	Undefined	R/W	The CPU-side pointer for the transmit FIFO is incremented by writing "H'FF"

**38.3.14 CANi Status Register (CiSTR) (i = 0, 1)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CAN0 Status Register (C0STR)

CAN1 Status Register (C1STR)



<After Reset: H'0500>

Bit	Symbol	Initial Value	R/W	Description
15	—	0	R	Reserved bit This bit is always read as 0. The write value should always be 0. Operation is not guaranteed if a value other than 0 is written to this bit.
14	RECST	0	R	Receive Status Flag (receiver) The RECST bit is set to "1" when the CAN module performs as a receiver node. The RECST bit is set to "0" when the CAN module performs as a transmitter node or is in bus-idle state. 0: Bus idle or transmission in progress 1: Reception in progress

Bit	Symbol	Initial Value	R/W	Description
13	TRMST	0	R	<p>Transmit Status Flag (transmitter)</p> <p>The TRMST bit is set to "1" when the CAN module performs as a transmitter node or is in the bus-off state. The TRMST bit is set to "0" when the CAN module performs as a receiver node or is in bus-idle state.</p> <p>0: Bus idle or reception in progress 1: Transmission in progress or in bus-off state</p>
12	BOST	0	R	<p>Bus-Off Status Flag</p> <p>The BOST bit is set to "1" when the value of the CiTECR register exceeds 255 and the CAN module is in the bus-off state (<math>TEC \geq 256</math>). The BOST bit is set to "0" when the CAN module is not in the bus-off state.</p> <p>0: Not in bus-off state 1: In bus-off state</p>
11	EPST	0	R	<p>Error-Passive Status Flag</p> <p>The EPST bit is set to "1" when the value of the CiTECR or CiRECR register exceeds 127 and the CAN module is in error-passive state (<math>128 \leq TEC &lt; 256</math> or <math>128 \leq REC &lt; 256</math>). The EPST bit is set to "0" when the CAN module is not in the error-passive state.</p> <p>TEC indicates the value of the transmit error counter (CiTECR register) and REC indicates the value of the receive error counter (CiRECR register).</p> <p>0: Not in error-passive state 1: In error-passive state</p>
10	SLPST	1	R	<p>CAN Sleep Status Flag</p> <p>The SLPST bit is set to "1" when the CAN module is in CAN sleep mode. The SLPST bit is set to "0" when the CAN module is not in CAN sleep mode.</p> <p>0: Not in CAN sleep mode 1: In CAN sleep mode</p>
9	HLTST	0	R	<p>CAN Halt Status Flag</p> <p>The HLTST bit is set to "1" when the CAN module is in CAN halt mode. The HLTST bit is set to "0" when the CAN module is not in CAN halt mode. Even when the state is changed from CAN halt mode to CAN sleep mode, the HLTST bit remains "1".</p> <p>0: Not in CAN halt mode 1: In CAN halt mode</p>
8	RSTST	1	R	<p>CAN Reset Status Flag</p> <p>The RSTST bit is set to "1" when the CAN module is in CAN reset mode. The RSTST bit is "0" when the CAN module is not in CAN reset mode. Even when the state is changed from CAN reset mode to CAN sleep mode, the RSTST bit remains "1".</p> <p>0: Not in CAN reset mode 1: In CAN reset mode</p>
7	EST	0	R	<p>Error Status Flag</p> <p>The EST bit is "1" when at least one error is detected by the CiEIFR register regardless of the value of the CiEIER register. The EST bit is set to "0" when no error is detected by the CiEIFR register.</p> <p>0: No error occurred 1: Error occurred</p>

Bit	Symbol	Initial Value	R/W	Description
6	TABST	0	R	<p>Transmission Abort Status Flag</p> <p>The TABST bit is set to "1" when at least one TRMABT bit in the CiMCTLj register is "1" regardless of the value of the CiMIER register.</p> <p>The TABST bit is set to "0" when all TRMABT bits are "0".</p> <p>0: No mailbox with TRMABT bit = "1"</p> <p>1: Mailbox(es) with TRMABT bit = "1"</p>
5	FMLST	0	R	<p>FIFO Mailbox Message Lost Status Flag</p> <p>The FMLST bit is set to "1" when the RFMLF bit in the CiRFCR register is "1" regardless of the value of the CiMIER register. The FMLST bit is set to "0" when the RFMLF bit is "0".</p> <p>0: RFMLF bit = "0"</p> <p>1: RFMLF bit = "1"</p>
4	NMLST	0	R	<p>Normal Mailbox Message Lost Status Flag</p> <p>The NMLST bit is set to "1" when at least one MSGLOST bit in the CiMCTLj register is "1" regardless of the value of the CiMIER register. The NMLST bit is set to "0" when all MSGLOST bits are "0".</p> <p>0: No mailbox with MSGLOST bit = "1"</p> <p>1: Mailbox(es) with MSGLOST bit = "1"</p>
3	TFST	0	R	<p>Transmit FIFO Status Flag</p> <p>The TFST bit is set to "1" when the transmit FIFO is not full. The TFST bit is set to "0" when the transmit FIFO is full. The TFST bit is set to "0" when normal mailbox mode is selected.</p> <p>0: Transmit FIFO is full</p> <p>1: Transmit FIFO is not full</p>
2	RFST	0	R	<p>Receive FIFO Status Flag</p> <p>The RFST bit is set to "1" when the receive FIFO is not empty. The RFST bit is set to "0" when the receive FIFO is empty.</p> <p>The RFST bit is set to "0" when normal mailbox mode is selected.</p> <p>0: No message in receive FIFO</p> <p>1: Message in receive FIFO</p>
1	SDST	0	R	<p>SENTDATA Status Flag</p> <p>The SDST bit is set to "1" when at least one SENTDATA bit in the CiMCTLj register is "1" regardless of the value of the CiMIER register. The SDST bit is set to "0" when all SENTDATA bits are "0".</p> <p>0: No mailbox with SENTDATA bit = "1"</p> <p>1: Mailbox(es) with SENTDATA bit = "1"</p>
0	NDST	0	R	<p>NEWDATA Status Flag</p> <p>The NDST bit is set to "1" when at least one NEWDATA bit in the CiMCTLj register is "1" regardless of the value of the CiMIER register. The NDST bit is set to "0" when all NEWDATA bits are "0".</p> <p>0: No mailbox with NEWDATA bit = "1"</p> <p>1: Mailbox(es) with NEWDATA bit = "1"</p>

**38.3.15 CANi Mailbox Search Mode Register (CiMSMR) (i = 0, 1)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Write to the CiMSMR register in CAN operation mode or CAN halt mode.

CAN0 Mailbox Search Mode Register (C0MSMR)

CAN1 Mailbox Search Mode Register (C1MSMR)

Bit:	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	MBSM	
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W

<After Reset: H'00>

Bit	Symbol	Initial Value	R/W	Description
7 to 2	—	All 0	R	Reserved bits These bits are always read as 0. The write value should always be 0. Operation is not guaranteed if a value other than 0 is written to these bits.
1, 0	MBSM	All 0	R/W	Mailbox Search Mode Select Bits The MBSM bit selects the search mode for the mailbox search function. When the MBSM bit is "00", receive mailbox search mode is selected. In this mode, the search targets are the NEWDATA bit in the CiMCTLj register (j = 0 to 63) for the normal mailbox and the RFEST bit in the CiRFCR register. When the MBSM bit is "01", transmit mailbox search mode is selected. In this mode, targets the SENTDATA bit in the CiMCTLj register. When the MBSM bit is "10", message lost search mode is selected. In this mode, targets the MSGLOST bit in the CiMCTLj register for the normal mailbox and the RFMLF bit in the CiRFCR register. When the MBSM bit is "11", channel search mode is selected. In this mode, the search target is the CiCSSR register. Refer to section 38.3.17, CANi Channel Search Support Register (CiCSSR) (i = 0, 1). 00: Receive mailbox search mode 01: Transmit mailbox search mode 10: Message lost search mode 11: Channel search mode

### 38.3.16 CANi Mailbox Search Status Register (CiMSSR) (i = 0, 1)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CAN0 Mailbox Search Status Register (C0MSSR)

CAN1 Mailbox Search Status Register (C1MSSR)

Bit:	7	6	5	4	3	2	1	0
	SEST	—	MBNST					
Initial value:	1	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R

<After Reset: H'80>

Bit	Symbol	Initial Value	R/W	Description
7	SEST	1	R	<p>Search Result Status Bit</p> <p>The SEST bit is set to "1" when no corresponding mailbox is found after searching all mailboxes. For example, in transmit mailbox search mode, the SEST bit is set to "1" when no SENTDATA bit for mailboxes is "1". The SEST bit is set to "0" when at least one SENTDATA bit is "1". When the SEST bit is "1", the value of the MBNST bits is undefined.</p> <p>0: Search result found 1: No search result</p>
6	—	0	R	<p>Reserved bit</p> <p>This bit is always read as 0. The write value should always be 0. Operation is not guaranteed if a value other than 0 is written to this bit.</p>
5 to 0	MBNST	All 0	R	<p>Search Result Mailbox Number Status Bits</p> <p>The MBNST bit outputs the smallest mailbox number that is searched in each mode of the CiMSMR register. In receive mailbox, transmit mailbox, and message lost search modes, the value of the mailbox i.e., the search result to be output, is updated as described below:</p> <p>When the NEWDATA, SENTDATA or MSGLOST bit for the output mailbox is set to "0".</p> <p>When the NEWDATA, SENTDATA or MSGLOST bit for a higher-priority mailbox is set to "1".</p> <p>In receive mailbox search and message lost search modes, the receive FIFO (mailbox [60]) is output when the receive FIFO is not empty and there are no unread received messages or no lost messages in any of the normal mailboxes (mailboxes [0] to [55]). In transmit mailbox search mode, the transmit FIFO (mailbox [56]) is not output. Table 38.7 lists the behavior of MBNST bit in FIFO mailbox mode.</p> <p>In channel search mode, the MBNST bit outputs the corresponding channel number. After the CiMSSR register is read by a program, the next target channel number is output.</p>

**Table 38.7 Operation of MBNST Bit in FIFO Mailbox Mode**

MBSM Bit	Mailbox [56] (Transmit FIFO)	Mailbox [60] (Receive FIFO)
"00"	Mailbox [56] is not output.	Mailbox [60] is output when no NEWDATA bit for the normal mailbox is set to "1" and the receive FIFO is not empty.
"01"		Mailbox [60] is not output.
"10"		Mailbox [60] is output when no MSGLOST bit for the normal mailbox is set to "1" and the RFMLF bit is set to "1" (receive FIFO message lost has occurred) in the receive FIFO.
"11"		Mailbox [60] is not output.

**38.3.17 CANi Channel Search Support Register (CiCSSR) (i = 0, 1)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

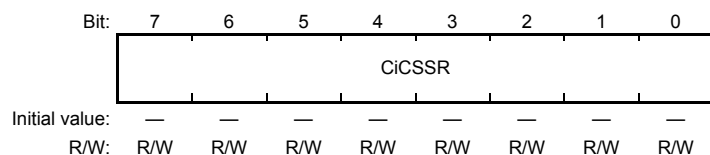
The bits in the CiCSSR register, which are set to "1", are encoded by an 8/3 encoder (the lower bit position, the higher priority) and output to the MBNST bits in the CiMSSR register.

The CiMSSR register outputs the updated value whenever the CiMSSR register is read by a program.

Write to the CiCSSR register only when the MBSM bit in the CiMSMR register is "11" (channel search mode). Write to this register in CAN operation mode or CAN halt mode.

CAN0 Channel Search Support Register (C0CSSR)

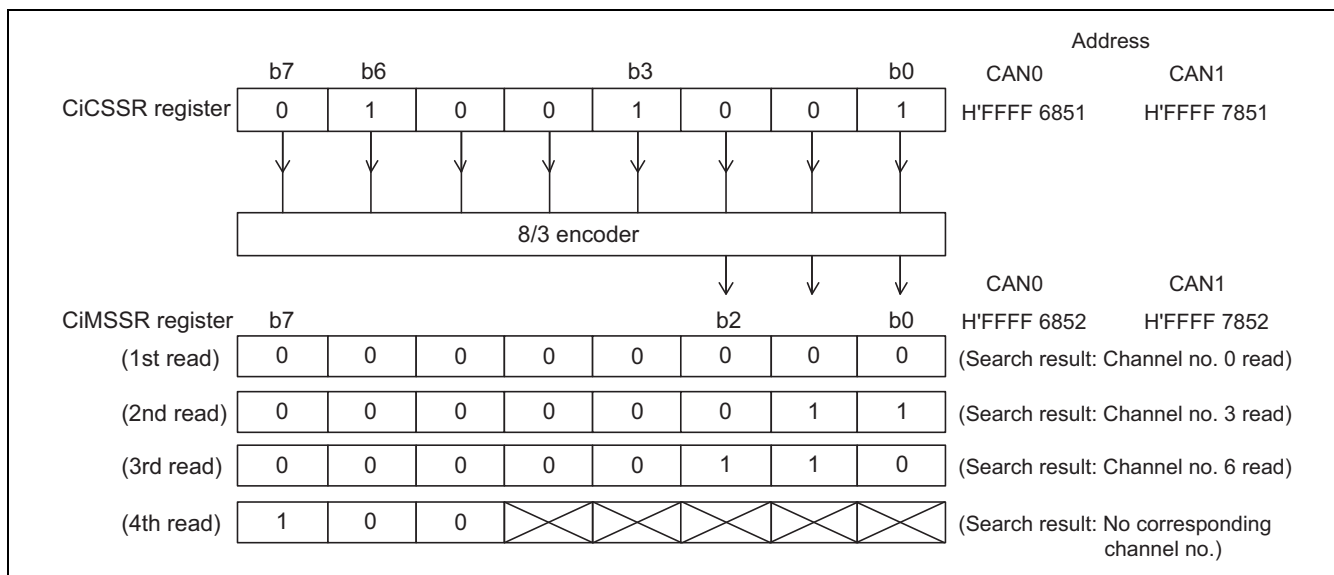
CAN1 Channel Search Support Register (C1CSSR)



<After Reset: Undefined>

Bit	Symbol	Initial Value	R/W	Description
7 to 0	CiCSSR	Undefined	R/W	When the value for the channel search is input, the channel number is output to the CiMSSR register.

Figure 38.4 shows the write and read of registers CiCSSR and CiMSSR.



**Figure 38.4 Write and Read of Registers CiCSSR and CiMSSR (i = 0, 1)**

The value of the CiCSSR register is also updated whenever the CiMSSR register is read. When the CiCSSR register is read, the value before the 8/3 encoder conversion is read.

**38.3.18 CANi Acceptance Filter Support Register (CiAFSR) (i = 0, 1)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

The acceptance filter support unit (ASU) can be used for data table (8 bits × 256) search. In the data table, all standard IDs created by the user are set to be valid/invalid in bit units. When the CAFSR register is written with the 16-bit unit data including the SID bit in the CiMBj register (j = 0 to 63), in which a received ID is stored, a decoded row (byte offset) position and column (bit) position for data table search can be read. The ASU can be used for standard (11-bit) IDs only.

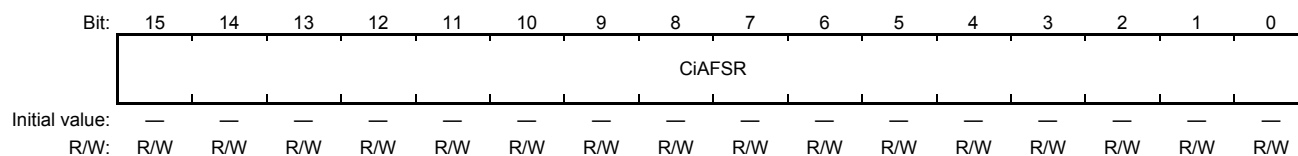
The ASU is enabled in the following cases:

- When the ID to receive cannot be masked by the acceptance filter.  
(Example) IDs to receive: H'078, H'087, H'111
- When there are too many IDs to receive and software filtering time is expected to be shortened.

Write to the CiAFSR register in CAN operation mode or CAN halt mode.

CAN0 Acceptance Filter Support Register (C0AFSR)

CAN1 Acceptance Filter Support Register (C1AFSR)

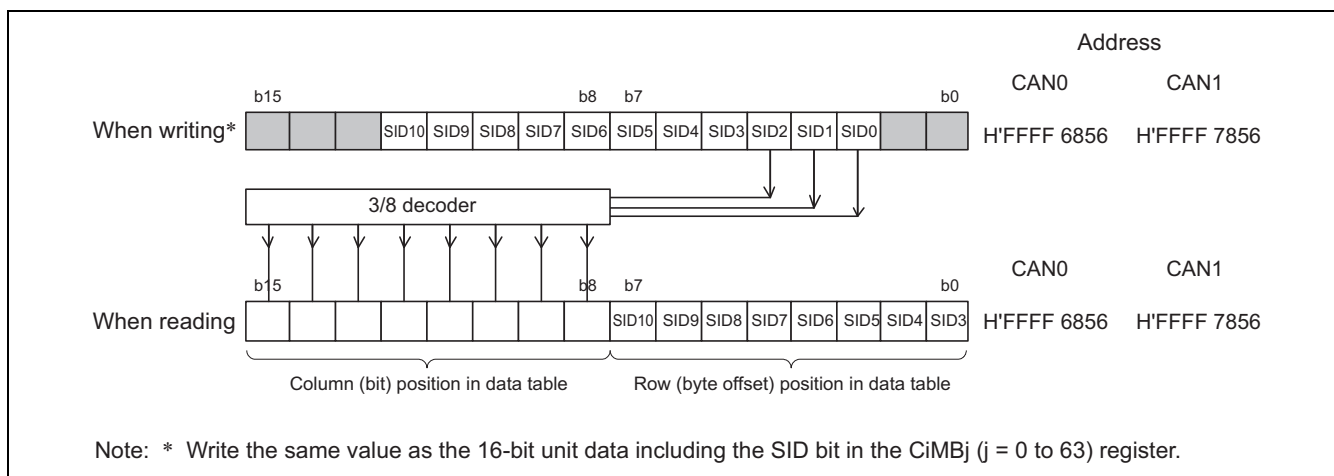


<After Reset: Undefined>

Bit	Symbol	Initial Value	R/W	Description
15 to 0	CiAFSR	Undefined	R/W	After the standard ID of a received message is written, the value converted for data table search can be read.



Figure 38.5 shows the write and read of CiAFSR register.



**Figure 38.5 Write and Read of CiAFSR Register (i = 0, 1)**

**38.3.19 CANi Error Interrupt Enable Register (CiEIER) (i = 0, 1)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

The CiEIER register is used to set the error interrupt enabled/disabled individually for each error interrupt source in the CiEIFR register.

Write to the CiEIER register in CAN reset mode.

CAN0 Error Interrupt Enable Register (C0EIER)

CAN1 Error Interrupt Enable Register (C1EIER)

Bit:	7	6	5	4	3	2	1	0
	BLIE	OLIE	ORIE	BORIE	BOEIE	EPIE	EWIE	BEIE
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

<After Reset: H'00>

Bit	Symbol	Initial Value	R/W	Description
7	BLIE	0	R/W	Bus Lock Interrupt Enable Bit When the BLIE bit is "0", no error interrupt request is generated even if the BLIF bit in the CiEIFR register is set to "1". When the BLIE bit is "1", an error interrupt request is generated if the BLIF bit is set to "1". 0: Bus lock interrupt disabled 1: Bus lock interrupt enabled

Bit	Symbol	Initial Value	R/W	Description
6	OLIE	0	R/W	<p>Overload Frame Transmit Interrupt Enable Bit</p> <p>When the OLIE bit is "0", no error interrupt request is generated even if the OLIF bit in the CiEIFR register is set to "1".</p> <p>When the OLIE bit is "1", an error interrupt request is generated if the OLIF bit is set to "1".</p> <p>0: Overload frame transmit interrupt disabled 1: Overload frame transmit interrupt enabled</p>
5	ORIE	0	R/W	<p>Receive Overrun Interrupt Enable Bit</p> <p>When the ORIE bit is "0", an error interrupt request is not generated even if the ORIF bit in the CiEIFR register is set to "1".</p> <p>When the ORIE bit is "1", an error interrupt request is generated if the ORIF bit is set to "1".</p> <p>0: Receive overrun interrupt disabled 1: Receive overrun interrupt enabled</p>
4	BORIE	0	R/W	<p>Bus-Off Recovery Interrupt Enable Bit</p> <p>When the BORIE bit is "0", an error interrupt request is not generated even if the BORIF bit in the CiEIFR register is set to "1". When the BORIE bit is set to "1", an error interrupt request is generated if the BORIF bit is set to "1".</p> <p>0: Bus-off recovery interrupt disabled 1: Bus-off recovery interrupt enabled</p>
3	BOEIE	0	R/W	<p>Bus-Off Entry Interrupt Enable Bit</p> <p>When the BOEIE bit is "0", no error interrupt request is generated even if the BOEIF bit in the CiEIFR register is set to "1".</p> <p>When the BOEIE bit is "1", an error interrupt request is generated if the BOEIF bit is set to "1".</p> <p>0: Bus-off entry interrupt disabled 1: Bus-off entry interrupt enabled</p>
2	EPIE	0	R/W	<p>Error-Passive Interrupt Enable Bit</p> <p>When the EPIE bit is "0", no error interrupt request is generated even if the EPIF bit in the CiEIFR register is set to "1".</p> <p>When the EPIE bit is "1", an error interrupt request is generated if the EPIF bit is set to "1".</p> <p>0: Error-passive interrupt disabled 1: Error-passive interrupt enabled</p>
1	EWIE	0	R/W	<p>Error-Warning Interrupt Enable Bit</p> <p>When the EWIE bit is "0", no error interrupt request is generated even if the EWIF bit in the CiEIFR register is set to "1".</p> <p>When the EWIE bit is "1", an error interrupt request is generated if the EWIF bit is set to "1".</p> <p>0: Error-warning interrupt disabled 1: Error-warning interrupt enabled</p>

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Bit	Symbol	Initial Value	R/W	Description
0	BEIE	0	R/W	Bus Error Interrupt Enable Bit When the BEIE bit is "0", no error interrupt request is generated even if the BEIF bit in the CiEIFR register is set to "1". When the BEIE bit is "1", an error interrupt request is generated if the BEIF bit is set to "1". 0: Bus error interrupt disabled 1: Bus error interrupt enabled

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**38.3.20 CANi Error Interrupt Factor Judge Register (CiEIFR) (i = 0, 1)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

If an event corresponding to each bit occurs, the corresponding bit in the CiEIFR register is set to "1" regardless of the setting of the CiEIER register.

To set each bit to "0", write "0" by a program. If the set timing occurs simultaneously with the clear timing by the program, the bit becomes "1".

When writing "0" to a single bit by a program, only the specified bit is set to "0" and the other bits are set to "1". Writing "1" has no effect to these bit values.

CAN0 Error Interrupt Factor Judge Register (C0EIFR)

CAN1 Error Interrupt Factor Judge Register (C1EIFR)

Bit:	7	6	5	4	3	2	1	0
	BLIF	OLIF	ORIF	BORIF	BOEIF	EPIF	EWIF	BEIF
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

<After Reset: H'00>

Bit	Symbol	Initial Value	R/W	Description
7	BLIF	0	R/W	<b>Bus Lock Detect Flag*</b> The BLIF bit becomes 1 if 32 consecutive dominant bits are detected on the CAN bus while the CAN module is in CAN operation mode. After the BLIF bit becomes 1, bus lock can be detected again after either of the following conditions is satisfied: <ul style="list-style-type: none"> <li>• After this bit is set to 0 from 1, recessive bits are detected (bus lock is resolved).</li> <li>• After this bit is set to 0 from 1, the CAN module enters CAN reset mode and then enters CAN operation mode again (internal reset).0: No bus lock detected 1: Bus lock detected</li> </ul>
6	OLIF	0	R/W	<b>Overload Frame Transmission Detect Flag*</b> The OLIF bit is set to "1" if the transmitting condition of an overload frame is detected when the CAN module performs transmission or reception. 0: No overload frame transmission detected 1: Overload frame transmission detected
5	ORIF	0	R/W	<b>Receive Overrun Detect Flag*</b> The ORIF bit is set to "1" when a receive overrun occurs. This bit is not to set to "1" in overwrite mode. In overwrite mode, a reception complete interrupt request is generated if an overwrite condition occurs and the ORIF bit is not set to "1". In normal mailbox mode, if an overrun occurs in any of mailboxes [0] to [63] in overrun mode, this bit is set to "1". In FIFO mailbox mode, if an overrun occurs in any of mailboxes [0] to [55] or the receive FIFO in overrun mode, this bit is set to "1". 0: No receive overrun detected 1: Receive overrun detected

Bit	Symbol	Initial Value	R/W	Description
4	BORIF	0	R/W	<p>Bus-Off Recovery Detect Flag*</p> <p>The BORIF bit is set to "1" when the CAN module recovers from the bus-off state normally by detecting 11 consecutive bits 128 times in the following conditions:</p> <p>When the BOM bit in the CiCTLR register is "00".</p> <p>When the BOM bit is "10".</p> <p>When the BOM bit is "11".</p> <p>The BORIF bit is not set to "1" if the CAN module recovers from the bus-off state in the following conditions:</p> <p>When the CANM bit in the CiCTLR register is set to "01" or "11" (CAN reset mode).</p> <p>When the RBOC bit in the CiCTLR register is set to "1" (forcible return from bus-off).</p> <p>When the BOM bit is "01".</p> <p>When the BOM bit is "11" and the CANM bit is set to "10" (CAN halt mode) before normal recovery occurs.</p> <p>0: No bus-off recovery detected 1: Bus-off recovery detected</p>
3	BOEIF	0	R/W	<p>Bus-Off Entry Detect Flag*</p> <p>The BOEIF bit is set to "1" when the CAN error state becomes bus-off (the TEC value exceeds 255).</p> <p>The BOEIF bit is also set to "1" when the BOM bit in the CiCTLR register is "01" (entry to CAN halt mode automatically at bus-off entry) and the CAN module becomes the bus-off state.</p> <p>0: No bus-off entry detected 1: Bus-off entry detected</p>
2	EPIF	0	R/W	<p>Error Passive Detect Flag*</p> <p>The EPIF bit is set to "1" when the CAN error state becomes error-passive (the REC or TEC value exceeds 127).</p> <p>The EPIF bit is set to "1" only when the REC or TEC initially exceeds 127. Thus, if "0" is written to the EPIF bit by a program while the REC or TEC remains greater than 127, the EPIF bit is not set to "1" until the REC and TEC goes below 127 and then exceeds 127 again.</p> <p>0: No error passive detected 1: Error passive detected</p>
1	EWIF	0	R/W	<p>Error Warning Detect Flag*</p> <p>The EWIF bit is set to "1" when the value of the receive error counter (REC) or transmit error counter (TEC) exceeds 95.</p> <p>The EWIF bit is set to "1" only when the REC or TEC initially exceeds 95. Thus, if "0" is written to the EWIF bit by a program while the REC or TEC remains greater than 95, the EWIF bit is not set to "1" until the REC and TEC goes below 95 and then exceeds 95 again.</p> <p>0: No error warning detected 1: Error warning detected</p>
0	BEIF	0	R/W	<p>Bus Error Detect Flag*</p> <p>The BEIF bit is set to "1" when a bus error is detected.</p> <p>0: No bus error detected 1: Bus error detected</p>

Note: \* Only "0" may be written to this bit. (Writing "1" has no effect.) When writing "0" to specific bits in software, write "0" to each bit to be cleared to "0" and "1" to all other bits.

Table 38.8 lists the behavior of bits BOEIF and BORIF according to BOM bit setting value.

**Table 38.8 Behavior of Bits BOEIF and BORIF according to BOM Bit Setting Value**

<b>BOM Bit</b>	<b>BOEIF Bit</b>	<b>BORIF Bit</b>
00	Set to "1" on entry to the bus-off state.	Set to "1" on exit from the bus-off state.
01		Do not set to "1".
10		Set to "1" on exit from the bus-off state.
11		Set to "1" if normal bus-off recovery occurs before the CANM bit is set to "10" (CAN halt mode).

**38.3.21 CANi Receive Error Count Register (CiRECR) (i = 0, 1)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

The CiRECR register indicates the value of the receive error counter.

For the increment/decrement conditions of the receive error counter, refer to the CAN Specifications (ISO11898-1).

The value in bus-off state is undefined.

CAN0 Receive Error Count Register (C0RECR)

CAN1 Receive Error Count Register (C1RECR)



<After Reset: H'00>

Bit	Symbol	Initial Value	R/W	Description
7 to 0	CiRECR	All 0	R	Receive Error Count Function The CiRECR register increments or decrements the counter value according to error status of the CAN module during reception.

**38.3.22 CANi Transmit Error Count Register (CiTECR) (i = 0, 1)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

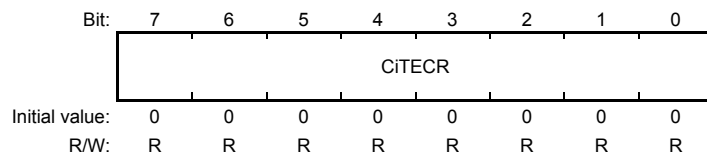
The CiTECR register indicates the value of the transmit error counter.

For the increment/decrement conditions of the transmit error counter, refer to the CAN Specifications (ISO11898-1).

The value in bus-off state is undefined.

CAN0 Transmit Error Count Register (C0TECR)

CAN1 Transmit Error Count Register (C1TECR)



<After Reset: H'00>

Bit	Symbol	Initial Value	R/W	Description
7 to 0	CiTECR	All 0	R	Transmit Error Count Function The CiTECR register increments or decrements the counter value according to error status of the CAN module during transmission.



**38.3.23 CANi Error Code Store Register (CiECSR) (i = 0, 1)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

The CiECSR register can be used to monitor whether an error has occurred on the CAN bus. Refer to the CAN Specifications (ISO11898-1) to check the generation conditions of each error.

To set each bit except the EDPM bit to "0", write "0" by a program. If the timing at which each bit is set to "1" and the timing at which "0" is written by a program are the same, the relevant bit is set to "1".

CAN0 Error Code Store Register (C0ECSR)

CAN1 Error Code Store Register (C1ECSR)

Bit:	7	6	5	4	3	2	1	0
	EDPM	ADEF	BE0F	BE1F	CEF	AEF	FEF	SEF
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

<After Reset: H'00>

Bit	Symbol	Initial Value	R/W	Description
7	EDPM	0	R/W	<p>Error Display Mode Select Bit*1*2</p> <p>The EDPM bit selects the output mode of the CiECSR register.</p> <p>When the EDPM bit is set to "0", the CiECSR register outputs the first error code.</p> <p>When the EDPM bit is set to "1", the CiECSR register outputs the accumulated error code.</p> <p>0: Output of first detected error code 1: Output of accumulated error code</p>
6	ADEF	0	R/W	<p>ACK Delimiter Error Flag*3*4</p> <p>The ADEF bit is set to "1" when a form error is detected with the ACK delimiter during transmission.</p> <p>0: No ACK delimiter error detected 1: ACK delimiter error detected</p>
5	BE0F	0	R/W	<p>Bit Error (dominant) Flag*3*4</p> <p>The BE0F bit is set to "1" when a dominant bit error is detected.</p> <p>0: No bit error (dominant) detected 1: Bit error (dominant) detected</p>
4	BE1F	0	R/W	<p>Bit Error (recessive) Flag*3*4</p> <p>The BE1F bit is set to "1" when a recessive bit error is detected.</p> <p>0: No bit error (recessive) detected 1: Bit error (recessive) detected</p>
3	CEF	0	R/W	<p>CRC Error Flag*3*4</p> <p>The CEF bit is set to "1" when a CRC error is detected.</p> <p>0: No CRC error detected 1: CRC error detected</p>

Bit	Symbol	Initial Value	R/W	Description
2	AEF	0	R/W	ACK Error Flag*3*4 The AEF bit is set to "1" when an ACK error is detected. 0: No ACK error detected 1: ACK error detected
1	FEF	0	R/W	Form Error Flag*3*4 The FEF bit is set to "1" when a form error is detected. 0: No form error detected 1: Form error detected
0	SEF	0	R/W	Stuff Error Flag*3*4 The SEF bit is set to "1" when a stuff error is detected. 0: No stuff error detected 1: Stuff error detected

- Notes:
1. Write to the EDPM bit in CAN reset mode or CAN halt mode.
  2. If more than one error condition is detected simultaneously, all related bits are set to "1".
  3. Writing "1" has no effect to these bit values.
  4. When writing "0" to bits SEF, FEF, AEF, CEF, BE1F, BE0F, and ADEF by a program, only the specified bit is set to "0" and the other bits are set to "1".

**38.3.24 CANi Time Stamp Register (CiTSR) (i = 0, 1)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

When the CiTSR register is read, the value of the time stamp counter (16-bit free-running counter) at that moment is read.

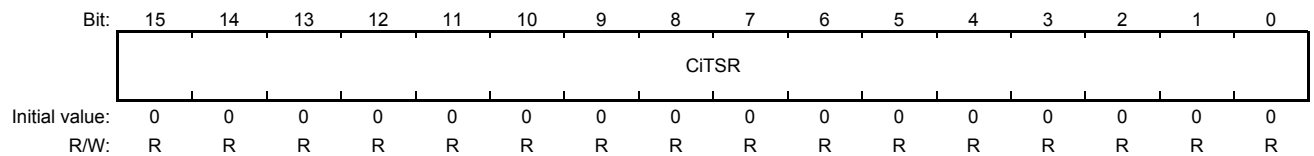
The value of the time stamp counter reference clock is a multiple of 1 bit time, as configured by the TSPS bit in the CiCTRL register.

The time stamp counter stops in CAN sleep mode and CAN halt mode, and is initialized in CAN reset mode.

The time stamp counter value is stored to TSL and TSH in the CiMBj register when a received message is stored in a receive mailbox.

CAN0 Time Stamp Register (C0TSR)

CAN1 Time Stamp Register (C1TSR)



<After Reset: H'0000>

Bit	Symbol	Initial Value	R/W	Description
15 to 0	CiTSR	All 0	R	Free-running counter value for the time stamp function

Note: Read the CiTSR register in 16-bit units.

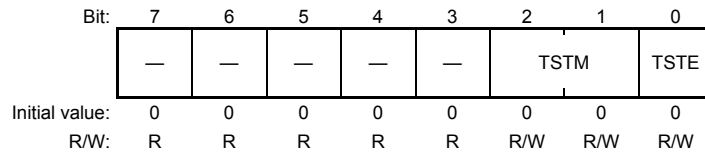
**38.3.25 CANi Test Control Register (CiTCR) (i = 0, 1)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Write to the CiTCR register in CAN halt mode only.

CAN0 Test Control Register (C0TCR)

CAN1 Test Control Register (C1TCR)



<After Reset: H'00>

Bit	Symbol	Initial Value	R/W	Description
7 to 3	—	All 0	R	Reserved bits These bits are always read as 0. The write value should always be 0. Operation is not guaranteed if a value other than 0 is written to these bits.
2, 1	TSTM	All 0	R/W	CAN Test Mode Select Bits The TSTM bit selects the CAN test mode. For details on the CAN test modes, see section 38.3.25 (1), Listen-Only Mode, section 38.3.25 (2), Self-Test Mode 0 (External Loop Back), and section 38.3.25 (3), Self-Test Mode 1 (Internal Loop Back). 00: Other than CAN test mode 01: Listen-only mode 10: Self-test mode 0 (external loop back) 11: Self-test mode 1 (internal loop back)
0	TSTE	0	R/W	CAN Test Mode Enable Bit When the TSTE bit is set to "0", CAN test mode is disabled. When the TSTE bit is set to "1", CAN test mode is enabled. 0: CAN test mode disabled 1: CAN test mode enabled

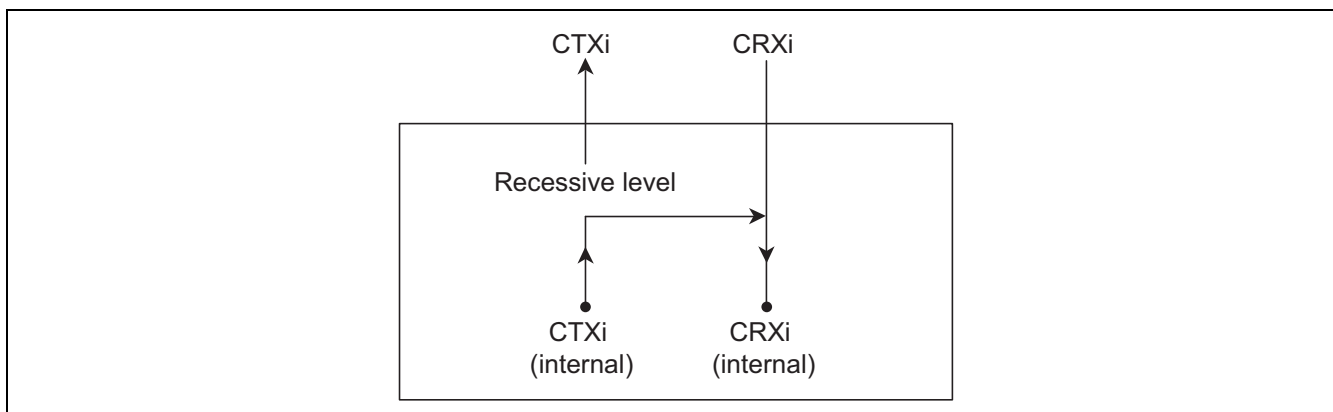
**(1) Listen-Only Mode**

The ISO 11898-1 recommends an optional bus monitoring mode. In listen-only mode, the CAN node is able to receive valid data frames and valid remote frames. It sends only recessive bits on the CAN bus, and the protocol controller is not required to send the ACK bit, overload flag, or active error flag.

Listen-only mode can be used for baud rate detection.

Do not request transmission from any mailboxes in this mode.

Figure 38.6 shows the connection when listen-only mode is selected.



**Figure 38.6 Connection when Listen-Only Mode is Selected**

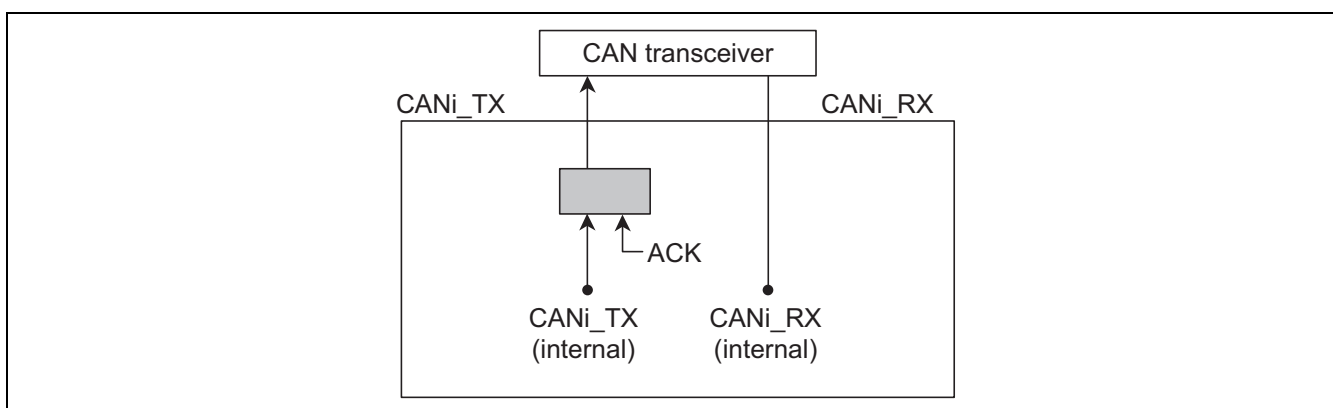
**(2) Self-Test Mode 0 (External Loop Back)**

Self-test mode 0 is provided for CAN transceiver tests.

In this mode, the protocol controller treats its own transmitted messages as messages received via the CAN transceiver and stores them into the receive mailbox. To be independent from external stimulation, the protocol controller generates the ACK bit.

Connect the CANi\_TX/CANi\_RX pins to the transceiver.

Figure 38.7 shows the connection when self-test mode 0 is selected.



**Figure 38.7 Connection when Self-Test Mode 0 is Selected**

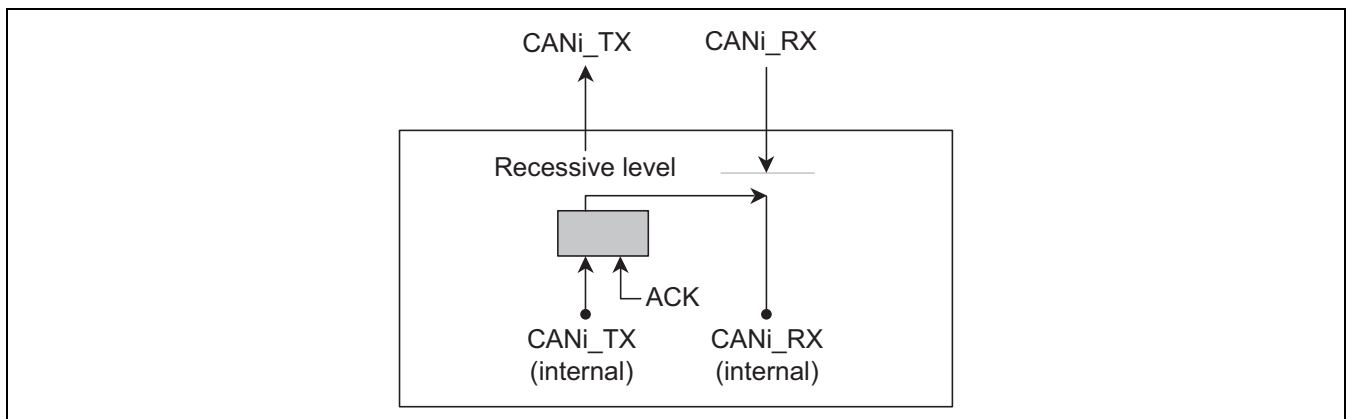
### (3) Self-Test Mode 1 (Internal Loop Back)

Self-test mode 1 is provided for self-test functions.

In this mode, the protocol controller treats its transmitted messages as received messages and stores them into the receive mailbox. To be independent from external stimulation, the protocol controller generates the ACK bit.

In self-test mode 1, the protocol controller performs an internal feedback from the internal CANi\_TX pin to the internal CANi\_RX pin. The input value of the external CANi\_RX pin is ignored. The external CANi\_TX pin outputs only recessive bits. The CANi\_TX/CANi\_RX pins do not need to be connected to the CAN bus or any external device.

Figure 38.8 shows the connection when self-test mode 1 is selected.



**Figure 38.8 Connection when Self-Test Mode 1 is Selected**

**38.3.26 CANi Interrupt Status Register (CiISR) (i = 0, 1)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

The CiISR register shows interrupt sources before masking by the CiIER register.

CAN0 Interrupt Status Register (C0ISR)

CAN1 Interrupt Status Register (C1ISR)

Bit:	7	6	5	4	3	2	1	0
	—	—	ERSF	RXFF	TXFF	RX MOF	RXM1F	TXMF
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R/W	R/W	R	R

<After Reset: H'00>

Bit	Symbol	Initial Value	R/W	Description
7, 6	—	All 0	R	Reserved bits These bits are always read as 0. The write value should always be 0. Operation is not guaranteed if a value other than 0 is written to these bits.
5	ERSF	0	R	Error (ERS) Interrupt Status Bit* <sup>1</sup> The ERSF bit shows the error interrupt source status. 0: ERS interrupt source not detected 1: ERS interrupt source detected
4	RXFF	0	R/W	Reception FIFO (RXF) Interrupt Status Bit* <sup>2</sup> The RXFF bit shows the FIFO receive interrupt source status. 0: RXF interrupt source not detected 1: RXF interrupt source detected The RXFF is cleared to "0" by writing "0" to it by software. (writing "1" has no effect)
3	TXFF	0	R/W	Transmission FIFO (TXF) Interrupt Status Bit* <sup>3</sup> The TXFF bit shows the FIFO transmit interrupt source status. 0: TXF interrupt source not detected 1: TXF interrupt source detected The TXFF is cleared to "0" by writing "0" to it by software. (writing "1" has no effect)
2	RXM0F	0	R	Mailbox 0 Successful Reception (RXM0) Interrupt Status Bit* <sup>4</sup> The RXM0F bit shows the successful reception interrupt source status for mailbox 0. 0: RXM0 interrupt source not detected 1: RXM0 interrupt source detected
1	RXM1F	0	R	Mailbox 1 to 63 Successful Reception (RXM1) Interrupt Status Bit* <sup>5</sup> The RXM1F bit shows the successful reception interrupt source status for mailboxes 1 to 63. 0: RXM1 interrupt source not detected 1: RXM1 interrupt source detected

Bit	Symbol	Initial Value	R/W	Description
0	TXMF	0	R	Mailbox 32 to 63 Successful Transmission (TXM) Interrupt Status Bit* <sup>6</sup> The TXMF bit shows the successful transmission interrupt source status for mailboxes 32 to 63. 0: TXM interrupt source not detected 1: TXM interrupt source detected

- Notes:
1. The ERSF bit is set to "1" when a bit in one of the CiEIFR[j] registers is set to "1" due to a communication error while the corresponding bit in the CiEIER[j] register is set to "1" (j = 0 to 7).
  2. The RXFF bit is set to "1" when bit 6 or 5 in the CiRFCR register is set to "1" because of a reception FIFO full or warning condition due to the setting of CiMIER[61].
  3. The TXFF bit is set to "1" when the transmission FIFO message count reaches the specified value due to the setting of CiMIER[57].
  4. After the NEWDATA bit in CiMCTL0 is set to "1" at the end of a receive operation, the RXM0F bit is set to "1" if storing of the receive data is complete (corresponding INVALIDDATA bit value changed from "1" to "0") and the CiMIER0[0] bit has been set to "1".
  5. After the NEWDATA bit in CiMCTLj is set to "1" at the end of a receive operation, the RXM1F bit is set to "1" if storing of the receive data is complete (corresponding INVALIDDATA bit value changed from "1" to "0") and the bit in CiMIER0 or CiMIER1 corresponding to mailbox j has the been set to "1" (j = 1 to 63).
  6. The TXMF bit is set to "1" when the bit in the CiMIER1 register corresponding to mailbox j is set to "1" while the value of the SENTDATA bit in the CiMCTLj register is "1" following a successful reception (j = 32 to 63).



**38.3.27 CANi Interrupt Enable Register (CiIER) (i = 0, 1)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

The CiIER register can be used by an application to cause some interrupts to be ignored while processing by an interrupt service routine is taking place. Each bit affects the individual interrupt source corresponding to it.

CAN0 Interrupt Enable Register (C0IER)

CAN1 Interrupt Enable Register (C1IER)

Bit:	7	6	5	4	3	2	1	0
	—	—	ERSIE	RXFIE	TXFIE	RXM0IE	RXM1IE	TXMIE
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W

<After Reset: H'00>

Bit	Symbol	Initial Value	R/W	Description
7, 6	—	All 0	R	Reserved bits These bits are always read as 0. The write value should always be 0. Operation is not guaranteed if a value other than 0 is written to these bits.
5	ERSIE	0	R/W	Error (ERS) Interrupt Enable Bit The ERSIE bit enables or disables the ERS interrupt controller. 0: ERS interrupt disabled 1: ERS interrupt enabled
4	RXFIE	0	R/W	Reception FIFO (RXF) Interrupt Enable Bit The RXFIE bit enables or disables the RXF interrupt controller. 0: RXF interrupt disabled 1: RXF interrupt enabled
3	TXFIE	0	R/W	Transmission FIFO (TXF) Interrupt Enable Bit The TXFIE bit enables or disables the TXF interrupt controller. 0: TXF interrupt disabled 1: TXF interrupt enabled
2	RXM0IE	0	R/W	Mailbox 0 Successful Reception (RXM0) Interrupt Enable Bit The RXM0IE bit enables or disables the RXM0 interrupt controller. 0: RXM0 interrupt disabled 1: RXM0 interrupt enabled
1	RXM1IE	0	R/W	Mailbox 1 to 63 Successful Reception (RXM1) Interrupt Enable Bit The RXM1IE bit enables or disables the RXM1 interrupt controller. 0: RXM1 interrupt disabled 1: RXM1 interrupt enabled
0	TXMIE	0	R/W	Mailbox 32 to 63 Successful Transmission (TXM) Interrupt Enable Bit The TXMIE bit enables or disables the TXM interrupt controller. 0: TXM interrupt disabled 1: TXM interrupt enabled

**38.3.28 CANi Mailbox Search Mask Register (CiMBSMR) (i = 0, 1)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Write to the CiMBSMR register in CAN halt mode only.

CAN0 Mailbox Search Mask Register (C0MBSMR)

CAN1 Mailbox Search Mask Register (C1MBSMR)

Bit:	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	MB0 SM
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W

<After Reset: H'00>

Bit	Symbol	Initial Value	R/W	Description
7 to 1	—	All 0	R	Reserved bits These bits are always read as 0. The write value should always be 0. Operation is not guaranteed if a value other than 0 is written to these bits.
0	MB0SM	0	R/W	Mailbox 0 Search Mask Bit* When the MB0SM bit is set to "1", message box 0 is excluded from the search target for the CANi mailbox search status register.

Note: \* The MB0SM bit is enabled in the search modes except channel search mode. In the RXM1 interrupt handling, this bit is usable to exclude message box 0 from the search target for the CiMSSR register in receive mailbox search mode.

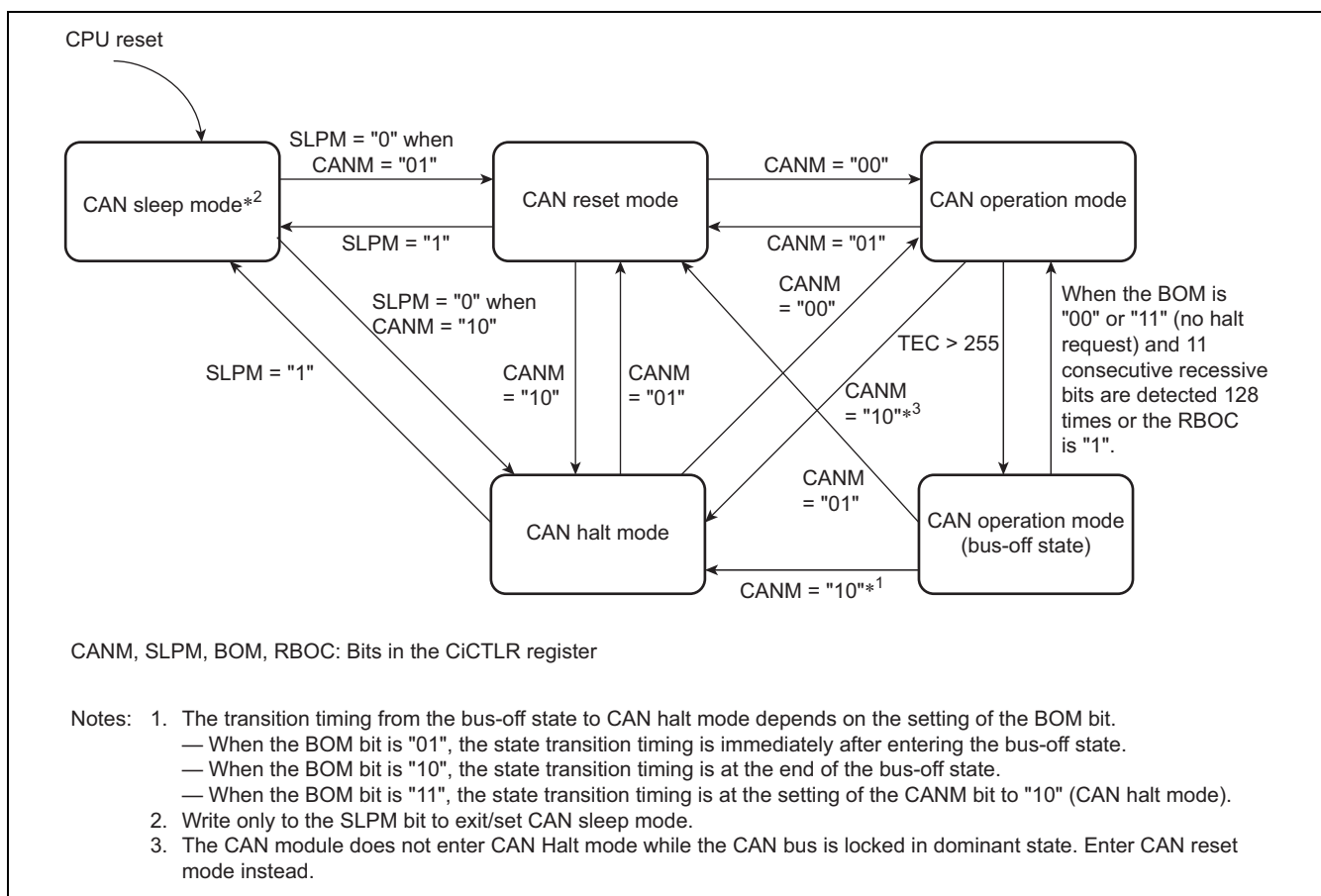
RZ/G1H	RZ/G1N
RZ/G1M	RZ/G1E

### 38.4 Operating Mode

The CAN module has the following four operating modes.

- CAN reset mode
- CAN halt mode
- CAN operation mode
- CAN sleep mode

Figure 38.9 shows the transition between CAN operating modes.



**Figure 38.9 Transition between CAN Operating Modes (i = 0, 1)**

### 38.4.1 CAN Reset Mode

CAN reset mode is provided for CAN communication configuration.

When the CANM bit in the CiCTLR register is set to "01" or "11", the CAN module enters CAN reset mode. Then the RSTST bit in the CiSTR register is set to "1". Do not change the CANM bit until the RSTST bit is set to "1". Configure the CiBCR register before exiting CAN reset mode to any other modes.

The following registers are initialized to their reset values after entering CAN reset mode and their initialized values are retained during CAN reset mode:

- CiMCTLj register
- CiSTR register (except bits SLPST and TFST)
- CiEIFR register
- CiRECR register
- CiTECR register
- CiTSR register
- CiMSSR register
- CiMSMR register
- CiRFCR register
- CiTFPCR register
- CiTCR register
- CiECSR register (except EDPM bit)
- CiISR register
- CiMBSMR register

The following registers retain their values after entering CAN reset mode.

- CiCLKR register
- CiCTLR register
- CiSTR register (bits SLPST and TFST)
- Registers CiMIER0 and CiMIER1
- CiEIER register
- CiBCR register
- CiCSSR register
- CiECSR register (EDPM bit only)
- CiMBj register
- Registers CiMKR0 to CiMKR9
- Registers CiFIDCR0 and CiFIDCR1
- Registers CiMKIVLR0 and CiMKIVLR1
- CiAFSR register
- CiRFPCR register
- CiTFPCR register
- CiIER register

### 38.4.2 CAN Halt Mode

CAN halt mode is used for mailbox configuration and test mode setting.

When the CANM bit in the CiCTLR register is set to "10", CAN halt mode is selected. Then the HLTST bit in the CiSTR register is set to "1". Do not change the CANM bit until the HLTST bit is set to "1".

Refer to Table 38.9, Operation in CAN Reset Mode and CAN Halt Mode regarding the state transition conditions when transmitting or receiving.

All registers except bits RSTST, HLTST, and SLPST in the CiSTR register remain unchanged when the CAN module enters CAN halt mode.

Do not change registers CiCLKR, CiCTLR (except bits CANM and SLPM), and CiEIER in CAN halt mode. The CiBCR register can be changed in CAN halt mode only when listen-only mode is selected to use for automatic bit rate detection.

**Table 38.9 Operation in CAN Reset Mode and CAN Halt Mode**

Mode	Receiver	Transmitter	Bus-Off
CAN reset mode	CAN module enters CAN reset mode without waiting for the end of message reception	CAN module enters CAN reset mode after waiting for the end of message transmission (1, 4)	CAN module enters CAN reset mode without waiting for the end of bus-off recovery
CAN halt mode	CAN module enters CAN halt mode after waiting for the end of message reception (2, 3)	CAN module enters CAN halt mode after waiting for the end of message transmission (1, 2, 4)	<ul style="list-style-type: none"> <li>When the BOM bit is "B'00" A halt request from a program will be acknowledged only after bus-off recovery</li> <li>When the BOM bit is "B'01" CAN module automatically enters CAN halt mode without waiting for the end of bus-off recovery (regardless of a halt request from a program)</li> <li>When the BOM bit is "B'10" CAN module automatically enters CAN halt mode after waiting for the end of bus-off recovery (regardless of a halt request from a program)</li> <li>When the BOM bit is "B'11" CAN module enters CAN halt mode (without waiting for the end of bus-off recovery) if a halt is requested by a program during bus-off</li> </ul>

BOM bit: Bit in the CiCTLR register (i = 0, 1)

- Notes:
- If several messages are requested to be transmitted, mode transition occurs after the completion of the first message transmission. When CAN reset mode is being requested during suspend transmission, mode transition occurs when the bus is idle, the next transmission ends, or the CAN module becomes a receiver.
  - If the CAN bus is locked in dominant state, the program can detect this state by monitoring the BLIF bit in the CiEIFR register. The CAN module does not enter CAN Halt mode while the CAN bus is locked in dominant state. Enter CAN reset mode instead.
  - If a CAN bus error occurs during reception after CAN halt mode is requested, the CAN module enters CAN halt mode. However, the CAN module does not enter CAN Halt mode when the CAN bus is locked in dominant state.
  - If a CAN bus error or arbitration lost occurs during transmission after CAN reset mode or CAN halt mode is requested, the CAN module enters the requested operating mode. However, the CAN module does not enter CAN Halt mode when the CAN bus is locked in dominant state.

### 38.4.3 CAN Sleep Mode

CAN sleep mode is used for reducing current consumption by stopping the clock supply to the CAN module. After MCU hardware reset or software reset, the CAN module starts from CAN sleep mode.

When the SLPM bit in the CiCTLR register is set to "1", the CAN module enters CAN sleep mode. Then the SLPST bit in the CiSTR register is set to "1". Do not change the value of the SLPM bit until the SLPST bit is set to "1". The other registers remain unchanged when the MCU enters CAN sleep mode.

Write to the SLPM bit in CAN reset mode and CAN halt mode. Do not change any registers (except the SLPM bit) during CAN sleep mode. Read operation is still allowed. When the SLPM bit is set to "0", the CAN module is released from CAN sleep mode. When the CAN module exits CAN sleep mode, the other registers remain unchanged.

### 38.4.4 CAN Operation Mode (Excluding Bus-Off State)

CAN operation mode is used for CAN communication.

When the CANM bit in the CiCTLR register is set to "B'00", the CAN module enters CAN operation mode.

Then bits RSTST and HLTST in the CiSTR register are set to "0". Do not change the value of the CANM bit until these bits are set to "0".

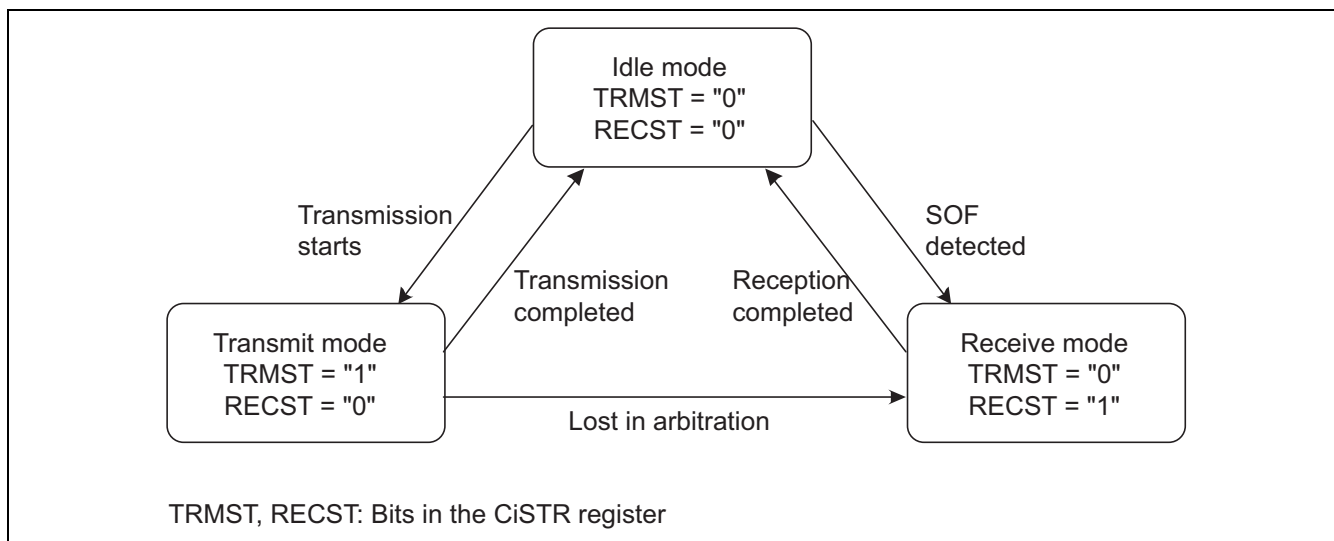
If 11 consecutive recessive bits are detected after entering CAN operation mode, the CAN module is in the following states:

- The CAN module becomes an active node on the network that enables transmission and reception of CAN messages.
- Error monitoring of the CAN bus, such as receive and transmit error counters, is performed.

During CAN operation mode, the CAN module may be in one of the following three sub-modes, depending on the status of the CAN bus:

- Idle mode: Transmission or reception is not being performed.
- Receive mode: A CAN message sent by another node is being received.
- Transmit mode: A CAN message is being transmitted. The CAN module may receive its own message simultaneously when self-test mode 0 (TSTM bit in the CiTCR register = "B'10") or self-test mode 1 (TSTM bit = "B'11") is selected.

Figure 38.10 shows the sub mode in CAN operation mode.



**Figure 38.10 Sub Mode in CAN Operation Mode (i = 0, 1)**

### 38.4.5 CAN Operation Mode (Bus-Off State)

The CAN module enters the bus-off state according to the increment/decrement rules for the transmit/error counters in the CAN Specifications.

The following cases apply when recovering from the bus-off state. When the CAN module is in bus-off state, the values of the associated registers, except registers CiSTR, CiEIFR, CiRECR, CiTECR and CiTSR, remain unchanged.

- When the BOM bit in the CiCTLR register is "B'00" (normal mode)
 

The CAN module enters the error-active state after it has completed the recovery from the bus-off state and CAN communication is enabled instantly. The BORIF bit in the CiEIFR register is set to "1" (bus-off recovery detected) at this time.
- When the RBOC bit in the CiCTLR register is set to "1" (forcible return from bus-off)
 

The CAN module enters the error-active state when it is in bus-off state and the RBOC bit is set to "1". CAN communication is enabled again after 11 consecutive recessive bits are detected. The BORIF bit is not set to "1" at this time.
- When the BOM bit is "B'01" (entry to CAN halt mode automatically at bus-off entry)
 

The CAN module enters CAN halt mode when it reaches the bus-off state. The BORIF bit is not set to "1" at this time.
- When the BOM bit is "B'10" (entry to CAN halt mode automatically at bus-off end)
 

The CAN module enters CAN halt mode when it has completed the recovery from bus-off. The BORIF bit is set to "1" at this time.
- When the BOM bit is "B'11" (entry to CAN halt mode by a program) and the CANM bit in the CiCTLR register is set to "B'10" (CAN halt mode) during the bus-off state
 

The CAN module enters CAN halt mode when it is in bus-off state and the CANM bit is set to "B'10" (CAN halt mode). The BORIF bit is not set to "1" at this time.

If the CANM bit is not set to "B'10" during bus-off, the same behavior as (1) applies.

### 38.5 CAN Communication Speed Configuration

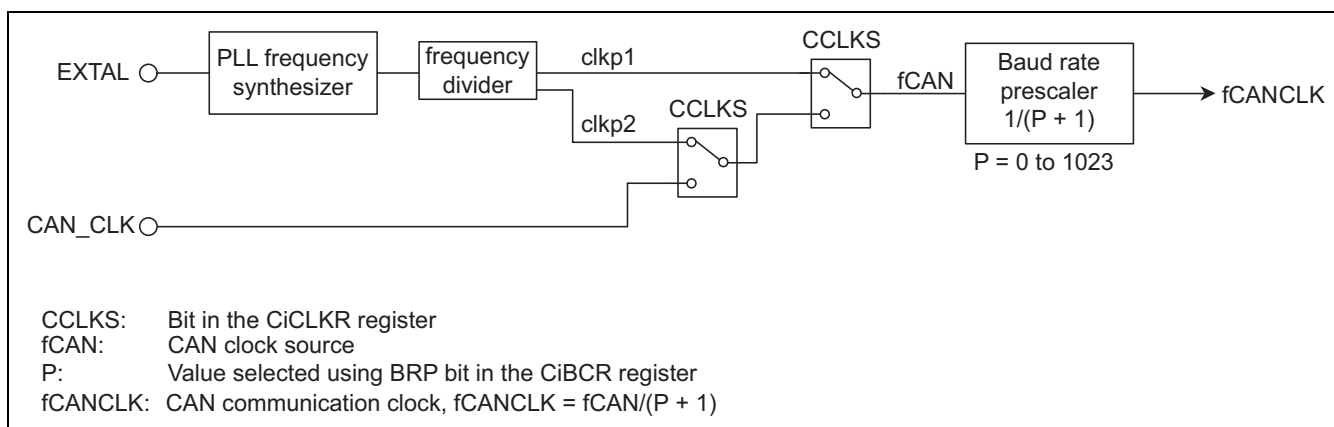
RZ/G1H	RZ/G1N
RZ/G1M	RZ/G1E

The following description explains about the CAN communication speed configuration.

#### 38.5.1 CAN Clock Configuration

This MCU has a CAN clock selector. The CAN clock can be configured by setting the CCLKS bit in the CiCLKR register and the BRP bit in the CiBCR register.

Figure 38.11 shows the block diagram of CAN clock generator.



**Figure 38.11 Block Diagram of CAN Clock Generator (i = 0, 1)**

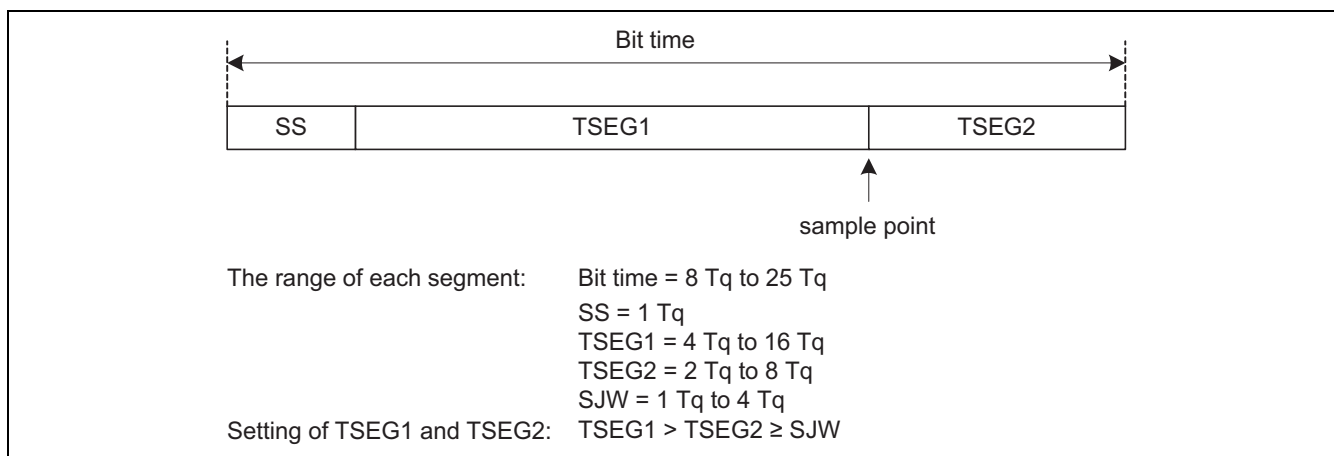
The CAN operating clock can be selected from the internal clock (clkp1, clkp2) from the CPG (PLL), and the external clock input to external pin (CAN\_CLK).

In the initial state, clkp1 is selected. If an external clock input is to be selected, set the CiCLKR register (section 38.3.2) before accessing the CAN module. The range of frequencies that may be input as an external clock is 8 to 50 MHz.

#### 38.5.2 Bit Timing Configuration

The bit time is a single bit time for transmitting/receiving a message and consists of the following three segments.

Figure 38.12 shows the bit timing.



**Figure 38.12 Bit Timing**



### 38.5.3 Bit-rate

The bit rate depends on the division value of the  $f_{CAN}$  (CAN clock source), the division value of the baud rate prescaler, and the number of  $T_q$  of one bit time.

$$\text{Bit rate [bps]} = \frac{f_{CAN}}{\text{Baud rate prescaler division value}^* \times \text{number of } T_q \text{ of one bit time}} = \frac{f_{CANCLK}}{\text{Number of } T_q \text{ of one bit time}}$$

Note: \* Division value of the baud rate prescaler =  $P + 1$  (P: 0 to 1023)  
P: Setting value of the BRP bit in the CiBCR register (i = 0, 1)

Table 38.10 lists bit rate examples.

**Table 38.10 Example of Bit-rate**

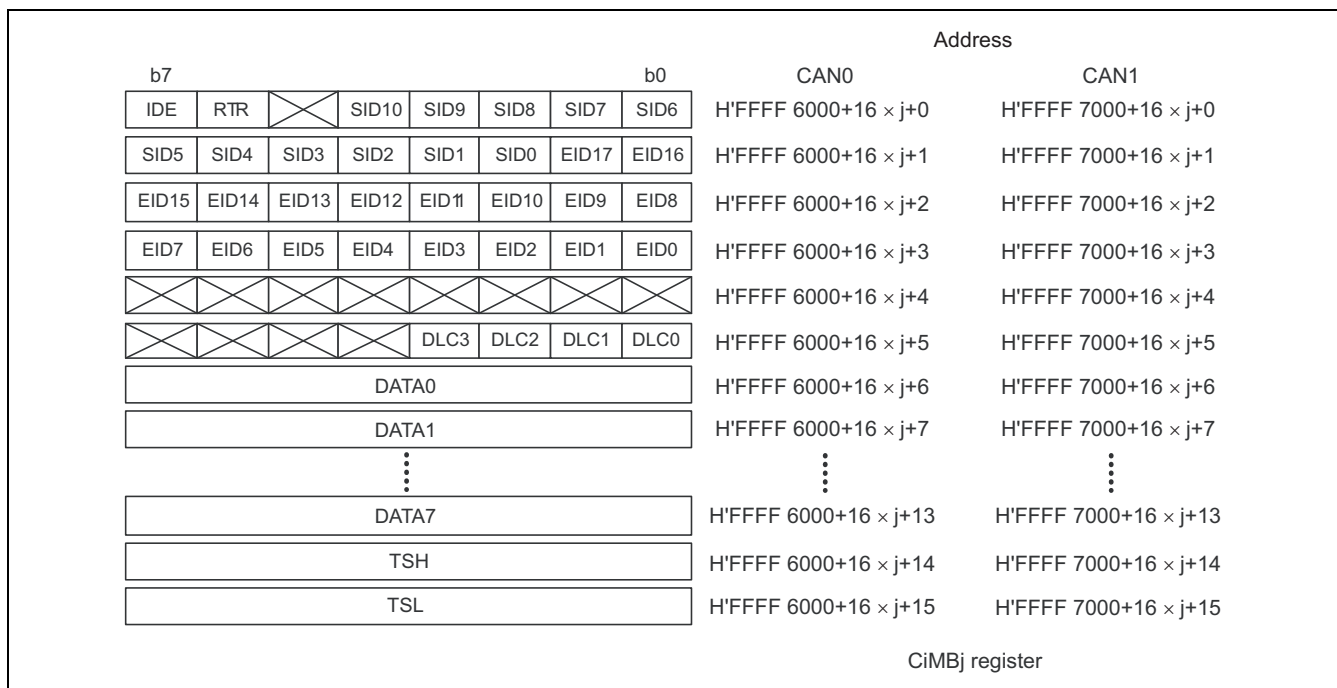
fCAN	40 MHz		32 MHz		20 MHz		16 MHz	
	No. of $T_q$	P + 1	No. of $T_q$	P + 1	No. of $T_q$	P + 1	No. of $T_q$	P + 1
1 Mbps	10 $T_q$	4	8 $T_q$	4	10 $T_q$	2	8 $T_q$	2
	20 $T_q$	2	16 $T_q$	2	20 $T_q$	1	16 $T_q$	1
500 kbps	10 $T_q$	8	8 $T_q$	8	10 $T_q$	4	8 $T_q$	4
	20 $T_q$	4	16 $T_q$	4	20 $T_q$	2	16 $T_q$	2
250 kbps	10 $T_q$	16	8 $T_q$	16	10 $T_q$	8	8 $T_q$	8
	20 $T_q$	8	16 $T_q$	8	20 $T_q$	4	16 $T_q$	4
83.3 kbps	8 $T_q$	60	8 $T_q$	48	8 $T_q$	30	8 $T_q$	24
	10 $T_q$	48	16 $T_q$	24	10 $T_q$	24	16 $T_q$	12
	16 $T_q$	30			16 $T_q$	15		
	20 $T_q$	24			20 $T_q$	12		
33.3 kbps	8 $T_q$	150	8 $T_q$	120	8 $T_q$	75	8 $T_q$	60
	10 $T_q$	120	10 $T_q$	96	10 $T_q$	60	10 $T_q$	48
	20 $T_q$	60	16 $T_q$	60	20 $T_q$	30	16 $T_q$	30
			20 $T_q$	48			20 $T_q$	24

### 38.6 Mailbox and Mask Register Structure

RZ/G1H	RZ/G1N
RZ/G1M	RZ/G1E

Figure 38.13 shows the structure of the CiMBj register.

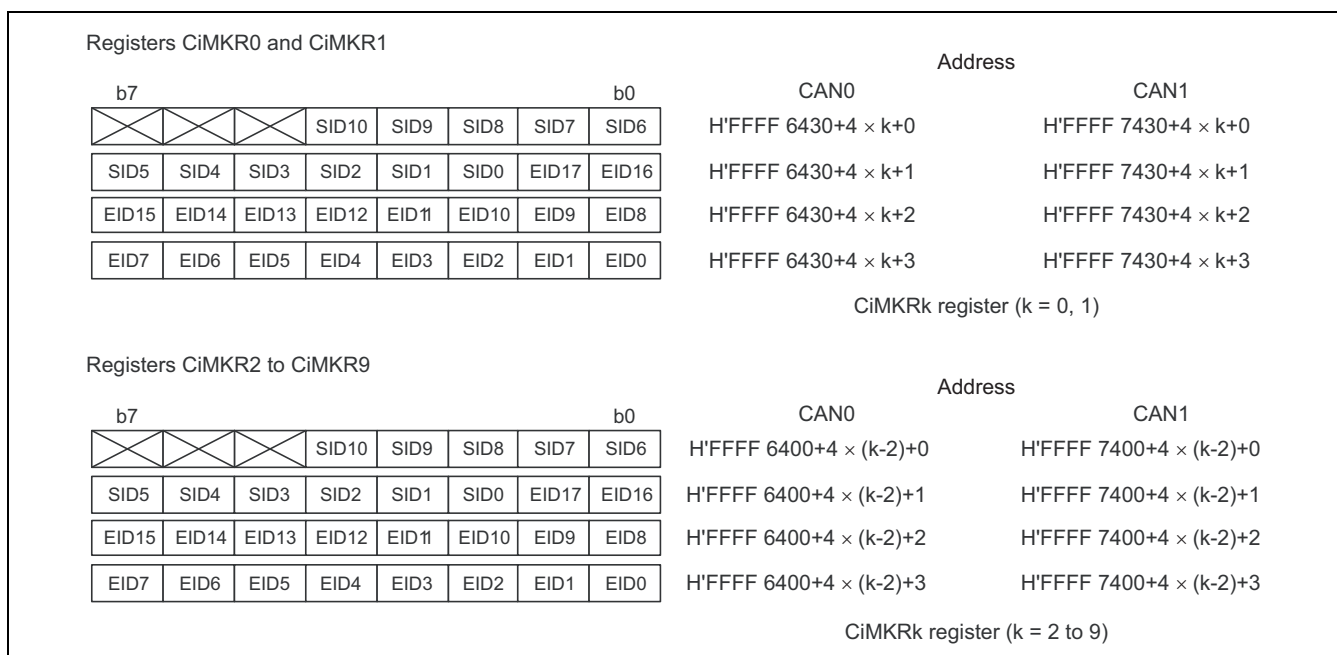
There are 64 mailboxes with the same structure.



**Figure 38.13 Structure of CiMBj Register (i = 0, 1; j = 0 to 63)**

Figure 38.14 shows the structure of registers CiMKR0, CiMKR1, and CiMKR2 to CiMKR9.

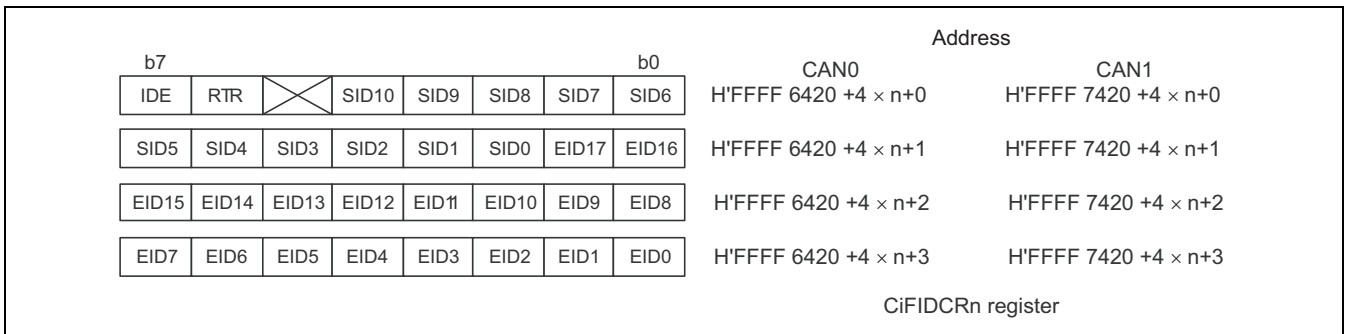
There are 10 mask registers with the same structure.



**Figure 38.14 Structure of CiMKRk Register (i = 0, 1; k = 0 to 9)**

Figure 38.15 shows the structure of the CiFIDCRn register.

There are 2 FIFO received ID compare registers with the same structure.



**Figure 38.15 Structure of CiFIDCRn register (i = 0, 1; n = 0, 1)**

## 38.7 Acceptance Filtering and Masking Function

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

Acceptance filtering allows the user to receive messages with a specified range of multiple IDs for mailboxes. Registers CiMKR0 to CiMKR9 can perform masking of the standard ID and the extended ID of 29 bits.

- The CiMKR0 register corresponds to mailboxes [0] to [15].
- The CiMKR1 register corresponds to mailboxes [16] to [31].
- The CiMKR2 register corresponds to mailboxes [32] to [35].
- The CiMKR3 register corresponds to mailboxes [36] to [39].
- The CiMKR4 register corresponds to mailboxes [40] to [43].
- The CiMKR5 register corresponds to mailboxes [44] to [47].
- The CiMKR6 register corresponds to mailboxes [48] to [51].
- The CiMKR7 register corresponds to mailboxes [52] to [55].
- The CiMKR8 register corresponds to mailboxes [56] to [59] in normal mailbox mode and the receive FIFO mailboxes [60] to [63] in FIFO mailbox mode.
- The CiMKR9 register corresponds to mailboxes [60] to [63] in normal mailbox mode and the receive FIFO mailboxes [60] to [63] in FIFO mailbox mode.

Registers CiMKIVLR0 and CiMKIVLR1 disable acceptance filtering individually for each mailbox.

The IDE bit in the CiMBj register is enabled when the IDFM bit in the CiCTRL register is "B'10" (mixed ID mode).

The RTR bit in the CiMBj register selects a data frame or a remote frame.

In FIFO mailbox mode, normal mailboxes (mailboxes [0] to [55]) use the single corresponding register among registers CiMKR0 to CiMKR7 for acceptance filtering. Receive FIFO mailboxes (mailboxes [60] to [63]) use two registers CiMKR8 and CiMKR9 for the acceptance filtering.

Also, the receive FIFO uses two registers CiFIDCR0 and CiFIDCR1 for ID comparison. Bits EID, SID, RTR, and IDE in registers CiMB60 to CiMB63 for the receive FIFO are disabled. As acceptance filtering depends on the result of two ID-mask sets, two ranges of IDs can be received into the receive FIFO.

Registers CiMKIVLR0 and CiMKIVLR1 are disabled for the receive FIFO.

If both setting of standard ID and extended ID are set in the IDE bits in registers CiFIDCR0 and CiFIDCR1 individually, both ID formats are received.

If both setting of data frame and remote frame are set in the RTR bits in registers CiFIDCR0 and CiFIDCR1 individually, both data and remote frames are received.

When combination with two ranges of IDs is not necessary, set the same mask value and the same ID into both of the FIFO ID/mask register sets.

Figure 38.16 shows the correspondence of mask registers to mailboxes. Figure 38.17 shows the acceptance filtering.

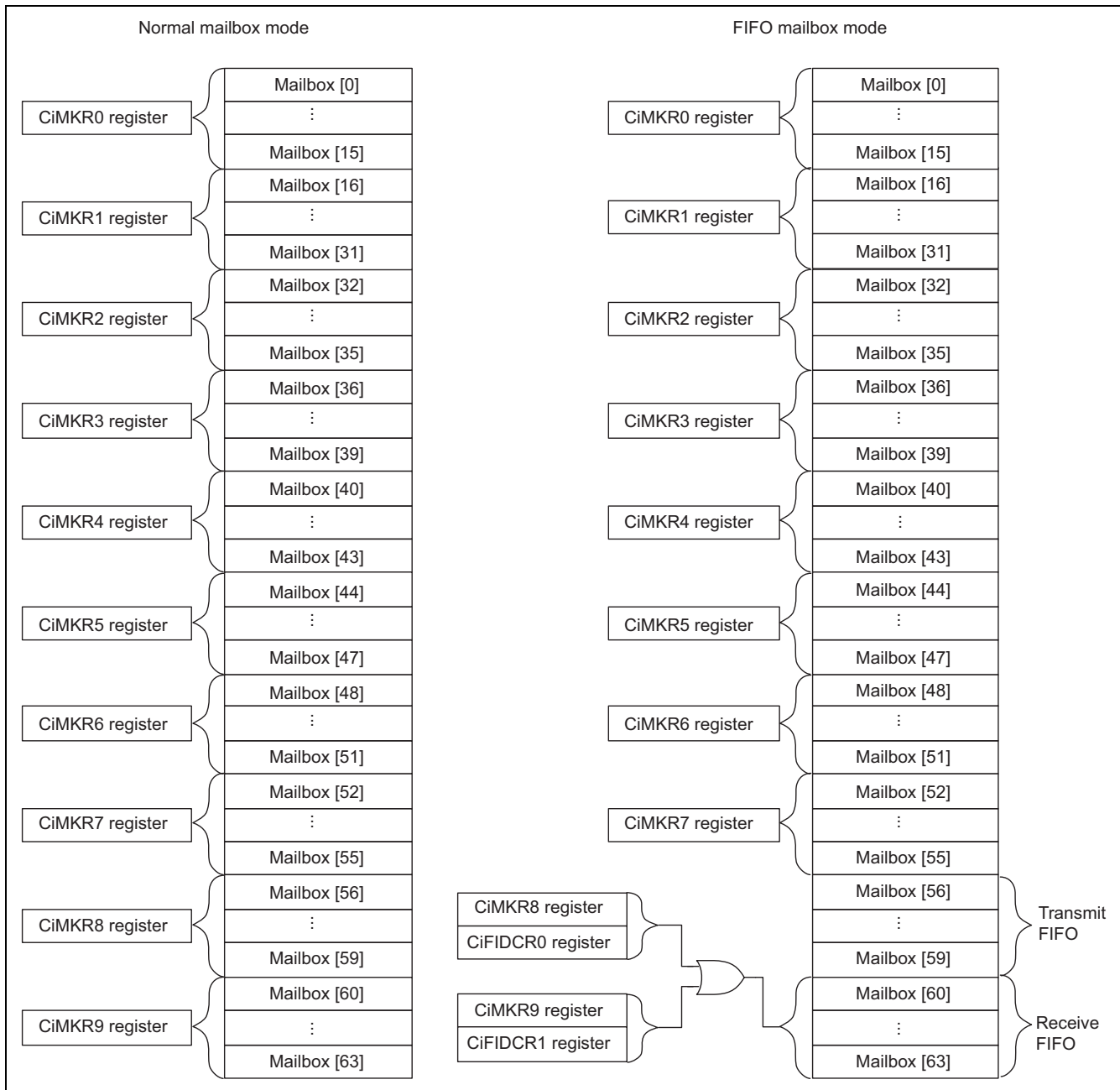
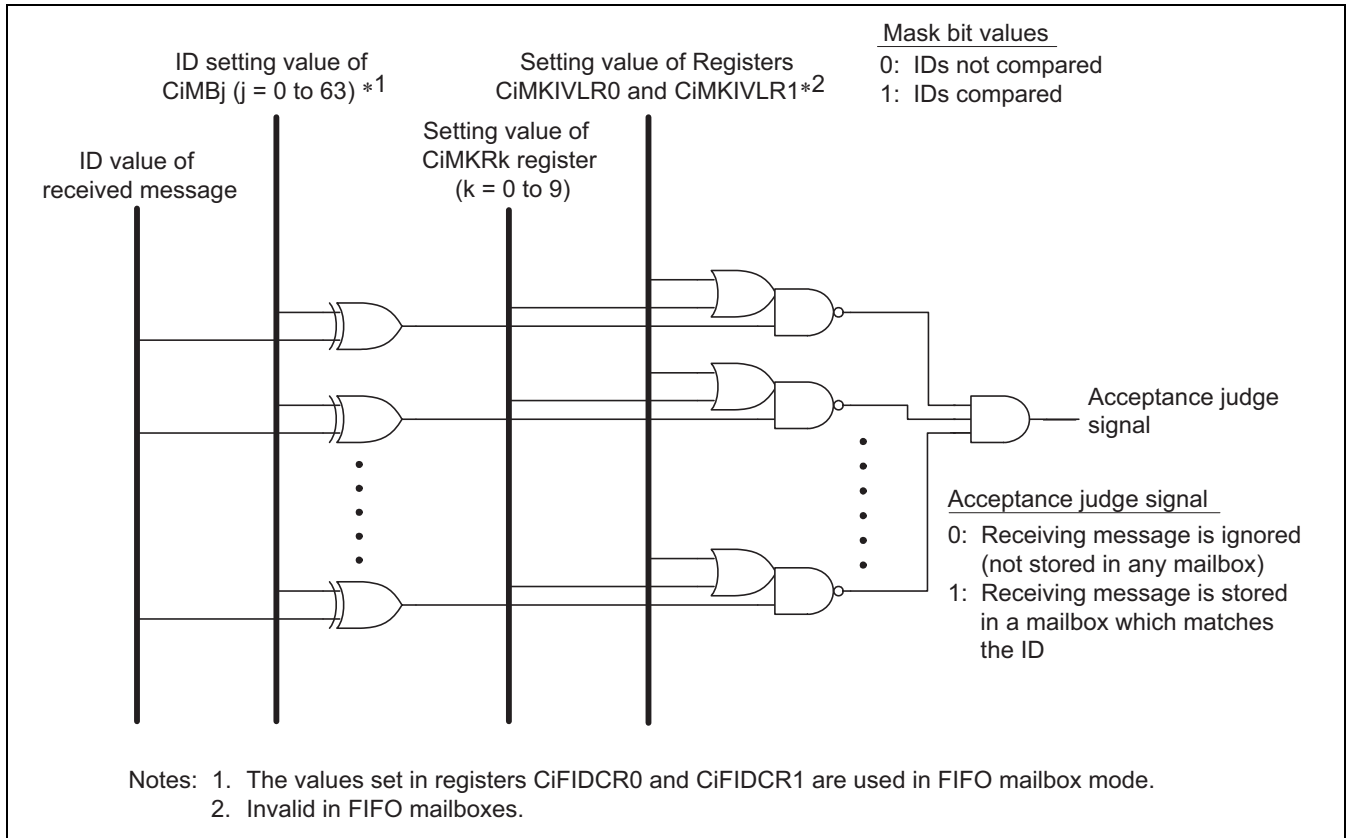


Figure 38.16 Correspondence of Mask Registers to Mailboxes (i = 0, 1)



**Figure 38.17 Acceptance Filtering (i = 0, 1)**

## 38.8 Reception and Transmission

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

Table 38.11 lists the CAN communication mode configuration.

**Table 38.11 Configuration for CAN Reception Mode and Transmission Mode**

TRMREQ	RECREQ	ONESHOT	Communication Mode of Mailbox
0	0	0	Mailbox disabled or transmission being aborted
0	0	1	Configurable only when transmission or reception from a mailbox (programmed in one-shot mode) is aborted.
0	1	0	Configured as a receive mailbox for a data frame or a remote frame.
0	1	1	Configured as a one-shot receive mailbox for a data frame or a remote frame.
1	0	0	Configured as a transmit mailbox for a data frame or a remote frame.
1	0	1	Configured as a one-shot transmit mailbox for a data frame or a remote frame.
1	1	0	Do not set.
1	1	1	Do not set.

Note: TRMREQ, RECREQ, ONESHOT: Bits in CiMCTLj register (i = 0, 1; j = 32 to 63)

When a mailbox is configured as a receive mailbox or a one-shot receive mailbox, note the following:

1. Before a mailbox is configured as a receive mailbox or a one-shot receive mailbox, set the CiMCTLj register to "H'00".
2. A received message is stored into the first mailbox that matches the condition according to the result of receive mode configuration and acceptance filtering. Upon deciding a mailbox which stores the received message, the mailbox with the smaller number has higher priority.
3. In CAN operation mode, when a CAN module transmits a message whose ID matches with the ID/mask set of a mailbox configured to receive messages, the CAN module never receives the transmitted data. In self-test mode, however, the CAN module may receive its transmitted data. In this case, the CAN module sends an ACK.

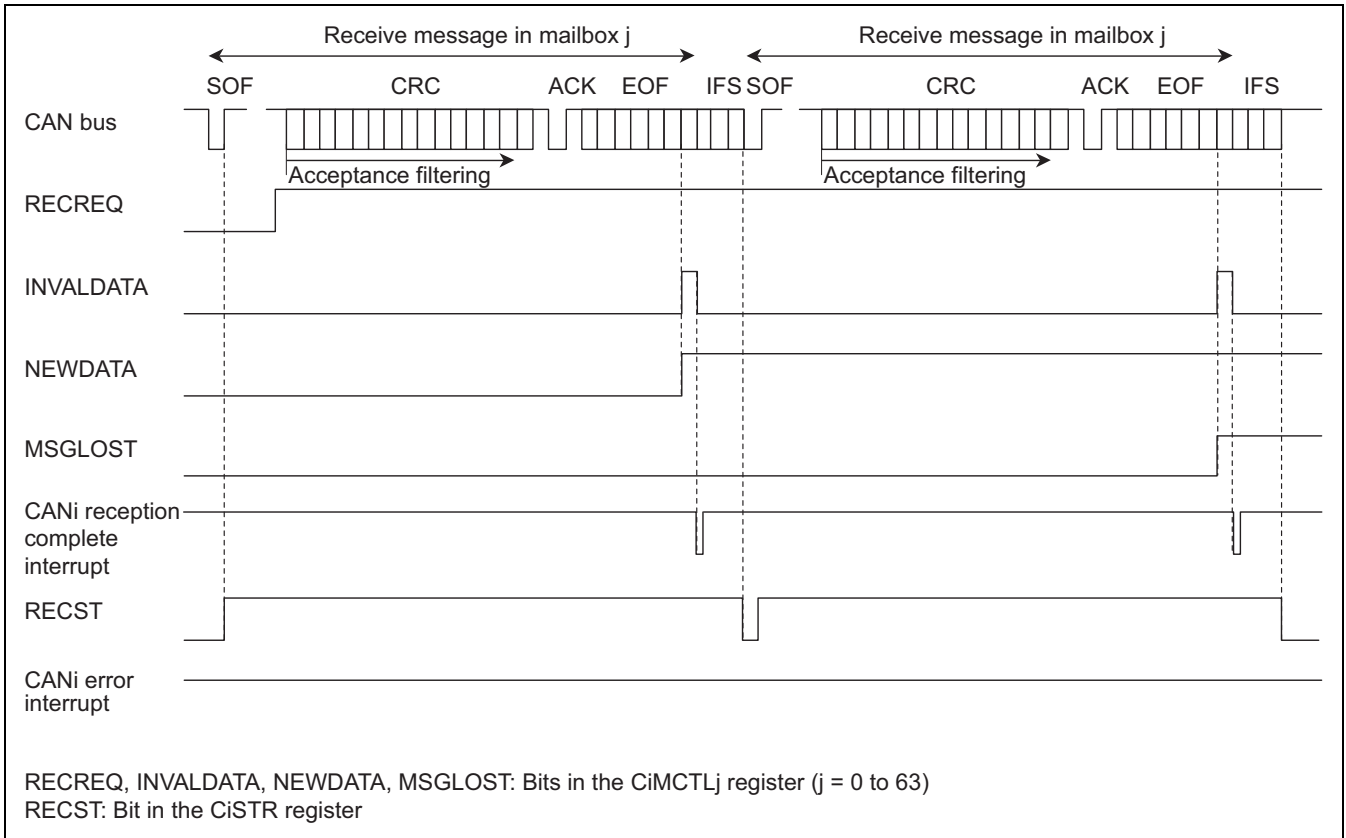
When configuring a mailbox as a transmit mailbox or a one-shot transmit mailbox, note the following:

1. Before a mailbox is configured as a transmit mailbox or one-shot transmit mailbox, ensure that the CiMCTLj register is "H'00" and that there is no pending abort process.

**38.8.1 Reception**

Figure 38.18 shows an operation example of data frame reception in overwrite mode.

This example shows the operation of overwriting the first message when the CAN module receives two consecutive CAN messages that matches the receiving conditions of the CiMCTLj register.

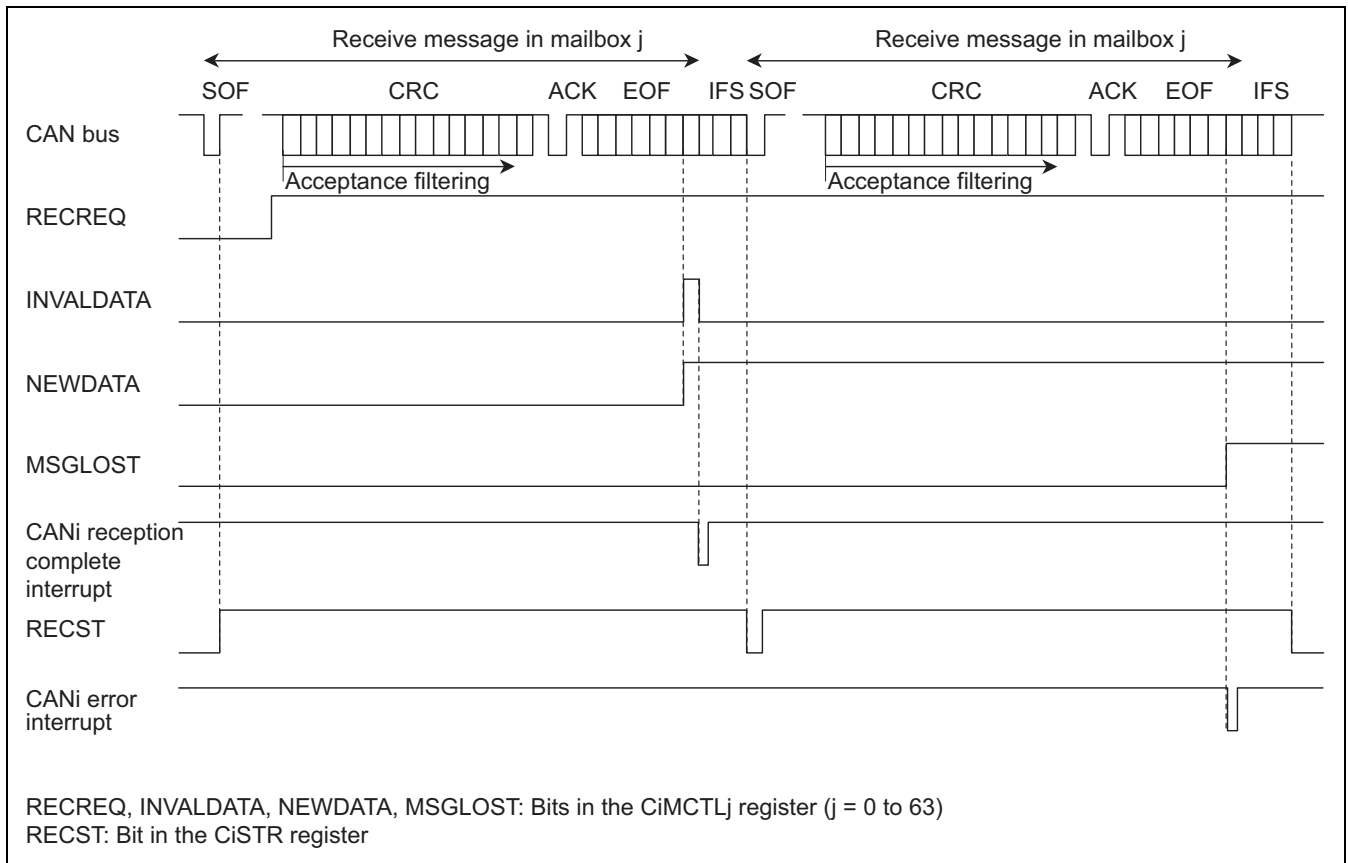


**Figure 38.18 Operation Example of Data Frame Reception in Overwrite Mode (i = 0, 1)**

1. When a SOF is detected on the CAN bus, the RECST bit in the CiSTR register is set to "1" (reception in progress) if the CAN module has no message ready to start transmission.
2. The acceptance filter procedure starts at the beginning of the CRC field to select the receive mailbox.
3. After a message has been received, the NEWDATA bit in the CiMCTLj register for the receive mailbox is set to "1" (new data being updated/stored in the mailbox). The INVALIDDATA bit in the CiMCTLj register is set to "1" (message is being updated) at the same time, and then the INVALIDDATA bit is set to "0" (message valid) again after the complete message is transferred to the mailbox.
4. When the interrupt enable bit in the CiMIER register for the receive mailbox is "1" (interrupt enabled), the CANi reception complete interrupt request is generated. This interrupt is generated when the INVALIDDATA bit is set to "0".
5. After reading the message from the mailbox, the NEWDATA bit needs to be set to "0" by a program.
6. In overwrite mode, if the next CAN message has been received into a mailbox whose NEWDATA bit is still set to "1", the MSGLOST bit in the CiMCTLj register is set to "1" (message has been overwritten). The new received message is transferred to the mailbox. The CANi reception complete interrupt request is generated the same as in 4.

Figure 38.19 shows the operation example of data frame reception in overrun mode. This example shows the operation of overrunning the second message when the CAN module receives two consecutive CAN messages that matches the receiving conditions of the CiMCTLj register.



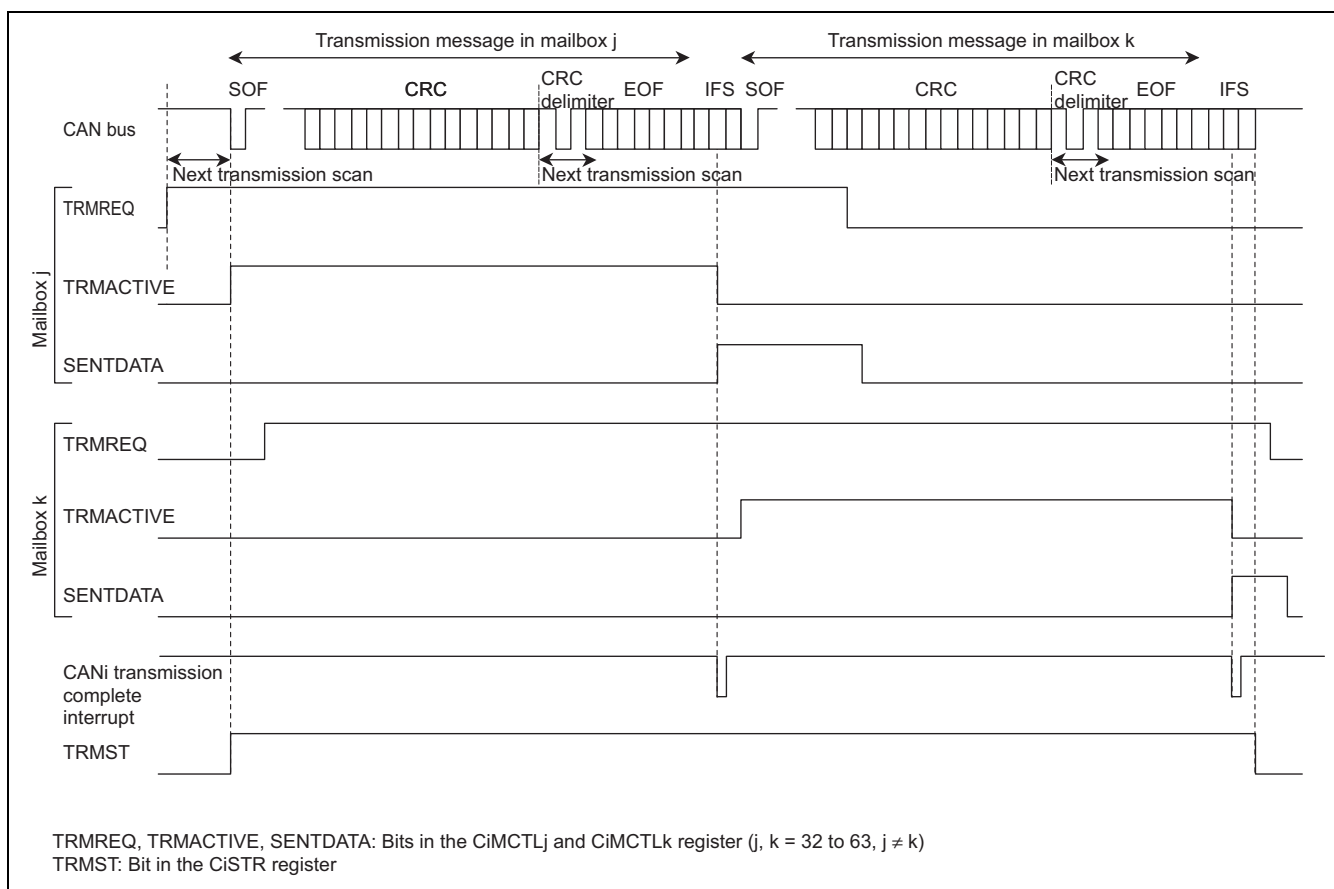


**Figure 38.19 Operation Example of Data Frame Reception in Overrun Mode (i = 0, 1)**

1. to 5. are the same as overwrite mode.
6. In overrun mode, if the next message has been received before the NEWDATA bit is set to "0", the MSGLOST bit in the CiMCTLj register is set to "1" (message has been overrun). The new received message is discarded and a CANi error interrupt request is generated if the corresponding interrupt enable bit in the CiEIER register is set to "1" (interrupt enabled).

### 38.8.2 Transmission

Figure 38.20 shows an operation example of data frame transmission.



**Figure 38.20 Operation Example of Data Frame Transmission (i = 0, 1)**

1. When a TRMREQ bit in the CiMCTLj register is set to 1 (transmit mailbox) in bus-idle state, the mailbox scan procedure starts to decide the highest-priority mailbox for transmission. Once the transmit mailbox is decided, the TRMACTIVE bit in the CiMCTLj register is set to "1" (from when a transmission request is received until transmission is completed, or an error/arbitration lost has occurred), the TRMST bit in the CiSTR register is set to "1" (transmission in progress), and the CAN module starts transmission.\*
2. If other TRMREQ bits are set, the transmission scan procedure starts with the CRC delimiter for the next transmission.
3. If transmission is completed without losing arbitration, the SENTDATA bit in the CiMCTLj register is set to "1" (transmission completed) and the TRMACTIVE bit is set to "0" (transmission is pending, or no transmission request). If the interrupt enable bit in the CiMIER register is "1" (interrupt enabled), the CANi transmission complete interrupt request is generated.
4. When requesting the next transmission from the same mailbox, set bits SENTDATA and TRMREQ to "0", then set the TRMREQ bit to "1" after checking that bits SENTDATA and TRMREQ have been set to "0".

Note: \* If arbitration is lost after the CAN module starts transmission, the TRMACTIVE bit is set to "0". The transmission scan procedure is performed again to search for the highest-priority transmit mailbox from the beginning of the CRC delimiter. If an error occurs either during transmission or following the arbitration lost the transmission scan procedure is performed again from the start of the error delimiter to search for the highest-priority transmit mailbox.

## 38.9 CAN Interrupt

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

The CAN module provides the following CAN interrupts for each channel. Table 38.12 lists CAN interrupts.

- CANi reception complete interrupt (mailbox 0) [RXM0i]
- CANi reception complete interrupt (mailbox 1 to 63) [RXM1i]
- CANi transmission complete interrupt (mailbox 32 to 63) [TXMi]
- CANi reception FIFO interrupt [RXFi]
- CANi transmission FIFO interrupt [TXFi]
- CANi error interrupt [ERSi]

There are eight types of interrupt sources for the CANi error interrupts. These sources can be determined by checking the CiEIFR register.

- Bus error
- Error-warning
- Error-passive
- Bus-off entry
- Bus-off recovery
- Receive overrun
- Overload frame transmission
- Bus lock

**Table 38.12 CAN Interrupts**

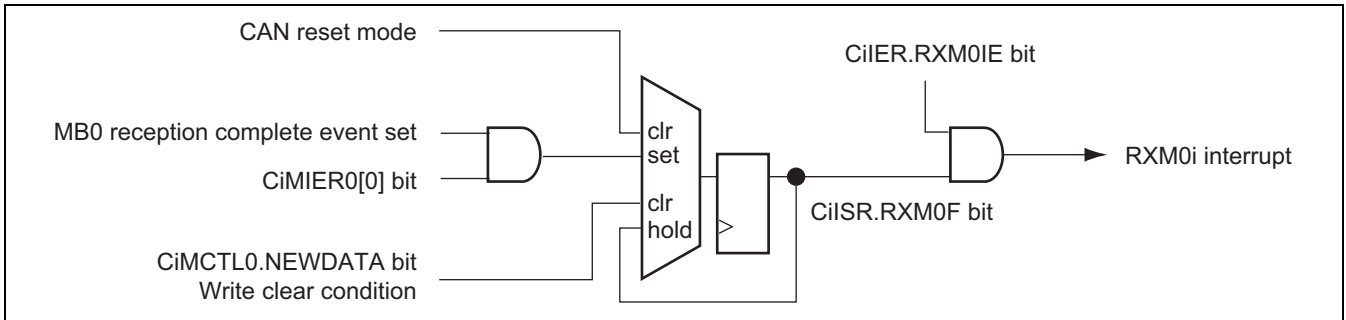
Module	Interrupt Symbol	Interrupt Source	Source Flag
CANi	ERSi	Bus lock detected	CiEIFR.BLIF
		Overload frame transmission detected	CiEIFR.OLIF
		Overrun detected	CiEIFR.ORIF
		Bus-off recovery detected	CiEIFR.BORIF
		Bus-off entry detected	CiEIFR.BOEIF
		Error-passive detected	CiEIFR.EPIF
		Error-warning detected	CiEIFR.EWIF
		Bus error detected	CiEIFR.BEIF
RXFi	RXFi	Receive FIFO message received (CiMIER1[29] = 0)	CiISR.RXFF
		Receive FIFO warning (CiMIER1[29] = 1)	
TXFi	TXFi	Transmit FIFO message transmission completed (CiMIER1[25] = 0)	CiISR.TXFF
		FIFO last message transmission completed (CiMIER1[25] = 1)	
RXM0i	RXM0i	Mailbox 0 message received	CiMCTL0.NEWDATA
RXM1i	RXM1i	Mailbox 1 to 63 message received	CiMCTL1.NEWDATA to CiMCTL63.NEWDATA
TXMi	TXMi	Mailbox 32 to 63 message transmission completed	CiMCTL32.SENTDATA to CiMCTL63.SENTDATA

Legend: i = 0, 1

**(1) CANi reception complete interrupt (mailbox 0) [RXM0i]**

After the CiMCTL0.NEWDATA bit is set by the completion of reception, if received data has been stored (the corresponding INVALIDDATA bit changes from "1" to "0"), the CiISR.RXM0F bit is set to "1" when CiMIER0[0] has been set to "1". When the mailbox 0 reception complete (RXM0) interrupt has been enabled, the RXM0 interrupt is requested to the interrupt controller.

To clear the RXM0 interrupt, clear the CiMCTL0.NEWDATA bit in the RXM0 interrupt handling routine. To change the CiIER.RXM0IE bit to disabled after having set the bit, make the change while no RXM0 interrupt is generated or during the RXM0 interrupt handling routine. This also applies to CiMIER0[0].

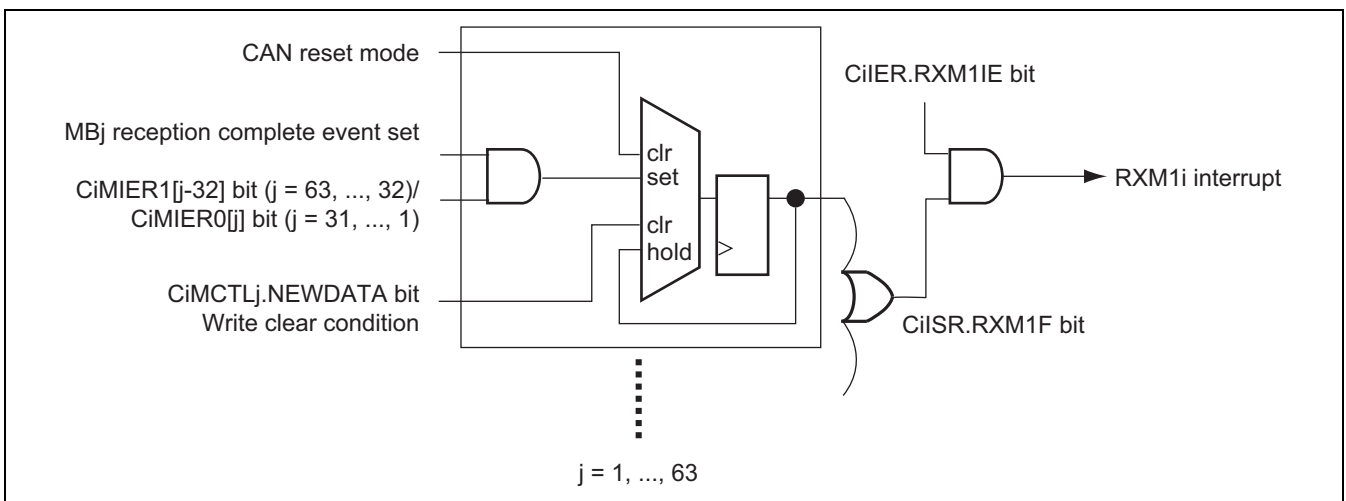


**Figure 38.21 Block Diagram of CANi Reception Complete Interrupt (Mailbox 0) [RXM0i]**

**(2) CANi reception complete interrupt (mailbox 1 to 63) [RXM1i]**

After the CiMCTLj.NEWDATA bit is set by the completion of reception, if received data has been stored (the corresponding INVALIDDATA bit changes from "1" to "0"), the CiISR.RXM1F bit is set to "1" when the CiMIER0 or CiMIER1 register bit corresponding to mailbox j has been set to "1". When the mailbox 1 to 63 reception complete (RXM1) interrupt has been enabled, the RXM1 interrupt is requested to the interrupt controller.

To clear the RXM1 interrupt, clear the CiMCTLj.NEWDATA bit in the RXM1 interrupt handling routine. To change the CiIER.RXM1IE bit to disabled after having set the bit, make the change while no RXM1 interrupt is generated or during the RXM1 interrupt handling routine. This also applies to CiMIER0[j] (j = 1 to 31) or CiMIER1[j-32] (j = 32 to 63).

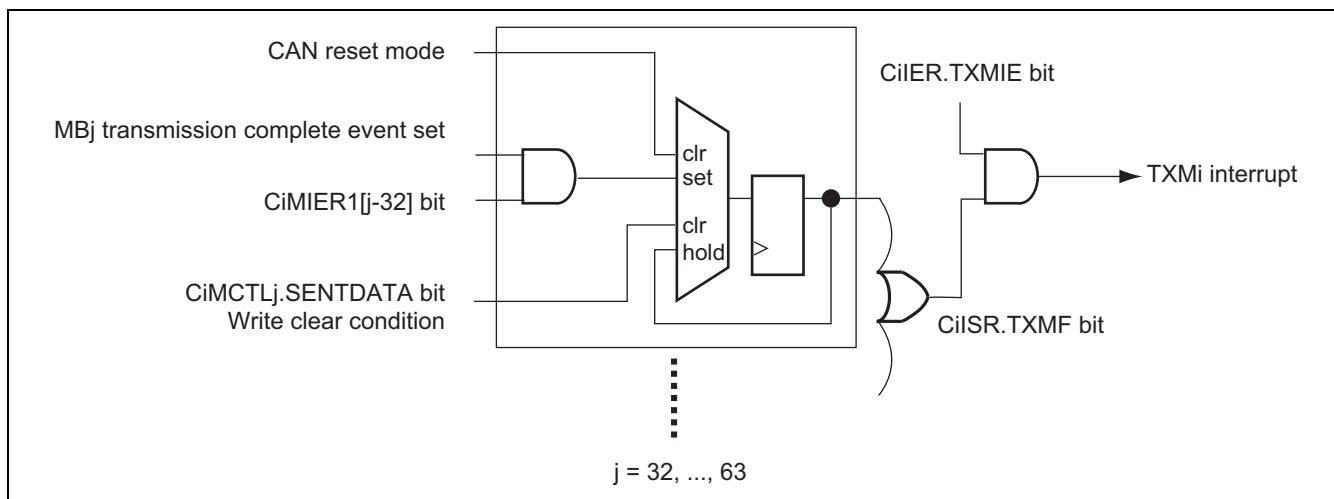


**Figure 38.22 Block Diagram of CANi Reception Complete Interrupt (Mailbox 1 to 63) [RXM1i]**

**(3) CANi transmission complete interrupt (mailbox 32 to 63) [TXMi]**

If the CiMCTLj.SENTDATA bit is set by the completion of transmission, the CiISR.TXMF bit is set to "1" when the CiMIER1 register bit corresponding to mailbox j has been set to "1". When the mailbox 32 to 63 transmission complete (TXM) interrupt has been enabled, the TXM interrupt is requested to the interrupt controller.

To clear the TXM interrupt, clear the CiMCTLj.SENTDATA bit in the TXM interrupt handling routine. To change the CiIER.TXMIE bit to disabled after having set the bit, make the change while no TXM interrupt is generated or during the TXM interrupt handling routine. This also applies to CiMIER1[j-32] (j = 32 to 63).

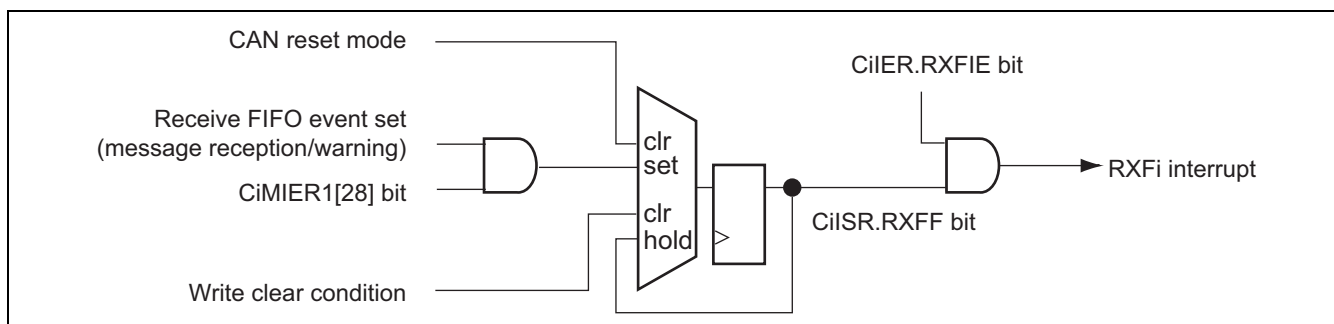


**Figure 38.23 Block Diagram of CANi Transmission Complete Interrupt (Mailbox 32 to 63) [TXMi]**

**(4) CANi receive FIFO interrupt [RXFi]**

If CiRFCR[6:5] are set by the reception of a receive FIFO message or by a warning with the settings of CiMIER1[29:28], the CiISR.RXFF bit is set to "1". When the receive FIFO (RXF) interrupt has been enabled with the CiIER.RXFIE bit, the RXF interrupt is requested to the interrupt controller.

To clear the RXF interrupt, clear the CiISR.RXFF bit in the RXF interrupt handling routine. To change the CiIER.RXFIE bit to disabled after having set the bit, make the change while no RXF interrupt is generated or during the RXF interrupt handling routine. This also applies to CiMIER1[28].

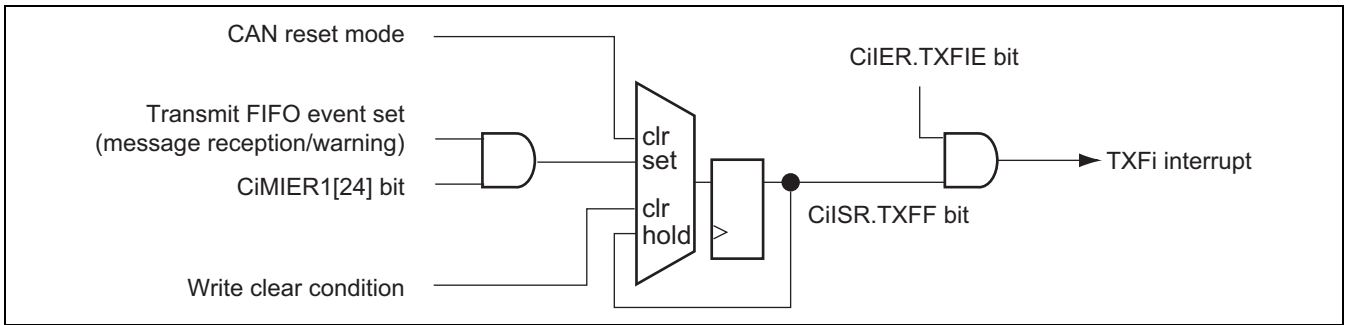


**Figure 38.24 Block Diagram of CANi Receive FIFO Interrupt [RXFi]**

**(5) CANi transmit FIFO interrupt [TXFi]**

When the transmission of a transmit FIFO message is counted for the specified number of times with the settings of CiMIER1 [25:24], the CiISR.TXFF bit is set to "1". When the transmit FIFO (TXF) interrupt has been enabled with the CiIER.TXFIE bit, the TXF interrupt is requested to the interrupt controller.

To clear the TXF interrupt, clear the CiISR.TXFF bit in the TXF interrupt handling routine. To change the CiIER.TXFIE bit to disabled after having set the bit, make the change while no TXF interrupt is generated or during the TXF interrupt handling routine. This also applies to CiMIER1[24].

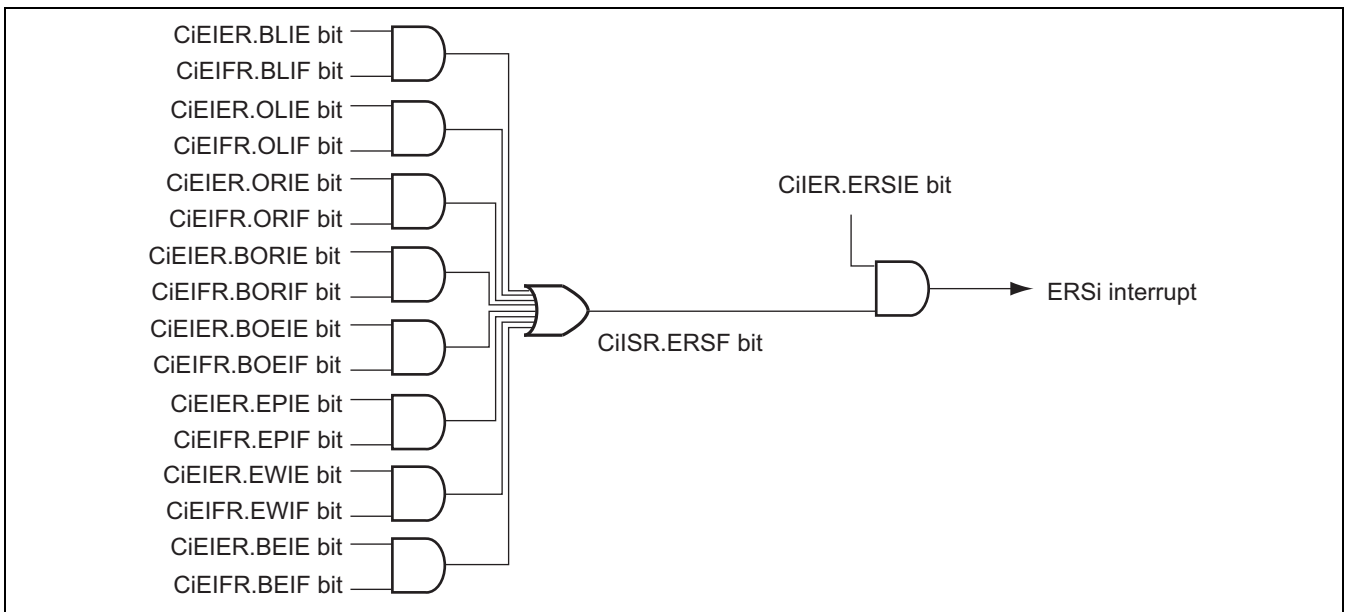


**Figure 38.25 Block Diagram of CANi Transmit FIFO Interrupt [TXFi]**

**(6) CANi error interrupt [ERSi]**

If CiEIFR[j] is set by a communication error, the CiISR.ERSF bit is set to "1" when the corresponding CiEIER[j] has been set to "1". When the error (ERS) interrupt has been enabled with the CiIER.ERSIE bit, the ERS interrupt is requested to the interrupt controller.

To clear the ERS interrupt, clear each CiEIFR[j] register bit in the ERS interrupt handling routine. To change the CiIER.ERSIE bit to disabled after having set the bit, make the change while no ERS interrupt is generated or during the ERS interrupt handling routine. This also applies to CiEIER[j] (j = 7 to 0).



**Figure 38.26 Block Diagram of CANi Error Interrupt [ERSi]**

## 39. PCIEC

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

### 39.1 Overview

This module performs PCIEC controls, and transfers data between this LSI internal bus (AXI bus) and the PCI devices connected to the PCIEC. This module facilitates the design of systems using the PCI Express while at the same time permitting high-speed data transfers in a compact system.

This module functions as a bus bridge connecting the PCI Express to this LSI internal bus (AXI bus), and provides transfer channels between PCI Express devices and devices connected to the LSI internal bus (AXI bus).

This LSI incorporates a PCI Express physical module that supports one lane ( $\times 1$ ).

This module has two modes: a Root Port and an Endpoint and can operate as a Root Port or Endpoint that is defined in the PCI Express specification.

#### 39.1.1 Features

This module has the following features.

- Functions as a bridge that connects the PCI Express to the LSI internal bus (AXI bus)
  - Generates a PCIe packet from the AXI bus transaction to the PCI area
  - Generates a AXI bus transaction from a PCI Express packet
- Supports high-speed data transfer between PCI Express devices and internal bus (AXI bus) via the internal DMAC
- Supports the subset of PCI Express Base Specification Revision 2.0 (Dec. 20, 2006)
- Operates as a PCI Express Endpoint or a PCI Express Root Port
- Supports the requester and completer functions for the PCIe transaction
- Incorporates configuration registers and the following capability structures
  - Power management capability structure
  - MSI capability structure (supports masking function and pending bits.)
  - PCI Express capability structure
  - Virtual channel capability structure
- Supports interrupts by INTx and MSI
- Supports one lane ( $\times 1$ )
- Supports multiple speeds (2.5 GT/s and 5.0 GT/s).
- Automatically performs link training and link configurations
- Supports the D+/D-line automatic swap function (lane polarity inversion)
- Achieves QoS through transaction ordering.
- Automatically performs flow control by managing six types of credits
- Automatic handling function by hardware
- Buffer for holding error packet headers and error indication status provided
- Supports the link power control function (L0, L0s, and L1 states)
- Supports device power control function (D0, D3<sub>hot</sub>, and D3<sub>cold</sub> states).
- Supports 128-byte max payload size.
- Supports completion timeout disable.

Note: This module does not support the following PCI Express functions.

- Expansion ROM for system boot
- Card bus

- Phantom function
- Power-management event (PME) handling by hardware
- Slot function (including Hot Plug)
- AER function
- BIST function
- Surprise Down error function
- ARI forwarding function
- Port arbitration function
- Peer-to-peer transfer

### 39.1.2 Block Diagram

Figure 39.1 shows a block diagram of the PCIEC.

The PCIEC comprises a bridge, PCIEC controller, and PCIEC physical unit.

The bridge provides the bridge function of connecting the internal bus (AXI bus) to the PCI Express controller.

The PCIEC controller is a block that controls the PCI Express packet transmission and reception, and it implements the functions of transaction and data link layers that are defined by the PCI Express standards. The configuration registers defined by the PCI Express standards are installed in this block.

The PCIEC physical unit is a block that controls PCI Express transmission paths, and implements the physical layer function that is defined by the PCI Express standards.

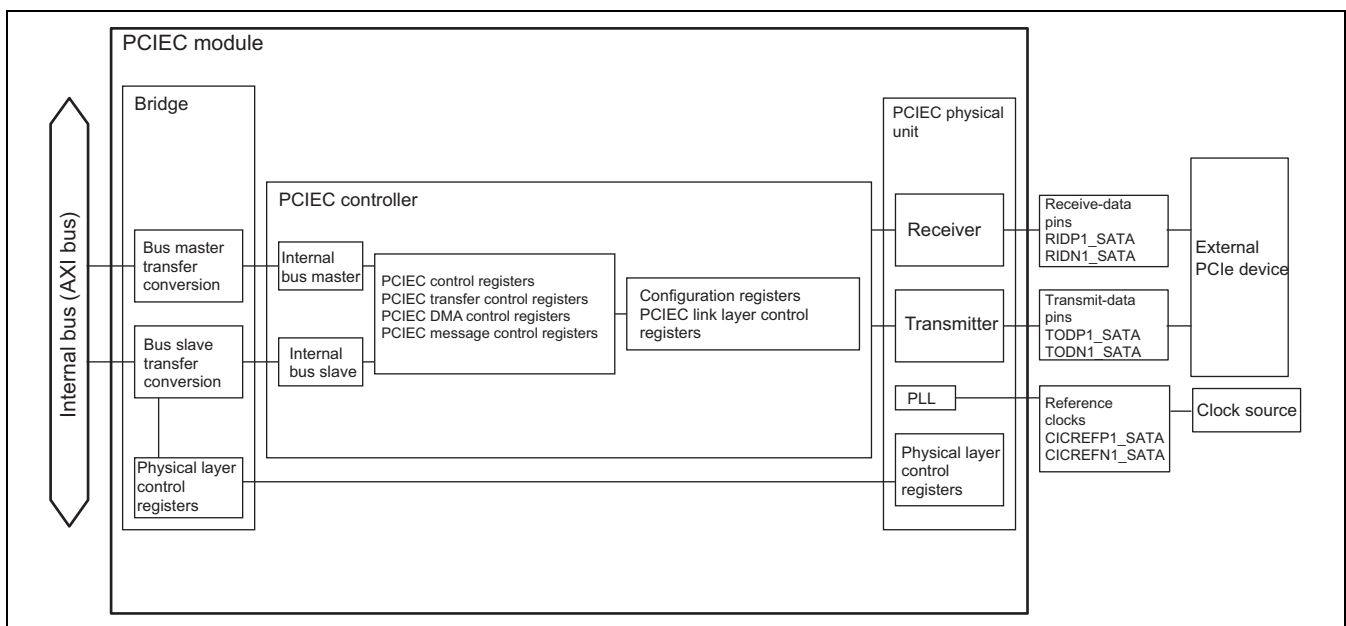


Figure 39.1 Block Diagram



### 39.1.3 External Pins

Table 39.1 shows the pin configuration.

**Table 39.1 Pin Configuration**

Signal Name	Signal Conforming to PCI Standard	I/O	Description	RZ/G Series Products			
				RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
CICREFP1_SATA CICREFN1_SATA	REFCLK+ REFCLK-	Input	Reference clock inputs to the PLL incorporated in the PCIEC module (differential inputs). 100-MHz clock should be applied.	√	√	√	—
AMON1_SATA	—	Input /Output	Debug pins for PCIEC; do not use these pins usually. Nothing must be connected to these pins on the board (NC).	√	√	√	—
TODP1_SATA TODN1_SATA	PETp0 PETn0	Output	Transmit data pins used by a physical module, where 2.5- or 5.0-GHz signals are propagated. (Differential output)	√	√	√	—
RIDP1_SATA RIDN1_SATA	PERp0 PERn0	Input	Receive data pins used by a physical module, where 2.5- or 5.0-GHz signals are propagated. (Differential input)	√	√	√	—

### 39.1.4 Register Configuration

Table 39.3 shows the PCIEC registers. In this table, the Address Offset columns show an offset for each register from the PCIEC base address. The actual access address is obtained by adding each offset to the PCIEC base address. Table 39.2 shows the PCIEC base address. These registers should be accessed through the AXI bus. Only the little endian mode can be used for this module.

**Table 39.2 PCIEC Base Address**

PCI Express	
Base Address	H'FE00_0000

Table 39.3 PCIEC Register Configuration

Register Name	Abbreviation	AX*1 R/W	PCI*1 R/W	Address Offset	Initial Value	Access Size	RZ/G Series Products			
							RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
<b>PCIEC control registers</b>										
Configuration transmission address register	PCIECAR	R/W	—	H'0_0010	H'0000 0000	32	√	√	√	—
Configuration transmission control register	PCIECTRL	R/W	—	H'0_0018	H'0000 0000	32	√	√	√	—
Configuration transmission data register	PCIECDR	R/W	—	H'0_0020	—	32	√	√	√	—
Mode setting register	PCIEMSR	R/W	—	H'0_0028	H'0000 0001	32	√	√	√	—
Unlock transmission control register	PCIEUNLOCKC R	R	—	H'0_0048	H'0000 0000	32	√	√	√	—
INTx register	PCIEINTXR	R/W	—	H'0_0400	H'0000 0000	32	√	√	√	—
Message reception status register	PCIERMSGR	R/W	—	H'0_0410	H'0000 0000	32	√	√	√	—
Message reception interrupt enable register	PCIERMSGIER	R/W	—	H'0_0440	H'0000 0000	32	√	√	√	—
Power management message transmission control register	PCIEPMMSGC R	R/W	—	H'0_0500	H'0000 0000	32	√	√	√	—
PHY layer status register	PCIEPHYSR	R/W	—	H'0_07F0	H'0000 0000	32	√	√	√	—
MSI transmission register	PCIEMSITXR	R/W	—	H'0_0840	H'0000 0000	32	√	√	√	—
<b>PCIEC transfer control registers</b>										
Transfer control register	PCIETCTRL	R/W	—	H'0_2000	H'0000 0008	32	√	√	√	—
Transfer status register	PCIETSTR	R/W	—	H'0_2004	H'0000 0000	32	√	√	√	—
Interrupt register	PCIEINTR	R/W	—	H'0_2008	H'2000 0000	32	√	√	√	—
Interrupt enable register	PCIEINTER	R/W	—	H'0_200C	H'0000 0000	32	√	√	√	—
Error factor register	PCIEERRFR	R/W	—	H'0_2020	H'0000 0000	32	√	√	√	—
Error interrupt enable register	PCIEERRFER	R/W	—	H'0_2024	H'0000 0000	32	√	√	√	—
Error factor register 2	PCIEERRFR2	R/W	—	H'0_2028	H'0000 0000	32	√	√	√	—
Transfer interrupt enable register	PCIETIER	R/W	—	H'0_2030	H'0000 0000	32	√	√	√	—
Power management state status register	PCIEPMSR	R/W	—	H'0_2034	H'0000 0000	32	√	√	√	—
Power management state interrupt enable register	PCIEPMSCIER	R/W	—	H'0_2038	H'0000 0000	32	√	√	√	—
MSIF register	PCIEMSIFR	R/W	—	H'0_2044	H'0000 0000	32	√	√	√	—
MSI address lower register	PCIEMSIALR	R/W	—	H'0_2048	H'0000 0000	32	√	√	√	—
MSI address upper register	PCIEMSIAUR	R/W	—	H'0_204C	H'0000 0000	32	√	√	√	—

Register Name	Abbreviation	AX*1 R/W	PCI*1 R/W	Address Offset	Initial Value	Access Size	RZ/G Series Products			
							RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
MSI interrupt enable register	PCIEMSIER	R/W	—	H'0_2050	H'0000 0000	32	√	√	√	—
PCIEC Root Port address register 0	PCIEPRAR0	R/W	—	H'0_2080	H'0000 0000	32	√	√	√	—
PCIEC Root Port address register 1	PCIEPRAR1	R/W	—	H'0_2084	H'0000 0000	32	√	√	√	—
PCIEC Root Port address register 2	PCIEPRAR2	R/W	—	H'0_2088	H'0000 0000	32	√	√	√	—
PCIEC Root Port address register 3	PCIEPRAR3	R/W	—	H'0_208C	H'0000 0000	32	√	√	√	—
PCIEC Root Port address register 4	PCIEPRAR4	R/W	—	H'0_2090	H'0000 0000	32	√	√	√	—
PCIEC Root Port address register 5	PCIEPRAR5	R/W	—	H'0_2094	H'0000 0000	32	√	√	√	—
Local address register 0	PCIELAR0	R/W	—	H'0_2200	H'0000 0000	32	√	√	√	—
Local address mask register 0	PCIELAMR0	R/W	—	H'0_2208	H'0000 0000	32	√	√	√	—
Local address register 1	PCIELAR1	R/W	—	H'0_2220	H'0000 0000	32	√	√	√	—
Local address mask register 1	PCIELAMR1	R/W	—	H'0_2228	H'0000 0000	32	√	√	√	—
Local address register 2	PCIELAR2	R/W	—	H'0_2240	H'0000 0000	32	√	√	√	—
Local address mask register 2	PCIELAMR2	R/W	—	H'0_2248	H'0000 0000	32	√	√	√	—
Local address register 3	PCIELAR3	R/W	—	H'0_2260	H'0000 0000	32	√	√	√	—
Local address mask register 3	PCIELAMR3	R/W	—	H'0_2268	H'0000 0000	32	√	√	√	—
Local address register 4	PCIELAR4	R/W	—	H'0_2280	H'0000 0000	32	√	√	√	—
Local address mask register 4	PCIELAMR4	R/W	—	H'0_2288	H'0000 0000	32	√	√	√	—
Local address register 5	PCIELAR5	R/W	—	H'0_22A0	H'0000 0000	32	√	√	√	—
Local address mask register 5	PCIELAMR5	R/W	—	H'0_22A8	H'0000 0000	32	√	√	√	—
PCIEC address lower register 0	PCIEPALR0	R/W	—	H'0_3400	H'0000 0000	32	√	√	√	—
PCIEC address upper register 0	PCIEPAUR0	R/W	—	H'0_3404	H'0000 0000	32	√	√	√	—
PCIEC address mask register 0	PCIEPAMR0	R/W	—	H'0_3408	H'0000 0000	32	√	√	√	—
PCIEC conversion control register 0	PCIEPTCLR0	R/W	—	H'0_340C	H'0000 0000	32	√	√	√	—
PCIEC address lower register 1	PCIEPALR1	R/W	—	H'0_3420	H'0000 0000	32	√	√	√	—
PCIEC address upper register 1	PCIEPAUR1	R/W	—	H'0_3424	H'0000 0000	32	√	√	√	—

Register Name	Abbreviation	AX*1 R/W	PCI*1 R/W	Address Offset	Initial Value	Access Size	RZ/G Series Products			
							RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
PCIEC address mask register 1	PCIEPAMR1	R/W	—	H'0_3428	H'0000 0000	32	√	√	√	—
PCIEC conversion control register 1	PCIEPTCTLR1	R/W	—	H'0_342C	H'0000 0000	32	√	√	√	—
PCIEC address lower register 2	PCIEPALR2	R/W	—	H'0_3440	H'0000 0000	32	√	√	√	—
PCIEC address upper register 2	PCIEPAUR2	R/W	—	H'0_3444	H'0000 0000	32	√	√	√	—
PCIEC address mask register 2	PCIEPAMR2	R/W	—	H'0_3448	H'0000 0000	32	√	√	√	—
PCIEC conversion control register 2	PCIEPTCTLR2	R/W	—	H'0_344C	H'0000 0000	32	√	√	√	—
PCIEC address lower register 3	PCIEPALR3	R/W	—	H'0_3460	H'0000 0000	32	√	√	√	—
PCIEC address upper register 3	PCIEPAUR3	R/W	—	H'0_3464	H'0000 0000	32	√	√	√	—
PCIEC address mask register 3	PCIEPAMR3	R/W	—	H'0_3468	H'0000 0000	32	√	√	√	—
PCIEC conversion control register 3	PCIEPTCTLR3	R/W	—	H'0_346C	H'0000 0000	32	√	√	√	—
<b>PCIEC DMA control registers</b>										
PCIEC DMAC DMA operation register	PCIEDMAOR	R/W	—	H'0_4000	H'0000 0000	32	√	√	√	—
PCIEC DMAC PCI Express address lower register 0	PCIEDMPALR0	R/W	—	H'0_4100	H'0000 0000	32	√	√	√	—
PCIEC DMAC PCI Express address upper register 0	PCIEDMPAUR0	R/W	—	H'0_4104	H'0000 0000	32	√	√	√	—
PCIEC DMAC internal bus address register 0	PCIEDMIAR0	R/W	—	H'0_4108	H'0000 0000	32	√	√	√	—
PCIEC DMAC byte count register 0	PCIEDMBCNT R0	R/W	—	H'0_4110	H'0000 0000	32	√	√	√	—
PCIEC DMAC command chain address register 0	PCIEDMCCAR 0	R/W	—	H'0_4120	H'0000 0000	32	√	√	√	—
PCIEC DMAC channel control register 0	PCIEDMCHCR 0	R/W	—	H'0_4128	H'0000 0000	32	√	√	√	—
PCIEC DMAC channel status register 0	PCIEDMCHSR 0	R/W	—	H'0_412C	H'0000 0000	32	√	√	√	—
PCIEC DMAC channel control 2 register 0	PCIEDMCHC2 R0	R/W	—	H'0_4130	H'0000 0000	32	√	√	√	—
PCIEC DMAC PCI Express address lower register 1	PCIEDMPALR1	R/W	—	H'0_4140	H'0000 0000	32	√	√	√	—
PCIEC DMAC PCI Express address upper register 1	PCIEDMPAUR1	R/W	—	H'0_4144	H'0000 0000	32	√	√	√	—

Register Name	Abbreviation	AX*1 R/W	PCI*1 R/W	Address Offset	Initial Value	Access Size	RZ/G Series Products			
							RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
PCIEC DMAC internal bus address register 1	PCIEDMIAR1	R/W	—	H'0_4148	H'0000 0000	32	√	√	√	—
PCIEC DMAC byte count register 1	PCIEDMBCNT R1	R/W	—	H'0_4150	H'0000 0000	32	√	√	√	—
PCIEC DMAC command chain address register 1	PCIEDMCCAR 1	R/W	—	H'0_4160	H'0000 0000	32	√	√	√	—
PCIEC DMAC channel control register 1	PCIEDMCHCR 1	R/W	—	H'0_4168	H'0000 0000	32	√	√	√	—
PCIEC DMAC channel status register 1	PCIEDMCHSR 1	R/W	—	H'0_416C	H'0000 0000	32	√	√	√	—
PCIEC DMAC channel control 2 register 1	PCIEDMCHC2 R1	R/W	—	H'0_4170	H'0000 0000	32	√	√	√	—
PCIEC DMAC PCI Express address lower register 2	PCIEDMPALR2	R/W	—	H'0_4180	H'0000 0000	32	√	√	√	—
PCIEC DMAC PCI Express address upper register 2	PCIEDMPAUR2	R/W	—	H'0_4184	H'0000 0000	32	√	√	√	—
PCIEC DMAC internal bus address register 2	PCIEDMIAR2	R/W	—	H'0_4188	H'0000 0000	32	√	√	√	—
PCIEC DMAC byte count register 2	PCIEDMBCNT R2	R/W	—	H'0_4190	H'0000 0000	32	√	√	√	—
PCIEC DMAC command chain address register 2	PCIEDMCCAR 2	R/W	—	H'0_41A0	H'0000 0000	32	√	√	√	—
PCIEC DMAC channel control register 2	PCIEDMCHCR 2	R/W	—	H'0_41A8	H'0000 0000	32	√	√	√	—
PCIEC DMAC channel status register 2	PCIEDMCHSR 2	R/W	—	H'0_41AC	H'0000 0000	32	√	√	√	—
PCIEC DMAC channel control 2 register 2	PCIEDMCHC2 R2	R/W	—	H'0_41B0	H'0000 0000	32	√	√	√	—
PCIEC DMAC PCI Express address lower register 3	PCIEDMPALR3	R/W	—	H'0_41C0	H'0000 0000	32	√	√	√	—
PCIEC DMAC PCI Express address upper register 3	PCIEDMPAUR3	R/W	—	H'0_41C4	H'0000 0000	32	√	√	√	—
PCIEC DMAC internal bus address register 3	PCIEDMIAR3	R/W	—	H'0_41C8	H'0000 0000	32	√	√	√	—
PCIEC DMAC byte count register 3	PCIEDMBCNT R3	R/W	—	H'0_41D0	H'0000 0000	32	√	√	√	—
PCIEC DMAC command chain address register 3	PCIEDMCCAR 3	R/W	—	H'0_41E0	H'0000 0000	32	√	√	√	—
PCIEC DMAC channel control register 3	PCIEDMCHCR 3	R/W	—	H'0_41E8	H'0000 0000	32	√	√	√	—
PCIEC DMAC channel status register 3	PCIEDMCHSR 3	R/W	—	H'0_41EC	H'0000 0000	32	√	√	√	—

Register Name	Abbreviation	AX*1 R/W	PCI*1 R/W	Address Offset	Initial Value	Access Size	RZ/G Series Products			
							RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
PCIEC DMAC channel control 2 register 3	PCIEDMCHC2 R3	R/W	—	H'0_41F0	H'0000 0000	32	√	√	√	—
PCIEC DMAC PCI Express address lower register 4	PCIEDMPALR4	R/W	—	H'0_4200	H'0000 0000	32	√	√	√	—
PCIEC DMAC PCI Express address upper register 4	PCIEDMPAUR4	R/W	—	H'0_4204	H'0000 0000	32	√	√	√	—
PCIEC DMAC internal bus address register 4	PCIEDMIAR4	R/W	—	H'0_4208	H'0000 0000	32	√	√	√	—
PCIEC DMAC byte count register 4	PCIEDMBCNT R4	R/W	—	H'0_4210	H'0000 0000	32	√	√	√	—
PCIEC DMAC command chain address register 4	PCIEDMCCAR 4	R/W	—	H'0_4220	H'0000 0000	32	√	√	√	—
PCIEC DMAC channel control register 4	PCIEDMCHCR 4	R/W	—	H'0_4228	H'0000 0000	32	√	√	√	—
PCIEC DMAC channel status register 4	PCIEDMCHSR 4	R/W	—	H'0_422C	H'0000 0000	32	√	√	√	—
PCIEC DMAC channel control 2 register 4	PCIEDMCHC2 R4	R/W	—	H'0_4230	H'0000 0000	32	√	√	√	—
PCIEC DMAC PCI Express address lower register 5	PCIEDMPALR5	R/W	—	H'0_4240	H'0000 0000	32	√	√	√	—
PCIEC DMAC PCI Express address upper register 5	PCIEDMPAUR5	R/W	—	H'0_4244	H'0000 0000	32	√	√	√	—
PCIEC DMAC internal bus address register 5	PCIEDMIAR5	R/W	—	H'0_4248	H'0000 0000	32	√	√	√	—
PCIEC DMAC byte count register 5	PCIEDMBCNT R5	R/W	—	H'0_4250	H'0000 0000	32	√	√	√	—
PCIEC DMAC command chain address register 5	PCIEDMCCAR 5	R/W	—	H'0_4260	H'0000 0000	32	√	√	√	—
PCIEC DMAC channel control register 5	PCIEDMCHCR 5	R/W	—	H'0_4268	H'0000 0000	32	√	√	√	—
PCIEC DMAC channel status register 5	PCIEDMCHSR 5	R/W	—	H'0_426C	H'0000 0000	32	√	√	√	—
PCIEC DMAC channel control 2 register 5	PCIEDMCHC2 R5	R/W	—	H'0_4270	H'0000 0000	32	√	√	√	—
PCIEC DMAC PCI Express address lower register 6	PCIEDMPALR6	R/W	—	H'0_4280	H'0000 0000	32	√	√	√	—
PCIEC DMAC PCI Express address upper register 6	PCIEDMPAUR6	R/W	—	H'0_4284	H'0000 0000	32	√	√	√	—
PCIEC DMAC internal bus address register 6	PCIEDMIAR6	R/W	—	H'0_4288	H'0000 0000	32	√	√	√	—

Register Name	Abbreviation	AX*1 R/W	PCI*1 R/W	Address Offset	Initial Value	Access Size	RZ/G Series Products			
							RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
PCIEC DMAC byte count register 6	PCIEDMBCNT R6	R/W	—	H'0_4290	H'0000 0000	32	√	√	√	—
PCIEC DMAC command chain address register 6	PCIEDMCCAR 6	R/W	—	H'0_42A0	H'0000 0000	32	√	√	√	—
PCIEC DMAC channel control register 6	PCIEDMCHCR 6	R/W	—	H'0_42A8	H'0000 0000	32	√	√	√	—
PCIEC DMAC channel status register 6	PCIEDMCHSR 6	R/W	—	H'0_42AC	H'0000 0000	32	√	√	√	—
PCIEC DMAC channel control 2 register 6	PCIEDMCHC2 R6	R/W	—	H'0_42B0	H'0000 0000	32	√	√	√	—
PCIEC DMAC PCI Express address lower register 7	PCIEDMPALR7	R/W	—	H'0_42C0	H'0000 0000	32	√	√	√	—
PCIEC DMAC PCI Express address upper register 7	PCIEDMPAUR7	R/W	—	H'0_42C4	H'0000 0000	32	√	√	√	—
PCIEC DMAC internal bus address register 7	PCIEDMIAR7	R/W	—	H'0_42C8	H'0000 0000	32	√	√	√	—
PCIEC DMAC byte count register 7	PCIEDMBCNT R7	R/W	—	H'0_42D0	H'0000 0000	32	√	√	√	—
PCIEC DMAC command chain address register 7	PCIEDMCCAR 7	R/W	—	H'0_42E0	H'0000 0000	32	√	√	√	—
PCIEC DMAC channel control register 7	PCIEDMCHCR 7	R/W	—	H'0_42E8	H'0000 0000	32	√	√	√	—
PCIEC DMAC channel status register 7	PCIEDMCHSR 7	R/W	—	H'0_42EC	H'0000 0000	32	√	√	√	—
PCIEC DMAC channel control 2 register 7	PCIEDMCHC2 R7	R/W	—	H'0_42F0	H'0000 0000	32	√	√	√	—
<b>Configuration registers</b>										
PCI configuration register 0	PCICONF0	R	R	H'1_0000	H'0018 1912	32	√	√	√	—
PCI configuration register 1	PCICONF1	R/W	R/W	H'1_0004	H'0010 0000	32	√	√	√	—
PCI configuration register 2	PCICONF2	R	R	H'1_0008	H'FF00 0000	32	√	√	√	—
PCI configuration register 3	PCICONF3	R/W	R/W	H'1_000C	H'0001 0000	32	√	√	√	—
PCI configuration register 4	PCICONF4	*2	RW/R	H'1_0010	*2	32	√	√	√	—
PCI configuration register 5	PCICONF5	*3	RW/R	H'1_0014	*3	32	√	√	√	—
PCI configuration register 6	PCICONF6	Header TYPE00:*4 Header TYPE01: R/W	Header TYPE00: RW/R Header TYPE01: —	H'1_0018	Header TYPE00:*4 Header TYPE01: H'0000 0000	32	√	√	√	—

Register Name	Abbreviation	AX*1 R/W	PCI*1 R/W	Address Offset	Initial Value	Access Size	RZ/G Series Products			
							RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
PCI configuration register 7	PCICONF7	Header TYPE00:*5 Header TYPE01: R/W	Header TYPE00: RW/R Header TYPE01: —	H'1_001C	Header TYPE00:*5 Header TYPE01: H'0000 0000	32	√	√	√	—
PCI configuration register 8	PCICONF8	Header TYPE00:*6 Header TYPE01: R/W	Header TYPE00: RW/R Header TYPE01: —	H'1_0020	Header TYPE00:*6 Header TYPE01: H'0000 0000	32	√	√	√	—
PCI configuration register 9	PCICONF9	Header TYPE00:*7 Header TYPE01: R/W	Header TYPE00: RW/R Header TYPE01: —	H'1_0024	Header TYPE00:*7 Header TYPE01: H'0000 0000	32	√	√	√	—
PCI configuration register 10	PCICONF10	Header TYPE00: R Header TYPE01: R/W	Header TYPE00: R Header TYPE01: —	H'1_0028	Header TYPE00: H'0000 0000 Header TYPE01: H'0000 0000	32	√	√	√	—
PCI configuration register 11	PCICONF11	Header TYPE00: R Header TYPE01: R/W	Header TYPE00: R Header TYPE01: —	H'1_002C	Header TYPE00: H'0000 0000 Header TYPE01: H'0000 0000	32	√	√	√	—
PCI configuration register 12	PCICONF12	Header TYPE00: R Header TYPE01: R/W	Header TYPE00: R Header TYPE01: —	H'1_0030	Header TYPE00: H'0000 0000 Header TYPE01: H'0000 0000	32	√	√	√	—
PCI configuration register 13	PCICONF13	R/W	R	H'1_0034	H'0000 0040	32	√	√	√	—
PCI configuration register 14	PCICONF14	Header TYPE00: R Header TYPE01: R	Header TYPE00: R Header TYPE01: —	H'1_0038	Header TYPE00: H'0000 0000 Header TYPE01: H'0000 0000	32	√	√	√	—
PCI configuration register 15	PCICONF15	Header TYPE00: R/W Header TYPE01: R/W	Header TYPE00: R/W Header TYPE01: —	H'1_003C	Header TYPE00: H'0000 00FF Header TYPE01: H'0000 00FF	32	√	√	√	—
PCI power management capability register 0	PMCAPO	R/W	R	H'1_0040	H'C803 5001	32	√	√	√	—



Register Name	Abbreviation	AX*1 R/W	PCI*1 R/W	Address Offset	Initial Value	Access Size	RZ/G Series Products			
							RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
PCI power management capability register 1	PMCAP1	R/W	R/W	H'1_0044	H'0000 0000	32	√	√	√	—
MSI capability register 0	MSICAP0	R/W	R/W	H'1_0050	H'0180 7005	32	√	√	√	—
MSI capability register 1	MSICAP1	R/W	R/W	H'1_0054	H'0000 0000	32	√	√	√	—
MSI capability register 2	MSICAP2	R/W	R/W	H'1_0058	H'0000 0000	32	√	√	√	—
MSI capability register 3	MSICAP3	R/W	R/W	H'1_005C	H'0000 0000	32	√	√	√	—
MSI capability register 4	MSICAP4	R/W	R/W	H'1_0060	H'0000 0000	32	√	√	√	—
MSI capability register 5	MSICAP5	R	R	H'1_0064	H'0000 0000	32	√	√	√	—
PCI Express capability register 0	EXPCAP0	R/W	R	H'1_0070	H'0042 0010	32	√	√	√	—
PCI Express capability list register										
PCI Express capabilities register										
PCI Express capability register 1	EXPCAP1	R/W	R	H'1_0074	H'0000 8020	32	√	√	√	—
Device capabilities register										
CI Express capability register 2	EXPCAP2	R/W	R/W	H'1_0078	H'0000 2810	32	√	√	√	—
Device control register										
Device status register										
PCI Express capability register 3	EXPCAP3	R/W	R	H'1_007C	H'0003 F412	32	√	√	√	—
Link capabilities register										
PCI Express capability register 4	EXPCAP4	R/W	R/W	H'1_0080	H'0041 0000	32	√	√	√	—
Link control register										
Link status register										
PCI Express capability register 5	EXPCAP5	Header TYPE00: R	Header TYPE00: R	H'1_0084	Header TYPE00: H'0000 0000	32	√	√	√	—
Slot capabilities register		Header TYPE01: R	Header TYPE01: —		Header TYPE01: H'0000 0000					
PCI Express capability register 6	EXPCAP6	Header TYPE00: R	Header TYPE00: R	H'1_0088	Header TYPE00: H'0000 0000	32	√	√	√	—
Slot control register		Header TYPE01: R	Header TYPE01: —		Header TYPE01: H'0040 0000					
Slot status register										

Register Name	Abbreviation	AX*1 R/W	PCI*1 R/W	Address Offset	Initial Value	Access Size	RZ/G Series Products			
							RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
PCI Express capability register 7	EXPCAP7	Header TYPE00: R	Header TYPE00: R	H'1_008C	Header TYPE00: H'0000 0000	32	√	√	√	—
Root control register										
Root capabilities register		Header TYPE01: R/W	Header TYPE01: —		Header TYPE01: H'0000 0000					
PCI Express capability register 8	EXPCAP8	Header TYPE00: R	Header TYPE00: R	H'1_0090	Header TYPE00: H'0000 0000	32	√	√	√	—
Root status register										
		Header TYPE01: R/W	Header TYPE01: —		Header TYPE01: H'0000 0000					
PCI Express capability register 9	EXPCAP9	R/W	R	H'1_0094	H'0000 0010	32	√	√	√	—
Device capabilities 2 register										
PCI Express capability register 10	EXPCAP10	R/W	R/W	H'1_0098	H'0000 0000	32	√	√	√	—
Device control 2 register										
Device status 2 register										
PCI Express capability register 11	EXPCAP11	R	R	H'1_009C	H'0000 0000	32	√	√	√	—
Link capabilities 2 register										
PCI Express capability register 12	EXPCAP12	R/W	R/W	H'1_00A0	H'0001 0002	32	√	√	√	—
Link control 2 register										
Link status 2 register										
PCI Express capability register 13	EXPCAP13	R	R	H'1_00A4	H'0000 0000	32	√	√	√	—
Slot capabilities 2 register										
PCI Express capability register 14	EXPCAP14	R	R	H'1_00A8	H'0000 0000	32	√	√	√	—
Slot control 2 register										
Slot status 2 register										
VC capability register 0	VCCAP0	R/W	R	H'1_0100	H'1B01 0002	32	√	√	√	—
Virtual channel enhanced capability header										
VC capability register 1	VCCAP1	R/W	R	H'1_0104	H'0000 0000	32	√	√	√	—
Port VC capability register 1										
VC capability register 2	VCCAP2	R	R	H'1_0108	H'0000 0000	32	√	√	√	—
Port VC capability register 2										

							RZ/G Series Products			
Register Name	Abbreviation	AX*1 R/W	PCI*1 R/W	Address Offset	Initial Value	Access Size	RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
VC capability register 3 Port VC status register Port VC control register	VCCAP3	R	R	H'1_010C	H'0000 0000	32	√	√	√	—
VC capability register 4 VC0 resource capability register	VCCAP4	R/W	R	H'1_0110	H'0000 0000	32	√	√	√	—
VC capability register 5 VC0 resource control register	VCCAP5	R/W	R/W	H'1_0114	H'8000 00FF	32	√	√	√	—
VC capability register 6 VC0 resource status register	VCCAP6	R	R	H'1_0118	H'0002 0000	32	√	√	√	—
Device serial number capability register 0	SERNUMCAP0	R/W	R	H'1_01B0	H'0001 0003	32	√	√	√	—
Device serial number capability register 1	SERNUMCAP1	R	R	H'1_01B4	H'0000 0000	32	√	√	√	—
Device serial number capability register 2	SERNUMCAP2	R	R	H'1_01B8	H'0000 0000	32	√	√	√	—
<b>PCIEC link layer control registers</b>										
ID setting register 0	IDSETR0	R/W	—	H'1_1000	H'0018 1912	32	√	√	√	—
ID setting register 1	IDSETR1	R/W	—	H'1_1004	H'FF00 0000	32	√	√	√	—
SUBID setting register	SUBIDSETR	R/W	—	H'1_1024	H'0000 0000	32	√	√	√	—
Device serial number setting register 0	DSERSETR0	R/W	—	H'1_102C	H'0000 0000	32	√	√	√	—
Device serial number setting register 1	DSERSETR1	R/W	—	H'1_1030	H'0000 0000	32	√	√	√	—
TL control register	TLCTLR	R/W	—	H'1_1048	H'0000 0000	32	√	√	√	—
MAC status register	MACCSR	R/W	—	H'1_1054	H'0041 0000	32	√	√	√	—
MAC control register	MACCTLR	R/W	—	H'1_1058	H'80FF 0001	32	√	√	√	—
PM status register	PMSR	R/W	—	H'1_105C	H'0000 0000	32	√	√	√	—
PM control register	PMCTLR	R/W	—	H'1_1060	H'0000 0000	32	√	√	√	—
MAC interrupt enable register	MACINTENR	R/W	—	H'1_106C	H'0000 0000	32	√	√	√	—
PM interrupt enable register	PMINTENR	R/W	—	H'1_1070	H'0000 0000	32	√	√	√	—
MAC status register 2	MACS2R	R	—	H'1_1078	H'0041 0001	32	√	√	√	—
MAC control register 2	MACCTL2R	R/W	—	H'1_107C	H'0000 0002	32	√	√	√	—
MAC speed change setting register	MACCGSPSET R	R/W	—	H'1_1084	H'0002 0000	32	√	√	√	—

Notes: 1. AX: AXI bus (internal bus)

PCI: PCI local bus

'—' in R/W column: Access prohibited.

For details of R/W attribute for each bit, see section 39.2, Register Description.

2. Depends on the setting of the local address mask register 0.

3. Depends on the setting of the local address mask register 1.
4. Depends on the setting of the local address mask register 2.
5. Depends on the setting of the local address mask register 3.
6. Depends on the setting of the local address mask register 4.
7. Depends on the setting of the local address mask register 5.

Do not write to any addresses other than listed above. Operations cannot be guaranteed if writing is attempted. Values read from addresses other than those listed above are undefined.

## 39.2 Register Description

[Legend for the Register Description]

A bit assignment figure is shown for each register. The initial value and R/W attribute are indicated for each bit.

Bit: Bit number or bit range

Bit Name: Bit name or field name

Initial value: Register value after a reset

—: Undefined value

R/W: Readable/writable. The written value can be read.

RWC1: Readable/writable. The bit is initialized when 1 is written. Writing 0 is ignored.

R: Read-only. The write value should always be 0. (If there is a direction on a read or write value in the Description column, set the bit as directed.)

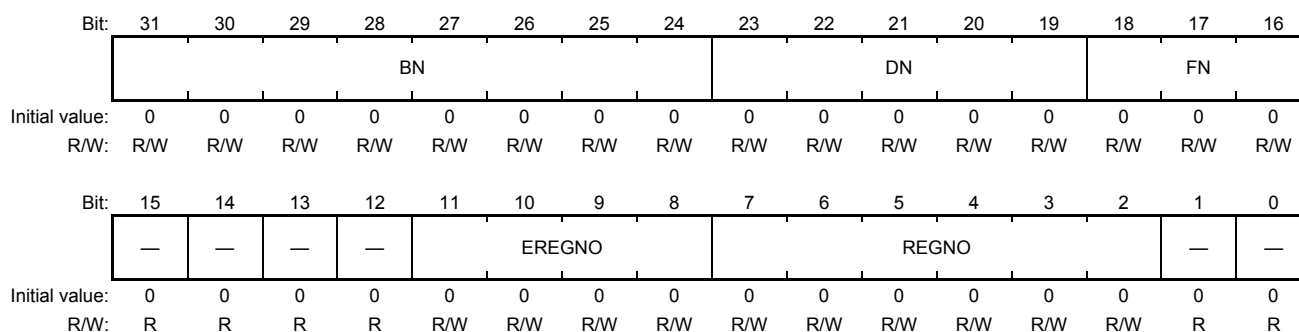
RWS\*: Sticky-read write bit. Readable/writable. The bit is not initialized by a hot reset.

RW1CS\*: Sticky-read-only status bit. The bit is initialized when 1 is written. Writing 0 is ignored. The bit is not initialized by a hot reset.

Note: \* RWS and RW1CS are only used for the configuration registers. For details, see section 39.4.1, Write/Read Attributes of Configuration Registers.

### 39.2.1 Configuration Transmission Address Register (PCIECAR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	BN	H'00	R/W	<b>Bus Number</b> Specifies the number of the bus to be accessed when a configuration request is issued.
23 to 19	DN	00000	R/W	<b>Device Number</b> Specifies the number of the device to be accessed when a configuration request is issued.  Note: A type 0 configuration request can be issued only to device #0; do not send a type 0 configuration request to the device with the other number.
18 to 16	FN	000	R/W	<b>Function Number</b> Specifies the number of the function to be accessed when a configuration request is issued.
15 to 12	—	All 0	R	<b>Reserved</b> These bits are always read as 0. The write value should always be 0.
11 to 8	EREGNO	H'0	R/W	<b>Extended Register No.</b> Specifies the number of the extended register to be accessed when a configuration request is issued.
7 to 2	REGNO	H'00	R/W	<b>Register No.</b> Specifies the number of the register to be accessed when a configuration request is issued.
1, 0	—	All 0	R	<b>Reserved</b> These bits are always read as 0. The write value should always be 0.

### 39.2.2 Configuration Transmission Control Register (PCIECCTLR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CCIE	—	—	—	—	—	—	—	—	—	WUR	WCRS	—	—	RUR	RCRS
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R	R	R	R	R	R	R	RW1C	RW1C	R	R	RW1C	RW1C
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	TYPE	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R	R	R	R	R	R	R	R

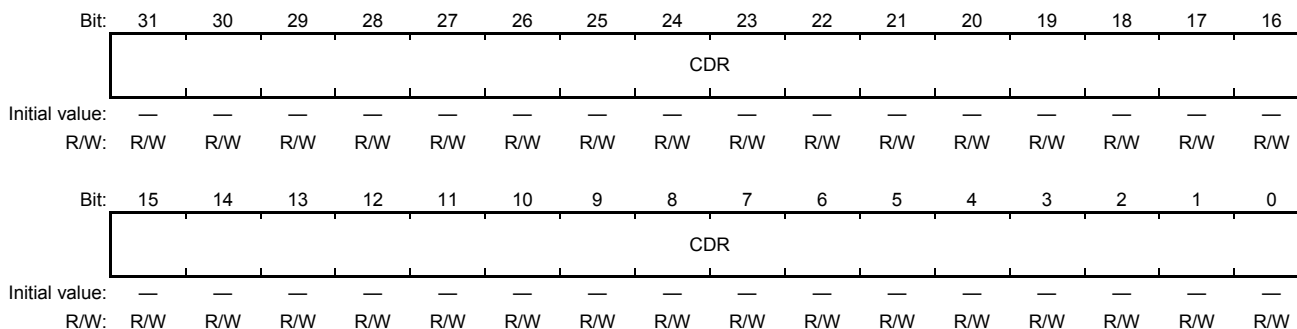
Bit	Bit Name	Initial Value	R/W	Description
31	CCIE	0	R/W	<p>Configuration Send Enable</p> <p>Enables issuance of a configuration request.</p> <p>Set to 1 when the configuration transmission address register and configuration transmission data register are used to issue the configuration cycle.</p>
30 to 22	—	All 0	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>
21	WUR	0	RW1C	<p>Write Unsupported Request</p> <p>Indicates that an unsupported request has been received.</p> <p>This bit is set to 1 when a completion with the unsupported request status is received in response to the configuration write request transmitted.</p>
20	WCRS	0	RW1C	<p>Write CRS</p> <p>Indicates that CRS (configuration retry status) has been received.</p> <p>This bit is set to 1 when a completion with the CRS status is received in response to the configuration write request transmitted.</p>
19, 18	—	All 0	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>
17	RUR	0	RW1C	<p>Read Unsupported Request</p> <p>Indicates that an unsupported request has been received.</p> <p>This bit is set to 1 when a completion with the unsupported request status is received in response to the configuration read request transmitted.</p>
16	RCRS	0	RW1C	<p>Read CRS</p> <p>Indicates that CRS (configuration retry status) has been received.</p> <p>This bit is set to 1 when a Completion with the CRS status is received in response to the configuration read request transmitted.</p>
15 to 9	—	All 0	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>

Bit	Bit Name	Initial Value	R/W	Description
8	TYPE	0	R/W	<p>TYPE</p> <p>Specifies the type of a configuration request issued by accessing the PCIECDR register.</p> <p>0: Type 0 configuration request 1: Type 1 configuration request</p> <p>Note: A type 0 configuration request can be issued only to device #0; do not send a type 0 configuration request to the device with the other number.</p>
7 to 0	—	All 0	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>



### 39.2.3 Configuration Transmission Data Register (PCIECDR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	CDR	—	R/W	<p>Configuration Data Register</p> <p>Allows a configuration request to be issued.</p> <p>A write access to this field allows issuance of a configuration write request containing the information written to this field as data.</p> <p>A read access to this field allows issuance of a configuration read request and reading of the data contained in the response.</p> <p>When the peer device returns an unsupported request response, the read value is H'FFFFFFFF.</p> <p>When EXPCAP7[4].CRSVISE = 0:</p> <p>When the peer device returns a CRS response, the read value is H'FFFFFFFF (error response).</p> <p>When EXPCAP7[4].CRSVISE = 1:</p> <p>Until the peer device returns a response other than a CRS response, the first access to the peer device should be a read access to register address 0.</p> <p>When the peer device returns a CRS response, the read value is H'FFF0001.</p> <p>In Endpoint mode, this field must not be accessed.</p> <p>Except when PCIECCTLR.CCIE = 1 and PCIETCTLR.CFINIT = 1, the read value is H'FFFFFFFF.</p>

### 39.2.4 Mode Setting Register (PCIEMSR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PEM
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	PEM	1	R/W	PCI Express Mode Sets operating mode of the PCI Express. 0: Operates as a PCI Express Endpoint. 1: Operates as a PCI Express Root Port.

### 39.2.5 Unlock Transmission Control Register (PCIEUNLOCKCR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ASTUN LOCK
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	ASTUNLOCK	0	R/W	Assert Unlock Specifies issuance of an unlock message. Writing 1 to this bit allows issuance of an unlock message (message code = B'0000_0000; routing = B'011). Transmission of an unlock message through a write access to this bit can be used only in Root Port mode. Transmission of an unlock message from an Endpoint is prohibited by the standard. While a link is not established, do not write 1 to this bit. This bit is always read as 0.

### 39.2.6 INTx Register (PCIEINTXR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ASTINT X
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	INTDE	INTCE	INTBE	INTAE	—	—	—	—	INTD	INTC	INTB	INTA
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 17	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
16	ASTINTX	0	R/W	Assert INTx Specifies generation of an INTx interrupt. Writing 1 to this bit asserts the INTx interrupt specified by the PCICONF15[15:8].Interrupt Pin bits and writing 0 deasserts the INTx interrupt. When generating an INTx interrupt using this bit, the PCICONF1[10].INTDIS bit must be 0. This bit is cleared if the PCICONF1[10].Interrupt Disable bit is set to 1 while this bit is 1. When MSI is used, an INTx interrupt cannot be used. Therefore, when the MSICAP0[16].MSI Enable bit is 1, 1 cannot be written to this bit. This bit is cleared if the MSICAP0[16].MSI Enable bit is set to 1 while this bit is 1. This bit is valid only in Endpoint mode. When a link goes down, this bit is cleared. A write access is ignored while a link is down.
15 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11	INTDE	0	R/W	INTD Enable Enables generation of an interrupt by INTD assertion. This bit is valid only in Root Port mode.
10	INTCE	0	R/W	INTC Enable Enables generation of an interrupt by INTC assertion. This bit is valid only in Root Port mode.
9	INTBE	0	R/W	INTB Enable Enables generation of an interrupt by INTB assertion. This bit is valid only in Root Port mode.
8	INTAE	0	R/W	INTA Enable Enables generation of an interrupt by INTA assertion. This bit is valid only in Root Port mode.

Bit	Bit Name	Initial Value	R/W	Description
7 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3	INTD	0	R	Indicates that INTD has been asserted by a PCI Express interrupt. This bit is asserted upon reception of an Assert_INTD message and deasserted upon reception of a Deassert_INTD message. When this bit is asserted while PCICONF15[7:0].Interrupt Line is not H'FF and PCIEINTXR[11].INTDE is 1, the interrupt is generated. This bit is valid only in Root Port mode.
2	INTC	0	R	Indicates that INTC has been asserted by a PCI Express interrupt. This bit is asserted upon reception of an Assert_INTC message and deasserted upon reception of a Deassert_INTC message. When this bit is asserted while PCICONF15[7:0].Interrupt Line is not H'FF and PCIEINTXR[10].INTCE is 1, the interrupt is generated. This bit is valid only in Root Port mode.
1	INTB	0	R	Indicates that INTB has been asserted by a PCI Express interrupt. This bit is asserted upon reception of an Assert_INTB message and deasserted upon reception of a Deassert_INTB message. When this bit is asserted while PCICONF15[7:0].Interrupt Line is not H'FF and PCIEINTXR[9].INTBE is 1, the interrupt is generated. This bit is valid only in Root Port mode.
0	INTA	0	R	Indicates that INTA has been asserted by a PCI Express interrupt. This bit is asserted upon reception of an Assert_INTA message and deasserted upon reception of a Deassert_INTA message. When this bit is asserted while PCICONF15[7:0].Interrupt Line is not H'FF and PCIEINTXR[8].INTAE is 1, the interrupt is generated. This bit is valid only in Root Port mode.

**39.2.7 Message Reception Status Register (PCIERMSGR)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	SLOT_POWER	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	RW1C	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12	SLOT_POWER	0	RW1C	SLOT_POWER Indicates that the Set_Slot_Power_Limit message has been received. This bit is valid only in Endpoint mode.
11 to 0	—	All 0	R	Reserved Ignore the value in this field. The read value is undefined. The write value should always be 0.

### 39.2.8 Message Reception Interrupt Enable Register (PCIERMSGIER)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	SLOT_P OWERE	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12	SLOT_POWERE	0	R/W	SLOT_POWERE Enables generation of an interrupt upon reception of a Set_Slot_Power_Limit message.
11 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

### 39.2.9 Power Management Message Transmission Control Register (PCIEPMMMSGCR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	PM_PME	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9	PM_PME	0	R/W	Specifies issuance of a PM_PME message. Writing 1 to this bit allows issuance of a PM_PME Message (message code = B'0001_1000; routing = B'000). This bit is always read as 0. Transmission of a PM_PME message through a write access to this bit can be used only in Endpoint mode. Transmission of a PM_PME message from a Root Port is prohibited by the standard. While a link is not established, do not write 1 to this bit.
8 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.



### 39.2.10 Physical Layer Status Register (PCIEPHYSR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	PHYRD YCE	—	—	—	—	—	—	—	PHYRD YC
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R	R	R	R	R	R	R	RW1C
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PHYRD Y
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 25	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
24	PHYRDYCE	0	R/W	PHYRDY Change Enable Enables generation of an INT_PCISC interrupt upon change of PHYRDY.
23 to 17	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
16	PHYRDYC	0	RW1C	PHYRDY Change Indicates that PHYRDY has changed.
15 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	PHYRDY	0	R	0: Indicates that the clock supplied by the physical layer has not been stabilized and that it is not ready to be used. 1: Indicates that the clock supplied by the physical layer has been stabilized and that it is ready to be used.

### 39.2.11 MSI Transmission Register (PCIEMSITXR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	MSIE	—	—	—	—	—	—	—	—	—	—	MMENUM				
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSIPC LR	—	—	—	—	—	—	—	—	—	—	MSIAST				
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	MSIE	0	R	MSI Enable Indicates the MSICAP0[16]. MSIE value.
30 to 21	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
20 to 16	MMENUM	0_0000	R	Multiple Message Enable Number Indicates the number of sources specified with MSICAP0[22:20].MMESE. 0_0000: 1 source (only source number 0 is available) 0_0001: 2 sources (source numbers 0 and 1 are available) 0_0011: 4 sources (source numbers 0 to 3 are available) 0_0111: 8 sources (source numbers 0 to 7 are available) 0_1111: 16 sources (source numbers 0 to 15 are available) 1_1111: 32 sources (source numbers 0 to 31 are available)
15	MSIPC LR	0	R/W	MSI Pending Clear Forcibly clears the MSI interrupt sources to be transmitted. If the MSI source is canceled because of the user side reason (internal source), set the information of the MSI interrupt to be cleared to the MSI Assert field, and simultaneously write 1 to this bit. In the other cases, hold this bit to 0. This bit is always read as 0.
14 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

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Bit	Bit Name	Initial Value	R/W	Description
4 to 0	MSIAST	0_0000	R/W	<p>MSI Assert</p> <p>Specifies generation of an MSI interrupt.</p> <p>This field is valid only when the MSI is enabled in Endpoint mode.</p> <p>A write access to this field allows setting of the relevant bits to 1 in MSICAP5.Message Pending. After that, among the MSI interrupts whose corresponding bits are 0 in MSICAP4.Message Mask, the MSI interrupts are allowed to be generated one by one in ascending order of the assigned number.</p> <p>The maximum source number that may be written to this field is indicated by the Multiple Message Enable Number field.</p> <p>These bits are always read as 0.</p> <p>While communication with the connection destination device is not established, do not write to this field.</p>

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### 39.2.12 Transfer Control Register (PCIETCLR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	DL_DOWN	—	—	CF_INIT
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3	DL_DOWN	1	R	DL_DOWN Indicates whether connection in the data link layer is lost. This bit is set to 1 after cancellation of a reset. This bit is cleared to 0 when a connection with the target device is established, and set to 1 when a connection in the data link layer is lost due to communication failure.
2, 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	CFINIT	0	R/W	Configuration Initialization Specifies initialization of registers to establish a PCI Express link. Set this bit to 1 after setting the appropriate values in the following registers. PCIELAR0 to PCIELAR 5 PCIELAMR0 to PCIELAMR5 The above registers must not be written to while this bit is 1. Setting this bit starts PCI Express link establishment process. Only writing 1 to this bit is valid; writing 0 is invalid. Write 1 at initialization only once and do not write any value to this bit after that. 0: Initialization has not yet been done. 1: Initialization has been completed. In Endpoint mode: Triggered by this bit, hardware sets the BARn registers based on PCIELAMRn.

### 39.2.13 Transfer Status Register (PCIETSTR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	MSIEC	—	—	—	—	—	—	—	—	—	—	—	DLLACTC
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	RW1C	R	R	R	R	R	R	R	R	R	R	R	RW1C

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	INTXDC	—	—	—	—	—	—	—	—	—	—	—	DLLACT
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	RW1C	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28	MSIEC	0	RW1C	MSI Enable Change Indicates that MSICAP0[16].MSIE has changed.
27 to 17	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
16	DLLACTC	0	RW1C	DLLACT Change Indicates that DLLACT has changed.
15 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12	INTXDC	0	RW1C	INTx Disable Change Indicates that PCICONF1[10].INTDIS has changed.
11 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	DLLACT	0	R	Data Link Layer Active Indicates that the data link layer is active.

## 39.2.14 Interrupt Register (PCIEINTR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	INT_PCI TE	INT_PM_ PME_RCV	INT_TX ALLEMP	INT_PCI BW	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	RW1C	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	INT_ MAC	INT_ PM	—	—	—	—	—	—	INT_PCI MES	INT_PCI POWER	INT_PCI CERR	INT_PCI NFERR	INT_PCI FERR	INT_PCI SERR
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	RW1C	R/RW1C	R/RW1C	R/RW1C	R

Bit	Bit Name	Initial Value	R/W	Description
31	INT_PCITE	0	RW1C	<p>Interrupt PCI Express Transfer Error</p> <p>Indicates that the interrupt by a PCI Express transfer error has been generated.</p> <p>The error can be either of the following.</p> <ul style="list-style-type: none"> <li>When PCIECCTLR[31].CCIE = 0, PCIECDR is accessed.</li> <li>When PCIEPCTLRn[31].PARE = 0, the corresponding PIO space is accessed.</li> <li>Transfer is executed with TC being set that is not mapped to VC0.</li> <li>When PCICONF1[2].BME = 0 in Endpoint mode, PIO transfer is executed (MRd, MWr).</li> <li>Transfer is executed with the attribute being set that is not enabled with the configuration register.</li> <li>Transfer other than PME message (PM_PME) transfer is executed in the non-D0 state.</li> <li>When PMCAP1[8].PMEE = 0 in Endpoint mode, PM_PME message transfer is executed.</li> </ul>
30	INT_PM_PME_RCV	0	R	<p>Interrupt PM_PME Receive</p> <p>Generates an interrupt when PM_PME is received.</p> <p>This bit is valid only in Root Port mode. To clear the interrupt, write 1 to EXPCAP8[16].PMEST.</p>
29	INT_TXALLEMP	1	R	<p>Interrupt TX All Empty</p> <p>Generates an interrupt when all the transmission buffers are empty for PCI Express.</p>
28	INT_PCIBW	0	R	<p>Interrupt PCI Express Bandwidth</p> <p>Indicates that the interrupt by change of the link bandwidth (link width × link speed) has been generated.</p> <p>This bit is valid only in Root Port mode. To clear the interrupt, write 1 to EXPCAP4[31].LKAUTOBWSTS or EXPCAP4[30].LKBWMNGSTS.</p>
27 to 14	—	All 0	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>

Bit	Bit Name	Initial Value	R/W	Description
13	INT_MAC	0	R	<p>Interrupt MAC</p> <p>Indicates that the MAC interrupt has been generated. To clear the interrupt, write 1 to the corresponding field in MACSR.</p>
12	INT_PM	0	R	<p>Interrupt PM</p> <p>Indicates that the PM interrupt has been generated. To clear the interrupt, write 1 to the corresponding field in PMSR.</p>
11 to 6	—	All 0	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>
5	INT_PCIMES	0	R	<p>Interrupt PCI Message</p> <p>Indicates that the interrupt has been generated upon reception of a PCI Express message.</p> <p>However, if the interrupt corresponding to individual message is not enabled, this interrupt is not generated; process the message through software when a message is received.</p>
4	INT_PCIPOWER	0	RW1C	<p>Interrupt PCI Express Power</p> <p>Indicates that a configuration write request has been received in Endpoint mode thus generating a request for a power down sequence to the L1 state.</p>
3	INT_PCICERR	0	R/RW1C	<p>Interrupt PCI Correctable Error</p> <p>Root Port:</p> <p>Indicates that the interrupt has been generated by detection of the correctable error or reception of the ERR_COR message. This bit is a read-only bit; to clear this bit, use the configuration register.</p> <p>Endpoint:</p> <p>Indicates that an error classified as ERR_COR has been generated. This bit is a read-write-1-to-clear bit; writing 1 clears this bit only.</p>
2	INT_PCINFERR	0	R/RW1C	<p>Interrupt PCI Non-Fatal Error</p> <p>Root Port:</p> <p>Indicates that the interrupt has been generated by detection of the non-fatal error or reception of the ERR_NONFATAL message. This bit is a read-only bit; to clear this bit, use the configuration register.</p> <p>Endpoint:</p> <p>Indicates that an error classified as ERR_NONFATAL has been generated. This bit is a read-write-1-to-clear bit; writing 1 clears this bit only.</p>

Bit	Bit Name	Initial Value	R/W	Description
1	INT_PCIFERR	0	R/RW1C	<p>Interrupt PCI Fatal Error</p> <p>Root Port: Indicates that the interrupt has been generated by detection of the fatal error or reception of the ERR_FATAL message. This bit is a read-only bit; to clear this bit, use the configuration register.</p> <p>Endpoint: Indicates that an error classified as ERR_FATAL has been generated. This bit is a read-write-1-to-clear bit; writing 1 clears this bit only.</p>
0	INT_PCISERR	0	R	<p>Interrupt PCI System Error</p> <p>Indicates that a system error has occurred.</p> <p>When a system error occurs, check the related registers through software and execute error recovery processing.</p> <p>A system error is: A PCIEERRFR error has occurred (when enabled).</p>



### 39.2.15 Interrupt Enable Register (PCIEINTER)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	INT_PCITEE	INT_PM_PME_RCVE	INT_TXALLEMPE	INT_PCIBWE	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	INT_MACE	INT_PME	—	—	—	—	—	—	INT_PCIMесе	INT_PCIPOWERE	INT_PCICERRE	INT_PCINFERRE	INT_PCIFERRE	INT_PCISERRE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	INT_PCITEE	0	R/W	Interrupt PCI Express Transfer Error Enable Enables generation of an interrupt by a PCI Express transfer error.
30	INT_PM_PME_RCVE	0	R/W	Interrupt PM_PME Receive Enable Enables generation of an interrupt by INT_PM_PME_RCV.
29	INT_TXALLEMPE	0	R/W	Interrupt TX All Empty Enable Enables generation of an interrupt when all the transmission buffers are empty for PCI Express.
28	INT_PCIBWE	0	R/W	Interrupt PCI Express Bandwidth Enable Enables generation of an interrupt by change of the link bandwidth.
27 to 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13	INT_MACE	0	R/W	Interrupt MAC Enable Enables generation of the MAC interrupt.
12	INT_PME	0	R/W	Interrupt PM Enable Enables generation of the PM interrupt.
11 to 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5	INT_PCIMесе	0	R/W	Interrupt Message Enable Enables generation of the PCI Express message reception interrupt.
4	INT_PCIPOWERE	0	R/W	Interrupt PCI Express Power Enable Enables generation of an interrupt by a request for a power down sequence to the L1 state.
3	INT_PCICERRE	0	R/W	Interrupt Correctable Error Enable Enables generation of an interrupt by a correctable error.
2	INT_PCINFERRE	0	R/W	Interrupt Non-Fatal Error Enable Enables generation of an interrupt by a non-fatal error.

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<b>Bit</b>	<b>Bit Name</b>	<b>Initial Value</b>	<b>R/W</b>	<b>Description</b>
1	INT_PCIFERRE	0	R/W	Interrupt Fatal Error Enable Enables generation of an interrupt by a fatal error.
0	INT_PCISERRE	0	R/W	Interrupt System Error Enable Enables generation of an interrupt by a system error.

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## 39.2.16 Error Factor Register (PCIEERRFR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	IBERR	MTLP	UR	PTLP	—	—	—	POVF	NPOVF	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	RW1C	RW1C	RW1C	RW1C	R	R	R	RW1C	RW1C	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	RCVCP LLK	UNEXP CPL	—	—	RCVSZ ECPL	CPLTO UT	—	RCVCR SCPL	RCVCA CPL	RCVUR CPL	—	—	SENDC ACPL	SENDU RCPL
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	RW1C	RW1C	R	R	RW1C	RW1C	R	RW1C	RW1C	RW1C	R	R	RW1C	RW1C

Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28	IBERR	0	RW1C	IBERR Indicates that a transfer error has occurred on the internal bus.
27	MTLP	0	RW1C	MTLP Indicates that a malformed TLP has been received.
26	UR	0	RW1C	UR Indicates that an unsupported request has been received.
25	PTLP	0	RW1C	PTLP Indicates that a poisoned TLP has been received.
24 to 22	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
21	POVF	0	RW1C	POVF Indicates that the posted request packet reception buffer has overflowed.
20	NPOVF	0	RW1C	NPOVF Indicates that the non-posted request packet reception buffer has overflowed.
19 to 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13	RCVCP LLK	0	RW1C	Receive Completion Lock Indicates that a completion lock (without data) has been received. This completion is returned when memory locking of the device supporting memory lock has failed.
12	UNEXP CPL	0	RW1C	Unexpected Completion Indicates that an unexpected completion has been received.

Bit	Bit Name	Initial Value	R/W	Description
11, 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9	RCVSZECPL	0	RW1C	Receive Size Error Completion Indicates that the size of the completion received is different from the requested size.
8	CPLTOUT	0	RW1C	CPL Timeout Indicates that a completion timeout has occurred.
7	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
6	RCVCRSCPL	0	RW1C	Receive Configuration Retry Status Completion Indicates that a completion with the configuration retry status has been received.
5	RCVCACPL	0	RW1C	Receive Completion Abort Status Completion Indicates that a completion with the completion abort status has been received.
4	RCVURCPL	0	RW1C	Receive Unsupported Request Status Completion Indicates that a completion with the unsupported request status has been received.
3, 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	SENDCACPL	0	RW1C	Send Completion Abort Status Completion Indicates that a completion with the completion abort status has been transmitted.
0	SENDURCPL	0	RW1C	Send Unsupported Request Status Completion Indicates that a completion with the unsupported request status has been transmitted.

### 39.2.17 Error Interrupt Enable Register (PCIEERRFER)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

This register determines whether to reflect the occurrence of errors to PCIEINTR.INT\_PCISERR.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	IB ERRE	—	—	—	—	—	—	POVFE	NPOVFE	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R	R	R	R	R	R	R/W	R/W	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	RCVCP LLKE	UNEXP CPLE	—	—	RCVSZ ECPLE	CPLTO UTE	—	RCVCR SCPLE	RCVCA CPLE	RCVUR CPLE	—	—	SENDC ACPLE	SENDU RCPLE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R	R	R/W	R/W	R	R/W	R/W	R/W	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28	IBERRE	0	R/W	IBERRE Enables generation of the INT_PCISERR interrupt upon occurrence of a transfer error on the internal bus.
27 to 22	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
21	POVFE	0	R/W	POVFE Enables generation of the INT_PCISERR interrupt upon overflow of a posted request packet reception buffer.
20	NPOVFE	0	R/W	NPOVFE Enables generation of the INT_PCISERR interrupt upon overflow of a non-posted request packet reception buffer.
19 to 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13	RCVCP LLKE	0	R/W	Receive Completion Lock Enables generation of the INT_PCISERR interrupt upon reception of the completion lock (without data).
12	UNEXP CPLE	0	R/W	Unexpected Completion Enabled Enables generation of the INT_PCISERR interrupt upon reception of the unexpected completion.
11, 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9	RCVSZ ECPLE	0	R/W	Receive Size Error Completion Enabled Enables generation of the INT_PCISERR interrupt upon reception of the completion whose size is different from the requested size.

Bit	Bit Name	Initial Value	R/W	Description
8	CPLTOUTE	0	R/W	Completion Timeout Interrupt Enable Enables generation of the INT_PCISERR interrupt upon detection of a completion timeout.
7	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
6	RCVCRSCPLE	0	R/W	Configuration Retry Status Completion Receive Interrupt Enable Enables generation of the INT_PCISERR interrupt upon reception of a completion with the configuration retry status.
5	RCVCACPLE	0	R/W	Completion Abort Status Completion Receive Interrupt Enable Enables generation of the INT_PCISERR interrupt upon reception of a completion with the completion abort status.
4	RCVURCPLE	0	R/W	Unsupported Request Status Completion Receive Interrupt Enable Enables generation of the INT_PCISERR interrupt upon reception of a completion with the unsupported request status.
3, 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	SENDACPLE	0	R/W	Send Completion Abort Status Completion Interrupt Enable Enables generation of the INT_PCISERR interrupt upon transmission of a completion with the completion abort status.
0	SENDURCPLE	0	R/W	Send Unsupported Request Status Completion Interrupt Enable Enables generation of the INT_PCISERR interrupt upon transmission of a completion with the unsupported request status.

### 39.2.18 Error Factor Register 2 (PCIEERRFR2)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	DLLPE	RTO	RNR	BAD TLP	BAD DLLP	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	RW1C	RW1C	RW1C	RW1C	RW1C	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	RW1C	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31, 30	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
29	DLLPE	0	RW1C	Data Link Layer Protocol Error Indicates that a data link layer protocol error has occurred.
28	RTO	0	RW1C	Replay Timeout Indicates that a replay timeout has occurred.
27	RNR	0	RW1C	Replay Number Rollover Indicates that a replay number rollover has occurred.
26	BADTLP	0	RW1C	Bad TLP Indicates that a Bad TLP has been detected.
25	BADDLLP	0	RW1C	Bad DLLP Indicates that a Bad DLLP has been detected.
24 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15	RE	0	RW1C	Receiver Error Indicates that a receiver error has been detected.
14 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

### 39.2.19 Transfer Interrupt Enable Register (PCIETIER)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	MSIEC E	—	—	—	—	—	—	—	—	—	—	—	DLLAC TCE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	INTXD CE	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28	MSIECE	0	R/W	MSI Enable Change Enable Enables generation of the INT_PCISC interrupt upon change of MSCAP0[16].MSIE.
27 to 17	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
16	DLLACTCE	0	R/W	DLLACT Change Enable Enables generation of the INT_PCISC interrupt upon change of DLLACT.
15 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12	INTXDCE	0	R/W	INTx Disable Change Enable Enables generation of the INT_PCISC interrupt upon change of PCICONF1[10].INTDIS.
11 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.



**39.2.20 Power Management State Status Register (PCIEPMSR)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	PSTC	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	RW1C	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	PST	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 25	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
24	PSTC	0	RW1C	Power State Change Indicates that PST has changed. This bit is valid only in Endpoint mode.
23 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	PST	0	R	Power State Indicates the power state. 0: D0 1: Non-D0 Do not issue a request in the non-D0 state. This bit is valid only in Endpoint mode.
7 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

### 39.2.21 Power Management State Interrupt Enable Register (PCIEPMSCIER)

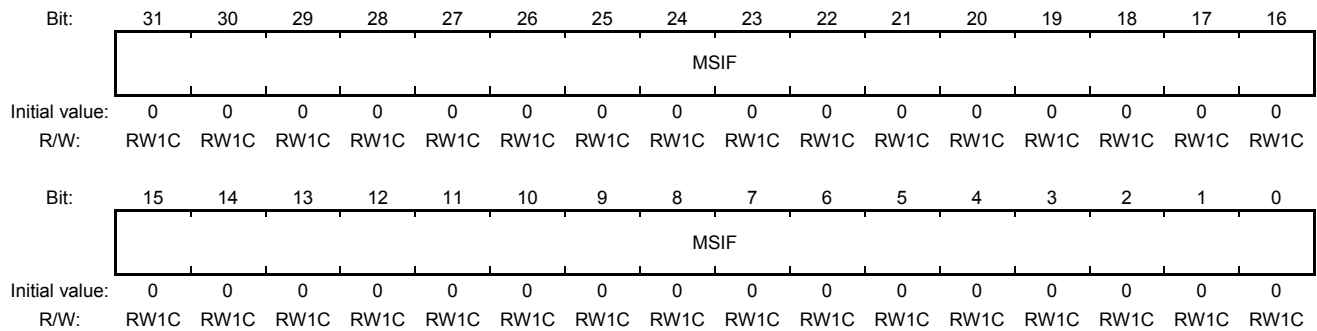
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	PSTCE	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 25	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
24	PSTCE	0	R/W	Power State Change Enable Enables generation of the INT_PCISC interrupt upon change of PST. This bit is valid only in Endpoint mode.
23 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

### 39.2.22 MSIF Register (PCIEMSIFR)

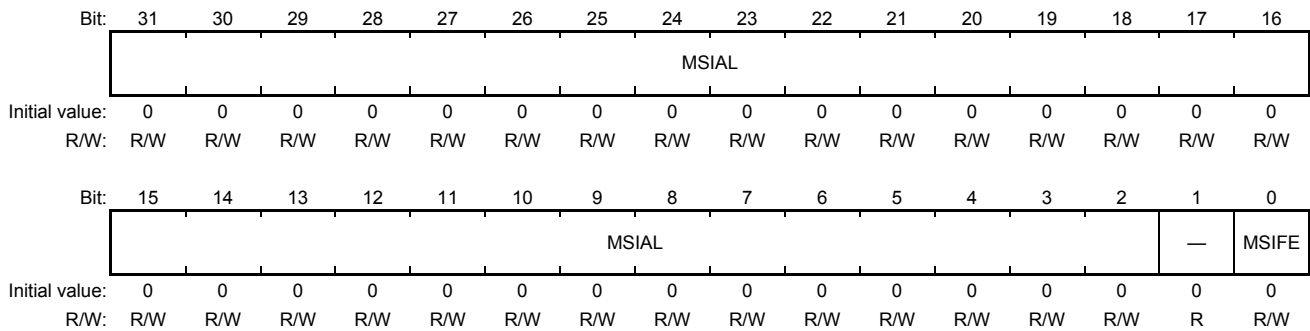
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	MSIF	All 0	RW1C	<p>MSIF</p> <p>Indicates that an MSI interrupt has occurred.</p> <p>This field is valid only when PCIEMSIALR.MSIFE = 1 in Root Port mode.</p> <p>A write from the internal bus is interpreted as interrupt cancellation thus clearing the bit to 0 to which 1 has been written. A read from the internal bus is processed as a normal read.</p> <p>A 1DW write to the address specified with PCIEMSAUR and PCIEMSIALR from the PCI Express side is interpreted as an MSI interrupt.</p> <p>This IP sets 1 to the bit determined by the sum of the values in bits [4:0] and [12:8] in the write data in order to convert the MSI message data into a flag. Set the function appropriately so that the interrupt should not be reflected to the same bit. A read from the address specified with PCIEMSAUR and PCIEMSIALR from the PCI Express side is processed as a normal read.</p>

**39.2.23 MSI Address Lower Register (PCIEMSIALR)**

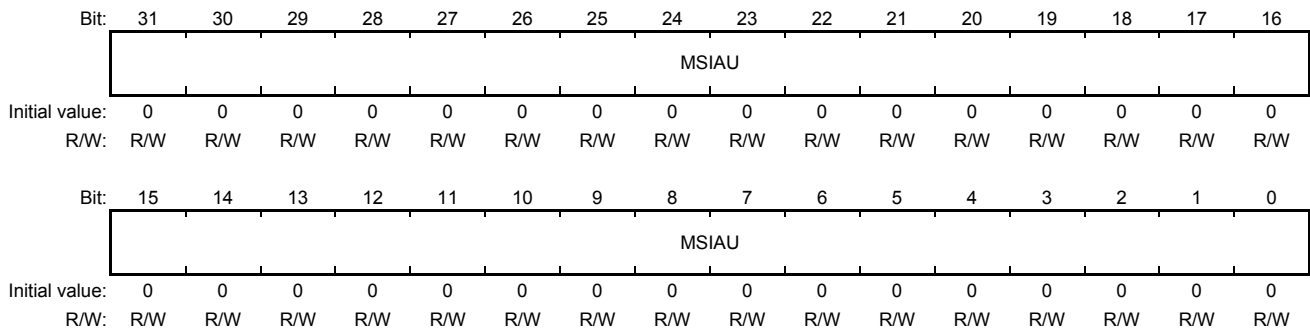
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—



Bit	Bit Name	Initial Value	R/W	Description
31 to 2	MSIAL	All 0	R/W	MSI Address Lower Specifies the lower address bits [31:2] of the memory write by MSI in the PCI space in Root Port mode. (Refer to section 39.3.3 (6), MSI Reception.) This field is invalid when PCIEMSIALR.MSIFE = 0.
1	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
0	MSIFE	0	R/W	MSIF Enable Enables address decoding of the MSI interrupt. Be sure to set this bit to 0 in Endpoint mode.

**39.2.24 MSI Address Upper Register (PCIEMSIUR)**

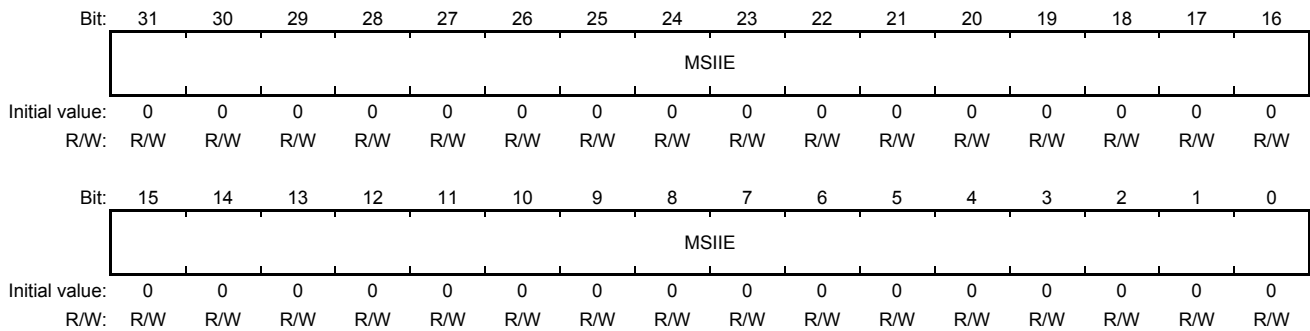
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	MSIAU	All 0	R/W	MSI Address Upper Specifies the upper address bits [63:32] of the memory write by MSI in the PCI space in Root Port mode. (Refer to section 39.3.3 (6), MSI Reception.) This field is invalid when PCIEMSIUR.MSIFE = 0.

**39.2.25 MSI Interrupt Enable Register (PCIEMSIER)**

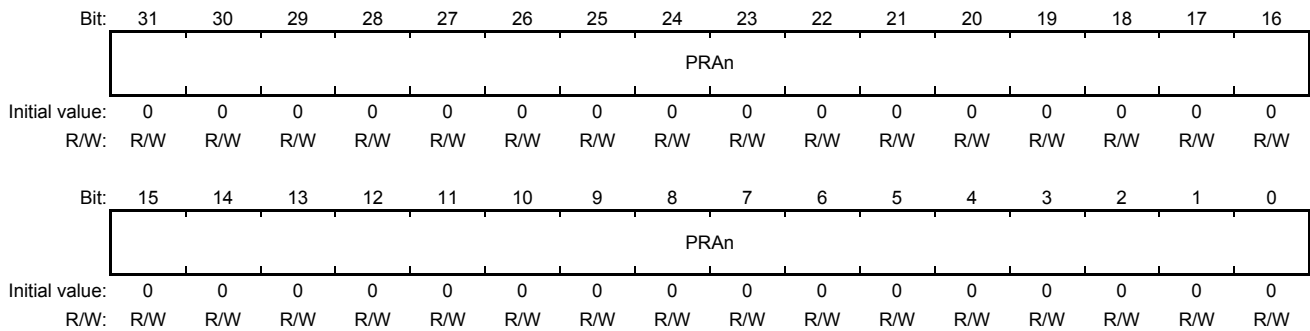
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	MSIIE	All 0	R/W	MSI Interrupt Enable Individually enables the interrupts by MSI in Root Port mode. This field is invalid when PCIEMSIALR.MSIFE = 0.

### 39.2.26 PCI Express Root Port Address Register 0 to 5 (PCIEPRAR0 to PCIEPRAR5)

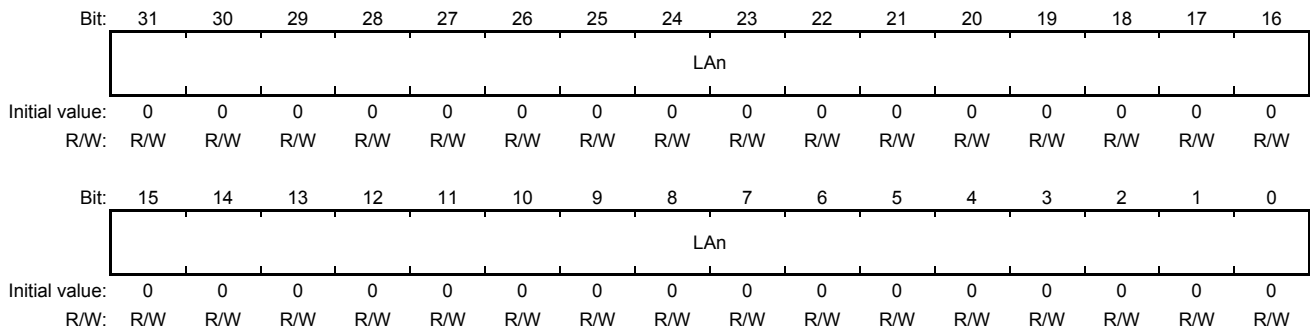
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	PRAn	All 0	R/W	<p>PCI Express Root Port Address n</p> <p>Specifies the PCI Express address for transferring a transaction from the PCI Express to the internal bus in Root Port mode.</p> <p>This field is invalid in Endpoint mode.</p> <p>Set the appropriate value corresponding to the local address registers and local address mask registers. Modify this field only when no access should occur to the corresponding PCI Express, for example, while a link is down and the master enable of the peer is off.</p>

**39.2.27 Local Address Register 0 to 5 (PCIELAR0 to PCIELAR5)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

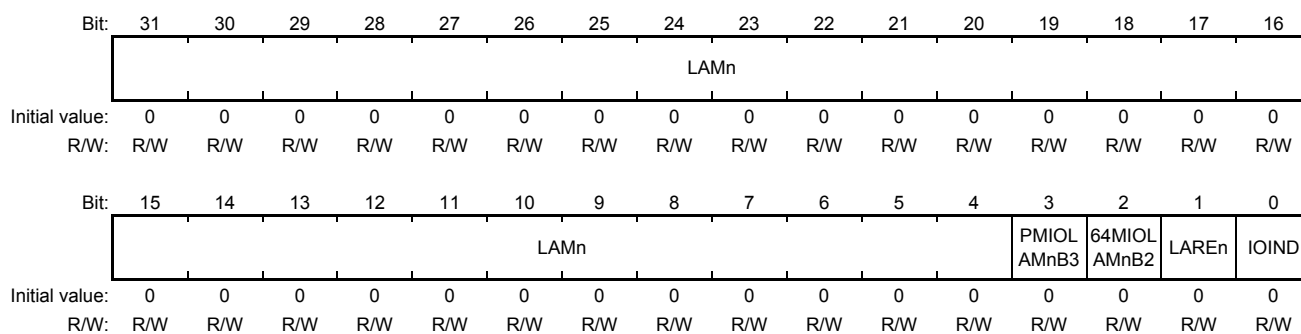


Bit	Bit Name	Initial Value	R/W	Description
31 to 0	LAn	All 0	R/W	<p>Local Address n</p> <p>Indicates the local (internal bus) address for transferring a transaction from the PCI Express to the internal bus.</p> <p>When the addresses in the space allocated by the BARn of the PCI Express are translated into the internal bus space addresses, this field is used as the upper address bits. The lower address bits of the PCI Express packets are used as the lower address bits. The boundary between upper and lower bits is determined by PCIELAMR0 to PCIELAMR5.</p> <p>Writing to this field is prohibited while PCIETCTLR.CFINIT is 1.</p> <p>When a 64-bit access is enabled with PCIELAMR0 to PCIELAMR5, write 0 to all the bits in PCIELARn + 1.</p> <p>The write value for bits 1 and 0 should always be 0.</p>



### 39.2.28 Local Address Mask Register 0 to 5 (PCIELAMR0 to PCIELAMR5)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—



Bit	Bit Name	Initial Value	R/W	Description
31 to 4	LAMn	All 0	R/W	<p>Local Address Mask n</p> <p>Masks the local (internal bus) addresses when transactions are transferred from PCI Express to the internal bus.</p> <p>When the addresses in the space allocated by the BARn of the PCI Express are translated into the internal bus space addresses, the PCIELARn.LAn value is used as the upper bits while the address in the PCI Express packet header is used as the lower bits. This field determines the boundary between upper and lower bits. Therefore, this field also determines the size of the space to be allocated to the PCI Express space.</p> <p>B'0000_0000_0000_0000_0000_0000_0000: 4, 8, or 16 bytes            B'0000_0000_0000_0000_0000_0000_0001: 32 bytes            B'0000_0000_0000_0000_0000_0000_0011: 64 bytes            B'0000_0000_0000_0000_0000_0000_0111: 128 bytes            B'0000_0000_0000_0000_0000_0000_1111: 256 bytes            (Omitted)            B'0000_1111_1111_1111_1111_1111_1111: 256 Mbytes            B'0001_1111_1111_1111_1111_1111_1111: 512 Mbytes            B'0011_1111_1111_1111_1111_1111_1111: 1 Gbyte            B'0111_1111_1111_1111_1111_1111_1111: 2 Gbytes            B'1111_1111_1111_1111_1111_1111_1111: 4 Gbytes</p> <p>This field must not be set to any value other than those given above.</p> <p>Writing to this field is prohibited when PCIETCTLR.CFINIT is 1.</p> <p>When using the space as a memory space, set a size of 128 bytes or more with BAR.</p> <p>When setting a 4-Gbyte space, set 64M_IOLAMB2 to 1.</p> <p>When 64-bit addresses are used with PCIELAMRn, PCIELAMRn + 1 is used as the upper address of PCIELAMRn, and so PCIELAMRn cannot be used as an independent space. In this case, set this field as follows.</p> <p>B'0000_0000_0000_0000_0000_0000_0000: 4 Gbytes or less</p>

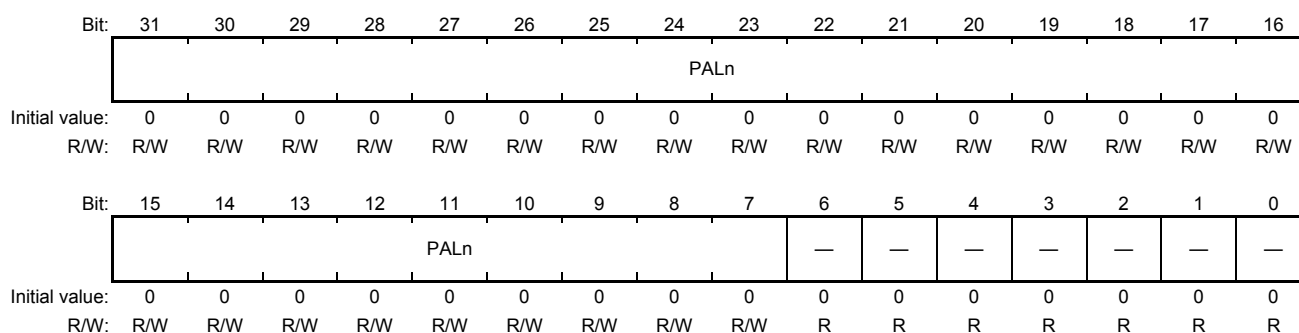
Bit	Bit Name	Initial Value	R/W	Description
3	PMIOLAMnB3	0	R/W	<p>Prefetchable Memory or IO Local Address Mask n Bit 3</p> <ul style="list-style-type: none"> <li>When IO indicator is 0: <ul style="list-style-type: none"> <li>Specifies memory space prefetch.</li> <li>0: A non-prefetchable memory space is allocated.</li> <li>1: A prefetchable memory space is allocated.</li> </ul> </li> <li>When IO indicator is 1: <ul style="list-style-type: none"> <li>Masks bit 3 as an extension of local address mask n.</li> <li>0: A space of 4 or 8 bytes is allocated.</li> <li>1: A space of 16 bytes or more is allocated.</li> </ul> </li> </ul> <p>Writing to this field is prohibited when PCIETCTLR.CFINIT is 1.</p> <p>When 64-bit addresses are used with PCIELAMRn, PCIELAMRn + 1 is used as the upper address of PCIELAMRn, and so PCIELAMRn cannot be used as an independent space. Set all the bits to 0.</p>
2	64MIOLAMnB2	0	R/W	<p>64-bit Access Space Memory or IO Local Address Mask n Bit 2</p> <ul style="list-style-type: none"> <li>When IO indicator is 0: <ul style="list-style-type: none"> <li>Specifies the width of the addresses to define BAR in the memory space.</li> <li>0: Indicates that 32-bit addresses are used with PCIELAMRn.</li> <li>1: Indicates that 64-bit addresses are used with PCIELAMRn.</li> </ul> </li> <li>When IO indicator is 1: <ul style="list-style-type: none"> <li>Masks bit 2 as an extension of local address mask n.</li> <li>0: A space of 4 bytes is allocated.</li> <li>1: A space of 8 bytes or more is allocated.</li> </ul> </li> </ul> <p>Writing to this field is prohibited when PCIETCTLR.CFINIT is 1.</p> <p>When 64-bit addresses are used with PCIELAMRn, PCIELAMRn + 1 is used as the upper address of PCIELAMRn, and so PCIELAMRn cannot be used as an independent space. Set all the bits to 0.</p>
1	LAREn	0	R/W	<p>Local Address Enable</p> <p>Enables local address.</p> <p>Setting this field to 1 enables transaction transfer in the area specified by PCIELARn and PCIELAMRn. Set this field to 1 to enable address translation by LAn and LAMn.</p> <p>Writing to this field is prohibited when PCIETCTLR.CFINIT is 1.</p> <p>When 64-bit addresses are used with PCIELAMRn, PCIELAMRn + 1 is used as the upper address of PCIELAMRn, and so PCIELAMRn cannot be used as an independent space. Set all the bits to 0.</p>

Bit	Bit Name	Initial Value	R/W	Description
0	IOIND	0	R/W	IO Indicator Specifies the type of space on the PCI Express side allocated for transaction transfer from the PCI Express to the internal bus. 0: Memory space 1: IO space Writing to this field is prohibited when PCIETCTLR.CFINIT is 1. When 64-bit addresses are used with PCIELAMRn, PCIELAMRn + 1 is used as the upper address of PCIELAMRn, and so PCIELAMRn cannot be used as an independent space. Set all the bits to 0.

Note: Setting the memory space type of 1 Mbyte or less (defined in the PCI Express standard 2.2 and the earlier versions) is not supported.

### 39.2.29 PCIEC Address Lower Register 0 to 3 (PCIEPALR0 to PCIEPALR3)

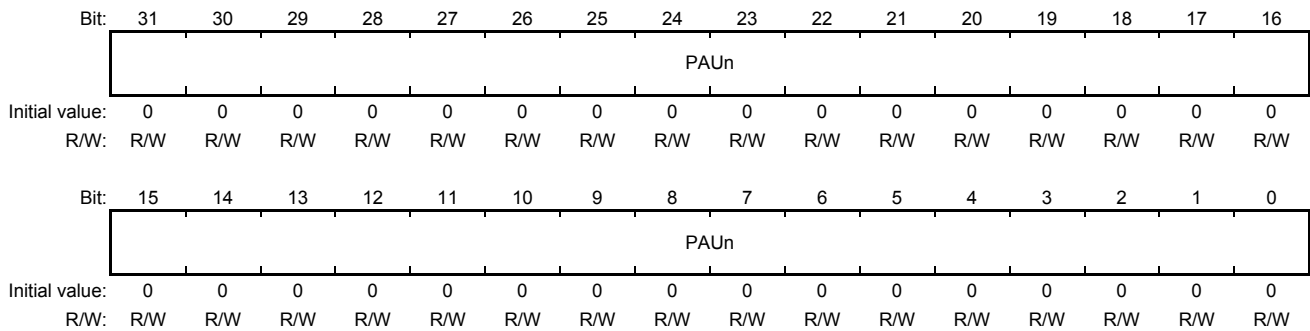
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—



Bit	Bit Name	Initial Value	R/W	Description
31 to 7	PALn	All 0	R/W	PCI Express Address Lower Sets the PCI Express address (lower) for PIO transfer from the internal bus to the PCI Express.
6 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

**39.2.30 PCIEC Address Upper Register 0 to 3 (PCIEPAUR0 to PCIEPAUR3)**

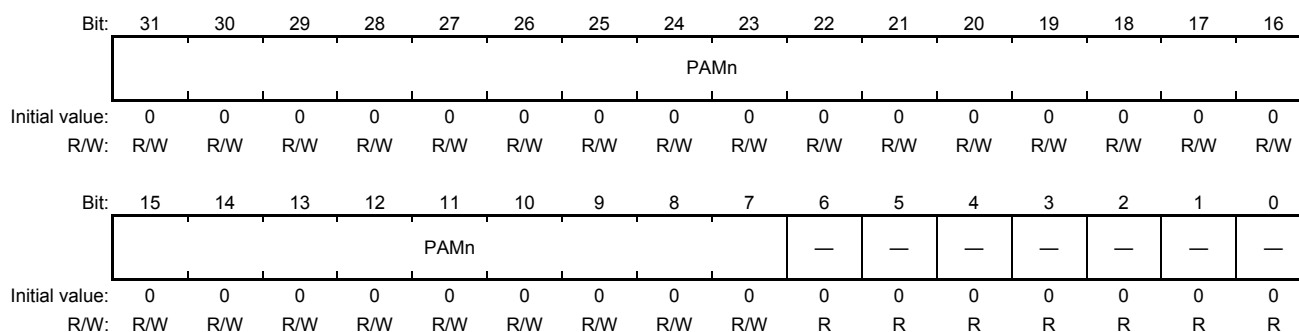
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	PAUn	All 0	R/W	PCI Express Address Upper Sets the PCI Express address (upper) for PIO transfer from the internal bus to the PCI Express.

### 39.2.31 PCIEC Address Mask Register 0 to 3 (PCIEPAMR0 to PCIEPAMR3)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—



Bit	Bit Name	Initial Value	R/W	Description
31 to 7	PAMn	All 0	R/W	<p>PCI Express Address Mask</p> <p>Masks the PCI Express addresses.</p> <p>When the packet accessing the internal bus space n is converted to the PCI Express packet, PAUn and PALn are used as the upper bits while the address on the internal bus packet is used as the lower bits. Here, PAMn determines the boundary between them. That is, the packet address addr[31:0] on the PCI Express is generated as follows.</p> <p>Addr[31:7] = PALn[31:7] when the corresponding bit in PAMn[31:7] is 0, and Addr[31:7] = internal bus - addr[31:7] when the corresponding bit in PAMn[31:7] is 1.</p> <p>Addr[6:0] = internal bus - addr[6:0]</p> <p>According to the setting of this field, the size of the space to which the PCI Express side transactions is transferred is determined as follows.</p> <p>B'0000 0000 0000 0000 0000 0000_0: 128 bytes            B'0000 0000 0000 0000 0000 0000_1: 256 bytes            B'0000 0000 0000 0000 0000 0001_1: 512 bytes            B'0000 0000 0000 0000 0000 0011_1: 1 Kbyte            B'0000 0000 0000 0000 0000 0111_1: 2 Kbytes</p> <p style="text-align: center;">(Omitted)</p> <p>B'0000 0111 1111 1111 1111 1111_1: 128 Mbytes            B'0000 1111 1111 1111 1111 1111_1: 256 Mbytes            B'0001 1111 1111 1111 1111 1111_1: 512 Mbytes            B'0011 1111 1111 1111 1111 1111_1: 1 Gbyte            B'0111 1111 1111 1111 1111 1111_1: 2 Gbytes</p> <p>The area size exceeding the size defined in the address map must not be set.</p> <p>Any value other than those given above must not be set.</p>
6 to 0	—	All 0	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>

### 39.2.32 PCIEC Conversion Control Register 0 to 3 (PCIEPTCLR0 to PCIEPTCLR3)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PARE	—	—	—	—	—	—	—	—	TCn		—	—	—	—	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	LOCKn	—	—	—	SPCn	—	—	—	ZLR	—	—	ATTRn	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R	R	R	R/W	R	R	R	R/W	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	PARE	0	R	PAR Enable Indicates that the PCI Express address upper and lower registers are enabled.
30 to 23	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
22 to 20	TCn	All 0	R/W	Traffic Class Specifies the traffic class (TC) of the PCI Express packet to be transferred.
19 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12	LOCKn	0	R/W	LOCK Sets the lock of PCI Express packets to be transmitted. When this bit is set, locked transactions are transmitted. In Endpoint mode, this bit must not be set. Before making access requiring exclusive processing, confirm that the locked transaction has not caused an error.
11 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	SPCn	0	R/W	SPC Specifies a transfer destination space. 0: Memory 1: IO (A request cannot be issued to the IO space in Endpoint mode.) When issuing a request to the IO space, be sure to separate the accesses at 1DW boundaries.
7 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
4	ZLR	0	R/W	<p>ZLR</p> <p>Sets the zero-length read.</p> <p>0: A read access to this space is output as a read access as is.</p> <p>1: A 1DW read access to this space is output after converted to a zero-length read.</p> <p>Do not make any read access other than 1DW read access when this bit is set.</p> <p>The read value depends on the dummy data used by PCI Express for zero-length read.</p> <p>According to the standard, the value is undefined.</p> <p>Setting this bit has no effect for write access.</p>
3, 2	—	All 0	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>
1, 0	ATTRn	All 0	R/W	<p>ATTR</p> <p>Specifies the attribute of the PCI Express packet to be transferred.</p> <p>ATTR[0]: No snoop</p> <p>ATTR[1]: Relaxed ordering</p> <p>Setting ATTR[0] (no snoop bit) to 1 disables snooping in the transfer destination.</p> <p>Setting ATTR[1] (relaxed ordering bit) to 1 relaxes ordering in the transfer destination.</p>

**39.2.33 PCIEC DMAC DMA Operation Register (PCIEDMAOR)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

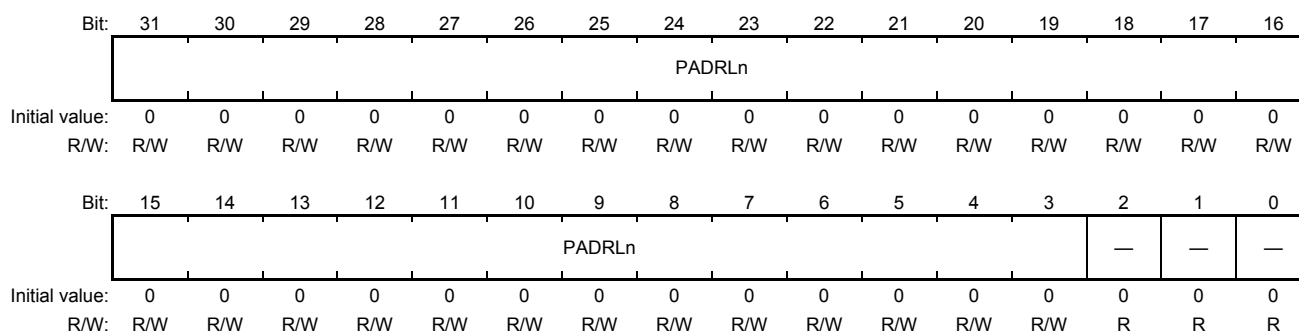
Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DMAE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DMAACT
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ABT
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	DMAE	0	R/W	DMA Enable Enables DMA function. Set this bit to 1 to use DMA function. This bit must not be cleared to 0 during DMA transfer (PCIEDMCHCR0-7.CHE = 1).
30 to 17	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
16	DMAACT	0	R	DMA Active Indicates whether there is a currently operating DMA channel. 0: No DMA channel is currently operating. 1: At least one DMA channel is currently operating.
15 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	ABT	0	R/W	Arbitration Specifies the method of arbitration among the channels. 0: CH0 > CH1 > CH2 > CH3 > CH4 > CH5 > CH6 > CH7 1: Round robin mode



**39.2.34 PCIEC DMAC PCIEC Address Lower Register 0 to 7 (PCIEDMPALR0 to PCIEDMPALR 7)**

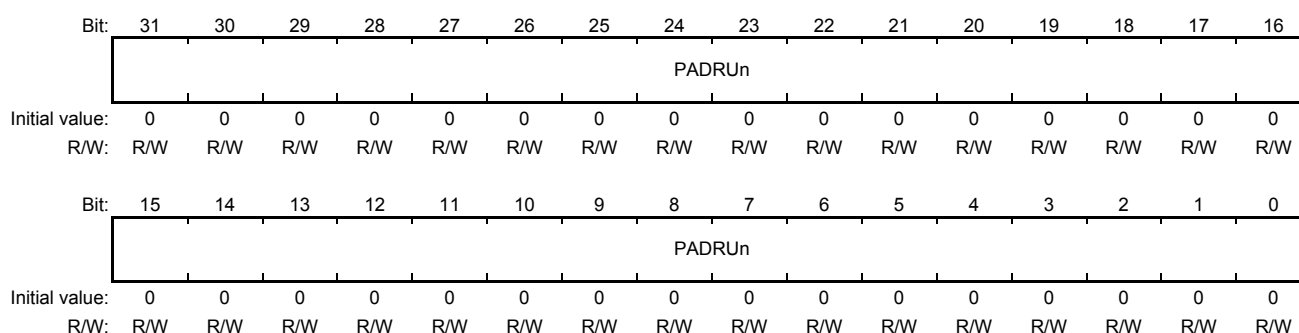
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—



Bit	Bit Name	Initial Value	R/W	Description
31 to 3	PADRLn	All 0	R/W	PCI Express Address Lower Sets the lower 32 bits of the PCI Express address for DMA transfer. Only an 8-byte boundary address can be set.
2 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

**39.2.35 PCIEC DMAC PCIEC Address Upper Register 0 to 7 (PCIEDMPAUR0 to PCIEDMPAUR7)**

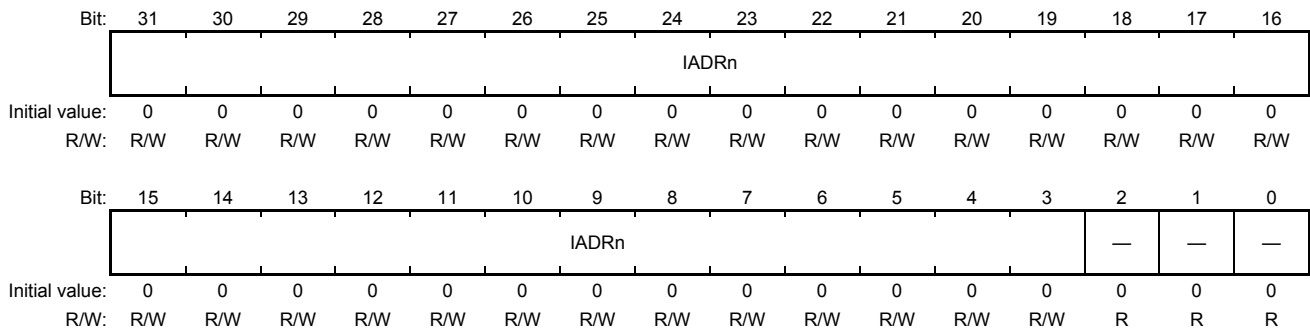
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	PADRU <sub>n</sub>	All 0	R/W	PCI Express Address Upper Sets the upper 32 bits of the PCI Express address for DMA transfer.

### 39.2.36 PCIEC DMAC Internal Bus Address Register 0 to 7 (PCIEDMIAR0 to PCIEDMIAR7)

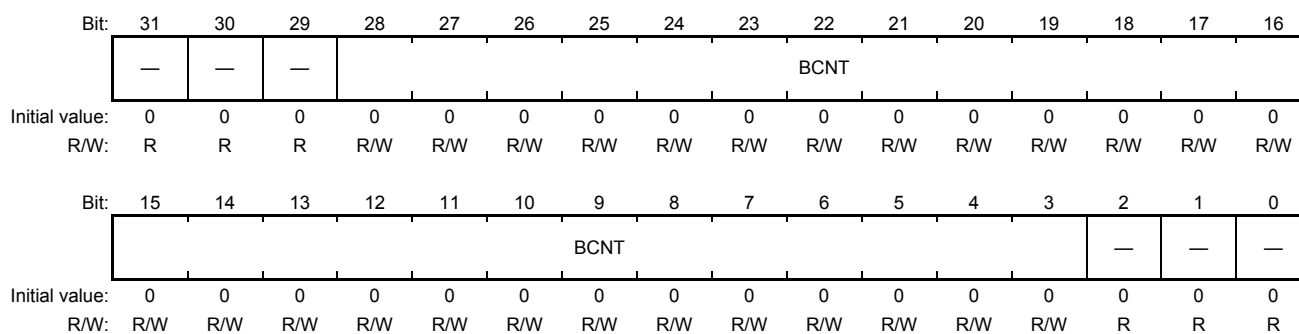
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—



Bit	Bit Name	Initial Value	R/W	Description
31 to 3	IADRn	All 0	R/W	Internal Address Lower Sets the internal bus address for DMA transfer. Only an 8-byte boundary address can be set. Internal bus addresses for registers or PIO transfer must not be set.
2 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

### 39.2.37 PCIEC DMAC Byte Count Register 0 to 7 (PCIEDMBCNTR0 to PCIEDMBCNTR7)

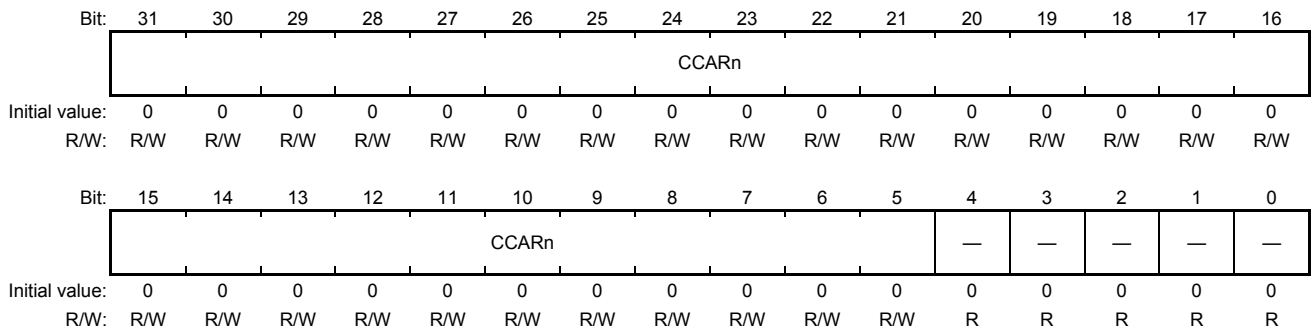
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—



Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28 to 3	BCNT	All 0	R/W	Byte Count Specifies the transfer byte count. Only a multiple of 8 can be specified. In this field, set one-eighth of the number to be specified (omit the lower three bits from the number). When 0 is set, 2 <sup>29</sup> bytes are transferred. Note: If the transfer direction is changed after a transfer, the byte count read value will be undefined until the next transfer byte count is set (written). Be sure to write the byte count after initialization or completion of the previous transfer and before the start of the next transfer. The value before modification cannot be referenced or used.
2 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

**39.2.38 PCIEC DMAC Command Chain Address Register 0 to 7 (PCIEDMCCAR0 to PCIEDMCCAR7)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—



Bit	Bit Name	Initial Value	R/W	Description
31 to 5	CCARn	All 0	R/W	Command Chain Address Specifies a command chain address for DMA transfer. Only a 32-byte boundary address can be set.
4 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

### 39.2.39 PCIEC DMAC Channel Control Register 0 to 7 (PCIEDMCHCR0 to PCIEDMCHCR7)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CHEn	DIRn	CCEn	CHTn	—	—	—	—	—	—	ATTRn	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R/W	R/W	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	TC	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31	CHEn	0	R/W	<p>Channel Enable</p> <p>Enables a DMA channel.</p> <p>Setting this bit to 1 starts DMA transfer on the corresponding channel. Note that, DMA transfer is not performed while the bit that indicates a transfer end (PCIEDMCHSRn.TE), a transfer error (PCIEDMCHSRn.PEE/IBE), or completion of DMA transfer suspension processing (PCIEDMCHSRn.CHTC) is 1.</p> <p>This bit must not be cleared during DMA transfer.</p> <p>This bit is not cleared to 0 by a transfer end or suspension.</p> <p>0: Disables data transfer.</p> <p>1: Enables data transfer.</p>
30	DIRn	0	R/W	<p>Direction</p> <p>Specifies the data transfer direction.</p> <p>0: PCI Express → internal bus</p> <p>1: Internal bus → PCI Express</p>
29	CCEn	0	R/W	<p>Command Chain Enable</p> <p>Enables a command chain.</p> <p>If data transfer is requested with this bit set to 1, the data is transferred by reading a command from an address set in PCIEDMCCARn.</p> <p>0: Disables a command chain.</p> <p>1: Enables a command chain.</p>
28	CHTn	0	R/W	<p>Channel Terminate</p> <p>Forcibly suspends DMA transfer in normal transfer.</p> <p>Setting this bit to 1 during DMA transfer suspends DMA transfer forcibly. Completion of DMA transfer suspension processing can be checked with PCIEDMCHSRn.CHTC. After transfer suspension, initialize the registers for the channel suspended.</p> <p>When setting this bit to 1, set other bits to the same value.</p> <p>This bit can be set to 1 only when a command chain is disabled (PCIEDMCHCRn.CCE = 0).</p> <p>When PCIEDMCHCRn.CCE is 1, this bit must be cleared to 0.</p> <p>This bit is always read as 0.</p>

Bit	Bit Name	Initial Value	R/W	Description
27 to 22	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
21, 20	ATTRn	All 0	R/W	ATTR Specifies the attribute of the PCI Express packet to be transferred. ATTR[0]: No snoop ATTR[1]: Relaxed ordering
19 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11 to 9	TC	All 0	R/W	TC Specifies the traffic class (TC) of the PCI Express packet to be transferred.
8 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

### 39.2.40 PCIEC DMAC Channel Status Register 0 to 7 (PCIEDMCHSR0 to PCIEDMCHSR7)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	CHTCE <sub>n</sub>	PEEE <sub>n</sub>	—	IBEE <sub>n</sub>	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R/W	R	R/W	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	CHTC <sub>n</sub>	PEE <sub>n</sub>	—	IBE <sub>n</sub>	—	—	—	—	—	IEn	—	—	TE <sub>n</sub>
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	RW1C	RW1C	R	RW1C	R	R	R	R	R	R/W	R	R	RW1C

Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28	CHTCE <sub>n</sub>	0	R/W	Channel Terminate Complete Interrupt Enable Enables an interrupt caused by completion of forced suspension. 0: Disables generation of an interrupt. 1: Enables generation of an interrupt.
27	PEEE <sub>n</sub>	0	R/W	PCIE Error Interrupt Enable Enables an interrupt caused by a transfer error on the PCI Express side. 0: Disables generation of an interrupt. 1: Enables generation of an interrupt.
26	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
25	IBEE <sub>n</sub>	0	R/W	Internal Bus Error Interrupt Enable Enables an interrupt caused by a transfer error on the internal bus side. 0: Disables generation of an interrupt. 1: Enables generation of an interrupt.
24 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12	CHTC <sub>n</sub>	0	RW1C	Channel Terminate Complete Indicates that the forced suspension processing started by setting PCIEDMCHCR <sub>n</sub> .CHT or PCIEDMCHC2R <sub>n</sub> .CHT has been completed. With this bit set, DMA transfer is not performed by setting PCIEDMCHCR <sub>n</sub> .CHE to 1.

Bit	Bit Name	Initial Value	R/W	Description
11	PEEn	0	RW1C	<p>PCIE Error</p> <p>Indicates that a transfer error has occurred on the PCI Express side.</p> <p>This error is caused in the following cases:</p> <ul style="list-style-type: none"> <li>• PCIEDMCHCRn.CHE is set to 1 while PCIEDMAOR.DMAE is 0.</li> <li>• DMA transfer is started while a link is not established, or DL_Down is caused during DMA transfer.</li> <li>• DMA transfer is started in the Non-D0 state.</li> <li>• DMA transfer is started with TC being set that is not mapped to VC0.</li> <li>• DMA transfer is started with PCICONF1[2].BME = 0 in Endpoint mode, or the bit is deasserted during DMA transfer.</li> <li>• DMA transfer is started with an attribute being set that is not enabled in the configuration registers.</li> <li>• A completion other than SC is received when PCI Express → internal bus.</li> <li>• A completion timeout occurs when PCI Express → internal bus.</li> <li>• A malformed completion is received when PCI Express → internal bus.</li> <li>• A poisoned completion is received when PCI Express → internal bus.</li> <li>• With this bit set, DMA transfer is not performed by setting PCIEDMCHCRn.CHE to 1.</li> </ul>
10	—	0	R	<p>Reserved</p> <p>This bit is always read as 0. The write value should always be 0.</p>
9	IBEn	0	RW1C	<p>Internal Bus Error</p> <p>Indicates that a transfer error has occurred on the internal bus side.</p> <p>With this bit set, DMA transfer is not performed by setting PCIEDMCHCRn.CHE to 1.</p>
8 to 4	—	All 0	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>
3	IEn	0	R/W	<p>Interrupt Enable</p> <p>Enables an interrupt request.</p> <p>When this bit is 1, setting TE bit requests an interrupt.</p> <p>0: Disables an interrupt request.</p> <p>1: Enables an interrupt request.</p>
2, 1	—	All 0	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>



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Bit	Bit Name	Initial Value	R/W	Description
0	TEn	0	RW1C	<p>Transfer End</p> <p>Indicates a transfer end.</p> <p>This bit is set to 1 when data transfer ends with the value in PCIEDMBCNTR0- PCIEDMBCNTR7 cleared to 0. This bit is not set to 1 when a transfer end is caused by a transfer error or data transfer is forcibly terminated by setting the PCIEDMCHCRn.CHT bit.</p> <p>With this bit set, DMA transfer is not performed by setting PCIEDMCHCRn.CHE to 1.</p> <p>0: Indicates that data transfer is being performed or has been suspended.</p> <p>1: Indicates that data transfer has ended (with PCIEDMBCNTRn cleared to 0).</p>

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### 39.2.41 PCIEC DMAC Channel Control 2 Register 0 to 7 (PCIEDMCHC2R0 to PCIEDMCHC2R7)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	CHTn	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

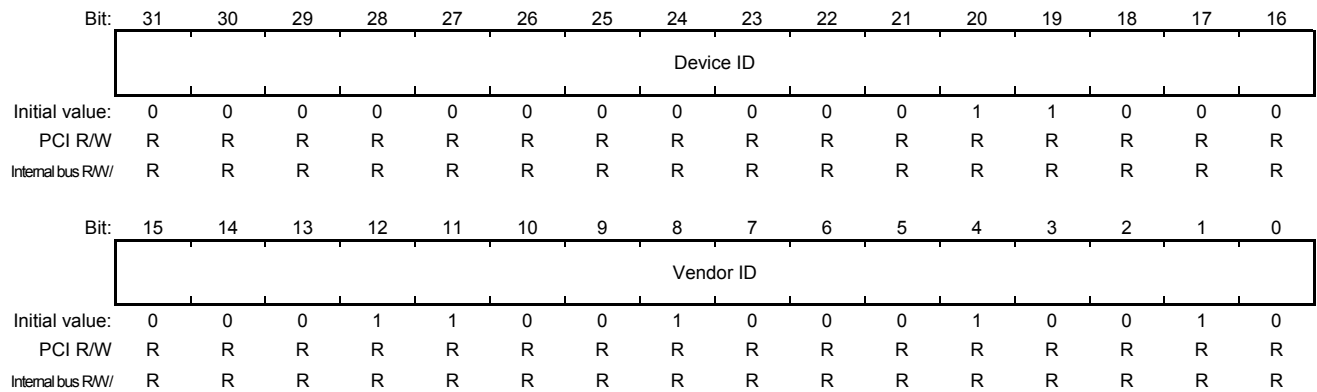
Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28	CHTn	0	R/W	Command Chain Channel Terminate Forcibly suspends DMA transfer when command chain is used. Setting this bit to 1 during DMA transfer suspends DMA transfer forcibly. Completion of DMA transfer suspension processing can be checked with PCIEDMCHSRn.CHTC. After transfer suspension, initialize the registers for the channel suspended. This bit can be set to 1 only when a command chain is enabled (PCIEDMCHCRn.CCE = 1). When PCIEDMCHCRn.CCE is 0, this bit must be cleared to 0. This bit is always read as 0.
27 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

**39.2.42 PCI Configuration Register 0 (PCICONF0)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	—	—	—

**[RZ/G1H]**

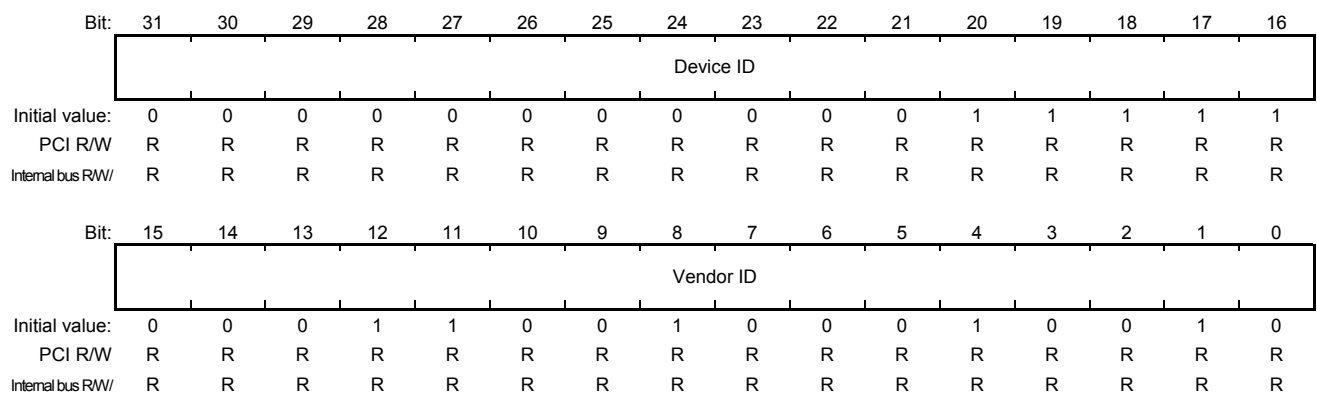
**Common to Header TYPE00/01**



Bit	Bit Name	Initial Value	PCI R/W	Internal Bus R/W	Description
31 to 16	Device ID	H'0018	R	R	Device ID Indicates the device ID. Reflects a value set in the IDSETR0.Device ID set. Indicates the device ID assigned to the PCI device vendor.
15 to 0	Vendor ID	H'1912	R	R	Vendor ID Indicates the vendor ID. Reflects a value set in the IDSETR0.Vendor ID set. Indicates the PCI device vendor ID.

**[RZ/G1M]**

**Common to Header TYPE00/01**



Bit	Bit Name	Initial Value	PCI R/W	Internal Bus R/W	Description
31 to 16	Device ID	H'001F	R	R	Device ID Indicates the device ID. Reflects a value set in the IDSETR0.Device ID set. Indicates the device ID assigned to the PCI device vendor.
15 to 0	Vendor ID	H'1912	R	R	Vendor ID Indicates the vendor ID. Reflects a value set in the IDSETR0.Vendor ID set. Indicates the PCI device vendor ID.

**[RZ/G1N]****Common to Header TYPE00/01**

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Device ID																
Initial value:	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1
PCI R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Internal bus R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Vendor ID																
Initial value:	0	0	0	1	1	0	0	1	0	0	0	1	0	0	1	0
PCI R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Internal bus R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	PCI R/W	Internal Bus R/W	Description
31 to 16	Device ID	H'0023	R	R	Device ID Indicates the device ID. Reflects a value set in the IDSETR0.Device ID set. Indicates the device ID assigned to the PCI device vendor.
15 to 0	Vendor ID	H'1912	R	R	Vendor ID Indicates the vendor ID. Reflects a value set in the IDSETR0.Vendor ID set. Indicates the PCI device vendor ID.

### 39.2.43 PCI Configuration Register 1 (PCICONF1)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

#### Common to Header TYPE00/01

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DPE	SSE	RMA	RTA	STA	DEVSEL Timing	MDPE	FBBTC AP	—	66MCA P	CAPL	INTST	—	—	—	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
PCI R/W	RW1C	RW1C	RW1C	RW1C	RW1C	R	R	RW1C	R	R	R	R	R	R	R	R
Internal bus R/W	RW1C	RW1C	RW1C	RW1C	RW1C	R	R	RW1C	R	R	R	R/W	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	INTDIS	FBTTE	SERRE	IDSS/W CC	PERS	VGAPS	MWIE	SC	BME	MSE	IOSE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PCI R/W	R	R	R	R	R	R/W	R	R/W	R	R/W	R	R	R	R/W	R/W	R/W
Internal bus R/W	R	R	R	R	R	R/W	R	R/W	R	R/W	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	PCI R/W	Internal Bus R/W	Description
31	DPE	0	RW1C	RW1C	<p>Detected Parity Error</p> <p>Indicates that a parity error has been detected on the primary bus side.</p> <ul style="list-style-type: none"> <li>Root Port: This bit is set to 1 when a poisoned TLP is transmitted.</li> <li>Endpoint: This bit is set to 1 when a poisoned TLP is received.</li> </ul>
30	SSE	0	RW1C	RW1C	<p>Signaled System Error</p> <p>Indicates that a system error has been detected.</p> <ul style="list-style-type: none"> <li>Root Port: This bit is set to 1 if a fatal/non-fatal error is detected while PCICONF1[8].SERRE = 1 or if a ERR_FATAL/ERR_NONFATAL message is received while PCICONF1[8].SERRE = 1 and PCICONF15[17].SERRE = 1.</li> <li>Endpoint: This bit is set to 1 if a ERR_FATAL/ERR_NONFATAL message is transmitted while PCICONF1[8].SERRE = 1.</li> </ul>
29	RMA	0	RW1C	RW1C	<p>Received Master Abort</p> <p>Indicates that a master abort has been detected on the primary bus side.</p> <ul style="list-style-type: none"> <li>Root Port: This bit is set to 1 when a completion with the unsupported request completion status is transmitted.</li> <li>Endpoint: This bit is set to 1 when a completion with the unsupported request completion status is received.</li> </ul>

Bit	Bit Name	Initial Value	PCI R/W	Internal Bus R/W	Description
28	RTA	0	RW1C	RW1C	<p>Received Target Abort</p> <p>Indicates that a target abort has been detected on the primary bus side.</p> <ul style="list-style-type: none"> <li>• Root Port: This bit is set to 1 when a completion with the completer abort completion status is transmitted.</li> <li>• Endpoint: This bit is set to 1 when a completion with the completer abort completion status is received.</li> </ul>
27	STA	0	RW1C	RW1C	<p>Signaled Target Abort</p> <p>Indicates that a target abort has been transmitted to the primary bus side.</p> <ul style="list-style-type: none"> <li>• Root Port: This bit is set to 1 when a completion with the completer abort completion status is received.</li> <li>• Endpoint: This bit is set to 1 when a completion with the completer abort completion status is transmitted.</li> </ul>
26, 25	DEVSEL Timing	All 0	R	R	<p>DEVSEL Timing</p> <p>Fixed to 0. These bits are not used for PCI Express.</p>
24	MDPE	0	RW1C	RW1C	<p>Master Data Parity Error</p> <p>Indicates that a master data parity error has occurred on the primary bus side. This bit is set to 1 when any of the following conditions are satisfied while PCICONF1[6].PERS is 1.</p> <ul style="list-style-type: none"> <li>• Root Port: <ul style="list-style-type: none"> <li>1. A poisoned completion is transmitted.</li> <li>2. A poisoned request is received.</li> </ul> </li> <li>• Endpoint: <ul style="list-style-type: none"> <li>1. A poisoned completion is received.</li> <li>2. A poisoned request is transmitted.</li> </ul> </li> </ul>
23	FBBTCAP	0	R	R	<p>Fast Back to Back Transaction Capable</p> <p>Fixed to 0. This bit is not used for PCI Express.</p>
22	—	0	R	R	<p>Reserved</p> <p>This bit is always read as 0. The write value should always be 0.</p>
21	66MCAP	0	R	R	<p>66 MHz Capable</p> <p>This bit is always read as 0. The write value should always be 0.</p> <p>This bit is not used for PCI Express.</p>
20	CAPL	1	R	R/W	<p>Capabilities List</p> <p>Indicates that the extended capabilities list exists in the PCI compatible configuration space. This IP supports the extended capabilities list.</p> <p>This bit must not be set to a value other than 1.</p>

Bit	Bit Name	Initial Value	PCI R/W	Internal Bus R/W	Description
19	INTST	0	R	R	<p>Interrupt Status</p> <p>This bit is set to 1 when an interrupt is generated by INTx message transmission. It is cleared to 0 when a requested interrupt processing ends. When MSI is used by the device, this field is not set to 1.</p> <p>Fixed to 0 in Root Port mode.</p>
18 to 16	—	All 0	R	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>
15 to 11	—	All 0	R	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>
10	INTDIS	0	RW	RW	<p>Interrupt Disable</p> <p>Disables an INTx message transmission.</p> <p>Setting this bit to 1 disables an INTx message transmission.</p>
9	FBBTE	0	R	R	<p>Fast Back to Back Transaction Enable</p> <p>This bit is always read as 0. The write value should always be 0.</p> <p>This bit is not used for PCI Express.</p>
8	SERRE	0	R/W	R/W	<p>System Error Enable</p> <p>Enables an error message transmission when a non-fatal/fatal error is detected.</p> <p>Setting this bit to 1 enables an error message transmission.</p>
7	IDSS/WCC	0	R	R	<p>IDSel Stepping/Wait Cycle Control</p> <p>This bit is always read as 0. The write value should always be 0.</p> <p>This bit is not used for PCI Express.</p>
6	PERS	0	RW	RW	<p>Parity Error Response</p> <p>Enables setting the PCICONF1[24].MDPE bit.</p>
5	VGAPS	0	R	R	<p>VGA Plate Snoop</p> <p>This bit is always read as 0. The write value should always be 0.</p> <p>This bit is not used for PCI Express.</p>
4	MWIE	0	R	R	<p>Memory Write and Invalidate Enable</p> <p>This bit is always read as 0. The write value should always be 0.</p> <p>This bit is not used for PCI Express.</p>
3	SC	0	R	R	<p>Special Cycle</p> <p>This bit is always read as 0. The write value should always be 0.</p> <p>This bit is not used for PCI Express.</p>

Bit	Bit Name	Initial Value	PCI R/W	Internal Bus R/W	Description
2	BME	0	R/W	R/W	Bus Master Enable <ul style="list-style-type: none"> <li>• Root Port: Enables software to transfer the memory/IO request received from the endpoint device to the upper layer. When this bit is 0, the memory/IO request received is handled as an unsupported request.</li> <li>• Endpoint: When this bit is cleared to 0, transmission of a memory/IO request is disabled.</li> </ul>
1	MSE	0	R/W	R/W	Memory Space Enable Enables an access to memory space. When this bit is 0, the memory request to this device is handled as an unsupported request.
0	IOSE	0	R/W	R/W	IO Space Enable Enables an access to I/O space. When this bit is 0, the IO request to this device is handled as an unsupported request.



### 39.2.44 PCI Configuration Register 2 (PCICONF2)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

#### Common to Header TYPE00/01

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Class Code								Sub Class Code							
Initial value:	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
PCI R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Internal bus R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Prog IF								Revision ID							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PCI R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Internal bus R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	PCI R/W	Internal Bus R/W	Description
31 to 24	Class Code	H'FF	R	R	Class Code Indicates the class code. The value set in the IDSETR1.Class code set field is reflected on these bits.
23 to 16	Sub Class Code	All 0	R	R	Sub Class Code Indicates the sub-class code. The value set in the IDSETR1.Sub Class Code Set field is reflected on these bits.
15 to 8	Prog IF	All 0	R	R	Prog IF Indicates the prog IF. The value set in the IDSETR1.PROG IF Set field is reflected on these bits.
7 to 0	Revision ID	All 0	R	R	Revision ID Indicates the revision ID. The value set in the IDSETR1.Rev ID Set field is reflected on these bits.

### 39.2.45 PCI Configuration Register 3 (PCICONF3)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

#### Common to Header TYPE00/01

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	BSTCAP	STBST	—	—	BSTCODE				SFMF	Header Type						
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
PCI R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Internal bus R/W	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Master Latency Timer								Cache Line Size							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PCI R/W	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Internal bus R/W	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

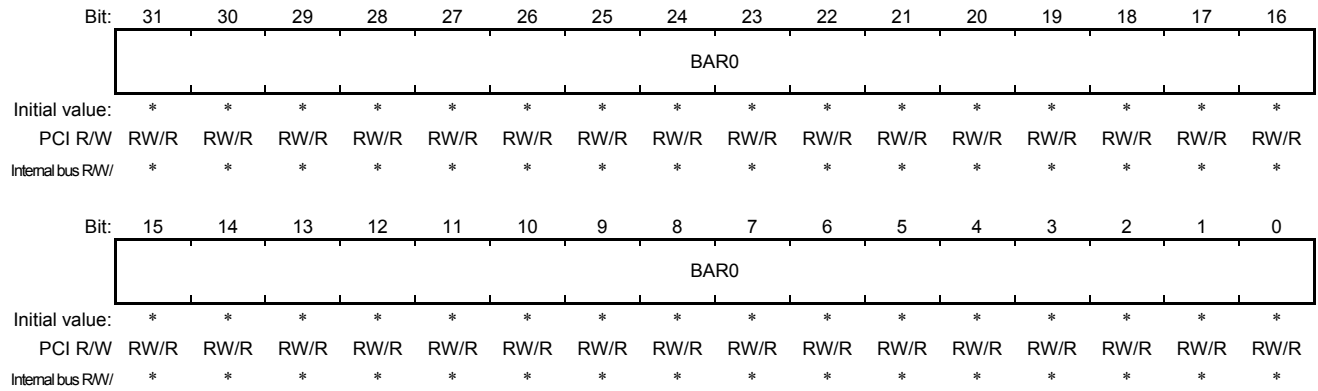
Bit	Bit Name	Initial Value	PCI R/W	Internal Bus R/W	Description
31	BSTCAP	0	R	R	BIST Capable Indicates the BIST function support status. 0: BIST function is not supported. 1: BIST function is supported. This IP does not support the BIST function.
30	STBST	0	R	R	Start BIST Indicates the BIST function execution status. 0: BIST function has ended. 1: BIST function execution is in progress. This IP does not support the BIST function.
29, 28	—	All 0	R	R	Reserved These bits are always read as 0. The write value should always be 0.
27 to 24	BSTCODE	H'0	R	R	BIST Completion Code Indicates the BIST completion status code. H'0: Passed BIST. H'1 to H'F: Failure has been detected. This IP does not support the BIST function.
23	SFMF	0	R	R/W	Single Function/ Multi-function Indicates whether single function device or multi-function device is used. 0: Single function device 1: Multi -function device (setting prohibited) This IP supports only single function. This bit must not be set to a value other than 0.

Bit	Bit Name	Initial Value	PCI R/W	Internal Bus R/W	Description
22 to 16	Header Type	H'01	R	R/W	<p>Header Type</p> <p>Specifies a layout of the configuration registers.</p> <p>H'00: Type00 layout</p> <p>H'01: Type01 layout</p> <p>H'02: Type02 layout (setting prohibited)</p> <ul style="list-style-type: none"> <li>• Root Port: Set Type01.</li> <li>• Endpoint: Set Type00.</li> </ul> <p>This IP supports Type00 and Type01, and does not support Type02.</p>
15 to 8	Master Latency Timer	All 0	R	R	<p>Master Latency Timer</p> <p>Fixed to 0. These bits are not used for PCI Express.</p>
7 to 0	Cache Line Size	All 0	R/W	R/W	<p>Cache Line Size</p> <p>These bits are not used for PCI Express functions.</p> <p>Updates the value on receiving a configuration write request for this field.</p>

**39.2.46 PCI Configuration Register 4 (PCICONF4)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

**Common to Header TYPE00/01**



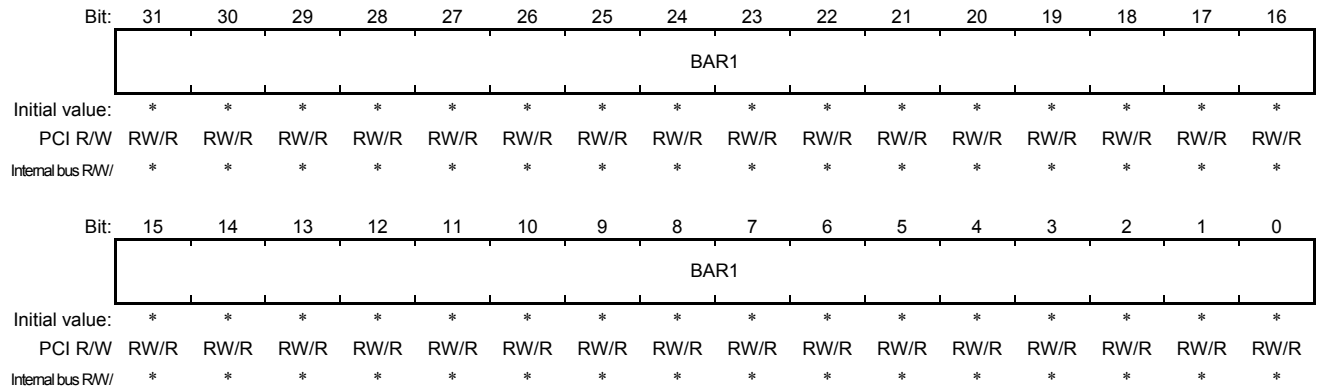
Bit	Bit Name	Initial Value	PCI R/W	Internal Bus R/W	Description
31 to 0	BAR0	*	RW/R	*	BAR0 Indicates the value of base address register 0. This field is set by local address mask register 0 in Endpoint mode. This field has no effect in Root Port mode.

Note: \* Depends on the value of local address mask register 0.

### 39.2.47 PCI Configuration Register 5 (PCICONF5)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

#### Common to Header TYPE00/01



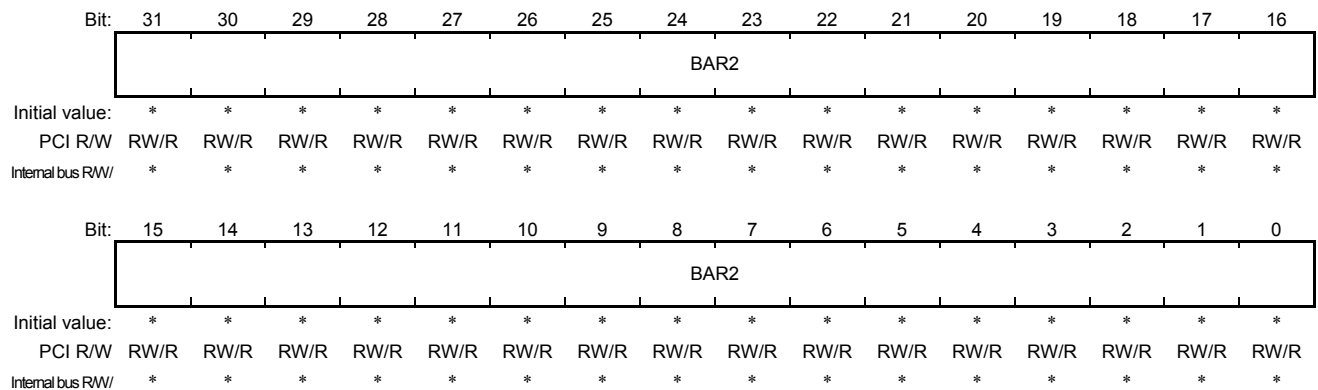
Bit	Bit Name	Initial Value	PCI R/W	Internal Bus R/W	Description
31 to 0	BAR1	*	RW/R	*	BAR1 Indicates the value of base address register 1. This field is set by local address mask register 1 in Endpoint mode. This field has no effect in Root Port mode.

Note: \* Depends on the value of local address mask register 1.

### 39.2.48 PCI Configuration Register 6 (PCICONF6)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

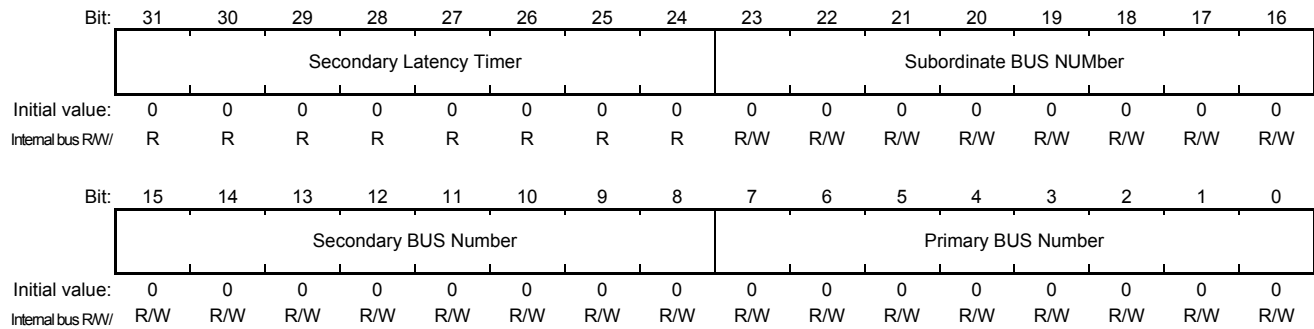
#### Header TYPE00



Bit	Bit Name	Initial Value	PCI R/W	Internal Bus R/W	Description
31 to 0	BAR2	*	RW/R	*	BAR2 Indicates the value of base address register 2. This field is set by local address mask register 2 in Endpoint mode.

Note: \* Depends on the value of local address mask register 2.

### Header TYPE01

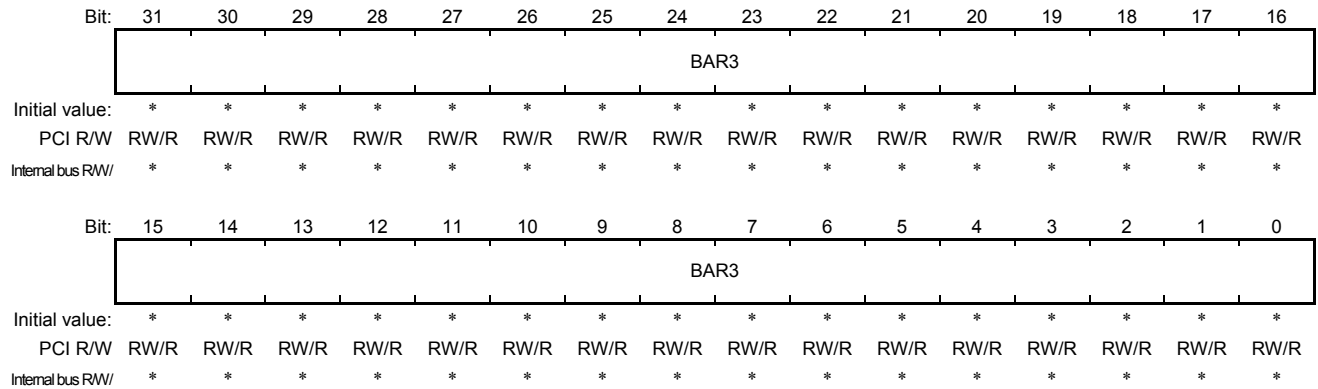


Bit	Bit Name	Initial Value	Internal Bus R/W	Description
31 to 24	Secondary Latency Timer	All 0	R	Secondary Latency Timer Fixed to 0. These bits are not used for PCI Express.
23 to 16	Subordinate BUS NUMber	All 0	R/W	Subordinate Bus Number According to the PCI standard, indicates the maximum bus number of the devices connected to the downstream link. In this IP, this field has no effect on the hardware.
15 to 8	Secondary BUS Number	All 0	R/W	Secondary Bus Number According to the PCI standard, indicates the number of the bus directly connected to the secondary IF. In this IP, this field has no effect on the hardware.
7 to 0	Primary BUS Number	All 0	R/W	Primary Bus Number According to the PCI standard, indicates the number of the bus directly connected to the primary IF. In this IP, this field has no effect on the hardware.

**39.2.49 PCI Configuration Register 7 (PCICONF7)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

**Header TYPE00**



Bit	Bit Name	Initial Value	PCI R/W	Internal Bus R/W	Description
31 to 0	BAR3	*	RW/R	*	BAR3 Indicates the value of base address register 3. This field is set by local address mask register 3 in Endpoint mode.

Note: \* Depends on the value of local address mask register 3.

**Header TYPE01**

- Secondary status register

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DPE	RSE	RMA	RTA	STA	DEVSELT	MDPE	FBBTC AP	—	66MCA P	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal bus R/W/	RW1C	RW1C	RW1C	RW1C	RW1C	R	R	RW1C	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IOLEA				IOLT				IOBEA				IOBT			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal bus R/W/	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	Internal Bus R/W	Description
31	DPE	0	RW1C	Detected Parity Error Indicates that a parity error has been detected on the secondary bus side. This bit is set to 1 upon reception of a poisoned TLP.
30	RSE	0	RW1C	Received System Error Indicates that a system error has been detected. This bit is set to 1 upon reception of an ERR_FATAL/NON_FATAL message.
29	RMA	0	RW1C	Received Master Abort Indicates that a master abort has been detected on the secondary bus side. This bit is set to 1 upon reception of a completion with the unsupported request completion status.
28	RTA	0	RW1C	Received Target Abort Indicates that a target abort has been detected on the secondary bus side. This bit is set to 1 upon reception of a completion with the completer abort completion status.
27	STA	0	RW1C	Signaled Target Abort Indicates that a target abort has been transmitted to the secondary bus side. This bit is set to 1 upon transmission of a completion with the completer abort completion status.
26, 25	DEVSELT	All 0	R	DEVSEL Timing Fixed to 0. These bits are not used for PCI Express.
24	MDPE	0	RW1C	MDPE Indicates that a master data parity error has occurred on the secondary bus side. This bit is set when either of the following conditions is satisfied while PCICONF15[16].PERS is 1. 1. A poisoned completion has been received. 2. A poisoned request has been transmitted.
23	FBTCA	0	R	Fast Back to Back Transaction Capable Fixed to 0. This bit is not used for PCI Express.
22	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.



Bit	Bit Name	Initial Value	Internal Bus R/W	Description
21	66MCAP	0	R	66 MHz Capable This bit is always read as 0. The write value should always be 0. This bit is not used for PCI Express.
20 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 12	IOLEA	All 0	R/W	IO Limit End Address According to the PCI standard, sets the address[15:12] of the upper limit address of the IO transaction to be transferred to the primary bus. In this IP, this field has no effect on the hardware.
11 to 8	IOLT	All 0	R/W	IO Limit Type According to the PCI standard, indicates the upper limit address decoding format of the IO transactions to be transferred to the primary bus. H'0: 16-bit I/O address H'1: 32-bit I/O address In this IP, this field has no effect on the hardware.
7 to 4	IOBEA	All 0	R/W	IO Base End Address According to the PCI standard, sets the address[15:12] of the base address of the IO transaction to be transferred to the primary bus. In this IP, this field has no effect on the hardware.
3 to 0	IOBT	All 0	R/W	IO Base Type According to the PCI standard, indicates the base address decoding format of the IO transactions to be transferred to the primary bus. H'0: 16-bit I/O address H'1: 32-bit I/O address In this IP, this field has no effect on the hardware.

### 39.2.50 PCI Configuration Register 8 (PCICONF8)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

#### Header TYPE00

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	BAR4															
Initial value:	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
PCI R/W	RW/R	RW/R	RW/R	RW/R	RW/R	RW/R	RW/R	RW/R	RW/R	RW/R	RW/R	RW/R	RW/R	RW/R	RW/R	RW/R
Internal bus R/W	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BAR4															
Initial value:	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
PCI R/W	RW/R	RW/R	RW/R	RW/R	RW/R	RW/R	RW/R	RW/R	RW/R	RW/R	RW/R	RW/R	RW/R	RW/R	RW/R	RW/R
Internal bus R/W	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*

Bit	Bit Name	Initial Value	PCI R/W	Internal Bus R/W	Description
31 to 0	BAR4	*	RW/R	*	BAR4 Indicates the value of base address register 4. This field is set by local address mask register 4 in Endpoint mode.

Note: \* Depends on the value of local address mask register 4.

#### Header TYPE01

Bit:	3	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Memory Limit												—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal bus R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Memory Base												—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal bus R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R

Bit	Bit Name	Initial Value	Internal Bus R/W	Description
31 to 20	Memory Limit	All 0	R/W	Memory Limit According to the PCI standard, sets the upper limit address of the memory mapped IO performing transfer between the primary IF and the secondary IF. This field corresponds to address[31:20]. In this IP, this field has no effect on the hardware.
19 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

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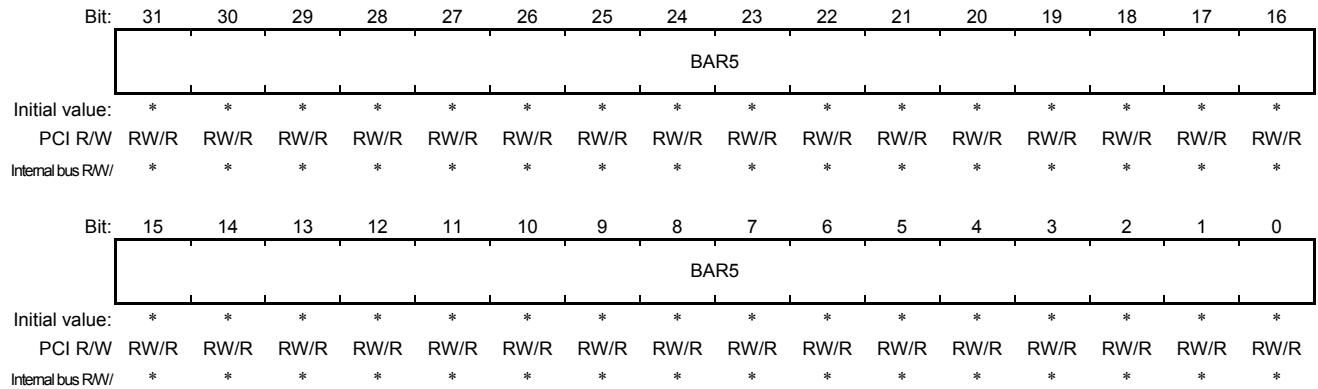
Bit	Bit Name	Initial Value	Internal Bus R/W	Description
15 to 4	Memory Base	All 0	R/W	Memory Base According to the PCI standard, sets the base address of the memory mapped IO performing transfer between the primary IF and the secondary IF. This field corresponds to address[31:20]. In this IP, this field has no effect on the hardware.
3 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

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### 39.2.51 PCI Configuration Register 9 (PCICONF9)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

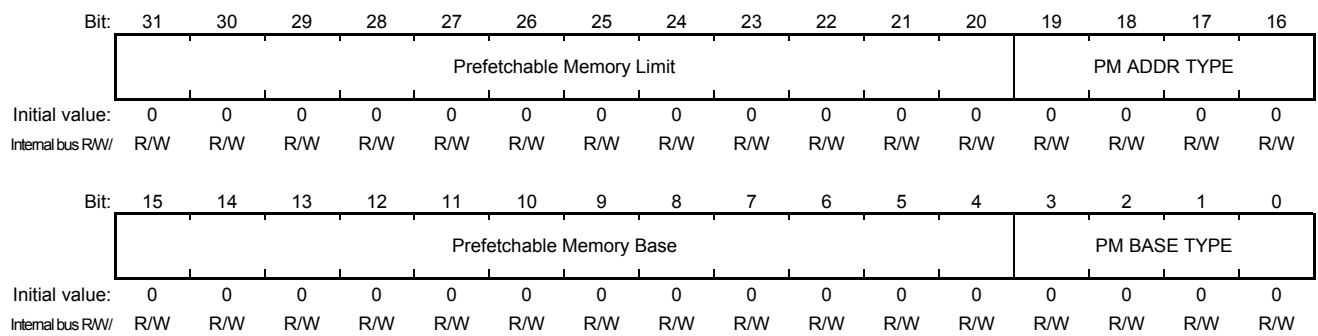
#### Header TYPE00



Bit	Bit Name	Initial Value	PCI R/W	Internal Bus R/W	Description
31 to 0	BAR5	*	RW/R	*	BAR5 Indicates the value of base address register 5. This field is set by local address mask register 5 in Endpoint mode.

Note: \* Depends on the value of local address mask register 5.

#### Header TYPE01



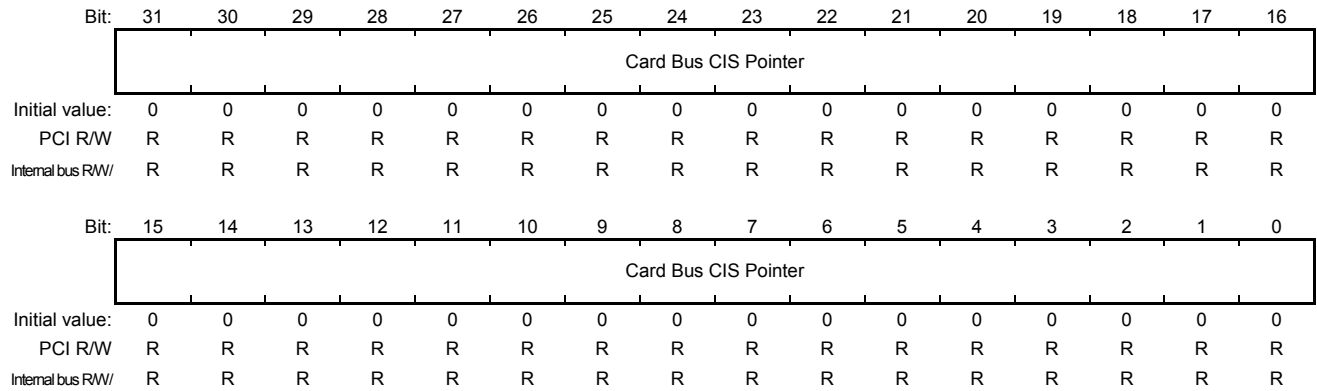
Bit	Bit Name	Initial Value	Internal Bus R/W	Description
31 to 20	Prefetchable Memory Limit	H'000	R/W	Prefetchable Memory Limit According to the PCI standard, sets the upper limit address of the prefetchable memory performing transfer between the primary IF and the secondary IF. This field corresponds to address[31:20]. In this IP, this field has no effect on the hardware.

Bit	Bit Name	Initial Value	Internal Bus R/W	Description
19 to 16	PM ADDR TYPE	H'0	R/W	<p>Prefetchable Memory Address Decode TYPE</p> <p>According to the PCI standard, indicates the upper limit address decoding format of the prefetchable memory performing transfer between the primary IF and the secondary IF.</p> <p>H'0: 32-bit address H'1: 64-bit address</p> <p>In this IP, this field has no effect on the hardware.</p>
15 to 4	Prefetchable Memory Base	H'000	R/W	<p>Prefetchable Memory Base</p> <p>According to the PCI standard, sets the base address of the prefetchable memory performing transfer between the primary IF and the secondary IF.</p> <p>This field corresponds to address[31:20]. In this IP, this field has no effect on the hardware.</p>
3 to 0	PM BASE TYPE	H'0	R/W	<p>Prefetchable Memory Base Type</p> <p>According to the PCI standard, indicates the base address decoding format of the prefetchable memory performing transfer between the primary IF and the secondary IF.</p> <p>H'0: 32-bit address H'1: 64-bit address</p> <p>In this IP, this field has no effect on the hardware.</p>

**39.2.52 PCI Configuration Register 10 (PCICONF10)**

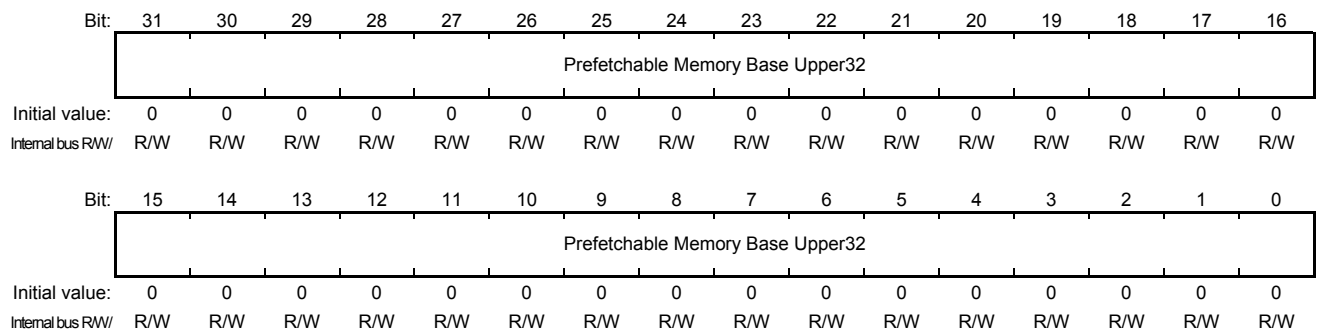
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

**Header TYPE00**



Bit	Bit Name	Initial Value	PCI R/W	Internal Bus R/W	Description
31 to 0	Card Bus CIS Pointer	All 0	R	R	Card Bus CIS Pointer According to the PCI standard, indicates the value of the card bus CIS pointer. This IP does not support the card bus CIS pointer. Fixed to 0.

**Header TYPE01**

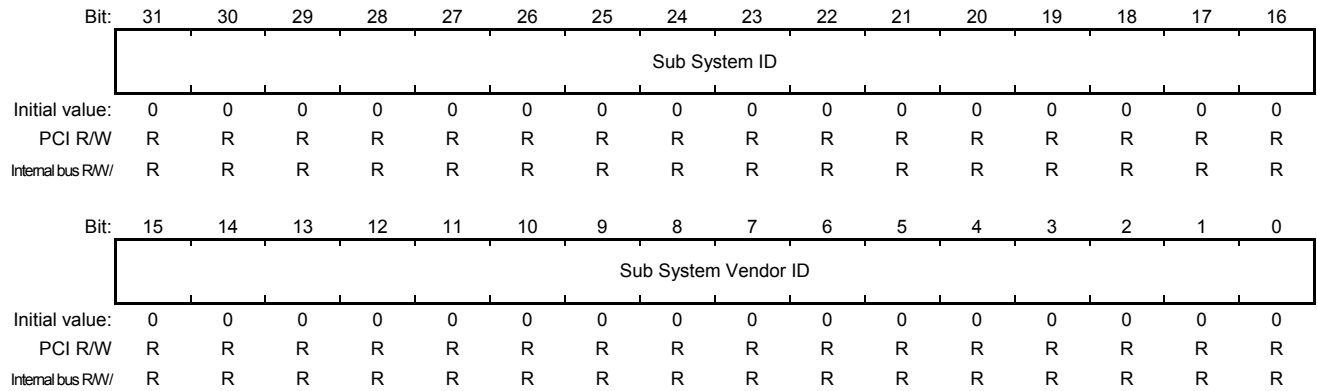


Bit	Bit Name	Initial Value	Internal Bus R/W	Description
31 to 0	Prefetchable Memory Base Upper32	All 0	R/W	Prefetchable Memory Base Upper 32 According to the PCI standard, sets the upper limit address of the prefetchable memory performing transfer between the primary IF and the secondary IF. This field corresponds to address[63:32]. This field is valid when PCICONF9[3:0].PM BASE TYPE = H'1 (64-bit address decode format). In this IP, this field has no effect on the hardware.

### 39.2.53 PCI Configuration Register 11 (PCICONF11)

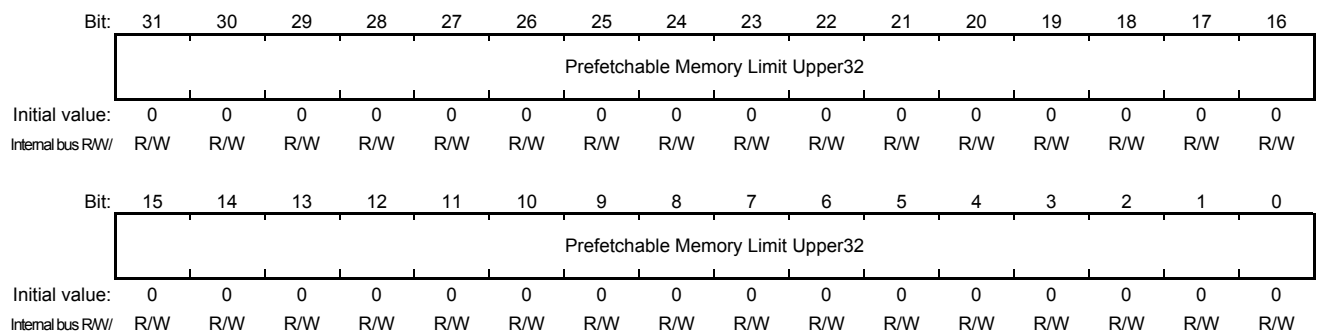
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

#### Header TYPE00



Bit	Bit Name	Initial Value	PCI R/W	Internal Bus R/W	Description
31 to 16	Sub System ID	All 0	R	R	Sub System ID I Indicates the sub-system ID. The value of SUBIDSETR.Sub System ID Set field is reflected on this field.
15 to 0	Sub System Vendor ID	All 0	R	R	Sub System Vendor ID Indicates the sub-system vendor ID. The value of SUBIDSETR.Sub System Vendor ID Set field is reflected on this field.

#### Header TYPE01



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Bit	Bit Name	Initial Value	Internal Bus R/W	Description
31 to 0	Prefetchable Memory Limit Upper32	All 0	R/W	<p>Prefetchable Memory Limit Upper 32</p> <p>According to the PCI standard, sets the base address of the prefetchable memory performing transfer between the primary IF and the secondary IF. This field corresponds to address[63:32].</p> <p>This field is valid when PCICONF9[19:16].PM ADDR TYPE = H'1 (64-bit address decode format).</p> <p>In this IP, this field has no effect on the hardware.</p>

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### 39.2.54 PCI Configuration Register 12 (PCICONF12)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

#### Header TYPE00

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Expansion ROM BAR															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PCI R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Internal bus	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Expansion ROM BAR															EROM E
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PCI R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Internal bus	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	PCI R/W	Internal Bus R/W	Description
31 to 11	Expansion ROM BAR	All 0	R	R	Expansion ROM BAR According to the PCI standard, indicates the value of expansion ROM base address register. This IP does not support expansion ROM.
10 to 1	—	All 0	R	R	Reserved These bits are always read as 0. The write value should always be 0.
0	EROME	0	R	R	Expansion ROM Enable According to the PCI standard, indicates that access to expansion ROM is enabled. This IP does not support expansion ROM.

#### Header TYPE01

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IO Limit Upper Address															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal bus R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IO Base Upper Address															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal bus R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	Internal Bus R/W	Description
31 to 16	IO Limit Upper Address	All 0	R/W	<p>IO Limit Upper Address</p> <p>According to the PCI standard, sets the address[31:16] of the upper limit address of the IO transaction to be transferred to the primary bus.</p> <p>This field is valid when PCICONF7[11:8].IO Limit Type = 1 (32-bit address decode format).</p> <p>In this IP, this field has no effect on the hardware.</p>
15 to 0	IO Base Upper Address	All 0	R/W	<p>IO Base Upper Address</p> <p>According to the PCI standard, sets the address[31:16] of the base address of the IO transaction to be transferred to the primary bus.</p> <p>This field is valid when PCICONF7[3:0].IO Base Type = 1 (32-bit address decode format).</p> <p>In this IP, this field has no effect on the hardware.</p>

### 39.2.55 PCI Configuration Register 13 (PCICONF13)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

#### Common to Header TYPE00/01

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PCI R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Internal bus R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	Capabilities Pointer							
Initial value:	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
PCI R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Internal bus R/W	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	PCI R/W	Internal Bus R/W	Description
31 to 8	—	All 0	R	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>
7 to 0	Capabilities Pointer	H'40	R	R/W	<p>Capabilities Pointer</p> <p>Pointer to the extended capability list.</p> <p>This IP has the extended capability list and this field points to PCI PM capability pointer H'40.</p>

### 39.2.56 PCI Configuration Register 14 (PCICONF14)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

#### Header TYPE00

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PCI R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Internal bus R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PCI R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Internal bus R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	PCI R/W	Internal Bus R/W	Description
31 to 0	—	All 0	R	R	Reserved These bits are always read as 0. The write value should always be 0.

#### Header TYPE01

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Expansion ROM BAR															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal bus R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Expansion ROM BAR															EROME
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal bus R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	Internal Bus R/W	Description
31 to 11	Expansion ROM BAR	All 0	R	Expansion ROM BAR According to the PCI standard, indicates the value of expansion ROM base address register. This IP does not support Expansion ROM.
10 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	EROME	0	R	Expansion ROM Enable According to the PCI standard, indicates that access to expansion ROM is enabled. This IP does not support expansion ROM.

## 39.2.57 PCI Configuration Register 15 (PCICONF15)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

## Header TYPE00

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	MAXLAT								MINGNT							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PCI R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Internal bus R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Interrupt Pin								Interrupt Line							
Initial value:	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
PCI R/W	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Internal bus R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	PCI R/W	Internal Bus R/W	Description
31 to 24	MAXLAT	All 0	R	R	MAXLAT Fixed to 0. These bits are not used for PCI Express.
23 to 16	MINGNT	All 0	R	R	MINGNT Fixed to 0. These bits are not used for PCI Express.
15 to 8	Interrupt Pin	All 0	R	R/W	Interrupt Pin Specifies the legacy interrupt message used by the device at initialization. When no legacy interrupts are used, set 0. 0: Legacy interrupt is not used. 1: INTA is used. 2: INTB is used. (Setting prohibited) 3: INTC is used. (Setting prohibited) 4: INTD is used. (Setting prohibited) This field must not be set to a value other than 0 and 1.
7 to 0	Interrupt Line	H'FF	R/W	R/W	Interrupt Line Indicates information on legacy interrupt routing.

## Header TYPE01

- Bridge control register

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	DTSEE	DTSTS	SECDT	PRDT	FBBTC AP	SECBR ST	MABM D	VGA16 DEC	VGAE	ISAE	SERRE	PERS
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal bus R/W	R	R	R	R	R	R	R	R	R	R/W	R	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Interrupt Pin								Interrupt Line							
Initial value:	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Internal bus R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	Internal Bus R/W	Description
31 to 28	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
27	DTSEE	0	R	Discard Timer SERR Enable This bit is always read as 0. The write value should always be 0. This bit is not used for PCI Express.
26	DTSTS	0	R	Discard Timer Status This bit is always read as 0. The write value should always be 0. This bit is not used for PCI Express.
25	SECDT	0	R	Secondary Discard Timer This bit is always read as 0. The write value should always be 0. This bit is not used for PCI Express.
24	PRDT	0	R	Primary Discard Timer This bit is always read as 0. The write value should always be 0. This bit is not used for PCI Express.
23	FBBTCAP	0	R	Fast Back to Back Transaction Capable This bit is always read as 0. The write value should always be 0. This bit is not used for PCI Express.
22	SECBRST	0	R/W	Secondary Bus Reset Resets the secondary IF. Setting this bit to 1 causes the LTSSM to make a transition to the hot reset state. Clearing this bit cancels the hot reset state of LTSSM.
21	MABMD	0	R	Master Abort Mode This bit is always read as 0. The write value should always be 0. This bit is not used for PCI Express.
20	VGA16DEC	0	R/W	VGA 16-bit Decode According to the PCI standard, enables VGA IO decoding. In this IP, this field has no effect on the hardware.
19	VGAE	0	R/W	VGA Enable According to the PCI standard, enables VGA address translation. In this IP, this field has no effect on the hardware.
18	ISAE	0	R/W	ISA Enable According to the PCI standard, enables ISA IO address translation. In this IP, this field has no effect on the hardware.

Bit	Bit Name	Initial Value	Internal Bus R/W	Description
17	SERRE	0	R/W	<p>SERR Enable</p> <p>Enables ERR_FATAL/ERR_NONFATAL/ERR_COR message transfer (notification) from the secondary IF to the primary IF.</p> <p>1: Enables error message transfer (notification). 0: Disables error message transfer (notification).</p>
16	PERS	0	R/W	<p>Parity Error Response</p> <p>Enables setting of the PCICONF7[24].MDPE bit.</p>
15 to 8	Interrupt Pin	All 0	R/W	<p>Interrupt Pin</p> <p>Specifies a legacy interrupt message to be used by the device. When no legacy interrupts are used, set 0.</p>
7 to 0	Interrupt Line	H'FF	R/W	<p>Interrupt Line</p> <p>According to the PCI standard, indicates information on legacy interrupt routing.</p> <p>According to this IP, the set values are defined as follows.</p> <p>H'00 - H'FE: INTx interrupt is reported to INTC. H'FF: INTx interrupt is not reported to INTC.</p>

### 39.2.58 PCI Power Management Capability Register 0 (PMCAP0)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

#### Common to Header TYPE00/01

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PMESP D3COLD	PMESP D3HOT	PMESP D2	PMESP D1	PMESP D0	D2SP	D1SP	AUX Current			DSI	—	PMECL K	PCI PM Version		
Initial value:	1	1	0	0	1	0	0	0	0	0	0	0	0	0	1	1
PCI R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Internal bus R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Next Capability Pointer								Capability ID							
Initial value:	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	1
PCI R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Internal bus R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	PCI R/W	Internal Bus R/W	Description
31	PMESPD3COLD	1	R	R/W	<p>PME Support D3COLD</p> <p>Indicates whether PME generation is supported or not in the D3Cold state.</p> <p>0: Does not support PME generation in the D3Cold state. 1: Supports PME generation in the D3Cold state.</p> <ul style="list-style-type: none"> <li>Root Port: Set this bit to 1 at initialization.</li> <li>Endpoint: Set the device function at initialization.</li> </ul>
30	PMESPD3HOT	1	R	R/W	<p>PME Support D3HOT</p> <p>Indicates whether PME generation is supported or not in the D3Hot state.</p> <p>0: Does not support PME generation in the D3Hot state. 1: Supports PME generation in the D3Hot state.</p> <ul style="list-style-type: none"> <li>Root Port: Set this bit to 1 at initialization.</li> <li>Endpoint: Set the device function at initialization.</li> </ul>
29	PMESPD2	0	R	R/W	<p>PME Support D2</p> <p>Indicates whether PME generation is supported or not in the D2 state.</p> <p>0: Does not support PME generation in the D2 state. 1: Supports PME generation in the D2 state.</p> <p>Set the device function at initialization.</p>

Bit	Bit Name	Initial Value	PCI R/W	Internal Bus R/W	Description
28	PMESPD1	0	R	R/W	<p>PME Support D1</p> <p>Indicates whether PME generation is supported or not in the D1 state.</p> <p>0: Does not support PME generation in the D1 state. 1: Supports PME generation in the D1 state.</p> <p>Set the device function at initialization.</p>
27	PMESPD0	1	R	R/W	<p>PME Support D0</p> <p>Indicates whether PME generation is supported or not in the D0 state.</p> <p>0: Does not support PME generation in the D0 state. 1: Supports PME generation in the D0 state.</p> <ul style="list-style-type: none"> <li>• Root Port: Set this bit to 1 at initialization.</li> <li>• Endpoint: Set the device function at initialization.</li> </ul>
26	D2SP	0	R	R/W	<p>D2 Support</p> <p>Indicates whether the D2 power management state is supported or not.</p> <p>0: Does not support the D2 state. 1: Supports the D2 state.</p> <p>Set the device function at initialization.</p>
25	D2SP	0	R	R/W	<p>D1 Support</p> <p>Indicates whether the D1 power management state is supported or not.</p> <p>0: Does not support the D1 state. 1: Supports the D1 state.</p> <p>Set the device function at initialization.</p>
24 to 22	AUX Current	H'0	R	R/W	<p>AUX Current</p> <p>Indicates the current of 3.3V auxiliary power supply. Set this field at initialization.</p> <p>H'0: 0 mA (without auxiliary power supply) H'1: 55 mA H'2: 100 mA H'3: 160 mA H'4: 220 mA H'5: 270 mA H'6: 320 mA H'7: 375 mA</p> <p>When PMCAP0[31].PMESPD3COLD = 0, use the device with this field set to the initial value (= 0).</p>



Bit	Bit Name	Initial Value	PCI R/W	Internal Bus R/W	Description
21	DSI	0	R	R/W	<p>Device Specific Initialization</p> <p>Indicates that the device-specific initialization sequence is required after D0 initialization.</p> <p>0: The device-specific initialization sequence is not necessary.</p> <p>1: The device-specific initialization sequence is required.</p> <p>Set this field at initialization.</p>
20	—	0	R	R	<p>Reserved</p> <p>This bit is always read as 0. The write value should always be 0.</p>
19	PMECLK	0	R	R	<p>PME Clock</p> <p>This bit is always read as 0. The write value should always be 0.</p> <p>This bit is not used for PCI Express.</p>
18 to 16	PCI PM Version	H'3	R	R/W	<p>PCI PM Version</p> <p>Indicate the corresponding PCI PM Interface Specification version. This device corresponds to the PCI PM Interface Specification version 1.2.</p>
15 to 8	Next Capability Pointer	H'50	R	R/W	<p>Next Capability Pointer</p> <p>Pointer to the extended capability list</p> <p>This field points to MSI capability pointer H'50.</p>
7 to 0	Capability ID	H'01	R	R/W	<p>Capability ID</p> <p>Capability List ID</p> <p>Indicates the power management capability (H'01).</p>

### 39.2.59 PCI Power Management Capability Register 1 (PMCAP1)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

#### Common to Header TYPE00/01

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
	DATA								BPCCE	B2B3SP	—	—	—	—	—	—	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
PCI R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	
Internal bus R/W	R	R	R	R	R	R	R	R	R/W	R/W	R	R	R	R	R	R	
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	PMEST	Data Scale		Data Select				PMEE	—	—	—	—	NOS RST	—	Power State		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
PCI R/W	RW1C or RW1C	R	R	R	R	R	R	RW or RWS	R	R	R	R	R	R	R	R/W	R/W
Internal bus R/W	RW1c	R	R	R	R	R	R	R/w	R	R	R	R	R	R	R/W	R/W	

Bit	Bit Name	Initial Value	PCI R/W	Internal Bus R/W	Description
31 to 24	DATA	All 0	R	R	DATA According to the PCI standard, indicates the value selected with PMCAP1[12:0].Data Select. This IP does not support this field.
23	BPCCE	0	R	R/W	Bus Power Clock Control Enable Enables the PCI bus power/clock control function. 0: Disables the PCI bus power/clock control function. 1: Enables the PCI bus power/clock control function. Set this field to 0 at initialization.
22	B2B3SP	0	R	R/W	B2 B3 Support Indicates the bus state in the D3Hot state. This field is valid when PMCAP1[23].BPCCE = 1. 0: Clock supply to the secondary IF does not stop in the D3Hot state. (B3) 1: Clock supply to the secondary IF stops in the D3Hot state. (B2) Set this field to 0 at initialization.
21 to 16	—	All 0	R	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	PCI R/W	Internal Bus R/W	Description
15	PMEST	0	RW1C or RW1CS	RW1C	<p>PME Status</p> <p>This field is valid when the PME is supported.</p> <p>Indicates the PME generation status.</p> <p>0: A PME message is not being transmitted.</p> <p>1: A PME message is being transmitted.</p> <p>This bit is set to 1 when a PME message is transmitted.</p> <p>Note: When PME generation is enabled in the D3Cold state, this field is RW1CS.</p>
14, 13	Data Scale	All 0	R	R	<p>Data Scale</p> <p>According to the PCI standard, indicates the scale used to indicate the value selected with PMCAP1[12:9].Data Select in PMCAP1[31:24].DATA.</p> <p>This IP does not support this field.</p>
12 to 9	Data Select	All 0	R	R	<p>Data Select</p> <p>According to the PCI standard, sets the value and unit to be indicated in PMCAP1[31:24].DATA and PMCAP1[14:13].Data Scale.</p> <p>This IP does not support this field.</p>
8	PMEE	0	R/W or RWS	R/W	<p>PME Enable</p> <p>Enables PME message transmission.</p> <p>0: Disables PME message transmission.</p> <p>1: Enables PME message transmission.</p> <p>When the device does not support the PME message transmission function, this bit should always be 0.</p> <p>Note: When PME generation is enabled in the D3Cold state, this field is RWS.</p>
7 to 4	—	All 0	R	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>
3	NOSRST	0	R	R/W	<p>No Soft Reset</p> <p>Indicates whether internal reset is performed or not when the device makes a transition from the D3Hot state to the D0 state.</p> <p>0: Internal reset is performed when the device makes a transition from D3Hot state to D0 state.</p> <p>1: Internal reset is not performed when the device makes a transition from D3Hot state to D0 state.</p> <p>Set the device function at initialization.</p>
2	—	0	R	R	<p>Reserved</p> <p>This bit is always read as 0. The write value should always be 0.</p>

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<b>Bit</b>	<b>Bit Name</b>	<b>Initial Value</b>	<b>PCI R/W</b>	<b>Internal Bus R/W</b>	<b>Description</b>
1, 0	Power State	00	R/W	R/W	Power State Specifies the power state. 00: D0 01: D1 10: D2 11: D3Hot Note: The setting is ignored when 1 is set with D1 unsupported or 2 is set with D2 unsupported.

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### 39.2.60 MSI Capability Register 0 (MSICAP0)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

#### Header TYPE00 only

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	PVMSK	64ADC AP	MMESE			MMESCAP			MSIE
Initial value:	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0
PCI R/W	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R	R	R	R/W
Internal bus R/W	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Next Capability Pointer								Capability ID							
Initial value:	0	1	1	1	0	0	0	0	0	0	0	0	0	1	0	1
PCI R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Internal bus R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	PCI R/W	Internal Bus R/W	Description
31 to 25	—	All 0	R	R	Reserved These bits are always read as 0. The write value should always be 0.
24	PVMSK	1	R	R	Per Vector Masking Indicates whether the per vector masking function is supported or not. 0: The per vector masking function is not supported. 1: The per vector masking function is supported. This device supports the per vector masking function.
23	64ADCAP	1	R	R	64-bit Address Capable Indicates whether transmission of a 64-bit address message is supported or not. 0: A 64-bit address message cannot be transmitted. 1: A 64-bit address message can be transmitted. This device supports transmission of a 64-bit address message.
22 to 20	MMESE	000	R/W	R/W	Multiple Message Enable Sets the number of interrupt vectors that can be transmitted. 000: 1 vector 001: 2 vectors 010: 4 vectors 011: 8 vectors 100: 16 vectors 101: 32 vectors 110: Reserved 111: Reserved

Bit	Bit Name	Initial Value	PCI R/W	Internal Bus R/W	Description
19 to 17	MMESCAP	000	R	R/W	<p>Multiple Message Capable</p> <p>Sets the number of interrupt vectors that a device can transmit.</p> <p>000: 1 vector            001: 2 vectors            010: 4 vectors            011: 8 vectors            100: 16 vectors            101: 32 vectors            110: Reserved            111: Reserved</p> <p>Set the device function at initialization.</p>
16	MSIE	0	R/W	R/W	<p>MSI Enable</p> <p>Enables the MSI function.</p> <p>0: Disables the MSI function.            1: Enables the MSI function.</p>
15 to 8	Next Capability Pointer	H'70	R	R/W	<p>Next Capability Pointer</p> <p>Pointer to the extended capability list.</p> <p>Points to the PCI Express capability pointer H'70.</p>
7 to 0	Capability ID	H'05	R	R/W	<p>Capability ID</p> <p>Capability list ID</p> <p>Indicates the MSI capability ID (H'05).</p>

**39.2.61 MSI Capability Register 1 (MSICAP1)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

**Header TYPE00 only**

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Lower Message Address															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PCI R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Internal bus R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

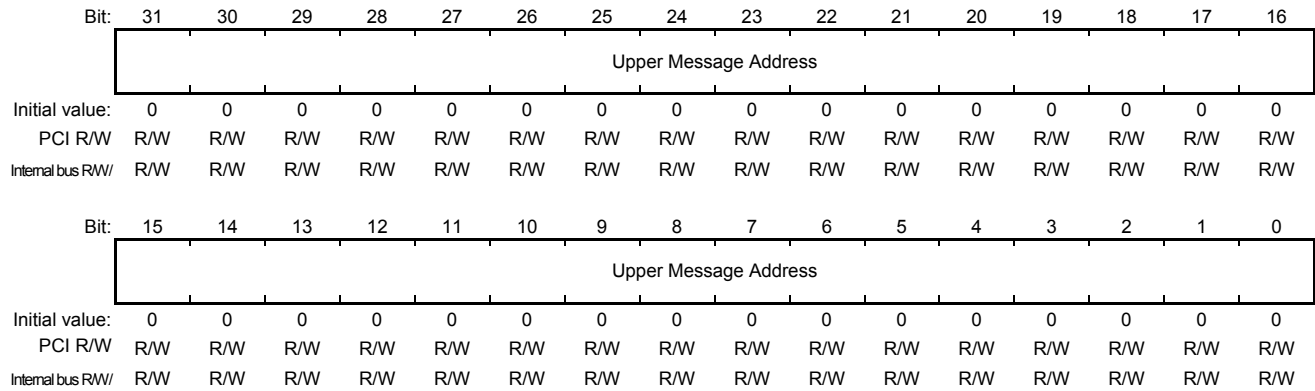
  

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Lower Message Address														—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PCI R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R
Internal bus R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R

Bit	Bit Name	Initial Value	PCI R/W	Internal Bus R/W	Description
31 to 2	Lower Message Address	All 0	R/W	R/W	Lower Message Address Specifies the address[31:2] of an MSI message during an MSI transmission. The value of this field is used for transmission of an MSI message.
1, 0	—	All 0	R	R	Reserved These bits are always read as 0. The write value should always be 0.

**39.2.62 MSI Capability Register 2 (MSICAP2)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

**Header TYPE00 only**

Bit	Bit Name	Initial Value	PCI R/W	Internal Bus R/W	Description
31 to 0	Upper Message Address	All 0	R/W	R/W	Upper Message Address Specifies the address[63:32] of an MSI message during an MSI transmission.  The value of this field is used for transmission of an MSI message.



**39.2.63 MSI Capability Register 3 (MSICAP3)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

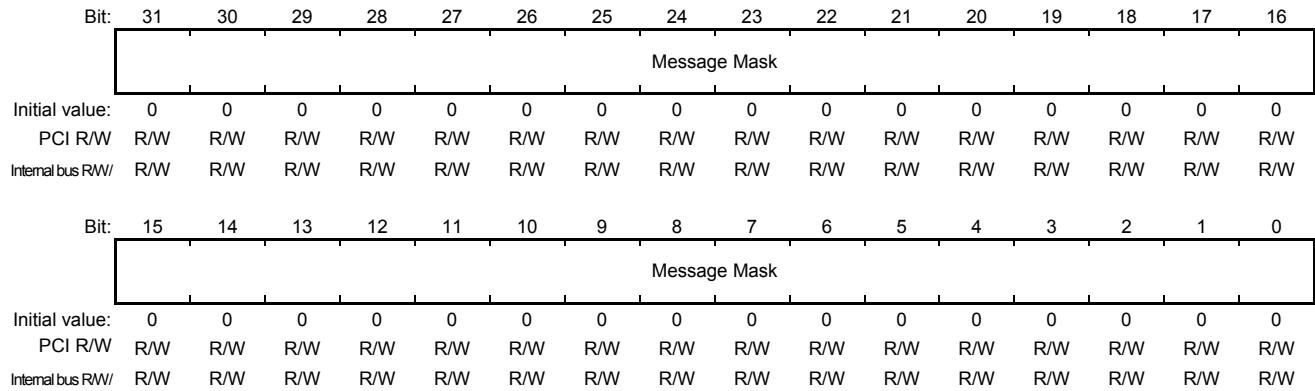
**Header TYPE00 only**

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PCI R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Internal bus R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Message Data															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PCI R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Internal bus R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	PCI R/W	Internal Bus R/W	Description
31 to 16	—	All 0	R	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 0	Message Data	All 0	RW	RW	Message Data Specifies the MSI message data during an MSI transmission. The value of this field is used for transmission of an MSI message. When more than one interrupt vector is assigned to this device through MSICAP0[22:20].MMESE, a quantity of transmit data equal to the assigned number of vectors can be changed.

**39.2.64 MSI Capability Register 4 (MSICAP4)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

**Header TYPE00 only**

Bit	Bit Name	Initial Value	PCI R/W	Internal Bus R/W	Description
31 to 0	Message Mask	All 0	R/W	R/W	<p>Message Mask</p> <p>Masks MSI transmission.</p> <p>Masks the MSI transmission of the interrupt vector assigned by MSICAP0[22:20].MMESE.</p> <p>Message Mask[N] = 1: Masks the MSI transmission of interrupt vector [N].</p> <p>Message Mask[N] = 0: Does not mask the MSI transmission of interrupt vector [N].</p>

**39.2.65 MSI Capability Register 5 (MSICAP5)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

**Header TYPE00 only**

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Message Pending															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PCI R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Internal bus R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Message Pending															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PCI R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Internal bus R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	PCI R/W	Internal Bus R/W	Description
31 to 0	Message Pending	All 0	R	R	<p>Message Pending</p> <p>Indicates that MSI transmission is pending.</p> <p>If a transmission request of the interrupt vector corresponding to bit [N] is generated while it is masked by MSICAP4.Message Mask[N] = 1, MSICAP5.Message Pending[N] is set to 1 to indicate that transmission is pending.</p> <p>When MSICAP4.Message Mask[N] is updated to 0 upon reception of a configuration write request, MSICAP5.Message Pending[N] is updated to 0 to transmit the MSI message.</p> <p>This field is set to 1 when an interrupt transmission request is detected while MSICAP4.Message Mask[N] = 1.</p> <p>When MSICAP4.Message Mask[N] is cleared to 0 while MSICAP5.Message Pending[N] = 1, MSICAP5.Message Pending[N] is cleared to 0, and at the same time an MSI message is transmitted.</p>

### 39.2.66 PCI Express Capability Register 0 (EXPCAP0)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

#### Common to Header TYPE00/01

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	Interrupt Message Number				SLTIMP	Device Port Type				Capability Version				
Initial value:	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0
PCI R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Internal bus R/W	R	R	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Next Capability Pointer								Capability ID							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
PCI R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Internal bus R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	PCI R/W	Internal Bus R/W	Description
31, 30	—	All 0	R	R	Reserved These bits are always read as 0. The write value should always be 0.
29 to 25	Interrupt Message Number	All 0	R	R/W	Interrupt Message Number According to the PCI standard, indicates the offset of the interrupt vectors used for HotPlug MSI or PME MSI. This IP does not support this field. The write value should always be 0.
24	SLTIMP	0	R	R	Slot Implemented Indicates whether the device link is connected to the PCI Express slot. 0: Not connected to the slot. 1: Connected to the slot. <ul style="list-style-type: none"> <li>Root Port: This IP does not support the slot function. In this IP, this field has no effect on the hardware.</li> <li>Endpoint: Use the initial value.</li> </ul>

Bit	Bit Name	Initial Value	PCI R/W	Internal Bus R/W	Description
23 to 20	Device Port Type	H'4	R	R/W	Device Port Type Indicates the device type. H'0: PCI Express Endpoint H'1: (Legacy PCI Express Endpoint) Setting prohibited H'4: Root Port of PCI Express Root Complex (initial value) H'5: (Upstream Port of PCI Express Switch) Setting prohibited H'6: (Downstream Port of PCI Express Switch) Setting prohibited H'7: (PCI Express to PCI/PCI-X Bridge) Setting prohibited H'8: (PCI/PCI-X to PCI Express Bridge) Setting prohibited H'9: (Root Complex Integrated Endpoint Device) Setting prohibited H'A: (Root Complex Event Collector) Setting prohibited <ul style="list-style-type: none"> <li>• Root Port: Set H'4 at initialization.</li> <li>• Endpoint: Set H'0 at initialization.</li> </ul>
19 to 16	Capability Version	H'2	R	R	Capability Version Indicates the version of this capability.
15 to 8	NEXT Capability Pointer	H'00	R	R/W	NEXT Capability Pointer Pointer to the extension capability list Indicates H'00, which is End Of List.
7 to 0	Capability ID	H'10	R	R/W	Capability ID Capability List ID Indicates the PCI Express capability ID (H'10).

### 39.2.67 PCI Express Capability Register 1 (EXPCAP1)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

#### Common to Header TYPE00/01

- Device capability register

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
	—	—	—	FLRCA P	CAPSLPLSC		Captured Slot Power Limit Value									—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
PCI R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	
Internal bus R/W	R	R	R	R/W	R	R	R	R	R	R	R	R	R	R	R	R	

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RBER	—	—	—	EL1ACLAT			EL0ACLAT			ETAGS	PFS		MPSS		
Initial value:	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
PCI R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Internal bus R/W	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	PCI R/W	Internal Bus R/W	Description
31 to 29	—	All 0	R	R	Reserved These bits are always read as 0. The write value should always be 0.
28	FLRCAP	0	R	R/W	Function Level Reset Capability Indicates that the function level reset function is supported. <ul style="list-style-type: none"> <li>Root Port: Not need to be set.</li> <li>Endpoint: This IP does not support the function level reset function. This bit should be fixed to 0.</li> </ul>
27, 26	CAPSLPLSC	00	R	R	Captured Slot Power Limit Scale Indicates the slot power limit value scale. <ul style="list-style-type: none"> <li>00: 1.0x</li> <li>01: 0.1x</li> <li>10: 0.01x</li> <li>11: 0.001x</li> </ul> <ul style="list-style-type: none"> <li>Root Port: Not need to be set.</li> <li>Endpoint: This field is updated on reception of the Set_Slot_Power_Limit message.</li> </ul>

Bit	Bit Name	Initial Value	PCI R/W	Internal Bus R/W	Description
25 to 18	Captured Slot Power Limit Value	H'00	R	R	<p>Captured Slot Power Limit Value</p> <p>Indicates the limit of power supplied from the slot (in Watts) in combination with EXPCAP1[27:26].CAPSLPLSC.</p> <ul style="list-style-type: none"> <li>• Root Port: Not need to be set.</li> <li>• Endpoint: This field is updated on reception of the Set_Slot_Power_Limit message.</li> </ul>
17, 16	—	All 0	R	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>
15	RBER	1	R	R	<p>Role-Based Error Reporting</p> <p>The value is fixed to 1 according to the PCI Express version 1.1 or later.</p>
14 to 12	—	All 0	R	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>
11 to 9	EL1ACLAT	000	R	R/W	<p>Endpoint L1 Acceptable Latency</p> <p>Indicates the maximum L1 to L0 transition latency that the device can accept.</p> <p>000: L0 recovery must be completed within 1 <math>\mu</math>s.            001: L0 recovery must be completed within 2 <math>\mu</math>s.            010: L0 recovery must be completed within 4 <math>\mu</math>s.            011: L0 recovery must be completed within 8 <math>\mu</math>s.            100: L0 recovery must be completed within 16 <math>\mu</math>s.            101: L0 recovery must be completed within 32 <math>\mu</math>s.            110: L0 recovery must be completed within 64 <math>\mu</math>s.            111: No time limit</p> <p>Set the device support status at initialization.</p>
8 to 6	ELOACLAT	000	R	R/W	<p>Endpoint L0s Acceptable Latency</p> <p>Indicates the maximum L0s to L0 transition latency that the device can accept.</p> <p>000: L0 recovery must be completed within 64 ns.            001: L0 recovery must be completed within 128 ns.            010: L0 recovery must be completed within 256 ns.            011: L0 recovery must be completed within 512 ns.            100: L0 recovery must be completed within 1 <math>\mu</math>s.            101: L0 recovery must be completed within 2 <math>\mu</math>s.            110: L0 recovery must be completed within 4 <math>\mu</math>s.            111: No time limit</p> <p>Set the device support status at initialization.</p>
5	ETAGS	1	R	R	<p>Extended Tag Field Supported</p> <p>Indicates the tag ID size supported as the requester ID.</p> <p>0: 5-bit tag            1: 8-bit extension tag</p> <p>This IP supports the extension 8-bit tag ID function.</p>

Bit	Bit Name	Initial Value	PCI R/W	Internal Bus R/W	Description
4, 3	PFS	00	R	R	<p>Phantom Function Supported</p> <p>Indicates the phantom function support status for transaction ID extension.</p> <p>00: The phantom function is not supported.</p> <p>01: The MSB of requester ID function number can be used for the phantom function.</p> <p>10: The upper two bits of requester ID function number can be used for the phantom function.</p> <p>11: All the three bits of requester ID function number can be used for the phantom function.</p> <p>This IP does not support the phantom function. Fixed to 0.</p>
2 to 0	MPSS	000	R	R/W	<p>Max Payload Size Supported</p> <p>Indicates the maximum payload size supported by the device.</p> <p>000: 128 bytes</p> <p>001: Reserved (setting prohibited)</p> <p>010: Reserved (setting prohibited)</p> <p>011: Reserved (setting prohibited)</p> <p>100: Reserved (setting prohibited)</p> <p>101: Reserved (setting prohibited)</p> <p>110: Reserved (setting prohibited)</p> <p>111: Reserved (setting prohibited)</p>



### 39.2.68 PCI Express Capability Register 2 (EXPCAP2)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

#### Common to Header TYPE00/01

- Device status register

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	TRPD	AUXPD TCD	URDTC D	FEDTC D	NFEDT CD	CEDTC D
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PCI R/W	R	R	R	R	R	R	R	R	R	R	R	R	RW1C	RW1C	RW1C	RW1C
Internal bus R/W	R	R	R	R	R	R	R	R	R	R	R	R	RW1C	RW1C	RW1C	RW1C

- Device control register

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	Max Read Request Size		ENSNP	AUXPP ME	PFE	ETAGE	Max Payload Size			ERLOD	URRPE	FERPE	NFERP E	CERPE	
Initial value:	0	0	1	0	1	0	0	0	0	0	0	1	0	0	0	0
PCI R/W	R	R/W	R/W	R/W	R/W	RWS	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Internal bus R/W	R	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	PCI R/W	Internal Bus R/W	Description
31 to 22	—	All 0	R	R	Reserved These bits are always read as 0. The write value should always be 0.
21	TRPD	0	R	R	Transaction Pending Indicates that there is a non-posted request not yet completed. 0: Non-posted request processing is not pending. 1: Non-posted request processing is pending. Non-posted requests issued are managed and the applicable value is reflected here.
20	AUXPDTCD	0	R	R	AUX Power Detected This field is fixed to 0 with this IP.
19	URDTC	0	RW1C	RW1C	Unsupported Request Detected Indicates the unsupported request detection status. 0: An unsupported request has not been detected. 1: An unsupported request has been detected. This field is set to 1 when an unsupported request is detected.
18	FEDTC	0	RW1C	RW1C	Fatal Error Detected Indicates the fatal error detection status. 0: A fatal error has not been detected. 1: A fatal error has been detected. This field is set to 1 when a fatal error is detected.

Bit	Bit Name	Initial Value	PCI R/W	Internal Bus R/W	Description
17	NFEDTCD	0	RW1C	RW1C	<p>Non-fatal Error Detected</p> <p>Indicates the non-fatal error detection status.</p> <p>0: A non-fatal error has not been detected.</p> <p>1: A non-fatal error has been detected.</p> <p>This field is set to 1 when a non-fatal error is detected.</p>
16	CEDTCD	0	RW1C	RW1C	<p>Correctable Error Detected</p> <p>Indicates the correctable error detection status.</p> <p>0: A correctable error has not been detected.</p> <p>1: A correctable error has been detected.</p> <p>This field is set to 1 when a correctable error is detected.</p>
15	Reserved	0	R	R	This bit is always read as 0. The write value should always be 0.
14 to 12	Max Read Request Size	010	R/W	R/W	<p>Max Read Request Size</p> <p>Indicates the maximum size of the read request that can be issued as the requester.</p> <p>000: 128 bytes max.</p> <p>001: 256 bytes max.</p> <p>010: 512 bytes max.</p> <p>011: 1024 bytes max.</p> <p>100: 2048 bytes max.</p> <p>101: 4096 bytes max.</p> <p>110: Reserved</p> <p>111: Reserved</p>
11	ENSNP	1	R/W	R/W	<p>Enable No Snoop</p> <p>Enables the device to issue the no-snoop transaction.</p> <p>0: The no-snoop transaction cannot be issued.</p> <p>1: The no-snoop transaction can be issued.</p>
10	AUXPPME	0	RWS	R/W	<p>AUX Power PM Enable</p> <p>Enables AUX power power management.</p> <p>0: AUX power power management is disabled.</p> <p>1: AUX power power management is enabled.</p> <p>Note: When the AUX power function is not implemented (when PMCAP0[24:22].AUX Current = 0), this bit is fixed to 0.</p>
9	PFE	0	R	R	<p>Phantom Function Enable</p> <p>Enables the phantom function.</p> <p>0: The phantom function is disabled.</p> <p>1: The phantom function is enabled.</p> <p>This IP does not support the phantom function.</p> <p>Fixed to 0.</p>

Bit	Bit Name	Initial Value	PCI R/W	Internal Bus R/W	Description
8	ETAGE	0	R/W	R/W	<p>Extended Tag Enable</p> <p>Enables the extension 8-bit tag ID function.</p> <p>0: The extension 8-bit tag ID function is disabled.</p> <p>1: The extension 8-bit tag ID function is enabled.</p> <p>This ID supports the extension 8-bit tag ID function.</p>
7 to 5	Max Payload Size	000	R/W	R/W	<p>Max Payload Size</p> <p>Indicates the maximum payload size for the device.</p> <p>000: 128 bytes max.</p> <p>001: 256 bytes max.</p> <p>010: 512 bytes max.</p> <p>011: 1024 bytes max.</p> <p>100: 2048 bytes max.</p> <p>101: 4096 bytes max.</p> <p>110: Reserved</p> <p>111: Reserved</p>
4	ERLOD	1	R/W	R/W	<p>Enabled Relax Ordering</p> <p>Enables the device to issue the relaxed ordering transaction.</p> <p>0: The relaxed ordering transaction cannot be issued.</p> <p>1: The relaxed ordering transaction can be issued.</p>
3	URRPE	0	R/W	R/W	<p>Unsupported Request Reporting Enable</p> <p>Enables the error message report on detection of an unsupported request.</p> <p>0: The FATAL_ERR or NONFATAL_ERR message is not transmitted on detection of an unsupported request.</p> <p>1: The FATAL_ERR or NONFATAL_ERR message is transmitted on detection of an unsupported request.</p>
2	FERPE	0	R/W	R/W	<p>Fatal Error Reporting Enable</p> <p>Enables the error message report on detection of a FATAL_ERR.</p> <p>0: The ERR_FATAL message is not transmitted on detection of a FATAL_ERR.</p> <p>1: The ERR_FATAL message is transmitted on detection of a FATAL_ERR.</p>
1	NFERPE	0	R/W	R/W	<p>Non-fatal Error Reporting Enable</p> <p>Enables the error message report on detection of a NON_FATAL_ERR.</p> <p>0: The ERR_NONFATAL message is not transmitted on detection of a NON_FATAL_ERR.</p> <p>1: The ERR_NONFATAL message is transmitted on detection of a NON_FATAL_ERR.</p>

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<b>Bit</b>	<b>Bit Name</b>	<b>Initial Value</b>	<b>PCI R/W</b>	<b>Internal Bus R/W</b>	<b>Description</b>
0	CERPE	0	R/W	R/W	Correctable Error Reporting Enable Enables the error message report on detection of a correctable error. 0: The ERR_COR message is not transmitted on detection of a correctable error. 1: The ERR_COR message is transmitted on detection of a correctable error.

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**39.2.69 PCI Express Capability Register 3 (EXPCAP3)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

**Common to Header TYPE00/01**

- Link capability register

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Port Number								—	—	LKBWN OTFCAP	DLLACT RPCAP	SDNERP CAP	CLKPM	L1ELAT	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
PCI R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Internal bus R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	L1ELAT	L0s Exit Latency			ASPM Supported		Maximum Link Width					Supported Link Speeds				
Initial value:	1	1	1	1	0	1	0	0	0	0	0	1	0	0	1	0
PCI R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Internal bus R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	PCI R/W	Internal Bus R/W	Description
31 to 24	Port Number	All 0	R	R/W	Port Number Indicates the port number of this PCI Express port. Specify the port number at initialization.
23, 22	—	All 0	R	R	Reserved These bits are always read as 0. The write value should always be 0.
21	LKBWNOTFCAP	0	R	R/W	Link Bandwidth Notification Capability Indicates whether or not the link bandwidth change report function is supported by EXPCAP4[30].LKBWMNGSTS or EXPCAP4[31].LKAUTOBWSTS. 0: The link bandwidth change report function is not supported. 1: The link bandwidth change report function is supported. • Root Port: To support this function, set 1 at initialization. • Endpoint: Use the initial value. Not need to be changed.

Bit	Bit Name	Initial Value	PCI R/W	Internal Bus R/W	Description
20	DLLACTRPCAP	0	R	R/W	<p>Data Link Layer Active Reporting Capable</p> <p>Indicates whether or not the Data Link Layer Active State can be indicated by EXPCAP4[29].DLLACT.</p> <p>0: The Data Link Layer Active State cannot be indicated. 1: The Data Link Layer Active State can be indicated.</p> <ul style="list-style-type: none"> <li>• Root Port: To support this function, set 1 at initialization.</li> <li>• Endpoint: Use the initial value. Not need to be changed.</li> </ul>
19	SDNERPCAP	0	R	R	<p>Surprise Down Error Reporting Capable</p> <p>Indicates that the Surprise Down error detection function is supported.</p> <p>0: The Surprise Down error detection function is not supported. 1: The Surprise Down error detection function is supported.</p> <p>This device does not support the Surprise Down error detection function. Fixed to 0.</p>
18	CLKPM	0	R	R/W	<p>Clock Power Management</p> <p>Indicates that the clock can be stopped when the link is in the L1, L2Ready, or L3Ready state.</p> <p>0: Clock cannot be stopped. 1: Clock can be stopped.</p> <p>Set the device function at initialization.</p> <p>Note: This field can be set with the device that conforms to the form factor supporting Clock Request Capability.</p>
17 to 15	L1ELAT	111	R	R/W	<p>L1 Exit Latency</p> <p>Indicates the L1 to L0 transition latency of the device.</p> <p>000: L0 recovery is completed in less than 1 <math>\mu</math>s. 001: L0 recovery is completed in 1 <math>\mu</math>s or more, but less than 2 <math>\mu</math>s. 010: L0 recovery is completed in 2 <math>\mu</math>s or more, but less than 4 <math>\mu</math>s. 011: L0 recovery is completed in 4 <math>\mu</math>s or more, but less than 8 <math>\mu</math>s. 100: L0 recovery is completed in 8 <math>\mu</math>s or more, but less than 16 <math>\mu</math>s. 101: L0 recovery is completed in 16 <math>\mu</math>s or more, but less than 32 <math>\mu</math>s. 110: L0 recovery is completed in 32 <math>\mu</math>s or more, but 64 <math>\mu</math>s or less. 111: L0 recovery is completed in more than 64 <math>\mu</math>s.</p> <p>Set the device condition at initialization.</p>

Bit	Bit Name	Initial Value	PCI R/W	Internal Bus R/W	Description
14 to 12	L0s Exit Latency	111	R	R/W	<p>L0s Exit Latency</p> <p>Indicates the L0s to L0 transition latency of the device.</p> <p>000: L0 recovery is completed in less than 64 ns.</p> <p>001: L0 recovery is completed in 64 ns or more, but less than 128 ns.</p> <p>010: L0 recovery is completed in 128 ns or more, but less than 256 ns.</p> <p>011: L0 recovery is completed in 256 ns or more, but less than 512 ns.</p> <p>100: L0 recovery is completed in 512 ns or more, but less than 1 <math>\mu</math>s.</p> <p>101: L0 recovery is completed in 1 <math>\mu</math>s or more, but less than 2 <math>\mu</math>s.</p> <p>110: L0 recovery is completed in 2 <math>\mu</math>s or more, but 4 <math>\mu</math>s or less.</p> <p>111: L0 recovery is completed in more than 4 <math>\mu</math>s.</p> <p>Set the device condition at initialization.</p>
11, 10	ASPM Supported	01	R	R	<p>ASPM Supported</p> <p>Indicates the ASPM support status.</p> <p>00: Reserved</p> <p>01: Supports L0s transition.</p> <p>10: Reserved</p> <p>11: Supports L0s and L1 transition (not supported with this IP).</p> <p>This IP only supports L0s transition.</p>
9 to 4	Maximum Link Width	H'01	R	R/W	<p>Maximum Link Width</p> <p>Indicates the maximum link width.</p> <p>H'00: Reserved</p> <p>H'01: x1 link</p> <p>H'02: x2 link (not supported)</p> <p>H'04: x4 link (not supported)</p> <p>H'08: x8 link (not supported)</p> <p>H'0C: x12 link (not supported)</p> <p>H'10: x16 link (not supported)</p> <p>H'20: x32 link (not supported)</p>
3 to 0	Supported Link Speeds	H'2	R	R/W	<p>Supported Link Speeds</p> <p>Indicates the maximum link speed.</p> <p>H'1: 2.5 GT/s</p> <p>H'2: 5.0 GT/s and 2.5 GT/s link speeds supported</p> <p>Other than above: Reserved</p>

### 39.2.70 PCI Express Capability Register 4 (EXPCAP4)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

#### Common to Header TYPE00/01

- Link status register

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	LKAUTO BWSTS	LKBWM NGSTS	DLLAC T	SLCLK CFG	LKTR	—	Negotiated Link Width					Current Link Speed				
Initial value:	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1
PCI R/W	-/R	-/R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Internal bus R/W	RW1C/R	RW1C/R	R	R/W	R	R	R	R	R	R	R	R	R	R	R	R

- Link control register

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	LKAUTO WINT	LKBWMN GINTE	HWAUTO WDIS	ECLKP M	EXTSY NC	CCLKC FG	RTRNL K	LKDIS	RCB	—	ASPM Control	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PCI R/W	R	R	R	R	-/R	-/R	R	R/W	R/W	R/W	R	R	R/W	R	R/W	R/W
Internal bus R/W	R	R	R	R	RW/R	RW/R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W

Bit	Bit Name	Initial Value	PCI R/W	Internal Bus R/W	Description
31	LKAUTOBWSTS	0	Root Port: —  Endpoint: R	Root Port: RW1C  Endpoint: R	<p>Link Autonomous Bandwidth Status</p> <ul style="list-style-type: none"> <li>Root Port: When a change of link bandwidth due to intentional factor is detected, 1 is set. This bit is cleared to 0 when 1 is written.</li> <li>Note: This field is only valid when EXCAP3[21].LKBWNOTFCAP is set to 1. If set to 0, this bit is fixed to 0.</li> <li>Endpoint: Use the initial value. Not need to be changed.</li> </ul>
30	LKBWMNGSTS	0	Root Port: —  Endpoint: R	Root Port: RW1C  Endpoint: R	<p>Link Bandwidth Management Status</p> <ul style="list-style-type: none"> <li>Root Port: When a change of link bandwidth due to reliability-related factor is detected, 1 is set. This bit is cleared to 0 when 1 is written.</li> <li>Note: This field is only valid when EXCAP3[21].LKBWNOTFCAP is set to 1. If set to 0, this bit is fixed to 0.</li> <li>Endpoint: Use the initial value. Not need to be changed.</li> </ul>
29	DLLACT	0	R	R	<p>Data Link Layer Active</p> <p>Indicates that DLCMSM is in the DL_ACTIVE state.</p> <p>0: Not in the DL_ACTIVE state 1: In the DL_ACTIVE state</p> <p>Note: This bit is only valid when EXCAP3[20].DLLACTRPCAP is set to 1. If set to 0, this bit is fixed to 0.</p>



Bit	Bit Name	Initial Value	PCI R/W	Internal Bus R/W	Description
28	SLCLKCFG	0	R	R/W	Slot Clock Configuration Indicates that the same reference clock as that supplied to the connector by the platform is used. 0: The same reference clock is not used. 1: The same reference clock is used.
27	LKTR	0	R	R	Link Training Indicates that link training by MAC LTSSM is in progress. • Root Port: Set to 1 when link training is in progress. • Endpoint: Fixed to 0.
26	—	0	R	R	Reserved This bit is always read as 0. The write value should always be 0.
25 to 20	Negotiated Link Width	H'04	R	R	Negotiated Link Width Indicates the link width determined by negotiation between links. H'01: x1 link width H'02: x2 link width H'04: x4 link width H'08: x8 link width H'0C: x12 link width H'10: x16 link width H'20: x32 link width This field value is undefined while a link is not established.
19 to 16	Current Link Speed	H'1	R	R	Current Link Speed Indicates the link speed determined by negotiation between links. H'1: 2.5 GT/s H'2: 5.0 GT/s
15 to 12	—	All 0	R	R	Reserved These bits are always read as 0. The write value should always be 0.
11	LKAUTOBWINT	0	Root Port: — Endpoint: R	Root Port: R/W Endpoint: R	Link Autonomous Bandwidth Interrupt Enable Enables generation of the interrupt by EXPCAP4[31].LKAUTOBWSTS. • Root Port: An interrupt is generated when LKAUTOBWSTS is 1. Note: This bit is only valid when EXCAP3[21].LKBMMNOTFCAP is set to 1. If set to 0, this bit is fixed to 0. • Endpoint: Use the initial value. Not need to be changed.

Bit	Bit Name	Initial Value	PCI R/W	Internal Bus R/W	Description
10	LKBWMNGINTE	0	Root Port: —  Endpoint: R	Root Port: R/W  Endpoint: R	<p>Link Bandwidth Management Interrupt Enable</p> <p>Enables generation of the interrupt by EXPCAP4[30].LKBWMNGSTS.</p> <ul style="list-style-type: none"> <li>• Root Port: Writing 1 to this bit sets it to 1, and enables generation of the interrupt when LKBWMNGSTS is 1.</li> </ul> <p>Note: This bit is only valid when EXCAP3[21].LKBMNOTFCAP is set to 1. If set to 0, this bit is fixed to 0.</p> <ul style="list-style-type: none"> <li>• Endpoint: Use the initial value. Not need to be changed.</li> </ul>
9	HWAUTOWDIS	0	R	R	<p>Hardware Autonomous Width Disable</p> <p>Disables autonomous change of link width by hardware except for the cases of poor link reliability.</p> <p>0: Autonomous change of link width by hardware is enabled.</p> <p>1: Autonomous change of link width by hardware is disabled.</p> <p>According to the standard, fixing this bit to 0 is allowed if hardware does not provide the autonomous link width changing mechanism.</p> <p>Since this IP does not provide the autonomous link width changing mechanism, this bit is fixed to 0.</p>
8	ECLKPM	0	R/W	R/W	<p>Enable Clock Power Management</p> <p>Enables the clock power management function.</p> <p>Note: This bit is only valid when EXCAP3[18].CLKPM is set to 1.</p> <p>If set to 0, this bit is fixed to 0.</p>
7	EXTSYNC	0	R/W	R/W	<p>Extended SYNC</p> <p>Transmits the ordered set when the MAC LTSSM makes a transition from L0s or in the recovery state.</p>
6	CCLKCFG	0	R/W	R/W	<p>Common Clock Configuration</p> <p>Indicates that the same clock is used by both ends of the link.</p>
5	RTRNLK	0	R	R/W	<p>Retrain Link</p> <p>Directs link retraining.</p> <p>Note: The read value is always 0.</p> <ul style="list-style-type: none"> <li>• Root Port: Write 1 to allow link retraining.</li> <li>• Endpoint: This bit is reserved. The write value should always be 0.</li> </ul>

Bit	Bit Name	Initial Value	PCI R/W	Internal Bus R/W	Description
4	LKDIS	0	R	R/W	<p>Link Disable</p> <p>Disables the link.</p> <ul style="list-style-type: none"> <li>• Root Port: Write 1 to disable the link.</li> <li>• Endpoint: This bit is reserved. The write value should always be 0.</li> </ul>
3	RCB	0	R/W	Root Port: R/W  Endpoint: R/W	<p>Read Completion Boundary</p> <p>Indicates the read completion boundary.</p> <p>0: 64-byte boundary 1: 128-byte boundary</p> <p>This field does not effect on the hardware. This IP divides a read completion only at 128-byte boundaries.</p>
2	Reserved	0	R	R	This bit is always read as 0. The write value should always be 0.
1, 0	ASPM Control	00	R/W	R/W	<p>ASPM Control</p> <p>Sets the ASPM support level.</p> <p>00: Disabled 01: L0s transition enabled 10: L1 transition enabled (setting prohibited) 11: L0s/L1 transition enabled (setting prohibited)</p>

### 39.2.71 PCI Express Capability Register 5 (EXPCAP5)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

#### Header TYPE00

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PCI R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Internal bus R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PCI R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Internal bus R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	PCI R/W	Internal Bus R/W	Description
31 to 0	—	All 0	R	R	Reserved
These bits are always read as 0. The write value should always be 0.					

#### Header TYPE01

- Slot capabilities register

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Physical Slot Number													NOCCS P	EMLKP RS	SLPLS C
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal bus R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SLPLS C	Slot Power Limit Value								HOTPL GCAP	HOTPL GSPR	PWIND PRS	ATIND PRS	MRLSE NPRS	PWCO NPRS	ATBTN PRS
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal bus R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	Internal Bus R/W	Description
31 to 19	Physical Slot Number	All 0	R	Physical Slot Number
According to the PCI standard, indicates the physical slot number connected to the device.				
This field is invalid with this IP.				

Bit	Bit Name	Initial Value	Internal Bus R/W	Description
18	NOCCSP	0	R	<p>No Command Complete Support</p> <p>According to the PCI standard, indicates that completion of a Hot Plug command is not to be reported.</p> <p>0: Upon completion of a Hot Plug command, it is reported.</p> <p>1: Upon completion of a Hot Plug command, it is not reported.</p> <p>This field is invalid with this IP.</p>
17	EMLKPRS	0	R	<p>Electro Mechanical Interlock Present</p> <p>According to the PCI standard, indicates that Electromechanical Interlock is provided for the slot.</p> <p>This field is invalid with this IP.</p>
16, 15	SLPLSC	00	R	<p>Slot Power Limit Scale</p> <p>According to the PCI standard, indicates the scale for slot power limit value.</p> <p>00: 1.0x 01: 0.1x 10: 0.01x 11: 0.001x</p> <p>This field is invalid with this IP.</p>
14 to 7	Slot Power Limit Value	All 0	R	<p>Slot Power Limit Value</p> <p>According to the PCI standard, indicates the upper limit of slot power supplied by the slot power supply in Watts.</p> <p>This field is invalid with this IP.</p>
6	HOTPLGCAP	0	R	<p>Hot Plug Capable</p> <p>According to the PCI standard, indicates the Hot Plug support status in this slot.</p> <p>This field is invalid with this IP.</p>
5	HOTPLGSPR	0	R	<p>Hot Plug Surprise</p> <p>According to the PCI standard, indicates that the adapter inserted to this slot can be unplugged without advance notice.</p> <p>This field is invalid with this IP.</p>
4	PWINDPRS	0	R	<p>Power Indicator Present</p> <p>According to the PCI standard, indicates that the power indicator is provided.</p> <p>This field is invalid with this IP.</p>
3	ATINDPRS	0	R	<p>Attention Indicator Present</p> <p>According to the PCI standard, indicates that the attention indicator is provided.</p> <p>This field is invalid with this IP.</p>
2	MRLSENPRS	0	R	<p>MRL Sensor Present</p> <p>According to the PCI standard, indicates that the MRL sensor is provided.</p> <p>This field is invalid with this IP.</p>

Bit	Bit Name	Initial Value	Internal Bus R/W	Description
1	PWCONPRS	0	R	Power Controller Present According to the PCI standard, indicates that the power controller is provided. This field is invalid with this IP.
0	ATBTNPRS	0	R	Attention Button Present According to the PCI standard, indicates that the attention button is provided. This field is invalid with this IP.

### 39.2.72 PCI Express Capability Register 6 (EXPCAP6)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

#### Header TYPE00

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PCI R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Internal bus R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PCI R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Internal bus R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	PCI R/W	Internal Bus R/W	Description
31 to 0	—	All 0	R	R	Reserved These bits are always read as 0. The write value should always be 0.

**Header TYPE01**

## • Slot status register

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	DLLST CHG	EMLKS TS	PRDET ST	MRLSE NST	COMC PL	PRDET CHG	MRLSE NCHG	PWFAL DET	ATBTN PRES
Initial value:	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
Internal bus R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

## • Slot control register

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	DLLSTC HGE	EMLKC ON	PWCON CON	PWINDCON	ATINDCON	HOTPLG INTE	COMCP LINTE	PRDETC HGE	MRLSEN CHGE	PWFALD ETE	ATBTN RESE		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Internal bus R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	

Bit	Bit Name	Initial Value	Internal Bus R/W	Description
31 to 25	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
24	DLLSTCHG	0	R	Data Link Layer ST Changed According to the PCI standard, indicates that the EXPCAP4[29].DLLACT has changed. This field is invalid with this IP.
23	EMLKSTS	0	R	Electro Mechanical Interlock Status According to the PCI standard, indicates the Electromechanical Interlock state. 0: Not locked by Electromechanical Interlock. 1: Locked by Electromechanical Interlock This field is invalid with this IP.
22	PRDETST	1	R	Presence Detect State According to the PCI standard, indicates that the adapter is inserted in the slot. 0: The slot is empty. 1: The adapter is inserted in the slot. This field is invalid with this IP.
21	MRLSENST	0	R	MRL Sensor State According to the PCI standard, indicates the MRL sensor state. 0: MRL is open. 1: MRL is closed. This field is invalid with this IP.

Bit	Bit Name	Initial Value	Internal Bus R/W	Description
20	COMCPL	0	R	<p>Command Completed</p> <p>According to the PCI standard, indicates that the Hot Plug command has been completed when EXPCAP5[18].NOCCSP = 0.</p> <p>0: The Hot Plug command is being executed. 1: The Hot Plug command execution has been completed.</p> <p>This field is invalid with this IP.</p>
19	PRDETCHG	0	R	<p>Presence Detect Changed</p> <p>According to the PCI standard, indicates that the EXPCAP6[22].PRDETST has changed.</p> <p>This field is invalid with this IP.</p>
18	MRLSENCHG	0	R	<p>MRL Sensor Changed</p> <p>According to the PCI standard, indicates that the EXPCAP6[21].MRLSENST has changed.</p> <p>This field is invalid with this IP.</p>
17	PWFALDET	0	R	<p>Power Fault Detect</p> <p>According to the PCI standard, indicates that the power fault has been detected.</p> <p>This field is invalid with this IP.</p>
16	ATBTNPRES	0	R	<p>Attention Button Pressed</p> <p>According to the PCI standard, indicates that the attention button has been pressed.</p> <p>This field is invalid with this IP.</p>
15 to 13	—	All 0	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>
12	DLLSTCHGE	0	R	<p>Data Link Layer State Change Enable</p> <p>According to the PCI standard, enables the setting of PCIEXP6[24].DLLSTCHG.</p> <p>This field is invalid with this IP.</p>
11	EMLKCON	0	R	<p>Electro Mechanical Interlock Control</p> <p>According to the PCI standard, toggles the state of Electromechanical Interlock.</p> <p>This field is invalid with this IP.</p>
10	PWCONCON	0	R	<p>Power Controller Control</p> <p>According to the PCI standard, controls the power controller.</p> <p>0: Power Off 1: Power On</p> <p>This field is invalid with this IP.</p>



Bit	Bit Name	Initial Value	Internal Bus R/W	Description
9, 8	PWINDCON	00	R	<p>Power Indicator Control</p> <p>According to the PCI standard, controls the power indicator.</p> <p>00: Reserved</p> <p>01: On</p> <p>10: Blink</p> <p>11: Off</p> <p>This field is invalid with this IP.</p>
7, 6	ATINDCON	00	R	<p>Attention Indicator Control</p> <p>According to the PCI standard, controls the attention indicator.</p> <p>00: Reserved</p> <p>01: On</p> <p>10: Blink</p> <p>11: Off</p> <p>This field is invalid with this IP.</p>
5	HOTPLGINTE	0	R	<p>Hot Plug Interrupt Enable</p> <p>According to the PCI standard, enables MSI generation upon Hot Plug.</p>
4	COMCPLINTE	0	R	<p>Command Completed Interrupt Enable</p> <p>According to the PCI standard, enables MSI generation upon Command Complete.</p> <p>This field is invalid with this IP.</p>
3	PRDETCHE	0	R	<p>Presence Detect Changed Enable</p> <p>According to the PCI standard, enables MSI generation by PRDETCHEG.</p> <p>This field is invalid with this IP.</p>
2	MRLSENCHGE	0	R	<p>MRL Sensor Changed Enable</p> <p>According to the PCI standard, enables MSI generation by MRLSENCHG.</p> <p>This field is invalid with this IP.</p>
1	PWFALDETE	0	R	<p>Power Fault Detect Enable</p> <p>According to the PCI standard, enables MSI generation by PWFALDET.</p> <p>This field is invalid with this IP.</p>
0	ATBTNPRES	0	R	<p>Attention Button Pressed Enable</p> <p>According to the PCI standard, enables MSI generation by ATBTNPRES.</p> <p>This field is invalid with this IP.</p>

### 39.2.73 PCI Express Capability Register 7 (EXPCAP7)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

#### Header TYPE00

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PCI R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Internal bus R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PCI R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Internal bus R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	PCI R/W	Internal Bus R/W	Description
31 to 0	—	All 0	R	R	Reserved These bits are always read as 0. The write value should always be 0.

#### Header TYPE01

- Root capabilities register

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal bus R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

- Root control register

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal bus R/W	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	Internal Bus R/W	Description
31 to 17	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
16	CRSVIS	0	RW	CRS Software Visibility Indicates whether Root Port has the function of returning Configuration Retry Status to the upper software. Set the device function at initialization.

Bit	Bit Name	Initial Value	Internal Bus R/W	Description
15 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	CRSVISE	0	RW	CRS Software Visibility Enable Enables Root Port to return Configuration Retry Status to the upper software. Before setting this bit to 1, the CRSVIS bit should be set. If these bits are set at the same time, CRSVISE is not set to 1. Setting this bit to 1 changes Configuration access behavior. For details, see section 39.3.2, Configuration Cycle.
3	PMEINTE	0	RW	PME Interrupt Enable Enables Root Port to generate the interrupt to the upper software upon reception of a PME message. 0: If a PM_PME has been received when another PM_PME is received, EXPCAP8[15:0].PME_RequesterID is overwritten. 1: If a PM_PME has been received when another PM_PME is received, EXPCAP8[15:0].PM_RequesterID is not overwritten. PM_RequesterID of the PM_PME received later is placed in the pending state. At this time, all the receive operations are stopped. Thus, always clear EXPCAP8[16].PMEST.
2	SERRFEE	0	RW	System Error on Fatal Error Enable Enables Root Port to generate the interrupt to the upper software upon reception of an ERR_FATAL message or occurrence of an error reported by Root Port itself.
1	SERRNFEE	0	RW	System Error on Non-fatal Error Enable Enables Root Port to generate the interrupt to the upper software upon reception of an ERR_NONFATAL message or occurrence of an error reported by Root Port itself.
0	SERRCEE	0	RW	System Error on Correctable Error Enable Enables Root Port to generate the interrupt to the upper software upon reception of an ERR_COR message or occurrence of an error reported by Root Port itself.

## 39.2.74 PCI Express Capability Register 8 (EXPCAP8)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

## Header TYPE00

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PCI R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Internal bus R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PCI R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Internal bus R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	PCI R/W	Internal Bus R/W	Description
31 to 0	—	All 0	R	R	Reserved These bits are always read as 0. The write value should always be 0.

## Header TYPE01

- Root status register

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PMEPD	PMEST
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal bus R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	RW1C

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PME Requester ID															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal bus R/W	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	Internal Bus R/W	Description
31 to 18	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
17	PMEPD	0	R	PME Pending Indicates that another PME is pending when this bit is 1. If the PME status is cleared by the upper software with PMEPD = 1 and PMEST = 1, PMEST is set to 1 again and the pending requester ID is set in the PME Requester ID bits.

Bit	Bit Name	Initial Value	Internal Bus R/W	Description
16	PMEST	0	RW1C	PME Status Indicates that PME has been received from the requester indicated by the PME Requester ID bits. This bit is set to 1 when the PME is received and cleared to 0 when the upper software writes 1 to this bit.
15 to 0	PME Requester ID	All 0	R	PME Requester ID Indicates the requester ID having issued the PME. This field sets the requester ID on reception of PME.

### 39.2.75 PCI Express Capability Register 9 (EXPCAP9)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

#### Common to Header TYPE00/01

- Device capabilities 2 register

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PCI R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Internal bus R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	ARIFWD SUP	CPLTOD ISSUP	Completion Timeout Range Supported			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
PCI R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Internal bus R/W	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R	R

Bit	Bit Name	Initial Value	PCI R/W	Internal Bus R/W	Description
31 to 6	—	All 0	R	R	Reserved These bits are always read as 0. The write value should always be 0.
5	ARIFWDSUP	0	R	R	ARI Forwarding Support Indicates the ARI Forwarding support status. <ul style="list-style-type: none"> <li>Root Port: This IP does not support the ARI Forwarding. Fixed to 0.</li> <li>Endpoint: Fixed to 0.</li> </ul>
4	CPLTODISSUP	1	R	R/W	Completion Timeout Disable Supported Indicates the Completion Timeout Disable function support status. <ul style="list-style-type: none"> <li>0: The Completion Timeout Disable function is not supported.</li> <li>1: The Completion Timeout Disable function is supported. This IP supports the Completion Timeout Disable function.</li> </ul>

Bit	Bit Name	Initial Value	PCI R/W	Internal Bus R/W	Description
3 to 0	Completion Timeout Range Supported	H'0	R	R	<p>Completion Timeout Range Supported</p> <p>Indicates the Completion Timeout Range support status.</p> <p>Timeout range specified by the standard:</p> <p>Range A: 50 <math>\mu</math>s to 10 ms</p> <p>Range B: 10 ms to 250 ms</p> <p>Range C: 250 ms to 4 s</p> <p>Range D: 4 s to 64 s</p> <p>Supported ranges:</p> <p>H'0: Setting the timeout value is prohibited (fixed).</p> <p>H'1: Range A</p> <p>H'2: Range B</p> <p>H'3: Range A and B</p> <p>H'6: Range B and C</p> <p>H'7: Range A, B and C</p> <p>H'E: Range B, C and D</p> <p>H'F: Range A, B, C and D</p> <p>Other than above: Reserved</p> <p>This IP does not support the timeout value setting.</p>

### 39.2.76 PCI Express Capability Register 10 (EXPCAP10)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

#### Common to Header TYPE00/01

- Device status 2 register

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PCI R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Internal bus R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

- Device control 2 register

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	ARIFW DE	CPLTO DIS	Completion Timeout Value			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PCI R/W	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R	R
Internal bus R/W	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R	R

Bit	Bit Name	Initial Value	PCI R/W	Internal Bus R/W	Description
31 to 6	—	All 0	R	R	Reserved These bits are always read as 0. The write value should always be 0.
5	ARIFWDE	0	R	R	ARI Forwarding Enable Enables the ARI Forwarding. <ul style="list-style-type: none"> <li>Root Port: This IP does not support the ARI Forwarding. Fixed to 0.</li> <li>Endpoint: Fixed to 0.</li> </ul>
4	CPLTODIS	0	RW	RW	Completion Timeout Disable Sets the Completion Timeout Disable function. 0: The Completion Timeout Disable function is disabled. 1: The Completion Timeout Disable function is enabled. This bit is fixed to 0 when EXPCAP9[4]. Completion Timeout Disable Supported is 0.



Bit	Bit Name	Initial Value	PCI R/W	Internal Bus R/W	Description
3 to 0	Completion Timeout Value	H'0	R	R	<p>Completion Timeout Value</p> <p>Sets the Completion Timeout value.</p> <p>H'0: Default Range 50 <math>\mu</math>s to 50 ms (fixed)</p> <p>Value of TLCTLR.Default Completion Timeout Time</p> <p>H'1: 50 <math>\mu</math>s to 100 <math>\mu</math>s (not supported)</p> <p>H'2: 1 ms to 10 ms (not supported)</p> <p>H'5: 16 ms to 55 ms (not supported)</p> <p>H'6: 65 ms to 210 ms (not supported)</p> <p>H'9: 260 ms to 900 ms (not supported)</p> <p>H'A: 1 s to 3.5 s (not supported)</p> <p>H'C: 4 s to 13 s (not supported)</p> <p>H'D: 17 s to 64 s (not supported)</p> <p>Other than above: Reserved</p> <p>This IP does not support the timeout value setting.</p>

### 39.2.77 PCI Express Capability Register 11 (EXPCAP11)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

#### Common to Header TYPE00/01

- Link capabilities 2 register

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PCI R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Internal bus R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PCI R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Internal bus R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	PCI R/W	Internal Bus R/W	Description
31 to 0	—	All 0	R	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>

### 39.2.78 PCI Express Capability Register 12 (EXPCAP12)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

#### Common to Header TYPE00/01

- Link status 2 register

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CURDEEMLEV
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
PCI R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Internal bus R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

- Link control 2 register

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	CMPDEEM	CMPSOS	ETMDFCMP	Transmit Margin			SELDEEM	HWATSPDIS	ENTCMP	Target Link Speed			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
PCI R/W	R	R	R	RWS	RWS	RWS	RWS	RWS	RWS	R	R	RWS	RWS	RWS	RWS	RWS
Internal bus R/W	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	PCI R/W	Internal Bus R/W	Description
31 to 17	—	All 0	R	R	Reserved These bits are always read as 0. The write value should always be 0.
16	CURDEEMLEV	1	R	R	Current De-emphasis Level Indicates the current de-emphasis level during 5-GT/s link operation. 0: -6 dB 1: -3.5 dB The value is undefined during 2.5-GT/s operation.
15 to 13	—	All 0	R	R	Reserved These bits are always read as 0. The write value should always be 0.
12	CMPDEEM	0	RWS	R/W	Compliance De-emphasis Specifies the de-emphasis level when setting EXPCAP12[4].ENTCMP bit to 1 causes LTSSM to be placed in Polling.Compliance mode. 0: -6 dB 1: -3.5 dB The value is undefined during 2.5-GT/s operation.
11	CMPSOS	0	RWS	R/W	Compliance SOS When this bit is 1, LTSSM periodically inserts the SKP ordered set between compliance patterns. 0: The SKP ordered set is not periodically inserted. 1: The SKP ordered set is periodically inserted.

Bit	Bit Name	Initial Value	PCI R/W	Internal Bus R/W	Description
10	ETMDFCMP	0	RWS	R/W	<p>Enter Modified Compliance</p> <p>When this bit is 1, LTSSM transmits modified compliance patterns on transition to the Polling.Compliance state.</p> <p>0: Normal compliance patterns are used.</p> <p>1: Modified compliance patterns are used.</p>
9 to 7	Transmit Margin	000	RWS	R/W	<p>Transmit Margin</p> <p>Sets the signal level without de-emphasis.</p> <p>000: Normal signal level</p> <p>001: 800 to 1200 mV for full swing, 400 to 700 mV for half swing</p> <p>010-(n-1): n is specified by PHY (<math>3 \leq n \leq 7</math>).</p> <p>n-111: Reserved</p> <p>Determine n according to the PHY specification.</p> <p>Do not set the value exceeding the PHY specification.</p>
6	SELDEEM	0	R	R/W	<p>Selectable De-emphasis</p> <p>Indicates the de-emphasis level during 5-GT/s upstream component operation.</p> <ul style="list-style-type: none"> <li>Root Port: Set a value appropriate for the PHY at initialization.</li> </ul> <p>0: -6 dB</p> <p>1: -3.5 dB</p> <ul style="list-style-type: none"> <li>Endpoint: Fixed to 0.</li> </ul>
5	HWATSPDIS	0	R	R	<p>Hardware Autonomous Speed Disable</p> <p>Disables autonomous change of link width by hardware except for the cases of poor reliability.</p> <p>0: Autonomous change of link width by hardware is enabled.</p> <p>1: Autonomous change of link width by hardware is disabled.</p> <p>According to the standard, fixing this bit to 0 is allowed if hardware does not provide the autonomous link width changing mechanism.</p> <p>Since this IP does not provide the autonomous link width changing mechanism, this bit is fixed to 0. The write value should always be 0.</p>
4	ENTCMP	0	RWS	R/W	<p>Enter Compliance</p> <p>Setting this bit of both ends of the link forcibly places a link into compliance mode at the specified speed.</p> <p>Used to set compliance mode.</p>

Bit	Bit Name	Initial Value	PCI R/W	Internal Bus R/W	Description
3 to 0	Target Link Speed	0010	RWS	R/W	Target Link Speed <ul style="list-style-type: none"> <li>• Root Port: Specifies the upper limit speed that is conveyed to the communication peer during link training. Also, specifies the speed in compliance mode. 0001: 2.5 GT/s 0010: 5.0 GT/s</li> <li>• Endpoint: Specifies the speed in compliance mode. 0001: 2.5 GT/s 0010: 5.0 GT/s</li> </ul>

### 39.2.79 PCI Express Capability Register 13 (EXPCAP13)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

#### Common to Header TYPE00/01

- Slot capabilities 2 register

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PCI R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Internal bus R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PCI R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Internal bus R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	PCI R/W	Internal Bus R/W	Description
31 to 0	—	All 0	R	R	Reserved  These bits are always read as 0. The write value should always be 0.

### 39.2.80 PCI Express Capability Register 14 (EXPCAP14)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

#### Common to Header TYPE00/01

- Slot status 2 register

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PCI R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Internal bus R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

- Slot control 2 register

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PCI R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Internal bus R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	PCI R/W	Internal Bus R/W	Description
31 to 16	—	All 0	R	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 0	—	All 0	R	R	Reserved These bits are always read as 0. The write value should always be 0.

### 39.2.81 VC Capability Register 0 (VCCAP0)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

- Virtual channel enhanced capability header

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Next Capability Offset												Capability Version			
Initial value:	0	0	0	1	1	0	1	1	0	0	0	0	0	0	0	1
PCI R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Internal bus R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PCI Express Extended Capability ID															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
PCI R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Internal bus R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	PCI R/W	Internal Bus R/W	Description
31 to 20	Next Capability Offset	H'1B0	R	R/W	Next Capability Offset Pointer to the capability list Points to the pointer to Device Serial Number Capability, H'1B0.
19 to 16	Capability Version	H'1	R	R	Capability Version Indicates the version of this capability.
15 to 0	PCI Express Extended Capability ID	H'0002	R	R	PCI Express Extended Capability ID Indicates the ID of this capability.

### 39.2.82 VC Capability Register 1 (VCCAP1)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

- Port VC capability register 1

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PCI R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Internal bus R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	PT ARBTBL SIZE		REFCLK	—		LPEXTVC		—		EXT VC		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PCI R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Internal bus R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	PCI R/W	Internal Bus R/W	Description
31 to 12	—	All 0	R	R	Reserved These bits are always read as 0. The write value should always be 0.
11, 10	PT ARBTBL SIZE	00	R	R	Port Arbitration Table entry Size Indicates the size of port arbitration table entry. This IP does not support port arbitration.
9, 8	REFCLK	00	R	R	Reference Clock Indicates the reference clock for Time Base WRR port arbitration. This IP does not support port arbitration.
7	—	0	R	R	Reserved This bit is always read as 0. The write value should always be 0.
6 to 4	LPEXTVC	000	R	R	Low Priority Extended VC Count Indicates the low priority VC count except the default VC0. With this IP, only VC0 is a low priority VC.
3	—	0	R	R	Reserved This bit is always read as 0. The write value should always be 0.
2 to 0	EXT VC	000	R	RW	Extended VC Count Indicates the VC count except the default VC0. The write value should always be 0.

### 39.2.83 VC Capability Register 2 (VCCAP2)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

- Port VC capability register 2

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	VC Arbitration Table Offset												—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PCI R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Internal bus R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	VCARB WRR128	VCARB WRR64	VCARB WRR32	VCARB FIX
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PCI R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Internal bus R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	PCI R/W	Internal Bus R/W	Description
31 to 24	VC Arbitration Table Offset	All 0	R	R	VC Arbitration Table Offset Indicates the position of VC arbitration. This IP does not provide VC arbitration based on the table.
23 to 4	—	All 0	R	R	Reserved These bits are always read as 0. The write value should always be 0.
3	VCARBWRR128	0	R	R	VC Arbitration WRR 128 Phase Indicates that Weighted Round Robin 128 Phase is applied to VC arbitration of Low Priority Group VC. This IP does not support this function.
2	VCARB WRR64	0	R	R	VC Arbitration WRR 64 Phase Indicates that Weighted Round Robin 64 Phase is applied to VC arbitration of Low Priority Group VC. This IP does not support this function.
1	VCARB WRR32	0	R	R	VC Arbitration WRR 32 Phase Indicates that Weighted Round Robin 32 Phase is applied to VC arbitration of Low Priority Group VC. This IP does not support this function.
0	VCARB FIX	0	R	R	VC Arbitration Hardware Fixed Indicates that HardWareFix scheme is applied to VC arbitration of Low Priority Group VC. This IP does not support this function.



### 39.2.84 VC Capability Register 3 (VCCAP3)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

- Port VC status register

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VCARB TBLST
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PCI R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Internal bus R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

- Port VC control register

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	VC Arbitration Select			LDVCA RBTBL
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PCI R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Internal bus R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	PCI R/W	Internal Bus R/W	Description
31 to 17	—	All 0	R	R	Reserved These bits are always read as 0. The write value should always be 0.
16	VCARB TBLST	0	R	R	VC Arbitration Table Status Indicates the VC arbitration table status. This IP does not provide VC arbitration based on the table.
15 to 4	—	All 0	R	R	Reserved These bits are always read as 0. The write value should always be 0.
3 to 1	VC Arbitration Select	000	R	R	VC Arbitration Select Selects the VC arbitration method for Low Priority Group VC. This IP does not provide VC arbitration.
0	LDVCARB TBL	0	R	R	Load VC Arbitration Table Loads the VC arbitration table. This IP does not provide VC arbitration.

### 39.2.85 VC Capability Register 4 (VCCAP4)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

This register is used to make settings for the VC0.

- VC resource capability register

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Port Arbitration Table Offset								—	Maximum Time Slot						
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PCI R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Internal bus R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RJCTS NPTR	—	—	—	—	—	—	—	—	—	PTARB WRR256	PTARB WRR128	PTARB WRR128	PTARB WRR64	PTARB WRR32	PTARB FIX
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PCI R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Internal bus R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	PCI R/W	Internal Bus R/W	Description
31 to 24	Port Arbitration Table Offset	All 0	R	R	Port Arbitration Table Offset Indicates that the offset address to the port arbitration table. VC0 does not have the port arbitration table.
23	—	0	R	R	Reserved This bit is always read as 0. The write value should always be 0.
22 to 16	Maximum Time Slot	All 0	R	R	Maximum Time Slot Indicates the maximum time slot in port arbitration according to Time Based WRR. VC0 does not provide the WRR port arbitration.
15	RJCTSNPTR	0	R	R/W	Reject Snoop Transactions Indicates that snoop transactions are rejected. <ul style="list-style-type: none"> <li>Root Port: Set the VC condition at initialization.</li> <li>Endpoint: The write value should always be 0.</li> </ul>
14 to 6	—	All 0	R	R	Reserved These bits are always read as 0. The write value should always be 0.
5	PTARBWRR256	0	R	R	Port Arbitration WRR256 Indicates that Weighted Round Robin 256 Phase is applied to port arbitration. This IP does not support port arbitration.

Bit	Bit Name	Initial Value	PCI R/W	Internal Bus R/W	Description
4	PTARBTBWRR128	0	R	R	Port Arbitration Time Base WRR128 Indicates that Time Base Weighted Round Robin 128 Phase is applied to port arbitration. This IP does not support port arbitration.
3	PTARBWRR128	0	R	R	Port Arbitration WRR128 Indicates that Weighted Round Robin 128 Phase is applied to port arbitration. This IP does not support port arbitration.
2	PTARBWRR64	0	R	R	Port Arbitration WRR64 Indicates that Weighted Round Robin 64 Phase is applied to port arbitration. This IP does not support port arbitration.
1	PTARBWRR32	0	R	R	Port Arbitration WRR32 Indicates that Weighted Round Robin 32 Phase is applied to port arbitration. This IP does not support port arbitration.
0	PTARBFIX	0	R	R	Port Arbitration Hardware Fixed Indicates that HardWareFix scheme is applied to port arbitration. This IP does not support port arbitration.

### 39.2.86 VC Capability Register 5 (VCCAP5)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

This register is used to make settings for the VC0.

- VC resource control register

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	VC Enable	—	—	—	—	VCID			—	—	—	—	Port Arbitration Select			LDPTA RBTBL
Initial value:	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PCI R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Internal bus R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	TC7	TC6	TC5	TC4	TC3	TC2	TC1	TC0
Initial value:	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
PCI R/W	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
Internal bus R/W	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R

Bit	Bit Name	Initial Value	PCI R/W	Internal Bus R/W	Description
31	VC Enable	1	R	R	VC Enable Indicates that VC is enabled. 0: VC0 is disabled. 1: VC0 is enabled. VC0 is always enabled.
30 to 27	—	All 0	R	R	Reserved These bits are always read as 0. The write value should always be 0.
26 to 24	VCID	All 0	R	R	VCID Indicates the VC ID. VC0 is always 0.
23 to 20	—	All 0	R	R	Reserved These bits are always read as 0. The write value should always be 0.
19 to 17	Port Arbitration Select	All 0	R	R	Port Arbitration Select Selects the port arbitration method. This IP does not support port arbitration.
16	LDPTARBTL	0	R	R	Load Port Arbitration Table Loads the port arbitration table. This IP does not support port arbitration.
15 to 8	—	All 0	R	R	Reserved These bits are always read as 0. The write value should always be 0.
7	TC7	1	R/W	R/W	TC7 Maps TC7 into VC0. All the TCs are mapped into VC0 by default.

Bit	Bit Name	Initial Value	PCI R/W	Internal Bus R/W	Description
6	TC6	1	R/W	R/W	TC6 Maps TC6 into VC0. All the TCs are mapped into VC0 by default.
5	TC5	1	R/W	R/W	TC5 Maps TC5 into VC0. All the TCs are mapped into VC0 by default.
4	TC4	1	R/W	R/W	TC4 Maps TC4 into VC0. All the TCs are mapped into VC0 by default.
3	TC3	1	R/W	R/W	TC3 Maps TC3 into VC0. All the TCs are mapped into VC0 by default.
2	TC2	1	R/W	R/W	TC2 Maps TC2 into VC0. All the TCs are mapped into VC0 by default.
1	TC1	1	R/W	R/W	TC1 Maps TC1 into VC0. All the TCs are mapped into VC0 by default.
0	TC0	1	R	R	TC0 Maps TC0 into VC0. TC0 is always mapped into VC0.

### 39.2.87 VC Capability Register 6 (VCCAP6)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

This register is used to make settings for the VC0.

- VC resource status register

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VCNGPD	PTARB TBLST
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
PCI R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Internal bus R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PCI R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Internal bus R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	PCI R/W	Internal Bus R/W	Description
31 to 18	—	All 0	R	R	Reserved These bits are always read as 0. The write value should always be 0.
17	VCNGPD	1	R	R	VC Negotiation Pending Indicates that VC0 is in the negotiation processing. 0: The VC0 negotiation processing is not in progress. 1: The VC0 negotiation processing is in progress.
16	PTARB TBLST	0	R	R	Port Arbitration Table Indicates the port arbitration table status. This IP does not provide port arbitration based on the table.
15 to 0	—	All 0	R	R	Reserved These bits are always read as 0. The write value should always be 0.

### 39.2.88 Device Serial Number Capability Register 0 (SERNUMCAP0)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

- Device serial number enhanced capability header

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Next Capability Offset												Capability Version			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
PCI R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Internal bus R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PCI Express Extended Capability ID															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
PCI R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Internal bus R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	PCI R/W	Internal Bus R/W	Description
31 to 20	Next Capability Offset	H'000	R	R/W	Next Capability Offset Pointer to the capability list. Indicates H'000, which is End Of List.
19 to 16	Capability Version	H'1	R	R	Capability Version Indicates the version of this capability.
15 to 0	PCI Express Extended Capability ID	H'0003	R	R	PCI Express Extended Capability ID Indicates the ID of this capability.

**39.2.89 Device Serial Number Capability Register 1 (SERNUMCAP1)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Device Serial Number 1st																
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PCI R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Internal bus R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Device Serial Number 1st																
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PCI R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Internal bus R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	PCI R/W	Internal Bus R/W	Description
31 to 0	Device Serial Number 1st	All 0	R	R	Device Serial Number 1st Indicates the serial number of the device. This field reflects the value of the DSERSETR0 field.

**39.2.90 Device Serial Number Capability Register 2 (SERNUMCAP2)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Device Serial Number 2 <sup>nd</sup> 1																
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PCI R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Internal bus R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

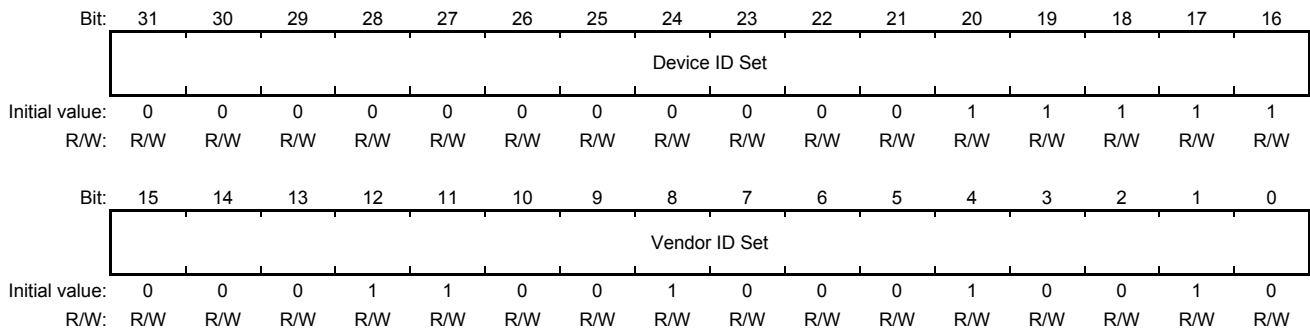
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Device Serial Number 2nd																
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PCI R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Internal bus R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	PCI R/W	Internal Bus R/W	Description
31 to 0	Device Serial Number 2nd	All 0	R	R	Device Serial Number 2nd Indicates the serial number of the device. This field reflects the value of the DSERSETR1 field.



**39.2.91 ID Setting Register 0 (IDSETR0)**

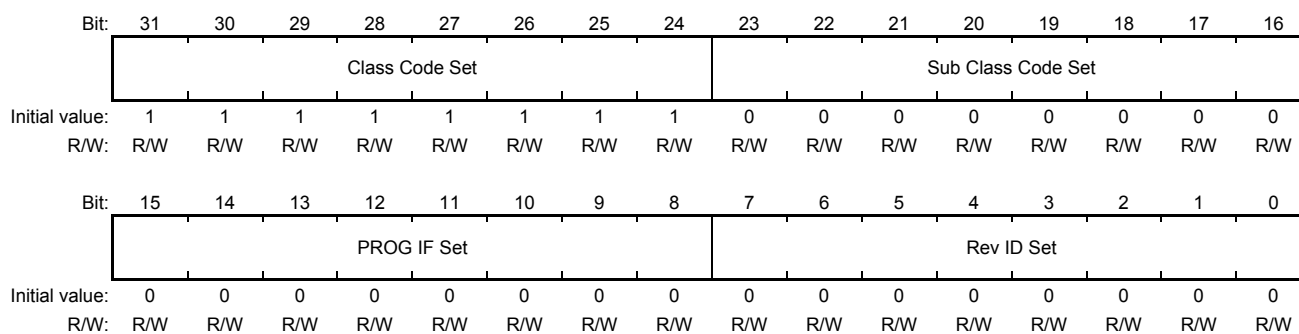
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—



Bit	Bit Name	Initial Value	R/W	Description
31 to 16	Device ID Set	H'001F	R/W	Device ID Set Indicates the device ID. The value of this field is reflected to PCICONF0[31:16].Device ID.
15 to 0	Vendor ID Set	H'1912	R/W	Vendor ID Set Indicates the PCI device vendor ID. The value of this field is reflected to PCICONF0[15:0].Vendor ID.

### 39.2.92 ID Setting Register 1 (IDSETR1)

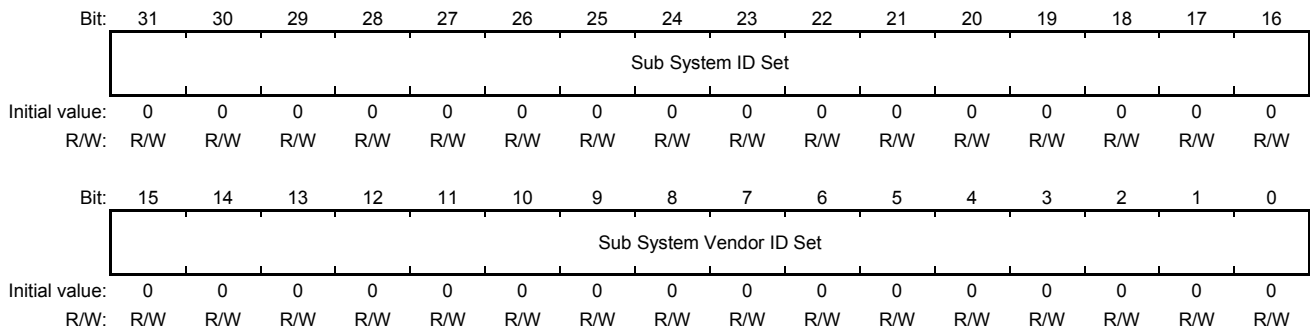
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	Class Code Set	H'FF	R/W	Class Code Set Set the class code at initialization. The value of this field is reflected to PCICONF2[31:24].Class Code.
23 to 16	Sub Class Code Set	H'00	R/W	Sub Class Code Set Set the sub-class code at initialization. The value of this field is reflected to PCICONF2[23:16].Sub Class Code.
15 to 8	PROG IF Set	H'00	R/W	PROG IF Set Set the programming IF code at initialization. The value of this field is reflected to PCICONF2[15:8].PROG IF.
7 to 0	Rev ID Set	H'00	R/W	Rev ID Set Set the revision ID at initialization. The value of this field is reflected to PCICONF2[7:0].Revision ID.

**39.2.93 SUBID Setting Register (SUBIDSETR)**

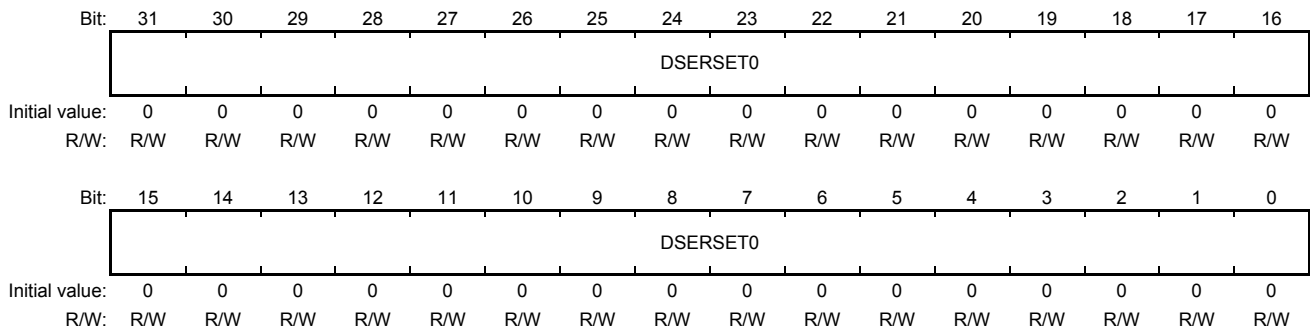
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—



Bit	Bit Name	Initial Value	R/W	Description
31 to 16	Sub System ID Set	H'0000	R/W	Sub System ID Set Sets the sub-system ID. Set the sub-system device ID allocated to the PCI device vendor at initialization. The value of this field is reflected to PCICONF11[31:16].Sub System ID.
15 to 0	Sub System Vendor ID Set	H'0000	R/W	Sub System Vendor ID Set Sets the sub-system vendor ID. Set the sub-system vendor ID allocated to the PCI device vendor at initialization. The value of this field is reflected to PCICONF11[15:0].Sub System Vendor ID.

**39.2.94 Device Serial Number Setting Register 0 (DSERSETR0)**

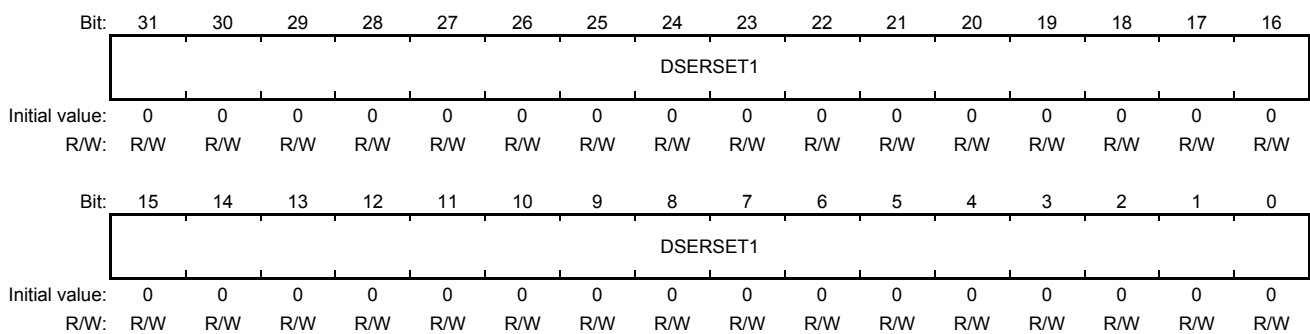
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	DSERSET0	All 0	R/W	DSERSET0 Set 4 bytes of 1stDW of the device serial number at initialization. The value of this field is reflected to SERNUMCAP1.Device Serial Number 1st.

**39.2.95 Device Serial Number Setting Register 1 (DSERSETR1)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	DSERSET1	All 0	R/W	DSERSET1 Set 4 bytes of 2ndDW of the device serial number at initialization. The value of this field is reflected to SERNUMCAP2.Device Serial Number 2nd.

### 39.2.96 TL Control Register (TLCTLR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
	Bus Number								Device Number				—	—	—		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	—	—	Default Completion Timeout Time					—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R	

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	Bus Number	H'00	R/W	<p>Bus Number</p> <p>The value of this field is used as the bus number at issuance of a request.</p> <p>The value of this field is used for checking the transaction ID bus number part within this IP on reception of Completion.</p> <p>Root Port:</p> <p>Set the device bus number.</p> <p>Endpoint:</p> <p>This field is always updated on reception of a Type0 Configuration Write request.</p>
23 to 19	Device Number	H'00	R/W	<p>Device Number</p> <p>The value of this field is used as the device number at issuance of a request.</p> <p>The value of this field is used for checking the transaction ID device number part within this IP on reception of Completion.</p> <p>Root Port:</p> <p>Set the device number.</p> <p>Endpoint:</p> <p>This field is always updated on reception of a Type0 Configuration Write request.</p>
18 to 14	—	All 0	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>
13 to 8	Default Completion Timeout Time	H'00	R/W	<p>Default Completion Timeout Time</p> <p>Sets the Completion Timer timeout time for default setting (unit: ms). If a Completion cannot be received within the time set by this field, it is handled as a Completion timeout. Set a value from 10 to 50 ms.</p>
7 to 0	—	All 0	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>

## 39.2.97 MAC Status Register (MACSR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	LKTR	LPBAK 1ST	LPBAK 2ST	DISST	HOTRS TST	Link Width					Link Speed				
Initial value:	—	0	0	0	0	0	0	0	0	11	0	0	0	0	0	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	SPCHG SUC	SPCHG FAIL	SPCHG	SPCHG FIN	LOENT	—	—	—
Initial value:	—	—	—	0	—	—	0	0	0	0	0	0	0	0	0	—
R/W:	R	R	R	R	R	R	R	R	RW1C	RW1C	RW1C	RW1C	RW1C	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31	—	—	R	Reserved The read value is undefined. The write value should always be 0.
30	LKTR	0	R	Link Training Indicates that MAC LTSSM is in the recovery or configuration state and that link training is in progress. 0: Link training is not in progress. 1: Link training is in progress. The value of this field is reflected to EXPCAP4[27].LKTR.
29	LPBAK1ST	0	R	Loop Back1 State Indicates that the MAC LTSSM is in Per Lane Loop BAK mode. Loopback test can be executed as a loopback master. Note: LTSSM has made a transition to the loopback state without executing Configuration. 0: Not in the Loop Back1 state 1: In the Loop Back1 state
28	LPBAK2ST	0	R	Loop Back2 State Indicates that the MAC LTSSM is in Configured Link Loop BAK mode. Loopback test can be executed as a loopback master. Note: LTSSM has made a transition to the loopback state after executing Configuration. 0: Not in the Loop Back2 state 1: In the Loop Back2 state
27	DISST	0	R	Disabled State Indicates that the MAC LTSSM is in the disabled state. Note: This bit is set only when this IP itself makes a request for link disable (sets 1 to EXPCAP4[4].LKDIS). Therefore, in Endpoint mode, 0 is always read. 0: Not in the disabled state 1: In the disabled state

Bit	Bit Name	Initial Value	R/W	Description
26	HOTRSTST	0	R	Hot Reset State Indicates that the MAC LTSSM is in the Hot Reset state. 0: Not in the Hot Reset state 1: In the Hot Reset state
25 to 20	Link Width	H'04	R	Link Width Indicates the width of the link established by MAC configuration. This field is valid when PCIETSTR.DLLACT = 1. H'01: x1 link width H'02: x2 link width H'04: x4 link width Indicates the same value as the value of EXPCAP4.Negotiated Link Width.
19 to 16	Link Speed	H'0	R	Link Speed Indicates the speed of the link established by the MAC configuration. This field is valid when PCIETSTR.DLLACT = 1. This IP supports the following link speeds: H'1: 2.5 GT/s H'2: 5.0 GT/s Indicates the same value as EXPCAP4.Current Link Speed. When read by firmware, the same value is read from the both fields.
15, 14	—	—	R	Reserved The read value is undefined. The write value should always be 0.
13	—	—	R	Reserved Ignore the value of this bit. The read value is undefined. The write value should always be 0.
12	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
11, 10	—	—	R	Reserved The read value is undefined. The write value should always be 0.
9, 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7	SPCHGSUC	0	RW1C	Speed Change Success Indicates that speed negotiation started by this module has succeeded. Clear this bit by writing 1. Writing 0 is invalid.
6	SPCHGFAIL	0	RW1C	Speed Change Fail Indicates that speed negotiation started by this module has failed. Clear this bit by writing 1. Writing 0 is invalid.

Bit	Bit Name	Initial Value	R/W	Description
5	SPCHG	0	RW1C	<p>Speed Change</p> <p>Indicates that speed has been changed.</p> <p>When this bit is set to 1, write 1 to clear the bit.</p> <p>Writing 0 is invalid.</p>
4	SPCHGFIN	0	RW1C	<p>Speed Change Finish</p> <p>Indicates that speed change processing requested by this IP has been completed.</p> <p>This bit is set to 1 at the same time that MACCTLR.SPCHG is cleared to 0.</p> <p>This bit is not updated if speed change processing is caused by the communication peer. For the usage, see section 39.3.9 (1), Changing Speed.</p> <p>When this bit is set to 1, write 1 to clear the bit.</p> <p>Writing 0 is invalid.</p>
3	LOENT	0	RW1C	<p>L0 Enter</p> <p>This bit is set to 1 when a transition to L0 is made. This bit is cleared by hardware when the MACSR.SPCHGFIN interrupt is generated.</p> <p>For the usage, see section 39.3.9 (1), Changing Speed.</p> <p>When this bit is set to 1, write 1 to clear the bit. However, the bit cannot be cleared in the L0 state.</p> <p>Writing 0 is invalid.</p>
2, 1	—	All 0	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>
0	—	—	R	<p>Reserved</p> <p>The read value is undefined. The write value should always be 0.</p>



### 39.2.98 MAC Control Register (MACCTLR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	LTSMDIS	—	LPBAK	—	SCRDIS	FRCMP	—	SPCHG	—	—	—	—	—	—	—	—
Initial value:	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
R/W:	R/W	R	R/W	R	R/W	R/W	R	R/W	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31	LTSMDIS	1	R/W	<p>LTSSM Disable</p> <p>Disables MAC LTSSM operation.</p> <p>LTSSM does not operate while this bit is 1.</p> <p>0: MAC LTSSM is not disabled and operation is performed.</p> <p>1: MAC LTSSM is disabled.</p> <p>This bit is automatically cleared when PCIETCTLR[0].CFINIT is set.</p>
30	—	0	R	<p>Reserved</p> <p>This bit is always read as 0. The write value should always be 0.</p>
29	LPBAK	0	R/W	<p>Loop Back</p> <p>Requests MAC LTSSM to perform loopback transfer.</p> <p>When this bit is set, MAC LTSSM will be a loopback master after the Configuration or Recovery state, and makes a transition to the loopback state.</p> <p>Read MACCSR.LPBAK1ST or LPBAK2ST to confirm that loopback state transition has been completed.</p> <p>0: MAC LTSSM will not be a loopback master.</p> <p>1: MAC LTSSM will be a loopback master.</p>
28	—	0	R	<p>Reserved</p> <p>This bit is always read as 0. The write value should always be 0.</p>
27	SCRDIS	0	R/W	<p>Scramble Disable</p> <p>Disables the MAC data scramble function.</p> <p>Note: Set this bit when MACCTLR.LTSMDIS is 1. If this bit is changed with MACCTLR.LTSMDIS being 0, operation is undefined.</p> <p>0: The data scramble function is enabled.</p> <p>1: The data scramble function is disabled.</p>

Bit	Bit Name	Initial Value	R/W	Description
26	FRCCM	0	R/W	<p>Force Compliance</p> <p>Directs a forcible transition to compliance mode.</p> <p>If set to 1 before a transition to the Polling.Active state is made, Polling.Compliance state transition is made after a timeout occurs in the Polling.Active state. If cleared to 0 during or after a transition, a transition to the Detect state is made.</p>
25	—	0	R	<p>Reserved</p> <p>This bit is always read as 0. The write value should always be 0.</p>
24	SPCHG	0	R/W	<p>Speed Change</p> <p>Directs speed change.</p> <p>If set to 1 when LTSSM is in the L0, L0s, or L1 state, LTSSM makes a transition to the recovery state thus allowing speed negotiation. Only writing 1 is valid and writing 0 is invalid. This bit is read as 1 during a transition.</p>
23 to 16	—	H'FF	R	<p>Reserved</p> <p>Modifying these bits is prohibited. The write value should be H'FF.</p>
15 to 1	—	All 0	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>
0	—	1	R	<p>Reserved</p> <p>The write value should always be 0.</p> <p>Note: Write 0 at initialization.</p>

## 39.2.99 PM Status Register (PMSR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	L1FAEG	—	—	—	—	—	—	—	PMEL1RX	—	—	—	—	PMSTATE		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	RW1C	R	R	R	R	R	R	R	RW1C	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31	L1FAEG	0	RW1C	L1 Fall Edge This bit is set to 1 when L1 activation sequence started by writing 1 to PMCTLR.L1IATN is stopped or completed. Writing 1 clears this bit. Writing 0 is invalid. 0: L1 activation sequence has not been completed or stopped. 1: L1 activation sequence has been completed or stopped.
30 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23	PMEL1RX	0	RW1C	PM Enter L1RX This bit is set to 1 when PM_ENTER_L1 DLLP is received. Writing 1 clears this bit. Writing 0 is invalid. 0: PM_ENTER_L1 DLLP has not been received. 1: PM_ENTER_L1 DLLP has been received.
22 to 19	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
18 to 16	PMSTATE	000	R	PMSTATE Indicates the state of the power management state machine. These bits cannot be written to. 000: LDn state 001: L0 state 011: L1 state 100: L0s state Other than above: Reserved
15 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

## 39.2.100 PM Control Register (PMCTLR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	L1IATN	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31	L1IATN	0	R/W	<p>L1 Initiation</p> <p>Writing 1 starts a transition to L1. Writing 0 is invalid.</p> <p>This bit is read as 1 during a transition to L1.</p> <p>This bit is 0 when the PM state makes a transition from L0 to another state.</p> <p>0: L1 transition sequence has not been started.</p> <p>1: Transition processing to the L1 state is in progress.</p>
30 to 0	—	All 0	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>

**39.2.101 MAC Interrupt Enable Register (MACINTENR)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	LKTRE	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	SPCHG SUCE	SPCHG FAILE	SPCHG E	SPCHG FINE	LOENT E	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
30	LKTRE	0	R/W	Link Training Enable Enables generation of the interrupt by link training. When this bit is set to 1, the interrupt is generated. 0: The interrupt by link training is disabled. 1: The interrupt by link training is enabled.
29 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7	SPCHGSUCE	0	R/W	Speed Change Success Enable Enables generation of the interrupt by Speed Change Success. When this bit is set to 1, the interrupt is generated. 0: The interrupt by Speed Change Success is disabled. 1: The interrupt by Speed Change Success interrupt is enabled.
6	SPCHGFAILE	0	R/W	Speed Change Fail Enable Enables generation of the interrupt by Speed Change Fail. When this bit is set to 1, the interrupt is generated. 0: The interrupt by Speed Change Fail is disabled. 1: The interrupt by Speed Change Fail is enabled.
5	SPCHGE	0	R/W	Speed Change Enable Enables generation of the interrupt by speed change. When this bit is set to 1, the interrupt is generated. 0: The interrupt by speed change is disabled. 1: The interrupt by speed change is enabled.

Bit	Bit Name	Initial Value	R/W	Description
4	SPCHGFINE	0	R/W	<p>Speed Change Finish Enable</p> <p>Enables generation of the interrupt by completion of speed change processing caused by this IP. When this bit is set to 1, the interrupt is generated.</p> <p>0: The interrupt by completion of speed change processing caused by this IP is disabled.</p> <p>1: The interrupt by completion of speed change processing caused by this IP is enabled.</p>
3	LOENTE	0	R/W	<p>L0 Enter Enable</p> <p>Enables generation of the interrupt by L0 transition. When this bit is set to 1, the interrupt is generated.</p> <p>0: The interrupt by L0 transition is disabled.</p> <p>1: The interrupt by L0 transition is enabled.</p>
2 to 0	—	All 0	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>

## 39.2.102 PM Interrupt Enable Register (PMINTENR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	L1FAE GE	—	—	—	—	—	—	—	PMEL1 RXE	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R	R	R	R	R	R/W	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31	L1FAEGE	0	R/W	<p>L1 Fall Edge Enable</p> <p>Enables generation of the interrupt by L1FAEG. When this bit is set to 1, the interrupt is generated.</p> <p>0: The interrupt by L1FAEG is disabled.</p> <p>1: The interrupt by L1FAEG is enabled.</p>
30 to 24	—	All 0	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>
23	PMEL1RXE	0	R/W	<p>PM_Enter_L1_RX Enable</p> <p>Enables generation of the interrupt by PMEnterL1RX. When this bit is set to 1, the interrupt is generated.</p> <p>0: The interrupt by PMEnterL1RX is disabled.</p> <p>1: The interrupt by PMEnterL1RX is enabled.</p>
22 to 0	—	All 0	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>

**39.2.103 MAC Status Register 2 (MACS2R)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	Compliance Status		—	—	Initial Link Width					Current Support Link Speed				
Initial value:	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	Max Support Link Speed			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31, 30	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
29, 28	Compliance Status	00	R	Compliance Status Indicates the compliance pattern transmission state. 00: Compliance patterns are not being transmitted. 01: Normal compliance patterns are being transmitted. 10: Modified compliance patterns are being transmitted.
27, 26	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
25 to 20	Initial Link Width	H'4	R	Initial Link Width Indicates the width of the initially established link. These bits are only valid when PCIETSTR.DLLACT = 1. H'01: x1 link width H'02: x2 link width H'04: x4 link width
19 to 16	Current Support Link Speed	H'1	R	Current Support Link Speed Indicates the maximum link speed currently supported by the peer. These bits are only valid when PCIETSTR.DLLACT = 1. H'1: 2.5 GT/s H'2: 5.0 GT/s
15 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3 to 0	Max Support Link Speed	H'1	R	Max Support Link Speed Indicates the maximum link speed supported by the peer after the link establishment. These bits are only valid when PCIETSTR.DLLACT = 1. H'1: 2.5 GT/s H'2: 5.0 GT/s



## 39.2.104 MAC Control Register 2 (MACCTL2R)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	EXITLP BAK	FRCLP BAK	—	—	EXIT CMP	—	—	—	Force Link Speed			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
R/W:	R	R	R	R	R/W	R/W	R	R	R/W	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11	EXITLPBAK	0	R/W	EXIT Loop Back If set to 1 during loopback slave operation in the Loopback.Active state, a transition to the Detect state is made. Only writing 1 is valid and writing 0 is invalid. This bit is read as 1 during a transition.
10	FRCLPBAK	0	R/W	Force Loop Back Sets the mode when MACCTL1R.LPBAK is set to 1. When this bit is 1, a transition to the Loopback.Active state is made after a specified time elapsed even if TSOS has not been received from the peer in the Loopback.Entry state.
9, 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7	EXIT CMP	0	R/W	EXIT Compliance When reception of TS1 (Compliance) causes transition to Polling.Compliance state, setting this bit to 1 causes transition to the Detect state. Only writing 1 is valid and writing 0 is invalid. This bit is read as 1 during a transition.
6 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3 to 0	Force Link Speed	H'2	R/W	Force Link Speed Specifies the upper limit of supported rate and loopback compliance rate to be conveyed to the peer when executing a loopback master operation or forcible compliance. H'1: 2.5 GT/s H'2: 5.0 GT/s

### 39.2.105 MAC Speed Change Setting Register (MACCGSPSETR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SPCNG RSN	—	—	—	—	—	—	—	—	—	—	—	Target Link Speed			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
R/W:	R/W	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31	SPCNGRSN	0	R/W	Speed Change Reason Indicates the factor of link speed change. 0: An intentional factor 1: A link reliability problem
30 to 20	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
19 to 16	Target Link Speed	H'2	R/W	Target Link Speed Specifies the speed of the link to be established using the link speed change in Endpoint mode. (In Root Port mode, EXPCAP12[3:0].Target Link Speed is used.) H'1: 2.5 GT/s H'2: 5.0 GT/s
15 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

### 39.3 Operation

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

The following describes the operation of this module.

Note: The following operation flowcharts are each divided in two parts and described. One part covers the H/W, hardware operation of this module and the other covers the S/W, software operation to control this module. The arrows originating from the outside of the figure frame indicate that the event arises from the user program.

In the explanation of the operation flows, interrupt sources are described in the H/W part. The S/W should first verify a given interrupt flag and then clear it.

If generation of interrupt sources is expected, enable each of the interrupt sources referring to Figures 39.31 and 39.32.

#### 39.3.1 Initialization

##### (1) Standby State Cancellation

- After canceling a reset, cancel the module standby state. For the module standby state, refer to section 7A, Module Standby and Software Reset. This module is in the module standby state after a power-on reset is canceled.

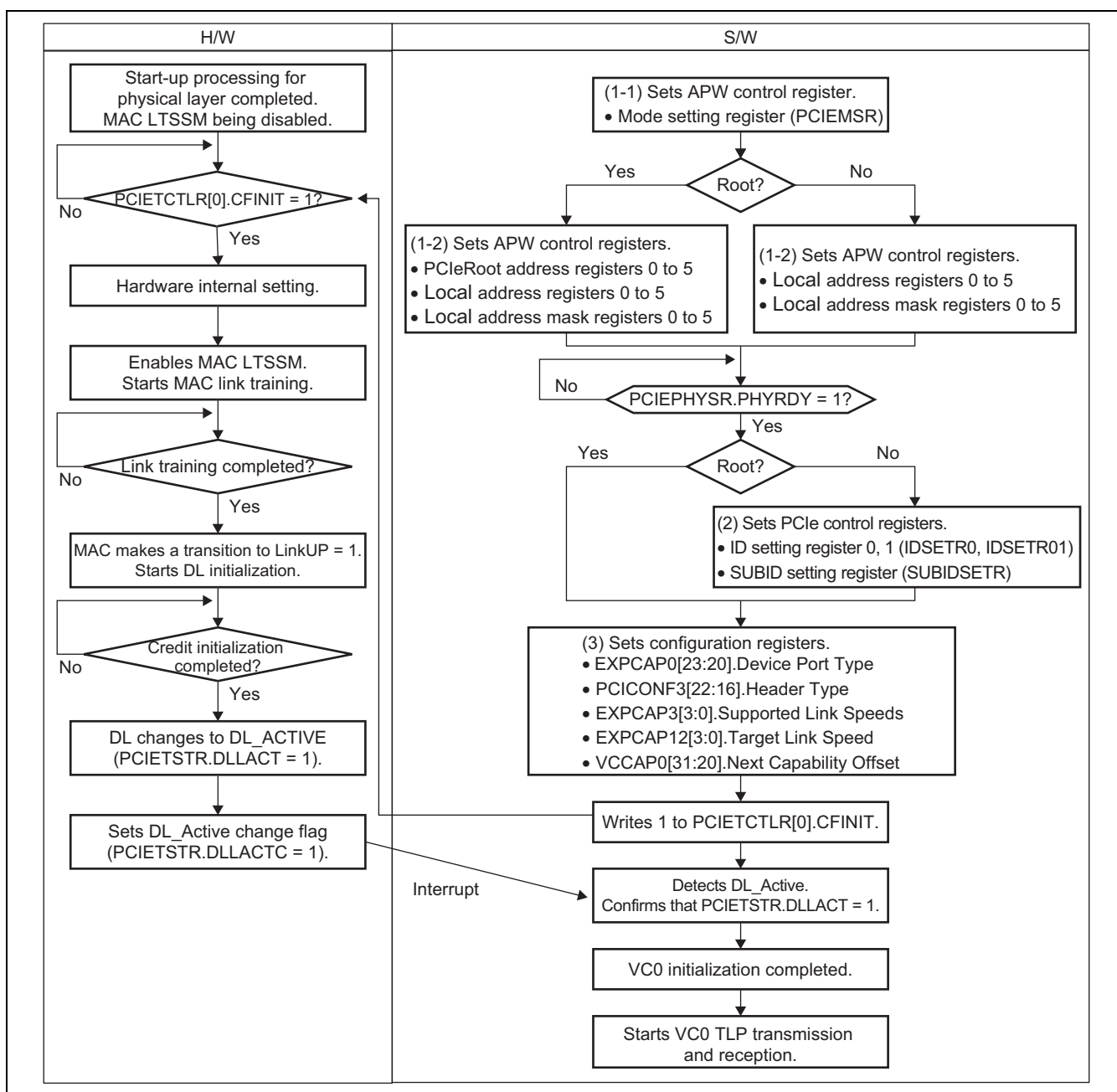
##### (2) Initialization of the Physical Layer

Before using this module, set the parameter values to the address fields as shown in the table below to initialize the physical layer.

Address	Parameter	Access size
H'780	H'000F_0030	32
H'784	H'0038_1203	32
H'78C	H'0000_0001	32
H'78C	H'0000_0006	32
H'780	H'000F_0054	32
H'784	Reference clock setting is AC connection, termination resistor OFF: H'1380_2003 Reference clock setting is DC connection, termination resistor OFF: H'1380_2007 Reference clock setting is AC connection, termination resistor ON: H'1380_200B Reference clock setting is DC connection, termination resistor ON: H'1380_200F	32
H'78C	H'0000_0001	32
H'78C	H'0000_0006	32

**(3) Initial Setting of PCI Express**

- Figure 39.2 shows the PCIEC operation in initial setting.
- After start-up processing for the physical layer is completed, the initial setting is executed to start operation as a PCI Express. Until the initial setting is completed, this module cannot work correctly as a PCI Express device. Therefore, a link is not established immediately after a reset is canceled. When the initial setting is completed, enable the PCIETCTLR.CFINIT to start operation.
- Set the bits in the configuration registers as directed in the related register description, if there is a direction on initialization.
- Set H'000 in the Next Capability Offset[31:20] bits in VCCAP0.
- Be sure to write the initial value (= H'80FF 0000) to MACCTLR before enabling PCIETCTLR.CFINIT.
- When a register is used with the default setting, setting the register is not required.

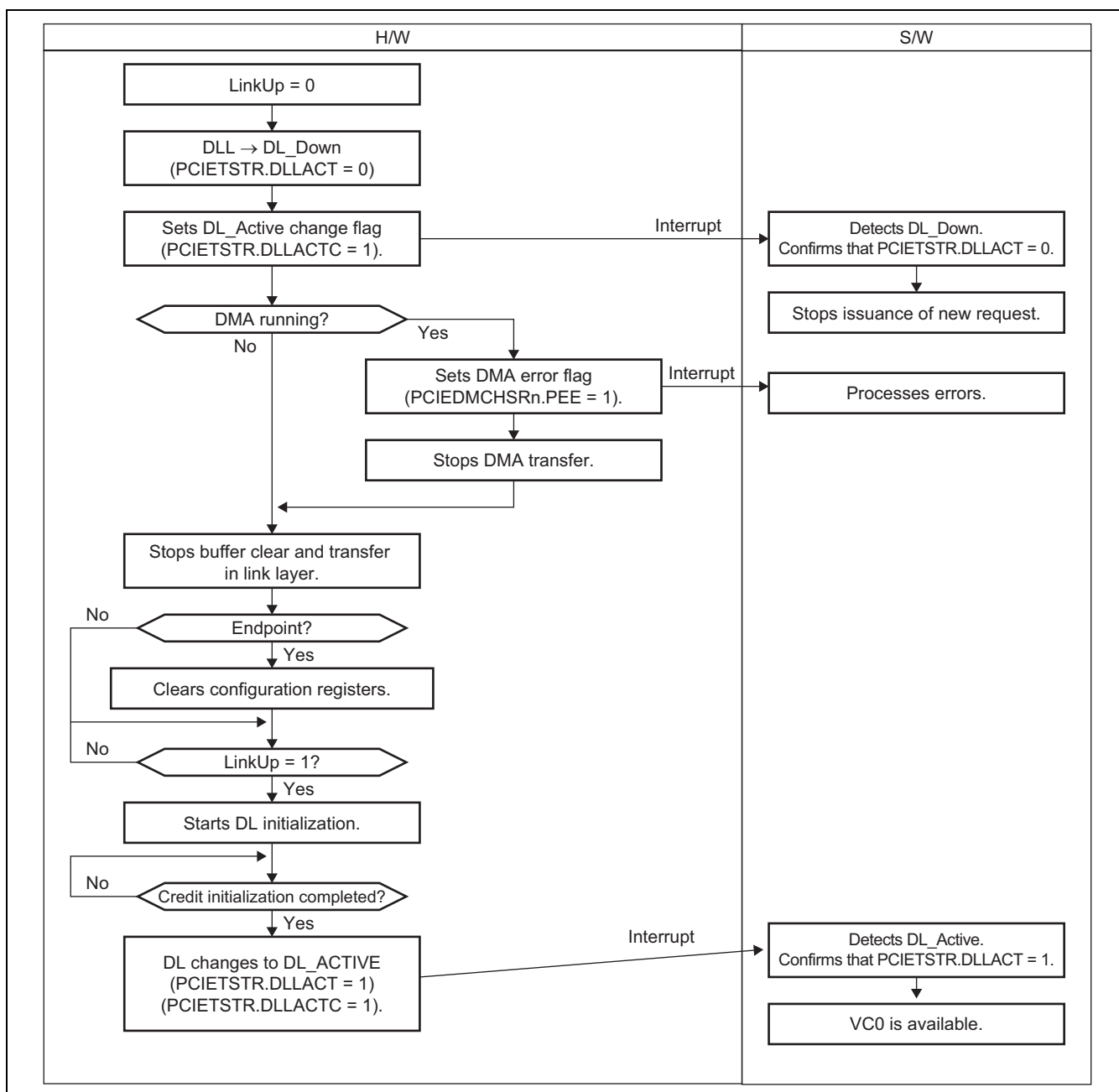


**Figure 39.2 Initial Setting of PCIEC**

**(4) DL\_Down Operation**

Figure 39.3 shows the operation when a link goes down (LinkUP = 0) in the state where a link is established, thus causing DL\_Down. When DL\_Down is caused, PCIETCTLR.DLDOWN is set to 1. Since the current data is invalidated, all the resources of the data transmitter/receiver of this module are initialized.

- Upon DL\_Down, a write to the transmission buffer is disabled thus stopping transmission.
- Upon DL\_Down, the receive buffer is forcibly cleared.
- If a link goes down, transmission and reception are suspended; therefore, data before and after DL\_Down becomes illegal. Since the specific process here differs depending on the application, the operation is simply indicated as “Processes errors.” in the flowchart shown in Figure 39.3.



**Figure 39.3 DL\_Down Operation**

## (5) Hot Reset Operation

### (a) Hot Reset Transmission

In Root Port mode, to send a hot reset to a downstream port, write 1 to the secondary bus reset bit in the configuration register. Before issuing a hot reset, confirm that this module has completed transfer.

### (b) Hot Reset Reception

In Endpoint mode, when a hot reset is received from an upstream port, the LTSSM on the link layer makes a transition to the hot reset state. This causes LinkUp = 0 and then DL\_Down = 1. After this, the same operation is performed as the operation upon the DL\_Down.

## 39.3.2 Configuration Cycle

When using this module as a Root Port, a configuration cycle must be generated to configure the connection-target device. A configuration cycle refers to the process of checking the status of the configuration register of the connection-target Endpoint, switch, or bridge through the use of configuration access, and assigning values to the configuration registers of the Root Port itself and the Endpoint according to the result of the checking. When the Root Port accesses its own configuration register, such access is normally made through the internal bus.

This section describes the transmission (write) and reception (read) operations of the configuration access, and the items to be specified during a configuration cycle.

When this module is used as an Endpoint, it receives a configuration access from a Root Port, and accepts the initialization processing.

### (1) Configuration Read Operation

Figure 39.4 shows a flow of configuration read operation.

With EXPCAP7[4].CRSVISE = 0, an error response is returned when the CRS status is received.

With EXPCAP7[4].CRSVISE = 1, response data is H'FFFF 0001 when the CRS status is received. Therefore, the first access to the peer device from which the CRS status may possibly be returned must be configuration read from register 0. Here, judgment is possible only by the VID that has read that no device is existent (including an unsupported request response) or that a CRS response is received, thus simplifying the procedure for setting the bus number of the PCI bus topology.

Automatic hardware response according to the CRS status is not supported.

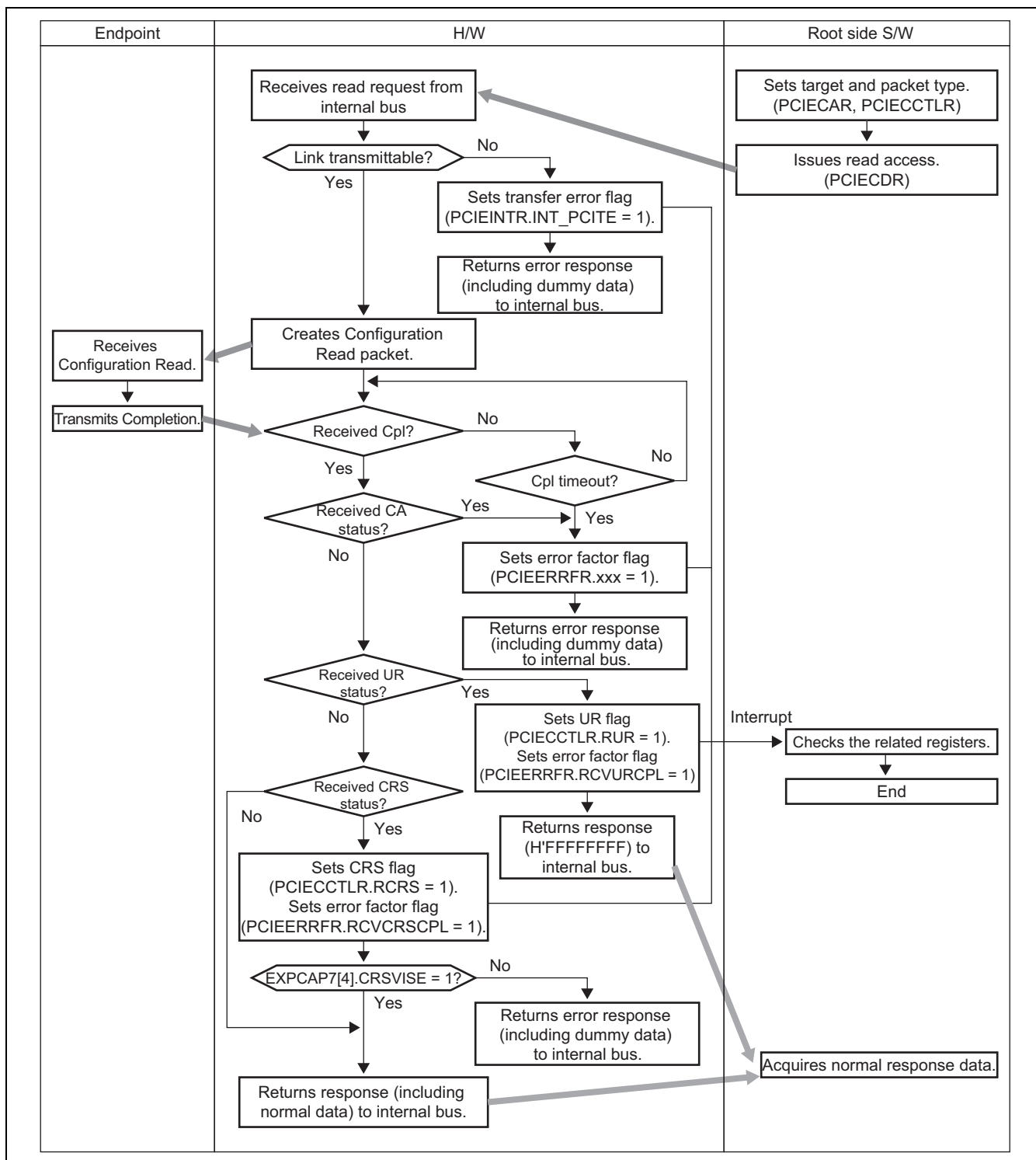
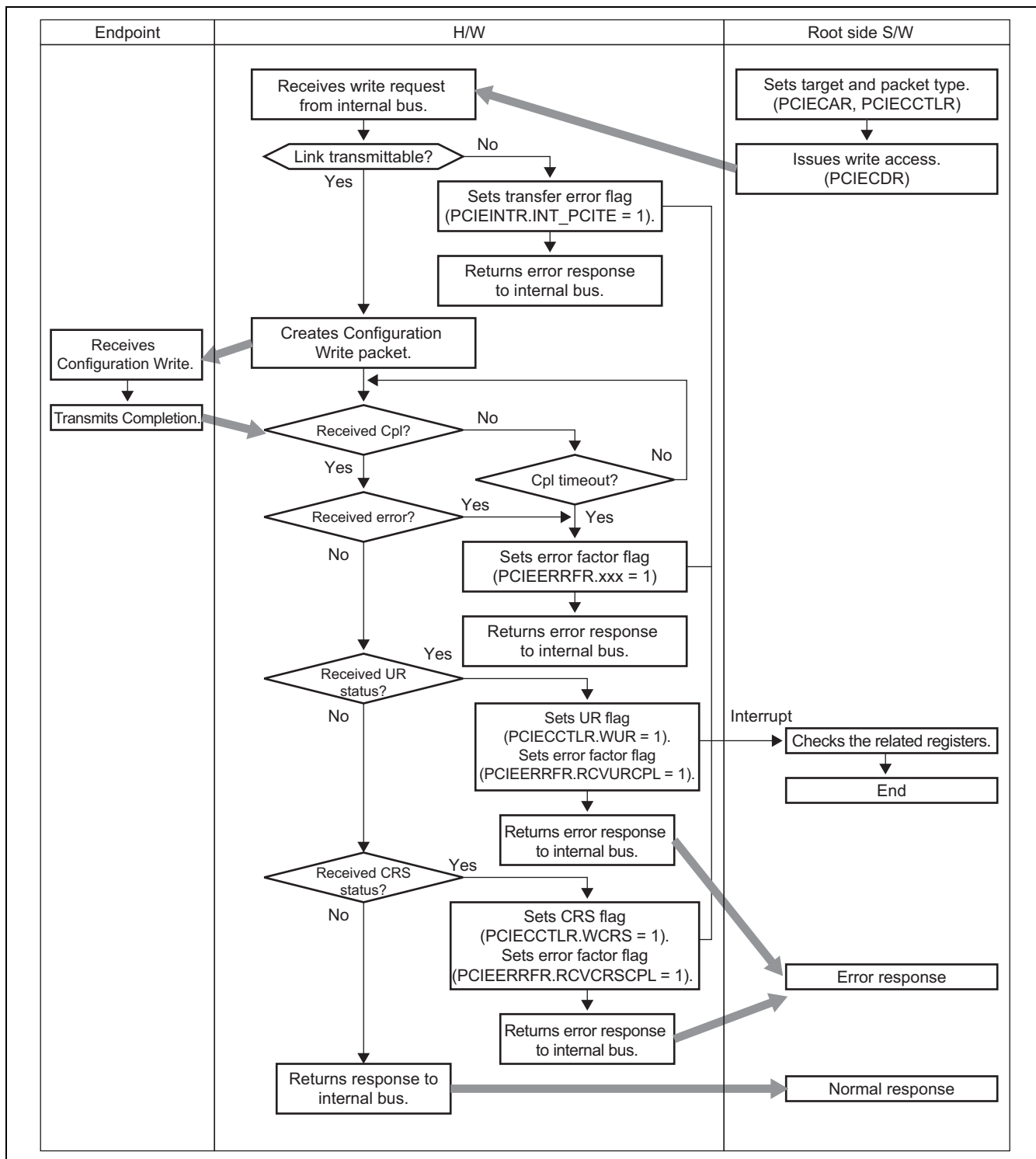


Figure 39.4 Configuration Read Operation

**(2) Configuration Write Operation**

Figure 39.5 shows a flow of configuration write operation.

The peer device should be the function for which configuration read has been succeeded (= the function from which CRS may never be returned).



**Figure 39.5 Configuration Write Operation**



### (3) Initialization of PCIEC in Root Port Mode

In Root Port mode, set all the Endpoints (indicated as system in the flow chart) connected to the PCIEC after link establishment. Figure 39.6 shows a sample setting flowchart.

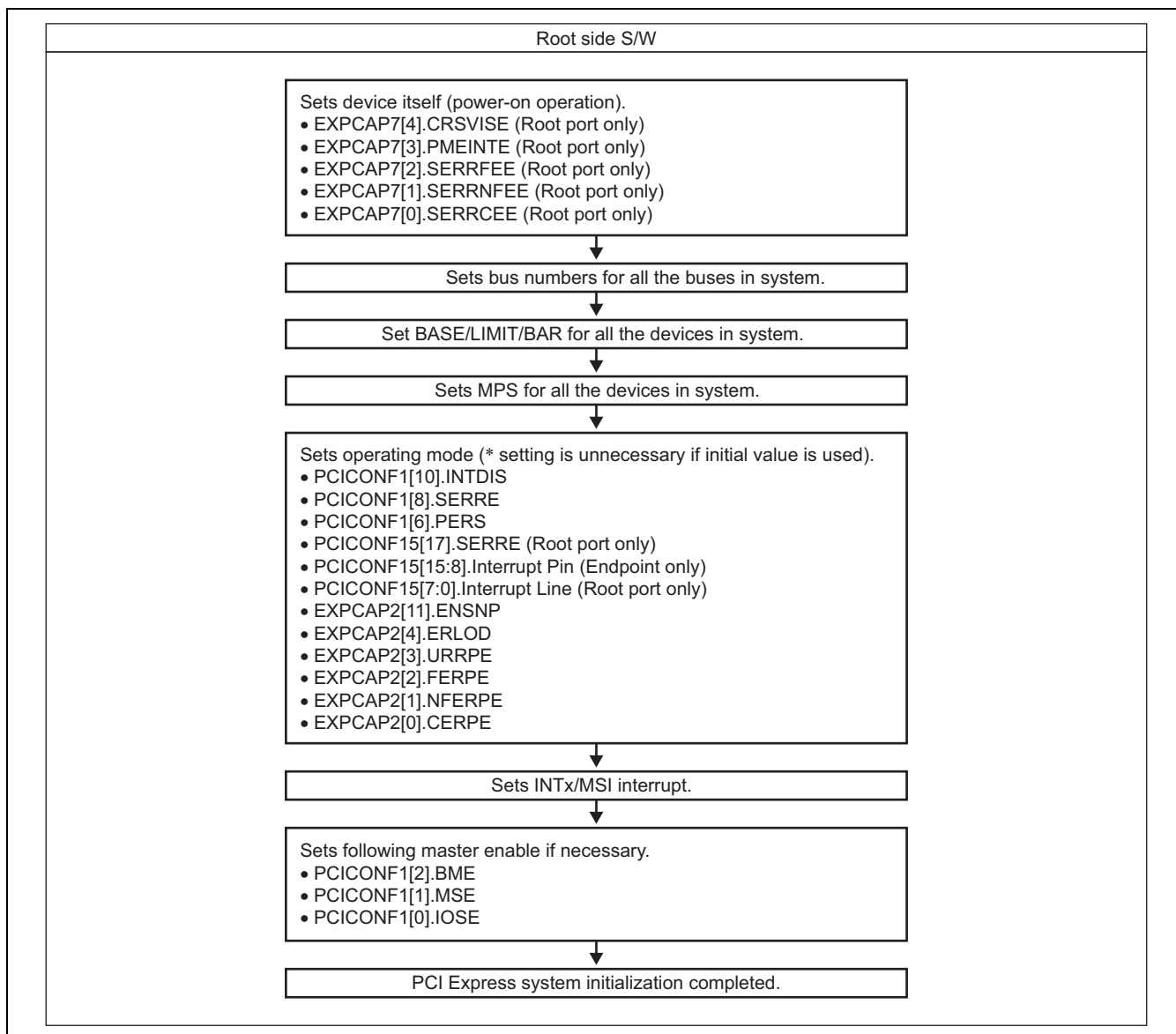


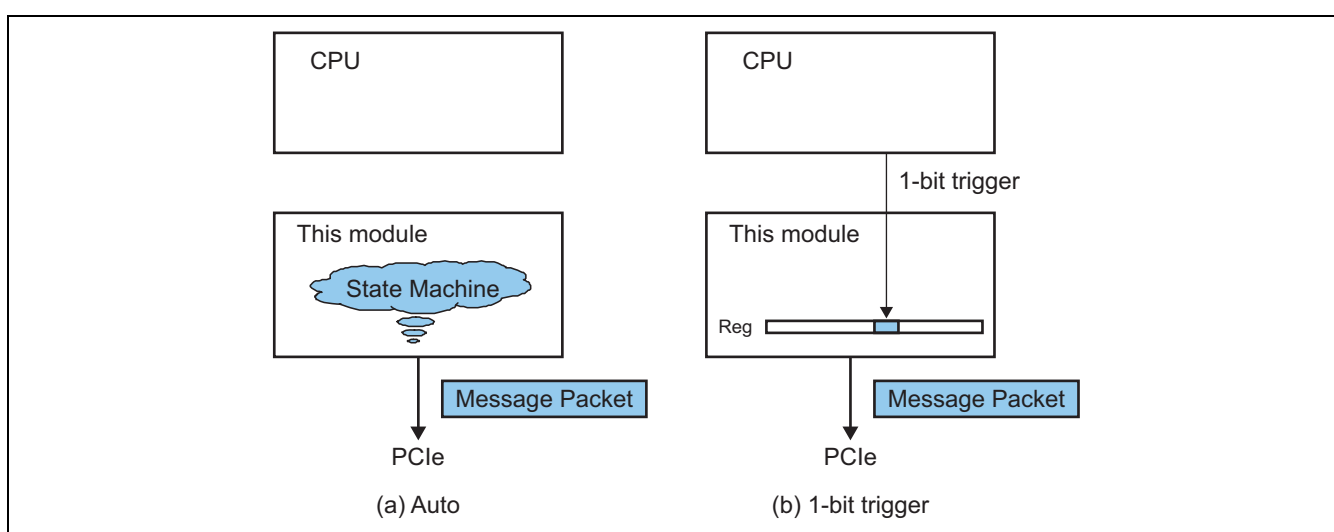
Figure 39.6 PCIEC Initialization in Root Port Mode

### 39.3.3 Messages and MSI

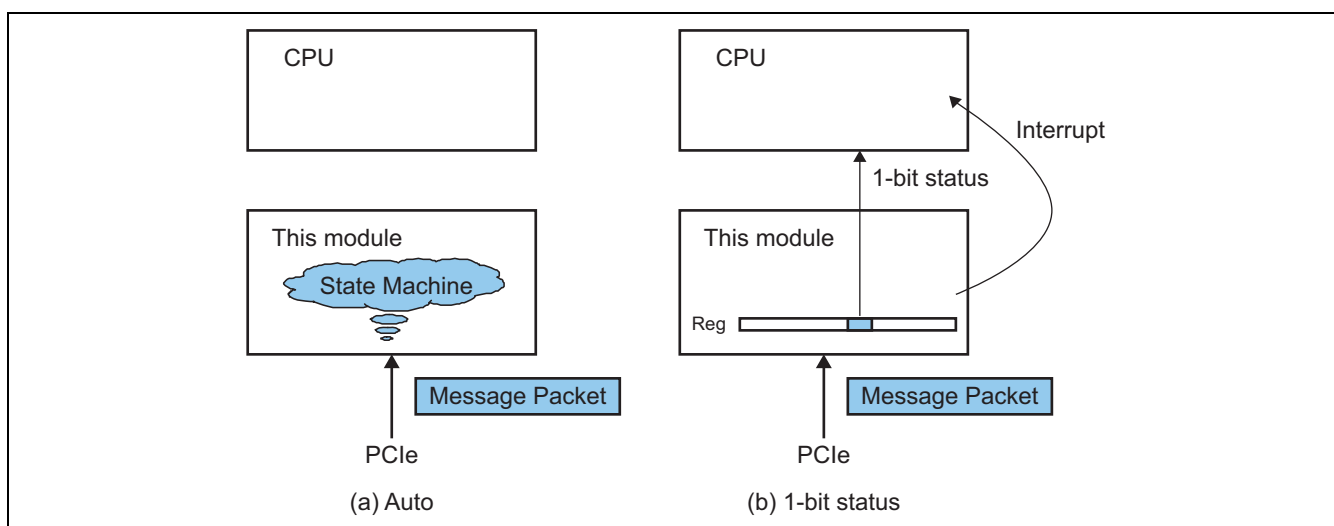
This module supports transmission and reception of the messages and MSI (Message Signaled Interrupt) defined in the PCI Express standard. The messages allow interrupt signaling, power management, error information notification, and unlocking. The MSI is used instead of INTx to signal interrupts. The following sections describe transmission and reception of the messages and MSI.

#### (1) Overview of Messages

This module automatically transmits and receives messages that indicate the error state of a link through hardware (Figures 39.7 (a) and 39.8 (a)). The other types of messages can be transmitted and received only by writing and reading the registers of this module (Figures 39.7 (b) and 39.8 (b)). The PM-related messages and INTx messages have separate 1-bit fields corresponding to the messages and simply writing to the pertinent bit allows this module to create and transmit a message. In message reception, reading the status of the pertinent bit completes reception.



**Figure 39.7 Message Transmission Methods**



**Figure 39.8 Message Reception Methods**

## (2) Message Transmission

Messages can be transmitted by either of the following two methods.

### (a) Automatic Message Transmission by Hardware

This module automatically sends a necessary message when an error occurs. The following messages are automatically sent.

- **ERR\_COR**: When transmission of the correctable error message is enabled, this message is automatically sent if a correctable error occurs.
- **ERR\_NONFATAL**: When transmission of the non-fatal error message is enabled, this message is automatically sent if a non-fatal error occurs.
- **ERR\_FATAL**: When transmission of the fatal error message is enabled, this message is automatically sent if a fatal error occurs.

### (b) Initiation of Message Transmission by 1-bit Writing through Software

This module sends unlock or INTx interrupt messages under control by software. To send these messages, access the following registers.

- **Unlocking (unlock message transmission)**: Writing 1 to PCIEUNLOCKCR[0].ASTUNLOCK allows transmission of the unlock message and unlocking. The unlock messages can be transmitted only by the Root Port.
- **Power management message transmission (PME\_\* message transmission)**: Writing 1 to the bits corresponding to the messages in the power management message transmission control register allows transmission of the messages given below: PME\_TO\_ACK, PME\_TOFF, and PM\_PME.
- **INTx interrupt generation and cancellation (Assert\_INTx/Deassert\_INTx message transmission: x=A, B, C, or D)**: Writing 1 to PCIEINTXR[16].ASTINTX allows transmission of the Assert\_INTx message corresponding to the INTx specified with PCICONF15[15:8].Interrupt Pin thus allowing generation of the INTx interrupt. Writing 0 to PCIEINTXR[16].ASTINTX allows transmission of the Deassert\_INTx message corresponding to the INTx specified with PCICONF15[15:8].Interrupt Pin thus allowing cancellation of the INTx interrupt. The INTx interrupts can be generated and canceled only by the Endpoint.

## (3) Message Reception

In this module, reception of some messages is automatically handled by hardware. For the message reception processes not performed through hardware, refer to the status and process reception through software. Note that the messages except Vendor\_Defined\_Message are required by the PCI Express standard to be transmitted and received with TC0. If such a message is received with the other TC, the PCIEC considers it as a malformed TLP (fatal error) thus performing error processing automatically.

### (a) Automatic Message Reception by Hardware

- **Assert\_INTx (x is A to D)**: When this message is received in Root Port mode, PCIEINTXR[0,1,2,3].INTx are set. The INTx interrupt is generated here when PCICONF15[7:0].Interrupt Line is not H'FF. When received in Endpoint mode, this message is considered as a malformed TLP and error processing is performed.
- **Deassert\_INTx (x is A to D)**: When this message is received in Root Port mode, PCIEINTXR[0,1,2,3].INTx are cleared. The INTx interrupt is canceled here (only in the Root Port) when PCICONF15[7:0].Interrupt Line is not H'FF. When received in Endpoint mode, this message is considered as a malformed TLP and error processing is performed.
- **ERR\_COR**: When this message is received, the appropriate value is set to the configuration register to indicate reception of a correctable error and the INT\_PCICERR interrupt is generated.
- **ERR\_NONFATAL**: When this message is received, the appropriate value is set to the configuration register to indicate reception of a non-fatal error and the INT\_PCINFERR interrupt is generated.
- **ERR\_FATAL**: When this message is received, the appropriate value is set to the configuration register to indicate reception of a fatal error and the INT\_PCIFERR interrupt is generated.

- **Unlock:** The unlock message is discarded since neither the PCI Express Endpoint nor Root Port accepts a lock request.
- **Set\_Slot\_Power\_Limit:** (When this message is received, the power information specified with the message is automatically reflected to the configuration register (EXPCAP1[27:18]) through hardware.)

#### (b) Reception of Messages Requiring Software Processing

The module hardware detects reception of the following messages but does not automatically process them. Reception of these messages must be checked and processed by software as described below.

- PM\_PME

A message reception can be checked via the following registers:

- PCIERMSGR
- PCIERMSGIER
- EXPCAP8

In the PCIERMSGR, bits are defined for each specified message, and 1 is set to a bit corresponding to the received message when a message is received. In this situation, if the corresponding bit in the PCIERMSGIER is set to 1 and if the PCIEINTER[5].INT\_PCIMSE is set to 1, a PCIMES interrupt is generated.

Table 39.4 shows the messages, reception of which is detected by hardware and which are processed by software.

**Table 39.4 Messages Whose Reception can be Detected by the PCIEC**

Register	Bit No.	Register	Bit No.	Receive Message
PCIEINTR	5	PCIERMSGR	12	Set_Slot_Power_Limit
	30	EXPCAP8	17	PM_PME

#### (4) Overview of MSI

This section describes the MSI interrupts.

This module supports MSI interrupts. Whether the PCI Express system should use INTx or MSI interrupts is determined by the Root Port during a configuration cycle. When this module is to be used as a Root Port, whether INTx or MSI interrupt is used should be determined during a configuration cycle, and the results of the determination must be set in the configuration register.

When this module is used as a Root Port, a maximum of 32 interrupt vectors can be used as MSI interrupts. In addition, this module supports both Per Vector Masking and the transmission of 64-bit address messages.

(5) MSI Transmission

MSI can be transmitted only in Endpoint mode. Figure 39.9 shows an MSI transmission flow.

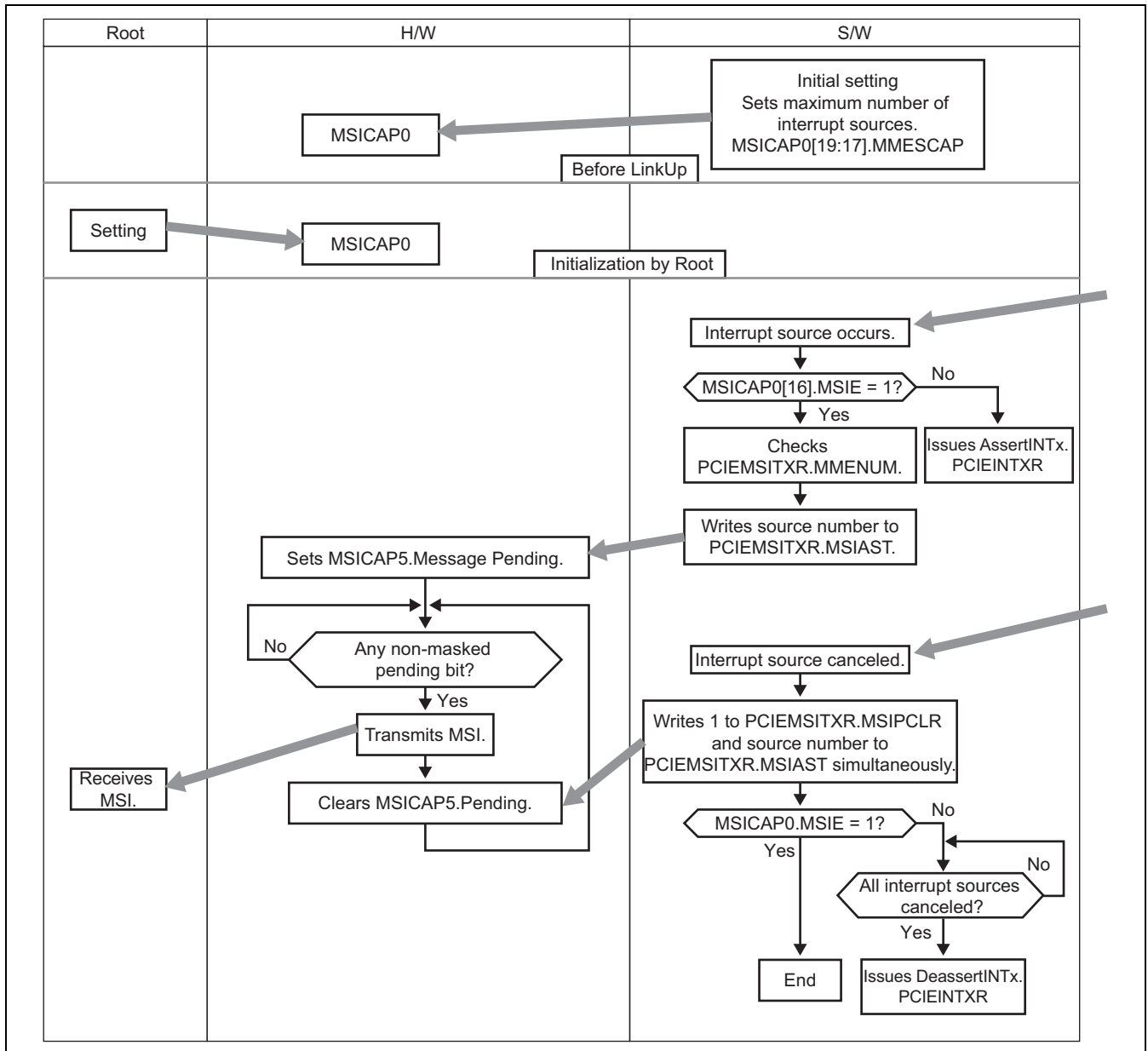


Figure 39.9 MSI Transmission

**(6) MSI Reception**

MSI can be received only in Root Port mode. The following describes a MSI reception flow.

**(a) MSI Interrupt Setting (Root Port)**

When this module is used as a Root Port, whether INTx or MSI interrupts are used should be determined during a configuration cycle. If MSI interrupts are selected, the following settings should be performed.

**(1) Assigning Interrupt Vectors to Endpoints**

Reference the MSICAP0[19:17].MMESCAP of the Endpoint device, and check the number of MSI interrupt vectors required by devices. Based on the result of the checking, the number of vectors to be assigned to the Endpoints is determined so that the number of vectors to be assigned to all devices is 32 or less, the number of vectors assigned to each Endpoint is 1 or greater and less than or equal to the requested number of assignments.

The number of vectors assigned to each Endpoint should be set in the MSICAP0[22:20].MMESE.

**(2) Setting Receive Message Address**

Specify the address to which the MSI is received to PCIEMSI AUR and PCIEMSI ALR and also enable MSI address decoding.

- Notes: 1. When there is a switch or bridge between the Endpoint and this module, set the address so that the memory write request to the address specified by the switch or bridge should be routed to the Root Port, or change the address specified by the switch or bridge and set the address so that the memory write request to the address specified by this module should be routed to the Root Port instead.
- 2. When the specified address falls within the target area, 1DW memory write request to the specified address is not handled as a target transfer, but as an MSI message.

**(3) Setting Endpoint Message Address**

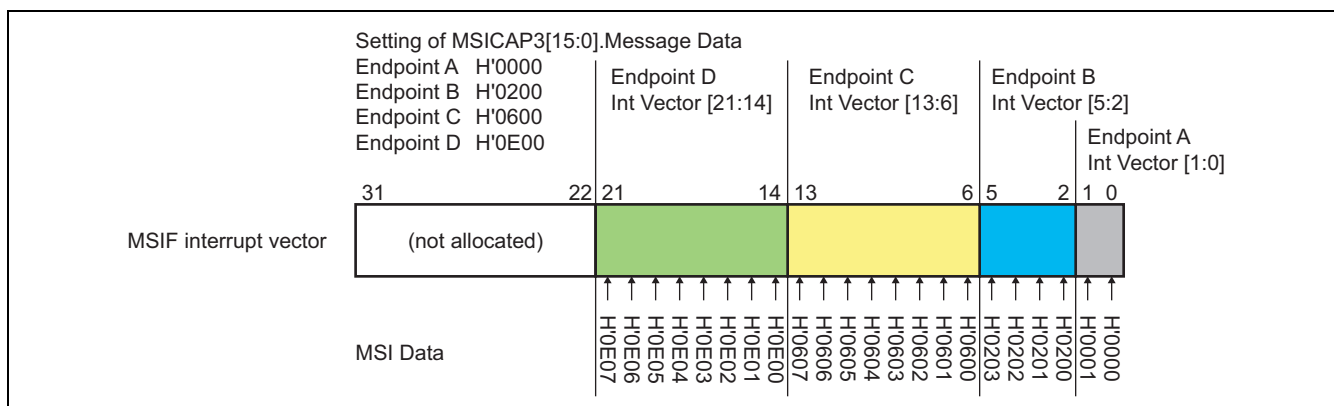
Set the transmission destination address of the MSI message to MSICAP1[31:2].Lower Message Address and MSICAP2[31:0].Upper Message Address of the Endpoint device.

The transmission destination address of MSI message should be the address set to PCIEMSI AUR and PCIEMSI ALR.

**(4) Setting Message Data**

Set the message data for transmission to the MSICAP3[15:0].Message Data of the Endpoint device.

In the 32-bit MSI vectors supported by this module, bits [12:8] in write data must specify the starting vector number of the MSI vectors assigned to the Endpoint, and all other bits must be cleared to 0. Figure 39.10 shows an example of an MSI message data to be set in an Endpoint.



**Figure 39.10 MSI Message Data to be Set in Endpoint**  
**(an example of setting where Vectors 2, 4, 8 and 8 are allocated to Endpoints A, B, C and D, respectively)**

(5) Enabling MSI Interrupts of the Peer Device

Set MSICAP0[16].MSIE of all the devices to 1.

(6) Enabling MSI Interrupts

Set the MSIIE bits.

### 39.3.4 Overview of Transmission and Reception

PCI Express transfers are classified into two types of requests and one type of completion.

The following three methods are provided for PCI Express transactions. For details on each transfer, refer to the following sections.

1. PIO transfer: A request is issued from the internal bus side to a device on the PCI Express.
2. Target transfer: A request is received by the internal bus side from the PCI Express.
3. DMA transfer: A great quantity of data is automatically written and read between the PCI Express and the internal bus without intervention of the CPU.

Table 39.5 shows the relationship between two types of requests and PCI Express transactions and also shows the transaction issuance methods with this module.

**Table 39.5 Relationship between Posted/Non-Posted Requests and PCI Express Transactions**

Transaction Type	Transfer Type	Completion	Device Type that can Issue Transaction	Transaction Issuance Method with This Module	Operation
Memory Write	Posted	Not provided	Root Port &Endpoint	PIO, DMA, (MSI Endpoint only)	Data is written to the memory of the communication peer. 1 byte to 4 Kbytes of data not exceeding MPS* <sup>1</sup> can be written.
Memory Read	Non-Posted	Provided	Root Port &Endpoint	PIO, DMA	A quantity of data not exceeding MRRS* <sup>2</sup> is read from the memory of the communication peer. The read data is returned with a completion separately from this request; no data is included in this request.
I/O Write	Non-Posted	Provided	Root Port only	PIO	Data is written to I/O. Data size is 1 DW. A completion is necessary that indicates whether this request has succeeded.
I/O Read	Non-Posted	Provided	Root Port only	PIO	Data is read from I/O. No data is included. The read data and a completion that indicates whether this request has succeeded are necessary.
Configuration Write	Non-Posted	Provided	Root Port only	PCI Express transfer control register	Configuration write is performed. Data size is 1 DW. A completion is necessary that indicates whether this request has succeeded.
Configuration Read	Non-Posted	Provided	Root Port only	PCI Express transfer control register	Configuration read is performed. No data is included. The read data and a completion that indicates whether this request has succeeded are necessary.
Message	Posted	Not provided	Root Port & Endpoint	Issued by this IP, message transmit register, message transmit module	A message request is transmitted. This is used for power management and interrupt control.



- Notes: 1. MPS: Max Payload Size  
2. MRRS: Max Read Request Size

In Table 39.5, the transactions for which “Provided” is indicated in the “Completion” column, make a response with a completion. The data returned with a completion differs depending on the transaction. Table 39.6 shows the particulars of the completion contents returned. Specifically, the table shows whether completion data for each type of transactions is included or not, the devices that can issue the transaction, and some other related information.

**Table 39.6 Relationship between Completion and PCI Express Transactions**

Transaction Type	Completion Data	Device Type that can Issue Transaction	Transaction Issuance Method with This Module	Operation
Memory Read	Included	Root Port & Endpoint	Automatically issued by this module.	Data requested by memory read request and status are returned.
I/O Write	Not included	Root Port only	Automatically issued by this module.	No data is included. Status in response to I/O write is returned.
I/O Read	Included	Root Port only	Automatically issued by this module.	Data size is 1 DW. The read data and a completion that indicates whether this request has succeeded are returned.
Configuration Write	Not included	Root Port only	Automatically issued by this module.	No data is included. Status in response to configuration write is returned.
Configuration Read	Included	Root Port only	Automatically issued by this module.	Data size is 1 DW. The read data and a completion that indicates whether this request has succeeded are returned.

### 39.3.5 PIO Transfer (Data Transfer from Internal Bus → PCIEC → External Device)

This section describes PIO transfer. PIO transfer here refers to the transfer method to create a PCI Express packet by accessing the memory space assigned to the PCI Express via the internal bus.

#### (1) Overview of PIO Transfer

PIO transfer is the transfer method with which the device on the internal bus transmits a packet to the PCI Express by writing to (or reading from) the space assigned to the PCI Express. When a write access is made, the written data is stored in the data payload of the PCI Express packet. The maximum data size that can be transmitted equals to the maximum data size of an internal bus packet. The type of the PCI Express packet to be transmitted can be specified using the appropriate setting register and either memory read/write or IO read/write can be selected.

Before starting transfer, it is necessary to set the internal bus space that is transferred to the PCIEC and to set the particulars of the packet to be transmitted. Section (2) describes these settings and section (3) describes specific transfer operations.

#### (2) Initial Setting of PIO Transfer

The internal bus address cannot unequivocally define one transfer destination since the address space of the PCI Express, which is the transfer destination, is represented with 64 bits. Therefore, the upper address of the PCI Express space is specified using the PCIEC address upper register  $n$  ( $0 \leq n \leq 3$ ) and PCIEC address lower register  $n$  ( $0 \leq n \leq 3$ ). Set the PCI conversion control register  $n$  (PCIEPTCTLR $n$ ;  $0 \leq n \leq 3$ ) [31].PARE to indicate that such area setting is valid. Set the PCIEC address upper and lower registers at initial setting.

Table 39.7 shows the PIO transfer control registers. The PCIEC memory areas 0 to 3 are mapped to the PCI memory space or I/O space according to the setting of these registers.

**Table 39.7 PIO Transfer Control Registers**

PCIEC address upper registers 0 to 3 (PCIEPAUR0 to PCIEPAUR3)	Address (upper 32 bits) of the PCI address space to which the PCIE memory areas 0 to 3 are to be mapped
PCIEC address lower registers 0 to 3 (PCIEPALR0 to PCIEPALR3)	Address (lower 32 bits) of the PCI address space to which the PCIE memory areas 0 to 3 are to be mapped
PCIEC address mask registers 0 to 3 (PCIEPAMR0 to PCIEPAMR3)	Specify the size in the PCIE memory areas 0 to 3 to be mapped to the PCI address space.
PCIEC conversion control registers 0 to 3 (PCIEPTCLR0 to PCIEPTCLR3)	Specify whether the PCI space is valid or invalid. Specify the transfer destination space (PCI memory space or PCI IO space). Specify attributes (TC, LOCK, ZLR, and ATTR) for conversion.

Table 39.8 shows the PCI Express memory area addresses on the AXI bus space.

**Table 39.8 AXI Bus Space Address Map**

Memory Area	Address	Physical Address Size
PCIEC memory 0	H'00_FE10_0000 to H'00_FE1F_FFFF	1 Mbyte
PCIEC memory 1	H'00_FE20_0000 to H'00_FE3F_FFFF	2 Mbytes
PCIEC memory 2	H'00_3000_0000 to H'00_37FF_FFFF	128 Mbytes
PCIEC memory 3	H'00_3800_0000 to H'00_3FFF_FFFF	128 Mbytes

The following shows the example of mapping the internal bus space to the PCIEC address space.

Example of mapping the internal bus space to the PCIEC address space:

```

PCIEC address lower register 0[31:0] = H'0000 0000
PCIEC address lower register 1[31:0] = H'5640 0000
PCIEC address lower register 2[31:0] = H'2000 0000
PCIEC address lower register 3[31:0] = H'8000 0000
PCIEC address upper register 0[31:0] = H'0000 0000
PCIEC address upper register 1[31:0] = H'0000 0008
PCIEC address upper register 2[31:0] = H'0000 0000
PCIEC address upper register 3[31:0] = H'0000 0000
PCIEC address mask register 0[31:0] = H'0000 FF80
PCIEC address mask register 1[31:0] = H'001F FF80
PCIEC address mask register 2[31:0] = H'1FFF FF80
PCIEC address mask register 3[31:0] = H'1FFF FF80
PCIEC conversion control register 0[31:0] = H'8000 0100
PCIEC conversion control register 1[31:0] = H'8000 0000
PCIEC conversion control register 2[31:0] = H'8000 0000
PCIEC conversion control register 3[31:0] = H'8000 0000

```

Figure 39.11 shows an example of mapping the internal bus space to the PCI Express space with the above setting.

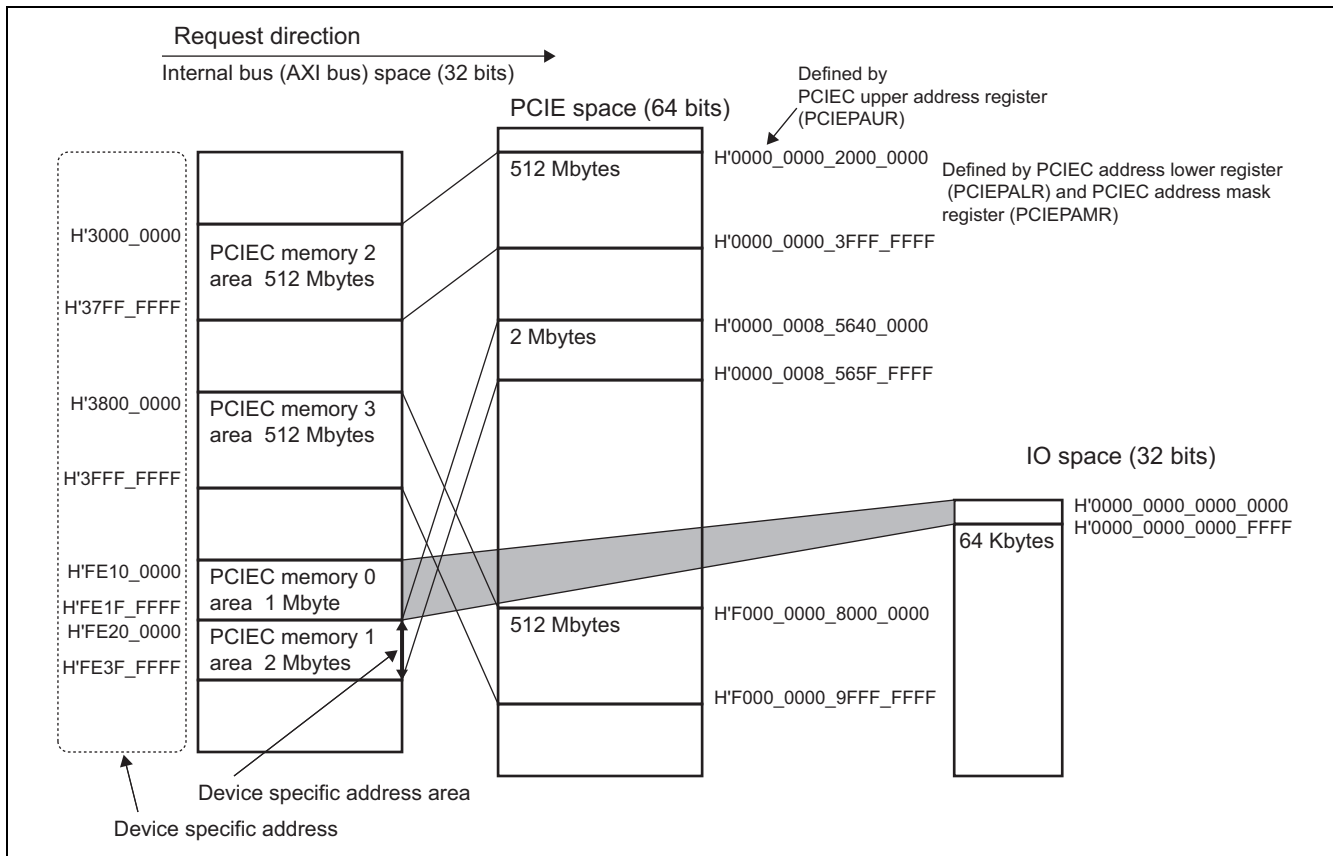


Figure 39.11 Example of Address Mapping for PIO Transfer

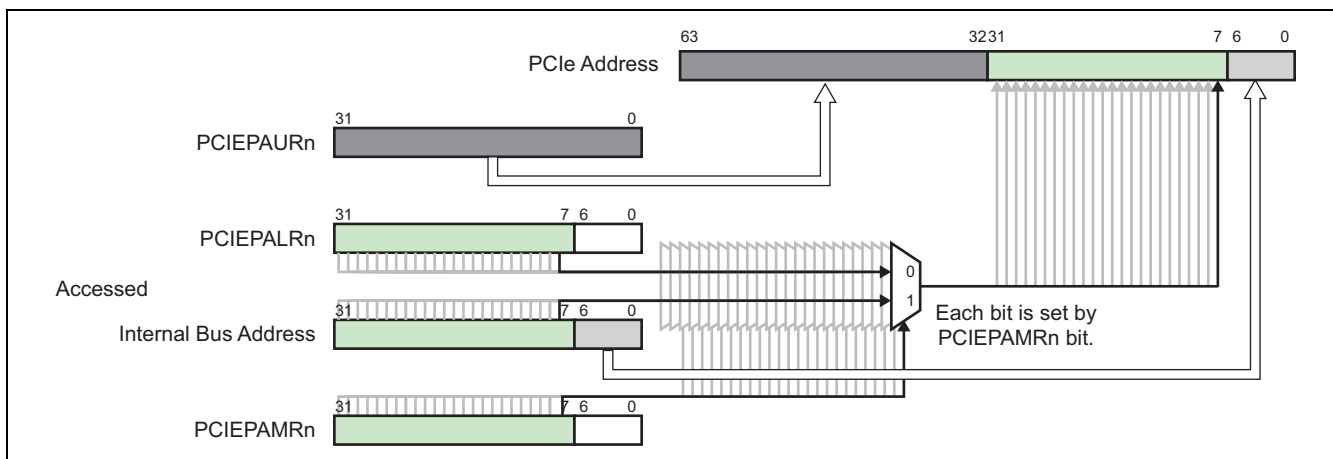
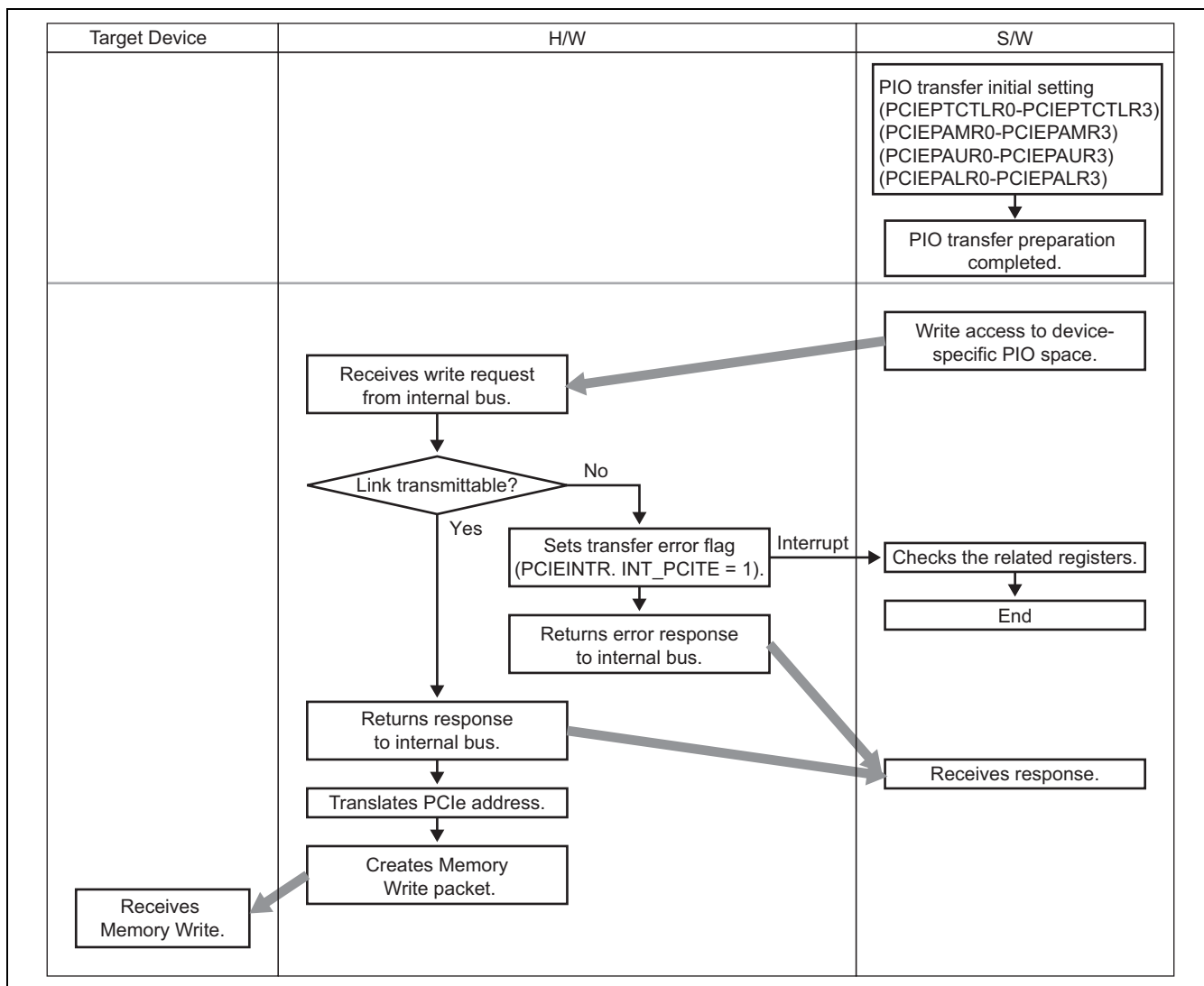


Figure 39.12 Address Translation for PIO Transfer

**(3) PIO Transfer Operation**

PIO transfer performs memory write/read to the corresponding memory/IO space on the PCI Express from the internal bus side. In reading, a read request is issued to the PCI Express, a completion from the device to be read is converted to data (response), and it is written to the area in the internal bus. Figures 39.13 and 39.14 show write and read operations of PIO transfer, respectively. In the figures, the processes for which “Check the related registers.” is indicated are software-dependent; perform appropriate processing for the application.



**Figure 39.13 PIO Transfer Operation (memory write request)**

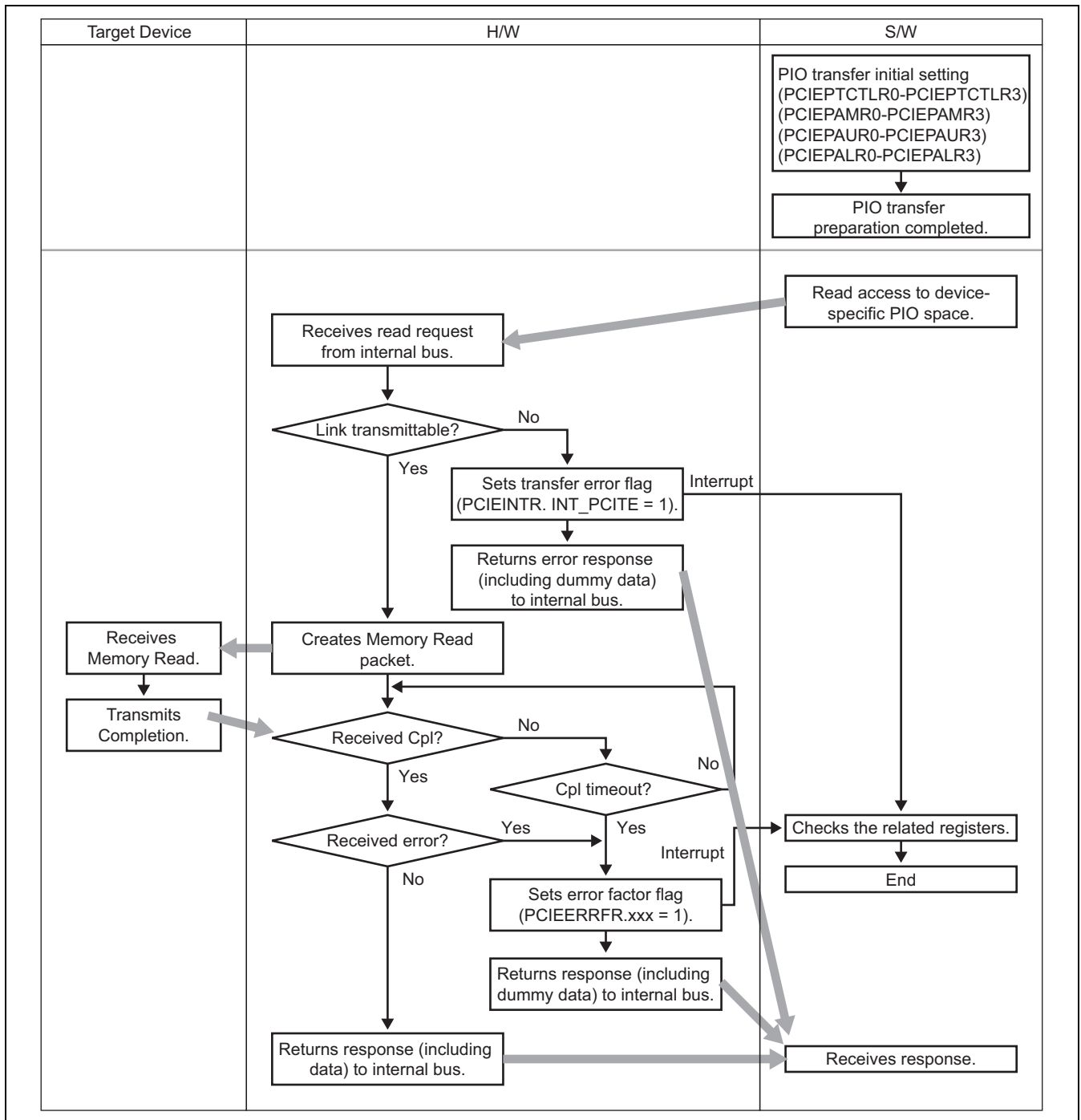


Figure 39.14 PIO Transfer Operation (memory read request)

### 39.3.6 Target Transfer (Data Transfer from External Device → PCIEC → Internal Bus)

With target transfer, the device on the PCI Express accesses the device on the internal bus of this module through a PCI Express request packet.

#### (1) Overview of Target Transfer

Using target transfer, the device on the PCI Express can send packets for memory read/write and I/O read/write to read from and write to the area in the internal bus.

In a target transfer, this module can receive packets of any data length less than or equal to the size specified in the MPS (Max Payload Size).

#### (2) Initial Setting of Target Transfer

The assignment of addresses in the PCI Express space is dynamically determined by the Root Port during a configuration cycle, based on the register settings at initialization. At initialization, the registers are set to specify the parameters such as the sizes of various areas and types of the areas (memory space, I/O space, or the other). When CFINIT is set to 1 and initialization is completed, the initial setting is reflected to BARn (Base Address Register n) of the configuration registers. In Root Port mode, PCIEPRARn is set through software. Here, BAR indicates the area to be released in response to the request from the downstream. In Endpoint mode, the BARn bits of configuration registers are set in the subsequent configuration cycle.

As an area in which memory space is to be allocated, this module supports either 64-bit PCI address space or 32-bit PCI address space (the first 4G area of the 64-bit space). When allocating an area in 32-bit address space, one BARn is used; when allocating an area in 64-bit address space, two contiguous BARn registers (BARn+1/BARn) are used. For this reason, a maximum of three 64-bit address space areas can be allocated.

In I/O space, areas are allocated using one PCIEPRAR or BAR register.

In Root Port mode, set the internal bus side space to be correlated to each of the PCIEPRAR registers in the PCI Express space to the local (internal bus) address registers 0 to 5 (PCIELAR0 to PCIELAR5). Also set the size to be allocated and the space type to the local (internal bus) address mask registers 0 to 5 (PCIELAMR0 to PCIELAMR5). Set these registers before a link is established (before setting CFINIT to 1). Although PCIEPRAR can be modified after a link is established, turn off the Master Enable of the communication peer or take other appropriate measures to prevent issuance of a request to the corresponding area during PCIEPRAR modification.

In Endpoint mode, set the internal bus side space to be correlated to each of the BAR registers in the PCI Express space to the local (internal bus) address registers 0 to 5 (PCIELAR0 to PCIELAR5). Also set the size to be allocated and the space type to the local (internal bus) address mask registers 0 to 5 (PCIELAMR0 to PCIELAMR5). Set these registers before a link is established (before setting CFINIT to 1).

The target transfer area must not be allocated to the internal bus space for the registers of this module or to the internal bus space for PIO transfer.

The following shows the example of mapping the PCI Express address space to the internal bus space.

Example of mapping the PCI Express address space to the internal bus space (Root Port):

Figure 39.15 shows an example of mapping the PCI Express space to the internal bus space (Root Port).

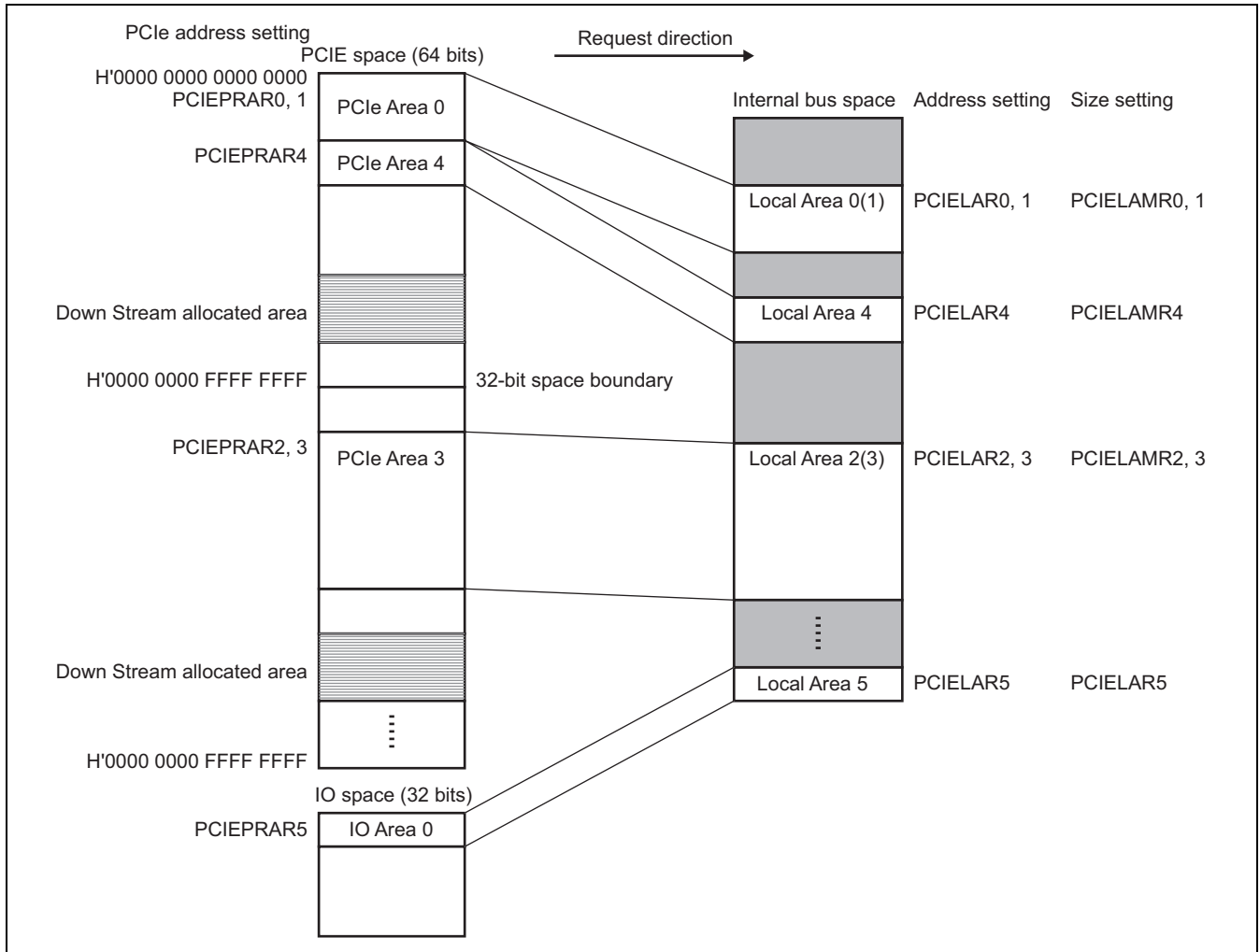
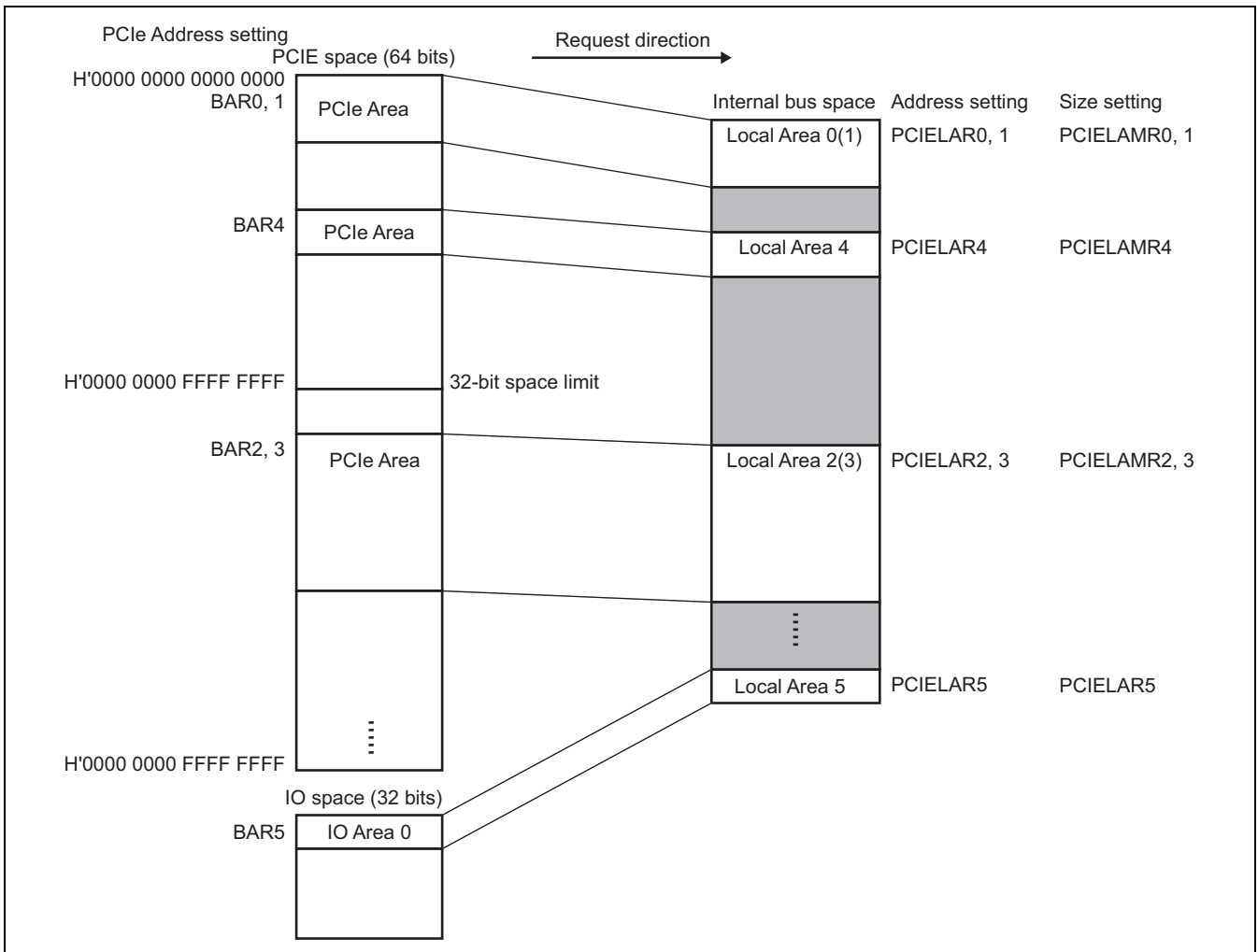


Figure 39.15 Example of Mapping PCI Express Address Space to Internal Bus Space (Root Port)

Example of mapping the PCI Express address space to the internal bus space (Endpoint):

Figure 39.16 shows an example of mapping the PCI Express space to the internal bus space (Endpoint)



**Figure 39.16 Example of Mapping PCI Express Address Space to Internal Bus Space (Endpoint)**



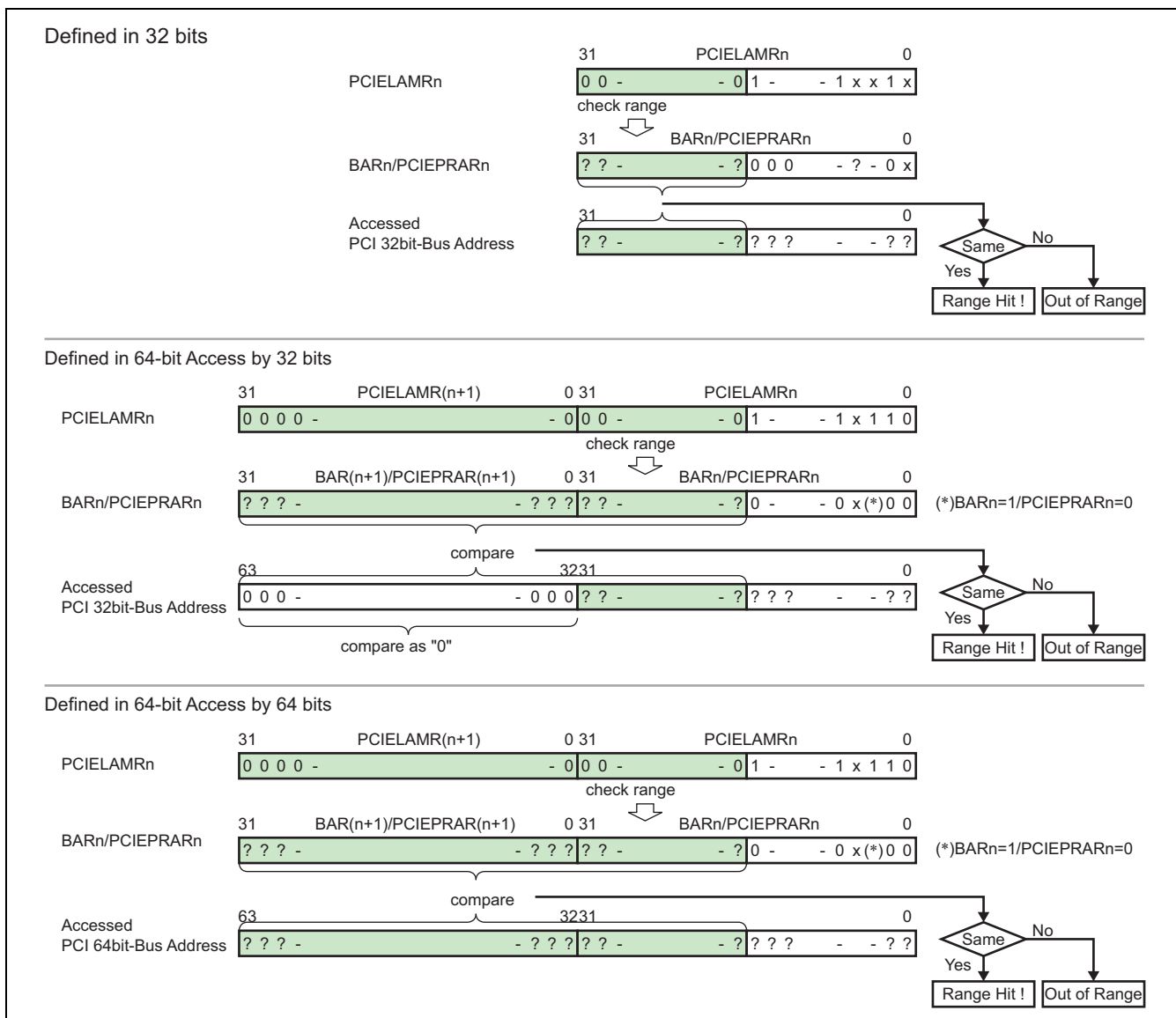


Figure 39.17 Address Comparison for Target Transfer

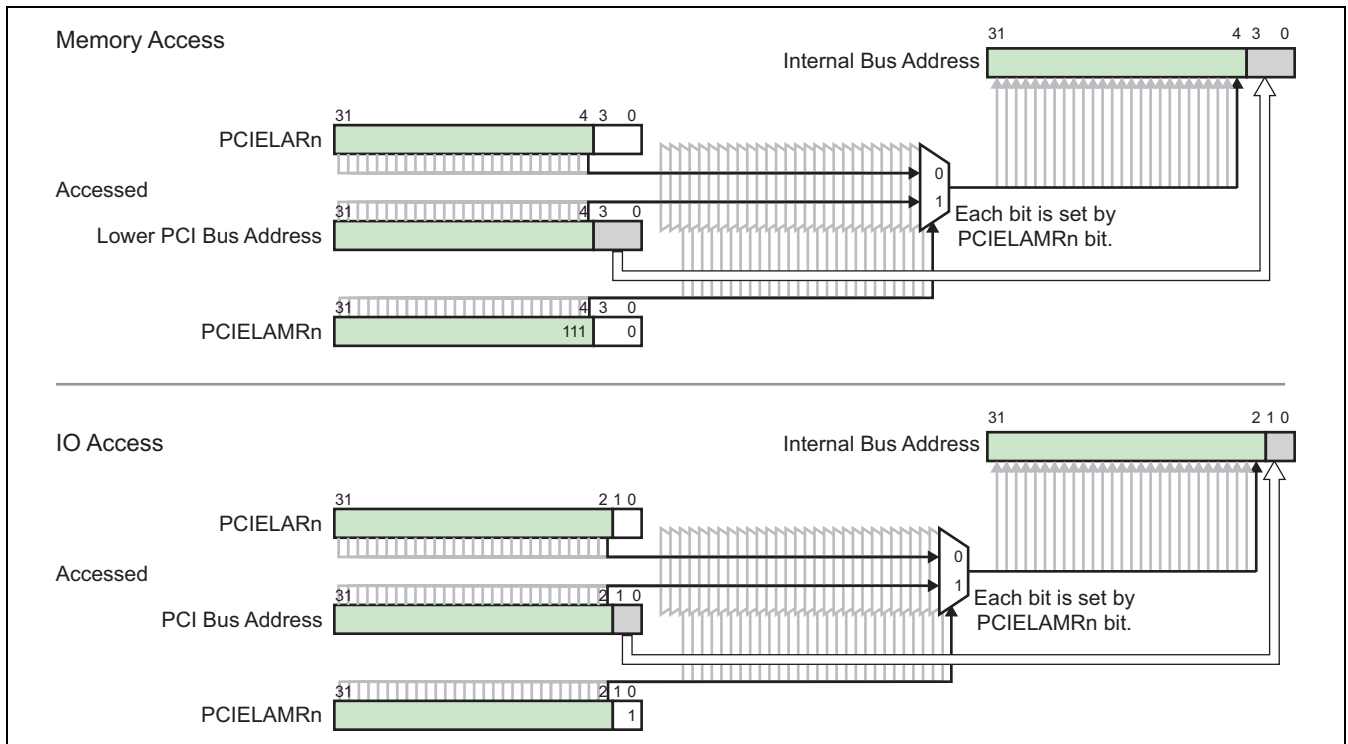
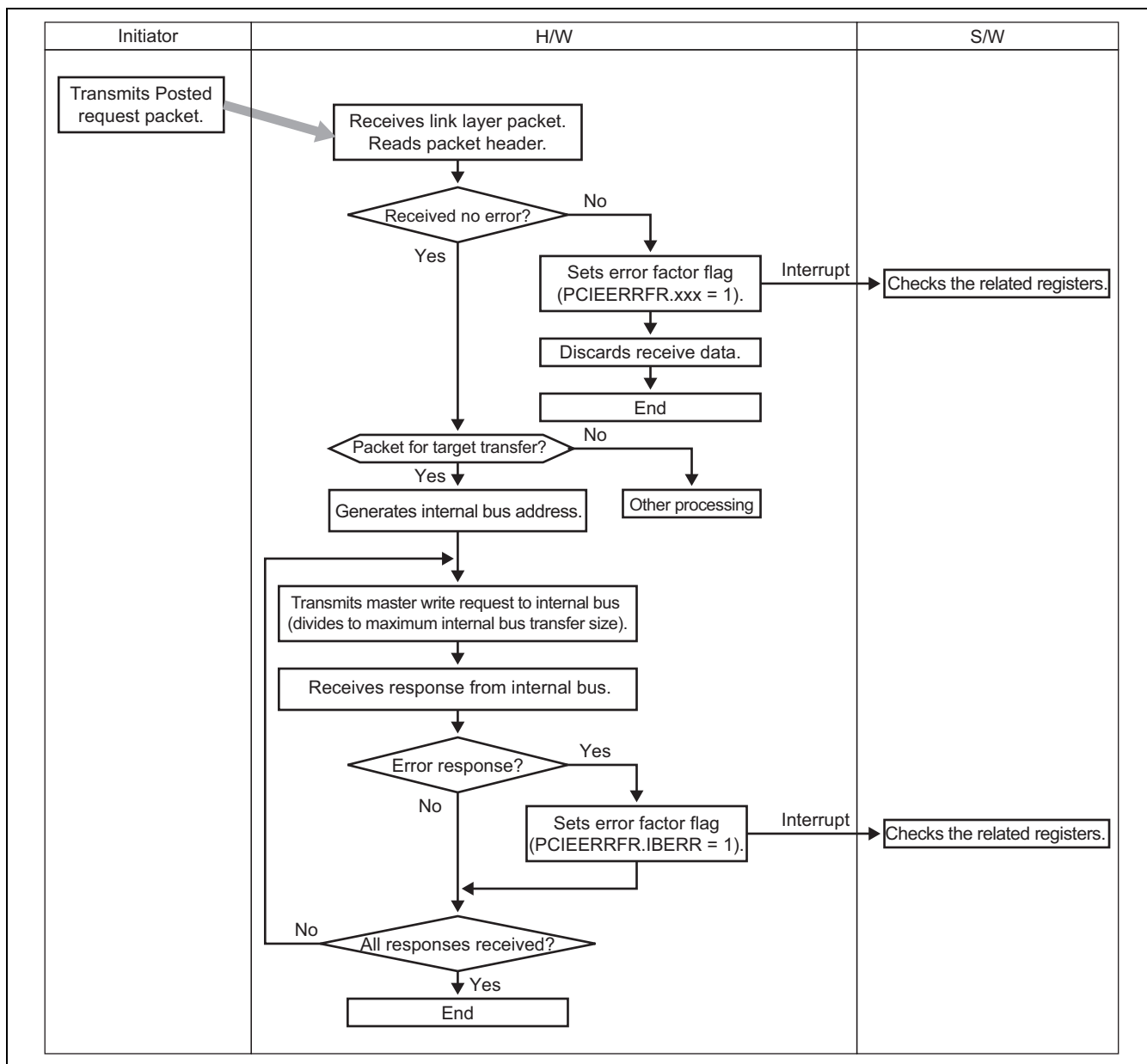


Figure 39.18 Address Translation for Target Transfer

**(3) Target Transfer Operation**

Figures 39.19 and 39.20 show the target transfer operations to receive a memory write request and the other request, respectively. In receiving a memory write request, the received data is written to the corresponding internal bus address. In receiving the other request, the internal bus is accessed, a completion packet is created and returned (note that when the internal bus is read, all the byte lanes are accessed irrespective of the PCIe space setting (prefetchable or non-prefetchable type) since the internal bus does not have a read strobe).



**Figure 39.19 Target Transfer (Reception of a Memory Write Request)**

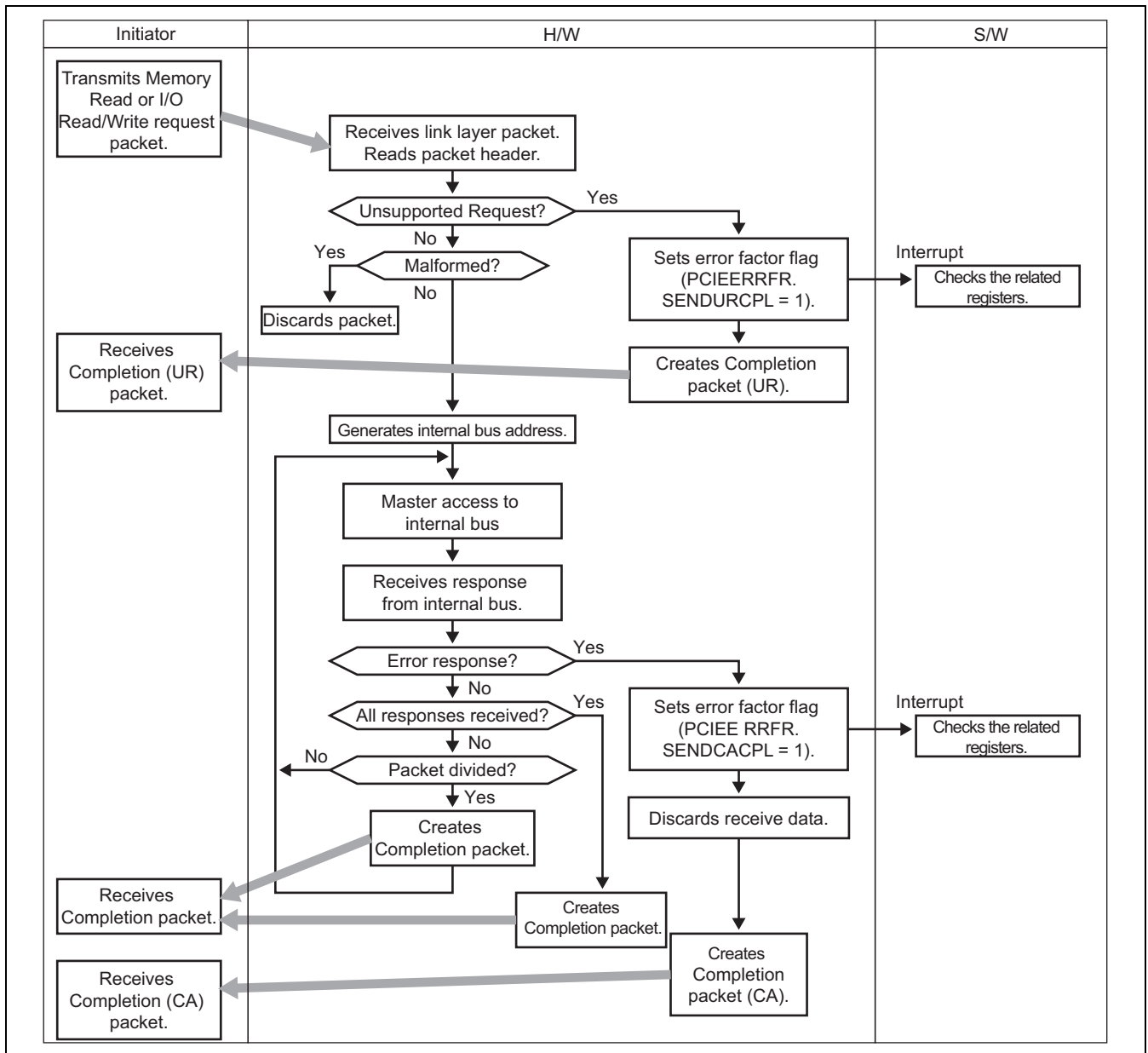


Figure 39.20 Target Transfer (Reception of a Request Other than a Memory Write Request)

### 39.3.7 DMA Transfer

This section describes the DMA transfer using the DMAC (PCIEC-DMAC) incorporated in this module.

#### (1) Overview of DMA Transfer

The PCIEC-DMAC enables effective data transfer between the PCI Express and the internal bus area. The PCIEC-DMAC can perform a maximum of  $2^{29}$  count of transfer without intervention of the CPU.

The PCIEC-DMAC supports the command chain function, which allows consecutive execution of multiple transfer commands. With the command chain function, the DMAC-related setting information, such as the addresses of the transfer destination and source and transfer size, is considered as a command; by reading and executing these commands from the memory one by one, consecutive execution of multiple transfer units is provided without intervention of the CPU.

The PCIEC-DMAC has the following features.

- Number of channels: 8 channels
- Address space: PCI Express = 32/64 bits, internal bus = 32 bits
- Transfer data length: PCI Express = 8 to 128 bytes, internal bus = 8 to 128 bytes
- Maximum transfer count: 536,870,912 ( $2^{29}$ )
- Address mode: Dual address mode
- Transfer request: Started by register control
- Data transfer: Normal mode (continuous transfer), command chain
- Priority: Either channel priority fixed mode or round-robin mode selectable
- Interrupt request: Interrupts can be requested to the INTC when a data transfer has completed or an error has occurred.

#### (2) Initial Setting of DMA Transfer

Set the PCI Express and internal bus addresses, byte count, transfer end interrupt. When the command chain is not used, set the PCIEDMCHCRn.CCE to 0. In the DMA transfer (internal bus side), access to the internal bus space for the registers and access to the internal bus space for PIO transfer are prohibited.

#### (3) DMA Transfer Operation

DMA transfer can be initiated by simultaneously setting the transfer direction and enabling the channels with PCIEDMCHCRn. Transfer end is detected by confirming PCIEDMCHSRn[0].TE = 1 or detecting a transfer end interrupt. After transfer is ended, transfer is completed by setting PCIEDMCHCRn[31].CHE to 0. Simultaneously, PCIEDMCHSRn[0].TE is set to 1 to clear this bit.

Figures 39.21 and 39.22 show DMA transfer from the internal bus to the PCI Express space and from the PCI Express space to the internal bus, respectively.

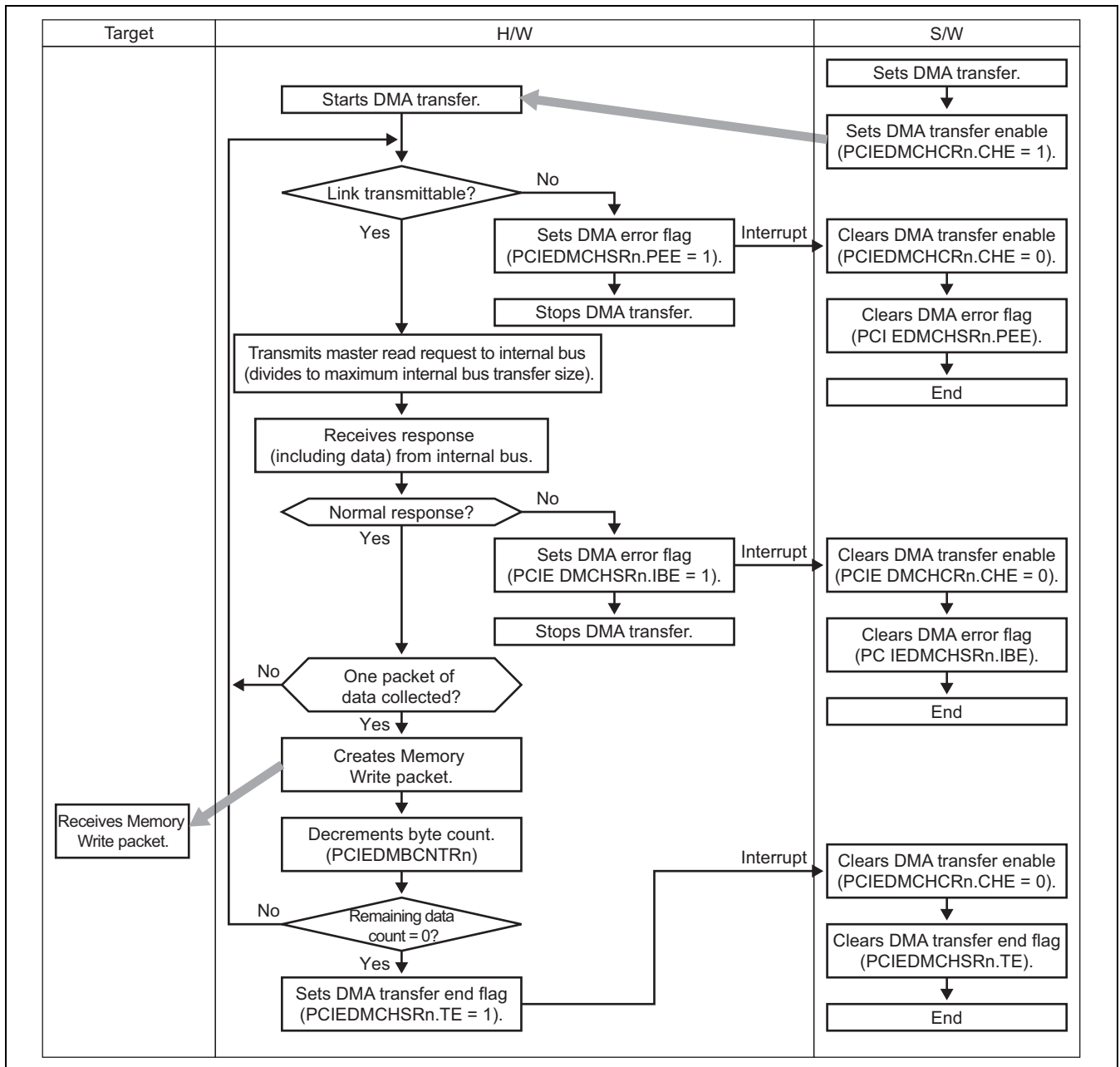


Figure 39.21 DMA Transfer (Internal Bus → PCI Express)

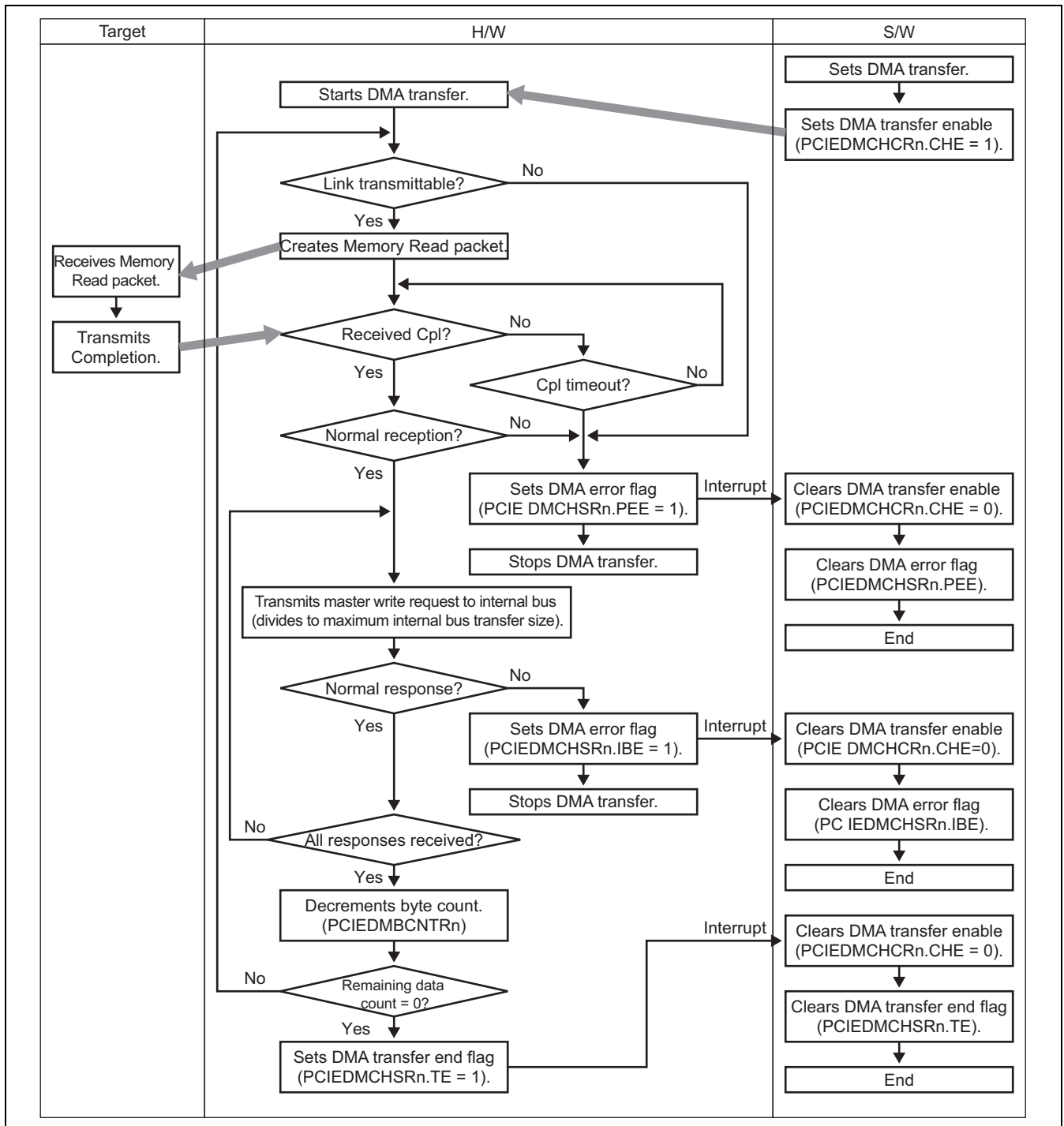


Figure 39.22 DMA Transfer (PCI Express → Internal Bus)

#### (4) DMA Channel Priority

When more than one DMA channel is used simultaneously, they are actually used according to the priority described in this section. The priority can be set with the PCIEDMAOR register. Set the relevant bit at the same time as setting PCIEDMAOR.DMAE to 1.

The channel priority is initialized to CH0 > CH1 > CH2 > CH3 > CH4 > CH5 > CH6 > CH7 while PCIEDMAOR.DMAE = 0.

##### (a) Arbitration Timing between DMA Channels

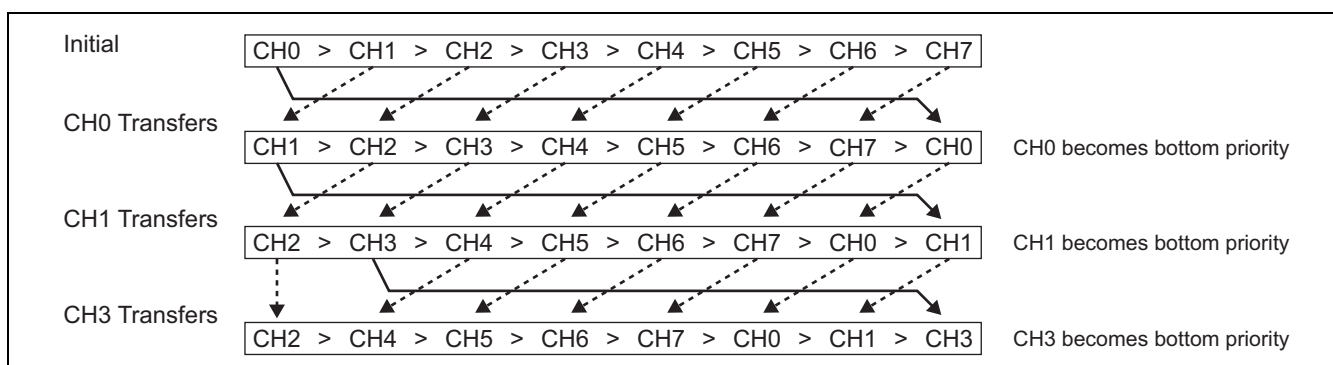
Arbitration is performed every transfer unit (128 bytes max.) of the DMA channel currently transferring data.

##### (b) Fixed Mode

When PCIEDMAOR.ABT is 0, the priority is fixed to the default setting.

##### (c) Round Robin Mode

When PCIEDMAOR.ABT is 1, round robin scheduling is applied to all the channels to determine the priority. When a certain channel completes transfer, the channel is given a bottom priority and the channels that have been given a lower priority than that channel are given a higher priority as shown in Figure 39.23.



**Figure 39.23 Round Robin Scheduling among All the Channels**

#### (5) Dividing Packet at Address Boundary

If the PCI Express side address or internal bus address of a packet crosses the 4-Kbyte boundary, the packet is divided.

#### (6) Command Chain

##### (a) Overview of Command Chain Operation

A command chain allows this module to continuously execute multiple DMAC commands. A DMAC command refers to a set of information related to the PCIEC-DMAC transfer; that is, the information specified by PCIEDMPALR<sub>n</sub>, PCIEDMPAUR<sub>n</sub>, PCIEDMIAR<sub>n</sub>, PCIEDMBCNTR<sub>n</sub>, PCIEDMCCAR<sub>n</sub>, and PCIEDMCHCR<sub>n</sub>. As well as in the PCIEC-DMA control register, the information can also be set in the memory in the format shown in Figure 39.24. With the command chain, each time a DMAC command execution is completed, the next DMAC command is read from memory and the content of the DMAC command is written to the relevant PCIEC-DMA control register, which allows execution of the DMAC command.

By specifying the next DMAC command in the DMAC command to be read, a command chain is created and thus data can be transferred consecutively.

During command chain operation, a DMAC command is read from the memory address indicated by PCIEDMCCAR<sub>n</sub> and the content of the read command is written to the register of the relevant channel to execute the command. If the CCE bit in the read DMAC command is 1, the next command is read from memory again and executed upon completion.



of the current command. If the CCE bit in the read DMAC command is 0, completion of the command completes the command chain operation.

### (b) Initial Setting of Command Chain

To start a command chain on a channel, enable the channel while PCIEDMCHCRn.CCE is set to 1. Before starting a command chain, store a chain of DMAC commands in a memory location accessible from the internal bus, and set the address of the first DMAC command in PCIEDMCCARn.

Note: As the setting (information) of the first transfer of the command chain, the information in the memory specified with PCIEDMCCARn is used; the setting in the PCI Express-DMA control registers is not used (here, any setting other than PCIEDMCCARn is ignored).

### (c) DMAC Command Format

Figure 39.24 shows the format of DMAC commands to be stored in memory. Set each field of the commands as described below and store such commands.

- CHE field: Always set 1.
- CCE field: Set 0 for the command to be executed last; set 1 for the other commands.
- CCA field: Set 0 in all the bits for the command to be executed last; set the address of the next command for the other commands.
- Reserved field: Always set 0.

Offset	Registers	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00	DMPALR	PADRL																												R			
04	DMPAUR	PADRU																															
08	DMIAR	IADR																												R			
0C	DMBCNTR	R	BCNT																										R				
10	-	R																															
14	-	R																															
18	DMCCAR	CCA																												R			
1C	DMCHCR	CHE	DIR	CCE	R								ATTR	R						TC	R												

R=Reserved

Figure 39.24 Formats of DMAC Commands

### (d) Channel Priority for Command Read

While the command chain operation is in progress on multiple DMA channels, DMAC command read requests are issued from the multiple DMA channels; here, round robin scheduling is applied to all the channels to determine the priority (refer to section 39.3.7 (4)(c), Round Robin Mode).

Note: The channel priority here is different from the priority of the DMA transfer operation specified with PCIEDMAOR.

The channel priority is initialized to CH0 > CH1 > CH2 > CH3 > CH4 > CH5 > CH6 > CH7 while PCIEDMAOR.DMAE = 0.

## (7) Notes on DMA Transfer

### (a) Handling upon DL\_Down → DL\_Active

If a DL\_Down occurs during DMA transfer, it is handled as a transfer error on the PCI Express side and thus transfer is ended after PCIEDMCHSRn.PEE is set. However, if a request is being made to the internal bus when a DL\_Down occurs, a response to the request is first received and then flag is set and transfer is ended. Therefore, not all the operations are stopped immediately after a DL\_Down.

When returned from a DL\_Down to DL\_Active, first read PCIEDMAOR.DMAACT = 0 to confirm that all the channels that have been operating before DL\_Down have stopped operating, and then re-set DMA and perform transfer again.

### 39.3.8 Transfer Priority

This section describes the transfer priority.

#### (1) Arbitration (Transmission to PCI Express)

Accesses to transmit packets to the PCI Express include: DMA transfer, response processing to target transfer, PIO transfer, and Message transfer. The DMAC and the modules controlling PIO transfer output posted and non-posted requests, respectively.

Arbitration between these accesses is performed according to the priority shown below.

(High priority)

- Completion of target transfer (configuration)
- Completion of target transfer (memory, IO)
- PIO transfer (configuration, memory read, IO)
- PIO transfer (memory write)
- Various messages
- DMA transfer (memory read)
- DMA transfer (memory write)

(Low priority)

#### (2) Arbitration (Reception from PCI Express)

The completion receiver and request receiver receive packets from the PCI Express and make reception access requests.

Arbitration between these accesses is performed according to the priority shown below.

(High priority)

- PCIEC completion receiver
- PCIEC request receiver

(Low priority)

The PCIEC link of this module, which processes the PCIe protocol, processes packets received from the PCI Express one by one in order of reception. After that, the processed packets are sequentially distributed to the target receiver, DMA receiver, message receiver, and PIO receiver according to the type of the received packet and then processed one by one there. If the receiver corresponding to the processing target is waiting for a certain process to be completed (for example, waiting for a request to the internal bus or a response), the PCIe link starts the next reception process after completion of the process. Until completion, the next packet is suspended from being processed.

### (3) PCI Express Transmit/Receive Ordering

The following describes the transaction ordering rules of this module.

Table 39.9 shows the transmit transaction ordering rules of this module.

**Table 39.9 Transmit Transaction Ordering Rules of This Module**

Row Pass Column?	1st Posted	1st Non-Posted	1st Completion
2nd posted	No	Yes	Yes
2nd non-posted		No	Yes
2nd completion		Yes	No

Note: Yes: The second transaction can pass the first transaction.

No: The second transaction cannot pass the first transaction.

Table 39.10 shows the receive transaction ordering rules of this module.

**Table 39.10 Receive Transaction Ordering Rules of This Module**

Row Pass Column?		1st Transaction						
		Request					Completion	
		Posted	Non-Posted					
		Memory Write/Message	Memory/IO Read	IO Write	Configuration Write/Read	Read/Write	Memory Read (DMA)	
2nd transaction	Posted	Memory write/message	No*	Yes	Yes	Yes	Yes	Yes
	Non-posted	Memory/IO read	No	Yes	No	Yes	Yes	Yes
		IO write request	No*	Yes	No	Yes	Yes	Yes
		Configuration write/read	No	Yes	Yes	No	Yes	Yes
Completion	Read/write	Yes	Yes	Yes	Yes	No	Yes	
	Memory read (DMA)	Yes	Yes	Yes	Yes	Yes	No	

Notes: Yes: The second transaction can pass the first transaction.

No: The second transaction cannot pass the first transaction.

\* For Memory/IO Write, the second request cannot pass the first request if they are issued to the same BAR space; the second request may pass the first request if issued to the different BAR spaces. For a combination of Memory Write and Message, the second request may pass the first request.

This module applies the ordering rules conforming to the standard to the transmission and reception sides. According to the rules, some packets cannot be passed by (to prevent an undesired influence on the order of sequential processing and such). Therefore, depending on the packet transfer order or combination, processing of a packet may be delayed until the previous packet processing is completed.

**(4) Arbitration (Bus Master Request)**

Accesses to output a master write request to the internal bus include: DMA transfer, target transfer, and message transfer.

Arbitration between these accesses is performed according to the priority shown below.

(High priority)

- Target transfer (reception of memory write and IO write)
- DMA transfer (reception of completion for memory read)

(Low priority)

Accesses to output a master read request to the internal bus include: DMA transfer, target transfer, and message transfer.

Arbitration between these accesses is performed according to the priority shown below.

(High priority)

- Target transfer (reception of memory read and IO read)
- DMA (command read)
- DMA (transmission of memory write)

(Low priority)

### 39.3.9 Link Function

#### (1) Changing Speed

The PCI Express 2.0 standard allows changing of the transfer speed intentionally or to handle the problem related to the link reliability. Figure 39.25 shows a flow of changing the transfer speed to 5.0 GT/s.

- Allow the factor of speed change to be generated while speed change is enabled. (According to the PCI Express 2.0 standard, if speed change is attempted by itself and ends in failure, starting of speed change by itself is prohibited for 200 ms.)
- If speed change is attempted while another speed change is in progress, it is impossible to know which speed change factor is used for judging the end of speed change. For reliable judgment of the end of speed change, do not make any attempt to change a speed during another speed change. (MACCTLR.SPCHG == 0 and MACSR.SPCHGFIN == 0 indicate that speed change has not been set or speed change processing is not in progress.)

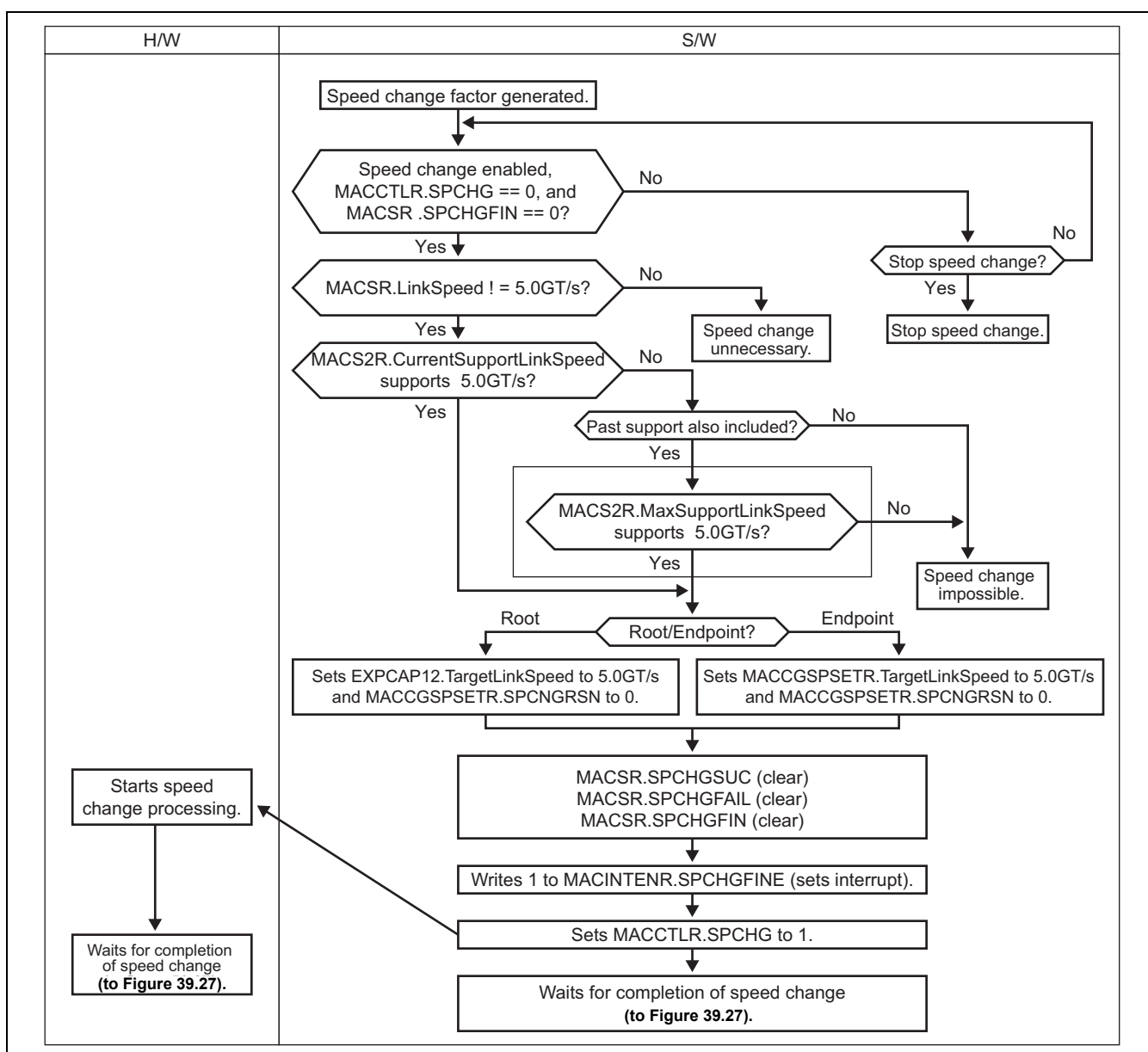


Figure 39.25 Changing Speed to 5.0 GT/s

Figure 39.26 shows a flow of changing the transfer speed to 2.5 GT/s.

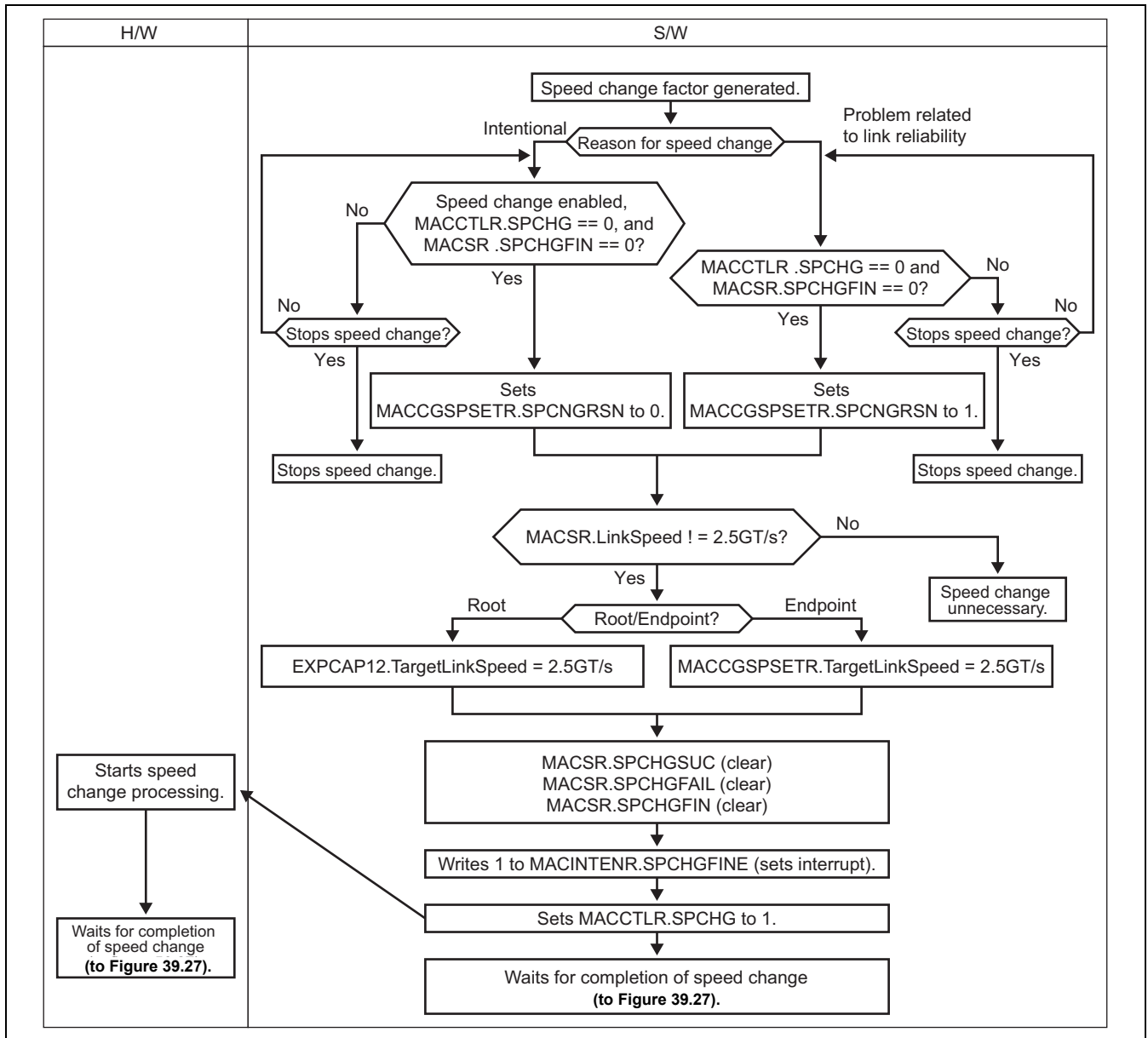


Figure 39.26 Changing Speed to 2.5 GT/s

Figure 39.27 shows a flow of the ending process for the transfer speed change.

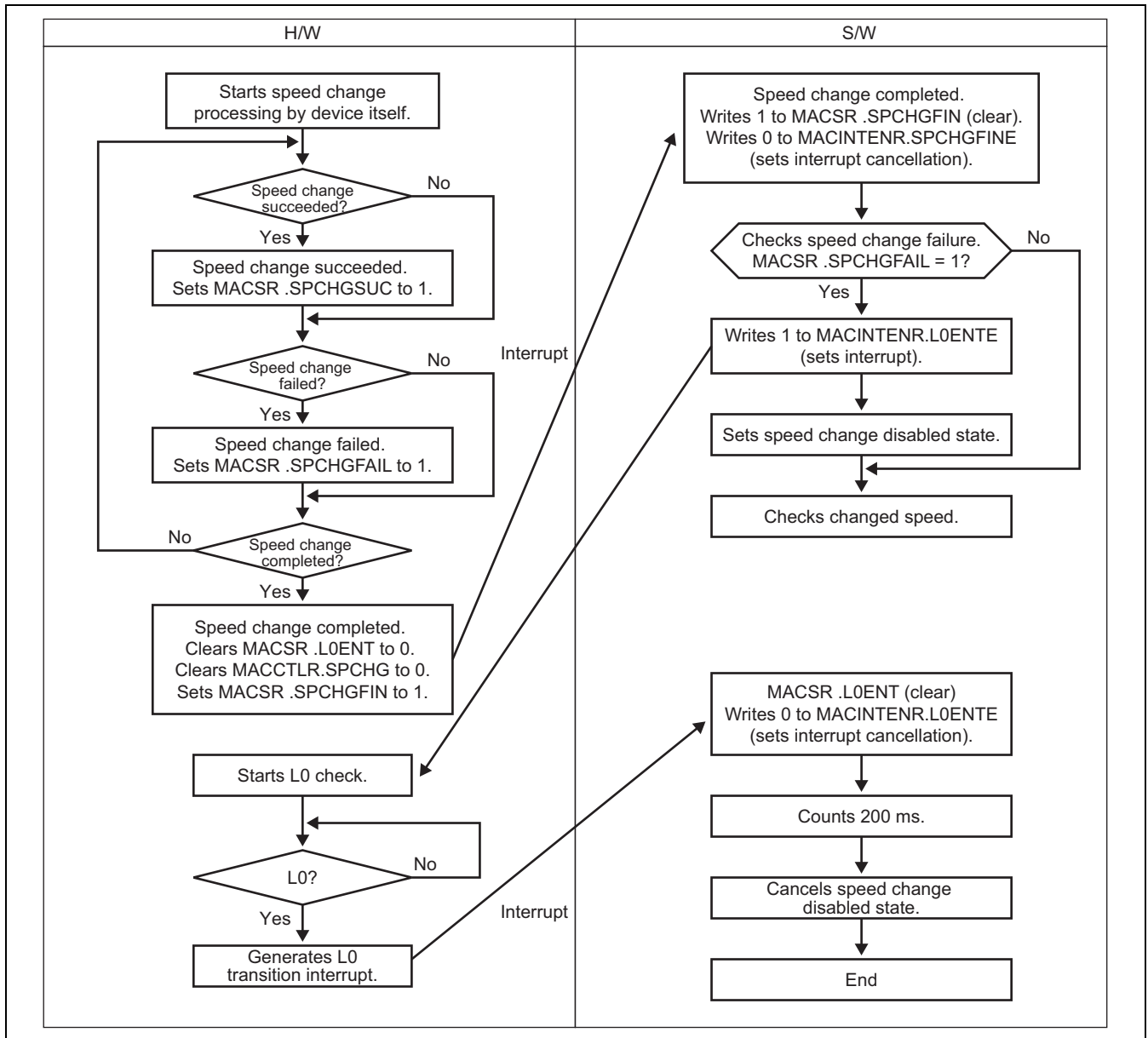


Figure 39.27 Ending Process of Speed Change

### 39.3.10 Power Management

This section describes power management of this module. This module has two power management modes below.

- PCI-PM
- ASPM (L0s)

PCI-PM is PCI-compatible and ASPM is specific to PCI Express. ASPM mode supports L0s only.

#### (1) PCI-PM

This section describes PCI-compatible power management mode. Table 39.11 shows power management operations in PCI-PM mode.

**Table 39.11 PCI-PM Operations**

No.	Transition	Target Device
1	L0 → L1 → L0	Endpoint
2		Root port

#### (a) L0 → L1 → L0 (Endpoint)

After modification of the Power State field, initiate the L1 transition sequence through software according to the flowchart shown in Figure 39.28.

After initiated through software, the L1 transition sequence is performed through hardware according to the following procedure.

1. Prepares for L1 transition.
  2. Processes the handshake with the peer device for L1 transition.
  3. Causes the LTSSM of this module to make an L1 transition.
- Triggered by a write of PMCTLR.L1IATN = 1, hardware initiates the L1 transition sequence. As preparation for causing L1 transition, this module first allows hardware to automatically perform the following. (1) Waits for the minimum amount of credits to be accumulated necessary to transmit the largest TLP for which all the types of credits are configured. (2) Waits for the retry buffer to be empty. (3) Waits for all the TLP to be transmitted.
  - After completion of the above preparation, this module transmits PM\_Enter\_L1 DLLP and receives PM\_Request\_Ack DLLP to process the handshake with the peer device for L1 transition.
  - After completion of the handshake for L1 transition, this module disables TLP/DLLP transmission and directs the LTSSM to make a transition to L1. If directions are given to make a transition to the detect or recovery state before the LTSSM completes L1 transition, this module gives priority to a transition to the detect or recovery state.
  - Hardware clears the PMCTLR.L1IATN bit to 0 when the LTSSM makes a transition to the state other than L0, recovery, and configuration, that is, when the LTSSM makes a transition to L1 (PMSR.PMSTATE = L1) properly or LDn (PMSR.PMSTATE = LDn). Simultaneously, the PMSR.L1FAEG bit is set. Software can confirm that TLP write is again enabled and the transition destination by reading PMSR.L1FAEG = 1 and PMSR.PMSTATE. After confirming PMSR.L1FAEG = 1, write 1 to PMSR.L1FAEG to clear the bit.
  - After initiation of the L1 transition sequence, if transitions are made as L0 → recovery → L0 or L0 → recovery → configuration → L0 before a transition to the L1 state is caused, hardware automatically initiates the L1 transition sequence again. Therefore, software has nothing to process. PMSR.L1FAEG is not set.

The sequence for a recovery from L1 is performed under the following conditions.

1. Cases in which recovery is initiated by this module itself (caused by software)



Software gives directions to transmit the PM\_PME message to prepare for communication again; or an error message is transmitted through software processing.

The message of the error caused by the PM\_PME message is scheduled for transmission by software when the PM\_PME message transmission is supported. Be sure to confirm that a transition to L1 has been properly made (PMSR.L1FAEG = 1 and PMSR.PMSTATE = L1) before scheduling.

2. Cases in which recovery is initiated by the peer

The receive lane becomes no longer electrically idle.

Typical example: The peer issues D0 configuration write for recovery and makes a transition to recovery itself.

3. Cases in which recovery is initiated by this module itself (caused by hardware)

An error message is transmitted through hardware processing.

Depending on the timing, an error message is transmitted after L1 transition and a recovery may be made.

A completion of the TLP received before L1 transition is transmitted.

After a recovery to L0, if the device is in the non-D0 state and there is no TLP to be transmitted, software should confirm that hardware is in the L0 state (PMSR.PMSTATE = L0) and initiate the L1 transition sequence again (write 1 to PMCTLR.L1IATN). In this case, the sequence is: L0 → L1 → L0 recovery → L1 again.

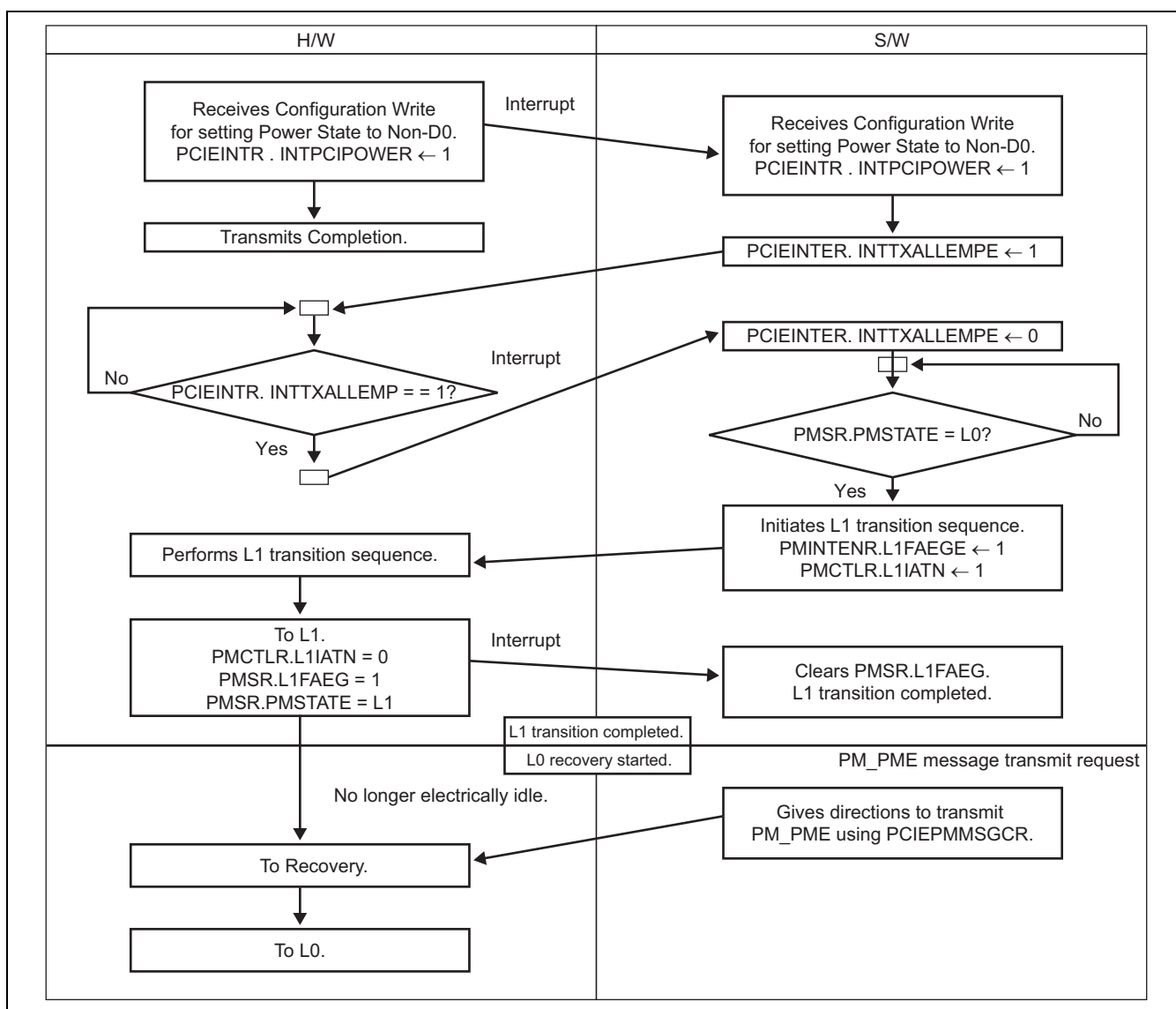


Figure 39.28 Transition from L0 to L1 to L0 (Endpoint)

**(b) L0 → L1 → L0 (Root Port)**

Initiate the L1 transition sequence through software according to the flowchart shown in Figure 39.29.

After initiated through software, the L1 transition sequence is performed through hardware according to the following procedure.

1. Prepares for L1 transition.
  2. Processes the handshake with the peer device for L1 transition.
  3. Causes the LTSSM of this module to make an L1 transition.
- Triggered by a write of PMCTLR.L1IATN = 1, hardware initiates the L1 transition sequence. As preparation for causing L1 transition, this module first allows hardware to automatically perform the following. (1) Waits for the retry buffer to be empty. (2) Waits for all the TLP to be transmitted.
  - After completion of the above preparation, this module transmits PM\_Request\_Ack DLLP and receives the electrical idle ordered set to process the handshake for L1 transition.
  - When having received the electrical idle ordered set on any lane, this module disables TLP/DLLP transmission. If directions are given to make a transition to the Detect or Recovery state before disabling TLP/DLLP transmission, this module gives priority to a transition to the Detect or Recovery state.
  - After completion of the handshake for L1 transition, this module directs the LTSSM to make a transition to L1 and transmits the electrical idle ordered set.
  - Hardware clears the PMCTLR.L1IATN bit to 0 when the LTSSM makes a transition to the state other than L0, Recovery, and Configuration, that is, when the LTSSM makes a transition to L1 (PMSR.PMSTATE = L1) properly or LDn (PMSR.PMSTATE = LDn). Simultaneously, the PMSR.L1FAEG bit is set. Software can confirm that TLP write is again enabled and the transition destination by reading PMSR.L1FAEG = 1 and PMSR.PMSTATE. After confirming PMSR.L1FAEG = 1, write 1 to PMSR.L1FAEG to clear the bit.
  - After initiation of the L1 transition sequence, if transitions are made as L0 → Recovery → L0 or L0 → Recovery → Configuration → L0 before a transition to the L1 state is caused, hardware automatically initiates the L1 transition sequence again. Therefore, software has nothing to process. PMSR.L1FAEG is not set.

The sequence for a recovery from L1 is performed under the following conditions.

1. Cases in which recovery is initiated by this module itself
  - Software performs configuration write to transmit TLP again.
  - The request for configuration write is scheduled for transmission by software. Be sure to confirm that a transition to L1 has been properly made (PMSR.L1FAEG = 1 and PMSR.PMSTATE = L1) before scheduling.
2. Cases in which recovery is initiated by the peer
  - The receive lane becomes no longer electrically idle.
  - Typical example: The Endpoint issues a PME message for requesting a recovery itself and the peer makes a transition to Recovery.

After a recovery to L0, if the device is in the Non-D0 state and PM\_Enter\_L1 DLLP is transmitted from the downstream device, software should confirm that hardware is in the L0 state (PMSR.PMSTATE = L0) and initiate the L1 transition sequence again (write 1 to PMCTLR.L1IATN). In this case, the sequence is: L0 → L1 → L0 recovery → L1 again.

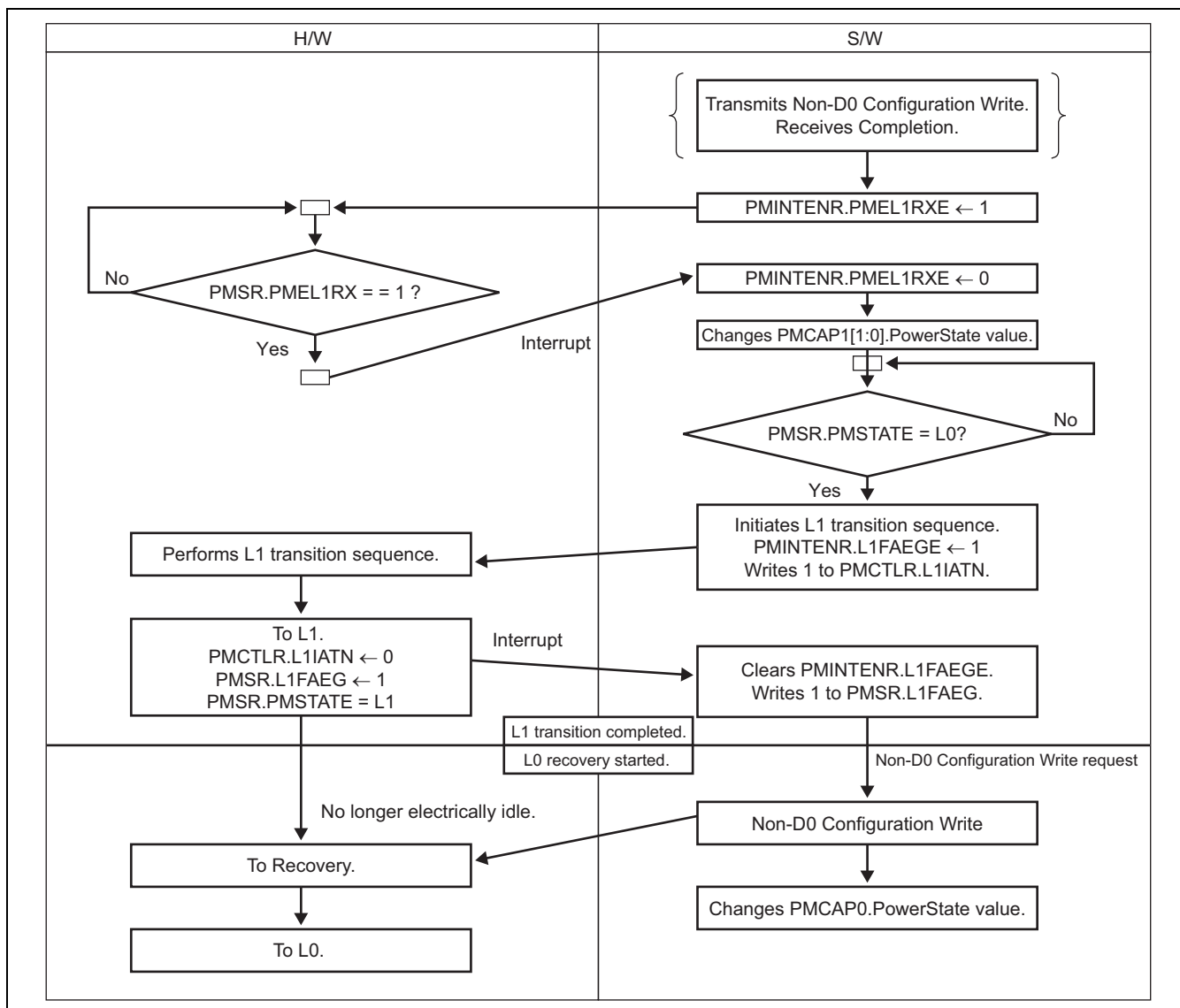


Figure 39.29 Transition from L0 to L1 to L0 (Root Port)

(2) Active State Power Management (ASPM)

This section describes PCI Express-specific power management mode. Table 39.12 shows power management operations in Active State Power Management (hereinafter referred to as ASPM) mode. ASPM is automatically controlled by hardware; software should take nothing particular into account.

Table 39.12 ASPM Operation

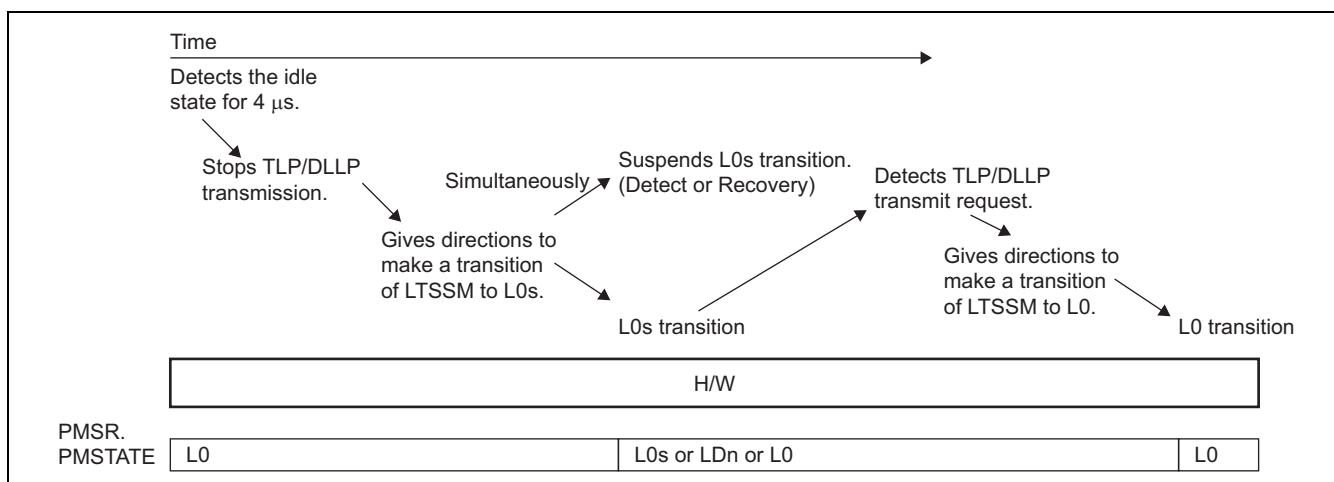
No.	Transition	Target Device
1	L0 → L0s → L0	Common to Endpoint and Root Port

**(a) L0 → L0s → L0**

When a link is in the idle state for 4 μs, hardware automatically initiates the L0s transition sequence. This module determines a link to be in the idle state in any of the following cases.

- Cases in which No TLP is transmitted
  1. No TLP to be transmitted is scheduled in the VC buffer.
  2. TLP is scheduled but there are not enough credits to transmit the TLP in the VC buffer.
  3. TLP is scheduled and there are enough credits but Non-posted cannot be issued according to the limitations on the number of Outstanding by this module.
- Cases in which no DLLP is scheduled for transmission

Figure 39.30 shows an overall overview of L0 → L0s → L0 transition.



**Figure 39.30 Overall Overview of L0 → L0s → L0 (Common to Endpoint/Root Port)**

The L0s transition sequence is as follows.

1. Detects the idle state for 4 μs.
2. Stops TLP/DLLP transmission.
3. Gives directions to make a transition to L0s.

Note that if the directions to make a transition to L0s and the directions to make a transition to Detect or Recovery are given simultaneously in this module, the directions to make a transition to Detect or Recovery are given priority. If the directions are given to make a transition to L0s and then the directions are given to make a transition to the other state (such as Detect and Recovery), a transition to L0s is first made and then a transition to the designated state is made.

The sequence for a recovery from L0s is: when there is TLP/DLLP to be transmitted, recovery from L0s to L0 is automatically made. After recovery, TLP/DLLP is transmitted.

### 39.3.11 Error Handling

This section describes handling of the errors detected by this module.

#### (1) Error Types

This module classifies detected errors into four types: three types defined in the PCI Express standard (correctable errors, non-fatal errors, and fatal errors) and other errors (system errors). It reports each type of error through the corresponding interrupt.

##### (a) Correctable Error

Correctable errors are defined as the type of errors from which recovery is possible through the PCI Express protocol. Recovery from the errors is performed by hardware.

When the conditions described later are satisfied, occurrence of a correctable error is signaled by the INT\_PCICERR interrupt.

##### (b) Non-Fatal Error

Non-fatal errors are defined as the type of errors from which recovery is impossible through the PCI Express protocol but which is not fatal. After this error, a single packet is discarded but the subsequent data communication can be continued. In most cases, error processing such as retransmission of the discarded packet is needed.

When the conditions described later are satisfied, occurrence of a non-fatal error is signaled by the INT\_PCINFERR interrupt.

##### (c) Fatal Error

Fatal errors are defined as the type of errors from which recovery is impossible through the PCI Express protocol and which is fatal. Specifically, the errors that require resetting the communication path or other appropriate processing fall into this type. In most cases, this module must be initialized.

When the conditions described later are satisfied, occurrence of a fatal error is signaled by the INT\_PCIFERR interrupt.

##### (d) Other Errors Detected by This Module (System Error)

The errors that do not fall into the above types are classified as system errors. The necessary processing depends on the cause of each error.

Occurrence of a system error is signaled by the INT\_PCISERR interrupt.

#### (2) Priority of Errors

Upon detecting multiple errors during reception of a single packet, this module reports only one error that it determines as the most important according to the following priority among errors.

Receiver Overflow

Malformed TLP

Unsupported request (UR), or unexpected completion

Poisoned TLP received

### (3) Correctable Error

Correctable errors are defined as the type of errors from which recovery is possible without loss of transfer data through hardware processing such as automatic retransmission request.

If a correctable error occurs, the EXPCAP2[16].CEDTCD bit is set to 1. If a correctable error occurs when the EXPCAP2[0].CERPE bit is 1 in Endpoint mode, the ERR\_COR message is transmitted to the Root Port to notify occurrence of an error. In Root Port mode, the INT\_PCICERR interrupt is generated if EXPCAP7[0].SERRCEE is 1.

In Root Port mode, if the ERR\_COR message is received from an Endpoint when all of the PCICONF15[17].SERRE, EXPCAP2[0].CERPE, and EXPCAP7[0].SERRCEE bits are 1, the INT\_PCICERR interrupt is generated.

The following errors are classified as correctable errors.

#### (a) Receiver error

8b/10b decode error

Disparity error

Elastic buffer overflow

Elastic buffer underflow

#### (b) BAD TLP

LCRC error

Sequence number error

#### (c) BAD DLLP

16-bit CRC error

#### (d) Replay timeout

Ack/Nak timeout

#### (e) Replay Num rollover

Replay Num rollover

#### (4) Non-Fatal Error

A non-fatal error cannot be corrected through hardware control and one packet of data will be lost. Therefore, recovery processing by software, such as retransmission processing, is needed.

If a non-fatal error occurs, the EXPCAP2[17].NFEDTCD bit is set to 1. If a non-fatal error occurs when PCICONF1[8].SERRE is 1, the PCICONF1[30].SSE bit is set to 1. If a non-fatal error occurs when the EXPCAP2[1].NFERPE bit or PCICONF1[8].SERRE bit is 1 in Endpoint mode, the ERR\_NONFATAL message is transmitted to the Root Port to notify occurrence of an error. In Root Port mode, the INT\_PCINFERR interrupt is generated if EXPCAP7[1].SERRNFEE is 1. However, if the error source is an unsupported request (described later), this module does not send the message or generate an interrupt when the conditions described later are satisfied.

In Root Port mode, if the ERR\_NONFATAL message is received, PCICONF7[30].RSE is set to 1. If the ERR\_NONFATAL message is received when the PCICONF15[17].SERRE and PCICONF1[8].SERRE bits are 1, the PCICONF1[30].SSE bit is set to 1. If the ERR\_NONFATAL message is received from an Endpoint when the PCICONF15[17].SERRE bit is 1, the EXPCAP2[1].NFERPE or PCICONF1[8].SERRE bit is 1, and the EXPCAP7[1].SERRNFEE bit is 1, the INT\_PCINFERR interrupt is generated. However, if the error source is an unsupported request (described later), this module does not generate an interrupt when the conditions described later are satisfied. In addition, if the non-fatal error comes under the advisory non-fatal error cases described later, separately defined processing is performed.

The following errors are classified as non-fatal errors.

##### (a) Poisoned TLP Reception

If a packet with the Poisoned attribute is written, it is handled as a non-fatal error.

This module does not transfer a write request of a packet from the PCI Express side to the internal bus side if the packet has the Poisoned attribute. If a request with the Poisoned attribute is received, the packet is discarded.

If the completion responding to the request issued by this module has the Poisoned attribute, the data in the completion is not transferred to the internal bus side.

If ConfigurationWrite Type0, I/O Write, Set\_Slot\_Power\_Limit, or MSI has the Poisoned attribute, it is handled also as an unsupported request.

##### (b) Unsupported Request (UR) Reception

The following requests are handled as unsupported requests.

- Access to the area other than the PCI address area specified with BAR
- Reception of memory/IO request in Root Port mode when PCICONF1[2].BME = 0
- Access to memory space when PCICONF1[1].MSE = 0
- Access to IO space when PCICONF1[0].IOSE = 0
- Reception of a message with an undefined message code
- Reception of MsgD with message code Msg
- Reception of a message to be received only by an Endpoint in Root Port mode
- Reception of a message to be received only by a Root/Switch in Endpoint mode
- Reception of a Type0 Vendor Defined Message
- Reception of TLP other than configuration access and message in the Non-D0 state
- Access to a configuration register not implemented
- Reception of a Type1 Configuration Request
- Reception of a Configuration Request in Root Port mode
- Reception of a packet without the No Snoop attribute when acceptance of a snoop transaction is rejected by VCCAP4[15].RJCTSNPTR

- Reception of a MRdLk request

If an unsupported request is received, the EXPCAP2[19].URDTCD bit is set to 1.

If an unsupported request is received when both the EXPCAP2[3].URRPE and PCICONF1[8].SERRE bits are 0, neither transmission of a message nor generation of an interrupt is performed.

If an unsupported request is received, the packet is discarded.

#### (c) Completer Abort (CA)

If an error occurs on the internal bus when the packet is transferred from the PCI Express to the internal bus, this module considers it as a Completer Abort and performs error handling. When the packet received from the PCI Express is a Non-Posted request, this module returns a completion with the Completer Abort (CA)– Completion Status thus setting the PCICONF1[27].STA bit to 1.

If the packet received by this module from the PCI Express side violates the PCI Express standard or is considered to be damaged, it is handled as an unsupported request or malformed TLP, not as a Completer Abort.

#### (d) Unexpected Completion Reception

If the completion not corresponding to the request issued by this module is received, it is considered as an unexpected completion and error handling is performed.

Reception of an unexpected completion falls into the advisory non-fatal error cases described later.

#### (5) Fatal Error

Fatal errors are defined as the type of errors from which recovery is impossible through hardware and which usually require system-level error recovery processing such as initialization of the PCI Express.

If a fatal error occurs, the EXPCAP2[18].FEDTCD bit is set to 1. If a fatal error occurs when the PCICONF1[8].SERRE bit is 1, the PCICONF1[30].SSE bit is set to 1. If a fatal error occurs when the EXPCAP2[2].FERPE or PCICONF1[8].SERRE bit is 1, in Endpoint mode the ERR\_FATAL message is transmitted to the Root Port to notify occurrence of an error. In Root Port mode, the INT\_PCINFERR interrupt is generated if EXPCAP7[2].SERRFEE is 1.

In Root Port mode, if the ERR\_FATAL message is received, PCICONF7[30].RSE is set to 1. If the ERR\_FATAL message is received when both of the PCICONF15[17].SERRE and PCICONF1[8].SERRE bits are 1, the PCICONF1[30].SSE bit is set to 1. If the ERR\_FATAL message is received from an Endpoint when the PCICONF15[17].SERRE bit is 1, the EXPCAP2[1].FERPE or PCICONF1[8].SERRE bit is 1, and the EXPCAP7[2].SERRFEE bit is 1, the INT\_PCIFERR interrupt is generated.

The following errors are classified as fatal errors.

- (a) Data Link Layer Protocol Error
- (b) Reception of malformed TLP

The following packets are considered as malformed TLPs, which cause a fatal error when received. These packets are discarded when received.

- Reception of a packet with data size exceeding the Max Payload Size
- Reception of a packet with data of different length from the length specified in the size field
- Reception of a TLP with TD field in header = 0 and with the digest field
- Reception of a TLP with TD field in header = 1 and without the digest field
- Reception of an Assert\_INTx/Deassert\_INTx message of non TC0
- Reception of a power management message of non TC0
- Reception of an error signal message of non TC0



- Reception of an unlock message of non TC0
- Reception of a Set\_Slot\_Power\_Limit message of non TC0
- Reception of a Set\_Slot\_Power\_Limit message without data
- Reception of a completion with data of different size from the size specified in the Length field
- Reception of a completion with data size exceeding the Max Payload Size
- Reception of a TLP of undefined type or fmt
- Reception of a TLP of the unassigned TC
- Reception of an IO request of TC!=0, Attr[1:0]!=0, Length[9:0]!=1, or Last DWBE[3:0]!=0
- Reception of a configuration request of TC!=0, Attr[1:0]!=0, Length[9:0]!=1, or Last DWBE[3:0]!=0
- Reception of an Assert\_INTx/Deassert\_INTx message in Endpoint mode
- Reception of a memory request with illegal DWBE
- Reception of a memory request crossing a 4-Kbyte boundary

## (6) System Error

System errors are defined as the errors that are not classified as any of the correctable, non-fatal, and fatal errors.

This module can signal the following events as the system errors by so setting PCIEERRFER.

- Internal bus error (reception of error response or disagreement of read data size)
- Posted/Non-Posted Buffer overflow
- CplLk reception
- Reception of an Unexpected Completion
- Disagreement of read data size requested and Completion data size
- Completion timeout
- Reception of a Completion with the CRS/CA/UR status
- Transmission of a Completion with the CA/UR status

If any system error occurs, the INT\_PCISERR interrupt is generated.

## (7) Advisory Non-Fatal Error Case

The PCI Express standard prescribes that some of non-fatal errors should not be processed when the applicable packet is received because the errors should be judged in terms of cause and significance by the packet transmission source, software, or system. These non-fatal errors are called advisory non-fatal error cases, which include the cases described in the following sections. If such a case is detected, general non-fatal error processing is not performed but processing prescribed individually is performed instead.

### (a) Return of Completion with Unsupported Request/Completer Abort Status

If a completion with unsupported request/Completer Abort status is returned, this module does not perform non-fatal error processing defined in the PCI Express standard. This module records occurrence of an error in PCIEERRFR[0].SENDURCPL or PCIEERRFR[1].SENDACPL, and generates an INT\_PCISERR interrupt if the corresponding bit in PCIEERRFER is set to 1.

### (b) Completion Timeout

If a completion timeout occurs, this module does not perform non-fatal error processing defined in the PCI Express standard. This module records occurrence of an error in PCIEERRFR[8].CPLTIMEOUT, and generates an INT\_PCISERR interrupt if the corresponding bit in PCIEERRFER is set to 1. When software determines that further retransmission is impossible, allow the software to perform error processing such as transmission of ERR\_COR.

**(c) Reception of Unexpected Completion**

If this module receives an unexpected completion, it does not perform non-fatal error processing defined in the PCI Express standard. This module records occurrence of an error in PCIEERRFR[12].UNEXPECTED COMPLETION, and generates an INT\_PCISERR interrupt if the corresponding bit in PCIEERRFER is set to 1.

**(d) Reception of Unsupported Request/Completer Abort Completion**

If this module receives a completion of unsupported request/Completer Abort, it does not perform non-fatal error processing defined in the PCI Express standard. This module records occurrence of an error in PCIEERRFR[4].RECEIVEURCPL or PCIEERRFR[5].RECEIVECACPL, and generates an INT\_PCISERR interrupt if the corresponding bit in PCIEERRFER is set to 1.

**(e) Reception of Poisoned TLP**

According to the PCI Express standard, the case in which a Poisoned TLP is received and reception is continued is also defined as an advisory non-fatal error case; however, an advisory non-fatal error of such a case does not occur with this module since this module prohibits continuation of Poisoned data processing. Although the cases related to the intermediate receiver are also defined by the standard, the corresponding processing is not performed since this module does not operate as an intermediate receiver.

### 39.3.12 Interrupts

Table 39.13 shows the interrupt signal lines of this module, definition, and the conditions under which interrupts are generated. The interrupt signals are synchronized with the internal bus clock.

**Table 39.13 List of Interrupt Signal Lines**

Name	Definition	Conditions of Generation	Related Registers
pci_int_serr	System error interrupt	<ul style="list-style-type: none"> <li>• Occurrence of a system error</li> <li>• Completion with the UR status is transmitted.</li> <li>• Completion with the CA status is transmitted.</li> <li>• Completion with the UR status is received.</li> <li>• Completion with the CA status is received.</li> <li>• Completion with the CRS status is received.</li> <li>• Completion timeout occurs.</li> <li>• Size error occurs.</li> <li>• Unexpected Completion is received.</li> <li>• CplLk is received.</li> <li>• Posted buffer overflows.</li> <li>• Non-Posted buffer overflows.</li> <li>• Transfer error occurs on the internal bus.</li> </ul>	<ul style="list-style-type: none"> <li>• PCIEINTR[0].INT_PCISERR</li> <li>• PCIEERRFR[0].SENDURCPL</li> <li>• PCIEERRFR[1].SENDACPL</li> <li>• PCIEERRFR[4].RCVURCPL</li> <li>• PCIEERRFR[5].RCVCACPL</li> <li>• PCIEERRFR[6].RCVCRSCPL</li> <li>• PCIEERRFR[8].CPLTOUT</li> <li>• PCIEERRFR[9].RCVSZECPL</li> <li>• PCIEERRFR[12].UNEXPCPL</li> <li>• PCIEERRFR[13].RCVCPCLK</li> <li>• PCIEERRFR[20].NPOVF</li> <li>• PCIEERRFR[21].POVF</li> <li>• PCIEERRFR[28].IBERR</li> </ul>
pci_int_ferr	PCI Express Fatal error interrupt	<ul style="list-style-type: none"> <li>• Occurrence of a fatal error</li> <li>• Malformed TLP</li> <li>• Data Link Layer Protocol Error</li> </ul>	<ul style="list-style-type: none"> <li>• PCIEINTR[1].INT_PCIFERR</li> <li>• EXPCAP2[18].FEDTCD</li> </ul>
pci_int_nferr	PCI Express Non Fatal Error interrupt	<ul style="list-style-type: none"> <li>• Occurrence of a non-fatal error</li> <li>• Unsupported request</li> <li>• Poisoned TLP</li> </ul>	<ul style="list-style-type: none"> <li>• PCIEINTR[2].INT_PCINFERR</li> <li>• EXPCAP2[17].NFEDTCD</li> </ul>
pci_int_cerr	PCI Express Correctable Error interrupt	<ul style="list-style-type: none"> <li>• Occurrence of a correctable error</li> <li>• Receiver Error</li> <li>• Bad DLLP</li> <li>• Bad TLP</li> <li>• Replay Number Rollover</li> <li>• Replay Timeout</li> </ul>	<ul style="list-style-type: none"> <li>• PCIEINTR[3].INT_PCICERR</li> <li>• EXPCAP2[16].CEDTCD</li> </ul>
pci_int_power	Power-down interrupt	<ul style="list-style-type: none"> <li>• PMCAP1[1:0] is set to the Non-D0 state by Configuration Write.</li> </ul>	<ul style="list-style-type: none"> <li>• PCIEINTR[4].INT_PCIPOWER</li> </ul>
pci_int_mes	PCI Express message reception or error interrupt	<ul style="list-style-type: none"> <li>• Reception of a message or occurrence of an error</li> <li>• PM_PME is received.</li> <li>• Set_Slot_Power_Limit is received.</li> </ul>	<ul style="list-style-type: none"> <li>• PCIEINTR[30].INT_PM_PME_RCV</li> <li>• EXPCAP8[16].PMEST</li> <li>• PCIEINTR[5].INT_PCIMES</li> <li>• PCIERMSGR[12].SLOTPOWER</li> </ul>

Name	Definition	Conditions of Generation	Related Registers
pci_int_bw	PCI Express link bandwidth change interrupt	Change of link bandwidth <ul style="list-style-type: none"> <li>Change of bandwidth is caused by intentional factor.</li> <li>Change of bandwidth is caused by reliability.</li> </ul>	PCIEINTR[28].INT_PCIBW <ul style="list-style-type: none"> <li>EXPCAP4[31].LKAUTOBWSTS</li> <li>EXPCAP4[30].LKBWMNGSTS</li> </ul>
pci_int_txallemp	PCI Express all transmission buffer empty interrupt	All the PCI Express transmit buffers are empty.	PCIEINTR[29].INT_TXALLEMP
pci_int_te	PCI Express transfer error interrupt	Occurrence of a PCI Express transfer error <ul style="list-style-type: none"> <li>PCIECDR is accessed with PCIECCLR[31].CCIE = 0.</li> <li>The pertinent PIO space is accessed with PCIEPTCLRn[31].PARE = 0.</li> <li>Transfer is executed with TC being set that is not mapped to VC0.</li> <li>PIO transfer is executed in Endpoint mode with PCICONF1[2].BME = 0.</li> <li>Transfer is executed with the attribute being set that is not enabled with the configuration register.</li> <li>Transfer other than PME message transfer is executed in the Non D0 state.</li> <li>PM_PME message transfer is executed in Endpoint mode with PMCAP1[8].PMEE = 0.</li> </ul>	PCIEINTR[31].INT_PCITE
pci_int_sc	PCI Express status change interrupt	Change of the following status <ul style="list-style-type: none"> <li>PHYRDY</li> <li>INTx Disable (PCICONF1[10].INTDIS)</li> <li>DL_Active· MSI Enable (MSICAP0[16].MSIE)</li> <li>PM Status (PMCAP1[1:0].Power State)</li> </ul>	PCIEPHYSR[16].PHYRDYC PCIETSTR[12].INTXDC PCIETSTR[16].DLLACTC PCIETSTR[28].MSIEC PCIEPMSR[24].PSTC
pci_int_pm	PCI Express-IP power management interrupt	Detection of PM status <ul style="list-style-type: none"> <li>PM_Enter_L1 DLLP is received.</li> <li>L1 initiation sequence is completed/suspended.</li> </ul>	PCIEINTR[12].INT_PM <ul style="list-style-type: none"> <li>PMSR[23].PMEL1RX</li> <li>PMSR[31].L1FAEG</li> </ul>
pci_int_mac	PCI Express IP MAC interrupt	Detection of MAC status <ul style="list-style-type: none"> <li>Transition of LTSSM to L0 is made.</li> <li>Link speed change is completed.</li> <li>Link speed change occurs.</li> <li>Link speed change fails.</li> <li>Link speed change succeeds.</li> <li>Link training is in progress.</li> </ul>	PCIEINTR[13].INT_MAC <ul style="list-style-type: none"> <li>MACSR[3].L0ENT</li> <li>MACSR[4].SPCHGFIN</li> <li>MACSR[5].SPCHG</li> <li>MACSR[6].SPCHGFAIL</li> <li>MACSR[7].SPCHGSUC</li> <li>MACSR[30].LKTR</li> </ul>

Name	Definition	Conditions of Generation	Related Registers
pci_int_dmace	PCI Express DMAC error interrupt	<p>Occurrence of a PCI Express error</p> <ul style="list-style-type: none"> <li>DMA transfer is initiated with DMAPCIEDMAOR.DMAE = 0.</li> <li>DMA transfer is initiated while a link is not established.</li> <li>DMA transfer is initiated in Non D0.</li> <li>DMA transfer is initiated with TC being set that is not mapped to VC0.</li> <li>DMA transfer is initiated in Endpoint mode with PCICONF1[2].BME = 0.</li> <li>DMA transfer is initiated with the attribute being set that is not enabled with the configuration register.</li> <li>A completion other than SC is received when PCI -&gt; internal bus.</li> <li>A completion timeout occurs when PCI -&gt; internal bus.</li> <li>A malformed completion is received when PCI -&gt; internal bus.</li> <li>A Poisoned Completion is received when PCI -&gt; internal bus.</li> </ul> <p>Occurrence of an internal bus error</p> <ul style="list-style-type: none"> <li>An error response is received.</li> <li>A response with data size different from the requested size is received.</li> </ul> <p>Forced termination</p> <ul style="list-style-type: none"> <li>Forced termination of DMA is completed.</li> </ul>	PCIEDMCHSR0-7[11].PEE PCIEDMCHSR0-7[9].IBE PCIEDMCHSR0-7[12].CHTC
pci_int_dmac0	PCI Express DMAC0 interrupt	Completion of data transfer	PCIEDMCHSR0[0].TE
pci_int_dmac1	PCI Express DMAC1 interrupt	Completion of data transfer	PCIEDMCHSR1[0].TE
pci_int_dmac2	PCI Express DMAC2 interrupt	Completion of data transfer	PCIEDMCHSR2[0].TE
pci_int_dmac3	PCI Express DMAC3 interrupt	Completion of data transfer	PCIEDMCHSR3[0].TE
pci_int_dmac4	PCI Express DMAC4 interrupt	Completion of data transfer	PCIEDMCHSR4[0].TE
pci_int_dmac5	PCI Express DMAC5 interrupt	Completion of data transfer	PCIEDMCHSR5[0].TE
pci_int_dmac6	PCI Express DMAC6 interrupt	Completion of data transfer	PCIEDMCHSR6[0].TE
pci_int_dmac7	PCI Express DMAC7 interrupt	Completion of data transfer	PCIEDMCHSR7[0].TE
pci_int_msi[31:0]	MSI interrupt	MSI reception	PCIEMSIFR[31:0]
pci_int_intx[3:0]	INTx interrupt	Assert_INTx message reception	PCIEINTXR[3:0]

Figures 39.31 and 39.32 show the interrupts whose corresponding interrupt status and enable bits are located in the multiple registers.

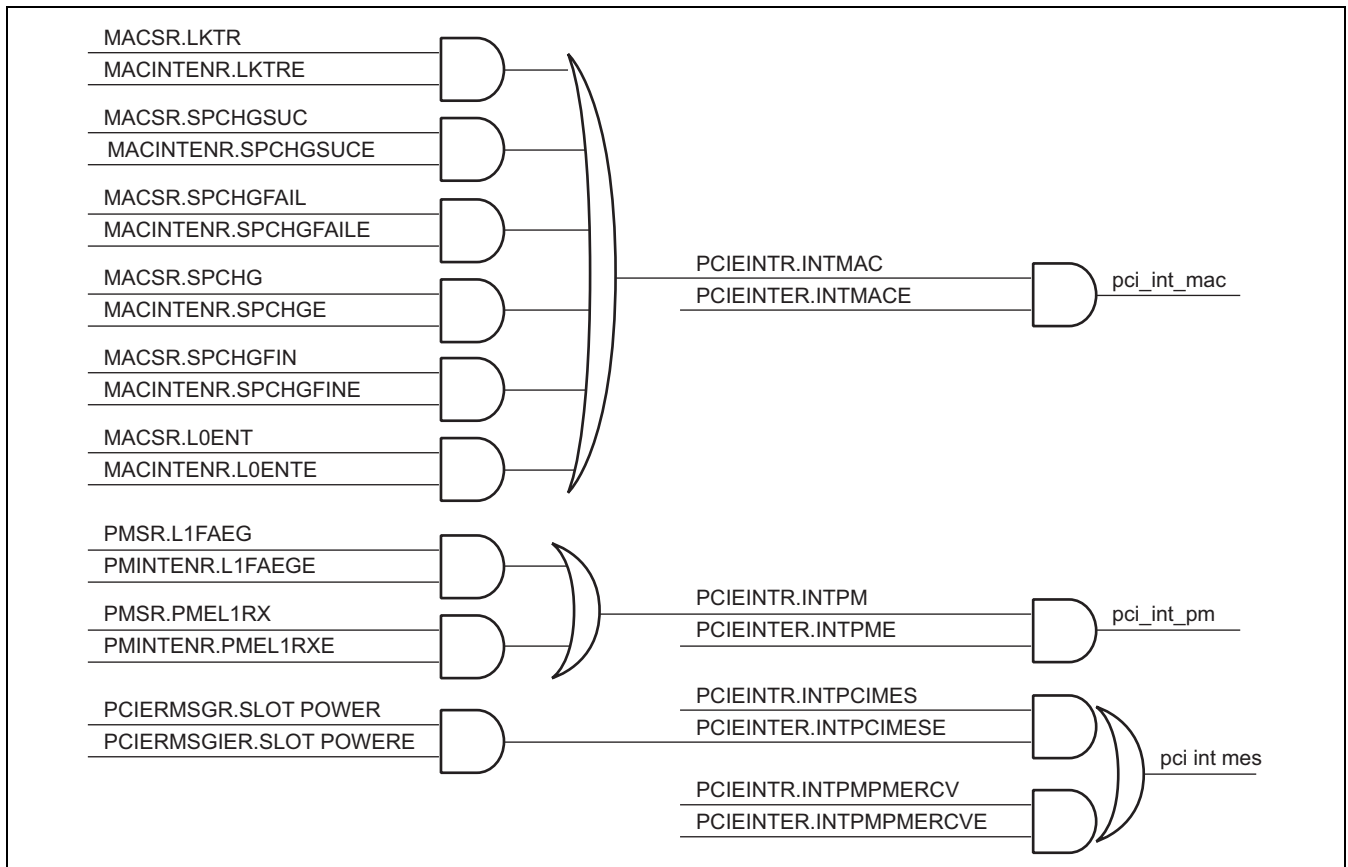


Figure 39.31 Interrupts Involving Multiple Registers (1)

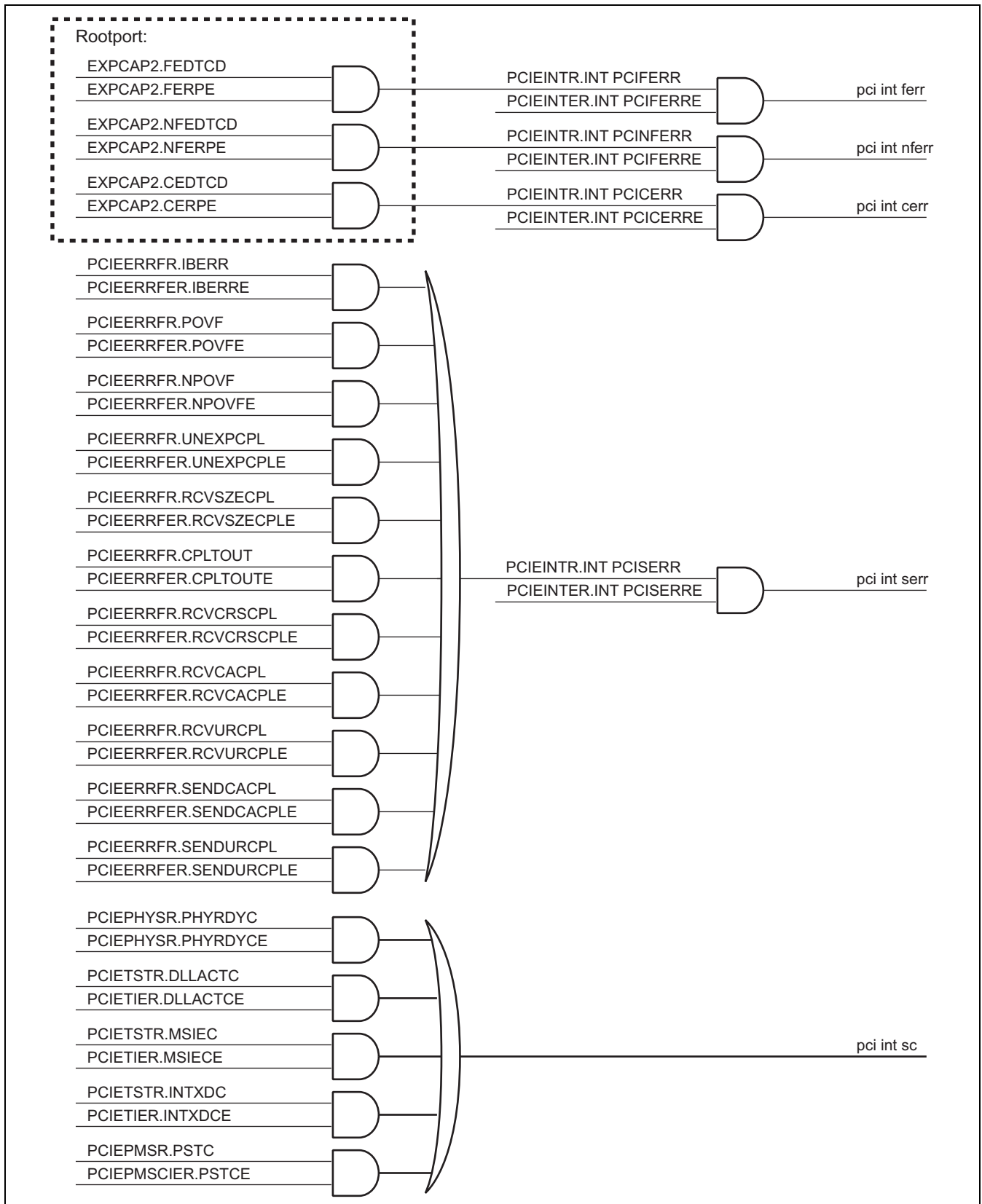


Figure 39.32 Interrupts Involving Multiple Registers (2)

## 39.4 Usage Notes

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

### 39.4.1 Write/Read Attributes of Configuration Registers

Although the registers in the configuration space have the register attributes defined by the PCI Express standard, these registers have different attributes when accessed by the internal bus. This section shows the attributes required for control. software refers to the software running on the device (i.e., CPU) on the internal bus.

**Table 39.14 Write/Read Attributes**

Attributes of PCI Express Registers	Description	Attributes of IP Registers	Example
HWInit	Hardware initialized bit. Initialized by hardware or software.	R for fields initialized by hardware.	EXPCAP0[24].SLTI_MP
		RW for fields initialized by software.	EXPCAP3[31:24].Port Number
RO	Read-only bit. Cannot be modified by software.	R for fields initialized by hardware.	PCICONF0[31:16].Device ID
		RW for fields initialized by software.	EXPCAP0[23:20].Device Port Type
RW	Read/Write bit. Can be modified by software.	RW	PCICONF1[2].BME
RW1C	Read-only status bit. Writing 1 clears the bit. Writing 0 has no effect.	RW1C	PCICONF1[24].MDPE
ROS	Sticky-read-only bit. Cannot be modified by software. Not initialized by hot reset.	Applies to no IP registers.	—
RWS	Sticky-read write bit. Can be modified by software. Not initialized by hot reset.	RW	EXPCAP2[10].AUXPPME
RW1CS	Sticky-read-only status bit. Writing 1 clears the bit. Writing 0 has no effect. Not initialized by hot reset.	RW1C	PMCAP1[15].PMEST
RsvdP	Reserved bit. Read-only. May be used as a RW bit in the future. Reading the bit returns 0.	R	EXPCAP4[15:12]
RsvdZ	Reserved bit. Read-only. May be used as a RW1C bit in the future. Reading the bit returns 0.	R	EXPCAP2[31:22]



The following shows which PCI Configuration Capability is supported by this IP.

		Offset	Capability	Spec Requirements	Root Port Type01	Endpoint Type00	
PCI Configuration Space	PCI3.0 Compatible Configuration Space	H'000	PCI Compatible Configuration Registers	Required	√	√	
		H'03F					
		H'040	PCI Power Management Capability Structure	Required	√	√	
			MSI or MSI-X Capability Structure	Required if an interrupt resource is required	—	√	
			PCI Express Capability Structure	Required	√	√	
		H'0FF					
	PCI Express Extended Configuration Space	H'0100		Virtual Channel Capability	Optional	√	√
				Device Serial Number Capability	Optional	x	x
				Advanced Error Reporting Capability	Optional	x	x
				PCI Express Root Complex Link Declaration Capability	Optional	x	x
				PCI Express Root Complex Internal Link Control Capability	Optional	x	x
				Power Budgeting Capability	Optional	x	x
				PCI Express Root Complex Event Collector Endpoint Association Capability	Optional	x	x
				Multi-Function Virtual Channel Capability	Optional	x	x
			Vendor-Specific Capability	Optional	x	x	
			RCRB Header Capability	Optional	x	x	
	H'0FFF						

### 39.4.2 Notes on Accessing Configuration Registers

- In Endpoint mode, writing to the configuration registers of this IP is prohibited except at initialization.
- "PCI RW" in the column header of the table in the description section of each register indicates the attribute of configuration access from the PCI Express bus in Endpoint mode; it is invalid in Root Port mode. For the registers with the same attribute shared in Endpoint mode and Root Port, "—" is indicated.

### 39.4.3 Registers Which Affect Hardware Internal Operation in Root Port Mode

Since the Endpoint configuration space may be accessed by the peer Root Port, it should be set appropriately. The registers implemented according to the Root Port configuration space are not accessed by Endpoint. Therefore, in Root Port mode, the user should appropriately set the registers that have influence on hardware operation shown in Table 39.15 at initialization. For details on register setting, refer to description of each register.

**Table 39.15 Root Port Configuration Registers Which Affect Hardware Internal Operation**

<b>Register Name</b>	<b>Bit Name</b>
PCICONF1	System Error Enable
	Parity Error Response
	Bus Master Enable
	Memory Space Enable
	IO Space Enable
PCICONF3	Header Type
PCICONF15	Secondary Bus Reset
	SERR Enable
	Parity Error Response
	Interrupt Line
PMCAP1	Power State
EXPCAP0	Device Port Type
EXPCAP1	Max Payload Size Supported
EXPCAP2	Max Read Request Size
	Enable No Snoop
	Extended Tag Enable
	Max Payload Size
	Enabled Relax Ordering
	Unsupported Request Reporting Enable
	Fatal Error Reporting Enable
	Non Fatal Error Reporting Enable
EXPCAP3	Link Bandwidth Notification Capability
	Data Link Layer Active Reporting Capability
	Maximum Link Width
	Supported Link Speeds
EXPCAP4	Link Autonomous Bandwidth Interrupt Enable
	Link Bandwidth Management Interrupt Enable
	Extended Sync
	Retrain Link
	Link Disable
	ASPM Control
EXPCAP7	CRS Software Visibility
	CRS Software Visibility Enable
	PME Interrupt Enable
	System Error on Fatal Error Enable
	System Error on Non Fatal Error Enable
EXPCAP10	System Error on Correctable Error Enable
	Completion Timeout Disable

<b>Register Name</b>	<b>Bit Name</b>
EXPCAP12	Compliance De-emphasis
	Compliance SOS
	Enter Modified Compliance
	Transmit Margin
	Selectable De-emphasis
	Enter Compliance
	Target Link Speed
VCCAP1	Extended VC Count
VCCAP4	VC(0) Reject Snoop Transaction
VCCAP5	TC/VC(0) MAP

Table 39.16 shows the registers which reflect the hardware status.

**Table 39.16 Root Port Configuration Registers Which Reflect Hardware Status**

Register Name	Bit Name
PCICONF1	Detected Parity Error
	Signaled System Error
	Received Master Abort
	Received Target Abort
	Signaled Target Abort
	Master Data Parity Error
PCICONF7	Detected Parity Error
	Received System Error
	Received Master Abort
	Received Target Abort
	Signaled Target Abort
	Master Data Parity Error
EXPCAP2	Transaction Pending
	Unsupported Request Detected
	Fatal Error Detected
	Non Fatal Error Detected
	Correctable Error Detected
EXPCAP4	Link Autonomous Bandwidth Status
	Link Bandwidth Management Status
	Data Link Layer Active
	Link Training
	Negotiated Link Width
	Current Link Speed
EXPCAP8	PME Pending
	PME Status
	PME Requester ID
EXPCAP12	Current De-emphasis
VCCAP6	VC(0) Negotiation Pending

#### 39.4.4 Power Management States

Do not stop inputting the reference clock signal in the power management states (L0s/L). Transition to the power management states (L0s/L1) is made from L0.

#### 39.4.5 State Transition

Transition to the L2 state is prohibited since L2 is not supported.

## 40. Serial Communication Interface with FIFO (SCIF)

RZ/G1H	RZ/G1N
RZ/G1M	RZ/G1E

### 40.1 Overview

This LSI has serial communication interfaces with FIFO buffers (SCIF) that handles asynchronous communication and clock synchronous serial communication. The SCIF has two 16-stage FIFO buffers separately for transmission and reception, which enables fast, efficient, and uninterrupted communication. The following table lists the functions of each interface.

The presence of the SCK, RTS, and CTS pins depends on the product or channel. The synchronous mode and mode control functions are supported in the interface channel which has the pins related to these functions.

Name	Function	Pin	Base Address	Remarks	RZ/G series products			
					RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
0 SCIF-0	Asynchronous mode (modem control is enabled) Clock synchronous mode	RX0, TX0, SCK0, RTS#0, and CTS#0	H'E6E6 0000	Transmission/reception clock can be supplied externally from SCK0 pin.	√	—	—	—
	Asynchronous mode	RX0*1, TX0*1	—	—	—	√	√	√
1 SCIF-1	Asynchronous mode (modem control is enabled) Clock synchronous mode	RX1, TX1, SCK1, RTS#1, and CTS#1	H'E6E6 8000	Transmission/reception clock can be supplied externally from SCK1*2 pin.	√	—	—	—
	Asynchronous mode Clock synchronous mode	RX1*2, TX1*2 and SCK1*2	—	—	—	√	√	√
2 SCIF-2	Asynchronous mode Clock synchronous mode	RX2*2, TX2*2 and SCK2*2	H'E6E5 6000 H'E6E5 8000	Transmission/reception clock can be supplied externally from SCK2*2 pin.	√ —	— √	— √	— √
	Asynchronous mode Clock synchronous mode	RX3*2, TX3*2 and SCK3*2	H'E6EA 8000	Transmission/reception clock can be supplied externally from SCK3*2 pin.	—	√	√	√
4 SCIF-4	Asynchronous mode	RX4*1, TX4*1	H'E6EE 0000	—	—	√	√	√
5 SCIF-5	Asynchronous mode	RX5*1, TX5*1	H'E6EE 8000	—	—	√	√	√

Notes: 1. RXm and TXm respectively refer to SCIFm\_RXD and SCIFm\_TXD in the RZ/G1E. (SCIF-0: m = 0, SCIF-4: m = 4, SCIF-5: m = 5)

2. RXn, TXn, and SCKn respectively refer to SCIFn\_RXD, SCIFn\_TXD, and SCIFn\_SCK in the RZ/G1E. SCKn refers to SCIFn\_SCK\_B in the RZ/G1M and RZ/G1N. (SCIF-1: n = 1, SCIF-2: n = 2, SCIF-3: n = 3)

### 40.1.1 Features

The SCIF has the following features.

- Asynchronous serial communication mode

The SCIF performs serial data communication based on a character-by-character asynchronous system. This feature enables serial data communication with standard asynchronous communication chips that support Universal Asynchronous Receiver/Transmitter (UART) or Asynchronous Communication Interface Adapter (ACIA). There is a choice of eight serial data transfer formats.

- Data length: 7 or 8 bits
- Stop bit length: 1 or 2 bits
- Parity: Even/odd/none
- Receive error detection: Parity, framing, and overrun errors
- Break detection:

A break is detected when a framing error lasts for more than 1 frame length at Space 0 (low level).

When a framing error occurs, a break can also be detected by reading the RX pin level directly from the serial port register (SCSPTR).

- Clock synchronous serial communication mode

The SCIF performs serial data communication synchronized with a clock. This feature enables serial data communication with other LSIs that support synchronous communication. There is a single serial data communication format for clock synchronous serial communication.

- Data length: 8 bits
- Receive error detection: Overrun errors

- Full-duplex communication capability

The SCIF has an independent transmitter and receiver that enable simultaneous transmission and reception. The transmitter and receiver both have a 16-stage FIFO buffer structure, enabling continuous serial data transmission and reception.

- On-chip baud rate generator, enabling any bit rate to be selected

The SCIF enables choice of a clock source for transmission/reception: a clock from the on-chip baud rate generator based on the internal clock or an external clock.

- Eight interrupt sources

The SCIF has eight types of interrupt sources – receive-data-ready, receive-FIFO-data-full, break, transmit-FIFO-data-empty, transmit-end, receive-error, overrun-error and time-out and enables any of them to be requested independently.

- DMA data transfer

When the transmit FIFO register is empty or the receive FIFO register has received data, issuing a DMA transfer request activates the DMA controller (DMAC) to execute a data transfer.

- The amount of data in the transmit/receive FIFO registers and the number of receive errors in receive data in the receive FIFO register are available.

- In asynchronous mode, a receive data ready (DR) or a timeout error (TO) can be detected during reception.

40.1.2 Block Diagram

Figure 40.1 shows the SCIF block diagram.

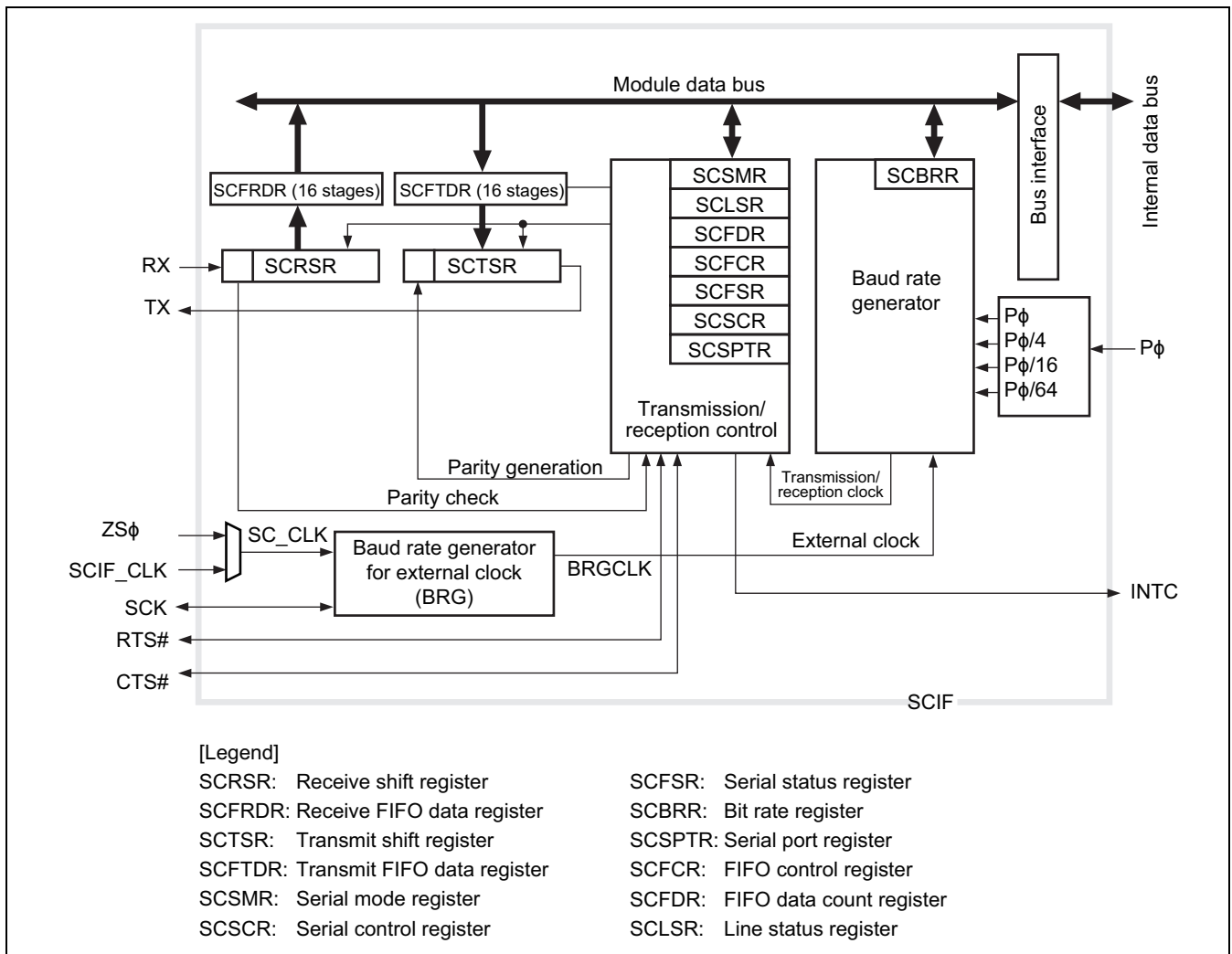


Figure 40.1 SCIF Block Diagram

### 40.1.3 Input/Output Pins

Table 40.1 shows the SCIF pin configuration. Pin functions can differ with the interface number. Other functions are also multiplexed on the same pins, so the multiplexed pin settings may restrict usage of the pins.

**Table 40.1 Pin Configuration**

Pin Name	Abbreviation	I/O	Function
Serial clock pin (SCKn*, SCIFn_SCK_B*, SCIFn_SCK*)	SCK	I/O	Synchronous clock I/O
Receive data pin (RXn*, SCIFn_RXD*)	RX	Input	Receive data input
Transmit data pin (TXn*, SCIFn_TXD*)	TX	Output	Transmit data output
Modem control pin (CTS#n*)	CTS#	I/O	Transmission enabled
Modem control pin (RTS#n*)	RTS#	I/O	Transmission request
Baud rate generation clock pin	SCIF_CLK	Input	Clock for input to the baud rate generator for the external clock

Note: These pins are made to function as serial pins by setting up SCIF operation using bit C/A# in SCSMR, bits TE, RE, CKE[1:0] in SCSCR, and bit MCE in SCFCR. SCSPTR of the SCIF can be used to handle the transmission and detection of break states.

\* n: Channel number



#### 40.1.4 Register Configuration

Table 40.2 shows the registers in the SCIF.

**Table 40.2 Register Configuration**

Register Name	Abbreviation	R/W	Offset from Base Address	Initial Value	Access Size
Serial mode register	SCSMR	R/W	H'00	H'0000	16
Bit rate register	SCBRR	R/W	H'04	H'FF	8
Serial control register	SCSCR	R/W	H'08	H'0000	16
Transmit FIFO data register	SCFTDR	W	H'0C	Undefined	8
Serial status register	SCFSR	R/W*1	H'10	H'0060	16
Receive FIFO data register	SCFRDR	R	H'14	Undefined	8
FIFO control register	SCFCR	R/W	H'18	H'0000	16
FIFO data count register	SCFDR	R	H'1C	H'0000	16
Serial port register	SCSPTR	R/W	H'20	H'00XX*3	16
Line status register	SCLSR	R/W*2	H'24	H'0000	16
Frequency division register	DL	R/W	H'30	H'0000	16
Clock Select register	CKS	R/W	H'34	H'0000	16

- Notes:
1. Only 0 can be written to bits 7 to 4, 1, and 0 to clear the flags. Bits 15 to 8, 3, and 2 are read-only bits and cannot be modified.
  2. Only 0 can be written to bits 2 and 1 to clear the flags. Bits 15 to 3, and 1 are read-only bits and cannot be modified.
  3. The initial values of SCSPTR bits 6, 4, 2, and 0 are undefined.

The table below lists the registers used in asynchronous mode, asynchronous mode with modem control, and clock synchronous mode. When setting up the registers, set the bits related to unsupported modes in each interface to their initial values. Otherwise, the SCIF may malfunction. Do not write to any registers other than listed below. Operations cannot be guaranteed if writing is attempted. Values read from registers other than listed below are undefined.

**Table 40.3 Register Settings in Each Mode**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCFRDR	—	—	—	—	—	—	—	—	*	*	*	*	*	*	*	*
SCFTDR	—	—	—	—	—	—	—	—	*	*	*	*	*	*	*	*
SCSMR	0	0	0	0	0	0	0	0	C	A	A	A	A	0	*	*
SCSCR	0	0	0	0	*	0	0	0	*	*	*	*	*	A	*	*
SCFSR	A	A	A	A	A	A	A	A	A	*	*	A	A	A	*	A
SCBRR	—	—	—	—	—	—	—	—	*	*	*	*	*	*	*	*
SCFCR	0	0	0	0	0	M	M	M	*	*	*	*	M	*	*	M
SCFDR	0	0	0	*	*	*	*	*	0	0	0	*	*	*	*	*
SCSPTR	0	0	0	0	0	0	0	0	M	M	M	M	C	C	*	*
SCLSR	0	0	0	0	0	0	0	0	0	0	0	0	0	A	0	*
DL	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
CKS	*	*	0	0	0	0	0	0	0	0	0	0	0	0	0	0

## [Legend]

\* : Used in any mode.

A : Used in asynchronous mode.

M : Used in asynchronous mode (modem control is enabled) (in addition to A).

C : Used in clock synchronous mode.

0 : Reserved (the write value should always be 0.)

— : Undefined

## 40.2 Register Descriptions

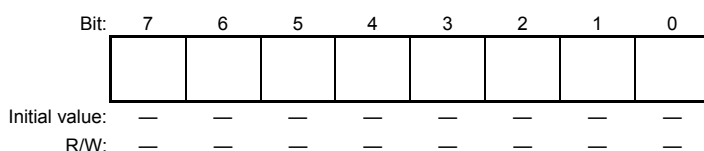
### 40.2.1 Receive Shift Register (SCRSR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SCRSR is a register that receives serial data.

The SCIF sets serial data input to the SCRSR from the RX pin in the order received, starting with the LSB (bit 0), and converts it to parallel data. When one byte of data has been received, it is transferred to the receive FIFO data register SCFRDR, automatically.

SCRSR cannot be read from and written to by the CPU.



### 40.2.2 Receive FIFO Data Register (SCFRDR)

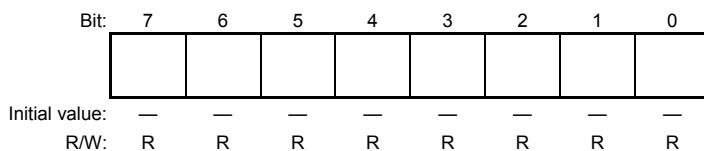
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SCFRDR is a 16-stage FIFO register that stores received serial data.

When the SCIF has received one byte of serial data, it transfers the received data from the receive shift register (SCRSR) to SCFRDR for storage, and reception is thus completed. SCRSR is then ready for reception, and is capable of receiving up to 16 consecutive bytes of data before SCFRDR is full.

SCFRDR is a read-only register and cannot be modified by the CPU. Note that the read value will be undefined while there is no receive data in SCFRDR. When SCFRDR is full of receive data, subsequent serial data is lost.

SCFRDR is read as an undefined value after a power-on reset.



### 40.2.3 Transmit Shift Register (SCTSR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SCTSR is a register that transmits serial data.

To perform serial data transmission, the SCIF first transfers transmit data from the transmit FIFO data register (SCFTDR) to SCTSR, then sends the data to the TX pin starting with the LSB (bit 0). When transmission of one byte is completed, the SCIF transfers the next transmit data from SCFTDR to SCTSR automatically, then starts transmission.

SCTSR cannot be read from and written to directly by the CPU.

Bit:	7	6	5	4	3	2	1	0
	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Initial value:	—	—	—	—	—	—	—	—
R/W:	—	—	—	—	—	—	—	—

### 40.2.4 Transmit FIFO Data Register (SCFTDR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SCFTDR is an 8-bit FIFO register of 16 stages that stores data for serial transmission.

If SCTSR is empty after transmit data has been written to SCFTDR, the SCIF transfers the data from SCFTDR to SCTSR and starts serial transmission.

SCFTDR is a write-only register and cannot be read from by the CPU. Writing further data to SCFTDR is no longer possible when it is full (contains 16 bytes of transmit data). Attempts at writing data to the register in this situation are ignored.

SCFTDR is read as an undefined value on a power-on reset.

Bit:	7	6	5	4	3	2	1	0
	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Initial value:	—	—	—	—	—	—	—	—
R/W:	W	W	W	W	W	W	W	W

### 40.2.5 Serial Mode Register (SCSMR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	—	—	—	—	—	—	—	—	C/A#	CHR	PE	O/E#	STOP	—	—	CKS[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W

SCSMR is a 16-bit register that sets the SCIF's serial transfer format and selects the baud rate generator clock source.

SCSMR can always be read from and written to by the CPU.

SCSMR is initialized to H'0000 by a power-on reset.

Bit	Bit Name	Initial Value	R/W	Description
15 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7	C/A#	0	R/W	Communication Mode Selects asynchronous mode or clock synchronous mode for the SCIF operation. 0: Asynchronous mode 1: Clock synchronous mode Note: Whether clock synchronous mode can be selected or not depends on the interface.
6	CHR	0	R/W	Character Length Selects 7 or 8 bits for asynchronous mode data length. In clock synchronous mode, the data length is fixed at 8 bits regardless of the CHR bit setting. 0: 8 bits 1: 7 bits* Note: * When the 7-bit data is selected, the MSB (bit 7) in the transmit FIFO data register (SCFTDR) is not transmitted.
5	PE	0	R/W	Parity Enable Determines whether parity bit is added in transmission or not, and parity bit is checked in reception in asynchronous mode or not. In clock synchronous mode, the parity bit is not added and checked regardless of the PE bit setting. When bit PE is set to 1, the parity (even or odd) specified by bit O/E# is added to transmit data. In reception, the parity bit is checked for the parity (even or odd) specified by bit O/E#. 0: Disables parity bit addition and check. 1: Enables parity bit addition and check.

Bit	Bit Name	Initial Value	R/W	Description
4	O/E#	0	R/W	<p>Parity Mode</p> <p>Selects either even or odd parity to use in parity addition and check.</p> <p>In asynchronous mode, the O/E# bit setting is valid only when bit PE is set to 1, enabling parity bit addition and check. In clock synchronous mode or when parity addition or check is disabled in asynchronous mode, the O/E# bit setting is invalid.</p> <p>0: Even parity*1 1: Odd parity*2</p> <p>Notes: 1. When even parity is set, the parity bit is added in transmission so that the total number of 1-bits in the transmit character plus the parity bit is even. In reception, a check is performed to see if the total number of 1-bits in the receive character plus the parity bit is even.</p> <p>2. When odd parity is set, the parity bit is added in transmission so that the total number of 1-bits in the transmit character plus the parity bit is odd. In reception, a check is performed to see if the total number of 1-bits in the receive character plus the parity bit is odd.</p>
3	STOP	0	R/W	<p>Stop Bit Length</p> <p>Selects 1 bit or 2 bits as the stop bit length in asynchronous mode.</p> <p>The stop bit setting is valid only in asynchronous mode. Since the stop bit is not added in clock synchronous mode, the STOP bit setting is invalid in this mode.</p> <p>In reception, only the first stop bit is checked, regardless of the STOP bit setting. If the second stop bit is 1, it is treated as a stop bit. If it is 0, it is treated as the start bit of the next transmit character.</p> <p>0: 1 stop bit*1 1: 2 stop bits*2</p> <p>Notes: 1. In transmission, a single 1-bit (stop bit) is added to the end of a transmit character before it is sent.</p> <p>2. In transmission, two 1-bits (stop bits) are added to the end of a transmit character before it is sent.</p>
2	—	0	R	<p>Reserved</p> <p>This bit is always read as 0. The write value should always be 0.</p>
1, 0	CKS[1:0]	00	R/W	<p>Clock Select 1 and 0</p> <p>These bits select the clock source for the on-chip baud rate generator.</p> <p>The clock source can be selected from P<math>\phi</math>, P<math>\phi</math>/4, P<math>\phi</math>/16, and P<math>\phi</math>/64, according to the setting of bits CKS1 and CKS0.</p> <p>00: P<math>\phi</math> 01: P<math>\phi</math>/4 10: P<math>\phi</math>/16 11: P<math>\phi</math>/64</p> <p>Note: P<math>\phi</math>: Peripheral clock (frequency dividing CPU clock into 12)</p>

### 40.2.6 Serial Control Register (SCSCR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SCSCR is a register that enables or disables transmission/reception by the SCIF, enables or disables interrupt requests, and selects transmission/reception clock source for the SCIF.

SCSCR can always be read from and written to by the CPU.

SCSCR is initialized to H'0000 by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	TEIE	—	—	—	TIE	RIE	TE	RE	REIE	TOIE	CKE[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11	TEIE	0	R/W	Transmit End Interrupt Enable When a transmit-end request is enabled by the TIE bit, the TEIE bit selects the source of the transmit end interrupt request from the following: <ul style="list-style-type: none"> <li>Setting the TDFE flag in SCFSR</li> <li>Setting the TEND flag in SCFSR</li> </ul> 0: The transmit FIFO data empty (TDFE) interrupt request is used. 1: The transmit end (TEND) interrupt request is used.
10 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
7	TIE	0	R/W	<p>Transmit Interrupt Enable</p> <p>Enables or disables a transmit-FIFO-data-empty interrupt (TDFE) request when the TEIE bit in SCSCR is pulled 0, if the following conditions are satisfied:</p> <ul style="list-style-type: none"> <li>Serial transmit data has been transferred from SCFTDR to SCTSR,</li> <li>The number of data bytes in SCFTDR is equal to or less than the transmit trigger count, and</li> <li>The TDFE flag in SCFSR is set to 1.</li> </ul> <p>Enables or disables a transmit-end interrupt (TEND) request when the TEIE bit of SCSCR is set to 1, if the following conditions are satisfied:</p> <ul style="list-style-type: none"> <li>Transmission was ended because there is no valid data in SCFTDR when the last bit of the transmit character in SCTSR was transmitted, and</li> <li>The TEND flag of SCFSR is set to 1.</li> </ul> <p>0: When the TEIE bit is 0, disables transmit-FIFO-data-empty interrupt (TDFE) request.* When the TEIE bit is 1, disables transmit-end interrupt (TEND) request.*</p> <p>1: When the TEIE bit is 0, enables transmit-FIFO-data-empty interrupt (TDFE) request. When the TEIE bit is 1, enables transmit-end interrupt (TEND) request.</p>
6	RIE	0	R/W	<p>Receive Interrupt Enable</p> <p>Enables or disables a receive-FIFO-data-full interrupt request when the RDF flag in SCFSR is set to 1, a receive-data-ready interrupt request when the DR flag in SCFSR is set to 1, a receive-error interrupt request when the ER flag in SCFSR is set to 1, a break interrupt request when the BRK flag in SCFSR is set to 1, and an overrun error interrupt request when the ORER flag in SCLSR is set to 1.</p> <p>0: Disables receive-FIFO-data-full interrupt (RDF) requests, receive-data-ready interrupt (DR) requests, receive-error interrupt (ER) requests, break interrupt (BRK) requests, and overrun error interrupt (ORER) requests.</p> <p>1: Enables receive-FIFO-data-full interrupt (RDF) requests, receive-data-ready interrupt (DR) requests, receive-error interrupt (ER) requests, break interrupt (BRK) requests, and overrun error interrupt (ORER) requests.</p>
5	TE	0	R/W	<p>Transmit Enable</p> <p>Enables or disables the start of SCIF serial transmission. The SCIF starts serial transmission when transmit data is written to the SCFTDR while TE is 1. Before setting TE to 1, set SCSMR and SCFCR to specify the transmission format and reset the transmit FIFO.</p> <p>0: Disables transmission.*</p> <p>1: Enables transmission.*</p>



Bit	Bit Name	Initial Value	R/W	Description
4	RE	0	R/W	<p>Receive Enable</p> <p>Enables or disables the start of SCIF serial reception. When RE is 1, the SCIF starts serial reception by detecting a start bit in asynchronous mode or by detecting a synchronization clock input in clock synchronous mode. Before setting RE to 1, set SCSMR and SCFCR to specify the reception format and reset the receive FIFO.</p> <p>0: Disables reception.* 1: Enables reception.</p> <p>Note: Even if RE is cleared to 0, the DR, ER, BRK, RDF, FER, PER, TO and ORER flags are not affected, and retain their states.</p>
3	REIE	0	R/W	<p>Receive Error Interrupt Enable</p> <p>Enables or Disables generation of receive-error interrupt (ER) requests, break interrupt (BRK) requests and overrun-error interrupt (ORER) requests.</p> <p>0: Disables receive-error interrupt (ER) requests, break interrupt (BRK) requests and overrun-error interrupt (ORER) requests.* 1: Enables receive-error interrupt (ER) requests, break interrupt (BRK) requests and overrun-error interrupt (ORER) requests.</p> <p>Note: * When REIE is 1, ER, BRK or ORER interrupt requests will occur even if RIE is cleared to 0. This setting is used to notify the interrupt controller of ER, BRK, and ORER interrupt requests during DMAC transfer.</p>
2	TOIE	0	R/W	<p>Timeout Interrupt Enable</p> <p>Enables or disables generation of timeout interrupt (TO) requests when the TO flag in SCLSR is set to 1.</p> <p>0: Disables timeout interrupts (TO). 1: Enables timeout interrupts (TO).</p>
1, 0	CKE[1:0]	00	R/W	<p>Clock Enable 1 and 0</p> <p>These bits select the SCIF clock source and enables or disables the clock output from the SCK pin.</p> <p>Whether the SCK pin functions as a serial clock output pin or a serial clock input pin is determined by combination of the CKE[1:0] bits settings. To specify synchronization clock output in clock synchronous mode, set C/A# to 1 in SCSMR then set CKE[1:0].</p> <p>See Table 40.4 for the bit settings.</p>

**Table 40.4 Clock Selection**

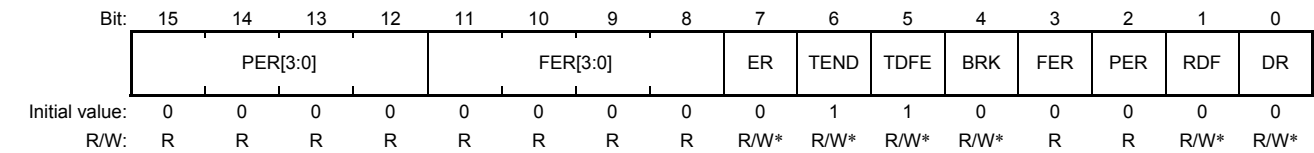
<b>CKE[1:0]</b>	<b>Mode</b>	<b>Clock Source</b>	<b>SCK Pin</b>
00	Asynchronous mode	Internal clock (P $\phi$ , P $\phi$ /4, P $\phi$ /16, P $\phi$ /64)	The SCK pin is not used. The SCK pin functions as an input pin (Input signals are ignored). (Initial value)
	Clock synchronous mode		The SCK pin outputs the synchronization clock. (Initial value)
01	Asynchronous mode		The SCK pin outputs the clock (with a frequency 16 times the bit rate).
	Clock synchronous mode		The SCK pin outputs the synchronization clock.
10	Asynchronous mode	Baud rate generator output for external clock or SCK	When SC_CLK is selected: The SCK pin is an input pin (Input signals are ignored). Set the SC_CLK frequency so that the frequency of BRGCLK is 16 times the bit rate.
			When SCK is selected: The SCK pin inputs the clock (with a frequency 16 times the bit rate).
	Clock synchronous mode	SCK*	The SCK pin inputs the synchronization clock.
11	Prohibited		

Notes: Some interfaces cannot select the clock synchronous mode.

- \* It is not allowed to set synchronous communication using SC\_CLK for input.

### 40.2.7 Serial Status Register (SCFSR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√



Note: Only 0 can be written to clear the flag.

SCFSR is a 16-bit register. The lower 8 bits are a status flag that indicates the operating status of the SCIF, and the upper 8 bits indicate the number of reception errors of data in the receive FIFO register.

SCFSR can always be read from and written to by the CPU. However, the flags ER, TEND, TDFE, BRK, RDF, and DR cannot be written by 1. The FER and PER flags are read-only flags and cannot be modified.

SCFSR is initialized to H'0060 by a power-on reset.

Bit	Bit Name	Initial Value	R/W	Description
15 to 12	PER[3:0]	All 0	R	<p>Parity Error Count</p> <p>These bits indicate the number of parity errors of receive data stored in the receive FIFO data register (SCFRDR).</p> <p>After the ER is set in SCFSR, the value represented by bits 15 to 12 indicates the number of parity errors. If a parity error occurs in all 16-byte receive data in SCFRDR, PER3 to PER0 are cleared to 0.</p>
11 to 8	FER[3:0]	All 0	R	<p>Framing Error Count</p> <p>These bits indicate the number of framing errors of receive data stored in the receive FIFO data register (SCFRDR).</p> <p>After the ER bit is set in SCFSR, the value represented by bits 11 to 8 indicates the number of framing errors. If a framing error occurs in all 16-byte receive data in SCFRDR, FER3 to FER0 are cleared to 0.</p>

Bit	Bit Name	Initial Value	R/W	Description
7	ER	0	R/W*	<p>Receive Error</p> <p>Indicates that a framing error or a parity error has occurred in reception.*<sup>1</sup> The ER flag is not affected by an error and retains its previous state when the RE bit is 0 in SCSCR.</p> <p>If a receive error occurs, receive data will be transferred to SCFRDR and reception operation will be continued. Whether there is a receive error in data read from SCFRDR can be determined by the FER and PER bits in SCFSR.</p> <p>0: Indicates that no framing or parity error has occurred in reception.</p> <p>[Clearing conditions]</p> <ul style="list-style-type: none"> <li>• A power-on reset is executed.</li> <li>• 0 is written to ER.</li> </ul> <p>1: Indicates that a framing error or a parity error has occurred in reception.</p> <p>[Setting conditions]</p> <ul style="list-style-type: none"> <li>• The SCIF checks whether the stop bit at the end of receive data is 1, but the stop bit is 0.*<sup>2</sup></li> <li>• The number of 1-bits in receive data plus the parity bit does not match the parity setting (even or odd) specified by the O/E# bit in SCSMR during reception.</li> </ul> <p>Note: In the 2-stop-bit mode, only the first stop bit is checked that the value is 1; the second stop bit is not checked.</p>
6	TEND	1	R/W*	<p>Indicates that transmission has been ended * because there was no valid data in SCFTDR when the last bit of the transmit character was transmitted.</p> <p>0: Indicates that transmission is in progress.</p> <p>[Clearing conditions]</p> <ul style="list-style-type: none"> <li>• Transmit data is written to SCFTDR, and 0 is written to TEND.</li> <li>• Data is written to SCFTDR by the DMAC.</li> </ul> <p>1: Indicates that transmission has been ended.</p> <p>[Setting conditions]</p> <ul style="list-style-type: none"> <li>• A power-on reset is executed.</li> <li>• The TE bit in SCSCR is 0.</li> <li>• There is no transmit data in SCFTDR when the last bit of a 1-byte serial transmission character is transmitted.</li> </ul> <p>Note: When transmit data is written to SCFTDR by the DMAC In clock synchronous mode, the TEND flag may not be cleared. Therefore, if the DMAC is used for transmission in clock synchronous mode, the TEND flag should be read using the following procedure.</p> <ol style="list-style-type: none"> <li>1. Check that data transfer is completed in the DMAC.</li> <li>2. Read the TEND flag.</li> <li>3. If TEND = 1, clear the TEND flag to 0.</li> <li>4. Read the TEND flag again.</li> <li>5. Use the second read TEND flag.</li> </ol>

Bit	Bit Name	Initial Value	R/W	Description
5	TDFE	1	R/W*	<p>Transmit FIFO Data Empty</p> <p>Indicates that the SCIF has transferred data from SCFTDR to SCTSR, the number of data bytes in SCFTDR becomes equal to or less than the transmit trigger count specified by the TTRG1 and TTRG0 bits in SCFCR, and SCFTDR is ready to be written by new transmit data.</p> <p>SCFTDR is a 16-byte FIFO register. The maximum number of bytes that can be written to when TDFE = 1 is "16 – [the transmit trigger count]". If data exceeding this value is attempted to be written, the data will be ignored. The number of data bytes in SCFTDR is indicated by the upper bits of SCFDR.</p> <p>If the number of data written in SCFTDR is equal to or less than the transmit trigger count, this bit will be set to 1 even if it is cleared to 0 after it is read as 1.</p> <p>0: Indicates that the number of transmit data written to SCFTDR exceeds the transmit trigger count.</p> <p>[Clearing conditions]</p> <ul style="list-style-type: none"> <li>• Transmit data exceeding the specified transmit trigger count have been written to SCFTDR, and 0 is written to TDFE.</li> <li>• Transmit data exceeding the specified transmit trigger count have been written to SCFTDR by the DMAC.</li> </ul> <p>1: Indicates that the number of transmit data in SCFTDR is equal to or less than the transmit trigger count.</p> <p>[Setting conditions]</p> <ul style="list-style-type: none"> <li>• A power-on reset is executed.</li> <li>• The number of transmit data in SCFTDR is equal to or less than the transmit trigger count after transmission.</li> </ul>
4	BRK	0	R/W*	<p>Break Detect</p> <p>Indicates that a receive data break signal has been detected. If a break signal is detected, receive data (H'00) transfer to SCFRDR is stopped. After the break is canceled and the receive signal returns to 1, the receive data transfer resumes.</p> <p>0: Indicates that no break signal has been received.</p> <p>[Clearing conditions]</p> <ul style="list-style-type: none"> <li>• A power-on reset is executed.</li> <li>• 0 is written to BRK.</li> </ul> <p>1: Indicates that a break signal has been received.</p> <p>[Setting condition]</p> <ul style="list-style-type: none"> <li>• Data with a framing error is received, followed by the space "0" (low level) for at least one frame length.</li> </ul>

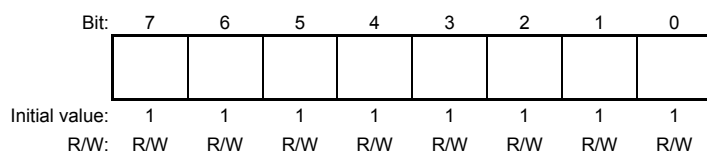
Bit	Bit Name	Initial Value	R/W	Description
3	FER	0	R	<p>Framing Error</p> <p>Indicates that a framing error has been found in the data that is to be read next from SCFRDR in asynchronous mode.</p> <p>0: Indicates that there is no framing error in the receive data that is to be read from SCFRDR.</p> <p>[Clearing conditions]</p> <ul style="list-style-type: none"> <li>• A power-on reset is executed.</li> <li>• There is no framing error in the data that is to be read next from SCFRDR.</li> </ul> <p>1: Indicates that there is a framing error in the receive data that is to be read from SCFRDR.</p> <p>[Setting condition]</p> <ul style="list-style-type: none"> <li>• There is a framing error in the data that is to be read next from SCFRDR.</li> </ul>
2	PER	0	R	<p>Parity Error</p> <p>This bit indicates that a parity error has been found in the data that is to be read next from SCFRDR in asynchronous mode.</p> <p>0: Indicates that there is no parity error in the receive data that is to be read from SCFRDR.</p> <p>[Clearing conditions]</p> <ul style="list-style-type: none"> <li>• A power-on reset is executed.</li> <li>• There is no parity error in the data that is to be read next from SCFRDR.</li> </ul> <p>1: Indicates that there is a parity error in the receive data that is to be read from SCFRDR.</p> <p>[Setting condition]</p> <ul style="list-style-type: none"> <li>• There is a parity error in the data that is to be read next from SCFRDR.</li> </ul>

Bit	Bit Name	Initial Value	R/W	Description
1	RDF	0	R/W*	<p>Receive FIFO Data Full</p> <p>Indicates that the received data has been transferred from SCRSR to SCFRDR, and the number of receive data bytes in SCFRDR becomes equal to or more than the receive trigger count specified by the RTRG1 and RTRG0 bits in SCFCR.</p> <p>SCFRDR is a 16-byte FIFO register. When RDF = 1, data equal to or more than the number of receive trigger data bytes can be read. When SCFRDR is empty, SCFRDR is read as an undefined value. The number of receive data bytes in SCFRDR is indicated by the lower bits of SCFDR.</p> <p>If the number of data in SCFRDR is equal to or more than the trigger count, this bit will be set to 1 even if it is cleared to 0. At this time, read receive data until the number of data in SCFRDR is less than the trigger count, read RDF as 1, and then clear RDF.</p> <p>0: Indicates that the number of receive data bytes in SCFRDR is less than the specified receive trigger count.</p> <p>[Clearing conditions]</p> <ul style="list-style-type: none"> <li>• A power-on reset is executed.</li> <li>• SCFRDR is read until the number of receive data bytes in SCFRDR is less than the receive trigger count, and 0 is written to RDF.</li> <li>• SCFRDR is read by the DMAC until the number of receive data bytes in SCFRDR is less than the receive trigger count.</li> </ul> <p>1: Indicates that the number of receive data bytes in SCFRDR is equal to or more than the specified receive trigger count.</p> <p>[Setting condition]</p> <ul style="list-style-type: none"> <li>• Receive data more than the receive trigger count have been stored in SDFRDR.</li> </ul>
0	DR	0	R/W*	<p>Receive Data Ready</p> <p>Indicates that the number of data bytes in SCFRDR is less than the receive trigger count and that no further data has been received for at least 15 etu after the stop bit of the data received last in asynchronous mode. This bit is not set in clock synchronous mode.</p> <p>0: Indicates that data is being received or has been successfully received, and there is no receive data in SCFRDR.</p> <p>[Clearing conditions]</p> <ul style="list-style-type: none"> <li>• A power-on reset is executed.</li> <li>• All the receive data in SCFRDR has been read, and 0 is written to DR.</li> <li>• All the receive data in SCFRDR has been read by the DMAC.</li> </ul> <p>1: Indicates that no further receive data has been received.</p> <p>[Setting condition]</p> <ul style="list-style-type: none"> <li>• The receive FIFO data register (SCFRDR) has the number of data byte that is below the receive trigger number of data bytes and no further data has arrived for at least 15 etu after the stop bit of the data received last.</li> </ul> <p>Note: etu: Elementary Time Unit (time for transfer of 1 bit) Equivalent to 1.5 frames with an 8-bit, 1-stop-bit format.</p>

Note: Writing 0 is only available to clear the flag.

### 40.2.8 Bit Rate Register (SCBRR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√



SCBRR is an 8-bit register that sets the serial transmission/reception bit rate in accordance with the baud rate generator operating clock selected by the CKS1 and CKS0 bits in SCSMR. This baud rate generator is intended for  $P\phi$ ,  $P\phi/4$ ,  $P\phi/16$ , and  $P\phi/64$ . For details on the baud rate generator for external clock, see section 40.6, Baud Rate Generator for External Clock (BRG).

SCBRR can always be read from and written to by the CPU except for during transfer.

SCBRR is initialized to H'FF by a power-on reset.

The SCBRR setting is determined by the following equation:

[Asynchronous mode]

$$N = \frac{P\phi}{64 \times 2^{2n-1} \times B} \times 10^6 - 1$$

[Clock synchronous mode]

$$N = \frac{P\phi}{8 \times 2^{2n-1} \times B} \times 10^6 - 1$$

B: Bit rate (bit/s)

N: SCBRR setting for the baud rate generator ( $0 \leq N \leq 255$ ) (which satisfies the electrical characteristics)

$P\phi$ : Peripheral module operating frequency (MHz)

n: Baud rate generator input clock ( $n = 0, 1, 2, 3$ )  
(See the Table 40.5 for the relation between n and the clock.)

**Table 40.5 SCSMR Settings**

n	Clock	SCSMR.CKS[1:0] Setting
0	$P\phi$	00
1	$P\phi/4$	01
2	$P\phi/16$	10
3	$P\phi/64$	11

The bit rate error in asynchronous mode is determined by the following equation:

$$\text{error (\%)} = \left\{ \frac{P\phi \times 10^6}{(N+1) \times B \times 64 \times 2^{2n-1}} - 1 \right\} \times 100$$



### 40.2.9 FIFO Control Register (SCFCR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SCFCR is a register that resets data counts and sets the number of trigger data bytes for the transmit and receive FIFO registers. It also has a loopback test enable bit.

SCFCR can always be read from and written to by the CPU except for during transfer.

SCFCR is initialized to H'0000 by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	RSTRG[2:0]		RTRG[1:0]		TTRG[1:0]		MCE	TFRST	RF RST	LOO P	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 11	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
10 to 8	RSTRG[2:0]	000	R/W	RTS Output Active Trigger The RTS# signal is high when the number of receive data bytes stored in SCFRDR is equal to or more than the specified trigger number shown below: 000: 15 001: 1 010: 4 011: 6 100: 8 101: 10 110: 12 111: 14
7, 6	RTRG[1:0]	00	R/W	Receive FIFO Data Count Trigger These bits specify the number of receive data bytes that makes the RDF (receive data full) flag to be set in SCFSR. The RDF flag is set when the number of receive data bytes in SCFRDR is equal to or more than the specified trigger number shown below:
	<b>RTRG[1:0]</b>	<b>Asynchronous Mode</b>	<b>Clock Synchronous Mode</b>	
	00	1	1	
	01	4	2	
	10	8	8	
	11	14	14	

Bit	Bit Name	Initial Value	R/W	Description
5, 4	TTRG[1:0]	00	R/W	<p>Transmit FIFO Data Count Trigger</p> <p>These bits specify the number of remaining transmit data bytes that makes the transmit FIFO data register empty (TDFE) flag to be set in SCFSR.</p> <p>The TDFE flag is set when the number of transmit data bytes in SCFTDR is equal to or less than the specified trigger count shown below, after transmission:</p> <p>00: 8 (8)            01: 4 (12)            10: 2 (14)            11: 0 (16)</p> <p>Note: Values in parentheses indicate the empty space in SCFTDR in bytes.</p>
3	MCE	0	R/W	<p>Modem Control Enable</p> <p>Enables or disables modem control signals CTS# and RTS#.</p> <p>This bit should always be set to 0 in clock synchronous mode. Whether modem control can be selected or not depends on the interface.</p> <p>0: Disables modem signals.*            1: Enables modem signals.</p> <p>Note: CTS# and RTS# control ports.</p>
2	TFRST	0	R/W	<p>Transmit FIFO Data Register Reset</p> <p>Enables or disables a transmit FIFO data register reset that empties the register.</p> <p>0: Disables the reset.*            1: Enables the reset.</p> <p>Note: The register is reset by a power-on reset.</p>
1	RFRST	0	R/W	<p>Receive FIFO Data Register Reset</p> <p>Enables or disables a receive FIFO data register reset that empties the register.</p> <p>0: Disables the reset.*            1: Enables the reset.</p> <p>Note: The register is reset by a power-on reset.</p>
0	LOOP	0	R/W	<p>Loopback Test</p> <p>Enables or disables the loopback test by internally connecting the transmit output pin (TX) and receive input pin (RX), and the RTS# pin and CTS# pin. If the loopback test is specified, the signal on the RTS# pin is internally conveyed to CTS# pin, and data transmission is automatically suspended when RTS# is asserted.</p> <p>0: Disables the loopback test.            1: Enables the loopback test.</p> <p>Even if loopback test is specified by this bit, SCSPTR.RTSDT and SCSPTR.CTSDT bits does not reflect signal on loopback path, because those registers shows signals on RTS#/CTS# pins.</p>

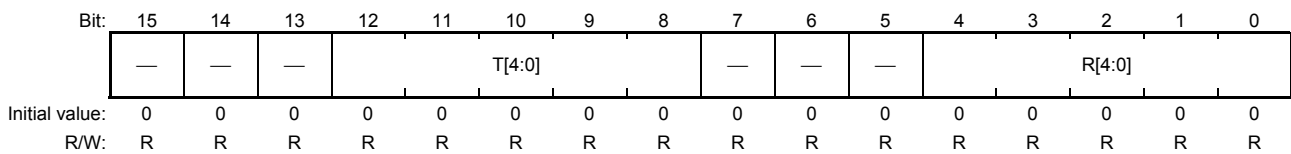
**40.2.10 FIFO Data Count Register (SCFDR)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SCFDR is a 16-bit register that indicates the number of data bytes stored in SCFTDR and that in SCFRDR.

The upper 8 bits indicate the number of transmit data bytes in SCFTDR, and the lower 8 bits indicates the number of receive data bytes in SCFRDR.

SCFDR can always be read by the CPU.



Bit	Bit Name	Initial Value	R/W	Description
15 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12 to 8	T[4:0]	H'00	R	These bits show the number of data bytes untransmitted and still stored in SCFTDR. H'00 indicates that there is no transmit data in SCFTDR. H'10 indicates that SCFTDR is full of transmit data.
7 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4 to 0	R[4:0]	H'00	R	These bits show the number of receive data stored in SCFRDR in bytes. H'00 indicates that there is no receive data in SCFRDR. H'10 indicates that SCFRDR is full of receive data.

### 40.2.11 Serial Port Register (SCSPTR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SCSPTR controls multiplexed input/output and data on the serial communication interface (SCIF) ports. Bits 1 and 0 control breaks in serial transmission/reception by reading input data from the RX pin and writing output data to the TX pin. Bits 3 and 2 read input data from and write output data to the SCK pin. Bits 5 and 4 read input data from and write output data to the CTS# pin. Bits 7 and 6 read input data from and write output data to the RTS# pin.

SCSPTR is a 16-bit register that can always be read from and written to by the CPU.

All SCSPTR bits except bits 6, 4, 2, and 0 are initialized to 0 by a power-on reset. The values of bits 6, 4, 2, and 0 are undefined.

Note: Whether modem control can be selected or not depends on the interface.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	RTSIO	RTSDT	CTSIO	CTSDT	SCKIO	SCKDT	SPB2I O	SPB2D T
Initial value:	0	0	0	0	0	0	0	0	0	—	0	—	0	—	0	—
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7	RTSIO	0	R/W	Serial Port RTS# Pin Input/Output Specifies input or output for the serial port RTS# pin. To actually set the RTS# pin as a port output pin to output the value set by the RTSDT bit, the MCE bit in SCFCR should be cleared to 0. 0: Indicates that this bit does not output the value of the RTSDT bit to the RTS# pin. 1: Indicates that this bit outputs the value of the RTSDT bit to the RTS# pin.
6	RTSDT	—	R/W	Serial Port RTS# Pin Data Specifies the input/output data level of the serial port RTS# pin. Whether the pin is set for input or output is determined by the RTSIO bit. When the pin is set for output, the value of the RTSDT bit is output to the RTS# pin. Regardless of the value of the RTSIO bit, the value of the RTS# pin is read from the RTSDT bit. The initial value of this bit is undefined after a power-on reset. 0: Indicates that the input/output data is low level. 1: Indicates that the input/output data is high level.
5	CTSIO	0	R/W	Serial Port CTS# Pin Input/Output Specifies input or output for the serial port CTS# pin. To actually set the CTS# pin as a port output pin to output the value set by the CTSDT bit, the MCE bit in SCFCR should be cleared to 0. 0: Indicates that the CTSDT bit value is not output to the CTS# pin. 1: Indicates that the CTSDT bit value is output to the CTS# pin.

Bit	Bit Name	Initial Value	R/W	Description
4	CTS DT	—	R/W	<p>Serial Port CTS# Pin Data</p> <p>Specifies the input/output data level of the serial port CTS# pin. Whether the pin is set for input or output is determined by the CTSIO bit. When the pin is set for output, the value of the CTS DT bit is output to the CTS# pin. Regardless of the value of the CTSIO bit, the value of the CTS# pin is read from the CTS DT bit.</p> <p>The initial value of this bit is undefined after a power-on.</p> <p>0: Indicates that the input/output data is low level.</p> <p>1: Indicates that the input/output data is high level.</p>
3	SCKIO	0	R/W	<p>Serial Port Clock Pin Input/Output</p> <p>Specifies input or output for the serial port SCK pin. To actually set the SCK pin as a port output pin to output the value set by the SCK DT bit, the CKE[1:0] bits in SCSCR should be cleared to 0.</p> <p>0: Indicates that the SCK DT bit value is not output to the SCK pin.</p> <p>1: Indicates that the SCK DT bit value is output to the SCK pin.</p>
2	SCK DT	—	R/W	<p>Serial Port Clock Pin Data</p> <p>Specifies the input/output data level of the serial port SCK pin. Whether the pin is set for input or output is determined by the SCKIO bit. When the pin is set for output, the value of the SCK DT bit is output to the SCK pin. Regardless of the value of the SCKIO bit, the value of the SCK pin is read from the SCK DT bit.</p> <p>The initial value of this bit is undefined after a power-on reset.</p> <p>0: Indicates that the input/output data is low level.</p> <p>1: Indicates that the input/output data is high level.</p>
1	SPB2IO	0	R/W	<p>Serial Port Break Input/Output</p> <p>Specifies the output condition of the serial port TX pin. To actually set the TX pin as a port output pin to output the value set by the SPB2 DT bit, the TE bit in SCSCR should be cleared to 0.</p> <p>0: Indicates that the SPB2 DT bit value is not output to the TX pin.</p> <p>1: Indicates that the SPB2 DT bit value is output to the TX pin.</p>
0	SPB2 DT	—	R/W	<p>Serial Port Break Data</p> <p>Specifies the input level of the serial port RX pin and the output level of the TX pin. The TX pin output conditions are determined by the SPB2IO bit. When the TX pin is set for output, the value of the SPB2 DT bit is output to the TX pin. Regardless of the value of the SPB2IO bit, the value of the RX pin is read from the SPB2 DT bit.</p> <p>The initial value of this bit is undefined after a power-on reset.</p> <p>0: Indicates that the input/output data is low level.</p> <p>1: Indicates that the input/output data is high level.</p>

Figures 40.2 to 40.6 show the block diagrams of the SCIF I/O ports.

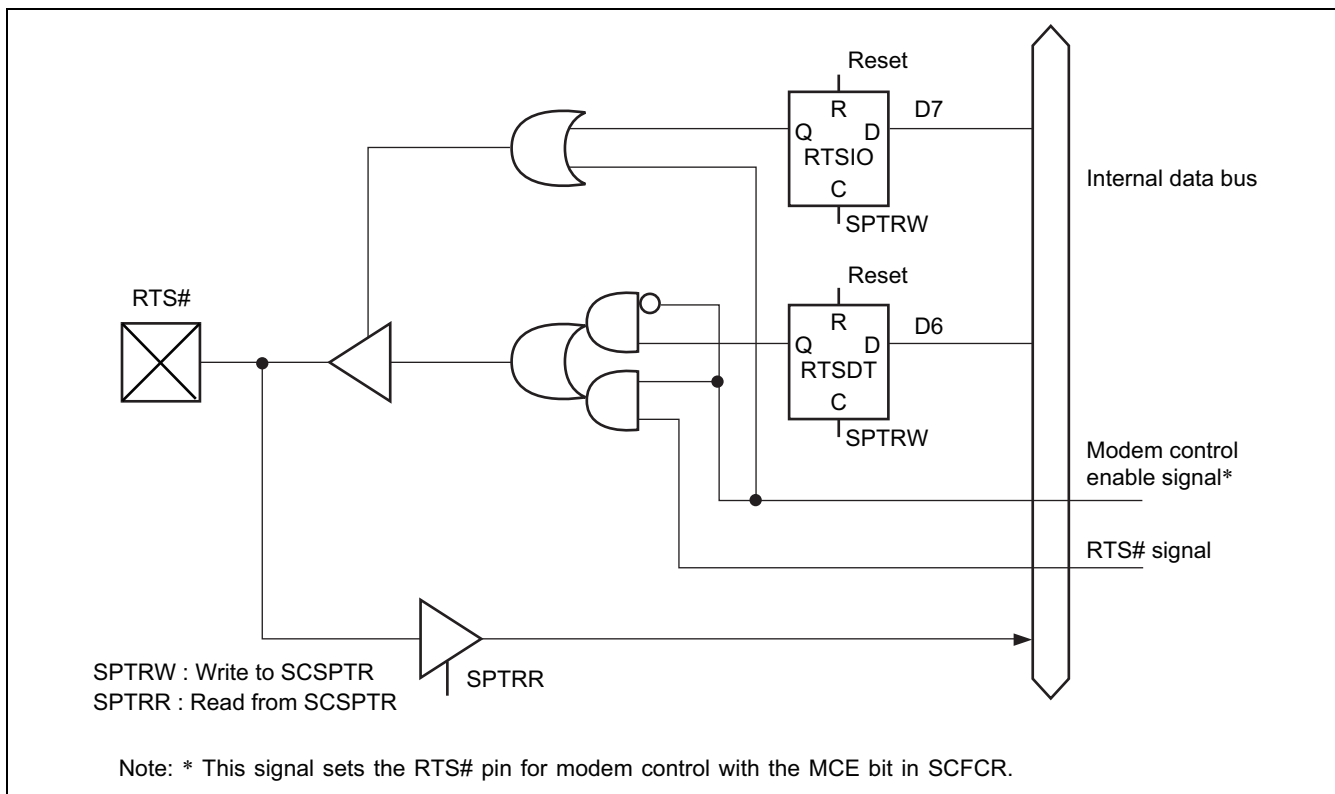


Figure 40.2 RTS# Pin

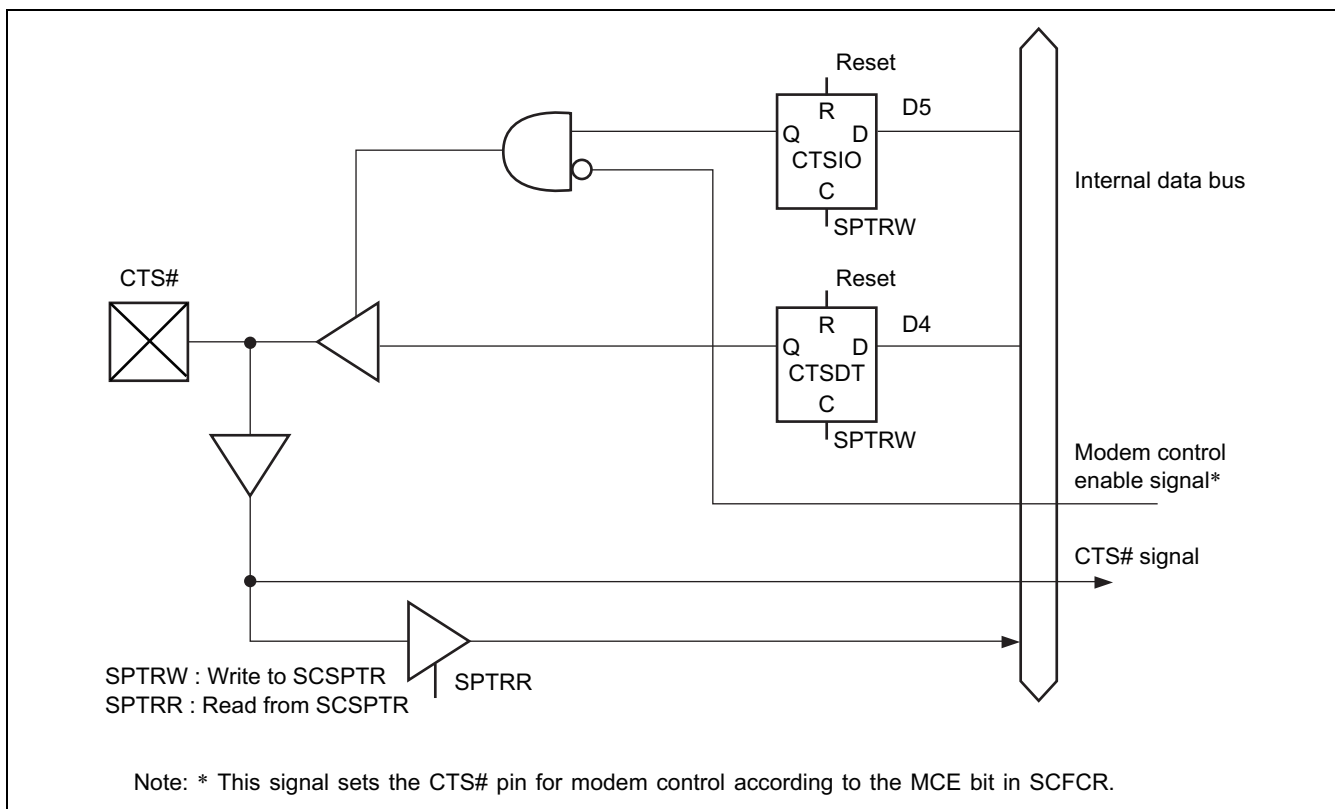


Figure 40.3 CTS# Pin

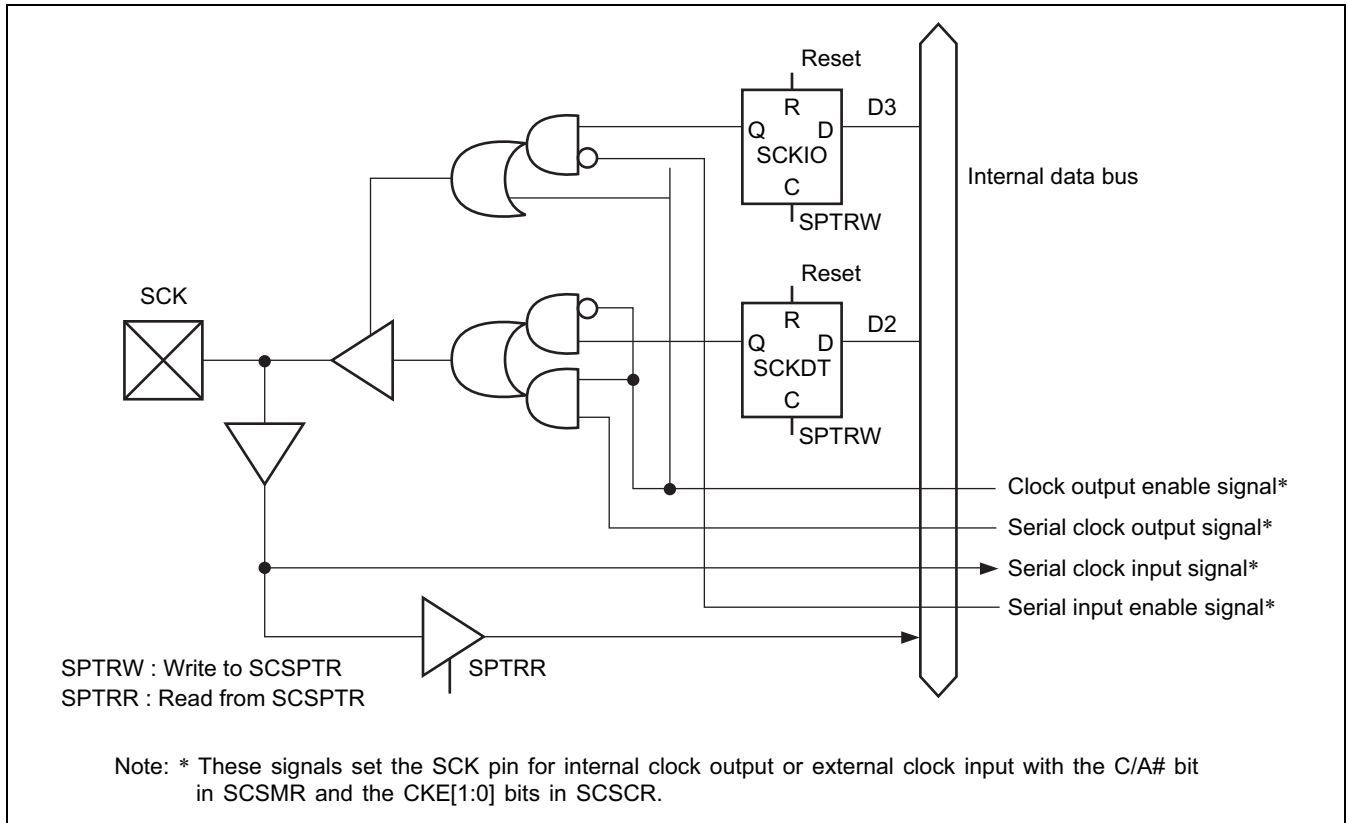


Figure 40.4 SCK Pin

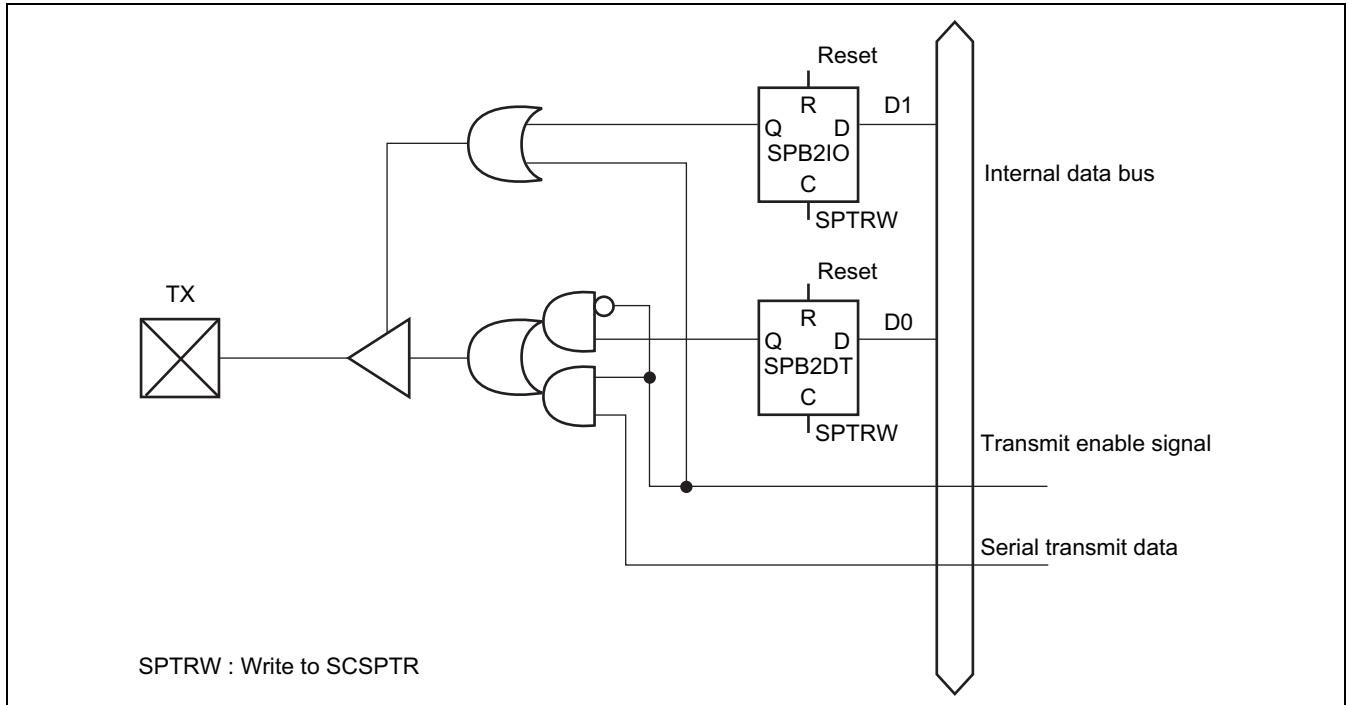


Figure 40.5 TX Pin

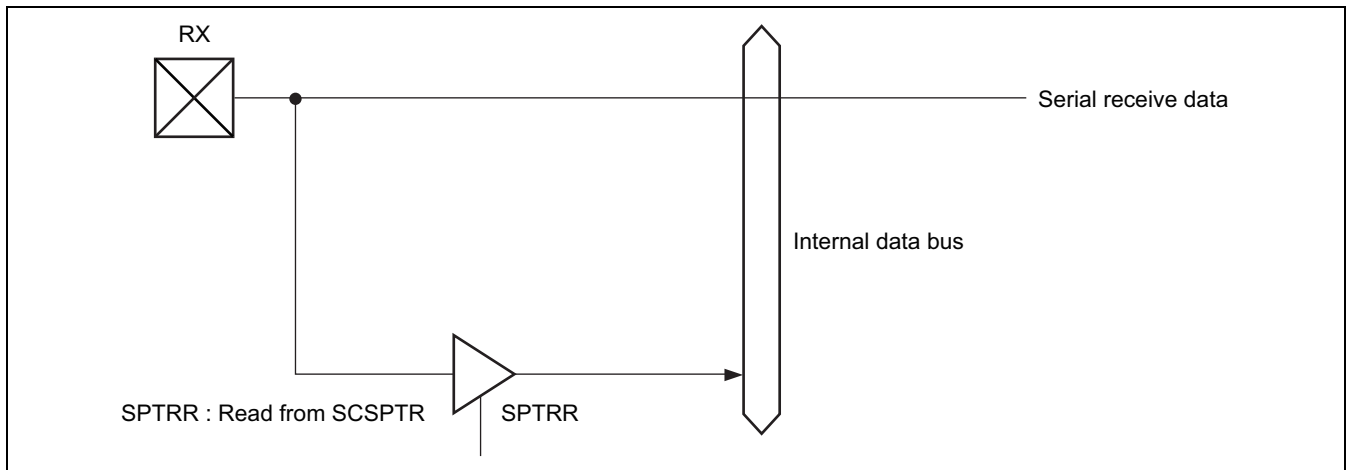


Figure 40.6 RX Pin



### 40.2.12 Line Status Register (SCLSR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	TO	—	ORER
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R/(W)*	R	R/(W)*

Note: Only 0 can be written to clear the flag.

Bit	Bit Name	Initial Value	R/W	Description
15 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2	TO	0	R/(W)*	<p>Timeout</p> <p>Indicates that the number of data bytes in SCFRDR is less than the receive trigger count, and that no further data has been received for at least 15 etu after the stop bit of the last receive data in asynchronous mode. This bit is not set in clock synchronous mode.</p> <p>0: Indicates that data is being received or has been successfully received and that there is no receive data in SCFRDR.</p> <p>[Clearing conditions]</p> <ul style="list-style-type: none"> <li>A power-on reset is executed.</li> <li>All the receive data in the SCFRDR has been read, and 0 is written to TO.</li> </ul> <p>1: Indicates that no further receive data has been received (receive timeout).</p> <p>[Setting condition]</p> <ul style="list-style-type: none"> <li>The number of data bytes in SCFRDR is less than the receive trigger count and no further data has been received for at least 15 etu after the stop bit of the last receive data.*</li> </ul> <p>Note: etu: Elementary Time Unit (time for transfer of 1 bit) Equivalent to 1.5 frames with an 8-bit, 1-stop-bit format.</p>
1	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
0	ORER	0	R/(W)*	<p>Overrun Error</p> <p>Indicates that an overrun error has occurred in reception and abnormal termination is caused.</p> <p>If an overrun error occurs, the receive data prior to the overrun error is retained in SCFRDR and the data received subsequently is discarded.</p> <p>Any subsequent serial reception is disabled while the ORER flag is 1.</p> <p>To resume data reception after clearing the ORER flag, be sure to first read (or clear) data in the receive FIFO and handle the error, then clear the ORER flag.</p> <p>0: Indicates that data is being received or has been successfully received.</p> <p>[Clearing conditions]</p> <ul style="list-style-type: none"> <li>• A power-on reset is executed.</li> <li>• 0 is written to ORER.</li> </ul> <p>1: Indicates that an overrun error has occurred in reception.</p> <p>[Setting condition]</p> <ul style="list-style-type: none"> <li>• The next serial reception has been completed while SCFRDR is full of 16-byte data.</li> </ul> <p>Note: When bit RE in SCSCR is cleared to 0, the ORER flag is not affected and its previous state is retained.</p>

Note: Writing 0 is only available to clear the flag.

### 40.3 Operation

<b>RZ/G1H</b>	<b>RZ/G1N</b>
<b>RZ/G1M</b>	<b>RZ/G1E</b>

#### 40.3.1 Operation in Asynchronous Mode

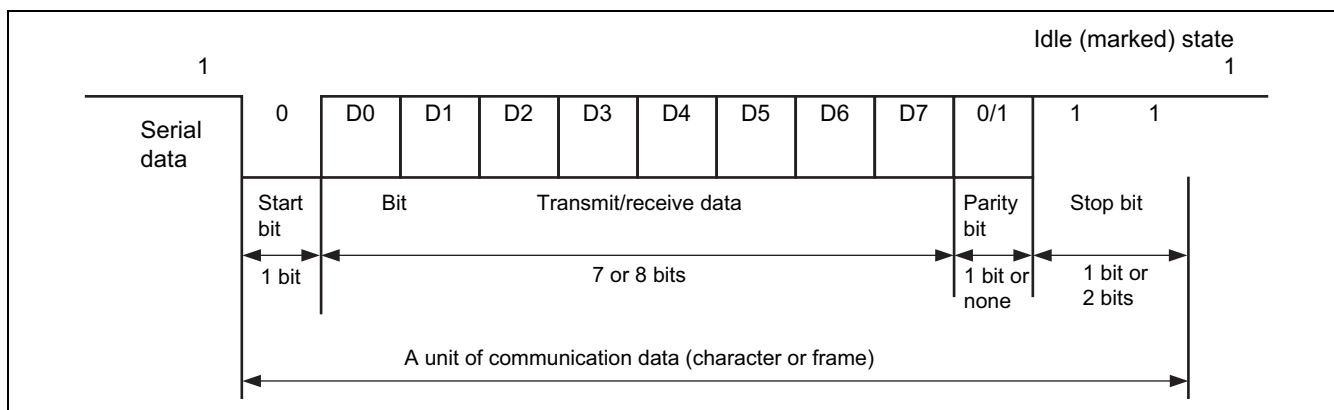
In asynchronous mode, the SCIF performs serial communication, in which data is transmitted/received in character units using the attached start bit indicating the start of communication and stop bit indicating the end of communication.

Figure 40.7 shows the general format for asynchronous serial communication.

In asynchronous serial communication, the transmission line is usually kept marked (high level). The SCIF monitors the transmission line, and when it finds a space (low level), it regards the space as a start bit and starts serial communication.

One character in serial communication consists of a start bit (low level), followed by transmit/receive data (LSB-first; from the lowest bit), a parity bit (high or low level), and a stop bit (high level).

During reception in asynchronous mode, the SCIF performs synchronization at the falling edge of the start bit. Communication data is acquired at the center of each bit because the SCIF samples data at the eighth pulse of the clock which has a frequency of 16 times the bit rate.



**Figure 40.7 Data Format in Asynchronous Mode  
(Example of 8-Bit Data with Parity and Two Stop Bits)**

**(1) Transmission/Reception Format**

Table 40.6 shows available data transfer formats. The SCIF supports 8 transfer formats, which can be specified by SCSMR.

**Table 40.6 Serial Transmission/Reception Formats (Asynchronous Mode)**

SCSMR Settings			Serial Transmission/Reception Format and Frame Length												
CHR	PE	STOP	1	2	3	4	5	6	7	8	9	10	11	12	
0	0	0	S	8-bit data							STOP				
		1	S	8-bit data							STOP	STOP			
1	0	0	S	8-bit data							P	STOP			
		1	S	8-bit data							P	STOP	STOP		
1	0	0	S	7-bit data						STOP					
		1	S	7-bit data						STOP	STOP				
	1	0	S	7-bit data						P	STOP				
		1	S	7-bit data						P	STOP	STOP			

[Legend]

- S: Start bit
- STOP: Stop bit
- P: Parity bit

**(2) Clock**

The transfer clock can be selected from the following two clocks using the CKE[1:0] bits in SCSCR:

- Internal clock generated by the on-chip baud rate generator
- External clock generated by an external clock baud rate generator

**(3) Data Transmission/Reception**

**(a) Initialization of SCIF (Asynchronous Mode)**

Before transmitting/receiving data or changing the operating mode or communication format, the SCIF should be initialized using the sample flowchart for SCIF initialization shown in Figure 40.8.

[Notes]

Clearing the TE bit to 0 initializes SCTSR. However, SCFSR, SCFTDR, and SCFRDR contents are retained even if the TE and RE bits are cleared to 0.

The TE bit should be cleared to 0 after all transmit data has been sent and the TEND flag has been set in SCFSR. The TE bit can be cleared to 0 during transmission, but the data being transmitted will enter the marked state after clearing. In addition, before setting the TE bit to 1 to restart the transmission, set the TFRST bit to 1 in SCFCR to reset SCFTDR.

When an external clock is used, do not stop the clock during operation or initialization. If stopped, the operation will be unreliable. Furthermore, when the baud rate generator for external clock is also to be used, be sure to make settings for it before starting initialization of the SCIF.

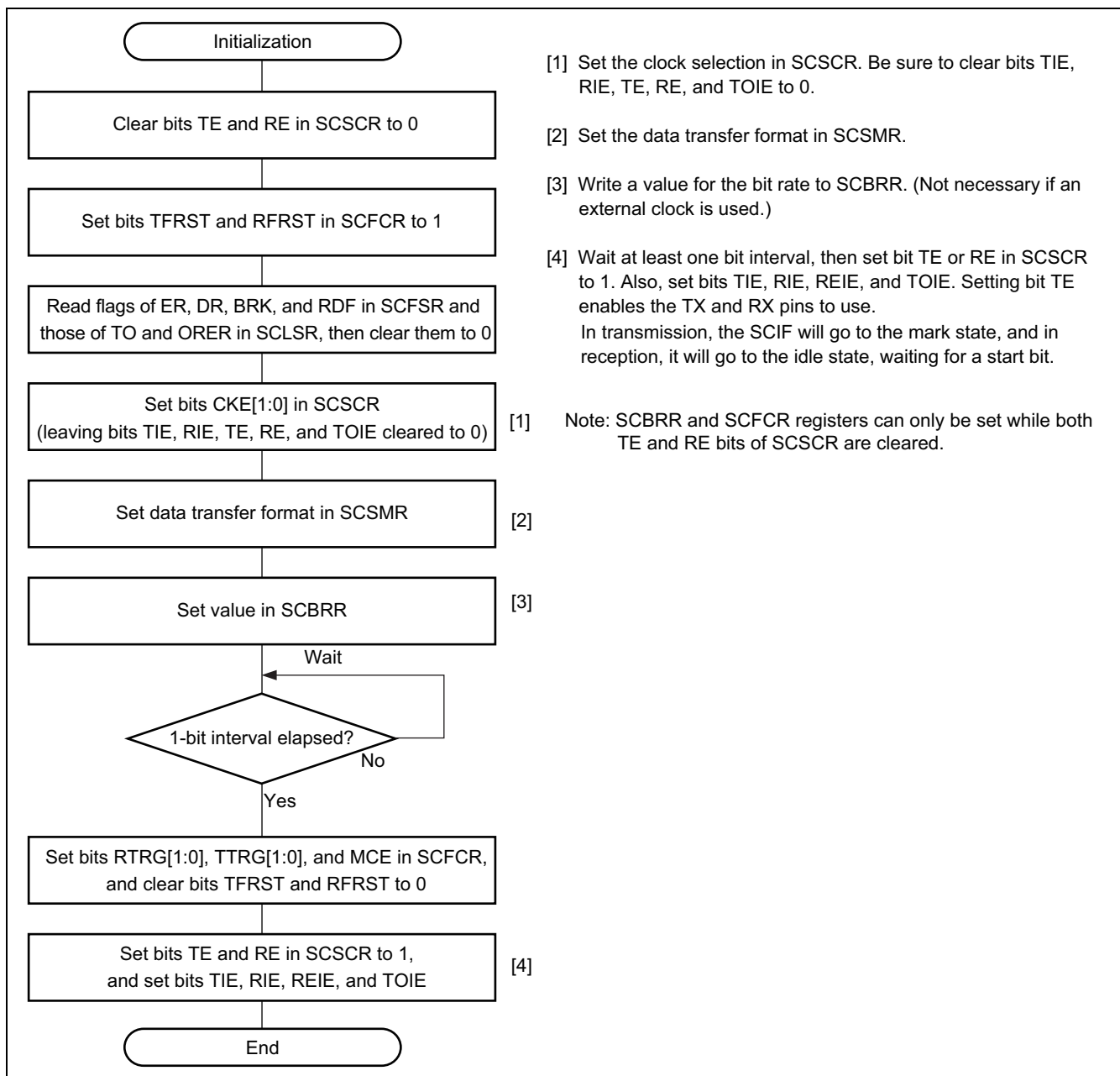
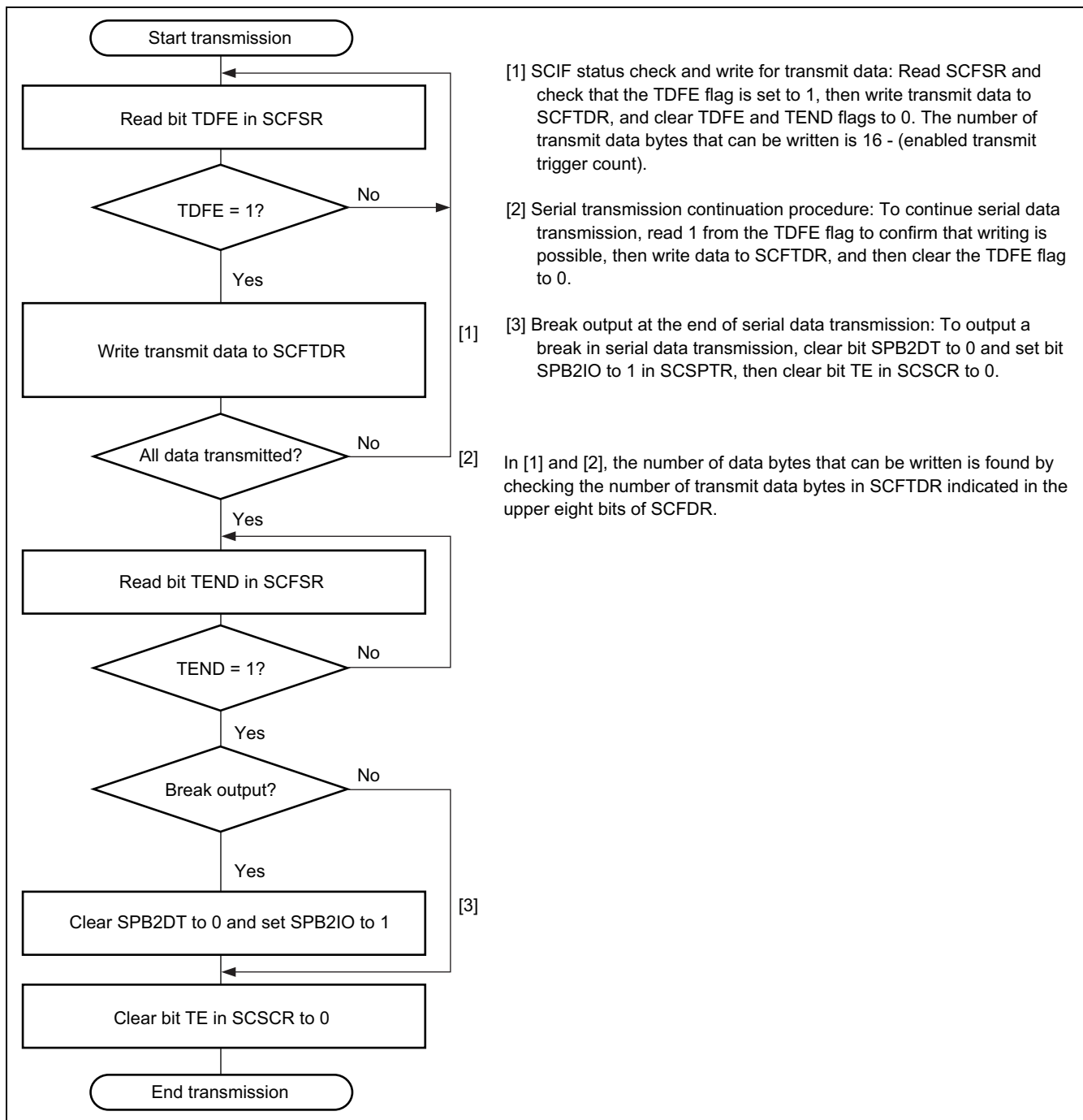


Figure 40.8 Sample Flowchart for Initializing the SCIF

**(b) Serial Data Transmission (Asynchronous Mode)**

Figure 40.9 shows a sample flowchart for serial transmission.

After the SCIF transmission operation is enabled, serial data transmission can be performed using the following procedure:

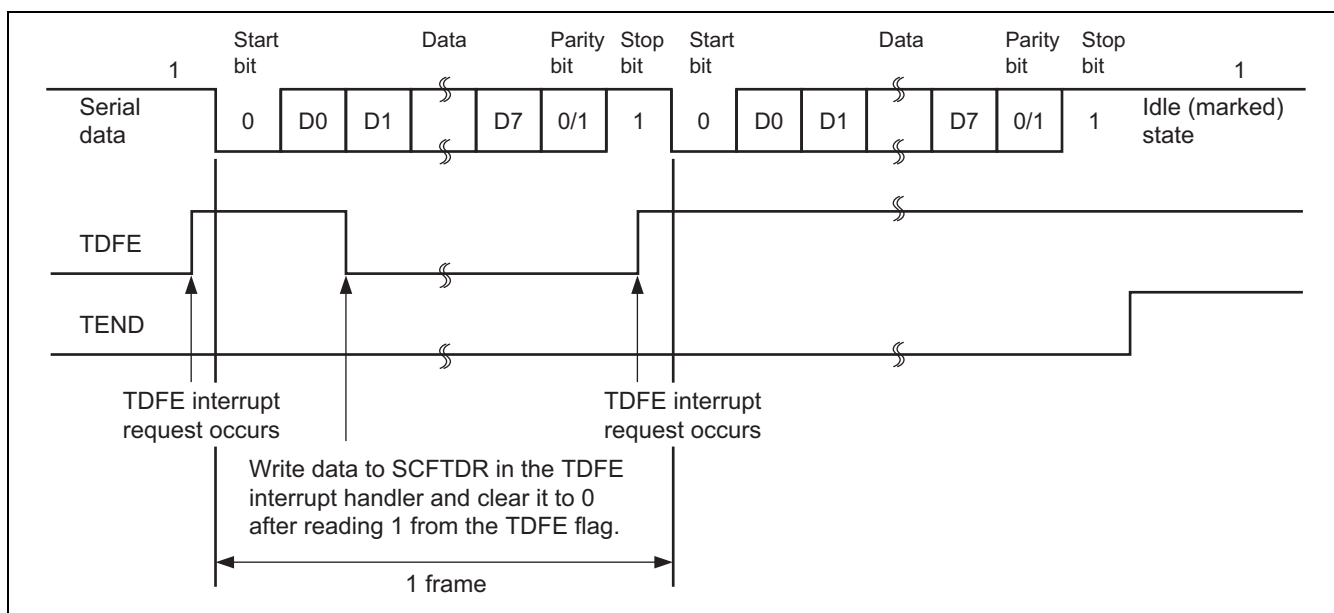


**Figure 40.9 Sample Flowchart for Serial Transmission**

In serial transmission, the SCIF operates as follows:

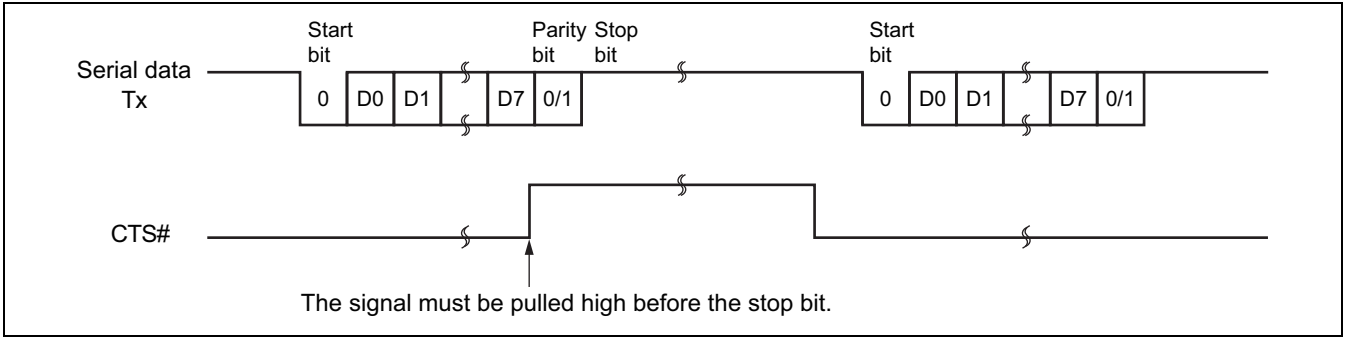
1. When data is written to SCFTDR, the SCIF transfers the data from SCFTDR to SCTSR and starts transmitting. Confirm that the TDFE flag in SCFSR is set to 1 before writing transmit data to SCFTDR. The number of data bytes that can be written is at least (16- (transmit trigger count)).
2. When data is transferred from SCFTDR to SCTSR and the SCIF starts transmission, consecutive transmission is performed until there is no transmit data left in SCFTDR. When the number of transmit data bytes in SCFTDR is equal to or less than the transmit trigger count specified in SCFCR, the TDFE flag is set. If the TIE and TEIE bits in SCSCR are set to 1 and 0, respectively at this time, a transmit-FIFO-data-empty interrupt (TDFE) request occurs. The serial transmit data is sent from the TX pin in the following order:
  - A. Start bit: One 0-bit is output.
  - B. Transmit data: 8- or 7-bit data is output in LSB-first order.
  - C. Parity bit: One parity bit (even or odd parity) is output.  
A format that does not output a parity bit can also be selected.
  - D. Stop bit(s): One or two 1-bits (stop bits) are output.
  - E. Marked state: 1 is output continuously until the start bit that starts the next transmission is sent.
3. The SCIF checks transmit data in SCFTDR when sending the stop bit. If there is data in it, the SCIF transfers the data from SCFTDR to SCTSR, sends the stop bit, and then starts serial transmission of the next frame. If there is no transmit data, the SCIF sets the TEND flag to 1 in SCFSR and sends out the stop bit, and then the marked state is entered to output 1 continuously. At this time, if the TIE and TEIE bits in SCSCR are set to 1, a transmit-end interrupt (TEND) request occurs.

Figure 40.10 shows an example of transmission in asynchronous mode.



**Figure 40.10 Sample SCIF Transmission Operation (Example of 8-Bit Data with Parity and One Stop Bit)**

4. When modem control is enabled, transmission can be stopped or resumed in accordance with the CTS# input value. When CTS# is set to 1 during transmission, the marked state is entered after one frame of data transmission is ended. Setting CTS# to 0 restarts outputting the next transmit data from the start bit. Figure 40.11 shows an example of the operation with modem control enabled.

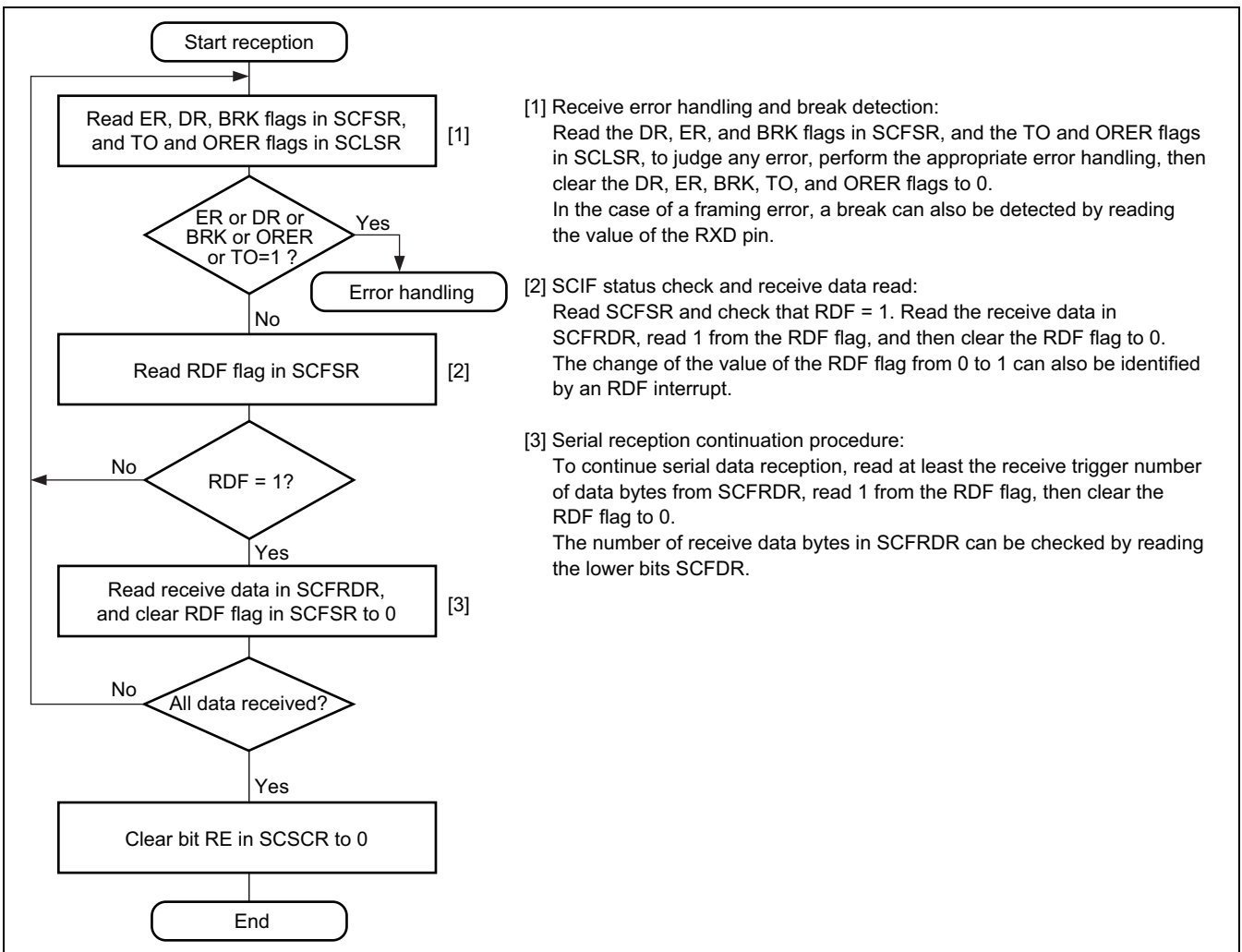


**Figure 40.11 Sample Operation with Modem Control Enabled (CTS#)**

**(c) Serial Data Reception (Asynchronous Mode)**

Figures 40.12 and 40.13 show sample flowcharts for serial reception.

After the SCIF reception operation is enabled, serial data reception can be performed using the following procedure:



**Figure 40.12 Sample Flowchart for Serial Reception (1)**



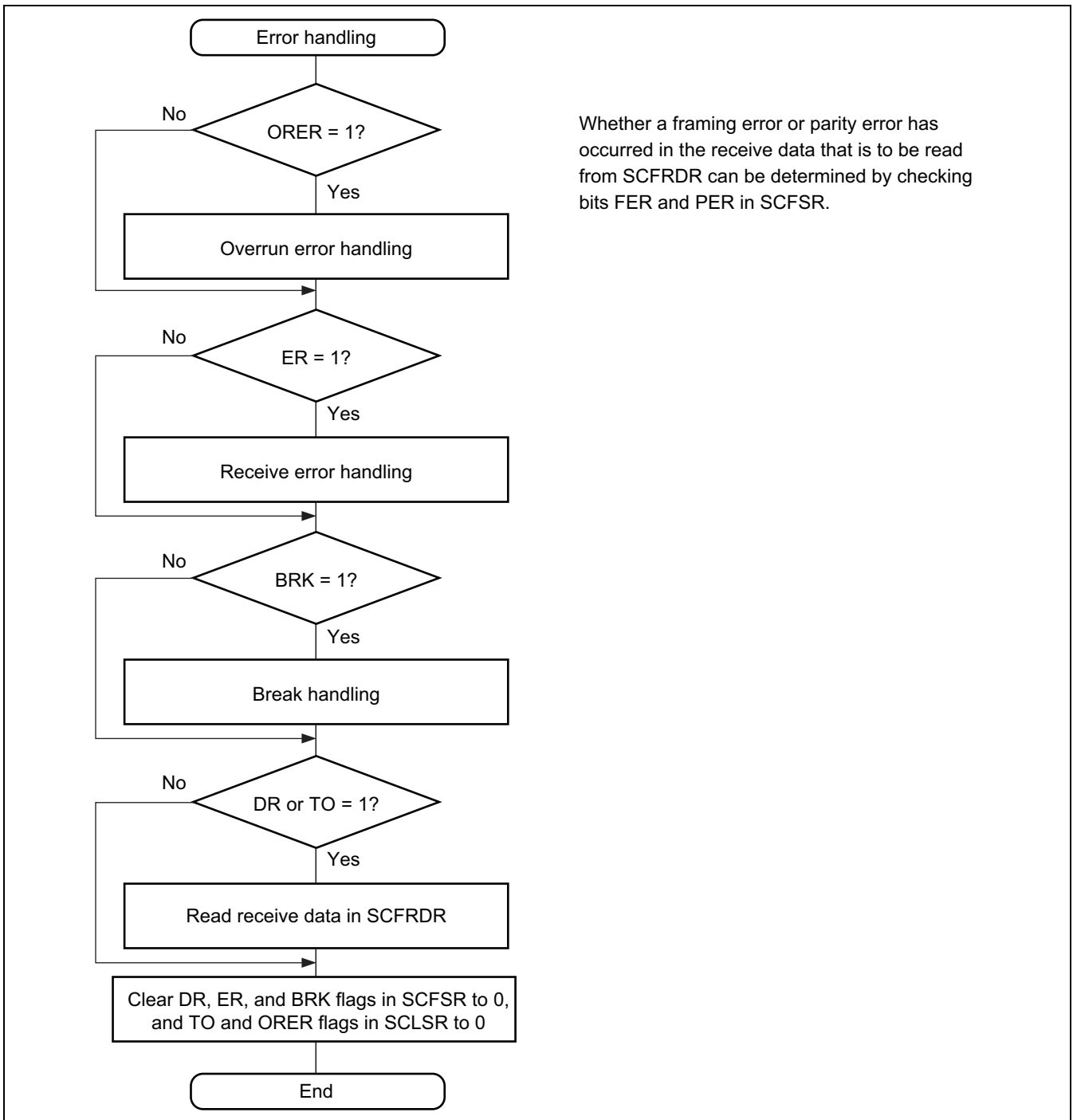


Figure 40.13 Sample Flowchart for Serial Reception (2)

In serial reception, the SCIF operates as follows:

1. The SCIF monitors the transmission line, and when detecting the start bit 0, it performs internal synchronization and starts reception.
2. The SCIF stores the received data in SCRSR in LSB-to-MSB order.
3. The SCIF receives the parity bit and stop bit.

After receiving these bits, the SCIF performs the following checks:

A. Stop bit: The SCIF checks whether the stop bit is 1.

If there are two stop bits, it checks only the first stop bit.

B. Receive data: The SCIF checks that receive data can be transferred from the receive shift register (SCRSR) to SCFRDR.

C. Overrun error: The SCIF checks that the ORER flag is 0, indicating that no overrun error has occurred.

D. Break state: The SCIF checks that the BRK flag is 0, indicating that the break state is not set.

If the SCIF can confirm the conditions of (b), (c), and (d), it stores the receive data in SCFRDR.

Note: The SCIF continues to receive data even when a parity error or a framing error occurs.

4. If the RDF flag changes to 1 while the RIE bit in SCSCR is 1, a receive-FIFO-data-full interrupt (RDF) request occurs.

If the DR flag changes to 1 while the RIE bit in SCSCR is 1, a receive-data-ready interrupt (DR) request occurs.

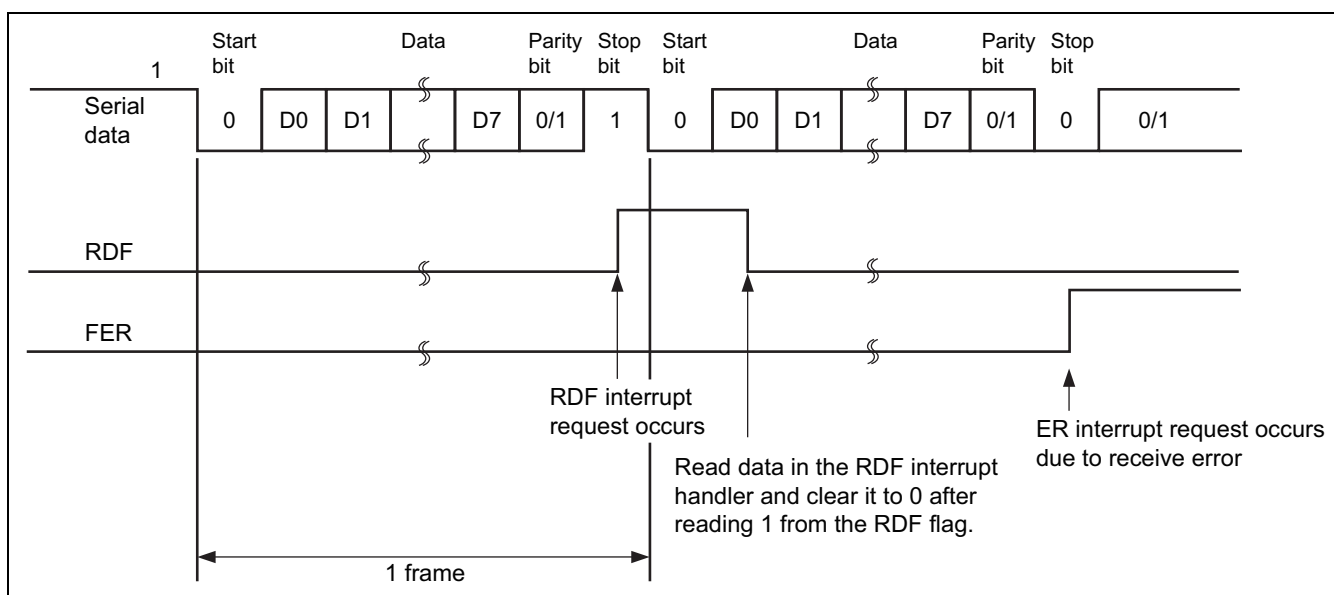
If the TO flag changes to 1 while the TOIE bit in SCSCR is 1, a timeout interrupt (TO) request occurs.

If the ER flag changes to 1 while the RIE or REIE bit in SCSCR is 1, a receive-error interrupt (ER) request occurs.

If the BRK flag changes to 1 while the RIE or REIE bit in SCSCR is 1, a break interrupt (BRK) request occurs.

If the ORER flag changes to 1 while the RIE or REIE bit in SCSCR is 1, an overrun-error interrupt (ORER) request occurs.

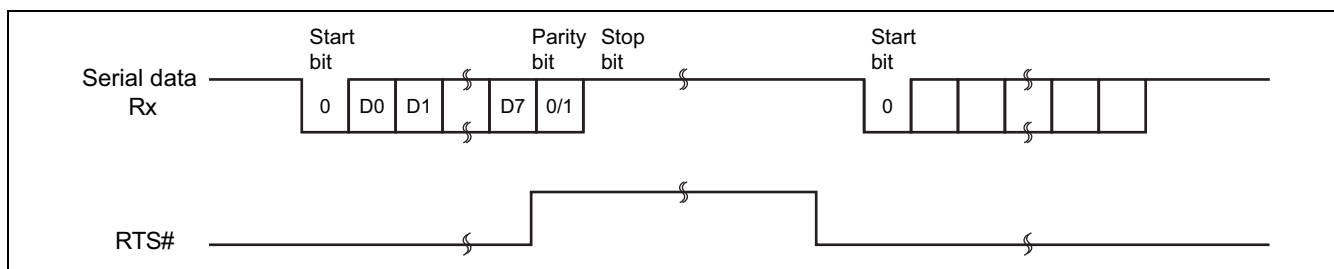
Figure 40.14 shows an example of reception in asynchronous mode.



**Figure 40.14 Sample SCIF Receive Operation  
(Example of 8-Bit Data with Parity and One Stop Bit)**

5. When modem control is enabled, the RTS# signal is output when SCFRDR is empty. When RTS# is 0, data can be received. When RTS# is set to 1, the number of data bytes in SCFRDR is equal to or more than the RTS# output active trigger count.

Figure 40.15 shows an example of the operation with modem control enabled.



**Figure 40.15 Example of the Operation with Modem Control Enabled (RTS#)**

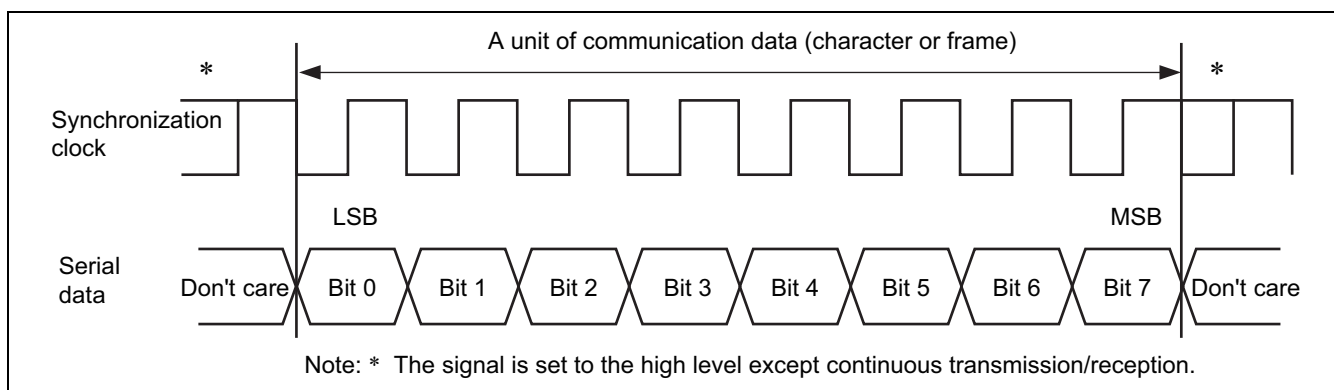
### 40.3.2 Operation in Clock Synchronous Mode

Clock synchronous mode, in which data is transmitted and received in synchronization with clock pulses, is suitable for fast serial communication.

Figure 40.16 shows the general format for clock synchronous serial communication. In the clock synchronous serial communication, data on the communication line is output between one falling edge of the synchronization clock and the next falling edge. The data decision is done at the rising edge of the clock.

In serial communication, each character is output starting with the LSB and ending with the MSB. After the MSB is output, the communication line retains the state of the last data.

In clock synchronous mode, the SCIF receives data in synchronization with a rising edge of the synchronization clock.



**Figure 40.16 Data Format for Clock Synchronous Communication**

#### (1) Data Transfer Format

The data transfer format is fixed to 8 bits. No parity bit can be added.

#### (2) Clock

The clock can be selected from the following two clocks using the C/A bit in SCSMR and the CKE[1:0] bits in SCSCR:

- Internal clock generated by the on-chip baud rate generator
- External synchronization clock input at the SCK pin

When the SCIF is operated on an internal clock, the synchronization clock is output from the SCK pin. Eight synchronization clock pulses are output in one-character transfer, and when no transfer is performed the clock is fixed high. When only reception operation is performed, selecting an internal clock outputs clock pulses until the number of data bytes in the receive FIFO reaches the specified receive trigger count, while the RE bit in SCSCR is 1.

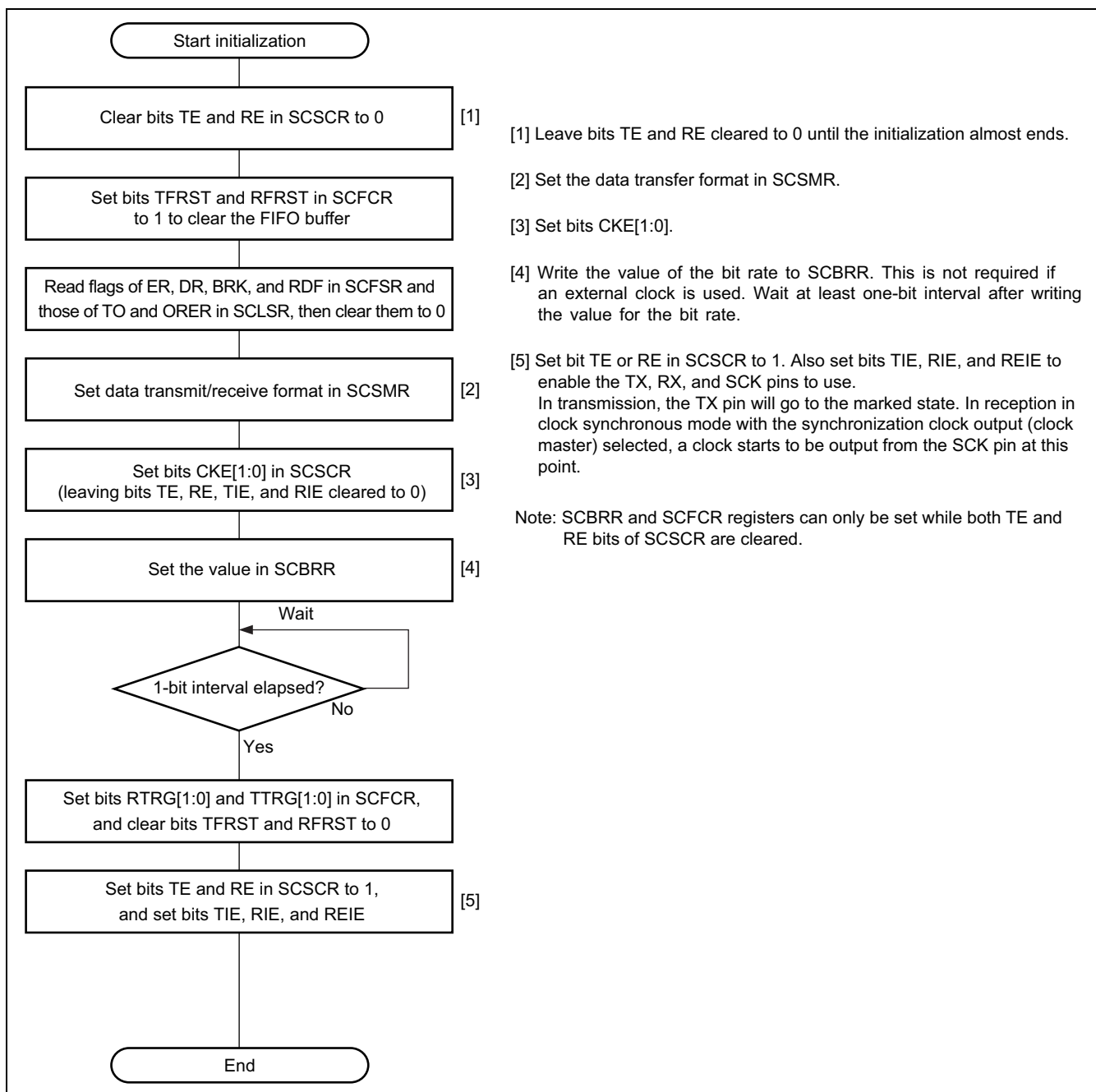
**(3) Data Transmission/Reception**

**(a) Initialization of SCIF (Synchronous Mode)**

Before transmitting/receiving data or changing the operating mode or communication format, the TE and RE bits in SCSCR to 0 and then the SCIF should be initialized using the sample flowchart for SCIF initialization shown in Figure 40.17.

[Note]

Clearing the TE bit to 0 initializes SCTSR. However, clearing the RE bit to 0 does not affect the RDF, PER, FER, and ORER flags and SCFRDR contents.

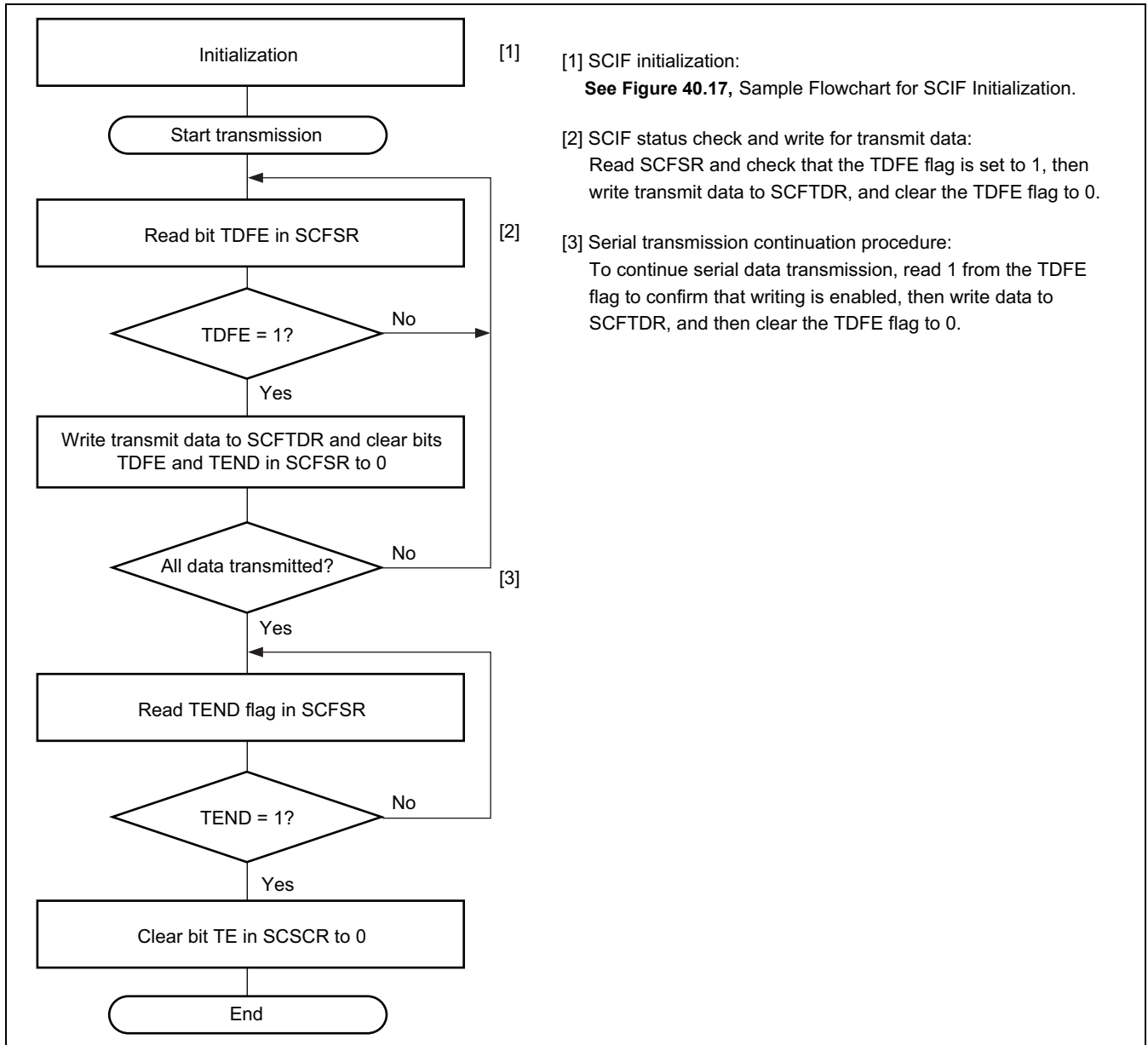


**Figure 40.17 Sample Flowchart for SCIF Initialization**

**(b) Serial Data Transmission (Clock Synchronous mode)**

Figure 40.18 shows a sample flowchart for serial transmission.

After the SCIF transmission operation is enabled, serial data transmission can be performed using the following procedure:



**Figure 40.18 Sample Flowchart for Serial Transmission**

In serial data transmission, the SCIF operates as described below:

1. When data is written to SCFTDR, the SCIF transfers the data from SCFTDR to SCTSR to start transmission. Confirm that the TDFE flag in SCFSR is set to 1 before writing transmit data to SCFTDR. The number of data bytes that can be written is at least (16- (the transmit trigger count)).
2. After the SCIF transfers data from SCFTDR to SCTSR and starts data serial transmission, the SCIF consecutively transmits it until there is no transmit data left in SCFTDR. When the number of transmit data bytes in SCFTDR is equal to or less than the transmit trigger count set in SCFCR, the TDFE flag is set. If the TIE and TEIE bits in SCSCR are set to 1 and 0, respectively at this time, a transmit-FIFO-data-empty interrupt (TDFE) request occurs. When the external clock is selected, data is output in synchronization with the input clock. The serial transmit data is output at the TX pin in the LSB-first order.
3. The SCIF checks transmit data in SCFTDR when sending the last bit. If there is transmit data, the SCIF transfers the data to SCTSR, and starts serial transmission of the next frame. If there is no transmit data left, the TEND flag in SCFSR is set to 1, and the transmit data pin (TX pin) retains its state after the last bit is sent. At this time, if the TIE and TEIE bits in SCSCR are set to 1, a transmit-end interrupt (TEND) request occurs.
4. After serial transmission ends, the SCK pin is fixed high.

Note: In clock synchronous mode, when transmit data is written to SCFTDR by the DMAC, the TEND flag may not be cleared. Therefore, if the DMAC is used for transmission in clock synchronous mode, read the TEND flag in the following method.

1. Confirm that data transfer is completed in the DMAC.
2. Read the TEND flag.
3. Clear the TEND flag to 0 if TEND = 1.
4. Read the TEND flag again.
5. Use the second-read TEND flag.

Figure 40.19 shows an example of SCIF serial transmission in clock synchronous mode.

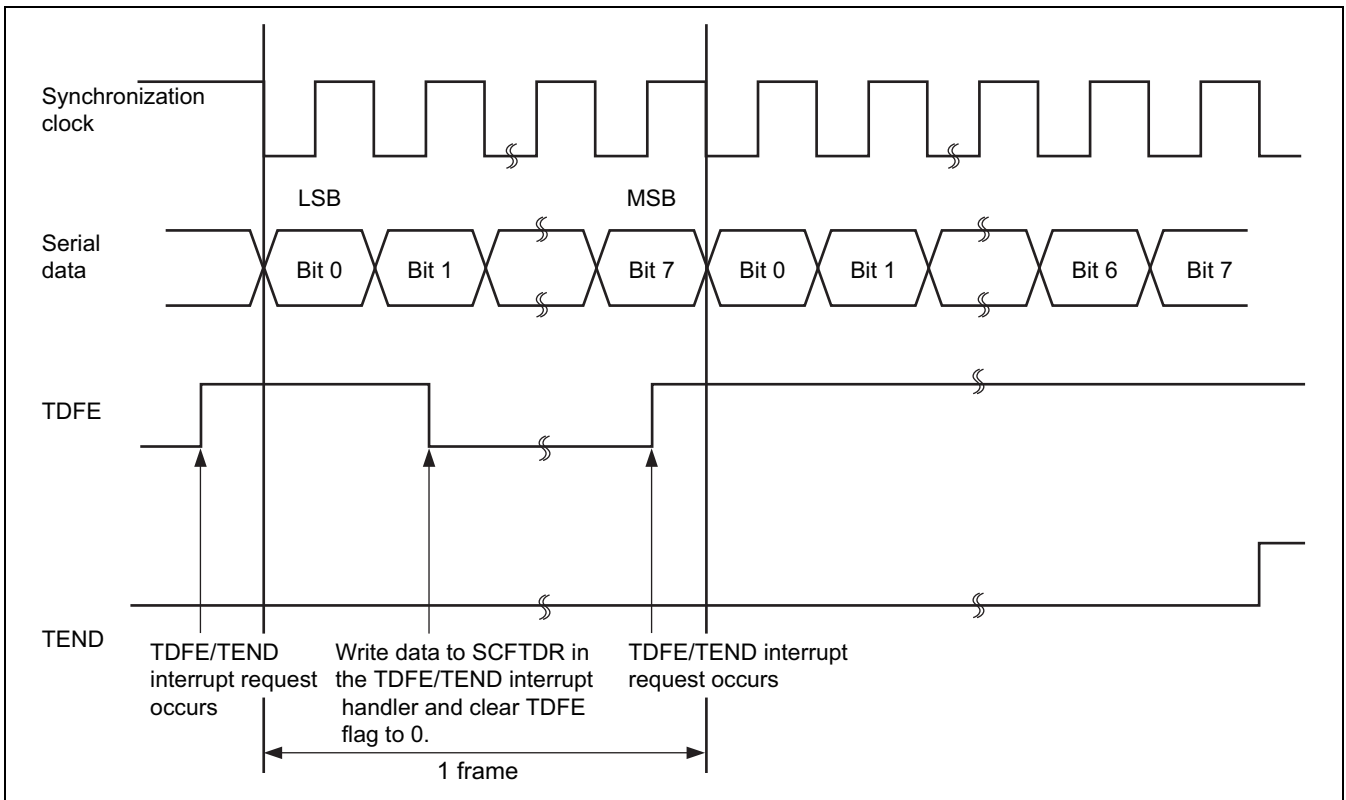


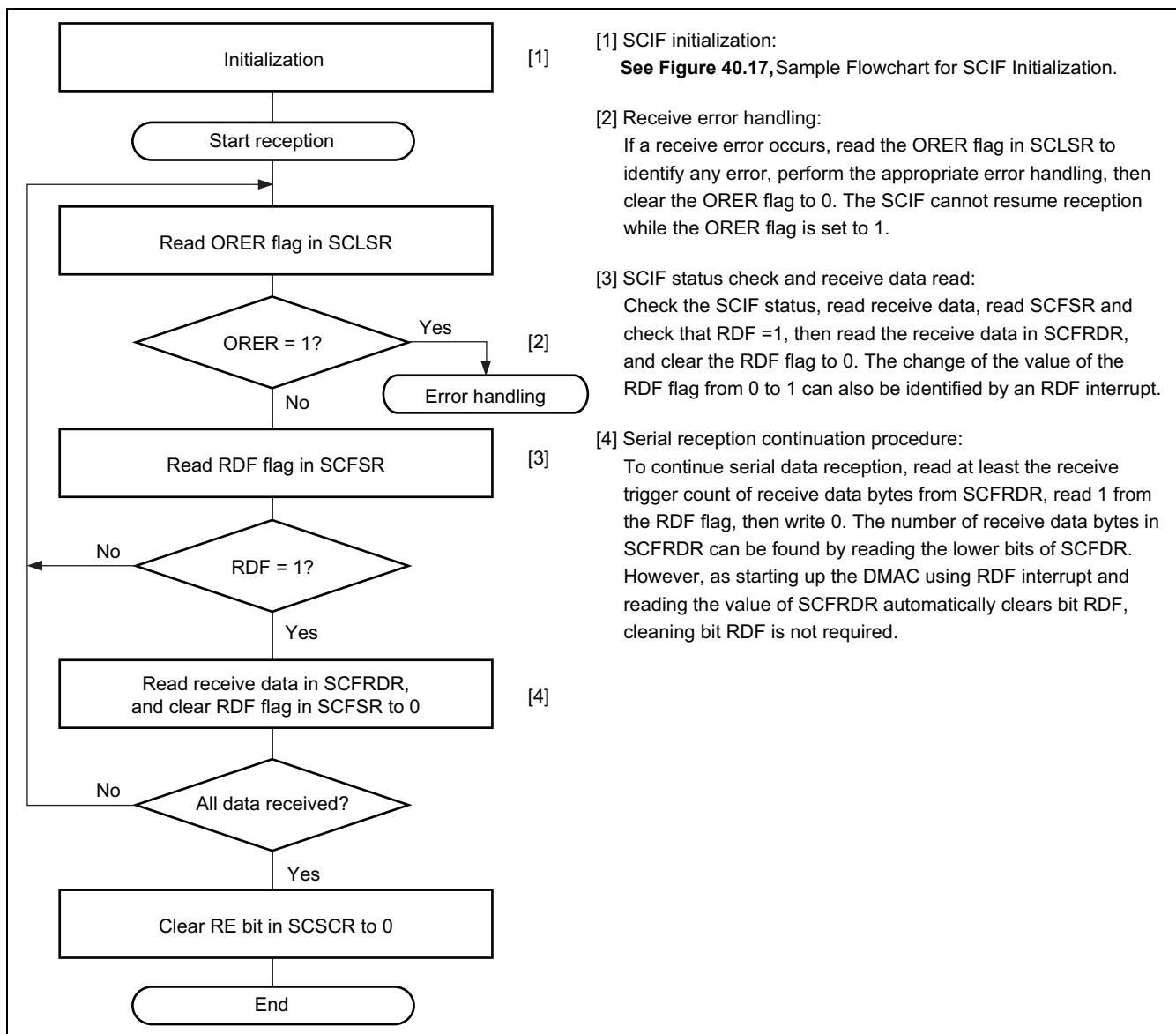
Figure 40.19 Example of SCIF Serial Transmission in Clock Synchronous Mode

**(c) Serial Data Reception (Clock Synchronous Mode)**

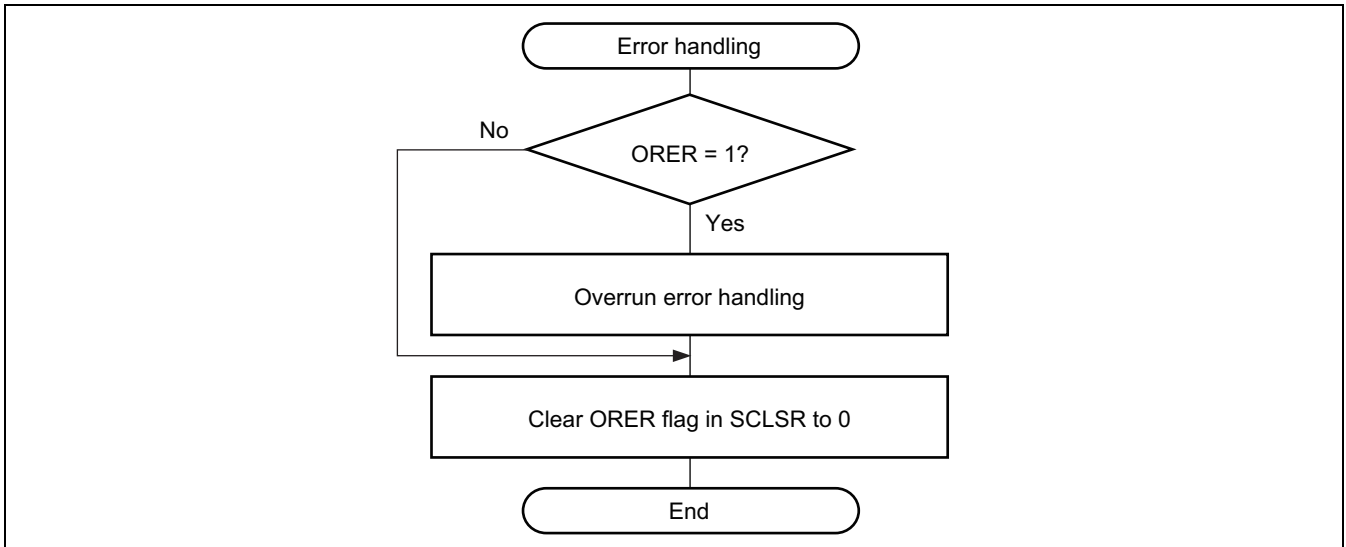
Figures 40.20 and 40.21 show sample flowcharts for serial reception.

The SCIF reception should be enabled before taking the following steps for serial data transmission.

When switching operating mode from asynchronous mode to clock synchronous mode without initializing the SCIF, check that the ORER, PER3 to PER0, and FER3 to FER0 flags are cleared to 0.



**Figure 40.20 Sample Flowchart for Serial Data Reception**



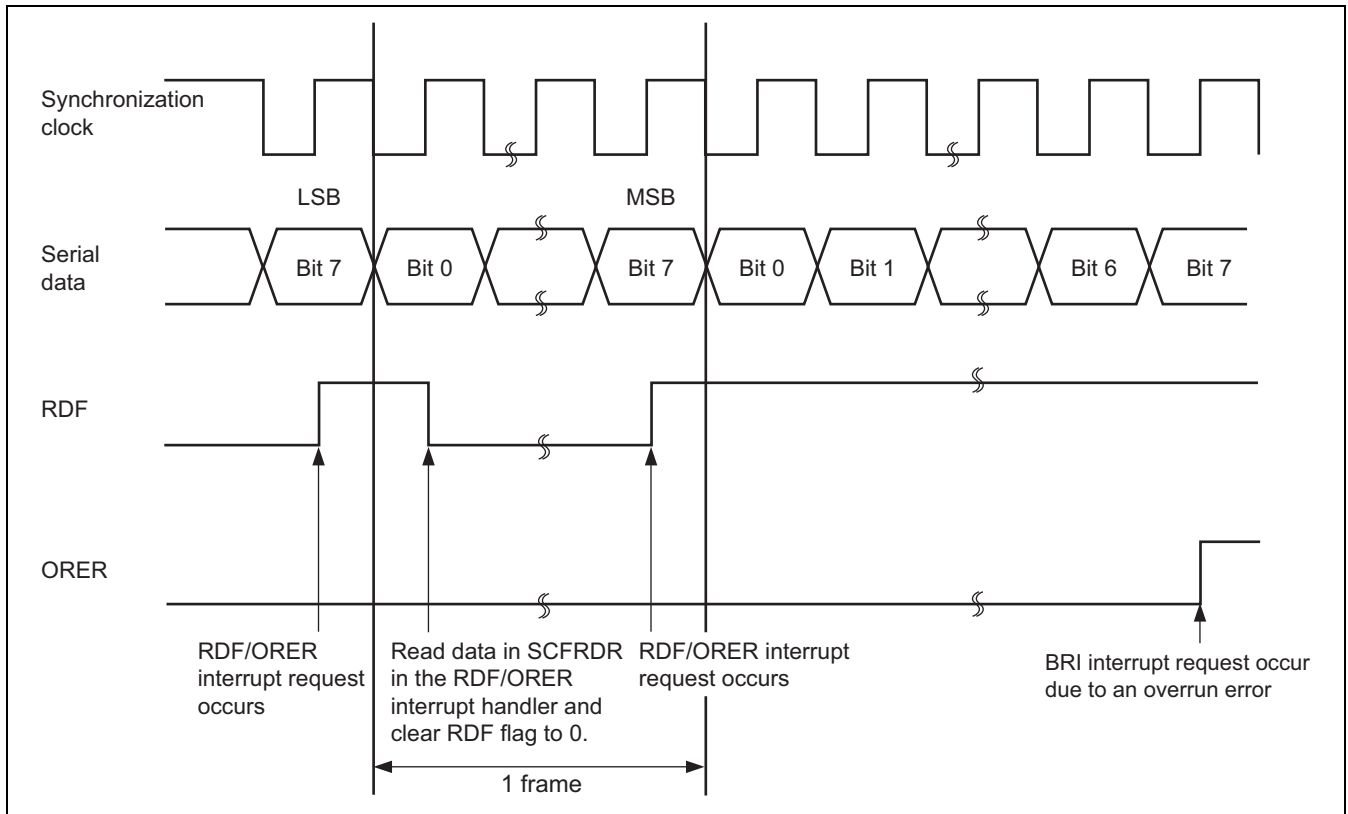
**Figure 40.21 Sample Flowchart for Serial Data Reception**

In serial data reception, the SCIF operates as described below:

1. The SCIF starts receiving data in synchronization with synchronization clock input or output.
2. The SCIF stores receive data in SCRSR in LSB-to-MSB order.  
After receiving the data, the SCIF first checks if the receive data can be transferred from SCRSR to SCFRDR, then starts storing the receive data in SCFRDR.  
If the SCIF detects an overrun error, the SCIF cannot receive subsequent data.
3. If the RDF flag changes to 1 while the RIE bit in SCSCR is 1, a receive-FIFO-data-full interrupt (RDF) request occurs. If the ORER flag changes to 1 while the RIE or REIE bit in SCSCR is 1, a break interrupt (BRI) request occurs.



Figure 40.22 shows an example of SCIF reception in clock synchronous mode.

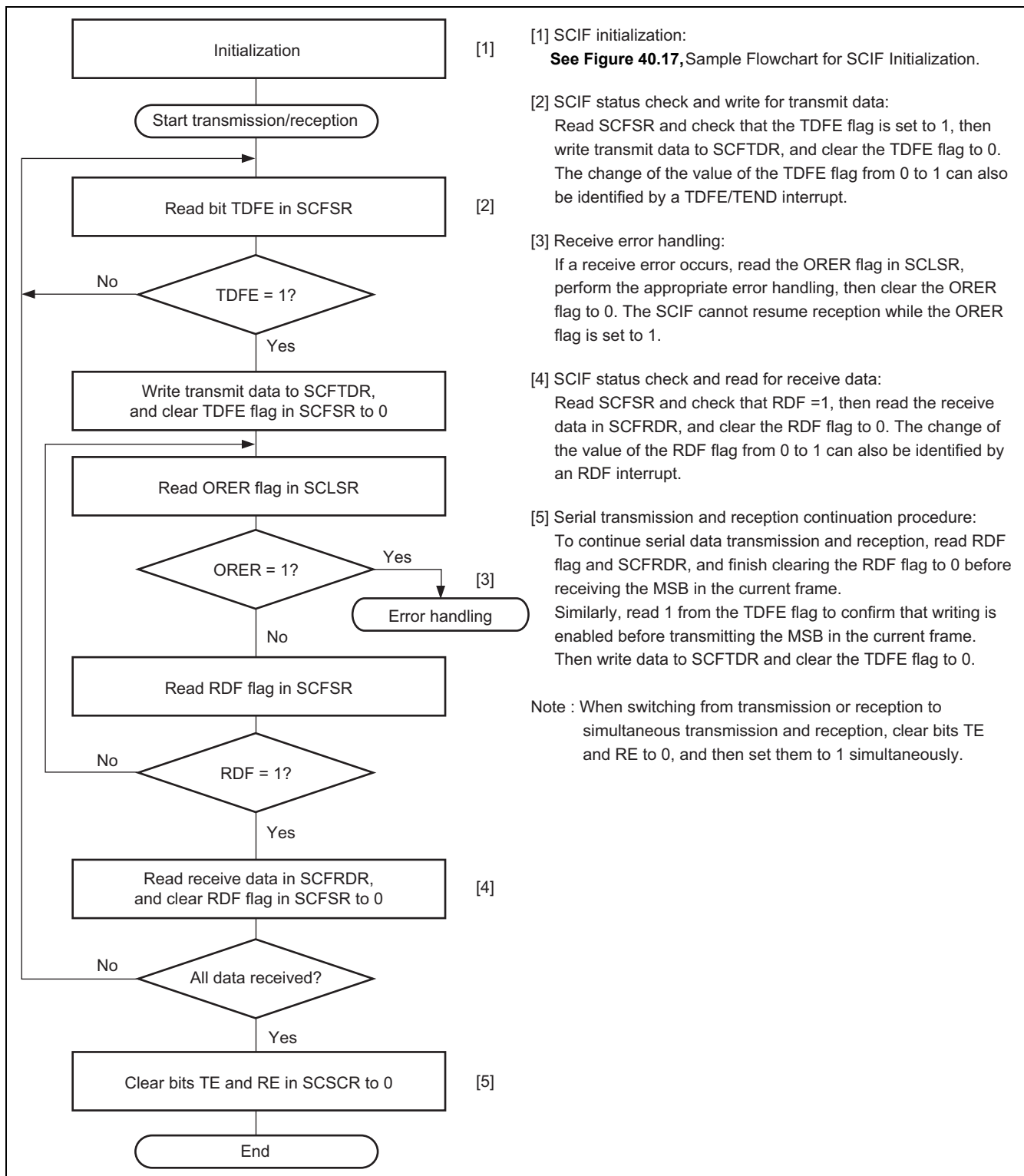


**Figure 40.22 Example of SCIF Reception in Clock Synchronous Mode**

**(d) Simultaneous Serial Data Transmission/Reception (Clock Synchronous Mode)**

Figure 40.23 shows a sample flowchart for simultaneous serial data transmission/reception.

The SCIF transmission and reception should be enabled before taking the following steps for simultaneous serial data transmission/reception.



**Figure 40.23 Sample Flowchart for Simultaneous Serial Data Transmission/Reception**

## 40.4 SCIF Interrupt Sources and the DMAC

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

If the DMAC is used for transmission/reception, set and enable the DMAC before setting the SCIF.

### Transmission Interrupts and DMA Transfer:

If the TDFE/TEND flag in SCFSR is set to 1 when the TDFE/TEND interrupt is enabled by the TIE bit, a TDFE/TEND interrupt request and a transmit-FIFO-data-empty DMA transfer request will occur. If the TDFE/TEND flag is set to 1 when TDFE/TEND interrupt is disabled by the TIE bit, only the transmit-FIFO-data-empty DMA transfer request will occur. (A transmit-FIFO-data-empty DMA transfer request is generated when the TDFE flag is set while TEIE is 0, or when the TEND flag is set while TEIE is 1. DMA transfer requests are not affected by the TEIE bit.)

When TDFE/TEND interrupt requests are enabled, the interrupt requests are cleared by the DMAC regardless of the interrupt handling program.

### Reception Interrupts and DMA Transfer:

If the RDF/DR flag in SCFSR is set to 1 when RDF/DR interrupt is enabled by the RIE bit, an RDF/DR interrupt request occurs. If the RDF/DR flag is set to 1, a receive-FIFO-data-full DMA transfer request occurs. If the RDF/DR flag is set to 1 when RDF/DR interrupt is disabled by the RIE bit, and only a receive-FIFO-data-full DMA transfer request occurs and DMAC can be activated to perform data transfer.

Setting the RIE bit in SCSCR to 0 and the REIE bit to 1 generates the ER/BRK/ORER interrupt requests without generating RDF/DR interrupt requests. When the BRK flag in SCFSR or the ORER flag in SCLSR is set to 1, BRK/ORER interrupt requests occur.

If the TO flag is set to 1 in SCLSR when TO interrupts are enabled by the TOIE bit, TO interrupt requests occur.

DR/TO interrupt requests generated by setting the DR or TO flag to 1 or receive-FIFO-data-full DMA transfer requests occur only in asynchronous mode.

When DR/TO interrupt requests are enabled to be issued, interrupt requests generated by the DR flag are cleared by the DMAC regardless of the interrupt handling program, however, those generated by the TO flag are not cleared by the DMAC. Therefore, the TO flag interrupt requests need to be cleared with the interrupt handling program. (The DR and TO flags are set at the same time, but cleared separately.)

**Table 40.7 SCIF Interrupt Sources**

Interrupt Source	DMAC Activation	Priority on Reset Release
Interrupts generated by receive error flag (ER)	Disabled	High
Interrupts generated by receive-FIFO-data-full (RDF), receive-data-ready (DR) or timeout (TO) *	Enabled	↑ ↓
Interrupts generated by break (BRK) or overrun error (ORER)	Disabled	
Interrupts generated by transmit FIFO data empty (TDFE)	Enabled	Low

Note: \* RXI interrupts by means of the DR or TO flag are available only in asynchronous mode.

## 40.5 Usage Notes

RZ/G1H	RZ/G1N
RZ/G1M	RZ/G1E

Note the following on use of the SCIF.

### (1) Break Detection and Operation

Break signals can also be detected by reading the RX pin value directly when a framing error (FER) is detected. In the break state, the input values from the RX pin are all 0s. So, the parity error flag (PER) may be set after the FER flag is set to 1.

Although the SCIF stops receive data transfer to SCFRDR after detecting a break, it continues data reception.

### (2) Sending a Break Signal

The input/output condition and level of the TX pin are determined by the SPB2IO and SPB2DT bits in SCSPTR. This enables to send a break signal.

The pin does not function as the TX pin from the initialization of the serial transmitter to setting of the TE bit (enabling transmission). In this period, the marked state is substituted by the value of the SPB2DT bit. Therefore, the SPB2IO and SPB2DT bits should be set to 1 (designating output and high level) beforehand.

To send a break signal during serial transmission, clear the SPB2DT bit to 0 (low level), and then clear the TE bit to 0 (halting transmission). When the TE bit is cleared, the transmitter is initialized regardless of the current transmission state, and the TX pin outputs 0.

### (3) Data Sampling Timing and Reception Margin in Asynchronous Mode

In asynchronous mode, the SCIF operates on the base clock with a frequency 16 times the bit rate.

In reception, the SCIF performs the internal synchronization by sampling the fall edge of the start bit using the base clock. In addition, the SCIF takes receive data at the rising edge of the eighth pulse on the base clock.

Figure 40.24 shows the timing of this operation.

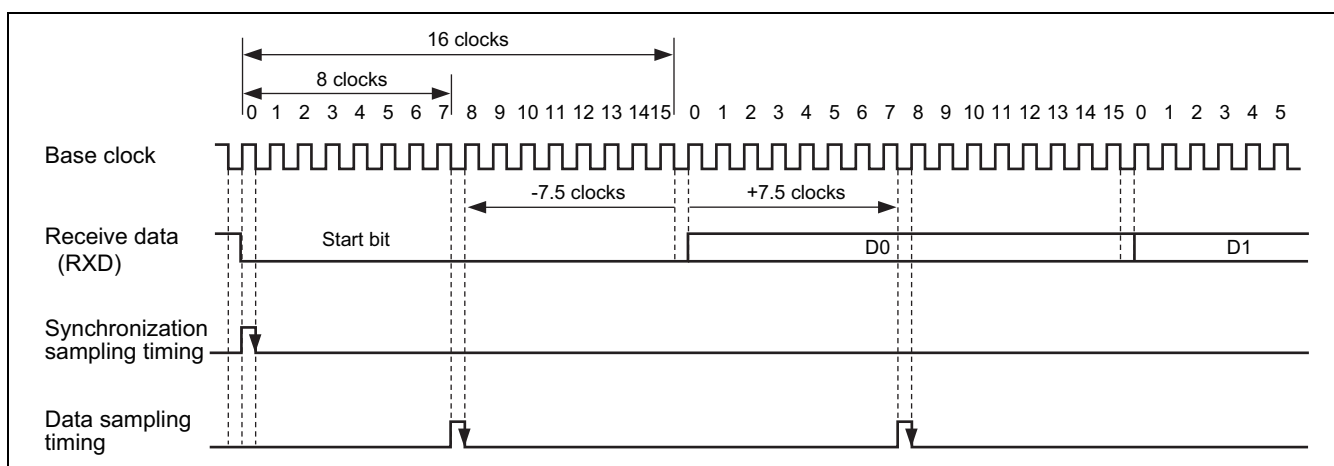


Figure 40.24 Timing Chart of Receive Data Sampling

The reception margin in asynchronous mode is given by formula (1).

$$M = \left| \left( 0.5 - \frac{1}{2N} \right) - (L - 0.5) F - \frac{|D - 0.5|}{N} (1 + F) \right| \times 100\% \dots\dots\dots \text{Expression (1)}$$

M: Receive margin (%)

N: Ratio of bit rate to clock (N = 16)

D: Clock duty (D = 0 to 1.0)

L: Frame length (L = 9 to 12)

F: Absolute value of clock frequency deviation

Assuming F = 0 and D = 0.5 for expression (1), the reception margin obtained with expression (2) is 46.875% as shown below:

Assuming D = 0.5 and F = 0

$$M = (0.5 - 1/(2 \times 16)) \times 100\%$$

$$= 46.875\% \dots\dots\dots \text{expression (2)}$$

This is a theoretical value. A reasonable margin allowed in system designs is 20% to 30%.

#### (4) Reception Margin and Baud Rate Error

The value of 46.875% obtained by the above expression (2) indicates the reception margin when the baud rate error is 0 (F = 0). If there is no error in the reception and transmission baud rates, reception is possible even with misalignment of approx. 1/2 bit. If there is an error in the reception and transmission baud rates, the errors are accumulated up to the stop bit reception, which reduces the reception margin. The allowable baud rate error can be obtained by modifying the F in expression (1). When D = 0.5:

$$F = \{(15/32 - M)/(L - 0.5)\} \times 100 (\%) \dots\dots\dots \text{expression (3)}$$

By using expression (3), the relationship between the allowable error and reception margin with the frame length = 12 can be summarized as follows:

Allowed Error (%)	Reception Margin (%)
4.07	0
3.64	5
3.20	10
2.33	20
1.46	30

## 40.6 Baud Rate Generator for External Clock (BRG)

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

### 40.6.1 Overview

The SCIF incorporates a baud rate generator for external clock (abbreviated as BRG, hereafter). The BRG supplies a sampling clock (BRGCLK) to the SCIF core by dividing the external clock SC\_CLK (selectable between SCIF\_CLK and ZSφ) by  $1$  to  $2^{16} - 1$ . In addition, the BRG switches the output between the external clock SCK and divided clock.

Figure 40.25 shows a block diagram of the BRG.

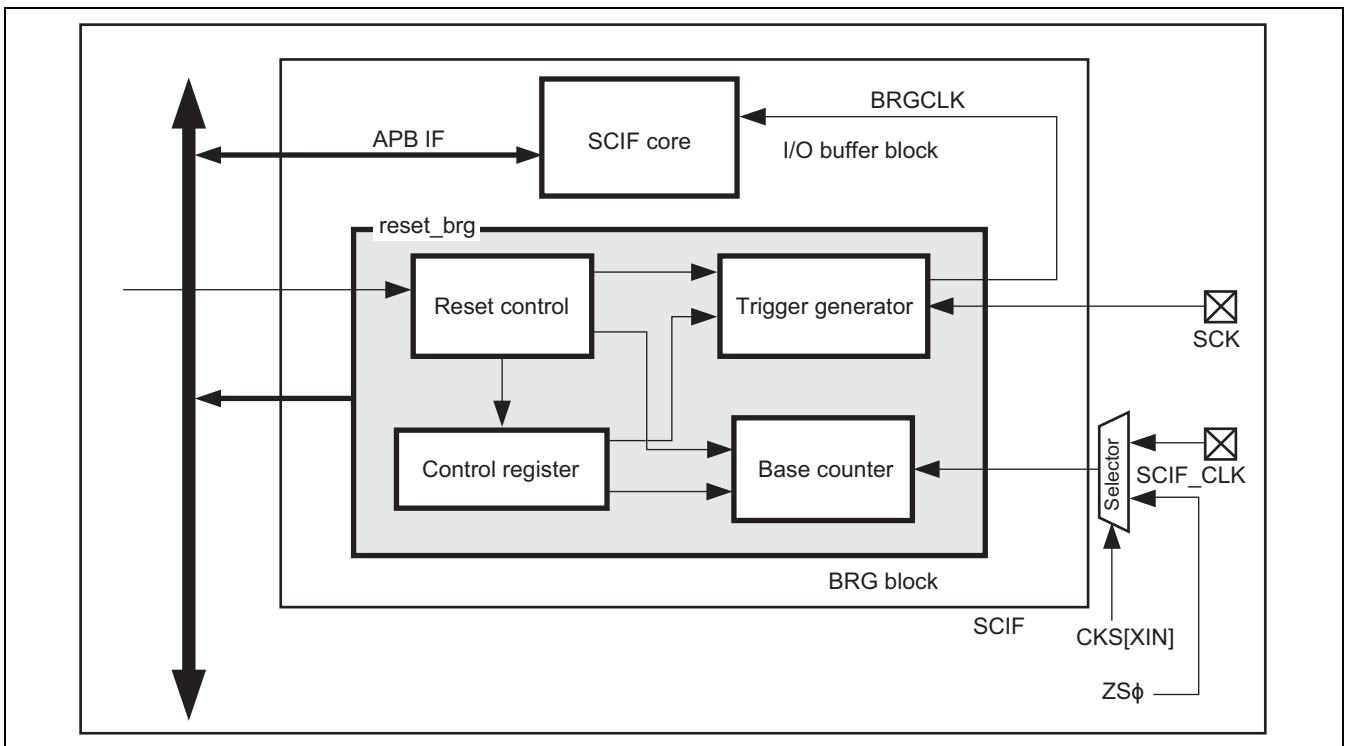


Figure 40.25 BRG Block Diagram

(1) Reset Controller:

The reset controller handles resetting the control register, base counter, and trigger generator.

(2) Control Register:

The control register has the frequency division register and clock select register.

(3) Base Counter:

The base counter is a 16-bit CLK synchronization counter that is used to determine the timing for generating a frequency divided clock.

(4) Trigger Generator:

The trigger generator generates rising-edge/falling-edge triggers for a frequency divided clock with the timing according to values of the frequency division register and base counter. The triggers are used to generate the frequency divided clock. In addition, the trigger generator switches the output between the SCK (external clock input) and frequency divided clock.

## 40.6.2 Register Configuration

Table 40.8 shows the registers in the BRG block.

**Table 40.8 List of Registers**

Name	Abbreviation	R/W	Initial Value	Relative Address	Access Size
Frequency division register	DL	R/W	H'0000	H'30	16
Clock select register	CKS	R/W	H'0000	H'34	16

### 40.6.2.1 Frequency Division Register (DL)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

This register specifies the value of frequency division for the frequency divided clock generated by the BRG.

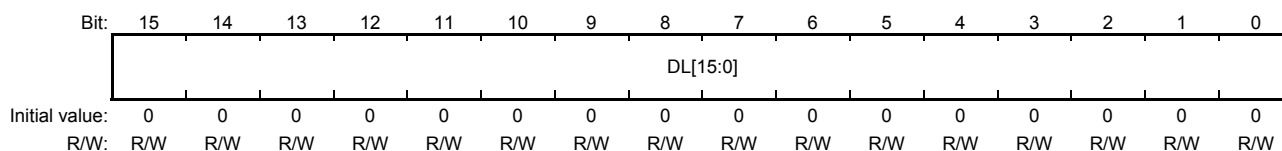
This register supports a 16-bit binary format that allows specifying a value in the range of 1 to 65535.

Setting all 0s in this register makes the BRG output the frequency divided clock at the low level.

The value of frequency division is given by the following formula:

The value of frequency division = (clock input frequency)/(required baud rate × 16)

Table 40.9 shows how to use the baud rate generator with a 3.6864-MHz crystal resonator.



Bit	Bit Name	Initial Value	R/W	Description
15 to 0	DL[15:0]	All 0	R/W	Specifies a division value of frequency clock generated in BRG. The value settings enabled in the range of 1 to 65535.

**Table 40.9 Baud Rate (3.6864-MHz clock)**

Baud Rate	Value of Frequency Division	Error Rate (*)
50	4608	—
75	3072	—
110	2095	-0.022
134.5	1713	0.001
150	1536	—
300	768	—
600	384	—
1200	192	—
1800	128	—
2000	115	0.174
2400	96	—
3600	64	—
4800	48	—
7200	32	—
9600	24	—
14400	16	—
19200	12	—
38400	6	—
76800	3	—
115200	2	—

Note: —: Indicates that the error rate is 0.



**40.6.2.2 Clock Select Register (CKS)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

This register switches the output between the frequency divided clock and specifies a source clock for the external baud rate.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CKS	XIN	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15	CKS	0	R/W	This bit switches the output between the frequency divided clock (SC_CLK) and external clock (SCK). 0: Selects the frequency divided clock. 1: Selects the external clock.
14	XIN	0	R/W	Selects the baud rate generator clock source for the external clock between SCIF_CLK and ZSφ. 0: Selects the external clock (SCIF_CLK). 1: Selects the internal clock (ZSφ).
13 to 0	All 0	0	R	Reserved These bits are always read as 0. Only 0 should be written to these bits.

### 40.6.3 Restrictions in BRG

#### (1) Notes on Setting Frequency Division Register

- For the initial setting of the register after a reset, at least one bit of waiting period is required to secure the clock stabilization time.

(Example) One bit period when DL = 2

$$3.68 \text{ (MHz)} \times 1/2 \times 1/16 = 0.115 \text{ (MHz)} \rightarrow 8695 \text{ (ns)}$$

- For modifying the register value after the setting stated in <1> above, at least one bit of waiting period at the maximum bit rate (DL = '65535') is required.

The SCIF registers and BRG registers should be set as the following table:

- Asynchronous mode (SC\_CLK external input)

SCIF		BRG	
Register Name	Setting Value	Register Name	Setting Value
SCSMR.C/A#	0	CKS	0000
SCSCR.CKE[1:0]	10	DL	1 to FFFF

- Asynchronous mode (SCK external input)

SCIF		BRG	
Register Name	Setting Value	Register Name	Setting Value
SCSMR.C/A#	0	CKS	8000
SCSCR.[1:0]	10	DL	Don't care

- Clock synchronous mode (external input)

SCIF		BRG	
Register Name	Setting Value	Register Name	Setting Value
SCSMR.C/A#	1	CKS	8000
SCSCR [1:0]	10	DL	Don't care

- The register settings for the baud rate generator for external clock should be made before starting initialization of the SCIF.

## 41. Serial Communications Interface with FIFO A (SCIFA)

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

This LSI has six serial communications interfaces A incorporating FIFO buffers (SCIFA) that can perform both asynchronous and clocked synchronous serial communications.

Each interface includes two 64-stage buffers, one for the transmit FIFO register, and one for the receive FIFO register, enabling fast, for efficient and continuous communications.

### 41.1 Features

- 6 channels are implemented.
- Asynchronous mode
 

Serial data communications is executed using an asynchronous system in which synchronization is achieved character by character. Serial data communications can be carried out with standard asynchronous communications chips such as a Universal Asynchronous Receiver/Transmitter (UART) or Asynchronous Communications Interface Adapter (ACIA).

There is a choice of 8 serial data communication formats.

  - Data length: 7 or 8 bits
  - Stop bit length: 1 or 2 bits
  - Parity: Even/odd/none
  - LSB-first transfer
  - Receive error detection: Parity, framing, and overrun errors
  - Break detection: If a framing error is followed by at least one frame at the space "0" (low level), a break is detected.
- Clocked synchronous mode
 

Serial data communications is synchronized with a clock. Serial data communications can be carried out with other LSIs that have a clocked synchronous communications function.

  - Data length: 8 bits
  - Receive error detection: Overrun errors
  - A rising or falling edge of a clock is selectable as the data transmit/receive timing.
- On-chip baud rate generator allows any bit rate to be selected.
  - Maximum:  $MP\phi/5$  bps, Minimum:  $MP\phi/(27 \times 256 \times 64)$  bps (asynchronous)
  - Maximum:  $MP\phi/(2 \times 2)$  bps, Minimum:  $MP\phi/(2 \times 256 \times 64)$  bps (clocked synchronous)
- Serial clock source: Internal clock signal generated by the baud rate generator.
- Seven interrupt sources
 

There are seven interrupt sources— transmit-data-stop, transmit-FIFO-data-empty, receive-FIFO-data-full, receive-error (framing/parity error), break-receive, and receive-data-ready interrupts. The vectors of each interrupt source are the same.
- The DMA controller (DMAC) can be activated to execute a data transfer in the event of a transmit-FIFO-data-empty, transmit-data-stop, or receive-FIFO-data-full interrupt. The DMAC requests of transmit-FIFO-data-empty and transmit-data-stop interrupts are the same.
- DMA multi-byte data transfer supported
- On-chip modem control functions (CTS# and RTS#) [RZ/G1H only]
- On-chip transmit-data-stop functions
- When not in use, SCIFA can be stopped by halting its clock supply to reduce power consumption.

- The amount of data in the transmit/receive FIFO registers, and the number of receive errors in the receive data in the receive FIFO register, can be ascertained.

Figures 41.1a and 41.1b are block diagrams of SCIFA.

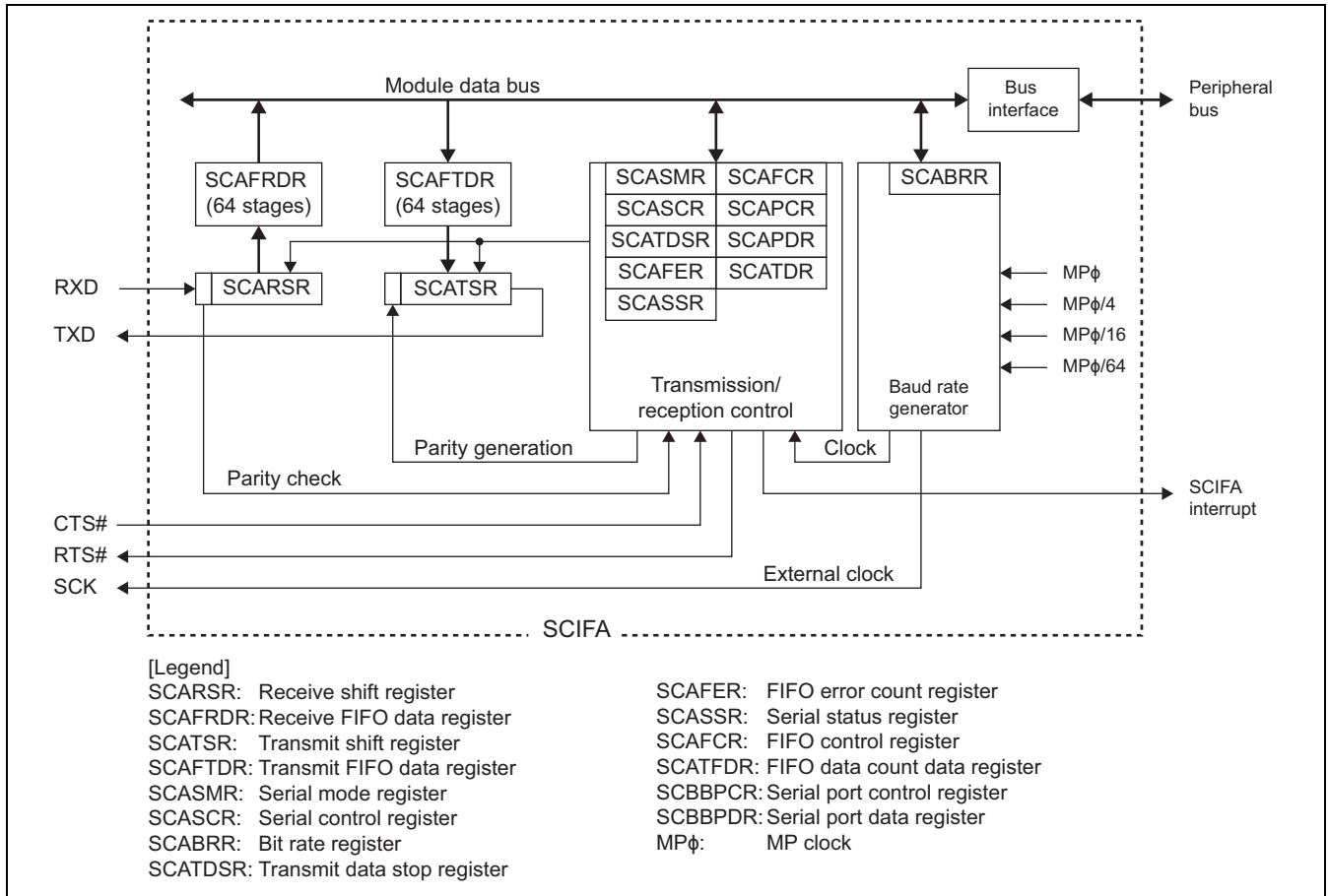


Figure 41.1a Block Diagram of SCIFA [RZ/G1H]

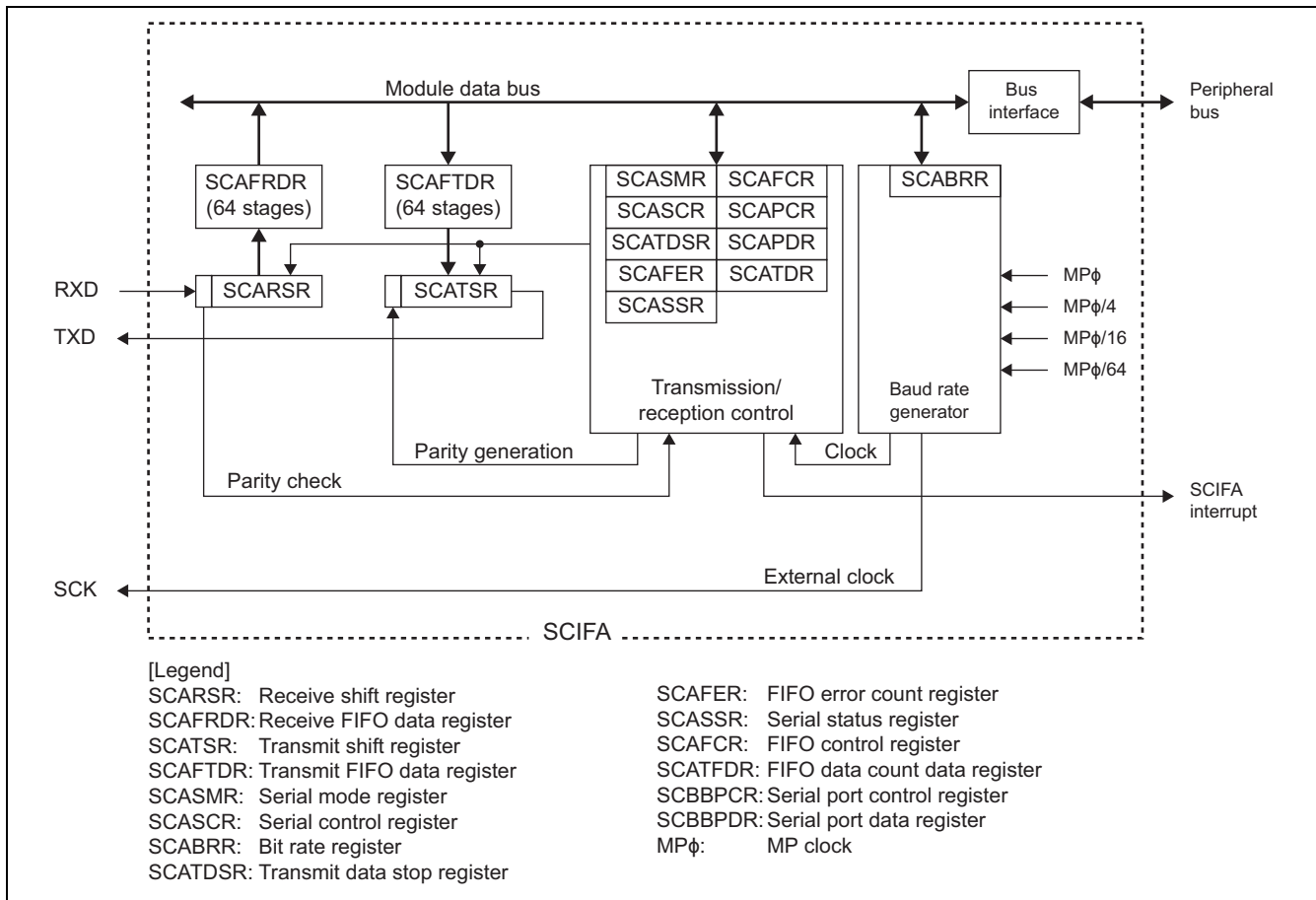


Figure 41.1b Block Diagram of SCIFA [RZ/G1M/N/E]

## 41.2 Input/Output Pins

Table 41.1 shows the SCIFA pin configuration.

**Table 41.1 Channel and Pin Configuration**

Pin Name	I/O	Function
SCIFAn_SCK	Output	Output pin for the clock signal n
SCIFAn_RXD	Input	Input pin for data for reception n
SCIFAn_TXD	Output	Output pin for data for transmission n
SCIFAn_CTS#	Input	Input pin for the transmit enable signal n [RZ/G1H only]
SCIFAn_RTS#	Output	Output pin for the transmit request signal n [RZ/G1H only]

Note: n is a channel number (n = 0 to 2 [RZ/G1H] / n = 0 to 5 [RZ/G1M/N/E]), and SCK, RXD, TXD, CTS#, and RTS# are used as generic terms in the following descriptions.

## 41.3 Register Descriptions

Table 41.2 shows the SCIFA registers. Table 41.3 shows the register states in the respective processing modes.

**Table 41.2 Register Configuration**

Register Name	Abbreviation		Address		RZ/G Series Products			
n: channel number			High order Address					
SCIFA0: 0			SCIFA0: H'E6C4					
SCIFA1: 1			SCIFA1: H'E6C5					
SCIFA2: 2			SCIFA2: H'E6C6					
SCIFA3: 3*3			SCIFA3: H'E6C7*3					
SCIFA4: 4*3			SCIFA4: H'E6C78*3	Access				
SCIFA5: 5*3		R/W	SCIFA5: H'E6C8*3	Size	RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Receive shift register An	SCARSRn	—*2	—	—	√	√	√	√
Transmit shift register An	SCATSRn	—*2	—	—	√	√	√	√
Serial mode register An	SCASMRn	R/W	H'xxxx 0000	16	√	√	√	√
Bit rate register An	SCABRRn	R/W	H'xxxx 0004	8	√	√	√	√
Serial control register An	SCASCRn	R/W	H'xxxx 0008	16	√	√	√	√
Transmit data stop register An	SCATDSRn	R/W	H'xxxx 000C	8	√	√	√	√
FIFO error count register An	SCAFERn	R	H'xxxx 0010	16	√	√	√	√
Serial status register An	SCASSRn	R/W*1	H'xxxx 0014	16	√	√	√	√
FIFO control register An	SCAFCRn	R/W	H'xxxx 0018	16	√	√	√	√
FIFO data count register An	SCAFDRn	R	H'xxxx 001C	16	√	√	√	√
Transmit FIFO data register An	SCAFTDRn	W	H'xxxx 0020	8	√	√	√	√
Receive FIFO data register An	SCAFRDRn	R	H'xxxx 0024	8	√	√	√	√
Serial port control register An	SCAPCRn	R/W	H'xxxx 0030	16	√	√	√	√
Serial port data register An	SCAPDRn	R/W	H'xxxx 0034	16	√	√	√	√

Notes: 1. To clear the flags, 0s can only be written to bits 9 to 7, 5, 4, 1, and 0.  
 2. These registers cannot be accessed by the CPU.  
 3. Only RZ/G1M, RZ/G1N and RZ/G1E.

**Table 41.3 Register States in Each Operating Mode**

<b>Abbreviation</b>	<b>Reset</b>	<b>Module Standby</b>
SCASMRn	Initialized	Retained
SCABRRn	Initialized	Retained
SCASCRn	Initialized	Retained
SCATDSRn	Initialized	Retained
SCAFERn	Initialized	Retained
SCASSRn	Initialized	Retained
SCAFCRn	Initialized	Retained
SCAFDRn	Initialized	Retained
SCAFTDRn	Undefined	Retained
SCAFRDRn	Undefined	Retained
SCAPCRn	Initialized	Retained
SCAPDRn	Undefined	Retained

n: Channel number (n = 0 to 2 [RZ/G1H] / n = 0 to 5 [RZ/G1M/N/E] )

### 41.3.1 Receive Shift Register An (SCARSRn)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SCARSR is the register used to receive serial data.

SCIFA sets serial data input from the RXD pin in SCARSR in the order received, starting with the LSB (bit 0), and converts it to parallel data. When one byte of data has been received, it is automatically transferred to SCAFRDR.

SCARSR cannot be directly read from or written to by the CPU.

### 41.3.2 Receive FIFO Data Register An (SCAFRDRn)

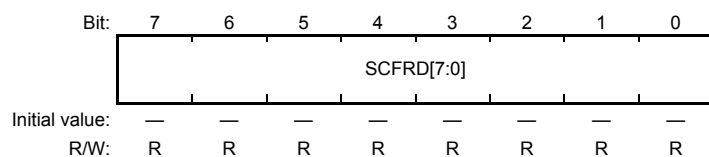
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SCAFRDR is a 64-stage FIFO register that stores received serial data.

When SCIFA has received one byte of serial data, it transfers the received data from SCARSR to SCAFRDR where it is stored, and completes the receive operation. SCARSR is then enabled for reception, and consecutive receive operations can be performed until SCAFRDR is full (64-character data).

SCAFRDR is a read-only register, and cannot be written to by the CPU.

If a read is performed when there is no receive data in SCAFRDR, an undefined value will be returned. When SCAFRDR is full of receive data, subsequent serial data is lost.



Bit	Bit Name	Initial Value	R/W	Description
7 to 0	SCFRD[7:0]	Undefined	R	Serial receive data FIFO

### 41.3.3 Transmit Shift Register An (SCATSRn)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SCATSR is the register used to transmit serial data.

To perform serial data transmission, SCIFA first transfers a transmit data from SCAFTDR to SCATSR, and then sends the data to the TXD pin starting with the LSB (bit 0).

When transmission of one byte is completed, the next transmit data is transferred from SCAFTDR to SCATSR, and transmission starts automatically.

SCATSR cannot be directly read from or written to by the CPU.



#### 41.3.4 Transmit FIFO Data Register An (SCAFTDRn)

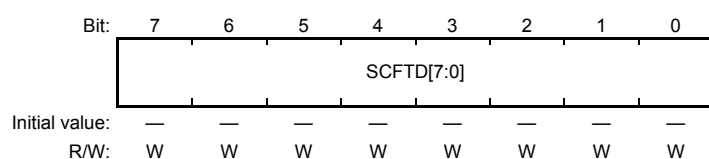
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SCAFTDR is an 8-bit 64-stage FIFO data register that stores data for serial transmission.

If SCATSr is empty when transmit data has been written to SCAFTDR, SCIFA transfers the transmit data written in SCAFTDR to SCATSr and starts serial transmission.

SCAFTDR is a write-only register, and cannot be read by the CPU.

The next data cannot be written when SCAFTDR is filled with 64 bytes of transmit data. Data written in this case is ignored.

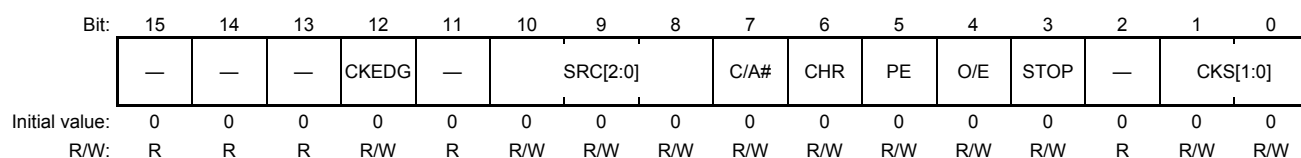


Bit	Bit Name	Initial Value	R/W	Description
7 to 0	SCFTD[7:0]	Undefined	W	Serial transmit data FIFO

#### 41.3.5 Serial Mode Register An (SCASMRn)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SCASMR is a 16-bit readable/writable register used to set an SCIFA's serial transfer format and select the baud rate generator clock source and the sampling rate.



Bit	Bit Name	Initial Value	R/W	Description
15 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12	CKEDG	0	R/W	Transmit/Receive Clock Edge Select Selects the clock edge at which the serial data is output in clocked synchronous mode. 0: Serial data is transmitted at the falling edge of output clock. Serial data is received at the rising edge of output clock. 1: Serial data is transmitted at the rising edge of output clock. Serial data is received at the falling edge of output clock.
11	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
10 to 8	SRC[2:0]	000	R/W	<p>Sampling Control</p> <p>This bit setting is valid only in asynchronous mode.</p> <p>These bits select the sampling rate.</p> <p>000: Sampling rate 1/16            001: Sampling rate 1/5*            010: Sampling rate 1/7            011: Sampling rate 1/11            100: Sampling rate 1/13            101: Sampling rate 1/17            110: Sampling rate 1/19            111: Sampling rate 1/27</p> <p>Note: * In asynchronous mode, when the sampling rate is 1/5, first received data may become invalid. To avoid this problem, wait more than 1 serial data time (1 bit time x serial data number) after setting SCASCR.RE = 1, or use sampling rate other than 1/5.</p>
7	C/A#	0	R/W	<p>Communication Mode</p> <p>Selects asynchronous mode or clocked synchronous mode as the SCIFA operating mode.</p> <p>0: Asynchronous mode            1: Clocked synchronous mode</p>
6	CHR	0	R/W	<p>Character Length</p> <p>This bit setting is valid only in asynchronous mode.</p> <p>Selects 7 or 8 bits as the data length.</p> <p>0: 8-bit data            1: 7-bit data*</p> <p>Note: * When the 7-bit character is selected, the MSB (bit 7) in SCAFTDR is not transmitted.</p>
5	PE	0	R/W	<p>Parity Enable</p> <p>This bit setting is valid only in asynchronous mode.</p> <p>Selects whether or not parity bit addition is performed in transmission, and parity bit checking in reception.</p> <p>0: Parity bit addition and checking disabled            1: Parity bit addition and checking enabled*</p> <p>Note: * When the PE bit is set to 1, the parity (even or odd) specified by the O/E bit is added to transmit data before transmission. In reception, the parity bit is checked for the parity (even or odd) specified by the O/E bit.</p>

Bit	Bit Name	Initial Value	R/W	Description
4	O/E	0	R/W	<p>Parity Mode</p> <p>This bit setting is valid only in asynchronous mode.</p> <p>Selects either even or odd parity for use in parity addition and checking. The O/E bit setting is only valid when the PE bit is set to 1, enabling parity bit addition and checking. The O/E bit setting is invalid when parity addition and checking are disabled.</p> <p>0: Even parity*1 1: Odd parity*2</p> <p>Notes: 1. When even parity is set, parity bit addition is performed in transmission so that the total number of 1-bits in the transmit character plus the parity bit is even. In reception, a check is performed to see if the total number of 1-bits in the receive character plus the parity bit is even.</p> <p>2. When odd parity is set, parity bit addition is performed in transmission so that the total number of 1-bits in the transmit character plus the parity bit is odd. In reception, a check is performed to see if the total number of 1-bits in the receive character plus the parity bit is odd.</p>
3	STOP	0	R/W	<p>Stop Bit Length</p> <p>This bit setting is valid only in asynchronous mode.</p> <p>Selects 1 or 2 bits as the stop bit length. In reception, only the first stop bit is checked, regardless of the STOP bit setting. If the second stop bit is 1, it is treated as a stop bit; if it is 0, it is treated as the start bit of the next transmit character.</p> <p>0: 1 stop bit*1 1: 2 stop bits*2</p> <p>Notes: 1. In transmission, a single logic-1 bit (stop bit) is added to the end of a transmit character before it is sent.</p> <p>2. In transmission, two logic-1 bits (stop bits) are added to the end of a transmit character before it is sent.</p>
2	—	0	R	<p>Reserved</p> <p>This bit is always read as 0. The write value should always be 0.</p>
1, 0	CKS[1:0]	00	R/W	<p>Clock Select</p> <p>These bits select the clock sources for the on-chip baud rate generator.</p> <p>00: MP<math>\phi</math> 01: MP<math>\phi</math>/4 10: MP<math>\phi</math>/16 11: MP<math>\phi</math>/64</p> <p>Note: MP<math>\phi</math>: MP clock</p>

### 41.3.6 Serial Control Register An (SCASCRn)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SCASCR is a 16-bit readable/writable register that enables or disables SCIFA transfer operations and interrupt requests, and selects the clock source for transmission and reception.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TDRQE	RDRQE	—	TENDE	TSIE	ERIE	BRIE	DRIE	TIE	RIE	TE	RE	—	—	—	CKE0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	TDRQE	0	R/W	Transmit Data Transfer Request Enable Switches the transmit-FIFO-data-empty interrupt or DMA transfer request when TIE = 1 and the transmit-FIFO-data-empty occurs. 0: Interrupt request to CPU is issued 1: Transmit data transfer request to DMAC is issued
14	RDRQE	0	R/W	Receive Data Transfer Request Enable Switches the receive-FIFO-data-full interrupt or DMA transfer request when RIE = 1 and the receive FIFO data full occurs. 0: Interrupt request to CPU is issued 1: Receive data transfer request to DMAC is issued
13	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
12	TENDE	0	R/W	Transmit End Interrupt Enable Enables or disables generation of a transmit-end interrupt when the TEND flag in SCASSR is set to 1. 0: Transmit-end interrupt disabled 1: Transmit-end interrupt enabled
11	TSIE	0	R/W	Transmit Data Stop Interrupt Enable Enables or disables generation of a transmit-data-stop interrupt when the TSE bit in SCAFCR is enabled and the TSF flag in SCASSR is set to 1. 0: Transmit-data-stop interrupt disabled* 1: Transmit-data-stop interrupt enabled Note: * The TDI interrupt request is cleared by clearing the TSF flag to 0 after reading 1 from it or clearing the TSIE bit to 0.
10	ERIE	0	R/W	Receive Error Interrupt Enable Enables or disables generation of a receive-error (framing or parity error) interrupt when the ER flag in SCASSR is set to 1. 0: Receive-error interrupt disabled* 1: Receive-error interrupt enabled Note: * The ERI interrupt request is cleared by clearing the ER flag to 0 after reading 1 from it or clearing the ERIE bit to 0.

Bit	Bit Name	Initial Value	R/W	Description
9	BRIE	0	R/W	<p>Break Interrupt Enable</p> <p>Enables or disables generation of a break-receive interrupt when the BRK flag in SCASSR is set to 1.</p> <p>0: Break-receive interrupt disabled*</p> <p>1: Break-receive interrupt enabled</p> <p>Note: * The BRI interrupt request is cleared by clearing the BRK flag to 0 after reading 1 from it or clearing the BRIE bit to 0.</p>
8	DRIE	0	R/W	<p>Receive Data Ready Interrupt Enable</p> <p>Enables or disables generation of a receive-data-ready interrupt when the DR flag in SCASSR is set to 1.</p> <p>0: Receive-data-ready interrupt disabled*</p> <p>1: Receive-data-ready interrupt enabled</p> <p>Note: * The DRI interrupt request is cleared by clearing the DR flag to 0 after reading 1 from it or clearing the DRIE bit to 0.</p>
7	TIE	0	R/W	<p>Transmit Interrupt Enable</p> <p>Enables or disables generation of a transmit-FIFO-data-empty interrupt request when the TDFE flag in SCASSR is set to 1.</p> <p>0: Transmit-FIFO-data-empty interrupt request disabled*</p> <p>1: Transmit-FIFO-data-empty interrupt request enabled</p> <p>Note: * Interrupt requests can be cleared by writing transmit data exceeding the transmit trigger set number to SCAFTDR, reading 1 from the TDFE flag, then clearing it to 0, or by clearing the TIE bit to 0.</p>
6	RIE	0	R/W	<p>Receive Interrupt Enable</p> <p>Enables or disables generation of a receive-FIFO-data-full interrupt request when the RDF flag in SCASSR is set to 1.</p> <p>0: Receive-FIFO-data-full interrupt request disabled*</p> <p>1: Receive-FIFO-data-full interrupt request enabled</p> <p>Note: * Interrupt requests can be cleared by reading 1 from the RDF flag, then clearing the flag to 0, or by clearing the RIE bit to 0.</p>
5	TE	0	R/W	<p>Transmit Enable</p> <p>Enables or disables the start of serial transmission by SCIFA.</p> <p>0: Transmission disabled</p> <p>1: Transmission enabled*</p> <p>Note: * SCASMR and SCAFCR settings must be made, the transmit format decided, and the transmit FIFO reset, before the TE bit is set to 1.</p>
4	RE	0	R/W	<p>Receive Enable</p> <p>Enables or disables the start of serial reception by SCIFA.</p> <p>0: Reception disabled*<sup>1</sup></p> <p>1: Reception enabled*<sup>2</sup></p> <p>Notes: 1. Clearing the RE bit to 0 does not affect the DR, ER, BRK, RDF, FER, PER, and ORER flags, which retain their state.</p> <p>2. Serial mode register (SCASMR) and FIFO control register (SACFCR) settings must be made, the receive format decided, and the receive FIFO reset, before the RE bit is set to 1.</p>
3 to 1	—	All 0	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>

Bit	Bit Name	Initial Value	R/W	Description
0	CKE0	0	R/W	<p>Clock Enable</p> <p>Enables or disables the clock output from the SCK pin. The CKE0 bit must be set before determining the SCIFA operating mode with SCASMR.</p> <p>0: SCK pin disabled SCK pin state is Hi-Z.*<sup>1</sup></p> <p>1: Clock output from SCK*<sup>2</sup></p> <p>Notes: 1. Even if this bit is 0, the SCK pin outputs data specified by SCAPDRn[2].SCKD, if SCAPCRn[2].SCKC is 1.</p> <p>2. In clocked synchronous mode, outputs a clock with the same frequency as the bit rate.</p>

### 41.3.7 FIFO Error Count Register An (SCAFERn)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SCAFER is a 16-bit read-only register that indicates the number of receive errors (framing errors and parity errors)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	—	—	PER[5:0]					—	—	FER[5:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15, 14	—	All 0	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>
13 to 8	PER[5:0]	000000	R	<p>Parity Error Count</p> <p>These bits indicate the number of data in which parity errors are generated, in receive data stored in SCAFRDR.</p> <p>After the ER bit in SCASSR is set, the value of bits PER5 to PER0 indicates the number of data in which parity errors are generated.</p> <p>When all 64 bytes of receive data in SCAFRDR have parity errors, these bits indicate 0.</p>
7, 6	—	All 0	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>
5 to 0	FER[5:0]	000000	R	<p>Framing Error Count</p> <p>These bits indicate the number of data in which framing errors are generated, in receive data stored in SCAFRDR.</p> <p>After the ER bit in SCASSR is set, the value of bits FER5 to FER0 indicates the number of data in which framing errors are generated.</p> <p>When all 64 bytes of receive data in SCAFRDR have framing errors, these bits indicate 0.</p>

### 41.3.8 Serial Status Register An (SCASSRn)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SCASSR is a 16-bit readable/writable register that indicates the SCIFA status.

However, 1 cannot be written to the ORER, TSF, ER, TDFE, BRK, RDF, and DR flags. Also note that in order to clear these flags to 0, they must be read as 1 beforehand. The TEND, FER, and PER flags are read-only flags and cannot be modified.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	ORER	TSF	ER	TEND	TDFE	BRK	FER	PER	RDF	DR
Initial value:	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/(W)*	R/(W)*	R/(W)*	R	R/(W)*	R/(W)*	R	R	R/(W)*	R/(W)*

Bit	Bit Name	Initial Value	R/W	Description
15 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9	ORER	0	R/(W)*	<p>Overrun Error</p> <p>Indicates that an overrun error occurred during reception.</p> <p>This bit setting is valid only in asynchronous mode.</p> <p>0: Reception in progress, or reception has ended normally*<sup>1</sup></p> <p>[Clearing conditions]</p> <ul style="list-style-type: none"> <li>Power-on reset or manual reset</li> <li>When 0 is written to ORER after reading ORER = 1</li> </ul> <p>1: An overrun error occurred during reception*<sup>2</sup></p> <p>[Setting condition]</p> <ul style="list-style-type: none"> <li>When serial reception is completed while receive FIFO is full</li> </ul> <p>Notes: 1. The ORER flag is not affected and retains its previous state when the RE bit in SCASCR is cleared to 0.</p> <p>2. The receive data prior to the overrun error is retained in SCAFRDR, and the data received subsequently is lost. Serial reception cannot be continued while the ORER flag is set to 1.</p>
8	TSF	0	R/(W)*	<p>Transmit Data Stop</p> <p>Indicates that the number of transmit data matches the value of SCATDSR.</p> <p>This bit setting is valid only in asynchronous mode.</p> <p>0: Number of transmit data does not match value of SCATDSR</p> <p>[Clearing conditions]</p> <ul style="list-style-type: none"> <li>Power-on reset or manual reset</li> <li>When 0 is written to TSF after reading TSF = 1</li> </ul> <p>1: Number of transmit data matches value of SCATDSR</p>

Bit	Bit Name	Initial Value	R/W	Description
7	ER	0	R/(W)*	<p>Receive Error</p> <p>Indicates that a framing error or parity error occurred during reception.*<sup>1</sup></p> <p>This bit setting is valid only in asynchronous mode.</p> <p>0: No framing error or parity error occurred during reception [Clearing conditions]</p> <ul style="list-style-type: none"> <li>Power-on reset or manual reset</li> <li>When 0 is written to ER after reading ER = 1</li> </ul> <p>1: A framing error or parity error occurred during reception [Setting conditions]</p> <ul style="list-style-type: none"> <li>When SCIFA checks whether the stop bit at the end of the receive data is 1 when reception ends, and the stop bit is 0*<sup>2</sup></li> <li>When, in reception, the number of logic-1 bits in the receive data and in the parity bit does not match the parity setting (even or odd) specified by the O/E bit in SCASMR</li> </ul> <p>Notes: 1. The ER flag is not affected and retains its previous state when the RE bit in SCASCR is cleared to 0. When a receive error occurs, the receive data is still transferred to SCAFRDR, and reception continues. The FER and PER bits in SCASSR can be used to determine whether there is a receive error in the data read from SCAFRDR.</p> <p>2. When the stop length is 2 bits, only the first stop bit is checked for a value of 1; the second stop bit is not checked.</p>
6	TEND	1	R	<p>Transmit End</p> <p>Indicates that there is no valid data in SCAFTDR when the last bit of the transmit character is sent, and transmission has been ended.</p> <p>0: Transmission is in progress [Clearing condition]</p> <ul style="list-style-type: none"> <li>When data is written to SCAFTDR</li> </ul> <p>1: Transmission has been ended [Setting condition]</p> <ul style="list-style-type: none"> <li>When there is no transmit data in SCAFTDR on transmission of a 1-byte serial transmit character</li> </ul>



Bit	Bit Name	Initial Value	R/W	Description
5	TDFE	1	R/(W)*	<p>Transmit FIFO Data Empty</p> <p>Indicates that data has been transferred from SCAFTDR to SCATSR, the number of data bytes in SCAFTDR has fallen to or below the transmit trigger data number set by bits TTRG[1:0] in SCAFCR, and new transmit data can be written to SCAFTDR.</p> <p>0: A number of transmit data bytes exceeding the transmit trigger set number have been written to SCAFTDR</p> <p>[Clearing condition]</p> <ul style="list-style-type: none"> <li>When transmit data exceeding the transmit trigger set number is written to SCAFTDR, and 0 is written to TDFE after reading TDFE = 1</li> </ul> <p>1: The number of transmit data bytes in SCAFTDR does not exceed the transmit trigger set number</p> <p>[Setting conditions]</p> <ul style="list-style-type: none"> <li>Power-on reset or manual reset</li> <li>When the number of SCAFTDR transmit data bytes falls to or below the transmit trigger set number as the result of a transmit operation*</li> </ul> <p>Note: * As SCAFTDR is a 64-byte FIFO register, the maximum number of bytes that can be written when TDFE = 1 is 64 – (transmit trigger set number). Data written in excess of this will be ignored. The number of data bytes in SCAFTDR is indicated by SCAFRDR.</p>
4	BRK	0	R/(W)*	<p>Break Detect</p> <p>Indicates that a receive data break signal has been detected. This bit setting is valid only in asynchronous mode.</p> <p>0: A break signal has not been received</p> <p>[Clearing conditions]</p> <ul style="list-style-type: none"> <li>Power-on reset or manual reset</li> <li>When 0 is written to BRK after reading BRK = 1</li> </ul> <p>1: A break signal has been received*</p> <p>[Setting condition]</p> <ul style="list-style-type: none"> <li>When data with a framing error is received, followed by the space 0 level (low level) for at least one frame length</li> </ul> <p>Note: * When a break is detected, the receive data (H'00) following detection is not transferred to SCAFRDR. When the break ends and the receive signal returns to mark 1, receive data transfer is resumed.</p>

Bit	Bit Name	Initial Value	R/W	Description
3	FER	0	R	<p>Framing Error</p> <p>Indicates a framing error in the data read from SCAFRDR. This bit setting is valid only in asynchronous mode.</p> <p>0: There is no framing error in the receive data read from SCAFRDR</p> <p>[Clearing conditions]</p> <ul style="list-style-type: none"> <li>Power-on reset or manual reset</li> <li>When there is no framing error in SCAFRDR read data</li> </ul> <p>1: There is a framing error in the receive data read from SCAFRDR</p> <p>[Setting condition]</p> <ul style="list-style-type: none"> <li>When there is a framing error in SCAFRDR read data</li> </ul>
2	PER	0	R	<p>Parity Error</p> <p>Indicates a parity error in the data read from SCAFRDR. This bit setting is valid only in asynchronous mode.</p> <p>0: There is no parity error in the receive data read from SCAFRDR</p> <p>[Clearing conditions]</p> <ul style="list-style-type: none"> <li>Power-on reset or manual reset</li> <li>When there is no parity error in SCAFRDR read data</li> </ul> <p>1: There is a parity error in the receive data read from SCAFRDR</p> <p>[Setting condition]</p> <ul style="list-style-type: none"> <li>When there is a parity error in SCAFRDR read data</li> </ul>
1	RDF	0	R/(W)*	<p>Receive FIFO Data Full</p> <p>Indicates that the received data has been transferred from SCARSR to SCAFRDR, and the number of receive data bytes in SCAFRDR is equal to or greater than the receive trigger number set by bits RTRG[1:0] in SCAFCR.</p> <p>0: The number of receive data bytes in SCAFRDR is less than the receive trigger set number</p> <p>[Clearing conditions]</p> <ul style="list-style-type: none"> <li>Power-on reset or manual reset</li> <li>When SCAFRDR is read until the number of receive data bytes in SCAFRDR falls below the receive trigger set number, and 0 is written to RDF after reading RDF = 1</li> </ul> <p>1: The number of receive data bytes in SCAFRDR is equal to or greater than the receive trigger set number</p> <p>[Setting condition]</p> <ul style="list-style-type: none"> <li>When SCAFRDR contains at least the receive trigger set number of receive data bytes*</li> </ul> <p>Note: * SCAFRDR is a 64-byte FIFO register. When RDF = 1, at least the receive trigger set number of data bytes can be read. If data is read when SCAFRDR is empty, an undefined value will be returned. The number of receive data bytes in SCAFRDR is indicated by the lower bits of SCAFRDR.</p>

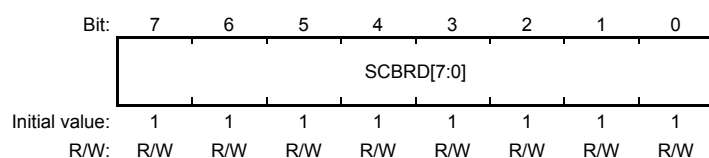
Bit	Bit Name	Initial Value	R/W	Description
0	DR	0	R/(W)*	<p>Receive Data Ready</p> <p>Indicates that there are data bytes fewer than the receive trigger set number in SCAFRDR, and no further data will arrive at least 15 etu after the stop bit of the last data received.</p> <p>This bit setting is valid only in asynchronous mode.</p> <p>0: Reception is in progress or has ended normally and there is no receive data left in SCAFRDR</p> <p>[Clearing conditions]</p> <ul style="list-style-type: none"> <li>• Power-on reset or manual reset</li> <li>• When all the receive data in SCAFRDR has been read, and 0 is written to DR after reading DR = 1</li> </ul> <p>1: No further receive data has arrived</p> <p>[Setting condition]</p> <ul style="list-style-type: none"> <li>• When SCAFRDR contains data bytes fewer than the receive trigger set number, and no further data will arrive at least 15 etu after the stop bit of the last data received*</li> </ul> <p>Note: * Corresponds to 1.5 frame time in 8-bit one-stop-bit format. etu: Elementary time unit (time for transfer of 1 bit)</p>

Note: \* Only 0 can be written for clearing the flags.

### 41.3.9 Bit Rate Register An (SCABRRn)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SCABRR is an 8-bit readable/writable register that sets the serial transfer bit rate in accordance with the baud rate generator operating clock selected by bits CKS[1:0] in SCASMR.



Bit	Bit Name	Initial Value	R/W	Description
7 to 0	SCBRD[7:0]	H'FF	R/W	Bit Rate $0 \leq \text{SCBRD} \leq 255$ (asynchronous mode) $1 \leq \text{SCBRD} \leq 255$ (clocked synchronous mode)

The SCABRR setting is found by using the following equations.

#### (1) Asynchronous Mode:

When the sampling rate is 1/16,

$$N = \{ \text{MP}\phi / (16 \times 2^{2n} \times B) \} \times 10^6 - 1$$

When the sampling rate is 1/5,

$$N = \{ \text{MP}\phi / (5 \times 2^{2n} \times B) \} \times 10^6 - 1$$

When the sampling rate is 1/11,

$$N = \{ \text{MP}\phi / (11 \times 2^{2n} \times B) \} \times 10^6 - 1$$

When the sampling rate is 1/13,

$$N = \{ \text{MP}\phi / (13 \times 2^{2n} \times B) \} \times 10^6 - 1$$

When the sampling rate is 1/27,

$$N = \{ \text{MP}\phi / (27 \times 2^{2n} \times B) \} \times 10^6 - 1$$

#### (2) Clocked Synchronous Mode:

$$N = \{ \text{MP}\phi / (2 \times 2^{2n} \times B) \} \times 10^6 - 1$$

Where B: Bit rate (bits/s)

N: SCABRR setting for baud rate generator  
 Asynchronous mode ( $0 \leq N \leq 255$ )  
 Clocked synchronous mode ( $1 \leq N \leq 255$ )

MP $\phi$ : Mp clock frequency (MHz)

n: Baud rate generator input clock ( $n = 0$  to 3)  
 (See the table below for the relation between n and the clock.)

**Table 41.4 SCASMR Settings**

n	Clock	SCASMR Setting
		CKS[1:0]
0	MP $\phi$	B'00
1	MP $\phi$ /4	B'01
2	MP $\phi$ /16	B'10
3	MP $\phi$ /64	B'11

The bit rate error in asynchronous mode is found by using the following equations.

When the sampling rate is 1/16,

$$\text{Error (\%)} = \{ \{ \text{MP}\phi / ((N + 1) \times 16 \times 2^{2n} \times B) \} \times 10^6 - 1 \} \times 100$$

When the sampling rate is 1/5,

$$\text{Error (\%)} = \{ \{ \text{MP}\phi / ((N + 1) \times 5 \times 2^{2n} \times B) \} \times 10^6 - 1 \} \times 100$$

When the sampling rate is 1/11,

$$\text{Error (\%)} = \{ \{ \text{MP}\phi / ((N + 1) \times 11 \times 2^{2n} \times B) \} \times 10^6 - 1 \} \times 100$$

When the sampling rate is 1/13,

$$\text{Error (\%)} = \{ \{ \text{MP}\phi / ((N + 1) \times 13 \times 2^{2n} \times B) \} \times 10^6 - 1 \} \times 100$$

When the sampling rate is 1/27,

$$\text{Error (\%)} = \{ \{ \text{MP}\phi / ((N + 1) \times 27 \times 2^{2n} \times B) \} \times 10^6 - 1 \} \times 100$$

### 41.3.10 FIFO Control Register An (SCAFCRn)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SCAFCR is a 16-bit readable/writable register that clears all data and sets the trigger data number for the transmit and receive FIFO registers, and also contains a loopback test enable bit.

[RZ/G1H]

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TSE	TCRST	—	—	—	RSTRG[2:0]		RTRG[1:0]		TTRG[1:0]		MCE	TFRST	RFRST	LOOP	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[RZ/G1M/N/E]

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TSE	TCRST	—	—	—	—	—	—	RTRG[1:0]		TTRG[1:0]		—	TFRST	RFRST	LOOP
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	TSE	0	R/W	Transmit Data Stop Enable Enables or disables the transmit data stop function. 0: Transmit data stop function disabled 1: Transmit data stop function enabled
14	TCRST	0	R/W	Transmit Count Reset Clears the transmit count to 0. This bit is valid only when the transmit data stop function is used. 0: Transmit count reset disabled* 1: Transmit count reset enabled (clearing to 0) Note: * Transmit count reset (clearing to 0) is performed at a power-on reset or module reset.
13 to 11	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
10 to 8	RSTRG[2:0]	000	R/W	<p>RTS# Output Active Trigger [RZ/G1H]</p> <p>The setting is valid only in asynchronous mode.</p> <p>The RTS# signal becomes high when the number of receive data stored in SCAFRDR reaches the trigger number shown below.</p> <p>000: 63 001: 1 010: 8 011: 16 100: 32 101: 48 110: 54 111: 60</p>
—	—	All 0	R	<p>Reserved [RZ/G1M/N/E]</p> <p>These bits are always read as 0. The write value should always be 0.</p>
7, 6	RTRG[1:0]	00	R/W	<p>Receive FIFO Data Number Trigger</p> <p>Set the number of receive data bytes that sets the RDF flag in SCASSR.</p> <p>The RDF flag is set when the number of receive data bytes in SCAFRDR is equal to or greater than the trigger set number shown below.</p> <p>00: 1 01: 16 10: 32 11: 48</p>
5, 4	TTRG[1:0]	00	R/W	<p>Transmit FIFO Data Number Trigger</p> <p>Set the number of remaining transmit data bytes that sets the TDFE flag in SCASSR.</p> <p>The TDFE flag is set when, as the result of a transmit operation, the number of transmit data bytes in SCAFTDR falls to or below the trigger set number shown below.</p> <p>00: 32 (32) 01: 16 (48) 10: 2 (62) 11: 0 (64)</p> <p>Note: The values in parentheses are the number of empty bytes in SCAFTDR when the flag is set.</p>
3	MCE	0	R/W	<p>Modem Control Enable [RZ/G1H]</p> <p>This bit setting is valid only in asynchronous mode.</p> <p>Enables the CTS# and RTS# modem control signals.</p> <p>0: Modem signals disabled* 1: Modem signals enabled</p> <p>Note: * CTS# is fixed at active low regardless of the input value, and RTS# output is also fixed at 0.</p>
—	—	0	R	<p>Reserved [RZ/G1M/N/E]</p> <p>This bit is always read as 0. The write value should always be 0.</p>

Bit	Bit Name	Initial Value	R/W	Description
2	TFRST	0	R/W	<p>Transmit FIFO Data Register Reset</p> <p>Invalidates the transmit data in SCAFTDR and resets it to the empty state.</p> <p>0: Reset operation disabled*</p> <p>1: Reset operation enabled</p> <p>Note: * A reset operation is performed at a power-on reset or manual reset.</p>
1	RFRST	0	R/W	<p>Receive FIFO Data Register Reset</p> <p>Invalidates the receive data in SCAFRDR and resets it to the empty state.</p> <p>0: Reset operation disabled*</p> <p>1: Reset operation enabled</p> <p>Note: * A reset operation is performed in the event of a power-on reset or manual reset.</p>
0	LOOP	0	R/W	<p>Loopback Test</p> <p>Internally connects the transmit output pin (TXD) to receive input pin (RXD) and RTS#* pin to CTS#* pin, enabling loopback testing.</p> <p>0: Loopback test disabled</p> <p>1: Loopback test enabled</p> <p>Note: * Only RZ/G1H is valid.</p>



### 41.3.11 FIFO Data Count Register An (SCAFDRn)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SCAFDR is a 16-bit read-only register that indicates the number of data bytes stored in SCAFTDR and SCAFRDR. The T6 to T0 bits show the number of transmit data bytes in SCAFTDR, and the R6 to R0 bits show the number of receive data bytes in SCAFRDR.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—		T[6:0]						—		R[6:0]					
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
14 to 8	T[6:0]	H'00	R	These bits show the number of untransmitted data bytes in SCAFTDR. A value of H'00 means that there is no transmit data, and a value of H'40 means that SCAFTDR is full of transmit data.
7	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
6 to 0	R[6:0]	H'00	R	These bits show the number of receive data bytes in SCAFRDR. A value of H'00 means that there is no receive data, and a value of H'40 means that SCAFRDR is full of receive data.

### 41.3.12 Transmit Data Stop Register An (SCATDSRn)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SCATDSR is an 8-bit readable/writable register that sets the number of transmit data bytes. SCATDSR is valid only when the TSE bit in SCAFCR is enabled. Transmit operation is stopped when the number of data bytes set in SCATDSR is transmitted. The setting value should be H'00 (one byte) to H'FF (256 bytes).

Bit:	7	6	5	4	3	2	1	0
	TDSRD[7:0]							
Initial value:	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7 to 0	TDSRD[7:0]	H'FF	R/W	Transmit Data Stop Setting

### 41.3.13 Serial Port Control Register An (SCAPCRn)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SCAPCR is a 16-bit readable/writable register. This register specifies whether the TXD, SCK and RTS#\* pins function as output ports or as the TXD, SCK and RTS#\* pins, respectively. It also specifies whether the RXD and CTS#\* pin functions as an input port or the RXD and CTS#\* pins, respectively.

This register function is valid only when the SCIFA pin function is selected through the pin function controller (PFC).

Note: \* Only RZ/G1H is valid.

[RZ/G1H]

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	RTSC	CTSC	SCKC	RXDC	TXDC
Initial value:	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W

[RZ/G1M/N/E]

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	SCKC	RXDC	TXDC
Initial value:	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	RTSC	1	R/W	Selects the RTS# pin function. [RZ/G1H] 0: The RTS# pin functions as the RTS# pin. 1: The RTS# pin functions as an output port.
	—	1	R	Reserved [RZ/G1M/N/E] This bit is always read as 1. The write value should always be 1.
3	CTSC	0	R/W	Selects the CTS# pin function. [RZ/G1H] 0: The CTS# pin functions as the CTS# pin. 1: The CTS# pin functions as an input port.
	—	1	R	Reserved [RZ/G1M/N/E] This bit is always read as 1. The write value should always be 1.
2	SCKC	1	R/W	Selects the SCK pin function. 0: The SCK pin functions as the SCK pin. 1: The SCK pin functions as an output port.
1	RXDC	0	R/W	Selects the RXD pin function. 0: The RXD pin functions as the RXD pin. 1: The RXD pin functions as an input port.

---

<b>Bit</b>	<b>Bit Name</b>	<b>Initial Value</b>	<b>R/W</b>	<b>Description</b>
0	TXDC	0	R/W	Selects the TXD pin function. 0: The TXD pin functions as the TXD pin. 1: The TXD pin functions as an output port.

---

### 41.3.14 Serial Port Data Register An (SCAPDRn)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SCAPDR is a 16-bit readable/writable register. This register specifies data output to the TXD, SCK and RTS#\* pins when the SCIFA pin function is selected by SCAPCR. It also specifies the pin level of the RXD and CTS#\* pins.

This register function is valid only when the SCIFA pin function is selected through the pin function controller (PFC).

Note: \* Only RZ/G1H is valid.

[RZ/G1H]

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	RTSD	CTSD	SCKD	RXDD	TXDD
Initial value:	0	0	0	0	0	0	0	0	0	0	0	1	—	0	—	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R/W	R	R/W

[RZ/G1M/N/E]

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	SCKD	RXDD	TXDD
Initial value:	0	0	0	0	0	0	0	0	0	0	0	1	1	0	—	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	RTSD	1	R/W	Specifies data output to the RTS# pin. [RZ/G1H] 0: Outputs 0. 1: Outputs 1.
	—	1	R	Reserved [RZ/G1M/N/E] This bit is always read as 1. The write value should always be 1.
3	CTSD	Undefined	R	Specifies the CTS# pin level. [RZ/G1H] 0: CTS# pin level is 0. 1: CTS# pin level is 1. This bit is valid only when SCAFCRn[3].MCE is 1, or SCAPCRn[3].CTSC is 1.
	—	1	R	Reserved [RZ/G1M/N/E] This bit is always read as 1. The write value should always be 1.
2	SCKD	0	R/W	Specifies data output to the SCK pin. 0: Outputs 0. 1: Outputs 1.

<b>Bit</b>	<b>Bit Name</b>	<b>Initial Value</b>	<b>R/W</b>	<b>Description</b>
1	RXDD	Undefined	R	Specifies the RXD pin level. 0: RXD pin level is 0. 1: RXD pin level is 1.
0	TXDD	0	R/W	Specifies data output to the TXD pin. 0: Outputs 0. 1: Outputs 1.

## 41.4 Operation

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

### 41.4.1 Overview

SCIFA supports serial communications in asynchronous mode, in which synchronization is achieved character by character, and in clocked synchronous mode, in which synchronization is achieved with clock pulses. 64-stage FIFO buffers are provided for both transmission and reception, reducing the CPU overhead and enabling high-speed continuous communications.

### 41.4.2 Asynchronous Mode

In the asynchronous mode, the transfer format is selected by the setting in SCASMR as shown in Table 41.5. Features in this mode are as follows.

- Data length: 7 or 8 bits
- The addition of parity (even, odd or none) and the choice of stop-bit length (1 or 2 bits), along with the data length, determine the transfer format and character length.
- Receive error detection: Framing, parity, and overrun errors, receive-FIFO-data-full, receive-data-ready, and breaks.
- Independent indications of the number of data stored in the registers of transmit and receive FIFOs.
- Clock source: Internal clock signal generated by the baud-rate generator.

**Table 41.5 SCASMR Settings for Serial Transfer Format Selection**

SCASMR Settings				Mode	SCIFA Transfer Format		
Bit 7: C/A#	Bit 6: CHR	Bit 5: PE	Bit 3: STOP		Data Length	Parity Bit	Stop Bit Length
0	0	0	0	Asynchronous mode	8-bit data	No	1 bit
			1				2 bits
		1	0			Yes	1 bit
			1			2 bits	
	1	0	0		7-bit data	No	1 bit
			1				2 bits
		1	0			Yes	1 bit
			1			2 bits	
1	*	*	*	Clocked synchronous mode	8-bit data	No	No

Note: \* Don't care.

### 41.4.3 Serial Operation in Asynchronous Mode

#### (1) Data Transfer Format

Table 41.6 shows the transfer formats that can be used in asynchronous mode. Any of eight transfer formats can be selected according to the SCASMR settings.

**Table 41.6 Serial Transfer Formats**

SCASMR Settings			Serial Transfer Format and Frame Length												
CHR	PE	STOP	1	2	3	4	5	6	7	8	9	10	11	12	
0	0	0	S	8-bit data							STOP				
		1	S	8-bit data							STOP	STOP			
	1	0	S	8-bit data							P	STOP			
		1	S	8-bit data							P	STOP	STOP		
1	0	0	S	7-bit data						STOP					
		1	S	7-bit data						STOP	STOP				
	1	0	S	7-bit data						P	STOP				
		1	S	7-bit data						P	STOP	STOP			

[Legend]

S: Start bit

STOP: Stop bit

P: Parity bit

#### (2) Clock

An internal clock signal generated by the on-chip baud rate generator provides the transfer clock for SCIFA.

**(3) Data Transfer Operations:**

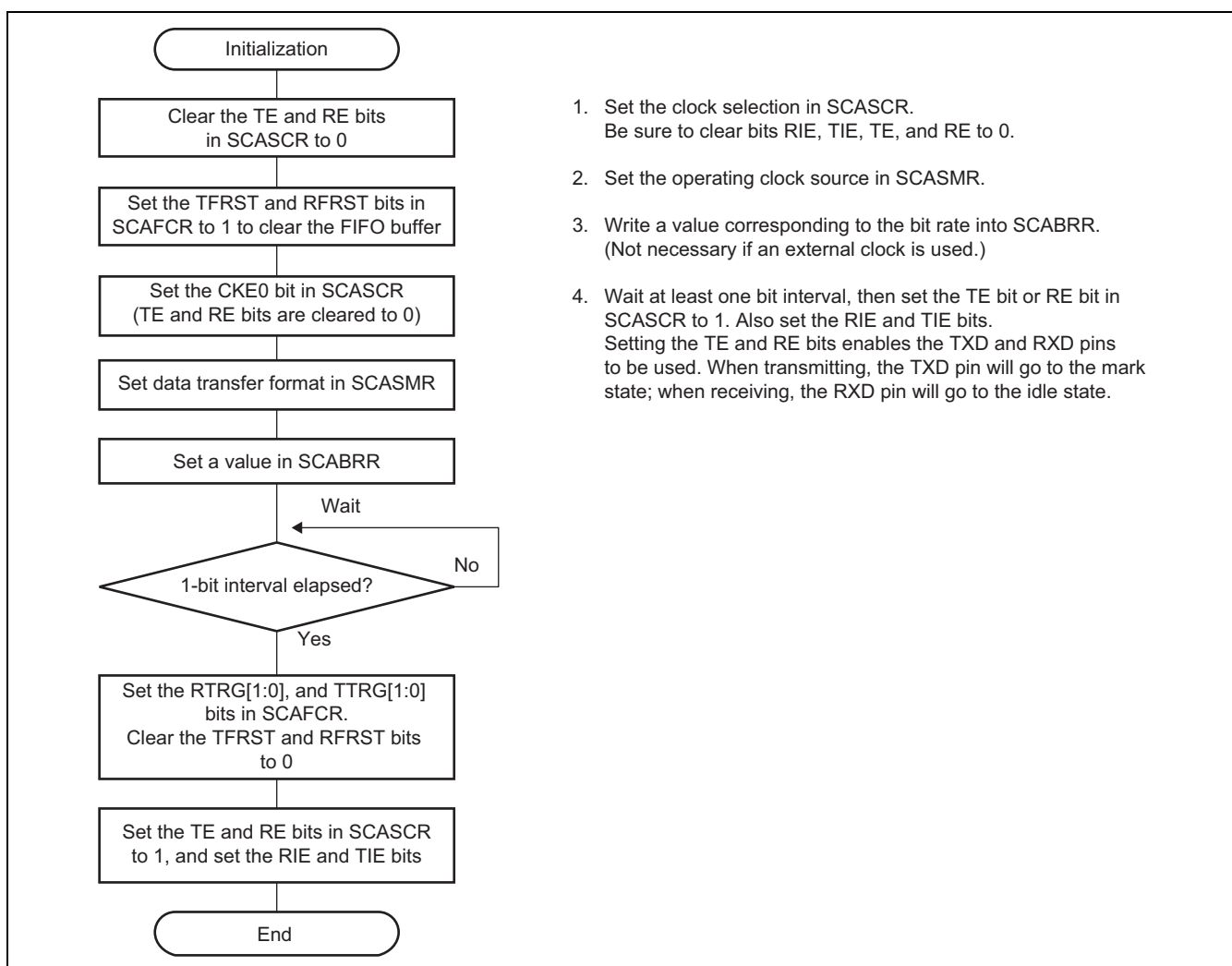
1. SCIFA initialization

Before transmitting and receiving data, it is necessary to clear the TE and RE bits in SCASCR to 0, then initialize SCIFA as described below.

When the transfer format, etc., is changed, the TE and RE bits must be cleared to 0 before making the change using the following procedure. When the TE bit is cleared to 0, SCATSR is initialized. Note that clearing the TE and RE bits to 0 does not change the contents of SCASSR, SCAFTDR, or SCAFRDR. The TE bit should be cleared to 0 after all transmit data has been sent and the TEND bit in SCASSR has been set to 1. Clearing to 0 can also be performed during transmission, but the data lines that transmit the data will go to the high-impedance state after the clearance.

Before setting TE to 1 again to start transmission, the TFRST bit in SCAFCR should first be set to 1 to reset SCAFTDR.

Figure 41.2 is an example of flow for the SCIFA initialization.



1. Set the clock selection in SCASCR. Be sure to clear bits RIE, TIE, TE, and RE to 0.
2. Set the operating clock source in SCASMR.
3. Write a value corresponding to the bit rate into SCABRR. (Not necessary if an external clock is used.)
4. Wait at least one bit interval, then set the TE bit or RE bit in SCASCR to 1. Also set the RIE and TIE bits. Setting the TE and RE bits enables the TXD and RXD pins to be used. When transmitting, the TXD pin will go to the mark state; when receiving, the RXD pin will go to the idle state.

**Figure 41.2 Example of Flow for SCIFA Initialization**



## 2. Serial data transmission

Figure 41.3 is an example of flow for serial transmission.

Use the following procedure for serial data transmission after enabling SCIFA for transmission.

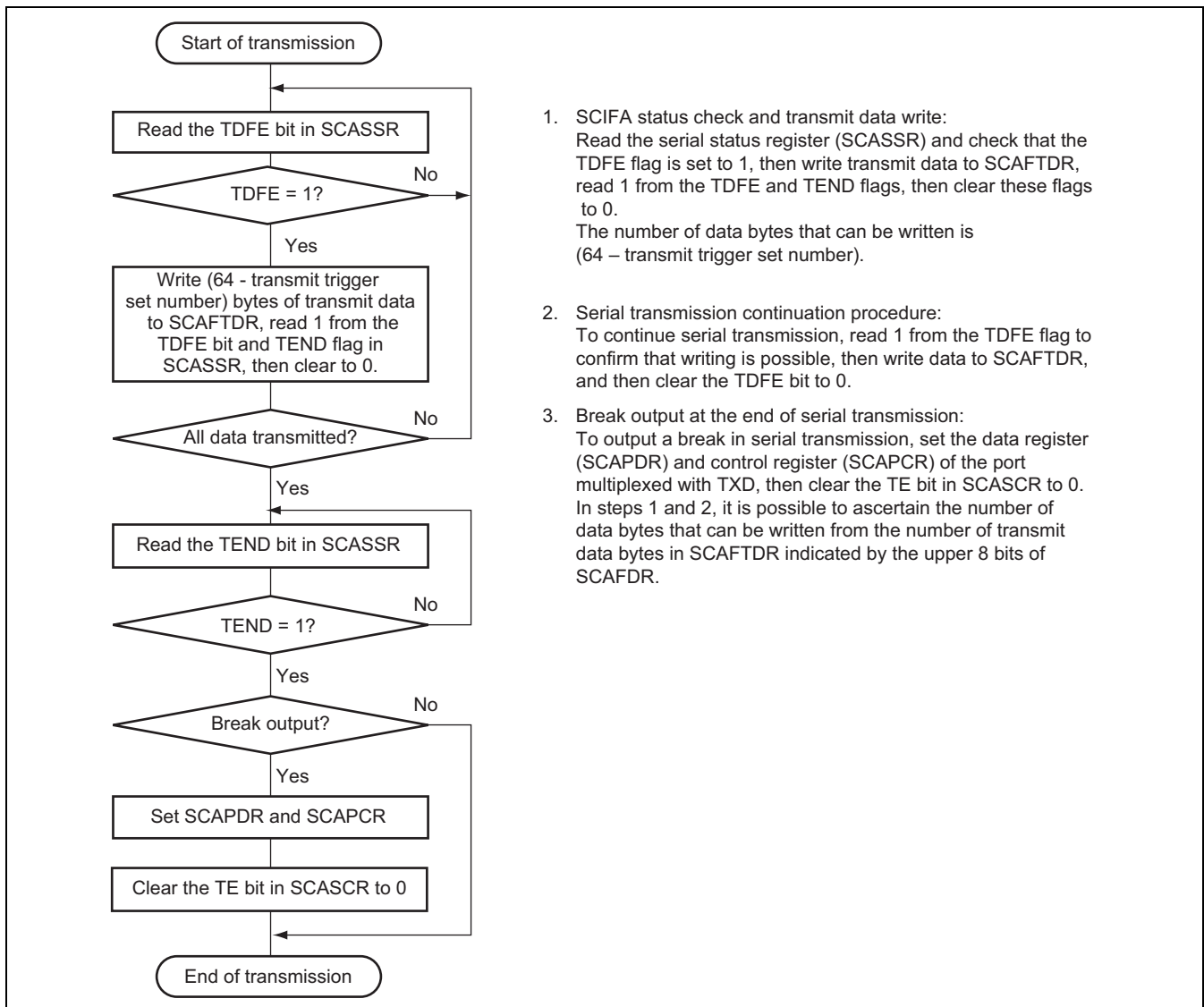


Figure 41.3 Example of Flow for Serial Transmission

In serial transmission, SCIFA operates as described below.

- A. When data is written into SCAFTDR, SCIFA transfers the data from SCAFTDR to SCATSR and starts transmitting. Confirm that the TDFE flag in SCASSR is set to 1 before writing transmit data to SCAFTDR. The number of data bytes that can be written is not less than (64 – transmit trigger set number).
- B. When data is transferred from SCAFTDR to SCATSR and transmission is started, consecutive transmit operations are performed until there is no transmit data left in SCAFTDR. When the number of transmit data bytes in SCAFTDR falls to or below the transmit trigger number set in SCAFCR, the TDFE flag is set. If the TIE bit in SCASCR is set to 1 at this time, a transmit-FIFO-data-empty interrupt (TXI) request is generated.

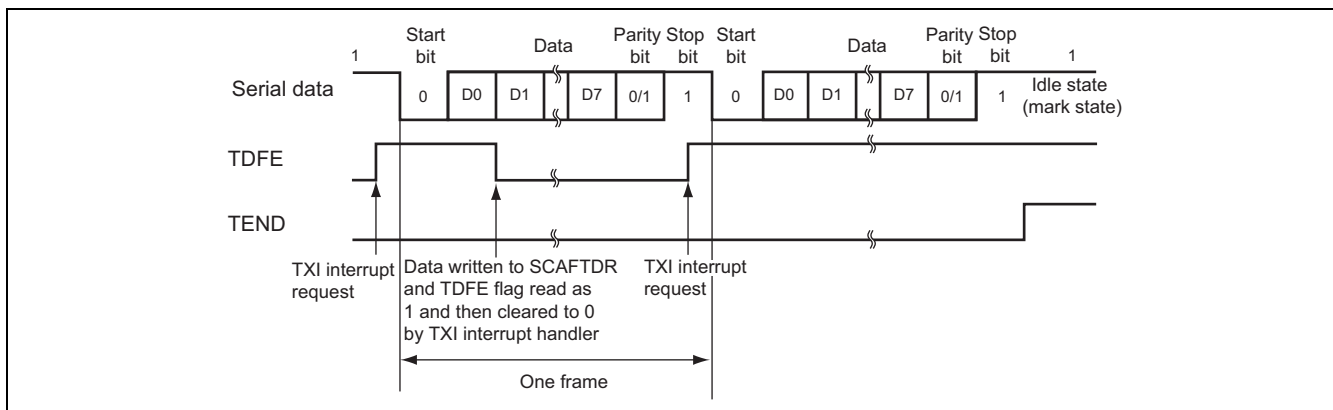
When the transmit data stop function is used and the number of data bytes set in SCATDSR is matched, transmit operation is stopped, and the TSF flag in SCASSR is set. If the TSIE bit in SCASCR is set to 1, a transmit-data-stop interrupt (TDI) request is generated. The vectors of TXI and TDI are the same.

The serial transmit data is sent from the TXD pin in the following order.

- a. Start bit: One logic-0 bit is output.
  - b. Transmit data: 8-bit or 7-bit data is output in LSB-first order.
  - c. Parity bit: One parity bit (even or odd parity) is output.
  - d. A format in which a parity bit is not output can also be selected.
  - e. Stop bit(s): One or two logic-1 bits (stop bits) are output.
  - f. Mark state: Output of 1 is continued until the start bit is sent to start the next transmission.
- C. SCIFA checks the SCAFTDR transmit data at the timing for sending the stop bit. If data is present, the data is transferred from SCAFTDR to SCATSR, the stop bit is sent, and then serial transmission of the next frame is started.

If there is no transmit data, the TEND flag in SCASSR is set to 1, the stop bit is sent, and then the line goes to the mark state in which 1 is output.

Figure 41.4 is an example of the transmission in asynchronous mode.

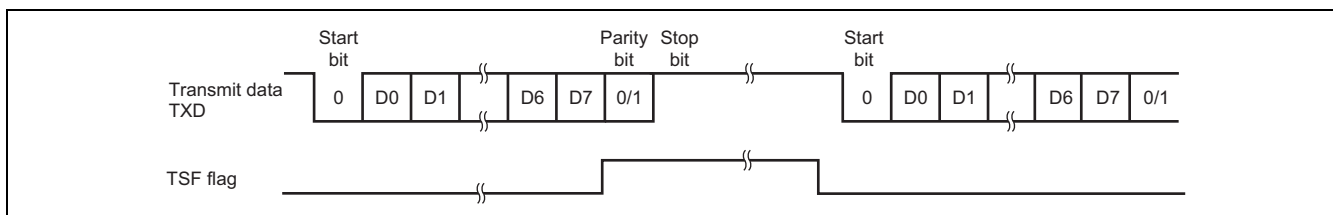


**Figure 41.4 Example of Transmission  
(Example with 8-Bit Data, Parity, and One Stop Bit)**

- Transmit data stop function

When (value in SCATDSR + 1) is matched with the number of transmitted data bytes, this function stops the transmit operation. Interrupts can be generated and the DMAC can be activated by setting the TSIE bit (interrupt enable bit) to 1.

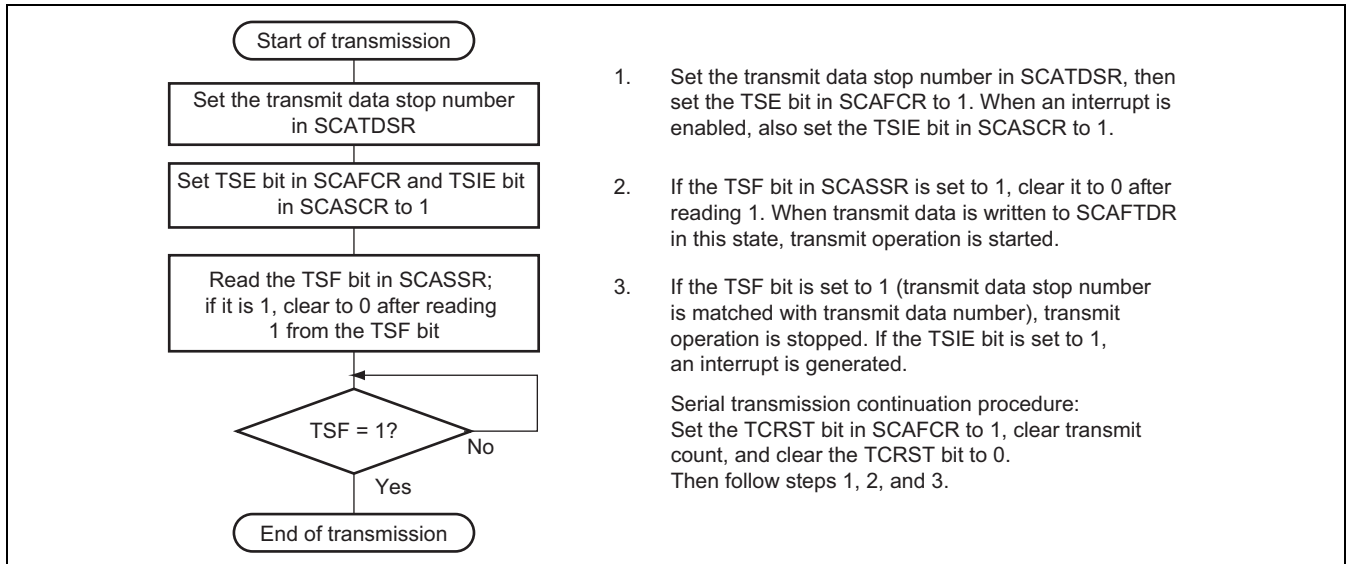
Figure 41.5 is an example of operation for the transmit data stop function.



**Figure 41.5 Example of Transmit Data Stop Function**

Figure 41.6 is a flow for the transmit data stop function.

Before using the transmit data stop function, set the TCRST bit in SCAFPCR to 1 to clear the transmit counter. After modifying SCASSR, always confirm that data has been updated.

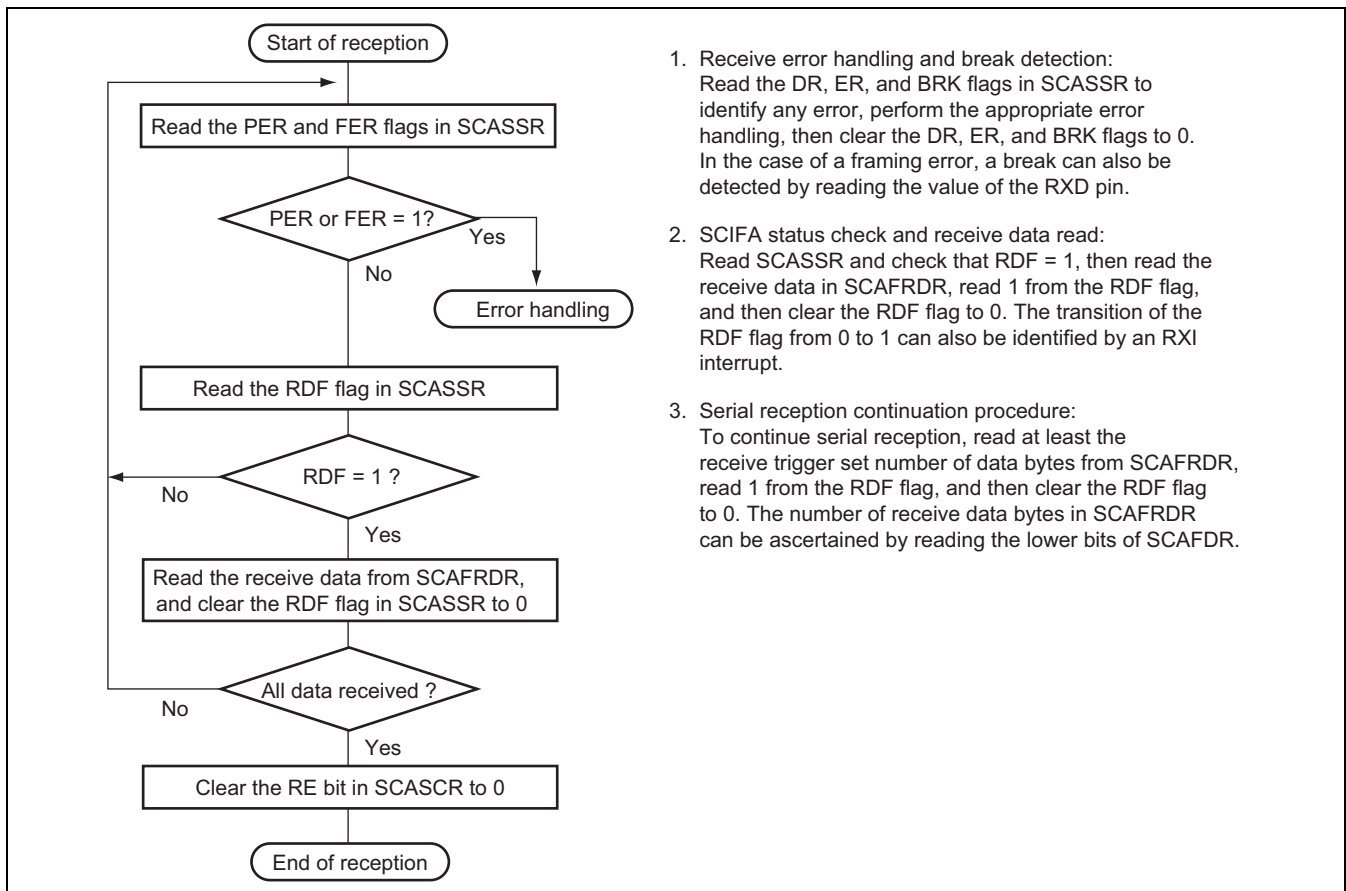


**Figure 41.6 Flow for Transmit Data Stop Function**

## 3. Serial data reception

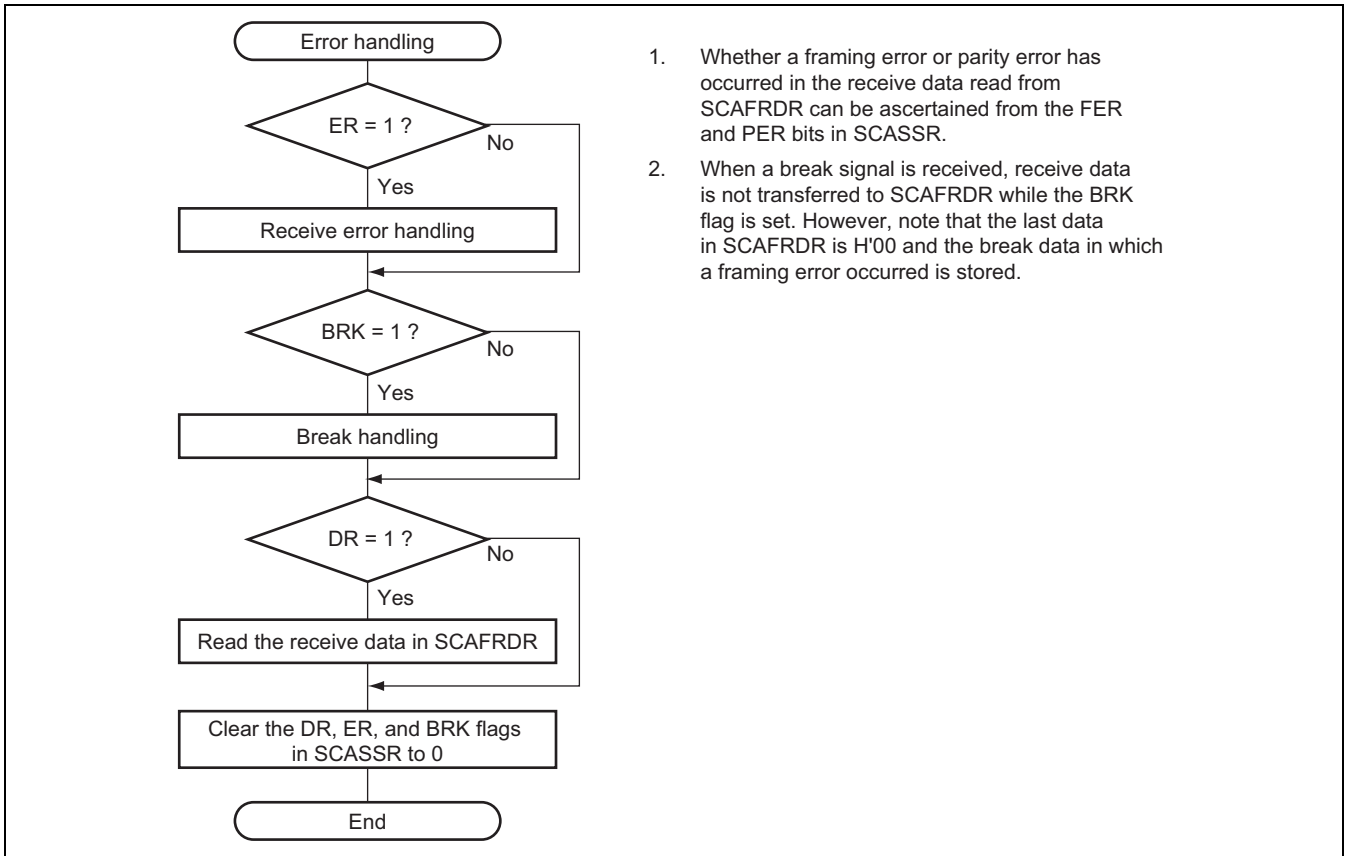
Figures 41.7 and 41.8 are examples of flows for serial reception.

Use the following procedure for serial data reception after enabling SCIFA for reception.



1. Receive error handling and break detection:  
Read the DR, ER, and BRK flags in SCASSR to identify any error, perform the appropriate error handling, then clear the DR, ER, and BRK flags to 0. In the case of a framing error, a break can also be detected by reading the value of the RXD pin.
2. SCIFA status check and receive data read:  
Read SCASSR and check that RDF = 1, then read the receive data in SCAFRDR, read 1 from the RDF flag, and then clear the RDF flag to 0. The transition of the RDF flag from 0 to 1 can also be identified by an RXI interrupt.
3. Serial reception continuation procedure:  
To continue serial reception, read at least the receive trigger set number of data bytes from SCAFRDR, read 1 from the RDF flag, and then clear the RDF flag to 0. The number of receive data bytes in SCAFRDR can be ascertained by reading the lower bits of SCAFDR.

**Figure 41.7 Example of Flow for Serial Reception (1)**



1. Whether a framing error or parity error has occurred in the receive data read from SCAFRDR can be ascertained from the FER and PER bits in SCASSR.
2. When a break signal is received, receive data is not transferred to SCAFRDR while the BRK flag is set. However, note that the last data in SCAFRDR is H'00 and the break data in which a framing error occurred is stored.

Figure 41.8 Example of Flow for Serial Reception (2)

In serial reception, SCIFA operates as described below.

- A. SCIFA monitors the communication line, and if a 0 start bit is detected, performs internal synchronization and starts reception.
- B. The received data is stored in SCARSR in LSB-to-MSB order.
- C. The parity bit and stop bit are received.

After receiving these bits, SCIFA carries out the following checks.

- a. Stop bit check: SCIFA checks to see if the value in the stop bit position is 1. If the two-stop-bit setting has been made, only the value in the first stop-bit position is checked.
- b. SCIFA checks whether received data can be transferred from SCARSR to SCAFRDR.
- c. Break check: SCIFA checks to confirm that the BRK flag is 0, indicating that the break state has not been set.

If all the above checks are passed, the receive data is stored in SCAFRDR.

Note: Reception continues when a receive error (a framing error or parity error) occurs.

- D. If the RIE bit in SCASCR is set to 1 when the RDF flag changes to 1, a receive-FIFO-data-full interrupt (RXI) request is generated.

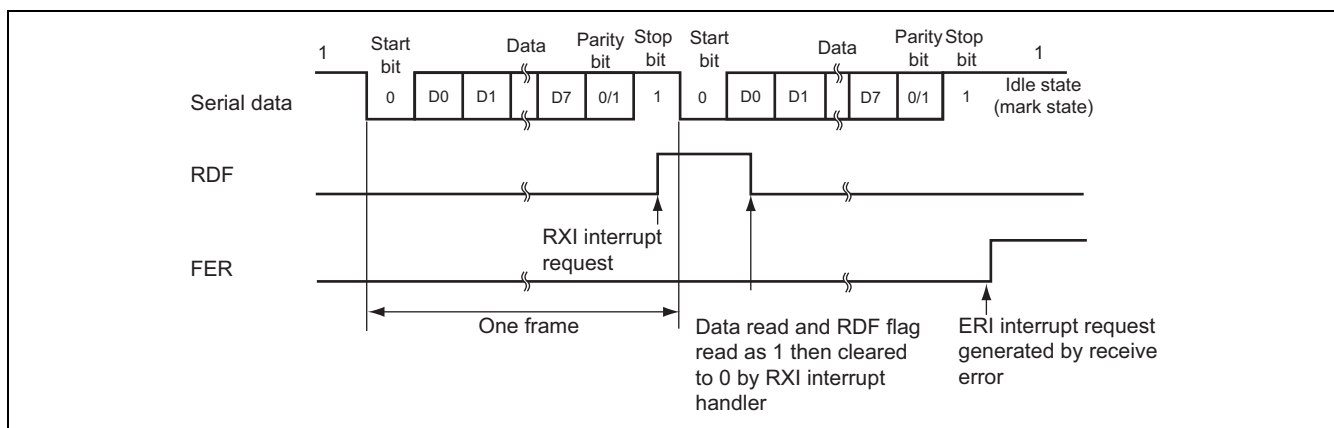
If the ERIE bit in SCASCR is set to 1 when the ER flag changes to 1, a receive-error interrupt (ERI) request is generated.

If the BRIE bit in SCASCR is set to 1 when the BRK flag changes to 1, a break-receive interrupt (BRI) request is generated.

If the DRIE bit in SCASCR is set to 1 when the DR flag changes to 1, a receive-data-ready interrupt (DRI) request is generated.

The vectors of each interrupt source are the same.

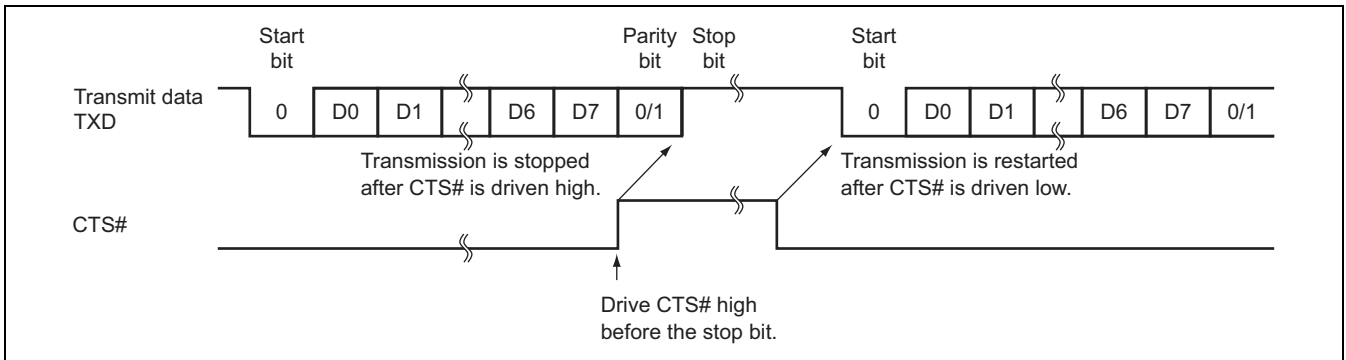
Figure 41.9 is an example of the reception in asynchronous mode.



**Figure 41.9 Example of SCIFA Receive Operation (Example with 8-Bit Data, Parity, One Stop Bit)**

SCIFA has a modem function that allows the stoppage and resumption of transmission according to the input value of CTS#. Setting CTS# to 1 places the transmission line in the mark state after transmission of the current frame. When CTS# is set to 0, the next frame for transmission is output, with a start bit as its leader.

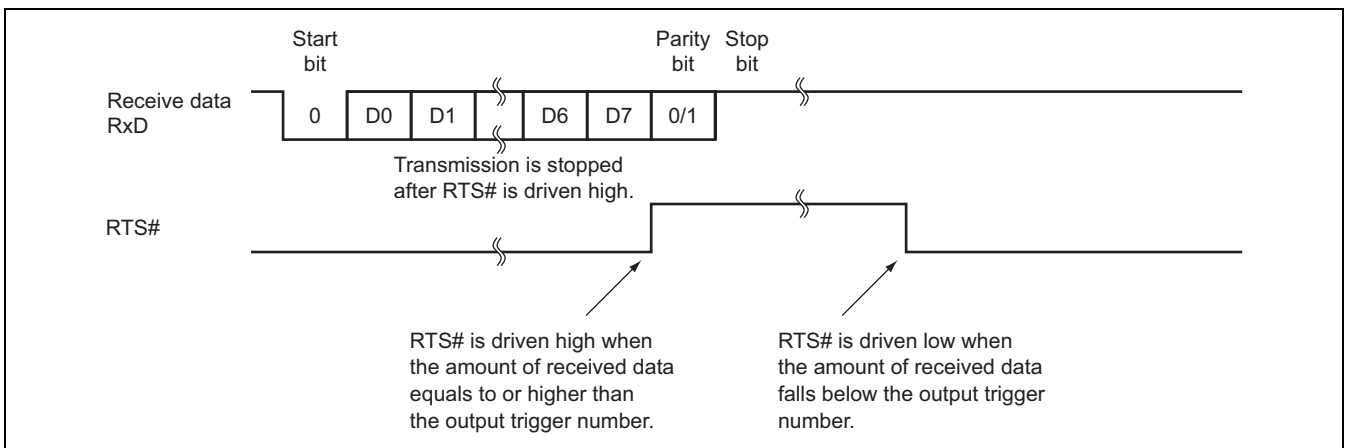
Figure 41.10 is an example of the operation of CTS# control.



**Figure 41.10 Example of CTS# Control Operation**

The RTS# signal is driven high when the modem function is in use and the received data stored in the receive FIFO register (SCAFRDR) equals or exceeds the number of the RTS# output triggers.

Figure 41.11 is an example of the operation for RTS# control.



**Figure 41.11 Example of RTS# Control Operation**



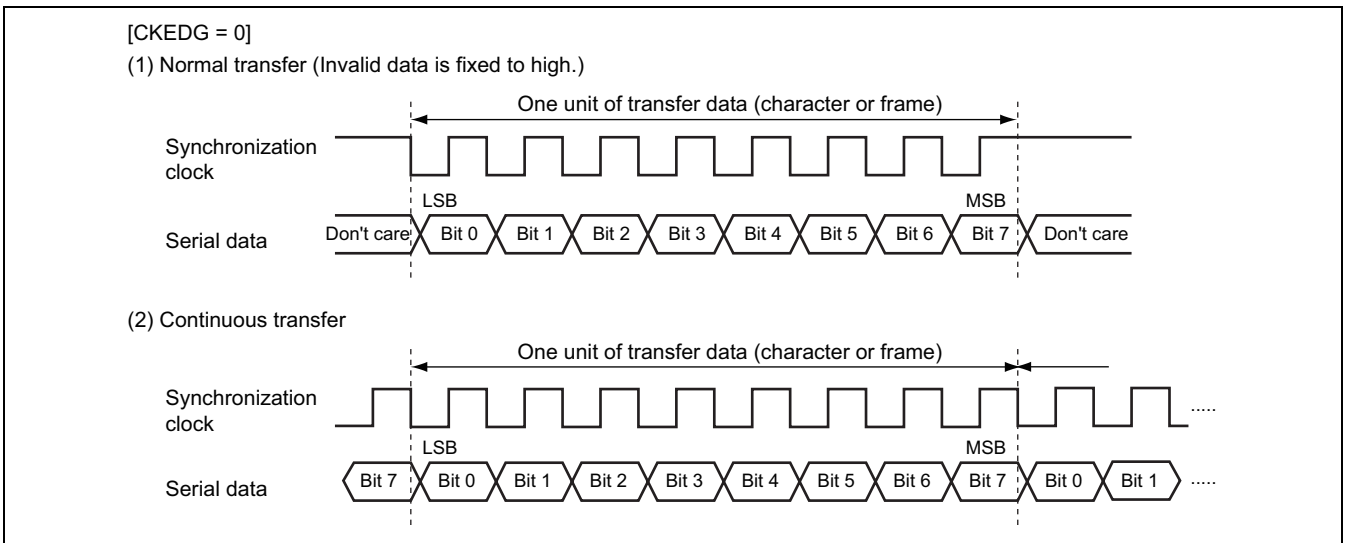
**41.4.4 Operation in Clocked Synchronous Mode**

Clocked synchronous mode, in which data is transmitted or received in synchronization with clock pulses, is suitable for fast serial communications.

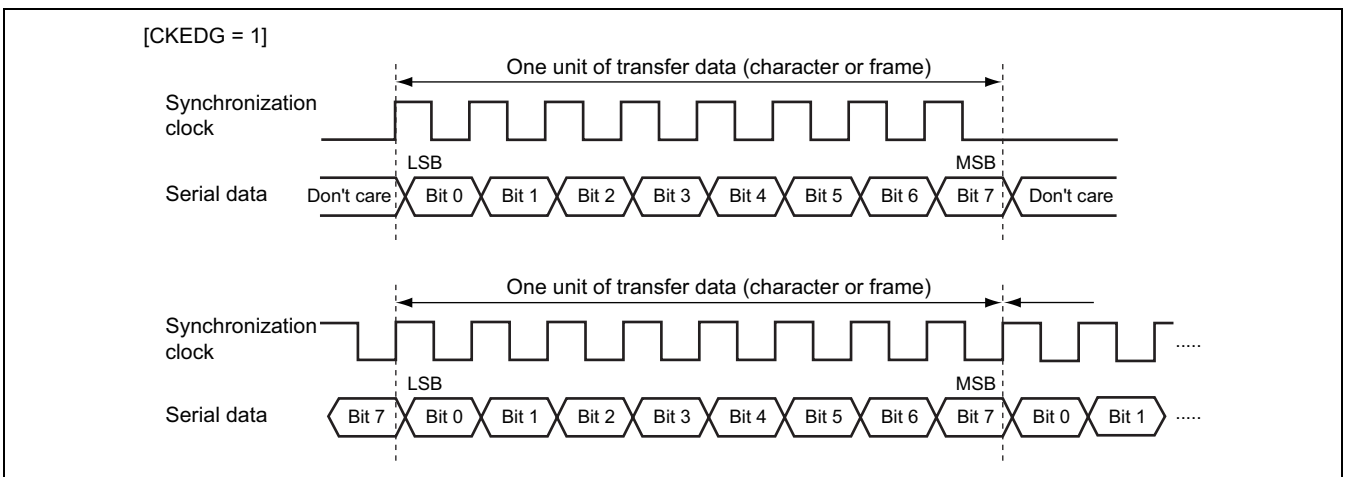
Since the transmitter and receiver are independent units in SCIFA, full-duplex communications can be achieved by sharing the clock. Both the transmitter and receiver have a 64-stage FIFO buffer structure, so that data can be read or written during transmission or reception, enabling continuous data transmission and reception.

Through the setting of the CKEDG bit, the format for clocked synchronous communications can be selected.

Figures 41.12 and 41.13 show the format for clocked synchronous communications.



**Figure 41.12 Data Format in Clocked Synchronous Communications (CKEDG = 0)**



**Figure 41.13 Data Format in Clocked Synchronous Communications (CKEDG = 1)**

In clocked synchronous serial communications, the data on the communications line is latched on one edge of the synchronization clock signal selected by the CKEDG bit and is output until the next edge. Accuracy of data is guaranteed on the next edge (i.e. that in the opposite direction to the latching edge).

In serial communications, each character is output starting with the LSB and ending with the MSB. After the MSB is output, the communications line remains in the state of the last bit.

Data is received on the opposite edge to that on which data is output.

### (1) Data Transfer Format

A fixed 8-bit data format is used. No parity bit can be added.

### (2) Clock

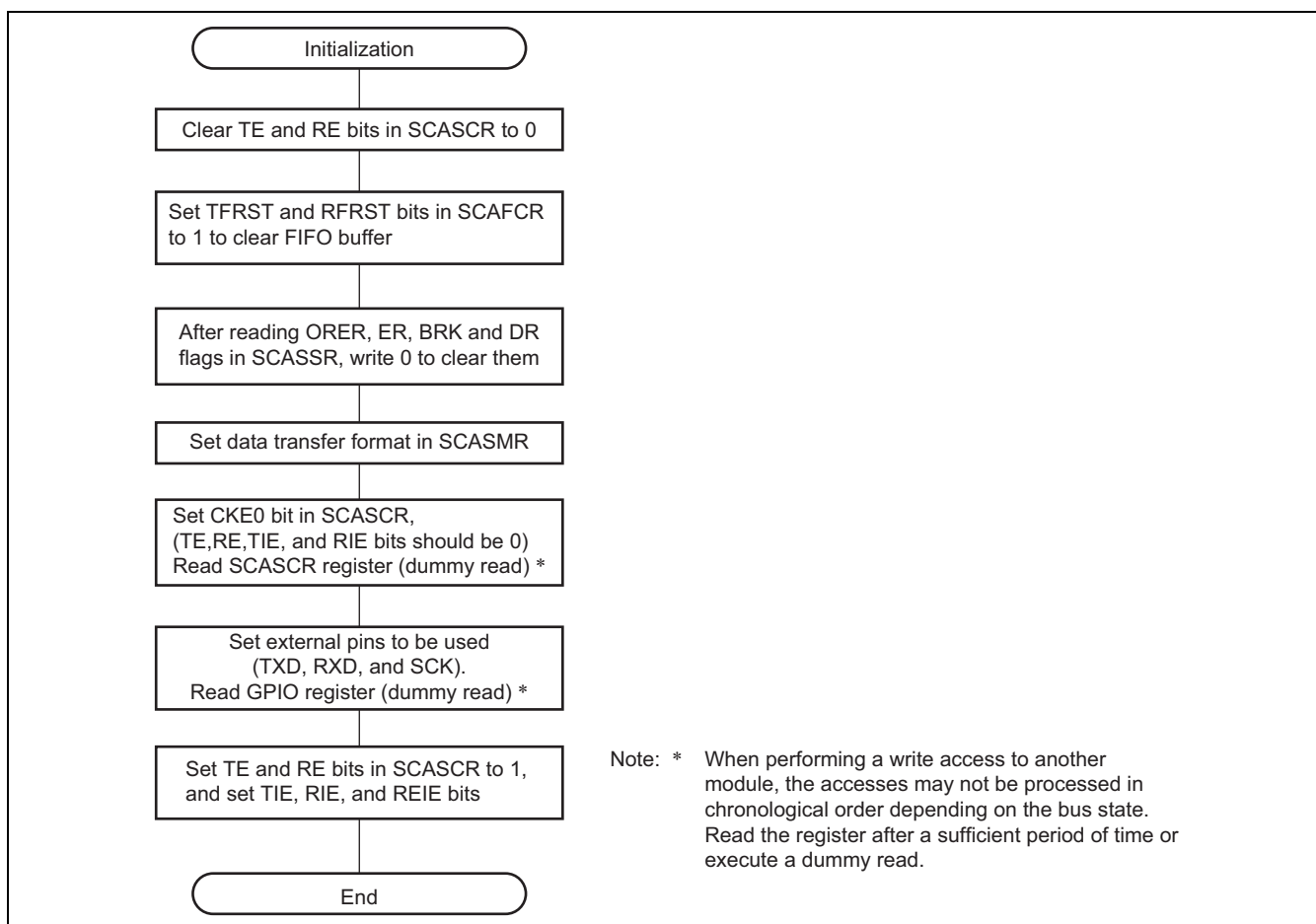
An internal clock signal generated by the on-chip baud rate generator provides the transfer clock for SCIFA. For details on SCIFA clock source selection, see Table 41.4.

### (3) SCIFA Initialization (Clocked Synchronous Mode)

Before transmitting and receiving data, it is necessary to clear the TE and RE bits in SCASCR to 0, and then initialize SCIFA as described below.

When changing the operating mode or transfer format, etc., the TE and RE bits must be cleared to 0 before making the change using the following procedure. When the TE bit is cleared to 0, SCATSR is initialized. Note that clearing the RE bit to 0 does not initialize the RDF, PER, FER, or ORER flag state or change the contents of SCAFRDR.

Figure 41.14 is an example of flow for the SCIFA initialization.

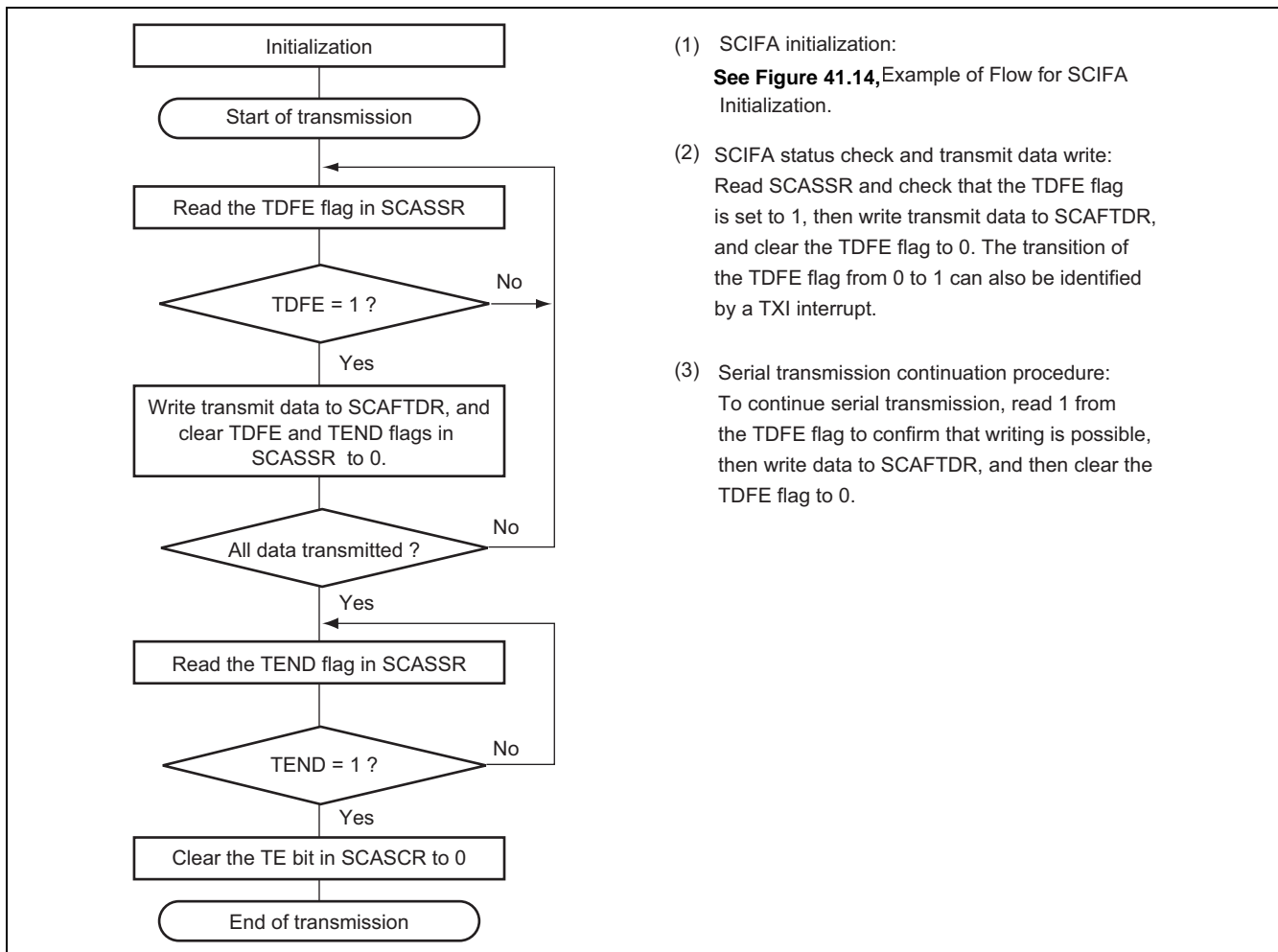


**Figure 41.14 Example of Flow for SCIFA Initialization**

**(4) Serial Data Transmission (Clocked Synchronous Mode)**

Figure 41.15 is an example of flow for serial transmission.

Use the following procedure for serial data transmission after enabling SCIFA for transmission.



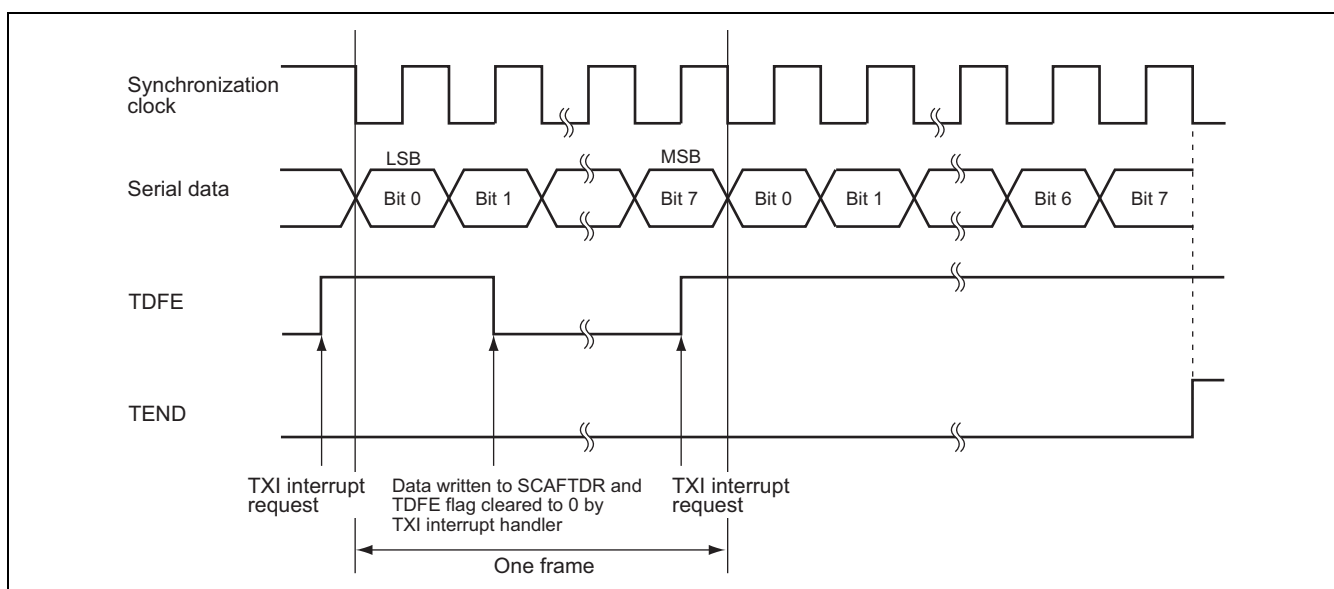
- (1) SCIFA initialization:  
**See Figure 41.14**, Example of Flow for SCIFA Initialization.
- (2) SCIFA status check and transmit data write:  
 Read SCASSR and check that the TDFE flag is set to 1, then write transmit data to SCAFTDR, and clear the TDFE flag to 0. The transition of the TDFE flag from 0 to 1 can also be identified by a TXI interrupt.
- (3) Serial transmission continuation procedure:  
 To continue serial transmission, read 1 from the TDFE flag to confirm that writing is possible, then write data to SCAFTDR, and then clear the TDFE flag to 0.

**Figure 41.15 Example of Flow for Serial Transmission**

In serial transmission, SCIFA operates as described below.

1. When data is written into SCAFTDR, SCIFA transfers data from SCAFTDR to SCATSR and starts transmitting. Confirm that the TDFE flag in SCASSR is set to 1 before writing transmit data to SCAFTDR. The number of data bytes that can be written is at least 16 – (transmit trigger set number).
2. When data is transferred from SCAFTDR to SCATSR and transmission is started, consecutive transmit operations are performed until there is no transmit data left in SCAFTDR. When the number of transmit data bytes in SCAFTDR falls to or below the transmit trigger number set in SCAFCR, the TDFE flag is set. If the TIE bit in SCASCR is set to 1 at this time, a transmit-FIFO-data-empty interrupt (TXI) request is generated. The SCIFA outputs data in synchronization with the synchronization clock. The serial transmit data is sent from the TXD pin in the LSB-first order.
3. SCIFA checks the SCAFTDR transmit data at the timing for sending the last bit. If data is present, the data is transferred from SCAFTDR to SCATSR, and then serial transmission of the next frame is started. If there is no transmit data, the TEND flag in SCASSR is set to 1 after the last bit is sent, and the transmit data pin (TXD pin) retains the output state of the last bit.

Figure 41.16 is an example of the SCIFA transmission in clocked synchronous mode.



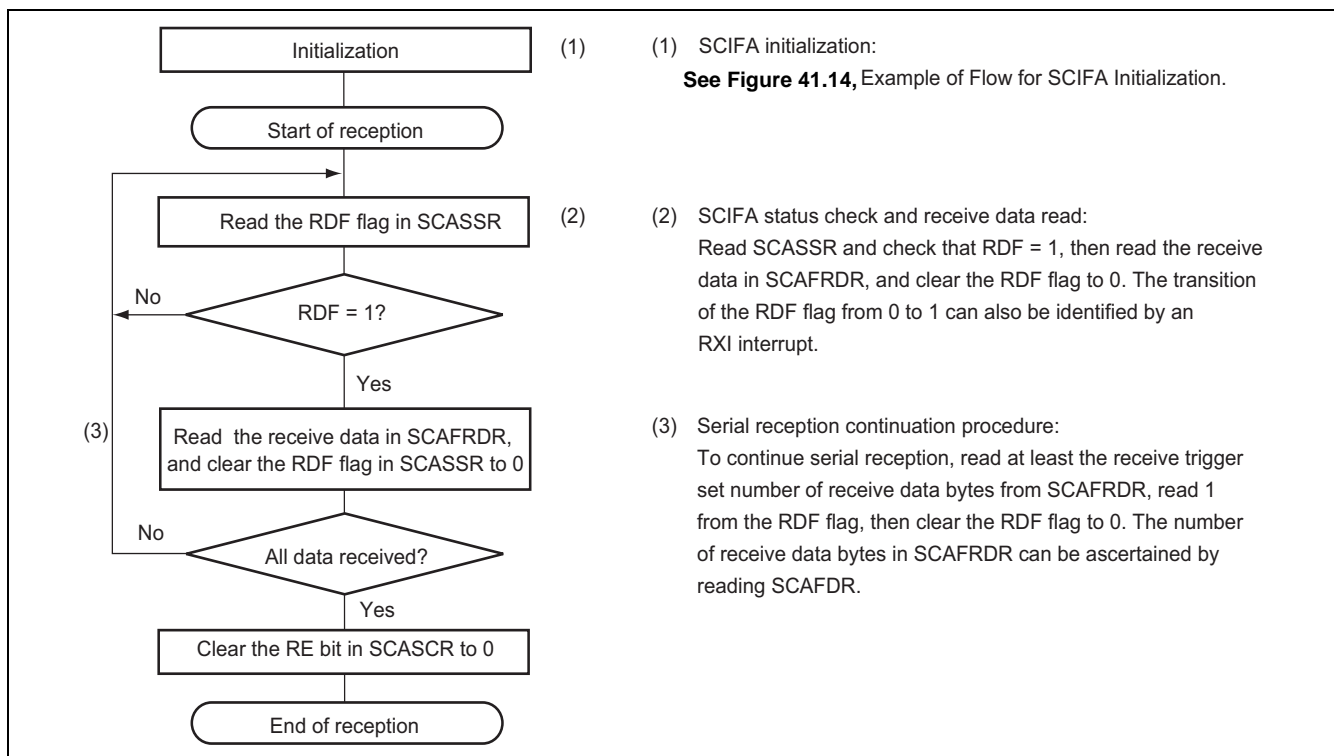
**Figure 41.16 Example of SCIFA Transmission in Clocked Synchronous Mode**

### (5) Serial Data Reception (Clocked Synchronous Mode)

Figure 41.17 is an example of flow for serial reception.

Use the following procedure for serial data reception after enabling SCIFA for reception.

When switching the operating mode from asynchronous mode to clocked synchronous mode without initializing SCIFA, make sure that the ORER flag in SCASSR, and PER and FER flags in SCASSR are cleared to 0.

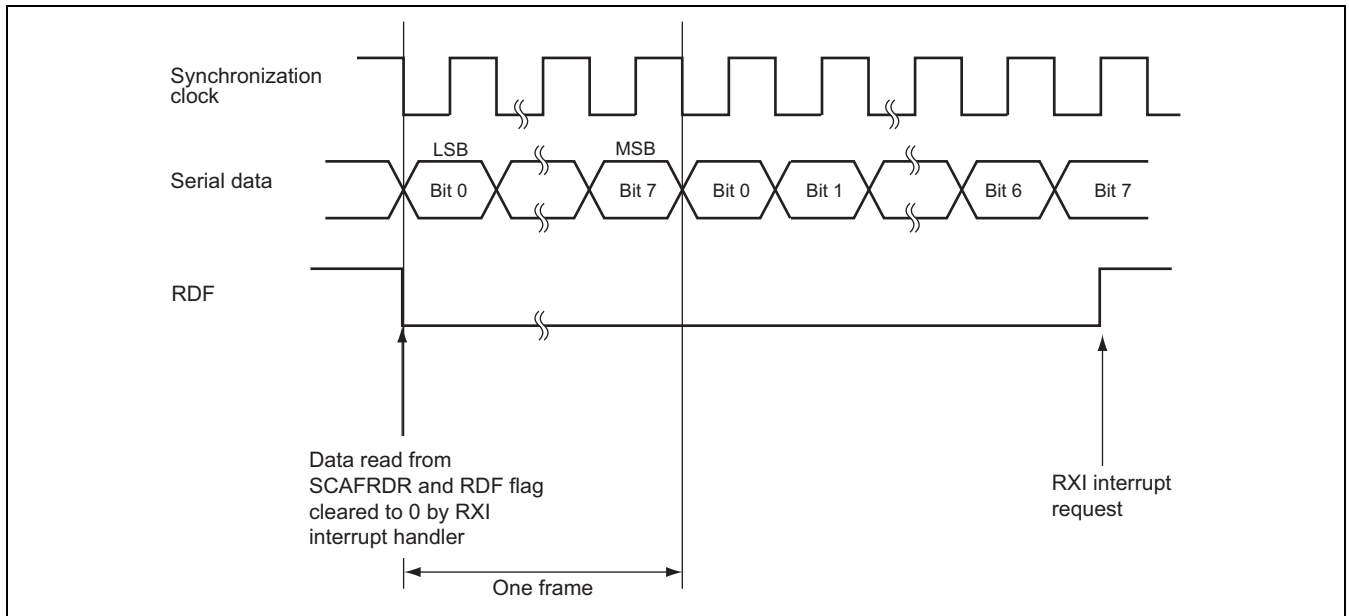


**Figure 41.17 Example of Flow for Serial Reception**

In serial reception, SCIFA operates as described below.

1. SCIFA starts reception in synchronization with the output of the synchronization clock.
2. The received data is stored in SCARSR in LSB-to-MSB order.  
After receiving the data, SCIFA checks whether the receive data can be transferred from SCARSR to SCAFRDR. If this check is passed, the receive data is stored in SCAFRDR. If an overrun error is detected in the error check, reception cannot continue.
3. If the RIE bit in SCASCR is set to 1 when the RDF flag changes to 1, a receive-FIFO-data-full interrupt (RXI) request is generated.

Figure 41.18 is an example of the reception in clocked synchronous mode.

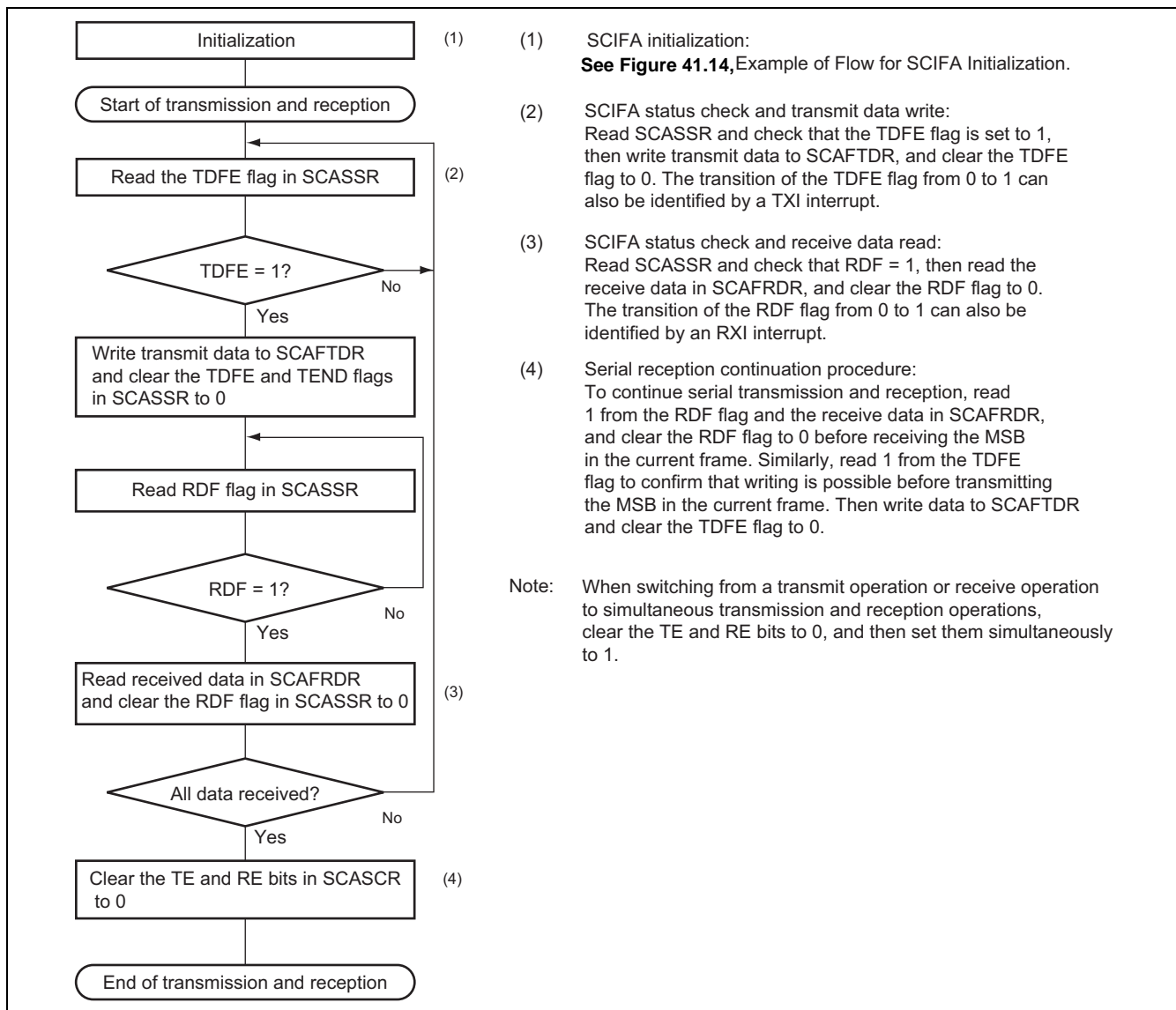


**Figure 41.18 Example of Reception in Clocked Synchronous Mode**

**(6) Simultaneous Serial Data Transmission and Reception (Clocked Synchronous Mode)**

Figure 41.19 is an example of flow for the simultaneous serial data transmission and reception.

Use the following procedure for simultaneous serial transmission and reception after enabling SCIFA for both the transmission and reception.



**Figure 41.19 Example of Flow for Simultaneous Serial Transmission and Reception**

## 41.5 SCIFA Interrupt Sources and DMAC

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

SCIFA supports seven interrupts: transmit-FIFO-data-empty (TXI), transmit-data-stop (TDI), receive-error (ERI), receive-FIFO-data-full (RXI), break (BRI), receive-data-ready (DRI), and transmit-end (TEND). The vectors of each interrupt source are the same.

Table 41.7 shows the interrupt sources. The TIE, RIE, ERIE, BRIE, DRIE, TSIE, and TENDE bits in SCASCR are used to enable or disable the respective interrupt sources.

If the TDFE flag in SCASSR is set to 1, a TXI interrupt request is generated. When the TSF flag in SCASSR is set to 1, a TDI interrupt request is generated. The DMAC can be activated and data transfer performed on generation of TXI and TDI interrupt requests. When data exceeding the transmit trigger set number is written to SCAFTDR by the DMAC, the DMAC transfer request is automatically cleared to 0. The DMAC requests of TXI and TDI are the same.

When the RDF flag in SCASSR is set to 1, an RXI interrupt request is generated. The DMAC can be activated and data transfer performed on generation of an RXI interrupt request. When receive data in SCAFRDR is read by the DMAC until the amount left is less than the receive trigger set number, the DMAC transfer request is automatically cleared to 0.

When using the DMAC for transmission/reception, set the DMAC to the DMAC transfer enabled state before making the SCIFA settings. Transmission/reception is complete when the DMA transfer is terminated.

When the TEND flag in SCASSR is set to 1, the ER flag in SCASSR is set to 1, the BRK flag in SCASSR is set to 1, the DR flag in SCASSR is set to 1, or the TSF flag in SCASSR is set to 1, an interrupt request is generated. Note that the vectors of each interrupt source are the same.

**Table 41.7 SCIFA Interrupt Sources**

Interrupt Source Type	DMAC Activation
Interrupt initiated by receive error flag (ER), break flag (BRK), receive data ready flag (DR), transmit data stop flag (TSF), or transmit-end flag(TEND)	Not possible
Interrupt initiated by receive FIFO data full flag (RDF)	Possible
Interrupt initiated by transmit FIFO data empty flag (TDFE)	Possible



## 41.6 Usage Notes

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

Note the following when using SCIFA.

### (1) SCAFTDR Writing and the TDFE Flag

The TDFE flag in SCASSR is set when the number of transmit data bytes written in SCAFTDR has fallen to or below the transmit trigger number set by bits TTRG[1:0] in SCAFCCR. After TDFE is set, transmit data up to the number of empty bytes in SCAFTDR can be written, allowing efficient continuous transmission.

However, if the number of data bytes written in SCAFTDR is equal to or less than the transmit trigger number, the TDFE flag will be set to 1 again after being read as 1 and cleared to 0. TDFE clearing should therefore be carried out when SCAFTDR contains more than the transmit trigger number of transmit data bytes.

The number of transmit data bytes in SCAFTDR can be found from the T[6:0] bits in SCAFDR.

### (2) SCAFRDR Reading and the RDF Flag

The RDF flag in SCASSR is set when the number of receive data bytes in SCAFRDR has become equal to or greater than the receive trigger number set by bits RTRG[1:0] in SCAFCCR. After RDF is set, receive data equivalent to the trigger number can be read from SCAFRDR, allowing efficient continuous reception.

However, if the number of data bytes in SCAFRDR is still equal to or greater than the trigger number after a read, the RDF flag will be set to 1 again if it is cleared to 0. RDF should therefore be cleared to 0 after being read as 1 after all received data has been read.

The number of receive data bytes in SCAFRDR can be found from the R[6:0] bits in SCAFDR.

### (3) Break Detection and Processing

Break signals can be detected by reading the RXD pin directly when a framing error (FER) is detected. In the break state, the input from the RXD pin consists of all 0s, so the FER flag is set and the parity error flag (PER) may also be set.

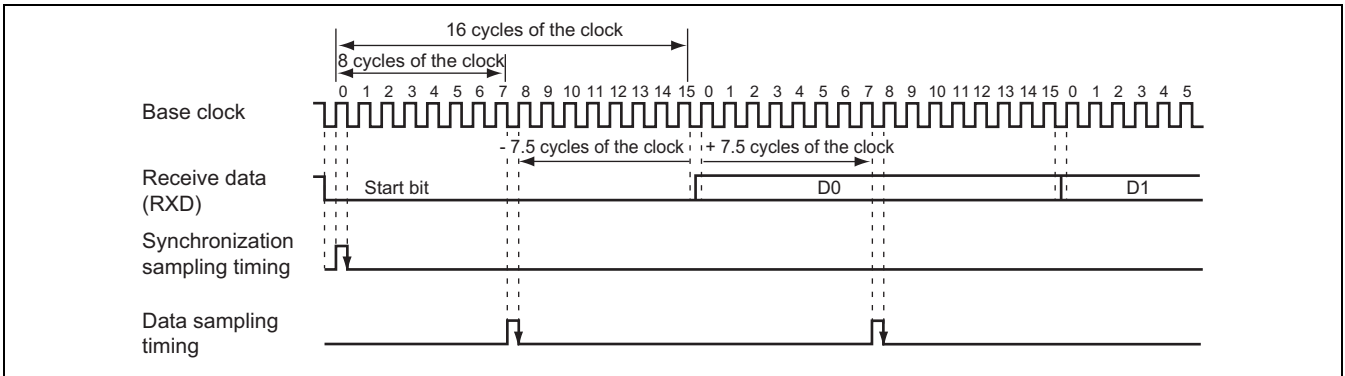
Although SCIFA stops transferring receive data to SCAFRDR after receiving a break, the receive operation continues.

**(4) Receive Data Sampling Timing and Receive Margin**

As an example, when the sampling rate is 1/16, SCIFA operates on a base clock with a frequency of 8 times the transfer rate.

In reception, SCIFA synchronizes internally with the fall of the start bit, which it samples on the base clock. Receive data is latched at the rising edge of the eighth base clock pulse (when the sampling rate is 1/16).

The timing is shown in Figure 41.20.



**Figure 41.20 Receive Data Sampling Timing**

The receive margin can therefore be expressed as shown in equation (1).

$$M = \left| \left( 0.5 - \frac{1}{2N} \right) - (L - 0.5)F - \frac{|D - 0.5|}{N} (1 + F) \right| \times 100\% \dots (1)$$

- M: Receive margin (%)
- N: Ratio of clock frequency to bit rate (N = 16)
- D: Clock duty cycle (D = 0 to 1.0)
- L: Frame length (L = 9 to 12)
- F: Absolute deviation of clock frequency

From equation (1), if F = 0 and D = 0.5, the receive margin is 46.875%, as given by equation (2).

When D = 0.5 and F = 0:

$$M = (0.5 - 1/(2 \times 16)) \times 100\% = 46.875\% \dots (2)$$

This is a theoretical value. A reasonable margin to allow in system designs is the value above (46.875%) plus 20% to 30%.

**(5) State of the PAD Pin when the Pin for SCIFA is Selected**

The table below shows the state of the PAD pin when the pin for SCIFA is selected.

**Table 41.8 State of PAD Pin**

<b>When the Pin for SCIFA is Selected</b>	<b>TXD</b>	<b>RXD</b>	<b>RTS#</b>	<b>CTS#</b>	<b>SCK</b>
PAD enable	1 (enabled)	1 (enabled)	RTSC in SCAPCR (initial value:1, serial port enabled), and MCE in SCAFCCR (initial value: 0, disabled)	MCE in SCAFCCR (initial value: 0, disabled)	SCKC in SCAPCR (initial value:1, serial port enabled), and CKE0 in SCASCR (Initial value: 0, disabled)
Pin state	Output (initial value: 1)	Input	Port output (initial value: 1)	Input	Port output (initial value: 0)
Pull-up/-down	—	Pull-up required	—	Pull-up required	—
Remarks	—	SCIFA fixes RXD to 1 internally when RE in SCASCR = 0.	RTS# is Hi-Z when RTSC in SCAPCR = 0, and MCE in SCAFCCR = 0.	SCIFA fixes CTS# to 1 internally when MCE in SCAFCCR = 0.	SCK is Hi-Z when SCKC in SCAPCR = 0, and CKE0 in SCASCR = 0.

## 42. Serial Communications Interface with FIFO B (SCIFB)

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

This LSI has three serial communications interfaces B incorporating FIFO buffers (SCIFB) that can perform both asynchronous and clocked synchronous serial communications.

Each interface includes two 256-stage buffers, one for the transmit FIFO register and, one for the receive FIFO register, enabling fast, efficient, and continuous communications.

### 42.1 Features

- 3 channels are implemented.
- Asynchronous mode
 

Serial data communications are executed using an asynchronous system in which synchronization is achieved character by character. Serial data communications can be carried out with standard asynchronous communications chips such as a Universal Asynchronous Receiver/Transmitter (UART) or Asynchronous Communications Interface Adapter (ACIA).

There is a choice of eight serial data communication formats.

  - Data length: 7 or 8 bits
  - Stop bit length: 1 or 2 bits
  - Parity: Even/odd/none
  - LSB-first transfer
  - Receive error detection: Parity, framing, and overrun errors
  - Break detection: If a framing error is followed by at least one frame at the space "0" (low level), a break is detected.
- Clocked synchronous mode
 

Serial data communications in synchronization with a clock can be carried out with other LSIs that have a clocked synchronous communications function.

  - Data length: 8 bits
  - Receive error detection: Overrun error
  - A rising or falling edge of a clock is selectable as the data transmit/receive timing.
- On-chip baud rate generator allows any bit rate to be selected.
  - Maximum:  $MP\phi/5$  bps, Minimum:  $MP\phi/(27 \times 256 \times 64)$  bps (asynchronous)
  - Maximum:  $MP\phi/(2 \times 2)$  bps, Minimum:  $MP\phi/(2 \times 256 \times 64)$  bps (clocked synchronous)
- Serial clock source: Internal clock signal generated by the baud rate generator.
- Nine interrupt sources
 

There are nine interrupt sources — receive-FIFO-data-full (RXI), transmit-FIFO-data-empty (TXI), receive-data-ready (DRI), break (BRI), receive-error (ERI), transmit-data-stop (TDI), transmit-end (TENDPOSE), receive-data-count-compare (RCE), and receive-reading-count-compare (RRCC). The vectors of each interrupt source are the same.
- The DMA controller (DMAC) can be activated to execute a data transfer in the event of a transmit-FIFO-data-empty, transmit-data-stop, or receive-FIFO-data-full interrupt. The DMAC requests of transmit-FIFO-data-empty and transmit-data-stop interrupts are the same.
- Supports multibyte DMA transfers.
- On-chip modem control functions (CTS# and RTS#)
- On-chip transmit-data-stop function
- When not in use, the SCIFB can be stopped by halting its clock supply to reduce power consumption.

- The amount of data in the transmit/receive FIFO registers, and the number of receive errors in the receive data in the receive FIFO register, can be ascertained.
- Interrupt can be generated at each receive reading frequency end set by using the receive-reading-count-compare interrupt.

Figure 42.1 shows a block diagram of SCIFB.

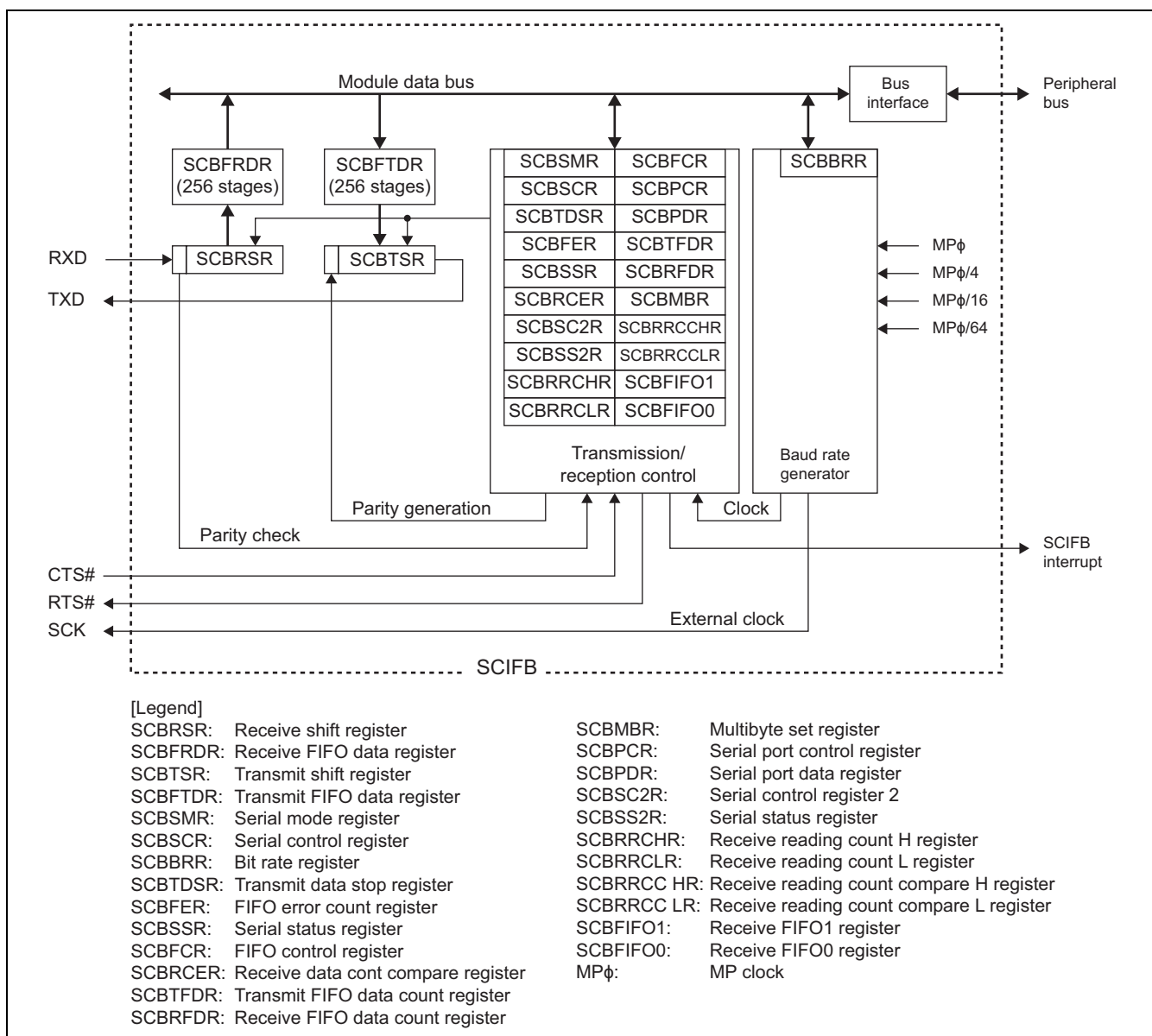


Figure 42.1 Block Diagram of SCIFB

## 42.2 Input/Output Pins

Table 42.1 shows the SCIFB pin configuration.

**Table 42.1 Channel and Pin Configuration**

Abbreviation	Input/output	Description
SCIFBn_SCK	Output	Output pin for the clock signal n
SCIFBn_RXD	Input	Input pin for data for reception n
SCIFBn_TXD	Output	Output pin for data for transmission n
SCIFBn_CTS#	Input	Input pin for the transmit enable signal n
SCIFBn_RTS#	Output	Output pin for transmit request signal n

Note: n is a channel number (n = 0 to 2).

SCK, RXD, TXD, CTS#, and RTS# are used as generic terms in the following descriptions.

## 42.3 Register Descriptions

Table 42.2 shows the SCIFB registers. Table 42.3 shows the register states in the respective processing modes.

**Table 42.2 Register Configuration**

Register Name	Abbreviation	Address	RZ/G Series Products					
			RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E		
<b>n: channel number</b>		<b>High order Address</b>						
<b>SCIFB0: 0</b>		<b>SCIFB0: H'E6C2</b>						
<b>SCIFB1: 1</b>		<b>SCIFB1: H'E6C3</b>						
<b>SCIFB2: 2</b>		<b>SCIFB2: H'E6CE</b>						
		<b>R/W</b>	<b>Access Size</b>					
Receive shift register Bn	SCBRSRn	—* <sup>3</sup>	—	√	√	√	√	
Transmit shift register Bn	SCBTSRn	—* <sup>3</sup>	—	√	√	√	√	
Serial mode register Bn	SCBSMRn	R/W	H'xxxx 0000	16	√	√	√	√
Bit rate register Bn	SCBBRRn	R/W	H'xxxx 0004	8	√	√	√	√
Serial control register Bn	SCBSCRn	R/W	H'xxxx 0008	16	√	√	√	√
Transmit data stop register Bn	SCBTDSRn	R/W	H'xxxx 000C	16	√	√	√	√
FIFO error count register Bn	SCBFERn	R	H'xxxx 0010	16	√	√	√	√
Serial status register Bn	SCBSSRn	R/W* <sup>1</sup>	H'xxxx 0014	16	√	√	√	√
FIFO control register Bn	SCBFCRn	R/W	H'xxxx 0018	16	√	√	√	√
Receive data count compare register Bn	SCBR CERn	R/W	H'xxxx 0028	16	√	√	√	√
Multibyte set register Bn	SCBMBRn	R/W	H'xxxx 002C	16	√	√	√	√
Serial port control register Bn	SCBPCRn	R/W	H'xxxx 0030	16	√	√	√	√
Serial port data register Bn	SCBPDRn	R/W	H'xxxx 0034	16	√	√	√	√
Transmit FIFO data count register Bn	SCBT FDRn	R	H'xxxx 0038	16	√	√	√	√
Receive FIFO data count register Bn	SCBR FDRn	R	H'xxxx 003C	16	√	√	√	√
Transmit FIFO data register Bn	SCBT FDRn	W	H'xxxx 0040	8	√	√	√	√
Receive FIFO data register Bn	SCBR FDRn	R	H'xxxx 0060	8	√	√	√	√
Serial control register2 Bn	SCBSC2Rn	R/W	H'xxxx 0080	16	√	√	√	√
Serial status register2 Bn	SCBSS2Rn	R/W* <sup>2</sup>	H'xxxx 0084	16	√	√	√	√
Receive reading count H register Bn	SCBRRCHRn	R/W	H'xxxx 0090	16	√	√	√	√
Receive reading count L register Bn	SCBRRCLRn	R/W	H'xxxx 0094	16	√	√	√	√
Receive reading count compare H register Bn	SCBRRCCHRn	R/W	H'xxxx 0098	16	√	√	√	√
Receive reading count compare L register Bn	SCBRRCCLRn	R/W	H'xxxx 009C	16	√	√	√	√
Receive FIFO1 register Bn	SCBFIFO1n	R	H'xxxx 00A8	8	√	√	√	√
Receive FIFO0 register Bn	SCBFIFO0n	R	H'xxxx 00AC	8	√	√	√	√

- Notes: 1. To clear the flags, only 0s can be written to bits 13, 9, 8, 7, 5, 4, 1, and 0.  
 2. To clear the flag, only 0 can be written to bit 0.  
 3. These registers cannot be accessed by the CPU.

**Table 42.3 Register States in Each Operating Mode**

<b>Register Abbreviation</b>	<b>Reset</b>	<b>Module Standby</b>
SCBSMRn	Initialized	Retained
SCBBRRn	Initialized	Retained
SCBSCRn	Initialized	Retained
SCBTDSRn	Initialized	Retained
SCBFERn	Initialized	Retained
SCBSSRn	Initialized	Retained
SCBFCRn	Initialized	Retained
SCBR CERn	Initialized	Retained
SCBMBRn	Initialized	Retained
SCBPCRn	Initialized	Retained
SCBPDRn	Undefined	Retained
SCBTFDRn	Initialized	Retained
SCBRFDRn	Initialized	Retained
SCBFTDRn	Undefined	Retained
SCBFRDRn	Undefined	Retained
SCBSC2Rn	Undefined	Retained
SCBSS2Rn	Undefined	Retained
SCBRRCHRn	Undefined	Retained
SCBRRCLRn	Undefined	Retained
SCBRRCCHRn	Undefined	Retained
SCBRRCCLRn	Undefined	Retained
SCBFIFO1n	Undefined	Retained
SCBFIFO0n	Undefined	Retained

n: Channel number (n = 0 to 2)



**42.3.1 Receive Shift Register Bn (SCBRSRn)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SCBRSR is the register used to receive serial data.

SCIFB sets serial data input from the RXD pin in SCBRSR in the order received, starting with the LSB (bit 0), and converts it to parallel data. When one byte of data has been received, it is automatically transferred to SCBFRDR.

SCBRSR cannot be directly read from or written to by the CPU.

**42.3.2 Transmit Shift Register Bn (SCBTSRn)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SCBTSR is the register used to transmit serial data.

To perform serial data transmission, SCIFB first transfers a transmit data from SCBFTDR to SCBTSR, and then sends the data to the TXD pin starting with the LSB (bit 0).

When transmission of one byte is completed, the next transmit data is transferred from SCBFTDR to SCBTSR, and transmission starts automatically.

SCBTSR cannot be directly read from or written to by the CPU.

### 42.3.3 Serial Mode Register Bn (SCBSMRn)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SCBSMR is a 16-bit readable/writable register used to set an SCIFB's serial transfer format and select the baud rate generator clock source and the sampling rate.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	CKEDG	—	SRC[2:0]		C/A#	CHR	PE	O/E	STOP	—	CKS[1:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12	CKEDG	0	R/W	Transmit/Receive Clock Edge Select Selects the clock edge at which the serial data is output in clocked synchronous mode. 0: Serial data is transmitted at the falling edge of output clock. Serial data is received at the rising edge of output clock. 1: Serial data is transmitted at the rising edge of output clock. Serial data is received at the falling edge of output clock.
11	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
10 to 8	SRC[2:0]	000	R/W	Sampling Control This bit setting is valid only in asynchronous mode. These bits select the sampling rate. 000: Sampling rate 1/16 001: Sampling rate 1/5* 010: Sampling rate 1/7 011: Sampling rate 1/11 100: Sampling rate 1/13 101: Sampling rate 1/17 110: Sampling rate 1/19 111: Sampling rate 1/27 Note: * In asynchronous mode, when the sampling rate is 1/5, first received data may become invalid. To avoid this problem, wait more than 1 serial data time (1bit time x serial data number) after setting SCBSCR.RE=1, or use sampling rate other than 1/5.
7	C/A#	0	R/W	Communication Mode Selects asynchronous mode or clocked synchronous mode as the SCIFB operating mode. 0: Asynchronous mode 1: Clocked synchronous mode

Bit	Bit Name	Initial Value	R/W	Description
6	CHR	0	R/W	<p>Character Length</p> <p>This bit setting is valid only in asynchronous mode.</p> <p>Selects 7 or 8 bits as the data length.</p> <p>0: 8-bit data 1: 7-bit data*</p> <p>Note: * When the 7-bit character is selected, the MSB (bit 7) in SCBFTDR is not transmitted.</p>
5	PE	0	R/W	<p>Parity Enable</p> <p>This bit setting is valid only in asynchronous mode.</p> <p>Selects whether or not parity bit addition is performed in transmission, and parity bit checking in reception.</p> <p>0: Parity bit addition and checking disabled 1: Parity bit addition and checking enabled*</p> <p>Note: * When the PE bit is set to 1, the parity (even or odd) specified by the O/E bit is added to transmit data before transmission. In reception, the parity bit is checked for the parity (even or odd) specified by the O/E bit.</p>
4	O/E	0	R/W	<p>Parity Mode</p> <p>This bit setting is valid only in asynchronous mode.</p> <p>Selects either even or odd parity for use in parity addition and checking. The O/E bit setting is only valid when the PE bit is set to 1, enabling parity bit addition and checking. The O/E bit setting is invalid when parity addition and checking are disabled.</p> <p>0: Even parity*<sup>1</sup> 1: Odd parity*<sup>2</sup></p> <p>Notes: 1. When even parity is set, parity bit addition is performed in transmission so that the total number of 1-bits in the transmit character plus the parity bit is even. In reception, a check is performed to see if the total number of 1-bits in the receive character plus the parity bit is even.</p> <p>2. When odd parity is set, parity bit addition is performed in transmission so that the total number of 1-bits in the transmit character plus the parity bit is odd. In reception, a check is performed to see if the total number of 1-bits in the receive character plus the parity bit is odd.</p>
3	STOP	0	R/W	<p>Stop Bit Length</p> <p>This bit setting is valid only in asynchronous mode.</p> <p>Selects 1 or 2 bits as the stop bit length. In reception, only the first stop bit is checked, regardless of the STOP bit setting. If the second stop bit is 1, it is treated as a stop bit; if it is 0, it is treated as the start bit of the next transmit character.</p> <p>0: 1 stop bit*<sup>1</sup> 1: 2 stop bits*<sup>2</sup></p> <p>Notes: 1. In transmission, a single logic-1 bit (stop bit) is added to the end of a transmit character before it is sent.</p> <p>2. In transmission, two logic-1 bits (stop bits) are added to the end of a transmit character before it is sent.</p>
2	—	0	R	<p>Reserved</p> <p>This bit is always read as 0. The write value should always be 0.</p>

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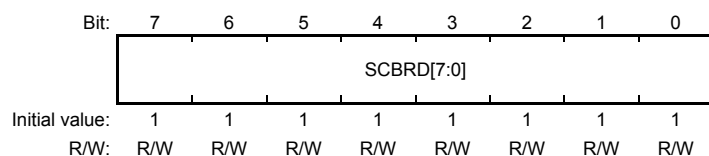
Bit	Bit Name	Initial Value	R/W	Description
1, 0	CKS[1:0]	00	R/W	Clock Select Select the clock source of the internal baud-rate generator. 00: MP $\phi$ 01: MP $\phi$ /4 10: MP $\phi$ /16 11: MP $\phi$ /64 Note: MP $\phi$ : MP clock

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### 42.3.4 Bit Rate Register Bn (SCBBRRn)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SCBBRR is an 8-bit readable/writable register that sets the serial transfer bit rate in accordance with the baud rate generator operating clock selected by bits CKS[1:0] in SCBSMR.



Bit	Bit Name	Initial Value	R/W	Description
7 to 0	SCBRD[7:0]	H'FF	R/W	Bit Rate $0 \leq \text{SCBRD} \leq 255$ (asynchronous) $1 \leq \text{SCBRD} \leq 255$ (clocked synchronous)

The SCBBRR setting is found by using the following equations.

#### (1) Asynchronous Mode:

- When the sampling rate is 1/16,  

$$N = \{ \text{MP}\phi / (16 \times 2^{2n} \times B) \} \times 10^6 - 1$$
- When the sampling rate is 1/5,  

$$N = \{ \text{MP}\phi / (5 \times 2^{2n} \times B) \} \times 10^6 - 1$$
- When the sampling rate is 1/11,  

$$N = \{ \text{MP}\phi / (11 \times 2^{2n} \times B) \} \times 10^6 - 1$$
- When the sampling rate is 1/13,  

$$N = \{ \text{MP}\phi / (13 \times 2^{2n} \times B) \} \times 10^6 - 1$$
- When the sampling rate is 1/27,  

$$N = \{ \text{MP}\phi / (27 \times 2^{2n} \times B) \} \times 10^6 - 1$$

#### (2) Clocked Synchronous Mode:

$$N = \{ \text{MP}\phi / (2 \times 2^{2n} \times B) \} \times 10^6 - 1$$

- Where
- B: Bit rate (bits/s)
  - N: SCBBRR setting for baud rate generator  
Asynchronous mode ( $0 \leq N \leq 255$ )  
Clocked synchronous mode ( $1 \leq N \leq 255$ )
  - MP $\phi$ : MP clock frequency (MHz)
  - n: Baud rate generator input clock ( $n = 0$  to 3)  
(See the table below for the relation between n and the clock.)

**Table 42.4 SCBSMR Setting**

n	Clock	SCBSMR Setting
		CKS[1:0]
0	MP $\phi$	B'00
1	MP $\phi$ /4	B'01
2	MP $\phi$ /16	B'10
3	MP $\phi$ /64	B'11

The bit rate error in asynchronous mode is found by using the following equations.

When the sampling rate is 1/16,

$$\text{Error (\%)} = \{ \{ \text{MP}\phi / ((N + 1) \times 16 \times 2^{2n} \times B) \} \times 10^6 - 1 \} \times 100$$

When the sampling rate is 1/5,

$$\text{Error (\%)} = \{ \{ \text{MP}\phi / ((N + 1) \times 5 \times 2^{2n} \times B) \} \times 10^6 - 1 \} \times 100$$

When the sampling rate is 1/11,

$$\text{Error (\%)} = \{ \{ \text{MP}\phi / ((N + 1) \times 11 \times 2^{2n} \times B) \} \times 10^6 - 1 \} \times 100$$

When the sampling rate is 1/13,

$$\text{Error (\%)} = \{ \{ \text{MP}\phi / ((N + 1) \times 13 \times 2^{2n} \times B) \} \times 10^6 - 1 \} \times 100$$

When the sampling rate is 1/27,

$$\text{Error (\%)} = \{ \{ \text{MP}\phi / ((N + 1) \times 27 \times 2^{2n} \times B) \} \times 10^6 - 1 \} \times 100$$

### 42.3.5 Serial Control Register Bn (SCBSCRn)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SCBSCR is a 16-bit readable/writable register that enables or disables SCIFB transfer operations and interrupt requests, and selects the clock source for transmission and reception.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TDRQE	RDRQE	RCEE	TENDE	TSIE	ERIE	BRIE	DRIE	TIE	RIE	TE	RE	—	—	—	CKE0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	TDRQE	0	R/W	<p>Transmit Data Transfer Request Enable</p> <p>Switches the transmit-FIFO-data-empty interrupt or DMA transfer request when TIE = 1 and the transmit FIFO data empty occurs.</p> <p>0: Interrupt request to CPU is issued.</p> <p>1: Transmit data transfer request to DMAC is issued.</p>
14	RDRQE	0	R/W	<p>Receive Data Transfer Request Enable</p> <p>Switches the receive-FIFO-data-full interrupt or DMA transfer request when RIE = 1 and the receive FIFO data full occurs.</p> <p>0: Interrupt request to CPU is issued.</p> <p>1: Receive data transfer request to DMAC is issued.</p>
13	RCEE	0	R/W	<p>Receive Data Count Compare Interrupt Enable</p> <p>Generates an interrupt when the receive data count comparison counter matches the current receive data count.</p> <p>0: Receive-data-count-compare interrupt disabled*</p> <p>1: Receive-data-count-compare interrupt enabled</p> <p>Note: * This interrupt request is cleared by clearing the RCEF flag to 0 after reading 1 from it or clearing the RCEE bit to 0.</p>
12	TENDPOSE	0	R/W	<p>Transmit End Interrupt Enable</p> <p>Enables or disables generation of a transmit-end interrupt when the TENDPOS flag in SCBSSR is set to 1.</p> <p>0: Transmit-end interrupt disabled*</p> <p>1: Transmit-end interrupt enabled</p> <p>Note: * This interrupt request is cleared by clearing the TENDPOS flag to 0 after reading 1.</p>
11	TSIE	0	R/W	<p>Transmit Data Stop Interrupt Enable</p> <p>Enables or disables generation of a transmit-data-stop interrupt when the TSE bit in SCBFCR is enabled and the TSF flag in SCBSSR is set to 1.</p> <p>0: Transmit-data-stop interrupt disabled*</p> <p>1: Transmit-data-stop interrupt enabled</p> <p>Note: * The TDI interrupt request is cleared by clearing the TSF flag to 0 after reading 1 from it or clearing the TSIE bit to 0.</p>

Bit	Bit Name	Initial Value	R/W	Description
10	ERIE	0	R/W	<p>Receive Error Interrupt Enable</p> <p>Enables or disables generation of a receive-error (framing or parity error) interrupt when the ER flag in SCBSSR is set to 1.</p> <p>0: Receive-error interrupt disabled*</p> <p>1: Receive-error interrupt enabled</p> <p>Note: * The ERI interrupt request is cleared by clearing the ER flag to 0 after reading 1 from it or clearing the ERIE bit to 0.</p>
9	BRIE	0	R/W	<p>Break Interrupt Enable</p> <p>Enables or disables generation of a break-receive interrupt when the BRK flag in SCBSSR is set to 1.</p> <p>0: Break-receive interrupt disabled*</p> <p>1: Break-receive interrupt enabled</p> <p>Note: * The BRI interrupt request is cleared by clearing the BRK flag to 0 after reading 1 from it or clearing the BRIE bit to 0.</p>
8	DRIE	0	R/W	<p>Receive Data Ready Interrupt Enable</p> <p>Enables or disables generation of a receive-data-ready interrupt when the DR flag in SCBSSR is set to 1.</p> <p>0: Receive-data-ready interrupt disabled*</p> <p>1: Receive-data-ready interrupt enabled</p> <p>Note: * The DRI interrupt request is cleared by clearing the DR flag to 0 after reading 1 from it or clearing the DRIE bit to 0.</p>
7	TIE	0	R/W	<p>Transmit Interrupt Enable</p> <p>Enables or disables generation of a transmit-FIFO-data-empty interrupt request when the TDFE flag in SCBSSR is set to 1.</p> <p>0: Transmit-FIFO-data-empty interrupt request disabled*</p> <p>1: Transmit-FIFO-data-empty interrupt request enabled</p> <p>Note: * This interrupt request is cleared by writing transmit data exceeding the transmit trigger set number to SCBFTDR, reading 1 from the TDFE flag, then clearing it to 0, or by clearing the TIE bit to 0.</p>
6	RIE	0	R/W	<p>Receive Interrupt Enable</p> <p>Enables or disables generation of a receive-FIFO-data-full interrupt request when the RDF flag in SCBSSR is set to 1.</p> <p>0: Receive-FIFO-data-full interrupt request disabled*</p> <p>1: Receive-FIFO-data-full interrupt request enabled</p> <p>Note: * This interrupt request is cleared by reading 1 from the RDF flag, then clearing the flag to 0, or by clearing the RIE bit to 0.</p>
5	TE	0	R/W	<p>Transmit Enable</p> <p>Enables or disables the start of serial transmission by SCIFB.</p> <p>0: Transmission disabled</p> <p>1: Transmission enabled*</p> <p>Note: * Make SCBSMR and SCBFCR settings, decide the transmit format, and reset the transmit FIFO before setting the TE bit to 1.</p>

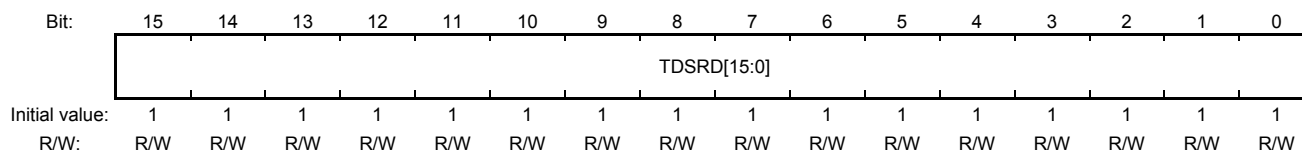


Bit	Bit Name	Initial Value	R/W	Description
4	RE	0	R/W	<p>Receive Enable</p> <p>Enables or disables the start of serial reception by SCIFB.</p> <p>0: Reception disabled*<sup>1</sup></p> <p>1: Reception enabled*<sup>2</sup></p> <p>Notes: 1. Clearing the RE bit to 0 does not affect the DR, ER, BRK, RDF, FER, PER, and ORER flags, which retain their state.</p> <p>2. Make SCBSMR and SCBFCR settings, decide the receive format, and reset the receive FIFO before setting the RE bit to 1.</p>
3 to 1	—	All 0	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>
0	CKE0	0	R/W	<p>Clock Enable</p> <p>Enables or disables the clock output from the SCK pin. The CKE0 bit must be set before determining the SCIFB operating mode with SCBSMR.</p> <p>0: SCK pin disabled*<sup>1</sup></p> <p>1: Clock output from SCK*<sup>2</sup></p> <p>Notes: 1. Even if this bit is 0, the SCK pin outputs data specified by SCBPDRn[2].SCKD, if SCBPCRn[2].SCKC is 1.</p> <p>2. In clocked synchronous mode, the SCK pin outputs a clock with the same frequency as the bit rate.</p>

#### 42.3.6 Transmit Data Stop Register Bn (SCBTDSRn)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SCBTDSR is a 16-bit readable/writable register that sets the number of transmit data bytes. SCBTDSR is valid only when the TSE bit in SCBFCR is enabled. Transmit operation is stopped when the number of data bytes set in SCBTDSR is transmitted. The setting value should be H'0000 (one byte) to H'FFFF (65536 bytes). SCBTDSR is initialized to H'FFFF.

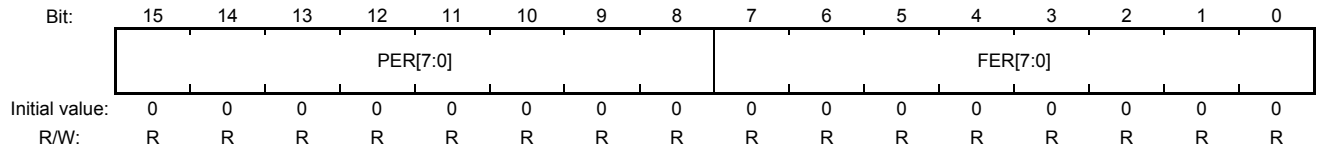


Bit	Bit Name	Initial Value	R/W	Description
15 to 0	TDSRD[15:0]	H'FFFF	R/W	Transmit Data Stop Setting

**42.3.7 FIFO Error Count Register Bn (SCBFERn)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SCBFER is a 16-bit read-only register that indicates the number of receive errors (framing errors and parity errors).



Bit	Bit Name	Initial Value	R/W	Description
15 to 8	PER[7:0]	H'00	R	<p>Parity Error Count</p> <p>These bits indicate the number of data in which parity errors are generated, in receive data stored in SCBFRDR.</p> <p>After the ER bit in SCBSSR is set, the value of bits PER7 to PER0 indicates the number of data in which parity errors are generated.</p> <p>When all 256 bytes of receive data in SCBFRDR have parity errors, these bits indicate 0.</p>
7 to 0	FER[7:0]	H'00	R	<p>Framing Error Count</p> <p>These bits indicate the number of data in which framing errors are generated, in receive data stored in SCBFRDR.</p> <p>After the ER bit in SCBSSR is set, the value of bits FER7 to FER0 indicates the number of data in which framing errors are generated.</p> <p>When all 256 bytes of receive data in SCBFRDR have framing errors, these bits indicate 0.</p>

### 42.3.8 Serial Status Register Bn (SCBSSRn)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SCBSSR is a 16-bit readable/writable register that indicates the SCIFB status.

However, 1 cannot be written to the RCEF, TENDPOS, ORER, TSF, ER, TDFE, BRK, RDF, and DR flags. Before these flags can be cleared to 0, they must first be read as 1. The TEND, FER, and PER flags are read-only flags and cannot be modified.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	RCEF	TEND POS	—	—	ORER	TSF	ER	TEND	TDFE	BRK	FER	PER	RDF	DR
Initial value:	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0
R/W:	R	R	R/(W)*	R/(W)*	R	R	R/(W)*	R/(W)*	R/(W)*	R	R/(W)*	R/(W)*	R	R	R/(W)*	R/(W)*

Bit	Bit Name	Initial Value	R/W	Description
15, 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13	RCEF	0	R/(W)*	Receive Data Count Match Indicates that the receive data count matches the receive data count comparison counter. 0: Receive data count does not match the receive data count comparison counter. [Clearing conditions] <ul style="list-style-type: none"> <li>Power-on reset or manual reset</li> <li>When 0 is written to RCEF after reading RCEF = 1</li> </ul> 1: Receive data count matches the receive data count comparison counter.* [Setting condition] <ul style="list-style-type: none"> <li>When the receive data count matches the counter value</li> </ul> Note: * Enable this bit by setting RCE bit in SCBFRC to 1.
12	TENDPOS	0	R/(W)*	Transmit End Detect Indicates that the transmission ends. 0: Transmit end has not been detected. [Clearing conditions] <ul style="list-style-type: none"> <li>Power-on reset or manual reset</li> <li>When 0 is written to TENDPOS after reading TENDPOS = 1</li> </ul> 1: The TEND flag in SCBSSR is set to 1 [Setting condition] <ul style="list-style-type: none"> <li>When the TEND flag in SCBSSR is set to 1.</li> </ul>
11, 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
9	ORER	0	R/(W)*	<p>Overrun Error</p> <p>Indicates that an overrun error occurred during reception.</p> <p>This bit is valid only in asynchronous mode.</p> <p>0: Reception is in progress or has been completed normally.*<sup>1</sup></p> <p>[Clearing conditions]</p> <ul style="list-style-type: none"> <li>Power-on reset or manual reset</li> <li>When 0 is written to ORER after reading ORER = 1</li> </ul> <p>1: An overrun error occurred during reception.*<sup>2</sup></p> <p>[Setting condition]</p> <ul style="list-style-type: none"> <li>When serial data reception is completed while receive FIFO is full</li> </ul> <p>Notes: 1. The ORER flag is not affected and retains its previous state when the RE bit in SCBSCR is cleared to 0.</p> <p>2. The receive data prior to the overrun error is retained in SCBFRDR, and the data received subsequently is lost. Serial data reception cannot be continued with the ORER flag set to 1.</p>
8	TSF	0	R/(W)*	<p>Transmit Data Stop</p> <p>Indicates that the number of transmit data matches the value of SCBTDSR.</p> <p>This bit is valid only in asynchronous mode.</p> <p>0: The number of transmit data does not match the SCBTDSR value.</p> <p>[Clearing conditions]</p> <ul style="list-style-type: none"> <li>Power-on reset or manual reset</li> <li>When 0 is written to TSF after reading TSF = 1</li> </ul> <p>1: The number of transmit data matches the SCBTDSR value.</p>

Bit	Bit Name	Initial Value	R/W	Description
7	ER	0	R/(W)*	<p>Receive Error</p> <p>Indicates that a framing error or parity error occurred during reception.*1 This bit is valid only in asynchronous mode.</p> <p>0: No framing error or parity error occurred during reception.</p> <p>[Clearing conditions]</p> <ul style="list-style-type: none"> <li>• Power-on reset or manual reset</li> <li>• When 0 is written to ER after reading ER = 1</li> </ul> <p>1: A framing error or parity error occurred during reception.</p> <p>[Setting conditions]</p> <ul style="list-style-type: none"> <li>• When the SCIFB checks whether the stop bit at the end of the receive data is 1 when reception ends, and the stop bit is 0*2</li> <li>• When, in reception, the number of logic-1 bits in the receive data and in the parity bit does not match the parity setting (even or odd) specified by the O/E bit in SCBSMR</li> </ul> <p>Notes: 1. The ER flag is not affected and retains its previous state when the RE bit in SCBSCR is cleared to 0. When a receive error occurs, the receive data is still transferred to SCBFRDR, and reception continues. The FER and PER bits in SCBSSR can be used to determine whether there is a receive error in the data read from SCBFRDR.</p> <p>2. When the stop-bit length is 2 bits, only the first stop bit is checked for a value of 1 and the second stop bit is not checked.</p>
6	TEND	1	R	<p>Transmit End</p> <p>Indicates that there is no valid data in SCBFTDR when the last bit of the transmit character is sent and that transmission has been completed.</p> <p>0: Transmission is in progress.</p> <p>[Clearing condition]</p> <ul style="list-style-type: none"> <li>• When data is written to SCBFTDR</li> </ul> <p>1: Transmission has been completed.</p> <p>[Setting condition]</p> <ul style="list-style-type: none"> <li>• When there is no transmit data in SCBFTDR during transmission of a 1-byte serial transmit character</li> </ul>

Bit	Bit Name	Initial Value	R/W	Description
5	TDFE	1	R/(W)*	<p>Transmit FIFO Data Empty</p> <p>Indicates that data has been transferred from SCBFTDR to SCBTSR, the number of data bytes in SCBFTDR has fallen to or below the transmit trigger data number set by bits TTRG[1:0] in SCBFCR, and new transmit data can be written to SCBFTDR.</p> <p>0: A number of transmit data bytes exceeding the transmit trigger set number have been written to SCBFTDR.</p> <p>[Clearing condition]</p> <ul style="list-style-type: none"> <li>When transmit data exceeding the transmit trigger set number is written to SCBFTDR, and 0 is written to TDFE after reading TDFE = 1</li> </ul> <p>1: The number of transmit data bytes in SCBFTDR is equal to or less than the transmit trigger set number.</p> <p>[Setting conditions]</p> <ul style="list-style-type: none"> <li>Power-on reset or manual reset</li> <li>When the number of SCBFTDR transmit data bytes falls to or below the transmit trigger set number after a transmit operation*</li> </ul> <p>Note: * As SCBFTDR is a 256-byte FIFO register, the maximum number of bytes that can be written when TDFE = 1 is 256 – (transmit trigger set number). Data written in excess of this will be ignored. The number of data bytes in SCBFTDR is indicated by SCBTFDR.</p>
4	BRK	0	R/(W)*	<p>Break Detect</p> <p>Indicates that a receive data break signal has been detected. This bit is valid only in asynchronous mode.</p> <p>0: A break signal has not been received.</p> <p>[Clearing conditions]</p> <ul style="list-style-type: none"> <li>Power-on reset or manual reset</li> <li>When 0 is written to BRK after reading BRK = 1</li> </ul> <p>1: A break signal has been received.*</p> <p>[Setting condition]</p> <ul style="list-style-type: none"> <li>When data with a framing error is received, followed by the space 0 level (low level) for at least one frame length</li> </ul> <p>Note: * When a break is detected, the receive data (H'00) following the detection is not transferred to SCBFRDR. When the break ends and the receive signal returns to mark 1, receive data transfer is resumed.</p>
3	FER	0	R	<p>Framing Error</p> <p>Indicates a framing error in the data read from SCBFRDR. This bit is valid only in asynchronous mode.</p> <p>0: There is no framing error in the receive data read from SCBFRDR.</p> <p>[Clearing conditions]</p> <ul style="list-style-type: none"> <li>Power-on reset or manual reset</li> <li>When there is no framing error in SCBFRDR read data</li> </ul> <p>1: There is a framing error in the receive data read from SCBFRDR.</p> <p>[Setting condition]</p> <ul style="list-style-type: none"> <li>When there is a framing error in SCBFRDR read data</li> </ul>

Bit	Bit Name	Initial Value	R/W	Description
2	PER	0	R	<p>Parity Error</p> <p>Indicates a parity error in the data read from SCBFRDR. This bit is valid only in asynchronous mode.</p> <p>0: There is no parity error in the receive data read from SCBFRDR. [Clearing conditions]</p> <ul style="list-style-type: none"> <li>Power-on reset or manual reset</li> <li>When there is no parity error in SCBFRDR read data</li> </ul> <p>1: There is a parity error in the receive data read from SCBFRDR. [Setting condition]</p> <p>When there is a parity error in SCBFRDR read data</p>
1	RDF	0	R/(W)*	<p>Receive FIFO Data Full</p> <p>Indicates that the received data has been transferred from SCBRSR to SCBFRDR, and the number of receive data bytes in SCBFRDR is equal to or greater than the receive trigger number set by bits RTRG[1:0] in SCBFCR.</p> <p>0: The number of receive data bytes in SCBFRDR is less than the receive trigger set number. [Clearing conditions]</p> <ul style="list-style-type: none"> <li>Power-on reset or manual reset</li> <li>When SCBFRDR is read until the number of receive data bytes in SCBFRDR falls below the receive trigger set number, and 0 is written to RDF after reading RDF = 1</li> </ul> <p>1: The number of receive data bytes in SCBFRDR is equal to or greater than the receive trigger set number. [Setting condition]</p> <ul style="list-style-type: none"> <li>When SCBFRDR contains at least the receive trigger set number of receive data bytes*</li> </ul> <p>Note: * SCBFRDR is a 256-byte FIFO register. When RDF = 1, at least the receive trigger set number of data bytes can be read. If data is read when SCBFRDR is empty, an undefined value will be returned. The number of receive data bytes in SCBFRDR is indicated by SCBRFDR.</p>

Bit	Bit Name	Initial Value	R/W	Description
0	DR	0	R/(W) *	<p>Receive Data Ready</p> <p>Indicates that there are data bytes fewer than the receive trigger set number in SCBFRDR, and no further data will arrive at least 15 etu after the stop bit of the last data received.</p> <p>This bit is valid only in asynchronous mode.</p> <p>0: Reception is in progress or has ended normally and no receive data is left in SCBFRDR.</p> <p>[Clearing conditions]</p> <ul style="list-style-type: none"> <li>• Power-on reset or manual reset</li> <li>• When all the receive data in SCBFRDR has been read, and 0 is written to DR after reading DR = 1</li> </ul> <p>1: No further receive data has arrived.</p> <p>[Setting condition]</p> <ul style="list-style-type: none"> <li>• When SCBFRDR contains data bytes fewer than the receive trigger set number, and no further data will arrive at least 15 etu after the stop bit of the last data received*</li> </ul> <p>Note: * Corresponds to 1.5 frame time in 8-bit one-stop-bit format. etu: Elementary time unit (time for transfer of 1 bit)</p>

Note: \* Only 0 can be written for flag clearing.



### 42.3.9 FIFO Control Register Bn (SCBFCRn)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SCBFCR is a 16-bit readable/writable register that clears all data and sets the trigger data number for the transmit and receive FIFO registers. The register also contains a loopback test enable bit.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TSE	TCRST	RCE	RCRST	—	RSTRG[2:0]			RTRG[1:0]		TTRG[1:0]		MCE	TFRST	RFRST	LOOP
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	TSE	0	R/W	Transmit Data Stop Enable The setting is valid only in asynchronous mode. Enables or disables the transmit data stop function. 0: Transmit data stop function disabled 1: Transmit data stop function enabled
14	TCRST	0	R/W	Transmit Count Reset The setting is valid only in asynchronous mode. Clears the transmit count to 0. This bit is valid only when the transmit data stop function is used. 0: Transmit count reset disabled* 1: Transmit count reset enabled (clearing to 0) Note: * The transmit count is reset (clearing to 0) by a power-on reset or manual reset.
13	RCE	0	R/W	Receive Data Count Comparison Enable Enables or disables the comparison of receive data count. 0: Comparison of receive data count disabled 1: Comparison of receive data count enabled
12	RCRST	0	R/W	Receive Count Reset Clears the receive count to 0. This bit is valid only when the receive data count comparison function is used. 0: Receive count reset disabled* 1: Receive count reset enabled (clearing to 0) Note: * The receive count is reset (clearing to 0) by a power-on reset or manual reset.
11	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

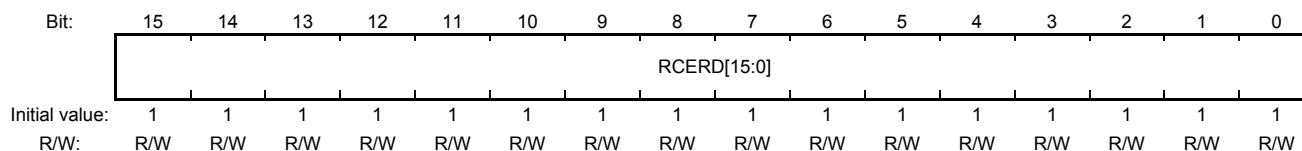
Bit	Bit Name	Initial Value	R/W	Description
10 to 8	RSTRG[2:0]	000	R/W	<p>RTS# Output Active Trigger</p> <p>This bit setting is valid only in asynchronous mode.</p> <p>The RTS# signal becomes high when the number of receive data stored in SCBFRDR reaches the trigger set number shown below.</p> <p>000: 255 001: 1 010: 32 011: 64 100: 128 101: 192 110: 224 111: 240</p>
7, 6	RTRG[1:0]	00	R/W	<p>Receive FIFO Data Number Trigger</p> <p>Set the number of receive data bytes that sets the RDF flag in SCBSSR.</p> <p>The RDF flag is set when the number of receive data bytes in SCBFRDR reaches the trigger set number shown below.</p> <p>00: 1 01: 16 10: 32 11: 48</p> <p>In multibyte transfer mode, a transfer request is made to the DMAC when the number of receive data bytes in SCBFRDR reaches the trigger set number shown below. (The RDF flag is undefined.)</p> <p>00: Reserved 01: 32 10: 16 11: 1</p>
5, 4	TTRG[1:0]	00	R/W	<p>Transmit FIFO Data Number Trigger</p> <p>Set the number of remaining transmit data bytes that sets the TDFE flag in SCBSSR.</p> <p>The TDFE flag is set when, as the result of a transmit operation, the number of transmit data bytes in SCBFTDR falls to or below the trigger set number shown below.</p> <p>00: 32 (32) 01: 16 (48) 10: 2 (62) 11: 0 (64)</p> <p>In multibyte transfer mode, a transfer request is made to the DMAC when the number of transmit data bytes in SCBFTDR falls to or below the trigger set number shown below. (The TDFE flag is undefined.)</p> <p>00: Reserved 01: 224 (32) 10: 240 (16) 11: 255 (1)</p> <p>Note: The values in parentheses are the number of empty bytes in SCBFTDR when the flag is set.</p>

Bit	Bit Name	Initial Value	R/W	Description
3	MCE	0	R/W	<p>Modem Control Enable</p> <p>This bit setting is valid only in asynchronous mode.</p> <p>Enables the CTS# and RTS# modem control signals.</p> <p>0: Modem signals disabled*</p> <p>1: Modem signals enabled</p> <p>Note: * CTS# is fixed at active low regardless of the input value, and RTS# output is also fixed at 0.</p>
2	TFRST	0	R/W	<p>Transmit FIFO Data Register Reset</p> <p>Invalidates the transmit data in SCBFTDR and resets it to the empty state.</p> <p>0: Reset operation disabled*</p> <p>1: Reset operation enabled</p> <p>Note: * A reset operation is performed at a power-on reset or manual reset.</p>
1	RFRST	0	R/W	<p>Receive FIFO Data Register Reset</p> <p>Invalidates the receive data in SCBFRDR and resets it to the empty state.</p> <p>0: Reset operation disabled*</p> <p>1: Reset operation enabled</p> <p>Note: * A reset operation is performed at a power-on reset or manual reset.</p>
0	LOOP	0	R/W	<p>Loopback Test</p> <p>Internally connects the transmit output pin (TXD) to receive input pin (RXD) and RTS# pin to CTS# pin, enabling loopback testing.</p> <p>0: Loopback test disabled</p> <p>1: Loopback test enabled</p>

**42.3.10 Receive Data Count Compare Register Bn (SCBRCERn)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SCBRCER is a 16-bit readable/writable register that sets the number of receive data bytes. SCBRCER is valid only when the RCE bit in SCBFCR is set to 1 (enabled). The data reception stops when the number of receive data bytes reaches the value of this register. A value between H'0000 (1 byte) to H'FFFF (65536 bytes) can be set. SCBRCER is initialized to H'FFFF.



Bit	Bit Name	Initial Value	R/W	Description
15 to 0	RCERD[15:0]	H'FFFF	R/W	Receive Data Stop

### 42.3.11 Multibyte Set Register Bn (SCBMBRn)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SCBMBR is a 16-bit readable/writable register for multibyte transfer setting. Settings for transmission in SCBMBR is valid when the TDRQE bit in SCBSCR is set to 1, and settings for reception is valid when the RDRQE bit in SCBSCR is set to 1.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ADD REQ	—	—	—	—	—	—	—	—	—	—	—	RCECR ON	—	MBR ON	MBT ON
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	ADDREQ	0	R/W	Enables or disables receive data transfer until the receive FIFO data count is decreased to 0. 0: Receive data transfer disabled until the receive FIFO data count is decreased to 0. 1: Receive data transfer enabled until the receive FIFO data count is decreased to 0.
14 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3	RCECRON	0	R/W	Enables or disables receive data transfer in conjunction with the RCEF bit in SCBSSR. Receive data transfer requests are made until the receive FIFO data count is decreased to 0. 0: Receive data transfer in conjunction with RCEF in SCBSSR enabled 1: Receive data transfer in conjunction with RCEF in SCBSSR disabled
2	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
1	MBRON	0	R/W	Enables or disables multibyte receive data transfer 0: Multibyte receive data transfer disabled 1: Multibyte receive data transfer enabled
0	MBTON	0	R/W	Enables or disables multibyte transmit data transfer 0: Multibyte transmit data transfer disabled 1: Multibyte transmit data transfer enabled

### 42.3.12 Serial Port Control Register Bn (SCBPCRn)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SCBPCR is a 16 bit readable/writable register. This register specifies whether the TXD, SCK and RTS# pins function as output ports with fixed values specified by SCBPDRn, or as the TXD, SCK and RTS# pins, respectively. It also specifies whether the RXD and CTS# pins function as input ports for general purpose, or as RXD and CTS# pins, respectively.

The initial value of this register is H'0000. This register function is valid only when the SCIFB pin function is selected through the pin function controller (PFC).

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	RTSC	CTSC	SCKC	RXDC	TXDC
Initial value:	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	RTSC	1	R/W	Selects the RTS# pin function. 0: The RTS# pin functions as the RTS# pin. 1: The RTS# pin functions as an output port.
3	CTSC	0	R/W	Selects the CTS# pin function. 0: The CTS# pin functions as the CTS# pin. 1: The CTS# pin functions as an input port.
2	SCKC	1	R/W	Selects the SCK pin function. 0: The SCK pin functions as the SCK pin. 1: The SCK pin functions as an output port.
1	RXDC	0	R/W	Selects the RXD pin function. 0: The RXD pin functions as the RXD pin. 1: The RXD pin functions as an input port.
0	TXDC	0	R/W	Selects the TXD pin function. 0: The TXD pin functions as the TXD pin. 1: The TXD pin functions as an output port.

### 42.3.13 Serial Port Data Register Bn (SCBPDRn)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SCBPDR is a 16-bit readable/writable register. This register specifies data output to the TXD, SCK and RTS# pins when the SCIFB pin function is selected by SCBPCR. It also specifies the pin level of the RXD and CTS# pins.

This register function is valid only when the SCIFB pin function is selected through the pin function controller (PFC).

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	RTSD	CTSD	SCKD	RXDD	TXDD
Initial value:	0	0	0	0	0	0	0	0	0	0	0	1	—	0	—	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R/W	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	RTSD	1	R/W	Specifies data output to the RTS# pin. 0: Outputs 0. 1: Outputs 1.
3	CTSD	Undefined	R	Specifies the CTS# pin level. 0: CTS# pin level is 0. 1: CTS# pin level is 1. This bit is valid only when SCBFCRn[3].MCE is 1, or SCBPCRn[3].CTSC is 1.
2	SCKD	0	R/W	Specifies data output to the SCK pin. 0: Outputs 0. 1: Outputs 1.
1	RXDD	Undefined	R	Specifies the RXD pin level. 0: RXD pin level is 0. 1: RXD pin level is 1. This bit is valid only when SCBSCRn[4].RE is 1, or SCBPCRn[1].RXDC is 1.
0	TXDD	0	R/W	Specifies data output to the TXD pin. 0: Outputs 0. 1: Outputs 1.

### 42.3.14 Transmit FIFO Data Count Register Bn (SCBTFDRn)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SCBTFDR is a 16-bit read-only register that indicates the number of data bytes stored in SCBFTDR. The T8 to T0 bits indicate the number of transmit data bytes in SCBFTDR.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	T[8:0]								
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8 to 0	T[8:0]	H'000	R	Indicate the number of data bytes remaining in SCBFTDR. H'000 shows that SCBFTDR contains no transmit data, and H'100 shows that SCBFTDR is filled with transmit data.

### 42.3.15 Receive FIFO Data Count Register Bn (SCBRFDRn)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SCBRFDR is a 16-bit read-only register that indicates the number of data bytes stored in SCBFRDR. The R8 to R0 bits indicate the number of receive data bytes in SCBFRDR.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	R[8:0]								
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8 to 0	R[8:0]	H'000	R	Indicate the number of data bytes remaining in SCBFRDR. H'000 shows that SCBFRDR contains no receive data, and H'100 shows that SCBFRDR is filled with receive data.

### 42.3.16 Transmit FIFO Data Register Bn (SCBFTDRn)

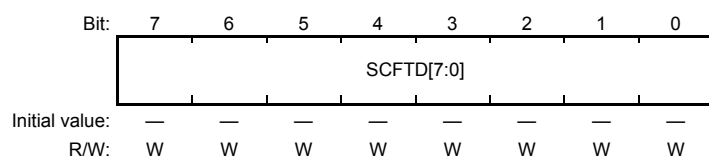
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SCBFTDR is an 8-bit 256-stage FIFO data register that stores data for serial transmission.

If SCBTSR is empty when transmit data has been written to SCBFTDR, the SCIFB transfers the transmit data written in SCBFTDR to SCBTSR and starts serial transmission.

SCBFTDR is a write-only register, and cannot be read by the CPU.

The next data cannot be written when SCBFTDR is filled with 256 bytes of transmit data. Data written in this case is ignored.



Bit	Bit Name	Initial Value	R/W	Description
7 to 0	SCFTD[7:0]	Undefined	W	Serial transmit data FIFO

### 42.3.17 Receive FIFO Data Register Bn (SCBFRDRn)

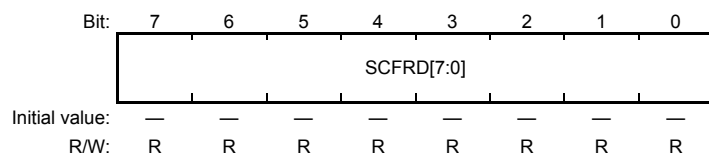
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SCBFRDR is 256-stage FIFO register that stores received serial data.

When the SCIFB has received one byte of serial data, it transfers the received data from SCBRSR to SCBFRDR where it is stored, and completes the receive operation. SCBRSR is then enabled for reception, and consecutive receive operations can be performed until SCBFRDR is full (256-byte data).

SCBFRDR is a read-only register, and cannot be written to by the CPU.

If a read is performed when there is no receive data in SCBFRDR, an undefined value will be returned. When SCBFRDR is full of receive data, subsequent serial data is lost.



Bit	Bit Name	Initial Value	R/W	Description
7 to 0	SCFRD[7:0]	Undefined	R	Serial receive data FIFO



**42.3.18 Serial Control Register 2 Bn (SCBSC2Rn)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SCBSC2R is a 16-bit readable/writable register that enables or disables the interrupt request.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RRCCE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	RRCCE	0	R/W	Receive Reading Count Compare Enable Enables or disables generation of a receive-reading-count-compare interrupt when the RRCCF bit in SCBSS2R is set to 1. 0: Receive-reading-count-compare interrupt disabled 1: Receive-reading-count-compare interrupt enabled

### 42.3.19 Serial Status Register 2 Bn (SCBSS2Rn)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SCBSS2R is a 16-bit readable/writable register that indicates the SCIFB status. However, 1 cannot be written to the RRCCF flag. The RRCCF flag is cleared to 0 after reading 1.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RRCCF
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	RRCCF	0	R/W*	Receive Reading Count Compare Indicates the result of comparison between a value of the receive reading count SCBRRCR and a value of the receive reading count compare SCBRRCCR. 0: A value of the receive reading count SCBRRCR is less than a value of the receive reading count compare SCBRRCCR. [Clearing conditions] <ul style="list-style-type: none"> <li>Power-on reset or manual reset</li> <li>When 0 is written to RRCCF after reading RRCCF = 1</li> </ul> 1: A value of the receive reading count SCBRRCR is greater than a value of the receive reading count compare SCBRRCCR. [Setting condition] <ul style="list-style-type: none"> <li>When a value of the receive reading count SCBRRCR is greater than a value of the receive reading count compare SCBRRCCR.</li> </ul>

Note: \* Only 0 can be written to clear the flag.

### 42.3.20 Receive Reading Count H Register Bn (SCBRRCHRn)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SCBRRCHR is a 16-bit readable/writable register. It is the upper 16 bits of the SCBRRCR register used by the receive-reading-count interrupt.

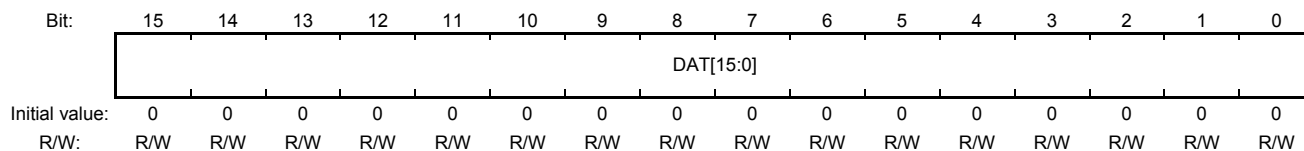
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DAT[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 0	DAT[15:0]	H'0000	R/W	Upper 16 bits of the receive reading count data

### 42.3.21 Receive Reading Count L Register Bn (SCBRRCLRn)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SCBRRCLR is a 16-bit readable/writable register. It is the lower 16 bits of the SCBRRCR register used by the receive-reading-count-compare interrupt.

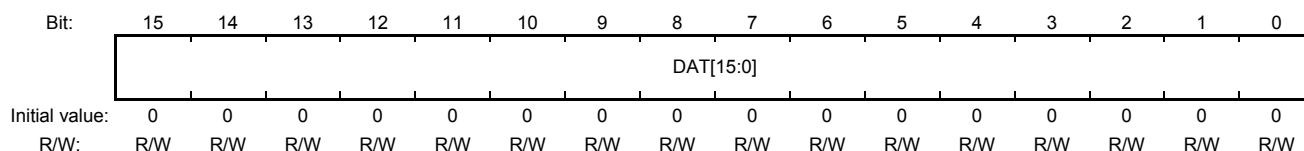


Bit	Bit Name	Initial Value	R/W	Description
15 to 0	DAT[15:0]	H'0000	R/W	<p>Lower 16 bits of the receive reading count data</p> <p>These bits function as 32-bit receive reading count data SCBRRCR together with the upper 16 bits of receive reading count data SCBRRCHR.</p> <p>It is incremented by 1 when SCBRFDR is read.</p> <p>When RRCCF bit in SCBSS2R is 1 and a value of SCBRRCR is greater than a value of SCBRRCCR, its value is updated by subtracting the SCBRRCCR value (SCBRRCR - SCBRRCCR).</p>

### 42.3.22 Receive Reading Count Compare H register Bn (SCBRRCCHRn)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SCBRRCCHR is a 16-bit readable/writable register. It is the upper 16 bits of the SCBRRCCR register used by the receive-reading-count-compare interrupt.

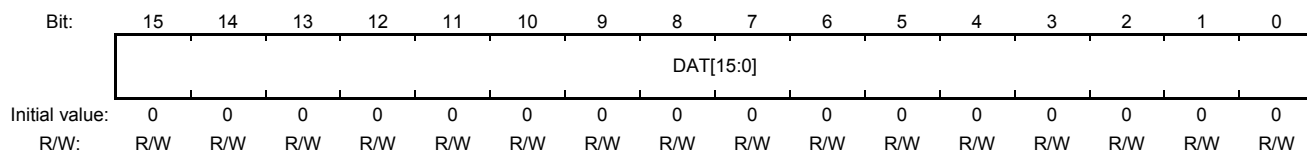


Bit	Bit Name	Initial Value	R/W	Description
15 to 0	DAT[15:0]	H'0000	R/W	Upper 16 bits of the receive reading count compare data

### 42.3.23 Receive Reading Count Compare L Register Bn (SCBRRCLRn)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SCBRRCLR is a 16-bit readable/writable register. It is the lower 16 bits of the SCBRRCCR register used by the receive-reading-count-compare interrupt.

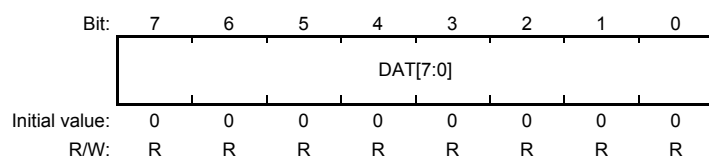


Bit	Bit Name	Initial Value	R/W	Description
15 to 0	DAT[15:0]	H'0000	R/W	Lower 16 bits of the receive reading count compare data It functions as 32-bit receive reading count compare data SCBRRCCR together with the upper 16 bits of receive reading count compare data SCBRRCCR. The data in comparison with receive reading count register is set up. When RRCCF = 0 and the value of SCBRRCCR is greater than the value of SCBRRCCR, this counter value is initialized to H'0000.

### 42.3.24 Receive FIFO1 Register Bn (SCBFIFO1n)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SCBFIFO1 is a read-only 8-bit register. A receive-reading-count-compare interrupt occurs when the number of times data have been received reaches (receive reading count compare value - 1). If the receive reading count value immediately after the interrupt generation is two or more, it does not change.

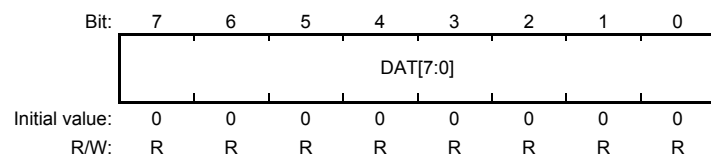


Bit	Bit Name	Initial Value	R/W	Description
7 to 0	DAT[7:0]	H'00	R	A receive-reading-count-compare interrupt indicates that the number of times data have been received has reached (SCBRRCCR-1).

**42.3.25 Receive FIFO0 Register Bn (SCBFIFO0n)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SCBFIFO0 is a read-only 8-bit register. When a receive-reading-count-compare interrupt occurs, it is the receive data equal to receive reading count compare value. If the receive reading count value immediately after the interrupt generation is two or more, it does not change.



Bit	Bit Name	Initial Value	R/W	Description
7 to 0	DAT[7:0]	H'00	R	A receive-reading-count-compare interrupt indicates that the number of times data have been received has reached SCBRRCR.

## 42.4 Operation

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

### 42.4.1 Overview

The SCIFB supports serial communications in asynchronous mode, in which synchronization is achieved character by character, and in clocked synchronous mode, in which synchronization is achieved with clock pulses. 256-stage FIFO buffers are provided for both transmission and reception, reducing the CPU overhead and enabling high-speed continuous communications.

### 42.4.2 Asynchronous Mode

In the asynchronous mode, the transfer format is selected by the setting in SCBSMR as shown in Table 42.5. Features in this mode are as follows.

- Data length: 7 or 8 bits
- The addition of parity (even, odd or none) and the choice of stop-bit length (1 or 2 bits), along with the data length, determine the transfer format and character length.
- Receive error detection: Framing, parity, and overrun errors, receive-FIFO-data-full, receive-data-ready, and breaks.
- Independent indications of the number of data stored in the transmit and receive FIFOs.
- Clock source: Internal clock signal generated by the baud rate generator.

**Table 42.5 SCBSMR Settings for Serial Transfer Format Selection**

SCBSMR Setting				Mode	SCIFB Transfer Format		
Bit 7	Bit 6	Bit 5	Bit 3		Data Length	Parity Bit	Stop Bit Length
C/A#	CHR	PE	STOP				
0	0	0	0	Asynchronous mode	8-bit data	None	1 bit
			1				2 bits
		1	0			Provided	1 bit
			1			2 bits	
	1	0	0		7-bit data	None	1 bit
			1				2 bits
		1	0			Provided	1 bit
			1			2 bits	
1	*	*	*	Clocked synchronous mode	8-bit data	None	None

Note: \* Don't care

### 42.4.3 Serial Operation in Asynchronous Mode

#### (1) Data Transfer Format

Table 42.6 shows the transfer formats that can be used in asynchronous mode. Any of eight transfer formats can be selected according to the SCBSMR settings.

**Table 42.6 Serial Transfer Formats**

SCBSMR Settings			Serial Transfer Format and Frame Length												
CHR	PE	STOP	1	2	3	4	5	6	7	8	9	10	11	12	
0	0	0	S	8-bit data								STOP			
		1	S	8-bit data								STOP	STOP		
	1	0	S	8-bit data								P	STOP		
		1	S	8-bit data								P	STOP	STOP	
1	0	0	S	7-bit data							STOP				
		1	S	7-bit data							STOP	STOP			
	1	0	S	7-bit data							P	STOP			
		1	S	7-bit data							P	STOP	STOP		

[Legend]

S: Start bit

STOP: Stop bit

P: Parity bit

#### (2) Clock

An internal clock signal generated by the on-chip baud rate generator provides the transfer clock for SCIFB.

#### (3) Data Transfer Operations:

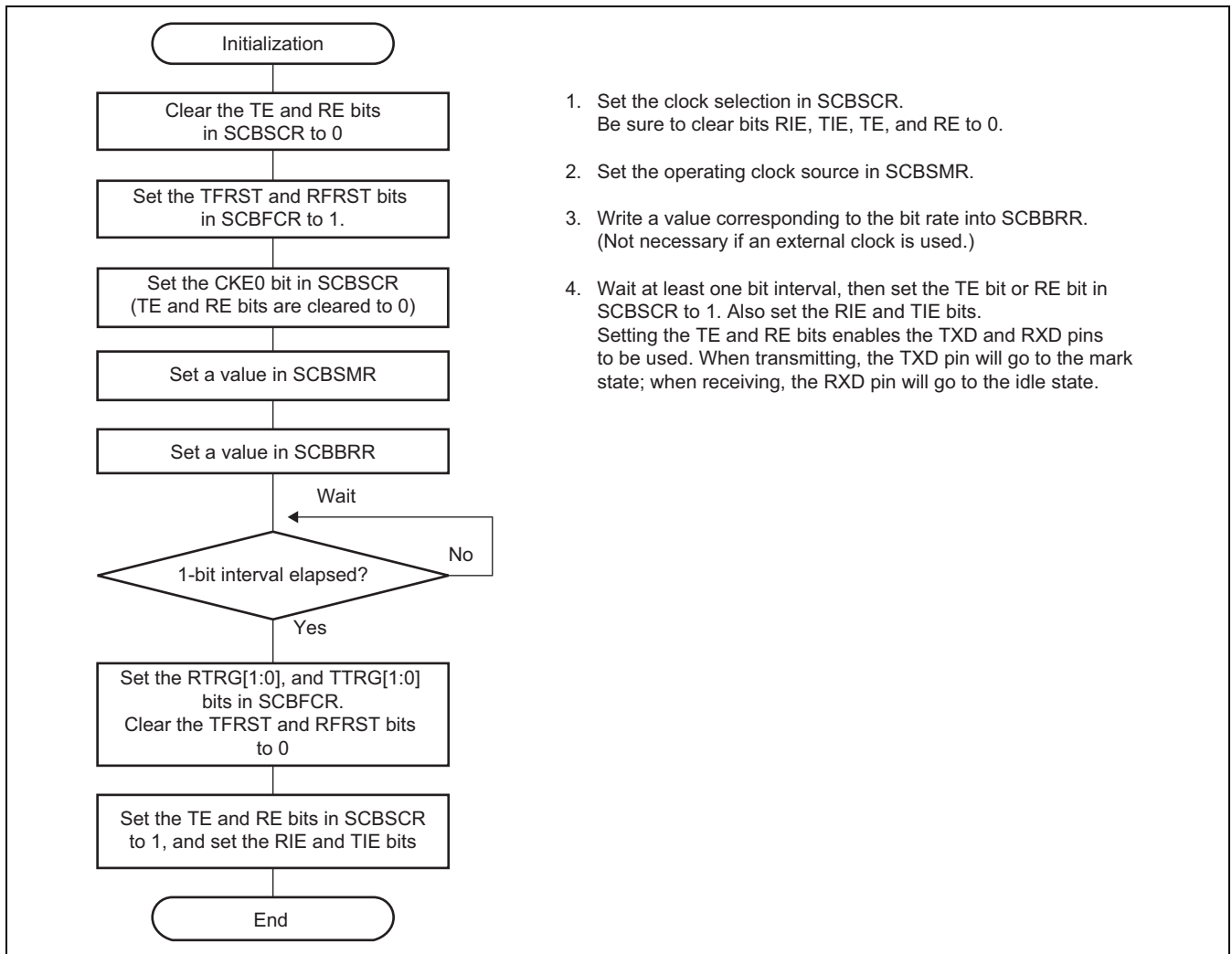
##### 1. SCIFB initialization

Before transmitting and receiving data, it is necessary to clear the TE and RE bits in SCBSCR to 0, then initialize the SCIFB as described below.

When the transfer format, etc., is changed, the TE and RE bits must be cleared to 0 before making the change using the following procedure. When the TE bit is cleared to 0, SCBTSR is initialized. Note that clearing the TE and RE bits to 0 does not change the contents of SCBSSR, SCBFTDR, or SCBFRDR. The TE bit should be cleared to 0 after all transmit data has been sent and the TEND bit in SCBSSR has been set to 1. Clearing to 0 can also be performed during transmission, but the data lines that transmit the data will go to the high-impedance state after the clearance.

Before setting TE to 1 again to start transmission, the TFRST bit in SCBFCR should first be set to 1 to reset SCBFTDR.

Figure 42.2 is an example of flow for the SCIFB initialization.



1. Set the clock selection in SCBSCR. Be sure to clear bits RIE, TIE, TE, and RE to 0.
2. Set the operating clock source in SCBSMR.
3. Write a value corresponding to the bit rate into SCBBRR. (Not necessary if an external clock is used.)
4. Wait at least one bit interval, then set the TE bit or RE bit in SCBSCR to 1. Also set the RIE and TIE bits. Setting the TE and RE bits enables the TXD and RXD pins to be used. When transmitting, the TXD pin will go to the mark state; when receiving, the RXD pin will go to the idle state.

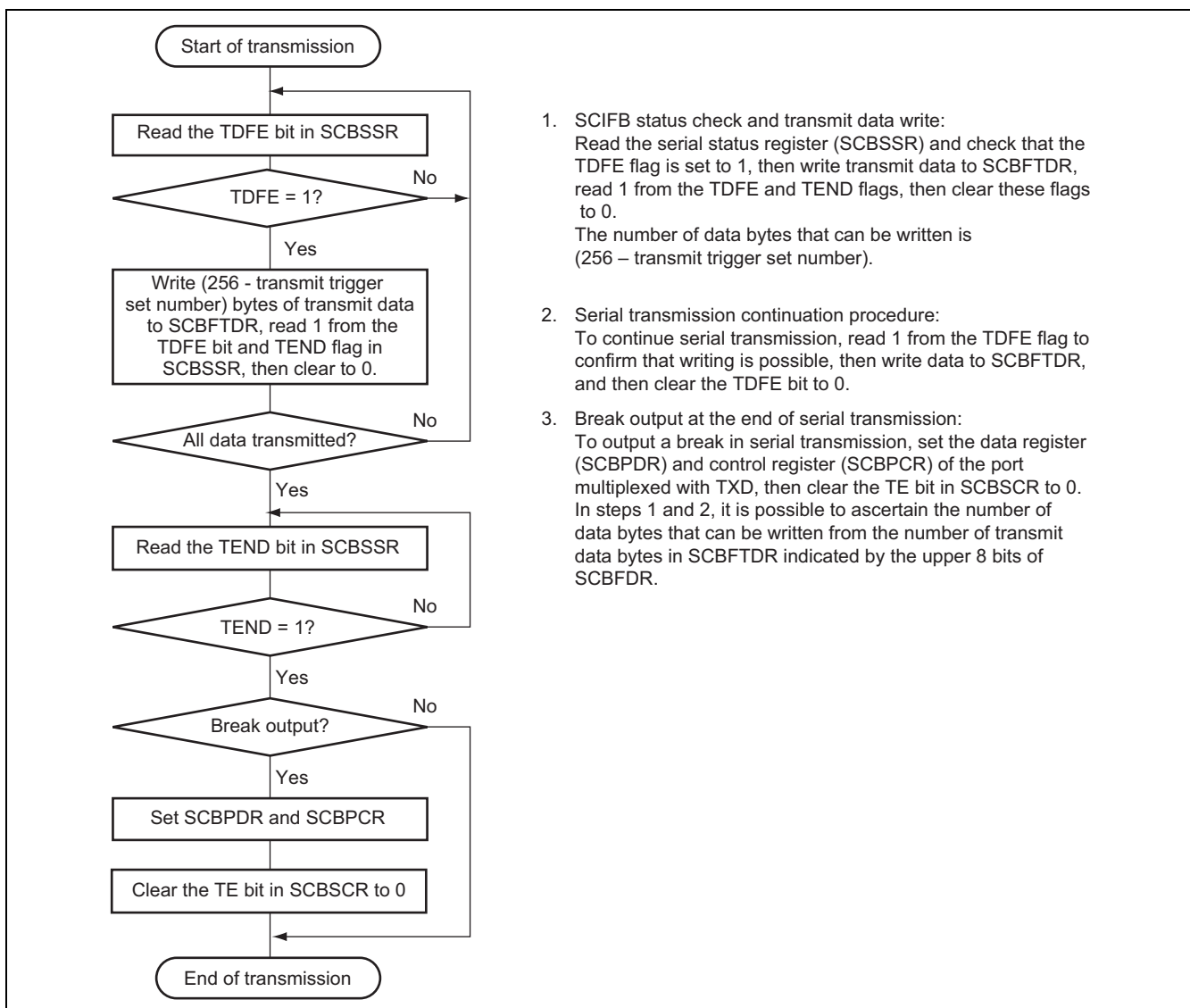
Figure 42.2 Example of Flow for SCIFB Initialization



2. Serial data transmission

Figure 42.3 an example of flow for the serial transmission.

Use the following procedure for serial data transmission after enabling the SCIFB for transmission.



1. SCIFB status check and transmit data write:  
Read the serial status register (SCBSSR) and check that the TDFE flag is set to 1, then write transmit data to SCBFTDR, read 1 from the TDFE and TEND flags, then clear these flags to 0.  
The number of data bytes that can be written is (256 – transmit trigger set number).
2. Serial transmission continuation procedure:  
To continue serial transmission, read 1 from the TDFE flag to confirm that writing is possible, then write data to SCBFTDR, and then clear the TDFE bit to 0.
3. Break output at the end of serial transmission:  
To output a break in serial transmission, set the data register (SCBPDR) and control register (SCBPCR) of the port multiplexed with TXD, then clear the TE bit in SCBSCR to 0. In steps 1 and 2, it is possible to ascertain the number of data bytes that can be written from the number of transmit data bytes in SCBFTDR indicated by the upper 8 bits of SCBFDR.

Figure 42.3 Example of Flow for Serial Transmission

In serial transmission, the SCIFB operates as described below.

- A. When data is written into SCBFTDR, the SCIFB transfers the data from SCBFTDR to SCBTSR and starts transmitting. Confirm that the TDFE flag in SCBSSR is set to 1 before writing transmit data to SCBFTDR. The number of data bytes that can be written is not less than (256 – transmit trigger set number).
- B. When data is transferred from SCBFTDR to SCBTSR and transmission is started, consecutive transmit operations are performed until there is no transmit data left in SCBFTDR. When the number of transmit data bytes in SCBFTDR falls to or below the transmit trigger number set in SCBFCR, the TDFE flag is set. If the TIE bit in SCBSCR is set to 1 at this time, a transmit-FIFO-data-empty interrupt (TXI) request is generated.

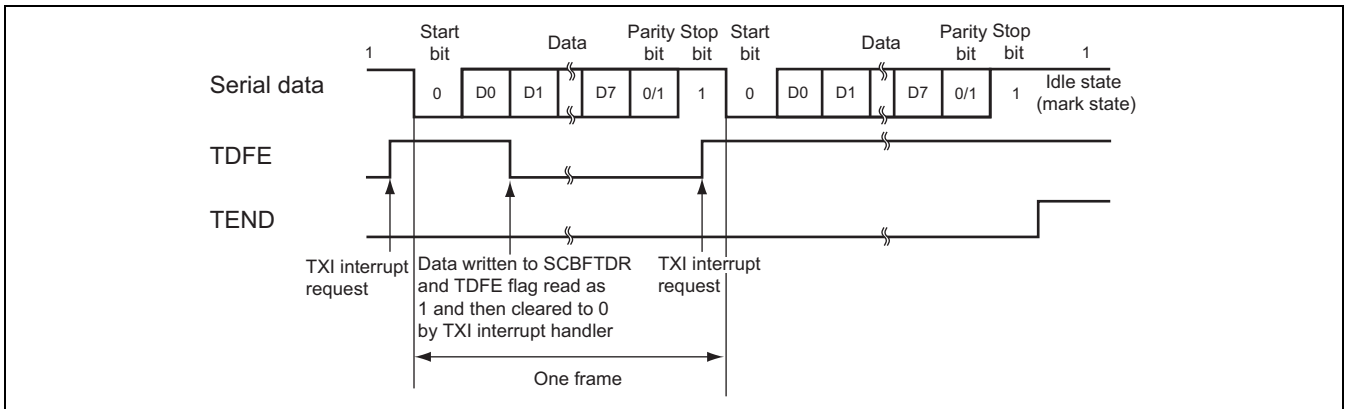
When the transmit data stop function is used and the number of data bytes set in SCBTDSR is matched, transmit operation is stopped and the TSF flag in SCBSSR is set. If the TSIE bit in SCBSCR is set to 1, a transmit-data-stop interrupt (TDI) request is generated. The vectors of TXI and TDI are the same.

The serial transmit data is sent from the TXD pin in the following order.

- a. Start bit: One logic-0 bit is output.
  - b. Transmit data: 8-bit or 7-bit data is output in LSB-first order.
  - c. Parity bit: One parity bit (even or odd parity) is output.
  - d. A format in which a parity bit is not output can also be selected.
  - e. Stop bit(s): One or two logic-1 bits (stop bits) are output.
  - f. Mark state: Output of 1 is continued until the start bit is sent to start the next transmission.
- C. The SCIFB checks the SCBFTDR transmit data at the timing for sending the stop bit. If data is present, the data is transferred from SCBFTDR to SCBTSR, the stop bit is sent, and then serial transmission of the next frame is started.

If there is no transmit data, the TEND flag in SCBSSR is set to 1, the stop bit is sent, and then the line goes to the mark state in which 1 is output.

Figure 42.4 shows an example of the operation for transmission in asynchronous mode.

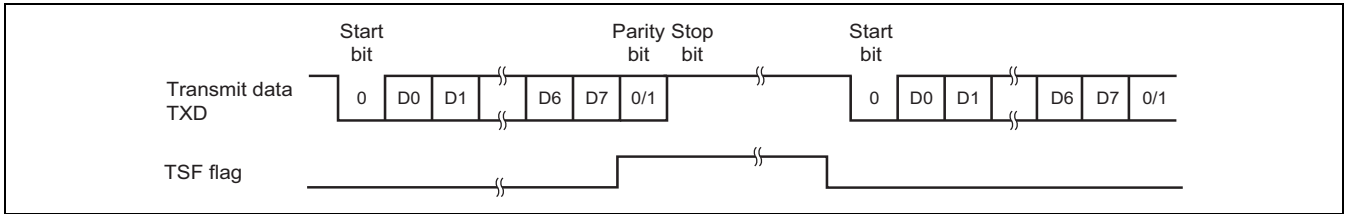


**Figure 42.4 Example of Transmit Operation (Example with 8-Bit Data, Parity, and One Stop Bit)**

- Transmit data stop function

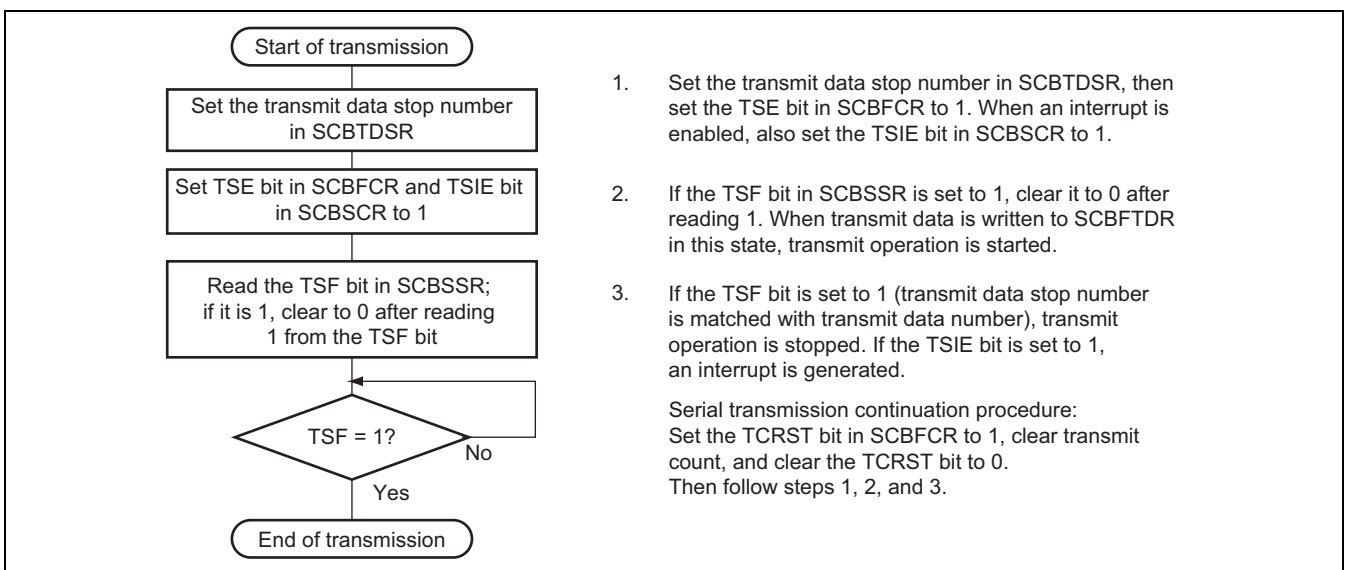
When the value in SCBTDSR equals the number of transmitted data bytes, this function stops the transmit operation. Interrupts can be generated and the DMAC can be activated by setting the TSIE bit (interrupt enable bit) to 1.

Figure 42.5 shows an example of operation for the transmit data stop function.



**Figure 42.5 Example of Transmit Data Stop Function**

Figure 42.6 shows a flowchart for the transmit data stop function.



**Figure 42.6 Transmit Data Stop Function Flowchart**

## 3. Serial data reception

Figures 42.7 and 42.8 are examples of flow for the serial reception.

Use the following procedure for serial data reception after enabling the SCIFB for reception.

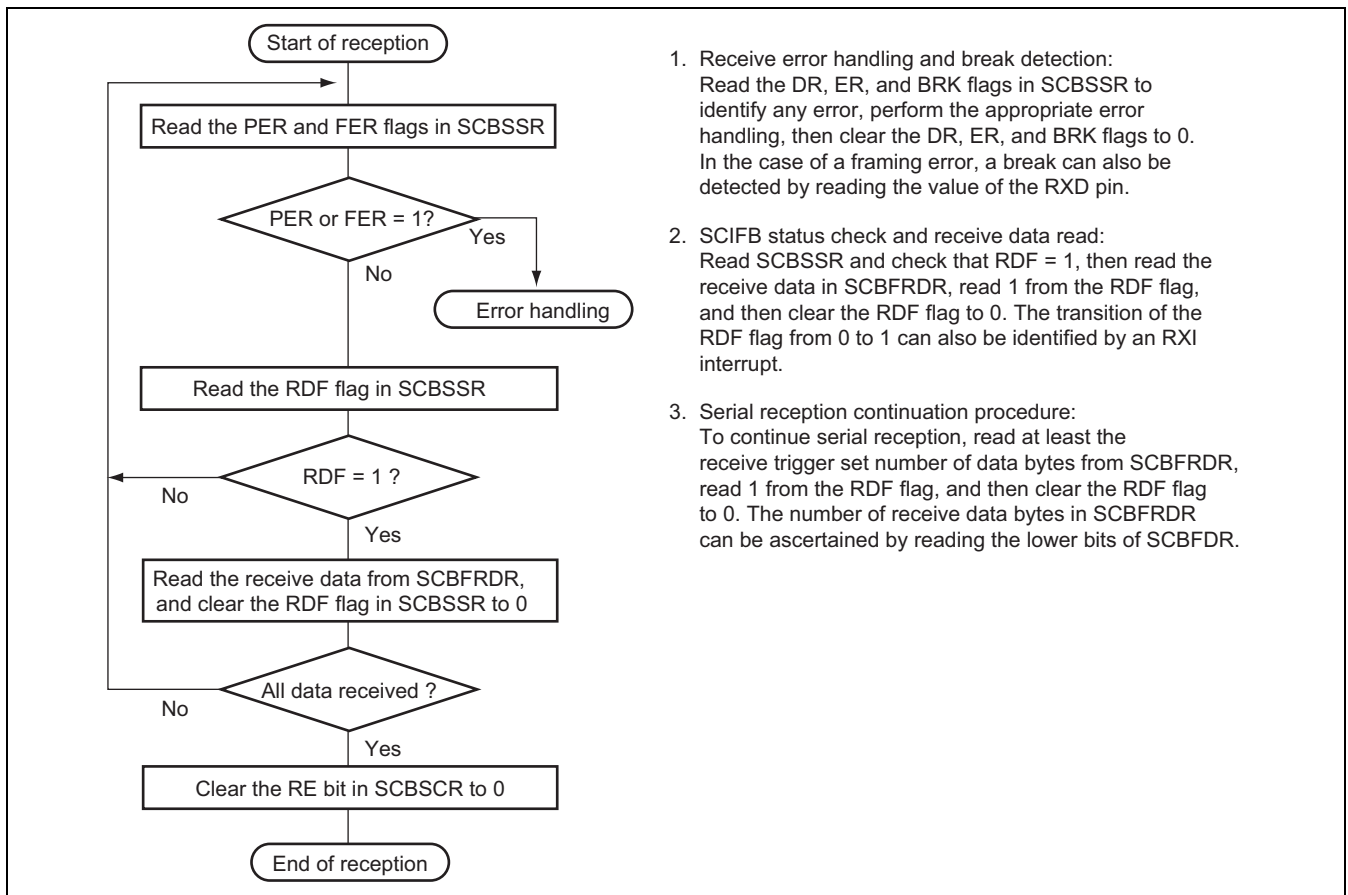
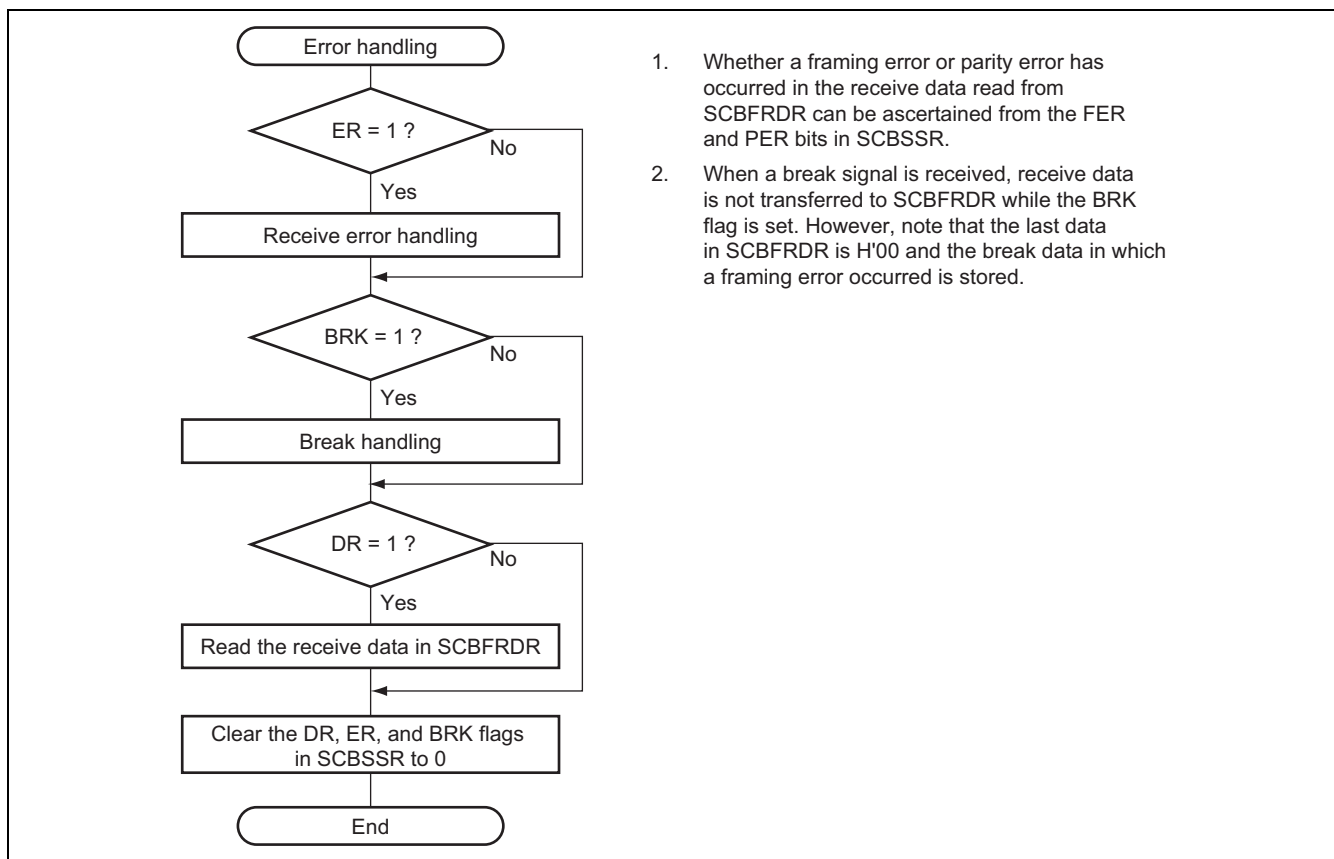


Figure 42.7 Example of Flow for Serial Reception (1)



**Figure 42.8 Example of Flow for Serial Reception (2)**

In serial reception, the SCIFB operates as described below.

- A. The SCIFB monitors the communication line, and if a 0 start bit is detected, performs internal synchronization and starts reception.
- B. The received data is stored in SCBRSR in LSB-to-MSB order.
- C. The parity bit and stop bit are received.

After receiving these bits, the SCIFB carries out the following checks.

- a. Stop bit check: The SCIFB checks to see if the value in the stop bit position is 1. If the two-stop-bit setting has been made, only the value in the first stop-bit position is checked.
- b. The SCIFB checks whether received data can be transferred from SCBRSR to SCBFRDR.
- c. Break check: The SCIFB checks to confirm that the BRK flag is 0, indicating that the SCIFB is not in the break state.

If all the above checks are passed, the receive data is stored in SCBFRDR.

Note: Reception continues when a receive error (framing error or parity error) occurs.

- D. If the RIE bit in SCBSCR is set to 1 when the RDF flag changes to 1, a receive-FIFO-data-full interrupt (RXI) request is generated.

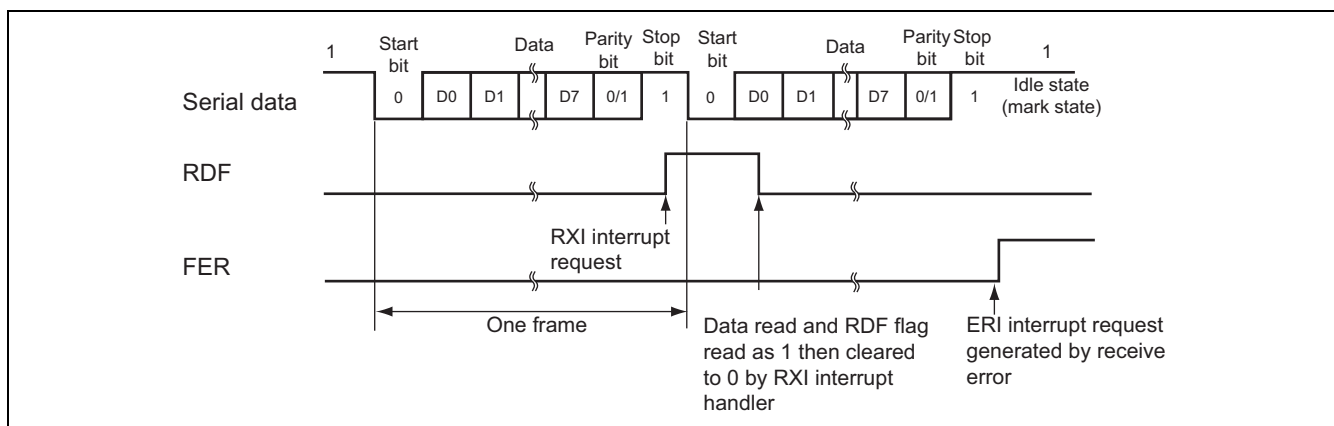
If the ERIE bit in SCBSCR is set to 1 when the ER flag changes to 1, a receive-error interrupt (ERI) request is generated.

If the BRIE bit in SCBSCR is set to 1 when the BRK flag changes to 1, a break reception interrupt (BRI) request is generated.

If the DRIE bit in SCBSCR is set to 1 when the DR flag changes to 1, a receive-data-ready interrupt (DRI) request is generated.

The vectors of each interrupt source are the same.

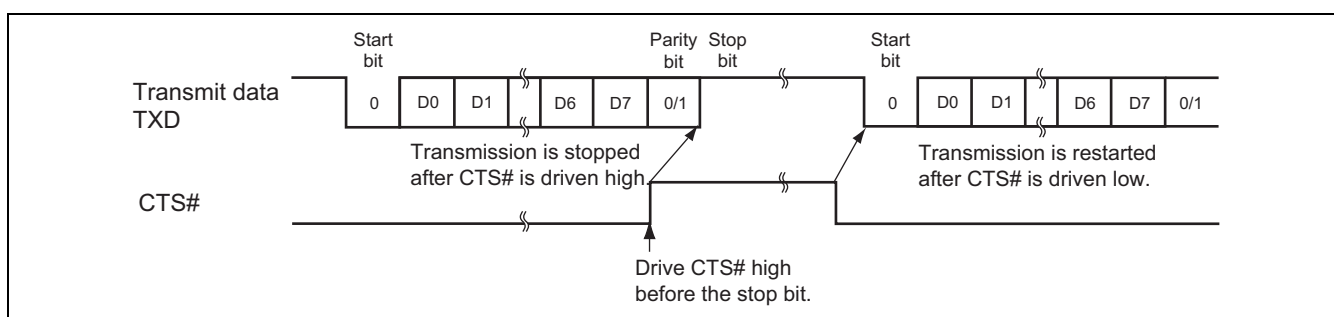
Figure 42.9 shows an example of the operation for reception in asynchronous mode.



**Figure 42.9 Example of SCIFB Receive Operation (Example with 8-Bit Data, Parity, One Stop Bit)**

The SCIFB has a modem function that allows the stoppage and resumption of transmission according to the input value of CTS#. Setting CTS# to 1 places the transmission line in the mark state after transmission of the current frame. When CTS# is set to 0, the next frame for transmission is output, with a start bit as its leader.

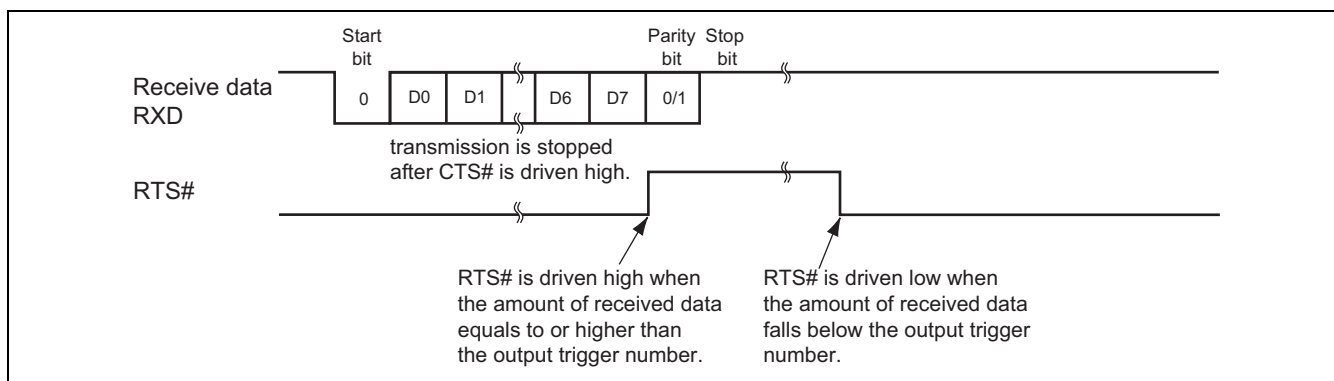
Figure 42.10 shows an example of the operation of CTS# control.



**Figure 42.10 Example of CTS# Control Operation**

The RTS# signal is driven high when the modem function is in use and the received data stored in the receive FIFO register (SCBFRDR) equals or exceeds the number of the RTS# output triggers.

Figure 42.11 shows an example of the operation for RTS# control.



**Figure 42.11 Example of RTS# Control Operation**

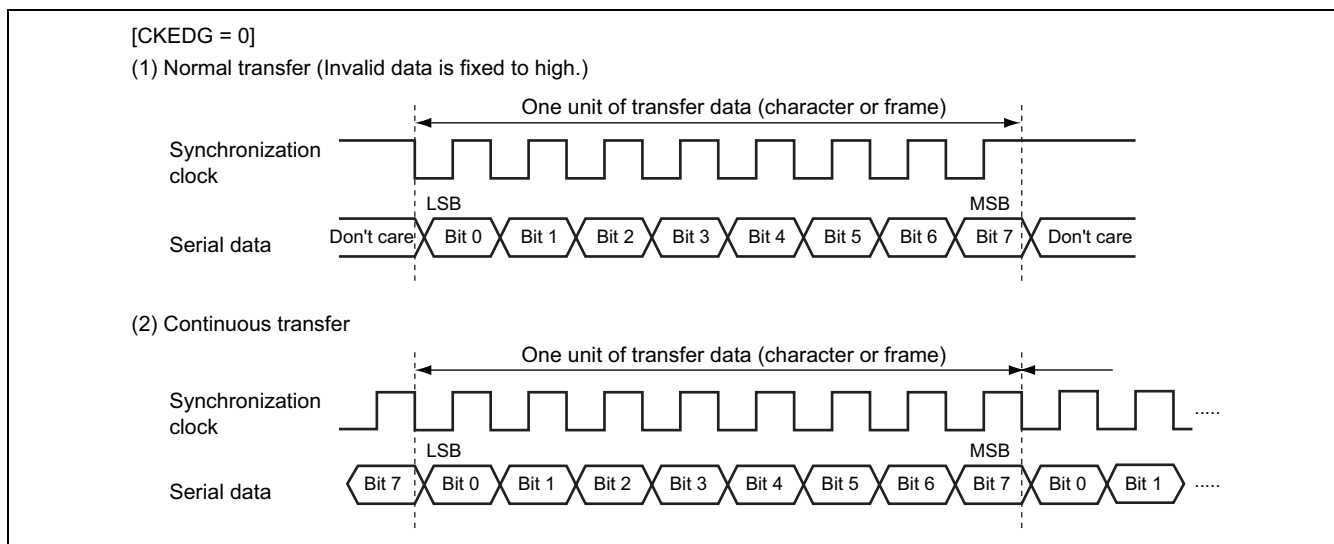
#### 42.4.4 Operation in Clocked Synchronous Mode

Clocked synchronous mode, in which data is transmitted or received in synchronization with clock pulses, is suitable for fast serial communications.

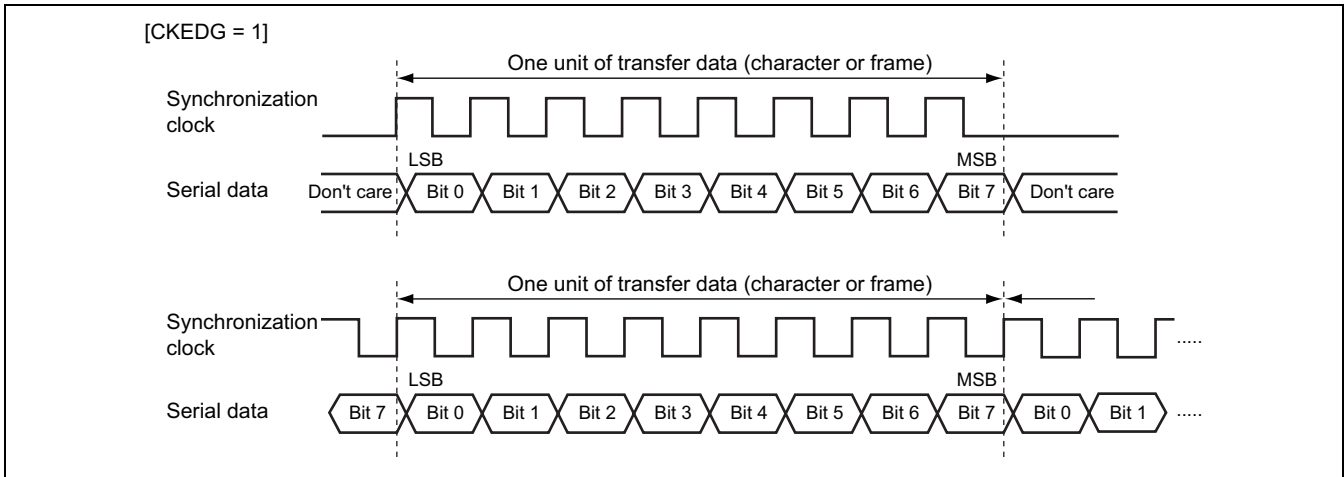
Since the transmitter and receiver are independent units in SCIFB, full-duplex communications can be achieved by sharing the clock. Both the transmitter and receiver have a 256-stage FIFO buffer structure, so that data can be read or written during transmission or reception, enabling continuous data transmission and reception.

Through the setting of the CKEDG bit, the format for clocked synchronous communications can be selected.

Figures 42.12 and 42.13 show the format for clocked synchronous communications.



**Figure 42.12 Data Format in Clocked Synchronous Communications (CKEDG = 0)**



**Figure 42.13 Data Format in Clocked Synchronous Communications (CKEDG = 1)**

In clocked synchronous serial communications, the data on the communications line is latched on one edge selected by the CKEDG bit in SCBSMR and is output until the next edge. Accuracy of data is guaranteed on the next edge (i.e. that in the opposite direction to the latching edge).

In serial communications, each character is output starting with the LSB and ending with the MSB. After the MSB is output, the communications line remains in the state of the last bit.

Data is received on the opposite edge to that on which data is output.

### (1) Data Transfer Format

A fixed 8-bit data format is used. No parity bit can be added.

### (2) Clock

An internal clock signal generated by the on-chip baud rate generator provides the transfer clock for SCIFB. For details on SCIFB clock source selection, see Table 42.4.

### (3) SCIFB Initialization (Clocked Synchronous Mode)

Before transmitting and receiving data, it is necessary to clear the TE and RE bits in SCBSCR to 0, and then initialize the SCIFB as described below.

When changing the operating mode or transfer format, etc., the TE and RE bits must be cleared to 0 before making the change using the following procedure. When the TE bit is cleared to 0, SCBTSR is initialized. Note that clearing the RE bit to 0 does not initialize the RDF, PER, FER, or ORER flag state or change the contents of SCBFRDR.



Figure 42.14 is an example of flow for the SCIFB initialization.

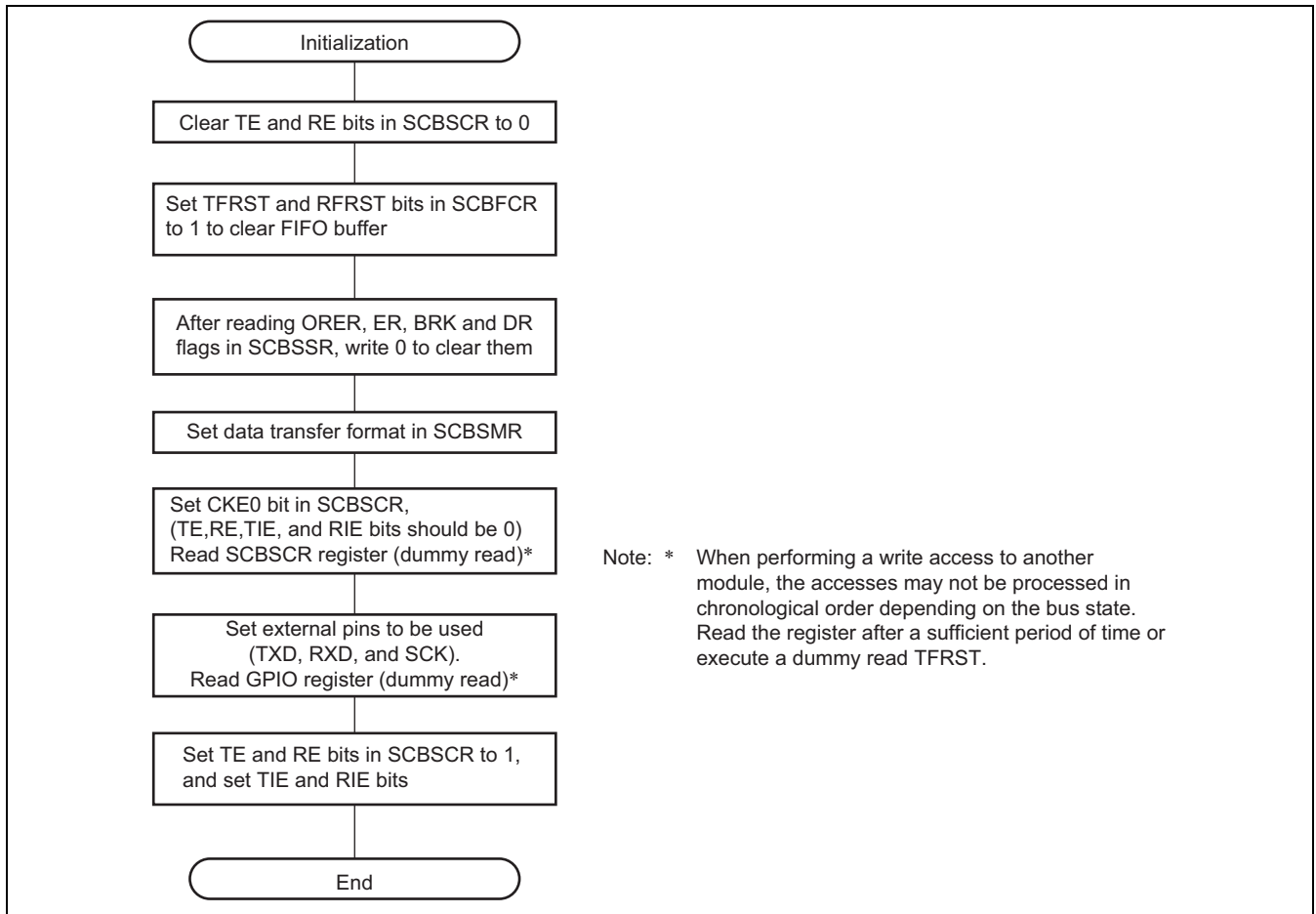
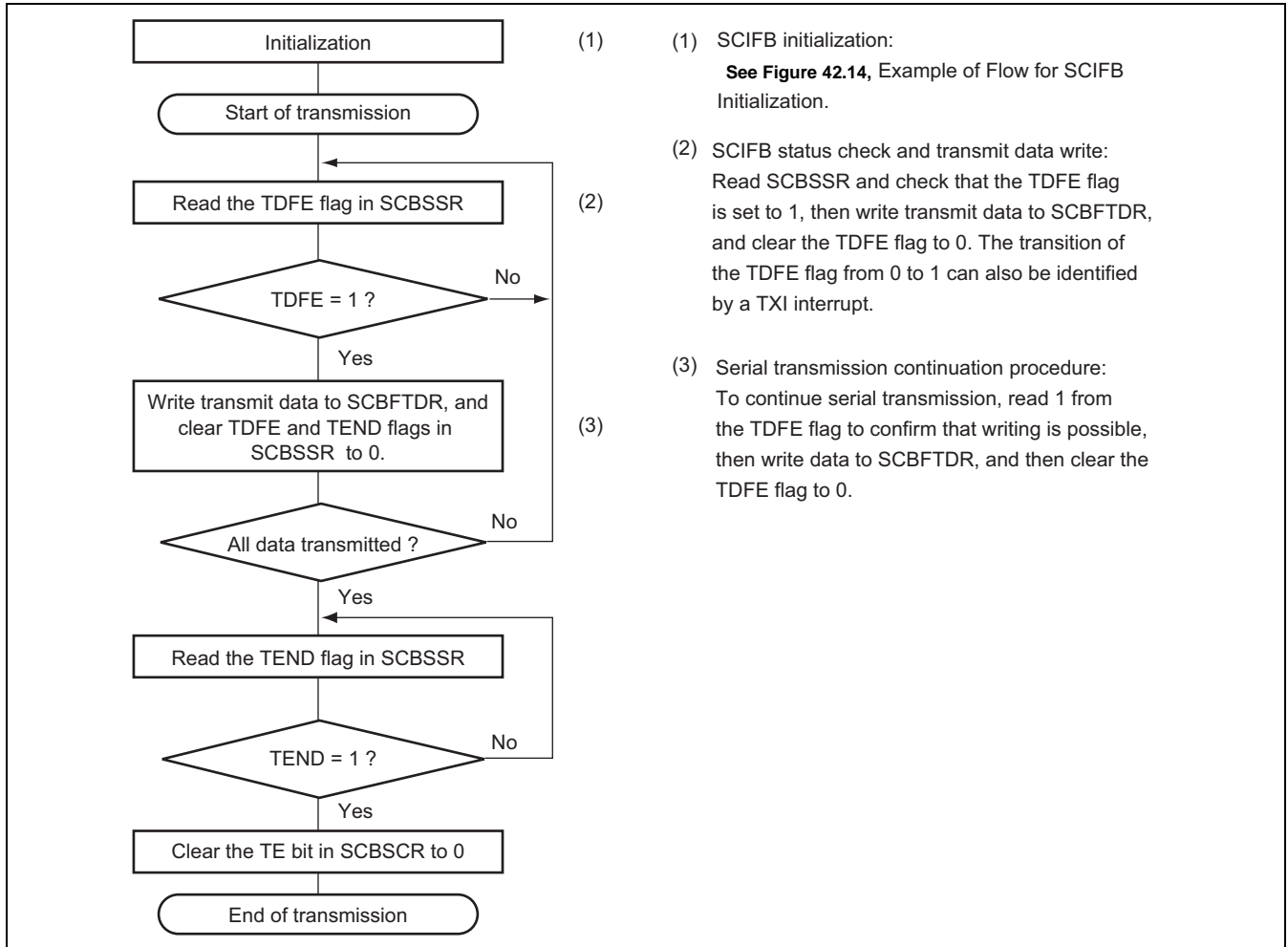


Figure 42.14 Example of Flow for SCIFB Initialization

**(4) Serial Data Transmission (Clocked Synchronous Mode)**

Figure 42.15 is an example of flow for the serial transmission.

Use the following procedure for serial data transmission after enabling the SCIFB for transmission.

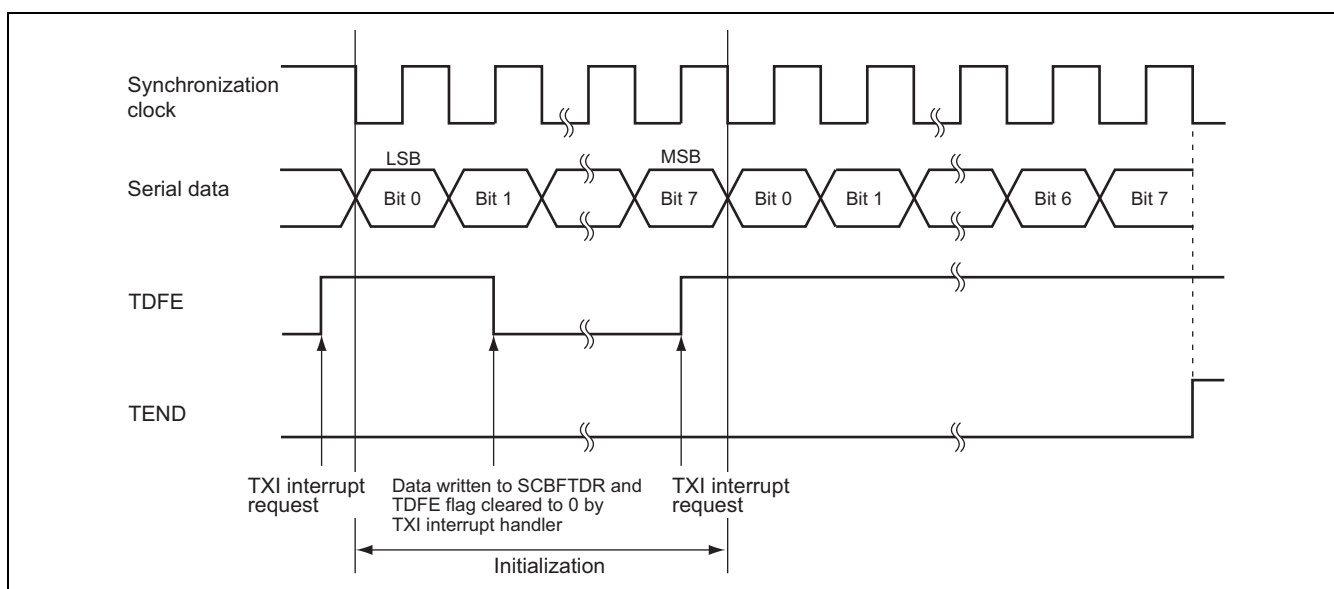


**Figure 42.15 Example of Flow for Serial Transmission**

In serial transmission, the SCIFB operates as described below.

1. When data is written into SCBFTDR, the SCIFB transfers data from SCBFTDR to SCBTSR and starts transmitting. Confirm that the TDFE flag in SCBSSR is set to 1 before writing transmit data to SCBFTDR. The number of data bytes that can be written is at least 16 – (transmit trigger set number).
2. When data is transferred from SCBFTDR to SCBTSR and transmission is started, consecutive transmit operations are performed until there is no transmit data left in SCBFTDR. When the number of transmit data bytes in SCBFTDR falls to or below the transmit trigger number set in SCBFCR, the TDFE flag is set. If the TIE bit in SCBSCR is set to 1 at this time, a transmit-FIFO-data-empty interrupt (TXI) request is generated. The SCIFB outputs data in synchronization with the synchronization clock. The serial transmit data is sent from the TXD pin in the LSB-first order.
3. The SCIFB checks the SCBFTDR transmit data at the timing for sending the last bit. If data is present, the data is transferred from SCBFTDR to SCBTSR, and then serial transmission of the next frame is started. If there is no transmit data, the TEND flag in SCBSSR is set to 1 after the last bit is sent, and the transmit data pin (TXD pin) retains the output state of the last bit.

Figure 42.16 shows an example of the SCIFB operation for transmission in clocked synchronous mode.



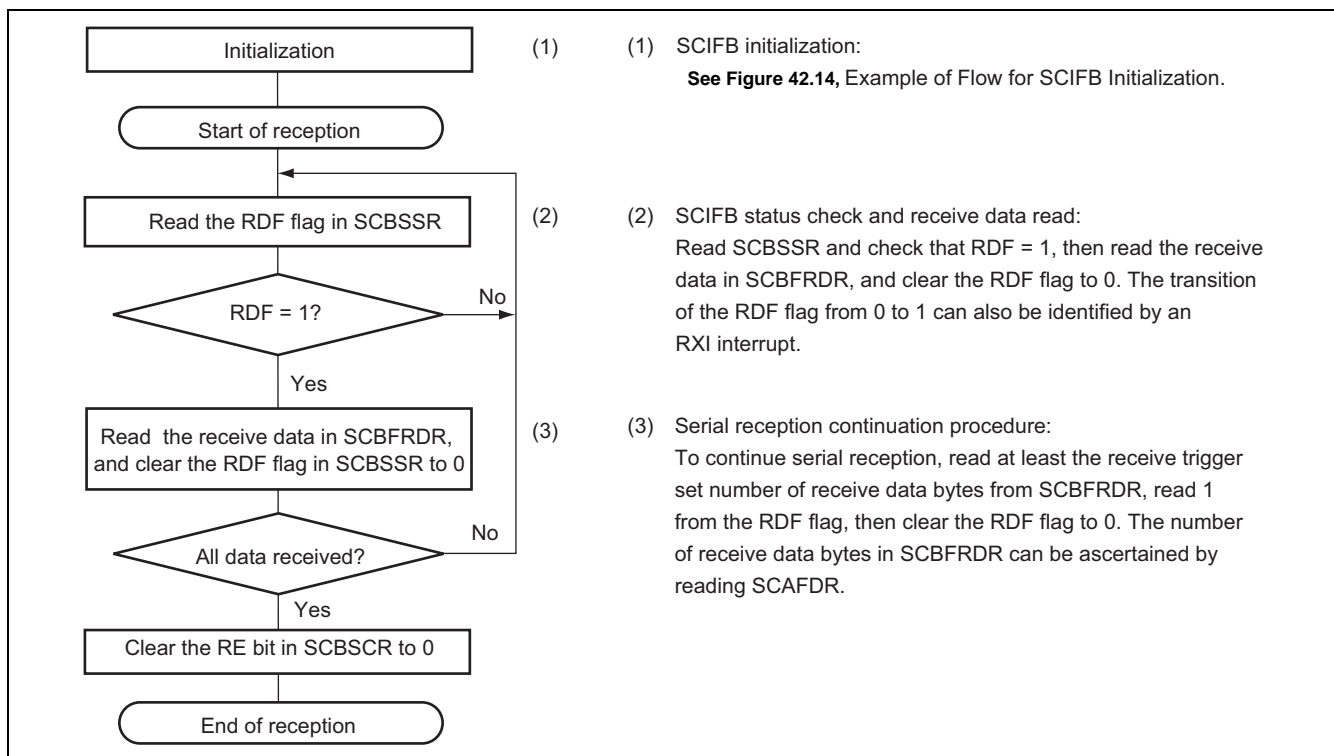
**Figure 42.16 Example of SCIFB Transmission in Clocked Synchronous Mode**

### (5) Serial Data Reception (Clocked Synchronous Mode)

Figure 42.17 is an example of flow for serial reception.

Use the following procedure for serial data reception after enabling the SCIFB for reception.

When switching the operating mode from asynchronous mode to clocked synchronous mode without initializing SCIFB, make sure that the ORER flag in SCBSSR, and PER and FER flags in SCBSSR are cleared to 0.

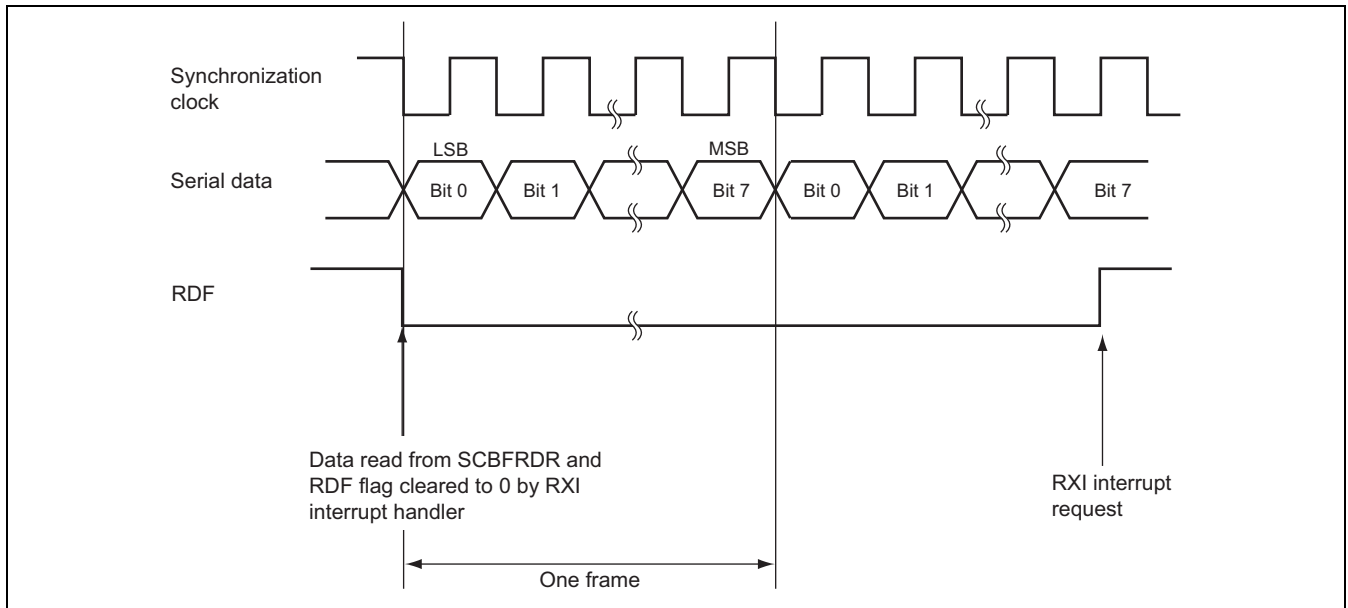


**Figure 42.17 Example of Flow for Serial Reception**

In serial reception, the SCIFB operates as described below.

1. The SCIFB starts reception in synchronization with the output of the synchronization clock.
2. The received data is stored in SCBRSR in LSB-to-MSB order.  
After receiving the data, the SCIFB checks whether the receive data can be transferred from SCBRSR to SCBFRDR. If this check is passed, the receive data is stored in SCBFRDR. If an overrun error is detected in the error check, reception cannot continue.
3. If the RIE bit in SCBSCR is set to 1 when the RDF flag changes to 1, a receive-FIFO-data-full interrupt (RXI) request is generated.

Figure 42.18 is an example of the reception in clocked synchronous mode.

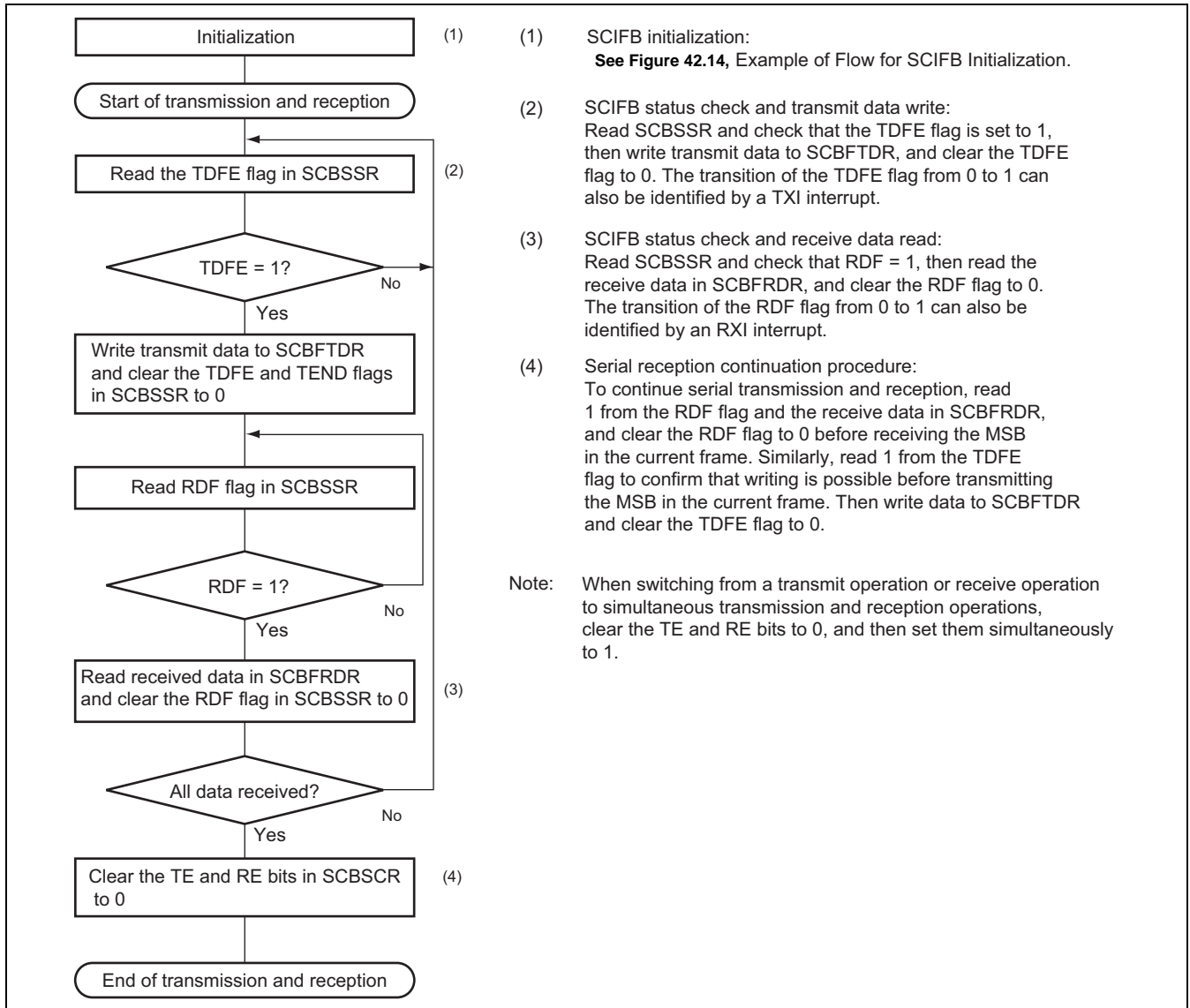


**Figure 42.18 Example of Reception in Clocked Synchronous Mode**

**(6) Simultaneous Serial Data Transmission and Reception (Clocked Synchronous Mode)**

Figure 42.19 is an example of flow for the simultaneous serial data transmission and reception.

Use the following procedure for simultaneous serial data transmission and reception after enabling the SCIFB for both the transmission and reception.



**Figure 42.19 Example of Flow for Simultaneous Serial Transmission and Reception**

## 42.5 SCIFB Interrupt Sources and DMAC

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

The SCIFB supports nine interrupts: receive-FIFO-data-full (RXI), transmit-FIFO-data-empty (TXI), receive-data-ready (DRI), break-receive (BRI), receive-error (ERI), transmit-data-stop (TDI), transmit-end (TENDPOSE), receive-data-count-compare (RCE), and receive-reading-count-compare (RRCC). The vectors of each interrupt source are the same.

Table 42.7 shows the interrupt sources. The RIE, TIE, DRIE, BRIE, ERIE, TSIE, TENDPOSE, and RCEE bits in SCBSCR, and RRCCE bit in SCBSC2R are used to enable or disable the respective interrupt sources.

If the TDFE flag in SCBSSR is set to 1, a TXI interrupt request is generated. When the TSF flag in SCBSSR is set to 1, a TDI interrupt request is generated. The DMAC can be activated for data transfer on generation of TXI and TDI interrupt requests. When data exceeding the transmit trigger set number is written to SCBFTDR by the DMAC, the DMAC transfer request is automatically cleared to 0. The DMAC requests of TXI and TDI are the same.

When the RDF flag in SCBSSR is set to 1, an RXI interrupt request is generated. The DMAC can be activated for data transfer on generation of an RXI interrupt request. When receive data in SCBFRDR is read by the DMAC until the amount left is less than the receive trigger set number, the DMAC transfer request is automatically cleared to 0.

When using the DMAC for transmission/reception, set the DMAC to the DMAC transfer enabled state before making the SCIFB settings. Transmission/reception is complete when the DMA transfer is terminated.

When the ER, BRK, DR, RCEF, TENDPOS or TSF flag in SCBSSR or RRCCF flag in SCBSS2R is set to 1, an interrupt request is generated. Note that the vectors of each interrupt source are the same.

**Table 42.7 SCIFB Interrupt Sources**

Interrupt Source Type	DMAC Activation
Interrupt initiated by receive error (ER) , break (BRK), receive data count match (RCEF), receive reading counter compare (RRCCF), transmit end detect (TENDPOS), receive data ready (DR) or transmit data stop (TSF) flag	Not possible
Interrupt initiated by receive FIFO data full (RDF) flag	Possible
Interrupt initiated by transmit FIFO data empty (TDFE) flag	Possible

## 42.6 Receive-Reading-Count-Compare Interrupt

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

The receive-reading-count-compare interrupt occurs when a value of the receive reading count SCBRRCR is greater than a value of the receive-reading-count-compare SCBRRCCR.

The value of receive-reading-count-compare is set to SCBRRCCR.

The receive-reading-count-compare interrupt is enabled by setting the RRCCE bit in SCBSC2R to 1.

The SCBRRCR value is incremented by 1 when SCBRFDR is read.

When the receive-reading-count-compare interrupt occurs, it is followed by the operations below.

- The RRCCF bit in SCBSS2R is set to 1.
- The value of SCBRRCCR is subtracted from that of SCBRRCR.
- SCBRRCCR is initialized to H'0000.

When using DMA transfer for the received data, there is a difference (of two max.) between the count value of the SCBRRCR and the data number transferred to RAM and so on because of the time lag. When SCBRRCR value is less than two after the interrupt occurrence, the DMA transfer may not be completed. In this case, the data should be read from SCBFIFO0 and SCBFIFO1.

SCBFIFO1: Indicates the (SCBRRCR-1)th data before SCBRRCR is subtracted when a receive-reading-count-compare interrupt occurs.

SCBFIFO0: Indicates the (SCBRRCR)th data before SCBRRCR is subtracted when a receive-reading-count-compare interrupt occurs.

The interrupt source clearance should be executed after setting the next interrupts and just before return from the interrupt.



## 42.7 Multibyte Transfer

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

### 42.7.1 Basic Multibyte Settings

Table 42.8 shows the SCIFB settings and DMA settings for multibyte transfer.

**Table 42.8 SCIFB Settings and DMA Settings for Multibyte Transfer**

Transfer Mode	Transmission/ Reception	SCIFB				DMAC	
		SCBMBR		SCBFCR		DMACHCR TS[3:0]	DMATCR TCR[23:0]
		MBTON	MBRON	RTRG [1:0]	TTRG [1:0]		
1-byte transfer	Transmission	1	—	B'11	—	B'0000	Transfer count
	Reception	—	1	—	B'11	B'0000	Transfer count
16-byte transfer	Transmission	1	—	B'10	—	B'1010	Transfer count/16 (roundup)
	Reception	—	1	—	B'10	B'1010	Transfer count/16 (roundup)
32-byte transfer	Transmission	1	—	B'01	—	B'1101	Transfer count/32 (roundup)
	Reception	—	1	—	B'01	B'1101	Transfer count/32 (roundup)

### 42.7.2 Specifying Transfer Count

#### (1) Number of Transfer Data Bytes for Transmission

In 16-byte or 32-byte transfer mode, data more than the transfer count is transferred to the transmit FIFO buffer. Therefore, specify the transfer count in SCBTDSR, and set the TSE bit in SCBFCR to 1 to enable the transmit data stop function before starting DMA transfer.

#### (2) Number of Transfer Data Bytes for Reception

In 16-byte or 32-byte transfer mode, when the receive data remaining in the receive FIFO buffer is less than 16 bytes (or 32 bytes), the data is still left in the FIFO buffer. When the RCEF bit in SCBSSR is set to 1 by setting the RCE bit in SCBFCR and the RCECRON bit in SCBMBR to 1, 16-byte (or 32-byte) transfer requests are made continuously to the DMAC until the receive FIFO buffer becomes empty. In this case, the DMAC attempts to transfer data more than the number of received data bytes, causing an underflow error.

When the ADDREQ bit in SCBMBR is set to 1 after the reception is completed, 16-byte (or 32-byte) transfer requests are made to the DMAC until the receive FIFO buffer becomes empty.

## 42.8 Usage Notes

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

Note the following when using SCIFB.

### (1) Writing Data to SCBFTDR and TDFE Flag

The TDFE flag in SCBSSR is set when the number of transmit data bytes written in SCBFTDR has fallen to or below the transmit trigger number set by bits TTRG[1:0] in SCBFCR. After TDFE is set, transmit data up to the number of empty bytes in SCBFTDR can be written, allowing efficient continuous transmission.

However, if the number of data bytes written in SCBFTDR is equal to or less than the transmit trigger number, the TDFE flag will be set to 1 again after being read as 1 and cleared to 0. TDFE should therefore be cleared when SCBFTDR contains transmit data more than the transmit trigger number bytes.

The number of transmit data bytes in SCBFTDR is indicated by the T[8:0] bits in SCBTFDR.

### (2) Reading Data from SCBFRDR and RDF Flag

The RDF flag in SCBSSR is set when the number of receive data bytes in SCBFRDR has become equal to or greater than the receive trigger number set by bits RTRG[1:0] in SCBFCR. After RDF is set, receive data equivalent to the trigger number can be read from SCBFRDR, allowing efficient continuous reception.

However, if the number of data bytes in SCBFRDR is still equal to or greater than the trigger number after a read, the RDF flag will be set to 1 again if it is cleared to 0. RDF should therefore be cleared to 0 after being read as 1 after all receive data has been read.

The number of receive data bytes in SCBFRDR is indicated by the R[8:0] bits in SCBRFDR.

### (3) Break Detection and Processing

Break signals can be detected by reading the RXD pin directly when a framing error (FER) is detected. Since the input from the RXD pin is always 0 in the break state, the FER flag is set and the parity error (PER) flag may also be set.

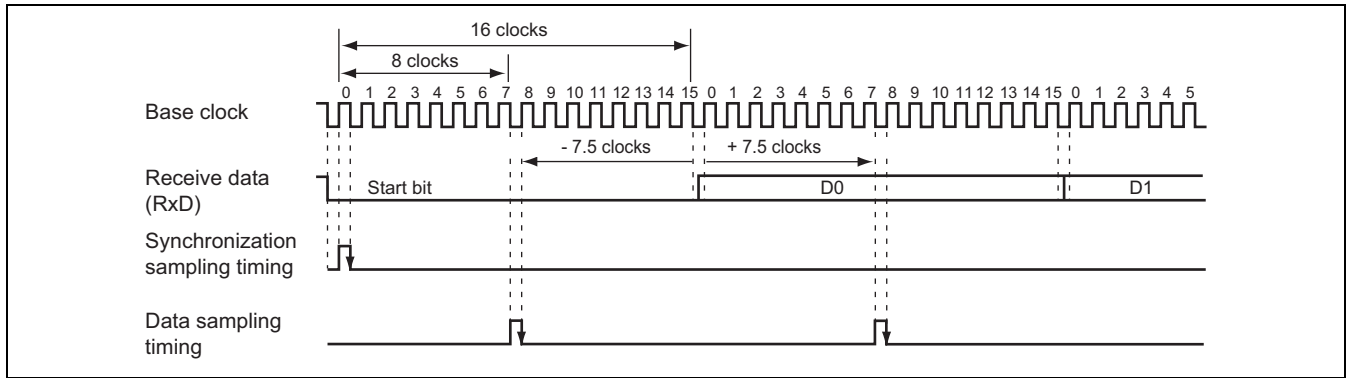
Although the SCIFB stops transferring receive data to SCBFRDR after receiving a break, it continues the receive operation.

### (4) Receive Data Sampling Timing and Receive Margin

As an example, when the sampling rate is 1/16, the SCIFB operates on a base clock with a frequency of 8 times the transfer rate.

In reception, the SCIFB synchronizes internally by sampling the fall of the start bit with the base clock. Receive data is latched at the rising edge of the eighth base clock pulse (when the sampling rate is 1/16).

The receive data sampling timing is shown in Figure 42.20.



**Figure 42.20 Receive Data Sampling Timing**

The receive margin can therefore be expressed as shown in equation (1).

$$M = \left| \left( 0.5 - \frac{1}{2N} \right) - (L - 0.5)F - \frac{|D - 0.5|}{N} (1 + F) \right| \times 100\% \dots (1)$$

- M: Receive margin (%)
- N: Ratio of clock frequency to bit rate (N = 16)
- D: Clock duty cycle (D = 0 to 1.0)
- L: Frame length (L = 9 to 12)
- F: Absolute deviation of clock frequency

From equation (1), if F = 0 and D = 0.5, the receive margin is 46.875%, as given by equation (2).

When D = 0.5 and F = 0:

$$M = (0.5 - 1 / (2 \times 16)) \times 100\% = 46.875\% \dots (2)$$

This is a theoretical value. A reasonable margin to allow in system designs is the value above (46.875%) plus 20 to 30%.

**(5) State of the PAD Pin when the Pin for SCIFB is Selected**

The table below shows the PAD pin state when the pin for the SCIFB is selected.

**Table 42.9 State of PAD**

When the pin for SCIFB is selected	TXD	RXD	RTS#	CTS#	SCK
PAD enable	1 (enabled)	1 (enabled)	RTSC in SCBPCR (initial value:1 serial port enabled), and MCE in SCBFCR (initial value: 0, disabled)	MCE in SCBFCR (initial value: 0, disabled)	SCKC in SCBPCR (initial value:1 serial port enabled), and CKE0 in SCBSCR (initial value: 0, disabled)
Pin state	Output (initial value: 1)	Input	Port output (initial value: 1)	Input	Port output (initial value: 0)
Pull-up/-down	—	Pull-up required	—	Pull-up required	—
Remarks	—	SCIFB fixes RXD to 1 internally when RE in SCBSCR = 0.	RTS# is Hi-Z when RTSC in SCBPCR = 0, and MCE in SCBFCR = 0.	SCIFB fixes CTS# to 0 internally when MCE in SCBFCR = 0.	SCK is Hi-Z when SCKC in SCBPCR = 0, and CKE0 in SCBSCR = 0.

## 43. High Speed Serial Communication Interface with FIFO (HSCIF)

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

### 43.1 Overview

The RZ/G series products have a high speed serial communication interface with built-in FIFO buffers (high-speed serial communication interface with FIFO: HSCIF) that handles asynchronous communication. The HSCIF has two 128-stage FIFO buffers separately for transmission and reception, which enables fast, efficient, and uninterrupted communication. RZ/G1H have 2 channels of HSCIF. RZ/G1M, RZ/G1N and RZ/G1E have 3 channels. All functions of each channel are same.

#### 43.1.1 Features

The HSCIF has the following features.

- Asynchronous serial communication mode
 

The HSCIF performs serial data communication based on a character-by-character asynchronous system. This feature enables serial data communication with standard asynchronous communication chips that support universal asynchronous receiver/transmitter (UART) or asynchronous communication interface adapter (ACIA). There is a choice of eight serial data transfer formats.

  - Data length: 7 or 8 bits
  - Stop bit length: 1 or 2 bits
  - Parity: Even/odd/none
  - Receive error detection: Parity, framing, and overrun errors
  - Break detection:
 

A break is detected when a framing error lasts for more than 1 frame length at space 0 (low level).

When a framing error occurs, a break can also be detected by reading the HRX pin level directly from the serial port register (HSSPTR).
  - Sampling rate: Variable (integer number from 8 to 32)
- Capable of full-duplex communication
 

The HSCIF has an independent transmitter and receiver that enable simultaneous transmission and reception. The transmitter and receiver both have a 128-stage FIFO buffer structure, enabling continuous serial data transmission and reception.
- On-chip baud rate generator, enabling any bit rate to be selected
 

The HSCIF enables choice of a clock source for transmission/reception: a clock from the on-chip baud rate generator based on the internal clock or an external clock.
- Eight interrupt sources
 

The HSCIF has eight types of interrupt sources: receive-data-ready, receive-FIFO-data-full, break detection, transmit-FIFO-data-empty, transmit-end, receive-error, overrun-error and time-out, and enables any of them to be requested independently.
- DMA data transfer
 

When the transmit FIFO register is empty or the receive FIFO register has received data, issuing a DMA transfer request activates the DMA controller (DMAC) to execute a data transfer.
- Modem control functions (HRTS# and HCTS#) are stored.
- The amount of data in the transmit/receive FIFO registers and the number of receive errors in receive data in the receive FIFO register are available.
- A receive data ready (DR) or a timeout error (TO) can be detected during reception.

43.1.2 Block Diagram

Figure 43.1 shows the HSCIF block diagram.

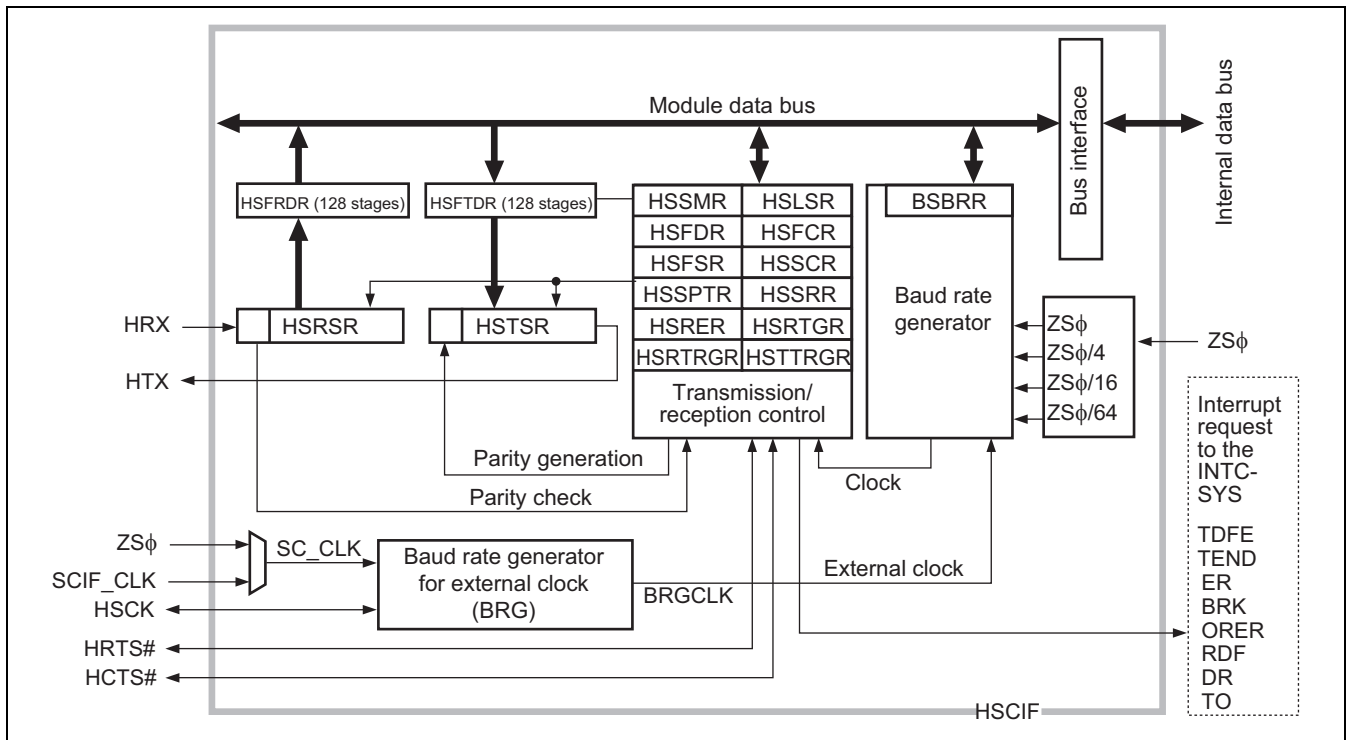


Figure 43.1 HSCIF Block Diagram

### 43.1.3 Pin Configuration

Table 43.1 shows the HSCIF pin configuration. These pins are multiplexed in other functions, so that the usage of the pins are may be restricted depending on the multiplexed pin settings.

**Table 43.1 Pin Configuration**

				<b>RZ/G Series Products</b>			
<b>Name</b>	<b>Function</b>	<b>I/O</b>	<b>Descriptions</b>	<b>RZ/G1H</b>	<b>RZ/G1M</b>	<b>RZ/G1N</b>	<b>RZ/G1E</b>
HSCK0	Serial clock pin	I/O	Clock I/O	√	√	√	√
HSCK1	Serial clock pin	I/O	Clock I/O	√	√	√	√
HSCK2	Serial clock pin	I/O	Clock I/O	—	√	√	√
HRX0	Receive data pin	Input	Receive data input	√	√	√	√
HRX1	Receive data pin	Input	Receive data input	√	√	√	√
HRX2	Receive data pin	Input	Receive data input	—	√	√	√
HTX0	Transmit data pin	Output	Transmit data output	√	√	√	√
HTX1	Transmit data pin	Output	Transmit data output	√	√	√	√
HTX,2	Transmit data pin	Output	Transmit data output	—	√	√	√
HCTS0#	Modem control pin	I/O	Transmission enabled	√	√	√	√
HCTS1#	Modem control pin	I/O	Transmission enabled	√	√	√	√
HCTS2#	Modem control pin	I/O	Transmission enabled	—	√	√	√
HRTS0#	Modem control pin	I/O	Transmission request	√	√	√	√
HRTS1#	Modem control pin	I/O	Transmission request	√	√	√	√
HRTS2#	Modem control pin	I/O	Transmission request	—	√	√	√
SCIF_CLK	Baud rate generation clock pin	Input	Clock for input to the baud rate generator for the external clock	√	√	√	√

Note: These pins are made to function as serial pins by setting up HSCIF operation using bits TE, RE, CKE[1:0] in HSSCR, and bit MCE in HSFCR. HSSPTR of the HSCIF can be used to handle the transmission and detection of break states.

### 43.1.4 Register Configuration

Table 43.2 shows the registers in the HSCIF. Do not write to any addresses other than listed below. Operations cannot be guaranteed if writing is attempted. Values read from addresses other than those listed below are undefined.

**Table 43.2 Register Configuration**

Ch. No.	Register Name	Abbreviation	R/W	Value after Reset	Address	Access Size	RZ/G Series Products			
							RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
0	Serial mode register	HSSMR	R/W	H'0000	H'E62C 0000	16	√	√	√	√
	Bit rate register	HSBRR	R/W	H'FF	H'E62C 0004	8	√	√	√	√
	Serial control register	HSSCR	R/W	H'0000	H'E62C 0008	16	√	√	√	√
	Transmit FIFO data register	HSFTDR	W	—	H'E62C 000C	8	√	√	√	√
	Serial status register	HSFSR	R/(W)* <sup>1</sup>	H'0060	H'E62C 0010	16	√	√	√	√
	Receive FIFO data register	HSFRDR	R	H'XX	H'E62C 0014	8	√	√	√	√
	FIFO control register	HSFCR	R/W	H'0000	H'E62C 0018	16	√	√	√	√
	FIFO data count register	HSFDR	R	H'0000	H'E62C 001C	16	√	√	√	√
	Serial port register	HSSPTR	R/W	H'00XX	H'E62C 0020	16	√	√	√	√
	Line status register	HLSLR	R/(W)* <sup>2</sup>	H'0000	H'E62C 0024	16	√	√	√	√
	Sampling rate register	HSSRR	R/W	H'000F	H'E62C 0040	16	√	√	√	√
	Serial error register	HSRER	R	H'0000	H'E62C 0044	16	√	√	√	√
	RTS output active trigger register	HSRTGR	R/W	H'000F	H'E62C 0050	16	√	√	√	√
	Receive FIFO data count trigger register	HSRTRGR	R/W	H'0001	H'E62C 0054	16	√	√	√	√
Transmit FIFO data count trigger register	HSTTRGR	R/W	H'0008	H'E62C 0058	16	√	√	√	√	
1	Serial mode register	HSSMR	R/W	H'0000	H'E62C 8000	16	√	√	√	√
	Bit rate register	HSBRR	R/W	H'FF	H'E62C 8004	8	√	√	√	√
	Serial control register	HSSCR	R/W	H'0000	H'E62C 8008	16	√	√	√	√
	Transmit FIFO data register	HSFTDR	W	—	H'E62C 800C	8	√	√	√	√
	Serial status register	HSFSR	R/(W)* <sup>1</sup>	H'0060	H'E62C 8010	16	√	√	√	√
	Receive FIFO data register	HSFRDR	R	H'XX	H'E62C 8014	8	√	√	√	√
	FIFO control register	HSFCR	R/W	H'0000	H'E62C 8018	16	√	√	√	√
	FIFO data count register	HSFDR	R	H'0000	H'E62C 801C	16	√	√	√	√
	Serial port register	HSSPTR	R/W	H'00XX	H'E62C 8020	16	√	√	√	√
	Line status register	HLSLR	R/(W)* <sup>2</sup>	H'0000	H'E62C 8024	16	√	√	√	√
	Sampling rate register	HSSRR	R/W	H'000F	H'E62C 8040	16	√	√	√	√
	Serial error register	HSRER	R	H'0000	H'E62C 8044	16	√	√	√	√
	RTS output active trigger register	HSRTGR	R/W	H'000F	H'E62C 8050	16	√	√	√	√



							RZ/G Series Products			
Ch. No.	Register Name	Abbreviation	R/W	Value after Reset	Address	Access Size	RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
1	Receive FIFO data count trigger register	HSRTRGR	R/W	H'0001	H'E62C 8054	16	√	√	√	√
	Transmit FIFO data count trigger register	HSTTRGR	R/W	H'0008	H'E62C 8058	16	√	√	√	√
2	Serial mode register	HSSMR	R/W	H'0000	H'E62D 0000	16	—	√	√	√
	Bit rate register	HSBRR	R/W	H'FF	H'E62D 0004	8	—	√	√	√
	Serial control register	HSSCR	R/W	H'0000	H'E62D 0008	16	—	√	√	√
	Transmit FIFO data register	HSFTDR	W	—	H'E62D 000C	8	—	√	√	√
	Serial status register	HSFSR	R/(W)* <sup>1</sup>	H'0060	H'E62D 0010	16	—	√	√	√
	Receive FIFO data register	HSFRDR	R	H'XX	H'E62D 0014	8	—	√	√	√
	FIFO control register	HSFCR	R/W	H'0000	H'E62D 0018	16	—	√	√	√
	FIFO data count register	HSFDR	R	H'0000	H'E62D 001C	16	—	√	√	√
	Serial port register	HSSPTR	R/W	H'00XX	H'E62D 0020	16	—	√	√	√
	Line status register	HLSLR	R/(W)* <sup>2</sup>	H'0000	H'E62D 0024	16	—	√	√	√
	Sampling rate register	HSSRR	R/W	H'000F	H'E62D 0040	16	—	√	√	√
	Serial error register	HSRER	R	H'0000	H'E62D 0044	16	—	√	√	√
	RTS output active trigger register	HSRTGR	R/W	H'000F	H'E62D 0050	16	—	√	√	√
	Receive FIFO data count trigger register	HSRTRGR	R/W	H'0001	H'E62D 0054	16	—	√	√	√
Transmit FIFO data count trigger register	HSTTRGR	R/W	H'0008	H'E62D 0058	16	—	√	√	√	

Notes: 1. Only 0 can be written to clear the flags. Bits 15 to 8, 3, and 2 are read-only bits and cannot be modified.

2. Only 0 can be written to clear the flags. Bits 15 to 3, and 1 are read-only bits and cannot be modified.

## 43.2 Register Descriptions

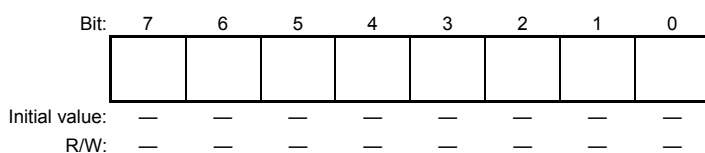
### 43.2.1 Receive Shift Register (HSRSR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

HSRSR is a register that receives serial data.

The HSCIF sets serial data input to the HSRSR from the HRX pin in the order received, starting with the LSB (bit 0), and converts it to parallel data. When one byte of data has been received, it is transferred to the receive FIFO register HSFRDR, automatically.

HSRSR cannot be read from and written to by the CPU.



### 43.2.2 Receive FIFO Data Register (HSFRDR)

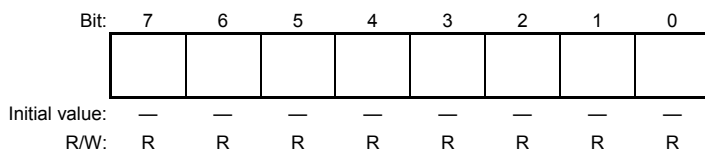
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

HSFRDR is a 128-stage FIFO register that stores received serial data.

When HSCIF has received one byte of serial data, it transfers the received data from the receive shift register (HSRSR) to HSFRDR for storage, and reception is thus completed. HSRSR is then ready for reception, and is capable of receiving up to 128 consecutive bytes of data before HSFRDR is full.

HSFRDR is a read-only register and cannot be modified by the CPU. Note that the read value will be undefined while there is no receive data in HSFRDR. When HSFRDR is full of receive data, subsequent serial data is lost.

HSFRDR is read as an undefined value after a power-on reset.



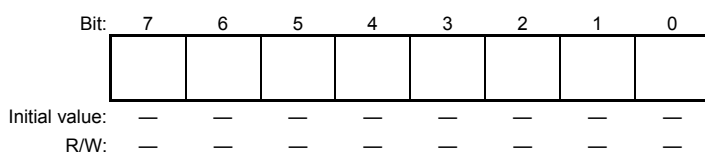
### 43.2.3 Transmit Shift Register (HSTSR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

HSTSR is a register that transmits serial data.

To perform serial data transmission, the HSCIF first transfers transmit data from the transmit fifo data register (HSFTDR) to HSTSR, then sends the data to the HTX pin starting with the LSB (bit 0). When transmission of one byte is completed, the HSCIF transfers the next transmit data from HSFTDR to HSTSR automatically, then starts transmission.

HSTSR cannot be read from and written to directly by the CPU.



### 43.2.4 Transmit FIFO Data Register (HSFTDR)

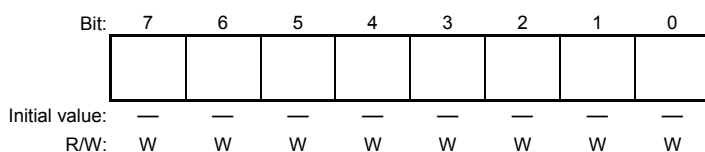
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

HSFTDR is an 8-bit FIFO register of 128 stages that stores data for serial transmission.

If HSTSR is empty after transmit data has been written to HSFTDR, the HSCIF transfers the data from HSFTDR to HSTSR and starts serial transmission.

HSFTDR is a write-only register and cannot be read from by the CPU. Writing further data to HSFTDR is no longer possible when it is full. Attempts at writing data to the register in this situation are ignored.

HSFTDR is read as an undefined value on a power-on reset.



### 43.2.5 Serial Mode Register (HSSMR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	CHR	PE	O/E#	STOP	—	CKS[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R	R/W	R/W

HSSMR is a 16-bit register that sets the HSCIF's serial transfer format and selects the baud rate generator clock source.

HSSMR can always be read from and written to by the CPU.

HSSMR is initialized to H'0000 by a power-on reset.

Bit	Bit Name	Initial Value	R/W	Description
15 to 7	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
6	CHR	0	R/W	Character Length Selects 7 or 8 bits for data length. When the 7-bit data is selected, the MSB (bit 7) in the transmit FIFO data register (HSFTDR) is not transmitted. 0: 8 bits 1: 7 bits
5	PE	0	R/W	Parity Enable Determines whether parity bit is added in transmission or not, and parity bit is checked in reception or not. When bit PE is set to 1, the parity (even or odd) specified by bit O/E# is added to transmit data. In reception, the parity bit is checked for the parity (even or odd) specified by bit O/E#. 0: Disables parity bit addition and check. 1: Enables parity bit addition and check.
4	O/E#	0	R/W	Parity Mode Selects either even or odd parity to use in parity addition and check. The O/E# bit setting is valid only when bit PE is set to 1, enabling parity bit addition and check. 0: Even parity 1: Odd parity When even parity is set, the parity bit is added in transmission so that the total number of 1-bit in the transmit character plus the parity bit is even. In reception, a check is performed to see if the total number of 1-bit in the receive character plus the parity bit is even. When odd parity is set, the parity bit is added in transmission so that the total number of 1-bit in the transmit character plus the parity bit is odd. In reception, a check is performed to see if the total number of 1-bit in the receive character plus the parity bit is odd.

Bit	Bit Name	Initial Value	R/W	Description
3	STOP	0	R/W	<p>Stop Bit Length</p> <p>Selects 1 bit or 2 bits as the stop bit length.</p> <p>In reception, only the first stop bit is checked, regardless of the STOP bit setting. If the second stop bit is 1, it is treated as a stop bit. If it is 0, it is treated as the start bit of the next transmit character.</p> <p>0: 1 stop bit*<sup>1</sup></p> <p>1: 2 stop bits*<sup>2</sup></p> <p>Notes: 1. In transmission, a single 1-bit (stop bit) is added to the end of a transmit character before it is sent.</p> <p>2. In transmission, two 1-bit (stop bits) are added to the end of a transmit character before it is sent.</p>
2	—	0	R	<p>Reserved</p> <p>This bit is always read as 0. The write value should always be 0.</p>
1, 0	CKS[1:0]	00	R/W	<p>Clock Select 1 and 0</p> <p>These bits select the clock source for the on-chip baud rate generator.</p> <p>The clock source can be selected from <math>ZS\phi</math>, <math>ZS\phi/4</math>, <math>ZS\phi/16</math>, and <math>ZS\phi/64</math>, according to the setting of bits CKS[1:0].</p> <p>00: <math>ZS\phi</math></p> <p>01: <math>ZS\phi/4</math></p> <p>10: <math>ZS\phi/16</math></p> <p>11: <math>ZS\phi/64</math></p>

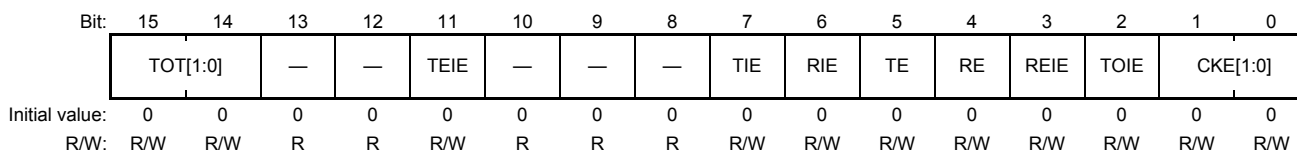
**43.2.6 Serial Control Register (HSSCR)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

HSSCR is a register that enables or disables transmission/reception by the HSCIF, enables or disables interrupt requests, and selects transmission/reception clock source for the HSCIF.

HSSCR can always be read from and written to by the CPU.

HSSCR is initialized to H'0000 by a power-on reset.



Bit	Bit Name	Initial Value	R/W	Description
15, 14	TOT[1:0]	00	R/W	Set the time for a data ready (DR) or a timeout (TO) to be set in asynchronous mode. 00: 15 etu* 01: 31 etu 10: 47 etu 11: 63 etu Note: * ETU: Elementary Time Unit (time for transfer of one bit) Equivalent to 1.5 frames with an 8-bit, 1-stop-bit format.
13, 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11	TEIE	0	R/W	Transmit End Interrupt Enable When a transmit-end request is enabled by the TIE bit, the TEIE bit selects the source of the transmit end interrupt request from the following: • Setting the TDFE flag in HSFSR • Setting the TEND flag in HSFSR 0: The transmit FIFO data empty (TDFE) interrupt request is used. 1: The transmit end (TEND) interrupt request is used.
10 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
7	TIE	0	R/W	<p>Transmit Interrupt Enable</p> <p>Enables or disables a transmit-FIFO-data-empty interrupt (TDFE) request when the TEIE bit in HSSCR is pulled 0, if the following conditions are satisfied:</p> <ul style="list-style-type: none"> <li>Serial transmit data has been transferred from HSFTDR to HSTSR,</li> <li>The number of data bytes in HSFTDR is equal to or less than the transmit trigger count, and</li> <li>The TDFE flag in HSFSR is set to 1.</li> </ul> <p>Enables or disables a transmit-end interrupt (TEND) request when the TEIE bit of HSSCR is set to 1, if the following conditions are satisfied:</p> <ul style="list-style-type: none"> <li>Transmission was ended because there is no valid data in HSFTDR when the last bit of the transmit character in HSTSR was transmitted, and</li> <li>The TEND flag of HSFSR is set to 1.</li> </ul> <p>0: When the TEIE bit is 0, disables transmit-FIFO-data-empty interrupt (TDFE) request. When the TEIE bit is 1, disables transmit-end interrupt (TEND) request.</p> <p>1: When the TEIE bit is 0, enables transmit-FIFO-data-empty interrupt (TDFE) request. When the TEIE bit is 1, enables transmit-end interrupt (TEND) request.</p>
6	RIE	0	R/W	<p>Receive Interrupt Enable</p> <p>Enables or disables a receive-FIFO-data-full interrupt request when the RDF flag in HSFSR is set to 1, a receive-data-ready interrupt request when the DR flag in HSFSR is set to 1, a receive-error interrupt request when the ER flag in HSFSR is set to 1, a break interrupt request when the BRK flag in HSFSR is set to 1, and an overrun error interrupt request when the ORER flag in HSLSR is set to 1.</p> <p>0: Disables receive-FIFO-data-full interrupt (RDF) requests, receive-data-ready interrupt (DR) requests, receive-error interrupt (ER) requests, break interrupt (BRK) requests, and overrun error interrupt (ORER) requests.</p> <p>1: Enables receive-FIFO-data-full interrupt (RDF) requests, receive-data-ready interrupt (DR) requests, receive-error interrupt (ER) requests, break interrupt (BRK) requests, and overrun error interrupt (ORER) requests.</p>
5	TE	0	R/W	<p>Transmit Enable</p> <p>Enables or disables the start of HSCIF serial transmission. The HSCIF starts serial transmission when transmit data is written to the HSFTDR while TE is 1. Before setting TE to 1, set HSSMR and HSFCR to specify the transmission format and reset the transmit FIFO.</p> <p>0: Disables transmission.</p> <p>1: Enables transmission.</p>

Bit	Bit Name	Initial Value	R/W	Description
4	RE	0	R/W	<p>Receive Enable</p> <p>Enables or disables the start of HSCIF serial reception. When RE is 1, the HSCIF starts serial reception by detecting a start bit. Before setting RE to 1, set HSSMR and HSFCR to specify the reception format and reset the receive FIFO.</p> <p>0: Disables reception.*</p> <p>1: Enables reception.</p> <p>Note: * Even if RE is cleared to 0, the DR, ER, BRK, RDF, FER, PER, TO and ORER flags are not affected, and retain their states.</p>
3	REIE	0	R/W	<p>Receive Error Interrupt Enable</p> <p>Enables or Disables generation of receive-error interrupt (ER) requests, break interrupt (BRK) requests and overrun-error interrupt (ORER) requests.</p> <p>0: Disables receive-error interrupt (ER) requests, break interrupt (BRK) requests and overrun-error interrupt (ORER) requests.*</p> <p>1: Enables receive-error interrupt (ER) requests, break interrupt (BRK) requests and overrun-error interrupt (ORER) requests.</p> <p>Note: * When REIE is 1, ER, BRK or ORER interrupt requests will occur even if RIE is cleared to 0. This setting is used to notify the interrupt controller of ER, BRK, and ORER interrupt requests during DMAC transfer.</p>
2	TOIE	0	R/W	<p>Timeout Interrupt Enable</p> <p>Enables or disables generation of timeout interrupt (TO) requests when the TO flag in HSLSR is set to 1.</p> <p>0: Disables timeout interrupts (TO).</p> <p>1: Enables timeout interrupts (TO).</p>
1, 0	CKE[1:0]	00	R/W	<p>Clock Enable 1 and 0</p> <p>These bits select the HSCIF clock source and enables or disables the clock output from the HSCK pin.</p> <p>Whether the HSCK pin functions as a serial clock output pin or a serial clock input pin is determined by CKE[1: 0] bit settings.</p> <p>See Table 43.3 for the bit settings.</p>

**Table 43.3 Clock Selection**

CKE[1]	CKE[0]	Clock Source	HSCK Pin
0	0	Internal clock (ZS $\phi$ , ZS $\phi$ /4, ZS $\phi$ /16, and ZS $\phi$ /64)	The HSCK pin is not used.
0	1		The HSCK pin functions as an input pin (input signals are ignored). (Initial value)
1	0	Baud rate generator output for external clock or HSCK	When SC_CLK is selected: The HSCK pin is an input pin (input signals are ignored). Set the SC_CLK frequency so that the frequency of BRGCLK is multiplied by the sampling rate.
1	1		When HSCK is selected: The HSCK pin inputs the clock (with the bit rate multiplied by the sampling rate).
	1	Prohibited	

Note: It is not allowed to set synchronous communication using SC\_CLK for input.



### 43.2.7 Serial Status Register (HSFSR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

HSFSR is a 16-bit register. The lower 8 bits are status flags that indicate the operating status of the HSCIF, and the upper 8 bits are all reserved.

HSFSR can always be read from and written to by the CPU. However, the flags ER, TEND, TDFE, BRK, RDF, and DR cannot be written by 1. The FER and PER flags are read-only flags and cannot be modified.

HSFSR is initialized to H'0060 by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	ER	TEND	TDFE	BRK	FER	PER	RDF	DR
Initial value:	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R	R	R/(W)*	R/(W)*

Note: \* Only 0 can be written to clear the flag.

Bit	Bit Name	Initial Value	R/W	Description
15 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7	ER	0	R/(W)*	<p>Receive Error</p> <p>Indicates that a framing error or a parity error has occurred in reception. The ER flag is not affected by an error and retains its previous state when the RE bit is 0 in HSSCR.</p> <p>If a receive error occurs, receive data will be transferred to HSFRDR and reception operation will be continued. Whether there is a receive error in data read from HSFRDR can be determined by the FER and PER bits in HSFSR.</p> <p>0: Indicates that no framing or parity error has occurred in reception.</p> <p>[Clearing conditions]</p> <ul style="list-style-type: none"> <li>A power-on reset is executed.</li> <li>0 is written to ER.</li> </ul> <p>1: Indicates that a framing error or a parity error has occurred in reception.</p> <p>[Setting conditions]</p> <ul style="list-style-type: none"> <li>The HSCIF checks whether the stop bit at the end of receive data is 1, but the stop bit is 0.*</li> <li>The number of 1-bit in receive data plus the parity bit does not match the parity setting (even or odd) specified by the O/E# bit in HSSMR during reception.</li> </ul> <p>Note: * In the 2-stop-bit mode, only the first stop bit is checked that the value is 1; the second stop bit is not checked.</p>

Bit	Bit Name	Initial Value	R/W	Description
6	TEND	1	R/(W)*	<p><b>Transmit End</b></p> <p>Indicates that transmission has been ended because there was no valid data in HSFTDR when the last bit of the transmit character was transmitted.</p> <p>0: Indicates that transmission is in progress.</p> <p>[Clearing conditions]</p> <ul style="list-style-type: none"> <li>• Transmit data is written to HSFTDR, and 0 is written to TEND.</li> <li>• Data is written to HSFTDR by the DMAC.</li> </ul> <p>1: Indicates that transmission has been ended.</p> <p>[Setting conditions]</p> <ul style="list-style-type: none"> <li>• A power-on reset is executed.</li> <li>• The TE bit in HSSCR is 0.</li> <li>• There is no transmit data in HSFTDR when the last bit of a 1-byte serial transmission character is transmitted.</li> </ul>
5	TDFE	1	R/(W)*	<p><b>Transmit FIFO Data Empty</b></p> <p>Indicates that the HSCIF has transferred data from HSFTDR to HSTSR, the number of data bytes in HSFTDR becomes equal to or less than the transmit trigger count specified by the HSTTRGR, and HSFTDR is ready to be written by new transmit data.</p> <p>HSFTDR is a 128-byte FIFO register. The maximum number of bytes that can be written to when TDFE = 1 is "128 – [the transmit trigger count]". If data exceeding this value is attempted to be written, the data will be ignored. The number of data bytes in HSFTDR is indicated by the upper bits of HSFDR.</p> <p>If the number of data written in HSFTDR is equal to or less than the transmit trigger count, this bit will be set to 1 even if it is cleared to 0 after it is read as 1.</p> <p>0: Indicates that the number of transmit data written to HSFTDR exceeds the transmit trigger count.</p> <p>[Clearing conditions]</p> <ul style="list-style-type: none"> <li>• Transmit data exceeding the specified transmit trigger count have been written to HSFTDR, and 0 is written to TDFE.</li> <li>• Transmit data exceeding the specified transmit trigger count have been written to HSFTDR by the DMAC.</li> </ul> <p>1: Indicates that the number of transmit data in HSFTDR is equal to or less than the transmit trigger count.</p> <p>[Setting conditions]</p> <ul style="list-style-type: none"> <li>• A power-on reset is executed.</li> <li>• The number of transmit data in HSFTDR is equal to or less than the transmit trigger count after transmission.</li> </ul>

Bit	Bit Name	Initial Value	R/W	Description
4	BRK	0	R/(W)*	<p>Break Detect</p> <p>Indicates that a receive data break signal has been detected. If a break signal is detected, receive data (H'00) transfer to HSFRDR is stopped. After the break is canceled and the receive signal returns to 1, the receive data transfer resumes.</p> <p>0: Indicates that no break signal has been received.</p> <p>[Clearing conditions]</p> <ul style="list-style-type: none"> <li>• A power-on reset is executed.</li> <li>• 0 is written to BRK.</li> </ul> <p>1: Indicates that a break signal has been received.</p> <p>[Setting condition]</p> <ul style="list-style-type: none"> <li>• Data with a framing error is received, followed by the space "0" (low level) for at least one frame length.</li> </ul>
3	FER	0	R	<p>Framing Error</p> <p>Indicates that a framing error has been found in the data that is to be read next from HSFRDR.</p> <p>0: Indicates that there is no framing error in the receive data that is to be read from HSFRDR.</p> <p>[Clearing conditions]</p> <ul style="list-style-type: none"> <li>• A power-on reset is executed.</li> <li>• There is no framing error in the data that is to be read next from HSFRDR.</li> </ul> <p>1: Indicates that there is a framing error in the receive data that is to be read from HSFRDR.</p> <p>[Setting condition]</p> <ul style="list-style-type: none"> <li>• There is a framing error in the data that is to be read next from HSFRDR.</li> </ul>
2	PER	0	R	<p>Parity Error</p> <p>This bit indicates that a parity error has been found in the data that is to be read next from HSFRDR.</p> <p>0: Indicates that there is no parity error in the receive data that is to be read from HSFRDR.</p> <p>[Clearing conditions]</p> <ul style="list-style-type: none"> <li>• A power-on reset is executed.</li> <li>• There is no parity error in the data that is to be read next from HSFRDR.</li> </ul> <p>1: Indicates that there is a parity error in the receive data that is to be read from HSFRDR.</p> <p>[Setting condition]</p> <ul style="list-style-type: none"> <li>• There is a parity error in the data that is to be read next from HSFRDR.</li> </ul>

Bit	Bit Name	Initial Value	R/W	Description
1	RDF	0	R/(W)*	<p>Receive FIFO Data Full</p> <p>Indicates that the received data has been transferred from HRSR to HSFRDR, and the number of receive data bytes in HSFRDR becomes equal to or more than the receive trigger count specified by the HSRTRGR.</p> <p>HSFRDR is a 128-byte FIFO register. When RDF = 1, data equal to or more than the number of receive trigger data bytes can be read. When HSFRDR is empty, HSFRDR is read as an undefined value. The number of receive data bytes in HSFRDR is indicated by the lower bits of HSFRDR.</p> <p>If the number of data in HSFRDR is equal to or more than the trigger count, this bit will be set to 1 even if it is cleared to 0. At this time, read receive data until the number of data in HSFRDR is less than the trigger count, read RDF as 1, and then clear RDF.</p> <p>0: Indicates that the number of receive data bytes in HSFRDR is less than the specified receive trigger count.</p> <p>[Clearing conditions]</p> <ul style="list-style-type: none"> <li>• A power-on reset is executed.</li> <li>• HSFRDR is read until the number of receive data bytes in HSFRDR is less than the receive trigger count, and 0 is written to RDF.</li> <li>• HSFRDR is read by the DMAC until the number of receive data bytes in HSFRDR is less than the receive trigger count.</li> </ul> <p>1: Indicates that the number of receive data bytes in HSFRDR is equal to or more than the specified receive trigger count.</p> <p>[Setting condition]</p> <ul style="list-style-type: none"> <li>• Receive data more than the receive trigger count have been stored in HSFRDR.</li> </ul>

Bit	Bit Name	Initial Value	R/W	Description
0	DR	0	R/(W)*	<p>Receive Data Ready</p> <p>Indicates that the receive FIFO data register (HSFRDR) contains fewer bytes than the trigger number for reception and no further data have arrived over at least the time corresponding to the setting of HSSCR[15:14]* since the stop bit for the byte to have been received.</p> <p>0: Indicates that data is being received or has been successfully received, and there is no receive data in HSFRDR.</p> <p>[Clearing conditions]</p> <ul style="list-style-type: none"> <li>• A power-on reset is executed.</li> <li>• All the receive data in HSFRDR has been read, and 0 is written to DR.</li> <li>• All the receive data in HSFRDR has been read by the DMAC.</li> </ul> <p>1: Indicates that no further receive data has been received.</p> <p>[Setting condition]</p> <p>The receive FIFO data register (HSFRDR) contains fewer bytes than the trigger number for reception and no further data have arrived over at least the time corresponding to the setting of HSSCR[15:14]* since the stop bit for the byte to have been received.</p> <p>Note: * When the setting is 00, the time is 15 etu. This is equivalent to 1.5 frames in an 8-bit, 1-stop-bit format.</p> <p>etu: Elementary Time Unit (time for transfer of one bit)</p>

Note: \* Only 0 can be written to clear the flag.

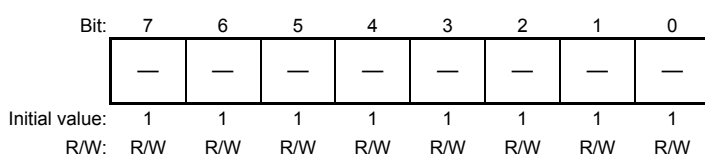
### 43.2.8 Bit Rate Register (HSBRR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

HSBRR is an 8-bit register that sets the serial transmission/reception bit rate in accordance with the baud rate generator operating clock selected by the CKS[1:0] bits in HSSMR. This baud rate generator is intended for  $ZS\phi$ ,  $ZS\phi/4$ ,  $ZS\phi/16$ , and  $ZS\phi/64$ . For details on the baud rate generator for external clock, see section 43.5, Baud Rate Generator for External Clock (BRG).

HSBRR can always be read from and written to by the CPU except for during transfer.

HSBRR is initialized to H'FF by a power-on reset.



The HSBRR setting is determined by the following equation:

[Asynchronous mode]

$$N = \frac{ZS\phi}{Sr \times 2^{2n+1} \times B} \times 10^6 - 1$$

B: Bit rate (bit/s)

N: HSBRR setting for the baud rate generator ( $0 \leq N \leq 255$ ) (which satisfies the electrical characteristics)

$ZS\phi$ : AXI bus clock operating frequency (MHz)

n: Baud rate generator input clock ( $n = 0, 1, 2, 3$ )  
(See the Table 43.4 for the relation between n and the clock.)

Sr: Sampling rate (8 to 32)

**Table 43.4 HSSMR Settings**

n	Baud Rate Generator Input Clock	HSSMR Setting	
		CKS[1]	CKS[0]
0	$ZS\phi$	0	0
1	$ZS\phi/4$	0	1
2	$ZS\phi/16$	1	0
3	$ZS\phi/64$	1	1

The bit rate error in asynchronous mode is determined by the following equation:

$$\text{error (\%)} = \left\{ \frac{ZS\phi \times 10^6}{(N+1) \times B \times Sr \times 2^{2n+1}} - 1 \right\} \times 100$$

### 43.2.9 FIFO Control Register (HSFCR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

HSFCR is a register that resets data counts for the transmit and receive FIFO registers. It also has a modem control and a loopback test enable bit.

HSFCR can always be read from and written to by the CPU except for during transfer.

HSFCR is initialized to H'0000 by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	MCE	TFRST	RFRST	LOOP
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3	MCE	0	R/W	Modem Control Enable Enables or disables modem control signals HCTS# and HRTS#. 0: Disables modem signals.* 1: Enables modem signals. Note: * HCTS# and HRTS# control ports.
2	TFRST	0	R/W	Transmit FIFO Data Register Reset Enables or disables a transmit FIFO data register reset that empties the register. 0: Disables the reset.* 1: Enables the reset. Note: * The register is reset by a power-on reset.
1	RFRST	0	R/W	Receive FIFO Data Register Reset Enables or disables a receive FIFO data register (HSFRDR) reset that empties the register. 0: Disables the reset.* 1: Enables the reset. Note: * The register is reset by a power-on reset.
0	LOOP	0	R/W	Loopback Test Enables or disables the loopback test by internally connecting the transmit output pin (HTX) and receive input pin (HRX), and the HRTS# pin and HCTS# pin. 0: Disables the loopback test. 1: Enables the loopback test.

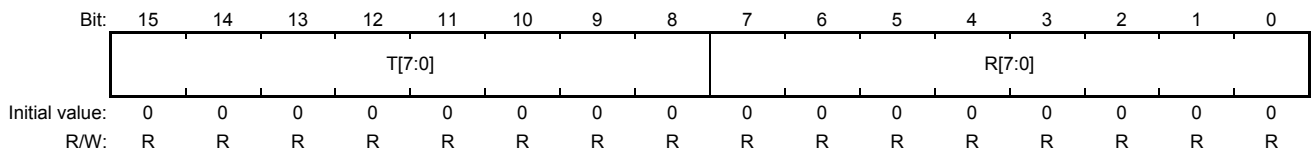
**43.2.10 FIFO Data Count Register (HSFDR)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

HSFDR is a 16-bit register that indicates the number of data bytes stored in HSFTDR and that in HSFRDR.

The upper 8 bits indicate the number of transmit data bytes in HSFTDR, and the lower 8 bits indicates the number of receive data bytes in HSFRDR.

HSFDR can always be read by the CPU.



Bit	Bit Name	Initial Value	R/W	Description
15 to 8	T[7:0]	H'00	R	These bits indicate the number of data bytes untransmitted and still stored in HSFTDR. H'00 indicates that there is no transmit data in HSFTDR, and H'80 indicates that HSFTDR is full of transmit data.
7 to 0	R[7:0]	H'00	R	These bits indicate the number of receive data stored in HSFRDR. H'00 indicates that there is no receive data in HSFRDR, and H'80 indicates that HSFRDR is full of receive data.



### 43.2.11 Serial Port Register (HSSPTR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

HSSPTR controls multiplexed input/output and data on the high speed serial communication interface (HSCIF) ports. Bits 1 and 0 control breaks in serial transmission/reception by reading input data from the HRX pin and writing output data to the HTX pin. Bits 3 and 2 read input data from and write output data to the HSCK pin. Bits 5 and 4 read input data from and write output data to the HCTS# pin. Bits 7 and 6 read input data from and write output data to the HRTS# pin.

HSSPTR is a 16-bit register that can always be read from and written to by the CPU.

All HSSPTR bits except bits 6, 4, 2, and 0 are initialized to 0 by a power-on reset. The values of bits 6, 4, 2, and 0 are undefined.

Note: Whether modem control can be selected or not depends on the channel.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	RTSIO	RTSDT	CTSIO	CTSDT	SCKIO	SCKDT	SPB 2IO	SPB 2DT
Initial value:	0	0	0	0	0	0	0	0	0	—	0	—	0	—	0	—
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7	RTSIO	0	R/W	Serial Port – RTS Port Input/Output Specifies input or output for the serial port HRTS# pin. To actually set the HRTS# pin as a port output pin to output the value set by the RTSDT bit, the MCE bit in HSFCR should be cleared to 0. 0: Indicates that this bit does not output the value of the RTSDT bit to the HRTS# pin. 1: Indicates that this bit outputs the value of the RTSDT bit to the HRTS# pin.
6	RTSDT	—	R/W	Serial Port – RTS Port Data Specifies the input/output data level of the serial port HRTS# pin. Whether the pin is set for input or output is determined by the RTSIO bit. When the pin is set for output, the value of the RTSDT bit is output to the HRTS# pin. Regardless of the value of the RTSIO bit, the value of the HRTS# pin is read from the RTSDT bit. The initial value of this bit is undefined after a power-on reset. 0: Indicates that the input/output data is low level. 1: Indicates that the input/output data is high level.
5	CTSIO	0	R/W	Serial Port – CTS Port Input/Output Specifies input or output for the serial port HCTS# pin. To actually set the HCTS# pin as a port output pin to output the value set by the CTSDT bit, the MCE bit in HSFCR should be cleared to 0. 0: Indicates that the CTSDT bit value is not output to the HCTS# pin. 1: Indicates that the CTSDT bit value is output to the HCTS# pin.

Bit	Bit Name	Initial Value	R/W	Description
4	CTS DT	—	R/W	<p>Serial Port – CTS Port Data</p> <p>Specifies the input/output data level of the serial port HCTS# pin. Whether the pin is set for input or output is determined by the CTSIO bit. When the pin is set for output, the value of the CTS DT bit is output to the HCTS# pin. Regardless of the value of the CTSIO bit, the value of the HCTS# pin is read from the CTS DT bit.</p> <p>The initial value of this bit is undefined after a power-on reset.</p> <p>0: Indicates that the input/output data is low level.</p> <p>1: Indicates that the input/output data is high level.</p>
3	SCKIO	0	R/W	<p>Serial Port – Clock Port Input/Output</p> <p>Specifies input or output for the serial port HSCK pin. To actually set the HSCK pin as a port output pin to output the value set by the SCKDT bit, the CKE1 and CKE0 bits in HSSCR should be cleared to 0.</p> <p>0: Indicates that the SCKDT bit value is not output to the HSCK pin.</p> <p>1: Indicates that the SCKDT bit value is output to the HSCK pin.</p>
2	SCKDT	—	R/W	<p>Serial Port – Clock Port Data</p> <p>Specifies the input/output data level of the serial port HSCK pin. Whether the pin is set for input or output is determined by the SCKIO bit. When the pin is set for output, the value of the SCKDT bit is output to the HSCK pin. Regardless of the value of the SCKIO bit, the value of the HSCK pin is read from the SCKDT bit.</p> <p>The initial value of this bit is undefined after a power-on reset.</p> <p>0: Indicates that the input/output data is low level.</p> <p>1: Indicates that the input/output data is high level.</p>
1	SPB2IO	0	R/W	<p>Serial Port – Break Input/Output</p> <p>Specifies the output condition of the serial port HTX pin. To actually set the HTX pin as a port output pin to output the value set by the SPB2DT bit, the TE bit in HSSCR should be cleared to 0.</p> <p>0: Indicates that the SPB2DT bit value is not output to the HTX pin.</p> <p>1: Indicates that the SPB2DT bit value is output to the HTX pin.</p>
0	SPB2DT	—	R/W	<p>Serial Port – Break Data</p> <p>Specifies the input level of the serial port HRX pin and the output level of the HTX pin. The HTX pin output conditions are determined by the SPB2IO bit. When the HTX pin is set for output, the value of the SPB2DT bit is output to the HTX pin. Regardless of the value of the SPB2IO bit, the value of the HRX pin is read from the SPB2DT bit.</p> <p>The initial value of this bit is undefined after a power-on reset.</p> <p>0: Indicates that the input/output data is low level.</p> <p>1: Indicates that the input/output data is high level.</p>

**43.2.12 Line Status Register (HLSLR)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	TO	—	ORER
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R/(W)*	R	R/(W)*

Note: \* Only 0 can be written to clear the flag.

Bit	Bit Name	Initial Value	R/W	Description
15 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2	TO	0	R/(W)*	Timeout Indicates that the receive FIFO data register (HSFRDR) contains fewer bytes than the trigger number for reception and no further data have arrived over at least the time corresponding to the setting of HSSCR[15:14]* since the stop bit for the byte to have been received. 0: Indicates that data is being received or has been successfully received and that there is no receive data in HSFRDR. [Clearing conditions] <ul style="list-style-type: none"> <li>A power-on reset is executed.</li> <li>All the receive data in the HSFRDR has been read, and 0 is written to TO.</li> </ul> 1: Indicates that no further receive data has been received (receive timeout). [Setting condition] <ul style="list-style-type: none"> <li>The receive FIFO data register (HSFRDR) contains fewer bytes than the trigger number for reception and no further data have arrived over at least the time corresponding to the setting of HSSCR[15:14]* since the stop bit for the byte to have been received.*</li> </ul> Note: * When the setting is 00, the time is 15 etu. This is equivalent to 1.5 frames in an 8-bit, 1-stop-bit format. etu: Elementary Time Unit (time for transfer of one bit)
1	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
0	ORER	0	R/(W)*	<p>Overrun Error</p> <p>Indicates that an overrun error has occurred in reception and abnormal termination is caused.</p> <p>If an overrun error occurs, the receive data prior to the overrun error is retained in HSFRDR and the data received subsequently is discarded.</p> <p>Any subsequent serial reception is disabled while the ORER flag is 1.</p> <p>To resume data reception after clearing the ORER flag, be sure to first read (or clear) data in the receive FIFO and handle the error, then clear the ORER flag.</p> <p>0: Indicates that data is being received or has been successfully received.</p> <p>[Clearing conditions]</p> <ul style="list-style-type: none"> <li>• A power-on reset is executed.</li> <li>• 0 is written to ORER.</li> </ul> <p>1: Indicates that an overrun error has occurred in reception.</p> <p>[Setting condition]</p> <ul style="list-style-type: none"> <li>• The next serial reception has been completed while HSFRDR is full of 128-byte data.</li> </ul> <p>Note: When bit RE in HSSCR is cleared to 0, the ORER flag is not affected and its previous state is retained.</p>

Note: \* Only 0 can be written to clear the flag.

### 43.2.13 Sampling Rate Register (HSSRR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SRE	SRDE	—	—	SRHP[3:0]				—	—	—	SRCYC[4:0]				
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
R/W:	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	SRE	0	R/W	Sampling Rate Register Enable (SRE) 0: Set the SRCYC[4: 0] bits to 15 (initial value). 1: Validates the setting of the SRCYC[4:0] bits.
14	SRDE	0	R/W	Sampling Point Register Enable (SRDE) 0: Invalidates the setting of the SRHP[3:0] bits and the sampling point will be (S+1)/2 for an odd sampling rate (S) and S/2 for an even sampling rate. 1: Validates the setting of the SRHP[3: 0] bits.
13, 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11 to 8	SRHP[3:0]	0000	R/W	Sampling Point Register (SRHP) The sampling point can be moved by setting the SDRE bit to 1 and setting a value in these bits. Normally, the sampling point is the point of S/2 or (S+1)/2 for a sampling rate of S. By setting a signed 4-bit integer in these bits, the sampling point can be shifted by the amount of the specified sampling clock cycles. This will improve the receive margin. When setting a value in these bits, take notice that the sampling point does not become a negative value or it does not exceed the sampling rate. The shifted sampling point must satisfy the setup margin and hold margin.
7 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4 to 0	SRCYC[4:0]	01111	R/W	Bits 4 to 0: Sampling Rate Register (SRCYC) Data transfer at a desired sampling rate can be enabled by setting the SRE bit to 1 and setting a value in these bits. Set a value of "S - 1" in these bits for a sampling rate of S. Note that the sampling rate must be from 8 to 32 (a value from 7 to 31 can be set in these bits). Set these bits to 15 (initial value) when the SRE bit is set to 0.

**43.2.14 Serial Error Register (HSRER)**

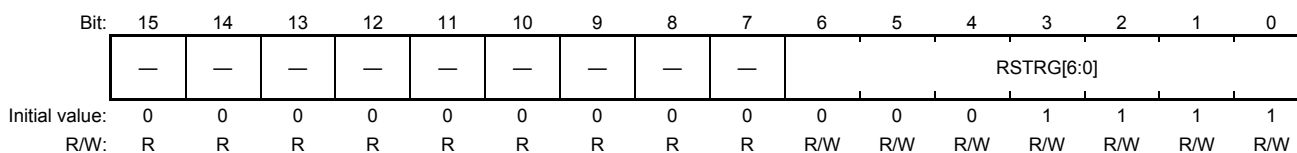
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	PER[6:0]						—	FER[6:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
14 to 8	PER[6:0]	H'00	R	Parity Error Count These bits indicate the number of data items in which a parity error occurred in the receive data stored in the receive FIFO data register (HSFRDR). After the ER bit in HSFSR is set, the value in bits 14 to 8 will be the number of data items in which a parity error occurred. If all 128 bytes of receive data in HSFRDR have parity errors, bits PER[6:0] will have the value 0.
7	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
6 to 0	FER[6:0]	H'00	R	Framing Error Count These bits indicate the number of data items in which a framing error occurred in the receive data stored in the receive FIFO data register (HSFRDR). After the ER bit in HSFSR is set, the value in bits 6 to 0 will be the number of data items in which a framing error occurred. If all 128 bytes of receive data in HSFRDR have framing errors, bits FER[6:0] will have the value 0.

### 43.2.15 RTS Output Active Trigger Register (HSRTGR)

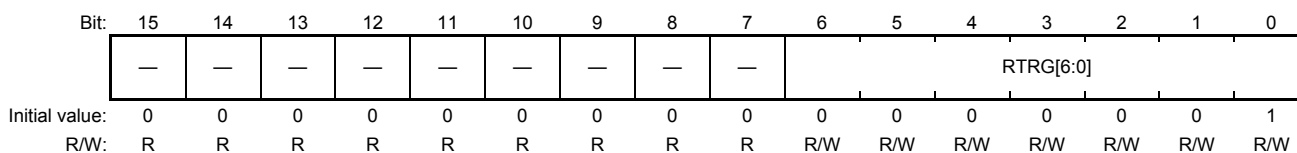
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√



Bit	Bit Name	Initial Value	R/W	Description
15 to 7	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
6 to 0	RSTRG[6:0]	H'0F	R/W	RTS Output Active Trigger Count The HRTS# signal goes high when the number of receive data items stored in the receive FIFO data register (HSFRDR) exceeds the value set in these bits. The initial value is 15.

### 43.2.16 Receive FIFO Data Count Trigger Register (HSRTRGR)

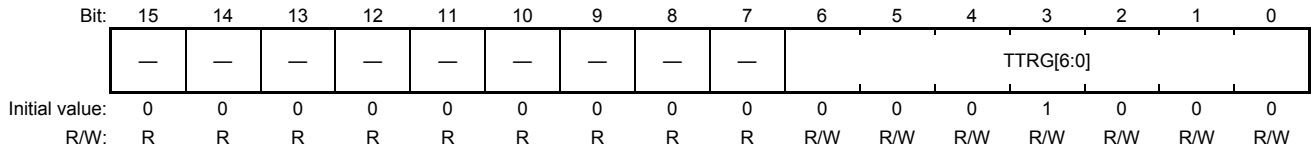
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√



Bit	Bit Name	Initial Value	R/W	Description
15 to 7	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
6 to 0	RTRG[6:0]	H'01	R/W	Receive FIFO Data Count Trigger These bits set the receive data item count at which the receive data full (RDF) flag in the serial status register (HSFSR) is set. The RDF flag is set when the number of receive data items stored in the receive FIFO data register (HSFRDR) equals or exceeds the value set in these bits. The initial value is 1.

**43.2.17 Transmit FIFO Data Count Trigger Register (HSTTRGR)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√



Bit	Bit Name	Initial Value	R/W	Description
15 to 7	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
6 to 0	TTRG[6:0]	H'08	R/W	Transmit FIFO Data Count Trigger These bits set the untransmitted data item count at which the transmit FIFO data register empty (TDFE) flag in the serial status register (HSFSR) is set. The TDFE flag is set when the number of transmit data items in the transmit FIFO data register (HSFTDR) falls under the value set in these bits due to transmit operations. The initial value is 8.



## 43.3 Operation

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

### 43.3.1 Operation in Asynchronous Serial Communication Mode

In asynchronous serial communication mode, the HSCIF performs serial communication, in which data is transmitted/received in character units using the attached start bit indicating the start of communication and stop bit indicating the end of communication.

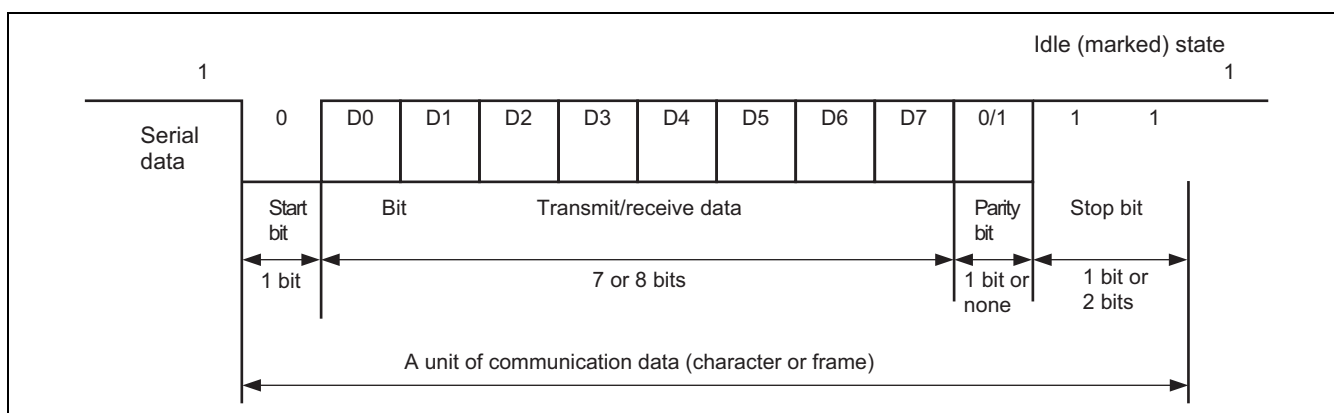
Figure 43.2 shows the general format for asynchronous serial communication.

In asynchronous serial communication, the transmission line is usually kept marked (high level). The HSCIF monitors the transmission line, and when it finds a space (low level), it regards the space as a start bit and starts serial communication.

One character in serial communication consists of a start bit (low level), followed by transmit/receive data (LSB-first; from the lowest bit), a parity bit (high or low level), and a stop bit (high level).

During reception in asynchronous mode, the HSCIF performs synchronization at the falling edge of the start bit. Transferred data is acquired at the center of each bit because the HSCIF samples on  $S/2$ th cycles of the clock which has a frequency of  $S$  times the bit rate, when the sampling rate as set in the sampling rate register (HSSRR) is  $S$  (if the sampling-rate setting is an odd number, the data is sampled on every  $(S+1)/2$ th pulse).

In addition, when the setting of the SRDE bit makes the setting of the sampling point bits effective, the point where the bits are latched can be intentionally moved from the centers of each bit.



**Figure 43.2 Data Format in Asynchronous Mode  
(Example of 8-Bit Data with Parity and Two Stop Bits)**

**(1) Transmission/reception format**

Table 43.5 shows available data transfer formats. The HSCIF supports 8 transfer formats, which can be specified by HSSMR.

**Table 43.5 Serial Transmission/Reception Formats (Asynchronous Mode)**

SCSMR settings			Serial transmission/reception format and frame length												
CHR	PE	STOP	1	2	3	4	5	6	7	8	9	10	11	12	
0	0	0	S	8-bit data								STOP			
0	0	1	S	8-bit data								STOP	STOP		
0	1	0	S	8-bit data								P	STOP		
0	1	1	S	8-bit data								P	STOP	STOP	
1	0	0	S	7-bit data							STOP				
1	0	1	S	7-bit data							STOP	STOP			
1	1	0	S	7-bit data							P	STOP			
1	1	1	S	7-bit data							P	STOP	STOP		

[Legend]

S : Start bit  
 STOP: Stop bit  
 P : Parity bit

**(2) Clock**

The transfer clock can be selected from the following two clocks using the CKE[1:0] bits in HSSCR:

- Internal clock generated by the on-chip baud rate generator
- External clock generated by an external clock baud rate generator

### (3) Data transmission/reception

#### (a) Initialization of HSCIF (asynchronous mode)

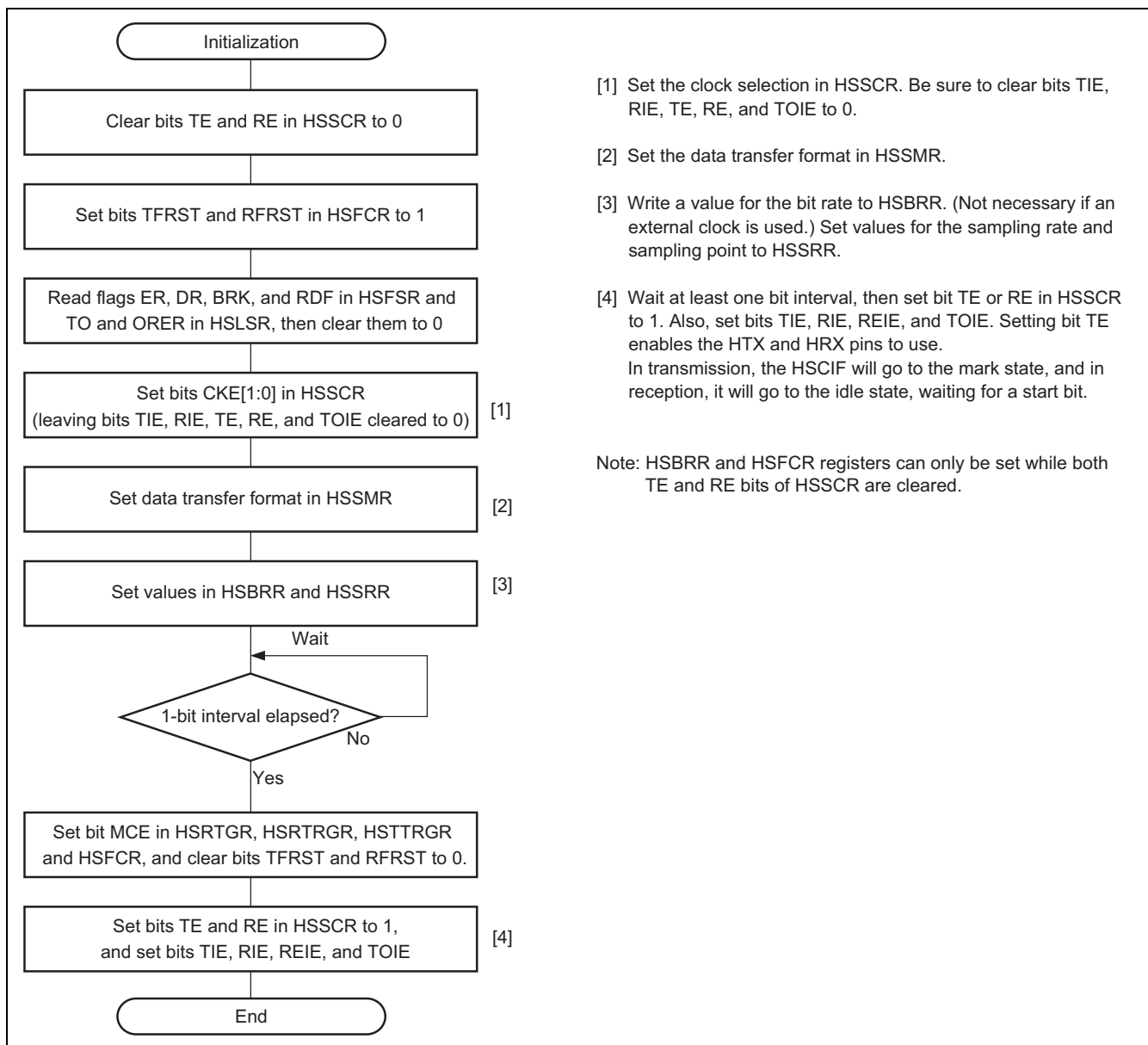
Before transmitting/receiving data or changing the operating mode or communication format, the HSCIF should be initialized using the sample flowchart for HSCIF initialization shown in Figure 43.3.

[Notes]

Clearing the TE bit to 0 initializes HSTSR. However, HSFSR, HSFTDR, and HSFRDR contents are retained even if the TE and RE bits are cleared to 0.

The TE bit should be cleared to 0 after all transmit data has been sent and the TEND flag has been set in HSFSR. The TE bit can be cleared to 0 during transmission, but the data being transmitted will enter the marked state after clearing. In addition, before setting the TE bit to 1 to restart the transmission, set the TFRST bit to 1 in HSFCR to reset HSFTDR.

When an external clock is used, do not stop the clock during operation or initialization. If stopped, the operation will be unreliable. Furthermore, when the baud rate generator for external clock is also to be used, be sure to make settings for it before starting initialization of the HSCIF.



**Figure 43.3 Sample Flowchart for Initializing the HSCIF**

**(b) Serial data transmission (asynchronous mode)**

Figure 43.4 shows a sample flowchart for serial transmission.

After the HSCIF transmission operation is enabled, serial data transmission can be performed using the following procedure:

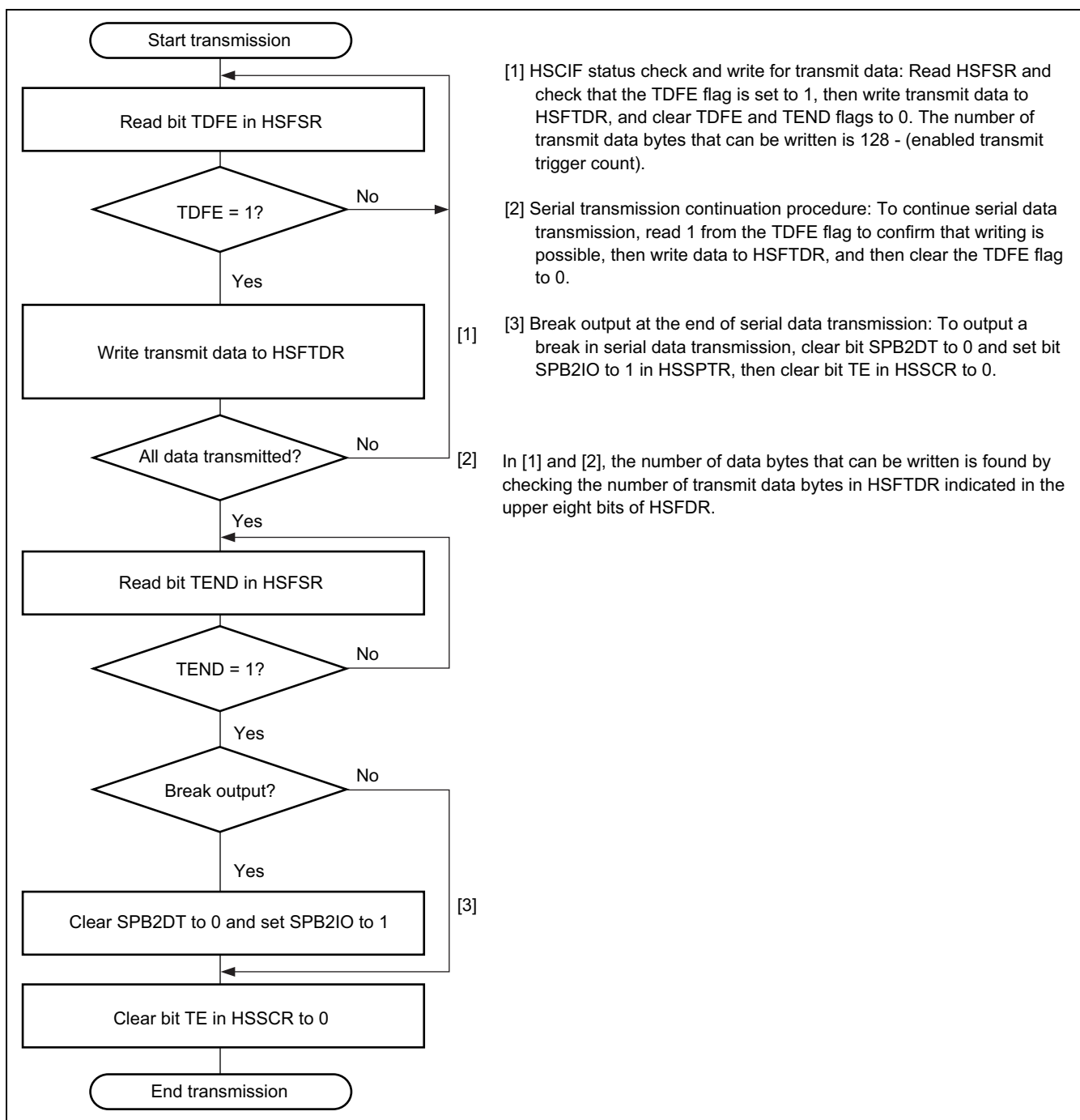
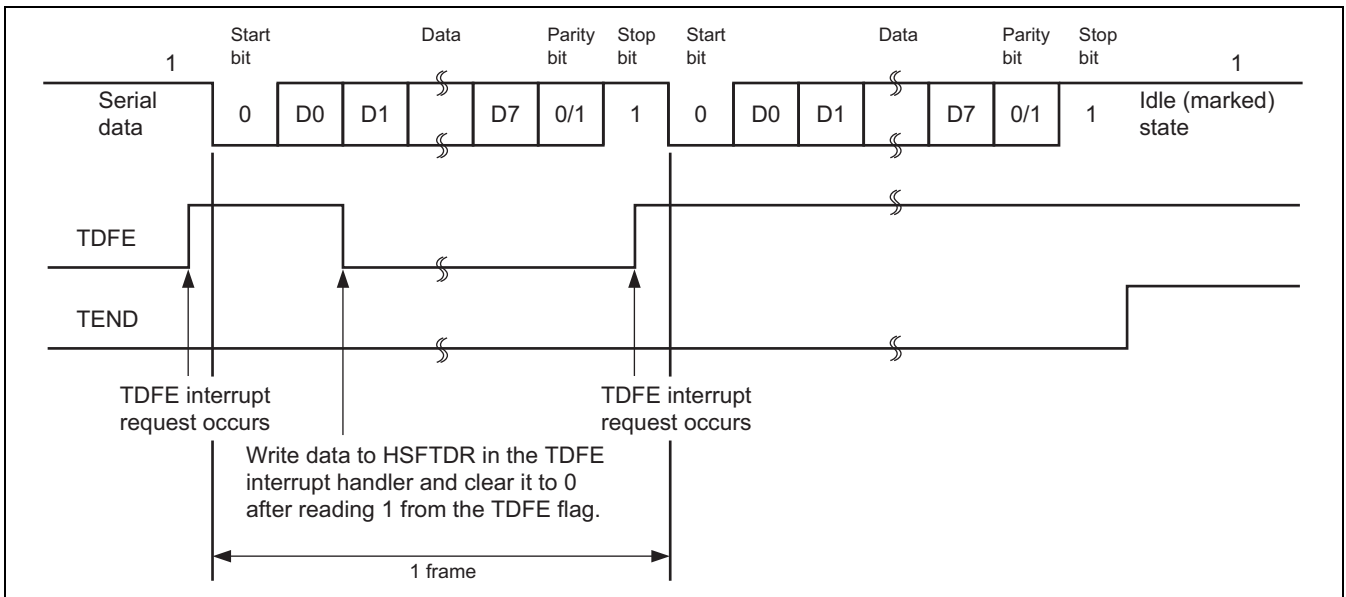


Figure 43.4 Sample Flowchart for Serial Transmission

In serial transmission, the HSCIF operates as follows:

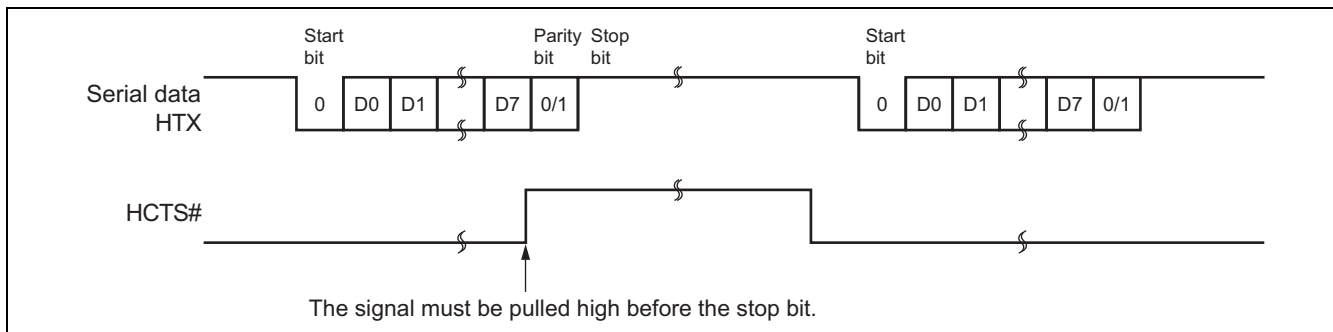
1. When data is written to HSFTDR, the HSCIF transfers the data from HSFTDR to HSTSR and starts transmitting. Confirm that the TDFE flag in HSF SR is set to 1 before writing transmit data to HSFTDR. The number of data bytes that can be written is at least 128 - (transmit trigger count).
2. When data is transferred from HSFTDR to HSTSR and the HSCIF starts transmission, consecutive transmission is performed until there is no transmit data left in HSFTDR. When the number of transmit data bytes in HSFTDR is equal to or less than the transmit trigger count specified in HSTTRGR, the TDFE flag is set. If the TIE and TEIE bits in HSSCR are set to 1 and 0, respectively at this time, a transmit-FIFO-data-empty interrupt (TDFE) request occurs. The serial transmit data is sent from the HTX pin in the following order:
  - A. Start bit: One 0-bit is output.
  - B. Transmit data: 8- or 7-bit data is output in LSB-first order.
  - C. Parity bit: One parity bit (even or odd parity) is output.  
A format that does not output a parity bit can also be selected.
  - D. Stop bit(s): One or two 1-bit (stop bits) are output.
  - E. Marked state: 1 is output continuously until the start bit that starts the next transmission is sent.
3. The HSCIF checks transmit data in HSFTDR when sending the stop bit. If there is data in it, the HSCIF transfers the data from HSFTDR to HSTSR, sends the stop bit, and then starts serial transmission of the next frame. If there is no transmit data, the HSCIF sets the TEND flag to 1 in HSF SR and sends out the stop bit, and then the marked state is entered to output 1 continuously. At this time, if the TIE and TEIE bits in HSSCR are set to 1, a transmit-end interrupt (TEND) request occurs.

Figure 43.5 shows an example of transmission in asynchronous mode.



**Figure 43.5 Sample HSCIF Transmission Operation (Example of 8-Bit Data with Parity and One Stop Bit)**

- When modem control is enabled, transmission can be stopped or resumed in accordance with the HCTS# input value. When HCTS# is set to 1 during transmission, the marked state is entered after one frame of data transmission is ended. Setting HCTS# to 0 restarts outputting the next transmit data from the start bit. Figure 43.6 shows an example of the operation with modem control enabled.

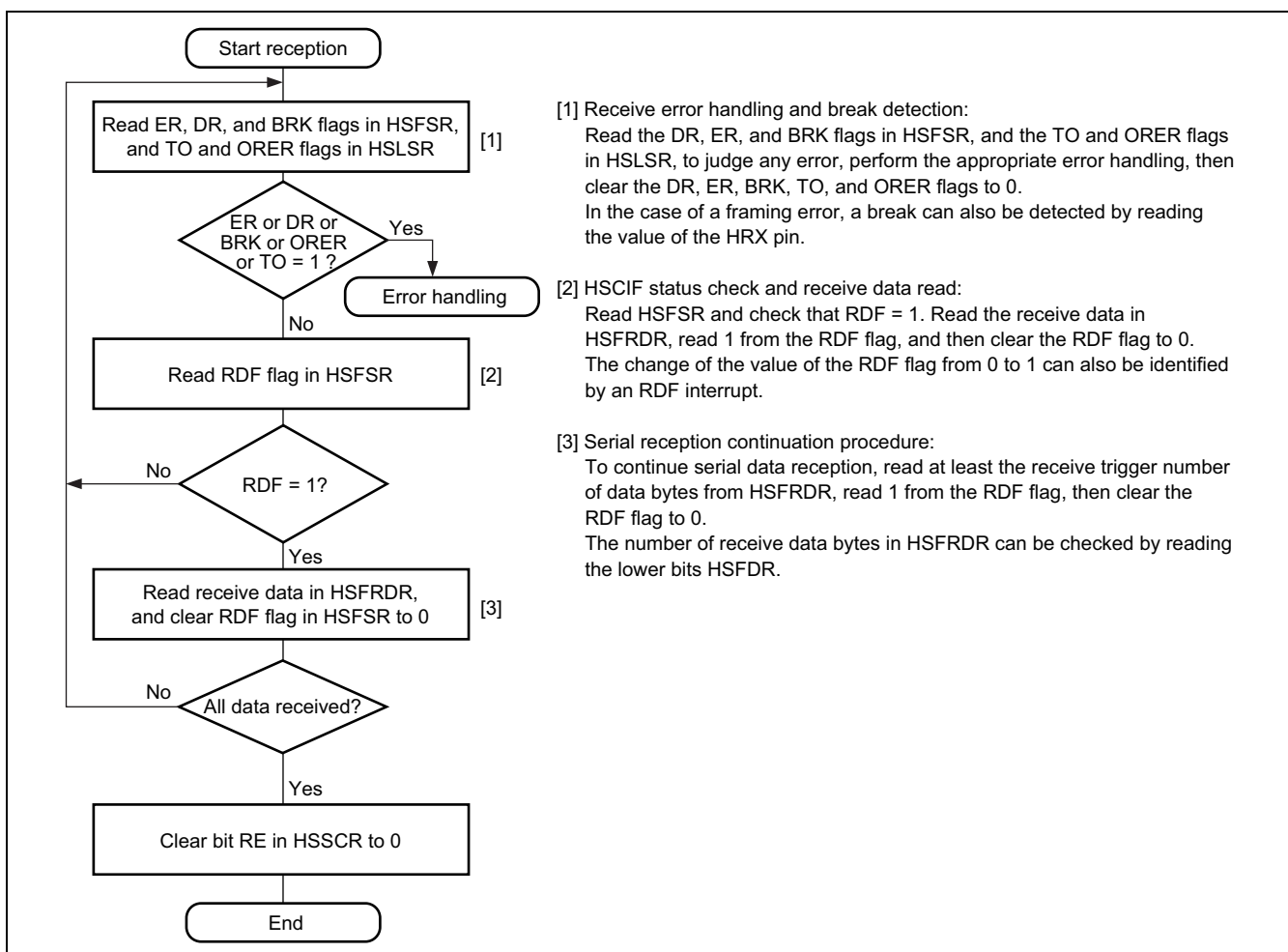


**Figure 43.6 Sample Operation with Modem Control Enabled (HCTS#)**

**(c) Serial data reception (asynchronous mode)**

Figures 43.7 and 43.8 show sample flowcharts for serial reception.

After the HSCIF reception operation is enabled, serial data reception can be performed using the following procedure:



**Figure 43.7 Sample Flowchart for Serial Reception (1)**

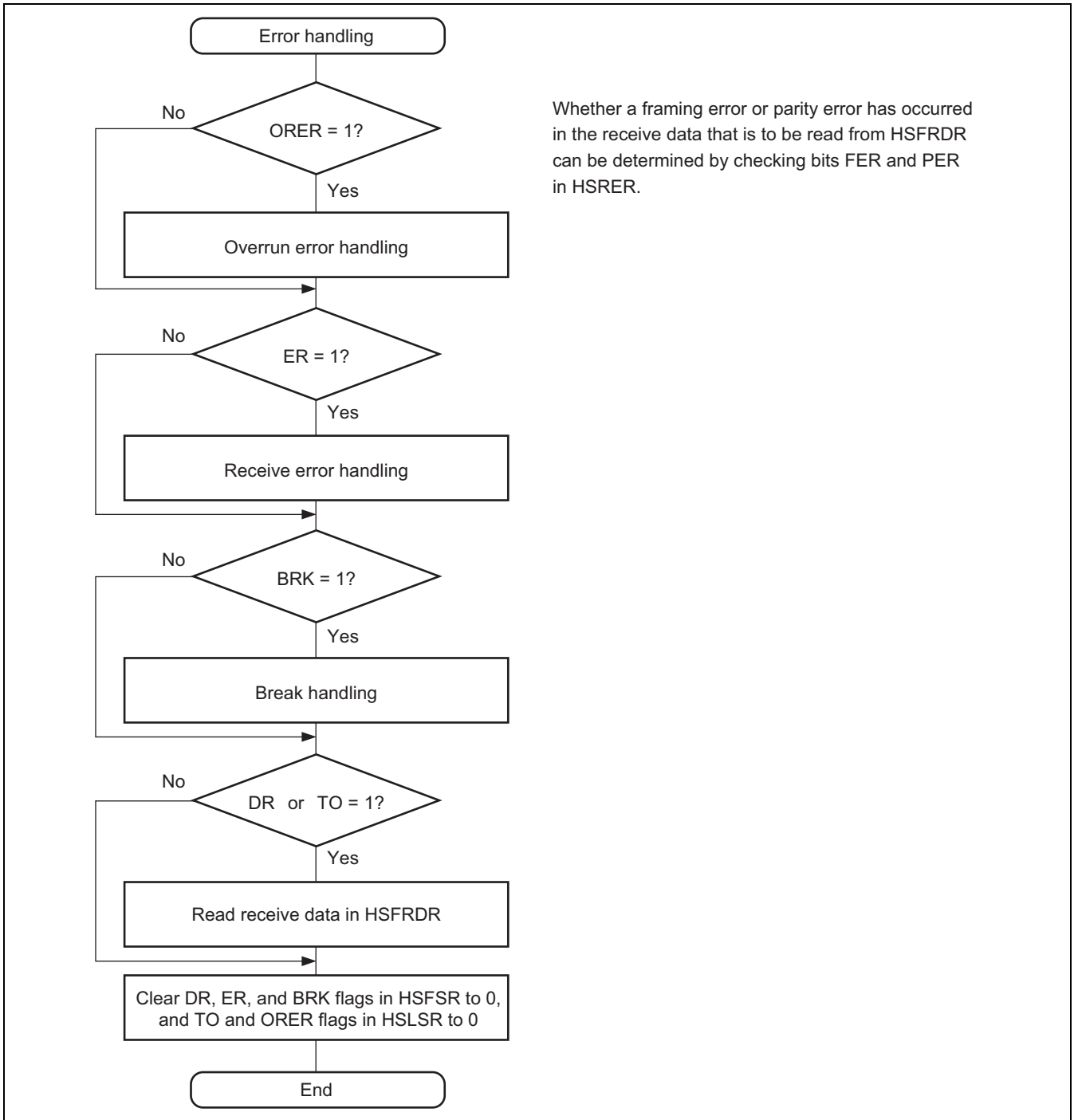


Figure 43.8 Sample Flowchart for Serial Reception (2)



In serial reception, the HSCIF operates as follows:

1. The HSCIF monitors the transmission line, and when detecting the start bit 0, it performs internal synchronization and starts reception.
2. The HSCIF stores the received data in HRSR in LSB-to-MSB order.
3. The HSCIF receives the parity bit and stop bit.

After receiving these bits, the HSCIF performs the following checks:

- A. Stop bit: The HSCIF checks whether the stop bit is 1.  
If there are two stop bits, it checks only the first stop bit.
- B. Receive data: The HSCIF checks that receive data can be transferred from the receive shift register (HRSR) to HSFRDR.
- C. Overrun error: The HSCIF checks that the ORER flag is 0, indicating that no overrun error has occurred.
- D. Break state: The HSCIF checks that the BRK flag is 0, indicating that the break state is not set.

If the HSCIF can confirm the conditions of (b), (c), and (d), it stores the receive data in HSFRDR.

Note: The HSCIF continues to receive data even when a parity error or a framing error occurs.

4. If the RDF flag changes to 1 while the RIE bit in HSSCR is 1, a receive-FIFO-data-full interrupt (RDF) request occurs.

If the DR flag changes to 1 while the RIE bit in HSSCR is 1, a receive-data-ready interrupt (DR) request occurs.

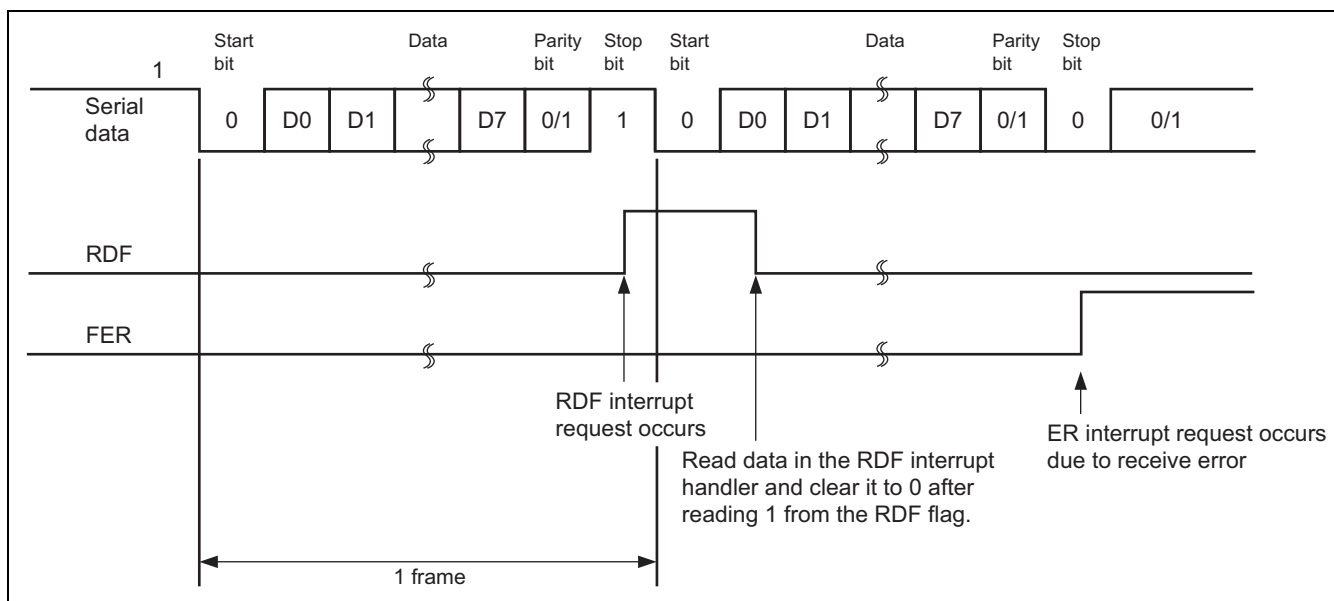
If the TO flag changes to 1 while the TOIE bit in HSSCR is 1, a timeout interrupt (TO) request occurs.

If the ER flag changes to 1 while the RIE or REIE bit in HSSCR is 1, a receive-error interrupt (ER) request occurs.

If the BRK flag changes to 1 while the RIE or REIE bit in HSSCR is 1, a break interrupt (BRK) request occurs.

If the ORER flag changes to 1 while the RIE or REIE bit in HSSCR is 1, an overrun-error interrupt (ORER) request occurs.

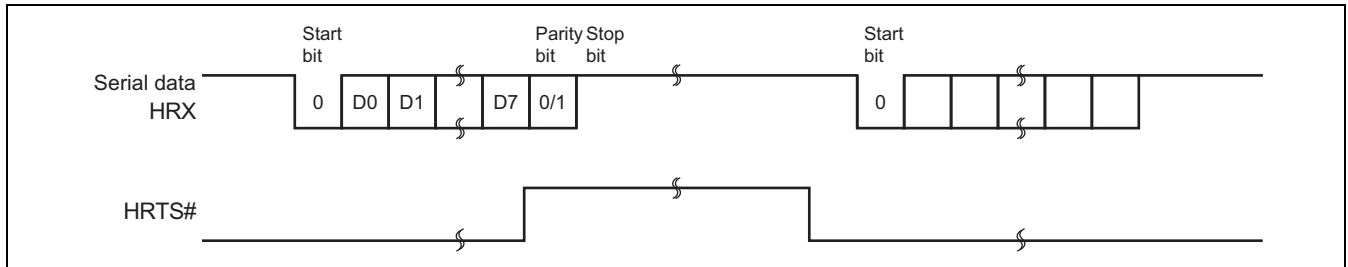
Figure 43.9 shows an example of reception in asynchronous mode.



**Figure 43.9 Sample HSCIF Receive Operation  
(Example of 8-Bit Data with Parity and One Stop Bit)**

- When modem control is enabled, the HRTS# signal is output when HSRDR is empty. When HRTS# is 0, data can be received. When HRTS# is set to 1, the number of data bytes in HSRDR is equal to or more than the RTS output active trigger count.

Figure 43.10 shows an example of the operation with modem control enabled.



**Figure 43.10 Example of the Operation with Modem Control Enabled (HRTS#)**

### 43.3.2 HSCIF Interrupt Sources and the DMAC

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

If the DMAC is used for transmission/reception, set and enable the DMAC before setting the HSCIF.

#### Transmission interrupts and DMA transfer:

If the TDFE/TEND flag in HSFSR is set to 1 when the TDFE/TEND interrupt is enabled by the TIE bit, a TDFE/TEND interrupt request and a transmit-FIFO-data-empty DMA transfer request will occur. If the TDFE/TEND flag is set to 1 when TDFE/TEND interrupt is disabled by the TIE bit, only the transmit-FIFO-data-empty DMA transfer request will occur. (A transmit-FIFO-data-empty DMA transfer request is generated when the TDFE flag is set while TEIE is 0, or when the TEND flag is set while TEIE is 1. DMA transfer requests are not affected by the TEIE bit.)

When TDFE/TEND interrupt requests are enabled, the interrupt requests are cleared by the DMAC regardless of the interrupt handling program.

#### Reception interrupts and DMA transfer:

If the RDF/DR flag in HSFSR is set to 1 when RDF/DR interrupt is enabled by the RIE bit, an RDF/DR interrupt request occurs. If the RDF/DR flag is set to 1, a receive-FIFO-data-full DMA transfer request occurs. If the RDF/DR flag is set to 1 when RDF/DR interrupt is disabled by the RIE bit, and only a receive-FIFO-data-full DMA transfer request occurs and DMAC can be activated to perform data transfer.

Setting the RIE bit in HSSCR to 0 and the REIE bit to 1 generates the ER/BRK/ORER interrupt requests without generating RDF/DR interrupt requests. When the BRK flag in HSFSR or the ORER flag in HSLSR is set to 1, BRK/ORER interrupt requests occur.

If the TO flag is set to 1 in HSLSR when TO interrupts are enabled by the TOIE bit, TO interrupt requests occur.

When DR/TO interrupt requests are enabled to be issued, interrupt requests generated by the DR flag are cleared by the DMAC regardless of the interrupt handling program, however, those generated by the TO flag are not cleared by the DMAC. Therefore, the TO flag interrupt requests need to be cleared with the interrupt handling program. (The DR and TO flags are set at the same time, but cleared separately.)

**Table 43.6 HSCIF Interrupt Sources**

Interrupt Source	DMAC Activation
Interrupts generated by receive error flag (ER)	Disabled
Interrupts generated by receive-FIFO-data-full (RDF), receive-data-ready (DR) or timeout (TO)	Enabled
Interrupts generated by break (BRK) or overrun error (ORER)	Disabled
Interrupts generated by transmit FIFO data empty (TDFE)	Enabled

**43.4 Usage Notes**

<b>RZ/G1H</b>	<b>RZ/G1N</b>
<b>RZ/G1M</b>	<b>RZ/G1E</b>

Note the following on use of the HSCIF.

**(1) Break detection and operation**

Break signals can also be detected by reading the HRX pin value directly when a framing error (FER) is detected. In the break state, the input values from the HRX pin are all 0s. So, the parity error flag (PER) may be set after the FER flag is set to 1.

Although the HSCIF stops receive data transfer to HSRDR after detecting a break, it continues data reception.

**(2) Sending a break signal**

The input/output condition and level of the HTX pin are determined by the SPB2IO and SPB2DT bits in HSSPTR. This enables to send a break signal.

The pin does not function as the HTX pin from the initialization of the serial transmitter to setting of the TE bit (enabling transmission). In this period, the marked state is substituted by the value of the SPB2DT bit. Therefore, the SPB2IO and SPB2DT bits should be set to 1 (designating output and high level) beforehand.

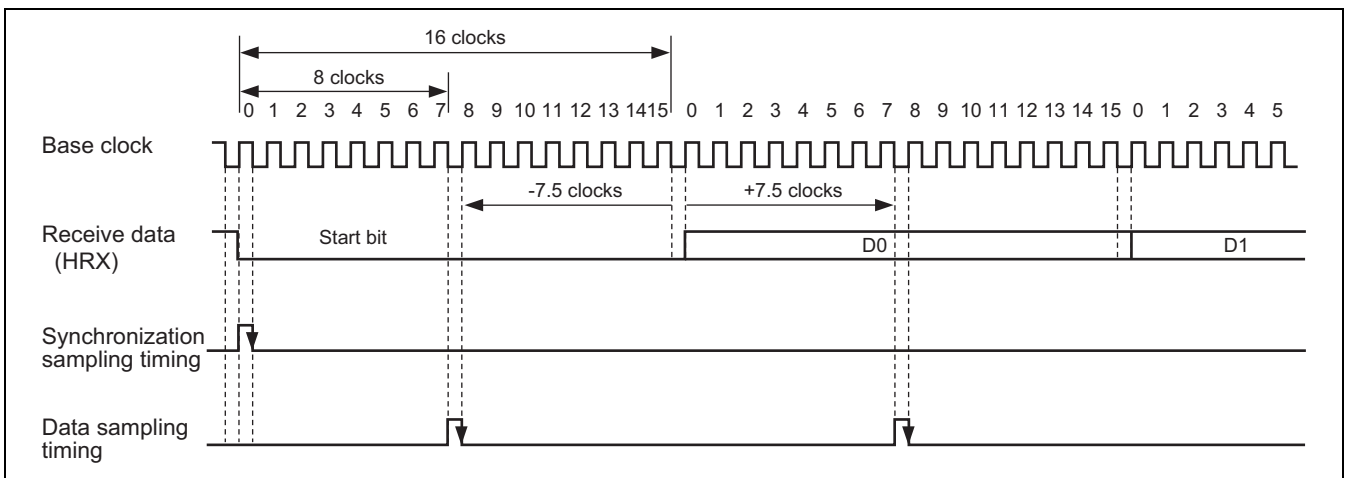
To send a break signal during serial transmission, clear the SPB2DT bit to 0 (low level), and then clear the TE bit to 0 (halting transmission). When the TE bit is cleared, the transmitter is initialized regardless of the current transmission state, and the HTX pin outputs 0.

**(3) Data sampling timing and reception margin in asynchronous mode**

The HSCIF operates on the base clock with a frequency multiplied by the number which is set as a sampling rate for the bit rate.

In reception, the HSCIF performs the internal synchronization by sampling the falling edge of the start bit using the base clock. In addition, the HSCIF takes receive data at the rising edge of the S/2 pulse (when S is an even number) or (S+1)/2 pulse (when S is an odd number) on the base clock when sampling rate is S.

Figure 43.11 shows the timing of this operation when S = 16.



**Figure 43.11 Timing Chart of Receive Data Sampling**

The reception margin in asynchronous mode is given by formula (1).

$$M = \left| \left( 0.5 - \frac{1}{2N} \right) - (L - 0.5) F - \frac{|D - 0.5|}{N} (1 + F) \right| \times 100\% \quad \text{..... Expression (1)}$$

M: Receive margin (%)

N: Ratio of bit rate to clock (N = sampling rate)

D: Clock duty (D = 0 to 1.0)

L: Frame length (L = 9 to 12)

F: Absolute value of clock frequency deviation

Assuming F = 0, D = 0.5 and sampling rate = 16 for expression (1), the reception margin obtained with expression (2) is 46.875% as shown below:

Assuming D = 0.5 and F = 0

$$M = (0.5 - 1/(2 \times 16)) \times 100\% \\ = 46.875\% \quad \text{.....expression (2)}$$

This is a theoretical value. A reasonable margin allowed in system designs is 20% to 30%.

#### (4) Reception margin and baud rate error

The value of 46.875% obtained by the above expression (2) indicates the reception margin when the baud rate error is 0 (F = 0). If there is no error in the reception and transmission baud rates, reception is possible even with misalignment of approx. 1/2 bit. If there is an error in the reception and transmission baud rates, the errors are accumulated up to the stop bit reception, which reduces the reception margin. The allowable baud rate error can be obtained by modifying the F in expression (1). When D = 0.5:

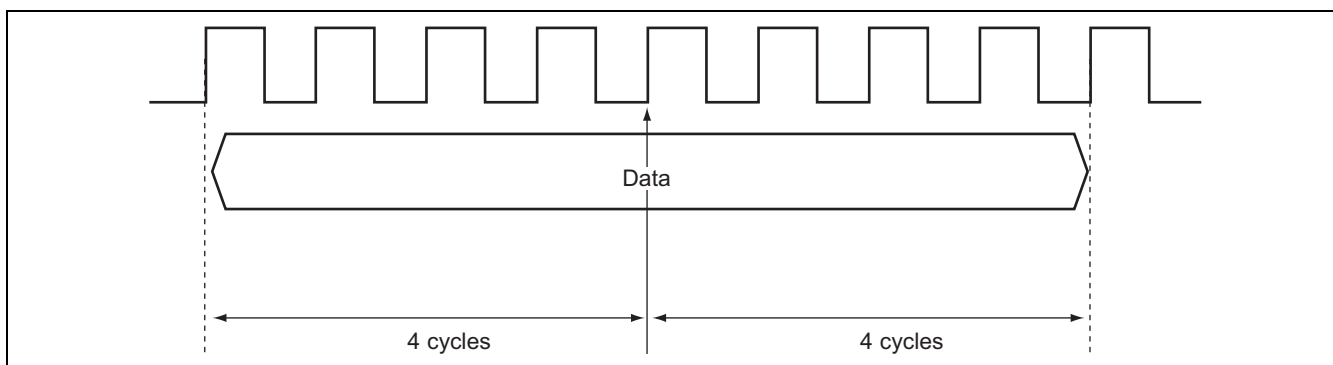
$$F = \{(15/32 - M)/(L - 0.5)\} \times 100 (\%) \quad \text{.....expression (3)}$$

By using expression (3), the relationship between the allowable error and reception margin with the frame length = 12 can be summarized as follows:

Allowed Error (%)	Reception Margin (%)
4.07	0
3.64	5
3.20	10
2.33	20
1.46	30

**(5) Usage method of SRHP bits**

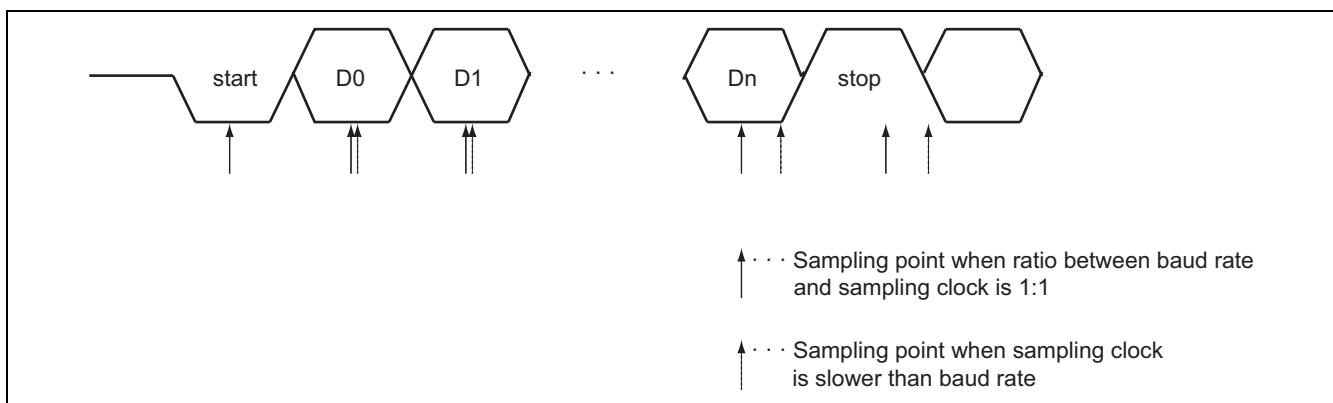
The method for using the SRHP bits in the sampling rate register is described below.



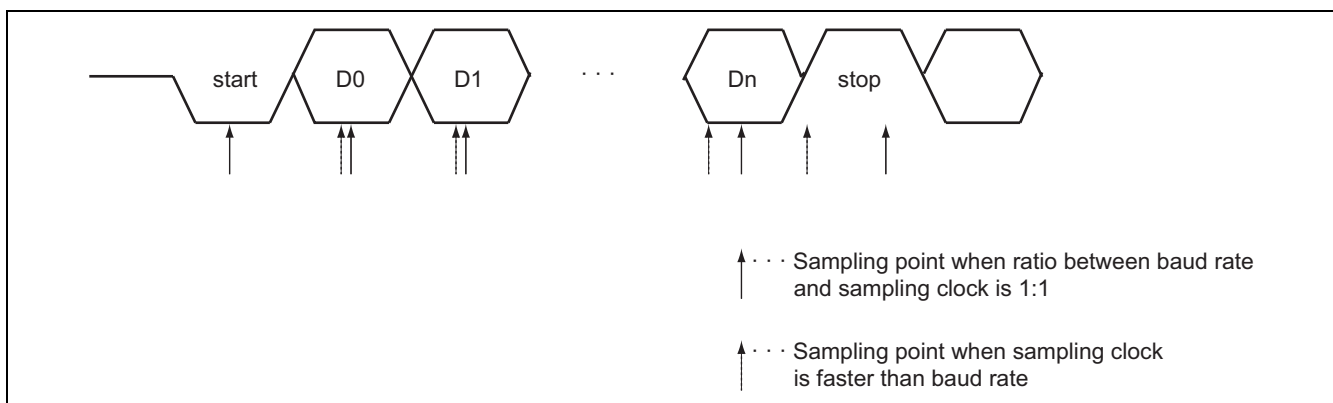
**Figure 43.12 Sampling with Invalid SRHP Bits**

Figure 43.12 shows a sampling example in which the SRHP bits are invalid (sampling rate = 8). In this case, the HSCIF samples data at half of the sampling rate, which is at the rising edge of the fourth pulse of the clock. This allows a setup margin and hold margin of 50% each to be provided.

However, if the ratio between the baud rate and sampling clock is not 1:1, either the setup margin or hold margin is omitted in data reception of a single frame. If the setup margin is omitted, the hold margin increases. On the other hand, if the hold margin is omitted, the setup margin increases. Figures 43.13 and 43.14 show examples.

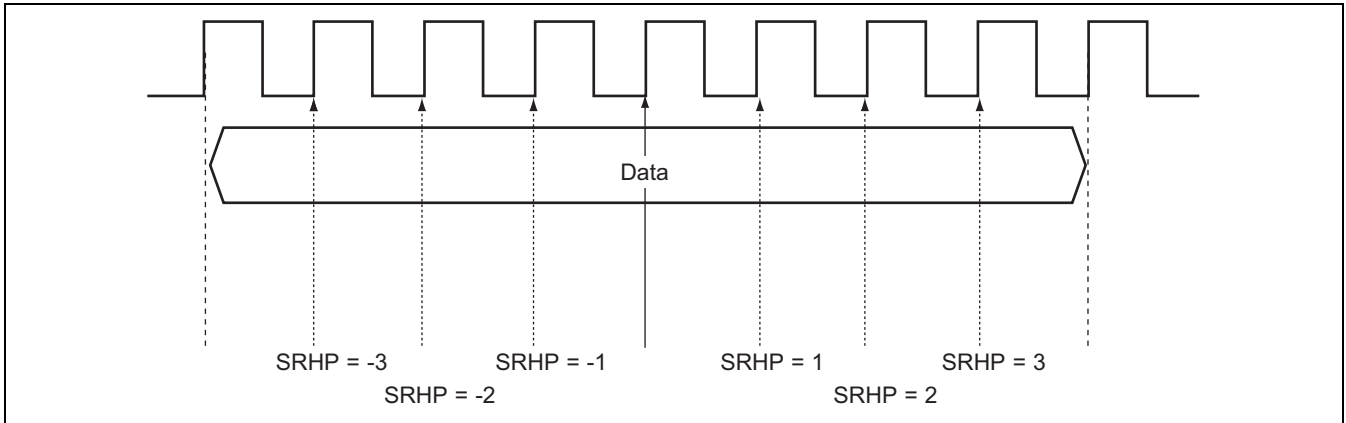


**Figure 43.13 Sampling Point with Sampling Clock Slower Than Baud Rate**



**Figure 43.14 Sampling Point with Sampling Clock Faster Than Baud Rate**

The ratio between the baud rate and sampling clock can be used to determine which margin among the setup margin and hold margin is to be omitted and which is to be increased. Based on this, the margin within a single frame can be increased by intentionally increasing the margin to be omitted in advance. The sampling point can be moved by setting a value in the SRHP bits. Figure 43.15 shows an example.



**Figure 43.15 Sampling Point Moved by SRHP Bits**

#### (6) Sampling rate and bit rate settings and respective margin

To set the baud rate in the HSCIF, in addition to setting the clock division ratio, the two registers, bit rate register (HSBRR) and sampling rate register (HSSRR), need to be set. These registers must be set so that the margin calculated by expression (1) in section 43.5 (3) will be a sufficient value.

The bit rate error is small when the value obtained by dividing the divided clock frequency used in the HSCIF with the sampling rate is near the desired baud rate. If there are many combinations of bit rate and sampling rate with the same bit rate error, choosing a combination with a large sampling rate provides a large margin. This is because when the bit rate error is constant in expression (1) in section 43.5 (3), that is, when the "absolute value of clock frequency deviation (F)" is constant, the margin (M) increases in accordance with the sampling rate (N).

If the sampling rate is made larger in a combination of bit rate and sampling rate with different bit rate errors, the bit rate error is increased. Accordingly, the "absolute value of clock frequency deviation (F)" on the right side in expression (1) in section 43.5 (3) gets larger and the margin (M) smaller.

Refer to the following procedure when selecting the sampling rate and bit rate settings.

1. Obtain the bit rate with the smallest bit rate error for sampling rates from 8 to 32.
2. Using expression (1) in section 43.5 (3), calculate the margin for each combination of sampling rate and bit rate which was obtained in step 1.
3. Select the combination with the largest margin among the combinations of sampling rate and bit rate.

## 43.5 Baud Rate Generator for External Clock (BRG)

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

### 43.5.1 Overview

The HSCIF incorporates a baud rate generator for external clock (abbreviated as BRG, hereafter). The BRG supplies a sampling clock (BRGCLK) to the HSCIF core by dividing the external clock SC\_CLK (selectable between SCIF\_CLK and ZSφ) by 1 to  $2^{16} - 1$ . In addition, the BRG switches the output between the external clock HSCK and divided clock.

### 43.5.2 Block Descriptions

Figure 43.16 shows a block diagram of the BRG.

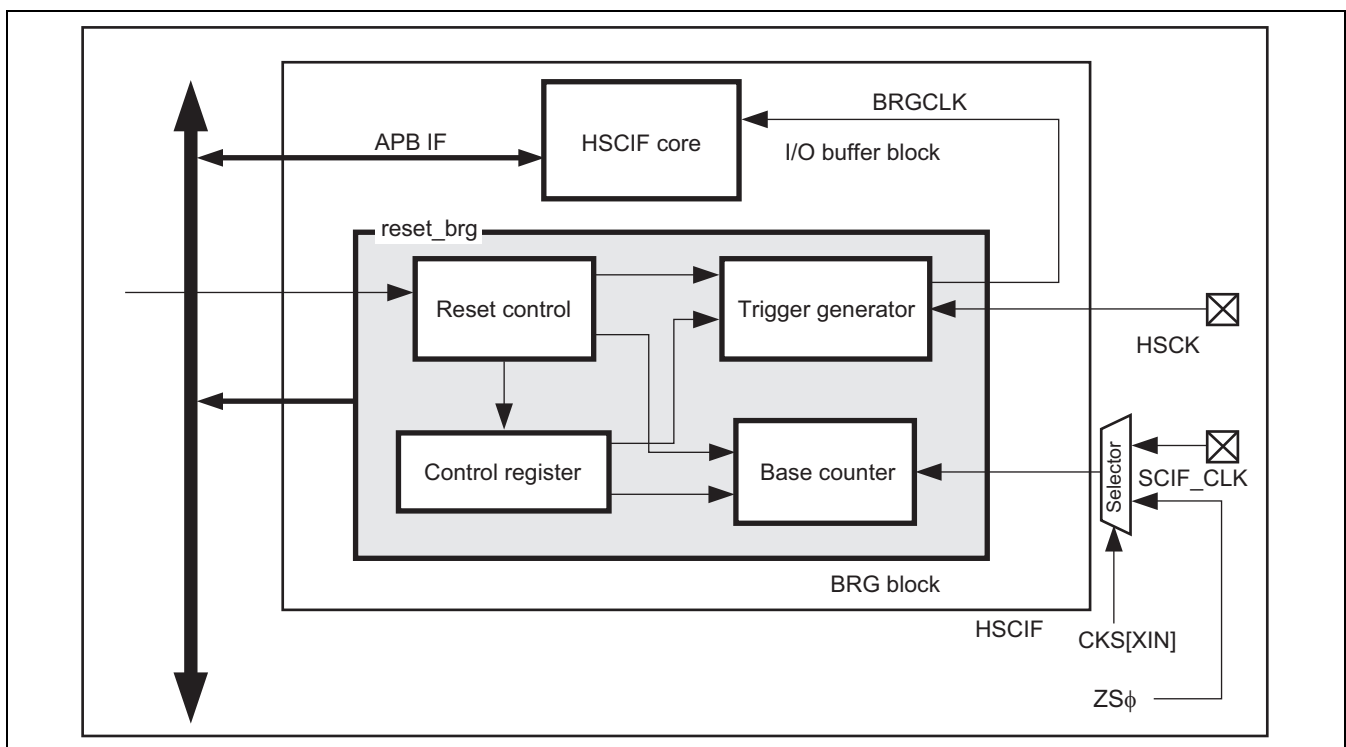


Figure 43.16 BRG Block Diagram

(1) Reset controller:

The reset controller handles resetting the control register, base counter, and trigger generator.

(2) Control register:

The control register has the frequency division register and clock select register.

(3) Base counter:

The base counter is a 16-bit CLK synchronization counter that is used to determine the timing for generating a frequency divided clock.

(4) Trigger generator:

The trigger generator generates rising-edge/falling-edge triggers for a frequency divided clock with the timing according to values of the frequency division register and base counter. The triggers are used to generate the frequency divided clock. In addition, the trigger generator switches the output between the HSK (external clock input) and frequency divided clock.



### 43.5.3 BRG Register Configuration

Table 43.7 shows the registers in the BRG block.

**Table 43.7 List of Registers**

Ch. No.	Name	Code	R/W	Initial Value	Address	Access Size	RZ/G Series Products			
							RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
0	Frequency division register 0	DL	R/W	H'00	H'E62C 0030	16	√	√	√	√
	Clock select register 0	CKS	R/W	H'00	H'E62C 0034	16	√	√	√	√
1	Frequency division register 1	DL	R/W	H'00	H'E62C 8030	16	√	√	√	√
	Clock select register 1	CKS	R/W	H'00	H'E62C 8034	16	√	√	√	√
2	Frequency division register 2	DL	R/W	H'00	H'E62D 0030	16	—	√	√	√
	Clock select register 2	CKS	R/W	H'00	H'E62D 0034	16	—	√	√	√

#### 43.5.3.1 Frequency Division Register (DL)

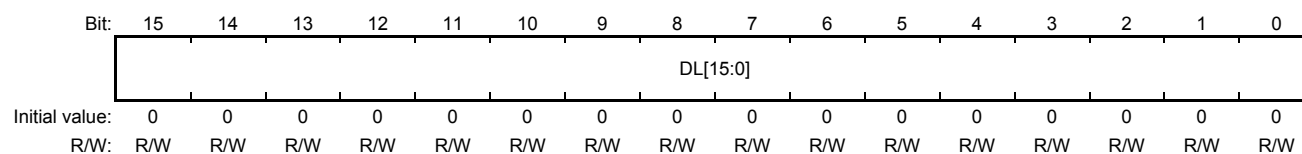
This register specifies the value of frequency division for the frequency divided clock generated by the BRG.

This register supports a 16-bit binary format that allows specifying a value in the range of 1 to 65535.

Setting all 0s in this register makes the BRG output the frequency divided clock at the low level.

The value of frequency division is given by the following formula:

The value of frequency division = (clock input frequency)/(required baud rate × sampling rate)



Bit	Bit Name	Initial Value	R/W	Description
15 to 0	DL[15:0]	All 0	R/W	Specifies a division value of frequency clock generated in BRG. The setting value is enabled in the range of 1 to 65535.

Tables 43.8 and 43.9 show how to use the baud rate generator with a 3.6864-MHz crystal resonator, and a 26-MHz crystal resonator.

**Table 43.8 Baud Rate (3.6864-MHz clock)**

Baud Rate	Value of Frequency Division	Sampling Rate	Error Rate*
50	4608	16	—
75	3072	16	—
110	4189	8	-0.002
134.5	1713	16	0.001
150	1536	16	—
300	768	16	—
600	384	16	—
1200	192	16	—
1800	128	16	—
2000	123	15	0.098
2400	96	16	—
3600	64	16	—
4800	48	16	—
7200	32	16	—
9600	24	16	—
14400	16	16	—
19200	12	16	—
38400	6	16	—
76800	3	16	—
115200	2	16	—

Note: \* "—" Indicates that the error rate is 0.

**Table 43.9 Baud Rate (26-MHz clock)**

Baud Rate	Value of Frequency Division	Sampling Rate	Error Rate*
9600	129	21	0.025
19200	52	26	-0.160
38400	26	26	-0.160
57600	15	30	-0.309
115200	9	25	-0.309
230400	4	28	-0.756
460800	2	28	-0.756
921600	1	28	-0.756
1843200	1	14	-0.756
3250000	1	8	—

Note: \* "—" Indicates that the error rate is 0.

### 43.5.3.2 Clock Select Register (CKS)

This register switches the output between the frequency divided clock and specifies a source clock for the external baud rate.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CKS	XIN	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15	CKS	0	R/W	This bit switches the output between the frequency divided clock (SC_CLK) and external clock (HSCK). 0: Selects the frequency divided clock. 1: Selects the external clock.
14	XIN	0	R/W	Selects the baud rate generator clock source for the external clock between SCIF_CLK and ZS $\phi$ . 0: Selects the external clock (SCIF_CLK). 1: Selects the internal clock (ZS $\phi$ ).
13 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

#### 43.5.4 Restrictions in BRG

##### (1) Notes on setting frequency division register

1. For the initial setting of the register after a reset, at least one bit of waiting period is required to secure the clock stabilization time.

(Example) One bit period when DL = 2

$$3.68 \text{ (MHz)} \times 1/2 \times 1/16 = 0.115 \text{ (MHz)} \rightarrow 8695 \text{ (ns)}$$

2. For modifying the register value after the setting stated in <1> above, at least one bit of waiting period at the maximum bit rate (DL = '65535') is required.

The HSCIF registers and BRG registers should be set as the following table:

- Asynchronous mode (SC\_CLK external input)

HSCIF		BRG	
Register Name	Setting Value	Register Name	Setting Value
HSSCR.CKE[1:0]	B'10	CKS	H'0000
		DL	H'1 to H'FFFF

- Asynchronous mode (HSC external input)

HSCIF		BRG	
Register Name	Setting Value	Register Name	Setting Value
HSSCR.CKE[1:0]	B'10	CKS	H'8000
		DL	Don't care

3. The register settings for the baud rate generator for external clock should be made before starting initialization of the HSCIF.

## 44. I2C Bus Interface (I2C)

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

### 44.1 Features

RZ/G series products have up to six I2C bus interfaces conformant with the Philips Semiconductors (now NXP Semiconductors) I2C bus (Inter-IC bus) specification. However, the configuration of registers that control the I2C bus differs partly from the NXP Semiconductors register configuration. The I2C bus interface has the following features. Note that "module clock (MOD\_CLK)" refers to the peripheral module clock (HP $\phi$ ) in this section.

- The I2C interfaces support the I2C bus specification from NXP Semiconductors
- Multi-master compatible
- Seven- or ten-bit address compatible master
- Seven-bit slave address
- Fast mode compatible
- Variable clock frequencies

Figure 44.1 shows a block diagram of the I2C bus interface.

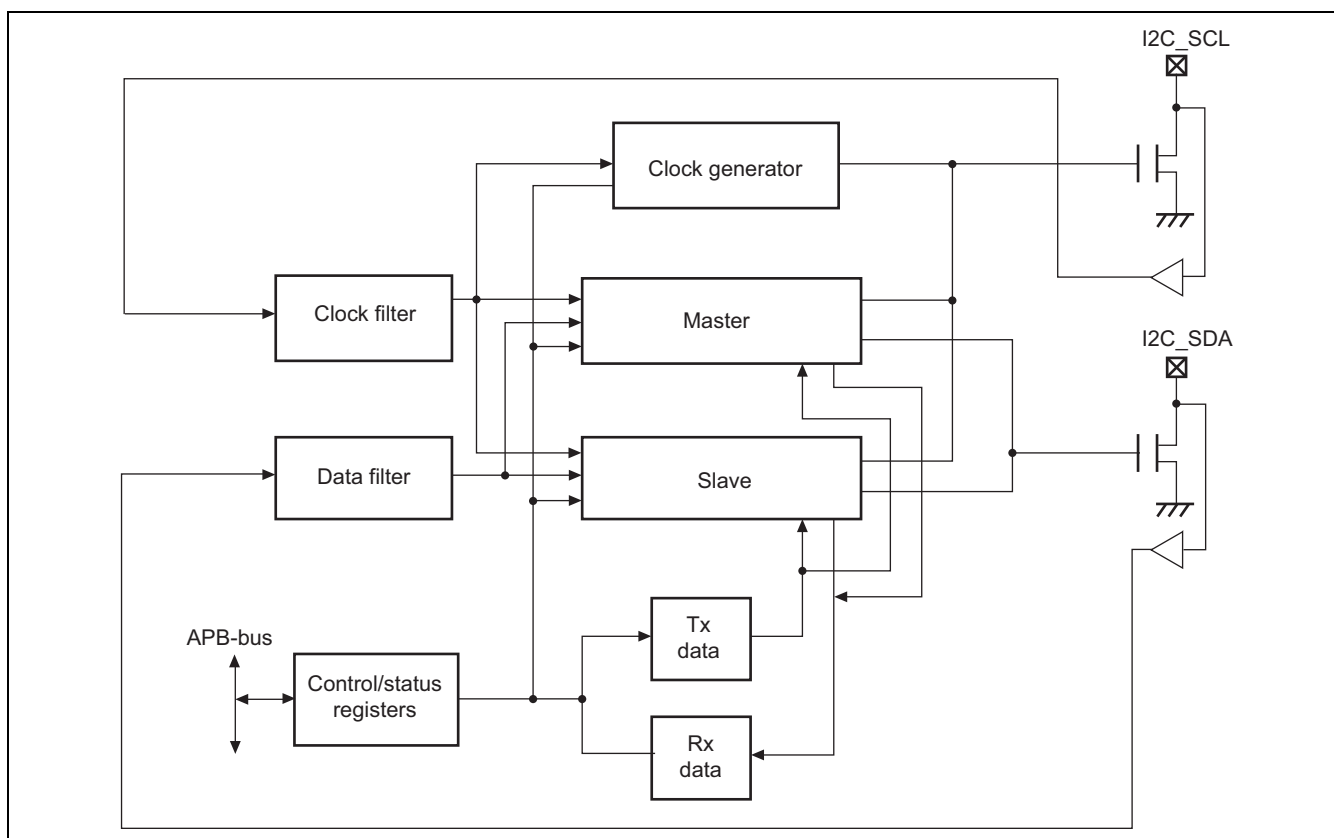


Figure 44.1 Block Diagram of I2C Bus Interface

## 44.2 Input/Output Pins

Table 44.1 lists the pins used in the I2C bus interface.

**Table 44.1 I2C Bus Interface**

Channel Number	Pin Name* <sup>1</sup>	I/O	Function	RZ/G Series Products			
				RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
				Output Buffer Type* <sup>2</sup>			
0	SCL	I/O	SCL:	OD* <sup>3</sup>	LVTTTL	LVTTTL	LVTTTL
	SDA		I2C serial clock input/output pin				
1	SCL		SDA:	LVTTTL* <sup>3</sup>	LVTTTL	LVTTTL	LVTTTL
	SDA		I2C serial data input/output pin				
2	SCL			LVTTTL* <sup>3</sup>	LVTTTL	LVTTTL	LVTTTL
	SDA						
3	SCL			OD* <sup>3</sup>	LVTTTL	LVTTTL	LVTTTL
	SDA						
4	SCL			—	LVTTTL	LVTTTL	LVTTTL
	SDA						
5	SCL			—	OD	OD	LVTTTL
	SDA						

Notes: 1. The actual pin names are I2Cn\_SCL and I2Cn\_SDA (n = 0 to 3 for RZ/G1H and 0 to 5 for RZ/G1M, N). These are referred to as I2C\_SCL and I2C\_SDA in this section.

2. Output buffer type: "OD" is open drain buffer and "LVTTTL" is low level drive only LVTTTL buffer. OD assigned channel pins are 1.8 V I/O and input/output 3.3 V tolerant; LVTTTL assigned channel pins are 3.3 V I/O.

3. For only RZ/G1H, these pins are shared with IIC module pins. Select one of the modules either I2C or IIC for each channel.

The I2C buffer in this LSI is not compliant with the 5V-input. When turning off the I/O power source (3.3 V) of this LSI, turn off the power source of the pull-up resistors connected to the I2C pins.

Note: When using 1.8V I2C/IIC pins (OD assigned channel) as 3.3 V tolerant, all the external pull-up voltage power supply to the I2C/IIC of this LSI must keep the same power on/off sequence as the VCCQ (3.3 V) of this LSI.

### 44.3 Register Descriptions

The base address for each channel of registers of the I2C bus interface is as follows:

- I2C0: H'E650\_8000 (RZ/G1H, M/N, E)
- I2C1: H'E651\_8000 (RZ/G1H, M/N, E)
- I2C2: H'E653\_0000 (RZ/G1H, M/N, E)
- I2C3: H'E654\_0000 (RZ/G1H, M/N, E)
- I2C4: H'E652\_0000 (RZ/G1M/N, E)
- I2C5: H'E652\_8000 (RZ/G1M/N, E)

Note. Number of I2C channels:  
 4 channels for RZ/G1H (channels 0 to3)  
 6 channels for RZ/G1M/N, E (channels 0 to 5)

Each channel of the I2C bus interface has the registers below.

**Table 44.2 Register Configuration (1)**

Register Name	Abbreviation	R/W	Offset Address from Base Address	Size	RZ/G Series Products			
					RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Slave control register	ICSCR	R/W	H'00	32	√	√	√	√
Master control register	ICMCR	R/W	H'04	32	√	√	√	√
Slave status register	ICSSR	R/(W)* <sup>1</sup>	H'08	32	√	√	√	√
Master status register	ICMSR	R/(W)* <sup>2</sup>	H'0C	32	√	√	√	√
Slave interrupt enable register	ICSIER	R/W	H'10	32	√	√	√	√
Master interrupt enable register	ICMIER	R/W	H'14	32	√	√	√	√
Clock control register	ICCCR	R/W	H'18	32	√	√	√	√
Slave address register	ICSAR	R/W	H'1C	32	√	√	√	√
Master address register	ICMAR	R/W	H'20	32	√	√	√	√
Receive data register	ICRXD	R	H'24	32	√	√	√	√
Transmit data register	ICTXD	W	H'24	32	√	√	√	√

Notes: Do not write to any addresses other than listed above. Operations cannot be guaranteed if writing is attempted. Values read from addresses other than those listed above are undefined.

Although the actual register name and its abbreviation have channel number as a suffix respectively, it is omitted in this section.

1. Only 0 can be written to bits 4 to 0 to clear the flags.
2. Only 0 can be written to bits 6 to 0 to clear the flags.

**Table 44.2 Register Configuration (2)**

<b>Name</b>	<b>Abbreviation</b>	<b>Power-On Reset</b>	<b>Module Standby</b>
Slave control register	ICSCR	H'0000 0000	Retained
Master control register	ICMCR	H'0000 0000*	Retained
Slave status register	ICSSR	H'0000 0000	Retained
Master status register	ICMSR	H'0000 0000	Retained
Slave interrupt enable register	ICSIER	H'0000 0000	Retained
Master interrupt enable register	ICMIER	H'0000 0000	Retained
Clock control register	ICCCR	H'0000 0000	Retained
Slave address register	ICSAR	H'0000 0000	Retained
Master address register	ICMAR	H'0000 0000	Retained
Receive data register	ICRXD	H'0000 0000	Retained
Transmit data register	ICTXD	—	—

Note: \* Bits 30, 29, 22, 21, 14, 13, 6, and 5 are undefined.



### 44.3.1 Slave Control Register (ICSCR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	SDBS	SIE	GCAE	FNA
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 4	—	All 0	R	Reserved When these bits are read, bits 31 to 24, 23 to 16, and 15 to 8 reflect the values of bits 7 to 0. The write value should always be 0.
3	SDBS	0	R/W	Slave Data Buffer Select This bit is used to select the data buffer. Select the single-buffer mode supported in this module. When this bit is set to 1, the single-buffer mode is selected. SCL will be held low from the timing when the receive data register acquires the data packet until the SDR flag is cleared. 0: Setting prohibited 1: Single-buffer mode
2	SIE	0	R/W	Slave Interface Enable This bit must be set for the slave operation. If this bit is low, the slave interface is reset.
1	GCAE	0	R/W	General Call Acknowledgement Enable When slave devices are to issue an acknowledgement in response to a general call address sent from a master, this bit must be set to 1.
0	FNA	0	R/W	Forced Non Acknowledgement In the slave receive mode, the level of this bit is sent to the transmitting device as the acknowledge signal. This bit is set to 0 during the period that the data packet is being received, and set to 1 on completion of data reception. Forced non acknowledgement is returned to the master during slave reception. When the slave has received the last byte of data in a data packet, the slave communicates with the master by sending a NACK, meaning that the acknowledgement is not driven. The master issues a stop on the bus after receiving a NACK. The setting of this bit does not affect the acknowledgement of the slave address.

### 44.3.2 Slave Status Register (ICSSR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bits 0 to 4 among the status bits in the slave status register are cleared by writing 0 to the respective status bit positions. The individual bits are held 1 until 0 is written to (other than the GCAR and STM bits).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	GCAR	STM	SSR	SDE	SDT	SDR	SAR
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W*	R/W*	R/W*	R/W*	R/W*

Bit	Bit Name	Initial Value	R/W	Description
31 to 7	—	All 0	R	Reserved When these bits are read, bits 31 to 24, 23 to 16, and 15 to 8 reflect the values of bits 7 to 0. The write value should always be 0.
6	GCAR	0	R	General Call Address Received Indicates that the address received from the bus is a general call address (H'00). This status bit does not cause an interrupt. This bit is automatically cleared by hardware when the SIE bit (bit 2 in the slave control register) is set to 0 or when the SSR bit (bit 4 in this register) is set to 1.
5	STM	0	R	Slave Transmit Mode Indicates whether the current slave transmit mode is read or write. When this bit is set to 0, the mode is write (slave reception). When this bit is set to 1, the mode is read (slave transmission). This status bit does not cause an interrupt. This bit is automatically cleared by hardware when the SIE bit (bit 2 in the slave control register) is set to 0 or when the SSR bit (bit 4 in the slave status register) is set to 1.
4	SSR	0	R/W*	Slave Stop Received A stop condition has been output on the bus. This status bit becomes active after the rising edge of SDA during reception of a stop bit.
3	SDE	0	R/W*	Slave Data Empty Indicates that data to be transmitted has been loaded into the shift register. At the start of byte data transmission, the contents of the ICTXD register are loaded into a shift register ready for outputting data on the bus. This status bit indicates that data has been loaded and the ICTXD register is again ready for further data. This status bit becomes active on the falling edge of SCL before reception of the first data bit. During the single-buffer mode, this bit must be reset every time new data has been written to ICTXD. This is because the slave holds SCL low to stop the bus while this bit is set to 1 even if a slave transmission cycle is started.

Bit	Bit Name	Initial Value	R/W	Description
2	SDT	0	R/W*	<p>Slave Data Transmitted</p> <p>A byte of data has been transmitted to the bus. This bit becomes active after the falling edge of SCL during reception of the last data bit.</p>
1	SDR	0	R/W*	<p>Slave Data Received</p> <p>A byte of data has been received from the bus and is ready for reading from the receive data register. This bit becomes active after the falling edge of SCL during reception of the last data bit. During the single-buffer mode, this bit must be reset after data has been read from the ICRXD register.</p> <p>When SDBS is set to 1, SCL will be held low from the timing when the receive data register acquires the data packet until the SDR flag is cleared.</p>
0	SAR	0	R/W*	<p>Slave Address Received</p> <p>Indicates that the slave has recognized its own address on the bus (defined by the contents of the slave address register). If the general call acknowledgement enable bit is enabled in the slave control register, then this status bit is also set to 1 even if the address on the bus is a general call address. In this case, the GCAR bit in this register is used to determine whether or not the address is a general call address. The STM bit indicates whether the access is read (high) or write (low). This status becomes active after the falling edge of SCL during reception of the last address bit. The slave holds the SCL signal low from the start of the ACK phase until the software resets this status bit.</p>

Note: \* This bit can be read from or written to. Writing 0 clears this bit to 0 and writing 1 is ignored.

**44.3.3 Slave Interrupt Enable Register (ICSIER)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	SSRE	SDEE	SDTE	SDRE	SARE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 5	—	All 0	R	Reserved When these bits are read, bits 31 to 24, 23 to 16, and 15 to 8 reflect the values of bits 7 to 0. The write value should always be 0.
4	SSRE	0	R/W	Slave Stop Received Interrupt Enable 0: Disables the SSR interrupt. 1: Enables the SSR interrupt.
3	SDEE	0	R/W	Slave Data Empty Interrupt Enable 0: Disables the SDE interrupt. 1: Enables the SDE interrupt.
2	SDTE	0	R/W	Slave Data Transmitted Interrupt Enable 0: Disables the SDT interrupt. 1: Enables the SDT interrupt.
1	SDRE	0	R/W	Slave Data Received Interrupt Enable 0: Disables the SDR interrupt. 1: Enables the SDR interrupt.
0	SARE	0	R/W	Slave Address Received Interrupt Enable 0: Disables the SAR interrupt. 1: Enables the SAR interrupt.

**44.3.4 Slave Address Register (ICSAR)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	SADD0 _6	SADD0 _5	SADD0 _4	SADD0 _3	SADD0 _2	SADD0 _1	SADD0 _0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 7	—	All 0	R	Reserved When these bits are read, bits 31 to 24, 23 to 16, and 15 to 8 reflect the values of bits 7 to 0. The write value should always be 0.
6 to 0	SADD0_6 to SADD0_0	All 0	R/W	Slave Address This is the unique 7-bit address allocated to the slave on the I2C bus. The slave interface compares this address with the first seven bits transmitted as the slave address, at the beginning of a data packet transmission.

### 44.3.5 Master Control Register (ICMCR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	—	—	0	0	0	0	0	0	—	—	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	MDBS	FSCL	FSDA	OBPC	MIE	TSBE	FSB	ESG
Initial value:	0	—	—	0	0	0	0	0	0	—	—	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0, except bits 30, 29, 22, 21, 14, and 13, in which case, initial value is undefined.	R	Reserved When these bits are read, bits 31 to 24, 23 to 16, and 15 to 8 reflect the values of bits 7 to 0. The write value should always be 0.
7	MDBS	0	R/W	Master Data Buffer Select This bit is used to select the data buffer mode. Select the single-buffer mode supported in this module. When this bit is set to 1, the single-buffer mode is selected. SCL will be held low from the timing when the receive data register acquires the data packet until the MDR flag is cleared. 0: Setting prohibited 1: Single-buffer mode
6	FSCL	—	R/W	Forced SCL This bit controls the status of the I2C_SCL pin (reading reflects the current status of the I2C_SCL pin). When the OBPC bit is set, this bit directly controls the SCL line on the bus. During a read cycle, the level on this bit (which includes the reset level) will change depending on the level on I2C_SCL since it directly reflects the level on the I2C_SCL.
5	FSDA	—	R/W	Forced SDA This bit controls the status of the I2C_SDA pin (reading reflects the busy status level on the I2C bus). When the OBPC bit is set, then this bit directly controls the SDA line on the bus. During a read cycle, the level on this bit (which includes the reset level) will show the busy status of the I2C bus (1 for busy; 0 for not busy).
4	OBPC	0	R/W	Override Bus Pin Control When this bit is set to 1, the FSDA and FSCL bits in this register control SDA and SCL directly. This mode is used for testing purposes only.

Bit	Bit Name	Initial Value	R/W	Description
3	MIE	0	R/W	<p>Master Interface Enable</p> <p>When this bit is set to 1, the master interface is enabled.</p> <p>This bit is automatically cleared to 0 when this interface loses in arbitration of bus mastership. If 0 is not subsequently written to the bit, the value of the bit is restored to 1 on detection of a STOP condition on the I2C bus, and data transmission is retried.</p> <p>Regarding the state following a loss in arbitration of bus mastership, see the description of the MAL bit in ICMSR.</p>
2	TSBE	0	R/W	<p>Start Byte Transmission Enable</p> <p>When this bit is set to 1, if the master issues a START or a repeated START condition, it continues by transmitting a start byte (01H) over the bus. The start byte is used for interfacing with slower microcontrollers that have I2C bus interfaces.</p>
1	FSB	0	R/W	<p>Forced Stop onto the Bus</p> <p>When this bit is set to 1, the master transmits a STOP condition on the bus at the end of the current transfer. If ESG is also set, the master immediately transmits a START condition and begins transmitting a new data packet. If ESG is not set, the master enters the idle state.</p>
0	ESG	0	R/W	<p>Enable Start Generation</p> <p>When this bit is set to 1, the master starts transmission of a data packet. If the bus is idle when ESG is set, the master transmits a START condition on the bus and then transmits the slave address. If the master is transferring data when ESG is set, at the end of that data byte transfer, the master transmits a repeated START condition before transmitting the slave address. When transmitting a data packet, the software must reset this bit when the slave address has been transmitted, otherwise a repeated START condition is transmitted after every transmission is completed.</p>

### 44.3.6 Master Status Register (ICMSR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

The status bits (bits 0 to 6) in the master status register are cleared by writing 0 to the respective status bit positions. The individual status bits are held 1 until a reset by writing 0 to the appropriate bit position.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	MNR	MAL	MST	MDE	MDT	MDR	MAT
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*

Bit	Bit Name	Initial Value	R/W	Description
31 to 7	—	All 0	R	Reserved When these bits are read, bits 31 to 24, 23 to 16, and 15 to 8 reflect the values of bits 7 to 0. The write value should always be 0.
6	MNR	0	R/W*	Master NACK Received When this bit is set to 1, this bit indicates that the master has received a NACK response (the SDA line is high during the acknowledge cycle on the bus) to either an address or data transmission.
5	MAL	0	R/W*	Master Arbitration Lost In a multi-master system, when this bit is set to 1, it indicates that the master has lost arbitration to other masters on the bus. At this point, MIE is reset and the master interface is disabled.
4	MST	0	R/W*	Master Stop Transmitted When this bit is set to 1, it indicates that the master has sent a STOP condition on the bus. A STOP condition can be sent either as a result of the setting of the forced stop bit in the control register, or from a NACK being received from a slave during a slave receive data packet.
3	MDE	0	R/W*	Master Data Empty At the start of a byte data transmission, the contents of the transmit data register are loaded into a shift register ready for transmitting on the bus. When this bit is set to 1, it indicates that the shift register has been loaded, so the transmit data register is ready to accept further data. During master transmission, the MDE bit is also set at the same time as the MAT bit is set after transmission of the slave address. In this case, you need to clear the MDE and MAT bits after the ICMSR's ESG bit is cleared. The clearing will restart the data transmission.
2	MDT	0	R/W*	Master Data Transmitted Byte data has been sent to the slave on the bus. This status bit becomes active after the falling edge of SCL during reception of the last data bit.



Bit	Bit Name	Initial Value	R/W	Description
1	MDR	0	R/W*	<p>Master Data Received</p> <p>Byte data has been received from the bus and is in the receive data register. This status bit becomes active after the falling edge of SCL during reception of the last data bit. During single-buffer mode, this status bit must be reset after data has been read from the receive data register.</p> <p>When MDBS is set to 1, SCL will be held low from the timing when the receive data register acquires the data packet until the MDR flag is cleared.</p> <p>During master reception mode, the MDR bit is also set at the same time as the MAT bit is set after transmission of the slave address. In this case, you must clear the MDR and MAT bits after the ICMCR's ESG bit is cleared. Clearing will start the data reception</p>
0	MAT	0	R/W*	<p>Master Address Transmitted</p> <p>The master has been transmitted the slave address byte of a data packet. This bit becomes active after the falling edge of SCL during reception of the ACK bit following transmission of the address.</p>

Note: \* This bit can be read from or written to. Writing 0 clears this bit to 0 and writing 1 is ignored.

**44.3.7 Master Interrupt Enable Register (ICMIER)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	MNRE	MALE	MSTE	MDEE	MDTE	MDRE	MATE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 7	—	All 0	R	Reserved When these bits are read, bits 31 to 24, 23 to 16, and 15 to 8 reflect the values of bits 7 to 0. The write value should always be 0.
6	MNRE	0	R/W	Master NACK Received Interrupt Enable 0: Disables the MNR interrupt. 1: Enables the MNR interrupt.
5	MALE	0	R/W	Master Arbitration Lost Interrupt Enable 0: Disables the MAL interrupt. 1: Enables the MAL interrupt.
4	MSTE	0	R/W	Master Stop Transmitted Interrupt Enable 0: Disables the MST interrupt. 1: Enables the MST interrupt.
3	MDEE	0	R/W	Master Data Empty Interrupt Enable 0: Disables the MDE interrupt. 1: Enables the MDE interrupt.
2	MDTE	0	R/W	Master Data Transmitted Interrupt Enable 0: Disables the MDT interrupt. 1: Enables the MDT interrupt.
1	MDRE	0	R/W	Master Data Received Interrupt Enable 0: Disables the MDR interrupt. 1: Enables the MDR interrupt.
0	MATE	0	R/W	Master Address Transmitted Interrupt Enable 0: Disables the MAT interrupt. 1: Enables the MAT interrupt.

**44.3.8 Master Address Register (ICMAR)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	SADD1_6	SADD1_5	SADD1_4	SADD1_3	SADD1_2	SADD1_1	SADD1_0	STM1
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved When these bits are read, bits 31 to 24, 23 to 16, and 15 to 8 reflect the values of bits 7 to 0. The write value should always be 0.
7 to 1	SADD1_6 to SADD1_0	All 0	R/W	Slave Address These bits are the address of the slave which the master communicates with.
0	STM1	0	R/W	Slave Transfer Mode This bit specifies the mode in which the slave operates. Bit STM1 sets the operating mode (transmit or receive mode) of the slave, which is an external slave device whose address matches the slave address (SADD1) sent from the master. The slave device is automatically set to transmit/receive mode by hardware on reception of the STM1 signal. When this bit is set to 1, it indicates a read operation. When this bit is cleared to 0, it indicates a write operation.

### 44.3.9 Clock Control Register (ICCCR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	SCGD					CDF			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 9	—	All 0	R	Reserved The read value is always 0. The write value should always be 0.
8 to 3	SCGD	All 0	R/W	SCL Clock Generation Divider When operation is in master mode, the SCL clock is generated from the internal clock by using SCGD as the ratio. This is also the operating clock in slave-mode operation while SCL is being held low to stop the bus after an overflow has occurred. SCGD must be specified in both master and slave modes. The formula expressing the relationship is: Equation 2: SCL rate calculation $SCLfreq = I2Cck / (20 + SCGD \times 8 + F[(tICF + tr + IntDelay) \times I2Cck])$ I2Cck: I2C internal clock frequency tICF: I2C SCL falling time (depending on external load) tr: I2C SCL rising time (depending on external load) IntDelay: LSI internal delay corresponds to output buffer type. Open drain buffer: 50 ns (typ.), 110 ns (max.) LVTTTL (low drive only) buffer: 5 ns (typ.), 6 ns (max.). F[n]: n rounded up to an integer Suggested settings for CDF and SCGD for CPU speeds and the two I2C bus speeds are given in Table 44.3.
2 to 0	CDF	All 0	R/W	Clock Division Factor The internal clock used in most blocks in the I2C module is a divided module clock. The internal I2C clock is generated from the module clock using the CDF as the division ratio: Equation 1: I2C internal clock frequency calculation $I2Cck = MOD\_CLK / (1 + CDF)$ MOD_CLK: module clock frequency Ensure that minimum values for setup and hold times of the SDA signal relative to the SCL signal on the bus are satisfied. The clock frequency is to ensure that the glitch filtering will operate with glitches of up to 50 ns as described in the fast mode I2C specification. Note: CDF must be set so that the clock frequency (I2Cck) is lower than 20 MHz.

**Table 44.3 Recommended Settings for CDF and SCGD\*1**

- Recommended register values for open drain buffer

Module Clock Frequency	100 kHz		400 kHz	
	CDF(*2)	SCGD(*3)	CDF(*2)	SCGD(*3)
130 MHz	6	20	6	3
Error		+0.93%		-3.27%

- Recommended register values for LVTTTL buffer (low drive only)

Module Clock Frequency	100 kHz		400 kHz	
	CDF(*2)	SCGD(*3)	CDF(*2)	SCGD(*3)
130 MHz	6	20	6	3
Error		+2.04%		+0.93%

Notes: 1. These recommended values are for the SCL rate with an external load that produces  $t_{ICF} = 20$  ns and  $t_r = 35$  ns.

Recalculate to obtain the actual values after measuring  $t_{ICF}$  and  $t_r$  under actual conditions of usage.

- Recommended value for CDF bit of ICCCR.
- Recommended value for SCGD bit of ICCCR.

### 44.3.10 Receive and Transmit Data Registers (ICRXD and ICTXD)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Reading from or writing to these registers access different physical internal registers. When data is to be transmitted, the contents of the shift register are loaded via TXD. After data has been received into the shift register from the I2C bus, it is then loaded into RXD.

#### (1) Receive data register (ICRXD)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	RXD							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved When these bits are read, bits 31 to 24, 23 to 16, and 15 to 8 reflect the values of bits 7 to 0. The write value should always be 0.
7 to 0	RXD	All 0	R	Read Receive Data Data received by master or slave.

#### (2) Transmit data register (ICTXD)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	TXD							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	W	W	W	W	W	W	W	W

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved The write value should always be 0.
7 to 0	TXD	All 0	W	Write Transmit Data Data to be transmitted by master or slave.

## 44.4 Operations

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

### 44.4.1 Data and Clock Filters

These blocks filter out glitches on signals coming from the I2C bus. Glitches up to one internal clock period in width are rejected (for details on the internal clock frequency, see section 44.3.9, Clock Control Register (ICCCR)). This is for the faster I2C bus rate (400 kHz) but does not violate the slower I2C bus rate specification.

These blocks also resynchronize bus signals with the internal clock.

### 44.4.2 Clock Generator

The clock generator has two functions. Firstly, it generates the SCL (I2C bus clock) according to commands of the master or slave interface. Secondly, it controls the internal clock rate, used by filtering blocks and the master and slave interfaces. This clock functions as a clock enable signal of the registers in these blocks.

### 44.4.3 Master/Slave Interfaces

These two interfaces run independently and in parallel. The master interface controls the transmission of address and data on the I2C bus. The slave interface monitors the I2C bus and takes part in transmissions if its programmed address is seen on the bus. The interfaces communicate with the control/status registers independently. There is only one interrupt line output from the I2C module. The interrupt source is either the master or the slave.

### 44.4.4 Software Status Interlocking

To make the software interface with the I2C module as robust and thus simple as possible, various interlocking status mechanisms have been included in the operation of the master and slave interfaces. The status bits involved are:

#### (1) MDR and SDR

MDR or SDR is set to 1 when data is received. Clear the status after reading the receive data register. If data is received while MDR or SDR is set, the hardware recognizes that unread data remains in the receive data register and automatically holds SCL at the low level to suspend data transmission. In this case, transmission can be resumed by clearing the status after reading the receive data.

Consequently, when receiving data continuously, be sure to clear the status bit (MDR or SDR) after reading the receive data register.

#### (2) MDE and SDE

If the MDE or SDE status bit is still set when data in the transmit data register is to be transmitted on the I2C bus by the slave or master, the SCL line must be held low until the MDE or SDE status bit is reset. The MDE or SDE status bit being set indicates that the data currently held in the transmit data register has already been transmitted on the I2C bus.

The software must clear this status bit when it writes to the transmit data register after transmission of the next data byte has become possible. This is not required for the first byte of data to be transmitted on the bus.

#### (3) MAL

When the master loses arbitration, the MAL bit (of the master status register) is set and the MIE bit (of the master control register) is reset. At this point, master mode is invalid and the I2C bus interface enters the slave mode. When master operation is restarted, data transfer from the master begins after the MAL bit has been cleared.

#### (4) SAR

The SAR status bit is set when the slave identifies its address on the I2C bus. At this point the slave interface forces the SCL line low until the SAR status bit is reset.

This is particularly important when a slave transmit is about to take place on the bus, and the slave will transmit the data from the transmit data register. The software responds to the SAR status by writing the required data into the transmit data register and then resetting the SAR status bit. This allows the slave interface to continue the access.

Unless the SAR bit is in use, when the slave is about to receive data, the software might still be reading out data that was loaded in previous access from the receive data register. In this case the valid data still held in the receive data register is overwritten. However, this is avoided using the SAR status bit. After the software has read data in the receive data register, reset the SAR bit (if it is set). Then overwriting the receive data register is avoided.

#### 44.4.5 I2C Bus Data Format

Figure 44.2 shows a timing chart for the I2C bus interface. Table 44.4 describes the meaning of each symbol in Figure 44.2.

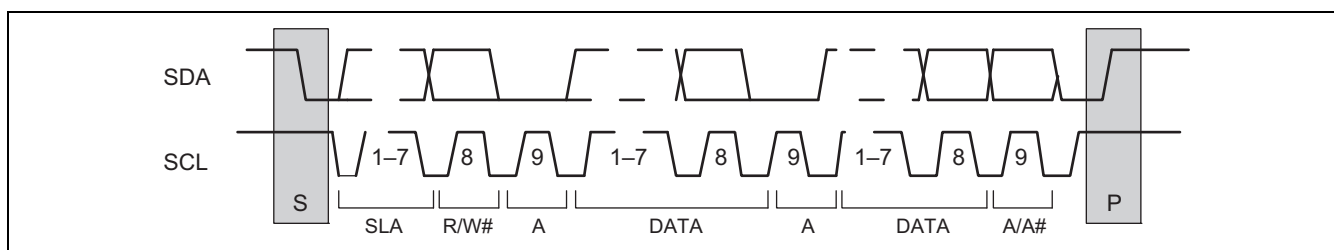


Figure 44.2 I2C Bus Timing

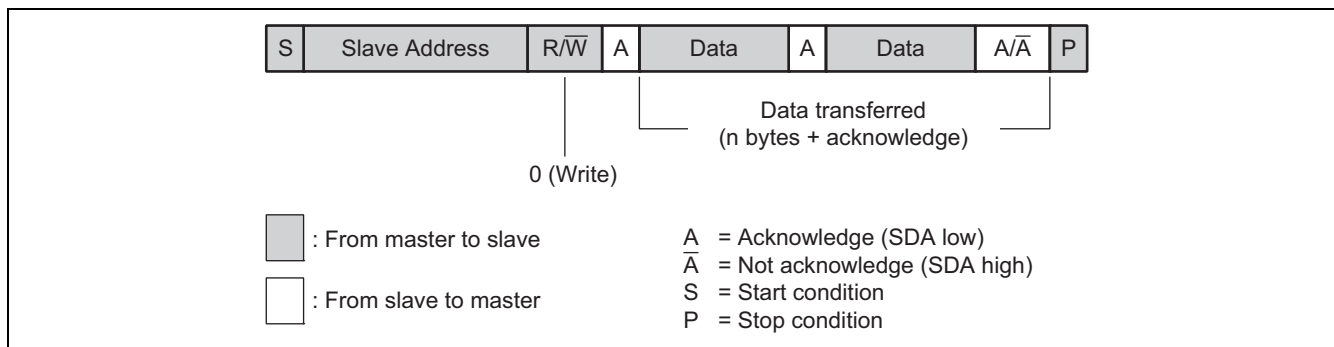
Table 44.4 Description on Symbols of I2C Bus Data Format

Symbol	Description
S	Indicates a start condition. A master device changes SDA from high to low while SCL is high level.
SLA	Indicates a slave address. A slave address is used when a master device selects a slave device.
R/W	Indicates the direction of data transmission. If the R/W bit is 1, the data flows from the slave to the master device. If the bit is 0, the data flows from the master to the slave device.
A	Indicates data acknowledge. Data receiving device makes SDA low level (the slave device returns a data acknowledge signal in master transmission mode, and vice versa).
DATA	Indicates transmit or receive data. The data length is eight bits, which are transferred in the MSB first.
P	Indicates a stop condition. A master device changes SDA from low to high while SCL is high.

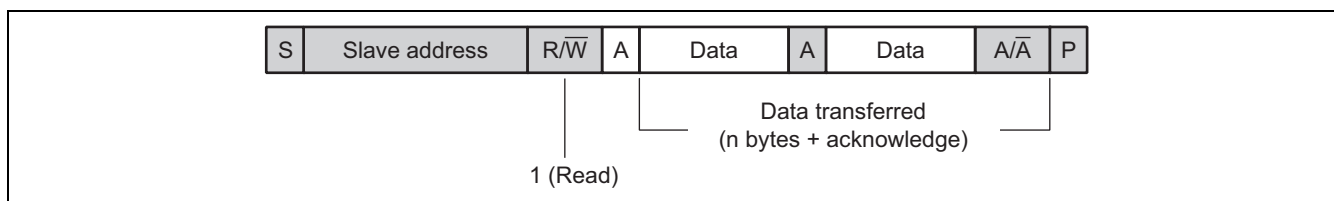


**44.4.6 7-Bit Address Format**

Figure 44.3 shows the format of data transfer from a master to a slave device (master data transmit format). Figure 44.4 shows the data transfer format (master data receive format) when a master device reads the second and the following byte data from a slave device.

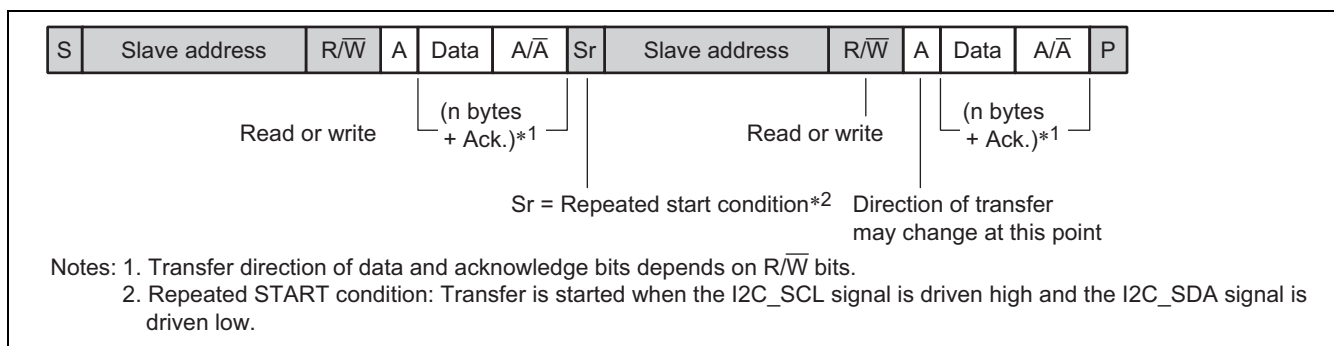


**Figure 44.3 Master Data Transmit Format**



**Figure 44.4 Master Data Receive Format**

Figure 44.5 shows the combined format when the data transfer direction changes during one transfer. When changing the direction after the first transfer, the repeated START condition (Sr), slave address and R/W bits are transmitted. In this case, the R/W bit is set to the direction opposite to the first transfer direction. The repeated START condition is issued by the master at the end of a transmit or receive cycle if the enable start generation bit in the master control register has been set.

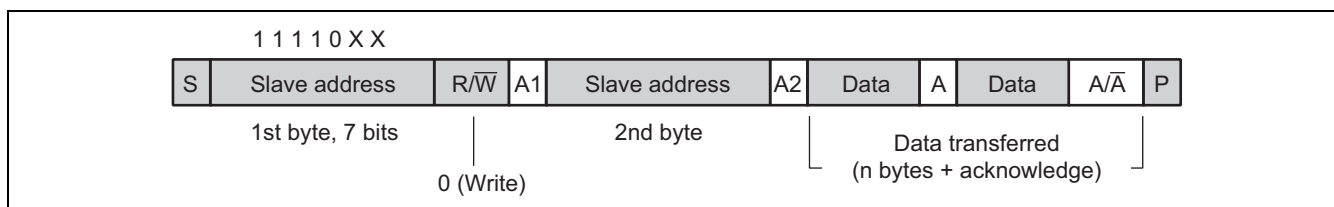


**Figure 44.5 Combination Transfer Format of Master Transfer**

### 44.4.7 10-Bit Address Format

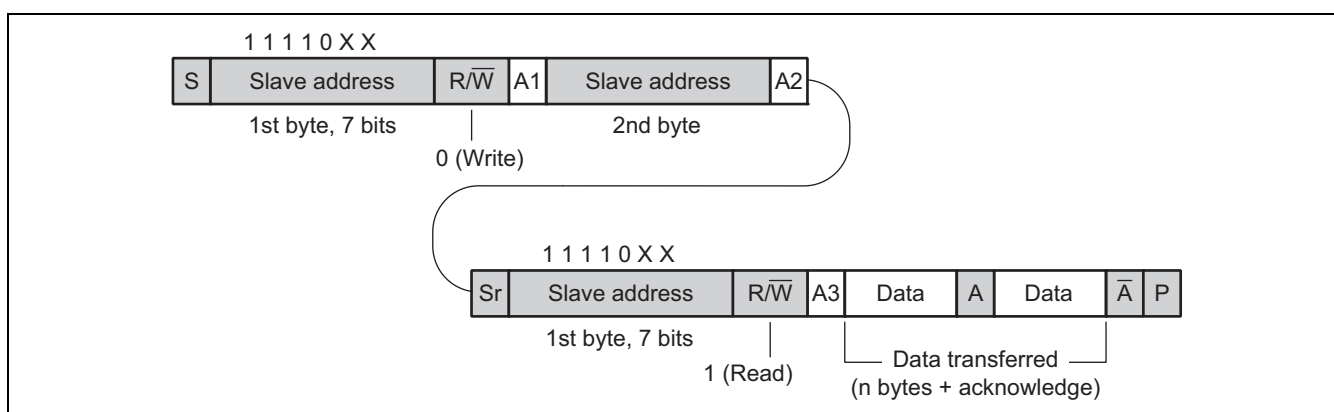
Description is given below on the 10-bit address transfer format supported in master mode. This format has three transfer methods as the 7-bit address transfer format.

Figure 44.6 shows the data transmit format. The set value in the master address register is output in one byte following the first START condition (S). The value set in the transmit data register (TXD) is transmitted as a slave address in the second byte. Data on and after the third byte is transferred in the same way as the 7-bit address data.



**Figure 44.6 10-Bit Address Data Transmit Format**

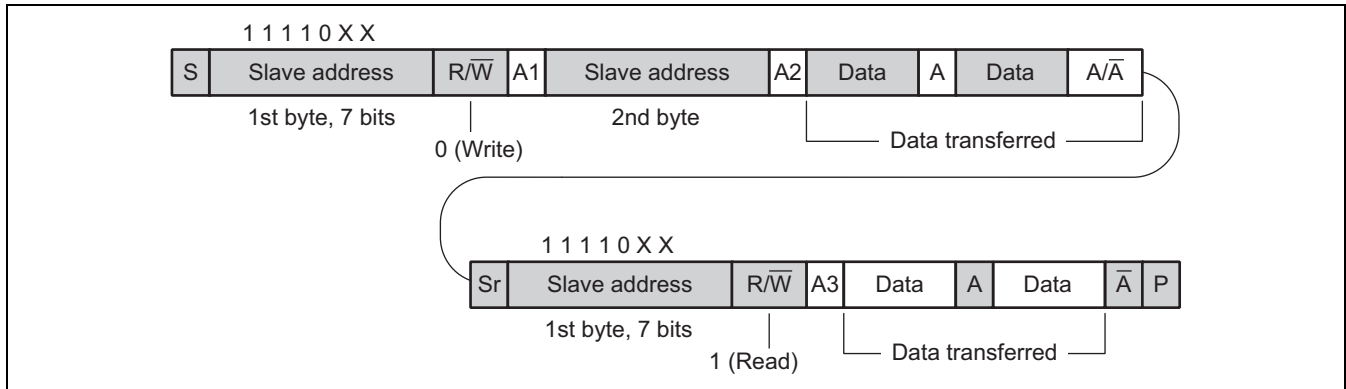
Figure 44.7 shows the data receive format. Two bytes of an address is transmitted in the same way as in the data transmit format. Then, repeated START condition (Sr) is transmitted and the value set in the address register is output. At this time, STM1 must be set to 1 (receive mode). Data is transferred in the same way as in the 7-bit address data receive format.



**Figure 44.7 10-Bit Address Data Receive Format**

Figure 44.8 shows the data transmit/receive combined format.

In the data transmit/receive combined format, data is transmitted after an address is transmitted with the first two bytes. Then, the repeated START condition (Sr) is transmitted instead of STOP condition (P). After Sr is transmitted, the procedure is the same as that in the data receive format.



**Figure 44.8 10-Bit Address Transmit/Receive Combined Format**

#### 44.4.8 Master Transmit Operation

The procedure and operations for transmission in master transmit mode are described below. Figure 44.9 shows the timing chart in master transmit mode. Setting the MDBS bit in the master control register allows the I2C to operate in single-buffer mode.

1. Set up the initial state by setting the slave address register, transmission data register, clock control register, and master interrupt enable register. Note that the setting of the clock control register must be in accord with the rate of transmission. Since slave mode is also required even when master mode is used, set the device address in the slave address register.
2. Monitor the FSDA bit in the master control register. Confirm that this bit is low, meaning that other I2C devices are not using the bus. After confirmation, set the MIE (bit 3) and ESG (bit 0) bits in the master control register to 1 to start master transmission.
3. After the transmit START condition, slave address, and data transfer direction bits are transmitted, an interrupt due to the MAT and MDE bits in the master status register is generated at the timing of (1) in Figure 44.9. At this time, clear the ESG bit to 0. To suspend the data transmission, the master device will hold SCL low until the MDE bit is cleared.
4. An interrupt due to the SAR bit is generated at the timing of (3) shown in Figure 44.9. If the IRQ handling in the slave device is delayed, the slave device extends the SCL period to suspend data transmission (at the timing of (7) in Figure 44.9). The slave device drives SDA low at the ninth clock and returns ACK.
5. Data is transmitted in units of nine bits: 8-bit data and 1-bit ACK. An interrupt of MDE (bit 3) is generated at the ninth clock before data transfer (at the timing of (2) in Figure 44.9). An interrupt of MDT (bit 2) is generated at the eighth clock after 1-byte data transfer (at the timing of (4) in Figure 44.9). Clear MDE to 0 after setting transmit data. An interrupt of SDR (slave data receive) of the slave device is generated at the eighth clock (at the timing of (6) in Figure 44.9). Clear SDR after the slave device reads the receive data. If this processing is delayed, the slave device extends the SCL period to suspend data transmit (at the timing of (8) in Figure 44.9).
6. To end data transfer, an interrupt of MNR (bit 6) in the master status register is generated at the ninth clock (at the timing of (5) in Figure 44.9) when ACK from the slave device is 1 (NACK). The master device receives this NACK and outputs the STOP condition. When data transmission ends on the master device side, set FSB (bit 1) in the master control register to 1 to output the STOP condition. After the I2C module fetches FSB on completion of transmission or reception of the last bit of byte data, it enters the stop state. Therefore in order to stop the communication after the predetermined number of byte data is transferred, the FSB bit needs to be set before the last byte data transfer is started.
7. The FSB bit needs to be set before the last byte data is transferred. In master transmit mode, after the last byte data is set, the MST (master stop transmitted) bit is checked by either interrupt or polling. At the same time MNR (master NACK received) bit must be checked. If NACK is returned, an error routine is executed to retransmit the last byte data.

Signal level changes of (1) to (6) in Figure 44.9 are generated after the falling edge of the clock.

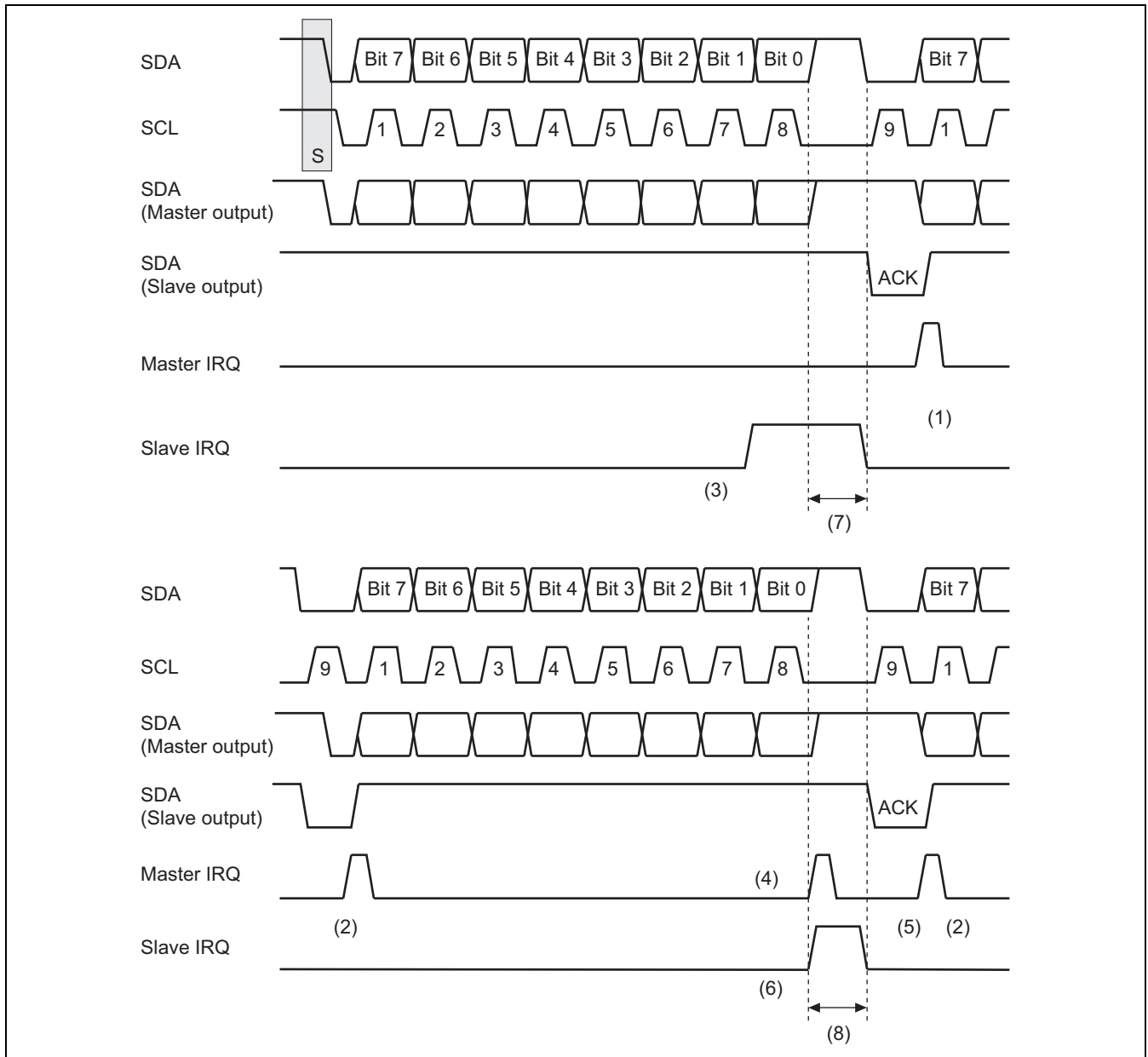


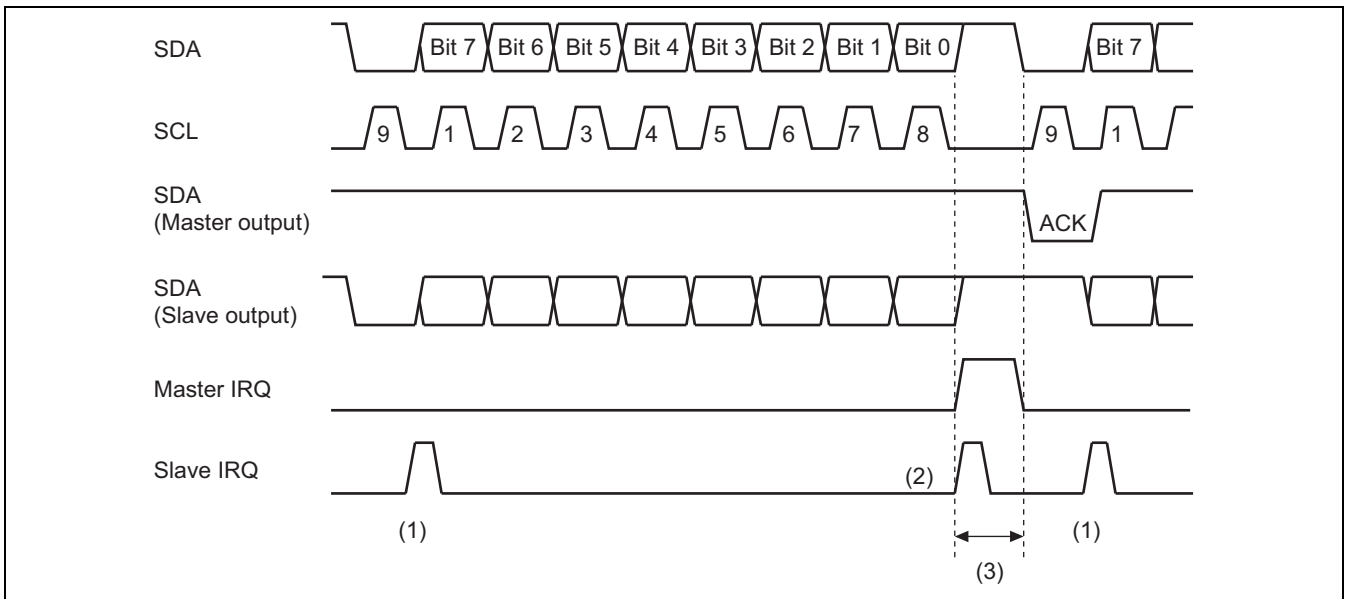
Figure 44.9 Data Transmit Mode Operation Timing

**44.4.9 Master Receive Operation**

The data receive procedure and operation in master receive mode are described below. Figure 44.10 shows the timing chart in master receive mode. Setting the MDBS bit in the master control register allows the I2C to operate in single-buffer mode.

1. In master receive mode, as to transmit of a slave address and a 1-bit signal indicating the data transfer direction, operation is the same as that in master transmit mode. At this time, set the data transfer direction to 1 (reception).
2. The slave device automatically enters the data transmit mode according to the signal that indicates the data transfer direction, and transmits 1-byte data in synchronization with the SCL clock output from the master device. The master device generates an interrupt of MDR (bit 1) at the eighth clock (at the timing of (2) in Figure 44.10). Clear the MDR bit after the master device reads receive data. If this processing is delayed, the master device extends the SCL period to suspend data transmission (at the timing of (3) in Figure 44.10).
3. The slave device generates an interrupt of the status SDT (bit 2) indicating 1-byte data transfer end at the eighth clock (at the timing of (2) in Figure 44.10) and an interrupt of the status SDE (bit 3) indicating data empty at the ninth clock (at the timing of (1) in Figure 44.10). Clear SDE after writing slave transmit data to TXD.
4. To end data transfer, set FSB (bit 1) in the master control register of the master device and output STOP condition. After the I2C module fetches FSB on completion of transmission or reception of the last of byte data, it enters the stop state. Therefore in order to stop the communication after predetermined number of byte data is transferred, FSB bit needs to be set before the last byte data transfer is started. After confirming reception of the last byte, even when the master receiver has completed the reception transaction, the protocol layer will inform the slave transmitter that retransmission is necessary if the last byte is incorrect.

Signal level changes of (1) to (3) in Figure 44.10 are generated after the falling edge of the clock.



**Figure 44.10 Data Receive Mode Operation Timing**

## 44.5 Programming Examples

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

### 44.5.1 Master Transmitter

In order to set up the master interface to transmit a data packet on the I2C bus, follow the procedure below (an example for I2C0):

#### (1) Load value for the clock control register

(When the module clock frequency is 130 MHz and SCL clock frequency is set to 400 kHz)

1. Set the SCL clock generation divider bit (SCGD) to H'3.
2. Set the clock division ratio bit (CDF) to H'6 (I2C internal clock I2Cck: 18.57 MHz).

#### (2) Load value for the master control register, first data byte, and address

1. Master address register = address of slave being accessed and STM1 bit (write mode: 0)
2. Transmit data register = first data byte to be transmitted
3. Master control register = H'89 (MDBS = 1, MIE = 1, ESG = 1)

#### (3) Wait for outputting address

1. Wait for master event (an interrupt of the MAT and MDE bits in the master status register).
2. Set the master control register to H'88 (to suspend the data transmission, the master device will hold the SCL low until the MDE bit is cleared).

If only one byte of data is transmitted, set the master control register to H'8A, meaning that the stop generation is enabled. This generates a stop on the bus as soon as one byte has been transmitted.

3. Reset the MAT and MDE bits.

#### (4) Monitor transmission of data

1. Wait for master event, MDE in the master status register.
2. Transmit data register = subsequent data.
3. Reset the MDE bit.

Clear MDE after setting the last byte to be transmitted. After the last byte data is transmitted, MDE is generated. Before clearing MDE, you must set the master control register to H'8A (set the force stop control bit).

#### (5) Wait for end of transmission

1. Wait for the master event, MST in the master status register.
2. Reset the MST bit after confirming MNR (master NACK received).

### 44.5.2 Master Receiver

In order to set up the master interface to receive a data packet on the I2C bus, follow the procedure below:

#### (1) Load value for the clock control register

The same procedure as the master transmitter is applied. See the program example for the master transmitter.

#### (2) Load value for the master control register and address

1. Master address register = address of slave being accessed and STM1 bit (read mode: 1)
2. Master control register = H'89 (MDBS = 1, MIE = 1, ESG = 1)

#### (3) Wait for outputting address

1. Wait for master event (an interrupt of the MAT and MDR bits in the master status register).
2. Set the master control register to H'88 (to suspend the data transmission, the master device will hold the SCL low until the MDR bit is cleared).

If only one byte of data is transmitted, set the master control register to H'8A, meaning that the stop generation is enabled. This generates a stop on the bus as soon as one byte has been transmitted.

3. Reset the MAT and MDR bits.

#### (4) Monitor reception of data

1. Wait for master event (the MDR bit in the master status register).
2. Read data from the received data register.

If the next byte of data is the second to last byte to be transmitted by the slave device, the following applies to the receive interrupt (that is, MDR interrupt) in the second to last byte.

3. Set the master control register to H'8A (set the force stop control bit).
4. Reset the MDR bit.

#### (5) Wait for end of reception

1. Handle the receive interrupt (MDR) in the last byte: that is, read the data and clear the MDR.
2. Wait for master event, MST in the master status register.
3. Reset the MST bit.

### 44.5.3 Master Transmitter—Repeated START—Master Receiver

In order to set up the master interface to transmit a data packet on the I2C bus, issue a repeated START condition, then read byte data back from the slave, follow the procedure below:

#### (1) Load value for the clock control register

The same procedure as the master transmitter is applied. See the program example for the master transmitter.

#### (2) Load value for the master control register and address

1. Master address register = address of slave being accessed and STM1 bit (write mode: 0)
2. Transmit data register = first data byte to be transmitted
3. Master control register = H'89 (MDBS = 1, MIE = 1, ESG = 1)
4. Wait until slave-address transfer have started, and set master control register to H'88 (MDBS=1, MIE=1, ESG=0). (Start of slave address transfer can be checked by FSDA bit, or waiting enough time after setting ESG bit).

#### (3) Wait for outputting slave-address for master transmission

1. Wait for master event (an interrupt of the MAT and MDE bits in the master status register).
2. Set the master address register to address of slave being accessed and STM1 bit (read mode: 1).  
When the enable start generation bit in the master control register is still set, at the end of the byte transmission the master will issue a repeated START condition. Since the new address has been loaded above, the bus direction will be changed.
3. Reset the MAT and MDE bits.

#### (4) Monitor transmission of data

1. Wait for master event (an interrupt of the MDE bit in the master status register).
2. Master control register = H'89 (MDBS = 1, MIE = 1, ESG = 1)
3. Reset the MDE bit.

#### (5) Wait for outputting slave-address for master reception

1. Wait for master event (an interrupt of the MAT and MDR bits in the master status register).
2. Set the master control register to H'88. (To suspend stop the data transmission, the master device will hold the SCL low until the MDR bit is cleared.)
3. Reset the MAT and MDR bits.

#### (6) Monitor reception of data

1. Wait for master event (the MDR bit in the master status register).
2. Read data from the received data register.  
If the next byte of data is the second to last byte to be transmitted by the slave device, the following applies to the receive interrupt (that is, MDR interrupt) in the second to last byte.
3. Set the master control register to H'8A (set the force stop control bit).
4. Reset the MDR bit.

#### (7) Wait for end of reception

1. Handle the receive interrupt (MDR) in the last byte: that is, read the data and clear the MDR.
2. Wait for master event, MST in the master status register.
3. Reset the MST bit.



## 44.6 Usage Note

### 44.6.1 SCL frequency calculation equation

In section 44.3.9, Clock Control Register (ICCCR), in the description of SCGD and CDF, following equation is described.

$$\text{SCLfreq} = \text{I2Cck} / (20 + \text{SCGD} \times 8 + F[(\text{tICF} + \text{tr} + \text{IntDelay}) \times \text{I2Cck}])$$

I2Cck: I2C internal clock frequency

tICF: I2C SCL falling time (depending on external load)

tr: I2C SCL rising time (depending on external load)

IntDelay: LSI internal delay corresponds to output buffer type.

Open drain buffer: 50 ns (typ.), 110 ns (max.)

LVTTL (low drive only) buffer: 5 ns (typ.), 6 ns (max.).

F[n]: n rounded up to an integer

$$\text{I2Cck} = \text{MOD\_CLK} / (1 + \text{CDF})$$

MOD\_CLK: module clock frequency

Based on parameter described above, this equation approximately estimates the SCL frequency, but includes some error in the resulting frequency. Before finalizing register setting to be used, measure actual SCL frequency on the board, and confirm that observed frequency satisfy the constraint. The reason why calculated result includes some error is parameters used in this equation varies depending on the characteristics of each sample. For example, tICF and tr depend on logical threshold of IO-cell, and intDelay depends on variation of fabrication process.

For adjustment of SCL frequency, modifying the setting of ICCCR[2:0].CDF and ICCCR[8:3].SCGD will be effective. Increasing the value of CDF or SCGD value will make SCL frequency lower. However, how they decrease SCL frequency is different. So, by increasing one register value and decreasing the other, SCL frequency can be adjusted.

## 45. IIC Bus Interface (IIC)

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

The IIC bus interface uses only one data line (SDA) and one clock line (SCL) to transfer data, saving board and connector space.

### 45.1 Features

The RZ/G series products have up to four IIC bus interface modules (IIC0, IIC1, IIC2, and IIC3).

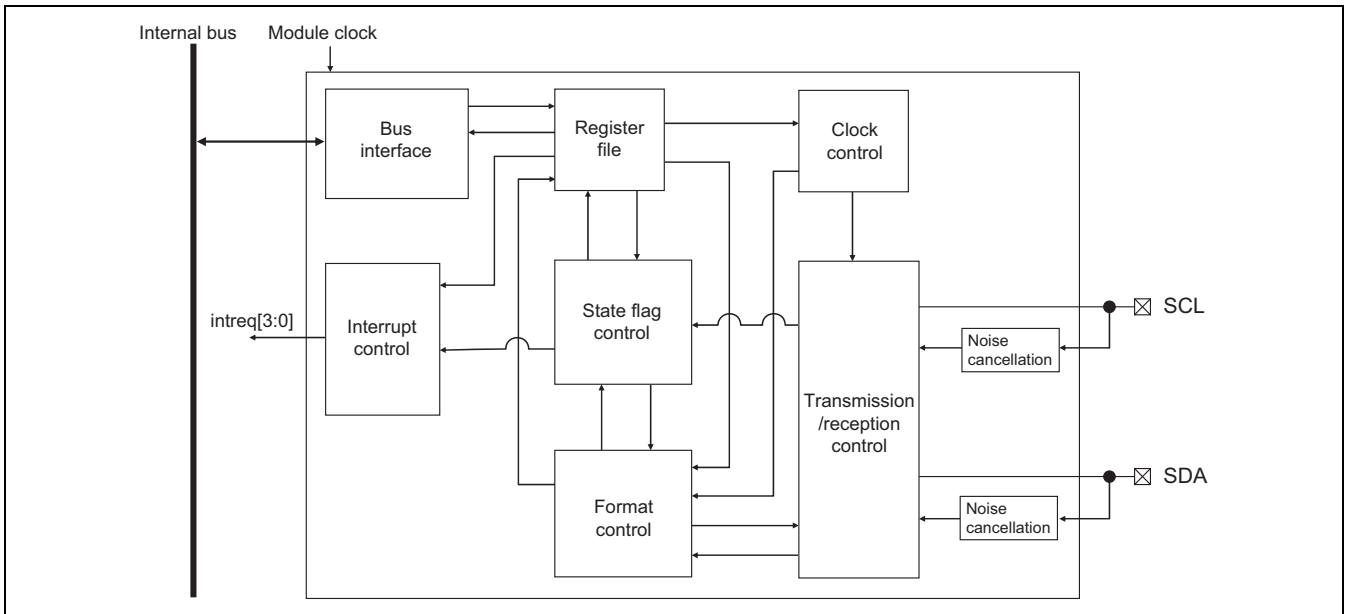
The module clock for the IIC0, IIC1, and IIC2 is HP $\phi$ .

The module clock for the IIC3 is CP $\phi$ .

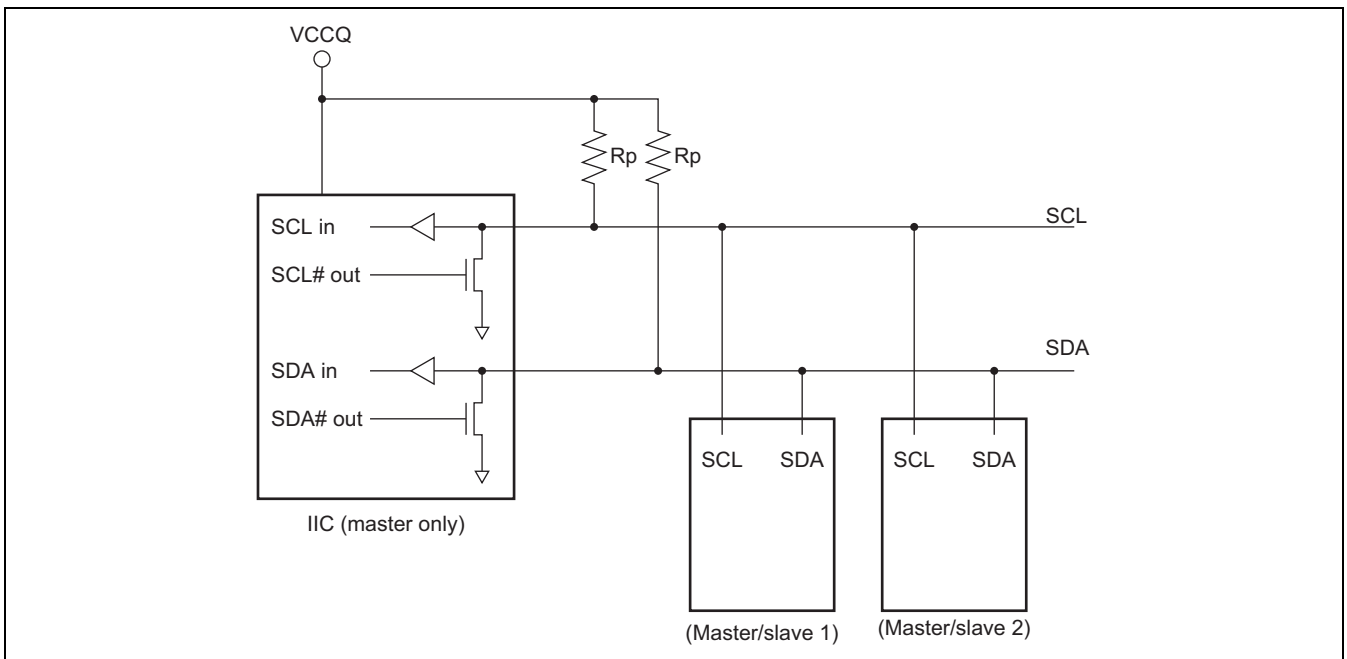
- Data transfer based on I2C bus format from Philips Semiconductor (now NXP Semiconductors)
- Automatic generation of START and STOP conditions
- Control of acknowledge level after receiving data
- Automatic checking of acknowledge bit after transmitting data
- Wait function
  - A wait can be inserted by driving the SCL pin low after data transfer, excluding acknowledgement.
  - The wait can be canceled by clearing the interrupt flag.
- This module supports only master mode.
  - If arbitration is lost, data transfer is stopped and I2C bus is released.
- Four interrupt sources
  - Data transfer enable
  - Wait state
  - Non-acknowledge detection
  - Arbitration lost
- Data transfer speed
  - Supports standard-mode (100 kHz) and fast-mode (400 kHz)
  - SCL clock frequency can be controlled by register setting.
- Supports clock synchronization of SCL line
  - A hazard (transient spike) in the SCL high-count period is detected as a loss of arbitration.
- DMA transfer
  - Supports DMA transfer (for both transmission and reception).

Note: Automatic transmission for PMIC control (DVFS) is not available because the RZ/G series products do not support the DVFS function (automatic transmission can be used as a hardware function, but this is not meaningful for actual use cases).

Figure 45.1 shows a block diagram of the IIC bus interface module.



**Figure 45.1 Block Diagram of IIC Bus Interface Module**



**Figure 45.2 Connection Example of IIC Bus Interface Module**

## 45.2 Input/Output Pins

Table 45.1 summarizes the input/output pins used by the IIC bus interface.

**Table 45.1 IIC Bus Interface Pins**

Channel Number	Pin Name* <sup>1</sup>	I/O	Function	RZ/G Series Products			
				RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
				Output Buffer Type* <sup>2</sup>			
0	SCL	I/O	SCL:	OD* <sup>3</sup>	LVTTL	LVTTL	LVTTL
	SDA		IIC serial clock input/output pin				
1	SCL		SDA:	LVTTL* <sup>3</sup>	LVTTL	LVTTL	OD
	SDA		IIC serial data input/output pin				
2	SCL			LVTTL* <sup>3</sup>	—	—	—
	SDA						
3	SCL			OD* <sup>3</sup>	OD	OD	—
	SDA						

Notes: 1. The actual pin names are IICn\_SCL and IICn\_SDA (n = 0 to 3 for RZ/G1H, and 0, 1 and 3 for RZ/G1M, N). These are referred to as SCL and SDA in this section.

2. Output buffer type: "OD" is open drain buffer and "LVTTL" is low level drive only LVTTL buffer. OD assigned channel pins are 1.8 V I/O and input/output 3.3 V tolerant; LVTTL assigned channel pins are 3.3 V I/O.

3. These pins are shared with the I2C module. Select either I2C or IIC for each channel.

The IIC buffer in this LSI is not compliant with the 5V-input. When turning off the I/O power source (3.3 V) of this LSI, turn off the power source of the pull-up resistors connected to the I2C pins.

Note: When using 1.8V I2C/IIC pins (OD assigned channel) as 3.3 V tolerant, all the external pull-up voltage power supply to the I2C/IIC of this LSI must keep the same power on/off sequence as the VCCQ (3.3 V) of this LSI.

### 45.3 Register Descriptions

Table 45.2 shows the register configuration of the IIC bus interface. Table 45.3 shows the register state in each processing mode.

The base address for each channel of the IIC bus interface registers is as follows:

- IIC0: H'E650\_0000 (RZ/G1H, M, N and E)
- IIC1: H'E651\_0000 (RZ/G1H, M, N and E)
- IIC2: H'E652\_0000 (RZ/G1H only)
- IIC3\*: H'E60B\_0000 (RZ/G1H, M and N)

Note:\* Automatic transmission for PMIC control (DVFS) is not available because the RZ/G series products do not support the DVFS function (automatic transmission can be used as a hardware function, but this is not meaningful for actual use cases).

Each channel of the IIC bus interface module has the registers below.

**Table 45.2 Register Configuration of Bus Interface**

Register Name	Abbreviation	R/W	Offset Address	Size	RZ/G Series Products			
					RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
IIC bus data register	ICDR	R/W	H'000	8	√	√	√	√
IIC bus control register	ICCR	R/W	H'004	8	√	√	√	√
IIC bus status register	ICSR	R/W	H'008	8	√	√	√	√
IIC interruption control register	ICIC	R/W	H'00C	8	√	√	√	√
IIC clock control register low	ICCL	R/W	H'010	8	√	√	√	√
IIC clock control register high	ICCH	R/W	H'014	8	√	√	√	√
IIC transmit register	ICTR	R	H'018	8	√	√	√	√
IIC receive register	ICRR	R	H'01C	8	√	√	√	√
IIC transmit monitor register	ICTA	R	H'020	8	√	√	√	√
IIC transmit buffer monitor register	ICTB	R	H'024	8	√	√	√	√
IIC transmit control register	ICTC	R/W	H'028	8	√	√	√	√
IIC transmit control status monitor register	ICTD	R	H'02C	8	√	√	√	√
IIC shift register	ICSF	R	H'030	8	√	√	√	√
IIC option enabling register*	ICVCON	R/W	H'06C	8	√	√	√	√
IIC automatic transmission interrupt mask register*	ICIMSK	R/W	H'050	8	√	√	√	—
IIC automatic transmission interrupt flag register*	ICINT	R	H'054	8	√	√	√	—
IIC automatic transmission processing enabling register*	ICACE	R/W	H'058	8	√	√	√	—
IIC automatic transmission timer control register 1*	ICTMC1	R/W	H'060	8	√	√	√	—
IIC automatic transmission timer control register 2*	ICTMC2	R/W	H'064	8	√	√	√	—

**RZ/G Series  
Products**

Register Name	Abbreviation	R/W	Offset Address	Size	RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
IIC automatic transmission wait control register*	ICTMCW	R/W	H'068	8	√	√	√	—
IIC automatic transmission transmit start register*	ICSTART	R/W	H'070	8	√	√	√	—
IIC automatic transmission transmit control register*	ICATFR	R/W	H'080	8	√	√	√	—
IIC automatic transmission transmit time register 1*	ICATSET1	R/W	H'084	8	√	√	√	—
IIC automatic transmission transmit time register 2*	ICATSET2	R/W	H'088	8	√	√	√	—
IIC automatic transmission reception time register 1*	ICARSET1	R/W	H'08C	8	√	√	√	—
IIC automatic transmission reception time register 2*	ICARSET2	R/W	H'090	8	√	√	√	—
IIC automatic transmission transmit data 00*	ICATD00	R/W	H'100	8	√	√	√	—
IIC automatic transmission transmit data 01*	ICATD01	R/W	H'104	8	√	√	√	—
IIC automatic transmission transmit data 02*	ICATD02	R/W	H'108	8	√	√	√	—
IIC automatic transmission transmit data 03*	ICATD03	R/W	H'10C	8	√	√	√	—
IIC automatic transmission transmit data 04*	ICATD04	R/W	H'110	8	√	√	√	—
IIC automatic transmission transmit data 05*	ICATD05	R/W	H'114	8	√	√	√	—
IIC automatic transmission transmit data 06*	ICATD06	R/W	H'118	8	√	√	√	—
IIC automatic transmission transmit data 07*	ICATD07	R/W	H'11C	8	√	√	√	—
IIC automatic transmission transmit data 08*	ICATD08	R/W	H'120	8	√	√	√	—
IIC automatic transmission transmit data 09*	ICATD09	R/W	H'124	8	√	√	√	—
IIC automatic transmission transmit data 10*	ICATD10	R/W	H'200	8	√	√	√	—
IIC automatic transmission transmit data 11*	ICATD11	R/W	H'204	8	√	√	√	—
IIC automatic transmission transmit data 12*	ICATD12	R/W	H'208	8	√	√	√	—
IIC automatic transmission transmit data 13*	ICATD13	R/W	H'20C	8	√	√	√	—
IIC automatic transmission transmit data 14*	ICATD14	R/W	H'210	8	√	√	√	—
IIC automatic transmission transmit data 15*	ICATD15	R/W	H'214	8	√	√	√	—
IIC automatic transmission transmit data 16*	ICATD16	R/W	H'218	8	√	√	√	—
IIC automatic transmission transmit data 17*	ICATD17	R/W	H'21C	8	√	√	√	—
IIC automatic transmission transmit data 18*	ICATD18	R/W	H'220	8	√	√	√	—
IIC automatic transmission transmit data 19*	ICATD19	R/W	H'224	8	√	√	√	—
IIC automatic transmission receipt data 00*	ICARD00	R	H'300	8	√	√	√	—
IIC automatic transmission receipt data 01*	ICARD01	R	H'304	8	√	√	√	—
IIC automatic transmission receipt data 02*	ICARD02	R	H'308	8	√	√	√	—
IIC automatic transmission receipt data 03*	ICARD03	R	H'30C	8	√	√	√	—
IIC automatic transmission receipt data 04*	ICARD04	R	H'310	8	√	√	√	—
IIC automatic transmission receipt data 05*	ICARD05	R	H'314	8	√	√	√	—
IIC automatic transmission receipt data 06*	ICARD06	R	H'318	8	√	√	√	—
IIC automatic transmission receipt data 07*	ICARD07	R	H'31C	8	√	√	√	—

Register Name	Abbreviation	R/W	Offset Address	Size	RZ/G Series Products			
					RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
IIC automatic transmission receipt data 08*	ICARD08	R	H'320	8	√	√	√	—
IIC automatic transmission receipt data 09*	ICARD09	R	H'324	8	√	√	√	—
IIC automatic transmission receipt data 10*	ICARD10	R	H'400	8	√	√	√	—
IIC automatic transmission receipt data 11*	ICARD11	R	H'404	8	√	√	√	—
IIC automatic transmission receipt data 12*	ICARD12	R	H'408	8	√	√	√	—
IIC automatic transmission receipt data 13*	ICARD13	R	H'40C	8	√	√	√	—
IIC automatic transmission receipt data 14*	ICARD14	R	H'410	8	√	√	√	—
IIC automatic transmission receipt data 15*	ICARD15	R	H'414	8	√	√	√	—
IIC automatic transmission receipt data 16*	ICARD16	R	H'418	8	√	√	√	—
IIC automatic transmission receipt data 17*	ICARD17	R	H'41C	8	√	√	√	—
IIC automatic transmission receipt data 18*	ICARD18	R	H'420	8	√	√	√	—
IIC automatic transmission receipt data 19*	ICARD19	R	H'424	8	√	√	√	—

Note: \* In automatic transmission mode, data transmission ends by interrupt or error detection. Do not perform register polling during automatic transmission.

**Table 45.3 Register State in Each Processing Mode**

Register name	Reset	Module Standby
ICDR	Initialized	Retained
ICCR	Initialized	Retained
ICSR	Initialized	Retained
ICIC	Initialized	Retained
ICCL	Initialized	Retained
ICCH	Initialized	Retained
ICTR	Initialized	Retained
ICRR	Initialized	Retained
ICTA	Initialized	Retained
ICTB	Initialized	Retained
ICTC	Initialized	Retained
ICTD	Initialized	Retained
ICSF	Initialized	Retained
ICVCON	Initialized	Retained
ICIMSK	Initialized	Retained
ICINT	Initialized	Retained
ICACE	Initialized	Retained
ICTMC1	Initialized	Retained
ICTMC2	Initialized	Retained
ICTMCW	Initialized	Retained
ICSTART	Initialized	Retained
ICATFR	Initialized	Retained

Register name	Reset	Module Standby
ICATSET1	Initialized	Retained
ICATSET2	Initialized	Retained
ICARSET1	Initialized	Retained
ICARSET2	Initialized	Retained
ICATD00	Initialized	Retained
ICATD01	Initialized	Retained
ICATD02	Initialized	Retained
ICATD03	Initialized	Retained
ICATD04	Initialized	Retained
ICATD05	Initialized	Retained
ICATD06	Initialized	Retained
ICATD07	Initialized	Retained
ICATD08	Initialized	Retained
ICATD09	Initialized	Retained
ICATD10	Initialized	Retained
ICATD11	Initialized	Retained
ICATD12	Initialized	Retained
ICATD13	Initialized	Retained
ICATD14	Initialized	Retained
ICATD15	Initialized	Retained
ICATD16	Initialized	Retained
ICATD17	Initialized	Retained
ICATD18	Initialized	Retained
ICATD19	Initialized	Retained
ICARD00	Initialized	Retained
ICARD01	Initialized	Retained
ICARD02	Initialized	Retained
ICARD03	Initialized	Retained
ICARD04	Initialized	Retained
ICARD05	Initialized	Retained
ICARD06	Initialized	Retained
ICARD07	Initialized	Retained
ICARD08	Initialized	Retained
ICARD09	Initialized	Retained
ICARD10	Initialized	Retained
ICARD11	Initialized	Retained
ICARD12	Initialized	Retained
ICARD13	Initialized	Retained
ICARD14	Initialized	Retained
ICARD15	Initialized	Retained
ICARD16	Initialized	Retained
ICARD17	Initialized	Retained
ICARD18	Initialized	Retained
ICARD19	Initialized	Retained



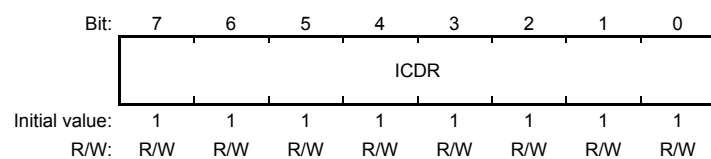
### 45.3.1 IIC Bus Data Register (ICDR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

ICDR is an 8-bit readable/writable register that is used as a transmit data register when transmitting and a receive data register when receiving.

In transmission mode, write transmit data to this register when the DTE bit in the IIC bus status register (ICSR) is 1.

In receive mode, read receive data from this register when the DTE bit in the IIC bus status register (ICSR) is 1.



### 45.3.2 IIC Bus Control Register (ICCR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

ICCR is an 8-bit readable/writable register that enables or disables the IIC bus interface, specifies the transmission/receive mode, issues START/STOP conditions, and confirms the IIC bus interface bus status.

**Table 45.4 ICCR Settings**

Operation	Write Data to ICCR (Transmission Mode)	Write Data to ICCR (Receive Mode)
START condition	H'94	—
Repeated START condition	H'94	—
Repeated START condition with transmission/receive mode change	H'81 (Change from transmission mode to receive mode)	H'D4 (Change from receive mode to transmission mode)
STOP condition	H'90	H'C0

Bit:	7	6	5	4	3	2	1	0
	ICE	RACK	—	TRS	—	BBSY	—	SCP
Initial value:	0	0	0	0	0	0	0	1
R/W:	R/W	R/W	R	R/W	R	R/W	R	(R/W)*

Bit	Bit Name	Initial Value	R/W	Description
7	ICE	0	R/W	<p>IIC Bus Interface Enable</p> <p>Enables or disables the IIC bus interface.</p> <p>When this bit is set to 1, transfer operation is enabled. When this bit is cleared to 0 during data transmission, the I2C bus is released and all registers in this module are initialized. (See section 45.6, Usage Note.)</p> <p>When this bit is cleared to 0 after data transmission, all registers in this module are initialized.</p> <p>When the ICCR is updated while this module is operating, this bit must be set to 1.</p> <p>0: IIC bus interface module is disabled. (All internal registers are initialized.)</p> <p>1: IIC bus interface module is enabled.</p>
6	RACK	0	R/W	<p>Receive Acknowledge</p> <p>Specifies the acknowledge level in receive mode.</p> <p>In reception, this bit provides the acknowledge level for output on the SDA line after the IIC module receives data.</p> <p>0: In receive mode, 0 is output to SDA at acknowledge output timing.</p> <p>1: In receive mode, 1 is output to SDA at acknowledge output timing.</p>
5	—	0	R	<p>Reserved</p> <p>This bit is always read as 0. The write value should always be 0.</p>

Bit	Bit Name	Initial Value	R/W	Description
4	TRS	0	R/W	<p>Transmit/Receive Select</p> <p>Specifies either transmission mode or receive mode.</p> <p>The setting of this bit can be rewritten even during data transfer, but actual operating mode is changed after completion of ongoing transfer including acknowledge bit.</p> <p>0: Master reception mode.</p> <p>1: Master transmission mode.</p> <p>When writing 1 to this bit, also set BBSY and SCP bits at the same time.</p>
3	—	0	R	<p>Reserved</p> <p>This bit is always read as 0. The write value should always be 0.</p>
2	BBSY	0	R/W	<p>Bus Busy</p> <p>This bit is used to issue START and STOP conditions.</p> <p>To issue a START condition, write 1 to this bit and 0 to the SCP bit. A repeated START condition is issued in the same way. To issue a STOP condition, write 0 to this bit and 0 to the SCP bit.</p> <p>0: A STOP condition is issued (the SCP bit is also used).</p> <p>1: A START or repeated START condition is issued (the SCP bit is also used).</p>
1	—	0	R	<p>Reserved</p> <p>This bit is always read as 0. The write value should always be 0.</p>
0	SCP	1	(R/W)*	<p>START Condition/STOP Condition Prohibit</p> <p>Controls issuance of START and STOP conditions. To issue a START condition, write 1 to the BBSY bit and 0 to this bit. A repeated START condition is issued in the same way. To issue a STOP condition, write 0 to the BBSY bit and 0 to this bit. This bit is always read as 1. Writing 1 to this bit is ignored.</p> <p>0: Writing 0 to this bit issues a START or STOP condition, in combination with the BBSY flag.</p> <p>1: Writing 1 to this bit is ignored.</p>

Note: \* For the SCP bit, only writing 0 is valid. Always read as 1.

### 45.3.3 IIC Bus Status Register (ICSR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

ICSR is an 8-bit readable/writable register that performs interrupt request.

Bit:	7	6	5	4	3	2	1	0
	SCLM	SDAM	—	BUSY	AL	TACK	WAIT	DTE
Initial value:	1	1	0	0	0	0	0	0
R/W:	R	R	R	R	R/(W)*	R/(W)*	R/(W)*	R

Bit	Bit Name	Initial Value	R/W	Description
7	SCLM	1	R	<p>SCL Monitor</p> <p>Indicates the SCL state sampled by the module clock.</p> <p>0: Indicates that SCL is 0.</p> <p>1: Indicates that SCL is 1.</p>
6	SDAM	1	R	<p>SDA Monitor</p> <p>Indicates the SDA state sampled by the module clock.</p> <p>0: Indicates that SDA is 0.</p> <p>1: Indicates that SDA is 1.</p>
5	—	0	R	<p>Reserved</p> <p>This bit is always read as 0. The write value should always be 0.</p>
4	BUSY	0	R	<p>IIC Transmit State Bit</p> <p>Indicates the IIC state. After the START condition is generated, the IIC enters the transfer state and this bit is set to 1. After the STOP condition is generated, the IIC enters the non-transfer state and this bit is cleared to 0.</p> <p>When a loss of arbitration is detected, the SDA line is immediately released, but output of the clock signal on SCL continues until frame acknowledgement is completed. This bit is cleared to 0 after end of frame transfer.</p> <p>0: The IIC module is not busy (transfer by the IIC module is not in progress).</p> <p>1: The IIC module is busy (transfer by the IIC module is in progress).</p> <p>Setting condition:</p> <p>The IIC module issues the START condition.</p> <p>Clearing condition:</p> <p>The IIC module issues the STOP condition.</p> <p>A loss of arbitration is detected (cleared after SCL clock output is stopped).</p>

Bit	Bit Name	Initial Value	R/W	Description
3	AL	0	R/(W)*	<p><b>Arbitration Lost</b></p> <p>Indicates a loss of arbitration.</p> <p>The IIC bus interface monitors the SDA. If the IIC bus interface detects data different from the data it sent, it sets this bit to 1 to indicate that the bus has been conflicted. This bit is reset by writing 0 to this bit or performing write access to ICDR in transmit mode or read access to ICDR in receive mode when the DTE bit is 1.</p> <p>When a loss of arbitration is detected during data transfer, the SDA line is immediately released. Output of the clock line on SCL continues until frame acknowledgement is completed. This bit does not depend on the ALE bit in ICIC and is always updated. When the ALE bit in ICIC is 0, an arbitration lost interrupt request is not issued to the interrupt controller. When other masters issue the START condition, a loss of arbitration is detected and operation is stopped.</p> <p>0: Bus arbitration won</p> <ul style="list-style-type: none"> <li>• When data are written to IDCR (transmit mode) or read from IDCR (receive mode)</li> <li>• When 0 is written to this bit after reading AL = 1</li> </ul> <p>1: Arbitration lost</p> <ul style="list-style-type: none"> <li>• When the level of the data being received changes during counting of the period at high level for the SCL clock in master receive mode</li> <li>• When the level on the SCL line becomes low during counting of the period at high level for the SCL clock</li> <li>• When a START condition is detected before this module issues its own START condition</li> <li>• When the monitored external SDA and data being output from this module not being equal</li> </ul>
2	TACK	0	R/(W)*	<p><b>Transmit Acknowledge Bit</b></p> <p>Indicates the level of the SDA line during acknowledge cycle in transmit mode. This bit is cleared by writing 0. This bit is always 0 when the TACK bit in ICIC is 0.</p> <p>0: Indicates that acknowledge (low level on SDA line) have been detected during acknowledge cycle.</p> <p>1: Indicates that no acknowledge (high level on SDA line) have been detected during acknowledge cycle.</p>
1	WAIT	0	R/(W)*	<p><b>Wait</b></p> <p>Indicates that this module have entered the wait state after data transmission other than the acknowledge bit.</p> <p>When the value of the WAITE bit in ICIC is 1, this module enters the wait state after data transfer (except for acknowledge bit), with driving the SCL to the low level. At this time, this bit is automatically set to 1 and a WAIT interrupt is generated. By writing 0 to this bit, this module recovers from the wait state.</p> <p>This bit is always 0 when WAITE in ICIC is 0.</p> <p>0: This module is in the normal state.</p> <p>1: This module is in the wait state.</p>

Bit	Bit Name	Initial Value	R/W	Description
0	DTE	0	R	<p>Data Transmit Enable</p> <p>Indicates the transmit state between ICDR and internal transmit/receive buffer. This bit is read only and automatically set or cleared.</p> <p>0: With the TACK bit set to 1,</p> <ul style="list-style-type: none"> <li>• When reset is performed</li> <li>• When data is written to ICDR in transmit mode (TRS = 1).</li> <li>• When data is read from ICDR in receive mode (TRS = 0).</li> <li>• When the TRS bit is changed.</li> <li>• When the repeated START condition/STOP conditions are written to the BBSY and SCP bits in ICCR.</li> </ul> <p>1:</p> <ul style="list-style-type: none"> <li>• When the START/repeated START conditions are generated.</li> <li>• When transmit data is sent to the transmit buffer from ICDR in transmit mode (TRS = 1).</li> <li>• When receive data is sent to ICDR in receive mode (TRS = 0).</li> </ul>

Note: \* Only 0 can be written for clearing the flag.

### 45.3.4 IIC Interrupt Control Register (ICIC)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

ICIC is an 8-bit register that enables or disables an interrupt request.

Bit:	7	6	5	4	3	2	1	0
	ICCLB8	ICCHB8	TDMAE	RDMAE	ALE	TACKE	WAITE	DTEE
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7	ICCLB8	0	R/W	IIC Clock Control Low Bit 8 Sets the low-level period of SCL when the period setting for the module in {ICIC[7], ICCL} is H'100 to H'1FF. Table 45.5 shows transfer rate settings.
6	ICCHB8	0	R/W	IIC Clock Control High Bit 8 Sets the high-level period of SCL when the period setting for the module in {ICIC[6], ICCH} is H'100 to H'1FF. Table 45.5 shows transfer rate settings.
5	TDMAE	0	R/W	Transmit Data DMA Transfer Request Enable When DTEE is 1, this bit specifies whether data transmit interrupt in transmission mode (TRS = 1) is used as an interrupt to the CPU or a DMA transfer request. When DMA is used for automatic transmission*, setup of this bit is unnecessary. 0: Uses TDMAE as an interrupt to the CPU. 1: Uses TDMAE as a DMA transfer request to DMAC.
4	RDMAE	0	R/W	Receive Data DMA Transfer Request Enable When the DTEE bit is 1, this bit specifies whether data receive interrupt in receive mode (TRS = 0) is used as an interrupt to the CPU or a DMA transfer request. When DMA is used for automatic transmission*, setup of this bit is unnecessary. 0: Uses RDMAE as an interrupt to the CPU. 1: Uses RDMAE as a DMA transfer request to DMAC.
3	ALE	0	R/W	Arbitration Lost Interrupt Enable and Function Enable Enables or disables arbitration lost interrupt request. An arbitration lost interrupt is generated if a loss of arbitration occurs when this bit is 1. At this time, the AL bit in ICSR is set to 1. Do not clear this bit to 0 with the AL bit set to 1. 0: Disables an arbitration lost Interrupt. 1: Enables an arbitration lost interrupt.

Bit	Bit Name	Initial Value	R/W	Description
2	TACKE	0	R/W	<p>Non-acknowledge Detection Interrupt Enable and Function Enable</p> <p>Enables or disables a non-acknowledge detection interrupt request.</p> <p>A non-acknowledge interrupt is generated if non-acknowledge is received when this bit is 1. At this time, the TACK bit in ICSR is set to 1. Do not clear this bit to 0 with the TACK bit set to 1.</p> <p>0: Disables non-acknowledge detection Interrupt.</p> <p>1: Enables non-acknowledge detection interrupt.</p>
1	WAITE	0	R/W	<p>Wait Interrupt Enable and Function Enable</p> <p>Enables or disables a wait interrupt request.</p> <p>When WAITE is 1, a wait state in which SCL is driven to the low level follows the transmission of data other than the acknowledge bit.</p> <p>At this time, a WAIT interrupt is generated and the WAIT bit in ICSR is set to 1. Do not clear this bit to 0 with the WAIT bit in ICSR set to 1.</p> <p>0: Disables an interrupt.</p> <p>1: A wait interrupt is generated.</p>
0	DTEE	0	R/W	<p>Data Transmit Enable Interrupt</p> <p>Enables or disables a data transmit enable interrupt request.</p> <p>An interrupt request is issued if the DTE bit in ICSR is set to 1 when this bit is 1.</p> <p>0: Disables an interrupt.</p> <p>1: A data transmit enable interrupt is generated.</p>

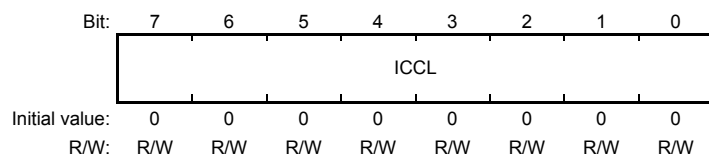
Note: \* Automatic transmission for PMIC (DVFS) is not available.

### 45.3.5 IIC Clock Control Register Low (ICCL)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

ICCL is an 8-bit readable/writable register that specifies the low-level period of SCL.

ICCL is initialized to H'00 by a reset.



Note: No SCL clock is generated when {ICIC[7], ICCL} = H'000 to H'0FF or H'1FF.

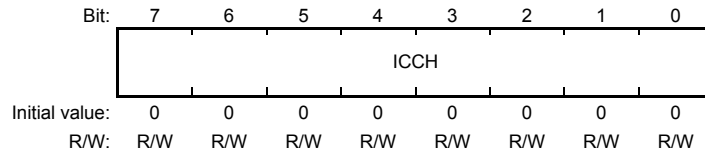


### 45.3.6 IIC Clock Control Register High (ICCH)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

ICCH is an 8-bit readable/writable register that specifies the high-level period of SCL.

ICCH is initialized to H'00 by a reset.

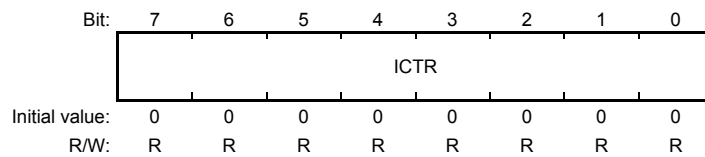


Note: No SCL clock is generated when {ICIC[7], ICCL} = H'000 to H'0FF or H'1FF.

### 45.3.7 IIC Transmit Register (ICTR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

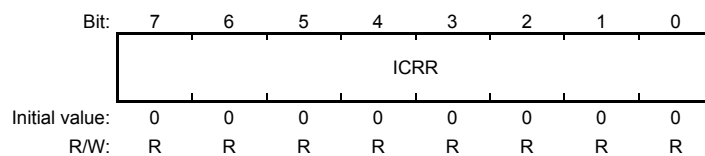
ICTR is an 8-bit register that indicates transmit data of the IIC bus interface.



### 45.3.8 IIC Receive Register (ICRR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

ICRR is an 8-bit register that monitors receive data of the IIC bus interface.



### 45.3.9 IIC Transmit Monitor Register (ICTA)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

ICTA is an 8-bit register that indicates the repeated START condition.

Bit:	7	6	5	4	3	2	1	0
	—	—	—	—	Rsetup	—	—	—
Initial value:	—	—	—	—	0	—	—	—
R/W:	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
7 to 4	—	—	R	Reserved Writing to these bits is prohibited.
3	Rsetup	0	R	Repeated START Condition Setup Specifies whether retransmission condition have been specified or not. This bit is 1 from the repeated START condition being specified (by writing H'94 to ICCR) until the repeated START condition is actually generated.
2 to 0	—	—	R	Reserved Writing to these bits is prohibited.

**45.3.10 IIC Transmit Buffer Monitor Register (ICTB)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

ICTB is an 8-bit register that indicates the communication status of the IIC bus interface.

Bit:	7	6	5	4	3	2	1	0
	—	—	—	—	Sbflg	Tbflg	Rbflg	Drflg
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R

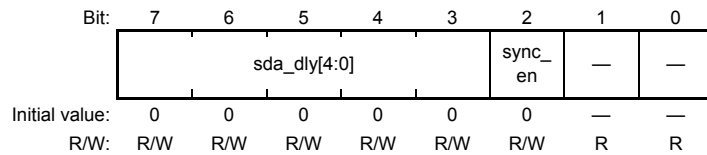
Bit	Bit Name	Initial Value	R/W	Description
7 to 4	—	—	R	Reserved
3	Sbflg	0	R	ICSF Buffer Flag 0: ICSF has no transmit data. 1: ICSF has transmit data.
2	Tbflg	0	R	ICTR Buffer Flag 0: ICTR has no transmit data. 1: ICTR has transmit data.
1	Rbflg	0	R	ICRR Buffer Flag 0: ICRR has no transmit data. 1: ICRR has transmit data.
0	Drflg	0	R	ICDR Buffer Flag 0: ICDR has no transmit data. 1: ICDR has transmit data.

**45.3.11 IIC Transmit Control Register (ICTC)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

ICTC is an 8-bit register that specifies SDA delay adjustment and SCL synchronization.

ICTC is initialized to H'00 by a reset.



Bit	Bit Name	Initial Value	R/W	Description
7 to 3	sda_dly[4:0]	00000	R/W	<p>SDA Data Delay Select</p> <p>These bits set the SDA data output delay from the SCL.</p> <p>00000: No SDA data delay (recommended)</p> <p>00001: SDA data is delayed by one cycle of the module clock.</p> <p>00010: SDA data is delayed by two cycles of the module clock.</p> <p>...</p> <p>11110: SDA data is delayed by 30 cycles of the module clock.</p> <p>11111: SDA data is delayed by 31 cycles of the module clock.</p> <p>When SDA data output is delayed, the AC specifications of the IIC bus may not be satisfied. Therefore, setting these bits to 00000 is recommended.</p>
2	sync_en	0	R/W	<p>SCL Synchronization Select</p> <p>Specifies whether the SCL line synchronizing function is activated or not.</p> <p>0: SCL line synchronization is activated (recommended).</p> <p>1: SCL line synchronization is not activated.</p> <p>When this bit is set to 1, the AC specifications of the IIC bus may not be satisfied. Therefore, setting this bit to 0 is recommended.</p>
1, 0	—	—	R	<p>Reserved</p> <p>The write value should always be 0.</p>

### 45.3.12 IIC Transmit Control Status Monitor Register (ICTD)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

ICTD is an 8-bit register that indicates the communication status of the IIC bus interface.

Bit:	7	6	5	4	3	2	1	0
	—	—	—	IIC_req 0	—	—	—	IIC_ack 0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
7 to 5	—	All 0	R	Reserved
4	IIC_req0	0	R	IIC Communication Request 0 0: No communication request 1: Under communication request
3 to 1	—	All 0	R	Reserved
0	IIC_ack0	0	R	IIC Communication Status 0 0: No communication 1: Under Communication

### 45.3.13 IIC Shift Register (ICSF)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

ICSF is an 8-bit register that indicates data being transmitted by the IIC bus interface.

Bit:	7	6	5	4	3	2	1	0
	ICSF							
Initial value:	1	1	1	1	1	1	1	1
R/W:	R	R	R	R	R	R	R	R

### 45.3.14 IIC Option Enabling Register (ICVCON)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√*

Note: \* Some restrictions apply.

ICVCON is an 8-bit register that enables or disable the optional feature of the IIC module.

Do not change the value of this register during IIC communication.

Bit:	7	6	5	4	3	2	1	0
	—	—	Req_Hold	D16EN	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
7, 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5	Req_Hold	0	R/W	Reserved This bit is always read as 0. The write value should always be 0.
4	D16EN	0	R/W	IIC Terminal Using 16-case Select Mode Enable 0: DVFS 16-case select is not used. 1: DVFS 16-case select is used. [RZ/G1H, M and N] Setting prohibited [RZ/G1E] Set D16EN to 1 for automatic transmission. Note that the RZ/G series products do not support the DVFS function.
3 to 0	—	All 0	R	Reserved When writing, always write 0.

### 45.3.15 IIC Automatic Transmission\* Interrupt Mask Register (ICIMSK)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

ICIMSK is an 8-bit register that enables or disables the interrupt request output of automatic transmission\*.

An interrupt is output to AL interrupt event code. The generated interrupt can be checked by ICINT.

Note: \* Automatic transmission for PMIC control (DVFS) is not available.

Bit:	7	6	5	4	3	2	1	0
	AEND M	TMC2M	TMC1M	TMOUT M	ALM	TACKM	—	—
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7	AENDM	0	R/W	Automatic Transmission* End Interrupt Mask 0: Interrupt is not output to INTC-SYS at the time of the end of automatic transmission*. 1: Interrupt is output to INTC-SYS at the time of the end of automatic transmission*.
6	TMC2M	0	R/W	Timer Count 2 End Interrupt Mask 0: Interrupt is not output to INTC-SYS at the time of the end of timer count 2. 1: Interrupt is output to INTC-SYS at the time of the end of timer count 2.
5	TMC1M	0	R/W	Timer Count 1 End Interrupt Mask 0: Interrupt is not output to INTC-SYS at the time of the end of timer count 1. 1: Interrupt is output to INTC-SYS at the time of the end of timer count 1.
4	TMOUTM	0	R/W	Timeout Error Interrupt Mask 0: Interrupt is not output to INTC-SYS at the time of a timeout error. 1: Interrupt is output to INTC-SYS at the time of a timeout error.
3	ALM	0	R/W	AL Interrupt Mask 0: Interrupt is not output to INTC-SYS at the time of the automatic transmission* AL. 1: Interrupt is output to INTC-SYS at the time of the automatic transmission* AL.
2	TACKM	0	R/W	TACK Interrupt Mask 0: Interrupt is not output to INTC-SYS at the time of the automatic transmission* TACK. 1: Interrupt is output to INTC-SYS at the time of the automatic transmission* TACK.
1, 0	—	All 0	R/W	Reserved These bits are always read as 0. The write value should always be 0.

Note: \* Automatic transmission for PMIC control (DVFS) is not available.

### 45.3.16 IIC Automatic Transmission\* Interruption Flag Register (ICINT)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

ICINT is an 8-bit register that indicates the interrupt state during automatic transmission\*.

The interrupt bit can be cleared by writing 1 to ICSTART[7] or clearing ICCR[7] to 0 at the start of automatic operation.

Note: \* Automatic transmission for PMIC control (DVFS) is not available.

Bit:	7	6	5	4	3	2	1	0
	AEND	TMC2	TMC1	TMOUT	AAL	ATACK	AWAIT	ADTE
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
7	AEND	0	R	Automatic Transmission* End Flag 0: Under automatic transmission* 1: End of automatic transmission*
6	TMC2	0	R	Timer Count 2 End Flag 0: Timer count 2 is not ended. 1: End of timer count 2
5	TMC1	0	R	Timer Count 1 End Flag 0: Timer count 1 is not ended. 1: End of timer count 1
4	TMOUT	0	R	Timeout Error Flag 0: No timeout error 1: Timeout error is detected.
3	AAL	0	R	Automatic Transmission* AL Flag 0: No AL 1: AL is detected.
2	ATACK	0	R	Automatic Transmission* TACK Flag 0: No TACK 1: TACK is detected.
1	AWAIT	0	R	Automatic Transmission* WAIT Flag 0: No WAIT 1: WAIT is detected.
0	ADTE	0	R	Automatic Transmission* DTE Flag 0: No DTE 1: DTE is detected.

Note: \* Automatic transmission for PMIC control (DVFS) is not available.



### 45.3.17 IIC Automatic Transmission\* Processing Enabling Register (ICACE)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

ICACE is an 8-bit register that specifies the usage of each function during automatic transmission\*.

Note: \* Automatic transmission for PMIC control (DVFS) is not available.

Bit:	7	6	5	4	3	2	1	0
	AENDE	TMC2E	TMC1E	TMOU E	ALE	TACKE	WAITE	—
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7	AENDE	0	R/W	Automatic Transmission* End Detection Enable 0: End of automatic transmission is not detected. 1: Detects the end of automatic transmission and outputs it to ICINT.
6	TMC2E	0	R/W	Timer Count 1 Enable, Timer Count 2 Enable
5	TMC1E	0	R/W	Specify whether wait by TMC1 or TMC2 timer is inserted before assertion of an automatic transmission* interrupt and a timeout error detection interrupt. Refer to Figure 45.3 for the wait timing of TMC1 and TMC2. ICACE[6:5] = 00: TMC1 and TMC2 are not used. ICACE[6:5] = 01: Interrupt is asserted after counting by TMC1 is finished. ICACE[6:5] = 11: Interrupt is asserted after counting by TMC1 and TMC2 is finished. ICACE[6:5] = 10: Setting prohibited
4	TMOUTE	0	R/W	Timeout Error Enable When SCL/SDA is driven to low even after the STOP condition is generated and counting by TMC1 and TMC2 is finished, a timeout error is detected. 0: Timeout error is not detected. 1: Timeout error is detected and recorded in ICINT.
3	ALE	0	R/W	Automatic Transmission* AL Error-Handling Enable Specifies whether handling for AL errors detected during automatic transmission is performed or not. 0: No automatic AL error handling (AL is not detected) 1: Automatic AL error handling is performed (to release the SDA bus, continue output of SCL until the time corresponding to 1 byte + ACK, and perform retry or stop processing).
2	TACKE	0	R/W	Automatic Transmission* ACK Error-Handling Enable Specifies whether handling for ACK error is performed or not (when error handling is selected, either retry or stop processing is performed). 0: No automatic ACK error handling 1: Automatic ACK error handling is performed (retry or stop processing is performed).

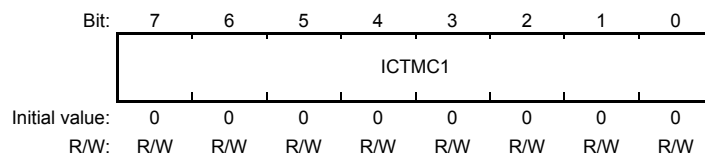
Bit	Bit Name	Initial Value	R/W	Description
1	WAITE	0	R/W	WAIT Processing Enable Specifies whether wait processing is inserted during automatic transmission*. 0: No automatic WAIT processing. 1: Automatic WAIT processing is performed (waiting for the period specified by the ICTMCW register).
0	—	0	R/W	Reserved The write value should always be 0.

Note: \* Automatic transmission for PMIC control (DVFS) is not available.

### 45.3.18 IIC Automatic Transmission\* Timer Control Register 1 (ICTMC1)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

ICTMC1 is an 8-bit register that specifies the delay time for the timing of detection of automatic transmission\* being completed and timeout errors.



The delay time is specified by ICTMC1 by following formula.

$$\text{Delay time} = (\text{ICTMC1})_{10} \times 200 \times t_{\text{Module clock}}$$

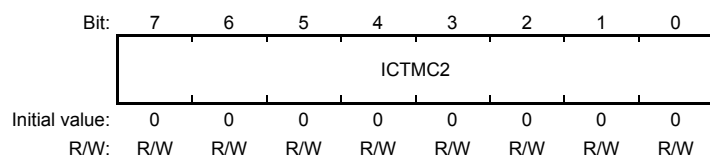
(When the frequency of the module clock is 104 MHz, the delay time can be specified within the range from 0 μs up to 490 μs in 2-μs increments.)

Note: \* Automatic transmission for PMIC control (DVFS) is not available.

### 45.3.19 IIC Automatic Transmission\* Timer Control Register 2 (ICTMC2)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

ICTMC2 is an 8-bit register that specifies the delay time for the timing of detection of automatic transmission\* being completed and timeout errors.



The delay time is specified by ICTMC2 by the following formula.

$$\text{Delay time} = (\text{ICTMC2}) \times 10 \times 200 \times t_{\text{Module clock}}$$

(When the frequency of the module clock is 104 MHz, the delay time can be specified within the range from 0 μs up to 490 μs in 2-μs increments.)

Note: \* Automatic transmission for PMIC control (DVFS) is not available.

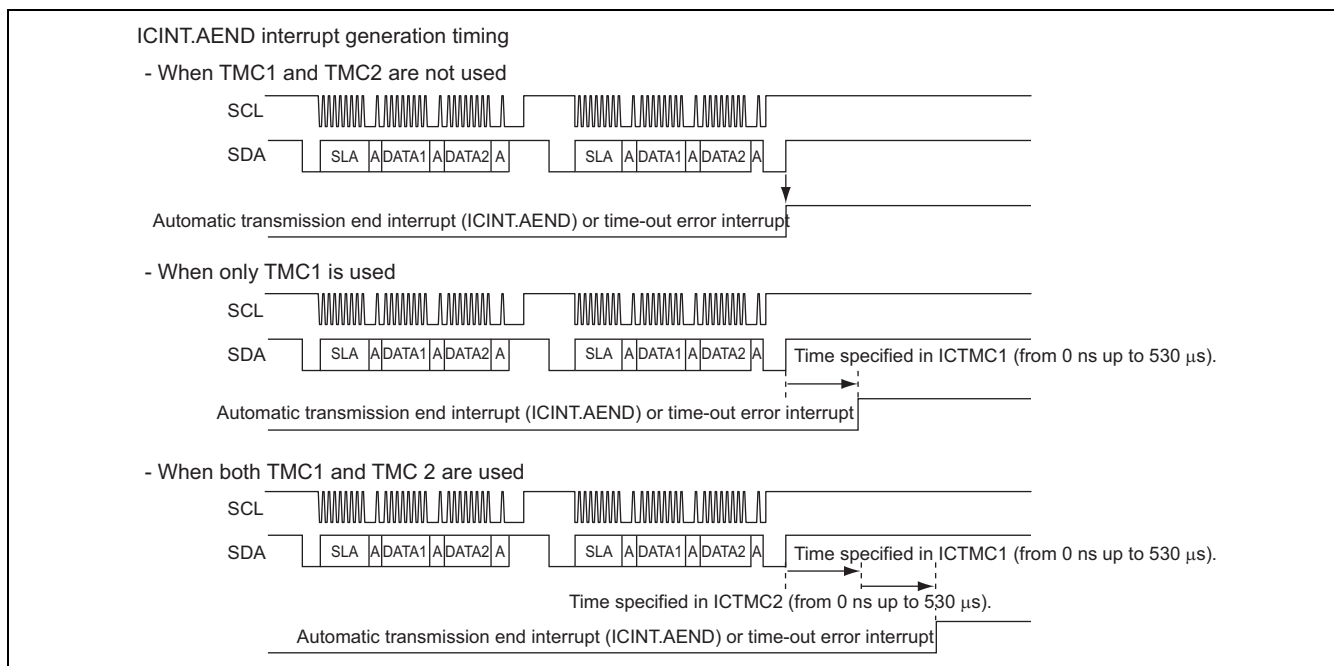
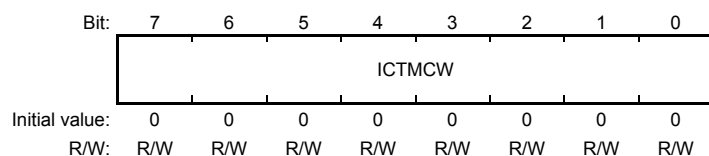


Figure 45.3 Wait Timing Chart of TMC1 and TMC2

### 45.3.20 IIC Automatic Transmission\* Wait Control Register (ICTMCW)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

ICTMCW is an 8-bit register that specifies the wait time during automatic transmission\*. When ICACE[1].WAITE is set to 1 for activating the wait processing function, set a value other than H'00 to this register.



The wait time is specified by ICTMCW by following formula.

$$\text{Delay time} = (\text{ICTMCW})_{10} \times 20 \times t_{\text{Module clock by ICTMCW}}$$

(When the frequency of the module clock is 104 MHz, the delay time can be specified within the range from 0 μs up to 49 μs in 2-μs increments.)

Although a wait time can be specified by this register, the period of waiting may be different from the specified value because a transition of the actual SCL bus may be delayed by a clock cycle. Also, in the case of automatic transmission\*, 1 cycle of waiting is always inserted automatically before the acknowledge cycle.

Note: \* Automatic transmission for PMIC control (DVFS) is not available.

### 45.3.21 IIC Automatic Transmission\* Transmit Start Register (ICSTART)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

ICSTART is an 8-bit register that specifies start, reset, and abort of automatic transmission\*.

Note: \* Automatic transmission for PMIC control (DVFS) is not available.

Bit:	7	6	5	4	3	2	1	0
	Auto Start	AutoTransReset	Auto Stop	—	—	—	ATDMA	ARDMA
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7	AutoStart	0	R/W	Automatic Transmission* Start Automatic transmission* starts by writing 1 to this bit. Do not clear this bit to 0 during automatic transmission*.
6	AutoTransReset	0	R/W	Automatic Transmission* Reset The internal state of automatic transmission* is reset by writing 1 to this bit. After reset, write 0 to this bit. Writing 1 to this bit does not initialize automatic transmission-related registers. For register initialization, use reset function by writing 0 to ICCR[7].ICE.
5	AutoStop	0	R/W	Automatic Transmission* Stop By writing 1 to this bit, the STOP condition is generated at the boundary of a 1byte + ACK-cycle unit and automatic transmission* stops. Writing 1 to this bit may result in stopping transmission such that the transfer format is not as expected. 0: Normal operation 1: STOP condition is generated and automatic transmission* stops.
4 to 2	—	All 0	R/W	Reserved The write value should always be 0.
1	ATDMA	0	R/W	Automatic Transmission* DMA Enable 0: DMA is not used for data transmission by automatic transmission*. 1: DMA is used for all data transmission by automatic transmission*.
0	ARDMA	0	R/W	Automatic Reception DMA Enable 0: DMA is not used for data reception by automatic transmission*. 1: DMA is used for all data reception by automatic transmission*.

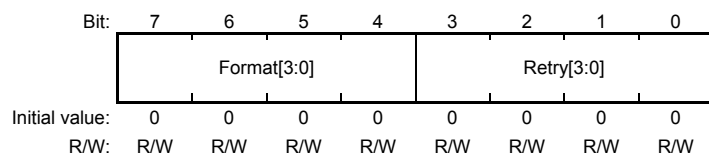
Note: \* Automatic transmission for PMIC control (DVFS) is not available.

### 45.3.22 IIC Automatic Transmission\* Transmit Control Register (ICATFR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

ICATFR is an 8-bit register that specifies an automatic transmission\* format and the number of retry processing.

Note: \* Automatic transmission for PMIC control (DVFS) is not available.



Bit	Bit Name	Initial Value	R/W	Description
7 to 4	Format[3:0]	0000	R/W	<p>IIC Automatic Transmission*<sup>1</sup> Format Selection</p> <p>Specify the format of automatic transmission*<sup>1</sup>. Refer to Figure 45.5 for a communication format.</p> <p>S = START condition, Sr = Repeated START condition, P = STOP condition</p> <p>0000: S → Transmission 1 → P</p> <p>0001: S → Transmission 1 → Reception 1 → P</p> <p>0010: S → Transmission 1 → Sr → Transmission 2 → P</p> <p>0011: S → Transmission 1 → Sr → Transmission 2 → Receive 1 → P</p> <p>0100: S → Transmission 1 → Reception 1 → Sr → Transmission 2 → P</p> <p>0101: S → Transmission 1 → Reception 1 → Sr → Transmission 2 → Reception 2 → P</p> <p>Others: Setting prohibited</p>
3 to 0	Retry[3:0]	0000	R/W	<p>Retry Number for Automatic Transmission*<sup>1:2</sup></p> <p>Specify the maximum number of retry when an AL error or non-acknowledge error occurs. When either of errors has reached the specified number, AL or TACK error is reported.</p> <p>H'0: No retry</p> <p>H'1: Retry once.</p> <p>H'2: Retry up to twice.</p> <p>-</p> <p>H'E: Retry up to 14 times.</p> <p>H'F: Setting prohibited.</p>

- Notes: 1. Automatic transmission for PMIC control (DVFS) is not available.  
 2. Retry processing cannot be performed when using DMA transfer.

### 45.3.23 IIC Automatic Transmission\* Transmit Time Register 1 (ICATSET1)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

ICATSET1 is an 8-bit register that specifies the number of data of the transmission 1 in the format specified by ICATFR[7:4].

The maximum value which can be specified in this register is 10 when using the ICATD00 to ICATD09 registers, and 256 when using a DMA transfer.

A slave address is also contained in the transmission data.

Specify the values as follows when ICATD00 to ICATD09 are in use.

1-byte transmission      ICATSET1[7:0] = H'00

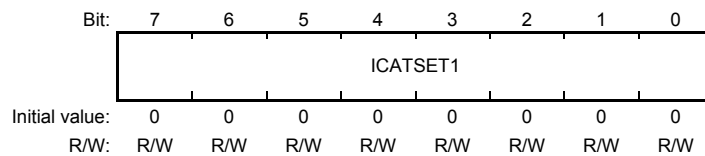
2-byte transmission      ICATSET1[7:0] = H'01

10-byte transmission      ICATSET1[7:0] = H'09

Specify the size of transmission for a DMA transfer.

256-byte transmission      ICATSET1[7:0] = H'FF (maximum)

Note: \* Automatic transmission for PMIC control (DVFS) is not available.



### 45.3.24 IIC Automatic Transmission\* Transmit Time Register 2 (ICATSET2)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

ICATSET2 is an 8-bit register that specifies the number of data of the transmission 2 in the format specified by ICATFR[7:4].

The maximum number which can be specified in this register is 10 when using the ICATD10 to ICATD19 registers, and 256 when using a DMA transfer.

A slave address is also contained in the transmission data.

Specify the values as follows when ICATD10 to ICATD19 are in use.

1-byte transmission      ICATSET2[7:0] = H'00

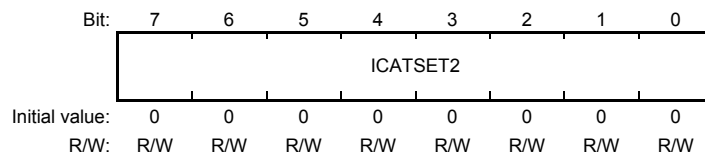
2-byte transmission      ICATSET2[7:0] = H'01

10-byte transmission      ICATSET2[7:0] = H'09

Specify the size of transmission for a DMA transfer.

256-byte transmission      ICATSET2[7:0] = H'FF (maximum)

Note: \* Automatic transmission for PMIC control (DVFS) is not available.





**45.3.25 IIC Automatic Transmission\* Reception Time Register 1 (ICARSET1)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

ICARSET1 is an 8-bit register that specifies the number of data of the reception 1 in the format specified by ICATFR[7:4].

The maximum number which can be specified in this register is 10 when using the ICARD00 to ICARD09 registers, and 256 when using a DMA transfer.

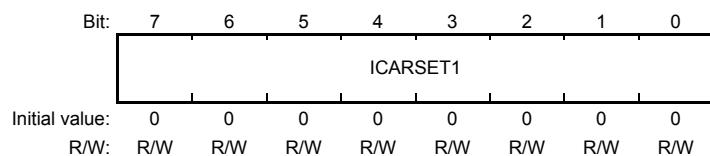
Specify the values as follows when ICARD00 to ICARD09 are in use.

- 1-byte transmission      ICARSET1[7:0] = H'00
- 2-byte transmission      ICARSET1[7:0] = H'01
- 10-byte transmission      ICARSET1[7:0] = H'09

Specify the size of transmission for a DMA transfer.

- 256-byte transmission      ICARSET1[7:0] = H'FF (maximum)

Note: \* Automatic transmission for PMIC control (DVFS) is not available.



### 45.3.26 IIC Automatic Transmission\* Receipt Time Register 2 (ICARSET2)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

ICARSET2 is an 8-bit register that specifies the number of data of the reception 1 in the format specified by ICATFR[7:4].

The maximum number which can be specified in this register is 10 when using the ICARD10 to ICARD19 registers, and 256 when using a DMA transfer.

Specify the values as follows when ICARD10 to ICARD19 are in use.

1-byte transmission      ICARSET2[7:0] = H'00

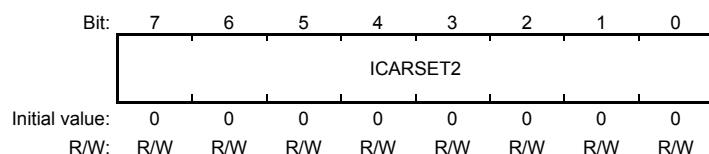
2-byte transmission      ICARSET2[7:0] = H'01

10-byte transmission      ICARSET2[7:0] = H'09

Specify the size of transmission for a DMA transfer.

256-byte transmission      ICARSET2[7:0] = H'FF (maximum)

Note: \* Automatic transmission for PMIC control (DVFS) is not available.

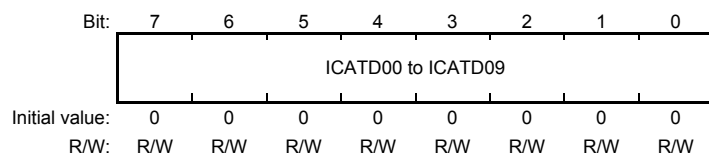


### 45.3.27 IIC Automatic Transmission\* Transmit Data 00 to 09 (ICATD00 to ICATD09)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

ICATD00 to ICATD09 are 8-bit registers that are used to store the transmit data of transmission 1.

Note: \* Automatic transmission for PMIC control (DVFS) is not available.

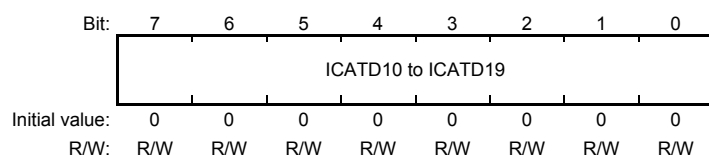


**45.3.28 IIC Automatic Transmission\* Transmit Data 10 to 19 (ICATD10 to ICATD19)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

ICATD10 to ICATD19 are 8-bit registers that are used to store the transmit data of transmission 2.

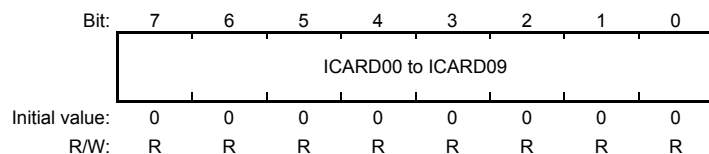
Note: \* Automatic transmission for PMIC control (DVFS) is not available.

**45.3.29 IIC Automatic Transmission\* Receipt Data 00 to 09 (ICARD00 to ICARD09)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

ICARD00 to ICARD09 are 8-bit registers that are used to store the received data of reception 1.

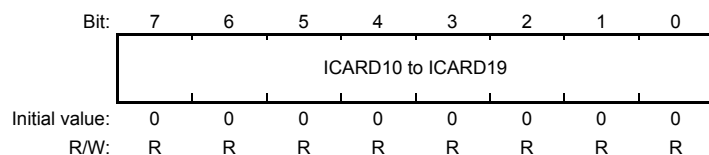
Note: \* Automatic transmission for PMIC control (DVFS) is not available.

**45.3.30 IIC Automatic Transmission\* Receipt Data 10 to 19 (ICARD10 to ICARD19)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

ICARD10 to ICARD19 are 8-bit registers that are used to store the received data of reception 2.

Note: \* Automatic transmission for PMIC control (DVFS) is not available.



**45.3.31 Transfer Rate**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

The IIC transfer rate can be specified by the settings in ICCL, ICCH, ICIC[7], and ICIC[6] and is based on the module clock.

Table 45.5 lists transfer rate settings, and Figure 45.5 shows SCL waveforms.

**Table 45.5 Transfer Rate Maximum Settings Example**

	Module clock	ICIC[7] + ICCL	ICIC[6] + ICCH	Transfer Rate*
Standard	7.5 MHz	H'14	H'0E	101.35 kHz
	10 MHz	H'1B	H'14	100.00 kHz
	13 MHz	H'24	H'1A	100.00 kHz
	15 MHz	H'29	H'1F	100.00 kHz
	32.5 MHz	H'5A	H'46	99.69 kHz
	52 MHz	H'90	H'71	100.00 kHz
	78 MHz	H'D8	H'AB	100.00 kHz
	104 MHz	H'120	H'E5	100.00 kHz
	130 MHz	H'169	H'11E	100.00 kHz
Fast-mode	7.5 MHz	H'05	H'02	375.00 kHz
	10 MHz	H'06	H'03	416.67 kHz
	13 MHz	H'09	H'05	382.35 kHz
	15 Hz	H'0A	H'06	394.74 kHz
	32.5Hz	H'16	H'10	396.34 kHz
	52 MHz	H'24	H'1A	400.00 kHz
	78 MHz	H'36	H'29	397.96 kHz
	104 MHz	H'48	H'37	400.00 kHz
	130 MHz	H'5A	H'46	398.77 kHz

Note: \* The transfer rates in above settings are theoretical values. The actual transfer rates are generally smaller than those theoretical values due to the pull-up resistor (Rp) and the capacitance (Cp). However, there is no harm in communication because the actual transfer rates satisfy the I2C bus specifications. (Smaller ICCL and ICCH can increase the actual transfer rates. In this case, though, set ICCL and ICCH to ensure that t<sub>LOW</sub> and t<sub>HIGH</sub> are within the specifications.)

**Calculation example of ICCL and ICCH:**

- Conditions

Module clock: 104 MHz

IIC transfer rate: 100 kHz

L/H sample ratio in SCL: L/H = 5/4

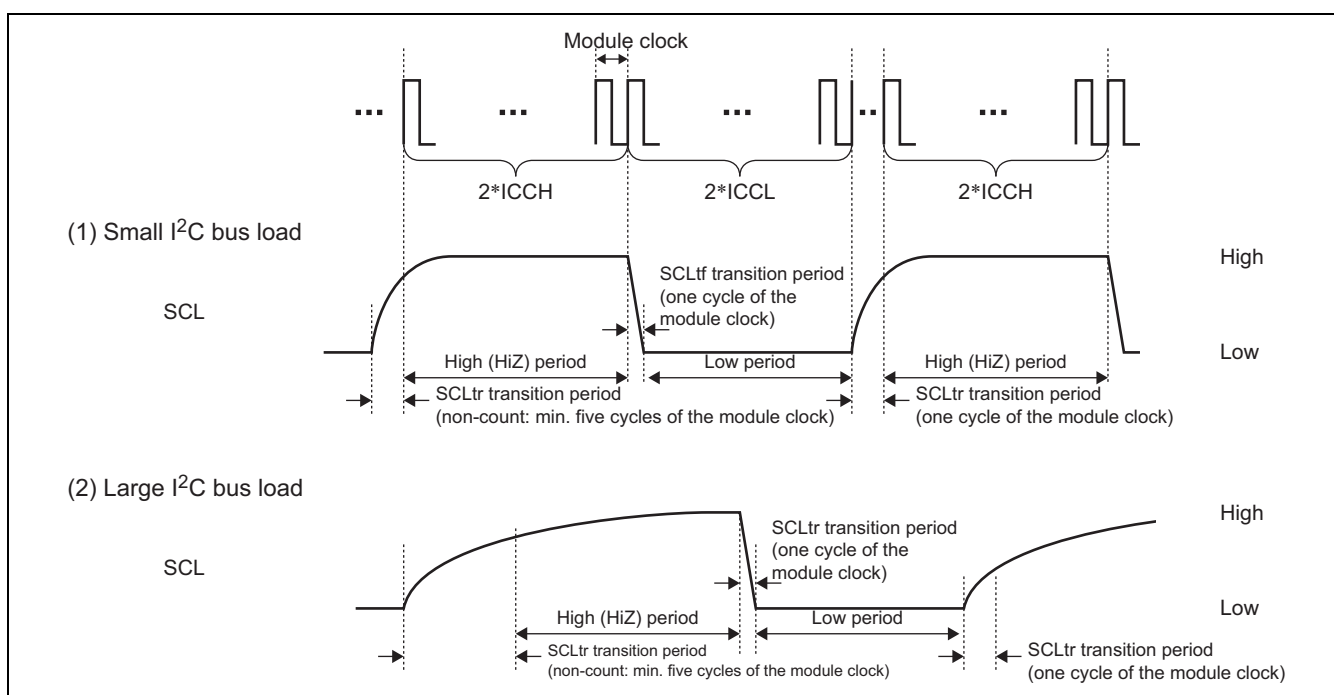
- Result

$$ICIC[7] + ICCL = ((Module\ clock / IIC\ transfer\ rate) \times (L / (L + H)) - 1) / 2$$

$$= (((104 \times 10^6) / (100 \times 10^3)) \times (5 / (5 + 4)) - 1) / 2 = 288 = H'120$$

$$ICIC[6] + ICCH = ((Module\ clock / IIC\ transfer\ rate) \times (H / (L + H)) - 5) / 2$$

$$= (((104 \times 10^6) / (100 \times 10^3)) \times (4 / (5 + 4)) - 5) / 2 = 229 = H'0E5$$



**Figure 45.4 SCL Waveforms**

## 45.4 Operation

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

### 45.4.1 I2C Bus Data Format

The I2C bus is based on protocol, which contains the slave address, data, and an acknowledge bit. These are shown in Figure 45.5. The first frame following a START condition always consists of 8 bits.

The symbols used in Figure 45.5 are explained in Table 45.6.

**Table 45.6 I2C Bus Data Format Symbols**

Symbol	Description
S	START condition. The master device drives SDA from high to low while SCL is high.
Sr	Repeated START condition. The master device drives SDA from high to low while SCL is high.
SLA	Slave address. The master device selects a slave device.
R/W	Indicates the direction of data transfer: from the slave device to the master device when R/W is 1, or from the master device to the slave device when R/W is 0.
A	Acknowledge. The receiving device (the slave device in master transmit mode, or the master device in master receive mode) drives SDA low to acknowledge a transfer.
DATA	Transmitted or received data. The bit length is 8 bits.
P	STOP condition. The master device drives SDA from low to high while SCL is high.

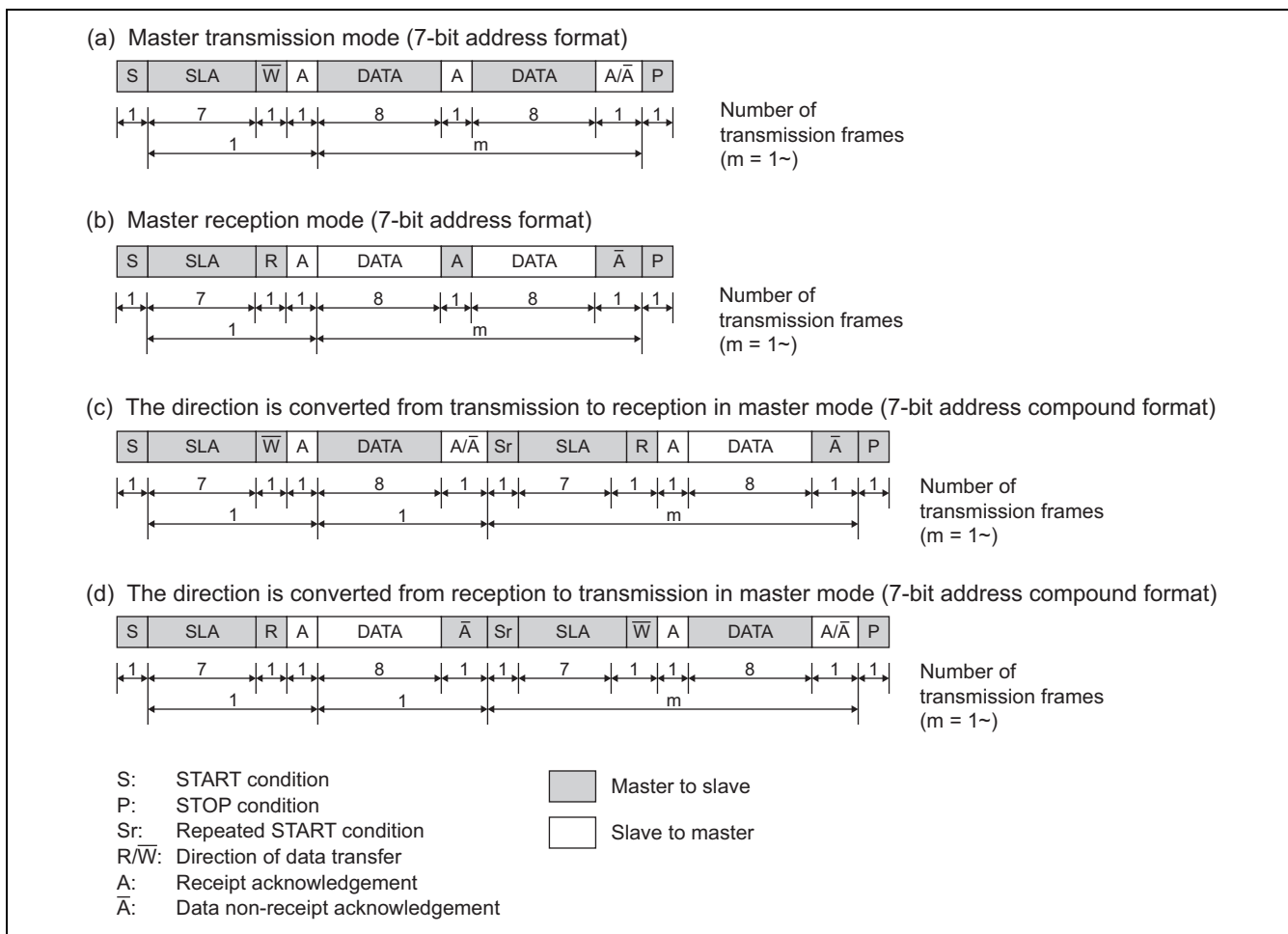


Figure 45.5 I2C Bus Data Formats (7-Bit Address Format)

#### 45.4.2 Master Transmit Operation (Using WAIT Function)

In master transmit mode, the master device outputs the transmission clock and transmission data, and receives the acknowledge signal after receiving data. The transmission procedure and operations are described below.

1. Set ICCR.ICE to activate the IIC module.
2. Set ICCL, ICCH, and ICIC[1:0], according to the operating mode.
3. Write H'94 to ICCR to issue the START condition. The DTE bit in ICSR is then set to 1.
4. Wait for a DTE interrupt or until ICSR.DTE becomes 1.
5. Clear ICIC.DTEE to disable a DTE interrupt when the ICSR.DTE bit becomes 1.  
And write transmission data (slave address and write bit) to ICDR. The ICSR.DTE bit is then automatically cleared.  
Data transmission starts after data is sent to the internal transmit buffer.
6. Wait for a WAIT interrupt or until ICSR.WAIT becomes 1.
7. If more transmission data remains, write transmission data (ex. register address or data) to ICDR. And clear ICSR.WAIT to exit from the WAIT status. After exiting from the WAIT state, go back to step 6.
8. If no more transmission data remains, write H'90 to ICCR to issue the STOP condition.  
And clear ICSR.WAIT to exit from the WAIT status. After exiting, go to step 9.
9. Wait until ICSR.BUSY is cleared to keep AC specification of  $t_{SU;STO}$ .
10. Clear ICCR.ICE to 0 to reset the IIC module.

Figure 45.6 shows the flowchart of the master transmission procedure.

By repeating steps 6 and 7, data can be transmitted consequently.

A non-acknowledge interrupt occurs if the received acknowledge signal is 1 (TACK = 1). If the received acknowledge bit is 1, it is recommended to STOP transmission after the STOP condition is generated. Refer to section 45.4.9, Non-Acknowledge Operation, for the stop method.

To change the transmission mode to the receive mode, write H'81 to ICCR, instead of generating the STOP condition in step 8.

To generate a repeated START condition, write H'94 to ICCR, instead of generating the STOP condition in step 8.



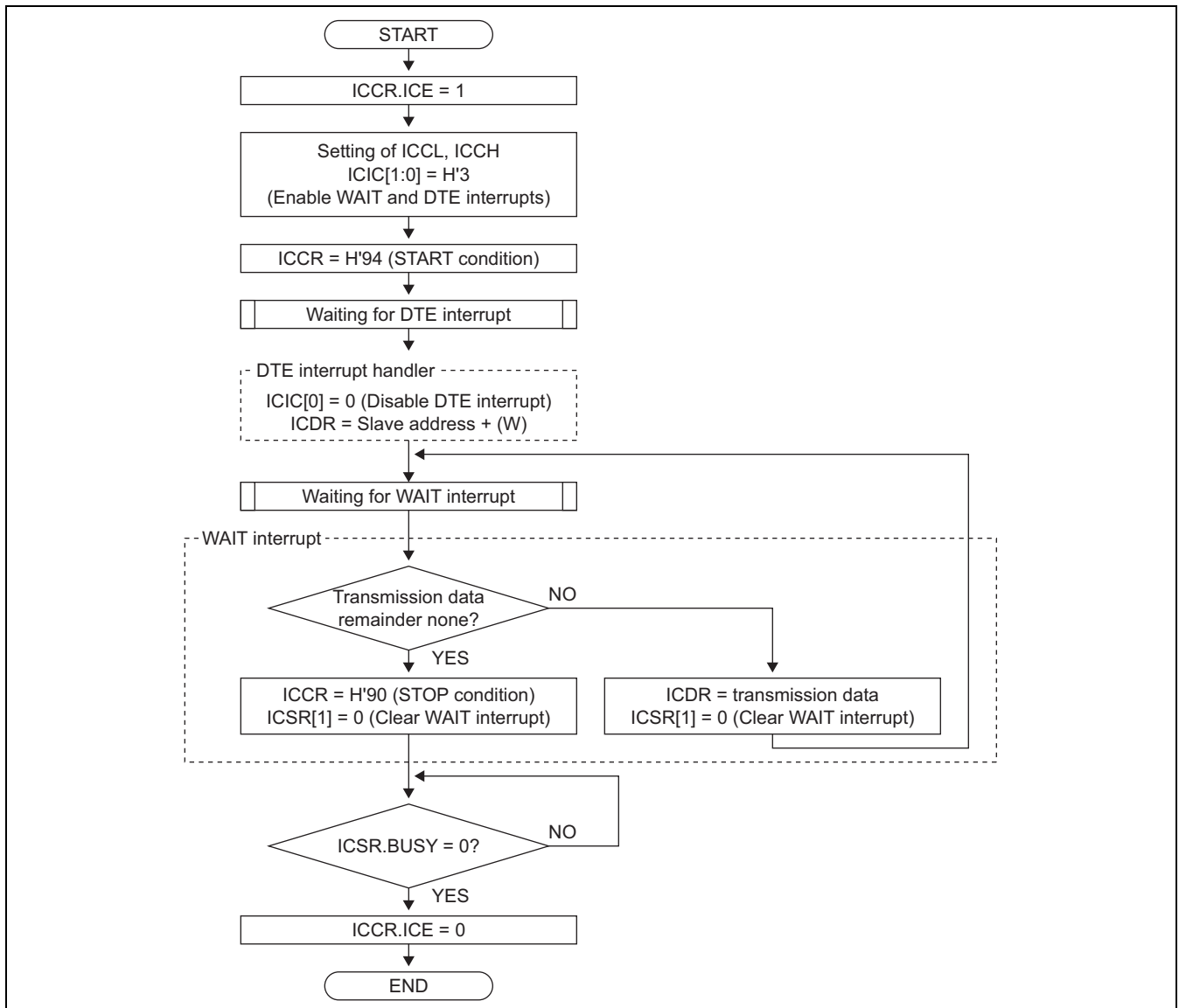


Figure 45.6 Example Flow for Transmission (a) Master Transmission Mode (Using WAIT Function)

### 45.4.3 Master Receive Operation (Using WAIT Function)

In master receive mode, the master device outputs the receive clock, and returns an acknowledge signal after the slave device transmits data. The reception procedure and operations in master receive mode are described below.

#### (1) When two or more bytes of data are received continuously

1. Set ICCR.ICE to activate the IIC module.
2. Set ICCL, ICCH, and ICIC [1:0], according to the operating mode.
3. Write H'94 to ICCR to issue the START condition. The DTE bit in ICSR is then set to 1.
4. Wait for a DTE interrupt or until ICSR.DTE becomes 1.
5. Clear ICIC.DTEE to disable a DTE interrupt when the ICSR.DTE bit becomes 1.  
And write the data (slave address and write bit) to ICDR. The ICSR.DTE bit is then automatically cleared. Data transmission starts when data is sent to the internal transmit buffer.
6. Wait for a WAIT interrupt or until CSR.WAIT becomes 1.
7. If more transmission data remains, write data (ex. register address or data) to ICDR. And clear ICSR.WAIT to exit from the WAIT status. After exiting from the WAIT status, go back to step 6.
8. If no more transmission data remains, write H'94 to ICCR to issue the repeated START condition. Set ICIC.DTEE to enable a DTE interrupt. And clear ICSR.WAIT to exit from the WAIT status. After exiting, go to step 9.
9. Wait for a DTE interrupt or until ICSR.DTE becomes 1.
10. Clear ICIC.DTEE to disable a DTE interrupt when the ICSR.DTE bit becomes 1. And write the data (ex. slave address and read bit) to ICDR. The ICSR.DTE bit is then automatically cleared.
11. Wait for a WAIT interrupt or until ICSR.WAIT becomes 1.
12. If more transmission data remains, write data (ex. register address or data) to ICDR. And clear ICSR.WAIT to exit from the WAIT status. After exiting from the WAIT status, go back to step 11.
13. If no more transmission data remains, write H'81 to ICCR to change the transmission mode to the receive mode. And clear ICSR.WAIT to exit from the WAIT status. After exiting, go to step 14.
14. Wait for a WAIT interrupt or until ICSR.WAIT becomes 1.
15. If two or more receive data remains,  
and if ICSR.DTE = 0, go to step 17,  
else if ICSR.DTE = 1 and three or more data remains, read data from ICDR then go to step 17.  
else if ICSR.DTE = 1 and two data remains, read data from ICDR and set ICCR = H'C0 for the STOP condition, then go to step 17.
16. If one receive data remains, set ICCR to H'C0 for the STOP condition then go to step 17.
17. Set ICIC.DTEE to enable a DTE interrupt. And clear ICSR.WAIT to exit from the WAIT status.
18. Wait for a DTE interrupt or until ICSR.DTE becomes 1.
19. If two or more receive data remains, read data from ICDR. The ICSR.DTE bit is then automatically cleared. After that, go back to step 14.
20. If one receive data remains, set ICIC.WAITE to disable a WAIT interrupt. And read data from ICDR. The ICSR.DTE bit is then automatically cleared.
21. Wait until ICSR.BUSY is cleared to keep AC specification of  $t_{SU;STO}$ .
22. Clear ICCR.ICE to 0 to reset the IIC module.

Figure 45.7 is the flow of this.

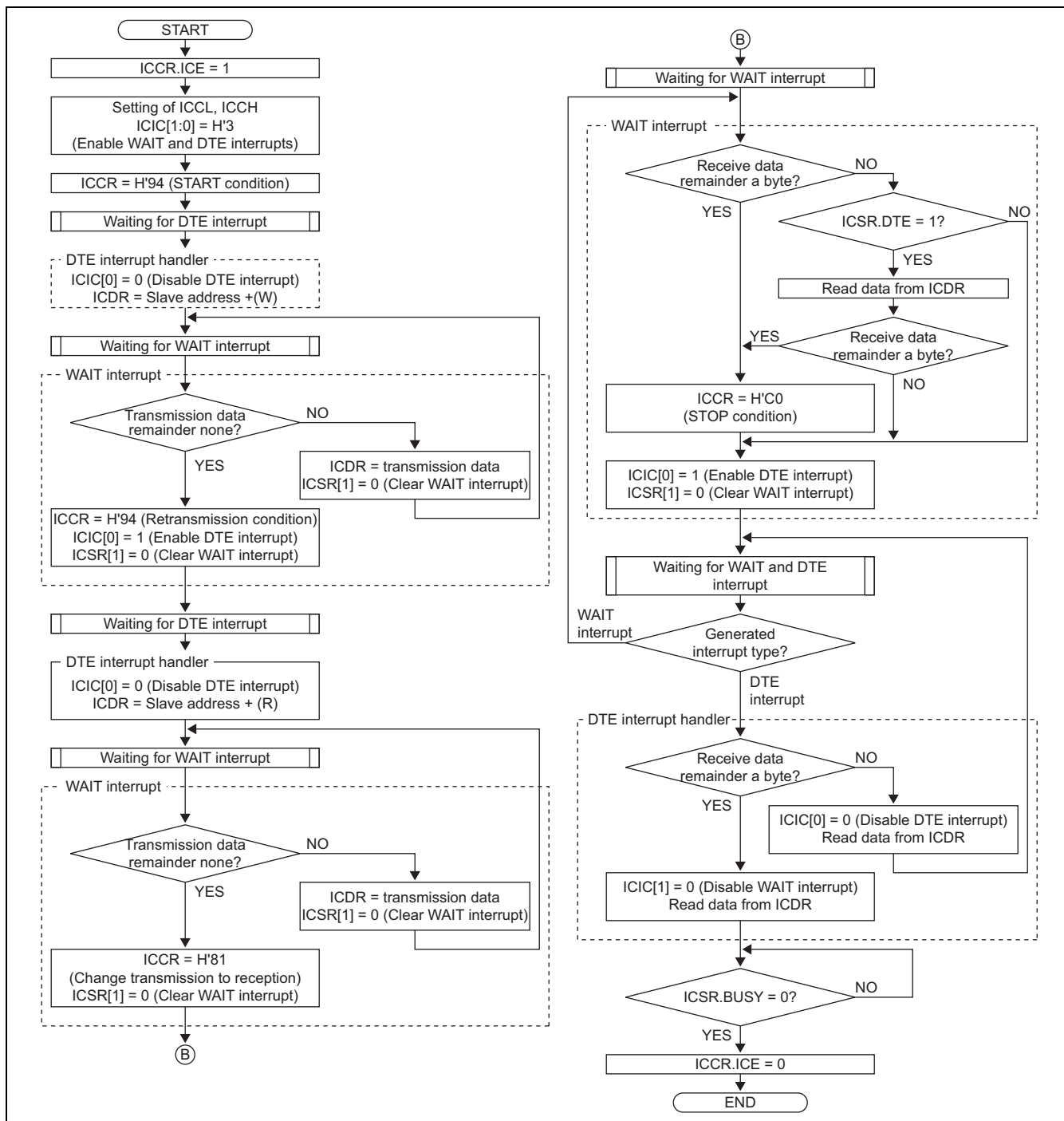


Figure 45.7 Example Flow for n-Byte Write/n-Byte Read (c) The Direction is Converted from Transmission to Reception (Using WAIT Function)

**(2) When only one byte of data is received**

When only one byte data is received, use a WAIT interrupt to issue the STOP or repeated START condition by writing to ICCR.

1. Set ICCR.ICE to activate the IIC module.
2. Set ICCL, ICCH, and ICIC[1:0], according to the operating mode.
3. Write H'94 to ICCR to issue the START condition. The DTE bit in ICSR is then set to 1.
4. Wait for a DTE interrupt or until ICSR.DTE becomes 1.
5. Clear ICIC.DTEE to disable a DTE interrupt when the ICSR.DTE becomes 1.  
And write data (ex. slave address and write bit) to ICDR. The ICSR.DTE bit is then automatically cleared. Data transmission starts when data is sent to the internal transmit buffer.
6. Wait for a WAIT interrupt or until ICSR.WAIT becomes 1.
7. Write H'81 to ICCR to issue the repeated START condition for changing the transmission mode to the receive mode.  
And clear ICSR.WAIT to exit from the WAIT status.
8. Wait for a WAIT interrupt or until ICSR.WAIT becomes 1.
9. Set ICCR to H'C0 for the STOP condition. Set ICIC.DTEE to enable a DTE interrupt, then clear ICSR.WAIT to exit from the WAIT status.
10. Wait for a DTE interrupt or until ICSR.DTE becomes 1.
11. Read data from ICDR. The ICSR.DTE bit is then automatically cleared.
12. Wait until ICSR.BUSY is cleared to keep AC specification of  $t_{SU:STO}$ .
13. Clear ICCR.ICE to 0 to reset the IIC module.

Figure 45.8 shows the flowchart of 1-byte reception.

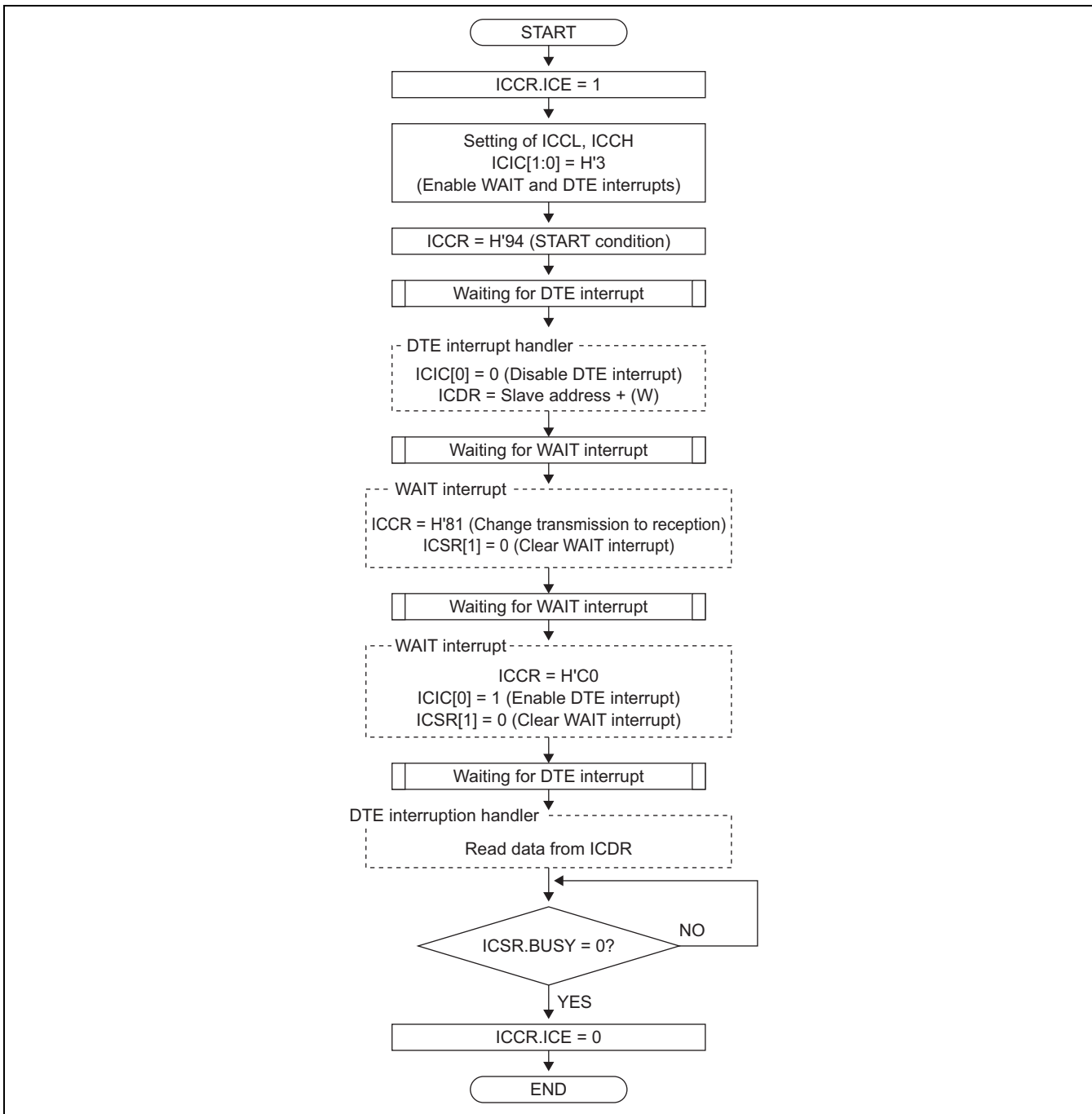


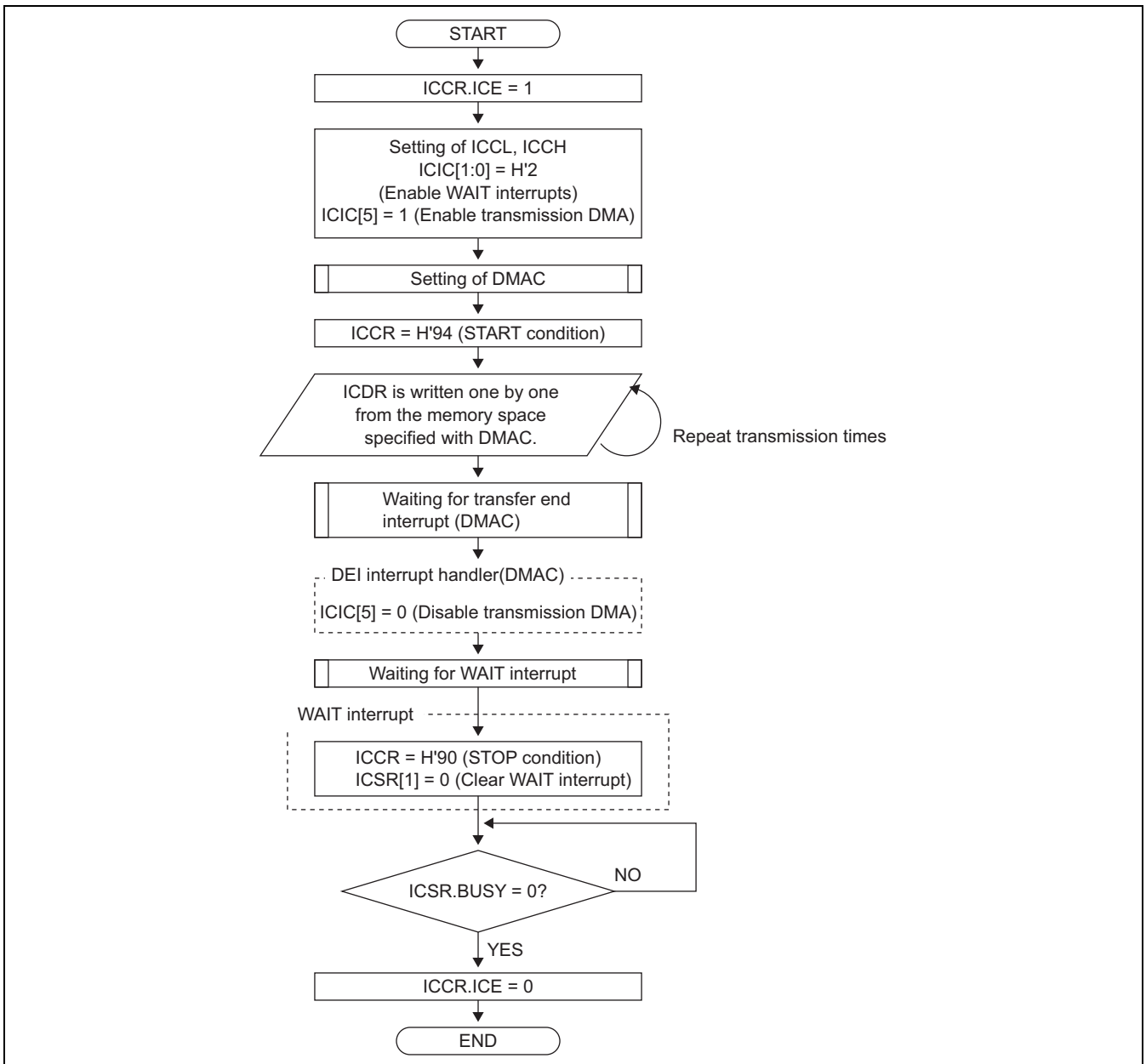
Figure 45.8 Example of Software Flow for 1-Byte Write/1-Byte Read (Using WAIT Function)

#### 45.4.4 IIC Continuous Transmission by DMA

In DMA transmit mode, the IIC module asserts a DMA request to the DMAC. The received DMAC writes data to ICDR, and returns DMARACK to the IIC module. The transmission procedure and operations are described below.

1. Set ICCR.ICE to activate the IIC module.
2. Set ICCL, ICCH, ICIC[1], and ICIC[5], according to the operating mode for DMA transmission. And set DMAC including number of transmission data.
3. Write H'94 to ICCR to issue the START condition.
4. DMAC writes the transmit data to ICDR from the memory space specified by DMAC register until transmission finishes.
5. Wait for a transfer end interrupt from DMAC.
6. Clear ICIC.TDMA to disable DMA transmission after a transfer end interrupt is asserted.
7. Wait for a WAIT interrupt or until ICSR.WAIT becomes 1.
8. Clear ICSR.WAIT to exit from the WAIT status. After the acknowledge clock, the STOP condition is generated and operation is stopped.
9. Wait until ICSR.BUSY is cleared to keep AC specification of  $t_{SU;STO}$ .
10. Clear ICCR.ICE to 0 to reset the IIC module.

Figure 45.9 shows the flow of data transmission with DMA.



**Figure 45.9 Example Flow for Transmission (a) Master Transmission Mode (Using WAIT and DMA Function)**

#### 45.4.5 IIC Continuous Receive by DMA

In DMA receive mode, the master device asserts DMA request to DMAC. The DMAC that received the request reads the received data from ICDR, and returns DMARACK to the IIC module. In case of receiving data continuously by DMA, 4 bytes or more receive data is required. The reception procedure and operations are described below.

1. Set ICCR.ICE to activate the IIC module.
2. Set ICCL, ICCH, and ICIC[1:0], according to the operating mode for DMA reception. And set DMAC register including number of receive data.
3. Write H'94 to ICCR to issue the START condition. The DTE bit in ICSR is then set to 1.
4. Wait for a DTE interrupt or until ICSR.DTE becomes 1.
5. Clear ICIC.DTEE to disable a DTE interrupt when the ICSR.DTE becomes 1.  
And write data (slave address and write bit) to ICDR. The ICSR.DTE bit is then automatically cleared. Data transmission starts when data is sent to the internal transmit buffer.
6. Wait for a WAIT interrupt or until ICSR.WAIT becomes 1.
7. If one or more transmission data remains, write data (ex. register address or data) to ICDR. And clear ICSR.WAIT to exit from the WAIT status. After exiting, go back to step 6.
8. If no more transmission data remains, write H'94 to ICCR to issue the repeated START condition. Set ICIC.DTEE to enable a DTE interrupt. And clear ICSR.WAIT to exit from the WAIT status. After exiting, go to step 9.
9. Wait for a DTE interrupt or until ICSR.DTE becomes 1.
10. Clear ICIC.DTEE to disable a DTE interrupt when the ICSR.DTE bit becomes 1. And write data (slave address and read bit) to ICDR. The ICSR.DTE is then automatically cleared.
11. Wait for a WAIT interrupt or until ICSR.WAIT becomes 1.
12. If one or more transmission data remains, write data (ex. register address or data) to ICDR. And clear ICSR.WAIT to exit from the WAIT status. After exiting, go back to step 11.
13. If no more transmission data remains, write H'81 to ICCR to issue the repeated START condition for changing the transmission mode to the receive mode. And clear ICSR.WAIT to exit from the WAIT status. After exiting, go to step 14.
14. DMAC reads the received data from ICDR, and stores them into the destination area until receiving data is finished.
15. Wait for a transfer end interrupt of DMAC.
16. Clear ICIC.RDMA to disable the received DMA, and set ICIC[1:0] to enable DTE and WAIT interrupts, when the transfer end interrupt is asserted.
17. Wait for a DTE interrupt or until ICSR.WAIT becomes 1.
18. Clear ICIC.DTEE to disable a DTE interrupt, and read data from ICDR. The ICSR.DTE bit is then automatically cleared.
19. Wait for a WAIT interrupt or until ICSR.WAIT becomes 1.
20. One receive data is remaining. And ICCR = H'C0 for the STOP condition.
21. Set ICIC.DTEE to enable a DTE interrupt. And clear ICSR.WAIT to exit from the WAIT status.
22. Wait for a DTE interrupt or until ICSR.DTE becomes 1.
23. Set ICIC.WAITE to disable a WAIT interrupt. And read data from ICDR. The ICSR.DTE bit is then automatically cleared.
24. Wait until CSR.BUSY is cleared to keep AC specification of  $t_{SU:STO}$ .
25. Clear ICCR.ICE to 0 to reset the IIC module.



Figure 45.10 is the flow of this.

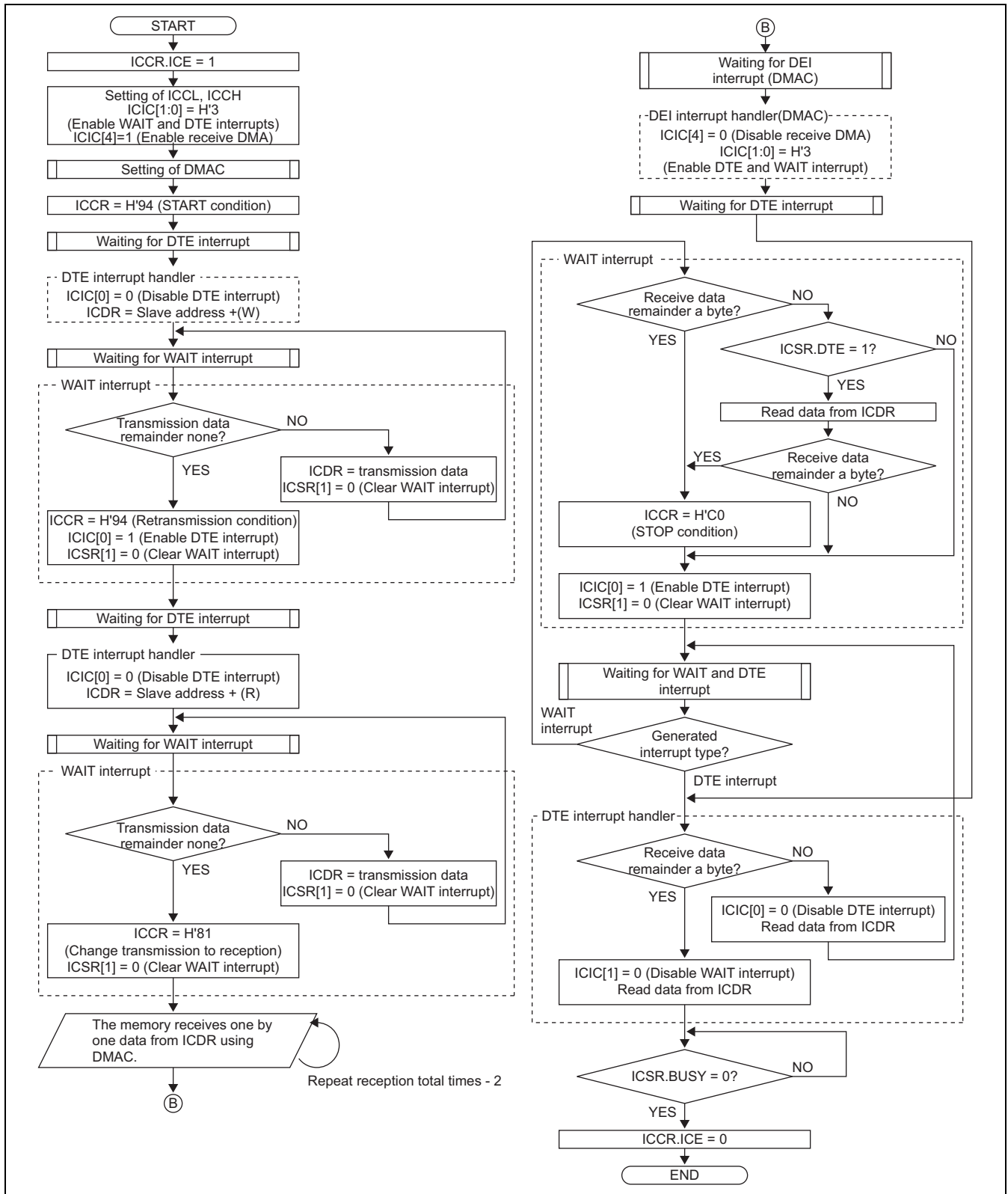


Figure 45.10 Example Flow for n-Byte Write/n-Byte Read (c) The Direction is Converted From Transmission to Reception (Using WAIT and DMA Function)

#### 45.4.6 Synchronizing SCL Line

When the SCL line state is changed from high to low, connected devices may start counting in the low period. When the clock of a device becomes low, the device holds the SCL line low until its clock becomes high (see Figure 45.11). However, even if the clock of the device is changed from low to high, the SCL line state does not change when clocks of other devices are in the low period. Therefore, the low period of the SCL line is determined by the device with the longest low period. At this time, a device with the short low period waits in the high state.

When all devices complete the low period, the clock line is open and in the high state. Therefore, the device clock and SCL line are in the same state, and start counting both of pulses in high level period. The SCL line enters the low state again by the device that has first completed the high period.

The low period is determined by the device with the longest low period, and the high period is determined by the device with the shortest high period. The SCL line is then synchronized.

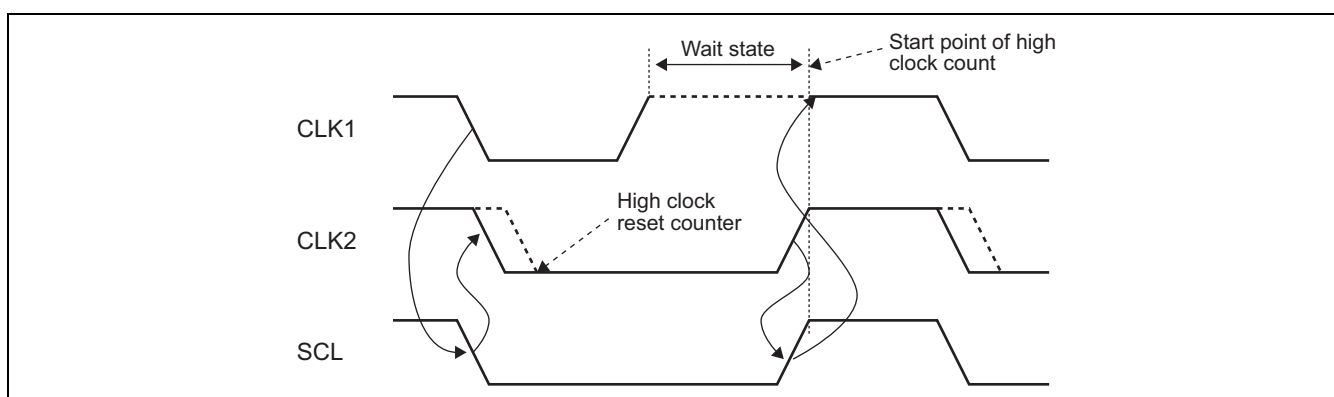
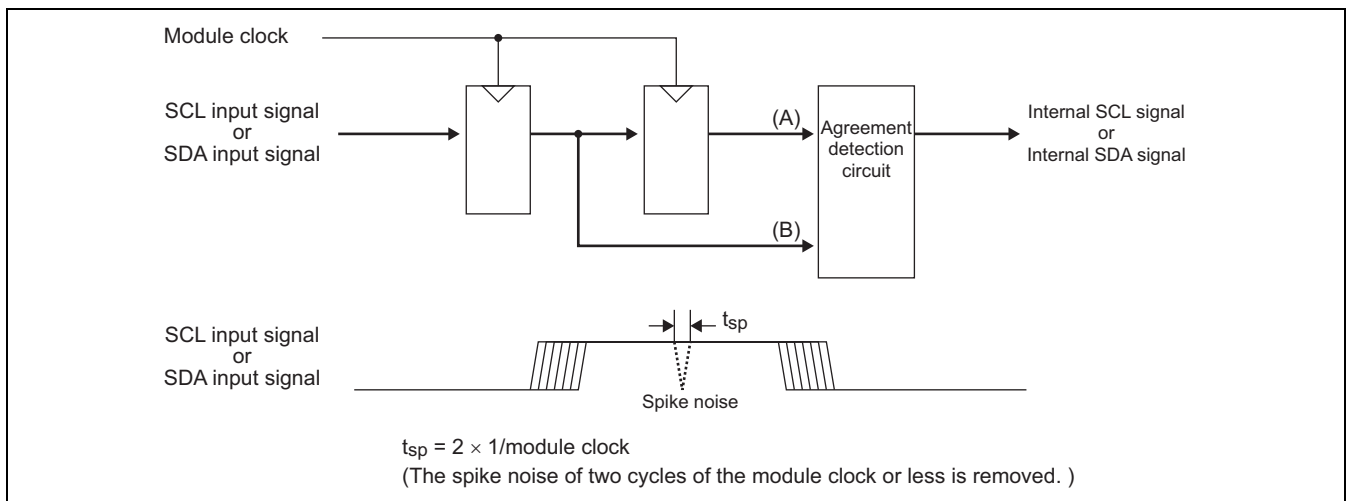


Figure 45.11 Synchronizing SCL Line

#### 45.4.7 Noise Canceller

For removing spike noise on the SCL and SDA line, the noise canceller circuit is implemented. Figure 45.12 shows a block diagram of the noise canceller circuit.

The noise canceller consists of two cascaded FFs and a match detector. The SCL/SDA signal is sampled by FFs with module clock, and recognize that SCL/SDA signals are toggled if both of two FF's outputs have toggled. If only one output of FFs have toggled, previously latched value is output to the internal logic.



**Figure 45.12 Block Diagram of Noise Canceller**

#### 45.4.8 Arbitration Lost Operation

This module can assert an arbitration lost interrupt request when bus conflict is detected.

Interrupt assert conditions are described below.

- When the level of the data being received changes during counting of the period at high level for the SCL clock.
- When the level on the SCL line becomes low, while the SCL clock is controlled by this module, and not driven by this module.
- When this module detects the START condition before issuing the START condition.
- When the SDA data driven by this module and monitored SDA signals are not equal.

In case of conditions above, the AL bit in ICSR is set to 1 and an arbitration lost interrupt is asserted.

When a loss of arbitration is detected in transmission mode, the SDA line is released right now. For SCL clock line, clocks kept be output until the end of the frame including acknowledge cycle and released. Figure 45.13 shows an example of arbitration lost interrupt operation timing.

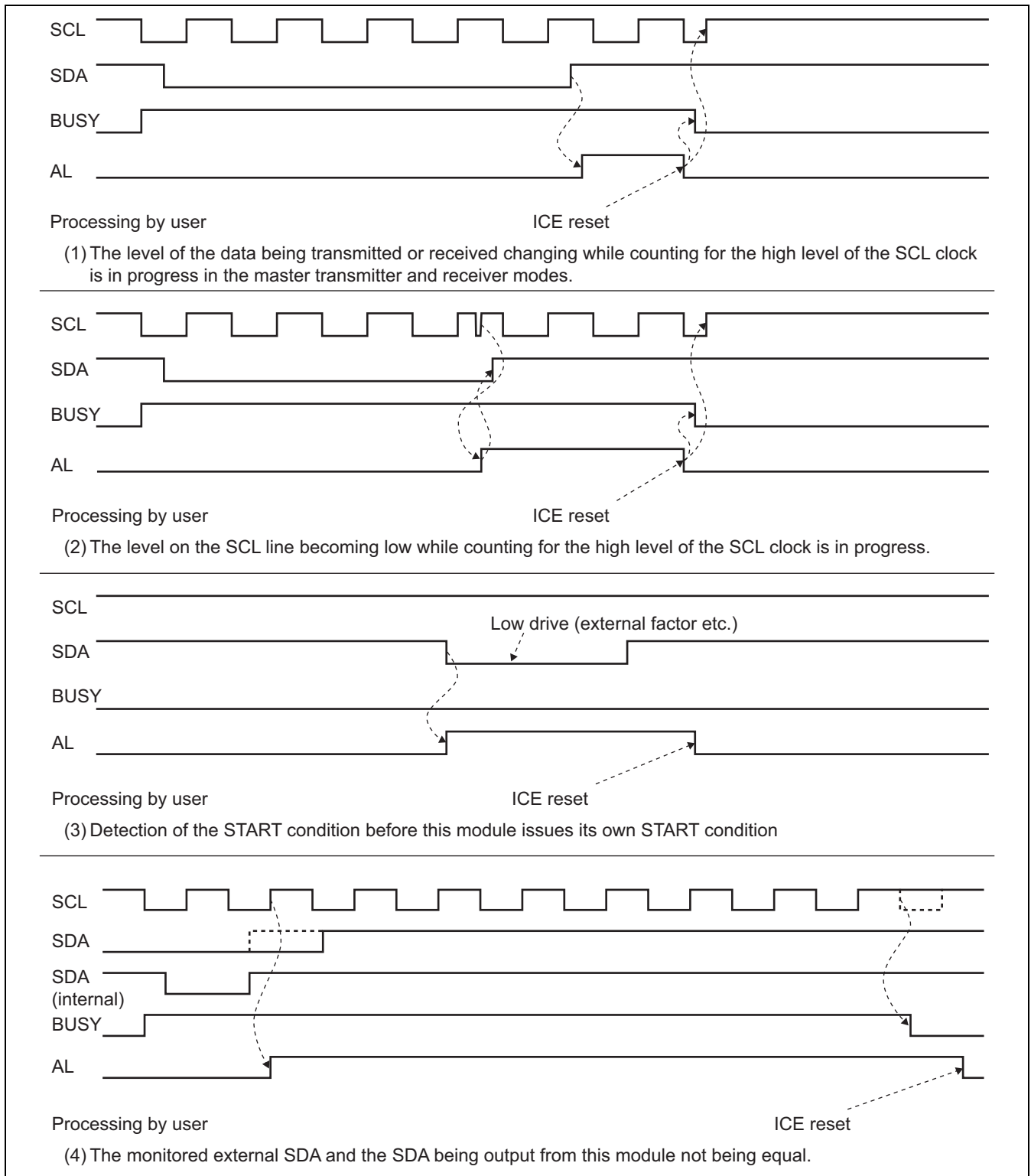
In case of conditions below, the AL bit in ICSR is set to 0.

- When data is written to ICDR (in transmission mode), or data is read (in receive mode) while DTE = 1.
- When 0 is written to the AL bit in ICSR.

When arbitration is lost by the acknowledge bit, hold SCL and SDA at a low level.

ICE reset must be performed by the software to release the bus.

Do not clear the ALE bit to 0 while the AL bit is 1. It is recommended to set ALE bit only before the start of communication.



**Figure 45.13 Example of Arbitration Lost Interrupt Operation Timing**

### 45.4.9 Non-Acknowledge Operation

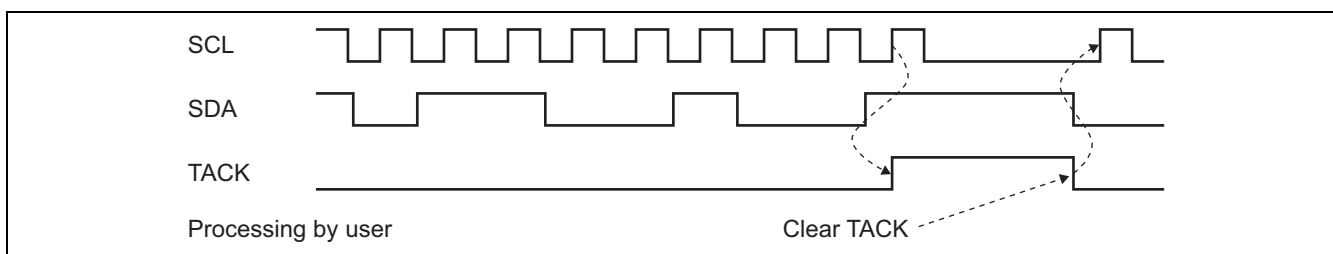
This module can assert a non-acknowledge interrupt when there is no acknowledge from the receiving device in transmission.

An acknowledge bit from the receiving device is stored in the TACK bit in ICSR. A non-acknowledge interrupt is asserted if the TACK bit is set to 1 when TACKE in ICIC is 1.

Generating a STOP condition after a non-acknowledge interrupt is recommended. The STOP condition should be generated even if the ICCR is already set for further processing (for example, generating the repeated START condition). Figure 45.15 shows an example processing of generating the STOP condition when non-acknowledge interrupt is asserted.

Do not set the TACKE bit in ICIC if processing for non-acknowledgement is not required. Do not clear TACKE bit to 0 while TACK bit is 1. It is recommended to set TACKE bit only before start of communication.

Figure 45.14 shows an example of non-acknowledge operation timing.



**Figure 45.14 Example of Non-Acknowledge Operation Timing**

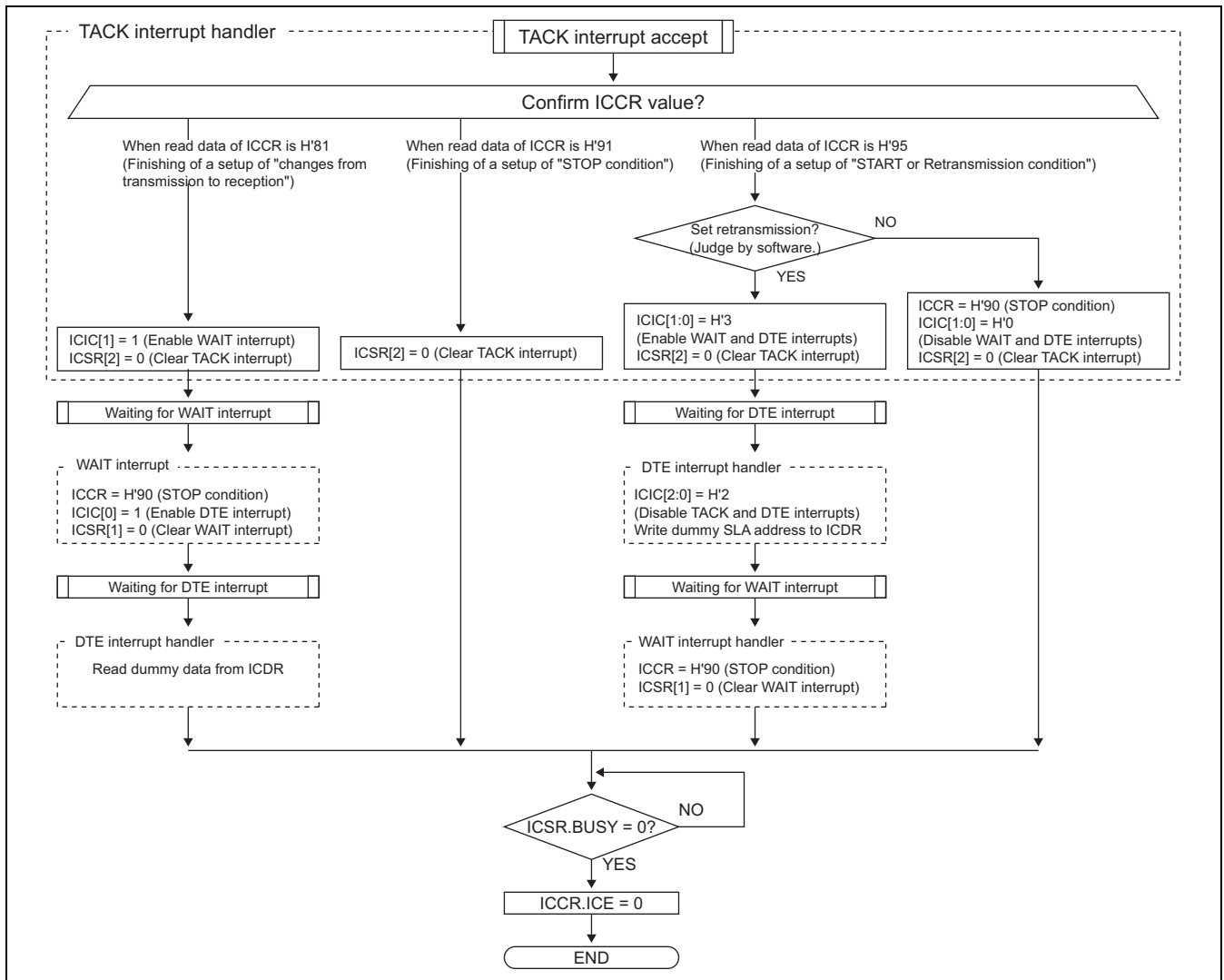


Figure 45.15 Generating a STOP Condition When Non-Acknowledge Interrupt Asserted

### 45.4.10 Wait Operation

This module can go into the wait state by assert of WAIT bit in ICSR. WAIT is set to 1 at the falling edge of the eighth transmit clock while this module is operating in master mode.

After that, the transmit clock is fixed to low until the WAIT bit is cleared to 0.

When the WAIT bit is cleared to 0, the ninth transmit clock is generated and the state is recovered from the wait state.

In case of using WAIT interrupt, data transfer by the I2C bus is suspended from the time WAIT is asserted by the hardware until the time WAIT is cleared by software.

It is recommended to set the WAITE bit only before the start of communication

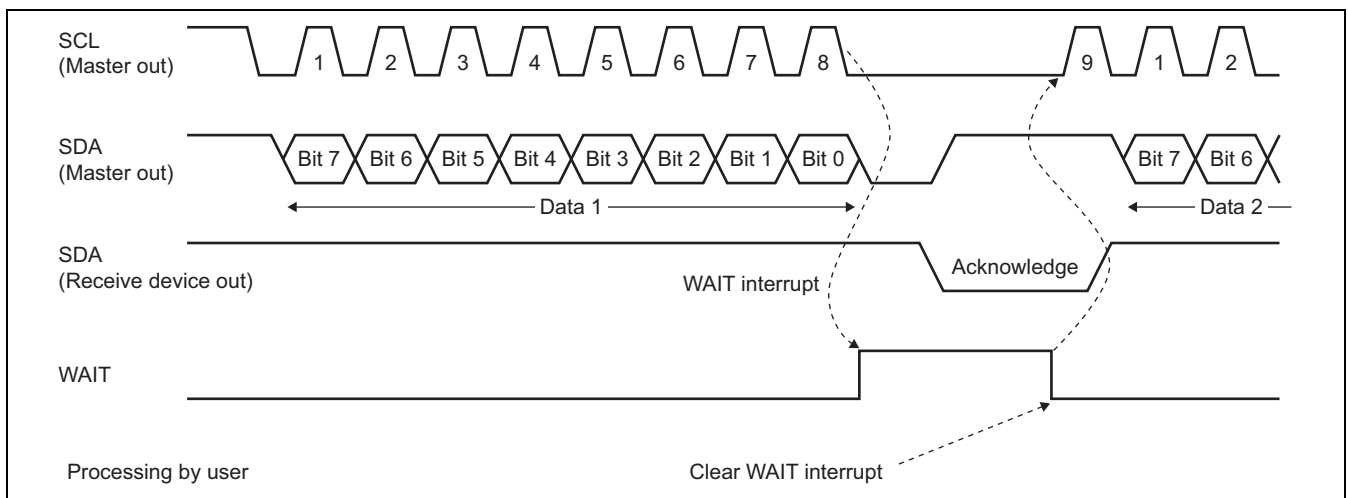


Figure 45.16 Example of Wait Operation Timing



## 45.5 Usage Note

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

### (1) Arbitration lost

When a loss of arbitration is detected, the I2C bus may not be released soon depending on the status of slave devices. Reset the IIC module by the ICE bit in ICCR register when re-starting data transfer after a loss of arbitration is detected.

### (2) ICE reset

When asserting ICE reset during data transfer, SCL clock is stopped immediately and the bus may not be released depending on the status of the slave device.

### (3) Processing for stop condition generation

When data is transmitted or received after a STOP condition is generated, it may not be possible to generate a STOP condition hereafter. Initialize all registers in the IIC module by clearing the ICE bit in ICCR to 0, after a STOP condition has been generated or before making settings to trigger data transmission or reception after a STOP condition has been generated.

### (4) Handling of IIC when not in use

Set the ICE bit in ICCR to 0 to disable the unused channels while the IIC bus interface is not used.

### (5) Abort of data transfer in the middle of IIC communication

Aborting data transfer may violate the I2C protocol. Make sure that the external device accepts such violations when you need to abort transfer in progress.

### (6) IIC Selection for Automatic Transmission (RZ/G1H, M and N)

When IIC3 is selected as automatic transmission control, initialize by software reset of the IIC (software reset for the IIC all channels must be performed before using the IIC3 as automatic transmission control).

## 46. Clock-Synchronized Serial Interface with FIFO (MSIOF)

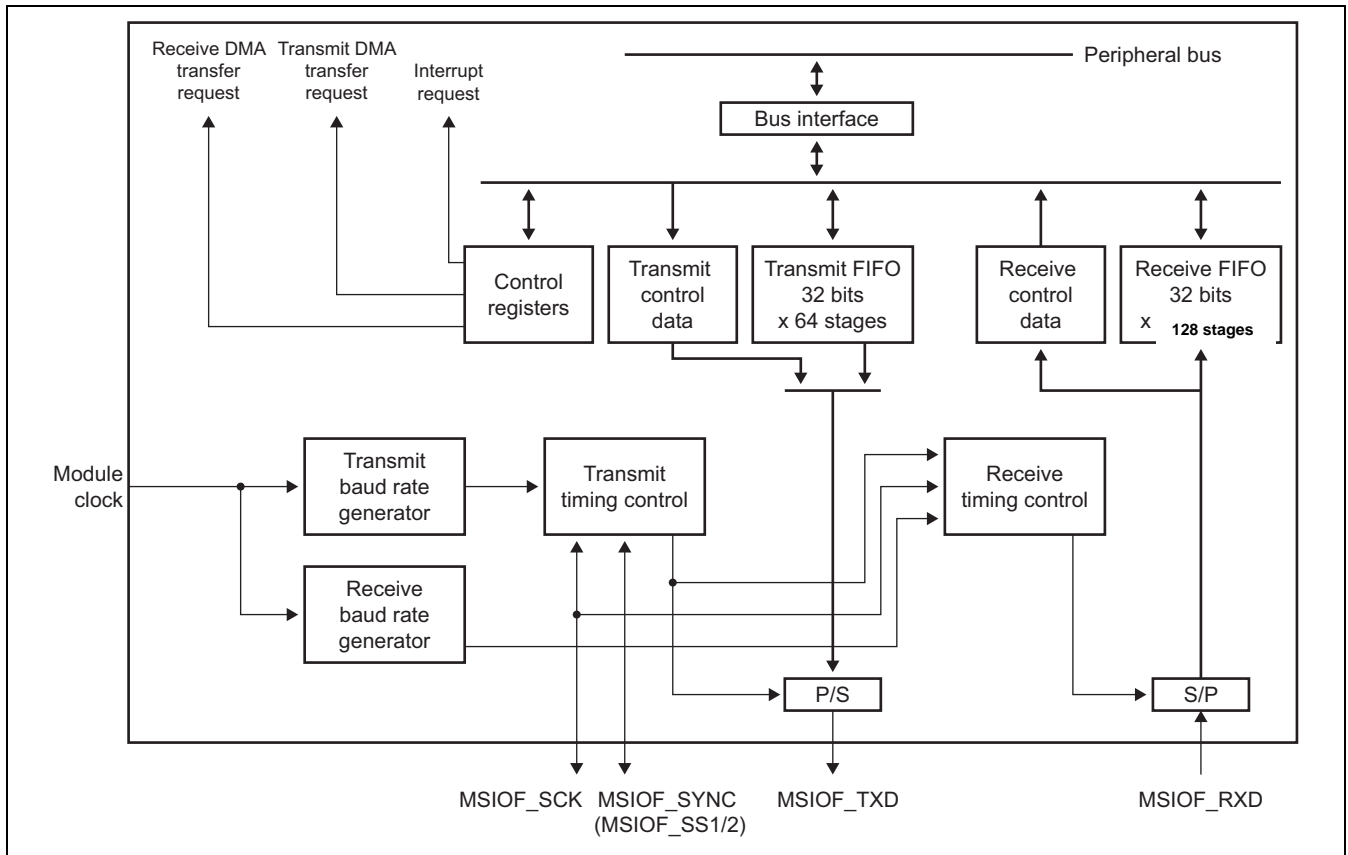
RZ/G1H	RZ/G1N
RZ/G1M	RZ/G1E

This LSI includes clock-synchronized serial I/O module with FIFO (MSIOF). In this module, MP $\phi$  is used as a module clock.

### 46.1 Features

- Number of channels: Four channels (RZ/G1H), three channels (RZ/G1M, N and E)
- FIFO capacity: 32 bits  $\times$  64 stages for transmission and 32 bits  $\times$  128 stages for reception
  - For reception FIFO, receiving 1 FRAME with 2 group with 64 words requires at most 128 FIFO stages.
- MSB first or LSB first selectable for data transmission and reception
- Synchronization by frame synchronization pulse, level, or left/right channel switch
- Supports master and slave modes
- Interrupts: One type
- Serial clock
- DMA transfer
- Serial format
  - Supports serial formats: IIS, SPI (master and slave\* modes).
  - Note: For SPI slave mode, refer to section 46.4.12, Limitation of SPI Mode.
- CLK/SYNC (SPI) in common transmit/receive mode
  - Up to 13 MHz for channels 0, 1 and 3 of RZ/G1H
  - Up to 26 MHz for channel 2 of RZ/G1H, and for all channels of RZ/G1M, RZ/G1N, and RZ/G1E

Figure 46.1 shows a block diagram of the MSIOF.



**Figure 46.1 Block Diagram of MSIOF**

## 46.2 Input/Output Pins

The pin configuration of this module is shown in Table 46.1.

**Table 46.1 Pin Configuration**

Name	Abbreviation	I/O	Function	RZ/G Series Products			
				RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
MSIOF_SCK	SCK	I/O	MSIOF serial clock for transmission Works as SCK when a common clock is used for transmission and reception.	√	√	√	√
MSIOF_SYNC	SYNC	I/O	MSIOF frame synchronization signal for transmission Works as SYNC when a common synchronization signal is used for transmission and reception.	√	√	√	√
MSIOF_SS1	SS1	Output	MSIOF frame synchronization signal 1 for transmission This signal can work only master mode.	√	√	√	√
MSIOF_SS2	SS2	Output	MSIOF frame synchronization signal 2 for transmission This signal can work only master mode.	√	√	√	√
MSIOF_TXD (MOSI/MISO)	MOSI/MISO (TXD)	Output	MSIOF transmit data	√	√	√	√
MSIOF_RXD (MISO/MOSI)	MISO/MOSI (RXD)	Input	MSIOF receive data	√	√	√	√

### 46.3 Register Descriptions

Tables 46.2 and 46.3 show the MSIOF register configuration and Table 46.4 shows the register state in each processing mode.

**Table 46.2 Module Base Address Summary**

		RZ/G Series Products			
Module Name	Base Address	RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
MSIOF0	H'E6E2 0000	√	√	√	√
MSIOF1	H'E6E1 0000	√	√	√	√
MSIOF2	H'E6E0 0000	√	√	√	√
MSIOF3	H'E6C9 0000	√	—	—	—

Note: Address H'E6xx can be accessed only by CPU.

**Table 46.3 Register Configuration**

						RZ/G Series Products			
Name	Abbreviation	R/W	Address Offset	Access Size	RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E	
MSIOF transmit mode register 1	SITMDR1	R/W	H'0000	32	√	√	√	√	
MSIOF transmit mode register 2	SITMDR2	R/W	H'0004	32	√	√	√	√	
MSIOF transmit mode register 3	SITMDR3	R/W	H'0008	32	√	√	√	√	
MSIOF receive mode register 1	SIRMDR1	R/W	H'0010	32	√	√	√	√	
MSIOF receive mode register 2	SIRMDR2	R/W	H'0014	32	√	√	√	√	
MSIOF receive mode register 3	SIRMDR3	R/W	H'0018	32	√	√	√	√	
MSIOF transmit clock select register	SITSCR	R/W	H'0020	16	√	√	√	√	
MSIOF control register	SICTR	R/W	H'0028	32	√	√	√	√	
MSIOF FIFO control register	SIFCTR	R/W	H'0030	32	√	√	√	√	
MSIOF status register	SISTR	R/W	H'0040	32	√	√	√	√	
MSIOF interrupt enable register	SIIER	R/W	H'0044	32	√	√	√	√	
MSIOF transmit FIFO data register	SITFDR	W	H'0050	32	√	√	√	√	
MSIOF receive FIFO data register	SIRFDR	R	H'0060	32	√	√	√	√	

**Table 46.4 Register States in Each Operating Mode**

<b>Abbreviation</b>	<b>Reset</b>	<b>Module Standby</b>
SITMDR1	Initialized	Retained
SITMDR2	Initialized	Retained
SITMDR3	Initialized	Retained
SIRMDR1	Initialized	Retained
SIRMDR2	Initialized	Retained
SIRMDR3	Initialized	Retained
SITSCR	Initialized	Retained
SICTR	Initialized	Retained
SIFCTR	Initialized	Retained
SISTR	Initialized	Retained
SIIER	Initialized	Retained
SITFDR	Initialized	Initialized
SIRFDR	Undefined	Initialized

### 46.3.1 MSIOF Transmit Mode Register 1 (SITMDR1)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SITMDR1 is a 32-bit readable/writable register that specifies the MSIOF transmit mode.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TRMD	PCON	SYNCMD[1:0]	SYNCCH[1:0]	SYNCA C	BITLSB	—	DTDL[2:0]	—	SYNCDL[2:0]	—	—	—	—	—	—
Initial value:	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	FLD[1:0]	—	TXSTP
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R

Bit	Bit Name	Initial Value	R/W	Descriptions
31	TRMD	1	R/W	Transfer Mode Selects the transfer mode. 0: Slave mode 1: Master mode
30	PCON	0	R/W	Transfer Signal Connection 0: Setting prohibited 1: MSIOF_SCK and MSIOF_SYNC are used as common signals for transmission and reception (MSIOF_SCK and MSIOF_SYNC).
29, 28	SYNCMD[1:0]	00	R/W	SYNC Mode These bits specify the mode for the MSIOF_SYNC signal. 00: Frame start synchronization pulse 01: Reserved 10: Level mode/SPI 11: L/R mode
27, 26	SYNCCH[1:0]	00	R/W	Synchronization Signal Channel Select These bits are valid only in master mode. 00: The frame synchronization signal output at MSIOF_SYNC. 01: The frame synchronization signal output at MSIOF_SS1. 10: The frame synchronization signal output at MSIOF_SS2. 11: Setting prohibited
25	SYNCA C	0	R/W	MSIOF_SYNC Polarity 0: Active-high signal in synchronization pulse or level mode, or driven high then low in L/R mode 1: Active-low signal in synchronization pulse or level mode, or driven low then high in L/R mode
24	BITLSB	0	R/W	MSB/LSB First 0: MSB first 1: LSB first

Bit	Bit Name	Initial Value	R/W	Descriptions
23	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
22 to 20	DTDLD[2:0]	001	R/W	Data Pin Bit Delay for MSIOF_SYNC Pin The value specified with TXDIZ in SICTR is output during transmission. B'1xx is valid only in SPI mode. In SPI mode, these bits should be specified so that the sum of the delays specified through DTDLD and SYNCDDL becomes an integer value. 000: No bit delay 001: 1-clock-cycle delay 010: 2-clock-cycle delay 101: 0.5-clock-cycle delay 110: 1.5-clock-cycle delay Other than above: Setting prohibited
19	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
18 to 16	SYNCDDL[2:0]	000	R/W	Frame Synchronization Signal Timing Delay These bits extend the transmit frame synchronization signal. The value specified with TXDIZ in SICTR is output during transmission. These bits are invalid when SYNCMD[1:0] = B'01. B'1xx is valid only in SPI mode. In SPI mode, these bits should be specified so that the sum of the delays specified through DTDLD and SYNCDDL becomes an integer value. When L/R mode, these bits should always be set to 000. 000: No bit delay 001: 1-clock-cycle delay 010: 2-clock-cycle delay 011: 3-clock-cycle delay 101: 0.5-clock-cycle delay 110: 1.5-clock-cycle delay Other than above: Setting prohibited
15 to 4	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
3, 2	FLD[1:0]	00	R/W	Frame Synchronization Signal Interval Specify the minimum idle time between frames in the number of serial clock cycles. This setting is valid only in master mode. When L/R mode, these bits should always be set to 00. When SPI mode, these bits shall not be set to 00. 00: 0-clock-cycle delay 01: 1-clock-cycle delay 10: 2-clock-cycle delay 11: 3-clock-cycle delay
1	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.



Bit	Bit Name	Initial Value	R/W	Descriptions
0	TXSTP	0	R/W	Transmission Stop 0: Setting prohibited 1: Temporarily stops transmission when the number of transmit FIFO stages is not enough to valid.

### 46.3.2 MSIOF Transmit Mode Register 2 (SITMDR2)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SITMDR2 is a 32-bit readable/writable register that specifies the MSIOF transmit mode.

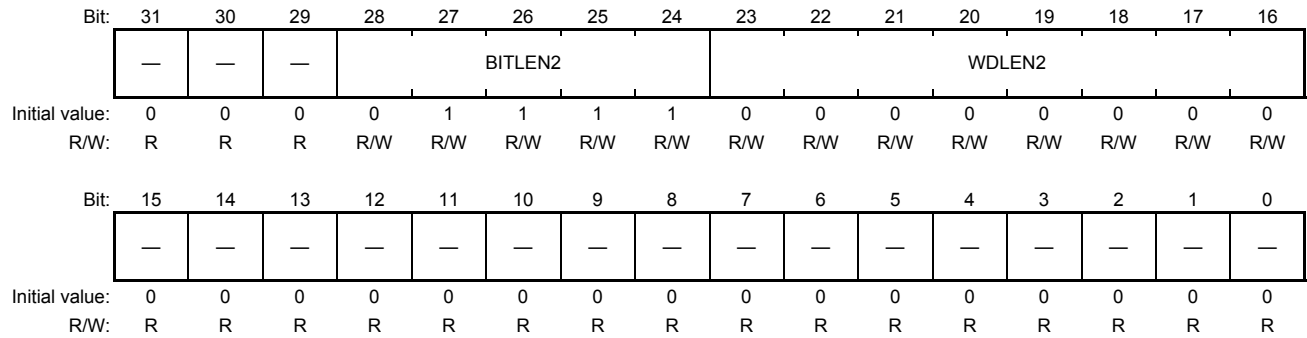
Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	GRP	—	BITLEN1				WDLEN1								
Initial value:	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0
R/W:	R	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Descriptions
31	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
30	GRP	0	R/W	Group Count The number of groups is set to the value specified in this bit + 1.
29	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
28 to 24	BITLEN1[4:0]	01111	R/W	Data Size (8 to 32 bits) The word size (bits) of groups 1 is set to the value specified in these bits + 1. Either 8, 16, 24, or 32 bits can be specified as word size.
23 to 16	WDLEN1[7:0]	H'00	R/W	Word Count (1 to 64 words) The word counts of groups 1 is set to WDLEN1 + 1 respectively. 8-bit value is set to WDLEN1.
15 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

**46.3.3 MSIOF Transmit Mode Register 3 (SITMDR3)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SITMDR3 is a 32-bit readable/writable register that specifies the MSIOF transmit mode.



Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28 to 24	BITLEN2	01111	R/W	Word Size (1 to 32 bits) The word size of groups 2 is set to the value specified in these bits + 1. Either 8, 16, 24, or 32 bits can be specified as word size.
23 to 16	WDLEN2	H'00	R/W	Word Count (1 to 64 words) The word counts of groups 2 are set to WDLEN2 + 1. 8-bit value is set to WDLEN2.
15 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

### 46.3.4 MSIOF Receive Mode Register 1 (SIRMDR1)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SIRMDR1 is a 32-bit readable/writable register that specifies the MSIOF receive mode.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TRMD	—	SYNCCMD[1:0]	—	—	SYNCA C	BITLSB	—	—	DTDL[2:0]	—	—	—	—	—	—
Initial value:	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
R/W:	R/W	R	R/W	R/W	R	R	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Descriptions
31	TRMD	1	R/W	Transfer Mode Selects the transfer mode. This bit should be set to 0.
30	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
29, 28	SYNCCMD [1:0]	00	R/W	SYNC Mode The mode setting in these bits should be the same as that in SITMDR1.SYNCCMD. 00: Frame start synchronization pulse 01: Reserved 10: Level mode/SPI 11: L/R mode
27, 26	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
25	SYNCCAC	0	R/W	SYNC Polarity 0: Active-high signal in synchronization pulse or level mode, or driven high then low in L/R mode 1: Active-low signal in synchronization pulse or level mode, or driven low then high in L/R mode This bit must have the same setting as the SYNCCAC bit of SITMDR1.
24	BITLSB	0	R/W	MSB/LSB First 0: MSB first 1: LSB first
23	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Descriptions
22 to 20	DTDLD[2:0]	001	R/W	<p>Data Pin Bit Delay for MSIOF_SYNC Pin</p> <p>000: No bit delay            001: 1-clock-cycle delay            010: 2-clock-cycle delay            101: 0.5-clock-cycle delay            110: 1.5-clock-cycle delay            Other than above: Setting prohibited</p> <p>In case of SPI mode, only 000 is allowed to set to this field.</p>
19	—	0	R	<p>Reserved</p> <p>This bit is always read as 0. The write value should always be 0.</p>
18 to 16	SYNCDL [2:0]	000	R/W	<p>MSIOF_SYNC Timing Delay</p> <p>The synchronization signal is extended for the clock cycles specified in these bits.</p> <p>These bits are invalid when SYNCMD[1:0] = B'01.</p> <p>In L/R mode, these bits should always be set to 000.</p> <p>000: No bit delay            001: 1-clock-cycle delay            010: 2-clock-cycle delay            011: 3-clock-cycle delay            101: 0.5-clock-cycle delay            110: 1.5-clock-cycle delay            Other than above: Setting prohibited</p> <p>In case of SPI mode, only 000 is allowed to set to this field.</p>
15 to 0	—	All 0	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>

### 46.3.5 MSIOF Receive Mode Register 2 (SIRMDR2)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SIRMDR2 is a 32-bit readable/writable register that specifies the MSIOF receive mode.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	GRP	—	BITLEN1[4:0]				WDLEN1[7:0]								
Initial value:	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0
R/W:	R	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Descriptions
31	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
30	GRP	0	R/W	Group Count The number of groups is set to the value specified in this bit + 1. Set the same value as the value specified by the GRP bit in SITMDR2.
29	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
28 to 24	BITLEN1[4:0]	01111	R/W	Word Size (8 to 32 bits) The word size (bits) of groups 1 is set to the value specified in these bits + 1. Either 8, 16, 24, or 32 bits can be specified as word size. Set the same value as the value specified by the BITLEN1 bits in SITMDR2.
23 to 16	WDLEN1[7:0]	H'00	R/W	Word Count (1 to 64 words) The word counts of groups 1 is set to WDLEN1 + 1. When one or two groups are used, the 8-bit value is set to WDLEN1. Set the same value as the value specified by the WDLEN1 bits in SITMDR2.
15 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

### 46.3.6 MSIOF Receive Mode Register 3 (SIRMDR3)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SIRMDR3 is a 32-bit readable/writable register that specifies the MSIOF receive mode.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16			
	—	—	—	BITLEN2[4:0]				WDLEN2[7:0]											
Initial value:	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0			
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R			

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28 to 24	BITLEN2[4:0]	01111	R/W	Word Size (1 to 32 bits) The word size is set to the value specified in these bits + 1. Either 8, 16, 24, or 32 bits can be specified as word size. Set the same value as the value specified by the BITLEN2 bits in SITMDR3.
23 to 16	WDLEN2[7:0]	H'00	R/W	Word Count (1 to 64 words) The word counts of groups 2 is set to WDLEN2 + 1. 8-bit value is set to WDLEN2. Set the same value as the value specified by the WDLEN2 bits in SITMDR3.
15 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

### 46.3.7 MSIOF Control Register (SICTR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SICTR is a 32-bit readable/writable register that specifies the MSIOF operating state.

The values written to the TXE, RXE, TFSE, RFSE, TSCKE, and RSCKE bits become valid (can be read from the bits) several cycles after writing. These bits should not be modified at the same time. Modify one bit at a time, and check that the new value can be read from the bit, and then modify another bit.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TSCKIZ[1:0]		RSCKIZ[1:0]		TEDG	REDG	—	—	TXDIZ[1:0]		—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TSCKE	TFSE	RSCKE	RFSE	—	—	TXE	RXE	—	—	—	—	—	—	TXRST	RXRST
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Descriptions
31, 30	TSCKIZ[1:0]	00	R/W	<p>Transmit Clock Input/Output Polarity Select in SPI Mode When Transmission is Disabled</p> <p>When SPI mode is not used, these bits must always be set to 00. These bits must always be set 10 or 11 when SPI mode.</p> <p>[Master mode]</p> <p>00: Outputs MSIOF_SCK when transmission is disabled.</p> <p>01: Setting prohibited</p> <p>10: Outputs 0.</p> <p>11: Outputs 1.</p> <p>[Slave mode]</p> <p>00: Inputs MSIOF_SCK when transmission is disabled.</p> <p>01: Setting prohibited</p> <p>10: Inputs 0 through MSIOF_SCK when transmission is disabled.</p> <p>11: Inputs 1 through MSIOF_SCK when transmission is disabled.</p>
29, 28	RSCKIZ[1:0]	00	R/W	<p>Receive Clock Polarity Select in SPI Mode</p> <p>Set the same value as the value specified by the TSCKIZ bits. Other setting is prohibited.</p>
27	TEDG	0	R/W	<p>Transmit Timing</p> <p>0: Outputs transmit data at the rising edge of the clock.</p> <p>1: Outputs transmit data at the falling edge of the clock.</p>
26	REDG	0	R/W	<p>Receive Timing</p> <p>0: Samples receive data at the falling edge of the clock.</p> <p>1: Samples receive data at the rising edge of the clock.</p>
25, 24	—	All 0	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>

Bit	Bit Name	Initial Value	R/W	Descriptions
23, 22	TXDIZ[1:0]	00	R/W	<p>Pin Output When Transmission is Disabled</p> <p>These bits specify the MSIOF_TXD pin output state when transmission is disabled.</p> <p>00: Outputs 0. 01: Outputs 1. 10: Output is in high-impedance state. 11: Setting prohibited</p>
21 to 16	—	All 0	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>
15	TSCKE	0	R/W	<p>Transmit Serial Clock Output Enable</p> <p>This bit is valid in master mode.</p> <p>When this bit is set to 1, the MSIOF initializes the baud rate generator and initiates the operation. At the same time, the MSIOF outputs the clock generated by the baud rate generator to the MSIOF_SCK pin. After the clock is output, 1 can be read.</p> <p>When transmitting data, set this bit to 1 before setting the TFSE and TXE bits. After data transmission, clear the TFSE and TXE bits and then clear this bit to 0.</p> <p>[Write data] 0: Disables the MSIOF_SCK output. (Outputs the value specified with TSCKIZ.) 1: Enables the MSIOF_SCK output.</p> <p>[Read data] 0: Does not output MSIOF_SCK. (Outputs the value specified with TSCKIZ.) 1: Outputs MSIOF_SCK.</p>
14	TFSE	0	R/W	<p>Transmit Frame Synchronization Signal Output Enable</p> <p>This bit is valid in master mode.</p> <p>When this bit is set to 1, the MSIOF initializes the frame counter and initiates the operation. After the transmit frame synchronization signal is output, 1 can be read. When 0 is written to this bit, 0 is set after transmission of the frame.</p> <p>[Write data] 0: Disables the MSIOF_SYNC output. (Outputs the value specified with SYNCAC.) 1: Enables the MSIOF_SYNC output.</p> <p>[Read data] 0: Does not output MSIOF_SYNC. (Outputs the value specified with SYNCAC.) 1: Outputs MSIOF_SYNC.</p>
13	RSCKE	0	R/W	<p>Receive Serial Clock Output Enable</p> <p>The write value should always be 0.</p>
12	RFSE	0	R/W	<p>Receive Frame Synchronization Signal Output Enable</p> <p>The write value should always be 0.</p>
11, 10	—	All 0	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>



Bit	Bit Name	Initial Value	R/W	Descriptions
9	TXE	0	R/W	<p>Transmit Enable</p> <p>When this bit is set to 1, the MSIOF starts data transmission from the beginning of the next frame (at the rising edge of the frame synchronization signal). After the valid data is output, 1 can be read.</p> <p>When value 1 set to this bit becomes valid, the MSIOF issues a transmit data transfer request according to the setting of the TFWM bits in SIFCTR. When transmit data is stored in the transmit FIFO, transmission of data from the MSIOF_TXD pin begins. When 0 is written to this bit, 0 is set after transmission of the frame.</p> <p>This bit is initialized upon a transmit reset.</p> <p>[Write data]</p> <p>0: Disables the MSIOF_TXD output. (Outputs the value specified with TXDIZ.)</p> <p>1: Enables the MSIOF_TXD output.</p> <p>[Read data]</p> <p>0: Does not output MSIOF_TXD. (Outputs the value specified with TXDIZ.)</p> <p>1: Outputs MSIOF_TXD.</p>
8	RXE	0	R/W	<p>Receive Enable</p> <p>When this bit is set to 1, the MSIOF starts data reception from the beginning of the next frame (at the rising edge of the frame synchronization signal).</p> <p>When value 1 set to this bit becomes valid, the MSIOF starts receiving data through the MSIOF_RXD pin. When receive data is stored in the receive FIFO, the MSIOF issues a receive data transfer request according to the setting of the RFWM bits in SIFCTR.</p> <p>This bit is initialized upon a receive reset.</p> <p>[Write data]</p> <p>0: Disables data reception through MSIOF_RXD.</p> <p>1: Enables data reception through MSIOF_RXD.</p> <p>[Read data]</p> <p>0: Data is not received through MSIOF_RXD.</p> <p>1: Data can be received through MSIOF_RXD.</p>
7 to 2	—	All 0	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>

Bit	Bit Name	Initial Value	R/W	Descriptions
1	TXRST	0	R/W	<p><b>Transmit Reset</b></p> <p>When value 1 set to this bit becomes valid, the MSIOF immediately sets transmit data through the MSIOF_TXD pin to 0, and initializes the transmit data registers and transmit-related status. When value 1 set to this bit becomes valid when PCON = 1, the RXRST bit is also becomes valid. The following registers and bits are initialized.</p> <p>SITFDR (Transmit FIFO write pointer)</p> <p>TDREQ bit in SISTR</p> <p>TXE bit</p> <p>This bit is read as 1 until the reset operation is completed for about 20 cycles of module clock. No data should be written to SICTR or the transmit FIFO during this time period.</p> <p>[Write data]</p> <p>0: Does not reset transmit operation. 1: Resets transmit operation.</p> <p>[Read data]</p> <p>0: Transmit operation reset is completed. 1: Transmit operation is being reset.</p>
0	RXRST	0	R/W	<p><b>Receive Reset</b></p> <p>When value 1 set to this bit becomes valid, the MSIOF immediately disables reception through the MSIOF_RXD pin, and initializes the receive data registers and receive-related status. The following registers and bits are initialized.</p> <p>SIRFDR (Receive FIFO read pointer)</p> <p>RDREQ bit in SISTR</p> <p>RXE bit</p> <p>This bit is read as 1 until the reset operation is completed for about 20 cycles of module clock. No data should be written to SICTR or read the receive FIFO during this time period.</p> <p>[Write data]</p> <p>0: Does not reset receive operation. 1: Resets receive operation.</p> <p>[Read data]</p> <p>0: Receive operation reset is completed. 1: Receive operation is being reset.</p>

### 46.3.8 MSIOF Transmit Clock Select Register (SITSCR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SITSCR is a 16-bit readable/writable register that specifies the conditions for generating transmit serial clock in master mode. SITSCR can be specified when the TRMD bit in SITMDR1 is set to B'1.

For the channels 0, 1 and 3 of the RZ/G1H, maximum transfer rate is limited up to 13 MHz. Please specify this register, to make transfer rate equal or less than 13 MHz.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSSEL[1:0]		MSIMM	BRPS[4:0]				—	—	—	—	—	BRDV[2:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R/W	R/W	R/W

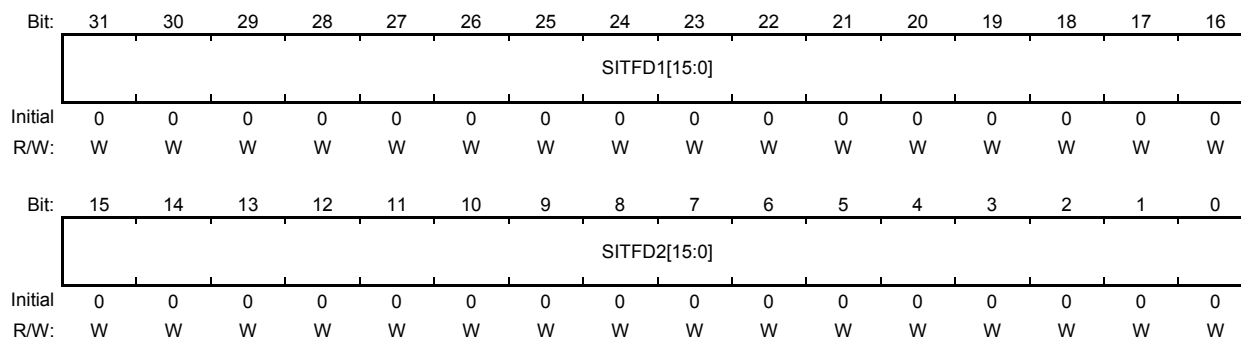
Bit	Bit Name	Initial Value	R/W	Descriptions
15, 14	MSSEL[1:0]	00	R/W	Master Clock Source Select The master clock is the clock input to the baud rate generator. 00: Selects module clock as the source of master clock. Others: Setting prohibited
13	MSIMM	0	R/W	Master Clock Direct Select 0: Selects the clock output from the baud rate generator as the serial clock. 1: Setting prohibited
12 to 8	BRPS[4:0]	00000	R/W	Prescaler Setting These bits specify the master clock (MP $\phi$ ) division ratio in the count value of the prescaler in the baud rate generator. The specifiable value is from B'00000 ( $\times 1/1$ ) to B'11111 ( $\times 1/32$ ).
7 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Descriptions
2 to 0	BRDV[2:0]	000	R/W	<p>Baud Rate Generator's Division Ratio</p> <p>These bits specify the frequency division ratio for the output stage of the baud rate generator.</p> <p>The final frequency division ratio of the baud rate generator is determined as <math>BRPS \times BRDV</math> (1/1024 max.).</p> <p>000: Prescalar output <math>\times 1/2</math>            001: Prescalar output <math>\times 1/4</math>            010: Prescalar output <math>\times 1/8</math>            011: Prescalar output <math>\times 1/16</math>            100: Prescalar output <math>\times 1/32</math>            101: Setting prohibited            110: Setting prohibited            111: Prescalar output <math>\times 1/1</math></p> <p>Note: B'111 is valid only when the BRPS[4:0] bits are set to B'00000 or B'00001.</p>

### 46.3.9 MSIOF Transmit FIFO Data Register (SITFDR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SITFDR is a 32-bit write-only register that specifies the transmit FIFO data of the MSIOF.

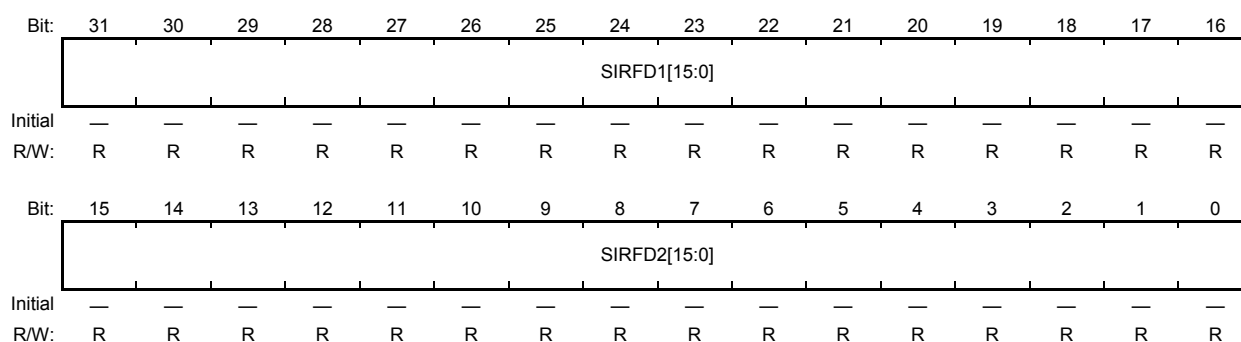


Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 16	SITFD1[15:0]	H'0000	W	These bits specify the upper 16 bits of the FIFO data to be output through MSIOF_TXD.
15 to 0	SITFD2[15:0]	H'0000	W	These bits specify the lower 16 bits of the FIFO data to be output through MSIOF_TXD.

### 46.3.10 MSIOF Receive FIFO Data Register (SIRFDR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SIRFDR is a 32-bit read-only register that stores the receive FIFO data of the MSIOF.



Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 16	SIRFD1[15:0]	Undefined	R	Store the upper 16 bits of the FIFO data received through MSIOF_RXD.
15 to 0	SIRFD2[15:0]	Undefined	R	Store the lower 16 bits of the FIFO data received through MSIOF_RXD.

### 46.3.11 MSIOF Status Register (SISTR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Each bit in SISTR becomes an MSIOF interrupt source when the corresponding bit in SIIER is set to 1.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	TFEMP	TDREQ	—	—	—	—	TEOF	—	TFS ERR	TFOVF	TFUDF	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R	R	R	R	R	R/W	R	R/W	R/W	R/W	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	RFFUL	RDREQ	—	—	—	—	REOF	—	RFS ERR	RFUDF	RFOVF	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R	R	R	R	R	R/W	R	R/W	R/W	R/W	R	R	R

Bit	Bit Name	Initial Value	R/W	Descriptions
31, 30	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
29	TFEMP	0	R/W	Transmit FIFO Empty This bit is set to 1, when the TXE bit in SICTR is 1, and transmit FIFO is empty. Writing 1 to this bit clears this bit. Writing 0 to this bit is ignored. If the interrupt request from this bit is enabled, an MSIOF interrupt is issued. 0: Transmit FIFO is not empty. 1: Transmit FIFO is empty.
28	TDREQ	0	R	Transmit Data Transfer Request This bit is set, when the empty space in the transmit FIFO exceeds the size specified by the TFWM bits in SIFCTR. When transferring transmit data through the DMAC, this bit is always cleared after one DMAC access. After DMAC access, when the conditions for setting this bit are satisfied, the MSIOF again sets this bit to 1. This bit is valid when the TXE bit in SICTR is 1. This bit indicates a state; if the size of empty space in the transmit FIFO becomes less than the size specified by the TFWM bits in SIFCTR, the MSIOF clears this bit. If the interrupt request from this bit is enabled, an MSIOF interrupt is issued. However, when the TDMAE bit is 1, only a DMAC transfer request is issued. 0: The size of empty space in the transmit FIFO has not exceeded the size specified by the TFWM bits in SIFCTR. 1: The size of empty space in the transmit FIFO has exceeded the size specified by the TFWM bits in SIFCTR.
27 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Descriptions
23	TEOF	0	R/W	<p>Frame Transmission End</p> <p>This bit is set, when one-frame data transmission is completed.</p> <p>This bit is valid when the TXE bit in SICTR is 1.</p> <p>Writing 1 to this bit clears this bit.</p> <p>Writing 0 to this bit is ignored.</p> <p>If the interrupt request from this bit is enabled, an MSIOF interrupt is issued.</p> <p>0: One-frame transmission end is not detected.</p> <p>1: One-frame transmission end is detected.</p>
22	—	0	R	<p>Reserved</p> <p>This bit is always read as 0. The write value should always be 0.</p>
21	TFSERR	0	R/W	<p>Transmit Frame Synchronization Error</p> <p>This bit is set, when the next transmit frame synchronization timing arrives before the previous data or control data transmission has been completed.</p> <p>If a transmit frame synchronization error occurs, the MSIOF performs transmission only for the slots that can be transferred.</p> <p>This bit is valid when the TXE bit in SICTR is 1.</p> <p>Writing 1 to this bit clears this bit.</p> <p>Writing 0 to this bit is ignored.</p> <p>If the interrupt request from this bit is enabled, an MSIOF interrupt is issued.</p> <p>0: No transmit frame synchronization error has occurred.</p> <p>1: A transmit frame synchronization error has occurred.</p>
20	TFOVF	0	R/W	<p>Transmit FIFO Overflow</p> <p>A transmit FIFO overflow means that there has been an attempt to write to SITFDR when the transmit FIFO is full.</p> <p>If a transmit FIFO overflow occurs, the MSIOF ignores the write operation causing the overflow.</p> <p>This bit is valid when the TXE bit in SICTR is 1.</p> <p>Writing 1 to this bit clears this bit.</p> <p>Writing 0 to this bit is ignored.</p> <p>If the interrupt request from this bit is enabled, an MSIOF interrupt is issued.</p> <p>0: No transmit FIFO overflow has occurred.</p> <p>1: A transmit FIFO overflow has occurred.</p>
19	TFUDF	0	R/W	<p>Transmit FIFO Underflow</p> <p>A transmit FIFO underflow means that loading for transmission has occurred when the transmit FIFO is empty. Output data is unknown when under flow is occurred.</p> <p>This bit is valid when the TXE bit in SICTR is 1.</p> <p>Writing 1 to this bit clears this bit.</p> <p>Writing 0 to this bit is ignored.</p> <p>If the interrupt request from this bit is enabled, an MSIOF interrupt is issued.</p> <p>0: No transmit FIFO underflow has occurred.</p> <p>1: A transmit FIFO underflow has occurred.</p>

Bit	Bit Name	Initial Value	R/W	Descriptions
18 to 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13	RFFUL	0	R/W	Receive FIFO Full This bit is valid when the RXE bit in SICTR is 1. Writing 1 to this bit clears this bit. Writing 0 to this bit is ignored. If the interrupt request from this bit is enabled, an MSIOF interrupt is issued. 0: Receive FIFO is not full. 1: Receive FIFO is full.
12	RDREQ	0	R	Receive Data Transfer Request This bit is set, when the valid data space in the receive FIFO exceeds the size specified by the RFWM bits in SIFCTR. When transferring receive data through the DMAC, this bit is always cleared by one DMAC access. After DMAC access, when the conditions for setting this bit are satisfied, the MSIOF again sets this bit to 1. This bit is valid when the RXE bit in SICTR is 1. This bit indicates a state; if the size of valid data space in the receive FIFO becomes less than the size specified by the RFWM bits in SIFCTR, the MSIOF clears this bit. If the interrupt request from this bit is enabled, an MSIOF interrupt is issued. However, when the RDMAE bit is 1, only a DMAC transfer request is issued. 0: The size of valid data space in the receive FIFO has not exceeded the size specified by the RFWM bits in SIFCTR. 1: The size of valid data space in the receive FIFO has exceeded the size specified by the RFWM bits in SIFCTR.
11 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7	REOF	0	R/W	Frame Reception End The MSIOF issues the frame reception end flag upon completion of one-frame data reception. This bit is valid when the RXE bit in SICTR is 1. Writing 1 to this bit clears this bit. Writing 0 to this bit is ignored. If the interrupt request from this bit is enabled, an MSIOF interrupt is issued. 0: One-frame reception end is not detected. 1: One-frame reception end is detected.
6	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.



Bit	Bit Name	Initial Value	R/W	Descriptions
5	RFSERR	0	R/W	<p>Receive Frame Synchronization Error</p> <p>A receive frame synchronization error occurs when the next receive frame synchronization timing arrives before the previous data or control data reception has been completed.</p> <p>If a receive frame synchronization error occurs, the MSIOF performs reception only for the slots that can be transferred.</p> <p>This bit is valid when the RXE bit in SICTR is 1.</p> <p>Writing 1 to this bit will clear this bit.</p> <p>Writing 0 to this bit will be ignored.</p> <p>If the interrupt request from this bit is enabled, an MSIOF interrupt is issued.</p> <p>0: No receive frame synchronization error has occurred 1: A receive frame synchronization error has occurred</p>
4	RFUDF	0	R/W	<p>Receive FIFO Underflow</p> <p>A receive FIFO underflow means that reading of SIRFDR has occurred when the receive FIFO is empty.</p> <p>If a receive FIFO underflow occurs, the value read from SIRFDR is not guaranteed.</p> <p>This bit is valid when the RXE bit in SICTR is 1.</p> <p>Writing 1 to this bit clears this bit.</p> <p>Writing 0 to this bit is ignored.</p> <p>If the interrupt request from this bit is enabled, an MSIOF interrupt is issued.</p> <p>0: No receive FIFO underflow has occurred. 1: A receive FIFO underflow has occurred.</p>
3	RFOVF	0	R/W	<p>Receive FIFO Overflow</p> <p>A receive FIFO overflow means that writing has been caused by receiving operation when the receive FIFO is full.</p> <p>If a receive FIFO overflow occurs, the receive data causing the overflow is lost.</p> <p>This bit is valid when the RXE bit in SICTR is 1.</p> <p>Writing 1 to this bit clears this bit.</p> <p>Writing 0 to this bit is ignored.</p> <p>If the interrupt request from this bit is enabled, an MSIOF interrupt is issued.</p> <p>0: No receive FIFO overflow has occurred. 1: A receive FIFO overflow has occurred.</p>
2 to 0	—	All 0	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>

### 46.3.12 MSIOF Interrupt Enable Register (SIER)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SIER is a 32-bit readable/writable register that enables the issuance of MSIOF interrupts. When each bit in this register is set to 1 and the corresponding bit in SISTR is set to 1, the MSIOF issues an interrupt.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TDMAE	—	TFEMPE	TDREQE	—	—	—	—	TEOFE	—	TFSERRE	TFOVFE	TFUDFE	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R/W	R/W	R	R	R	R	R/W	R	R/W	R/W	R/W	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RDMAE	—	RFFUL E	RDREQE	—	—	—	—	REOFE	—	RFSERRE	RFUDFE	RFOVFE	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R/W	R/W	R	R	R	R	R/W	R	R/W	R/W	R/W	R	R	R

Bit	Bit Name	Initial Value	R/W	Descriptions
31	TDMAE	0	R/W	Transmit Data DMA Transfer Request Enable Specifies whether to send an interrupt as an interrupt request to the CPU or a transfer request to the DMAC. The TDREQE bit can be set as the request source. 0: Sends an interrupt request to the CPU. 1: Sends a DMA transfer request to the DMAC.
30	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
29	TFEMPE	0	R/W	Transmit FIFO Empty Enable 0: Disables interrupts due to transmit FIFO empty. 1: Enables interrupts due to transmit FIFO empty.
28	TDREQE	0	R/W	Transmit Data Transfer Request Enable 0: Disables interrupts due to transmit data transfer requests. 1: Enables interrupts due to transmit data transfer requests.
27 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23	TEOFE	0	R/W	Frame Transmission End Enable 0: Disables a frame transmission end interrupt. 1: Enables a frame transmission end interrupt.
22	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
21	TFSERRE	0	R/W	Transmit Frame Synchronization Error Enable 0: Disables interrupts due to transmit frame synchronization errors. 1: Enables interrupts due to transmit frame synchronization errors.

Bit	Bit Name	Initial Value	R/W	Descriptions
20	TFOVFE	0	R/W	Transmit FIFO Overflow Enable 0: Disables interrupts due to transmit FIFO overflow. 1: Enables interrupts due to transmit FIFO overflow.
19	TFUDFE	0	R/W	Transmit FIFO Underflow Enable 0: Disables interrupts due to transmit FIFO underflow. 1: Enables interrupts due to transmit FIFO underflow.
18 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15	RDMAE	0	R/W	Receive Data DMA Transfer Request Enable Specifies whether to send an interrupt as an interrupt request to the CPU or a transfer request to the DMAC. The RDREQE bit can be set as the request source. 0: Sends an interrupt request to the CPU. 1: Sends a DMA transfer request to the DMAC.
14	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
13	RFFULE	0	R/W	Receive FIFO Full Enable 0: Disables interrupts due to receive FIFO full. 1: Enables interrupts due to receive FIFO full.
12	RDREQE	0	R/W	Receive Data Transfer Request Enable 0: Disables interrupts due to receive data transfer requests. 1: Enables interrupts due to receive data transfer requests.
11 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7	REOFE	0	R/W	Frame Reception End Enable 0: Disables a frame reception end interrupt. 1: Enables a frame reception end interrupt.
6	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
5	RFSEERE	0	R/W	Receive Frame Synchronization Error Enable 0: Disables interrupts due to receive frame synchronization errors. 1: Enables interrupts due to receive frame synchronization errors.
4	RFUDFE	0	R/W	Receive FIFO Underflow Enable 0: Disables interrupts due to receive FIFO underflow. 1: Enables interrupts due to receive FIFO underflow.
3	RFOVFE	0	R/W	Receive FIFO Overflow Enable 0: Disables interrupts due to receive FIFO overflow. 1: Enables interrupts due to receive FIFO overflow.
2 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

## 46.3.13 MSIOF FIFO Control Register (SIFCTR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SIFCTR is a 32-bit readable/writable register that indicates the area available for the transmit/receive FIFO transfer.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TFWM[2:0]			—	—	TFUA[6:0]						—	—	—	—	
Initial	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RFWM[2:0]			RFUA[8:0]								—	—	—	—	
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 29	TFWM[2:0]	000	R/W	<p>Transmit FIFO Watermark</p> <p>A transfer request of the transmit FIFO is issued by the TDREQE bit in SIIER.</p> <p>The transmit FIFO always operates as a 64-stage FIFO regardless of the setting of these bits.</p> <p>000: Issues a transfer request when 64 stages of the transmit FIFO are empty.</p> <p>001: Issues a transfer request when 32 or more stages of the transmit FIFO are empty.</p> <p>010: Issues a transfer request when 24 or more stages of the transmit FIFO are empty.</p> <p>011: Issues a transfer request when 16 or more stages of the transmit FIFO are empty.</p> <p>100: Issues a transfer request when 12 or more stages of the transmit FIFO are empty.</p> <p>101: Issues a transfer request when 8 or more stages of the transmit FIFO are empty.</p> <p>110: Issues a transfer request when 4 or more stages of the transmit FIFO are empty.</p> <p>111: Issues a transfer request when 1 or more stages of transmit FIFO are empty.</p>
28, 27	—	All 0	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>
26 to 20	TFUA[6:0]	H'40	R	<p>Transmit FIFO Usable Area</p> <p>Indicate the number of words that can be transferred by the CPU or DMAC as B'0000000 (full) to B'1000000 (empty).</p>
19 to 16	—	All 0	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>

Bit	Bit Name	Initial Value	R/W	Descriptions
15 to 13	RFWM[2:0]	000	R/W	<p>Receive FIFO Watermark</p> <p>A transfer request of the receive FIFO is issued by the RDREQE bit in SIIER.</p> <p>The receive FIFO always operates as a 128-stage FIFO regardless of the setting of these bits.</p> <p>000: Issues a transfer request when 1 stage or more of the receive FIFO are valid.</p> <p>001: Issues a transfer request when 4 or more stages of the receive FIFO are valid.</p> <p>010: Issues a transfer request when 8 or more stages of the receive FIFO are valid.</p> <p>011: Issues a transfer request when 16 or more stages of the receive FIFO are valid.</p> <p>100: Issues a transfer request when 32 or more stages of the receive FIFO are valid.</p> <p>101: Issues a transfer request when 64 or more stages of the receive FIFO are valid.</p> <p>110: Issues a transfer request when 128 stages of the receive FIFO are valid.</p> <p>111: The setting of 111 is prohibited.</p>
12 to 4	RFUA[8:0]	All 0	R	<p>Receive FIFO Usable Area</p> <p>Indicate the number of words that can be transferred by the CPU or DMAC as B'0000000 (empty) to B'1000000 (full).</p>
3 to 0	—	All 0	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>

## 46.4 Operation

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

### 46.4.1 Operating Mode

#### (1) Common transmit/receive mode

Common clock and frame synchronization signals are used for transmission and reception.

Master mode: MSIOF\_SCK and MSIOF\_SYNC are output.

Slave mode: MSIOF\_SCK and MSIOF\_SYNC are input.

### 46.4.2 Serial Clocks

#### (1) Clock output in master mode

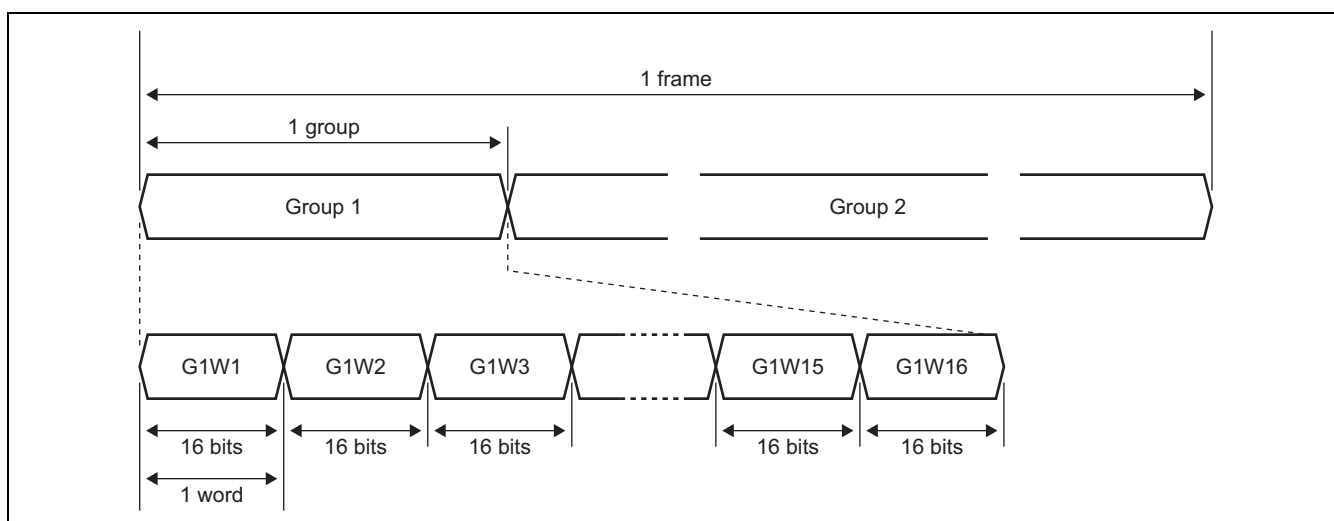
In master mode, the baud rate generator is used to generate the serial clock. The division ratio is from 1/1 to 1/1024.

#### (2) Clock input in slave mode

In slave mode, the clock input for transmission and reception is used as the serial clock.

#### (3) Multiple channel function

This module provides the multiple channel function as shown in Figure 46.2.



**Figure 46.2 Multiple Channel Structure**

The following conditions can be specified for the multiple channel function.

- Up to 2 groups in one frame
- Up to 64 words in one group
- 8, 16, 24, or 32 bits one word

### 46.4.3 Serial Timing

#### (1) MSIOF\_SYNC

The MSIOF\_SYNC is a frame synchronization signal. The following four modes are available.

- Frame start synchronization pulse: 1-bit-width pulse indicating the start of a frame
- Level/SPI: Level signal asserted during frame transmission
- L/R: 1/2-frame-width pulse indicating the first-half groups in a high level and the last-half groups in a low level

Figures 46.3 to 46.5 show the synchronization timing in these modes using the MSIOF\_SYNC signal.

#### (a) Frame start synchronization pulse

The rising edge of the synchronization pulse indicates the start of a frame.

The delay between the rising edge of the synchronization signal and the start of data transmission or reception can be specified with the DTDL bits. The width of the synchronization pulse can be extended through the SYNCDL bit setting.

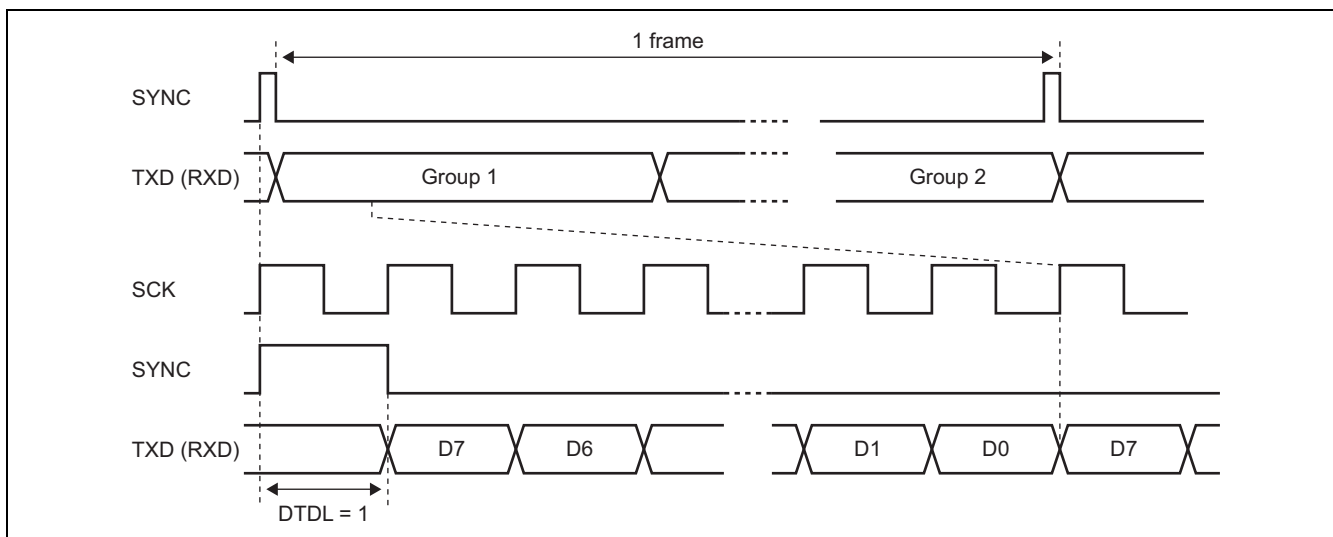
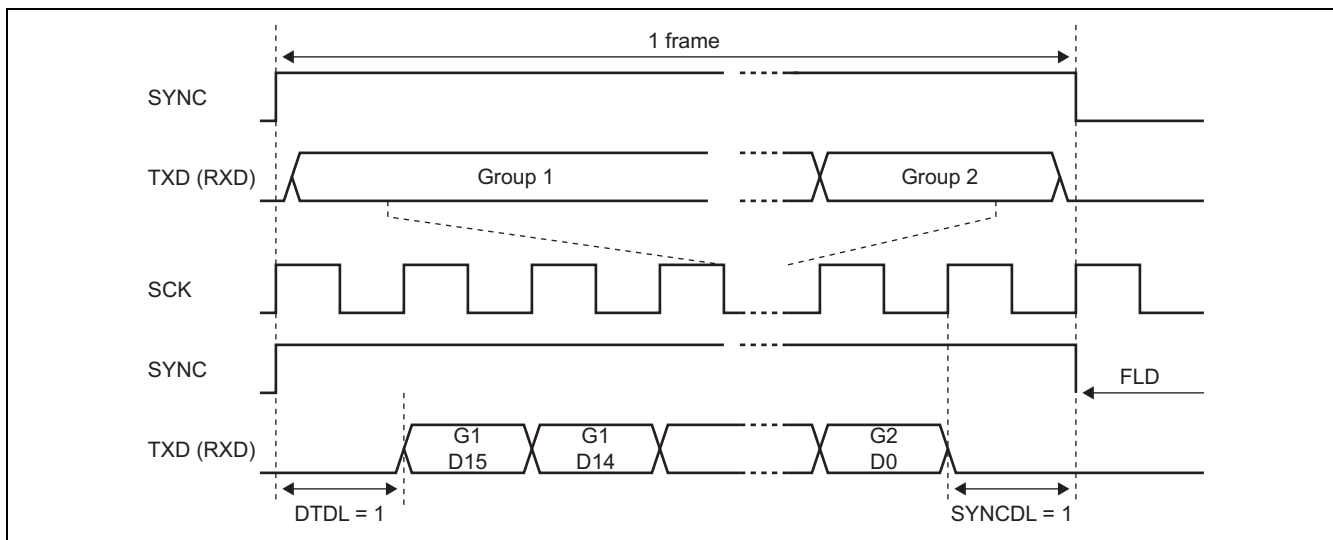


Figure 46.3 Synchronization Timing in Start Frame Synchronization Pulse Mode

**(b) Level synchronization**

The synchronization signal is driven high for the frame length.

The delay between the rising edge of the synchronization signal and the start of transmission or reception can be specified with the DTDL bits and the delay between the end of transmission or reception and the falling edge of the synchronization signal can be specified with the SYNCNL bits (DTDL = 0 to 2 and SYNCNL = 0 to 3). This mode is available for the SPI master or slave operation.

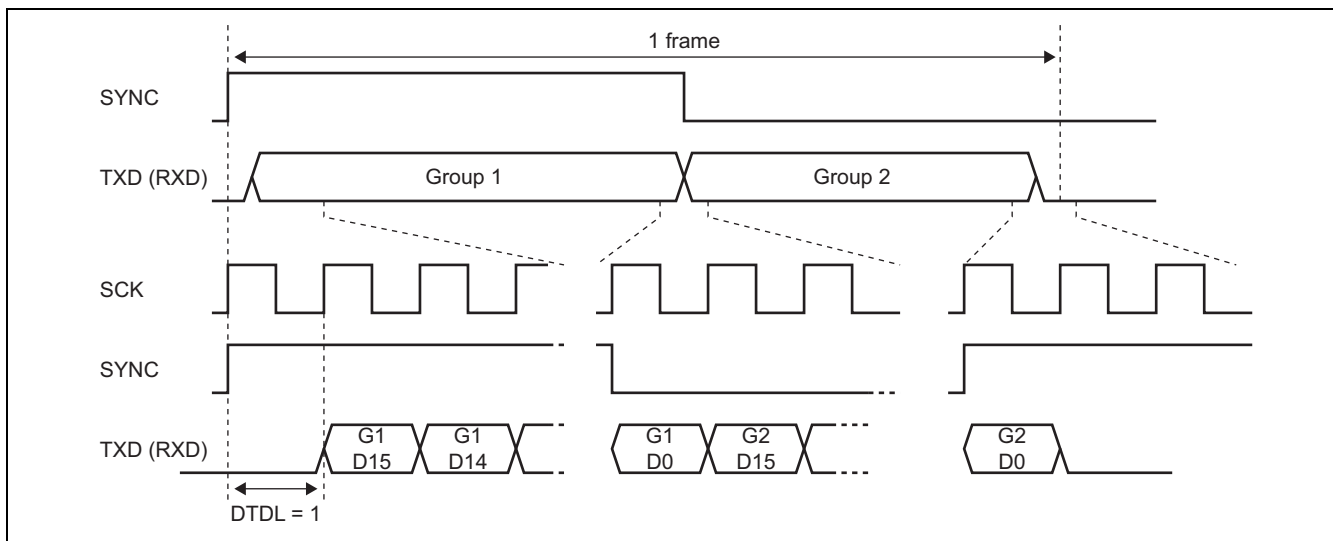


**Figure 46.4 Synchronization Timing in Level Synchronization Mode**

**(c) L/R synchronization**

A high level in the synchronization signal indicates the first-half groups and a low level indicates the last-half groups.

The delay between the rising or falling edge of the synchronization signal and the start of transmission or reception can be specified with the DTDL bits.



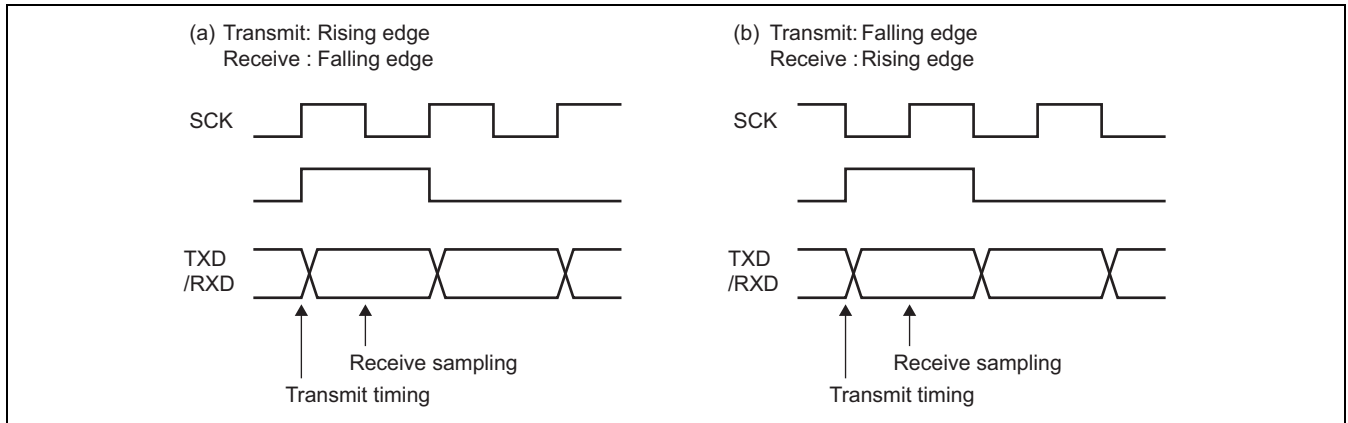
**Figure 46.5 Synchronization Timing in L/R Synchronization Mode**



**(2) Transmit/receive timing**

The timing of MSIOF\_TXD transmission relative to MSIOF\_SCK and of MSIOF\_RXD can be specified as sampling on either edge, as listed below. The respective settings are made in TEDG and REDG bits of SICTR.

- Falling-edge sampling
- Rising-edge sampling



**Figure 46.6 Transmit/Receive Timing.**

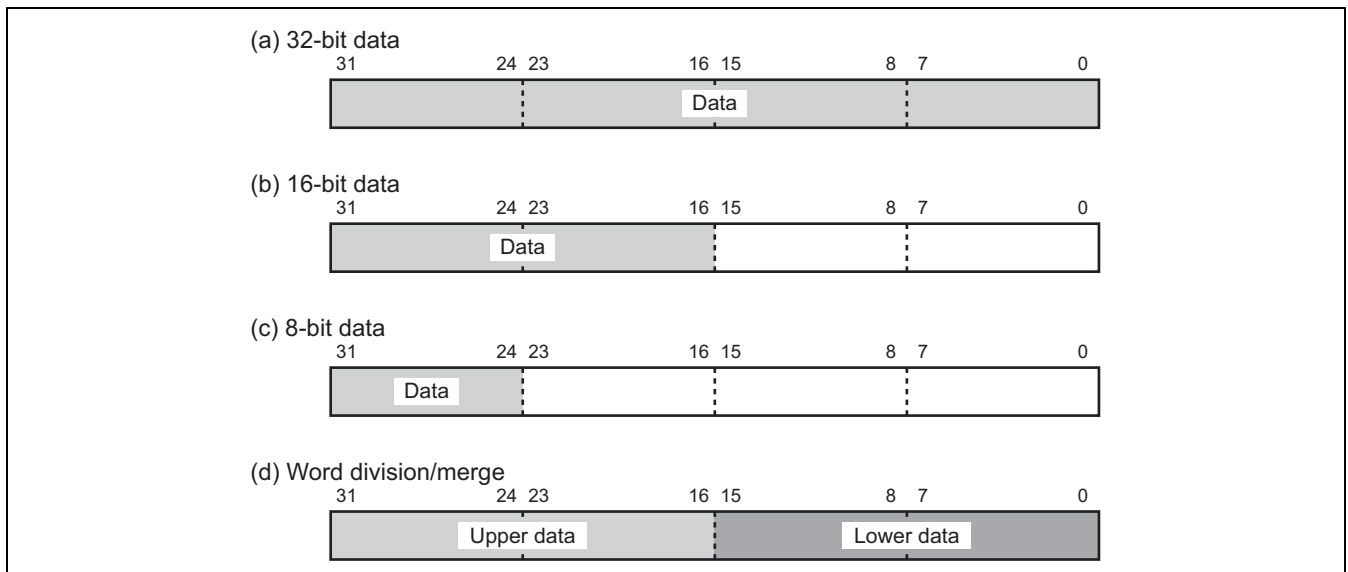
**46.4.4 Transfer Data Allocation to Registers**

**(1) Transmit/receive data**

Transmit/receive data (FIFO data and control data) should be written to or read from the following registers.

- Transmit FIFO data writing: SITFDR (32-bit access)
- Receive FIFO data reading: SIRFDR (32-bit access)

Figure 46.7 shows the bit alignment of these registers.



**Figure 46.7 Transmit/Receive Data Bit Alignment**

### 46.4.5 FIFO

#### (1) Overview

The transmit and receive FIFOs of the MSIOF have the following features.

- 32 bits × 64 stages for transmission and 32 bits × 128 stages for reception
- The FIFO pointer is updated in one read or write cycle regardless of the access size of the CPU or DMAC. (One access cannot be divided into multiple accesses.)


#### (2) Transfer request

A request for FIFO data transfer can be issued to the CPU or DMAC as the following interrupt sources.


- FIFO transmit request: TDREQ (interrupt source for transmission)
- FIFO receive request: RDREQ (interrupt source for reception)

The conditions for requesting FIFO data transfer can be specified separately for transmission and reception. The conditions for the transmit FIFO and receive FIFO are specified in the TFWM[2:0] bits and RFWM[2:0] bits in SIFCTR, respectively.

**Table 46.5 Condition for Issuing Transmit Request**

TFWM[2:0]	Number of Requested Stages	Condition for Transmit Request	Areas Used
000	1	64 stages of empty area	Smallest
001	32	32 or more stages of empty area	
010	40	24 or more stages of empty area	
011	48	16 or more stages of empty area	
100	52	12 or more stages of empty area	
101	56	8 or more stages of empty area	
110	60	4 or more stages of empty area	
111	64	1 or more stages of empty area	

**Table 46.6 Condition for Issuing Receive Request**

RFWM[2:0]	Number of Requested Stages	Condition for Receive Request	Areas Used
000	1	1 or more stages of valid data	Smallest
001	4	4 or more stages of valid data	
010	8	8 or more stages of valid data	
011	16	16 or more stages of valid data	
100	32	32 or more stages of valid data	
101	64	64 or more stages of valid data	
110	128	128 stages of valid data	
111	128	128 stages of valid data	

The maximum FIFO stages are always available even if the data area or empty area exceeds the size specified for the transfer condition. Accordingly, an overflow error or an underflow error occurs if the data area or empty area exceeds the maximum number of FIFO stages.

The FIFO transfer request is canceled when the specified condition is not satisfied even if the FIFO does not become empty or full.

**(3) Number of FIFOs**

The number of transmit and receive FIFO stages used are indicated by the following registers.

- Transmit FIFO: The number of empty FIFO stages is indicated by the TFUA[6:0] bits in SIFCTR.
- Receive FIFO: The number of valid data stages is indicated by the RFUA[8:0] bits in SIFCTR.

These registers show the number of data stages that can be transferred by the CPU. DMA transfer should be set the number of stage 1.

**46.4.6 Transmit and Receive Procedures**

**(1) Transmission in master mode**

Figure 46.8 shows an example of settings and operation for transmission in master mode.

No.	Operating flow	Description	Operation
1	SITMDR1/2/3 SITSCR SIFCTR SIIER setting	Operating mode Clock setting FIFO water mark Setting interrupt/DMA enable	
2	SICTR Set SICTR.TSCKE to 1	Transmission rate setting Baud rate generator starting	Output serial clock
3		Read SICTR.TSCKE = 1	
4	SITFDR SITMDR1/2 setting	Write transmission data to FIFO	
5	Set SICTR.TXE to 1	Transmission enable	
6		Read SICTR.TXE = 1	
7	Set SICTR.TFSE to 1	Starting MSIOF_SYNC output	
8		Read SICTR.TFSE = 1	
9	Starting transmission		Data transmission
10			Generating interrupt/DMA request
11	Write transmission data to FIFO		
12			
13	Set SICTR.TFSE to 0	Frame sync disable	
14		Read SICTR.TFSE = 0	
15	Set SICTR.TXE to 0	Transmission disable	
16		Read SICTR.TXE = 0	

**Figure 46.8 Example of Transmit Procedure in Master Mode**

(2) Reception in master mode (with SITMDR1.PCON = 1)

Figure 46.9 shows an example of settings and operation for reception in master mode with SITMDR1.PCON = 1.

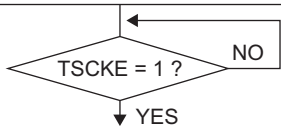
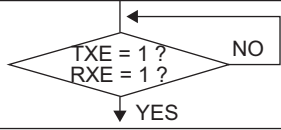
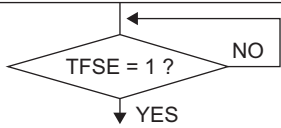
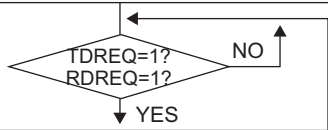
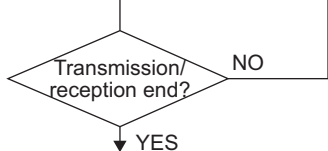
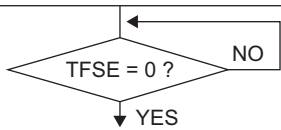
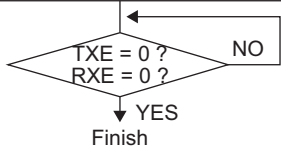
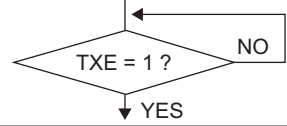
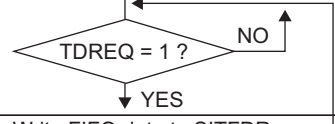
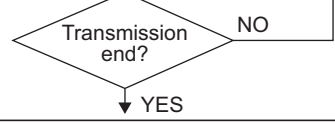
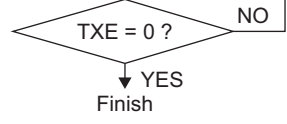
No.	Operating flow	Description	Operation
1	SIRMDR1/2/3 SITMDR1/2/3 SITSCR SIFCTR SIIER setting	Operating mode Operating mode (for SPI dummy transmission) Serial clock FIFO water mark Interrupt/DMA setting	
2	SICTR Set SICTR.TSCKE to 1	Baud rate setting Baud rate generator starting	Output serial clock
3		Read SICTR.TSCKE = 1	
4	SITFDR  SITMDR1/2 setting	Write dummy transmission data to SITFDR The number of dummy data should equal the number of reception data.	
5	Set SICTR.TXE to 1 Set SICTR.RXE to 1	Transmission enable Reception enable	
6		Read SICTR.TXE = 1 Read SICTR.RXE = 1	
7	Set SICTR.TFSE to 1	Frame sync enable	Output MSIOF_SYNC
8		Read SICTR.TFSE = 1	
9	Synchronizing with MSIOF_SYNC (1) Transmission FIFO dummy data (2) Reception data		Transmission and reception
10			Generating interrupt/DMA request
11	Write dummy data to FIFO Read fifo data from SIRFDR	Transmission dummy data Reception data reading	
12			
13	Set SICTR.TFSE to 0	Disable frame sync enable	
14		Read SICTR.TFSE = 0	
15	Set SICTR.TXE and SICTR.RXE to 0	Disable transmission enable and reception enable	
16		Read SICTR.TXE = 0 Read SICTR.RXE = 0	

Figure 46.9 Example of Receive Procedure in Master Mode (SITMDR1.PCON = 1)

**(3) Transmission in slave mode**

Figure 46.10 shows an example of settings and operation for transmission in slave mode.

No.	Operating flow	Description	Operation
1	Master device setting	Depend on master device	Signal polarity
2	SITMDR1/2/3 SIFCTR SIIER setting	Operating mode FIFO water mark Interrupt/DMA enable	
3	SITFDR SITMDR1/2 setting	Transmission data setting	
4	Set SICTR.TXE to 1	Setting transmission enable	
5		Read SICTR.TXE = 1	
6	Data transmission synchronize with MSIOF_SYNC		Data transmission
7			Generating interrupt/DMA request
8	Write FIFO data to SITFDR	Data transmission	
9			
10	Set SICTR.TXE to 0	Transmission disable	
11		Read SICTR.TXE = 0	

**Figure 46.10 Example of Transmit Procedure in Slave Mode**

**(4) Reception in slave mode**

Figure 46.11 shows an example of settings and operation for reception in slave mode.

No.	Operating flow	Description	Operation
1	Master device setting	Depend on master device	Signal polarity
2	SIRMDR1/2/3 SIFCTR SIIER setting	Operating mode FIFO water mark Interrupt/DMA enable	
3	Set SICTR.RXE to 1	Setting receive enable	
4		Read SICTR.RXE = 1	
5	Data reception		Receive data
6			Generating interrupt/DMA request
7	Read SIRFDR	Data read from FIFO	
8			
9	Set SICTR.RXE to 0	Reception disable	
10		Read SICTR.RXE = 0	

**Figure 46.11 Example of Receive Procedure in Slave Mode**

**(5) Reset**

After a power-on reset is applied, module stop state is canceled, or a reset signal is asserted through the TXRST or RXRST setting in SICTR, it takes about 20 cycles of module clock to complete the internal reset of the module. During a period from the beginning of reset until the TXRST or RXRST value is read as 0, do not modify the control register or access the FIFOs.

The MSIOF can separately reset the transmit and receive units by setting the following bits to 1.

- Transmit reset: TXRST bit in SICTR
- Receive reset: RXRST bit in SICTR

**Table 46.7 Transmit and Receive Reset**

Type	Objects Initialized
Transmit reset	SITFDR (Transmit FIFO write pointer) TDREQ bit in SISTR TXE bit in SICTR
Receive reset	SIRFDR (Receive FIFO read pointer) RDREQ bit in SISTR RXE bit in SICTR

**(6) Initial operating mode**

After a power-on reset, both transmit and receive units are initialized to master mode (0 is output through MSIOF\_SCK and MSIOF\_SYNC). When using slave mode, keep the connected device outputting 0 until the operating mode setting is completed.



### 46.4.7 Interrupts

The MSIOF has one type of interrupt.

#### (1) Interrupt sources

Interrupts can be generated by several sources. Each source is shown as an MSIOF status in SISTR. Table 46.8 lists the MSIOF interrupt sources.

**Table 46.8 MSIOF Interrupt Sources**

No.	Classification	Bit Name	Function Name	Description
1	Transmission	TDREQ	Transmit FIFO transfer request	The transmit FIFO has empty space of specified size or more.
2		TFEMP	Transmit FIFO empty	The transmit FIFO is empty.
3		TEOF	Frame transmission end	Transmission of data with a length of one frame is completed.
4	Reception	RDREQ	Receive FIFO transfer request	The receive FIFO stores data of specified size or more.
5		RFFUL	Receive FIFO full	The receive FIFO is full.
6		REOF	Frame reception end	Reception of data with a length of one frame is completed.
7	Error	TFUDF	Transmit FIFO underflow	Serial data transmit timing has arrived while the transmit FIFO is empty.
8		TFOVF	Transmit FIFO overflow	The transmit FIFO is written to while it is full.
9		RFOVF	Receive FIFO overflow	Serial data is received while the receive FIFO is full.
10		RFUDF	Receive FIFO underflow	The receive FIFO is read while the receive FIFO is empty.
11		TFSERR	Transmit FS error	A transmit frame synchronization signal is input before the specified number of bits has been reached (in slave mode).
12		RFSERR	Receive FS error	A receive frame synchronization signal is input before the specified number of bits has been reached (in slave mode).

Whether an interrupt is issued from an interrupt source is determined by the SIIER settings. If an interrupt source bit is set to 1 and the corresponding bit in SIIER is set to 1, an MSIOF interrupt is issued.

#### (2) TDREQ and RDREQ

The transmit FIFO transfer request (TDREQ) and receive FIFO transfer request (RDREQ) are signals indicating the state. If the state changes after TDREQ or RDREQ is set, it is automatically cleared by the MSIOF.

When the DMA transfer is used, a DMA transfer request signal is pulled low for one cycle at the end of DMA transfer.

**(3) Processing when errors occur**

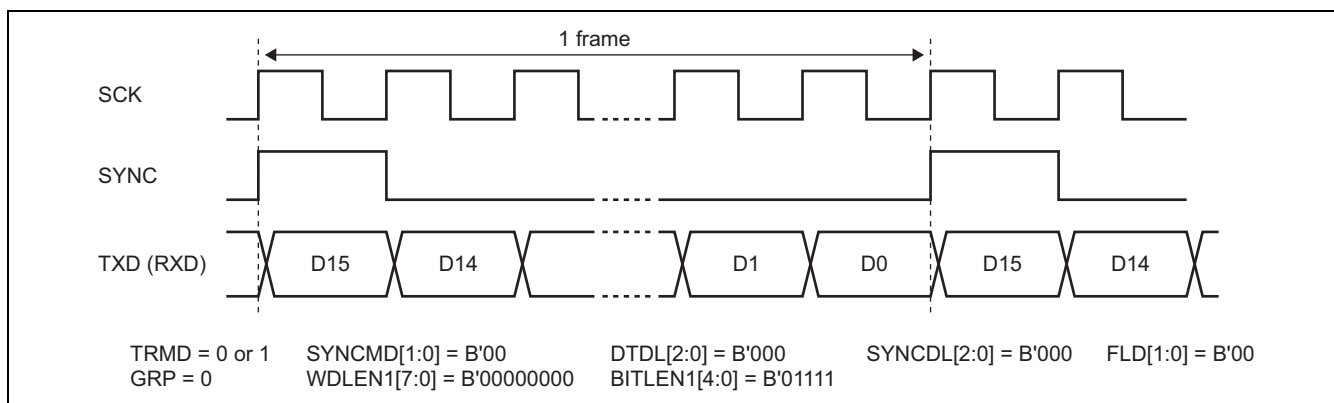
- Transmit FIFO underflow (TFUDF)  
The value specified with TXDIZ in SICTR is output.
- Transmit FIFO overflow (TFOVF)  
The contents of the transmit FIFO are protected, and the write operation causing the overflow is ignored.
- Receive FIFO overflow (RFOVF)  
Data causing the overflow is discarded and lost.
- Receive FIFO underflow (RFUDF)  
An undefined value is output on the bus.
- Transmit FS error (TFSERR)  
The internal counter is reset according to the synchronization signal in which an error occurs.
- Receive FS error (RFSERR)  
The internal counter is reset according to the synchronization signal in which an error occurs.

**46.4.8 Transmit and Receive Timing**

Examples of the MSIOF serial transmission and reception are shown in Figures 46.12 and 46.13.

**(1) 16-bit synchronization pulse**

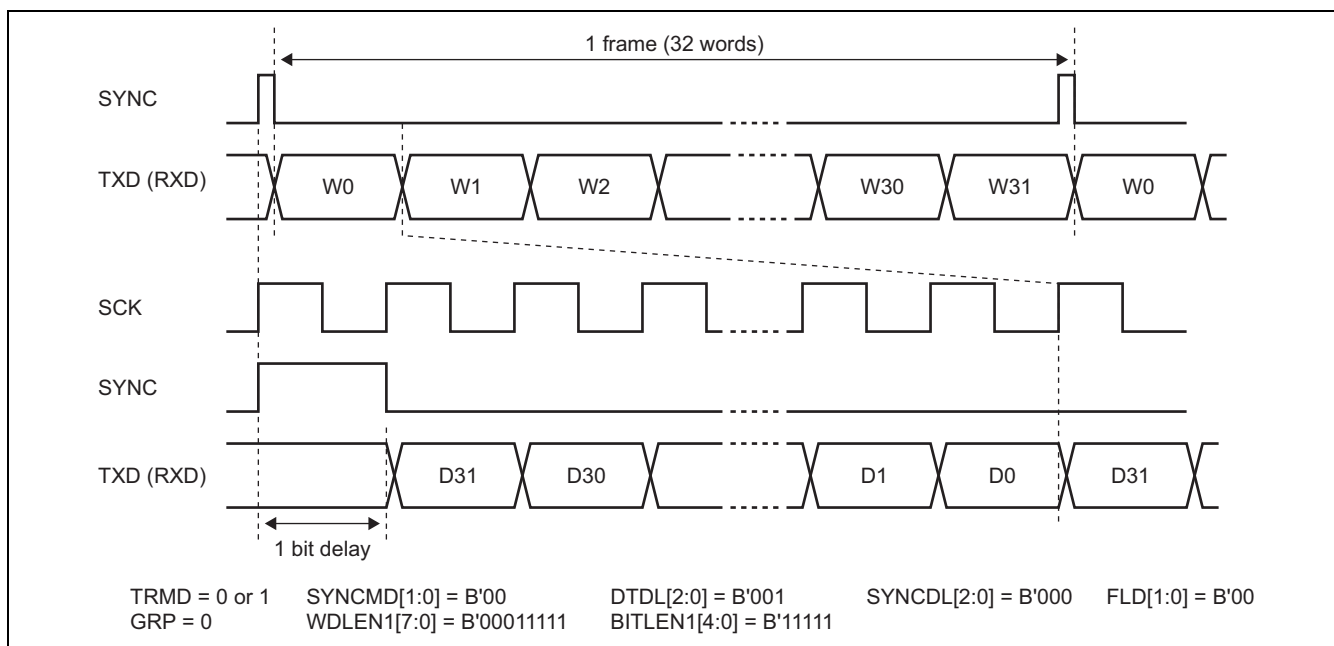
Synchronization pulse method, one group, one word, 16 bits in a word, no bit delay



**Figure 46.12 Transmit and Receive Timing (16 Bits)**

**(2) 32-bit synchronization pulse**

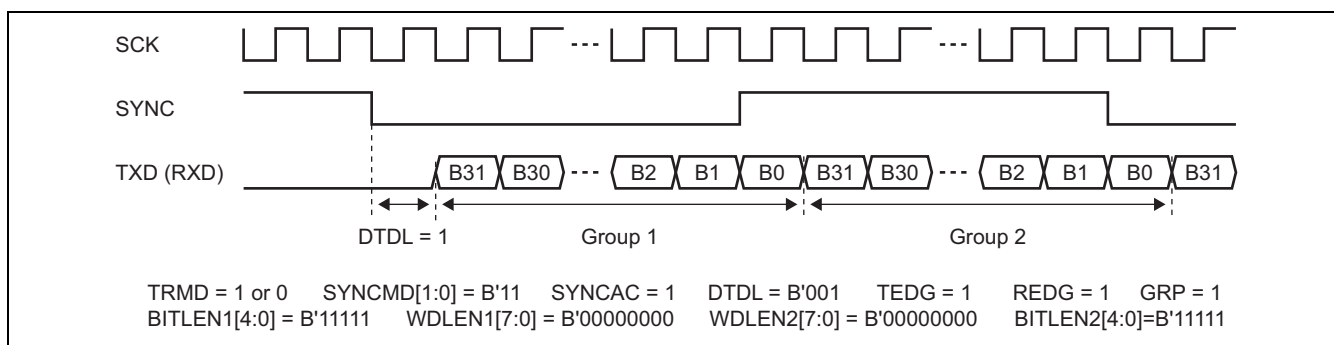
Synchronization pulse method, one group, 32 words, 32 bits in a word, 1-bit delay



**Figure 46.13 Transmit and Receive Timing (32 Bits)**

**(3) 32-bit iis transmission**

L/R mode, 2 groups, 1 word for each group, 32-bit word for each group, 1-bit delay



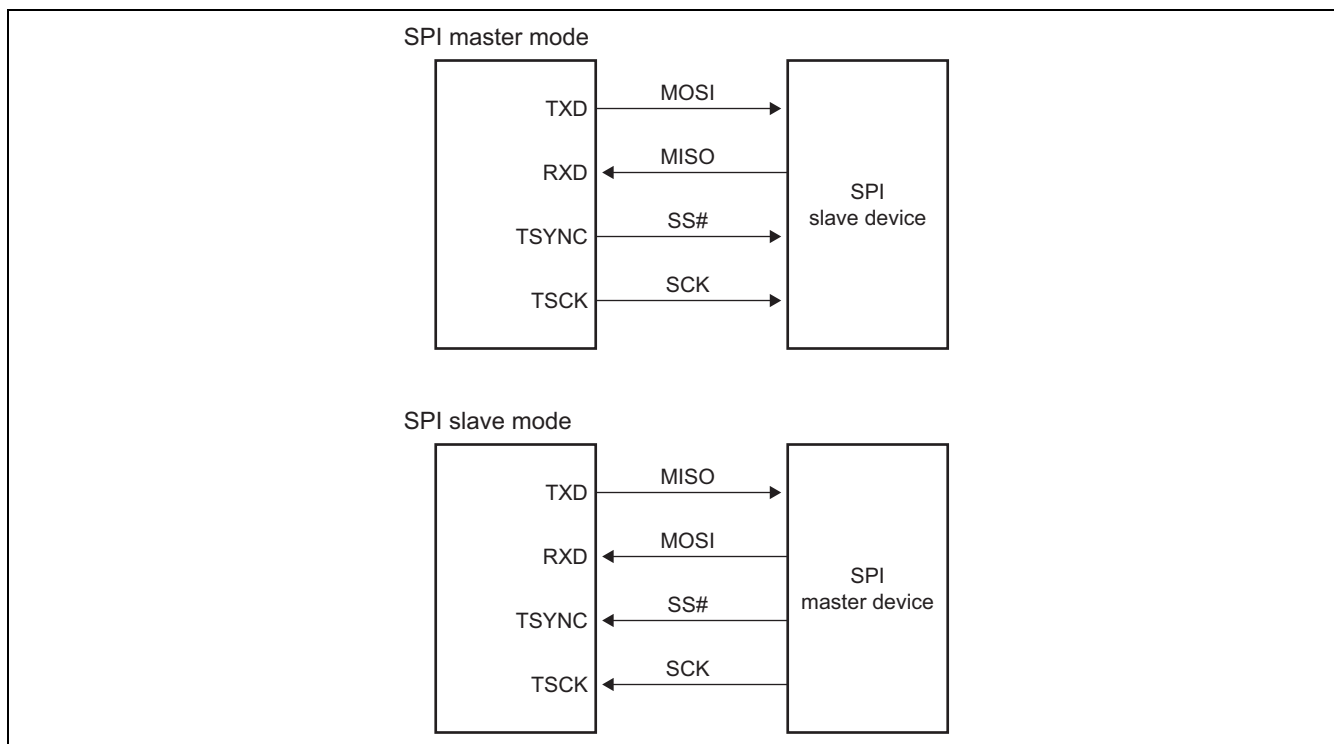
**Figure 46.14 Transmit Timing (24-Bit IIS)**

### 46.4.9 SPI

With the appropriate register settings, the MSIOF can be used as an SPI device.

#### (1) Example of SPI device connection

Figure 46.15 shows an example of connection with an SPI device.



**Figure 46.15 Example of SPI Device Connection**

(2) SPI serial clock timing

Figures 46.16 and 46.17 show the data and clock timing in SPI mode. As shown in the figures, four types of serial transfer formats can be used.

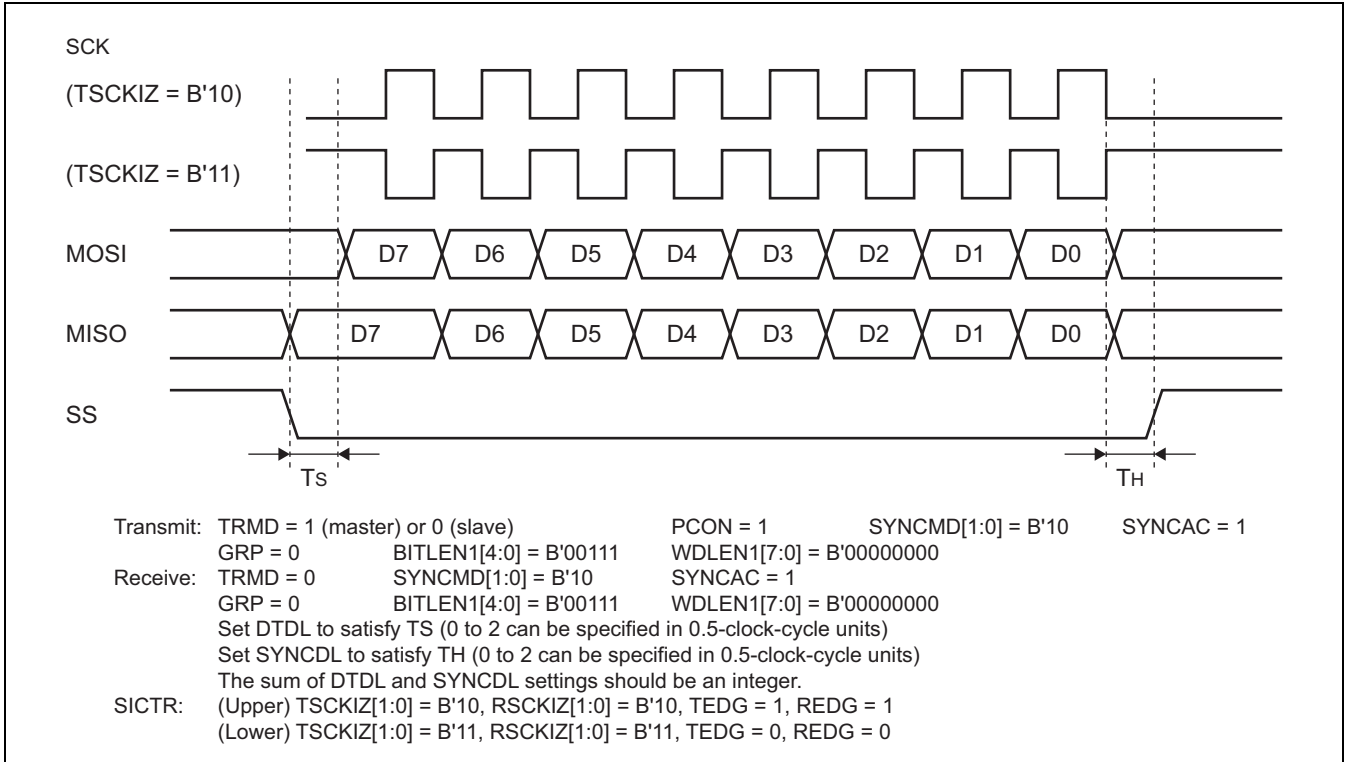


Figure 46.16 SPI Clock and Data Timing 1

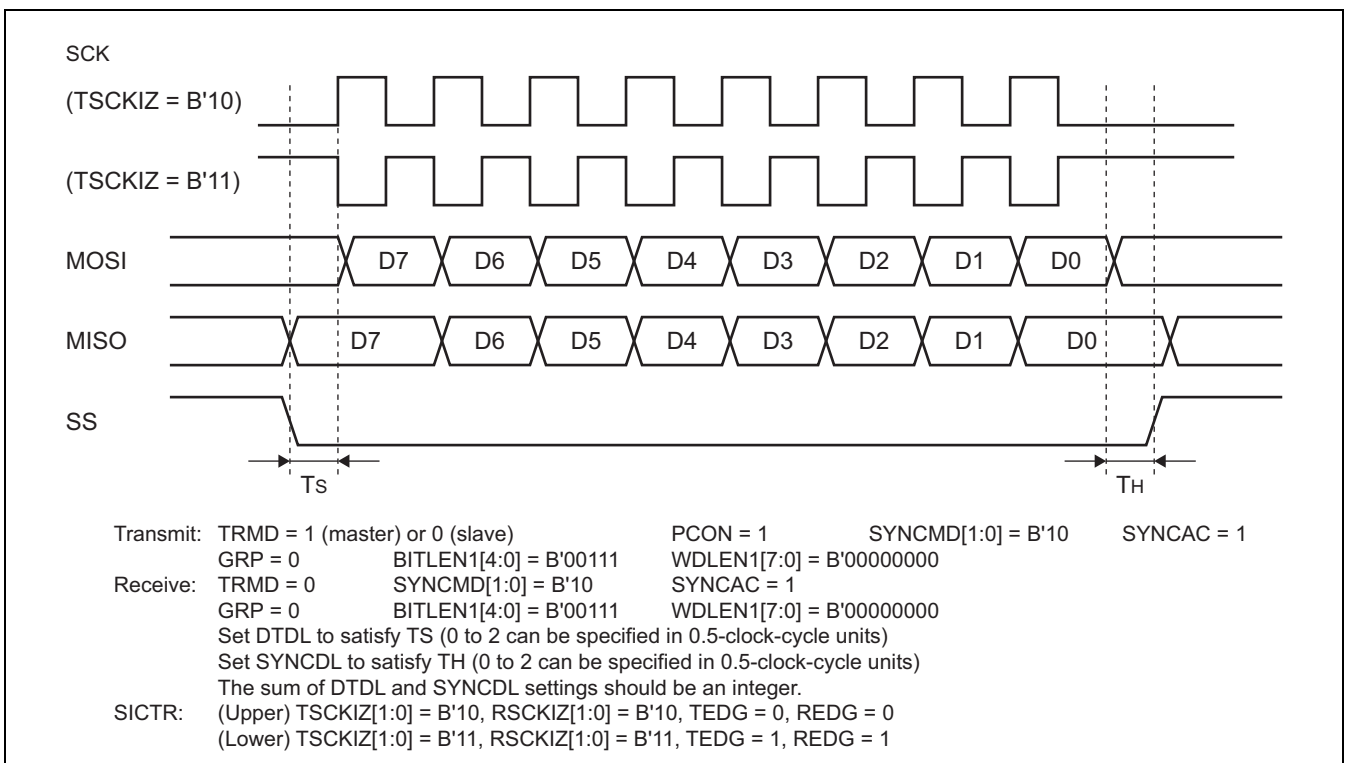


Figure 46.17 SPI Clock and Data Timing 2

#### 46.4.10 Notes for Using SPI Mode

- For SPI master mode operation, set the FLD bits in SITMDR1 for at least 3 cycles of module clock.
- For SPI slave mode operation, set the frame synchronization signal interval to at least 4 cycles of module clock.
- For SPI slave mode operation, the setting for data delay should be always set to 0.
- For SPI slave mode operation, TXDIZ bits work on SS signal invalid state.

#### 46.4.11 SPI Mode Transfer Rate Limitation of RZ/G1H

For channels 0, 1 and 3 of the RZ/G1H, maximum transfer rate is limited to 13 MHz. Please specify SITSCR to make the bit rate equal to or less than 13 MHz.

#### 46.4.12 Limitation of SPI Mode

When the MSIOF operates with all of the following condition 1 to 3, the MSIOF in SPI slave mode cannot start the next transmission. The MSIOF cannot support SPI mode under following condition.

- Condition
  - 1) MSIOF is in SPI slave mode (SITMDR1.TRMD=0, SITMDR1.SYNCMD[1:0]=10)
  - 2) SYNC (CS) signal is being asserted from master
  - 3) TXE or RXE in SICTR is set to 1 during SYNC (CS) is asserted

This limitation means the MSIOF cannot respond to the SYNC (CS).

It is necessary to control the MSIOF enabling timing by the master and system.

[Workaround]

Use master mode for SPI.

If use slave mode for SPI, consider following alternative.

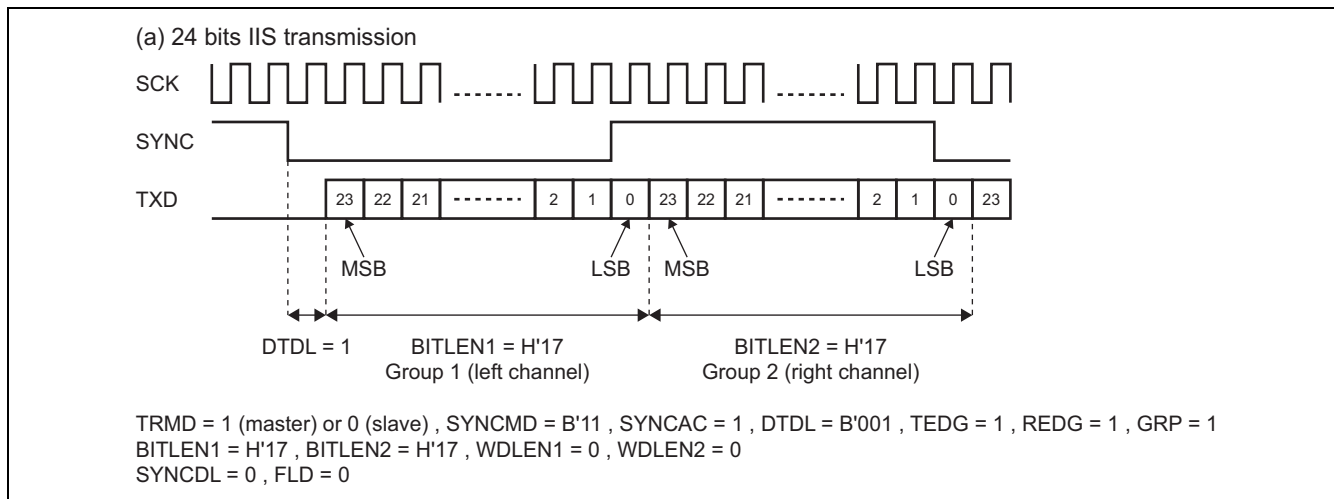
[Alternative]

If the master device can support handshaking, use the handshaking transmission.

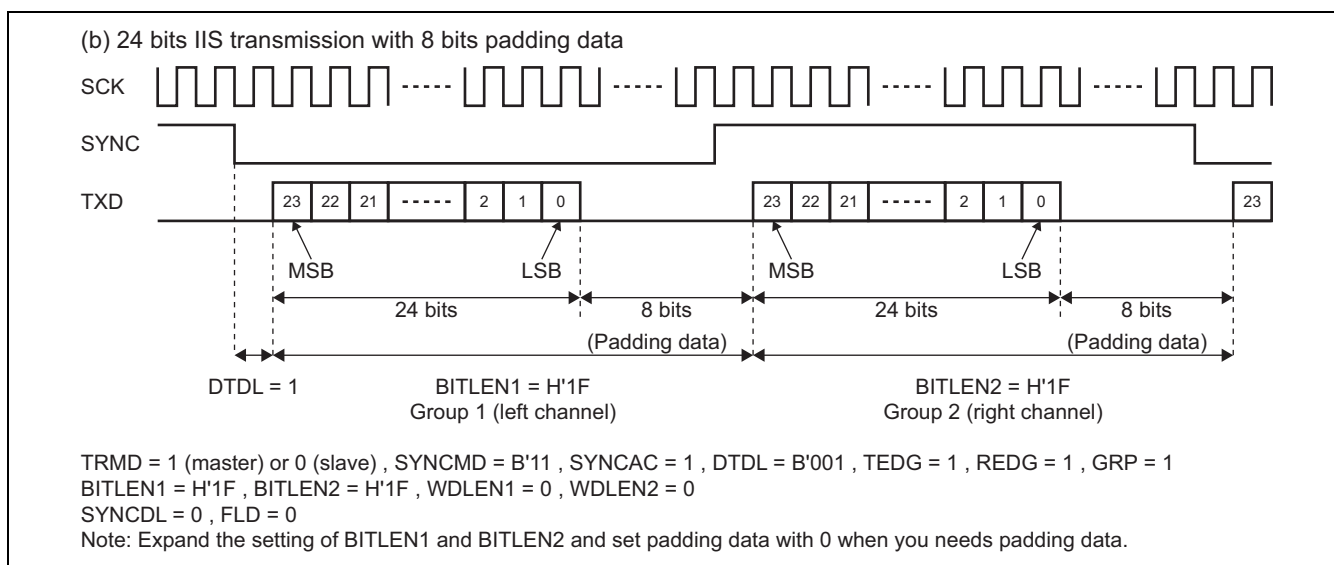
For the MSIOF in SPI slave mode, use with the GPIO output for SPI handshaking; the system operation must be tested and evaluated thoroughly by user.

**46.4.13 IIS**

This module can support IIS format with following setting which is shown in Figures 46.18 and 46.19. BITLEN1 and BITLEN2 bits will change by usage.



**Figure 46.18 24 Bits IIS Transmission**



**Figure 46.19 24 Bits IIS Transmission with 8 Bits Padding Data**

## 47. Quad Serial Peripheral Interface

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

### 47.1 Overview

The RZ/G series products have one channel of QSPI. Features and functions of each product are basically the same, however, read value of WSWAP bit of SPCR register and BSWAP bit of SPCR register for RZ/G1H and RZ/G1M are always 0. See section 47.4.1.

### 47.2 Features

This module has the following features.

- Capable of serial communications through single-/dual-/quad-SPI operation
  - Single-SPI operation
    - Use of MOSI (master out–slave in), MISO (master in–slave out), SSL (slave select), and SPCLK (SPI clock) signals allows for serial access (four-wire method).
    - Single-direction MOSI and MISO pins.
    - Only master mode is available.
    - SSL and SPCLK serve as output pins.
  - Dual-SPI operation
    - Use of IO1, IO0, SSL, and SPCLK signals allows for serial access (four-wire method).
    - Bidirectional IO1 and IO0 pins.
    - Only master mode is available.
  - Quad-SPI operation
    - Use of IO3 to IO0, SSL, and SPCLK signals allow for serial access (six-wire method).
    - Bidirectional IO3 to IO0 pins.
    - Only master mode is available.
- Transfer data length
  - Transfer data length is selectable from 8 bits to 128 Gbits in single-SPI master mode or dual-/quad-SPI modes.
  - Data is continuously transferred one through 4,294,967,296 times in 8-, 16-, or 32-bit units.
- Bit rate
  - SPCLK is generated by the on-chip baud rate generator, by dividing QSPI $\phi$  with division rate 1 to 4080 in master mode.
  - (SPCLK can be generated by dividing QSPI $\phi$  by the on-chip baud rate generator.)
- Buffer configuration
  - 8 bits  $\times$  32 buffers for transmission and 8 bits  $\times$  32 buffers for reception
- Shift registers
  - 32 bits each for transmission and reception
- SSL pin control function
  - Master mode: Controllable delay from SSL output assertion to SPCLK operation (clock delay)
    - Range: 0 to 8 SPCLK cycles (set in one SPCLK-cycle units)
    - Controllable delay from SPCLK stoppage to SSL output negation (SSL negation delay)
      - Range: 0 to 8 SPCLK cycles (set in one SPCLK-cycle units)
      - Controllable wait for next-access SSL output assertion (next-access delay)
        - Range: 0 to 8 SPCLK cycles (set in one SPCLK-cycle units)
  - Capable of holding SSL output value from transfer end to next access
  - Function for changing SSL polarity



- Master transfer control

A transfer of up to four commands can be executed sequentially in looped execution.

Single-SPI mode or dual-/quad-SPI write operation: A transfer can be started when data is written to the transmit buffer.

Dual-/quad-SPI read operation: A transfer can be started when the SPI function is enabled while there is enough space for receiving the specified length of data in the receive buffer.

IO3 to IO0 and MOSI output values can be specified during SSL negation.

IO3 and IO2 output values can be specified in single-/dual-SPI modes.

- Interrupt sources

Maskable interrupt sources:

Receive buffer full interrupt

Transmit buffer empty interrupt

Error interrupt (underrun error, overrun error, and mode fault error)

- Others

Provides loop back mode.

Provides a function for initializing this module.

Hereafter, the single-/dual-/quad-SPI master modes are collectively called the maser mode.

### 47.3 Input/Output Pins

Table 47.1 shows the pin configuration.

**Table 47.1 Pin Configuration**

Name	Pin Name	I/O	Function	RZ/G Series Products			
				RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Clock pin	SPCLK	I/O	Clock input/output	√	√	√	√
Master transmit data pin/data 0 pin* <sup>1</sup>	MOSI/IO0	I/O	Master transmit data/data 0	√	√	√	√
Slave transmit data pin/data 1 pin* <sup>1</sup>	MISO/IO1	I/O	Slave transmit data/data 1	√	√	√	√
Data 2 pin* <sup>2</sup>	IO2	I/O	Data 2	√	√	√	√
Data 3 pin* <sup>2</sup>	IO3	I/O	Data 3	√	√	√	√
Slave select pin	SSL	I/O	Slave selection	√	√	√	√

Notes: 1. In single-SPI mode, MOSI and MISO are enabled; IO0 and IO1 in dual-/quad-SPI modes.

2. In single-/dual-SPI modes, a fixed value according to register setting is output; IO2 and IO3 are output in quad-SPI mode.

## 47.4 Register Descriptions

Table 47.2 shows the register configuration. The base address is H'E6B1\_0000.

**Table 47.2 Register Configuration**

Register Name	Abbreviation	R/W	Initial Value	Address	Access Size	RZ/G Series Products			
						RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Control register	SPCR	R/W	H'00	H'00	8, 16, 32	√	√	√	√
Slave select polarity register	SSLP	R/W	H'00	H'01	8, 16, 32	√	√	√	√
Pin control register	SPPCR	R/W	H'06	H'02	8, 16, 32	√	√	√	√
Status register	SPSR	R/(W)*	H'60	H'03	8, 16, 32	√	√	√	√
Data register	SPDR	R/W	Undefined	H'04	8, 16, 32	√	√	√	√
Sequence control register	SPSCR	R/W	H'00	H'08	8, 16, 32	√	√	√	√
Sequence status register	SPSSR	R	H'00	H'09	8, 16, 32	√	√	√	√
Bit Rate register	SPBR	R/W	H'FF	H'0A	8, 16, 32	√	√	√	√
Data control register	SPDCR	R/W	H'00	H'0B	8, 16, 32	√	√	√	√
Clock delay register	SPCKD	R/W	H'00	H'0C	8, 16, 32	√	√	√	√
Slave select negation delay register	SSLND	R/W	H'00	H'0D	8, 16, 32	√	√	√	√
Next-access delay register	SPND	R/W	H'00	H'0E	8, 16, 32	√	√	√	√
Command register 0	SPCMD0	R/W	H'E001	H'10	16, 32	√	√	√	√
Command register 1	SPCMD1	R/W	H'E001	H'12	16, 32	√	√	√	√
Command register 2	SPCMD2	R/W	H'E001	H'14	16, 32	√	√	√	√
Command register 3	SPCMD3	R/W	H'E001	H'16	16, 32	√	√	√	√
Buffer control register	SPBFCR	R/W	H'00	H'18	8, 16, 32	√	√	√	√
Buffer data count register	SPBDCR	R/W	H'0000	H'1A	16, 32	√	√	√	√
Transfer data length multiplier setting register 0	SPBMUL0	R/W	H'00000001	H'1C	32	√	√	√	√
Transfer data length multiplier setting register 1	SPBMUL1	R/W	H'00000001	H'20	32	√	√	√	√
Transfer data length multiplier setting register 2	SPBMUL2	R/W	H'00000001	H'24	32	√	√	√	√
Transfer data length multiplier setting register 3	SPBMUL3	R/W	H'00000001	H'28	32	√	√	√	√

Note: \* Only 0 can be written to clear the flag.

### 47.4.1 Control Register (SPCR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SPCR sets the operating mode. If the master/slave mode select bit (MSTR) is modified while the SPI function enable bit (SPE) is set to 1 (that is, this module is enabled), the subsequent operation cannot be guaranteed.

Bit:	7	6	5	4	3	2	1	0
	SPRIE	SPE	SPTIE	SPEIE	MSTR	—	WSWA P	BSWA P
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7	SPRIE	0	R/W	<p>Receive Interrupt Enable</p> <p>Enables or disables generation of receive interrupt requests when the number of receive data units in the receive buffer is equal to or greater than the specified receive buffer data triggering number and the receive buffer full flag (SPRFF) in the status register (SPSR) is set to 1.</p> <p>0: Disables the generation of receive interrupt requests. 1: Enables the generation of receive interrupt requests.</p>
6	SPE	0	R/W	<p>SPI Function Enable</p> <p>Setting this bit to 1 enables the SPI module function. Setting this bit to 0 initializes a part of the module function.</p> <p>0: Disables the module function. 1: Enables the module function.</p>
5	SPTIE	0	R/W	<p>Transmit Interrupt Enable</p> <p>Enables or disables generation of transmit interrupt requests when the number of transmit data units in the transmit buffer is equal to or less than the specified transmit buffer data triggering number and the transmit buffer empty flag (SPTEF) in SPSR is set to 1.</p> <p>0: Disables the generation of transmit interrupt requests. 1: Enables the generation of transmit interrupt requests.</p>
4	SPEIE	0	R/W	<p>Error Interrupt Enable</p> <p>Enables or disables generation of error interrupt requests when an underrun error, an overrun error, or a mode fault error is detected and the corresponding flag in SPSR is set to 1.</p> <p>0: Disables the generation of error interrupt requests. 1: Enables the generation of error interrupt requests.</p> <p>Note: This setting is valid only in single-SPI slave mode.</p>

Bit	Bit Name	Initial Value	R/W	Description
3	MSTR	0	R/W	<p>Master/Slave Mode Select</p> <p>Selects the master or slave mode.</p> <p>This bit specifies the direction of the signals through the SPCLK and SSL pins. The slave mode can be selected only when the SPI operating mode is set to single-SPI. Master/slave switching should be done only while the SPE bit is 0; otherwise, the subsequent operation cannot be guaranteed.</p> <p>This module supports only the master mode; be sure to set this bit to 1 to use this module.</p> <p>0: Slave mode 1: Master mode</p>
2	—	0	R/W	<p>Reserved</p> <p>The write value should always be 0. Otherwise, operation cannot be guaranteed.</p>
1	WSWAP	0	R/W	<p>Word Swap</p> <p>Selects word-swap of read-data for DMAC.</p> <p>By setting this bit to 1, read-data to DMAC is swapped in word units. That is, bit[31:16] and bit[15:0] are swapped.</p> <p>0: No word swap for read-data for DMAC. 1: Perform word swap for read-data for DMAC.</p> <p>Note: The read value of this bit is always 0 [RZ/G1H, M].</p>
0	BSWAP	0	R/W	<p>Byte Swap</p> <p>Selects byte-swap of read-data for DMAC.</p> <p>By setting this bit to 1, read-data to DMAC is swapped in byte units. That is, bit[31:24] and bit[23:16] are swapped, and at the same time, bit[15:8] and bit[7:0] are also swapped.</p> <p>0: No byte swap for read-data for DMAC. 1: Perform byte swap for read-data for DMAC.</p> <p>Note: The read value of this bit is always 0 [RZ/G1H, M].</p>

#### 47.4.2 Slave Select Polarity Register (SSLP)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SSLP sets the polarity of the SSL signal. If the contents of SSLP are modified while the SPE bit in the control register (SPCR) is set to 1, the subsequent operation cannot be guaranteed.

Bit:	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	SSLP
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
7 to 1	—	All 0	R	Reserved The write value should always be 0. Otherwise, operation cannot be guaranteed.
0	SSLP	0	R/W	SSL Signal Polarity Setting Sets the polarity of the SSL signal. 0: SSL signal low-active 1: SSL signal high-active

### 47.4.3 Pin Control Register (SPPCR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SPPCR sets the modes of the pins. If the contents of SPPCR are modified while the SPE bit in SPCR is set to 1, the subsequent operation cannot be guaranteed.

Bit:	7	6	5	4	3	2	1	0
	—	—	MOIFE	MOIFV	—	IO3FV	IO2FV	SPLP
Initial value:	0	0	0	0	0	1	1	0
R/W:	R	R	R/W	R/W	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7, 6	—	All 0	R	Reserved The write value should always be 0. Otherwise, operation cannot be guaranteed.
5	MOIFE	0	R/W	Master-Mode Output Idle Value Fixing Enable Fixes the pin output value in an SSL negation period or the SSL keeping period during a burst transfer in master mode. In single-SPI mode, this bit setting applies to MOSI. In dual-SPI mode, the setting of this bit is applied to IO1 and IO0. In quad-SPI mode, the setting of this bit is applied to IO3 to IO0. 0: Output value equals final data from previous transfer. 1: Output value equals the value set in the MOIFV bit. Note: In dual-/quad-SPI modes, IO1 and IO0/IO3 to IO0 are driven to the Hi-Z state regardless of the setting of this bit (see section 47.5.2, Pin Control).
4	MOIFV	0	R/W	Master-Mode Output Idle Fixed Value If the MOIFE bit is 1 in master mode, this module, according to the setting of this bit, determines the output value during the SSL negation period. 0: Output pin idle fixed value equals 0. 1: Output pin idle fixed value equals 1.
3	—	0	R	Reserved The write value should always be 0. Otherwise, operation cannot be guaranteed.
2	IO3FV	1	R/W	Single-/Dual-SPI Mode IO3 Output Fixed Value Fixes the output direction of the IO3 pin in single-/dual-SPI modes. This bit is valid only in single-/dual-SPI modes, and is not affected by the value of MOIFE or MOIFV bit. 0: IO3 output fixed value equals 0. 1: IO3 output fixed value equals 1.
1	IO2FV	1	R/W	Single-/Dual-SPI Mode IO2 Output Fixed Value Fixes the output direction of the IO2 pin in single-/dual-SPI modes. This bit is valid only in single-/dual-SPI modes, and is not affected by the value of MOIFE or MOIFV bit. 0: IO2 output fixed value equals 0. 1: IO2 output fixed value equals 1.

---

Bit	Bit Name	Initial Value	R/W	Description
0	SPLP	0	R/W	<p>Loopback Mode</p> <p>When the SPLP bit is set to 1, this module shuts off the path between the data I/O pin and the transmit/receive shift register, and connects the input path and the output path for the transmit/receive shift register.</p> <p>0: Normal mode 1: Loopback mode</p> <p>Note: When the loopback mode is specified in dual-/quad-SPI modes, the SPI read/write access setting bit (SPRW) in command registers 0 to 3 (SPCMD0 to SPCMD3) should be set to 0 (write operation).</p> <p>Do not modify the setting of this bit during data transfer.</p>

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#### 47.4.4 Status Register (SPSR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SPSR indicates the operating status.

Bit:	7	6	5	4	3	2	1	0
	SPRFF	TEND	SPTEF	—	—	—	—	—
Initial value:	0	1	1	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R

Note: Only 0 can be written to the flags after 1 is read.

Bit	Bit Name	Initial Value	R/W	Description
7	SPRFF	0	R	<p>Receive Buffer Full Flag</p> <p>Indicates that the number of receive data units in the receive buffer is equal to or greater than the receive buffer data triggering number specified in the buffer control register.</p> <p>0: The number of receive data units in the receive buffer is less than the receive buffer data triggering number.</p> <p>1: The number of receive data units in the receive buffer is equal to or greater than the receive buffer data triggering number.</p> <p>[Clearing conditions]</p> <ul style="list-style-type: none"> <li>The receive buffer data is read until the number of data units in the receive buffer becomes less than the specified receive buffer data triggering number.</li> <li>Receive buffer data reset is enabled.</li> <li>Power-on reset.</li> </ul> <p>[Setting condition]</p> <ul style="list-style-type: none"> <li>The number of data units in the receive buffer is equal to or greater than the specified receive buffer data triggering number.</li> </ul>
6	TEND	1	R	<p>Transmit End Flag</p> <p>This bit is set to 1 when transmission is completed, and this bit is 0 when transmission is not completed.</p> <p>[Clearing conditions]</p> <ul style="list-style-type: none"> <li>When transmit data are moved from the transmit register to the transmit shift register.</li> <li>When data reception is started in dual-/quad-SPI modes.</li> </ul> <p>[Setting conditions]</p> <ul style="list-style-type: none"> <li>When the number of data units in the transmit buffer is zero when a serial transfer is completed (except when the dummy data transmission enable bit (TXDMY) is set to 1).</li> <li>When there is not enough space for receiving the specified length of data in the receive buffer when a serial transfer is completed.</li> </ul>

Bit	Bit Name	Initial Value	R/W	Description
5	SPTEF	1	R	<p>Transmit Buffer Empty Flag</p> <p>Indicates that the number of transmit data units in the transmit buffer is equal to or less than the transmit buffer data triggering number specified in the buffer control register.</p> <p>0: The number of transmit data units in the transmit buffer exceeds the specified transmit buffer data triggering number.</p> <p>1: The number of transmit data units in the transmit buffer is equal to or less than the specified transmit buffer data triggering number.</p> <p>[Clearing condition]</p> <ul style="list-style-type: none"> <li>When data is written to the transmit buffer until the number of transmit data units in the transmit buffer exceeds the specified transmit buffer data triggering number.</li> </ul> <p>[Setting conditions]</p> <ul style="list-style-type: none"> <li>When the number of transmit data units in the transmit buffer is equal to or less than the specified transmit buffer data triggering number.</li> <li>When transmit buffer data reset is enabled.</li> <li>Power-on reset.</li> </ul>
4 to 0	—	All 0	R	<p>Reserved</p> <p>The write value should always be 0. Otherwise, operation cannot be guaranteed.</p>

**47.4.5 Data Register (SPDR)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SPDR accesses transmit/receive data buffer.

The transmit buffer (SPTXB) and receive buffer (SPRXB) are independent and are mapped to SPDR.

When data is written to SPDR, the data will be written to the transmit buffer.

When data is read from SPDR, the data will be read from the receive buffer.

SPDR should be read or written to in byte, word, or longword units.

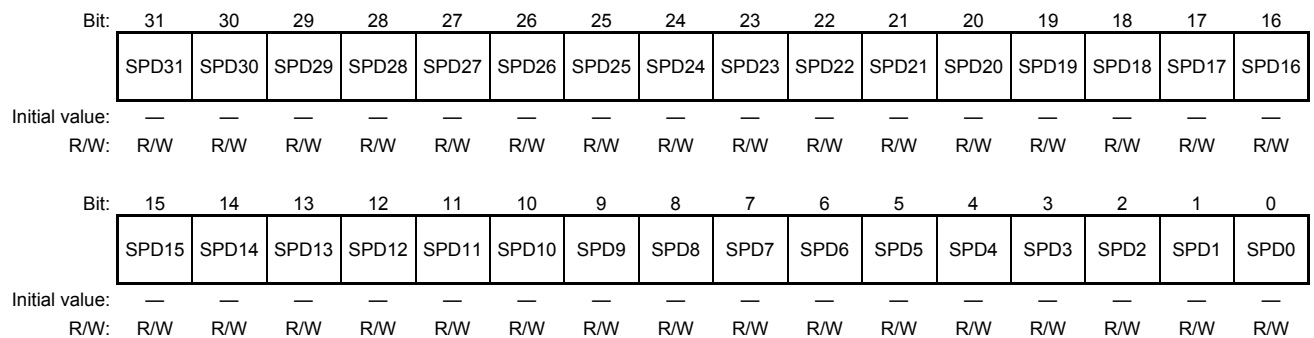
When SPDR is read or written to with the longword-, word-, or byte-access width, the receive or transmit data should be read from or written to the following bits.

Longword: Bits 31 to 0

Word: Bits 15 to 0

Byte: Bits 7 to 0

Note: The QSPI data is in little endian.



#### 47.4.6 Sequence Control Register (SPSCR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SPSCR sets the sequence control method when this module operates in master mode. If the contents of SPSCR are modified while the SPE and MSTR bits in SPCR are 1, the subsequent operation cannot be guaranteed.

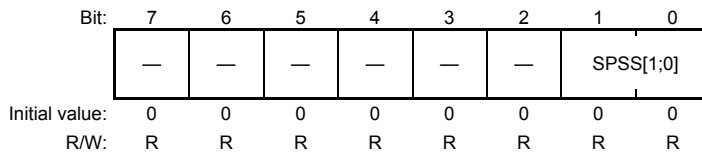
Bit:	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	SPSC[1:0]	
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7 to 2	—	All 0	R	Reserved The write value should always be 0. Otherwise, operation cannot be guaranteed.
1, 0	SPSC[1:0]	00	R/W	Sequence Control Specification These bits specify sequential operations when this module operates in master mode. In master mode, this module references SPCMD0 to SPCMD3 in the order according to the setting of these bits. 00: 0 → 0 → ... 01: 0 → 1 → 0 → ... 10: 0 → 1 → 2 → 0 → ... 11: 0 → 1 → 2 → 3 → 0 → ...

**47.4.7 Sequence Status Register (SPSSR)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SPSSR indicates the sequence control status when this module operates in master mode.

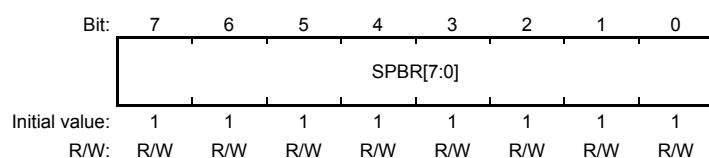


Bit	Bit Name	Initial Value	R/W	Description
7 to 2	—	All 0	R	Reserved The write value should always be 0. Otherwise, operation cannot be guaranteed.
1, 0	SPSS[1:0]	00	R	Sequence Status During sequence control, these bits indicate one of SPCMD0 to SPCMD3 that is currently referenced. 00: SPCMD0 01: SPCMD1 10: SPCMD2 11: SPCMD3

### 47.4.8 Bit Rate Register (SPBR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SPBR sets the bit rate when this module operates in master mode. If the contents of SPBR are modified while the SPE and MSTR bits in SPCR are 1, the subsequent operation cannot be guaranteed.



The bit rate is determined by combinations of SPBR settings and the values in the bit rate division setting bits (BRDV[1:0]) in SPCMD0 to SPCMD3.

In single-SPI slave mode, the bit rate depends on the input clock bit rate regardless of the setting of SPBR[1:0] and BRDV[1:0] bits.

When SPBR is set to 0, the base bit rate is selected.

The equation for calculating the bit rate when SPBR is not 0 is given below. In the equation, n denotes an SPBR setting (1, ..., 255), and N denotes bit settings in the bits BRDV[1:0] (0, 1, 2, 3).

$$\text{Bit rate} = \frac{f(\text{QSPI}\phi)}{2 \times n \times 2^N}$$

Table 47.3 shows examples of the relationship between SPBR and BRDV[1:0] bits settings.

**Table 47.3 Relationship between SPBR and BRDV[1:0] Settings**

SPBR[7:0] (n)	BRDV[1:0] (N)	Division Ratio	Bit Rate	
			QSPIφ = 78 MHz	QSPIφ = 97.5 MHz
0	0	1	78.0 Mbps	97.50 Mbps
1	0	2	39.0 Mbps	48.75 Mbps
2	0	4	19.5 Mbps	24.38 Mbps
3	0	6	13.0 Mbps	16.25 Mbps
4	0	8	9.75 Mbps	12.19 Mbps
5	0	10	7.80 Mbps	9.75 Mbps
6	0	12	6.50 Mbps	8.13 Mbps
6	1	24	3.25 Mbps	4.06 Mbps
6	2	48	1.625 Mbps	2.03 Mbps
6	3	96	812.5 kbps	1.02 Mbps
255	3	4080	19.12 kbps	23.90 kbps

**47.4.9 Data Control Register (SPDCR)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SPDCR enables or disables dummy data transmission when this module operates in master mode.

Bit:	7	6	5	4	3	2	1	0
	TXDMY	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
7	TXDMY	0	R/W	<p>Dummy Data Transmission Enable</p> <p>Enables or disables dummy data transmission from the MOSI pin when the transmit buffer is empty in single-SPI master mode. The last output value in the previous transmit data is used as dummy data.</p> <p>Specifically, if this bit is set to 1 when the transmit buffer is empty, 0 is output from the MOSI pin as dummy data.</p> <p>This bit setting can be changed while the transmit end flag (TEND) in SPSR is 1. Otherwise, operation cannot be guaranteed.</p> <p>0: Disables dummy data transmission. 1: Enables dummy data transmission.</p>
6 to 0	—	All 0	R	<p>Reserved</p> <p>The write value should always be 0. Otherwise, operation cannot be guaranteed.</p>

**47.4.10 Clock Delay Register (SPCKD)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SPCKD sets a period (clock delay) from the beginning of SSL signal assertion to SPCLK oscillation when the clock delay setting enable bit (SCKDEN) in SPCMD0 to SPCMD3 is 1 in master mode. If the contents of SPCKD are modified while the SPE and MSTR bits in SPCR are 1, the subsequent operation cannot be guaranteed.

Be sure to set this register to H'00 when using this module in single-SPI slave mode.

Bit:	7	6	5	4	3	2	1	0
	—	—	—	—	—	SCKDL[2:0]		
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7 to 3	—	All 0	R	Reserved The write value should always be 0. Otherwise, operation cannot be guaranteed.
2 to 0	SCKDL[2:0]	000	R/W	Clock Delay Setting These bits set a period (clock delay) from the beginning of SSL signal assertion to SPCLK oscillation when the SCKDEN bit in SPCMD0 to SPCMD3 is 1. 000: 1 SPCLK cycle 001: 2 SPCLK cycles 010: 3 SPCLK cycles 011: 4 SPCLK cycles 100: 5 SPCLK cycles 101: 6 SPCLK cycles 110: 7 SPCLK cycles 111: 8 SPCLK cycles



#### 47.4.11 Slave Select Negation Delay Register (SSLND)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SSLND sets a period (SSL negation delay) from the transmission of a final SPCLK edge to the negation of the SSL signal during a serial transfer when the SSL negation delay setting enable bit (SLNDEN) in SPCMD0 to SPCMD3 is 1 in master mode. If the contents of SSLND are modified while the SPE and MSTR bits in SPCR are 1, the subsequent operation cannot be guaranteed.

Be sure to set this register to H'00 when using this module in single-SPI slave mode.

Bit:	7	6	5	4	3	2	1	0
	—	—	—	—	—	SLNDL[2:0]		
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7 to 3	—	All 0	R	Reserved The write value should always be 0. Otherwise, operation cannot be guaranteed.
2 to 0	SLNDL[2:0]	000	R/W	SSL Negation Delay Setting These bits set a period (SSL negation delay) from the transmission of a final SPCLK edge to the negation of the SSL signal during a serial transfer when the SLNDEN bit in SPCMD0 to SPCMD3 is 1. 000: 0.5 SPCLK cycle 001: 1.5 SPCLK cycles 010: 2.5 SPCLK cycles 011: 3.5 SPCLK cycles 100: 4.5 SPCLK cycles 101: 5.5 SPCLK cycles 110: 6.5 SPCLK cycles 111: 7.5 SPCLK cycles

**47.4.12 Next-Access Delay Register (SPND)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SPND sets a period (next-access delay) from termination of a serial transfer to the beginning of the next serial transfer when the next-access delay enable bit (SPNDEN) in SPCMD0 to SPCMD3 is 1 in master mode. If the contents of SPND are modified while the SPE and MSTR bits in SPCR are 1, the subsequent operation cannot be guaranteed.

Be sure to set this register to H'00 when using this module in single-SPI slave mode.

Bit:	7	6	5	4	3	2	1	0
	—	—	—	—	—	SPNDL[2:0]		
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7 to 3	—	All 0	R	Reserved The write value should always be 0. Otherwise, operation cannot be guaranteed.
2 to 0	SPNDL[2:0]	000	R/W	Next-Access Delay Setting These bits set a period (next-access delay) from termination of a serial transfer to the beginning of the next serial transfer when the SPNDEN bit in SPCMD0 to SPCMD3 is 1. 000: 1 SPCLK cycle 001: 2 SPCLK cycles 010: 3 SPCLK cycles 011: 4 SPCLK cycles 100: 5 SPCLK cycles 101: 6 SPCLK cycles 110: 7 SPCLK cycles 111: 8 SPCLK cycles

**47.4.13 Command Register n (SPCMDn) (n = 0 to 3)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

This module has four command registers (SPCMD0 to SPCMD3). SPCMD0 to SPCMD3 are used to set a transfer format in master mode. In master mode, this module sequentially references SPCMD0 to SPCMD3 according to the settings in the sequence control register (SPSCR), and executes the serial transfer that is set in the referenced SPCMD.

If the contents of currently referred-to SPCMD are modified while the TEND bit in SPSR indicates that communication has not been completed, the subsequent operation cannot be guaranteed. The currently referred-to SPCMD can be checked by reading the sequence status register (SPSSR). In addition, if the contents of SPCMD0 are modified during operation in single-SPI slave mode, the subsequent operation cannot be guaranteed.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SCKDEN	SLNDEN	SPNDEN	LSBF	SPB[3:0]			SSLKP	SPIMOD[1:0]	SPRW	BRDV[1:0]	CPOL	CPHA			
Initial value:	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	SCKDEN	1	R/W	<p>Clock Delay Setting Enable</p> <p>Sets a period (clock delay) from the beginning of SSL signal assertion to SPCLK oscillation in master mode. If this bit is 0, this module sets the clock delay to 0 SPCLK cycle. If this bit is 1, this module starts SPCLK oscillation in compliance with the clock delay register (SPCKD) settings. For the continuous access in which SSL is kept asserted over the multiple commands, this bit can be set to 0 only when the pertinent command is the second or subsequent one. Otherwise, this bit should be set to 1.</p> <p>0: A clock delay of 0 SPCLK cycle 1: A clock delay equal to SPCKD settings.</p>
14	SLNDEN	1	R/W	<p>SSL Negation Delay Setting Enable</p> <p>Sets a period (SSL negation delay) from SPCLK oscillation stoppage to SSL signal negation in master mode. If this bit is 0, this module sets the SSL negation delay to 0 SPCLK cycle. If this bit is 1, this module negates the SSL signal in compliance with the slave select negation delay register (SSLND) settings. For the continuous access in which SSL is kept asserted over the multiplier commands, this bit can be set to 0 only when the pertinent command is not the last one. Otherwise, this bit should be set to 1.</p> <p>When using this module in single-SPI slave mode, set this bit to 1 and the slave select negation delay register (SSLND) to H'0.</p> <p>0: An SSL negation delay of 0 SPCLK cycle 1: An SSL negation delay equal to SSLND settings.</p>

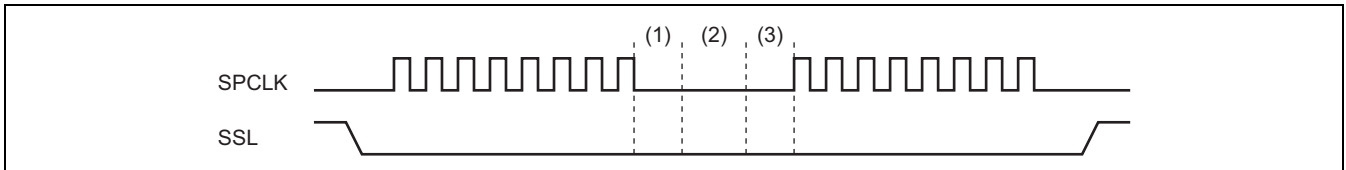
Bit	Bit Name	Initial Value	R/W	Description
13	SPNDEN	1	R/W	<p>Next-Access Delay Enable</p> <p>Sets the period (next-access delay) from termination of a serial transfer to the beginning of the next serial transfer in master mode. If this bit is 0, this module sets the next-access delay to 0 SPCLK cycle. If this bit is 1, this module starts next serial transfer in compliance with the next-access delay register (SPND) settings. For the continuous access in which SSL is kept asserted over the multiple commands, this bit can be set to 0 only when the pertinent command is not the last one. Otherwise, this bit should be set to 1.</p> <p>When using this module in single-SPI slave mode, set this bit to 1 and the next-access delay register (SPND) to B'000.</p> <p>0: A next-access delay of 0 SPCLK cycle. 1: A next-access delay equal to SPND settings.</p>
12	LSBF	0	R/W	<p>LSB First</p> <p>Sets the data format to MSB first or LSB first in master mode or single-SPI slave mode.</p> <p>0: MSB first 1: LSB first</p>
11 to 8	SPB[3:0]	0000	R/W	<p>Transfer Data Length Setting</p> <p>These bits set the basic transfer data length for serial transfer. For LSB-first transfer, the transfer data is reversed within the data width specified with these bits. The actual amount of data to be transferred is determined by multiplying the value set with these bits by the value set with SPBMUL0 to SPBMUL3.</p> <p>0000: 8 bits (1 byte) 0001: 16 bits (2 bytes) 0010: 32 bits (4 bytes) 0011 to 1111: Setting prohibited</p>
7	SSLKP	0	R/W	<p>SSL Signal Level Keeping</p> <p>Specifies whether or not the SSL signal level for the current command is to be kept from the end of the transfer for the current command to the beginning of the transfer for the next command in master mode.</p> <p>Setting this bit to 1 enables a transition to the next access while the SSL signal is kept asserted.</p> <p>0: Negates all SSL signals upon completion of transfer. 1: Keeps the SSL signal level from the end of the transfer to the beginning of the next access.</p>
6, 5	SPIMOD[1:0]	00	R/W	<p>SPI Operating Mode</p> <p>These bits select the operating mode of this module from single-, dual-, or quad-SPI.</p> <p>00: Single-SPI 01: Dual-SPI 10: Quad-SPI 11: Setting prohibited</p>

Bit	Bit Name	Initial Value	R/W	Description
4	SPRW	0	R/W	<p>SPI Read/Write Access</p> <p>Sets an access direction in dual-/quad-SPI modes. This bit is invalid in single-SPI mode</p> <p>0: Write operation (IO1 and IO0/IO3 to IO0: Output)</p> <p>1: Read operation (IO1 and IO0/IO3 to IO0: Input)</p>
3, 2	BRDV[1:0]	00	R/W	<p>Bit Rate Frequency Division Setting</p> <p>These bits are used to determine the bit rate in master mode. The settings of these bits and of the bit rate register (SPBR) together determine the bit rate. The base bit rate depends on the setting of the SPBR.</p> <p>The setting of this field selects division of the base bit rate by one, two, four, or eight.</p> <p>Individual BRDV[1:0] values can be set in each of command registers 0 to 3. Therefore, serial transfers can be at different bit rates for each of the commands.</p> <p>00: Base bit rate</p> <p>01: Two division of the base</p> <p>10: Four division of the base</p> <p>11: Eight division of the base</p>
1	CPOL	0	R/W	<p>SPCLK Polarity Setting</p> <p>Sets an SPCLK polarity. When data communication is performed between this quad serial peripheral interface module and another module, the same SPCLK polarity should be set for both modules.</p> <p>0: Positive (SPCLK = 0 when idle)</p> <p>1: Negative (SPCLK = 1 when idle)</p>
0	CPHA	1	R/W	<p>SPCLK Phase Setting</p> <p>Sets an SPCLK edge for latching and shifting data to be transferred. When data communication is performed between this quad serial peripheral interface module and another module, the same SPCLK edge should be set for both modules.</p> <p>0: Data latch on odd edge, data shift on even edge</p> <p>1: Data shift on odd edge, data latch on even edge</p> <p>Note: The first SPCLK edge is treated as the first edge.</p>

Reference: Some serial flash memory datasheets refer to SPCLK specifications, which are determined by what this document refers to as CPOL and CPHA bits, as SPI modes 0 to 3. Assuming that SPI modes 0 to 3 are controlled by SPI mode bits [1:0], CPOL and CPHA in this document correspond to SPI mode bits 1 and 0, respectively.

In this module, the initial values of CPOL and CPHA are 0 and 1, respectively, selecting SPI mode 1 as the initial mode.

- Notes:
1. When setting any or all of the clock delay period, SSL negation delay period, and next-access delay period to 0, be sure to set SSLKP to 1 to select the continuous access in which SSL is not negated. Otherwise, operation cannot be guaranteed. For the method of setting the various delay periods for the continuous access in which SSL is not negated, see below.
  2. For the continuous access in which SSL is not negated, SPCLK clock stopping is followed by the SSL negation delay period, next-access delay period, and next command clock delay period, in this order. When setting any of the setting enable bit (SPCKDEN), SSL negation delay setting enable bit (SLNDEN), and next-access delay enable bit (SPNDEN) to 0, be sure to set the bit corresponding to the later period prior to the bit corresponding to the earlier period.



In the above figure, (1), (2), and (3) refer to the SSL negation delay period, next-access delay period, and next command clock delay period, respectively. When setting any of these bits to 0, be sure to set (3) first. In other words, setting 1 after 0 as in  $\{(1), (2), (3)\} = \{0, 0, 1\}, \{0, 1, 1\}, \{0, 1, 0\} \dots$  is prohibited. Allowed setting is  $\{(1), (2), (3)\} = \{1, 1, 1\}, \{1, 1, 0\}, \{1, 0, 0\}, \{0, 0, 0\}$ . If set otherwise, operation cannot be guaranteed.

3. When changing BRDV[1:0] or CPOL for each command for the continuous access in which the SSL level is held, be sure to insert the SSL negation delay period, next-access delay period, and clock delay period between commands. Otherwise, operation cannot be guaranteed.
4. When changing SPIMOD[1:0] or CPHA for each command for the continuous access in which the SSL level is held, be sure to insert one cycle or more between commands. Otherwise, operation cannot be guaranteed.

**47.4.14 Buffer Control Register (SPBFCR)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SPBFCR resets the number of data units in the transmit buffer (SPTXB) or receive buffer (SPRXB) and sets the number of triggering data units.

Bit:	7	6	5	4	3	2	1	0
	TXRST	RXRST	TXTRG[1:0]		—	RXTRG[2:0]		
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7	TXRST	0	R/W	<b>Transmit Buffer Data Reset</b> Invalidates transmit data in the transmit buffer and resets the transmit buffer to an empty state. 0: Allows the transmit buffer normal operation. 1: Resets the transmit buffer.
6	RXRST	0	R/W	<b>Receive Buffer Data Reset</b> Invalidates receive data in the receive buffer and resets the receive buffer to an empty state. 0: Allows the receive buffer normal operation. 1: Resets the receive buffer.
5, 4	TXTRG[1:0]	00	R/W	<b>Transmit Buffer Data Triggering Number</b> Specifies the timing at which the transmit buffer empty state is determined, that is when the SPTEF flag in the status register is set. When the number of bytes of data in the transmit buffer (SPTXB) is equal to or less than the specified triggering number, the SPTEF flag is set to 1. 00: 31 bytes (1 byte available) 01: 30 bytes (2 bytes available) 10: 28 bytes (4 bytes available) 11: 0 byte (32 bytes available)
3	—	0	R	<b>Reserved</b> The write value should always be 0. Otherwise, operation cannot be guaranteed.

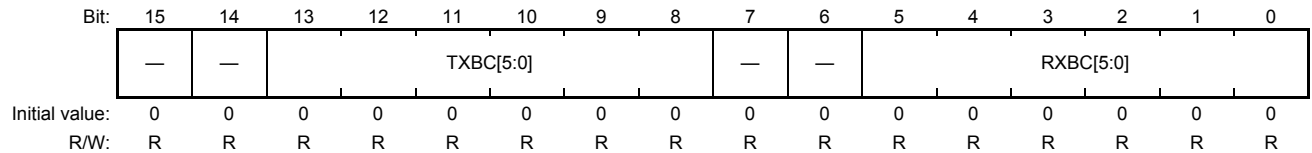
Bit	Bit Name	Initial Value	R/W	Description
2 to 0	RXTRG[2:0]	000	R/W	<p>Receive Buffer Data Triggering Number</p> <p>Specify the timing at which the receive buffer full state is determined, that is when the SPRFF flag in the status register is set. When the number of bytes of data in the receive buffer (SPRXB) is equal to or greater than the specified triggering number, the SPRFF flag is set to 1.</p> <p>000: 1 byte (31 bytes available)            001: 2 bytes (30 bytes available)            010: 4 bytes (28 bytes available)            011: 5 bytes (27 bytes available)            100: 8 bytes (24 bytes available)            101: 16 bytes (16 bytes available)            110: 24 bytes (8 bytes available)            111: 32 bytes (0 byte available)</p>



**47.4.15 Buffer Data Count Register (SPBDCR)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SPBDCR indicates the number of data units stored in the transmit buffer (SPTXB) and receive buffer (SPRXB). The upper eight bits indicate the number of transmit data units in the transmit buffer and the lower eight bits indicate the number of receive data units in the receive buffer.



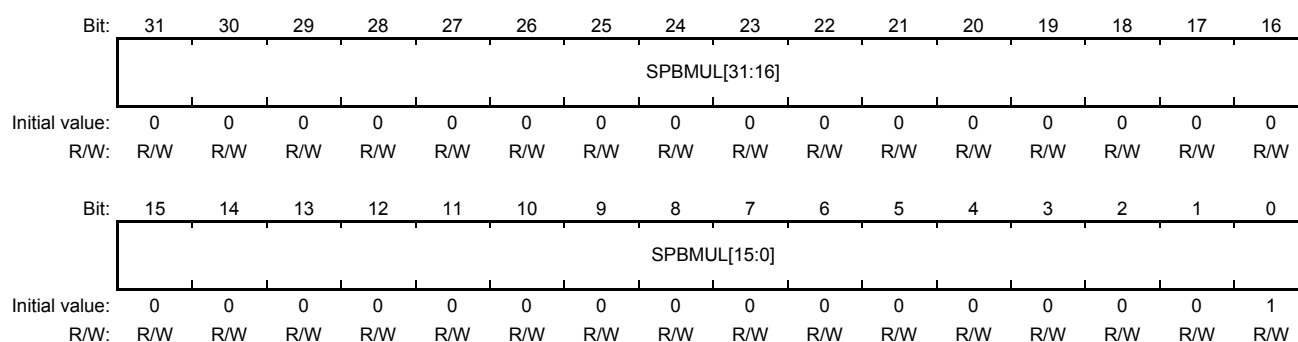
Bit	Bit Name	Initial Value	R/W	Description
15, 14	—	All 0	R	Reserved The write value should always be 0. Otherwise, operation cannot be guaranteed.
13 to 8	TXBC[5:0]	000000	R	Transmit Data Byte Counter Indicate the number of transmit data bytes in the transmit data buffer (SPTXB). B'000000 indicates that SPTXB is empty. B'100000 indicates that SPTXB is full.
7, 6	—	All 0	R	Reserved The write value should always be 0. Otherwise, operation cannot be guaranteed.
5 to 0	RXBC[5:0]	000000	R	Receive Data Byte Counter Indicates the number of receive data bytes in the receive data buffer (SPRXB). B'000000 indicates that SPRXB is empty. B'100000 indicates that SPRXB is full.

**47.4.16 Transfer Data Length Multiplier Setting Register n (SPBMULn) (n = 0, 1, 2, 3)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SPBMUL0 to SPBMUL3 set the number of times to transfer the specific length of data defined by the transfer data length setting bits (SPB[3:0]) in SPCMD0 to SPCMD3. SPBMUL0 to SPBMUL3 correspond to SPCMD0 to SPCMD3, respectively. This register setting is valid only in master mode. In single-SPI slave mode, this register should be set to the initial value; other values are prohibited.

If a command register is referred to while the TEND bit in SPSR indicates that communication has not been completed and SPBMUL corresponding to the referred-to command register is modified, the subsequent operation is not guaranteed. The currently referred-to command register can be checked by reading the sequence status register (SPSSR).



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	SPBMUL [31:0]	H'0000 0001	R/W	<p>Transfer Data Length Multiplier Setting</p> <p>These bits set the multiplier for transfer data; that is, the number of times to transfer the specific length of data defined by SPB[3:0] bits in SPCMD0 to SPCMD3.</p> <p>The actual amount of data to be transferred is determined by <math>SPB[3:0] \times SPBMUL[31:0]</math>.</p> <p>Setting these bits to H'00000000 allows the defined size of data to be transferred 4,294,967,296 times.</p>

## 47.5 Operation

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

In this section, the serial transfer period means a period from the beginning of driving valid data to the fetching of the final valid data, and the SSL negation period means the idle period.

### 47.5.1 Overview of Operations

This module is capable of serial transfers in single-/dual-/quad-SPI master modes and single-SPI slave mode. Table 47.4 gives the features of single-/dual-/quad-SPI modes.

**Table 47.4 Features of Each SPI Mode**

	Single-SPI	Dual-SPI	Quad-SPI
Number of data lines	One input line and one output line	Two IO lines	Four IO lines
Data line direction	Single-directional	Bidirectional	Bidirectional
Slave operation	Not supported	Not supported	Not supported
Simultaneous transmission/reception	Supported	Not supported	Not supported

Table 47.5 gives the overview of master-mode operation.

**Table 47.5 Overview of Master Mode**

Items	Master Mode
MSTR bit setting in the control register	1
SPCLK signal	Output
MOSI signal (single-SPI)	Output
MISO signal (single-SPI)	Input
IO1 and IO0 (dual-SPI)/ IO3 to IO0 (quad-SPI)	Input/output
SSL signal	Output
Switching SSL polarity	Supported
Transfer rate	Up to QSPI $\phi$
Clock source	On-chip baud rate generator
Clock polarity	Positive/negative
Clock phase	Latch at rising/output at falling Latch at falling/output at rising
Transfer bit order	MSB first/LSB first
Transfer data length	(8/16/32) $\times$ (1 to 4,294,967,296) bits
Burst transfer	Supported
SPCLK delay control	Supported
SSL negation delay control	Supported
Next-access delay control	Supported
Transfer start method	Writing data to the transmit buffer when SPE = 1 There is space in the receive buffer when SPE = 1*
Sequence control	Supported
Transmit buffer empty detection	Supported
Receive buffer full detection	Supported
Overrun error detection	Not supported
Underrun error detection	Not supported
Mode fault error detection	Not supported

Note: \* During single-SPI operation and dual-/quad-SPI mode write operation, a transfer is started by setting SPE to 1 and writing data to the transmit buffer. During dual-/quad-SPI mode read operation, a transfer is started by setting SPE to 1 when there is space for the specified length of data in the receive buffer.

### 47.5.2 Pin Control

This module automatically switches the pin states according to the status after write/read transfer in single-SPI master or slave mode or dual-/quad-SPI mode. The status of the data pins (MOSI/MISO/IO[3:0]) in the idle state depends on the MOIFE and MOIFV bit settings, the single-/dual-SPI mode IO3 output fixed value bit (IO3FV) setting, and the single-/dual-SPI mode IO2 output fixed value bit (IO2FV) setting. Table 47.6 shows the pin states in single-SPI master mode. Table 47.7 shows the pin states in dual-/quad-SPI modes.

**Table 47.6 Pin States in Single-SPI Master Mode**

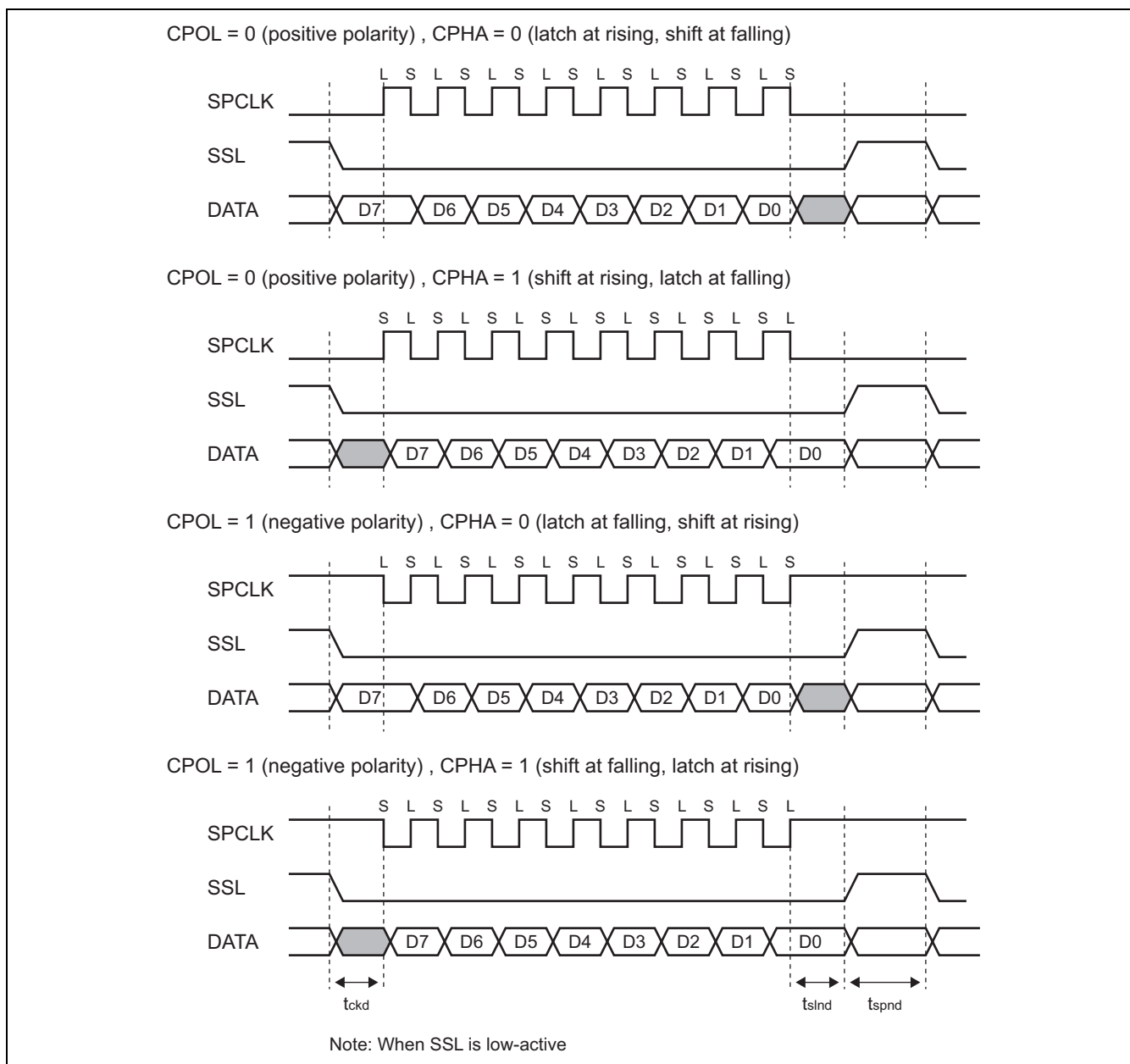
Items	Single-SPI Master Mode
SSL	Output
SPCLK	Output
MOSI	Output
MISO	Input
MOSI in the idle state	MOIFE = 0: Final output value MOIFE = 1: MOIFV setting value
MISO in the idle state	—
IO2	IO2FV setting value output or not used
IO3	IO3FV setting value output or not used

**Table 47.7 Pin States in Dual-/Quad-SPI Modes**

Items	Dual-SPI Mode	Quad-SPI Mode
SSL	Output	Output
SPCLK	Output	Output
IO0	I/O	I/O
IO1	I/O	I/O
IO2	IO2FV setting value output or not used	I/O
IO3	IO3FV setting value output or not used	I/O
IO0 in the idle state	After writing: MOIFE = 0: Final output value MOIFE = 1: MOIFV setting value After reading: Hi-Z	After writing: MOIFE = 0: Final output value MOIFE = 1: MOIFV setting value After reading: Hi-Z
IO1 in the idle state	After writing: MOIFE = 0: Final output value MOIFE = 1: MOIFV setting value After reading: Hi-Z	After writing: MOIFE = 0: Final output value MOIFE = 1: MOIFV setting value After reading: Hi-Z
IO2 in the idle state	IO2FV setting value output or not used	After writing: MOIFE = 0: Final output value MOIFE = 1: MOIFV setting value After reading: Hi-Z
IO3 in the idle state	IO3FV setting value output or not used	After writing: MOIFE = 0: Final output value MOIFE = 1: MOIFV setting value After reading: Hi-Z

### 47.5.3 Transfer Format

The SPI has four clock settings determined by the SPCLK polarity setting (CPOL) and SPCLK phase setting (CPHA) bits in SPCMD0 to SPCMD3. Figure 47.1 shows the data latch/shift timing based on each setting in an 8-bit MSB first transfer. In Figure 47.1, L indicates the latch timing and S indicates the shift timing. DATA corresponds to MISO/MOSI in single-SPI mode; IO1 and IO0 in dual-SPI mode; or IO3 to IO0 in quad-SPI mode.  $t_{ckd}$  indicates the clock delay period when the SCKDEN bit in SPCMD0 to SPCMD3 is set to 1. Similarly,  $t_{slnd}$  indicates the SSL negation delay period when the SLNDEN bit in SPCMD0 to SPCMD3 is set to 1, and  $t_{spnd}$  indicates the next-access delay period when the SPNDEN bit in SPCMD0 to SPCMD3 is set to 1.



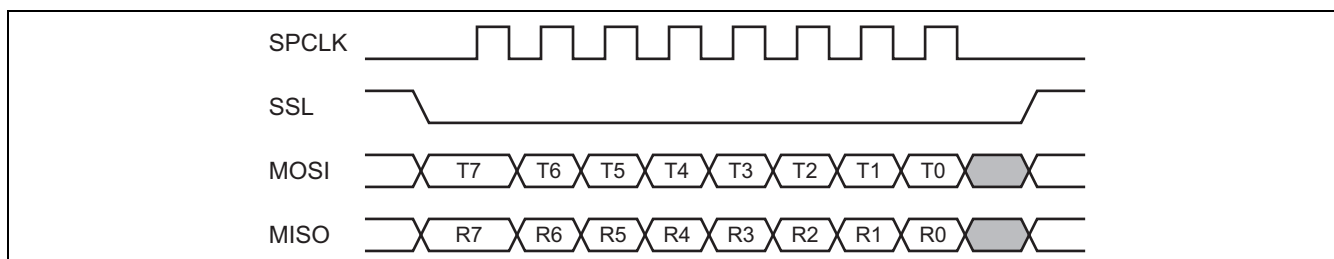
**Figure 47.1 SPI Clock Setting and Transfer Timing**

Note that when the base bit rate is used, transmission and reception when CPHA = 0 is not available.

The following describes 8-bit MSB first transfer in single-/dual-/quad-SPI modes when CPOL = 0 and CPHA = 0.

**(1) Single-SPI mode**

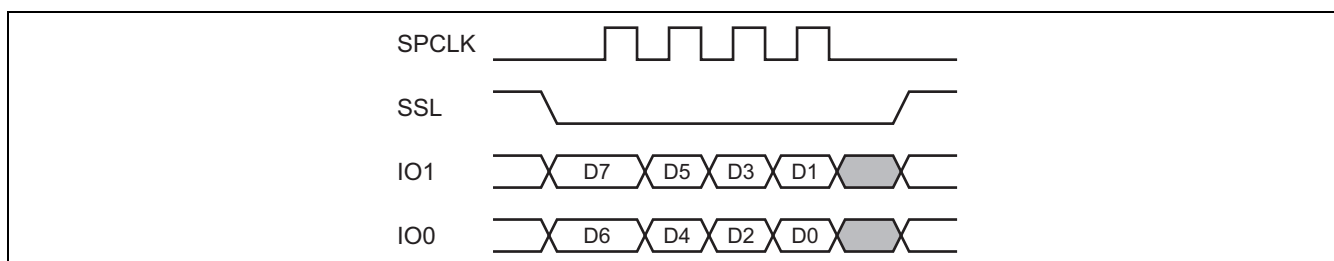
Figure 47.2 shows the transfer format in single-SPI mode. This mode provides transmission and reception simultaneously. Since one data line is used for serial communication both in transmission and reception, the communication speed is 1 bit per SPCLK clock cycle. Transfer data is specified using SPCMD0 to SPCMD3. For details of transfer data, see section 47.5.4, Transfer Data.



**Figure 47.2 Transfer Format in Single-SPI Mode**

**(2) Dual-SPI mode**

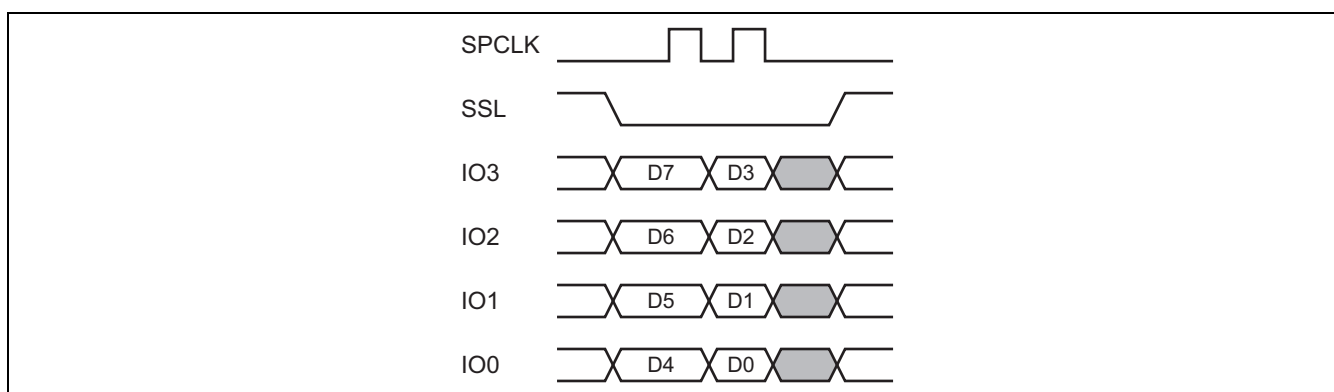
Figure 47.3 shows the transfer format in dual-SPI mode. This mode only provides operation of a single direction, that is, either transmission or reception. Transmission or reception can be set using the SPI read/write access setting bit (SPRW) in SPCMD0 to SPCMD3. Transmission is carried out by write operation and reception by read operation. The I/O directions of IO1 and IO0 are switched accordingly. Since two data lines are used for serial communication both in transmission and reception, the communication speed is 2 bits per SPCLK clock cycle. The start bit of the transfer data is output from IO1. Transfer data is specified using SPCMD0 to SPCMD3. For details of transfer data, see section 47.5.4, Transfer Data.



**Figure 47.3 Transfer Format in Dual-SPI Mode**

### (3) Quad-SPI mode

Figure 47.4 shows the transfer format in quad-SPI mode. This mode provides operation of a single direction, that is, either transmission or reception. Transmission or reception can be set using the SPRW bit in SPCMD0 to SPCMD3. Transmission and reception are accomplished by writing and reading, respectively. The I/O directions of IO3 to IO0 are switched accordingly. Since four data lines are used for serial communication both in transmission and reception, the communication speed is 4 bits per SPCLK clock cycle. The start bit of the transfer data is output from IO3. Transfer data is specified using SPCMD0 to SPCMD3. For details of transfer data, see section 47.5.4, Transfer Data.



**Figure 47.4 Transfer Format in Quad-SPI Mode**

#### 47.5.4 Transfer Data

The data format is determined by the SPB[3:0] and the LSB first (LSBF) bits in SPCMD0 to SPCMD3 and SPBMUL0 to SPBMUL3. In both MSB first and LSB first transfers, this module treats the specified size of data beginning at the MSB of the transmit shift register as transmit data, and the specified length of data beginning at the LSB of the receive shift register as receive data, regardless of whether the actual arrangement is MSB- or LSB-first. The following sections describe MSB-first and LSB-first transfers in 32-bit, 16-bit, and 8-bit data units.



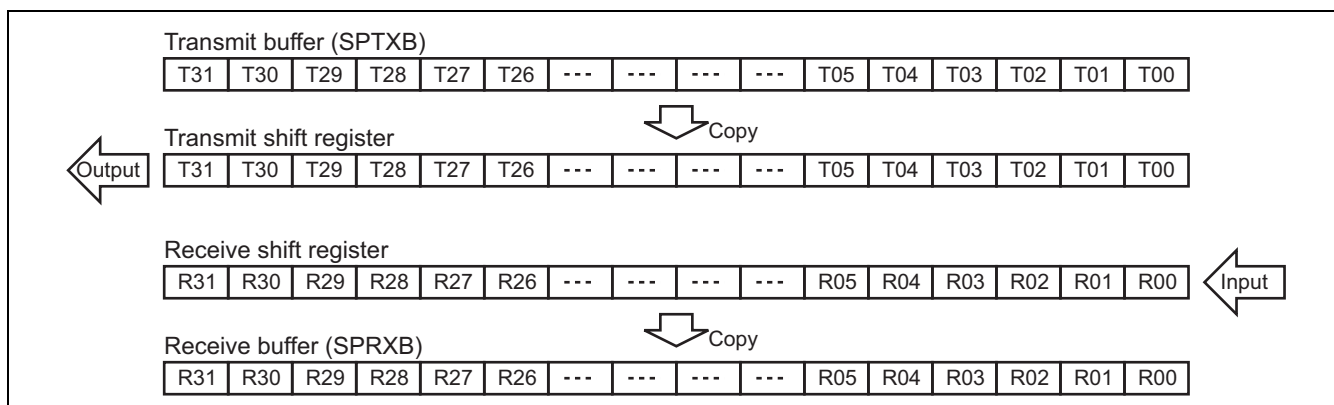
**(1) MSB-first transfer (32-bit data)**

Figure 47.5 shows the operation of the transmit buffer and transmit shift register, and the receive shift register and receive buffer when this module performs a 32-bit MSB-first data transfer.

For data transmission, the CPU or direct memory access controller (DMAC) writes 32-bit transmit data to the transmit buffer (SPTXB). If the transmit shift register is empty, this module copies the data with MSB-aligned in the transmit buffer to the transmit shift register, and fills the transmit shift register. When data transmission is started, this module outputs data beginning at the MSB (bit 31) of the transmit shift register, and when the SPCLK clock cycle required for the serial transfer of 32 bits has passed, the transmit shift register becomes empty.

For data reception, data received from the data pin is stored in the receive shift register beginning at the LSB (bit 0). When the SPCLK clock cycle required for the serial transfer of 32 bits has passed, the receive shift register becomes full. If the receive buffer (SPRXB) has a space for 32 bits or more, this module copies the 32-bit data beginning at the LSB from the receive shift register to the receive buffer, and empties the receive shift register. If the receive buffer does not have a space for 32 bits or more in master mode, data reception is not carried out. In order to start reception, the specified length of data should be read from the receive buffer to secure the space for 32 bits or more in the receive buffer.

In actual transfer, this operation is repeated for the number of times defined by SPBMUL0 to SPBMUL3.



**Figure 47.5 MSB-First Transfer (32-Bit Data)**

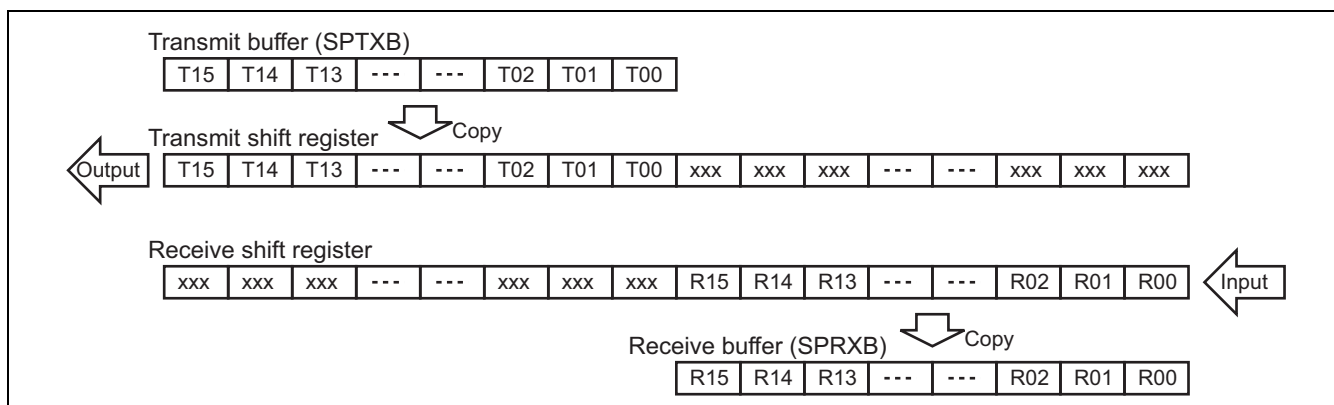
**(2) MSB-first transfer (16-bit data)**

Figure 47.6 shows the operation of the transmit buffer and transmit shift register, and the receive shift register and receive buffer when this module performs a 16-bit MSB-first data transfer.

For data transmission, the CPU or direct memory access controller (DMAC) writes 16-bit transmit data to the transmit buffer (SPTXB). If the transmit shift register is empty, this module copies the data with MSB-aligned in the transmit buffer to the transmit shift register, and fills the transmit shift register. When data transmission is started, this module outputs data beginning at the MSB (bit 31) of the transmit shift register, and when the SPCLK clock cycle required for the serial transfer of 16 bits has passed, the transmit shift register becomes empty.

For data reception, data received from the data pin is stored in the receive shift register beginning at the LSB (bit 0). When the SPCLK clock cycle required for the serial transfer of 16 bits has passed, the receive shift register becomes full. If the receive buffer (SPRXB) has a space for 16 bits or more, this module copies the 16-bit data beginning at the LSB from the receive shift register to the receive buffer, and empties the receive shift register. If the receive buffer does not have a space for 16 bits or more in master mode, data reception is not carried out. In order to start reception, the specified length of data should be read from the receive buffer to secure the space for 16 bits or more in the receive buffer.

In actual transfer, this operation is repeated for the number of times defined by SPBMUL0 to SPBMUL3.



**Figure 47.6 MSB-First Transfer (16-Bit Data)**

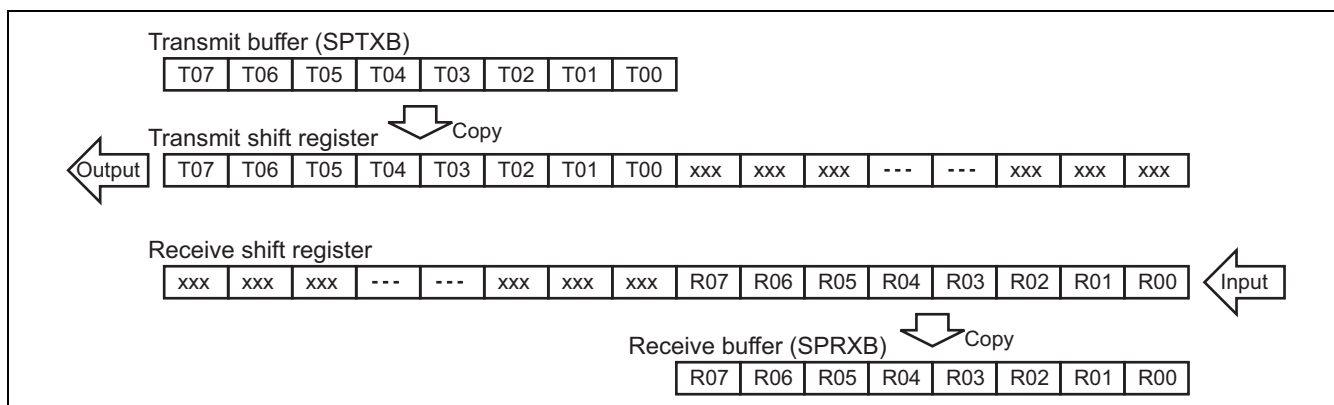
**(3) MSB-first transfer (8-bit data)**

Figure 47.7 shows the operation of the transmit buffer and transmit shift register, and the receive shift register and receive buffer when this module performs an 8-bit MSB-first data transfer.

For data transmission, the CPU or direct memory access controller (DMAC) writes 8-bit transmit data to the transmit buffer (SPTXB). If the transmit shift register is empty, this module copies the data with MSB-aligned in the transmit buffer to the transmit shift register, and fills the transmit shift register. When data transmission is started, this module outputs data beginning at the MSB (bit 31) of the transmit shift register, and when the SPCLK clock cycle required for the serial transfer of 8 bits has passed, the transmit shift register becomes empty.

For data reception, data received from the data pin is stored in the receive shift register beginning at the LSB (bit 0). When the SPCLK clock cycle required for the serial transfer of 8 bits has passed, the receive shift register becomes full. If the receive buffer (SPRXB) has a space for 8 bits or more, this module copies the 8-bit data beginning at the LSB from the receive shift register to the receive buffer, and empties the receive shift register. If the receive buffer does not have a space for 8 bits or more in master mode, data reception is not carried out. In order to start reception, data for the specified length of data should be read from the receive buffer to secure the space for 8 bits or more in the receive buffer.

In actual transfer, this operation is repeated for the number of times defined by SPBMUL0 to SPBMUL3.



**Figure 47.7 MSB-First Transfer (8-Bit Data)**

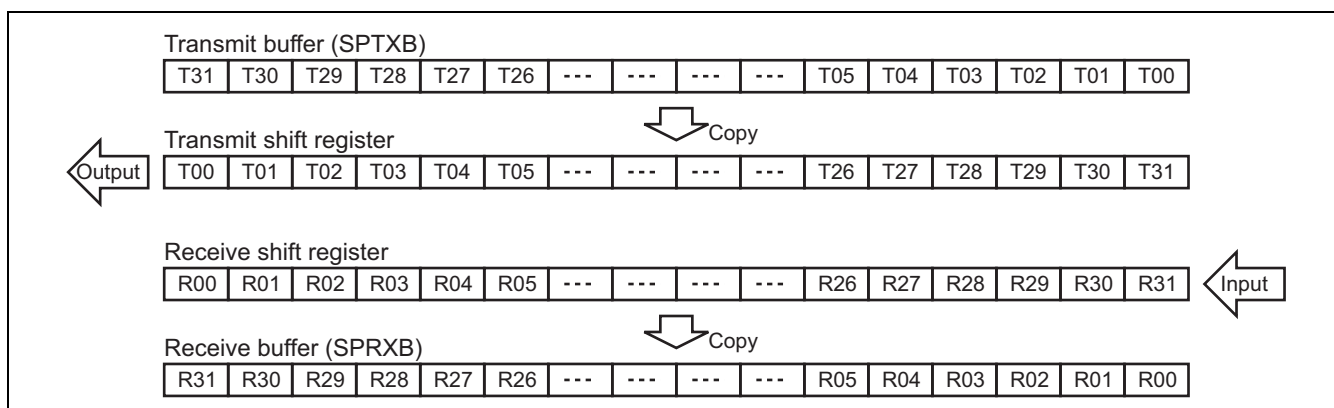
**(4) LSB-first transfer (32-bit data)**

Figure 47.8 shows the operation of the transmit buffer and transmit shift register, and the receive shift register and receive buffer when this module performs a 32-bit LSB-first data transfer.

For data transmission, the CPU or direct memory access controller (DMAC) writes 32-bit transmit data to the transmit buffer (SPTXB). If the transmit shift register is empty, this module reverses the bit order in the 32-bit transmit data, copies it with MSB-aligned to the transmit shift register, and fills the transmit shift register. When data transmission is started, this module outputs data beginning at the MSB (bit 31) of the transmit shift register, and when the SPCLK clock cycle required for the serial transfer of 32 bits has passed, the transmit shift register becomes empty.

For data reception, data received from the data pin is stored in the receive shift register beginning at the LSB (bit 0). When the SPCLK clock cycle required for the serial transfer of 32 bits has passed, the receive shift register becomes full. If the receive buffer (SPRXB) has a space for 32 bits or more, this module reverses the order of the bits of the 32-bit data, copies it beginning at the LSB from the receive shift register to the receive buffer, and empties the receive shift register. If the receive buffer does not have a space for 32 bits or more in master mode, data reception is not carried out. In order to start reception, the specified length of data should be read from the receive buffer to secure the space for 32 bits or more in the receive buffer.

In actual transfer, this operation is repeated for the number of times defined by SPBMUL0 to SPBMUL3.



**Figure 47.8 LSB-First Transfer (32-Bit Data)**

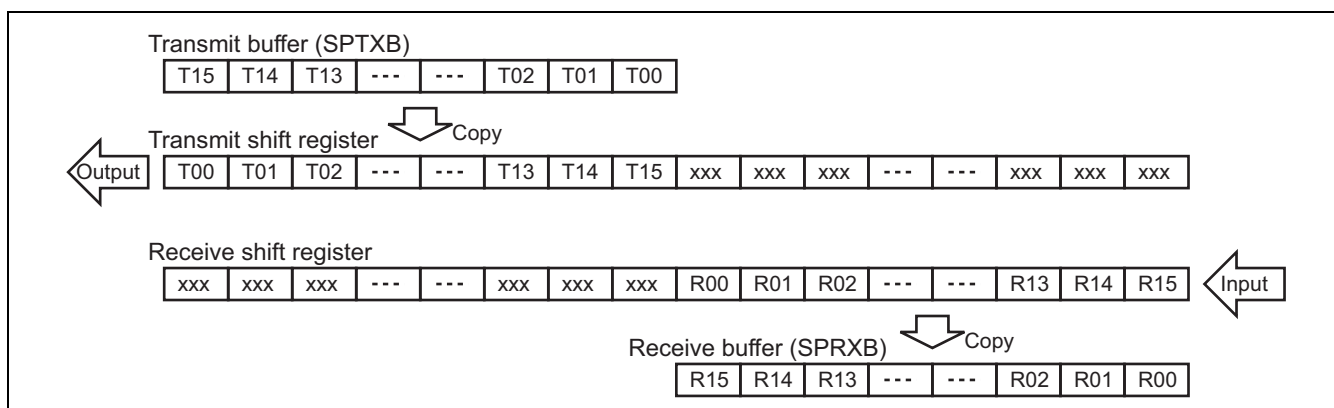
**(5) LSB-first transfer (16-bit data)**

Figure 47.9 shows the operation of the transmit buffer and transmit shift register, and the receive shift register and receive buffer when this module performs a 16-bit LSB-first data transfer.

For data transmission, the CPU or direct memory access controller (DMAC) writes 16-bit transmit data to the transmit buffer (SPTXB). If the transmit shift register is empty, this module reverses the bit order in the 16-bit transmit data, copies it with MSB-aligned to the transmit shift register, and fills the transmit shift register. When data transmission is started, this module outputs data beginning at the MSB (bit 31) of the transmit shift register, and when the SPCLK clock cycle required for the serial transfer of 16 bits has passed, the transmit shift register becomes empty.

For data reception, data received from the data pin is stored in the receive shift register beginning at the LSB (bit 0). When the SPCLK clock cycle required for the serial transfer of 16 bits has passed, the receive shift register becomes full. If the receive buffer (SPRXB) has a space for 16 bits or more, this module reverses the bit order in the 16-bit data, copies it beginning at the LSB from the receive shift register to the receive buffer, and empties the receive shift register. If the receive buffer does not have a space for 16 bits or more in master mode, data reception is not carried out. In order to start reception, the specified length of data should be read from the receive buffer to secure the space for 16 bits or more in the receive buffer.

In actual transfer, this operation is repeated for the number of times defined by SPBMUL0 to SPBMUL3.



**Figure 47.9 LSB-First Transfer (16-Bit Data)**

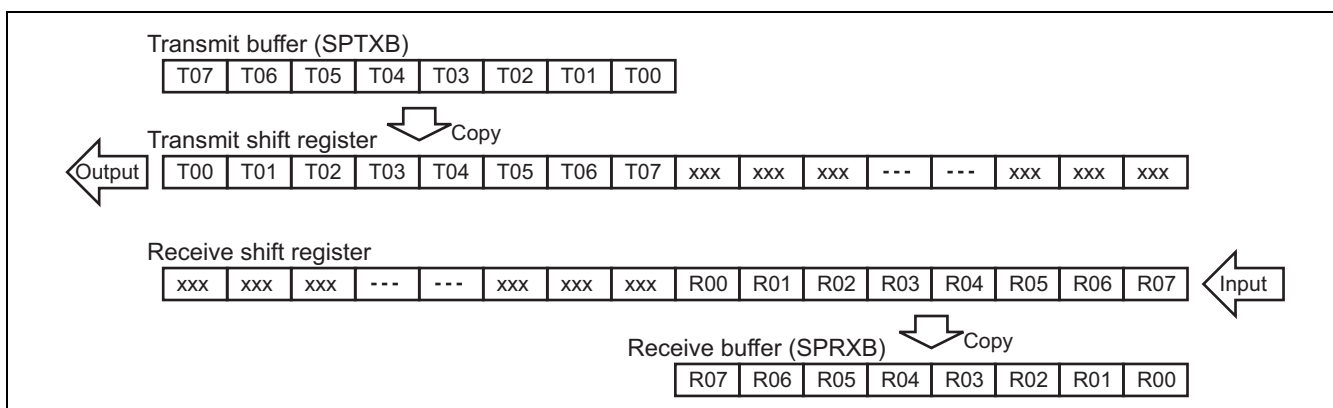
**(6) LSB-first transfer (8-bit data)**

Figure 47.10 shows the operation of the transmit buffer and transmit shift register, and the receive shift register and receive buffer when this module performs an 8-bit LSB-first data transfer.

For data transmission, the CPU or direct memory access controller (DMAC) writes 8-bit transmit data to the transmit buffer (SPTXB). If the transmit shift register is empty, this module reverses the bit order in the 8-bit transmit data, copies it with MSB-aligned to the transmit shift register, and fills the transmit shift register. When data transmission is started, this module outputs data beginning at the MSB (bit 31) of the transmit shift register, and when the SPCLK clock cycle required for the serial transfer of 8 bits has passed, the transmit shift register becomes empty.

For data reception, data received from the data pin is stored in the received shift register beginning at the LSB (bit 0). When the SPCLK clock cycle required for the serial transfer of 8 bits has passed, the receive shift register becomes full. If the receive buffer (SPRXB) has a space for 8 bits or more, this module reverses the bit order in the 8-bit data, copies it beginning at the LSB from the receive shift register to the receive buffer, and empties the receive shift register. If the receive buffer does not have a space for 8 bits or more in master mode, data reception is not carried out. In order to start reception, the specified length of data should be read from the receive buffer to secure the space for 8 bits or more in the receive buffer.

In actual transfer, this operation is repeated for the number of times defined by SPBMUL0 to SPBMUL3.



**Figure 47.10 LSB-First Transfer (8-Bit Data)**

### 47.5.5 Error Detection

In the normal serial transfer, the data written from SPDR to the transmit buffer is serially transmitted, and the serially received data can be read from the receive buffer of SPDR. If access is made to SPDR or serial transfer is started or completed, depending on the status of the transmit buffer/receive buffer, non-normal transfers may be executed in some cases.

This module detects certain types of non-normal transfers as underrun, overrun, or mode fault errors. Table 47.8 shows the relationship between non-normal transfer operations and the error detection function.

**Table 47.8 Relationship between Non-Normal Transfer Operations and Error Detection Function**

	<b>Occurrence Condition</b>	<b>Operation</b>	<b>Error Detection</b>
A	SPDR is written when the transmit buffer is full.	Missing write data.	Not detected
C	SPDR is read when the receive buffer is empty.	The output data is undefined.	Not detected

On operation A shown in Table 47.8, this module detects no error. Whether SPDR can be written to or not can be checked using the transmit data byte counter bits (TXBC[5:0]) in the buffer data count register (SPBDCR).

Similarly, on operation C shown in Table 47.8, this module detects no error. Whether the valid data is stored in the receive buffer or not can be checked by reading the receive data byte counter bits (RXBC[5:0]) in SPBDCR.

### 47.5.6 Initialization

If 0 is written to the SPE bit in SPCR, or a mode fault error is detected and the SPE bit is cleared to 0, this module disables the module function, and initializes a part of the module function. When a power-on reset is generated, this module initializes all of the module function.

When the SPE bit in SPCR is cleared to 0, this module performs the following initialization:

- Suspending any serial transfer that is being executed
- Initializing the transmit shift register and the receive shift register
- Initializing the internal state machine
- Initializing the sequence
- Initializing the TEND bit in SPSR

Initialization by clearing the SPE bit to 0 does not initialize the control bits of this module and the transmit/receive buffer. For this reason, this module can be started in the same transfer mode as prior to the initialization if the SPE bit is re-set to 1. However, clearing the SPE bit to 0 initializes the transmit shift register and the receive shift register and allows the data that is being transferred to be discarded.

### 47.5.7 SPI Operation

The operating modes of this module are listed below.

- Single-SPI master mode
- Dual-SPI mode/quad-SPI mode

The operation in each mode is described below.

#### (1) Single-SPI master mode

##### (a) Starting serial transfer

The serial transfer start conditions are: there is the specified length of data in the transmit buffer; and there is space for the specified length of data in the receive buffer.

##### (b) Terminating serial transfer

Irrespective of the clock setting, this module terminates the serial transfer after transmitting an SPCLK edge corresponding to the final sampling timing. After the serial transfer is completed, receive data is copied from the receive shift register to the receive buffer. If there is not enough space for the specified length of data in the receive buffer after receive data is copied from the receive shift register to the receive buffer, another serial transfer will not be performed.

##### (c) Sequence control

In single-SPI master mode, according to the sequence length that is assigned to the sequence control register (SPSCR), this module makes up a sequence comprised of a part or all of SPCMD0 to SPCMD3 and SPBMUL0 to SPBMUL3. This module contains a pointer to the SPCMD that makes up the sequence. The value of this pointer can be checked by reading SPSSR.

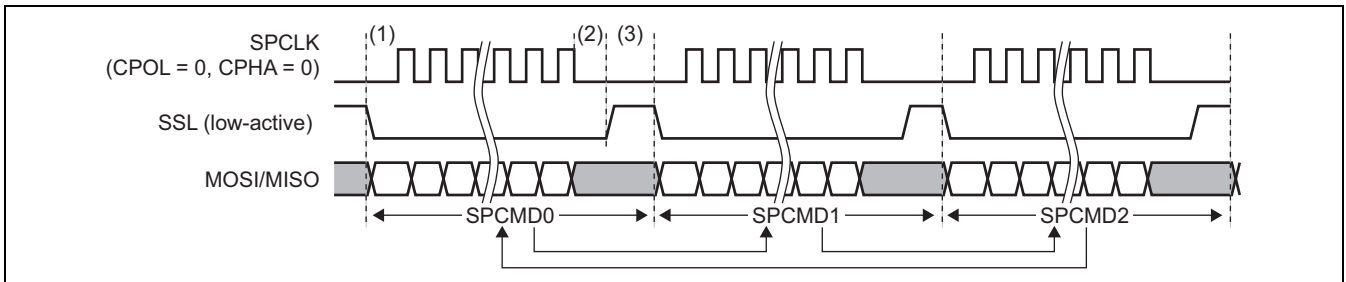
When the SPE bit in SPCR is set to 1 and the function of this module is enabled, this module loads the pointer to the commands in SPCMD0, and incorporates the SPCMD0 and SPBMUL0 settings into the transfer format at the beginning of serial transfer. This module increments the pointer each time the next-access delay period for a data transfer that corresponds to the referenced SPCMD0 to SPCMD3 ends. Upon completion of the serial transfer that corresponds to the final command comprising the sequence, this module sets the pointer in SPCMD0, and in this manner the sequence is executed repeatedly.



The following items are set in command registers SPCMD0 to SPCMD3: basic transfer data length, MSB or LSB first, clock settings, some of the bit rate settings, SPI transfer mode and transfer direction (only in dual-/quad-SPI modes), whether SSL level is held, a clock delay period, an SSL negation delay period, and a next-access delay period. The total amount of data to be transferred is determined by multiplying the basic length of data to be transferred by the value set with SPBMUL0 to SPBMUL3.

Figure 47.11 shows an operation example when SPSCR is set to H'02, and the sequence is configured based on SPCMD0 to SPCMD2 settings. In Figure 47.11, shaded areas of MOSI/MISO indicate invalid data. Periods (1) to (3) in Figure 47.11 indicate the followings.

- (1) Clock delay period (SPCKD) setting value = B'000 (one SPCLK cycle)
- (2) SSL negation delay period (SSLND) setting value = B'000 (one SPCLK cycle)
- (3) Next-access delay period (SPND) setting value = B'000 (one SPCLK cycle)



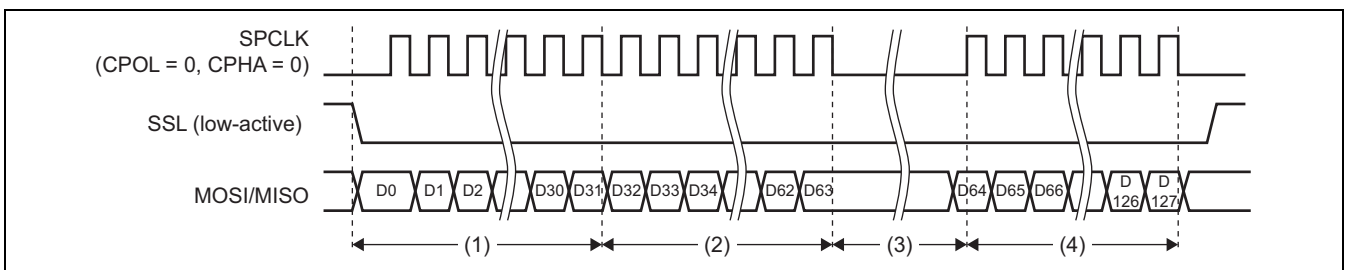
**Figure 47.11 Sequence Control Operation**

**(d) Burst transfer**

This module can execute burst transfer with the following two methods in single-SPI master mode.

One method uses the SPB[3:0] bits in SPCMD0 to SPCMD3 and SPBMUL0 to SPBMUL3. Setting SPB[3:0] to select 8, 16, or 32 bits and setting SPBMUL0 to SPBMUL3 to select one through 4,294,967,296 allows the specified length of data to be continuously transferred for the specified times, where the length is specified by SPB[3:0] and the number of times is specified by SPBMUL0 to SPBMUL3. However, if the transmit buffer (SPTXB) becomes empty during transfer, or the receive buffer (SPRXB) has no longer a space enough to receive the specified length of data defined by SPB[3:0], the clock is stopped until transfer is resumed. Figure 47.12 shows a burst transfer example in which SPB[3:0] are set to select 32 bits and SPBMUL to select four times thus specifying 128 bits as a total transfer data amount. The following describes operations (1) to (4) in the figure.

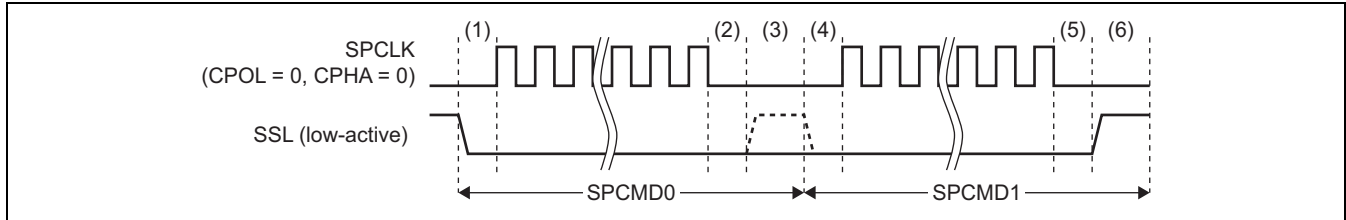
- (1) First 32-bit data transfer
- (2) Second 32-bit data transfer
- (3) When the transmit buffer becomes empty or the receive buffer has no longer a space for 32 or more bits, the clock is stopped. Here, the MOSI continues outputting the previous value. When data is written to the transmit buffer or an enough space is created in the receive buffer, the clock output is resumed to restart transfer.
- (4) Third and fourth 32-bit data transfer



**Figure 47.12 Burst Transfer Example in which Total Transfer Data Amount is 128 Bits (Single-SPI Master Mode Used)**

In the other method, SSL is kept asserted after a serial transfer is completed until the next serial transfer. Setting the SSL signal level keeping bit (SSLKP) to 1 in SPCMD0 to SPCMD3 allows the SSL signal to be kept asserted after the transfer corresponding to the pertinent command register is completed until the next transfer. Figure 47.13 shows a burst transfer example in which the SSL signal level keeping function is used. The following describes operations (1) to (6) in the figure.

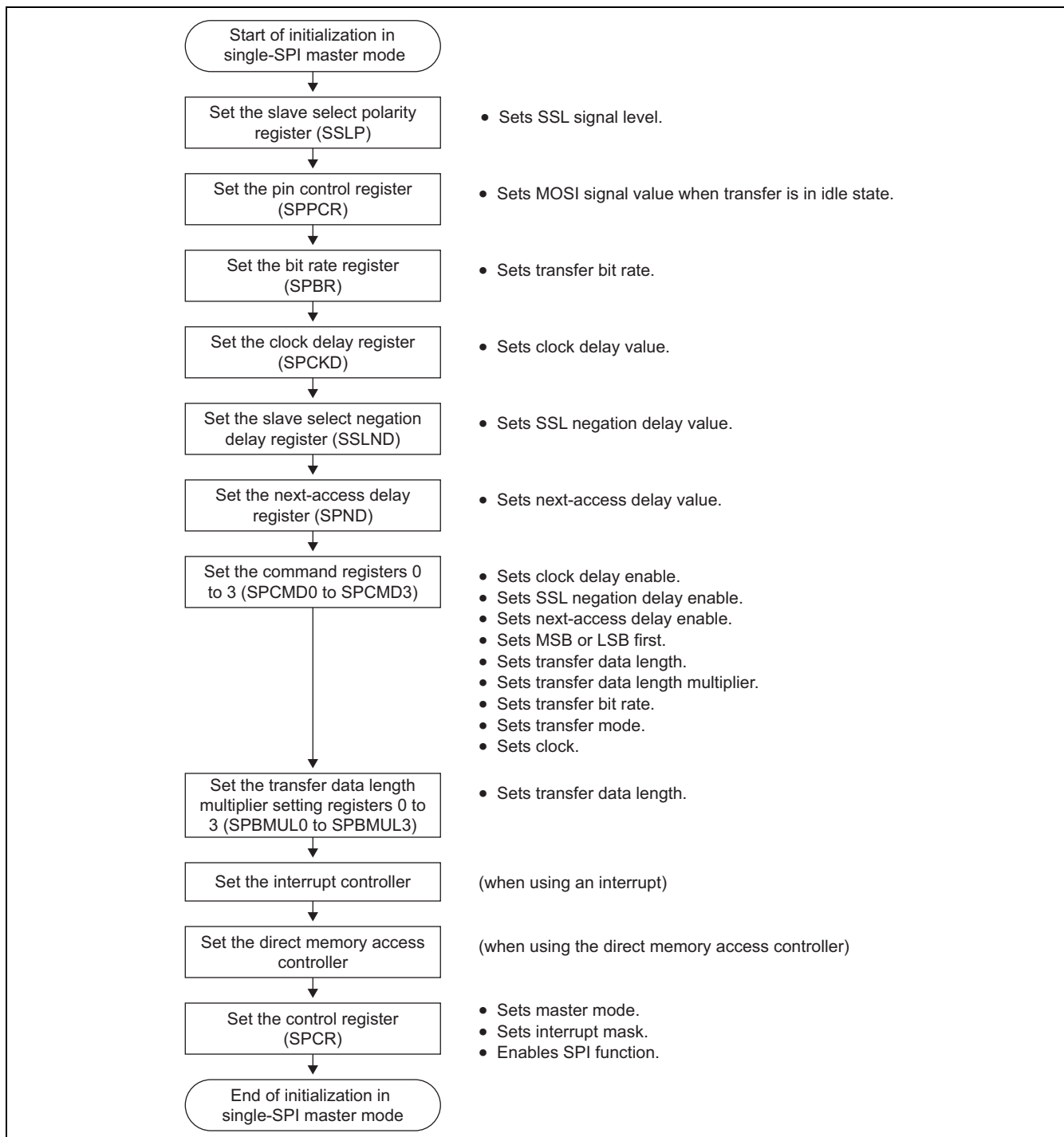
- (1) Clock delay period according to the SPCMD0 setting. The setting must be made so that the delay period should be at least one SPCLK cycle for the first transfer in the burst transfer.
- (2) SSL negation delay period according to the SPCMD0 setting. Since SSLKP is set to 1, SSL is not negated even after SSL negation delay period is over. The SSL negation delay period depends on the SLNDEN bit setting in SPCMD0. When SLNDEN is 1, the SSL negation delay period is determined by the SSLND setting, and the delay period is 0 SPCLK cycle when SLNDEN is 0.
- (3) Next-access delay period according to the SPCMD0 setting. Since SSLKP is set to 1, SSL is not negated even during the next-access delay period. The next-access delay period depends on the SPNDEN bit setting in SPCMD0. When SPNDEN is 1, the next-access delay period is determined by the SPND setting, and the delay period is 0 SPCLK cycle when SPNDEN is 0.
- (4) Clock delay period according to the SPCMD1 setting. The clock delay period depends on the SCKDEN bit setting in SPCMD1. When SCKDEN is 1, the clock delay period is determined by the SPCKD setting, and the delay period is 0 SPCLK cycle when SCKDEN is 0.
- (5) SSL negation delay period according to the SPCMD1 setting. The setting must be made so that the delay period should be at least one SPCLK cycle for the last transfer in the burst transfer. Since SSLKP in SPCMD1 is set to 0, SSL is negated after SSL negation delay period is over.
- (6) Next-access delay period according to the SPCMD1 setting. The setting must be made so that the delay period should be at least one SPCLK cycle for the last transfer in the burst transfer. Be sure to set SSLKP to 0 to negate SSL.



**Figure 47.13 Burst Transfer Example in which SSL Signal Level Keeping Function is Used (Single-SPI Mode)**

**(e) Initialization flowchart**

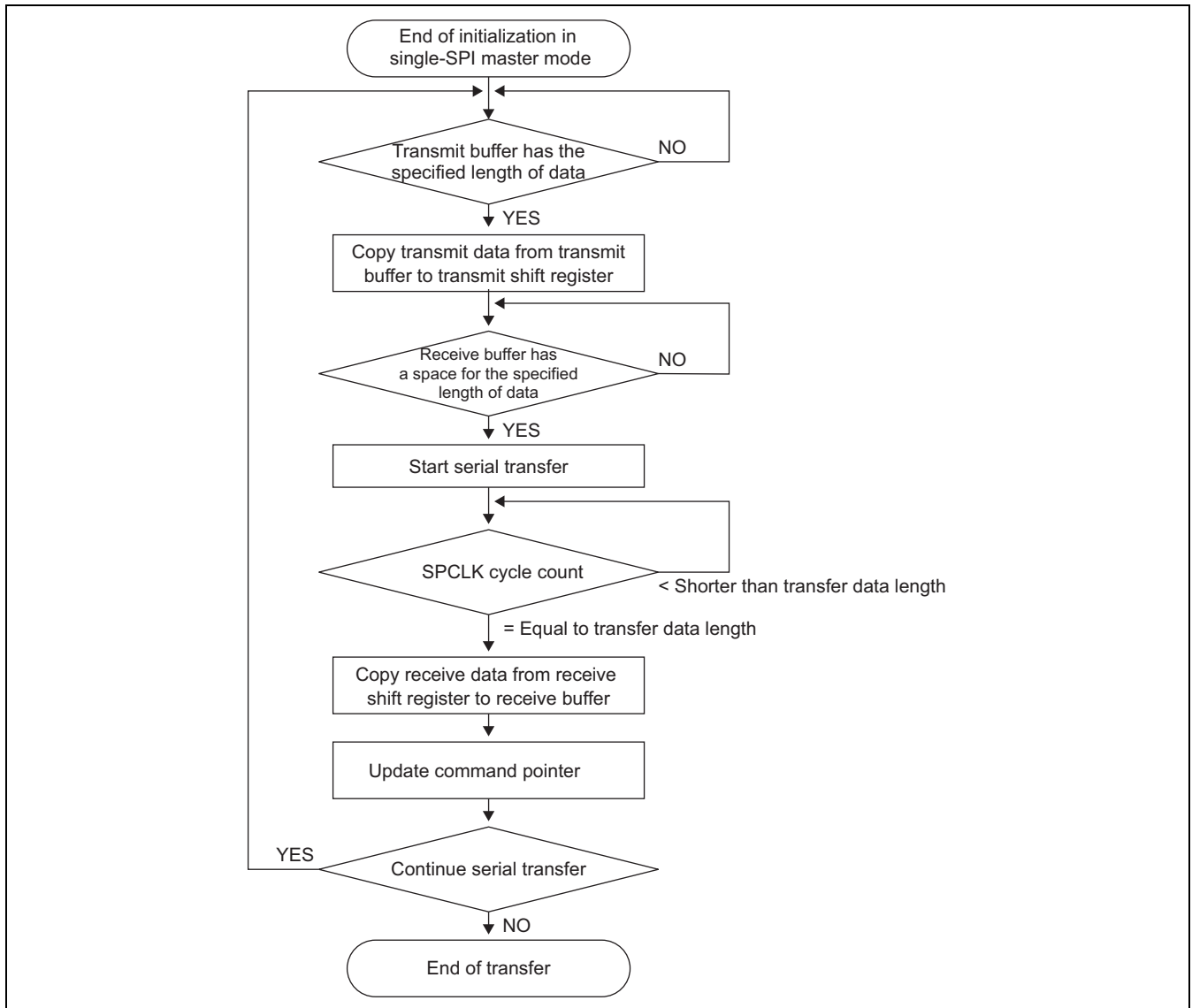
Figure 47.14 is a flowchart illustrating an example of initialization in SPI operation when this module is used in single-SPI master mode. For a description of how to set up the interrupt controller and direct memory access controller, see the descriptions given in the individual blocks.



**Figure 47.14 Example of Initialization Flowchart in Single-SPI Master Mode**

**(f) Transfer operation flowchart**

Figure 47.15 is a flowchart illustrating a transfer in SPI operation when this module is used in single-SPI master mode. Burst transfer by setting the transfer data length is also executed based on this flowchart.



**Figure 47.15 Transfer Operation Flowchart in Single-SPI Master Mode**

## (2) Dual-SPI/Quad-SPI mode

### (a) Starting serial transfer

In dual-/quad-SPI modes, the serial transfer start condition differs depending on the data transfer direction (transmission or reception).

In data transmission, the serial transfer start condition is that there is the specified length of data in the transmit buffer.

In data reception, the serial transfer start condition is that there is a space for the specified length of data in the receive buffer.

### (b) Terminating serial transfer

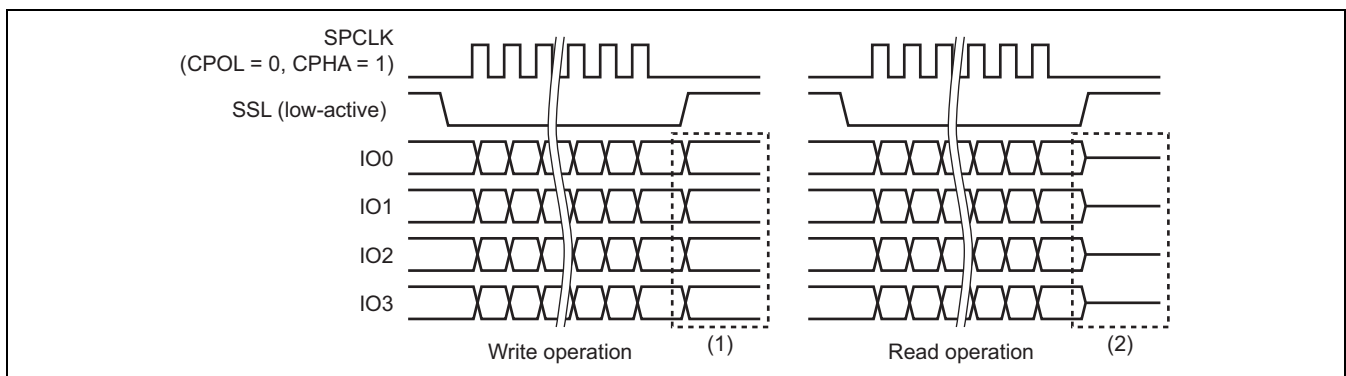
Irrespective of data transmission or reception, this module terminates the serial transfer after transmitting an SPCLK edge corresponding to the final sampling timing.

During idle cycles in dual-/quad-SPI modes, the IO pins are controlled differently depending on whether it is after write or read operation. Specifically, the IO pins output either the last output data or the fixed level depending on the register setting after write operation, whereas the IO pins are driven to the Hi-Z state after read operation. Figure 47.16 shows an example of the pin states after quad-SPI mode access is completed. The following describes operations (1) and (2) in the figure.

(1) During write operation, IO0 to IO3 serve as output pins. Thus, when SSL is negated upon completion of write operation, IO0 to IO3 output different values depending on the value of MOIFE in the SPPCR. Specifically, the IO pins output the level specified by MOIFV when MOIFE is 1, whereas the IO pins output the last output data when MOIFE is 0.

(2) During read operation, IO0 to IO3 serve as input pins. Thus, when SSL is negated upon completion of read operation, IO0 to IO3 are driven to Hi-Z state irrespective of the values of MOIFE and MOIFV.

For details on the pin control in dual-/quad-SPI modes, see section 47.5.2, Pin Control.

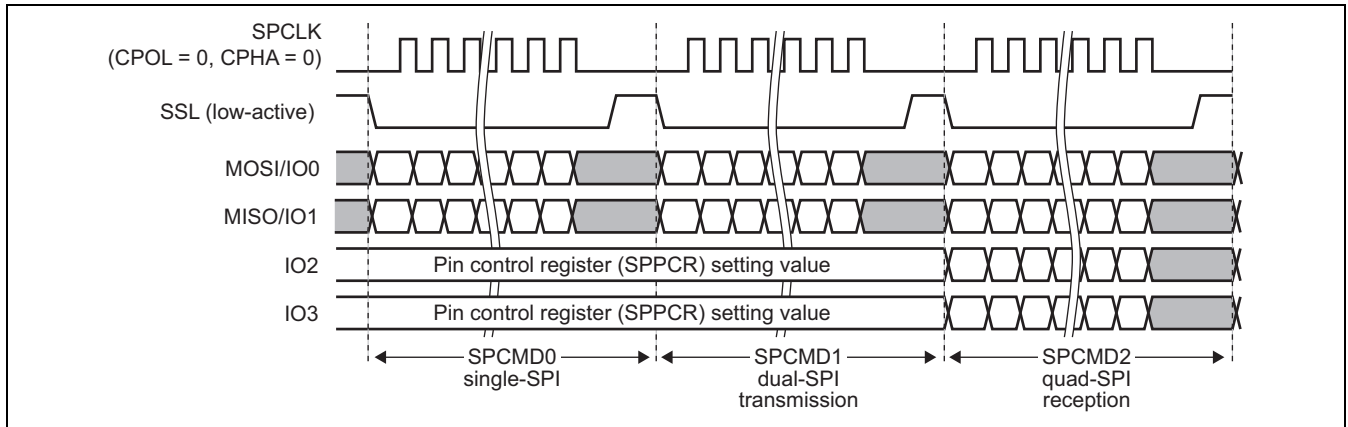


**Figure 47.16 Example of Pin States after Quad-SPI Mode Access is Completed**

### (c) Sequence control

As with the single-SPI master mode, in dual-/quad-SPI modes, according to the sequence length that is assigned to SPSCR, this module makes up a sequence comprised of SPCMD0 to SPCMD3 and SPBMUL0 to SPBMUL3. For details on operation, see section 47.5.7 (1) (c), Sequence control.

Dual-/quad-SPI modes only provide operation of a single direction, that is, either transmission or reception for serial transfer. Transmission or reception is set using the SPI read/write access setting bit (SPRW) in SPCMD0 to SPCMD3. One of the three operating modes including dual-SPI mode, quad-SPI mode, and single-SPI master mode is set using the SPI operating mode setting bits (SPIMOD[1:0]) in SPCMD0 to SPCMD3. Combining these bits allows switching single-SPI master mode, dual-SPI mode transmission/reception, and quad-SPI mode transmission/reception to control sequence. Figure 47.17 shows an example of sequence configuration with transfer mode switching.



**Figure 47.17 Example of Sequence Configuration with Transfer Mode Switching**

Note the following when configuring a sequence in dual-/quad-SPI modes.

When all the commands configuring a sequence are dual-/quad-SPI read operations, the sequential operation is continued as long as the receive buffer has an enough space for the receive data.

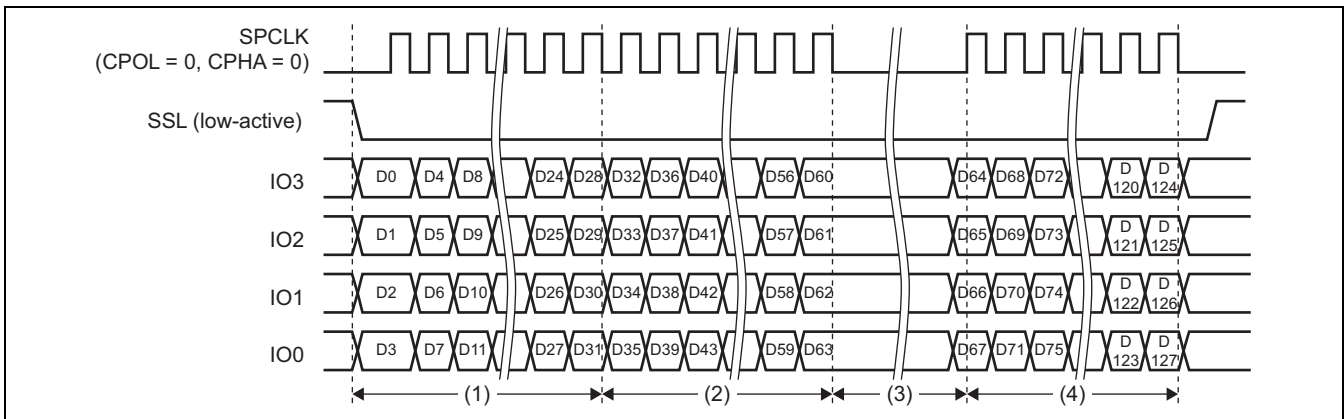
To terminate read operation, clear the SPE bit to 0 in SPCR after receiving the required length of data, or execute write operation for the last sequence to empty the transmit buffer.

**(d) Burst transfer**

This module can execute burst transfer with the following two methods in dual/quad SPI modes.

One method uses the SPB[3:0] bits in SPCMD0 to SPCMD3 and SPBMUL0 to SPBMUL3. As with the single-SPI master mode, setting SPB[3:0] to select 8, 16, or 32 bits and setting SPBMUL0 to SPBMUL3 to select one through 4,294,967,296 allows the specified length of data to be continuously transferred for the specified times, where the length is specified by SPB[3:0] and the number of times is specified by SPBMUL0 to SPBMUL3. However, if the transmit buffer (SPTXB) becomes empty during transfer, or the receive buffer (SPRXB) has no longer a space enough to receive the specified length of data defined by SPB[3:0], the clock is stopped until transfer is resumed. This method is effective to transfer a large amount of data in dual-/quad SPI modes. Figure 47.18 shows a burst transfer example in which SPB[3:0] are set to select 32 bits and SPBMUL to select four times thus specifying 128 bits as a total transfer data amount. The following describes operations (1) to (4) in the figure.

- (1) First 32-bit data transfer
- (2) Second 32-bit data transfer
- (3) When the transmit buffer becomes empty or the receive buffer has no longer a space for 32 or more bits, the clock is stopped. Here, when IO3 to IO0 serve as output pins, IO3 to IO0 continue outputting the previous value. When IO3 to IO0 serve as input pins, the inputs to IO3 to IO0 depend on the output value of the device to communicate with. When data is written to the transmit buffer or an enough space is created in the receive buffer, the clock output is resumed to restart transfer.
- (4) Third and fourth 32-bit data transfers

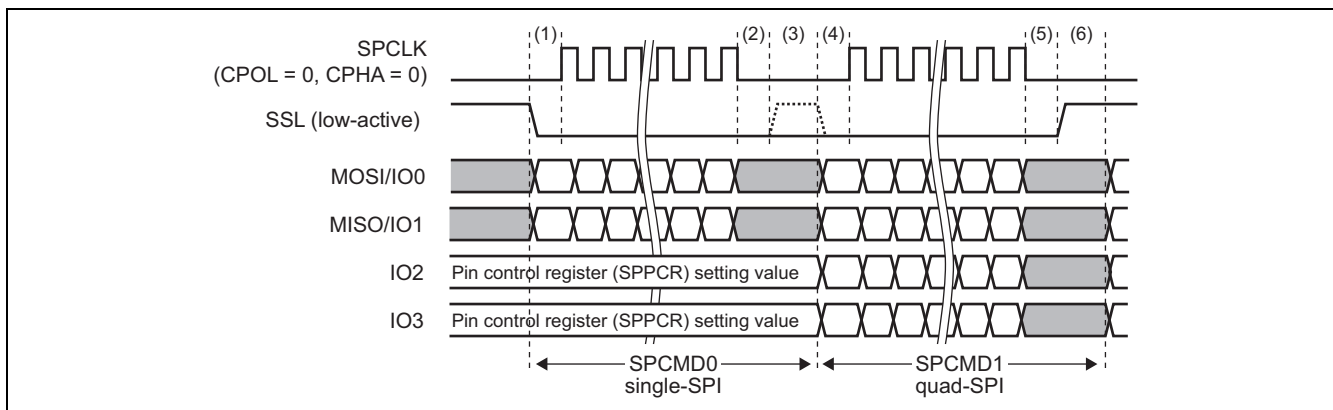


**Figure 47.18 Burst Transfer Example in which Total Transfer Data Amount is 128 Bits (Quad-SPI Mode)**

The other method uses the SSL signal level keeping function as in single-SPI master mode. Since this method allows switching the SPI transfer modes (single-/dual-/quad-SPI) during a transfer, it is particularly convenient when used with devices such as serial flash memory, where command data is written in single-SPI mode and data to be stored in memory is written in quad-SPI mode. Note, however, that at least one delay cycle should be inserted between transfers when switching the SPI transfer modes. Figure 47.19 shows a burst transfer example in which both single-SPI and quad-SPI modes are used. The following describes operations (1) to (6) in the figure.

- (1) Clock delay period according to the SPCMD0 setting. The setting must be made so that the delay period should be at least one SPCLK cycle for the first transfer in the burst transfer.
- (2) SSL negation delay period according to the SPCMD0 setting. Since SSLKP in SPCMD0 is set to 1, SSL is not negated even after SSL negation delay period is over. The SSL negation delay period depends on the SLNDEN bit setting in SPCMD0. When SLNDEN is 1, the SSL negation delay period is determined by the SSLND setting, and the delay period is 0 SPCLK cycle when SLNDEN is 0.
- (3) Next-access delay period according to the SPCMD0 setting. Since SSLKP is set to 1, SSL is not negated even during the next-access delay period. The next-access delay period depends on the SPNDEN bit setting in SPCMD0. When SPNDEN is 1, the next-access delay period is determined by the SPND setting, and the delay period is 0 SPCLK cycle when SPNDEN is 0.

- (4) Clock delay period according to the SPCMD1 setting. The clock delay period depends on the SCKDEN bit setting in SPCMD1. When SCKDEN is 1, the clock delay period is determined by the SPCKD setting, and the delay period is 0 SPCLK cycle when SCKDEN is 0.
- (5) SSL negation delay period according to the SPCMD1 setting. The setting must be made so that the delay period should be at least one SPCLK cycle for the last transfer in the burst transfer. Since SSLKP in SPCMD1 is set to 0, SSL is negated after SSL negation delay period is over.
- (6) Next-access delay period according to the SPCMD1 setting. The setting must be made so that the delay period should be at least one SPCLK cycle for the last transfer in the burst transfer. Be sure to set SSLKP to 0 to negate SSL.



**Figure 47.19 Burst Transfer Example in which SSL Signal Level Keeping Function is Used (Single- and Quad-SPI Modes Used)**



(e) Initialization flowchart

Figure 47.20 is a flowchart illustrating an example of initialization in SPI operation when this module is used in dual-/quad-SPI mode. For a description of how to set up the interrupt controller and direct memory access controller, see the descriptions given in the individual blocks.

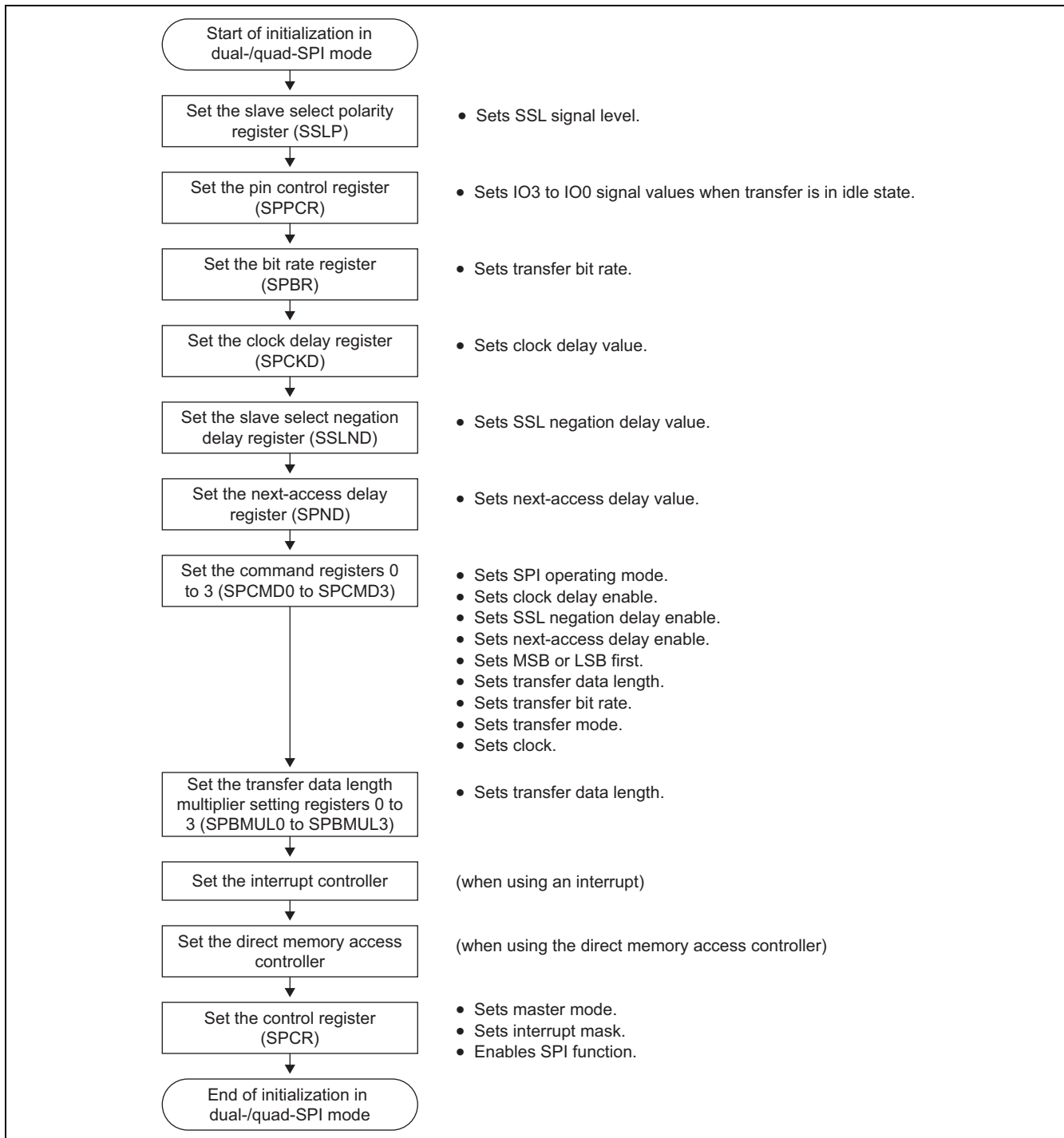


Figure 47.20 Example of Initialization Flowchart in Dual-/Quad-SPI Mode

(f) Transfer operation flowchart

Figure 47.21 is a flowchart illustrating a transfer in SPI operation when this module is used in dual-/quad-SPI mode.

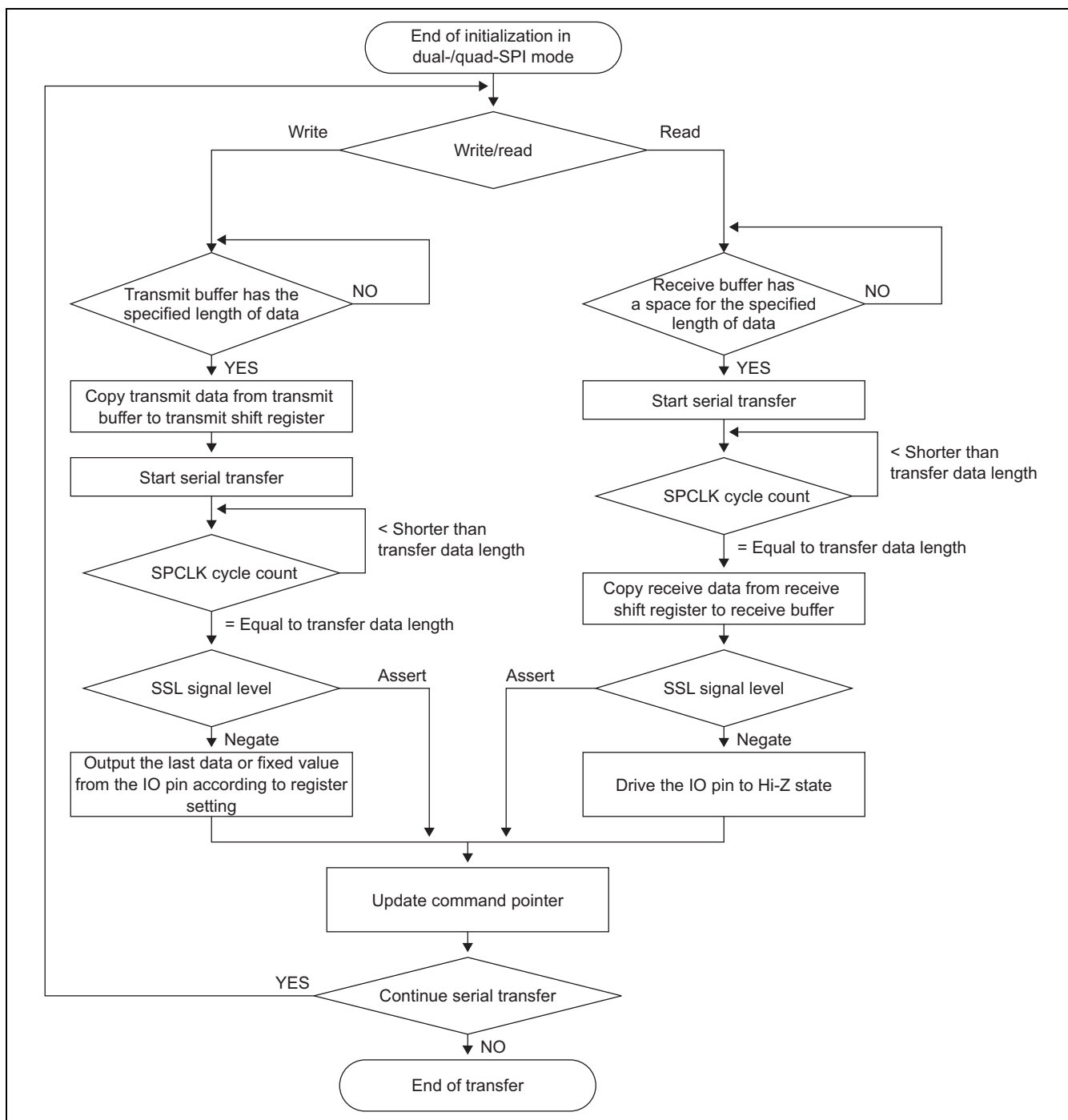


Figure 47.21 Transfer Operation Flowchart in Dual-/Quad-SPI Mode

### 47.5.8 Interrupt Sources

This module has interrupt sources of receive buffer full, transmit buffer empty, underrun error, overrun error, and mode fault error. In addition, the direct memory access controller can be activated by the receive buffer full or transmit buffer empty interrupt for data transfer.

Table 47.9 shows the interrupt sources.

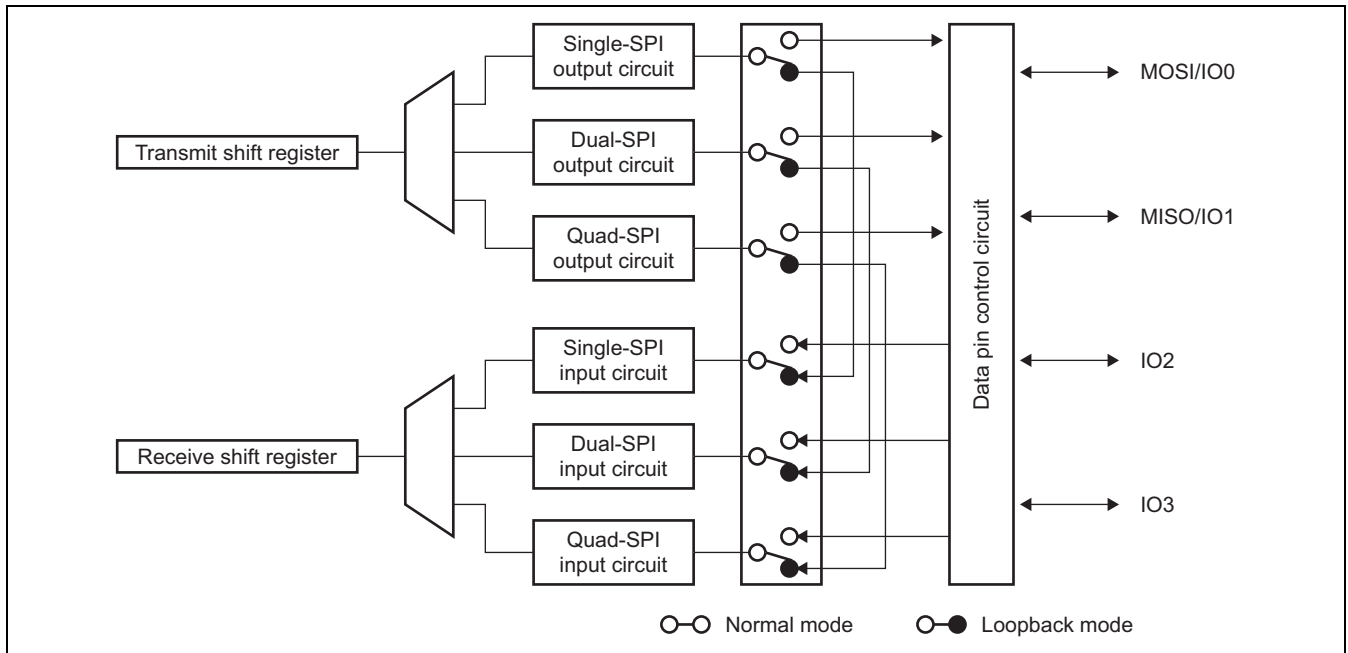
When any of the interrupt conditions in Table 47.9 is met, an interrupt is generated. The interrupt sources should be cleared with data transfer by the CPU or direct memory access controller.

**Table 47.9 Interrupt Sources**

Name	Interrupt Source	Abbreviation	Interrupt Condition	Activation of Direct Memory Access Controller
SPRI	Receive buffer full	RXI	SPRIE = 1 and SPRFF = 1	Possible
SPTI	Transmit buffer empty	TXI	SPTIE = 1 and SPTEF = 1	Possible
SPEI	Underrun error	UDI	SPEIE = 1 and UDRF = 1	Not possible
	Overrun error	OVI	SPEIE = 1 and OVRF = 1	Not possible
	Mode fault error	MOI	SPEIE = 1 and MODF = 1	Not possible

### 47.5.9 Loopback Mode

This module provides loopback mode for testing. Writing 1 to the loopback mode bit (SPLP) in the pin control register (SPPCR) enables loopback mode. In loopback mode, this module disconnects the paths between the transmit/receive shift registers and the MISO/MOSI and IO3 to IO0 pins, and connects the outputs from the transmit shift register to the inputs to the receive shift register instead. Figure 47.22 shows a schematic internal connection in loopback mode.



**Figure 47.22 Schematic Internal Connection in Loopback Mode**

## 48. SD Card Host Interface (SDHI)

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

### 48.1 Overview

This LSI provides an SD card host interface (SDHI) module.

This section only introduces the features of the SDHI module. Contact your local Renesas sales representative if you need detailed information on the SDHI module, including registers, usage, and other information.

Note: The number of interfaces depends on the product.  
The RZ/G1H has four, and RZ/G1M/N and RZ/G1E have three interface.

#### 48.1.1 Features

- SD memory or I/O card interface (1-bit or 4-bit SD bus)
- SD clock frequency  $\leq 195$  MHz (for interfaces 0 and 1) (SDR104)  
SD clock frequency  $\leq 97.5$  MHz (for interfaces 2 and 3) (SDR50)
- Error check functions: CRC7 (command and response) and CRC16 (data)
- Authentication and encryption/decryption function: Not available
- Interrupt requests: Card access interrupt, SDIO access interrupt, and card detection interrupt
- DMA transfer request: SD\_BUF write/SD\_BUF read
- Support for four cards (with simultaneous operation possible)
- SDXC supported
- Card detection function
- Write protection supported

	RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
SDR104	√ <sup>1</sup>	√ <sup>2</sup>	√ <sup>2</sup>	√ <sup>2</sup>
SDR50	√	√	√	√
High-speed	√	√	√	√
Default	√	√	√	√

Notes: 1. Interfaces 0 and 1  
2. Interface 0

Figures 48.1 to 48.2 are block diagrams of the SDHI.

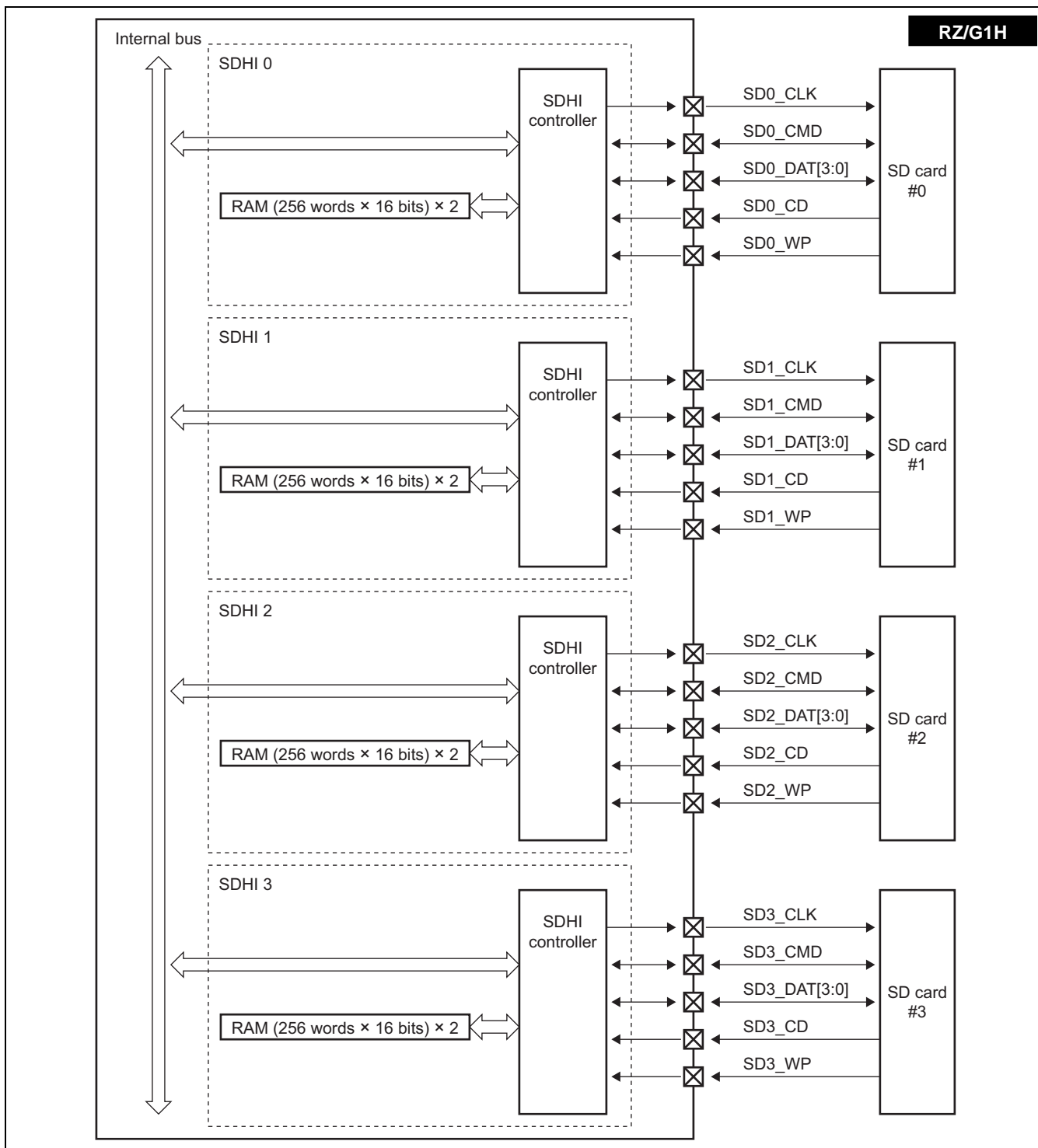


Figure 48.1 Block Diagram of SDHI [RZ/G1H]

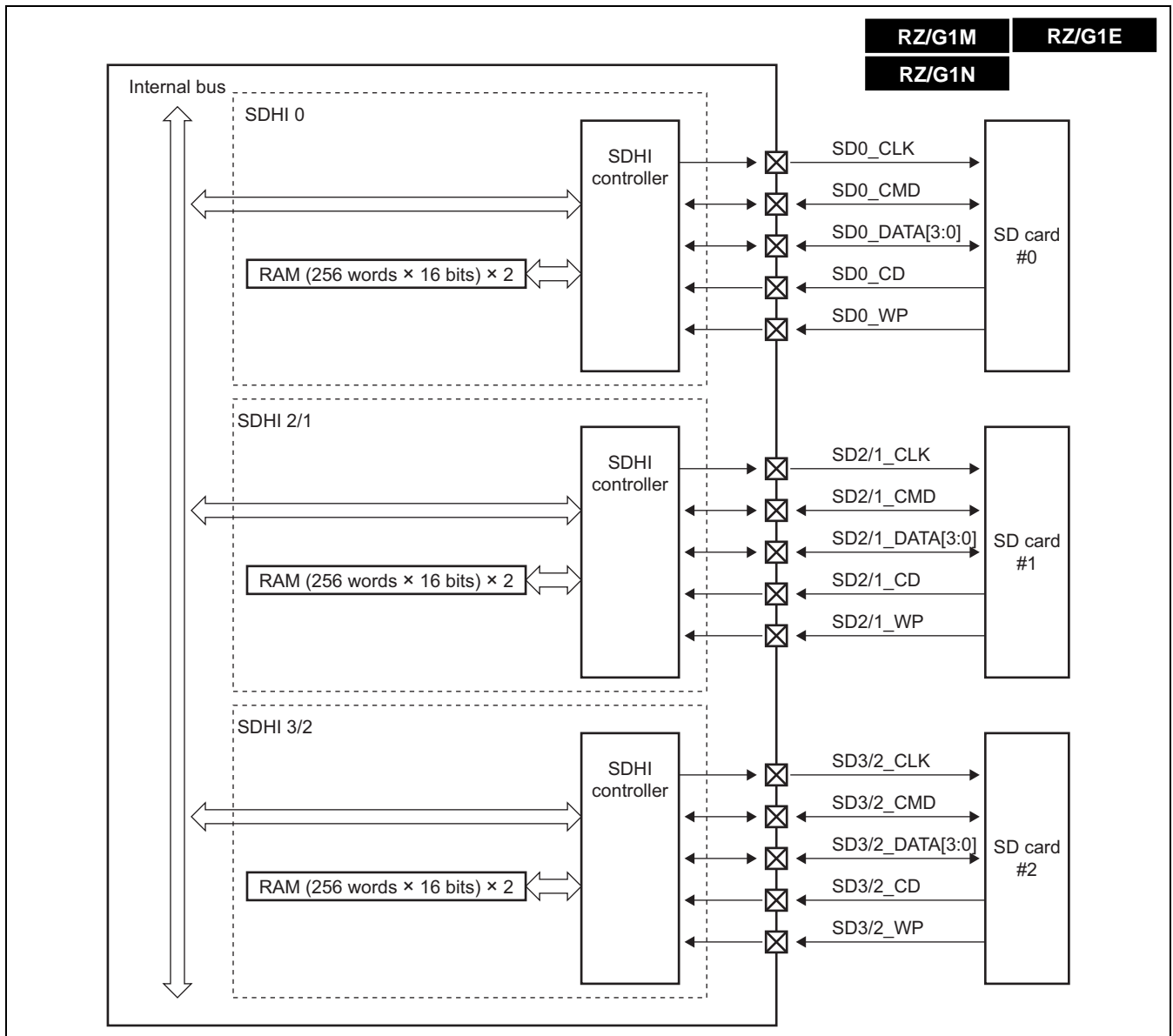


Figure 48.2 Block Diagram of SDHI [RZ/G1M, N, E]

### 48.1.2 Input/Output Pins

**Table 48.1 Pin Configuration**

				<u>RZ/G Series Products</u>			
Pin Name	Function	I/O	Description	RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
SDn_CLK	SD clock	Output	SD clock	√	√	√	√
SDn_CMD	Command response signal	Input/output	Command/response	√	√	√	√
SDn_DAT0 or SDn_DATA0	Data input/output	Input/output	Data [bit 0]	√	√	√	√
SDn_DAT1 or SDn_DATA1	Data input/output SDIO interrupt	Input/output	Data [bit 1]/SDIO interrupt	√	√	√	√
SDn_DAT2 or SDn_DATA2	Data input/output Read wait	Input/output	Data [bit 2]/read wait	√	√	√	√
SDn_DAT3 or SDn_DATA3	Data input/output card detection	Input/output	Data [bit 3]/card detection	√	√	√	√
SDn_CD	Card detection	Input	Card detection	√	√	√	√
SDn_WP	Write protection	Input	Write protection	√	√	√	√

Note: n = 0 to 3 [RZ/G1H], n = 0, 2, 3 [RZ/G1M, N], n = 0 to 2 [RZ/G1E]

### 48.1.3 Register Description

**Table 48.2 Register Configuration**

		<u>RZ/G Series Products</u>			
Register	Address	RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
SDHI 0	H'00 EE100000 to H'00 EE11FFFF	√	√	√	√
SDHI 1	H'00 EE120000 to H'00 EE13FFFF	√	—	—	—
SDHI 2 (SDHI 1*)	H'00 EE140000 to H'00 EE15FFFF	√	√	√	√
SDHI 3 (SDHI 2*)	H'00 EE160000 to H'00 EE17FFFF	√	√	√	√

Note: \* Applicable to the RZ/G1E.



## 49. Multi Media Card Interface (MMC)

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

### 49.1 Overview

#### 49.1.1 Features

##### (1) MMC interface

- Compliant with JEDEC STANDARD JESD84-A441 (neither DDR mode nor 1.8-V operation is supported)
- Supports 1-/4-/8-bit MMC bus width
- MMC clock frequency = MMCxf clock frequency/ $2^n$  (n = 1 to 10)
- Supports block transfer\*<sup>1</sup>
- Supports boot operation\*<sup>2</sup>
- MMC clock frequency settings are adjustable in boot mode.
- Supports high priority interrupt (HPI)\*<sup>3</sup>
- Supports background operation
- Two types of interrupt requests: normal operation interrupts and error/timeout interrupts
- DMA transfer requests: buffer write and buffer read

Notes: 1. Stream transfer is not supported.

2. The alternative boot operation is not supported.

3. HPIs in the sequence of CMD6, CMD24, CMD25 (pre-defined), and CMD38 are supported.

#### 49.1.2 Block Diagram

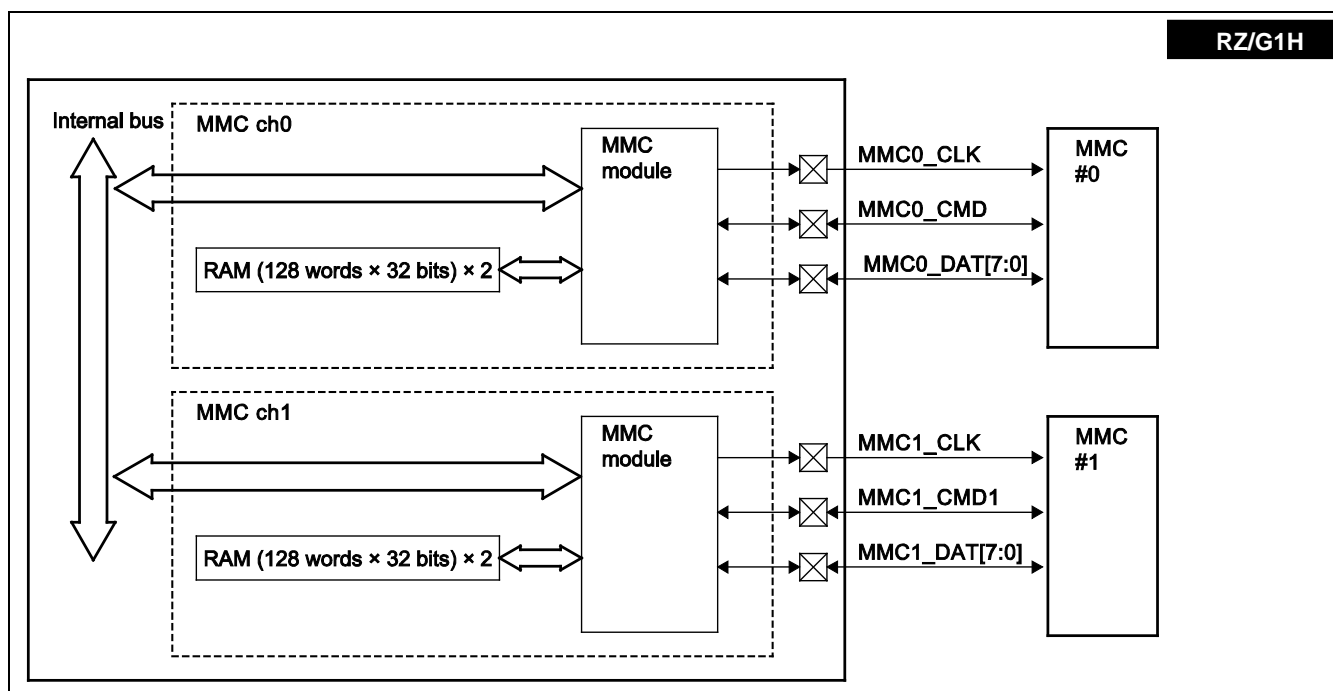


Figure 49.1 Block Diagram of MMC [RZ/G1H]

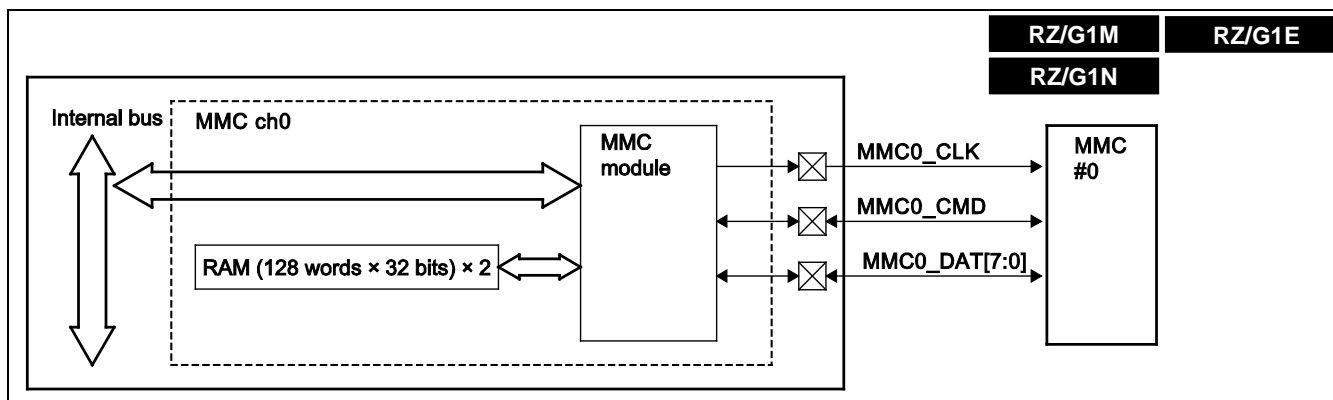


Figure 49.2 Block Diagram of MMC [RZ/G1M, RZ/G1N, RZ/G1E]

### 49.1.3 External Pins

Table 60.1 shows the pin configuration of the MMC.

Table 49.1 Pin Configuration

Name	Pin Name*	I/O	Function	RZ/G Series Products			
				RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
MMCCLK	MMcN_CLK	Output	MMC clock	√	√	√	√
MMCCMD	MMcN_CMD	Input/output	MMC command/response	√	√	√	√
MMCDAT[7:0]	MMcN_D[7:0]	Input/output	MMC data [7:0]	√	√	√	√

Note: \* n represents 0 or 1.

#### 49.1.4 Register Configuration

Table 60.2 shows the register configuration of the MMC.

The base address of each channel is as follows:

Channel 0: H'EE20\_0000

Channel 1: H'EE22\_0000\*

Note: \* Channel 1 applies to only RZ/G1H.

**Table 49.2 Register Configuration**

Register Name	Abbreviation	R/W	Address	Initial Value	Access Size	RZ/G Series Products			
						RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Command setting register	CE_CMD_SET	R/W	H'00	H'0000_0000	16, 32	√	√	√	√
Argument register	CE_ARG	R/W	H'08	H'0000_0000	16, 32	√	√	√	√
Argument register for automatically-issued CMD12	CE_ARG_CMD12	R/W	H'0C	H'0000_0000	16, 32	√	√	√	√
Command control register	CE_CMD_CTRL	R/W	H'10	H'0000_0000	16, 32	√	√	√	√
Transfer block setting register	CE_BLOCK_SET	R/W	H'14	H'0000_0200	16, 32	√	√	√	√
Clock control register	CE_CLK_CTRL	R/W	H'18	H'0000_0000	16, 32	√	√	√	√
Buffer access configuration register	CE_BUF_ACC	R/W	H'1C	H'0000_0000	16, 32	√	√	√	√
Response register 3	CE_RESP3	R	H'20	H'0000_0000	16, 32	√	√	√	√
Response register 2	CE_RESP2	R	H'24	H'0000_0000	16, 32	√	√	√	√
Response register 1	CE_RESP1	R	H'28	H'0000_0000	16, 32	√	√	√	√
Response register 0	CE_RESP0	R	H'2C	H'0000_0000	16, 32	√	√	√	√
Response register for automatically-issued CMD12	CE_RESP_CMD12	R	H'30	H'0000_0000	16, 32	√	√	√	√
Data register	CE_DATA	R/W	H'34	H'0000_0000	16*1, 32	√	√	√	√
Boot operation setting register	CE_BOOT	R/W	H'3C	H'0000_0000	16, 32	√	√	√	√
Interrupt flag register	CE_INT	R/(W)*2	H'40	H'0000_0000	16, 32	√	√	√	√
Interrupt enable register	CE_INT_EN	R/(W)*2	H'44	H'0000_0000	16, 32	√	√	√	√
Status register 1	CE_HOST_STS1	R	H'48	H'X0XX_0000	16, 32	√	√	√	√
Status register 2	CE_HOST_STS2	R	H'4C	H'0000_0000	16, 32	√	√	√	√
Clock control register 2	CE_CLK_CTRL2	R/W	H'70	H'00X0_XX00	16, 32	√	√	√	√
Version register	CE_VERSION	R/W	H'7C	H'0000_0003	16, 32	√	√	√	√
Data output phase select register	CE_ODATSEL	R/W	H'80	H'0000_0000	16, 32	√	√	√	√

Notes: Do not write to addresses other than those listed above. Otherwise, correct operation is not guaranteed.

1. For 16-bit access, H'34 is the only address for access.

2. Only 0 can be written to clear the flag.

## 49.2 Register Description

The registers of the MMC interface are assigned to and arranged in the internal bus address space.

### Legend for register description:

Initial value: Register value after a reset

$\frac{3}{4}$ : Undefined value

R/W: Readable/writable. The written value can be read.

R/WC0: Readable/writable. Writing 0 initializes the bit. Writing 1 is ignored.

R/WC1: Readable/writable. Writing 1 initializes the bit. Writing 0 is ignored.

R: Read-only.

$\frac{3}{4}$ /WB: Write-only. The read value is undefined.

### 49.2.1 Command Setting Register (CE\_CMD\_SET)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CE\_CMD\_SET sets a command sequence. For the setting values of CE\_CMD\_SET, see section 60.3.4 (13), Setting values of CE\_CMD\_SET. The command sequence starts when the settings have been made in bits 31 to 16. Note that writing to CE\_CMD\_SET is disabled while a command sequence is proceeding (the CMDSEQ bit in CE\_HOST\_STS1 is 1).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	BOOT	CMD[5:0]							RTYP[1:0]	RBSY	—	WDAT	DWEN	CMLTE	CMD 12EN
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RIDXC[1:0]	RCRC7C[1:0]	—	CRC 16C	BOOT ACK	CRC STE	TBIT	OPDM	—	—	SBIT	—	DATW[1:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	¾	0	R	Reserved The write value should always be 0.
30	BOOT	0	R/W	Boot Operation 0: Command sequence other than for boot operations 1: Command sequence for boot operations
29 to 24	CMD[5:0]	H'00	R/W	Command Index Set a command index ([45:40]).
23, 22	RTYP[1:0]	00	R/W	Response Type 00: No response 01: 6-byte response (R1, R1b, R3, R4, R5) 10: 17-byte response (R2) 11: Setting prohibited
21	RBSY	0	R/W	Response Busy Select Selects whether "busy" is involved in response reception. 0: No response busy 1: Response busy involved (R1b)
20	¾	0	R/W	Reserved The write value should always be 0.
19	WDAT	0	R/W	Presence/Absence of Data 0: No data 1: With data
18	DWEN	0	R/W	Read/Write (valid when "with data" is selected) 0: Read from the card. 1: Write to the card.

Bit	Bit Name	Initial Value	R/W	Description
17	CMLTE	0	R/W	Single/Multi Block Transfer Select (valid when "with data" is selected) 0: Single-block transfer 1: Multi-block transfer
16	CMD12EN	0	R/W	Automatic CMD12 Issuance (valid when multi-block transfer is selected)* 0: Disables automatic CMD12 issuance. 1: Enables automatic CMD12 issuance. For details of automatic CMD12 issuance, see section 60.3.3 (4), Automatic CMD12 issuance. Note: Set the transfer block size to 512 bytes. Set the RBSY bit to 0.
15, 14	RIDXC[1:0]	00	R/W	Response Index Check Specify the items to be checked in bits [45:40] of a 6-byte response or bits [133:128] of a 17-byte response. 00: Checks the response index (check whether matched with a command index). 01: Checks the check bits (check whether all the bits are set to 1). 10: No checking 11: Setting prohibited
13, 12	RCRC7C [1:0]	00	R/W	Response CRC7 Check Specify the items to be checked in bits [7:1] of a 6-byte response or of a 17-byte response. 00: Checks CRC7 (set the response type to 01). 01: Checks the check bits (check whether all the bits are set to 1) (set the response type to 01). 10: Checks internal CRC7 (R2 only) (set the response type to 10). 11: No checking
11	$\frac{3}{4}$	0	R/W	Reserved The write value should always be 0.
10	CRC16C	0	R/W	CRC16 Check in Reception (valid when "with data" and "read" are selected) 0: Checks CRC16 in reception. 1: Does not check CRC16 in reception (used when CMD14).
9	BOOTACK	0	R/W	Receive Boot Acknowledge (valid in boot mode) 0: Boot acknowledge is not received. 1: Boot acknowledge is received.
8	CRCSTE	0	R/W	CRC Status Reception (valid when "with data" and "write" are selected) 0: Receives CRC status. 1: Does not receive CRC status (used when CMD19).
7	TBIT	0	R/W	Transmission Bit Setting 0: Sets the transmission bit ([46]) to 1. 1: Sets the transmission bit ([46]) to 0.
6	OPDM	0	R/W	Open-Drain Output Mode 0: Normal output 1: Open-drain output Note: This setting is only applied to the MMC_CMD line.

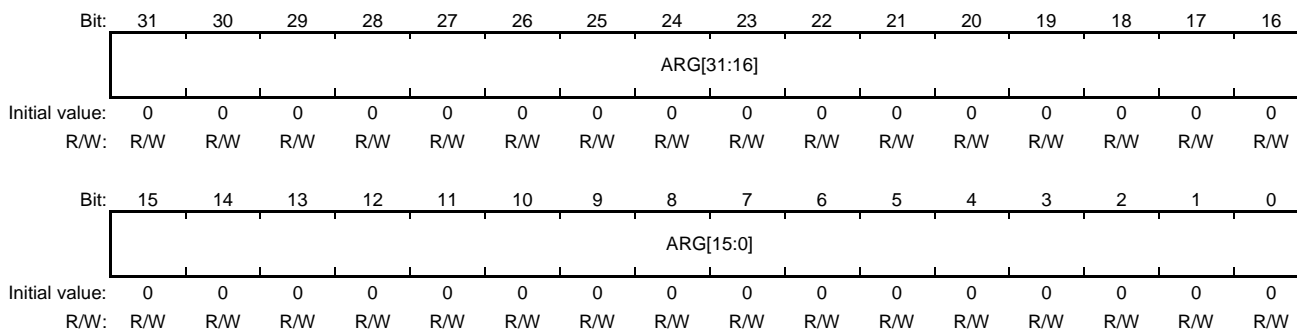
Bit	Bit Name	Initial Value	R/W	Description
5	$\frac{3}{4}$	0	R/W	Reserved The write value should always be 0.
4	$\frac{3}{4}$	0	R	Reserved The write value should always be 0.
3	SBIT	0	R/W	Read Data Start Bit Detection Setting (valid when "with data" and "read" are selected) 0: Detects a start bit when the valid MMCDAT signals specified by the DATW bits are all 0. 1: Detects a start bit when MMCDAT[0] is 0.
2	$\frac{3}{4}$	0	R/W	Reserved The write value should always be 0.
1, 0	DATW[1:0]	00	R/W	Data Bus Width Setting (valid when "with data" is selected) 00: 1 bit 01: 4 bits 10: 8 bits 11: Setting prohibited

Note: \* It is recommended to use the pre-defined multi-block transfer by setting this bit to 0 for a higher data transfer rate.

### 49.2.2 Argument Register (CE\_ARG)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CE\_ARG sets the argument for the command to be transmitted. Set this register before starting a command sequence.

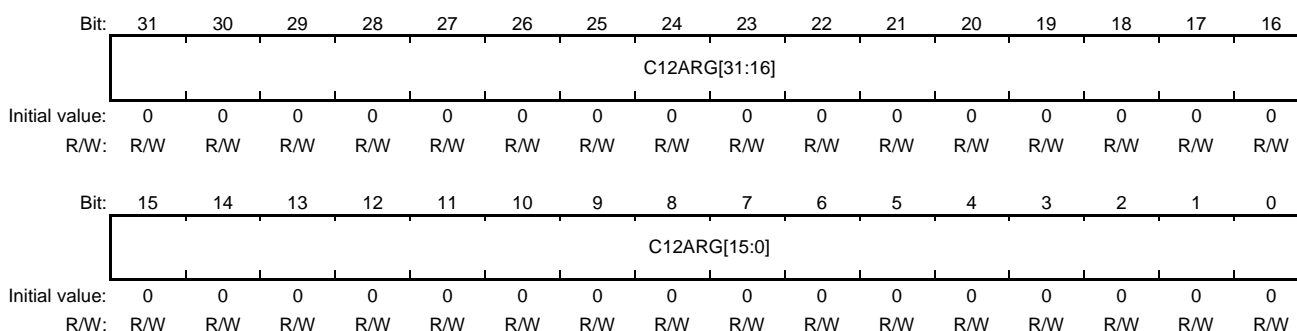


Bit	Bit Name	Initial Value	R/W	Description
31 to 0	ARG[31:0]	All 0	R/W	Set bits [39:8] of the command. Note: Set the argument of automatically-issued CMD12 by CE_ARG_CMD12.

### 49.2.3 Argument Register for Automatically-Issued CMD12 (CE\_ARG\_CMD12)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CE\_ARG\_CMD12 is used to set the argument for the automatically-issued CMD12. This register is valid when issuing CMD12 automatically in multi-block transfer. For automatic issuance of CMD12, see section 60.3.3 (4), Automatic CMD12 issuance. Set this register before starting a command sequence.



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	C12ARG[31:0]	All 0	R/W	Set bits [39:8] of the automatically-issued CMD12.



#### 49.2.4 Command Control Register (CE\_CMD\_CTRL)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CE\_CMD\_CTRL is used to terminate a command sequence forcibly.

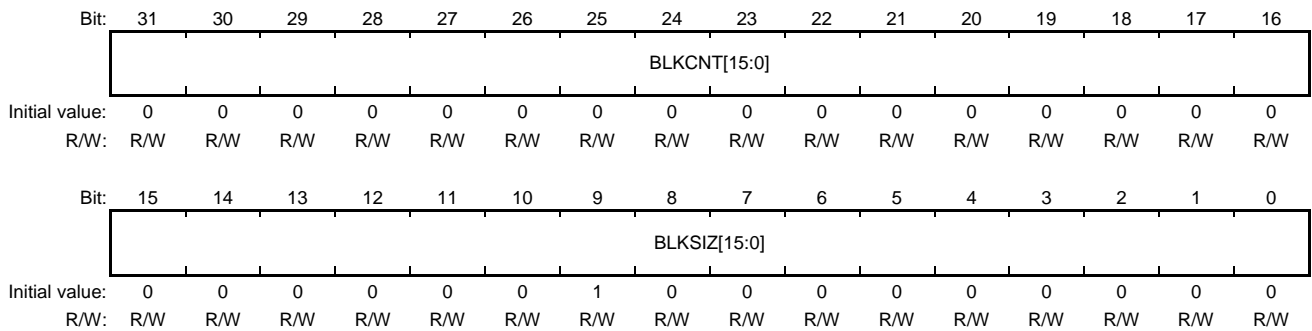
Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	BREAK
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	$\frac{3}{4}$	All 0	R	Reserved The write value should always be 0.
15 to 2	$\frac{3}{4}$	All 0	R	Reserved The write value should always be 0.
1	$\frac{3}{4}$	0	R/W	Reserved The write value should always be 0.
0	BREAK	0	R/W	Forcible Termination of Command Sequence Writing 1 to this bit while it is 0 and then writing 0 to it discontinues the current command sequence. After this bit is set as described above, check if the value of the CMDSEQ bit in CE_HOST_STS1 has become 0. If this is the case, execute software reset. Note: A software reset initializes the value of this register, so the setting in this register needs to be remade.

### 49.2.5 Transfer Block Setting Register (CE\_BLOCK\_SET)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CE\_BLOCK\_SET specifies the size of the block and the number of blocks for the data to be transferred. Set this register before starting a command sequence.



Bit	Bit Name	Initial Value	R/W	Description
31 to 16	BLKCNT[15:0]	H'0000	R/W	Number of Blocks for Transfer Note: This setting is valid for multi-block transfer.
15 to 0	BLKSIZ[15:0]	H'0200	R/W	Transfer Block Size Note: Transfer block size should be set as follows. <ul style="list-style-type: none"> <li>· Single-block transfer: 1 to 512 bytes</li> <li>· Multi-block transfer: 512 bytes</li> </ul>

### 49.2.6 Clock Control Register (CE\_CLK\_CTRL)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CE\_CLK\_CTRL controls the MMC clock and sets timeout values. Do not change the setting of this register while a command sequence is in progress.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	CLKEN	—	—	—	—	CLKDIV[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R	R	R	R	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	SRSPTO[1:0]		SRBSYTO[3:0]			SRWDTO[3:0]			—	—	—	—		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 25	$\frac{3}{4}$	All 0	R	Reserved The write value should always be 0.
24	CLKEN	0	R/W	MMC Clock Output Control 0: Does not output the MMC clock (fixed to low level). 1: Outputs the MMC clock.
23 to 20	$\frac{3}{4}$	All 0	R	Reserved The write value should always be 0.
19 to 16	CLKDIV[3:0]	H'0	R/W	MMC Clock Frequency Setting 0000: MMCxf /2 <sup>1</sup> 0001: MMCxf /2 <sup>2</sup> : 0111: MMCxf /2 <sup>8</sup> 1000: MMCxf /2 <sup>9</sup> 1001: MMCxf /2 <sup>10</sup> 1001 to 1111: Setting prohibited For details of MMC clock frequency settings in boot operations, see section 60.3.3 (5), MMC clock frequency in boot operations and section 60.2.11, Boot Operation Setting Register (CE_BOOT).
15	$\frac{3}{4}$	0	R/W	Reserved The write value should always be 0.
14	$\frac{3}{4}$	0	R	Reserved The write value should always be 0.
13, 12	SRSPTO[1:0]	00	R/W	Response Timeout Setting 00: 64 MMC clock cycles 01: 128 MMC clock cycles 10: 256 MMC clock cycles 11: Setting prohibited

Bit	Bit Name	Initial Value	R/W	Description
11 to 8	SRBSYTO[3:0]	0000	R/W	Response Busy Timeout Setting 0000: $2^{14}$ ´ MMC clock cycles 0001: $2^{15}$ ´ MMC clock cycles : 1110: $2^{28}$ ´ MMC clock cycles 1111: $2^{29}$ ´ MMC clock cycles
7 to 4	SRWDTO[3:0]	0000	R/W	Write Data/Read Data Timeout Setting 0000: $2^{14}$ ´ MMC clock cycles 0001: $2^{15}$ ´ MMC clock cycles : 1110: $2^{28}$ ´ MMC clock cycles 1111: $2^{29}$ ´ MMC clock cycles
3 to 0	$\frac{3}{4}$	All 0	R/W	Reserved The write value should always be 0.

### 49.2.7 Buffer Access Configuration Register (CE\_BUF\_ACC)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CE\_BUF\_ACC configures the method of accessing data registers and mode of DMA transfer. Do not set this register again during a command sequence. For explanation of the buffers, see section 60.3.3 (3), Buffer structure and buffer access.

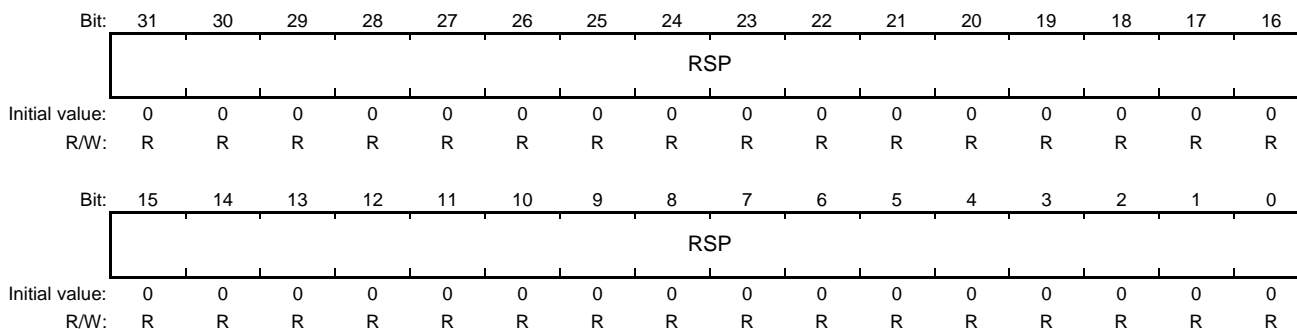
Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	DMAW EN	DMARE N	—	—	—	—	—	—	BUSW	ATYP
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 27	$\frac{3}{4}$	All 0	R	Reserved The write value should always be 0.
26	$\frac{3}{4}$	0	R/W	Reserved The write value should always be 0.
25	DMAWEN	0	R/W	Buffer Write DMA Transfer Request Enable 0: Disables DMA transfer request for buffer writing. 1: Enables DMA transfer request for buffer writing.
24	DMAREN	0	R/W	Buffer Read DMA Transfer Request Enable 0: Disables DMA transfer request for buffer reading. 1: Enables DMA transfer request for buffer reading.
23, 22	$\frac{3}{4}$	All 0	R/W	Reserved The write value should always be 0.
21 to 18	$\frac{3}{4}$	All 0	R	Reserved The write value should always be 0.
17	BUSW	0	R/W	Data register access size selection 0: When access to CE_DATA in 32 bits. 1: When access to CE_DATA in 16 bits.
16	ATYP	0	R/W	Buffer access selection 0: When not swapped byte-wise. 1: When swapped byte-wise. Note: For buffer access, see section 60.3.3 (3), Buffer structure and buffer access.
15 to 0	$\frac{3}{4}$	All 0	R	Reserved The write value should always be 0.

**49.2.8 Response Registers 3 to 0 (CE\_RESP3 to CE\_RESP0)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CE\_RESP3 to CE\_RESP0 are the registers in which the response that has been received is stored. For the formats of response values, see section 60.3.3 (1), Command/response formats.



• CE\_RESP3

Bit	Bit Name	Initial Value	R/W	Description (CE_RESP3)
31 to 0	RSP[127:96]	All 0	R	Bits [127:96] of a 17-byte response are stored.

• CE\_RESP2

Bit	Bit Name	Initial Value	R/W	Description (CE_RESP2)
31 to 0	RSP[95:64]	All 0	R	Bits [95:64] of a 17-byte response are stored.

• CE\_RESP1

Bit	Bit Name	Initial Value	R/W	Description (CE_RESP1)
31 to 0	RSP[63:32]	All 0	R	Bits [63:32] of a 17-byte response are stored.

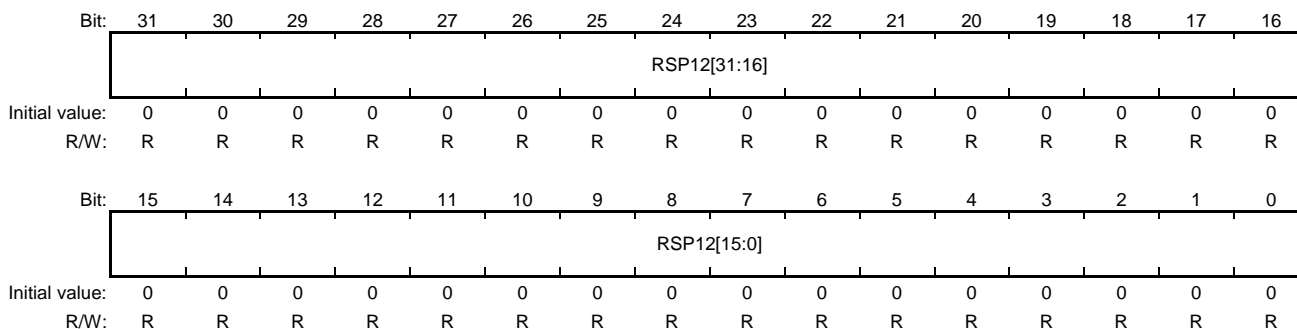
• CE\_RESP0

Bit	Bit Name	Initial Value	R/W	Description (CE_RESP0)
31 to 0	RSP[31:0]	All 0	R	Bits [39:8] of a 6-byte response or bits [31:0] of a 17-byte response are stored. Note: The response to an automatically issued CMD12 is stored in the CE_RESP_CMD12 register.

**49.2.9 Response Register for Automatically-Issued CMD12 (CE\_RESP\_CMD12)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CE\_RESP\_CMD12 is a register in which the response to the automatically-issued CMD12 is stored.

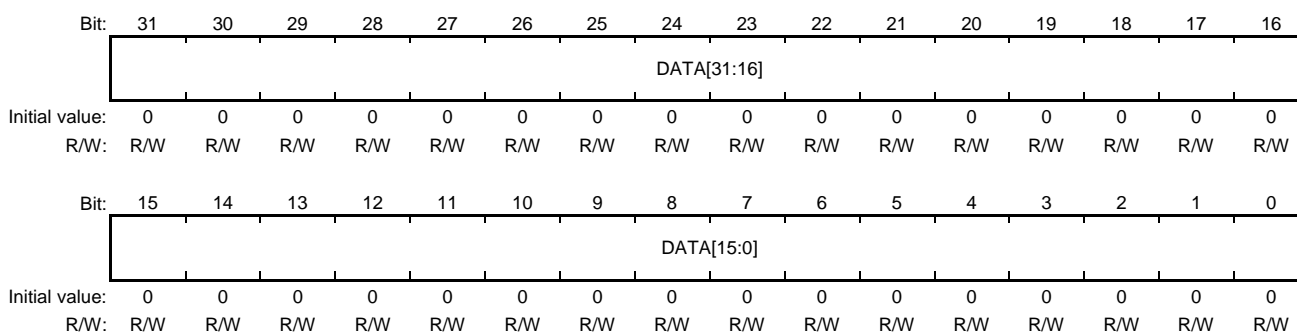


Bit	Bit Name	Initial Value	R/W	Description
31 to 0	RSP12[31:0]	All 0	R	Bits [39:8] of the response to automatically-issued CMD12 are stored.

**49.2.10 Data Register (CE\_DATA)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CE\_DATA is used to access the buffers of this module. In 16-bit access, only DATA[31:16] are accessible. For the write/read data formats, see section 60.3.3 (2), Data block format.



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	DATA[31:0]	All 0	R/W	Buffer write/read data [31:0]

### 49.2.11 Boot Operation Setting Register (CE\_BOOT)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CE\_BOOT controls the MMC clock and sets timeout values in boot mode. Do not set this register again during a command sequence.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	BTCLKDIV[3:0]				SBTACKTO[3:0]				S1STBTDATTO[3:0]				SBTDATTO[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 28	BTCLKDIV[3:0]	0000	R/W	MMC Clock Frequency Setting in Boot Mode 0000: $MMCxf / 2^1$ 0001: $MMCxf / 2^2$ 0010: $MMCxf / 2^3$ 0011: $MMCxf / 2^4$ 0100 to 1111: Settings prohibited Set these bits to a value lower than that in the CLKDIV bits of CE_CLK_CTRL. For MMC clock frequency in boot mode, see section 60.3.3 (5), MMC clock frequency in boot operations.
27 to 24	SBTACKTO[3:0]	0000	R/W	Boot Acknowledge Timeout Setting 0000: $2^{14}$ ´ MMC clock cycles 0001: $2^{15}$ ´ MMC clock cycles : 1110: $2^{28}$ ´ MMC clock cycles 1111: $2^{29}$ ´ MMC clock cycles
23 to 20	S1STBTDATTO [3:0]	0000	R/W	1st Boot Data Timeout Setting 0000: $2^{14}$ ´ MMC clock cycles 0001: $2^{15}$ ´ MMC clock cycles : 1110: $2^{28}$ ´ MMC clock cycles 1111: $2^{29}$ ´ MMC clock cycles
19 to 16	SBTDATTO[3:0]	0000	R/W	Interval Between Boot Data Timeout Setting 0000: $2^{14}$ ´ MMC clock cycles 0001: $2^{15}$ ´ MMC clock cycles : 1110: $2^{28}$ ´ MMC clock cycles 1111: $2^{29}$ ´ MMC clock cycles



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Bit	Bit Name	Initial Value	R/W	Description
15 to 0	¾	All 0	R	Reserved The write value should always be 0.

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### 49.2.12 Interrupt Flag Register (CE\_INT)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CE\_INT indicates various statuses during execution of a command sequence. Each bit is set when its setting condition has been met. To clear flag(s), write 0 only to the bit(s) to be cleared and write 1 to the other bits.

For the handling of this module in the case of an error or timeout, see section 60.3.3 (8), Handling of this module in the case of error/timeout.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	CMD12 DRE	CMD12 RBE	CMD12 CRE	DTRAN E	BUF RE	BUF WEN	BUF REN	—	—	RBSYE	CRSPE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/WC0	R	R	R/WC0	R/WC0	R/WC0	R/WC0	R/WC0	R/WC0	R/WC0	R/WC0	R	R/WC0	R/WC0

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CMD VIO	BUF VIO	—	—	WDAT ERR	RDAT ERR	RIDX ERR	RSP ERR	—	—	—	CRCS TO	WDAT TO	RDAT TO	RBSY TO	RSP TO
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/WC0	R/WC0	R	R	R/WC0	R/WC0	R/WC0	R/WC0	R	R	R/WC0	R/WC0	R/WC0	R/WC0	R/WC0	R/WC0

Bit	Bit Name	Initial Value	R/W	Description
31, 30	¾	All 0	R	Reserved The write value should always be 1.
29	¾	0	R/WC0	Reserved The write value should always be 1.
28, 27	¾	All 0	R	Reserved The write value should always be 1.
26	CMD12DRE	0	R/WC0	Automatic CMD12 Issuance & Buffer Read Complete [Setting condition] Response busy for automatically-issued CMD12 and buffer reading have been completed. [Clearing condition] Writing a 0 to this bit. Note: When CMD12DRE has been set, CMD12RBE, CMD12CRE, and BUFRE have also been set. So, these bits should be cleared as well.
25	CMD12RBE	0	R/WC0	Automatic CMD12 Issuance Response Busy Complete [Setting condition] Reception of the response and response busy for an automatically-issued CMD12 have been completed. [Clearing condition] Writing a 0 to this bit. Note: When CMD12RBE has been set, CMD12CRE has also been set. So, this bit should be cleared as well. When CMD12RBE is set during a multi-block write, DTRANE is also set. So clear the bit as well.

Bit	Bit Name	Initial Value	R/W	Description
24	CMD12CRE	0	R/WC0	<p>Automatic CMD12 Response Complete</p> <p>[Setting condition] The response to an automatically-issued CMD12 has been received.</p> <p>[Clearing condition] Writing a 0 to this bit.</p>
23	DTRANE	0	R/WC0	<p>Data Transmission Complete</p> <p>[Setting conditions] Transmission of all blocks of data has been completed.</p> <ul style="list-style-type: none"> <li>· When configured to receive CRC status: Completion of busy (data busy) after reception of CRC status</li> <li>· When configured not to receive CRC status: Completion of data transmission</li> </ul> <p>[Clearing condition] Writing a 0 to this bit.</p>
22	BUFRE	0	R/WC0	<p>Buffer Read Complete</p> <p>[Setting conditions]</p> <ul style="list-style-type: none"> <li>· Other than in boot operations All blocks of data have been received and the data have been read from the buffer.</li> <li>· In boot operations All blocks of data have been received and the data have been read from the buffer, MMCCMD has been modified from 0 to 1, and 48 MMC clock cycles have elapsed.</li> </ul> <p>[Clearing condition] Writing a 0 to this bit</p>
21	BUFWEN	0	R/WC0	<p>Buffer Write Ready</p> <p>[Setting conditions] The buffer has become empty and ready for writing.</p> <p>[Clearing condition] Writing a 0 to this bit.</p> <p>Note: When writing data to CE_DATA by the CPU, this bit should be cleared first and the data corresponding to the block size set in CE_BLOCK_SET should be written. Note that this bit is not set when DMA transfer request for buffer writing is enabled.</p>
20	BUFREN	0	R/WC0	<p>Buffer Read Ready</p> <p>[Setting conditions] Transfer block size of data have been stored in the buffer and it has become ready for reading.</p> <p>[Clearing condition] Writing a 0 to this bit.</p> <p>Note: When reading data from CE_DATA by the CPU, this bit should be cleared first and the data corresponding to the block size set in CE_BLOCK_SET should be read. Note that this bit is not set when DMA transfer request for buffer reading is enabled.</p>
19	$\frac{3}{4}$	0	R/WC0	<p>Reserved</p> <p>The write value should always be 1.</p>
18	$\frac{3}{4}$	0	R	<p>Reserved</p> <p>The write value should always be 1.</p>

Bit	Bit Name	Initial Value	R/W	Description
17	RBSYE	0	R/WC0	<p>Response Busy Complete</p> <p>[Setting condition]</p> <p>Reception of a response and response busy have been completed.</p> <p>[Clearing condition]</p> <p>Writing a 0 to this bit.</p> <p>Note: When RBSYE has been set, CRSPE has also been set. So, this bit should be cleared as well. Completion of reception of the response and response busy for automatically-issued CMD12 is reflected in CMD12RBE.</p>
16	CRSPE	0	R/WC0	<p>Command/Response Complete</p> <p>[Setting conditions]</p> <ul style="list-style-type: none"> <li>· Other than in boot operations           <ul style="list-style-type: none"> <li>When configured not to receive response:               <ul style="list-style-type: none"> <li>A command has been transmitted.</li> <li>When configured to receive 6- or 17-byte response:                   <ul style="list-style-type: none"> <li>A response has been received.</li> </ul> </li> </ul> </li> <li>· In boot operations               <ul style="list-style-type: none"> <li>When reception of boot acknowledge has been selected:                   <ul style="list-style-type: none"> <li>The boot acknowledge pattern has been received.</li> </ul> </li> </ul> </li> </ul> <p>[Clearing condition]</p> <p>Writing a 0 to this bit.</p> <p>Note: Completion of reception of the response to automatically-issued CMD12 is reflected in CMD12CRE.</p> </li></ul>

Bit	Bit Name	Initial Value	R/W	Description
15	CMDVIO	0	R/WC0	<p>Command Issuance Error</p> <p>[Setting conditions]</p> <p>Illegal setting has been made in CE_CMD_SET or CE_BLOCK_SET.</p> <ul style="list-style-type: none"> <li>· During execution of a command sequence:               <ul style="list-style-type: none"> <li>Writing to CMD[5:0] in CE_CMD_SET.</li> <li>(The command sequence is not stopped automatically.)</li> </ul> </li> <li>· At the start of command sequence:               <ul style="list-style-type: none"> <li>Writing to CMD[5:0] in CE_CMD_SET when the registers have been set for one of the following combinations of selection.</li> <li><math>\frac{3}{4}</math> No response + response busy</li> <li><math>\frac{3}{4}</math> No response + with data + not during boot operations</li> <li><math>\frac{3}{4}</math> No data + automatic CMD12 issuance</li> <li><math>\frac{3}{4}</math> With data + single-block transfer + automatic CMD12 issuance</li> <li><math>\frac{3}{4}</math> With data + response busy + automatic CMD12 issuance</li> <li><math>\frac{3}{4}</math> With data + transfer block size = 0</li> <li><math>\frac{3}{4}</math> With data + transfer block size <math>\neq</math> 513</li> <li><math>\frac{3}{4}</math> With data + multi-block transfer + number of blocks for transfer = 0</li> <li><math>\frac{3}{4}</math> Boot operations + no data</li> <li><math>\frac{3}{4}</math> Boot operations + write</li> <li><math>\frac{3}{4}</math> Boot operations + response busy</li> <li><math>\frac{3}{4}</math> Boot operations + automatic CMD12 issuance</li> <li><math>\frac{3}{4}</math> Boot acknowledge reception + not during boot operations</li> </ul> </li> </ul> <p>[Clearing condition]</p> <p>Writing a 0 to this bit.</p>
14	BUFVIO	0	R/WC0	<p>Buffer Access Error</p> <p>[Setting conditions]</p> <p>Illegal buffer access has been attempted.</p> <ul style="list-style-type: none"> <li>· CE_DATA has been accessed exceeding the block size set in BLKSIZ[15:0] in CE_BLOCK_SET.</li> <li>· While data is being read from the card:               <ul style="list-style-type: none"> <li>CE_DATA has been accessed with BUFREN not set (when DMA is used, with no DMA transfer request asserted for buffer reading).</li> </ul> </li> <li>· While data is being written to the card:               <ul style="list-style-type: none"> <li>CE_DATA has been accessed with BUFWEN not set (when DMA is used, with no DMA transfer request asserted for buffer writing).</li> </ul> </li> </ul> <p>[Clearing condition]</p> <p>Writing a 0 to this bit.</p> <p>Note: When BUFVIO has been set, the command sequence is not stopped automatically. If an error occurs, this bit will be set.</p>
13, 12	$\frac{3}{4}$	All 0	R	<p>Reserved</p> <p>The write value should always be 1.</p>

Bit	Bit Name	Initial Value	R/W	Description
11	WDATERR	0	R/WC0	<p>Write Data Error</p> <p>[Setting conditions]</p> <p>Error is found in the data that has been written.</p> <ul style="list-style-type: none"> <li>Error is in the status of the CRC status.</li> <li>Error is in the end bits of the CRC status.</li> </ul> <p>[Clearing condition]</p> <p>Writing a 0 to this bit.</p> <p>Note: When WDATERR has been set, the command sequence is stopped automatically.</p>
10	RDATERR	0	R/WC0	<p>Read Data Error</p> <p>[Setting conditions]</p> <p>Error is found in the read data.</p> <ul style="list-style-type: none"> <li>Error is in CRC16 of the read data.</li> <li>Error is in the end bits of the read data.</li> </ul> <p>[Clearing condition]</p> <p>Writing a 0 to this bit.</p> <p>Note: When RDATERR has been set, the command sequence is stopped automatically.</p>
9	RIDXERR	0	R/WC0	<p>Response Index Error</p> <p>[Setting conditions]</p> <p>Error has been found in the index value of the response.</p> <ul style="list-style-type: none"> <li>When an error has been found in bits [45:40] of a 6-byte response (including automatically-issued CMD12) or bits [133:128] of a 17-byte response. (The items to be checked are set by RIDXC in CE_CMD_SET.)</li> </ul> <p>[Clearing condition]</p> <p>Writing a 0 to this bit.</p> <p>Note: When RIDXERR has been set, the command sequence is stopped automatically.</p>
8	RSPERR	0	R/WC0	<p>Response Error</p> <p>[Setting conditions]</p> <p>Error has been found in the response values of the response.</p> <ul style="list-style-type: none"> <li>Transmission bit in the response is 1.</li> <li>Error is in the end bits of the response.</li> <li>When an error has been found in bits [7:1] of a 6-byte response (including automatically-issued CMD12) or a 17-byte response. (The items to be checked are set by RCRC7C in CE_CMD_SET.)</li> <li>Error in the boot acknowledge pattern</li> <li>Error in the end bits of the boot acknowledge</li> </ul> <p>[Clearing condition]</p> <p>Writing a 0 to this bit.</p> <p>Note: When RSPERR has been set, the command sequence is stopped automatically.</p>
7, 6	$\frac{3}{4}$	All 0	R	<p>Reserved</p> <p>The write value should always be 1.</p>
5	$\frac{3}{4}$	0	R/WC0	<p>Reserved</p> <p>The write value should always be 1.</p>

Bit	Bit Name	Initial Value	R/W	Description
4	CRCSTO	0	R/WC0	<p>CRC Status Timeout</p> <p>[Setting condition] CRC status could not be received.</p> <p>[Clearing condition] Writing a 0 to this bit.</p> <p>Note: The command sequence is not stopped even if CRCSTO is set.</p>
3	WDATTO	0	R/WC0	<p>Write Data Timeout</p> <p>[Setting condition] The busy status remains unchanged after the period set by SRWDTO in CE_CLK_CTRL after the CRC status was received.</p> <p>[Clearing condition] Writing a 0 to this bit.</p> <p>Note: The command sequence is not stopped even if WDATTO is set.</p>
2	RDATTO	0	R/WC0	<p>Read Data Timeout</p> <p>[Setting conditions]</p> <ul style="list-style-type: none"> <li>· Other than in boot operations <ul style="list-style-type: none"> <li>¾ Read data could not be received within the period set by SRWDTO in CE_CLK_CTRL after the read command was transmitted.</li> <li>¾ Read data could not be received within the period set by SRWDTO in CE_CLK_CTRL after the read data was received.</li> </ul> </li> <li>· In boot operations <ul style="list-style-type: none"> <li>¾ The first read data could not be received within the period set by S1STBTDATTO in CE_BOOT.</li> <li>¾ Read data could not be received within the period set by SBTDATTO in CE_BOOT after the read data was received.</li> </ul> </li> </ul> <p>[Clearing condition] Writing a 0 to this bit.</p> <p>Note: The command sequence is not stopped even if RDATTO is set.</p>
1	RBSYTO	0	R/WC0	<p>Response Busy Timeout</p> <p>[Setting condition] The busy status remains unchanged after the period set by SRBSYTO in CE_CLK_CTRL after the command (including automatically-issued CMD12) was transmitted.</p> <p>[Clearing condition] Writing a 0 to this bit.</p> <p>Note: The command sequence is not stopped even if RBSYTO is set.</p>

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Bit	Bit Name	Initial Value	R/W	Description
0	RSPTO	0	R/WC0	<p>Response Timeout</p> <p>[Setting conditions]</p> <ul style="list-style-type: none"><li>Other than in boot operations Response could not be received within the period set by SRSPTO in CE_CLK_CTRL after the command (including automatically-issued CMD12) was transmitted.</li><li>In boot operations When reception of boot acknowledge has been selected: The boot acknowledge could not be received within the period set by SBTACKTO in CE_BOOT.</li></ul> <p>[Clearing condition]</p> <p>Writing a 0 to this bit.</p> <p>Note: The command sequence is not stopped even if RSPTO is set.</p>

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### 49.2.13 Interrupt Enable Register (CE\_INT\_EN)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CE\_INT\_EN controls output of the CE\_INT-related interrupt signals. For details on interrupt requests, see section 60.3.1, Interrupt Requests.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	MCMD 12DRE	MCMD 12RBE	MCMD 12CRE	MDTRA NE	MBUF RE	MBUF WEN	MBUF REN	—	—	MRB SYE	MCR SPE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MCMD VIO	MBUF VIO	—	—	MWDA TERR	MRDAT ERR	MRIDX ERR	MRSP ERR	—	—	—	MCRC STO	MWDA TTO	MRDAT TO	MRBSY TO	MRSP TO
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31, 30	$\frac{3}{4}$	All 0	R	Reserved The write value should always be 0.
29	$\frac{3}{4}$	0	R/W	Reserved The write value should always be 0.
28, 27	$\frac{3}{4}$	All 0	R	Reserved The write value should always be 0.
26	MCMD12DRE	0	R/W	CMD12DRE Interrupt Enable 0: Disables interrupt output by the CMD12DRE flag. 1: Enables interrupt output by the CMD12DRE flag.
25	MCMD12RBE	0	R/W	CMD12RBE Interrupt Enable 0: Disables interrupt output by the CMD12RBE flag. 1: Enables interrupt output by the CMD12RBE flag.
24	MCMD12CRE	0	R/W	CMD12CRE Interrupt Enable 0: Disables interrupt output by the CMD12CRE flag. 1: Enables interrupt output by the CMD12CRE flag.
23	MDTRANE	0	R/W	DTRANE Interrupt Enable 0: Disables interrupt output by the DTRANE flag. 1: Enables interrupt output by the DTRANE flag.
22	MBUFRE	0	R/W	BUFRE Interrupt Enable 0: Disables interrupt output by the BUFRE flag. 1: Enables interrupt output by the BUFRE flag.
21	MBUFWEN	0	R/W	BUFWEN Interrupt Enable 0: Disables interrupt output by the BUFWEN flag. 1: Enables interrupt output by the BUFWEN flag.
20	MBUFREN	0	R/W	BUFREN Interrupt Enable 0: Disables interrupt output by the BUFREN flag. 1: Enables interrupt output by the BUFREN flag.

Bit	Bit Name	Initial Value	R/W	Description
19	$\frac{3}{4}$	0	R/W	Reserved The write value should always be 0.
18	$\frac{3}{4}$	0	R	Reserved The write value should always be 0.
17	MRBSYE	0	R/W	RBSYE Interrupt Enable 0: Disables interrupt output by the RBSYE flag. 1: Enables interrupt output by the RBSYE flag.
16	MCRSPE	0	R/W	CRSPE Interrupt Enable 0: Disables interrupt output by the CRSPE flag. 1: Enables interrupt output by the CRSPE flag.
15	MCMDVIO	0	R/W	CMDVIO Interrupt Enable 0: Disables interrupt output by the CMDVIO flag. 1: Enables interrupt output by the CMDVIO flag.
14	MBUFVIO	0	R/W	BUFVIO Interrupt Enable 0: Disables interrupt output by the BUFVIO flag. 1: Enables interrupt output by the BUFVIO flag.
13, 12	$\frac{3}{4}$	All 0	R	Reserved The write value should always be 0.
11	MWDATERR	0	R/W	WDATERR Interrupt Enable 0: Disables interrupt output by the WDATERR flag. 1: Enables interrupt output by the WDATERR flag.
10	MRDATERR	0	R/W	RDATERR Interrupt Enable 0: Disables interrupt output by the RDATERR flag. 1: Enables interrupt output by the RDATERR flag.
9	MRIDXERR	0	R/W	RIDXERR Interrupt Enable 0: Disables interrupt output by the RIDXERR flag. 1: Enables interrupt output by the RIDXERR flag.
8	MRSPEERR	0	R/W	RSPERR Interrupt Enable 0: Disables interrupt output by the RSPERR flag. 1: Enables interrupt output by the RSPERR flag.
7, 6	$\frac{3}{4}$	All 0	R	Reserved The write value should always be 0.
5	$\frac{3}{4}$	0	R/W	Reserved The write value should always be 0.
4	MRCRCSTO	0	R/W	CRCSTO Interrupt Enable 0: Disables interrupt output by the CRCSTO flag. 1: Enables interrupt output by the CRCSTO flag.
3	MWDATTO	0	R/W	WDATTO Interrupt Enable 0: Disables interrupt output by the WDATTO flag. 1: Enables interrupt output by the WDATTO flag.
2	MRDATTO	0	R/W	RDATTO Interrupt Enable 0: Disables interrupt output by the RDATTO flag. 1: Enables interrupt output by the RDATTO flag.

Bit	Bit Name	Initial Value	R/W	Description
1	MRBSYTO	0	R/W	RBSYTO Interrupt Enable 0: Disables interrupt output by the RBSYTO flag. 1: Enables interrupt output by the RBSYTO flag.
0	MRSPTO	0	R/W	RSPTO Interrupt Enable 0: Disables interrupt output by the RSPTO flag. 1: Enables interrupt output by the RSPTO flag.

#### 49.2.14 Status Register 1 (CE\_HOST\_STS1)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CE\_HOST\_STS1 indicates the number of blocks that have been transferred, the states of the MMCCMD line and MMCDAT lines, the index of the response that has been received, and whether a command sequence is in progress.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CMD SEQ	CMD SIG	RSPIDX[5:0]					DATSIG[7:0]								
Initial value:	0	—	0	0	0	0	0	0	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RCVBLK[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31	CMDSEQ	0	R	Command Sequence in Progress 0: Command sequence is in the initial state. 1: Command sequence is being executed.
30	CMSIG	—	R	MMCCMD State Indicates the state on the MMCCMD line.
29 to 24	RSPIDX[5:0]	H'00	R	Response Index Indicate bits [45:40] of a 6-byte response or bits [133:128] of a 17-byte response.
23 to 16	DATSIG[7:0]	—	R	MMCDAT[7:0] State Indicate the state on the MMCDAT[7:0] lines. Note: When a communication error or a timeout error occurs, MMCDAT[0] may remain 0.
15 to 0	RCVBLK[15:0]	H'0000	R	Number of Transferred Blocks Indicate the number of blocks that have been transferred. <ul style="list-style-type: none"> <li>When the DWEN bit in CE_CMD_SET is 0: Number of blocks read from the card</li> <li>When the DWEN bit in CE_CMD_SET is 1: Number of blocks written to the card</li> </ul>

### 49.2.15 Status Register 2 (CE\_HOST\_STS2)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CE\_HOST\_STS2 indicates timeout and error statuses.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CRC STE	CRC 16E	AC12C RCE	RSPCR C7E	CRCST EBE	RDATE BE	AC12R EBE	RSPEB E	AC12ID XE	RSP IDXE	BTACK PATE	BTACK EBE	—	CRCST[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	STRD ATTO	DATBS YTO	CRCST TO	AC12B SYTO	RSPBS YTO	AC12 RSPTO	STRSP TO	BTACK TO	1STBT DATTO	BTDAT TO	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31	CRCSTE	0	R	CRC Status Error This bit is set to 1 when an error is found in the CRC status value.
30	CRC16E	0	R	Read Data CRC16 Error This bit is set to 1 when an error is found in CRC16 in the read data.
29	AC12CRCE	0	R	Automatic CMD12 Response CRC7 Error This bit is set to 1 when an error is found in bits [7:1] of the response to the automatically-issued CMD12. Note: The items to be checked are set by RCRC7C in CE_CMD_SET.
28	RSPCRC7E	0	R	Command Response CRC7 Error (other than automatically-issued CMD12) This bit is set to 1 when an error is found in bits [7:1] of a 6-byte response or a 17-byte response. Note: The items to be checked are set by RCRC7C in CE_CMD_SET.
27	CRCSTEBE	0	R	CRC Status End Bit Error This bit is set to 1 when an error is found in the end bits in CRC status.
26	RDATEBE	0	R	Read Data End Bit Error This bit is set to 1 when an error is found in the end bits in the read data.
25	AC12REBE	0	R	Automatic CMD12 Response End Bit Error This bit is set to 1 when an error is found in the end bits of the response to the automatically-issued CMD12.
24	RSPEBE	0	R	Command Response End Bit Error (other than automatically-issued CMD12) This bit is set to 1 when an error is found in the end bits of the response.
23	AC12IDXE	0	R	Automatic CMD12 Response Index Error This bit is set to 1 when an error is found in bits [45:40] of the response to the automatically-issued CMD12. Note: The items to be checked are set by RIDXC in CE_CMD_SET.

Bit	Bit Name	Initial Value	R/W	Description
22	RSPIDX	0	R	Command Response Index Error (other than automatically-issued CMD12) This bit is set to 1 when an error is found in bits [45:40] of a 6-byte response or bits [133:128] of a 17-byte response. Note: The items to be checked are set by RIDXC in CE_CMD_SET.
21	BTACKPATE	0	R	Boot Acknowledge Pattern Error This bit is set to 1 when an error is found in the boot acknowledge pattern.
20	BTACKEBE	0	R	Boot Acknowledge End Bit Error This bit is set to 1 when an error is found in the end bits of the boot acknowledge.
19	¾	0	R	Reserved The write value should always be 0.
18 to 16	CRCST[2:0]	00	R	CRC Status/Boot Acknowledge Pattern Indication This bit indicates the value for CRC status that was received or the pattern value from the boot-acknowledge.
15	¾	0	R	Reserved The write value should always be 0.
14	STRDATTO	0	R	Read Data Timeout (valid other than in boot operations) <ul style="list-style-type: none"> <li>This bit is set to 1 if read data is not received within the period set by the SRWDTO bits in CE_CLK_CTRL after a read command was transmitted.</li> <li>This bit is set to 1 if read data is not received within the period set by the SRWDTO bits in CE_CLK_CTRL after a read data was received.</li> </ul>
13	DATBSYTO	0	R	Data Busy Timeout This bit is set to 1 if busy status remains unchanged after the period set by the SRWDTO bits in CE_CLK_CTRL after the CRC status was received.
12	CRCSTTO	0	R	CRC Status Timeout This bit is set to 1 if CRC status could not be received.
11	AC12BSYTO	0	R	Automatic CMD12 Response Busy Timeout This bit is set to 1 if busy state remains unchanged after the period set by the SRBSYTO bits in CE_CLK_CTRL after the automatically-issued CMD12 was transmitted.
10	RSPBSYTO	0	R	Response Busy Timeout This bit is set to 1 if busy state remains unchanged after the period set by the SRBSYTO bits in CE_CLK_CTRL after a command (other than automatically-issued CMD12) was transmitted.
9	AC12RSPTO	0	R	Automatic CMD12 Response Timeout This bit is set to 1 if the response is not received within the period set by the SRSPTO bits in CE_CLK_CTRL after the automatically-issued CMD12 was transmitted.
8	STRSPTO	0	R	Response Timeout This bit is set to 1 if the response is not received within the period set by the SRSPTO bits in CE_CLK_CTRL after a command (other than automatically-issued CMD12) was transmitted.

Bit	Bit Name	Initial Value	R/W	Description
7	BTACKTO	0	R	<p>Boot Acknowledge Timeout</p> <p>In boot operations, this bit is set to 1 if boot acknowledge is not received within the period set by the SBTACKTO bits in CE_BOOT.</p>
6	1STBTDATTO	0	R	<p>1st Boot Data Timeout</p> <p>In boot operations, this bit is set to 1 if the 1st read data is not received within the period set by the S1STBTDATTO bits in CE_BOOT.</p>
5	BTDATTO	0	R	<p>Interval between Boot Data Timeout</p> <p>In boot operations, this bit is set to 1 if read data is not received within the period set by the SBTDATTO bits in CE_BOOT after a read data was received.</p>
4 to 0	¾	All 0	R	<p>Reserved</p> <p>The write value should always be 0.</p>

### 49.2.16 Clock Control Register 2 (CE\_CLK\_CTRL2)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CE\_CLK\_CTRL2 is a register used for initialization of the MMC. Set the MMC\_CLKU bits (bits 27 to 24) and the MMC\_CLKL bits (bits 19 to 16) to H'F before using the MMC.

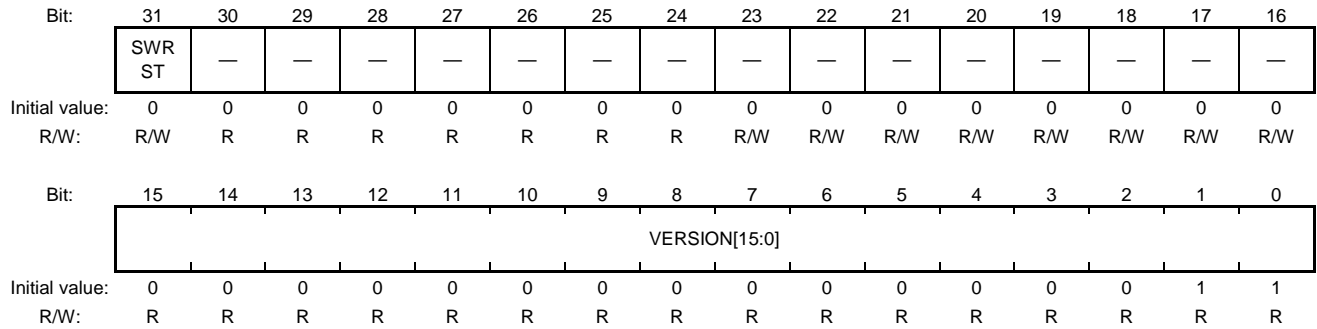
Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	MMC_CLKU				—	—	—	—	MMC_CLKL			
Initial value:	0	0	0	0	0	0	0	0	—	—	—	—	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R	R	R	R	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	—	0	0	0	—	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/WC0	R/WC0	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 28	—	All 0	R	Reserved The write value should always be 0.
27 to 24	MMC_CLKU	H'0	R/W	Set these bits to H'F before using the MMC.
23 to 20	—	—	R	Reserved The write value should always be 0.
19 to 16	MMC_CLKL	H'0	R/W	Set these bits to H'F before using the MMC.
15	—	0	R	Reserved The write value should always be 0.
14	—	—	R	Reserved The write value should always be 0.
13, 12	—	All 0	R/WC0	Reserved The write value should always be 1.
11	—	0	R	Reserved The write value should always be 0.
10	—	—	R	Reserved The write value should always be 0.
9 to 0	—	All 0	R	Reserved The write value should always be 0.

**49.2.17 Version Register (CE\_VERSION)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CE\_VERSION indicates the version number and controls software reset of this module.



Bit	Bit Name	Initial Value	R/W	Description
31	SWRST	0	R/W	Software Reset 0: Software reset cleared (normal operation). 1: Executes software reset. When this bit is set to 1, the values of all registers are initialized. (SWRST is not initialized.)
30 to 24	¾	All 0	R	Reserved The write value should always be 0.
23 to 16	¾	All 0	R/W	Reserved The write value should always be 0.
15 to 0	VERSION [15:0]	H'0003	R	Version Information Indicates the version number of this module.



**49.2.18 Data Output Phase Select Register (CE\_ODATSEL)**

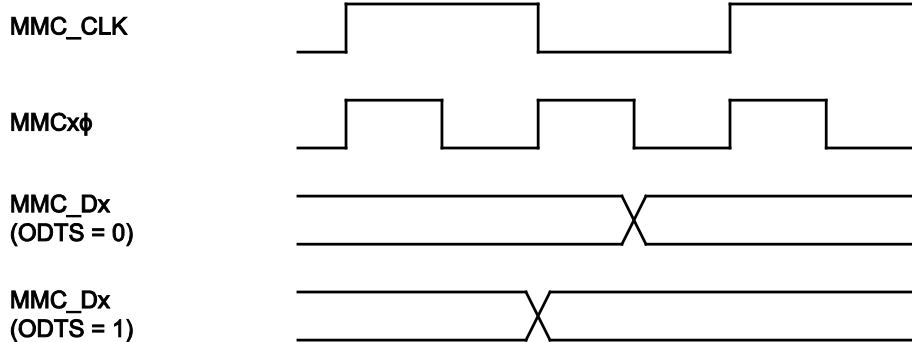
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CE\_ODATSEL is a register which adjusts data output timing.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	ODTS	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 9	—	All 0	R	Reserved The write value should be 0.
8	ODTS	0	R/W	Output Data Timing Select 0: Data being output are changed 1/4 of an MMC_CLK cycle before rising edges of MMC_CLK. 1: Data being output are changed on falling edges of MMC_CLK.
7 to 0	—	All 0	R	Reserved The write value should be 0.

(Waveform)



## 49.3 Operations

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

### 49.3.1 Interrupt Requests

Table 60.3 shows the specification of the interrupt requests. This module generates two types of interrupt requests: normal operation and error/timeout. When a bit in the flag register is set to 1 and also the corresponding bit in the interrupt enable register is set to 1 (enabled), an interrupt request is asserted.

**Table 49.3 Specification of Interrupt Requests**

Flag Register	Bit	Enable Register	Bit	Interrupt Request
CE_INT	CMD12DRE	CE_INT_EN	MCMD12DRE	Normal operation interrupt
	CMD12RBE		MCMD12RBE	
	CMD12CRE		MCMD12CRE	
	DTRANE		MDTRANE	
	BUFRE		MBUFRE	
	BUFWEN		MBUFWEN	
	BUFREN		MBUFREN	
	RBSYE		MRBSYE	
	CRSPE		MCRSPE	
	CMDVIO		MCMDVIO	
	BUFVIO		MBUFVIO	
	WDATERR		MWDATERR	
	RDATERR		MRDATERR	
	RIDXERR		MRIDXERR	
	RSPERR		MRSPERR	
	CRCSTO		MCRSTO	
	WDATTO		MWDATTO	
	RDATTO		MRDATTO	
	RBSYTO		MRBSYTO	
	RSPTO		MRSPTO	

### 49.3.2 DMA Specifications

This module has two types of DMA transfer requests: for buffer reading and for buffer writing.

The method of DMA transfer is configured by CE\_BUF\_ACC.

#### (1) DMA for buffer writing

The DMA transfer request is asserted for buffer writing when the buffer has become empty while the DMAWEN bit in CE\_BUF\_ACC is set to 1.

The DMA transfer request stays asserted for the amount of data specified by BLKSIZ (the block size set in CE\_BLOCK\_SET) ´ BLKCNT (the number of blocks for transfer set in CE\_BLOCK\_SET), and negated after the last block has been transferred. Note that the BUFWEN bit in CE\_INT will not be asserted during DMA transfer.

If an error has occurred during DMA transfer or DMA transfer is forcibly terminated, the command sequence is stopped automatically, which causes the DMA transfer request to be negated.

#### (2) DMA for buffer reading

The DMA transfer request is asserted for buffer reading when the buffer stores data of the block size specified in CE\_BLOCK\_SET while the DMAREN bit in CE\_BUF\_ACC is set to 1.

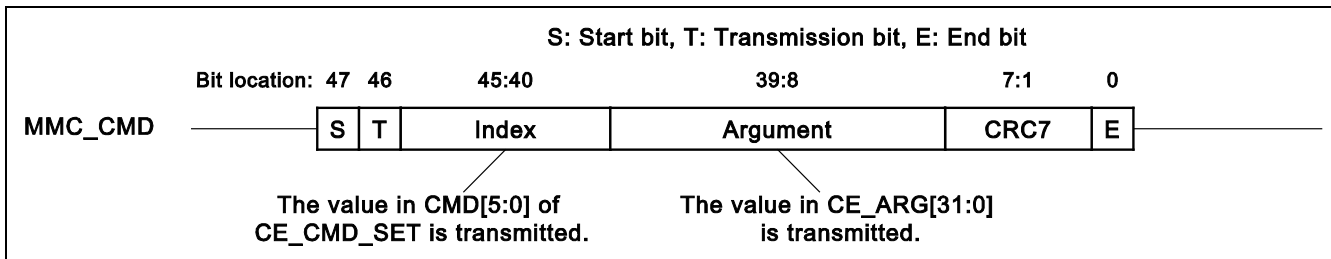
The DMA transfer request stays asserted for the amount of data specified by BLKSIZ (the block size set in CE\_BLOCK\_SET) ´ BLKCNT (the number of blocks for transfer set in CE\_BLOCK\_SET), and negated after the last block has been transferred. Note that the BUFREN bit in CE\_INT will not be asserted during DMA transfer.

If an error has occurred during DMA transfer or DMA transfer is forcibly terminated, the command sequence is stopped automatically, which causes the DMA transfer request to be negated.

**49.3.3 Operations**

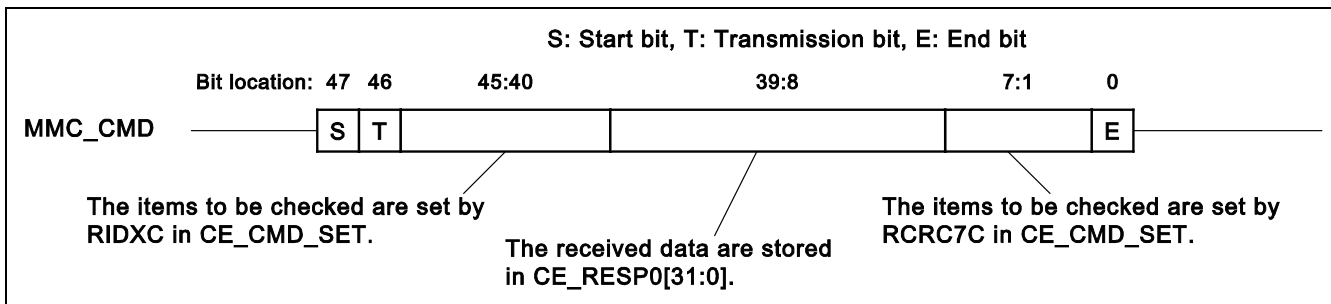
**(1) Command/response formats**

Figure 60.3 shows the format of the command to be transferred. The command index that is set in the CMD[5:0] bits in CE\_CMD\_SET and the argument set in the ARG[31:0] bits in CE\_ARG are reflected in the command.

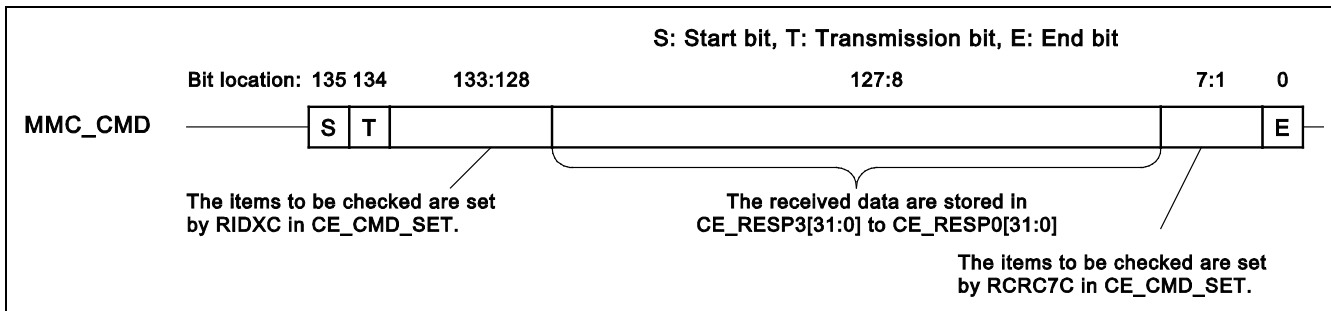


**Figure 49.3 Command Format**

Figures 60.4 and figure 60.5 show the formats when a 6-byte response and 17-byte response (R2) are received, respectively. The received response is stored in CE\_RESP0 or CE\_RESP3 to CE\_RESP0. The items to be checked are set by the RIDXC bits and the RCRC7C bits in CE\_CMD\_SET.



**Figure 49.4 Format of 6-Byte Response**



**Figure 49.5 Format of 17-Byte Response (R2)**

(2) Data block format

Figure 60.6 shows the format of data blocks. For D0 to D3 in the figure, see section 60.3.3 (3), Buffer structure and buffer access. When data are written to the card, the data stored in the buffer are transmitted. When data are read from the card, the received data are stored in the buffer.

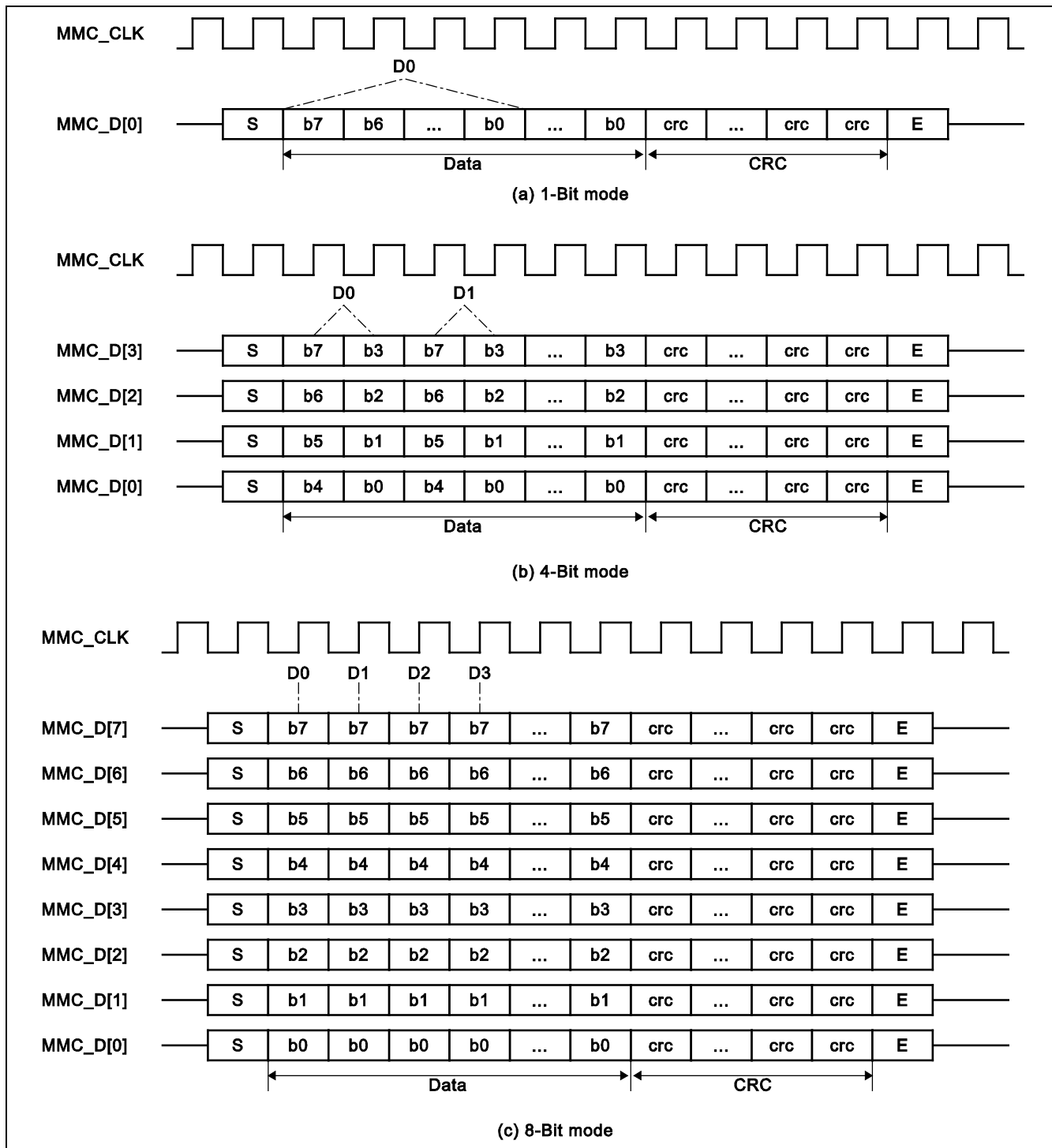


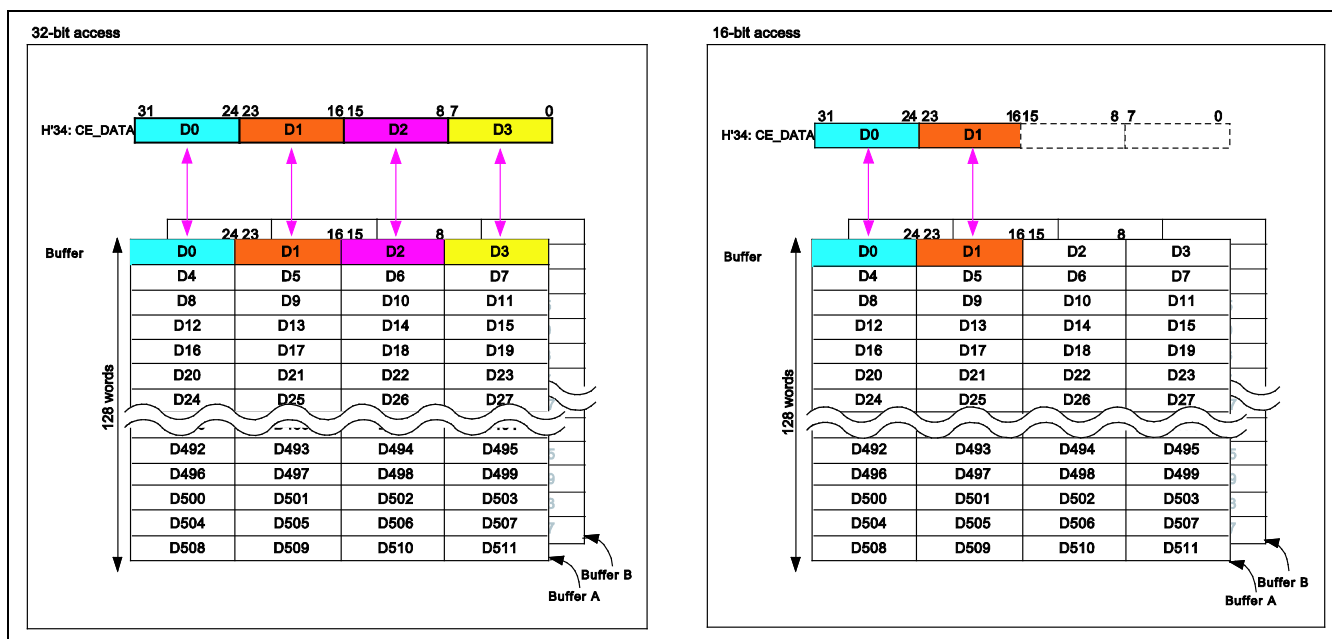
Figure 49.6 Data Block Format

**(3) Buffer structure and buffer access**

As shown in figure 60.7, this module has two 512-byte RAM units for double buffering. If a block of data (512 bytes) stored in one buffer is transmitted during multi-block writing, the next block of data can be transmitted as soon as the other buffer is full. If a block of received data (512 bytes) is stored in one buffer during multi-block reading, the next block of received data can be stored in the other buffer once it is empty.

If neither buffer is empty during multi-block reading, the MMC clock is stopped, which in turn temporarily stops reception. Once either of the buffers becomes empty, supply of the MMC clock signal is re-started and data reception is resumed.

The buffers are accessed by CE\_DATA. If the transfer block size is set to  $4 \cdot n + 1$  or  $4 \cdot n + 3$ , access should be made for  $4 \cdot (n + 2)$  bytes or  $4 \cdot (n + 1)$  bytes in 16-bit access, and for  $4 \cdot (n + 1)$  bytes in 32-bit access. ( $n = 0, 1, 2, \dots, 127$ )



**Figure 49.7 Double Buffer Structure**

This module has the buffer access select function that allows byte-wise swapping of data when the buffer is accessed by writing to or reading from CE\_DATA. This function is enabled by the setting of CE\_BUFF\_ACC. Figure 60.8 shows the specification of 32-bit and 16-bit accesses.

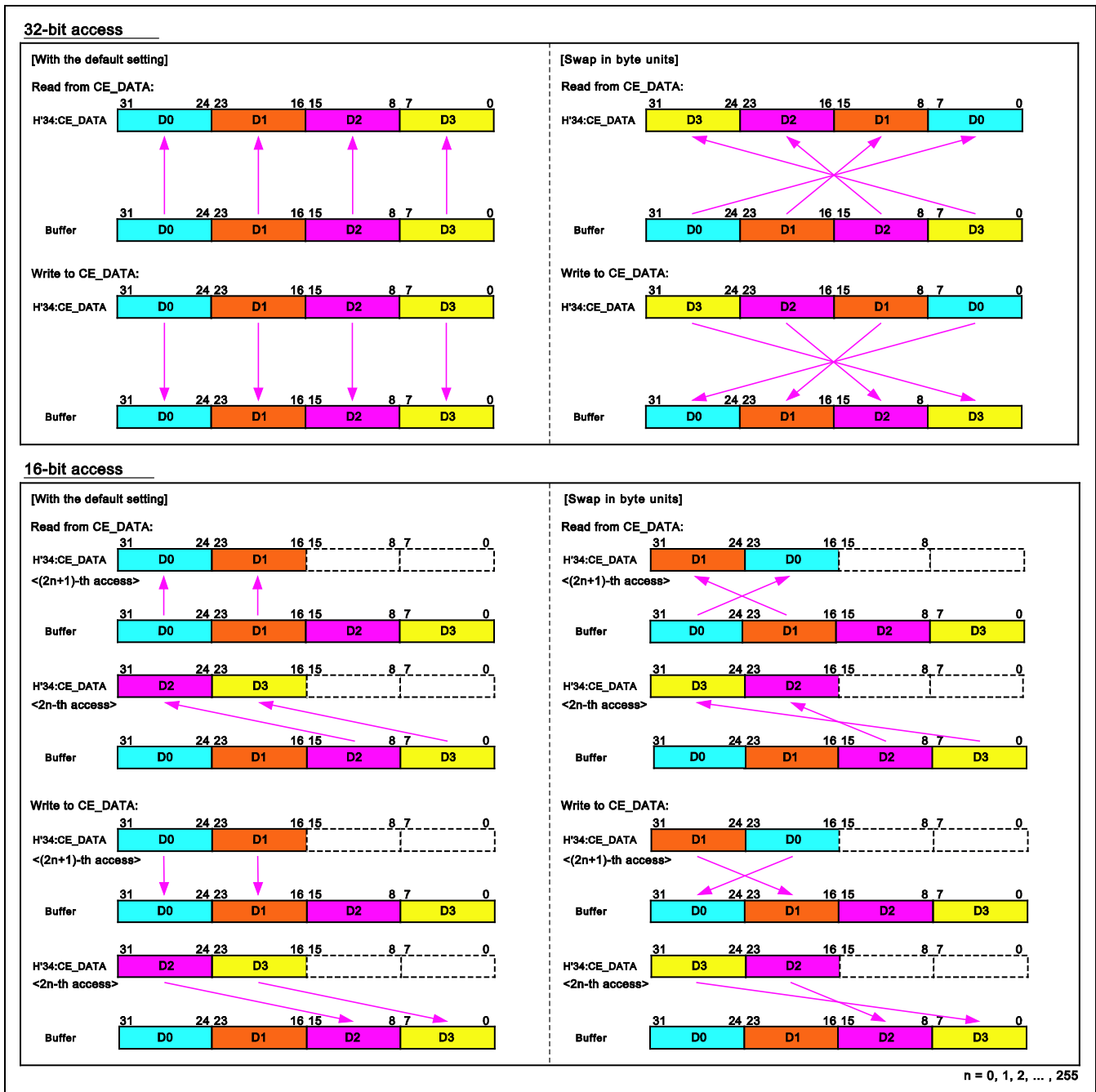
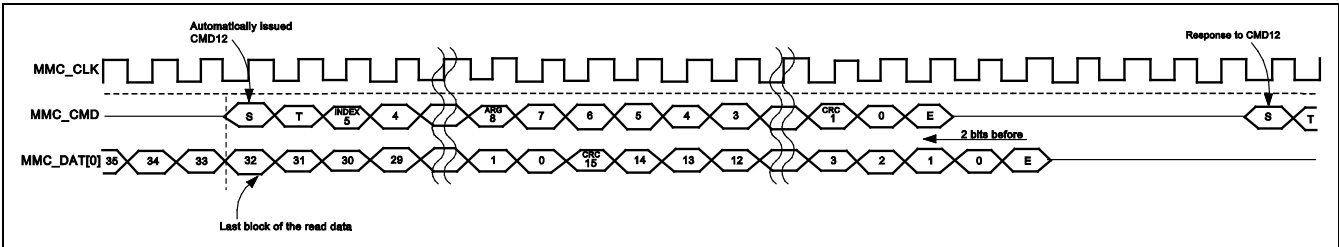


Figure 49.8 Specification of Byte-Swapping in 32-/16-Bit Accesses

**(4) Automatic CMD12 issuance**

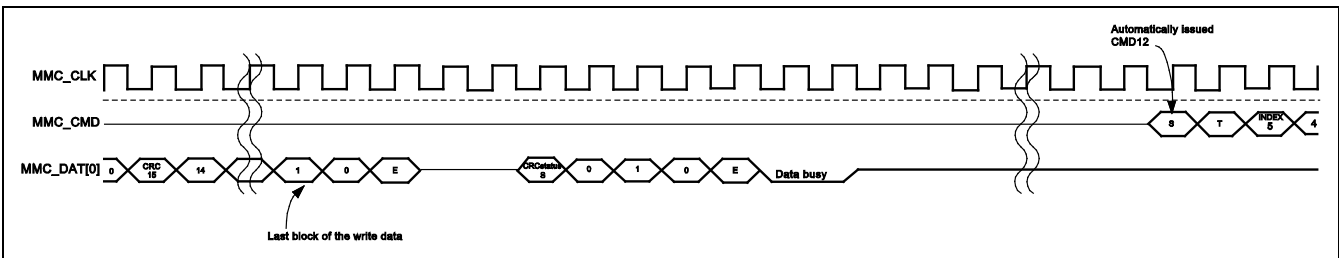
This module has the function that automatically issues CMD12 when multi-block transfer is performed with the CMD12EN bit in CE\_CMD\_SET set to 1.

Figure 60.9 shows the timing of automatic CMD12 issuance in multi-block read. CMD12 is issued such that the end bit of the command is sent two bits before the end bit of the data during reception of the last block.



**Figure 49.9 Timing of Automatically-Issued CMD12 in Multi-Block Read (1-Bit Mode)**

Figure 60.10 shows the timing of automatic CMD12 issuance in multi-block write. CMD12 is issued after the data busy after transmission of the last block has ended.

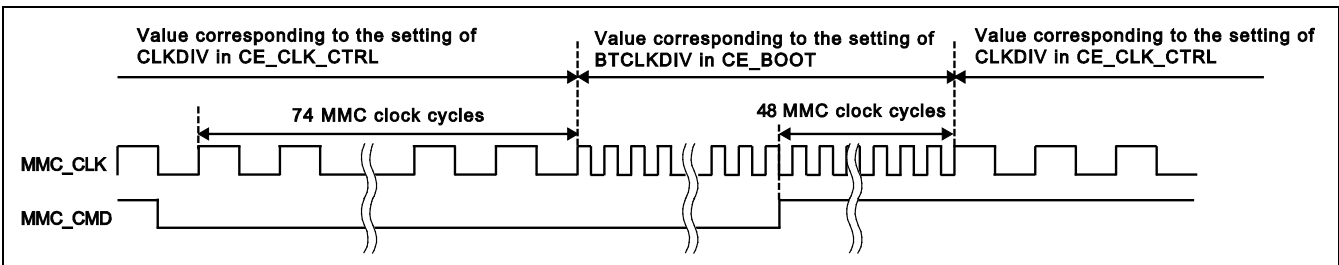


**Figure 49.10 Timing of Automatically-Issued CMD12 in Multi-Block Write (1-Bit Mode)**

The argument for the automatically-issued CMD12 is set in CE\_ARG\_CMD12. Bits [39:8] of the response to the CMD12 is stored in CE\_RESP\_CMD12. "Busy" is involved in response reception.

**(5) MMC clock frequency in boot operations**

Figure 60.11 shows the timing for changing the MMC clock frequency in boot operations. In boot operations, the MMC clock frequency can be switched to the value corresponding to the setting of the BTCLKDIV bits of CE\_BOOT 74 MMC clock cycles after MMCCMD is modified from 1 to 0. Alternatively, it can be switched to the value corresponding to the setting of the CLKDIV bits of CE\_CLK\_CTRL 48 MMC clock cycles after MMC\_CMD is modified from 0 to 1.



**Figure 49.11 MMC Clock Frequency in Boot Operations**



## (6) High priority interrupt (HPI)

The HPI should be processed according to the following procedure. Refer to section 60.2, Register Description, and section 60.3.4, Examples of Setting.

### (a) To execute the HPI during a write to the device

- Terminate the command sequence forcibly.
- Wait until the CMDSEQ bit in CE\_HOST\_STS1 becomes 1.
- Issue CMD12 (R1) to cause a device state transition from rcv to prg. If the device is already in the prg state here, the device does not output a response.
- Issue CMD13 (R1).
- Issue the HPI command.\*

### (b) To execute the HPI in the response busy state not during a write to the device

- Terminate the command sequence forcibly.
- Wait until the CMDSEQ bit in CE\_HOST\_STS1 turns 0.
- Issue CMD13 (R1).
- Issue the HPI command.\*

HPIs in the sequence of CMD6, CMD24, CMD25 (pre-defined), and CMD38 are supported.

Note: \* CMD12 (R1b) or CMD13 (R1b) differs depending on the e-MMC connected.

## (7) Background operation

The background operation should be processed according to the following procedure. Refer to section 60.2, Register Description, and section 60.3.4, Examples of Setting.

To execute background operation, issue CMD6 (R1) to write to the BKOPS\_START byte in the EXT\_CSD register of the device.

To confirm that background operation has been completed, issue CMD6 (R1) and then CMD13 (R1) to check the device state, or poll the MMCDAT[0]. If the device state is trans after issuing CMD13 (R1) or MMCDAT[0] is high, background operation has been completed.

To suspend background operation, use the HPI (see section 60.3.3 (6), High priority interrupt (HPI)).

## (8) Handling of this module in the case of error/timeout

This module may not be stopped when an error has occurred. If an error has occurred and the CMDSEQ bit in CE\_HOST\_STS1 is still indicating that the command sequence is in progress, terminate the sequence forcibly and execute software reset. Note that the data for transmission or received data that had been stored in the buffers at the time of error occurrence are not guaranteed.

This module is not stopped when a timeout has occurred. Before issuing the next command after the timeout has occurred, terminate the sequence forcibly and execute software reset.

### 49.3.4 Examples of Setting

This section shows the procedures for executing typical command sequences.

#### (1) Legends

Figure 60.12 shows the legends for the symbols used in the figures in the following subsections.

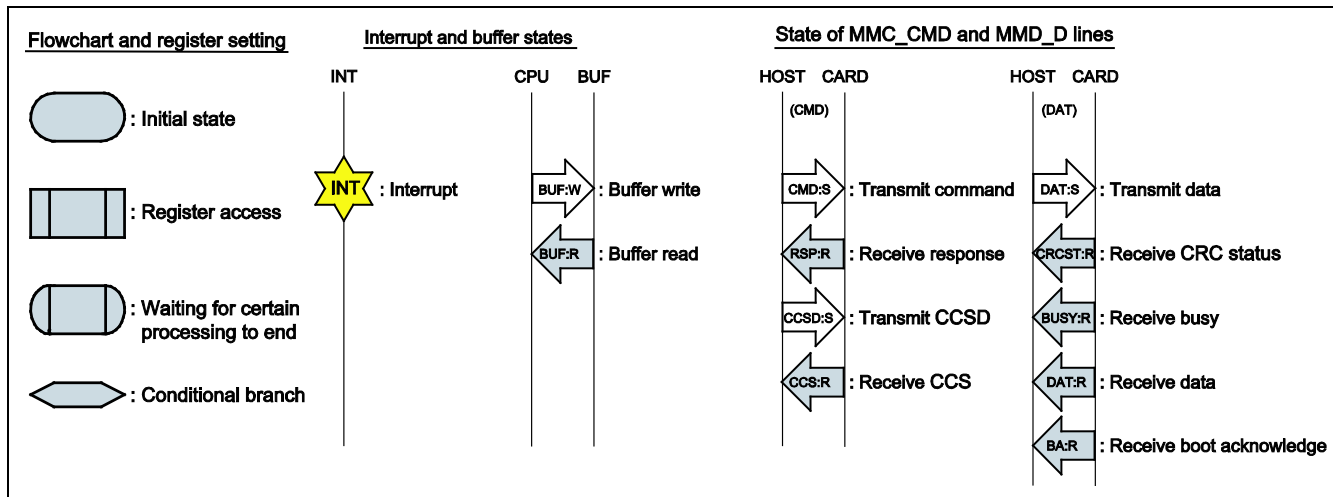


Figure 49.12 Legends for Symbols Used in Figures

#### (2) Command transmission

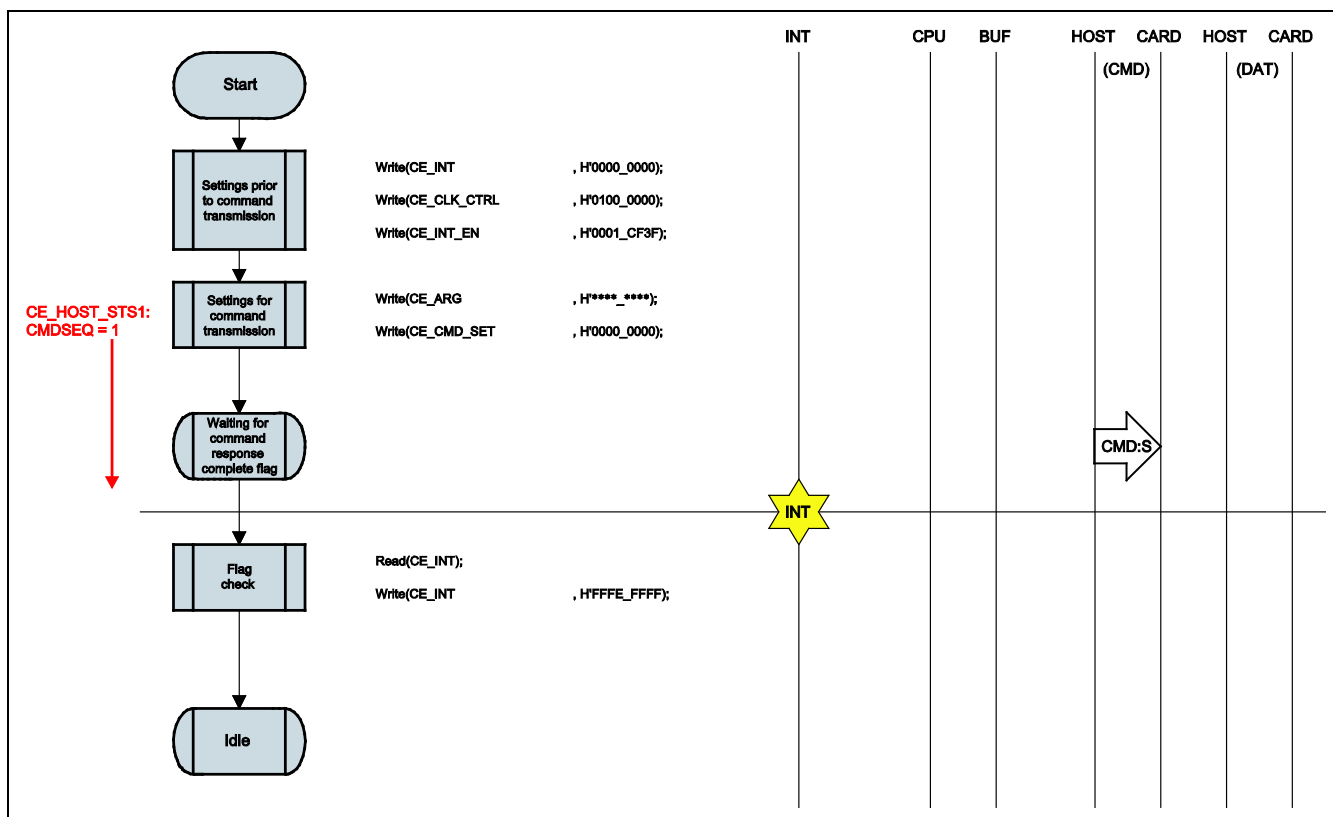


Figure 49.13 Command Transmission (CMD0)

(3) Command transmission @ response reception

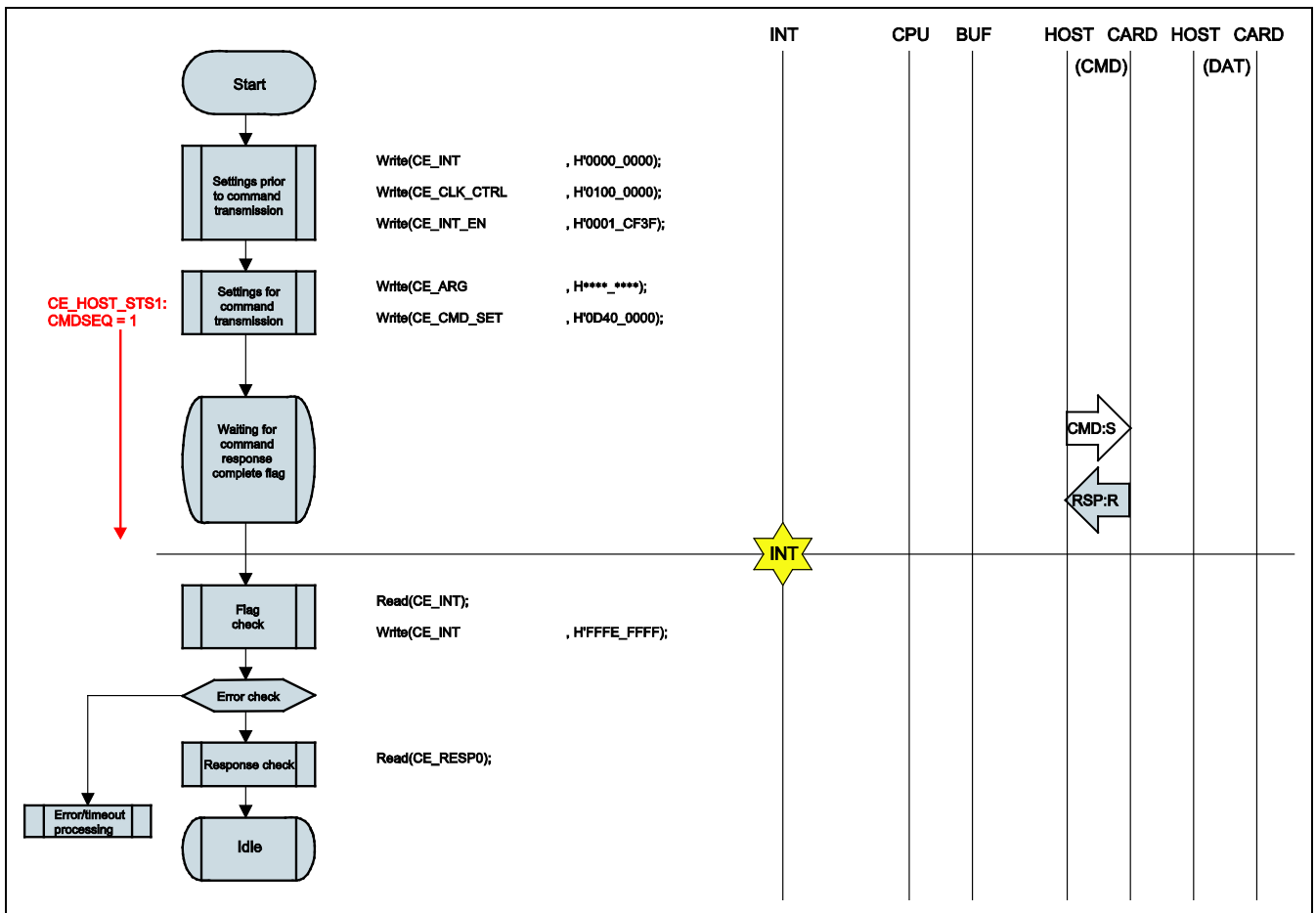


Figure 49.14 Command Transmission @ Response Reception (CMD13)

(4) Command transmission ® response reception (with response busy)

- When the busy time period is less than the period set by the SRBSYTO bits in CE\_CLK\_CTRL

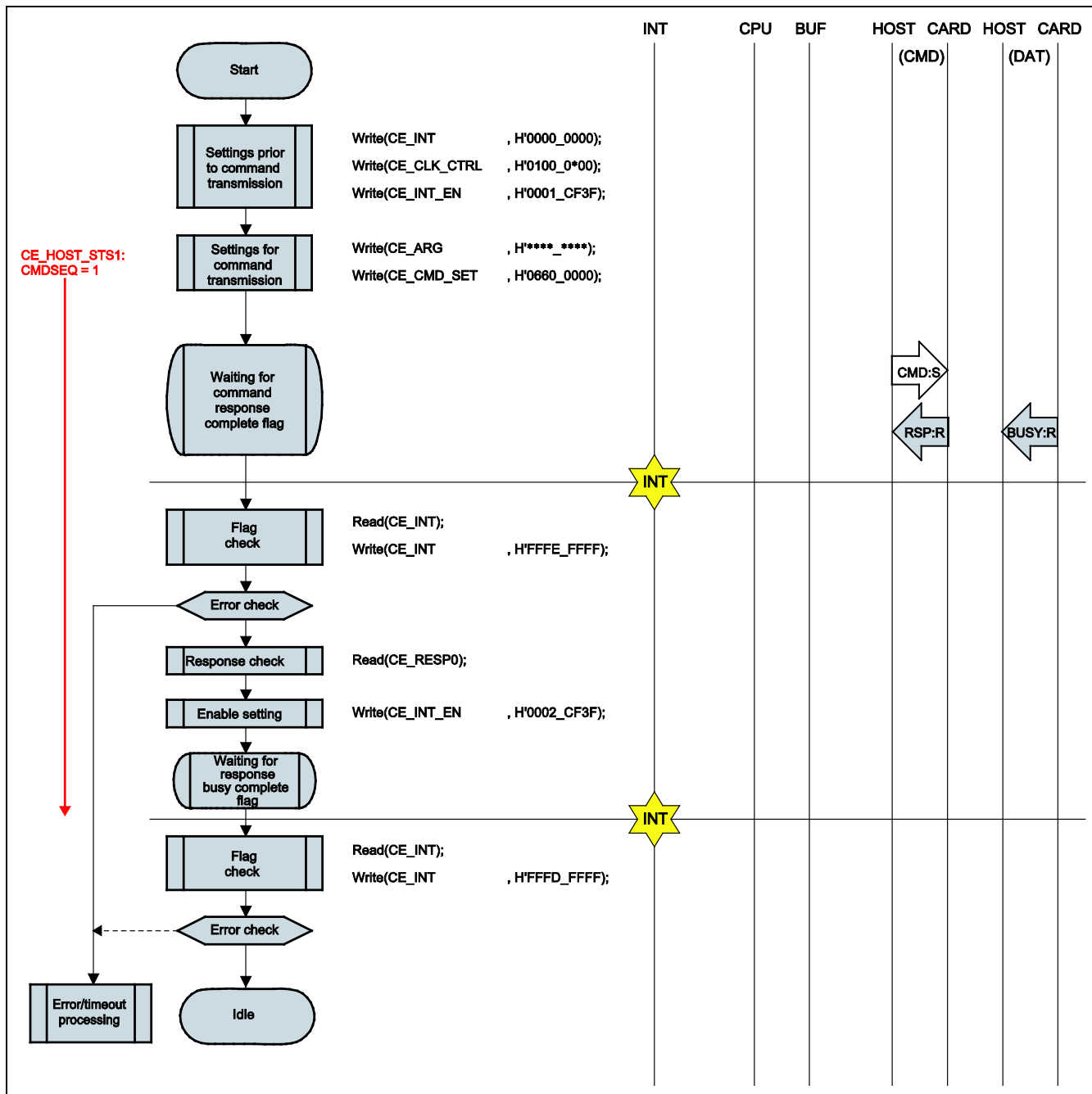


Figure 49.15 Command Transmission ® Response Reception (with Response Busy) (CMD6)

- When the busy time period may be equal to or beyond the period set by the SRBSYTO bits in CE\_CLK\_CTRL

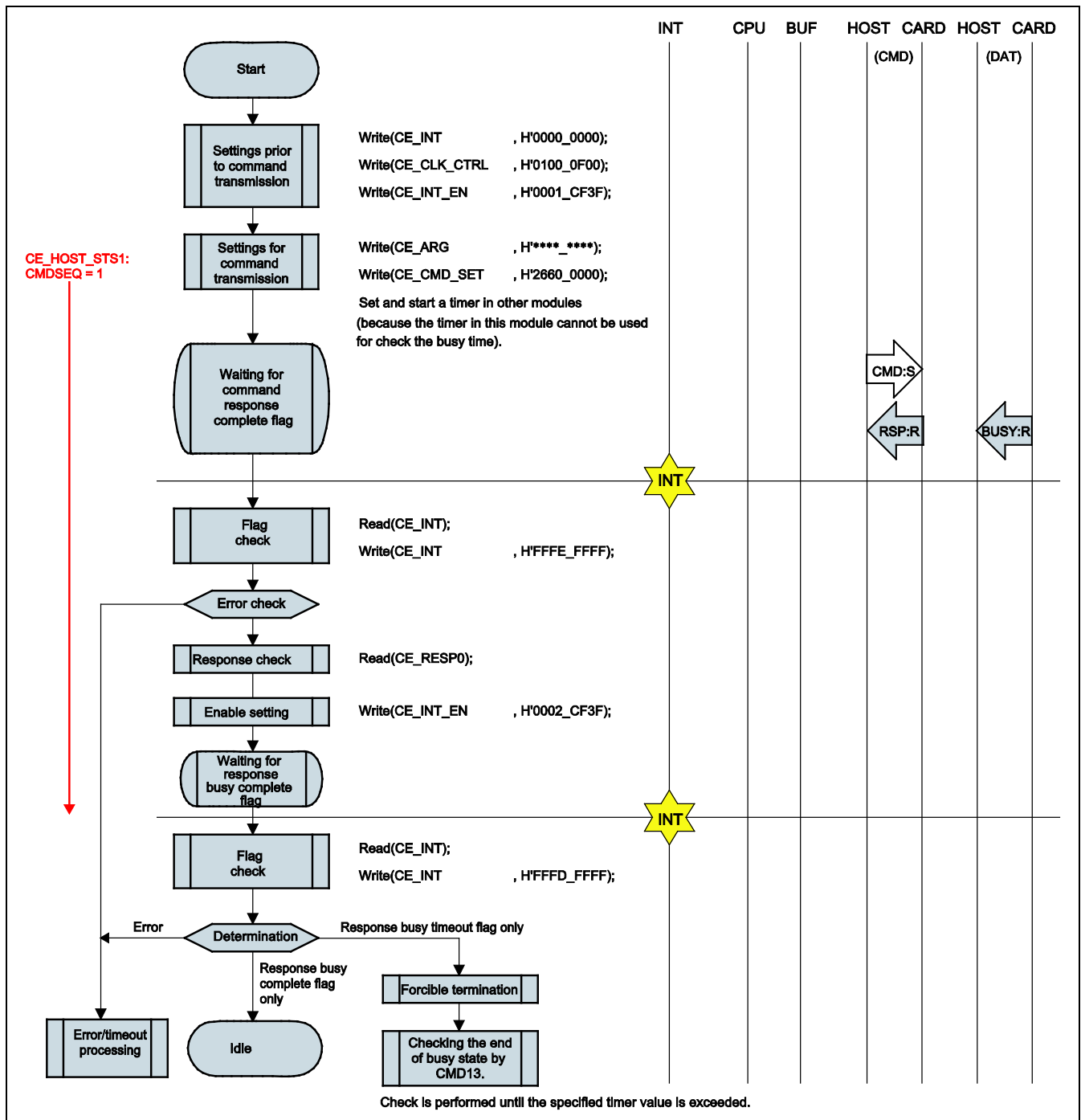


Figure 49.16 Command Transmission & Response Reception (with Response Busy) (CMD38)

(5) Single-block read

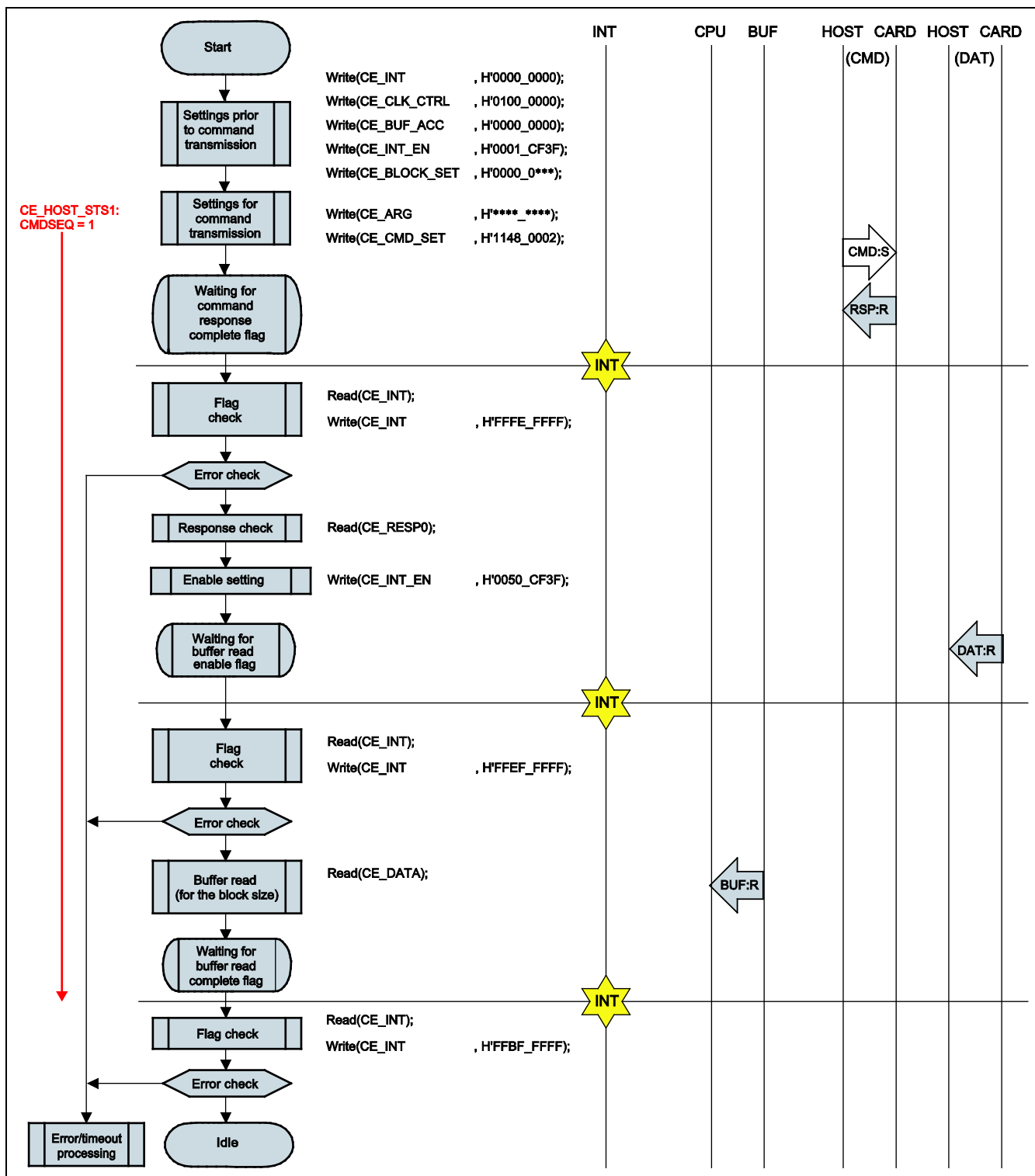


Figure 49.17 Single-Block Read (CMD17)

(6) Multi-block read

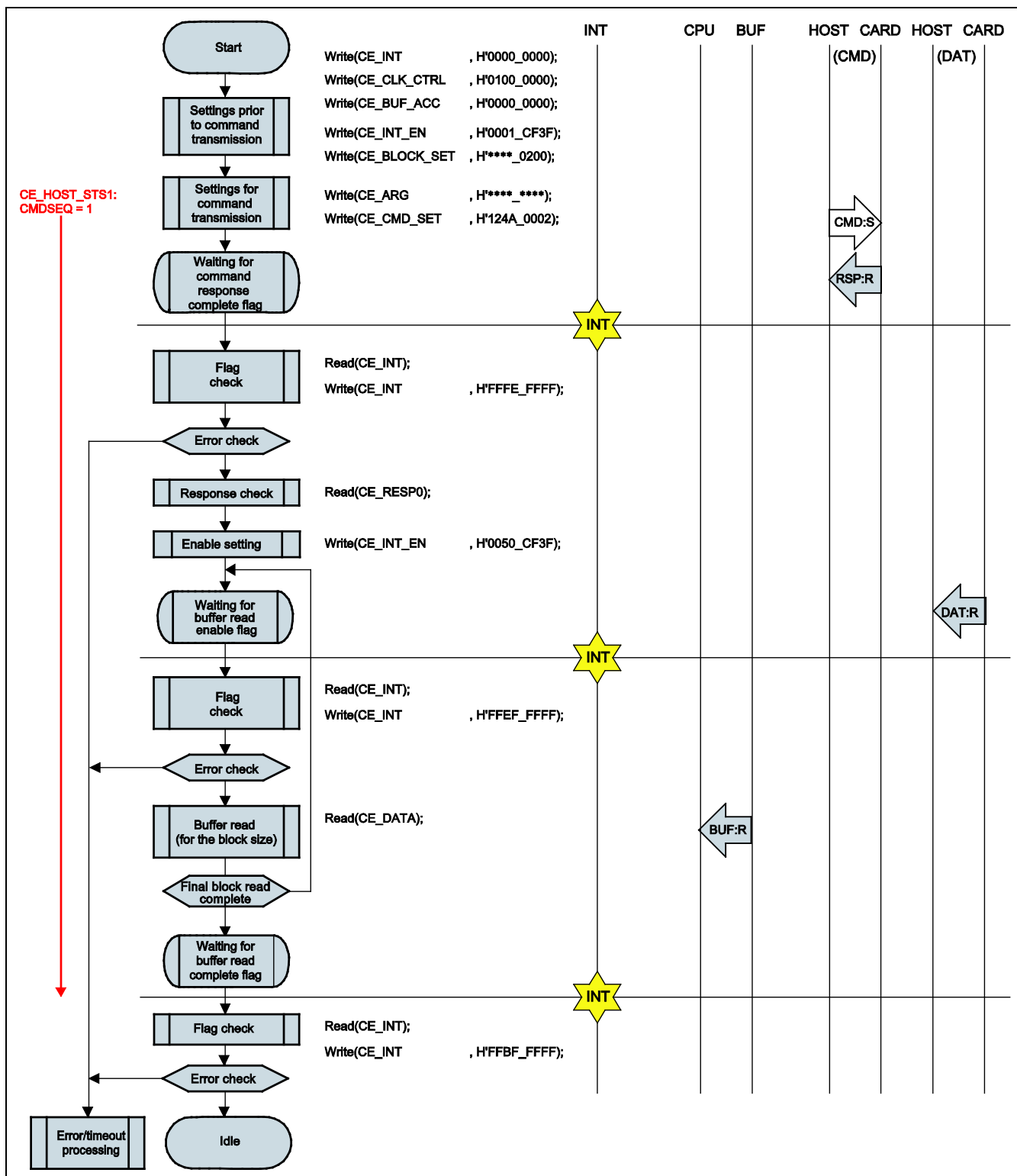


Figure 49.18 Multi-Block Read (CMD18 Pre-Defined)

(7) Multi-block read (with automatic CMD12 issuance)

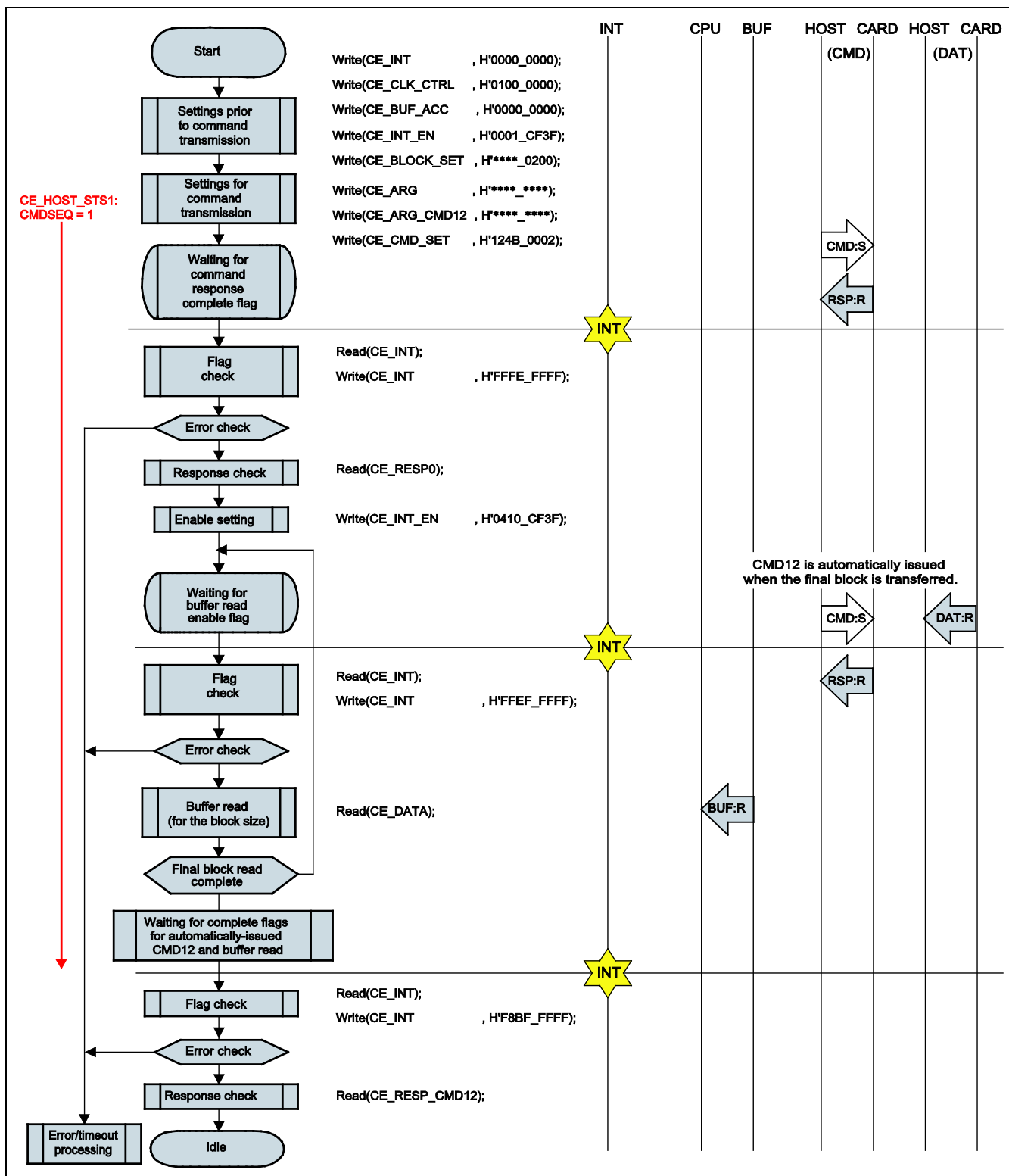


Figure 49.19 Multi-Block Read (with Automatic CMD12 Issuance) (CMD18 Open-Ended)



(8) Single-block write

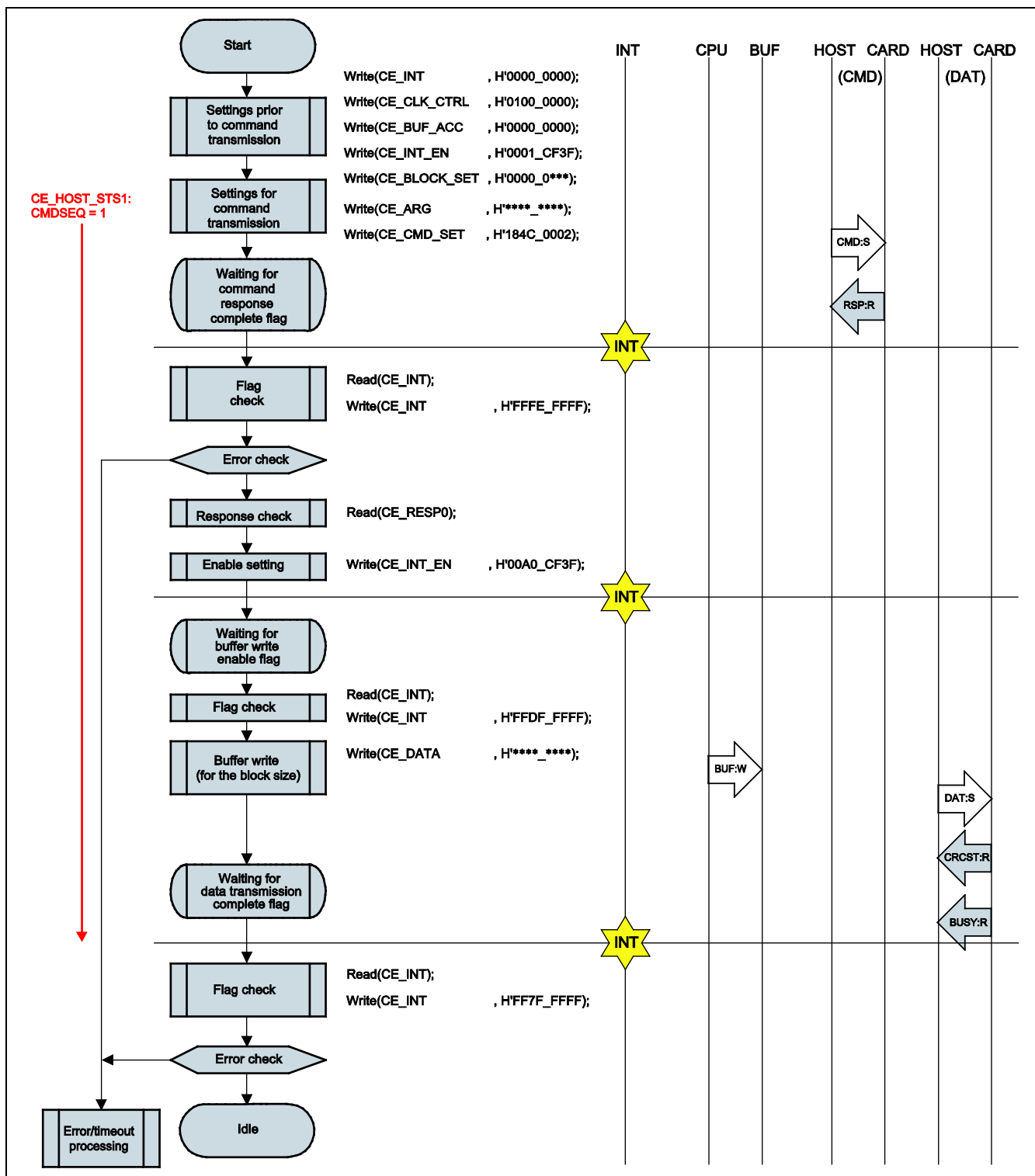


Figure 49.20 Single-Block Write (CMD24)

(9) Multi-block write

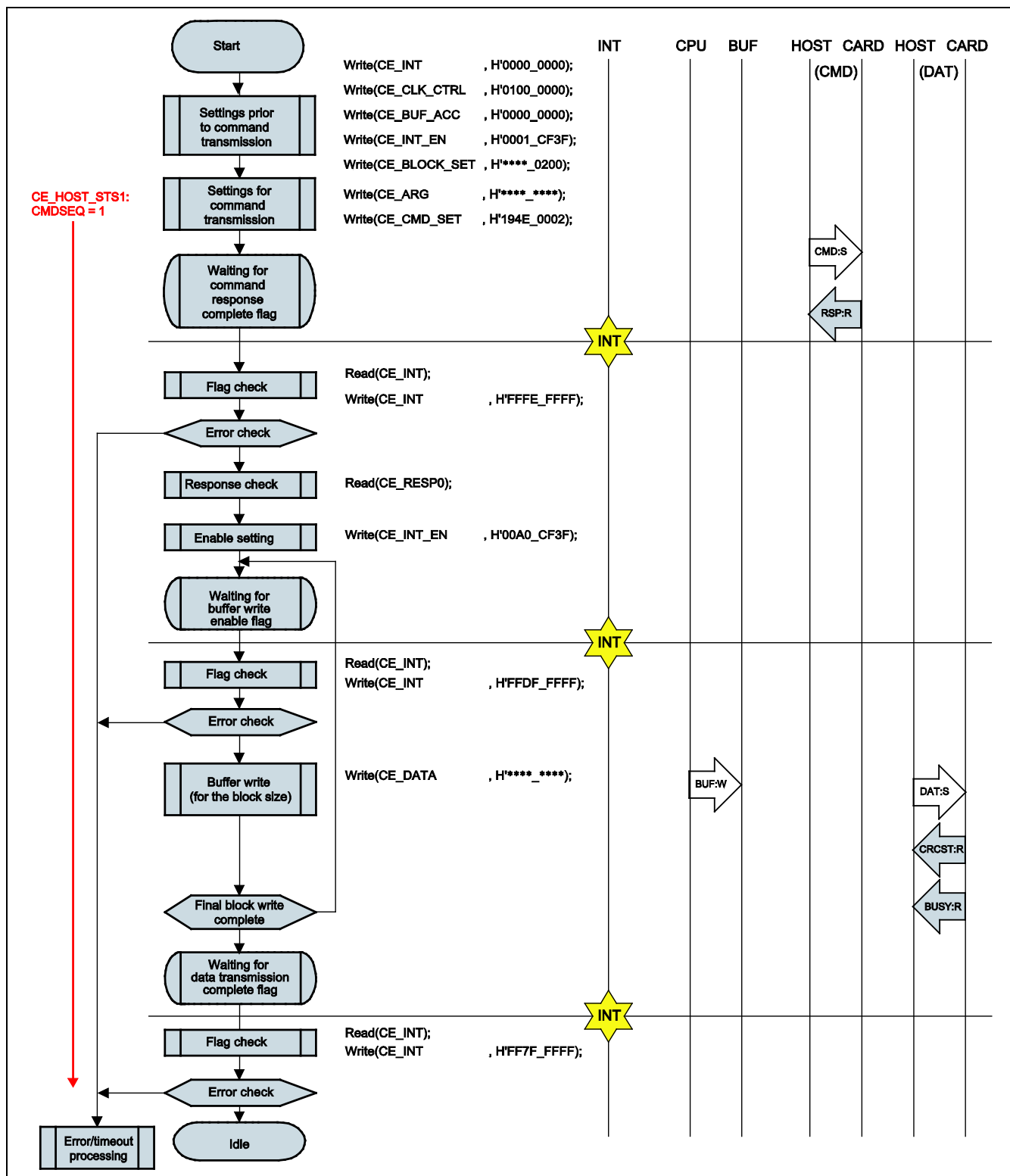


Figure 49.21 Multi-Block Write (CMD25 Pre-Defined)

(10) Multi-block write (with automatic CMD12 issuance)

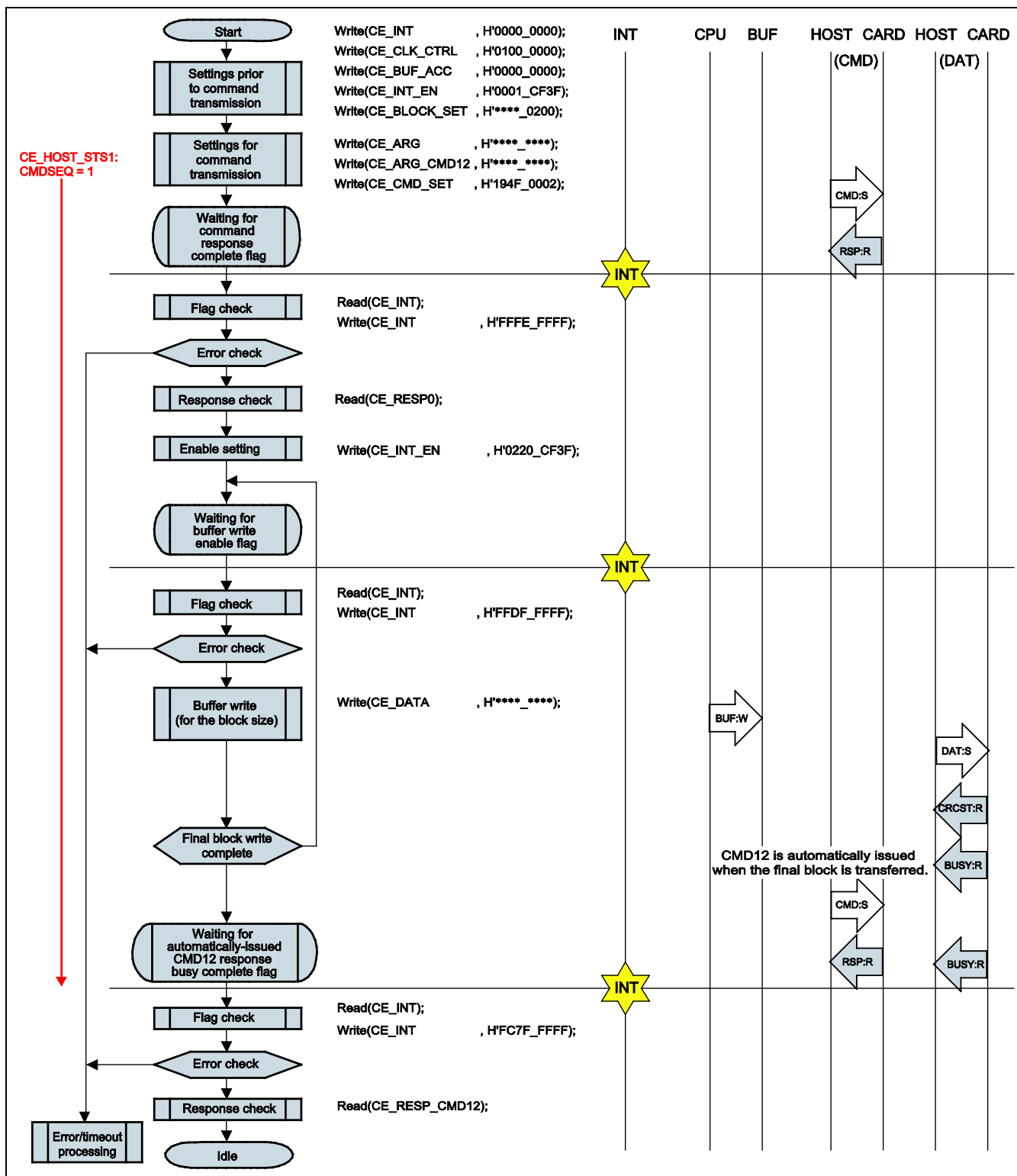


Figure 49.22 Multi-Block Write (with Automatic CMD12 Issuance) (CMD25 Open-Ended)

(11) Boot operations

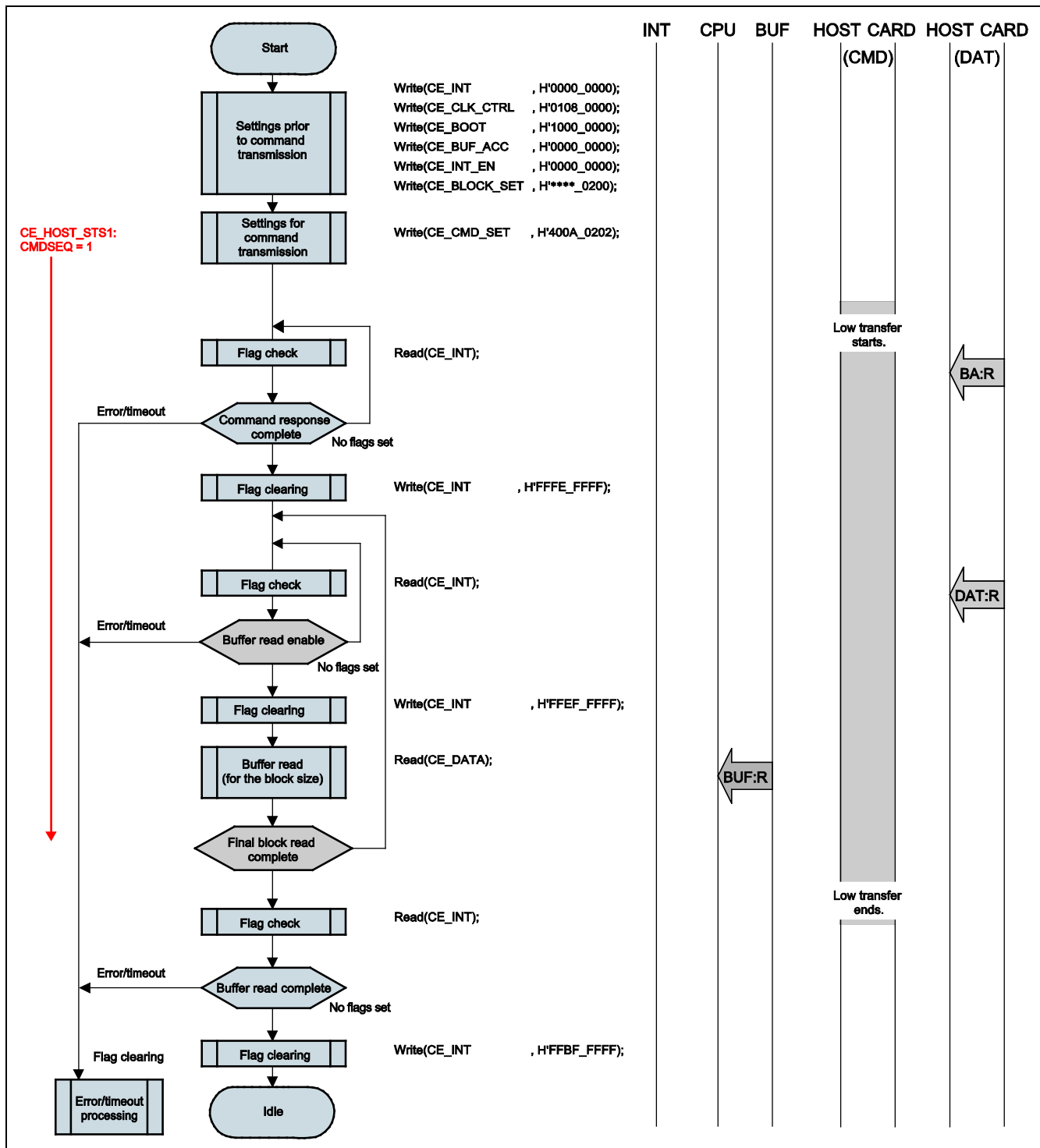


Figure 49.23 Boot Operations (with Boot Acknowledge)

(12) Forcible termination

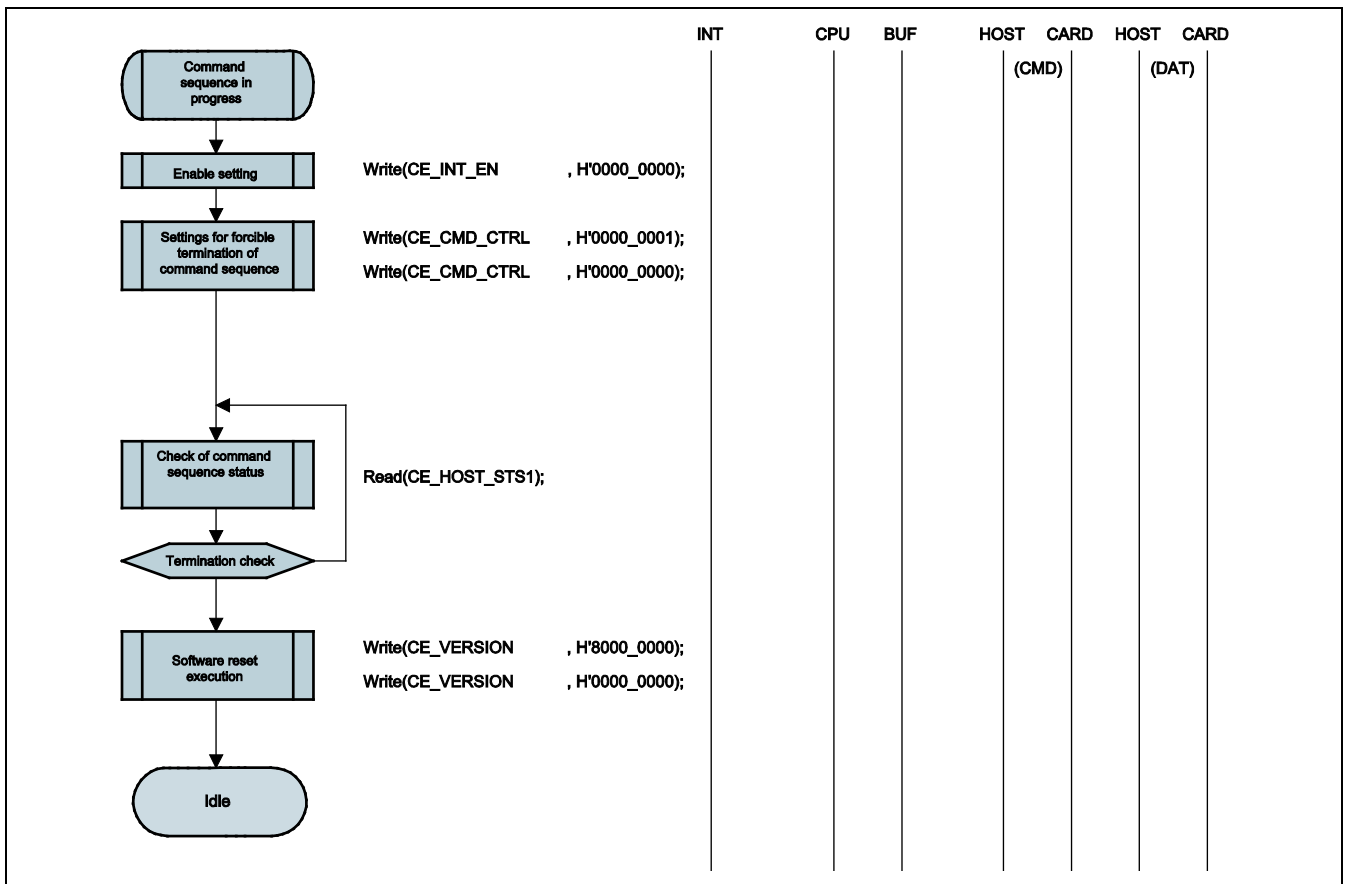


Figure 49.24 Forcible Termination



## 49.4 Usage Note

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

### 49.4.1 Multi-Block Transfer

It is recommended to use the pre-defined multi-block transfer for a higher data transfer rate.

## 50. Serial-ATA Interface

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

### 50.1 Overview

The serial-ATA interface provides a serial ATA physical interface which complies with the serial-ATA standard.

Note: References to the SH-Navi2G in this section refer to a previous product from Renesas. The serial-ATA interface of the RZ/G1H and M/N has backward compatibility with that of the SH-Navi2 series.

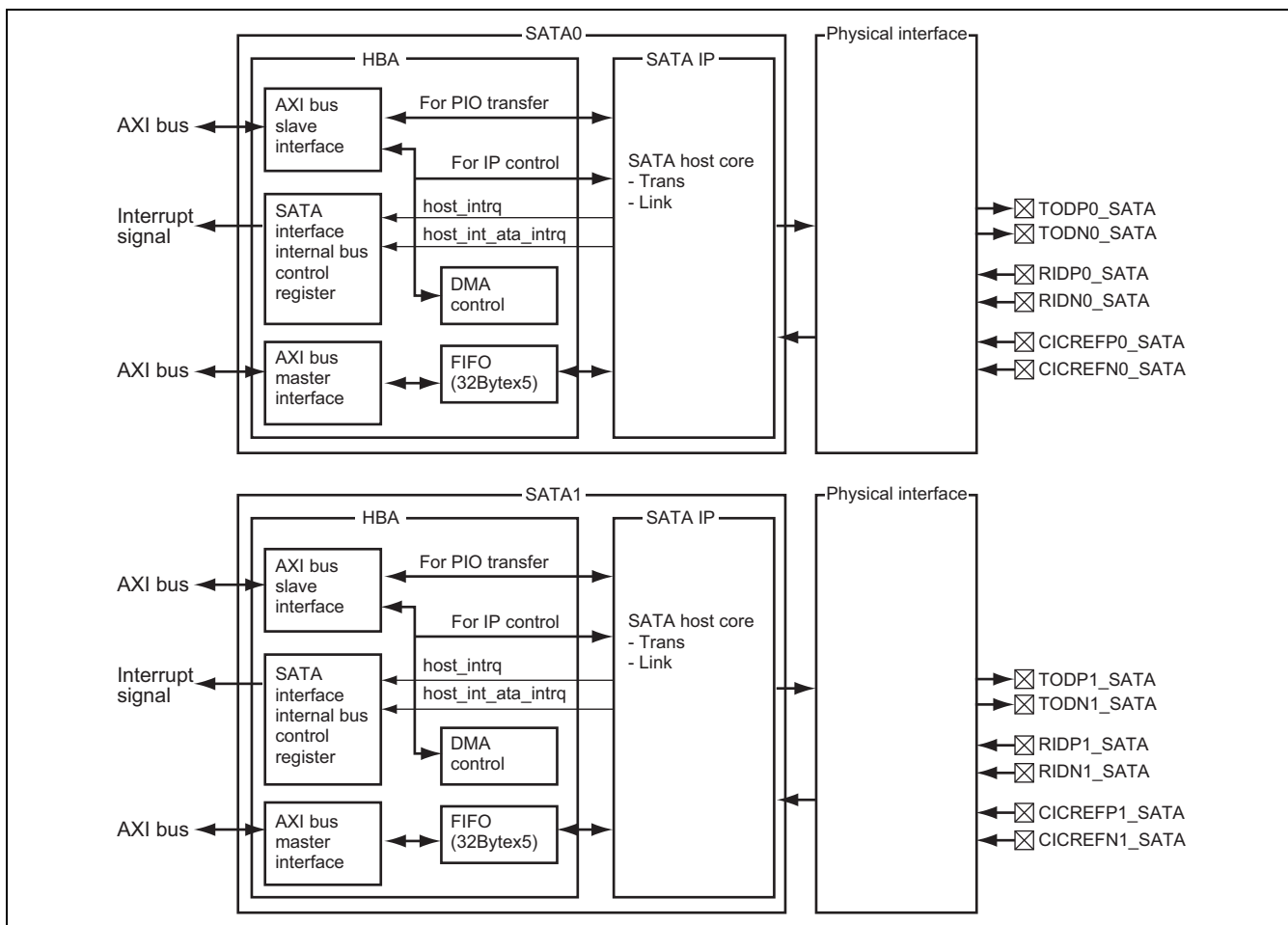
#### 50.1.1 Features

- Supports 3.0 Gbps (second generation) and 1.5 Gbps (first generation) transfer rate.
- Two interfaces in master mode
- Supports the emulation and descriptor modes of the SH-Navi2 parallel-ATAPI (host controller).
- Parallel-ATA emulation
- Packet protocol transfer
- Supports SATA standard 8b/10b encoding, cyclic redundancy check (CRC), and scrambling modes.
- Supports the SATA power management mode (partial mode/slumber mode).
- Does not support reset speed negotiation (RSN).

#### 50.1.2 Block Diagram

Figure 50.1 shows the block diagram of the SATA interfaces.





**Figure 50.1 Block Diagram of SATA Interfaces**

host\_intrq and host\_int\_ata\_intrq are internal interrupt request signals. For the interrupt sources of these signals, refer to the description of the SATA INT status register.

For a physical interface, the SATA function must be selected by the M23 or M24 pin.

### 50.1.3 Input/Output Pins

Table 50.1 shows the external pins of the SATA interface.

**Table 50.1 External Pins**

Name	Pin Name	SATA Symbol	I/O	Description	RZ/G Series Products			
					RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Reference clock	CICREFP0_SATA	—	Input	Reference clock input to the PLL circuit in the Serial-ATA module (differential input). Apply a 100-MHz clock.	√	√	√	—
	CICREFN0_SATA							
	CICREFP1_SATA							
	CICREFN1_SATA							
Transmit data	TODP0_SATA	TX+	Output	Pins for data transmission pins. A 3.0-GHz (second generation) signal or 1.5-GHz (first generation) signal is transmitted through these pins.  The pins with names ending in P and N are combined to provide a differential signal.	√	√	√	—
	TODN0_SATA	TX-						
	TODP1_SATA							
	TODN1_SATA							
Receive data	RIDP0_SATA	RX+	Input	Pins for data reception. A 1.5-GHz (first generation) or 3.0-GHz (second generation) signal is received through these pins.  The pins with names ending in P and N are combined to provide a differential signal.	√	√	√	—
	RIDN0_SATA	RX-						
	RIDP1_SATA							
	RIDN1_SATA							

### 50.1.4 Register Configuration

Table 50.2 shows the register configuration of the SATA interface. The set of registers shown below are allocated to the register map space.

The area allocated for the SATA0 interface is from H'EE30 0000 to H'EE4F FFFF (2-Mbyte space).

The area allocated for the SATA1 interface is from H'EE50 0000 to H'EE6F FFFF (2-Mbyte space).

These registers must not be accessed in any access sizes other than those listed in the table.

Addresses other than those listed below must not be write-accessed to. If written to, operation is not guaranteed. If read, an undefined value is read.

**Table 50.2 Register Configuration**

Add the offsets under “address” below to H'EE30 0000 for SATA0 and to H'EE50 0000 for SATA1.

Name	Symbol	R/W	Address	Access Size (Available Bit Size)	RZ/G Series Products			
					RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
<b>OPSH-Navi2G/ATAPI-ATA compatible task registers</b>					√	√	√	—
Shadow data register	DATA	R/W	H'0100	32 (16)* <sup>1</sup>	√	√	√	—
Shadow error register	SERR	R	H'0104	32 (8)* <sup>2</sup>	√	√	√	—
Shadow features register	SFEATURES	W	H'0104	32 (8)* <sup>2</sup>	√	√	√	—
Shadow sector CNT register	SECCNT	R/W	H'0108	32 (8)* <sup>2</sup>	√	√	√	—
Shadow LBA low register	LBALOW	R/W	H'010C	32 (8)* <sup>2</sup>	√	√	√	—
Shadow LBA mid register	LBAMID	R/W	H'0110	32 (8)* <sup>2</sup>	√	√	√	—
Shadow LBA high register	LBAHIGH	R/W	H'0114	32 (8)* <sup>2</sup>	√	√	√	—
Shadow device/head register	DEVHEAD	R/W	H'0118	32 (8)* <sup>2</sup>	√	√	√	—
Shadow status register	SSTATUS	R	H'011C	32 (8)* <sup>2</sup>	√	√	√	—
Shadow command register	SCOM	W	H'011C	32 (8)* <sup>2</sup>	√	√	√	—
Obsolete	—	R	H'0120 to H'0134		√	√	√	—
Shadow alternates status register	SALTSTS	R	H'0138	32 (8)* <sup>2</sup>	√	√	√	—
Shadow device control register	SDEVCON	W	H'0138	32 (8)* <sup>2</sup>	√	√	√	—
ATAPI control register	ATAPI_CONTROL1	R/W	H'0180	32	√	√	√	—
ATAPI status register	ATAPI_STATUS	R/WC0	H'0184	32	√	√	√	—
Interrupt enable register	ATAPI_INT_ENABLE	R/W	H'0188	32	√	√	√	—
Descriptor table base address register	ATAPI_DTB_ADR	R/W	H'0198	32	√	√	√	—
DMA start address register	ATAPI_DMA_START_ADR	R/W	H'019C	32	√	√	√	—
DMA transfer count register	ATAPI_DMA_TRANS_CNT	R/W	H'01A0	32	√	√	√	—
ATAPI control 2 register	ATAPI_CONTROL2	R/W	H'01A4	32	√	√	√	—
ATAPI signal status register	ATAPI_SIG_ST	R	H'01B0	32	√	√	√	—
Byte swap register	ATAPI_BYTE_SWAP	R/W	H'01BC	32	√	√	√	—
BIST config register	BISTCONF	R/W	H'102C	32	√	√	√	—
Shadow data register	SDATA	R/W	H'1100	32	√	√	√	—
Shadow error register	SSERR	R	H'1104	32	√	√	√	—
Shadow features register	SSFEATURES	W	H'1104	32	√	√	√	—
Shadow sector CNT register	SSECCNT	R/W	H'1108	32	√	√	√	—

Name	Symbol	R/W	Address	Access Size (Available Bit Size)	RZ/G Series Products			
					RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Shadow LBA low register	SLBALOW	R/W	H'110C	32	√	√	√	—
Shadow LBA mid register	SLBAMID	R/W	H'1110	32	√	√	√	—
Shadow LBA high register	SLBAHIGH	R/W	H'1114	32	√	√	√	—
Shadow device/head register	SDEVHEAD	R/W	H'1118	32	√	√	√	—
Shadow status register	SSSTATUS	R	H'111C	32	√	√	√	—
Shadow command register	SSCOM	W	H'111C	32	√	√	√	—
Shadow alternate status register	SSALTSTS	R	H'1204	32	√	√	√	—
Shadow device control register	SSDEVCON	W	H'1204	32	√	√	√	—
SATA extend register	SATAER	R/W	H'1220	32	√	√	√	—
SCR Sstatus register	SCRSSSTS	R	H'1400	32	√	√	√	—
SCR Serror register	SCRSEERR	R/WC1	H'1404	32	√	√	√	—
SCR Scontrol register	SCRSCON	R/W	H'1408	32	√	√	√	—
SCR Sactive register	SCRSACT	R/W	H'140C	32	√	√	√	—
SATA INT status register	SATAINTSTAT	RC	H'1508	32	√	√	√	—
SATA INT mask register	SATAINTMASK	R/W	H'150C	32	√	√	√	—
PHY STOP register	PHYSTOP	R/W	H'1568	32	√	√	√	—
Rx DMA setup FIS dword 0 register	DMADW0	R/W	H'1620	32	√	√	√	—
Rx DMA setup FIS dword 1 register	DMADW1	R/W	H'1624	32	√	√	√	—
Rx DMA setup FIS dword 2 register	DMADW2	R/W	H'1628	32	√	√	√	—
Rx DMA setup FIS dword 3 register	DMADW3	R/W	H'162C	32	√	√	√	—
Rx DMA setup FIS dword 4 register	DMADW4	R/W	H'1630	32	√	√	√	—
Rx DMA setup FIS dword 5 register	DMADW5	R/W	H'1634	32	√	√	√	—
Rx DMA setup FIS dword 6 register	DMADW6	R/W	H'1638	32	√	√	√	—

Notes: See the descriptions of individual registers for the R/W attributes of the valid bits.

1. Bits 15 to 0 of the data bus are used.
2. Bits 7 to 0 of the data bus are used.

## 50.2 Register Descriptions

- Legend:
  - Address: Address of the register
  - Bit map: Bit configuration of the entire register. The initial value and R/W of the individual bits are also indicated.
  - Bit: Bit number and range
  - Bit name: Bit name or field name
  - Initial value: Register value after a reset
  - : Undefined value
  - R/W: Readable/writable. The written value can be read.
  - R/WC0: Readable/writable. Writing 0 initializes the bit. Writing 1 is ignored.
  - R/WC1: Readable/writable. Writing 1 initializes the bit. Writing 0 is ignored.
  - R: Read-only. The write value should always be 0. (If a read/write value is specified in the bit description, however, it must be observed.)
  - /W: Write-only. The read value is undefined.
  - RC: Read-only. The bit is cleared to 0 after it has been read.

### 50.2.1 Note on the Access to the Registers Allocated to H'1018 to H'10A8

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

No normal access can basically be made to the registers that are allocated to H'1018 to H'10A8 unless the PHYRDY state is established. The PHYRDY state here refers to the state in which the rate of transfer between the host and device is established and they are ready for data transfer. In this state, bits 3-0 of the SCR SStatus register described in section 50.2.26, SCR SStatus Register (SCRSSSTS), is set to B'0011\*. The integrity of the value of a register that is accessed in the non-PHYRDY state is not guaranteed.

### 50.2.2 ATAPI Control Register (ATAPI\_CONTROL1)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ISM
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	DTA32 M	—	—	—	RESET	—	—	—	DESE	R/W	STOP	START
Initial value:	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0
R/W:	R	R	R	R	R/W	R	R	R	R/W	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 17	—	—	R	Reserved The write value should always be 0.
16	ISM	0	R/W	Interrupt Status mode 0: IP compatible mode Normal operating mode of the SATA INT status register (SATAINTSTAT). 1: CIS interrupt mode A valid interrupt source specified by the SATA INT mask register is set in the SATA INT status register (SATAINTSTAT). No interrupts are generated by valid sources specified in the SATA INT mask register (SATAINTMASK). Read access to the SATA INT status register (SATAINTSTAT) will not negate the ATA-sourced DEVINT interrupt signal. Note: For details, refer to section 50.3.6, Interrupt Modes. Set ISM to 1 while the SATA-IP host core block is being reset (bit 7 (RESET) is 1). Do not change the value of ISM after the SATA-IP host core block has been released from the reset state (bit 7 (RESET) is 0).
15 to 12	—	All 0	R	This bit is fixed to 0 and cannot be set to 1.
11	DTA32M	0	R/W	DTA32M enables bits 31 to 29 of the descriptor DMA start address in descriptor table operation mode. This causes the termination flag to be changed from bit 31 to bit 0. 0: SH-Navi1-compatible mode 1: Enabled bits of the descriptor DMA start address are bits 31 to 2.
10 to 8	—	All 0	R	These bits are fixed to 0 and cannot be set to 1.
7	RESET	0	R/W	RESET controls the SATA-IP host core block. Setting this bit to 1 resets the SATA-IP host core block.
6 to 4	—	All 1	R	These bits are fixed to 1. Attempting to set these bits to 0 is ignored and not reflected in the value of the bits.

Bit	Bit Name	Initial Value	R/W	Description
3	DESE	0	R/W	DESE controls the descriptor table operation mode. 0: Descriptor functions disabled 1: Descriptor functions enabled
2	R/W	0	R/W	R/W controls FIFO read/write. 0: FIFO write (data-out operation at DMA transfer) 1: FIFO read (data-in operation at DMA transfer) Set this bit to 1 when reading data from the SATA device. Clear it to 0 when writing data to the SATA device.
1	STOP	0	R/W	This bit forces termination of DMA transfer. When writing 0: Ignored 1: Forcibly terminates data transfer When reading 0: Forced termination command is not issued. 1: Forced termination of data transfer command is issued. This bit is cleared to 0 when the next DMA starts. To power down (SATA internal clock turns off) while DMA is active (ACT = 1), DMA transfer should be forcibly terminated. Note: Transfer cannot always be resumed from the address at which DMA transfer has been forcibly terminated.
0	START	0	R/W	This bit initiates DMA transfer. If this bit set to 1 then the DMA transfer is started. When cleared to 0, this bit is ignored. When writing 0: Ignored 1: Starts DMA transfer When reading 0: DMA transfer is not active 1: DMA transfer is in busy state Note: Access to the task file register is prohibited while DMA is active.

### 50.2.3 ATAPI Status Register (ATAPI\_STATUS)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SSBSY	SSDRDY	—	—	SSDRQ	—	—	SSERR	—	—	—	—	—	—	—	—
Initial value:	0	0	—	—	0	—	—	0	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	SATAINT	—	—	SWERR	—	DNEND	DEVTRM	DEVINT	—	ERR	NEND	ACT
Initial value:	—	—	—	—	0	—	—	0	—	0	0	0	—	0	0	0
R/W:	R	R	R	R	R	R	R	R/WC0	R	R/WC0	R/WC0	R	R	R/WC0	R/WC0	R

Bit	Bit Name	Initial Value	R/W	Description
31	SSBSY	0	R	SSBSY corresponds to INTBSY of the SATA INT status register (SATAINTSTAT), the BSY bit value of the shadow status register (SSTATUS). This bit is enabled when ISM = 1 and disabled (0) when ISM = 0. The write value should always be 0.
30	SSDRDY	0	R	SSDRDY corresponds to INTDRDY of the SATA INT status register (SATAINTSTAT), the DRDY bit value of the shadow status register (SSTATUS). This bit is enabled when ISM = 1 and disabled (0) when ISM = 0. The write value should always be 0.
29, 28	—	—	R	Reserved The write value should always be 0.
27	SSDRQ	0	R	SSDRQ corresponds to INTDRQ of the SATA INT status register (SATAINTSTAT), the DRQ bit value of the shadow status register (SSTATUS). This bit is enabled when ISM = 1 and disabled (0) when ISM = 0. The write value should always be 0.
26, 25	—	—	R	Reserved The write value should always be 0.
24	SSERR	0	R	SSERR corresponds to INTERR of the SATA INT status register (SATAINTSTAT), the ERR bit value of the shadow status register (SSTATUS). This bit is enabled when ISM = 1 and disabled (0) when ISM = 0. The write value should always be 0.
23 to 12	—	—	R	Reserved The write value should always be 0.
11	SATAINT	0	R	SATAINT indicates the status of host-intrq of the SATA-IP block. This bit is read-only. host_intrq is the internal interrupt request signal. For the interrupt source of this signal, refer to the description of the SATA INT Status register. The write value should always be 0.
10, 9	—	—	R	Reserved The write value should always be 0.



Bit	Bit Name	Initial Value	R/W	Description
8	SWERR	0	R/WC0	Software error bit. 1 in this bit indicates that the task file register is accessed when the DMA is active. Access to the SH-Navi2G/ATAPI-ATA-compatible task register is prohibited while DMA is active. This bit is set to 1 when a PIO transfer is performed during DMA transfer. In this case, no output is directed to the SATA-IP block and the access is ignored. Writing 0 resets this bit.
7	—	—	R	Reserved The write value should always be 0.
6	DNEND	0	R/WC0	DNEND indicates that all DMAs have successfully ended in the descriptor mode. Writing 0 resets this bit.
5	DEVTRM	0	R/WC0	DEVTRM is set to 1 when the DMA mode for the SATA_IP block is terminated before the number of DMA transfer bytes defined in the DMA transfer count register (ATAPI_DMA_TRANS_CNT) is reached (corresponds to P-ATA device's device termination operation). Writing 0 resets this bit.
4	DEVINT	0	R	DEVINT indicates the status of host_int_ata_intrq in the SATA-IP block (host_int_ata_intrq signal corresponds to the IDEINT signal of the P-ATA device and ATA of the SATA INT status register (SATAINTSTAT)). This bit is read-only. Since this LSI chip preserves no status, this bit is cleared to 0 when host_int_ata_intrq is set to 0. The SATA_HBA block regards any interrupt signal from the SATA-IP block as a level trigger input. host_int_ata_intrq is negated by the SATA device to clear the interrupt pending state after the shadow status register (SSTATUS) is read out. There is no time specification. The write value should always be 0.
3	—	—	R	Reserved The write value should always be 0.
2	ERR	0	R/WC0	ERR is set to 1 when the host forcibly terminated the DMA transfer. Writing 0 resets this bit.
1	NEND	0	R/WC0	NEND indicates that DMA has been successfully terminated. Writing 0 resets this bit.
0	ACT	0	R	ACT indicates that DMA is active. To power down (SATA internal clock turns off) while DMA is active (ACT = 1), DMA transfer should be forcibly terminated (STOP = 1). The write value should always be 0.

### 50.2.4 Interrupt Enable Register (ATAPI\_INT\_ENABLE)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

When 1 is written to a bit, the interrupt signal corresponding to the bit in the ATAPI status register (ATAPI\_STATUS) is enabled.

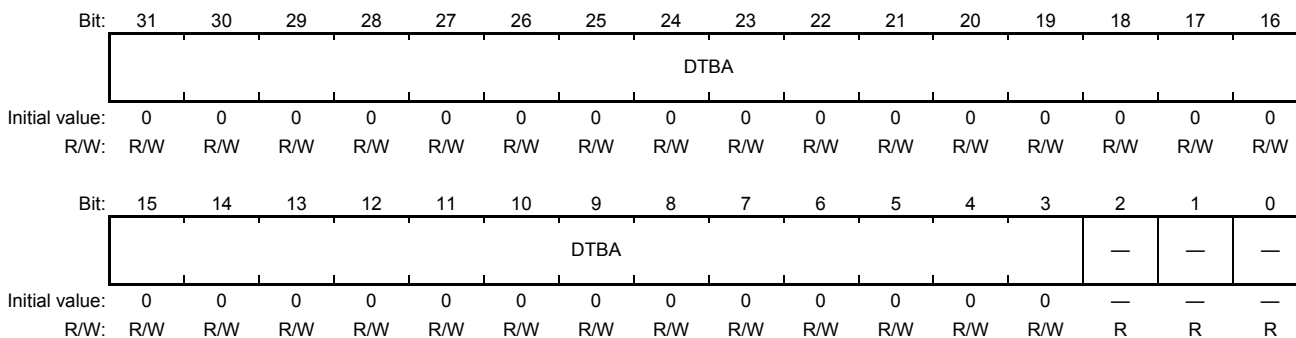
Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	iSATAI NT	—	—	iSWER R	—	iDNEN D	iDEV TRM	iDEVIN T	—	iERR	iNEND	iACT
Initial value:	—	—	—	—	0	—	—	0	—	0	0	0	—	0	0	0
R/W:	R	R	R	R	R/W	R	R	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 12	—	—	R	Reserved The write value should always be 0.
11	iSATAINT	0	R/W	SATAINT interrupt enable
10, 9	—	—	R	Reserved The write value should always be 0.
8	iSWERR	0	R/W	SWERR interrupt enable
7	—	—	R	Reserved The write value should always be 0.
6	iDNEND	0	R/W	DNEND interrupt enable
5	iDEVTRM	0	R/W	DEVTRM interrupt enable
4	iDEVINT	0	R/W	DEVINT interrupt enable
3	—	—	R	Reserved The write value should always be 0.
2	iERR	0	R/W	ERR interrupt enable
1	iNEND	0	R/W	NEND interrupt enable
0	iACT	0	R/W	ACT interrupt enable bit. Since ACT is cleared automatically when a DMA transfer is completed, interrupt processing should be completed during assertion.

Note: Writing 1 to a bit enables the interrupt signal corresponding to the bit in the ATAPI status register. Do not clear the interrupt mask of the INTC while the SATA module is being reset. For resetting of the SATA module, refer to the descriptions of SRCR8 register and SRSTCLR8 register of the RESET module. For the interrupt mask of INTC, refer to the description of IMR4S3 register in the section on the INTC module.

### 50.2.5 Descriptor Table Base Address Register (ATAPI\_DTBA\_ADR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—



Bit	Bit Name	Initial Value	R/W	Description
31 to 3	DTBA	0	R/W	These bits indicate the descriptor table base address. Bits 31 to 0 are used to set the descriptor table base address.
2 to 0	—	—	R	Reserved The write value should always be 0.

Note: This address does not change and the set value is retained even after the DMA becomes active.

#### (1) Descriptor Table

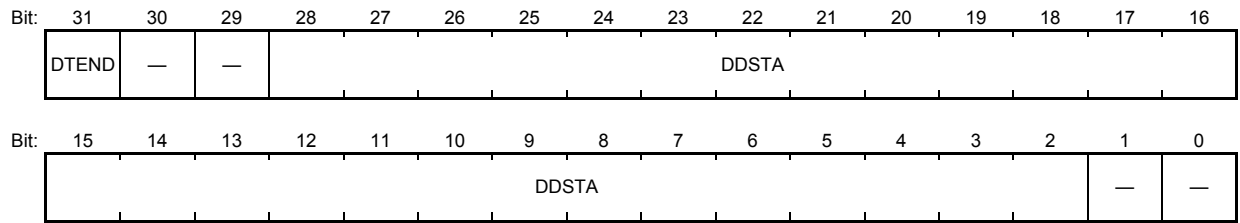
The descriptor table consists of the termination flag, the descriptor DMA start address (DDSTA), and the descriptor DMA transfer count (DDTRC).

##### (a) For SH-Navi1-compatible (DTA32M = 0, Initial value)

Table 50.3 Descriptor Table Map in Memory

Address	Data Description
DTBA	The first termination flag (bit 31 = 0) and DDSTA
DTBA + 4	The first DDTRC
DTBA + 8	The second termination flag (bit 31 = 0) and DDSTA
DTBA + 12	The second DDTRC
...	...
DTBA+8* (n - 1)	The n-th termination flag (bit 31 = 1) and DDSTA
DTBA+8* (n - 1) + 4	The n-th DDTRC

• Termination Flag and Descriptor DMA Start Address



Bit	Bit Name	Description
31	DTEND	DTEND controls the termination of a descriptor DMA operation 0: Validating the descriptor table When DTEND is 0, the system reads the DMA transfer count, transfers the DMA, and reads the next descriptor table. 1: Terminating the descriptor DMA operation When DTEND is 1, the system recognizes that the descriptor table is the last one.
30, 29	—	Reserved The write value should always be 0.
28 to 2	DDSTA	DDSTA shows the DMA start address in descriptor operation. Bits 28 to 0 are used to set the descriptor table start address on a byte basis. Bits 1 and 0 are ignored because it is necessary to secure the boundary of 32-bit addresses in the DMA start address.
1, 0	—	Reserved The write value should always be 0.

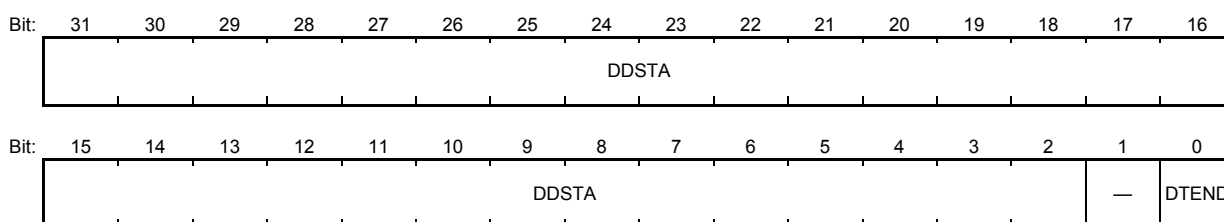
The valid flag and descriptor DMA start address should be set in the descriptor table base address + "m" in the memory, where m is multiple of 2 (such as 0, 2, 4, ...).

**(b) When Bits 31 to 29 of Descriptor DMA Start Address are Valid (DTA32M = 1)**

**Table 50.4 Descriptor Table Map in Memory**

Address	Data Description
DTBA	The first termination flag (bit 0 = 0) and DDSTA
DTBA + 4	The first DDTRC
DTBA + 8	The second termination flag (bit 0 = 0) and DDSTA
DTBA + 12	The second DDTRC
...	...
DTBA + 8* (n - 1)	The n-th termination flag (bit 0 = 1) and DDSTA
DTBA + 8* (n - 1) + 4	The n-th DDTRC

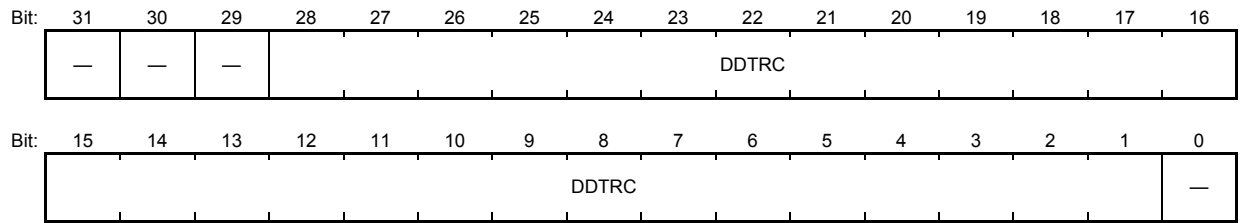
• Termination Flag and Descriptor DMA Start Address



Bit	Bit Name	Description
31 to 2	DDSTA	DDSTA shows the DMA start address in descriptor operation. Bits 31 to 0 are used to set the descriptor table start address on a byte basis. Bits 1 and 0 are ignored because it is necessary to secure the boundary of 32-bit addresses in the DMA start address.
1	—	Reserved The write value should always be 0.
0	DTEND	DTEND controls the termination of a descriptor DMA operation. 0: Validates the descriptor table When DTEND is 0, the DMA transfer count is read, DMA transfer is performed, and the next descriptor table is read. 1: Terminates the descriptor DMA operation When DTEND is 1, the last descriptor table is detected.

The valid flag and descriptor DMA start address should be set in the descriptor table base address + "m" in the memory, where m is multiple of 2 (such as 0, 2, 4, ...).

• Descriptor DMA Transfer Count

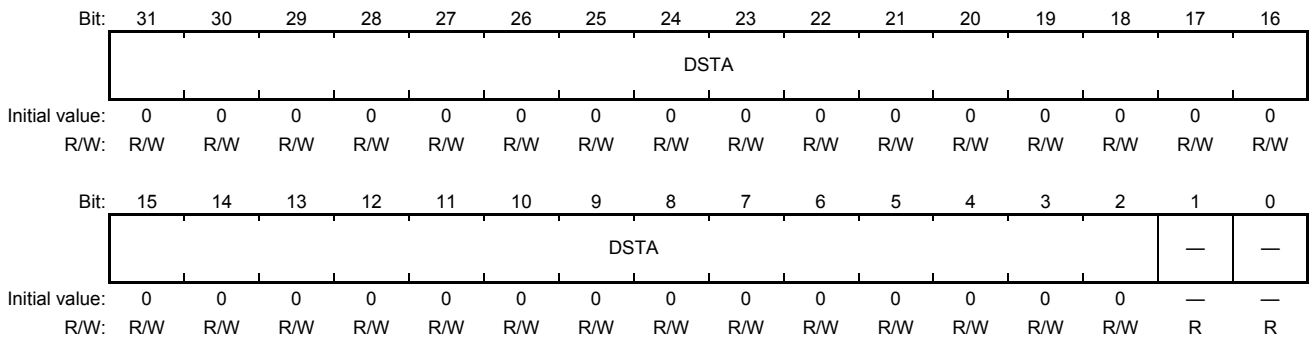


Bit	Bit Name	R/W	Description
31 to 29	—	R	Reserved The write value should always be 0.
28 to 1	DDTRC	R/W	These bits set the DMA transfer count during descriptor operation. Bits 28 to 0 are used to set the DMA transfer count on a byte basis. Bit 0 is ignored because the SATA data bus is handled on a 16-bit basis (on a word basis).
0	—	R	Reserved The write value should always be 0.

The descriptor DMA transfer count should be set in the descriptor table base address + "m" in the memory, where the value of m is any multiple number of 2 plus 1 (such as 1, 3, 5, ...).

**50.2.6 DMA Start Address Register (ATAPI\_DMA\_START\_ADR)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

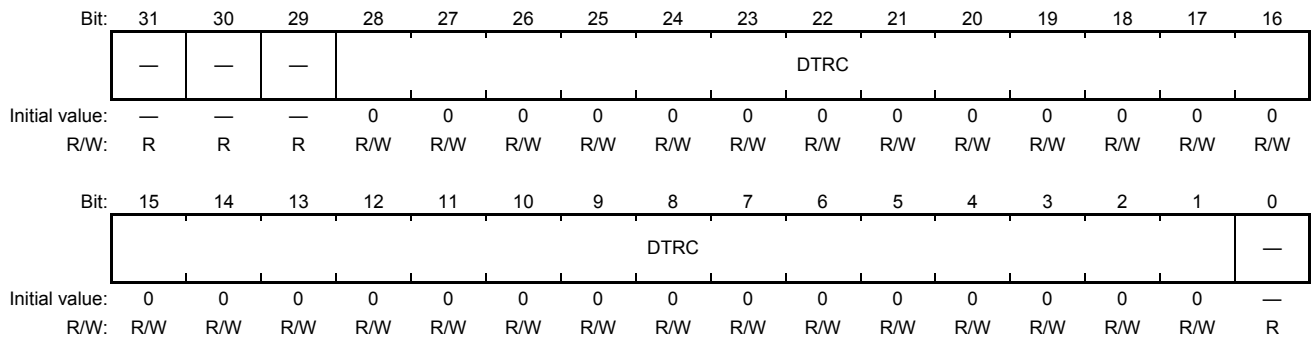


Bit	Bit Name	Initial Value	R/W	Description
31 to 2	DSTA	All 0	R/W	DSTA sets a DMA start address that indicates the data transfer start address in the memory. Bits 31 to 0 are used to set the DMA start address on a byte basis.  Bits 1 and 0 are ignored because it is necessary to secure the boundary of 32-bit addresses in the DMA start address.
1, 0	—	—	R	Reserved  The write value should always be 0.

Note: This address does not change and the set value is retained even after the DMA becomes active.

**50.2.7 DMA Transfer Count Register (ATAPI\_DMA\_TRANS\_CNT)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—



Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	—	R	Reserved The write value should always be 0.
28 to 1	DTRC	All 0	R/W	DTRC sets the DMA transfer count. Bits 28 to 0 are used to set the DMA transfer count on a byte basis. Bit 0 is ignored because the ATAPI data bus is handled on a 16-bit basis (on a word basis).
0	—	—	R	Reserved The write value should always be 0.

Note: This count value does not change and the set value is retained even after the DMA becomes active.



**50.2.8 ATAPI Control 2 Register (ATAPI\_CONTROL2)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	LWORD SWAP	WORD SWAP	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	0	0	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 3	—	—	R	Reserved The write value should always be 0.
2	LWORDSWAP	0	R/W	LWORDSWAP controls the swapping of the upper 32-bit data and the lower 32-bit data on a 2-longword basis (64-bit data) on the AXI bus. 0: Longword swap is not executed. The 64-bit data on the AXI bus appears in a big endian format. 1: Longword swap is executed between the SATA interface and the AXI bus interface. Note that longword swap is only available on data transfer when bit 0 (START) in the ATAPI control register (ATAPI_CONTROL1) = 1: DMA mode start.
1	WORDSWAP	0	R/W	WORDSWAP controls the swapping of the upper 16-bit data and the lower 16-bit data on a longword basis when the 64-bit data bus is enabled in the AXI bus. 0: Word swap is not executed. 1: Word swap is executed between the SATA interface and the AXI bus interface. Note that word swap is only available on data transfer when bit 0 (START) in the ATAPI control register (ATAPI_CONTROL1) = 1: DMA mode start.
0	—	—	R	Reserved The write value should always be 0.

**50.2.9 ATAPI Signal Status Register (ATAPI\_SIG\_ST)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DPIOR DY	DMAR Q
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 2	—	—	R	Reserved The write value should always be 0.
1	DPIORDY	—	R	DPIORDY indicates the state of the IF signal for PIO transfer in the SATA_IP block.
0	DMARQ	—	R	DMARQ indicates ATAPIDMARQ (IDEDREQ) signal state.

**Note:** Since the SATA interface has separate PIO and DMA interfaces, the DDMARDY signal of conventional ATAPI cannot be monitored.  
 The IORDY signal is not emulated. DPIORDY monitors the PIO-transfer interface signal only. Monitoring of the DMA-transfer interface signals is not possible.  
 The DPIORDY bit actually monitors the HREADY signal, i.e. the AHB for the internal PIO bus.

**50.2.10 Byte Swap Register (ATAPI\_BYTE\_SWAP)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	BYTE SWAP
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	—	R	Reserved The write value should always be 0.
0	BYTESWAP	0	R/W	BYTESWAP controls the swapping of the upper 8-bit data and the lower 8-bit data in the SATA interface. 0: Byte swap is not executed between the SATA interface and the AXI bus. 1: Byte swap is executed between the SATA interface and the AXI bus. Note that byte swap is only available on data transfer when START in the ATAPI control register (ATAPI_CONTROL1) = 1: DMA mode start.

**50.2.11 BIST Config Register (BISTCONF)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

The BISTCONF register is used to configure the operation to be performed in BIST mode.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	LOOPB
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

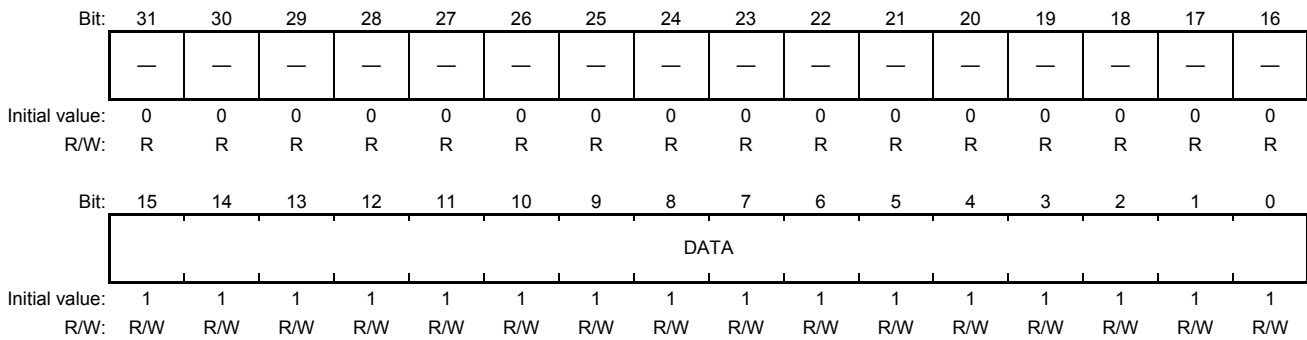
Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	LOOPB	0	R/W	Loopback mode bit (Loopback Mode) 0: Loopback (for far-end retimed loopback mode) is not formed in the link layer of the host. 1: Loopback (for far-end retimed loopback mode) is formed in the link layer of the host.

- Notes:
1. No read access can be made to this register and no correct data can be read from this register until the PHYRDY state is established. (See section 50.2.1, Note on the Access to the Registers Allocated to H'1018 to H'10A8.)
  2. BIST mode is not operational unless the SATA interface is in PHYRDY state.

**50.2.12 Shadow Data Register (DATA) (SDATA)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

The Shadow Data Register corresponds to the ATA standard's Data Register/Port. This is a data register that is read and written in PIO transfer mode.



Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 0	DATA	All 1	R/W	Transmit/receive data (SHADOW_DATA)

- Notes:
1. Refer to the ATA/ATAPI-7 and Serial-ATA specification for further information about this register.
  2. In PIO transfer mode, that is, except when the host\_shdw\_stat\_DRQ signal is being asserted, both of R/W operations are canceled, and therefore the initial value H'FFFF is not read out but H'0000 is read out. When a read attempt is made after the PIO mode read transfer, the last read value is read out.
  3. Access to the data register is prohibited while DMA is active. The SDATA register is accessible.

**50.2.13 Shadow Error Register (SERR[Read Mode]) (SSERR[Read Mode])**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

The shadow error register corresponds to the ATA standard's error register. (The actual register is on the device side; the host side value is handled as a mirror value.)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R		
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
	—	—	—	—	—	—	—	—	SERR								—	—
Initial value:	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1		
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R		

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved These bits are always read as 0.
7 to 0	SERR	All 1	R	Error monitor bit (SHADOW_ERROR) The bit definitions except that for bit 2 vary with the commands. Bit 2: ABRT bit. Set to 1 when the command that is issued is Abort.

- Notes:
1. Refer to the ATA/ATAPI-7 and Serial-ATA specification for further information about this register. Note that a write to the address of this register essentially causes the shadow features register (SFEATURES[Write Mode]) (SSFEATURES[Write Mode]) to be accessed.
  2. The initial value of this register cannot be read out since the value of this register is normally rewritten by the device immediately after the interface gets ready for communication following a power-on reset. See section 50.4.3, Signature of the Shadow Register (INFORMATIVE).
  3. Access to the SERR register is prohibited while DMA is active. The SSERR register is accessible.

**50.2.14 Shadow Features Register (SFEATURES[Write Mode]) (SSFEATURES[Write Mode])**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

The shadow features register corresponds to the ATA standard's features register. (\* The real entity of the register lies on the device side; the host side value is handled as a mirror value.)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R		
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
	—	—	—	—	—	—	—	—	SFEATURES								—	—
Initial value:	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1		
R/W:	R	R	R	R	R	R	R	R	W	W	W	W	W	W	W	W		

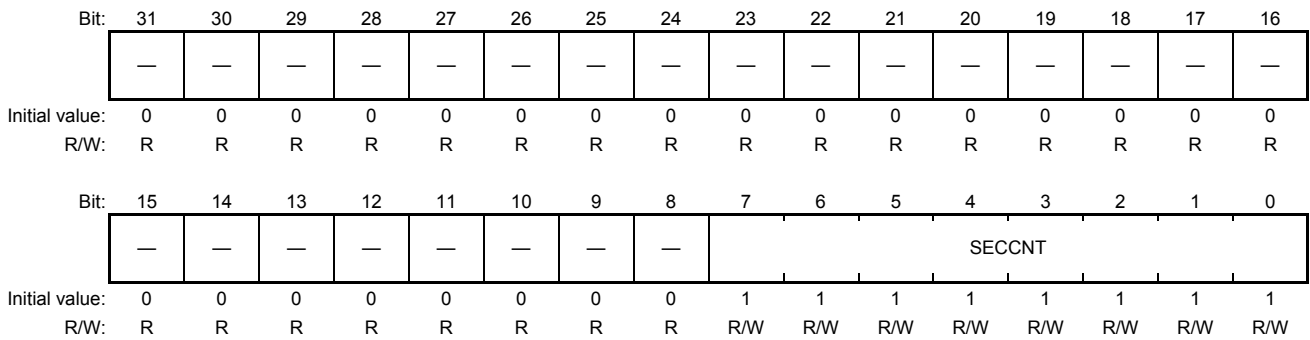
Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved The write value should always be 0.
7 to 0	SFEATURES	All 1	W	Subcommand setup bits (SHADOW_FEATURES) The bit definitions vary with the commands.

- Notes:
1. Refer to the ATA/ATAPI-7 and Serial-ATA specification for further information about this register. Note that a read from the address of this register essentially causes the shadow error register (SERR[Read Mode]) (SSERR[Read Mode]) to be accessed.
  2. This register functions in a 2-stage FIFO configuration when a device that is compatible with the 48-bit Address features set is connected. For details, see section 50.4.2, Extended ATA Registers.
  3. Access to the SFEATURES register is prohibited while DMA is active. The SSFEATURES register is accessible.

**50.2.15 Shadow Sector CNT Register (SECCNT) (SSECCNT)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

The shadow sector CNT register corresponds to the ATA standard's sector count register.  
 (\* The real entity of the register lies on the device side; the host side value is handled as a mirror value.)



Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7 to 0	SECCNT	All 1	R/W	Sector count bits (SHADOW_SECTOR_CNT) The bit definitions vary with the commands.

- Notes:
1. Refer to the ATA/ATAPI-7 and Serial-ATA specification for further information about this register.
  2. The initial value of this register cannot be read out since the value of this register is normally rewritten by the device immediately after the interface gets ready for communication following a power-on reset. See section 50.4.3, Signature of the Shadow Register (INFORMATIVE).
  3. This register functions in a 2-stage FIFO configuration when a device that is compatible with the 48-bit Address features set is connected. For details, see section 50.4.2, Extended ATA Registers.
  4. Access to the SECCNT register is prohibited while DMA is active. The SSECCNT register is accessible.



### 50.2.16 Shadow LBA Low Register (LBALOW) (SLBALOW)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

The shadow LBA low register corresponds to the ATA standard's LBA low (sector number) register.  
 (\* The real entity of the register lies on the device side; the host side value is handled as a mirror value.)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	LBALOW							
Initial value:	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

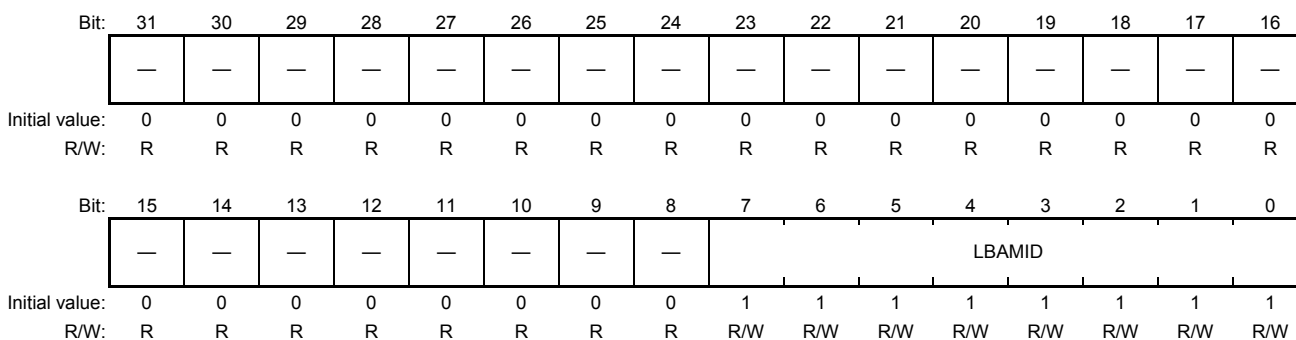
Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7 to 0	LBALOW	All 1	R/W	LBA_low address bits (SHADOW_LBA_LOW) The bit definitions vary with the commands.

- Notes:
1. Refer to the ATA/ATAPI-7 and Serial-ATA specification for further information about this register.
  2. The initial value of this register cannot be read out since the value of this register is normally rewritten by the device immediately after the interface gets ready for communication following a power-on reset. See section 50.4.3, Signature of the Shadow Register (INFORMATIVE).
  3. This register functions in a 2-stage FIFO configuration when a device that is compatible with the 48-bit Address features set is connected. For details, see section 50.4.2, Extended ATA Registers.
  4. Access to the LBALOW register is prohibited while DMA is active. The SLBALOW register is accessible.

### 50.2.17 Shadow LBA Mid Register (LBAMID) (SLBAMID)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

The shadow LBA mid register corresponds to the ATA standard's LBA mid (cylinder low) register. (\* The real entity of the register lies on the device side; the host side value is handled as a mirror value.)



Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7 to 0	LBAMID	All 1	R/W	LBA_MID address bits (SHADOW_LBA_MID) The bit definitions vary with the commands.

- Notes:
1. Refer to the ATA/ATAPI-7 and Serial-ATA specification for further information about this register.
  2. The initial value of this register cannot be read out since the value of this register is normally rewritten by the device immediately after the interface gets ready for communication following a power-on reset. See section 50.4.3, Signature of the Shadow Register (INFORMATIVE).
  3. This register functions in a 2-stage FIFO configuration when a device that is compatible with the 48-bit Address features set is connected. For details, see section 50.4.2, Extended ATA Registers.
  4. Access to the LBAMID register is prohibited while DMA is active. The SLBAMID register is accessible.

**50.2.18 Shadow LBA High Register (LBAHIGH) (SLBAHIGH)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

The shadow LBA high register corresponds to the ATA standard's LBA high (cylinder high) register. (\* The real entity of the register lies on the device side; the host side value is handled as a mirror value.)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R		
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
	—	—	—	—	—	—	—	—	LBAHIGH								—	—
Initial value:	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1		
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7 to 0	LBAHIGH	All 1	R/W	LBA_high address bits (SHADOW_LBA_HIGH) The bit definitions vary with the commands.

- Notes:
1. Refer to the ATA/ATAPI-7 and Serial-ATA specification for further information about this register.
  2. The initial value of this register cannot be read out since the value of this register is normally rewritten by the device immediately after the interface gets ready for communication following a power-on reset. See section 50.4.3, Signature of the Shadow Register (INFORMATIVE).
  3. This register functions in a 2-stage FIFO configuration when a device that is compatible with the 48-bit Address features set is connected. For details, see section 50.4.2, Extended ATA Registers.
  4. Access to the LBAHIGH register is prohibited while DMA is active. The SLBAHIGH register is accessible.

**50.2.19 Shadow Device/Head Register (DEVHEAD) (SDEVHEAD)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

The shadow device/head register corresponds to the ATA standard's device/head register.  
 (\* The real entity of the register lies on the device side; the host side value is handled as a mirror value.)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	DEVHEAD							
Initial value:	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7 to 0	DEVHEAD	All 1	R/W	Device function select bits (SHADOW_DEVHEAD) The bit definitions except those for bits 7, 5, and 4 vary with the commands. Bits 7 and 5: Obsolete Bit 4: DEV bit. Selects either the Master or Slave. This bit must always be set to 0.

- Notes:
1. Refer to the ATA/ATAPI-7 and Serial-ATA specification for further information about this register.
  2. The initial value of this register cannot be read out since the value of this register is normally rewritten by the device immediately after the interface gets ready for communication following a power-on reset. See section 50.4.3, Signature of the Shadow Register (INFORMATIVE).
  3. Access to the DEVHEAD register is prohibited while DMA is active. The SDEVHEAD register is accessible.

### 50.2.20 Shadow Status Register (SSTATUS[Read Mode]) (SSSTATUS[Read Mode])

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

The SSTATUS or SSSTATUS register corresponds to the ATA standard's status register. Its value can be read out correctly only when the DEV bit (bit 4) of the shadow device/head register (DEVHEAD) (SDEVHEAD) is set to 0. Its read value is always H'0000\_0000 when the DEV bit is set to 1.

Accessing this register for read causes the ATA-sourced host\_intrq interrupt signal to be negated. (\* The real entity of the register lies on the device side; the host side value is handled as a mirror value.)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	BSY	DRDY	DFSE	SSTATUS	DRQ	—	—	ERR
Initial value:	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved These bits are always read as 0.
7	BSY	0	R	BSY bit
6	DRDY	1	R	DRDY bit
5	DFSE	1	R	DF/SE bit
4	SSTATUS	1	R	Definition varies with the command.
3	DRQ	1	R	DRQ bit
2, 1	—	11	R	Reserved This bit is always read as 1.
0	ERR	1	R	ERR/CHK bit

- Notes:
1. Refer to the ATA/ATAPI-7 and Serial-ATA specification for further information about this register. Note that a write to the address of this register essentially causes the shadow command register (SCOM[Write Mode]) (SSCOM[Write Mode]) to be accessed.
  2. The initial value of this register cannot be read out since the value of this register is normally rewritten by the device immediately after the interface gets ready for communication following a power-on reset. See section 50.4.3, Signature of the Shadow Register (INFORMATIVE).
  3. Access to the SSTATUS register is prohibited while DMA is active. The SSSTATUS register is accessible.

**50.2.21 Shadow Command Register (SCOM[Write Mode]) (SSCOM[Write Mode])**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

The shadow command register corresponds to the ATA standard's command register. The ATA command code is set by this register.

Accessing this register for write causes the command to be issued to the device (sending command register FIS). (\* The real entity of the register lies on the device side; the host side value is handled as a mirror value.)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R		
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
	—	—	—	—	—	—	—	—	SCOM								—	—
Initial value:	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1		
R/W:	R	R	R	R	R	R	R	R	W	W	W	W	W	W	W	W		

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved The write value should always be 0.
7 to 0	SCOM	All 1	W	Transmit command setup bits (SHADOW_COMMAND)

- Notes:
1. Refer to the ATA/ATAPI-7 and Serial-ATA specification for further information about this register. Note that a read from the address of this register essentially causes the shadow status register (SSTATUS[Read Mode]) (SSSTATUS[Read Mode]) to be accessed.
  2. Access to the SCOM register is prohibited while DMA is active. The SSCOM register is accessible.

### 50.2.22 Shadow Alternates Status Register (SALTSTS[Read Mode]) (SSALTSTS[Read Mode])

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

The SALTSTS or SSALTSTS register is the ATA standard's alternate status register. Its value can be read out correctly only when the DEV bit (bit 4) of the shadow device/head register (DEVHEAD) (SDEVHEAD) is set to 0. Its read value is always H'0000\_0000 when the DEV bit is set to 1.

The bits of this register always have the same bit value as the corresponding bits of the shadow status register. Any attempt to access this register for read, however, does not cause the ATA-sourced host\_intrq interrupt signal to be negated.

(\* The real entity of the register lies on the device side; the host side value is handled as a mirror value.)

control register (SDEVCON[Write Mode])

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	ABSY	ADRDY	ADFSE	SALTSTS	ADRQ	—	—	AERR
Initial value:	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved These bits are always read as 0.
7	ABSY	0	R	BSY bit
6	ADRDY	1	R	DRDY bit
5	ADFSE	1	R	DF/SE bit
4	SALTSTS	1	R	Definition varies with the command.
3	ADRQ	1	R	DRQ bit
2, 1	—	11	R	Reserved These bits are always read as 1.
0	AERR	1	R	ERR/CHK bit

- Notes:
1. Refer to the ATA/ATAPI-7 and Serial-ATA specification for further information about this register. Note that a write to the address of this register essentially causes the shadow device control register (SDEVCON[Write Mode]) (SSDEVCON[Write Mode]) to be accessed.
  2. The initial value of this register cannot be read out since the value of this register is normally rewritten by the device immediately after the interface gets ready for communication following a power-on reset. See section 50.4.3, Signature of the Shadow Register (INFORMATIVE).
  3. Access to the SALTSTS register is prohibited while DMA is active. The SSALTSTS register is accessible.

**50.2.23 Shadow Device Control Register (SDEVCON[Write Mode]) (SSDEVCON[Write Mode])**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

The shadow device control register is the ATA standard's device control register.

(\* The real entity of the register lies on the device side; the host side value is handled as a mirror value.)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	HOB	—	—	—	—	SRST	NIEN	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	W	R	R	R	R	W	W	R

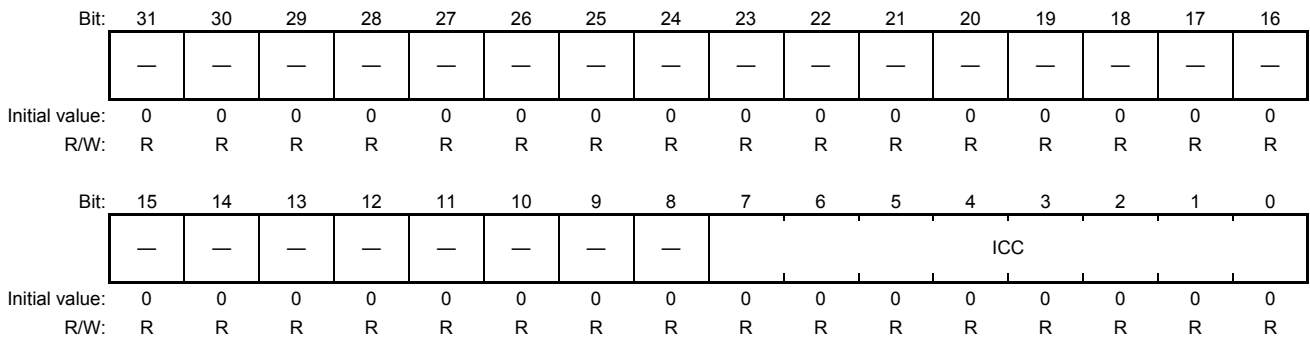
Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved The write value should always be 0.
7	HOB	0	W	HOB bit
6 to 3	—	All 0	R	Reserved The write value should always be 0.
2	SRST	0	W	SRST bit
1	NIEN	0	W	nIEN bit
0	—	0	R	Reserved The write value should always be 0.

- Notes: 1. Refer to the ATA/ATAPI-7 and Serial-ATA specification for further information about this register. Note that a read from the address of this register essentially causes the shadow alternates status register (SALTSTS[Read Mode]) (SSALTSTS[Read Mode]) to be accessed.
2. Access to the SDEVCON register is prohibited while DMA is active. The SSDEVCON register is accessible.



**50.2.24 SATA Extend ICC Register**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

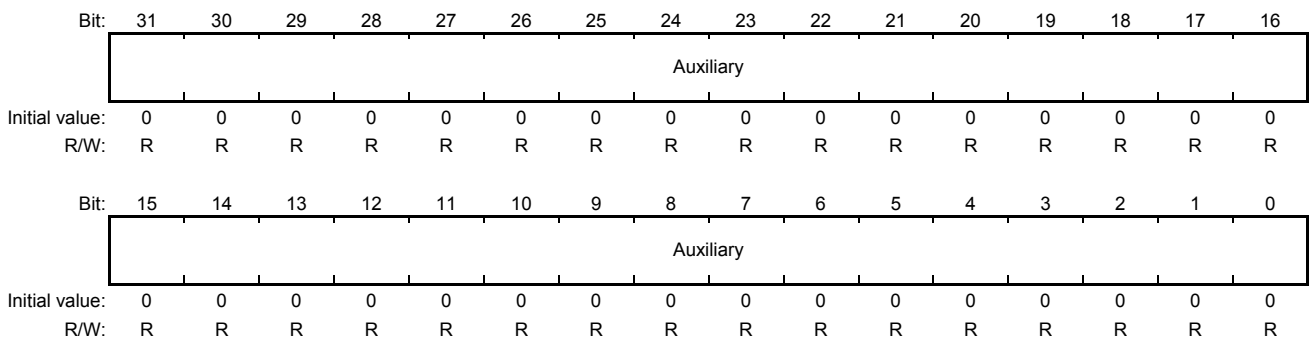


Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved The write value should always be 0.
7 to 0	ICC	All 0	R	ICC stands for Isochronous Command Completion

Note: Refer to the Serial-ATA specification for further information about this register.

**50.2.25 SATA Extend Auxiliary Register**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	Auxiliary	All 0	R	Auxiliary Contains parameter values specified on per command basis

Note: Refer to the Serial-ATA specification for further information about this register.

### 50.2.26 SCR SStatus Register (SCRSSTS)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	IPM			SPD				DET				
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 12	—	All 0	R	Reserved These bits are always read as 0.
11 to 8	IPM	0000	R	Interface power manager state monitor bits These bits indicate the interface's Power Management mode or state. 0000: No device is connected or the device is not ready for communication. 0001: Active mode 0010: Partial mode 0110: Slumber mode Other: Setting prohibited. After a transition to the slumber mode from the partial mode by automatic partial to slumber, IPM is set to B'0110 to indicate the slumber mode.
7 to 4	SPD	0000	R	Communication speed monitor bits These bits indicate the speed at which the interface communicates with the device. 0000: No device is connected or the device is not ready for communication. 0001: First generation (1.5 Gbps) 0010: Second generation (3.0 Gbps) Other: Setting prohibited.
3 to 0	DET	0000	R	Device communication state monitor bits These bits indicate the PHY state with respect to device detection. 0000: No device is detected or the device is not ready for communication. 0001: A device is detected but the device is not ready for communication. 0011: A device is detected and the device is ready for communication. 0100: Offline mode or loopback mode Other: Setting prohibited.

Note: Refer to the Serial-ATA specification for further information about this register.

### 50.2.27 SCR SError Register (SCRSERR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	DIAGA	DIAGX	DIAGF	DIAGT	DIAGS	DIAGH	DIAGC	DIAGD	DIAGB	DIAGW	DIAGI	DIAGN
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	ERRE	ERRP	ERRC	ERRT	—	—	—	—	—	—	ERRM	ERRI
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/WC1	R/WC1	R/WC1	R/WC1	R	R	R	R	R	R	R/WC1	R/WC1

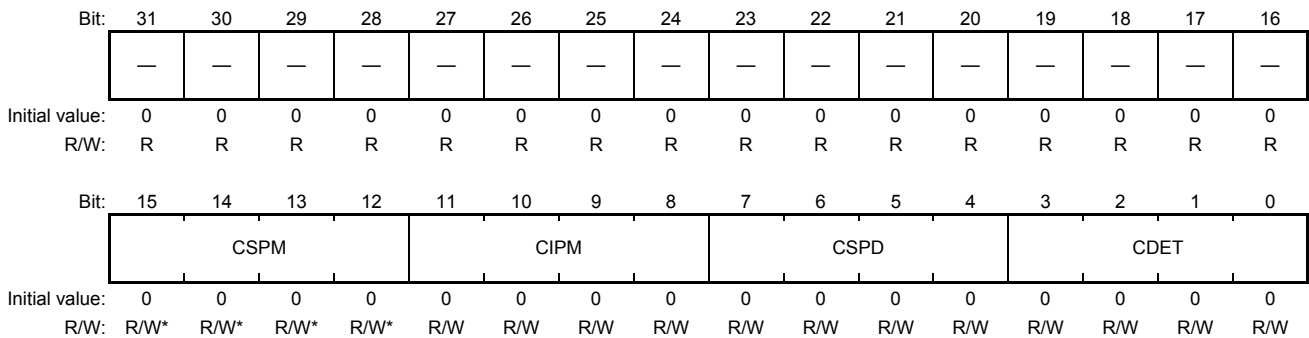
Bit	Bit Name	Initial Value	R/W	Description
31 to 28	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
27	DIAGA	0	R/WC1	DIAGA is used to sense COMWAKE before detecting a device. Port Selector Presence Detect (set when COMWAKE is detected before the Phy layer detects a device)
26	DIAGX	0	R/WC1	DIAGX is used to sense the change in device connection state. Exchanged (Set when the Phy layer detects a device connection or disconnection)
25	DIAGF	0	R/WC1	FIS type error bit Unrecognized FIS Type
24	DIAGT	0	R/WC1	Abnormal timing transfer result reception bit Transport state transition error (Set when transfer result notification is received at an invalid timing)
23	DIAGS	0	R/WC1	Abnormal state transition bit Link Sequence Error (Set when an illegal state transition occurs in the Link layer)
22	DIAGH	0	R/WC1	Handshake error bit
21	DIAGC	0	R/WC1	CRC error bit
20	DIAGD	0	R/WC1	Disparity error bit
19	DIAGB	0	R/WC1	10b/8b decode error bit
18	DIAGW	0	R/WC1	COMWAKE detect bit COMWAKE Detect (Set when COMWAKE is detected at any timing)
17	DIAGI	0	R/WC1	Error state bit Phy Internal Error (Set when an error occurs in the Phy layer)
16	DIAGN	0	R/WC1	Transfer Ready state change bit PHYRDY change (Set when the PhyRdy signal indicating the Phy layer's transfer ready state is toggled)
15 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
11	ERRE	0	R/WC1	Internal FIFO flow error bit Internal Error (Set when a flow error occurs in the internal FIFO. Perform a software reset whenever this bit is set.)
10	ERRP	0	R/WC1	Protocol error bit Protocol Error (Set when either one of the following conditions occurs): An illegal state transition occurs in the Link layer (same as the DIAGS bit) An unsupported FIS is received (same as the DIAGF bit). The size of the received FIS is found invalid. A transfer result notification is received at an invalid timing (same as the DIAGT bit).
9	ERRC	0	R/WC1	FIS transmission PhyRdy signal negated bit Non-recovered persistent communication or data integrity error (Set when the PhyRdy signal is negated during transmission of a FIS except Data FIS (including retries))
8	ERRT	0	R/WC1	Data FIS transfer error bit Non-recovered transient data integrity error (Set when an error occurs during Data FIS transfer. Be sure to check this bit during PIO reads.)
7 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	ERRM	0	R/WC1	Communication error recovery monitor bit Recovered communications error (The PhyRdy signal indicating the Phy layer's transfer ready state is negated but asserted again within approximately 200 $\mu$ s.)
0	ERRI	0	R/WC1	Retransmission result bit Recovered data integrity error (Set when retransmission of an FIS is successful)

- Notes:
1. Refer to the Serial-ATA specification for further information about this register.
  2. There are cases in which the DIAGW and DIAGN bits of this register are already set before a first access is made since the initial data is automatically set in the register when it is provided with a clock signal after a power-on reset. Consequently, it is recommended that all bits of this register be cleared (writing H'FFFF\_FFFF) at the beginning of the startup sequence.
  3. The operation of this register is irrelevant to the settings of the SATA INT status register (SATAINTSTAT) and SATA INT mask register (SATAINTMASK). The way in which the SCR SError register behaves remain unchanged even when bits b1, b2, and b3 of the SATA INT mask register are set (that is, interrupt sources are masked as the result of the update of the SCR SError result).

**50.2.28 SCR SControl Register (SCRSCON)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—



Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 12	CSPM	0000	R/W*	Power Management Mode transition request bits (SPM) CSPM is a set of bits that request for the state of the Power Management mode. Set as follows to have Power Management to transit to the required state: 0000: No request 0001: Request transition to the Partial Mode. 0010: Request transition to the Slumber Mode. 0100: Request to restoration to the Active Mode. Other: Setting prohibited. (* The transition request to the Partial/Slumber Mode is not retried. When using this field, unmask the SLUMMSK and PARTIMSK bits (bits 6 and 5) of the SATA INT mask register (SATAINTMASK) and enable "device rejects transition to Slumber Mode" and "device rejects transition to Partial Mode" interrupts.)
11 to 8	CIPM	0000	R/W	Interface Power Management Mode enable bit (IPM) CIPM enables or disables the interface's Power Management mode. 0000: No limitation. 0001: Partial Mode Disable 0010: Slumber Mode Disable 0011: Partial/Slumber Mode Disable Other: Setting prohibited.
7 to 4	CSPD	0000	R/W	Communication speed bits (SPD) The CSPD bits define the limiting speed at which communication with the device is to be made. 0000: No limitation (same as B'0010) 0001: First generation (1.5 Gbps) 0010: Second generation (3.0Gbps) or less Other: Setting prohibited. (This field is not initialized by a hardware reset. It is initialized at power-on reset time.)

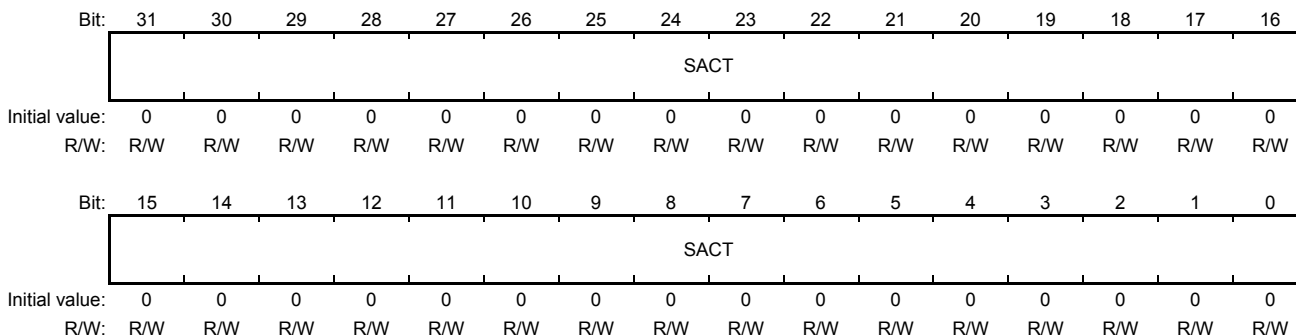
Bit	Bit Name	Initial Value	R/W	Description
3 to 0	CDET	0000	R/W	RESET/Offline mode bits (DET) The CDET bits specify the RESET/Offline mode. 0000: No request 0001: RESET. Handled as a hardware reset. 0100: Places the PHY in offline mode. Other: Setting prohibited. (The SCR SControl register is initialized after the switching of the CDET field value from B'0001 to B'0000 is detected. Consequently, the values of the CSPM, CIPM, and CSPD fields are invalid when a write access such that the CDET field is set to B'0000 is made to this register.)

- Notes:
1. Refer to the Serial-ATA specification for further information about this register.
  2. It is impossible to check the value of this field since the field is reset to B'0000 as soon as setting of the value is internally detected.

**50.2.29 SCR SActive Register (SCRSACT)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

The SCR SActive register is used to set up the TAG value to be used for Native Command Queuing.



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	SACT	All 0	R/W	b31: Corresponds to a TAG value of B'11111. b30: Corresponds to a TAG value of B'11110. b29: Corresponds to a TAG value of B'11101. b28: Corresponds to a TAG value of B'11100. b27: Corresponds to a TAG value of B'11011. b26: Corresponds to a TAG value of B'11010. b25: Corresponds to a TAG value of B'11001. b24: Corresponds to a TAG value of B'11000. b23: Corresponds to a TAG value of B'10111. b22: Corresponds to a TAG value of B'10110. b21: Corresponds to a TAG value of B'10101. b20: Corresponds to a TAG value of B'10100. b19: Corresponds to a TAG value of B'10011. b18: Corresponds to a TAG value of B'10010. b17: Corresponds to a TAG value of B'10001. b16: Corresponds to a TAG value of B'10000. b15: Corresponds to a TAG value of B'01111. b14: Corresponds to a TAG value of B'01110. b13: Corresponds to a TAG value of B'01101. b12: Corresponds to a TAG value of B'01100. b11: Corresponds to a TAG value of B'01011. b10: Corresponds to a TAG value of B'01010. b9: Corresponds to a TAG value of B'01001. b8: Corresponds to a TAG value of B'01000. b7: Corresponds to a TAG value of B'00111. b6: Corresponds to a TAG value of B'00110. b5: Corresponds to a TAG value of B'00101. b4: Corresponds to a TAG value of B'00100. b3: Corresponds to a TAG value of B'00011. b2: Corresponds to a TAG value of B'00010. b1: Corresponds to a TAG value of B'00001. b0: Corresponds to a TAG value of B'00000.

- Notes:
1. Refer to the Serial-ATA specification for further information about this register.
  2. This register is write-only. To reset this register, it is necessary to reset the device (Software Reset will do).

### 50.2.30 SATA INT Status Register (SATAINTSTAT)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

Bits 31 to 24 of the SATA INT status register are Shadow Status bits and mirror the value of the shadow status register. As with the shadow status register, accessing this register for read causes the ATA-sourced host\_int\_ata\_intrq interrupt signal to be negated. (\* The real entity of the register lies on the device side; the host side value is handled as a mirror value.)

Bits 11 to 0 of this register identify the interrupt source of the host\_intrq signal. The bits that are masked by the SATA INT mask register (SATAINTMASK) do not cause the host\_intrq signal to be asserted when the corresponding interrupt source event occurs. In this case, the pertinent bit is not set either.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	INT BSY	INT DRDY	INT DFSE	INTSST ATUS	INT DRQ	—	—	INT ERR	—	—	—	—	—	—	—	—
Initial value:	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	SDBF	SLUMR	PARTI R	VEND	BIST	SLUM	PARTI	DMAST	SERR	ERR	ERR CRT	ATA
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	RC	RC	RC	RC	RC	RC	RC	RC	RC	RC	RC	RC

Bit	Bit Name	Initial Value	R/W	Description
31	INTBSY	0	R	BSY bit
30	INTDRDY	1	R	DRDY bit
29	INTDFSE	1	R	DF/SE bit
28	INTSSTATUS	1	R	Definition varies with the command.
27	INTDRQ	1	R	DRQ bit.
26, 25	—	11	R	Reserved These bits are always read as 1.
24	INTERR	1	R	ERR/CHK bit
23 to 12	—	All 0	R	Reserved These bits are always read as 0.
11	SDBF	0	RC	Set Device Bits FIS reception Refer to notes 3 and 4.
10	SLUMR	0	RC	A request for transition to the Slumber state has been received (for device-initiated power management, i.e. DIPM). Refer to notes 3 and 4
9	PARTIR	0	RC	A request for transition to the Partial state has been received (for device-initiated power management, i.e. DIPM). Refer to notes 3 and 4.
8	VEND	0	RC	Vendor Specific FIS reception Refer to notes 3 and 4.
7	BIST	0	RC	BIST Active FIS reception Refer to notes 3 and 4.



Bit	Bit Name	Initial Value	R/W	Description
6	SLUM	0	RC	Device rejects transition to Slumber Mode. Refer to notes 2, 3, and 4.
5	PARTI	0	RC	Device rejects transition to Partial Mode. Refer to notes 2, 3, and 4
4	DMAST	0	RC	Same meaning as DMA Setup FIS reception (fpdma_req signal asserted) Refer to notes 3 and 4.
3	SERR	0	RC	SCR SERROR register update Refer to notes 3 and 4.
2	ERR	0	RC	SCR SERROR register (SCRSERR) ERRE, ERRP, ERRC, ERRT, ERM, and ERRI bits update Refer to notes 3 and 4.
1	ERRCRT	0	RC	SCR SERROR register (SCRSERR) ERRE, ERRP, and ERRT bits update Refer to notes 1, 3, and 4.
0	ATA	0	RC	ATA source (equivalent to P-ATA's INTRQ) Refer to notes 3 and 4.

Notes: 1. When the "SCR SError register ERRE, ERRP, and ERRT bits update" interrupt bit is set, it indicates that the condition cannot be recovered by this host controller module. In such a case, take appropriate actions according to the operating state established before the error occurred and the value of the SCR SError register (SCRSERR).

Example:

- 1) When the ERRT bit of the SCR SError register (SCRSERR) is set on completion of a PIO Read (data-in) transfer:  
The read data contains an error bit. Restart processing at the issuance of the command.
  - 2) When the ERRE bit of the SCR SError register (SCRSERR) is set during DMA transfer:  
The data that is being transferred contains an error but since it cannot be detected by the device, it is necessary to perform a software reset and restart processing at the issuance of the command.
  - 3) When the ERRP bit of the SCR SError register (SCRSERR) is set:  
Perform a hardware reset and re-execute the preceding operation.
2. When a "device rejects transition to Slumber Mode" or "device rejects transition to Partial Mode" interrupt occurs, no request is reissued (retried) to the device. If requests should be made again, reset the SCR SControl register with a correct value.
  3. Table 50.5 lists the combinations of twelve interrupt source bits (bit 11 to bit 0) that are likely to be set at the same timing.

**Table 50.5 Interrupt Source Bits That are Likely to be Set at the Same Time**  
(√: Possible, —: Impossible)

	Bit11	Bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Bit11	—	—	—	—	—	—	—	—	√	√	√	—
bit10	—	—	—	—	—	—	—	—	√	√	√	—
bit9	—	—	—	—	—	—	—	—	√	√	√	—
bit8	—	—	—	—	—	—	—	—	√	√	√	—
bit7	—	—	—	—	—	—	—	—	√	√	√	—
bit6	—	—	—	—	—	—	—	—	√	√	√	—
bit5	—	—	—	—	—	—	—	—	√	√	√	—
bit4	√	—	—	—	—	—	—	—	√	√	√	—
bit3	√	√	√	√	√	√	√	√	√	√	√	√
bit2	√	√	√	√	√	√	√	√	√	√	√	√
bit1	—	√	√	√	√	√	√	√	√	√	√	√
bit0	—	—	—	—	—	—	—	—	√	√	√	√

4. Examples of operations that are performed when the SATA INT status register (SATAINTSTAT) interrupt sources are masked by the SATA INT mask register (SATAINTMASK)

Example 1): The SATA INT mask register (SATAINTMASK) is not set up for an interrupt source before the pertinent interrupt source occurs.

If BIST Activate FIS which is the interrupt source for bit7 is received when SATAINTMASK[11:0] = B'1111\_0111\_1111,

the results are:

SATAINTSTAT[11:0] = B'0000\_1000\_0000;

host\_intrq: High (asserted)

Example 2): The SATA INT mask register (SATAINTMASK) is set up for an interrupt source before the pertinent interrupt source occurs.

If Vendor Specific FIS which is the interrupt source for bit8 is received when

SATAINTMASK[11:0] = B'1111\_0111\_1111;

the results are:

SATAINTSTAT[11:0] = B'0000\_0000\_0000;

host\_intrq: Low (not asserted)

Example 3): Another interrupt source occurs after an interrupt occurs.

If BIST Activate FIS which is the interrupt source for bit7 is received when SATAINTMASK[11:0] = B'1111\_0111\_1110,

SATAINTSTAT[11:0] = B'0000\_0000\_0001, and host\_intrq: High (asserted),

the results are:

SATAINTSTAT[11:0] = B'0000\_1000\_0001;

host\_intrq: High (remains asserted)

Example 4): Another interrupt source (but the interrupt source is masked on) occurs after an interrupt occurs.

If Vendor Specific FIS which is the interrupt source for bit8 is received when

SATAINTMASK[11:0] = B'1111\_0111\_1110, SATAINTSTAT[11:0] = B'0000\_0000\_0001, and

host\_intrq: High (asserted),

the results are:

SATAINTSTAT[11:0] = B'0000\_0000\_0001;

host\_intrq: High (remains asserted)

### 50.2.31 SATA INT Mask Register (SATAINTMASK)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

The SATA INT mask register is used to mask the interrupt sources configured in the SATA INT status register (SATAINTSTAT). Interrupt sources corresponding to bits for which 1s have been specified are masked.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	SDBF MSK	SLUMR MSK	PARTIT MSK	VEND MSK	BIST MSK	SLUM MSK	PARTI MSK	DMAST MSK	SERR MSK	ERR MSK	ERR CRT MSK	ATA MSK
Initial value:	0	0	0	0	1	0	0	1	1	1	1	1	1	1	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11	SDBFMSK	1	R/W	Masks the "Set Device Bits FIS received" interrupt.
10	SLUMRMSK	0	R/W	Mask for the "request for transition to Slumber mode" interrupt (for DIPM).
9	PARTITMSK	0	R/W	Mask for the "request for transition to Partial mode" interrupt (for DIPM).
8	VENDMSK	1	R/W	Masks the "Vendor Specific FIS received" interrupt.
7	BISTMSK	1	R/W	Masks the "BIST Activate FIS received" interrupt.
6	SLUMMSK	1	R/W	Masks the "device reject transition to Slumber mode" interrupt.
5	PARTIMSK	1	R/W	Masks the "device reject transition to Partial mode" interrupt.
4	DMASTMSK	1	R/W	Masks the "DMA Setup FIS received" interrupt.
3	SERRMSK	1	R/W	Masks the "SCR SError register (SCRSERR) update" interrupt.
2	ERRMSK	1	R/W	Masks the "SCR SError register (SCRSERR) ERRE, ERRP, ERRC, ERRT, ERRM, and ERRI bits update" interrupt.
1	ERRCRTMSK	0	R/W	Masks the "SCR SError register (SCRSERR) ERRE, ERRP, and ERRT bits update" interrupt.
0	ATAMSK	0	R/W	Masks the "ATA source (equivalent to P-ATA's INTRQ)" interrupt. The NIEN bit of the shadow device control register (SDEVCON) provides the same effect.

**50.2.32 PHY STOP Register (PHYSTOP)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PHY STOP
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are read as 0. The write value should be 0.
0	PHY STOP	0	R/W	0: Normal 1: PHY STOP

Note: PHY STOP mode is used to stop the AFE. Apply a power-on reset to return the AFE from the PHY STOP mode (a software reset will not do this).

### 50.2.33 Rx DMA Setup FIS Dword0 Register (DMADW0)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

The Rx DMA setup FIS Dword0 Register contains the most recently received DMA Setup FIS information. It should be referenced when a DMA Setup FIS received interrupt occurs as indicated in the SATA INT status register (SATAINTSTAT).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	AUTO ACT	DMA INT	DMA DIR	—	PMPORT				FISTYPE							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

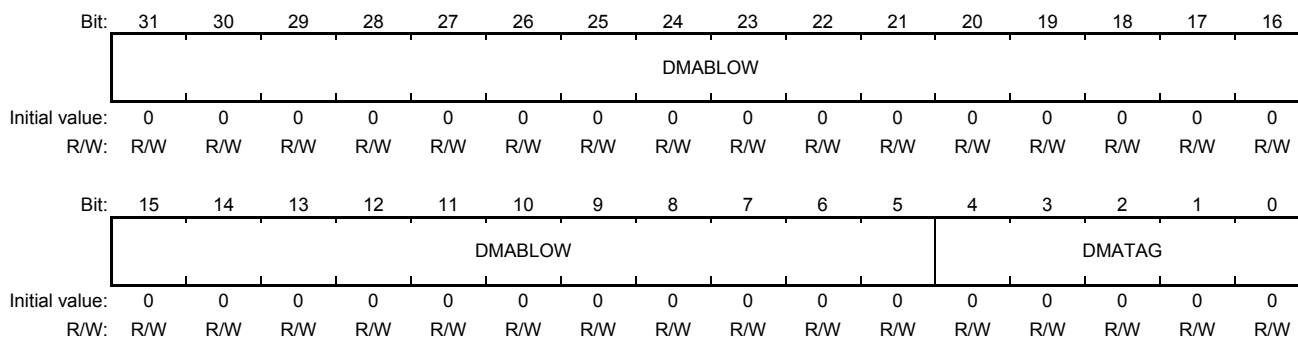
Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15	AUTOACT	0	R/W	Auto-Activation bit 1 indicates Auto-Activation.
14	DMAINT	0	R/W	Interrupt bit
13	DMADIR	0	R/W	Data transfer direction bit The direction of the next data transfer. 0: Host -> device 1: Device -> host
12	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
11 to 8	PMPORT	All 0	R/W	Source device ID Always set to B'0000 in NCQ mode.
7 to 0	FISTYPE	All 0	R/W	FIS type bits FISTYPE indicates the type of a received FIS. The value is "41" when a DMA setup FIS is received.

Note: Refer to the Serial-ATA specification for further information about this register.

### 50.2.34 Rx DMA Setup FIS Dword1 Register (DMADW1)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

The Rx DMA setup FIS Dword1 Register contains the most recently received DMA Setup FIS information. It should be referenced when a DMA Setup FIS received interrupt occurs as indicated in the SATA INT status register (SATAINTSTAT).



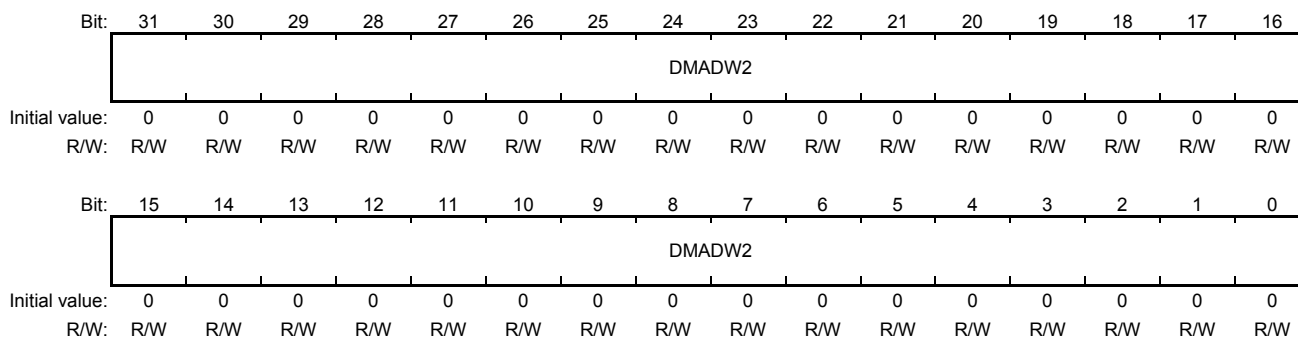
Bit	Bit Name	Initial Value	R/W	Description
31 to 5	DMABLOW	All 0	R/W	DMA Buffer Identifier Low field value in the DMA Setup FIS (set to H'0000_0000 in NCQ mode)
4 to 0	DMATAG	All 0	R/W	TAG field for NCQ

Note: Refer to the Serial-ATA specification for further information about this register.

### 50.2.35 Rx DMA Setup FIS Dword2 Register (DMADW2)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

The Rx DMA setup FIS Dword2 Register contains the most recently received DMA Setup FIS information. It should be referenced when a DMA Setup FIS received interrupt occurs as indicated in the SATA INT status register (SATAINTSTAT).



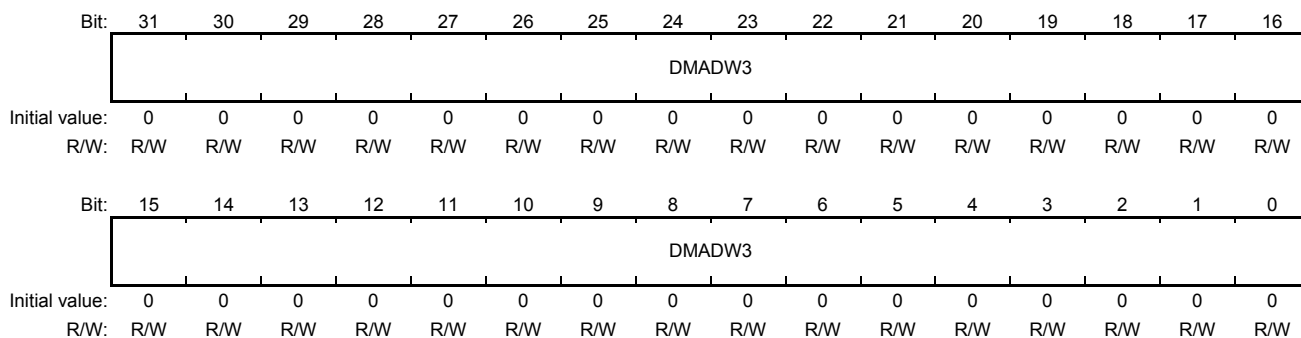
Bit	Bit Name	Initial Value	R/W	Description
31 to 0	DMADW2	All 0	R/W	DMA Buffer Identifier High field value (Set to H'0000_0000 in NCQ mode)

Note: Refer to the Serial-ATA specification for further information about this register.

### 50.2.36 Rx DMA Setup FIS Dword3 Register (DMADW3)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

The Rx DMA setup FIS Dword3 Register contains the most recently received DMA Setup FIS information. It should be referenced when a DMA Setup FIS received interrupt occurs as indicated in the SATA INT status register (SATAINTSTAT).



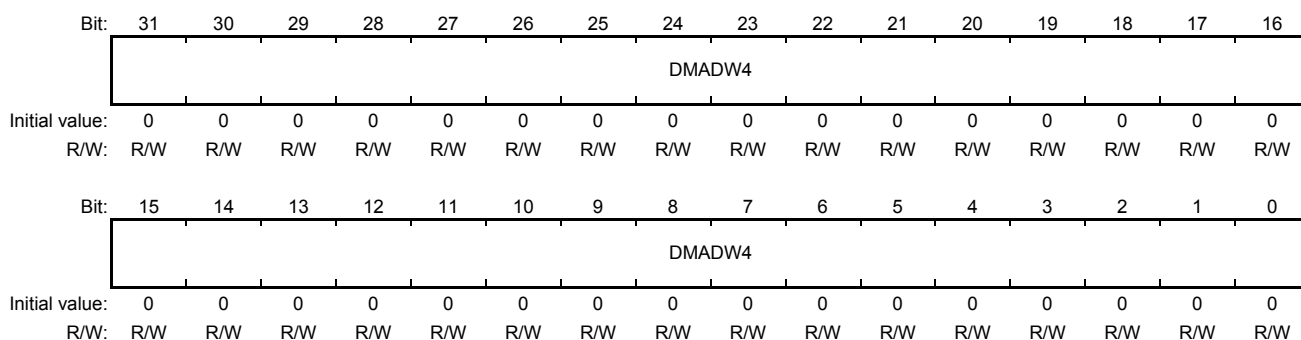
Bit	Bit Name	Initial Value	R/W	Description
31 to 0	DMADW3	All 0	R/W	Dword3 value in the DMA Setup FIS (Normally set to H'0000_0000 as DMADW3 is handled as Reserved)

Note: Refer to the Serial-ATA specification for further information about this register.

### 50.2.37 Rx DMA Setup FIS Dword4 Register (DMADW4)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

The Rx DMA setup FIS Dword4 Register contains the most recently received DMA Setup FIS information. It should be referenced when a DMA Setup FIS received interrupt occurs as indicated in the SATA INT status register (SATAINTSTAT).



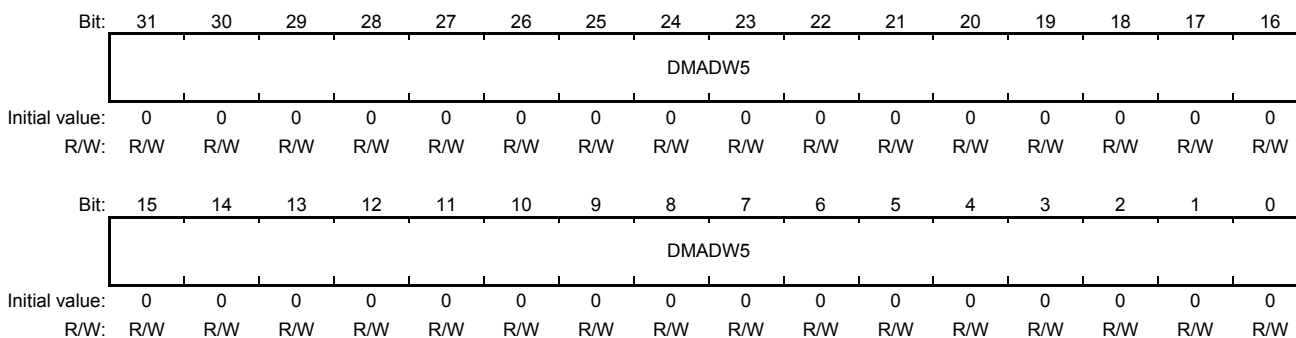
Bit	Bit Name	Initial Value	R/W	Description
31 to 0	DMADW4	All 0	R/W	DMA Buffer Offset value in the DMA Setup FIS

Note: Refer to the Serial-ATA specification for further information about this register.

### 50.2.38 Rx DMA Setup FIS Dword5 Register (DMADW5)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

The Rx DMA setup FIS Dword5 Register contains the most recently received DMA Setup FIS information. It should be referenced when a DMA Setup FIS received interrupt occurs as indicated in the SATA INT status register (SATAINTSTAT).



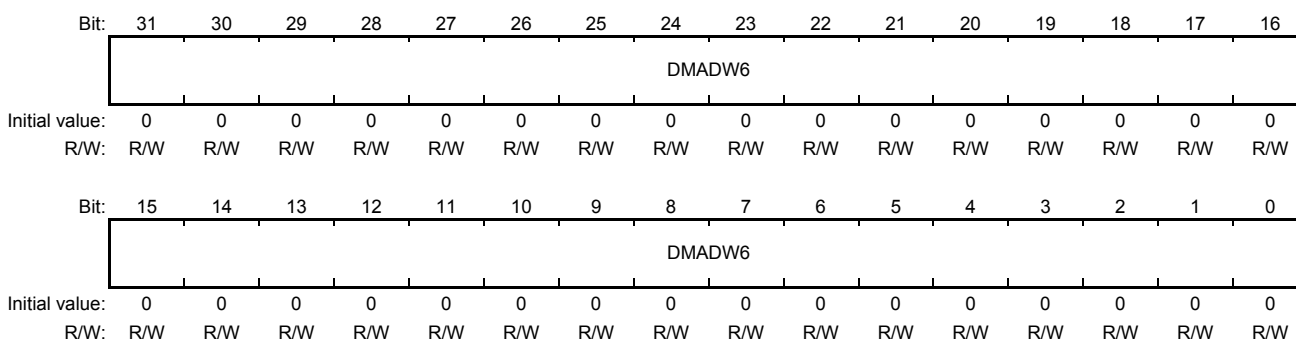
Bit	Bit Name	Initial Value	R/W	Description
31 to 0	DMADW5	All 0	R/W	DMA Transfer Count value in the DMA Setup FIS

Note: Refer to the Serial-ATA Specification for further information about this register.

### 50.2.39 Rx DMA Setup FIS Dword6 Register (DMADW6)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

The Rx DMA setup FIS Dword6 register contains the most recently received DMA Setup FIS information. It should be referenced when a DMA Setup FIS received interrupt occurs as indicated in the SATA INT status register (SATAINTSTAT).



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	DMADW6	All 0	R/W	Dword6 value in the DMA Setup FIS (Normally set to H'0000_0000 as DMADW6 is handled as Reserved)

Note: Refer to the Serial-ATA specification for further information about this register.



## 50.3 Operation

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

### 50.3.1 Power Management Mode

The SATA interface can be switched into Partial, Slumber, or Active mode by setting up the CSPM field of the SCR SControl register (SCRSCON) for the required mode.

Note: Whenever restoring the SATA interface from Partial or Slumber mode to Active mode, be sure to verify with the SCR SStatus register (SCRSSTS) that the SATA interface is in Partial or Slumber mode. Any request issued to the device to switch into Power Management Mode with this register setting is not retried when it is rejected. To reissue the request, it is necessary to set up the SCR SControl register (SCRSCON) again.

### 50.3.2 Initialization

To perform communication using this module, it is necessary to set up the bridge function and establish an SATA connection.

Follow the procedure shown below to initialize the SATA.

#### (1) Release the Module from Standby

After resetting, release the module from the standby state. Refer to section 7, Clock Pulse Generator (CPG), for details on module standby. The module enters the module standby state after release from the power-on reset state.

#### (2) Initializing the Physical Layer

Access the physical layer control register, and, please perform the nerdy initialization that assumes a physical layer an operation state.

For the method of accessing the physical layer control registers, see section 50.3.3, Access to the Physical Layer Control Registers.

#### (3) Establishing OOB and Speed Negotiation

Start OOB and speed negotiation at the resetting of the standby state.

### 50.3.3 Access to the Physical Layer Control Registers

Before using this module, set the parameter values to the address fields as shown in the table below to initialize the physical layer.

**Table 50.6 Access to the Physical Layer**

Address	Parameter	Access size
H'1704	SSCG OFF: H'3418_0002 SSCG ON: H'3418_C182	32
H'170C	H'0000_2303	32
H'171C	H'000B_0194	32
H'1724	H'0003_0994	32
H'1740	Reference clock setting is AC connection, termination resistor OFF: H'0300_4001	32
	Reference clock setting is DC connection, termination resistor OFF: H'0300_4003	
	Reference clock setting is AC connection, termination resistor ON: H'0300_4005	
	Reference clock setting is DC connection, termination resistor ON: H'0300_4007	

### 50.3.4 SH-Navi2G Compatibilities

The compatibility items of the SH-Navi2G/ATAPI (P-ATA host controller) include the internal bus related DMA transfer functions and PATA task register access functions.

### 50.3.5 SH-Navi2G Compatible Descriptor Function

SATA allows two or more non-overlapping contiguous memory spaces to be specified in the memory space for DMA data transfer. The DMA start address and DMA transfer count of the individual memory spaces must be specified in the descriptor table.

### 50.3.6 Interrupt Modes

The Link block supports two operating modes in addition to the ATA compliant registers.

This section describes the interrupt source masks and the specifications with respect to the clearing of the interrupt sources.

Figure 50.2 illustrates interrupt functions.

#### (1) IP Compatible Mode (Initial Value, when ISM = 0)

##### (a) Interrupt Source Mask

When an interrupt is masked, the corresponding interrupt flag is not set in the status register.

##### (b) Clearing Interrupt Sources

Interrupt sources are cleared by reading the SATA INT status register (SATAINTSTAT).

As with the shadow status register (SSTATUS), a read access causes the ATA-sourced (corresponding to INTRQ of P-ATA) host\_intrq interrupt signal to be negated.

The ATA-specified interrupt source, SCR SError register (SCRSERR), is cleared by writing 1.

**(2) CIS Interrupt Mode (when ISM = 1)**

**(a) Interrupt Source Mask**

Interrupts are masked but corresponding flags are still set in the status register.

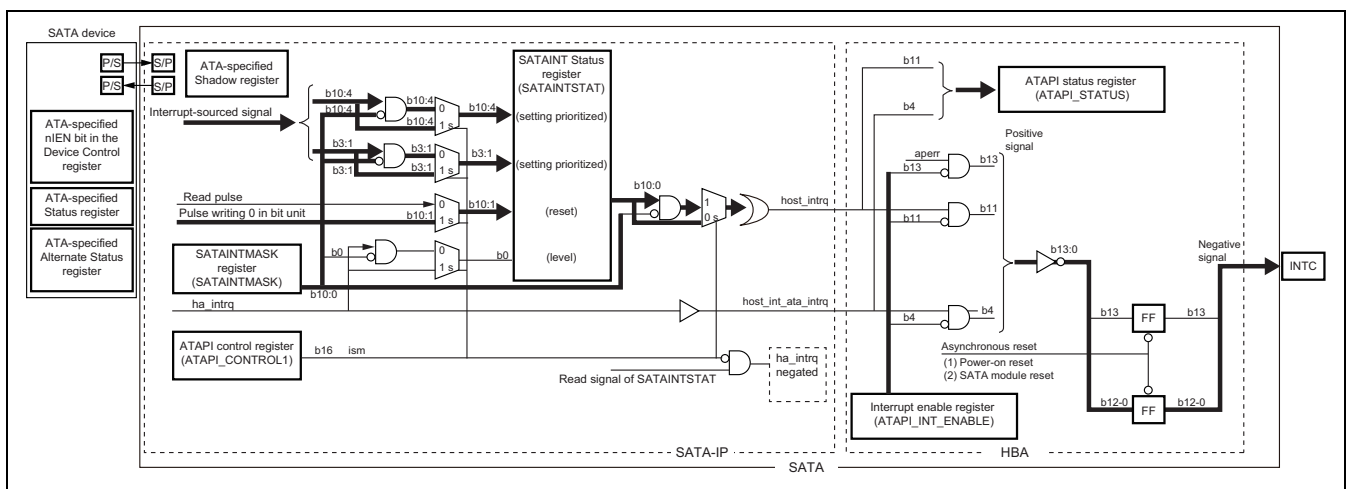
During negotiation, bit 3 in the Interrupt Status register is set. After negotiation ends, all bits in the Interrupt Status register must be cleared to 0.

**(b) Clearing Interrupt Sources**

Interrupt sources are cleared by writing 0.

A read access does not cause the ATA-sourced (corresponding to INTRQ of P-ATA) host\_intrq interrupt signal to be negated.

The ATA-specified interrupt source, SCR Error register (SCRERR), is cleared by writing 1; there is no change with this respect.



**Figure 50.2 Interrupt Functions**

### 50.3.7 Interrupt Processing Flow

The end of host device transfer interrupt and the ERR interrupt need to be considered.

The use of a timer in the wait processing is recommended to detect abnormal operations.

The device and host sources conflict. Figures 50.3 to 50.10 show the flow diagrams of interrupt processing.

The meanings of the words in the flow diagrams are given below.

CMD:	The CPU requests data transfer by writing to the SATA host and device registers.
Data ready:	Data for writing to (DATA-OUT) the SATA device by the CPU are prepared in memory.
DATA:	Data to be transferred (data to be transferred by DMA)
Data reference:	The CPU refers to data to be read from (DATA-IN) the SATA device in memory.
DMA request:	Request for DMA transfer from the SATA device
DEVINT, SERR, SATAINT:	Interrupt request originating in the device, such as the request corresponding to DEVINT (bit 4) in the ATAPI status register (ATAPI_STATUS)
NEND:	Interrupt request for the end of normal transfer of the SATA host, such as the requests corresponding to NEND (bit 1) in the ATAPI status register (ATAPI_STATUS)
response:	Response to completion of writing to memory of data read from the SATA device
'Order may be reversed.':	The order of the error interrupt or the interrupt at the end of normal transfer to or from the device may be reversed before or after the end of normal transfer.
End of normal transfer:	The time of generation of the interrupt request corresponding to NEND (bit 1) or DNEND (bit 6) in the ATAPI status register (ATAPI_STATUS) as the source

One of the two sets of events listed below will occur according to the response time of the device and the internal response time.

States (1) to (3) occur at the end of normal transfer of DATA-OUT:

- (1) Errors originating in the SATA device overlap.
- (2) Errors due to SATA communications and the host overlap.
- (3) The device's end interrupts will overlap if the device response is fast.

States (4) to (6) occur at the end of normal transfer of DATA-IN:

- (4) Errors originating in the SATA device overlap.
- (5) Errors due to SATA communications or the host overlap.
- (6) The device's end interrupts will overlap if the internal response is fast.

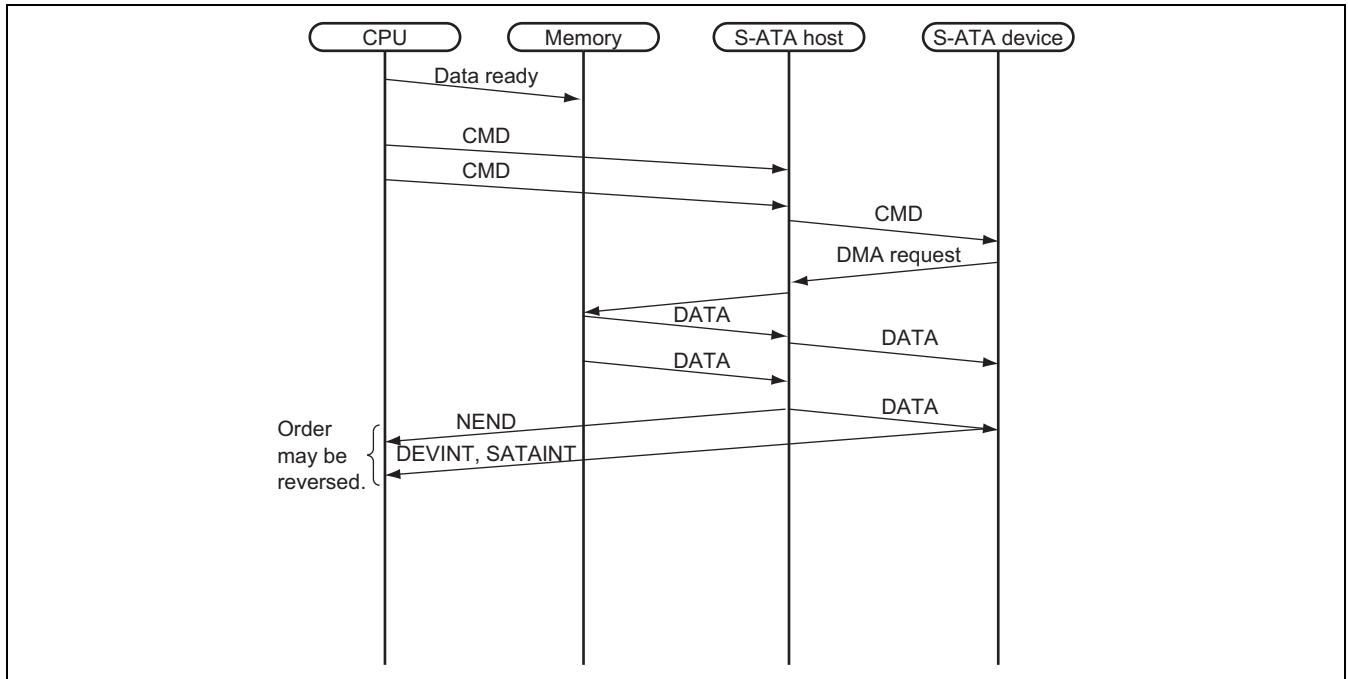


Figure 50.3 DATA-OUT (Normal Mode Interrupts)

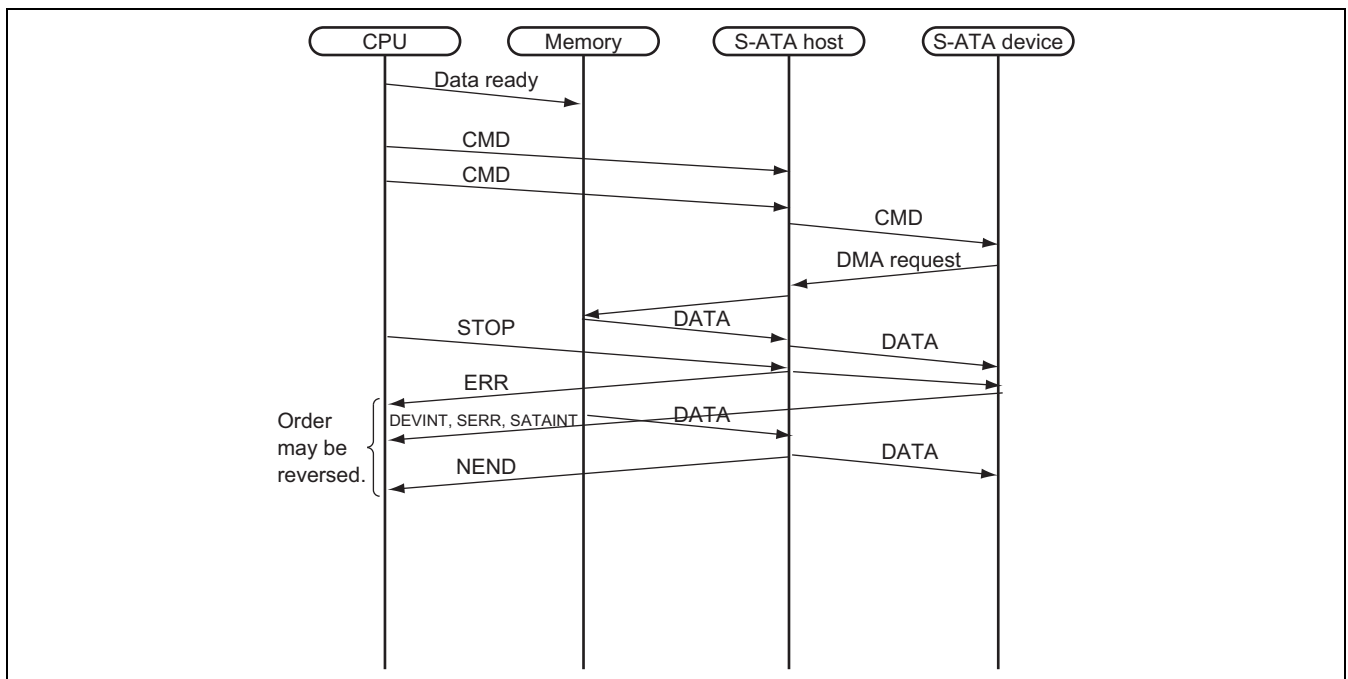


Figure 50.4 DATA-OUT (Internal Bus or CPU Sources)

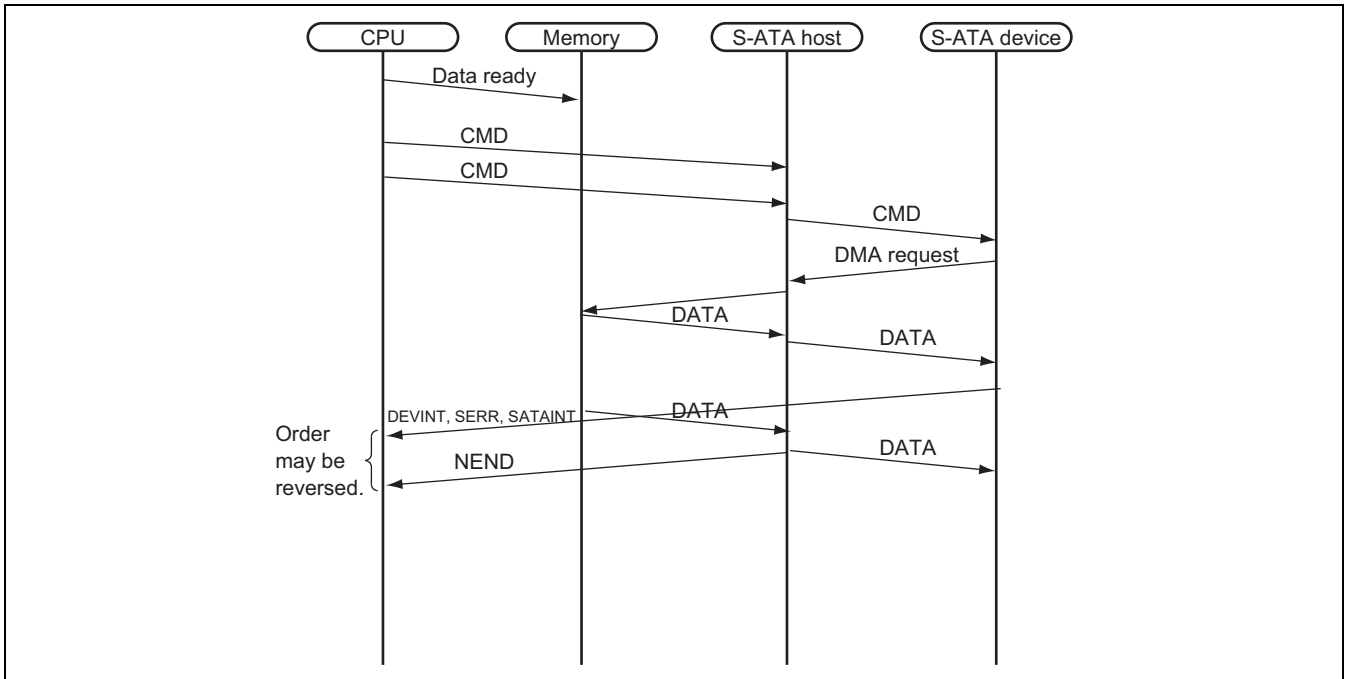


Figure 50.5 DATA-OUT (SATA Device Error)

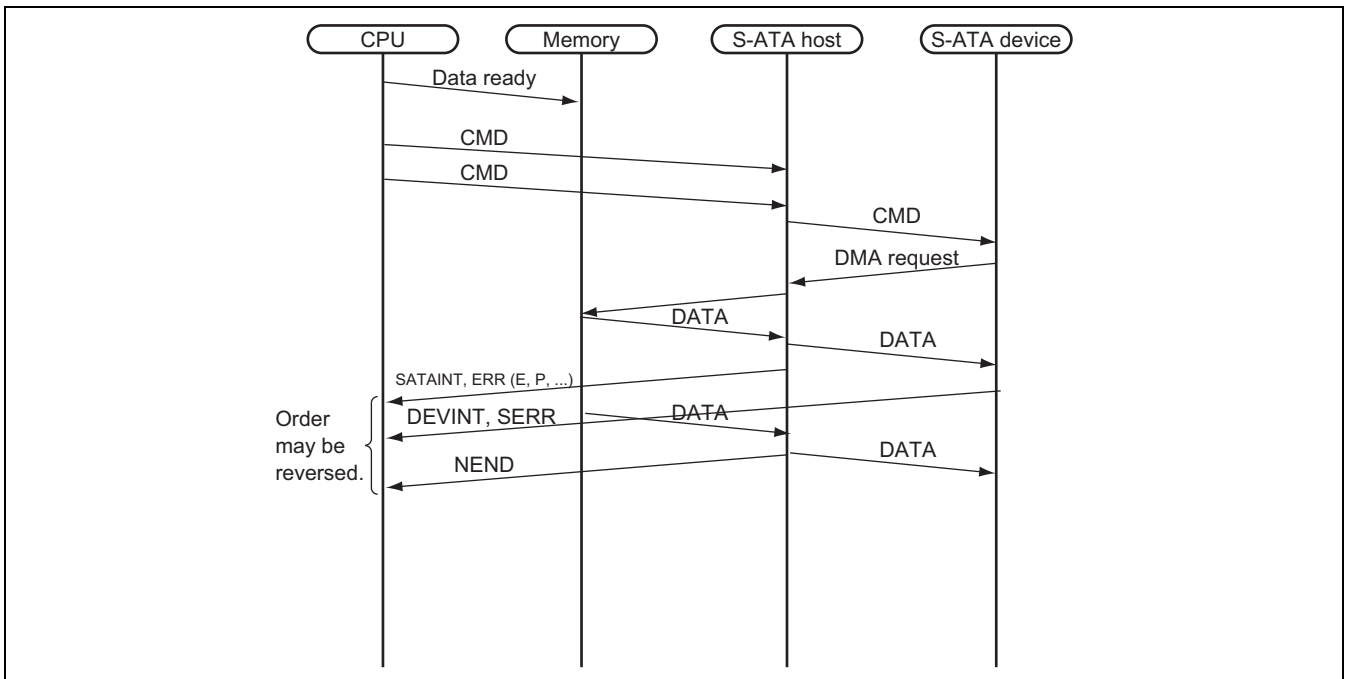


Figure 50.6 DATA-OUT (SATA Communication/Host-Sourced Error)

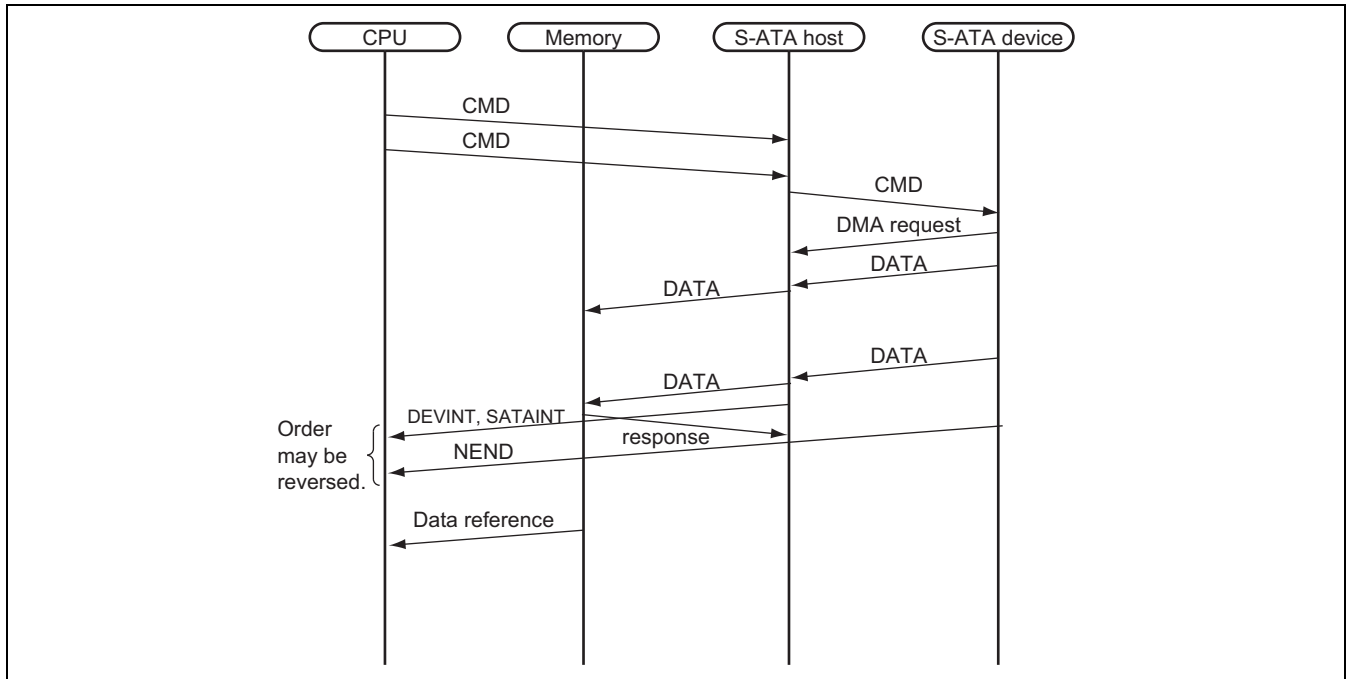


Figure 50.7 DATA-IN (Normal Mode Interrupts)

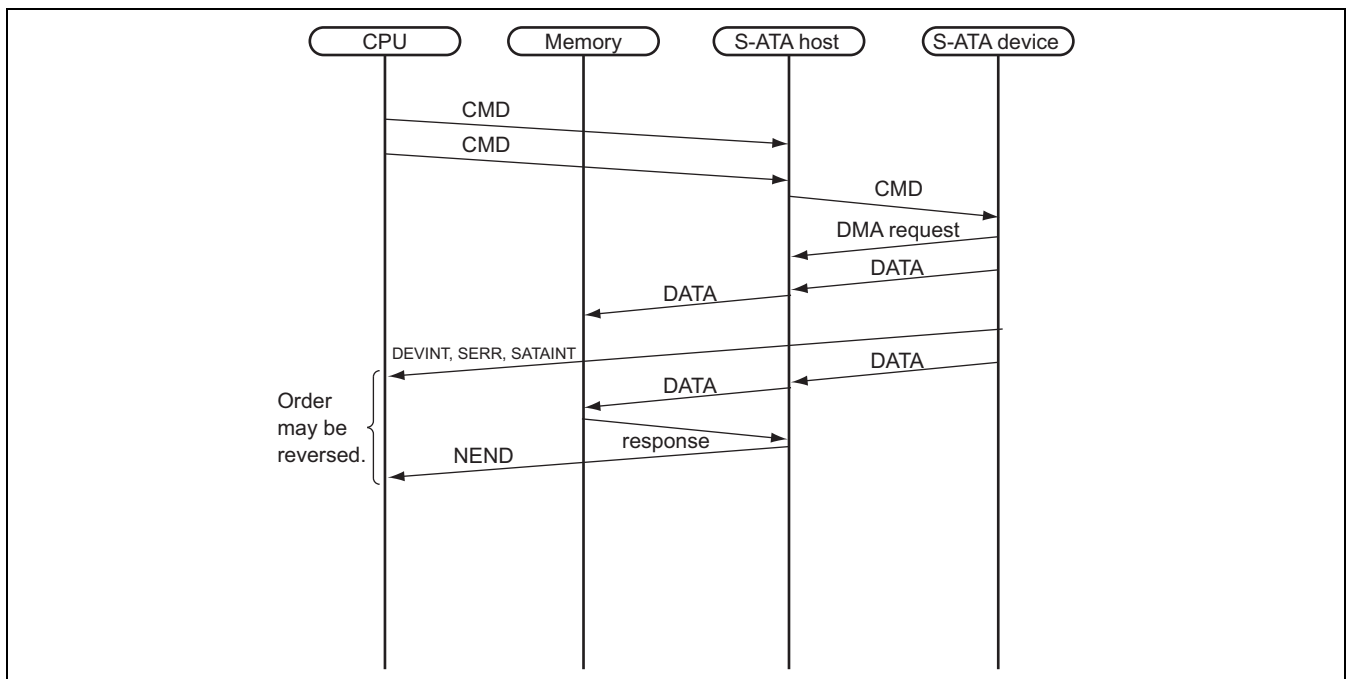


Figure 50.8 DATA-IN (SATA Device Error)

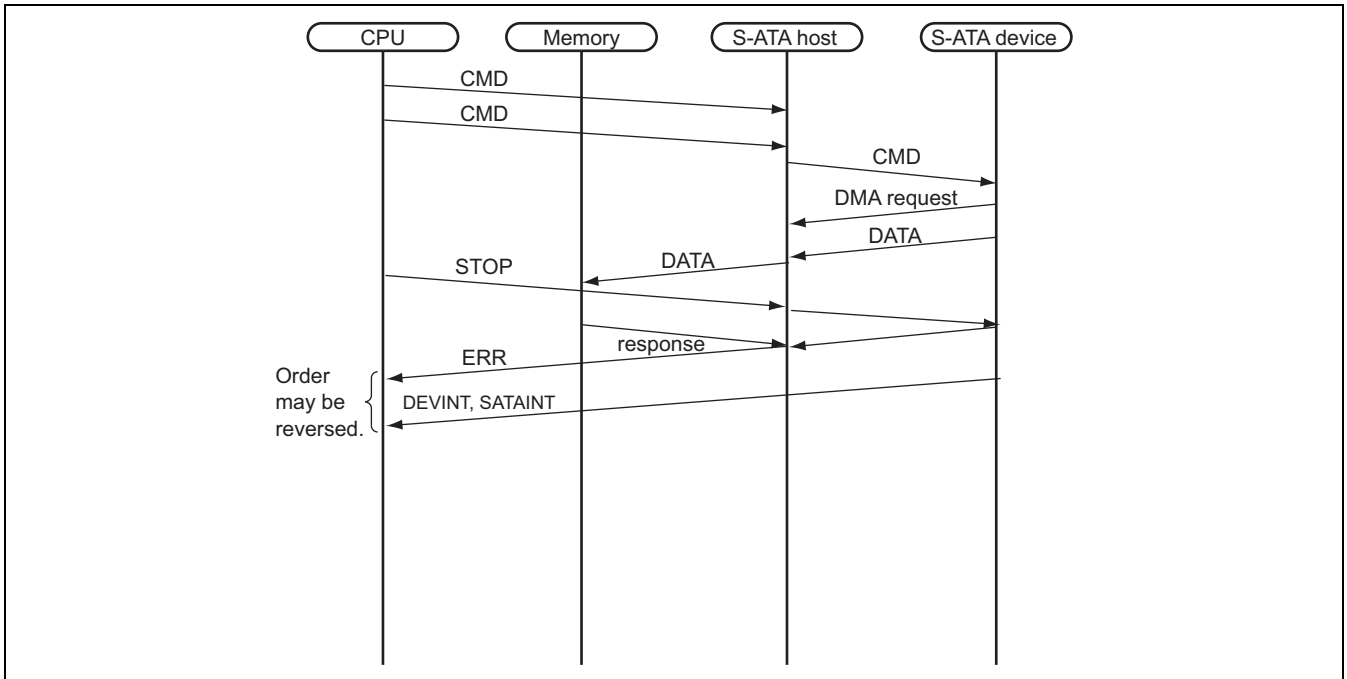


Figure 50.9 DATA-IN (Internal Bus or CPU Sources)

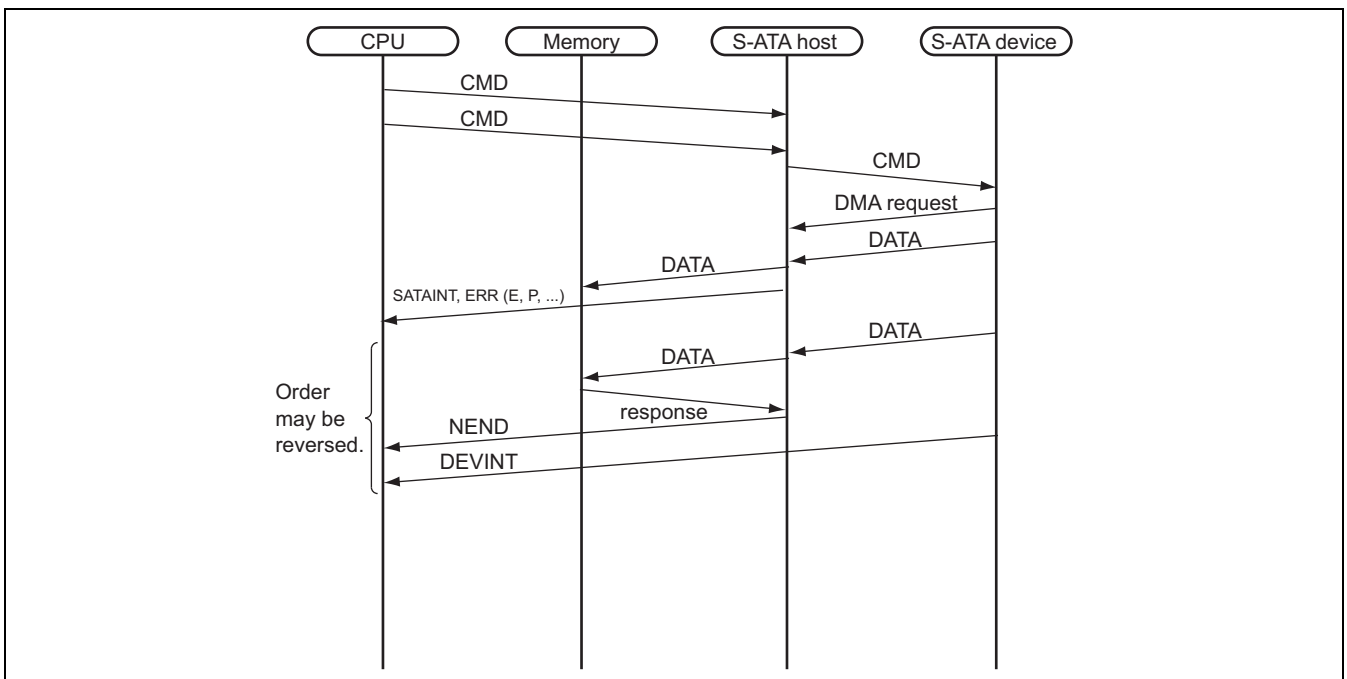


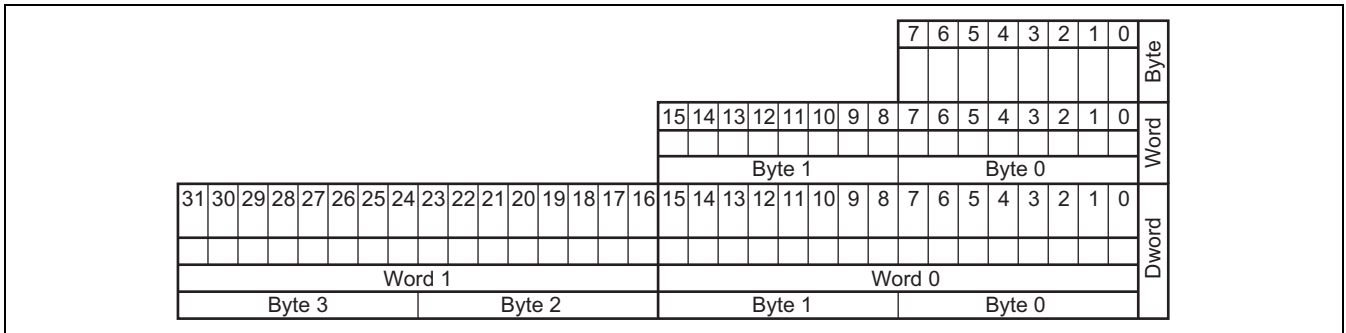
Figure 50.10 DATA-IN (SATA Communication/Host-Sourced Error)



**50.3.8 Endian**

This module adopts little endian. Consequently, data is represented in the same way as specified in the ATA/ATAPI-7 Specification and Serial-ATA Specification.

The bits of the registers are assigned in the order shown in Figure 50.11.



**Figure 50.11 Endian and Bit Order**

### 50.3.9 SATA BIST Modes

This module supports the Far-end Retimed Loopback and Far-end Analog Loopback modes that are stipulated in the Serial-ATA standard. The SATA BIST mode is the Loopback mode in which Loopback is formed on the host side. This mode can be configured and controlled for operation using the BIST config register (BISTCONF).

No match is performed between the transmit data from this module and the receive data from the device.

#### (1) Loopback Mode

In this mode, the data characters that are received are looped back to the sending side. The processing passes through the steps of input for reception → 10b/8b conversion → (Loopback) → 8b/10b conversion → output for transmission. This corresponds to the Serial-ATA Specification's Far-end Retimed Loopback (Figure 50.12).

There are cases in which some action is requested by the device side in this mode. More specifically, the device side will request the module to transmit the BIST Activate FIS. The module, however, can reject the request.

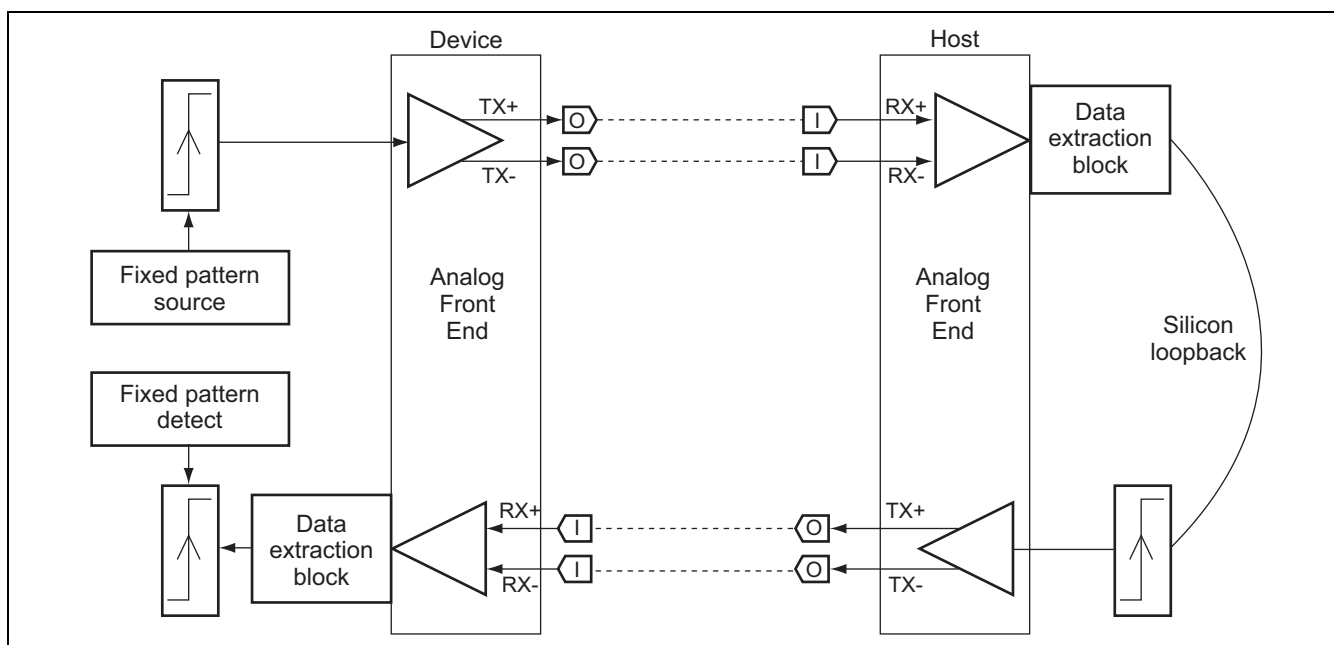
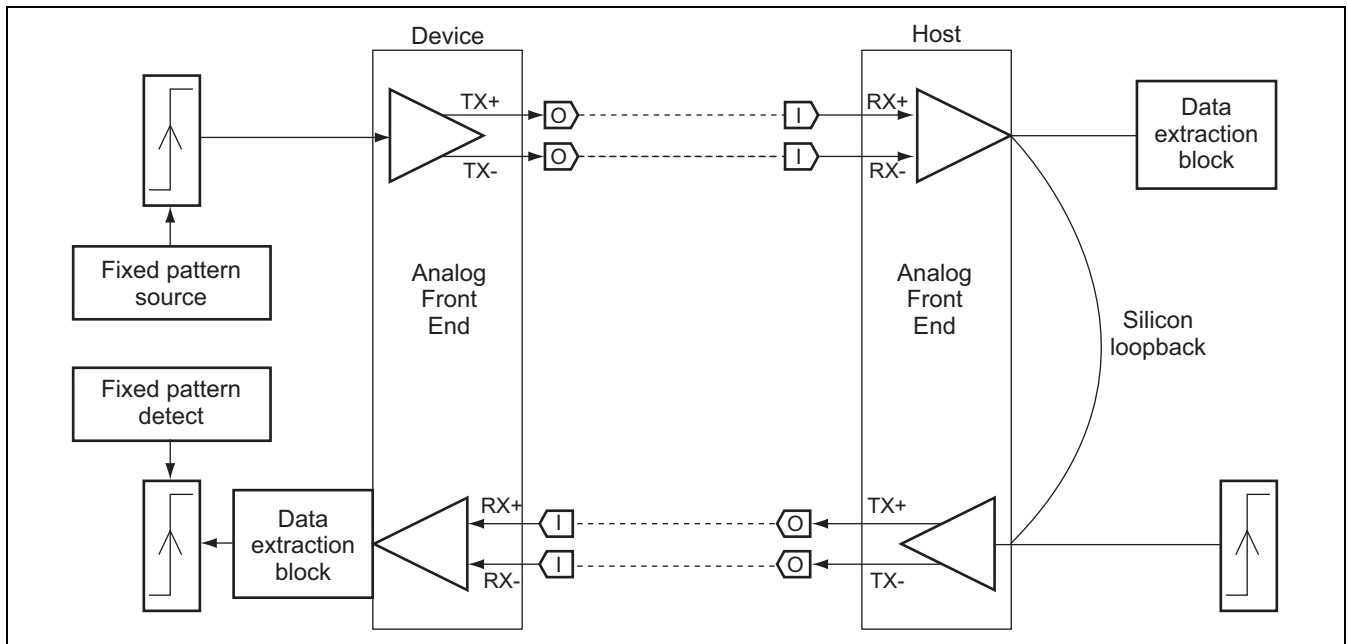


Figure 50.12 Far-End Retimed Loopback

**(2) Analog Loopback Mode**

This module does not support the Far-End Analog Loopback Mode (Figure 50.13) that is stipulated in the Serial-ATA Specification. In this mode, the received signal loops back through the AFE and output without modification as the result of which none of the Link and Transport layers get activated.

There are cases in which some action is requested by the device side in this mode. More specifically, the device side will request the module to transmit the BIST Activate FIS. The module, however, can reject the request.



**Figure 50.13 Far-End Analog Loopback**

### 50.3.10 Operation Flow

Figure 50.14 shows the flow of operations for turning on the power, setting the interrupt mode, and initializing the PHY layer.

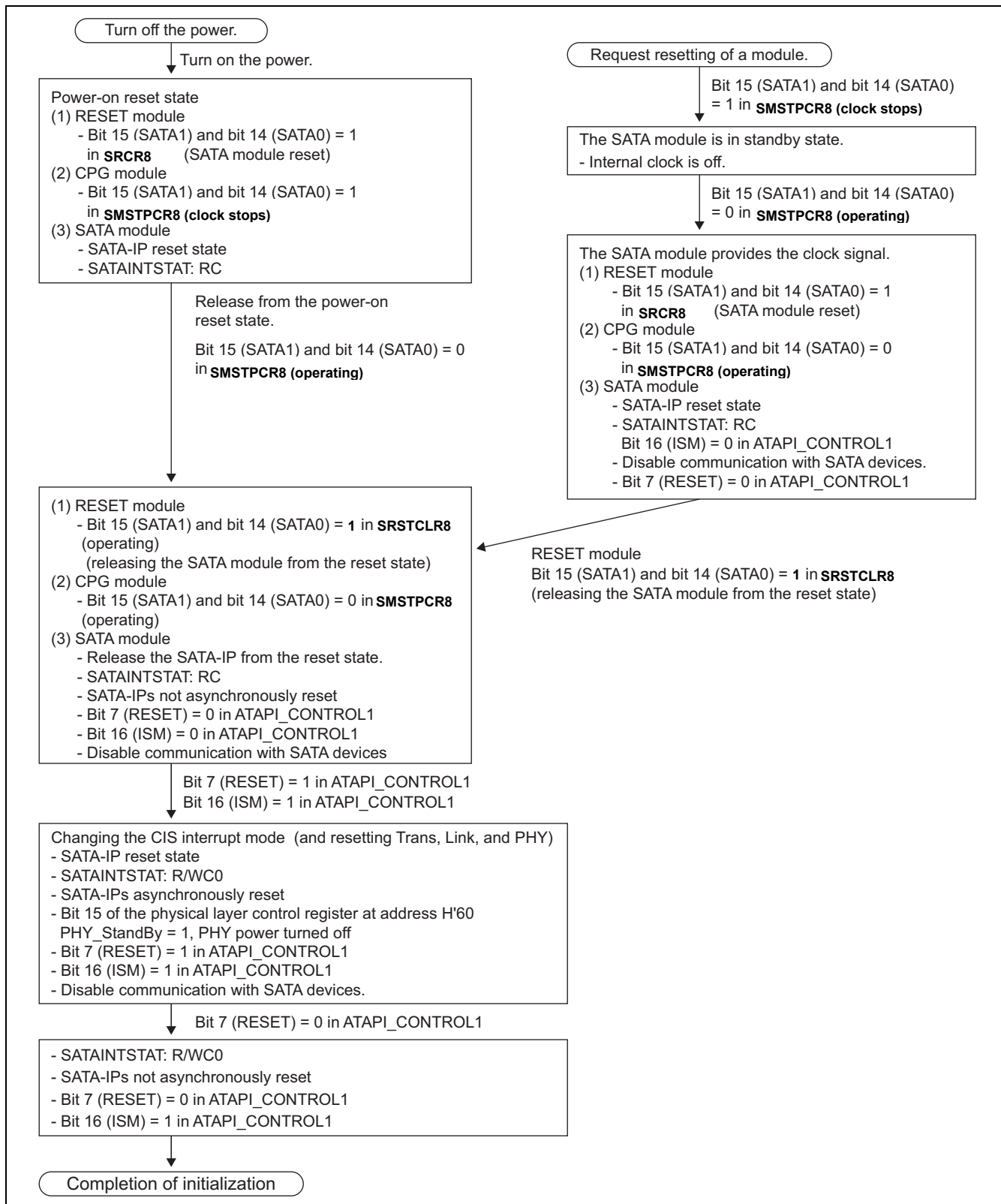


Figure 50.14 Operation Flow

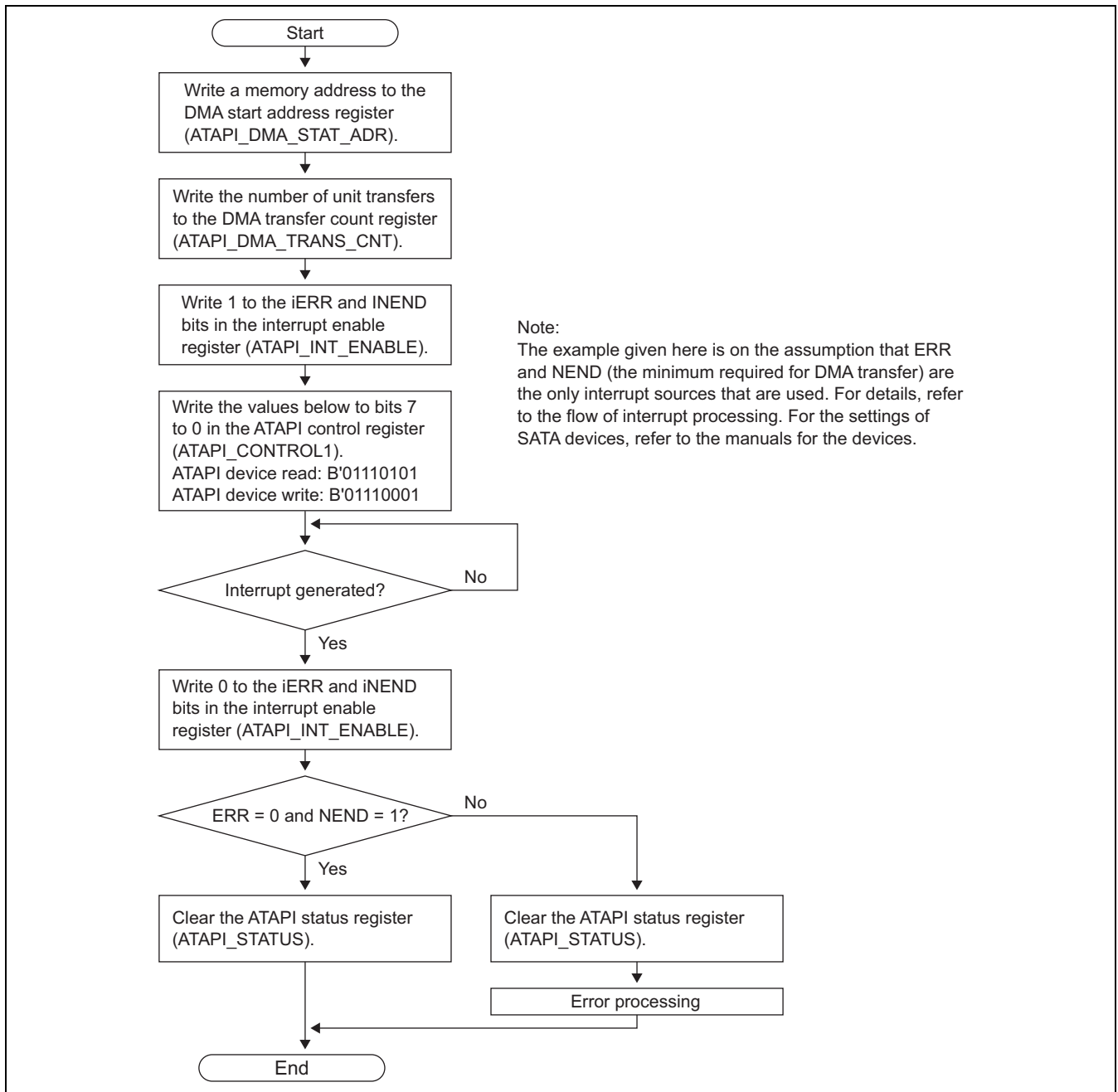


Figure 50.15 Flow of Data Transfer

## 50.4 Notes on Use

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

### 50.4.1 Resets

#### (1) Power-on Reset

It is possible to reset this module into the initial state that is entered when the module is started by performing a power-on reset. Set and hold this line low for 25  $\mu$ s or longer before releasing the signal. When the reset sequence subsequently gets completed, the BSY bit of the shadow status register (SSTATUS) is set to 0 (the same sequence as in a hardware reset is carried out after the SATA interface is stabilized).

#### (2) Resetting the SATA Module

The RESET module has reset functions equivalent to those of a power-on reset. Refer to the descriptions of SATA\_0 (bit 15) and SATA\_1 (bit 14) in the SRCR8 register and SRSTCLR8 register of the RESET module.

#### (3) SH-Navi2G-Compatible P-ATA Interface Reset

This module supports a reset function that is compatible with the reset function for the SH-Navi2G's parallel ATA interface. Refer to the description of RESET (bit 7) in the ATAPI control register (ATAPI\_CONTROL1).

This function resets the SATA Link and PHY blocks, as well as the SATA devices.

Release from the reset state should be after retention at the low level for at least 25  $\mu$ s. On completion of the reset sequence, the BSY bit of the shadow status register (SSTATUS) is set to 0 (after the SATA interface has become stable, the same sequence as for a hardware reset is executed).

#### (4) Hardware Reset

Changing the value of the CDET field of the SCR SControl register (SCRSCON) from B'0001 to B'0000 resets the device and the Phy, Link, and Transport layers' state machines. This handling corresponds to the Hardware Reset stipulated in the ATA standard. Reset the CDET field to B'0001 and, after the lapse of 25  $\mu$ s or longer, reset it to B'0000. When the reset sequence subsequently is completed, the BSY bit of the shadow status register (SSTATUS) is set to 0.

The hardware reset causes all of the shadow task registers (shadow data (DATA), shadow error (SERR), shadow features (SFEATURES), shadow sector CNT (SECCNT), shadow LBA low (LBALOW), shadow LBA mid (LBAMID), shadow LBA high (LBAHIGH), shadow device/head (DEVHEAD), shadow status (SSTATUS), shadow command (SCOM), shadow alternates status (SALTSTS), and shadow device control (SDEVCON) registers), SATA extend register and SCR registers (SCR SStatus (SCRSSSTS), SCR SError (SCRSEERR), SCR SControl (SCRSCON), and SCR SActive (SCRSACT) registers) to be reset.

Note: Refer also to the ATA/ATAPI-7 specification and Serial-ATA specification for further information about register update and hardware reset.

#### (5) Software Reset

The ATA specified software reset can be carried out by setting and resetting the SRST bit of the shadow device control register (DEVHEAD). Set the SRST bit to 1 and, after the lapse of 5  $\mu$ s or longer, reset the bit to 0. When the reset sequence subsequently is completed, the BSY bit of the shadow status register (SSTATUS) is set to 0.

Note: Refer also to the ATA/ATAPI-7 specification and Serial-ATA specification for further information about register update and software reset.

### 50.4.2 Extended ATA Registers

The five ATA stipulated registers, i.e., Features, sector count, LBA low, LBA mid, and LBA high registers, are provided with an 8-bit extended (exp) register. This register is used by the 48-bit Address feature set commands, WRITE FPDMA QUEUED, and READ FPDMA QUEUED commands.

This host controller module implements the exp registers for the above registers according to the ATA standard.

The following steps are required when writing data into the exp register of, for example, the Sector Count register:

- 1) Write a desired value to be set in sector count exp register to the sector count register.
- 2) Write a desired value to be set in sector count register to the sector count register.

Consequently, the value that is written in step 1) is pushed into the exp register by the access that is made in step 2).

This host controller module transmits the data corresponding to the exp register as contents of the (H2D) Register FIS irrespective of the command code specified. Whether the data corresponding to the exp register is used or not is at the discretion of the command interpreter on the device side and the host side makes no intervention.

### 50.4.3 Signature of the Shadow Register (INFORMATIVE)

The Serial-ATA Specification stipulates that the device shall transmit a Register FIS\*<sup>1</sup> immediately after a power-on reset, hardware reset, or software reset\*<sup>2</sup> for the purpose of loading a shadow register with a value called the signature. This is also stipulated in the ATA/ATAPI-7 standard in the same way. Even when this SATA module reads out the shadow register for the purpose of receiving this register FIS and having its value reflected in the shadow register, for example, following the completion of OOB processing at power-on time, it cannot read the original initial value of the register because its value has already been modified.

For details on the signature, refer to the section on "Device command layer protocol" in the Serial-ATA Specification.

- Notes:
1. There are commands such as EXECUTE DEVICE DIAGNOSTIC which take the signature as their return value. Their detailed description is omitted here. For details, refer to the Serial-ATA Specification.
  2. This refers to the PHYRDY state, that is, immediately after bits 3-0 of the SCR SStatus register (SCRSSSTS) are set to B'0011 for power-on reset and hardware reset, and to the time immediately after the reset processing is completed on the device side for software reset.

### 50.4.4 Host Termination

#### (1) Restriction

Immediately after host termination is executed in this IP, conduct a power-on reset or reset the hardware immediately.  
Fractional Data in DOUT Transfer

For host termination in DOUT transfer, the last DWORD is copied, including the end of the data management unit for the device. Zero padding is applied where data do not take up 16 bits.

### 50.4.5 SH-Navi2G Compatible Registers

#### (1) Parallel-ATA Compatible Task Registers (SATA-IP Task Registers)

**Table 50.7 Parallel-ATA Compatible Task Register (SATA-IP Task Register) Map**

(The registers listed below are allocated to the SATA device and their mirror values are retained in this module.)

Address	Read Register	Write Register	Access Size*1 (Possible Bit Size)	Register Location	Register Abbreviation	
					Read	Write
H'0100	Data	Data	32 (16)*2	Drive	DATA	DATA
H'0104	Error	Function	32 (8)*3	Drive	SERR	SFEATURES
H'0108	Sector count	Sector count	32 (8)*3	Drive	SECCNT	SECCNT
H'010C	Sector number	Sector number	32 (8)*3	Drive	LBALOW	LBALOW
H'0110	Cylinder low	Cylinder low	32 (8)*3	Drive	LBAMID	LBAMID
H'0114	Cylinder high	Cylinder high	32 (8)*3	Drive	LBAHIGH	LBAHIGH
H'0118	Device/head	Device/head	32 (8)*3	Drive	DEVHEAD	DEVHEAD
H'011C	Status	Command	32 (8)*3	Drive	SSTATUS	SCOM
H'0120	Obsolete	Obsolete	32 (8)*2		—	—
H'0124	Obsolete	Obsolete	32 (8)*2		—	—
H'0128	Obsolete	Obsolete	32 (8)*2		—	—
H'012C	Obsolete	Obsolete	32 (8)*2		—	—
H'0130	Obsolete	Obsolete	32 (8)*2		—	—
H'0134	Obsolete	Obsolete	32 (8)*2		—	—
H'0138	Alternate status	Device control	32 (8)*3	Drive	SALTSTS	SDEVCON
H'013C	Obsolete	Obsolete	32 (8)*3		—	—

Notes: 1. The CPU must access the above listed registers in longword (32-bit) units. Accesses in byte or word units are not allowed.

2. Bits 15 to 0 of the data bus are used.

3. Bits 7 to 0 of the data bus are used.

"Enable external accesses when ATAPI control register, RADRE = 1" has been made obsolete.

The real value of the mirror value of this task register is held in the SATAIP unit and doubly decoded.

While the PATA registers use a 32-bit APB bus, the SATA registers use a 64-bit AXI Bus. The registers hold addresses in their 32 bits and map them onto the 64-bit bus.



**(2) Parallel-ATA Compatible ATAPI Packet Command Task File Registers (SATA-IP Task Registers)****Table 50.8 Parallel-ATA Compatible ATAPI Packet Command Task File Register Map**

(The registers listed below are allocated to the SATA device and their mirror values are retained in this module.)

Address	Read Register	Write Register	Access Size*1 (Possible Bit Size)	Register Location	Register Abbreviation	
					Read	Write
H'0100	Data	Data	32 (16)*2	Drive	DATA	DATA
H'0104	Error	Function	32 (8)*3	Drive	SERR	SFEATURES
H'0108	Interrupt source	—	32 (8)*3	Drive	SECCNT	SECCNT
H'010C	—	—	32 (8)*3	Drive	LBALOW	LBALOW
H'0110	Byte count low	Byte count low	32 (8)*3	Drive	LBAMID	LBAMID
H'0114	Byte count high	Byte count high	32 (8)*3	Drive	LBAHIGH	LBAHIGH
H'0118	Device select	Device select	32 (8)*3	Drive	DEVHEAD	DEVHEAD
H'011C	Status	Command	32 (8)*3	Drive	SSTATUS	SCOM
H'0120	Obsolete	Obsolete	32 (8)*2		—	—
H'0124	Obsolete	Obsolete	32 (8)*2		—	—
H'0128	Obsolete	Obsolete	32 (8)*2		—	—
H'012C	Obsolete	Obsolete	32 (8)*2		—	—
H'0130	Obsolete	Obsolete	32 (8)*2		—	—
H'0134	Obsolete	Obsolete	32 (8)*2		—	—
H'0138	Alternate status	Device control	32 (8)*2	Drive	SALTSTS	SDEVCON
H'013C	Obsolete	Obsolete	32 (8)*3		—	—

Notes: 1. The above listed registers must be accessed in longword (32-bit) units. Accesses in byte or word units are not allowed.

2. Bits 15 to 0 of the data bus are used.

3. Bits 7 to 0 of the data bus are used.

The above listed registers must be accessed in longword (32-bit) units. Accesses in byte or word units are not allowed.

"Enable external accesses when ATAPI control register, RADRE = 1" has been made obsolete.

The real value of the mirror value of this task register is held in the SATAIP unit and doubly decoded.

While the PATA registers use a 32-bit APB bus, the SATA registers use a 64-bit AXI Bus. The registers hold addresses in their 32 bits and map them onto the 64-bit bus.

**(3) SH-Navi2G/ATAPI Module Compatible Control Register (Parallel-ATA) Map****Table 50.9 ATAPI Interface Control Register Map**

(The registers listed below are allocated to the internal bus bridge block of this LSI SATA module.)

Address	Register Name	Symbol	Access Type	Register Access Size*1
H'0000 to H'00FC	Reserved	—	R	32
H'0140 to H'017C	Reserved	—	R	32
H'0180	ATAPI control register	ATAPI_CONTROL1	R/W	32
H'0184	ATAPI status register	ATAPI_STATUS	R/WC0	32
H'0188	Interrupt enable register	ATAPI_INT_ENABLE	R/W	32
H'018C to H'0194	Reserved	—	R	32
H'0198	Descriptor table base address register	ATAPI_DTB_ADR	R/W	32
H'019C	DMA start address register	ATAPI_DMA_START_ADR	R/W	32
H'01A0	DMA transfer count register	ATAPI_DMA_TRANS_CNT	R/W	32
H'01A4	ATAPI control 2 register	ATAPI_CONTROL2	R/W	32
H'01A8	Reserved	—	R	32
H'01AC	Reserved	—	R	32
H'01B0	ATAPI signal status register	ATAPI_SIG_ST	R	32
H'01BC	Byte swap register	ATAPI_BYTE_SWAP	R/W	32
H'01C0 to H'01FC	Reserved	—	R	32

Note: The above listed registers must be accessed in longword (32-bit) units. Accesses in byte or word units are not allowed.

**(4) Differences in Registers and Flags****Table 50.10 Differences in Registers**

RZ/G1H Register Name		SH-Navi2G Register Name		Description
Name	Abbreviation	Name	Abbreviation	
Obsolete	—	As at left	—	For SATA, discarded addresses from the ATA Specification are allocated to IP-specific debugging functions such as monitoring. Access to these registers is prohibited.
ATAPI control	ATAPI_CONTROL1	As at left	As at left	Refer to ATAPI_CONTROL1 in Table 50.11, Differences in Flags.
ATAPI status	ATAPI_STATUS	As at left	As at left	Refer to ATAPI_STATUS in Table 50.11, Differences in Flags.
Interrupt enable	ATAPI_INT_ENABLE	As at left	As at left	<p>Although this register is inherited, there are differences in the interrupt sources. Also, interrupt masking in the INTC register is required during a module reset.</p> <p>Do not clear the interrupt mask of the INTC while the SATA module is being reset. For resetting of the SATA module, refer to the descriptions of SRCR8 register and SRSTCLR8 register of the RESET module. For the interrupt mask of INTC, refer to the description of IMR4S3 register of the INTC module.</p>
ATAPI control 2	ATAPI_CONTROL2	As at left	As at left	Refer to ATAPI_CONTROL2 in Table 50.11, Differences in Flags.
Reserved	—	PIO timing 1	ATAPI_PIO_TIMING1	The settings for timing are ignored.
Reserved	—	PIO timing 2	ATAPI_PIO_TIMING2	
Reserved	—	Multi-word DMA timing	ATAPI_MULTI_TIMING	
Reserved	—	Ultra DMA timing	ATAPI_ULTRA_TIMING	

Table 50.11 Differences in Flags

- ATAPI control register (ATAPI\_CONTROL)

RZ/G1H/M/N Flag Name				SH-Navi2G Flag Name		Description
Bit	Bit Name	Initial Value	R/W	Bit Name	Initial Value	
16	ISM	0	R/W	—	—	An interrupt mode was added. The initial setting and interrupt handling differ from those for SH-Navi2G.
12	—	0	R	RADRE	0	This bit is allocated to IP-specific debugging functions such as monitoring. Setting this bit to 1 is prohibited.
9	—	0	R	DTCD	0	When device termination occurs, completion of DMA transfer is not possible.
7	RESET	0	R/W	RESET	0	The SATAIP module and SATA devices are reset. In parallel ATA, only the devices were reset.
6	—	1	R	M/S	0	Only the master setting is available. In the SH-Navi2G, the slave setting was the initial value.
5	—	1	R	—	1	In the SH-Navi2G, setting this bit to 0 was prohibited. In the SH-Navi3, setting this bit to 0 is ignored.
4	—	1	R	UDMAEN	0	SATA is set to emulate the ultra DMA mode. In the SH-Navi2G, the setting for the multi-word DMA mode was the initial value.

- ATAPI status register (ATAPI\_STATUS)

RZ/G1H/M/N Flag Name				SH-Navi2G Flag Name		Description
Bit	Bit Name	Initial Value	R/W	Bit Name	Initial Value	
31	SSBSY	0	R	—	—	This function was added for SATA.
30	SDDRQ	0	R	—	—	This function was added to SATA.
27	SDDRQ	0	R	—	—	This function was added to SATA.
24	SSERR	0	R	—	—	This function was added to SATA.
11	SATAINT	0	R	—	—	This function was added to SATA.
8	SWERR	0	R/WC0	SWERR	0	The shadow task registers are mapped to the Serial-ATA HOST control registers and are accessible during DMA transfer.
7	—	—	R	IFERR	0	SATA has functions to suit the IP module. Refer to the SCR Error register (SCRSEERR) to check the values of flags such as that for protocol errors.
3	—	—	R	TOUT	0	SATA has functions to suit the IP module. Refer to the SCR Error register (SCRSEERR) to check the values of flags such as that for protocol errors.
2	ERR	0	R/WC0	ERR	0	Since DTCD is fixed to 0, 'DTCD = 1 and ACT = 0 because of device termination' was deleted.

- ATAPI signal status register (ATAPI\_SIG\_ST)

RZ/G1H Flag Name				SH-Navi2G Flag Name		Description
Bit	Bit Name	Initial Value	R/W	Bit Name	Initial Value	
1	DPIORDY	—	R	DDMARDY	—	IORDY cannot be monitored during DMA transfer.

**50.4.6 Clock Input in the Partial and Slumber States**

Do not stop input of the reference clock signal while the interface is in the Partial or Slumber state.

## 51. USB2.0 Host (EHCI/OHCI)

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

### 51.1 Overview

Complies with Universal Serial Bus Specification Revision 2.0

Complies with Open Host Controller Interface (OHCI) Specification for USB Rev 1.0a

Complies with Enhanced Host Controller Interface (EHCI) Specification for USB Rev 1.0

Supports USB2.0 High-Speed (480 Mbps)/Full-Speed (12 Mbps)/Low-Speed (1.5 Mbps) transfer

Supports USB2.0 compliance test function.

USB reference clock fixed 48 MHz.

Required address size: 128 Kbytes (Align on a 128-Kbyte boundary.)

<b>RZ/G1H</b>	<b>RZ/G1N</b>
<b>RZ/G1M</b>	<b>RZ/G1E</b>

## 51.2 Register Mapping

There are following three register areas:

1. OHCI/EHCI Operational Registers area
2. PCI Configuration Space
3. AHB-PCI Bridge PCI Communication area

To access each area in the PCI Configuration Space, the AHB-PCI Bridge register AHBPCI\_WIN1\_CTR should be set. Addresses should be correctly allocated for the areas such as OHCI/EHCI Operational Registers and PCI Communication Space in the PCI space in the USB in addition to mapping registers in the AHB space. For details on the register accesses and address mapping, refer to section 51.7, Register Accesses.

Offset address from each channel base address [Ch.0: H'EE080000, Ch.1: H'EE0A0000, Ch.2: H'EE0C0000]. [RZ/G1H]

Offset address from each channel base address [Ch.0: H'EE080000, Ch.1: H'EE0C0000]. [RZ/G1M/N/E]

Note: Do not access registers in the reserved area.

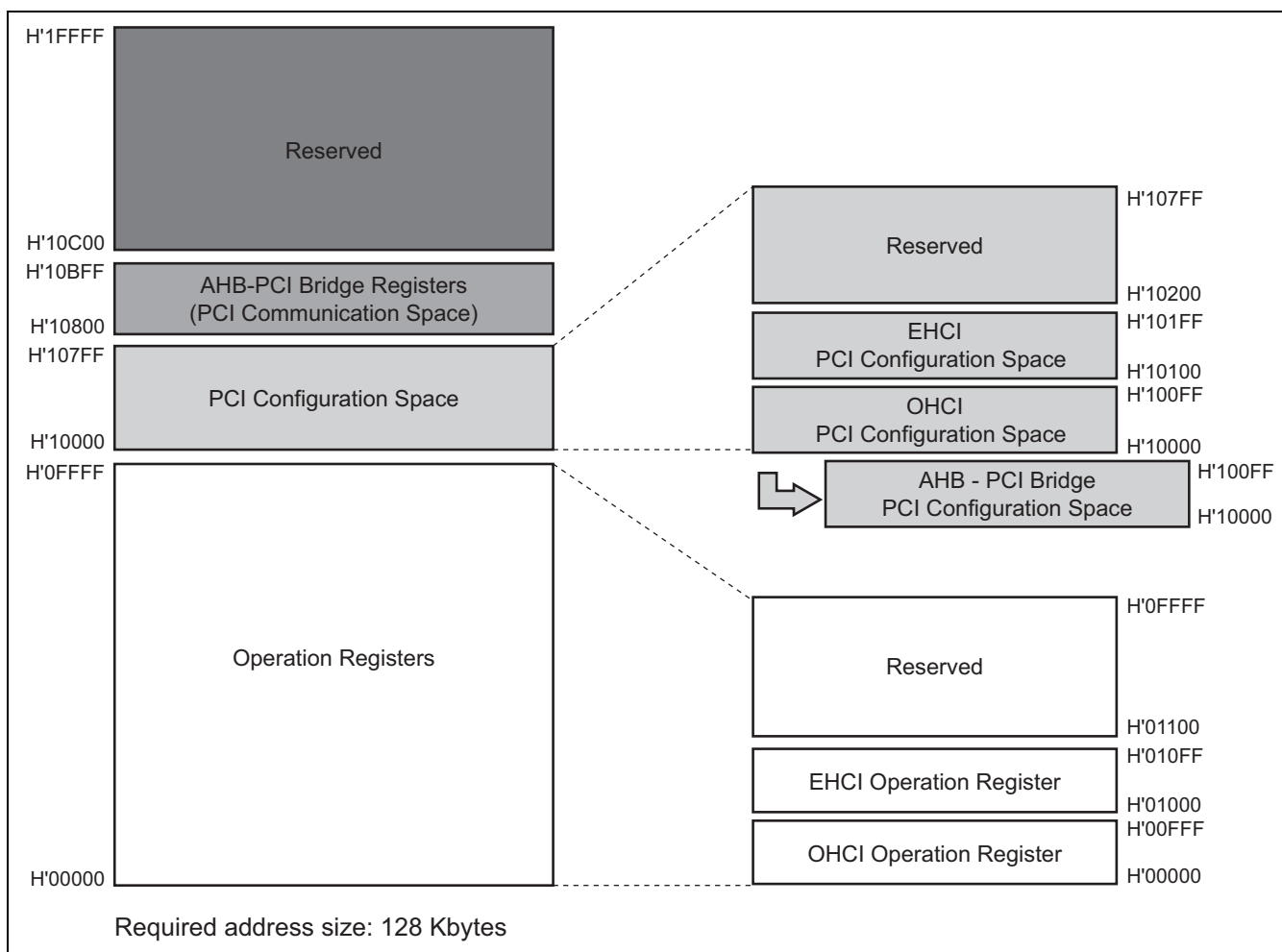


Figure 51.1 Register Mapping

**Table 51.1 Register Mapping List**

Address Offset	Register Name	Abbreviation
H'00000	HcRevision	HcRevision
H'00004	HcControl	HcControl
H'00008	HcCommandStatus	HcCommandStatus
H'0000C	HcInterruptStatus	HcInterruptStatus
H'00010	HcInterruptEnable	HcInterruptEnable
H'00014	HcInterruptDisable	HcInterruptDisable
H'00018	HcHCCA	HcHCCA
H'0001C	HcPeriodCurrentED	HcPeriodCurrentED
H'00020	HcControlHeadED	HcControlHeadED
H'00024	HcControlCurrentED	HcControlCurrentED
H'00028	HcBulkHeadED	HcBulkHeadED
H'0002C	HcBulkCurrentED	HcBulkCurrentED
H'00030	HcDoneHead	HcDoneHead
H'00034	HcFmInterval	HcFmInterval
H'00038	HcFmRemaining	HcFmRemaining
H'0003C	HcFmNumber	HcFmNumber
H'00040	HcPeriodicStart	HcPeriodicStart
H'00044	HcLSThreshold	HcLSThreshold
H'00048	HcRhDescriptorA	HcRhDescriptorA
H'0004C	HcRhDescriptorB	HcRhDescriptorB
H'00050	HcRhStatus	HcRhStatus
H'00054	HcRhPortStatus1	HcRhPortStatus1
H'00058 to H'00FFC	Reserved	—
H'01000	HCIVERSION / CAPLENGTH	CAPL_VERSION
H'01004	HCSPARAMS	HCSPARAMS
H'01008	HCCPARAMS	HCCPARAMS
H'0100C	HCSP_PORTROUTE	HCSP_PORTROUTE
H'01010 to H'0101C	Reserved	—
H'01020	USBCMD	USBCMD
H'01024	USBSTS	USBSTS
H'01028	USBINTR	USBINTR
H'0102C	FRINDEX	FRINDEX
H'01030	CTRLDSSEGMENT	CTRLDSSEGMENT
H'01034	PERIODICLISTBASE	PERIODICLISTBASE
H'01038	ASYNCLISTADDR	ASYNCLISTADDR
H'0103C to H'0105C	Reserved	—
H'01060	CONFIGFLAG	CONFIGFLAG
H'01064	PORTSC1	PORTSC1
H'01068 to H'0FFFC	Reserved	—
H'10000 to H'107FC	PCI Configuration Space (AHB-PCI Bridge / OHCI / EHCI )	—
H'10800	PCIAHB_WIN1_CTR	PCIAHB_WIN1_CTR



Address Offset	Register Name	Abbreviation
H'10804	PCIAHB_WIN2_CTR	PCIAHB_WIN2_CTR
H'10808 to H'1080C	Reserved	—
H'10810	AHBPCI_WIN1_CTR	AHBPCI_WIN1_CTR
H'10814	AHBPCI_WIN2_CTR	AHBPCI_WIN2_CTR
H'10818 to H'1081C	Reserved	—
H'10820	PCI_INT_ENABLE	PCI_INT_ENABLE
H'10824	PCI_INT_STATUS	PCI_INT_STATUS
H'10828 to H'1082C	Reserved	—
H'10830	AHB_BUS_CTR	AHB_BUS_CTR
H'10834	USBCTR	USBCTR
H'10838 to H'1083C	Reserved	—
H'10840	PCI_ARBITER_CTR	PCI_ARBITER_CTR
H'10844	Reserved	—
H'10848	PCI_UNIT_REV	PCI_UNIT_REV
H'1084C to H'1FFFC	Reserved	—

### 51.3 PCI Configuration Space for AHB-PCI Bridge

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

Table 51.2 shows the mapping of PCI-Configuration Space registers for the AHB-PCI Bridge.

**Table 51.2 PCI Configuration Space for AHB-PCI Bridge**

Offset	31	24	23	16	15	8	7	0	Abbreviation
H'000	Device ID				Vendor ID				VID_DID
H'004	Status				Command				CMND_STS
H'008	Class Code						Revision ID		REVID_CC
H'00C	BIST	Header Type		Latency Timer		Cache Line Size		CLS_LT_HT_BIST	
H'010	AHB-PCI Bridge Registers Base Address								BASEAD
H'014	PCI-AHB Window1 Base Address								WIN1_BASEAD
H'018	PCI-AHB Window2 Base Address								WIN2_BASEAD
H'01C	Reserved								—
H'020									
H'024									
H'028									
H'02C	Subsystem ID				Subsystem Vendor ID				SSVID_SSID
H'030	Reserved								—
H'034									
H'038									
H'03C	Max_Lat	Min_Gnt		Interrupt Pin		Interrupt Line		INTR_LINE_PIN	
H'040	Reserved								—
...									
H'0FC									

## 51.4 PCI Configuration Space for OHCI Host Logic

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

Table 51.3 shows the mapping of PCI-Configuration Space registers for the OHCI host logic.

**Table 51.3 PCI Configuration Space for OHCI**

Offset	31	24	23	16	15	8	7	0	Abbreviation
H'000	Device ID			Vendor ID				VID_DID	
H'004	Status			Command				CMND_STS	
H'008	Class Code					Revision ID		REVID_CC	
H'00C	BIST	Header Type		Latency Timer	Cache Line Size		CLS_LT_HT_BIST		
H'010	OHCI Base Address							BASEAD	
H'014	Reserved							—	
H'018									
H'01C									
H'020									
H'024									
H'028									
H'02C	Subsystem ID			Subsystem Vendor ID				SSVID_SSID	
H'030	Expansion ROM Base Address							EROM_BASEAD	
H'034	Reserved					Cap_ptr		CAPPTR	
H'038	Reserved							—	
H'03C	Max_Lat	Min_Gnt		Interrupt Pin	Interrupt Line		INTR_LINE_PIN		
H'040	PMC			Next_Item_Ptr	Cap_ID		CAPID_NIP_PMCAP		
H'044	Data	PMCSR_BSE		PMCSR			PMC_STS_PMCSR		
H'048 to H'0DC	Reserved							—	
H'0E0	EXT1							EXT1	
H'0E4	EXT2							EXT2	
H'0E8 to H'0FC	Reserved							—	

## 51.5 PCI Configuration Space for EHCI Host Logic

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

Table 51.4 shows the mapping of PCI-Configuration Space registers for the EHCI host logic.

**Table 51.4 PCI Configuration Space for EHCI**

Offset	31	24	23	16	15	8	7	0	Abbreviation
H'100	Device ID			Vendor ID				VID_DID	
H'104	Status			Command				CMND_STS	
H'108	Class Code					Revision ID		REVID_CC	
H'10C	BIST	Header Type		Latency Timer	Cache Line Size			CLS_LT_HT_BIST	
H'110	EHCI Base Address							BASEAD	
H'114	Reserved							—	
H'118									
H'11C									
H'120									
H'124									
H'128									
H'12C	Subsystem ID			Subsystem Vendor ID				SSVID_SSID	
H'130	Expansion ROM Base Address							EROM_BASEAD	
H'134	Reserved					Cap_ptr		CAPPTR	
H'138	Reserved							—	
H'13C	Max_Lat	Min_Gnt		Interrupt Pin		Interrupt Line		INTR_LINE_PIN	
H'140	PMC			Next_Item_Ptr		Cap_ID		CAPID_NIP_PMCAP	
H'144	Data	PMCSR_BSE		PMCSR				PMC_STS_PMCSR	
H'148	Reserved							—	
...									
H'15C									
H'160	PORTWAKECAP			FLAD	SBRN		SBRN_FLADJ_PW		
H'164 to H'1DC	Reserved							—	
H'1E0	EXT1							EXT1	
H'1E4	EXT2							EXT2	
H'1E8 to H'1FC	Reserved							—	

## 51.6 Register Descriptions

This section describes the register functions. The following shows the legends for the register bit maps.

Bit: Bit position in 32-bit space

R/W: R indicates readable space and W indicates writable space.

Reset: Read value after a reset

Note: A blank in the bit name space indicates a reserved bit.

### 51.6.1 OHCI Operational Registers

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Please refer to the OHCI standard for the details of the OHCI register. The meaning follows the OHCI standard.

#### 51.6.1.1 HcRevision Register

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	Revision[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved (Don't care)
7 to 0	Revision[7:0]	H'10	R	These bits indicate the HCI standard version implemented by the host logic. The set value H'10 indicates that this host logic complies with OHCI Standard 1.0a.

## 51.6.1.2 HcControl Register

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	RWE	RWC	IR	HCFS[1:0]	BLE	CLE	IE	PLE	CBSR[1:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 11	—	All 0	R	Reserved The write value should be 0.
10	RWE	0	R/W	Remote Wakeup Enable Controls PME assertion. When this bit is 1, PME is asserted when the RD (bit 3) in HcInterruptStatus is set to 1. 0: PME is not asserted when Resume is detected (PME disabled). 1: PME is asserted when Resume is detected (PME enabled).
9	RWC	0	R/W	Remote Wakeup Connect Selects whether or not the host logic supports the remote wakeup function or not. To support the remote wakeup by the system, set this bit during initialization. 0: Remote wakeup is not supported. 1: Remote wakeup is supported.
8	IR	0	R/W	Interrupt Routing Sets the host logic interrupt output route. Specifies the interrupt source notification method of interrupt source indicated in HcInterruptStatus to the system. This bit should not be changed from the initial value since SMI is not used in this module. 0: Interrupt generated through INTA 1: Interrupt generated through SMI
7, 6	HCFS[1:0]	00	R/W	Host Controller Functional State Sets the host logic operation state. A transition to USB operational state begins management of frames divided into 1 ms. The operation state is always controlled by the software except when transition to USB resume is caused during USB suspend state by the remote wakeup. These bits are set to the USB reset after a hardware reset, and set to USB suspend after a software reset. 00: USB reset 01: USB resume 10: USB operational 11: USB suspend

Bit	Bit Name	Initial Value	R/W	Description										
5	BLE	0	R/W	<p>Bulk List Enable</p> <p>Sets whether to perform Bulk list processing or not. This bit setting becomes effective from the next frame. To modify the Bulk list, this bit should be 0.</p> <p>0: Blk list processing is not performed. 1: Blk list processing is performed.</p>										
4	CLE	0	R/W	<p>Control List Enable</p> <p>Sets whether to perform Control list processing or not. This bit setting becomes effective from the next frame. To modify the Control list, this bit should be 0.</p> <p>0: Control list processing is not performed. 1: Control list processing is performed.</p>										
3	IE	0	R/W	<p>Isochronous Enable</p> <p>Sets whether or not to perform Isochronous ED processing. This bit setting becomes effective from the next frame. When the Isochronous ED is detected during list processing, this bit status is checked to determine whether or not to perform the Isochronous ED processing or not.</p> <p>0: Isochronous transfer is not performed 1: Isochronous transfer is performed</p>										
2	PLE	0	R/W	<p>Periodic List Enable</p> <p>Sets whether or not to perform Periodic list processing. This bit setting becomes effective from the next frame.</p> <p>0: Periodic list processing is not performed 1: Periodic list processing is performed</p>										
1, 0	CBSR[1:0]	00	R/W	<p>Control Bulk Service Ratio</p> <p>Sets the service ratio between the Bulk transfer and Control transfer.</p> <p>During the Periodic list processing, transfer is performed keeping the service ratio specified by these bits.</p> <table border="0"> <tr> <td>CBSR</td> <td>Service Ratio (BulkED:Control ED)</td> </tr> <tr> <td>00:</td> <td>1:1</td> </tr> <tr> <td>01:</td> <td>2:1</td> </tr> <tr> <td>10:</td> <td>3:1</td> </tr> <tr> <td>11:</td> <td>4:1</td> </tr> </table>	CBSR	Service Ratio (BulkED:Control ED)	00:	1:1	01:	2:1	10:	3:1	11:	4:1
CBSR	Service Ratio (BulkED:Control ED)													
00:	1:1													
01:	2:1													
10:	3:1													
11:	4:1													

### 51.6.1.3 HcCommandStatus Register

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SOC[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	OCR	BLF	CLF	HCR
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	W	R/W	R/W	W

Bit	Bit Name	Initial Value	R/W	Description
31 to 18	—	All 0	R	Reserved The write value should be 0.
17, 16	SOC[1:0]	00	R	Scheduling Overrun Count Indicates the number of schedule overruns. These bits are incremented on each schedule overruns. When the value reaches B'11, it returns to B'00. Increment is continued even if the SO (bit 0) in HcInterruptStatus is set.
15 to 4	—	All 0	R	Reserved The write value should be 0.
3	OCR	0	W	Ownership Change Request Changes the control right of the host logic.
2	BLF	0	R/W	Bulk List Filled Indicates whether there are any TDs on the Bulk list or not. The host logic checks this bit status to start the first ED processing on the Bulk list. When this bit is 0, the host logic does not start the list processing. When 1, the host logic starts the Bulk list processing and sets this bit to 0. If the host logic finds a TD on the Bulk list, this bit is set to 1 and the Bulk list processing is continued. When the host logic completes the list processing, this bit is cleared to 0. If a TD is not detected in the list or the software does not set this bit to 1, this bit remains to be 0 and the list processing is stopped. To re-configure the list and start the processing, set the BLE (bit 5) in HcCommand and set this bit before starting the list processing.



Bit	Bit Name	Initial Value	R/W	Description
1	CLF	0	R/W	<p>Control List Filled</p> <p>Indicates whether there are any TDs on the Control list or not.</p> <p>The host logic checks this bit status to start the first ED processing on the Control list.</p> <p>When this bit is 0, the host logic does not start the list processing. When 1, the host logic starts the Control list processing and sets this bit to 0. If the host logic finds a TD on the Control list, this bit is set to 1 and the Control list processing is continued.</p> <p>When the host logic completes the list processing, this bit is cleared to 0. If a TD is not detected in the list or the software does not set this bit to 1, this bit remains to be 0 and the list processing is stopped.</p> <p>To re-configure the list and start the processing, set the CLE (bit 4) in HcCommand and set this bit before starting the list processing.</p>
0	HCR	0	W	<p>Host Controller Reset</p> <p>Initiates the host logic software reset.</p> <p>When this bit is set, a transition to the USB suspend state is made regardless of the functional state of the host logic.</p>

## 51.6.1.4 HcInterruptStatus Register

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	RHSC	FNO	UE	RD	SF	WDH	SO
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 7	—	All 0	R/W	Reserved The write value should be 0.
6	RHSC	0	R/W	Root Hub Status Change This is an interrupt bit that indicates that the HcRhStatus or HcRhPortStatus register status has changed. This bit is set when HcRhStatus or HcRhPortStatus changes by a hardware source. Writing 1 to this bit clears the interrupt. 0: RHSC interrupt has not been generated. 1: RHSC interrupt has been generated.
5	FNO	0	R/W	Frame Number Overflow This is an interrupt bit that indicates that MSB of bits 15 to 0 (FrameNumber) in HcFmNumber has changed. This bit is set after HccaFrameNumber has been updated in the frame where the MSB of the FrameNumber bits changes from 0 to 1 or 1 to 0, Writing 1 to this bit clears the interrupt. 0: FNO interrupt has not been generated. 1: FNO interrupt has been generated.
4	UE	0	R/W	Unrecoverable Error This is an interrupt bit that indicates that a system error not related to the USB has been detected in the PCI bus. Writing 1 to this bit clears the interrupt. 0: UE interrupt has not been generated. 1: UE interrupt has been generated.
3	RD	0	R/W	Resume Detected This is an interrupt bit that indicates that Resume has been detected. This bit is set when it is detected that the device on the USB is asserting the Resume signal. This bit is not set when the USB Resume has been detected by the software. Writing 1 to this bit clears the interrupt. 0: RD interrupt has not been generated. 1: RD interrupt has been generated.

Bit	Bit Name	Initial Value	R/W	Description
2	SF	0	R/W	<p>Start of Frame</p> <p>This is an interrupt bit that indicates that HccaFrameNumber has been updated at the start of each frame.</p> <p>The host logic updates HccaFrameNumber on transmission of SOF packet and sets this bit.</p> <p>Writing 1 to this bit clears the interrupt.</p> <p>0: SF interrupt has not been generated.</p> <p>1: SF interrupt has been generated.</p>
1	WDH	0	R/W	<p>Writeback Done Head</p> <p>This is an interrupt bit that indicates that the host logic has updated the HccaDoneHead contents.</p> <p>The host logic sets this bit immediately after updating the HccaDoneHead, and does not update HccaDoneHead until this bit is cleared.</p> <p>Writing 1 to this bit clears the interrupt.</p> <p>0: WDH interrupt has not been generated.</p> <p>1: WDH interrupt has been generated.</p>
0	SO	0	R/W	<p>Scheduling Overrun</p> <p>This is an interrupt bit that indicates that USB schedule has overrun in the frame. This bit is set after HccaFrameNumber in the next frame has been updated.</p> <p>When this bit is set, the SOC (bits 17 and 16) in HcCommandStatus is also incremented</p> <p>Writing 1 to this bit clears the interrupt.</p> <p>0: SO interrupt has not been generated.</p> <p>1: SO interrupt has been generated.</p>

### 51.6.1.5 HcInterruptEnable Register

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	MIE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	RHSCE	FNOE	UEE	RDE	SFE	WDHE	SOE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	MIE	0	R/W	<p>Master Interrupt Enable</p> <p>Enables interrupt source settings of bits 6 to 0 in this register.</p> <p>When this bit is 0, all the interrupts are masked.</p> <p>To clear this bit, write 1 in the pertinent bit in HcInterruptDisable.</p> <p>0: Ignored</p> <p>1: Interrupt generation settings are enabled</p>
30 to 7	—	All 0	R	<p>Reserved</p> <p>The write value should be 0.</p>
6	RHSCE	0	R/W	<p>Root Hub Status Change Enable</p> <p>Enables interrupt generation by RHSC.</p> <p>Writing 1 to this bit enables the RHSC interrupt</p> <p>To clear this bit, write 1 in the pertinent bit in HcInterruptDisable.</p> <p>0: Ignored.</p> <p>1: RHSC interrupt enabled.</p>
5	FNOE	0	R/W	<p>Frame Number Overflow Enable</p> <p>Enables interrupt generation by FNO.</p> <p>Writing 1 to this bit enables the FNO interrupt</p> <p>To clear this bit, write 1 in the pertinent bit in HcInterruptDisable.</p> <p>0: Ignored.</p> <p>1: FNO interrupt enabled.</p>
4	UEE	0	R/W	<p>Unrecoverable Error Enable</p> <p>Enables interrupt generation by UE.</p> <p>Writing 1 to this bit enables the UE interrupt</p> <p>To clear this bit, write 1 in the pertinent bit in HcInterruptDisable.</p> <p>0: Ignored.</p> <p>1: UE interrupt enabled.</p>
3	RDE	0	R/W	<p>Resume Detected Enable</p> <p>Enables interrupt generation by RD.</p> <p>Writing 1 to this bit enables the RD interrupt</p> <p>To clear this bit, write 1 in the pertinent bit in HcInterruptDisable.</p> <p>0: Ignored.</p> <p>1: RD interrupt enabled.</p>

Bit	Bit Name	Initial Value	R/W	Description
2	SFE	0	R/W	<p>Start of Frame Enable</p> <p>Enables interrupt generation by SF.</p> <p>Writing 1 to this bit enables the SF interrupt</p> <p>To clear this bit, write 1 in the pertinent bit in HcInterruptDisable.</p> <p>0: Ignored.</p> <p>1: SF interrupt enabled.</p>
1	WDHE	0	R/W	<p>Writeback Done Head Enable</p> <p>Enables interrupt generation by WDH.</p> <p>Writing 1 to this bit enables the WDH interrupt</p> <p>To clear this bit, write 1 in the pertinent bit in HcInterruptDisable.</p> <p>0: Ignored.</p> <p>1: WDH interrupt enabled.</p>
0	SOE	0	R/W	<p>Scheduling Overrun Enable</p> <p>Enables interrupt generation by SO.</p> <p>Writing 1 to this bit enables the SO interrupt</p> <p>To clear this bit, write 1 in the pertinent bit in HcInterruptDisable.</p> <p>0: Ignored.</p> <p>1: SO interrupt enabled.</p>

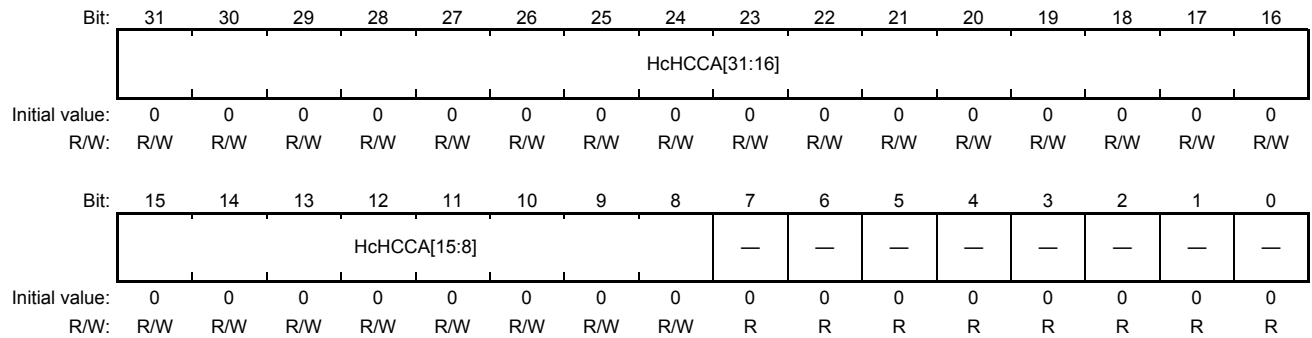
## 51.6.1.6 HcInterruptDisable Register

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	MID	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	RHSCD	FNOD	UED	RDD	SFD	WDHD	SOD
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	MID	0	R/W	<p>Master Interrupt Disable</p> <p>Disables interrupt source settings of bits 6 to 0 in HcInterruptEnable.</p> <p>When this bit is 0, all the interrupts are masked.</p> <p>Writing 1 to this bit clears bits 6 to 0 in HcInterruptEnable.</p> <p>To set the interrupt generation to be enabled, write 1 in the pertinent bit in HcInterruptEnable.</p> <p>0: Ignored</p> <p>1: Interrupt generation settings are disabled</p>
30 to 7	—	0	R	<p>Reserved</p> <p>The write value should be 0.</p>
6	RHSCD	0	R/W	<p>Root Hub Status Change Disable</p> <p>Removes RHSC from interrupt sources.</p> <p>Writing 1 to this bit clears the RHSC interrupt setting.</p> <p>To set RHSC as an interrupt source, write 1 in the pertinent bit in HcInterruptEnable.</p> <p>0: Ignored</p> <p>1: RHSC is removed from interrupt sources.</p>
5	FNOD	0	R/W	<p>Frame Number Overflow Disable</p> <p>Removes FNO from interrupt sources.</p> <p>Writing 1 to this bit clears the FNO interrupt setting.</p> <p>To set FNO as an interrupt source, write 1 in the pertinent bit in HcInterruptEnable.</p> <p>0: Ignored</p> <p>1: FNO is removed from interrupt sources.</p>
4	UED	0	R/W	<p>Unrecoverable Error Disable</p> <p>Removes UE from interrupt sources.</p> <p>Writing 1 to this bit clears the UE interrupt setting.</p> <p>To set UE as an interrupt source, write 1 in the pertinent bit in HcInterruptEnable.</p> <p>0: Ignored</p> <p>1: UE is removed from interrupt sources.</p>

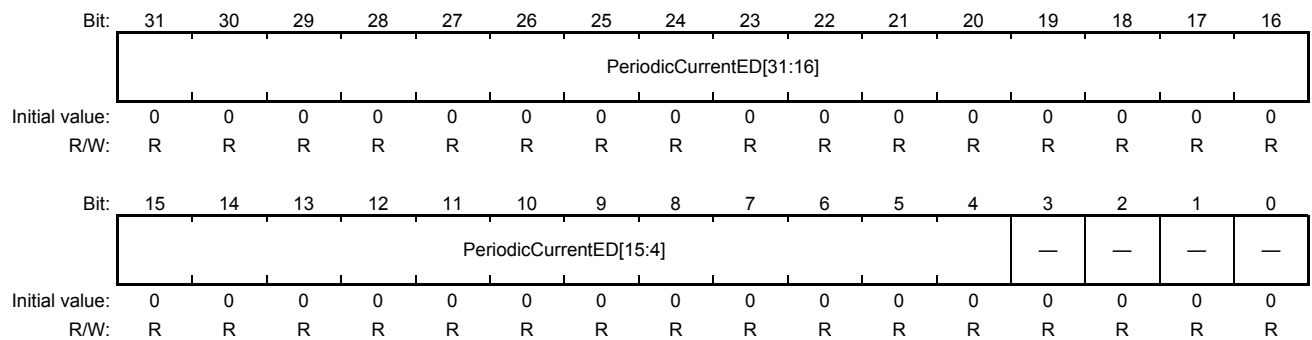
Bit	Bit Name	Initial Value	R/W	Description
3	RDD	0	R/W	<p>Resume Detected Disable</p> <p>Removes RD from interrupt sources.</p> <p>Writing 1 to this bit clears the RD interrupt setting.</p> <p>To set RD as an interrupt source, write 1 in the pertinent bit in HcInterruptEnable.</p> <p>0: Ignored</p> <p>1: RD is removed from interrupt sources.</p>
2	SFD	0	R/W	<p>Start of Frame Disable</p> <p>Removes SF from interrupt sources.</p> <p>Writing 1 to this bit clears the SF interrupt setting.</p> <p>To set SF as an interrupt source, write 1 in the pertinent bit in HcInterruptEnable.</p> <p>0: Ignored</p> <p>1: SF is removed from interrupt sources.</p>
1	WDHD	0	R/W	<p>Writeback Done Head Disable</p> <p>Removes WDH from interrupt sources.</p> <p>Writing 1 to this bit clears the WDH interrupt setting.</p> <p>To set WDH as an interrupt source, write 1 in the pertinent bit in HcInterruptEnable.</p> <p>0: Ignored</p> <p>1: WDH is removed from interrupt sources.</p>
0	SOD	0	R/W	<p>Scheduling Overrun Disable</p> <p>Removes SO from interrupt sources.</p> <p>Writing 1 to this bit clears the SO interrupt setting.</p> <p>To set SO as an interrupt source, write 1 in the pertinent bit in HcInterruptEnable.</p> <p>0: Ignored</p> <p>1: SO is removed from interrupt sources.</p>

### 51.6.1.7 HcHCCA Register



Bit	Bit Name	Initial Value	R/W	Description
31 to 8	HcHCCA[31:8]	H'00 0000	R/W	Sets the base address of RAM allocated as the Host Controller Communication Area.  Set these bits during initialization. The host logic requires 256 bytes of area for HCCA from this base address.
7 to 0	—	All 0	R	Reserved  The write value should be 0.

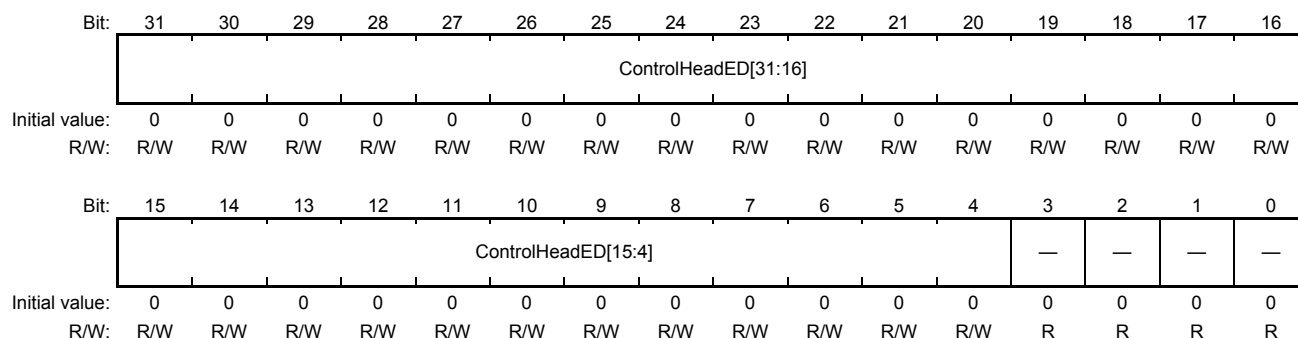
### 51.6.1.8 HcPeriodicCurrentED Register



Bit	Bit Name	Initial Value	R/W	Description
31 to 4	PeriodicCurrent ED[31:4]	H'000 0000	R	Indicates the physical address of the ED currently processed in the Periodic list.  The host logic updates these bits on completion of the list processing of the ED.
3 to 0	—	All 0	R	Reserved  The write value should be 0.

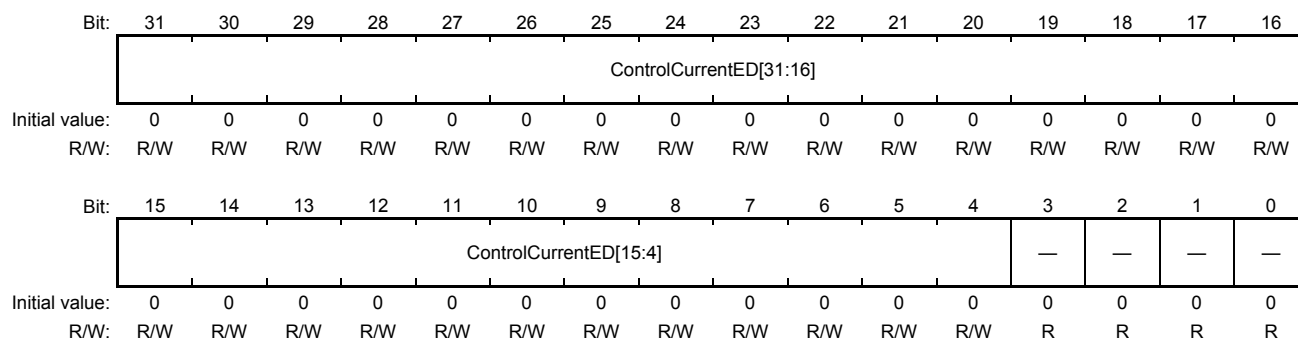


### 51.6.1.9 HcControlHeadED Register



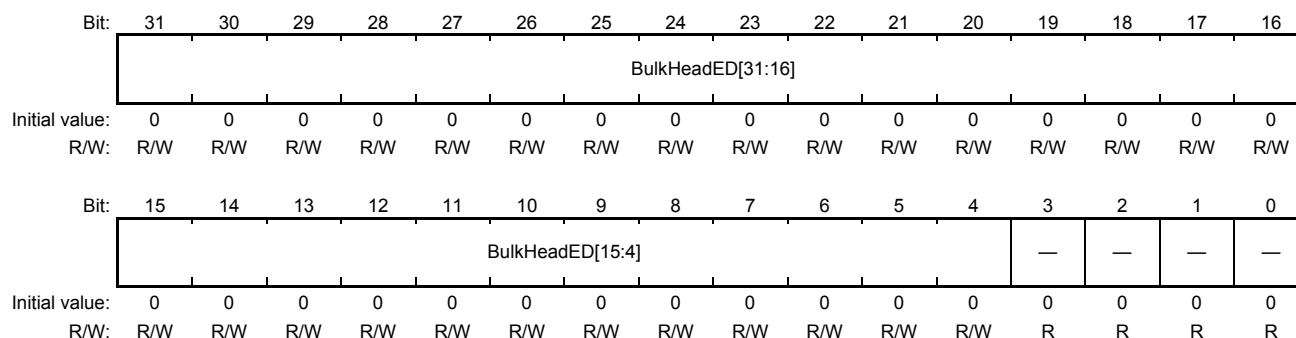
Bit	Bit Name	Initial Value	R/W	Description
31 to 4	ControlHeadED [31:4]	H'000 0000	R/W	Sets the physical address of the first ED in the Control list. To perform Control transfer, set these bits before setting the CLE (bit 4) in HcControl.
3 to 0	—	All 0	R	Reserved The write value should be 0.

### 51.6.1.10 HcControlCurrentED Register



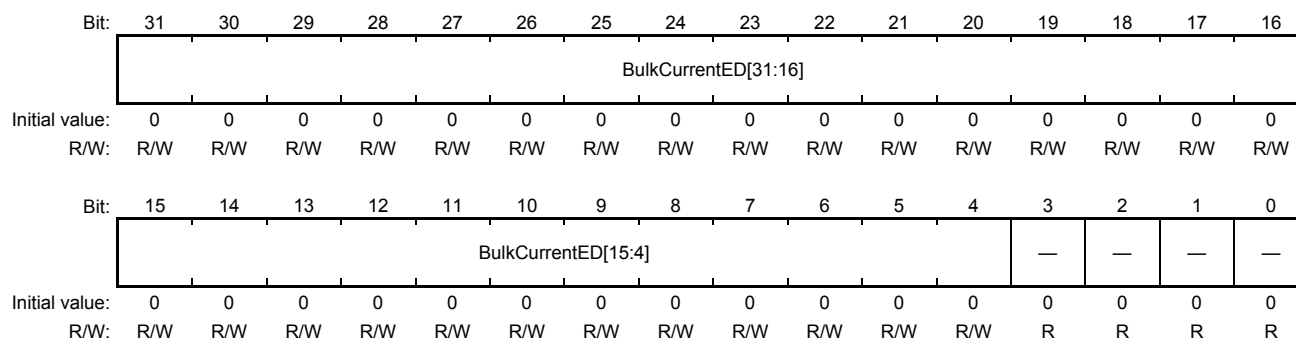
Bit	Bit Name	Initial Value	R/W	Description
31 to 4	ControlCurrent ED[31:4]	H'000 0000	R/W	Indicates the physical address of the ED currently processed in the Control list. The host logic updates these bits on each completion of the Control ED processing. To newly configure the list, set these bits to H'00000000 that indicates the list end. To stop the transfer and restart it, check to see that the ED indicated by the ControlCurrentED link pointer exists.
3 to 0	—	All 0	R	Reserved The write value should be 0.

### 51.6.1.11 HcBulkHeadED Register



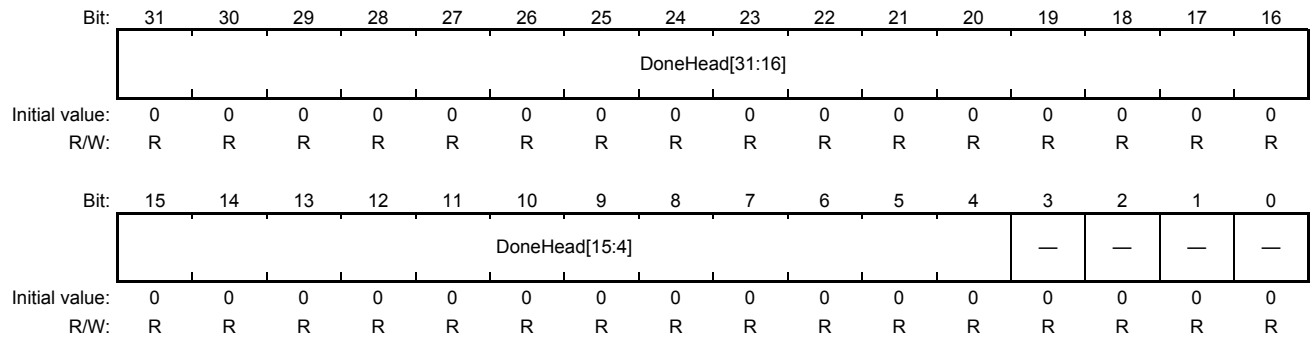
Bit	Bit Name	Initial Value	R/W	Description
31 to 4	BulkHeadED [31:4]	H'000 0000	R/W	Sets the physical address of the first ED in the Bulk list. To perform Bulk transfer, set these bits before setting the BLE (bit 5) in HcControl.
3 to 0	—	All 0	R	Reserved The write value should be 0.

### 51.6.1.12 HcBulkCurrentED Register



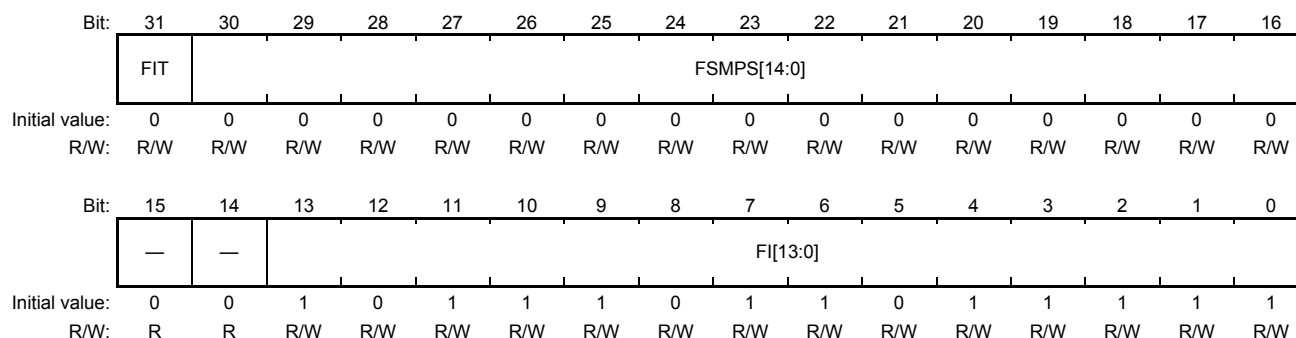
Bit	Bit Name	Initial Value	R/W	Description
31 to 4	BulkCurrentED [31:4]	H'000 0000	R/W	Indicates the physical address of the ED currently processed in the Bulk list. The host logic updates these bits on each completion of the Bulk ED processing. To newly configure the list, set these bits to H'00000000 that indicates the list end. To stop the transfer and restart it, check to see that the ED indicated by the BulkCurrentED link pointer exists.
3 to 0	—	All 0	R	Reserved The write value should be 0.

**51.6.1.13 HcDoneHead Register**



Bit	Bit Name	Initial Value	R/W	Description
31 to 4	DoneHead [31:4]	H'000 0000	R	Indicates the physical address of HcDoneHead of the host logic. The physical address of the last completed TD that was added to the Done queue is indicated.
3 to 0	—	All 0	R	Reserved The write value should be 0.

## 51.6.1.14 HcFmInterval Register



Bit	Bit Name	Initial Value	R/W	Description
31	FIT	0	R/W	<p>Frame Interval Toggle</p> <p>This bit is used for synchronization of the frame settings between the software and host logic.</p> <p>This bit should be toggled by the software when the FI bit is updated.</p> <p>The host logic sets this bit value to the FRT (bit 31) in HcFmRemaining when the FI bit is loaded. By comparing this bit value that is set on the write of the FI bit with the read FRT bit value, whether or not a new FI bit is reflected can be checked by the software.</p>
30 to 16	FSMPS[14:0]	H'0000	R/W	<p>FS Largest Data Packet</p> <p>Sets the largest amount data to be transmitted or received without causing a schedule overrun. By comparing the current frame position with the setting value, to which frame the transfer can be performed is determined. Since the data amount differs depending on system bus capability, these bits are set by the driver.</p>
15, 14	—	All 0	R	<p>Reserved</p> <p>The write value should be 0.</p>
13 to 0	FI[13:0]	H'2EDF	R/W	<p>Frame Interval</p> <p>Sets the frame length (bit time) used in a FS transfer.</p> <p>Set H'2EDF to satisfy one frame (= 1ms) defined by the USB standard.</p>

**51.6.1.15 HcFmRemaining Register**

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	FRT	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	FR[13:0]													
Initial value:	0	0	1	0	1	1	1	0	1	1	0	1	1	1	1	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

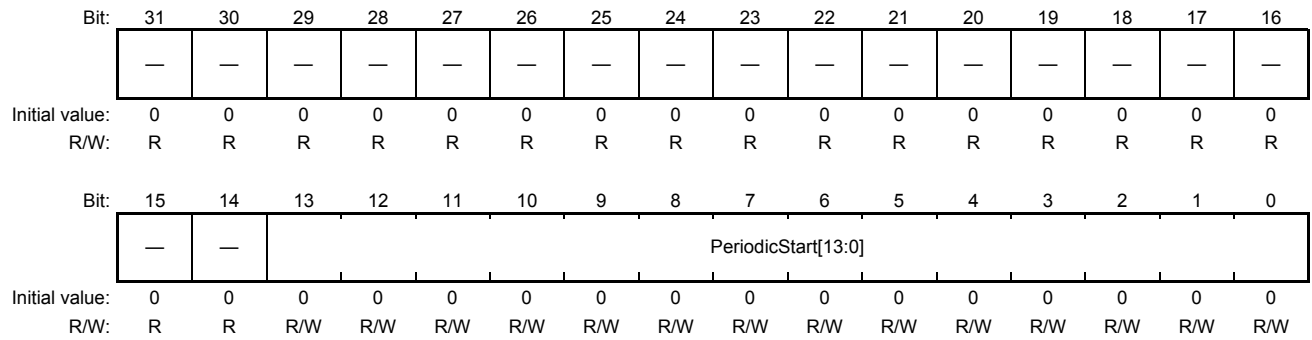
Bit	Bit Name	Initial Value	R/W	Description
31	FRT	0	R	<p>Frame Remaining Toggle</p> <p>This bit is used for synchronization of the frame settings between the software and host logic.</p> <p>When the FR bit reaches H'0000, the host logic copies the FI value (bits 13 to 0) in HcFmInterval into the FR bit, and also copies the FIT value (bit 31) in HcFmInterval into this bit.</p> <p>By comparing the FIT bit value with this bit value, whether the new FI value is set in the FR bit can be checked by the software.</p>
30 to 14	—	All 0	R	Reserved (Don't care)
13 to 0	FR[13:0]	H'2EDF	R	<p>Frame Remaining</p> <p>Indicates the current frame value in the 14-bit down counter.</p> <p>This bit is decremented as the time elapses.</p> <p>When these bits reach H'0000, the value of the FI (bits 13 to 0) in HcFmInterval is copied into these bits to re-load the frame value, and counting is restarted.</p>

**51.6.1.16 HcFmNumber Register**

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FrameNumber[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

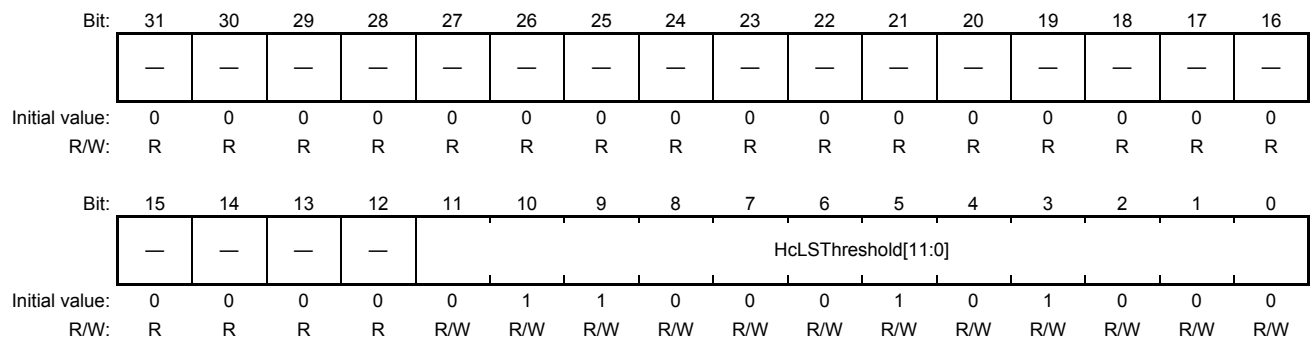
Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved (Don't care)
15 to 0	FrameNumber [15:0]	H'0000	R	<p>Indicates the number of frames elapsed.</p> <p>When the FR (bits 13 to 0) in HcFmRemaining reaches H'0000, these bits are incremented.</p>

**51.6.1.17 HcPeriodicStart Register**



Bit	Bit Name	Initial Value	R/W	Description
31 to 14	—	All 0	R	Reserved The write value should be 0.
13 to 0	PeriodicStart [13:0]	H'0000	R/W	Indicates the time when the host logic should start periodic list processing in the frame.  This bit value should be set in the host logic initialization by the software. If the value of the FR (bits 13 to 0) in HcFmRemaining is larger than the set value, NonPeriodic list takes priority over Periodic list.  These bits are recommended to be set to the value approximately 90% of the FI (bits 13 to 0) in HcFmInterval by the OHCI standard. Thus, the recommended value is H'2A2F.

**51.6.1.18 HcLSThreshold Register**



Bit	Bit Name	Initial Value	R/W	Description
31 to 12	—	All 0	R	Reserved The write value should be 0.
11 to 0	HcLSThreshold [11:0]	H'628	R/W	These bits are used to determine whether or not the transfer can be performed in the remaining frame time during LS transfer.  If the FmRemaining value is larger than this value, LS transfer can be started.

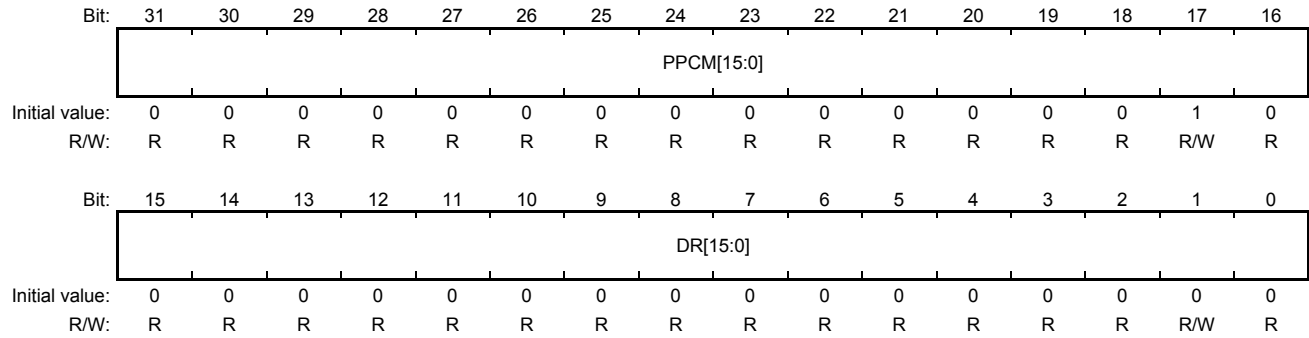
## 51.6.1.19 HcRhDescriptorA Register

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	POTPGT[7:0]								—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	NOCP	OCPM	DT	NPS	PSM	NDP[7:0]							
Initial value:	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	1
R/W:	R	R	R	R/W	R/W	R	R/W	R/W	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	POTPGT[7:0]	H'0F	R/W	Power On To Power Good Time Sets the wait time from power supply to the root-hub port to access by the software. The time unit is 2ms. Thus, the wait time is calculated as POTPGT × 2ms.
23 to 13	—	All 0	R	Reserved The write value should be 0.
12	NOCP	0	R/W	No Over Current Protection Module Specifies whether to support the root-hub overcurrent function. 0: Overcurrent status supported. 1: Overcurrent status not supported.
11	OCPM	1	R/W	Over Current Protection Mode Specifies how to notify the root-hub overcurrent status. This bit should indicate the same mode as the PSM bit. This bit is only valid when the NOCP bit is cleared. 0: Overcurrent status is notified collectively for all the ports. 1: Overcurrent status is notified for each port.
10	DT	0	R	Device Type Indicates that the root-hub is not a composite device. This bit is always read as 0 since the root-hub is not permitted to be a composite device.
9	NPS	0	R/W	No Power Switching Specifies the port power supply control method. 0: Port power can be switched on or off. 1: Port power is always on during host logic operation.
8	PSM	1	R/W	Power Switching Mode Specifies how to control the power switching of each root-hub port. The port responds only to the Set/ClearPortPower when the PPCM (bits 31 to 16) in HcRhDescriptorB is set. When PPCM is cleared, the power switching is controlled by Set/ClearGlobalPower. This bit is only valid when the NPS bit is cleared. 0: All the ports are powered on or off at the same time. 1: Ports are powered on or off individually.

Bit	Bit Name	Initial Value	R/W	Description
7 to 0	NDP[7:0]	H'00	R	Number Downstream Port Specifies the number of down-stream ports supported by the host logic root-hub.

**51.6.1.20 HcRhDescriptorB Register**



Bit	Bit Name	Initial Value	R/W	Description															
31 to 16	PPCM[15:0]	H'0002	R/W	Port Power Control Mask Sets the power supply control command for each port. These bits are valid when the PSM (bit 8) in HcRhDescriptorA is set. Each bit is dedicated to a port. Only port 1 is available in this module. <table border="1"> <thead> <tr> <th>Bit</th> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>—</td> <td>Reserved</td> </tr> <tr> <td>1</td> <td>0:</td> <td>All the ports are collectively controlled (Set/ClearGlobalPower).</td> </tr> <tr> <td></td> <td>1:</td> <td>Port 1 is individually controlled (Set/ClearPortPower).</td> </tr> <tr> <td>[15:2]</td> <td>—</td> <td>Reserved</td> </tr> </tbody> </table>	Bit	Value	Description	0	—	Reserved	1	0:	All the ports are collectively controlled (Set/ClearGlobalPower).		1:	Port 1 is individually controlled (Set/ClearPortPower).	[15:2]	—	Reserved
Bit	Value	Description																	
0	—	Reserved																	
1	0:	All the ports are collectively controlled (Set/ClearGlobalPower).																	
	1:	Port 1 is individually controlled (Set/ClearPortPower).																	
[15:2]	—	Reserved																	
15 to 0	DR[15:0]	H'0000	R/W	Device Removable Sets whether each root-hub port is removable or not. Each bit is dedicated to a port. Only port 1 is available in this module. <table border="1"> <thead> <tr> <th>Bit</th> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>—</td> <td>Reserved</td> </tr> <tr> <td>1</td> <td>0:</td> <td>A device connected to port 1 is not removable.</td> </tr> <tr> <td></td> <td>1:</td> <td>A device connected to port 1 is removable.</td> </tr> <tr> <td>[15:2]</td> <td>—</td> <td>Reserved</td> </tr> </tbody> </table>	Bit	Value	Description	0	—	Reserved	1	0:	A device connected to port 1 is not removable.		1:	A device connected to port 1 is removable.	[15:2]	—	Reserved
Bit	Value	Description																	
0	—	Reserved																	
1	0:	A device connected to port 1 is not removable.																	
	1:	A device connected to port 1 is removable.																	
[15:2]	—	Reserved																	



**51.6.1.21 HcRhDescriptorA Register**

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CRWE	—	—	—	—	—	—	—	—	—	—	—	—	—	OCIC	LPSC/SGP
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	W	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DRWE/SRWE	—	—	—	—	—	—	—	—	—	—	—	—	—	OCI	LPS/CGP
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description																				
31	CRWE	0	W	Clear Remote Wakeup Enable Clears the DRWE bit. Setting this bit clears the DRWE bit. Writing 0 has no effect.																				
30 to 18	—	All 0	R	Reserved The write value should be 0.																				
17	OCIC	0	R/W	Over Current Indicate Change Indicates that the OCI bit has changed. This bit is set to 1 when a change occurs in the OCI bit. This bit can be cleared by writing 1 while this bit is set. Writing 0 has no effect. 0: Overcurrent status has not changed. 1: Overcurrent status has changed																				
16	LPSC	0	R/W	Local Power Status Change This bit is always read as 0 because LocalPowerStatus is not supported.																				
	SGP	0	R/W	Set Global Power Setting this bit to 1 turns on power to the pertinent ports. The ports to be powered on are determined by the PSM (bit 8) in HcRhDescriptorA and PPCM (bits 31 to 16) in HcRhDescriptorB. Only port 1 is available in this module.																				
				<table border="1"> <thead> <tr> <th>Value</th> <th>PSM</th> <th>PPCM[1]</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>—</td> <td>—</td> <td>No Change</td> </tr> <tr> <td>1</td> <td>0</td> <td>—</td> <td>PPS in HcRhPortStatus1 is set.</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>PPS in HcRhPortStatus1 is set.</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>No Change</td> </tr> </tbody> </table>	Value	PSM	PPCM[1]	Description	0	—	—	No Change	1	0	—	PPS in HcRhPortStatus1 is set.	1	1	0	PPS in HcRhPortStatus1 is set.	1	1	1	No Change
Value	PSM	PPCM[1]	Description																					
0	—	—	No Change																					
1	0	—	PPS in HcRhPortStatus1 is set.																					
1	1	0	PPS in HcRhPortStatus1 is set.																					
1	1	1	No Change																					

Bit	Bit Name	Initial Value	R/W	Description																			
15	DRWE	0	R/W	<p>Device Remote Wakeup Enable</p> <p>Sets whether to enable the CSC (bit 16) in HcRhPortStatus 1 as the RemoteWakeup event.</p> <p>If the ConnectStatusChange event occurs while this bit is 1, a transition is made from USB Suspend to USB Resume and the Resume Detect interrupt occurs.</p> <p>0: ConnectStatusChange is not a RemoteWakeup source. 1: ConnectStatusChange is a RemoteWakeup source.</p>																			
	SRWE	0	R/W	<p>Set Remote Wakeup Enable</p> <p>Sets the DRWE bit.</p> <p>Setting this bit sets the DRWE bit.</p> <p>Writing 0 has no effect.</p>																			
14 to 2	—	All 0	R	<p>Reserved</p> <p>The write value should be 0.</p>																			
1	OCI	0	R	<p>Over Current Indicator</p> <p>Notifies the overcurrent status in global overcurrent detection mode.</p> <p>When the overcurrent notification for individual port is set, this bit is always 0.</p> <p>0: Normal 1: Overcurrent</p>																			
0	LPS	0	R/W	<p>Local Power Status</p> <p>This bit is always read as 0 because LocalPowerStatus is not supported.</p>																			
	CGP	0	R/W	<p>Clear Global Power</p> <p>Setting this bit to 1 turns off power to the pertinent ports.</p> <p>The ports to be powered off are determined by the PSM (bit 8) in HcRhDescriptorA and PPCM (bits 31 to 16) in HcRhDescriptorB.</p> <p>Only port 1 is available in this module.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>PSM</th> <th>PPCM[1]</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>—</td> <td>—</td> <td>No Change</td> </tr> <tr> <td>1</td> <td>0</td> <td>—</td> <td>PPS in HcRhPortStatus1 is cleared.</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>PPS in HcRhPortStatus1 is cleared.</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>No Change</td> </tr> </tbody> </table>	Value	PSM	PPCM[1]	Description	0	—	—	No Change	1	0	—	PPS in HcRhPortStatus1 is cleared.	1	1	0	PPS in HcRhPortStatus1 is cleared.	1	1	1
Value	PSM	PPCM[1]	Description																				
0	—	—	No Change																				
1	0	—	PPS in HcRhPortStatus1 is cleared.																				
1	1	0	PPS in HcRhPortStatus1 is cleared.																				
1	1	1	No Change																				

## 51.6.1.22 HcRhPortStatus1 Register

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	PRSC	OCIC	PSSC	PESC	CSC
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	LSDA/ CPP	PPS/ SPP	—	—	—	PRS/ SPR	POCI/ CSS	PSS/ SPS	PES/ SPE	CCS/ CPE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 21	—	All 0	R	Reserved The write value should be 0.
20	PRSC	0	R/W	Port Reset Status Change Indicates that a port reset is completed. This bit is set to 1 on completion of the 10-ms hardware reset by the host logic. Writing 1 by the software clears this bit. 0: Port reset not completed or PRS not changed 1: Port reset completed
19	OCIC	0	R/W	Over Current Indicate Change This bit is set when the port overcurrent status has been detected. This bit is only valid when the overcurrent status notification for individual port is set (OCPM in HcRhDescriptorA = 1). Writing 1 by the software clears this bit. 0: Overcurrent status not changed 1: Overcurrent status changed
18	PSSC	0	R/W	Port Suspend Status Change Indicates that RESUME sequence is completed. This bit is set to 1 on completion of all of the RESUME processings by the hardware. Writing 1 by the software clears this bit. This bit is cleared when the PRSC bit is set. 0: RESUME processing not completed 1: RESUME processing completed
17	PESC	0	R/W	Port Enable Status Change Indicates that the PES bit has changed. This bit is set when the port status has changed due to a hardware event such as an overcurrent status, disconnection, power-off, and babble error. Writing 1 by the software clears this bit. 0: PES status not changed 1: PES status changed

Bit	Bit Name	Initial Value	R/W	Description
16	CSC	0	R/W	<p>Connect Status Change</p> <p>Indicates that the CCS bit has changed.</p> <p>This bit is set by the host logic when the CCS bit has changed by the device connection or disconnection.</p> <p>When a port reset, port suspend, or port enable is requested during disconnection, this bit is also set to re-evaluate the device connection status by the software.</p> <p>Writing 1 by the software clears this bit.</p> <p>0: CCS status not changed 1: CCS status changed</p>
15 to 10	—	All 0	R	<p>Reserved</p> <p>The write value should be 0.</p>
9	LSDA	0	R/W	<p>Low Speed Device Attached</p> <p>Indicates the speed of the device connected to the port.</p> <p>This status bit is only valid when the CCS bit is set.</p> <p>0: FS device is connected. 1: LS device is connected.</p>
	CPP	0	R/W	<p>Clear Port Power</p> <p>This bit is used to turn off power to the port when power control for individual port is set.</p> <p>Writing 1 turns off power to the port. Writing 0 has no effect.</p>
8	PPS	0	R/W	<p>Port Power Status</p> <p>Indicates the port power supply status.</p> <p>This bit is cleared when an overcurrent status has been detected.</p> <p>0: Port power off 1: Port power on</p>
	SPP	0	R/W	<p>Set Port Power</p> <p>This bit is used to turn on power to the port when power control for individual port is set.</p> <p>Writing 1 turns on power to the port. Writing 0 has no effect.</p>
7 to 5	—	All 0	R	<p>Reserved</p> <p>The write value should be 0.</p>
4	PRS	0	R/W	<p>Port Reset Status</p> <p>Indicates the port reset status.</p> <p>This bit is cleared when the PRSC bit is set on completion of a 10-ms port reset.</p> <p>When the CCS bit is cleared (device disconnected), this bit cannot be set.</p> <p>0: Port reset not performed 1: Port reset in progress</p>
	SPR	0	R/W	<p>Set Power Reset</p> <p>Issues the port reset to the down-stream port.</p> <p>Writing 1 to this bit initiates the 10-ms port reset. If this bit is written to when the CCS bit is cleared, the PRS bit cannot be written to. At this time, the CSC bit is set to notify the software of the attempt of resetting the port to which no device is connected.</p> <p>Writing 0 has no effect.</p>

Bit	Bit Name	Initial Value	R/W	Description
3	POCI	0	R/W	<p>Port Over Current Indicator</p> <p>Indicates that the down-stream port is in the overcurrent status.</p> <p>This bit is only valid when the overcurrent status notification for individual port is set (OCPM in HcRhDescriptorA is 1). When the collective overcurrent status notification for all the ports is set, this bit is set to 0.</p> <p>0: Normal status 1: Overcurrent status</p>
	CSS	0	R/W	<p>Clear Suspend Status</p> <p>Terminates the Suspend status and activates the Resume sequence.</p> <p>Writing 1 activates the Resume sequence. Writing 0 has no effect. The Resume sequence is activated only when the PSS bit is set.</p>
2	PSS	0	R/W	<p>Port Suspend Status</p> <p>Indicates that the port is in the Suspend status or in the Resume sequence.</p> <p>This bit is set by writing to the SPS bit.</p> <p>This bit cannot be set when the CCS bit is 0 (device disconnected).</p> <p>This bit is cleared when:</p> <ul style="list-style-type: none"> <li>the Resume sequence is completed and PSSC bit is set.</li> <li>the port reset is completed and the PRSC bit is set.</li> <li>the port is in USB RESUME state.</li> </ul> <p>0: Normal transfer state 1: Suspend state</p>
	SPS	0	R/W	<p>Set Port Suspend</p> <p>Causes the port state transition to the Suspend state.</p> <p>When 1 is written to this bit, the port state is transitioned to the Suspend state. Writing 0 has no effect.</p> <p>If this bit is written to when the CCS bit is cleared, the CSC bit is set to notify the driver of the attempt of suspending a disconnected port.</p>
1	PES ( )	0	R/W	<p>Port Enable Status</p> <p>Indicates whether the port is enabled or disabled.</p> <p>When the overcurrent state, disconnection, power-off, babble error is detected, this bit is automatically cleared by the host logic and the PES bit is set.</p> <p>This bit cannot be set when the CCS bit is 0 (device disconnected).</p> <p>The host logic sets this bit on completion of a port reset or a suspend state.</p> <p>0: Disabled 1: Enabled</p>
	SPE	0	R/W	<p>Set Port Enable</p> <p>Sets the PES bit.</p> <p>Writing 1 sets the port to be enabled. Writing 0 has no effect.</p> <p>Note: The port state transition should be made using the SPR (bit 4) in HcRhPortStatus1. Port state transition to Enable by the SPE bit is supported by the OHCI standard, but not supported by the USB standard.</p>

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Bit	Bit Name	Initial Value	R/W	Description
0	CCS	0	R/W	Current Connect Status Indicates the current connection state of the down-stream port. 0: Device not connected 1: Device connected
	CPE	0	R/W	Clear Port Enable Clears the PES bit. Writing 1 makes the port transition to Disable. Writing 0 has no effect.

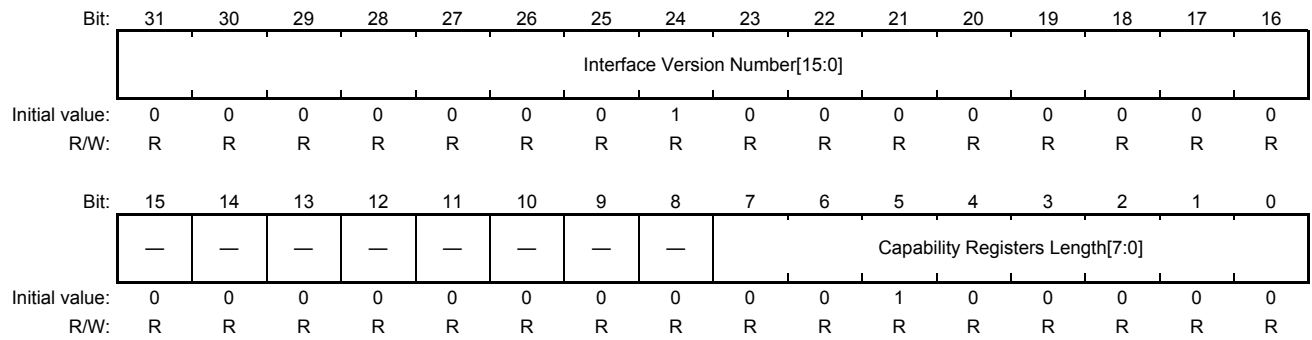
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### 51.6.2 EHCI Operational Registers

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Please refer to the EHCI standard for the details of the EHCI register. The meaning follows the EHCI standard.

#### 51.6.2.1 HCIVERSION/CAPLENGTH Register



Bit	Bit Name	Initial Value	R/W	Description
31 to 16	Interface Version Number[15:0]	H'0100	R	Indicates the EHCI standard version supported by the host logic. The set value H'0100 indicates that the host logic complies with EHCI Rev.1.0.
15 to 8	—	All 0	R	Reserved (Don't care)
7 to 0	Capability Registers Length[7:0]	H'20	R	Indicates the start address of the operational register area. The set value H'20 indicates that the operational register area is started at H'20.

## 51.6.2.2 HCSPARAMS Register

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	DPN[3:0]			—	—	—	P_INDICATOR	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	N_CC[3:0]			N_PCC[3:0]				PRR	—	—	PPC	N_PORTS[3:0]				
Initial value:	0	0	0	1	0	0	0	1	1	0	0	1	0	0	0	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved (Don't care)
23 to 20	DPN[3:0]	0000	R	Debug Port Number Indicates a debugging port. The set value is B'0000 since the host logic does not support a debugging port.
19 to 17	—	All 0	R	Reserved (Don't care)
16	P_INDICATOR	0	R	Indicates whether or not the host logic supports the port indicator control function. The set value is 0 since the host logic does not support the port indicator control function.
15 to 12	N_CC[3:0]	H'1	R	Number of Companion Controller Indicates the number of OHCI host logics related to the EHCI host logic. The set value is H'1 since one OHCI host logic is incorporated.
11 to 8	N_PCC[3:0]	H'1	R	Number of Ports per Companion Controller Indicates the number of ports supported by one OHCI host logic. These bits are set according to the Port_no (bits 1 and 0) setting in PCI Configuration EXT1. The set value is H'1 since one port is supported.
7	PRR	1	R	Port Routing Rules Indicates how the ports are mapped by the OHCI host logic. The set value is H'1 since the ports are mapped according to the HCSP_PORTROUTE register setting.
6, 5	—	All 0	R	Reserved (Don't care)
4	PPC	1	R	Port Power Control Indicates how the port power is controlled. This bit is set according to the Ppcnt (bit 2) setting in PCI Configuration EXT1. The set value is 1 since the power supply control is supported by this module.



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Bit	Bit Name	Initial Value	R/W	Description
3 to 0	N_PORTS [3:0]	H'1	R	<p>Number of ports</p> <p>Indicates the number of down-stream ports. The set value is 1h since one port is supported.</p> <p>The number of physical down-stream ports used by the host logic is indicated.</p> <p>These bits change according to the Port_no (bits 1 and 0) setting in PCI Configuration EXT1.</p> <p>The set value is H'1 since one port is supported.</p>

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## 51.6.2.3 HCCPARAMS Register

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EECP[7:0]							IST[3:0]				—	ASPC	PFLF	64AC	
Initial value:	1	1	1	0	1	0	0	0	0	0	0	0	0	1	1	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved (Don't care)
15 to 8	EECP[7:0]	H'E8	R	EHCI Extend Capabilities Pointer Indicates the offset address for the EHCI extend capabilities registers. These bits indicate that an extend register exists on H'E8 in the EHCI configuration space. The read value is invalid since the legacy function is not supported by the host logic.
7 to 4	IST[3:0]	H'0	R	Isochronous Scheduling Threshold The set value is H'0 since the host logic does not support the cache mode for isochronous schedule data for the whole frame.
3	—	0	R	Reserved (Don't care)
2	ASPC	1	R	Asynchronous Schedule Park Capability Indicates whether or not the park mode function is supported for high-speed queue heads in asynchronous schedules. The set value is 1 since the park mode function is supported by the host logic.
1	PFLF	1	R	Programming Frame List Flag Indicates how the size of the frame list to be used by the software is set. The set value is 1. When this bit is 1, the frame list size can be set with the FLS (bits 3 and 2) in the USBCMD register, which allows the setting of 4-kbyte or less frame list size.
0	64AC	0	R	64-bit Addressing Capability Indicates whether the data structure uses the 32-bit or 64-bit address memory pointer. The set value is 0 since the 32-bit address memory pointer is used in this host logic data structure. The 64-bit address memory pointer is not supported by this host logic.

### 51.6.2.4 HCSP\_PORTROUTE Register

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Companion Port Route[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Companion Port Route[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	Companion Port Route [31:0]	All 0	R	Indicates the correspondence between the ports and OHCI host logics. The set value is all 0 since one OHCI host logic is incorporated in this host logic.

### 51.6.2.5 USBCMD Register

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
	—	—	—	—	—	—	—	—	ITC[7:0]								—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0		
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
	—	—	—	—	ASPME	—	ASPMC[1:0]	LHCR	IAAD	ASE	PSE	FLS[1:0]	HC RESET	RS	—	—		
Initial value:	0	0	0	0	1	0	1	1	0	0	0	0	0	0	0	0		
R/W:	R	R	R	R	R/W	R	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W		

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved The write value should be 0.
23 to 16	ITC[7:0]	H'08	R/W	Interrupt Threshold Control Specifies the maximum rate for interrupts generated by the host logic. If a value other than below is set, the operation cannot be guaranteed. H'00: Reserved H'01: 1 microframe H'02: 2 microframes H'04: 4 microframes H'08: 8 microframes (1 ms) H'10: 16 microframes (2 ms) H'20: 32 microframes (4 ms) H'40: 64 microframes (8 ms)
15 to 12	—	All 0	R	Reserved The write value should be 0.

Bit	Bit Name	Initial Value	R/W	Description
11	ASPME	1	R/W	Asynchronous Schedule Park Mode Enable Enables or disables park mode. 0: Park mode is disabled. 1: Park mode is enabled
10	—	All 0	R	Reserved The write value should be 0.
9, 8	ASPMC[1:0]	11	R/W	Asynchronous Schedule Park Mode Count Specifies the number of transactions that can be executed continuously from one QH. The settable range is from H'1 to H'3. These bits are valid when the ASPME (bit 11) is 1.
7	LHCR	0	R/W	Light Host Controller Reset Indicates the execution status of the Light Host Controller Reset command. This bit is fixed to 0 since Light Host Controller Reset is not supported by this host logic.
6	IAAD	0	R/W	Interrupt on Async Advance Doorbell This bit is used as a doorbell by the software. The software sets this bit to 1 to generate an interrupt on a transition to the next QH processing. When the IAAE (bit 5) in USBINTR is 1, the interrupt is generated in the next interrupt timing after this bit is set to 1. If this bit is set when IAAE bit is 0, the operation cannot be guaranteed. This bit is cleared by the host logic. The host logic clears this bit to 0 on completion of one QH processing and sets the IAA (bit 5) in USBSTS to 1.
5	ASE	0	R/W	Asynchronous Schedule Enable Specifies that the host logic executes or skips asynchronous list processing. 0: Asynchronous list processing is not executed (skipped). 1: Asynchronous list processing is executed using the ASYNCLISTADDR register.
4	PSE	0	R/W	Periodic Schedule Enable Specifies that the host logic executes or skips periodic list processing. 0: Periodic list processing is not executed (skipped). 1: Periodic list processing is executed using the PERIODICLISTBASE register.
3, 2	FLS[1:0]	00	R/W	Frame List Size Specifies the frame list size. The size of Frame List Current index of FRINDEX is determined depending on the frame list size specified with this field. 00: 1024 elements (4096 bytes) 01: 512 elements (2048 bytes) 10: 256 elements (1024 bytes) 11: Reserved

Bit	Bit Name	Initial Value	R/W	Description
1	HCRESET	0	R/W	<p>Host Controller Reset</p> <p>Resets the host logic.</p> <p>When this bit is set to 1, the host logic resets the internal pipeline and state machine and sets the initial value. In addition, the host logic immediately terminates communication on the USB. At this time, the USB reset is not issued to the down-stream port.</p> <p>Although the resetting does not initialize the PCI configuration registers, the EHCI operation registers are reset to their initial value. The ownership of the port is returned to the OHCI.</p> <p>This bit is automatically cleared to 0 by the host logic upon completion of the resetting operation. During the resetting process, software cannot clear this bit and interrupt the resetting process.</p> <p>This bit should be set when the HCH (bit 12) in USBSTS is 1.</p>
0	RS	0	R/W	<p>Run/Stop</p> <p>Controls the ON/OFF action of the EHCI host logic.</p> <p>Setting this bit to 1 starts the host logic operation.</p> <p>While the bit is 1, the host logic continues execution.</p> <p>This bit should be set to 1 while the host logic is in the halt state.</p> <p>The HCH (bit 12) in USBSTS indicates that the host logic has terminated the transaction and transitioned into the Stop state</p> <p>0: Stopped (The host logic has terminated the transaction and halted the operation.)</p> <p>1: Executed (The host logic executes the schedule.)</p>

## 51.6.2.6 USBSTS Register

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ASS	PSS	REC	HCH	—	—	—	—	—	—	IAA	HSE	FLR	PCD	USBER RINT	USBIN T
Initial value:	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved The write value should be 0.
15	ASS	0	R	Asynchronous Schedule Status Indicates the current status of asynchronous schedules. Asynchronous schedules are enabled (1) or disabled (0) when this bit matches the ASE (bit 5) in USBCMD. 0: Asynchronous schedules are disabled. 1: Asynchronous schedules are enabled.
14	PSS	0	R	Periodic Schedule Status Indicates the current status of periodic schedules. Periodic schedules are enabled (1) or disabled (0) when this bit matches the PSE (bit 4) in USBCMD. 0: Periodic schedules are disabled. 1: Periodic schedules are enabled.
13	REC	0	R	Reclamation This bit is used to detect empty asynchronous schedule state. The host logic clears this bit to 0 after a reset or a QH fetch with H = 1. The host logic also sets this bit when executing an asynchronous transaction or having detected a start event. The host logic transitions to Async Schedule Sleeping mode when a QH with H = 1 is fetched while this bit is 0.
12	HCH	1	R	This bit is cleared to 0 when the RS (bit 0) in USBCMD is 1. When the RS bit is set to 0 by the host logic or software, the EHCI host logic stops the execution and the host logic sets this bit to 0. 0: EHCI host logic execution in progress 1: EHCI host logic execution stopped
11 to 6	—	All 0	R	Reserved The write value should be 0.

Bit	Bit Name	Initial Value	R/W	Description
5	IAA	0	R/W	<p>Interrupt on Async Advance</p> <p>Indicates the Async Advance interrupt status.</p> <p>Fetching a QH, the host logic checks the Interrupt on Async Advance Doorbell (IAAD) bit status in USBCMD. If the IAAD bit is 1, the host logic clears the IAAD bit on the successful completion of the QH processing and sets this bit.</p> <p>When the IAAE bit (bit 5) in USBINTR is 1, the Async Advance interrupt is generated on the next timing after this bit is set to 1.</p> <p>This bit can be cleared by writing 1 by the software. Writing 0 has no effect.</p> <p>0: Async Advance interrupt has not been generated. 1: Async Advance interrupt generation has been detected.</p>
4	HSE	0	R/W	<p>Host System Error</p> <p>This bit is set to 1 if a severe error, such as a parity error on the PCI system, has occurred in the host logic.</p> <p>When a severe error has occurred, the host logic clears the RS (bit 0) in USBCMD to 0 to prevent any TD from being executed.</p> <p>This bit can be cleared by writing 1 by the software. Writing 0 has no effect.</p> <p>0: A system error has not occurred. 1: A system error has occurred.</p>
3	FLR	0	R/W	<p>Frame List Rollover</p> <p>The host logic sets this bit to 1 if the Frame Index bit in FRINDEX rolls over from its maximum value to H'0000.</p> <p>The maximum value (at what value a Rollover occurs) depends on the FLS (bits 3 and 2) of USBCMD.</p> <p>This bit can be cleared by writing 1 by the software. Writing 0 has no effect.</p> <p>0: Rollover to H'000 has not occurred in frame list. 1: Rollover to H'000 has occurred in frame list.</p>
2	PCD	0	R/W	<p>Port Change Detect</p> <p>Indicates that port status has changed.</p> <p>The host logic sets this bit when any of the following conditions is satisfied in a port with the Port Owner (bit 13) of PORTSC1 being 0:</p> <ul style="list-style-type: none"> <li>• The CSC (bit 1) of PORTSC1 changes from 0 to 1 (device connection/disconnection detected)</li> <li>• The PEDC (bit 3) of PORTSC1 changes from 0 to 1 (port enable state changed)</li> <li>• The OC (bit 5) of PORTSC1 changes from 0 to 1 (overcurrent state detected)</li> <li>• The FPR (bit 6) of PORTSC1 changes from 0 to 1 (a transition from J to K detected in a suspended port)</li> </ul> <p>This bit can be cleared by writing 1 by the software. Writing 0 has no effect.</p>

Bit	Bit Name	Initial Value	R/W	Description
1	USBERRINT	0	R/W	<p>USB Error Interrupt</p> <p>Indicates that a USB transaction has ended with an error.</p> <p>The host logic sets this bit when a USB transaction ends with an error, such as an error counter underflow.</p> <p>This bit can be cleared by writing 1 by the software. Writing 0 has no effect.</p> <p>0: Normal USB transaction 1: USB transaction has ended with an error</p>
0	USBINT	0	R/W	<p>USB Interrupt</p> <p>Indicates that the USB transfer has ended.</p> <p>The host logic sets this bit when:</p> <ul style="list-style-type: none"> <li>• USB transfer is completed, or</li> <li>• A short packet is received</li> </ul> <p>If the IOC (Interrupt on Complete) of the TD is 1, this bit is also set even if the USB transfer ends with an error.</p> <p>This bit can be cleared by writing 1 by the software. Writing 0 has no effect.</p> <p>0: USB transfer has not ended 1: USB transfer has ended</p>

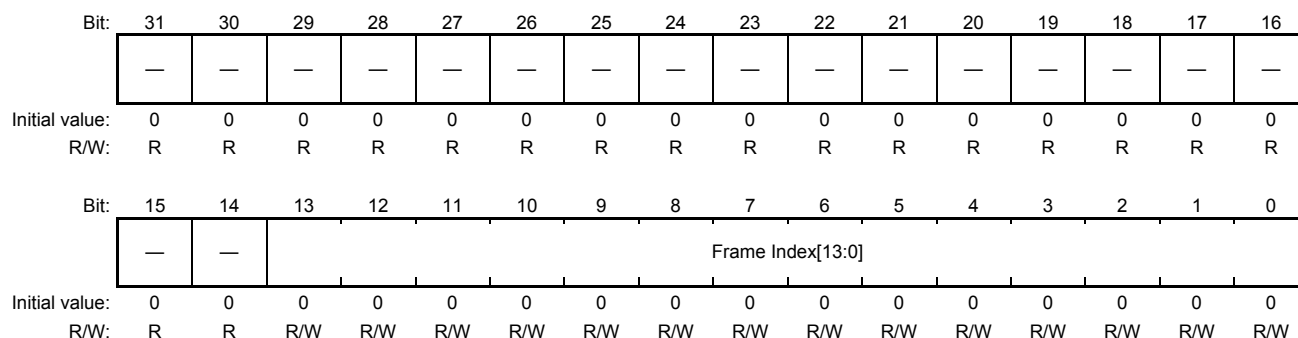


## 51.6.2.7 USBINTR Register

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	IAAE	HSEE	FLRE	PCIE	USBEI E	USBIE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W

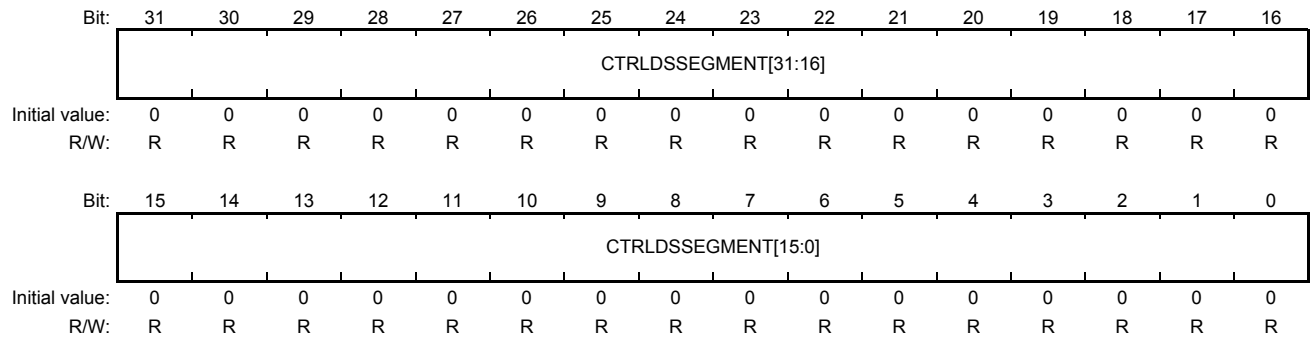
Bit	Bit Name	Initial Value	R/W	Description
31 to 6	—	All 0	R	Reserved The write value should be 0.
5	IAAE	0	R/W	Interrupt on Async Advance Enable Enables or disables the IAA bit (bit 5) in USBSTS. The interrupt can be cleared with the IAA bit. 0: Disable 1: Enable
4	HSEE	0	R/W	Host System Error Enable Enables or disables the HSE bit (bit 4) in USBSTS. The interrupt can be cleared with the HSE bit. 0: Disable 1: Enable
3	FLRE	0	R/W	Frame List Rollover Enable Enables or disables the FLR bit (bit 3) in USBSTS. The interrupt can be cleared with the FLR bit. 0: Disable 1: Enable
2	PCIE	0	R/W	Port Change Interrupt Enable Enables or disables the PCD bit (bit 2) in USBSTS. The interrupt can be cleared with the PCD bit. 0: Disable 1: Enable
1	USBEIE	0	R/W	USB Error Interrupt Enable Enables or disables the USBERRINT bit (bit 1) in USBSTS. The interrupt can be cleared with the USBERRINT bit. 0: Disable 1: Enable
0	USBIE	0	R/W	USB Interrupt Enable Enables or disables the USBINT bit (bit 0) in USBSTS. The interrupt can be cleared with the USBINT bit. 0: Disable 1: Enable

**51.6.2.8 FRINDEX Register**



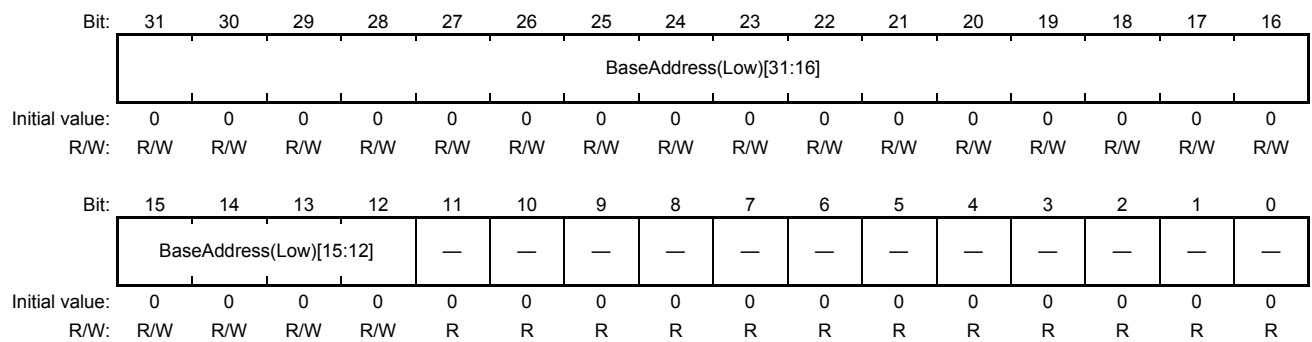
Bit	Bit Name	Initial Value	R/W	Description															
31 to 14	—	All 0	R	Reserved The write value should be 0.															
13 to 0	Frame Index [13:0]	H'0000	R/W	<p>This bit is used to attach an index to a periodic frame list by the host logic.</p> <p>This value is incremented at every end of microframe.</p> <p>Bits[N:3] are used for the Current Index of the frame list. In other words, the current frame list is accessed eight times before a transition is made to the next index. N depends on the FLS bits (bits 3 and 2) in USBCMD as follows:</p> <table border="1"> <thead> <tr> <th>Frame List Size</th> <th>Number of Elements</th> <th>N</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>1024</td> <td>12</td> </tr> <tr> <td>01</td> <td>512</td> <td>11</td> </tr> <tr> <td>10</td> <td>256</td> <td>10</td> </tr> <tr> <td>11</td> <td>Reserved</td> <td></td> </tr> </tbody> </table> <p>This register should be accessed only when the host logic is stopped (HCH bit (bit 12) in USBSTS = 1)</p> <p>The value of this register is used as the SOF frame number of an SOF token.</p>	Frame List Size	Number of Elements	N	00	1024	12	01	512	11	10	256	10	11	Reserved	
Frame List Size	Number of Elements	N																	
00	1024	12																	
01	512	11																	
10	256	10																	
11	Reserved																		

**51.6.2.9 CTRLDSSEGMENT Register**



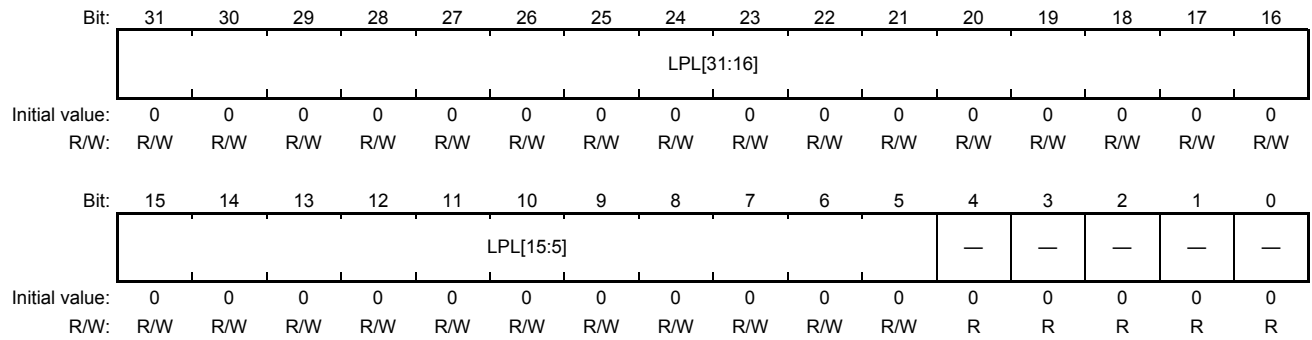
Bit	Bit Name	Initial Value	R/W	Description
31 to 0	CTRLDSSEGM ENT[31:0]	All 0	R	This register is not used since the host logic does not support the 64-bit addressing. Do not access this register.

**51.6.2.10 PERIODICLISTBASE Register**



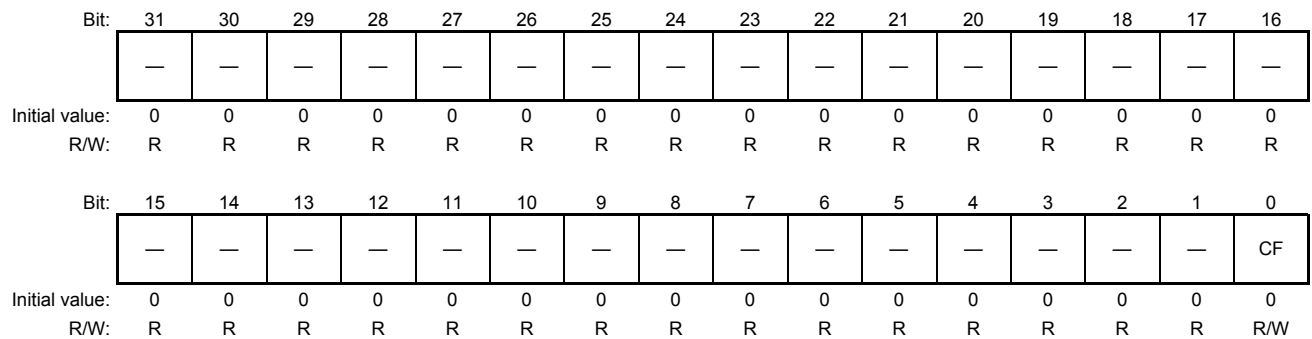
Bit	Bit Name	Initial Value	R/W	Description
31 to 12	BaseAddress (Low)[31:12]	All 0	R/W	Specifies the start address of the periodic frame list placed on the system memory. This register value is loaded by software before the list processing is executed by the host logic. The host logic determines the frame list to be executed using these bits and the Frame Index (bits 13 to 0) in FRINDEX. A periodic frame list address should be allocated on the 4-Kbyte boundary. If these bits are changed during operation, the operation cannot be guaranteed.
11 to 0	—	All 0	R	Reserved The write value should be 0.

**51.6.2.11 ASYNCLISTADDR Register**



Bit	Bit Name	Initial Value	R/W	Description
31 to 5	LPL[31:5]	All 0	R/W	Link Pointer Low Specifies the asynchronous queue head for the next execution in the system memory. An asynchronous queue head address should be allocated on the 32-byte boundary.
4 to 0	—	All 0	R	Reserved The write value should be 0.

**51.6.2.12 CONFIGFLAG Register**



Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved The write value should be 0.
0	CF	0	R/W	Configure Flag Specifies whether the OHCI or EHCI is routed by the port routing control circuit by default. This bit is set to 1 by the software at the end of the host logic configuration process. 0: Each port is routed to the OHCI host logic by default. 1: Each port is routed to the EHCI host logic by default.

## 51.6.2.13 PORTSC1 Register

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	WKOC _E	WKDSC NNT_E	WKCNT E	PTC[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PIC[1:0]		PO	PP	LS[1:0]		—	PR	SUS	FPR	OC	OCA	PEDC	PED	CSC	CCS
Initial value:	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R	R	R	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 23	—	All 0	R	Reserved The write value should be 0.
22	WKOC_E	0	R/W	Wake on Over-current Enable Setting this bit to 1 enables detecting overcurrent for ports as a wakeup event. The host logic operation is not affected by this bit. When the PP bit is 0, this bit is 0.
21	WKDSCNNT_E	0	R/W	Wake on Disconnect Enable Setting this bit to 1 enables detecting device disconnection as a wakeup event. The host logic operation is not affected by this bit. When the PP bit is 0, this bit is 0.
20	WKCNTNT_E	0	R/W	Wake on Connect Enable Setting this bit to 1 enables detecting device connection as a wakeup event. The host logic operation is not affected by this bit. When the PP bit is 0, this bit is 0.
19 to 16	PTC[3:0]	0000	R/W	Port Test Control Controls test mode. For details of the test mode, see section 7 in the USB2.0 Specifications. 0000: Normal 0001: Test J_STATE 0010: Test K_STATE 0011: Test SE0_NAK 0100: Test Packet 0101: Test FORCE_ENABLE Other: Reserved
15, 14	PIC[1:0]	00	R/W	Port Indicator Control Since the host logic does not support the port indicator control function, these bits are set to B'00. Writing these bits has no effect.

Bit	Bit Name	Initial Value	R/W	Description																				
13	PO	1	R/W	<p>Port Owner</p> <p>Specifies whether the OHCI or EHCI has the port ownership.</p> <p>0: The EHCI has the port ownership.</p> <p>1: The OHCI has the port ownership.</p> <p>This bit is cleared to 0 when the CF (bit 0) in CONFIGFLAG changes from 0 to 1. When the CF bit is 0, this bit is 1.</p> <p>When the connected device is not a high-speed device, this bit is set to 1 and the ownership is passed to the OHCI.</p>																				
12	PP	0	R/W	<p>Port Power</p> <p>Controls the port power.</p> <p>When this bit is 0 or the port power is turned off, the port does not function and connection/disconnection is not detected.</p> <p>If overcurrent is detected with this bit being 1, the host logic clears this bit and turns off the power to the port.</p> <p>0: The port power is turned off.</p> <p>1: The port power is turned on.</p> <p>The function of this bit differs depending on the PPC bit (bit 4) in HCSPARAMS.</p> <table border="1"> <thead> <tr> <th>PPC</th> <th>PP</th> <th>Function</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>1</td> <td>This bit is always 1 and the port power is always turned on.</td> </tr> <tr> <td>1</td> <td>0 or 1</td> <td>The port power can be switched on and off depending on this bit.</td> </tr> </tbody> </table>	PPC	PP	Function	0	1	This bit is always 1 and the port power is always turned on.	1	0 or 1	The port power can be switched on and off depending on this bit.											
PPC	PP	Function																						
0	1	This bit is always 1 and the port power is always turned on.																						
1	0 or 1	The port power can be switched on and off depending on this bit.																						
11, 10	LS[1:0]	00	R	<p>Line Status</p> <p>These bits indicate the current D+/D- logic level of the current USB port. D+ is indicated at the 11th bit (bit 11) and D- is indicated at the 10th bit (bit 10).</p> <p>This field is used for detecting a low-speed device connection before port-reset or port-enable processing sequence is executed.</p> <p>This field is only valid when PED (bit 3) = 0 and CCS (bit 0) = 1.</p> <p>This bit is 0 when the PP bit is 0.</p> <table border="1"> <thead> <tr> <th>Bit 11 (D+)</th> <th>Bit 10 (D-)</th> <th>USB State</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>SE0</td> <td>Not a low-speed device. Performs EHCI port reset</td> </tr> <tr> <td>0</td> <td>1</td> <td>K-state</td> <td>Low-speed device connected Releases port ownership from EHCI to OHCI.</td> </tr> <tr> <td>1</td> <td>0</td> <td>J-state</td> <td>Not a low-speed device. Performs EHCI port reset</td> </tr> <tr> <td>1</td> <td>1</td> <td>Undefined</td> <td>Not a low-speed device. Performs EHCI port reset</td> </tr> </tbody> </table>	Bit 11 (D+)	Bit 10 (D-)	USB State	Description	0	0	SE0	Not a low-speed device. Performs EHCI port reset	0	1	K-state	Low-speed device connected Releases port ownership from EHCI to OHCI.	1	0	J-state	Not a low-speed device. Performs EHCI port reset	1	1	Undefined	Not a low-speed device. Performs EHCI port reset
Bit 11 (D+)	Bit 10 (D-)	USB State	Description																					
0	0	SE0	Not a low-speed device. Performs EHCI port reset																					
0	1	K-state	Low-speed device connected Releases port ownership from EHCI to OHCI.																					
1	0	J-state	Not a low-speed device. Performs EHCI port reset																					
1	1	Undefined	Not a low-speed device. Performs EHCI port reset																					
9	—	0	R	<p>Reserved</p> <p>The write value should be 0.</p>																				

Bit	Bit Name	Initial Value	R/W	Description												
8	PR	0	R/W	<p><b>Port Reset</b></p> <p>Controls the port resetting processing.</p> <p>The setting of this bit by software commences the bus resetting operation that is defined in the USB 2.0 specifications. To complete the bus resetting operation, the software must write a 0 to this bit. The software must keep this bit at 1 until such time as the reset time defined in the USB 2.0 specifications has elapsed.</p> <p>When HCH (bit 12) in USBSTS is 1, the software must not set this bit.</p> <p>This bit is 0 when either of the following conditions are satisfied:</p> <ul style="list-style-type: none"> <li>• PP bit = 0</li> <li>• Port Owner bit = 1</li> <li>• Current Connect Status = 0</li> </ul> <p>1: The port being reset 0: The port not being reset</p>												
7	SUS	0	R/W	<p><b>Suspend</b></p> <p>Indicates the suspend state of the port.</p> <p>1: The port is in the Suspend state. 0: The port is not in the Suspend state.</p> <p>Depending on the setting of this bit and PED (bit 2), the port assumes the following condition:</p> <table border="1"> <thead> <tr> <th>PED</th> <th>Suspend</th> <th>Port State</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>X</td> <td>Disable</td> </tr> <tr> <td>1</td> <td>0</td> <td>Enable</td> </tr> <tr> <td>1</td> <td>1</td> <td>Suspend</td> </tr> </tbody> </table> <p>In the Suspend state, any data transfer from this port to the downstream port is blocked, except that Port Reset is conveyed. If this bit is set to 1 during data transfer, the status is updated and the data is blocked after the current transfer operation is completed.</p> <p>This bit is set to 1 by the software. This bit can be set to 1 only when the PP bit = 1, PO bit = 0, and CCS bit = 1.</p> <p>This bit is unconditionally cleared to 0 when:</p> <ul style="list-style-type: none"> <li>• the software clears the Force PR bit to 0 or</li> <li>• the software sets the PR bit to 1.</li> </ul> <p>This bit is 0 when the PP bit is 0.</p>	PED	Suspend	Port State	0	X	Disable	1	0	Enable	1	1	Suspend
PED	Suspend	Port State														
0	X	Disable														
1	0	Enable														
1	1	Suspend														

Bit	Bit Name	Initial Value	R/W	Description
6	FPR	0	R/W	<p>Force Port Resume</p> <p>Indicates that the Resume operation of the port has been detected.</p> <p>The host logic sets this bit and PCD (bit 2) in USBSTS to 1 when a transition from J to K (RemoteWakeUp) is detected when the ports is in the Suspend state. In addition, the software sets this bit to output the Resume signal. At this time, Port Change Detect bit must not be set.</p> <p>As long as this bit is 1, the Resume signal (Full-Speed K) continues to be driven. The software must clear this bit after an appropriate length of time. By changing this bit from 1 to 0, the port returns to the HS idle state. The bit remains 1 until the port returns to the HS idle state.</p> <p>This bit is 0 when the PP bit is 0.</p> <p>0: Resume (K-state) has not been detected/output 1: Resume (K-state) has been detected/output</p>
5	OC	0	R/W	<p>Over-current Change</p> <p>Indicates that the OCA (bit 4) status has changed.</p> <p>This bit can be cleared by writing 1 by software. Writing 0 has no effect.</p> <p>0: Indicates that the Over-Current Active bit has not changed. 1: Indicates that the Over-Current Active bit has changed.</p>
4	OCA	0	R	<p>Over-current Active</p> <p>Indicates the port overcurrent status.</p> <p>Detecting the overcurrent status, the host logic clears the PP (bit 12) and related bits to 0 and sets this bit to 1.</p> <p>This bit is automatically cleared to 0 when the over-current state is cancelled.</p> <p>0: Indicates that the port is not in the overcurrent state. 1: Indicates that the port is in the overcurrent state.</p>
3	PEDC	0	R/W	<p>Port Enable/Disable Change</p> <p>Indicates that the port enable/disable status has changed.</p> <p>Detecting the Frame Babble, the host logic disables the port and sets this bit to 1.</p> <p>This bit can be cleared by writing 1 by the software. Writing 0 has no effect.</p> <p>This bit is 0 when the PP bit is 0.</p> <p>0: Indicates that the port state has not changed. 1: Indicates that the port state has changed from enable to disable status.</p>

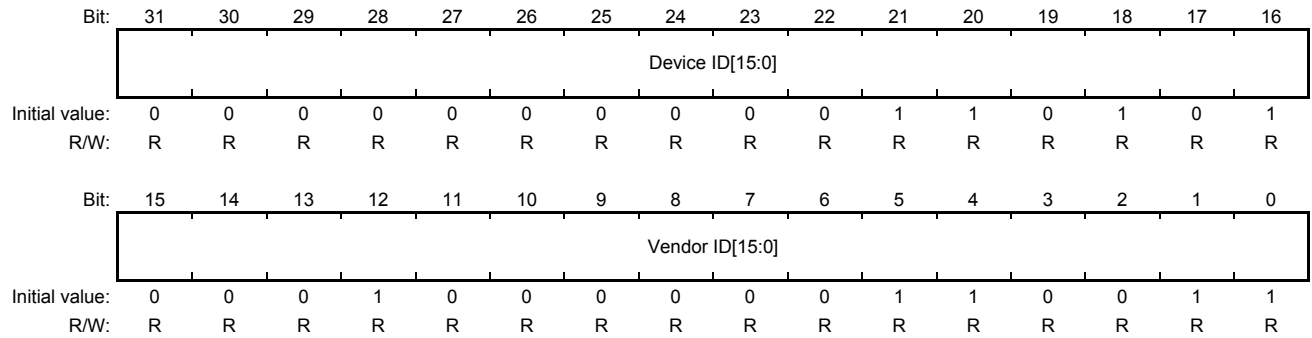


Bit	Bit Name	Initial Value	R/W	Description
2	PED	0	R/W	<p>Port Enabled/Disabled</p> <p>Indicates that the port is enabled or disabled.</p> <p>The host logic enables the port and sets this bit to 1 when it resets the port and verifies that the connected device is a HS device. This bit cannot be set by the software.</p> <p>The host logic disables the port and clears this bit to 0 when it detects a disconnection of a device or other errors. The port is also disabled by writing 0 by the software. The status of this bit does not change until the port status actually changes.</p> <p>If the port is disabled, data does not propagate to the down-stream port; the port reset, however, is conveyed.</p> <p>This bit is 0 when the PP bit is 0.</p> <p>When the PTC (bits 3 to 0) is B'0101 (Test FORCE_ENABLE), the port is unconditionally enabled and this bit is set to 1.</p> <p>0: The port is disabled. 1: The port is enabled.</p>
1	CSC	0	R/W	<p>Connect Status Change</p> <p>Indicates that the CCS (bit 0) has changed.</p> <p>This bit can be cleared by writing 1 by the software. Writing 0 has no effect.</p> <p>This bit is 0 when the PP bit is 0.</p> <p>0: Status has not changed. 1: The Current Connect Status bit has changed.</p>
0	CCS	0	R/W	<p>Current Connect Status</p> <p>Indicates the port connection status.</p> <p>Detecting a connection of a device, the host logic sets this bit to 1.</p> <p>When the PTC (bits 3 to 0) is B'0101 (Test FORCE_ENABLE), this bit is set to 1 even if a device is not connected.</p> <p>Detecting a disconnection of a device clears this bit to 0.</p> <p>This bit is 0 when the PP or PO bit is 0.</p> <p>0: No device has been connected to the port. 1: A device has been connected to the port.</p>

**51.6.3 PCI Configuration Registers for OHCI**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

**51.6.3.1 Offset H'00 (Vendor ID, Device ID)**



Bit	Bit Name	Initial Value	R/W	Description
31 to 16	Device ID[15:0]	H'0035	R	This register indicates the device type. This is used to select a driver that operates the device as specified in the PCI standard. This register does not need to be used in the embedded host.
15 to 0	Vendor ID[15:0]	H'1033	R	This register indicates the vendor of the device. This is used to select a driver that operates the device as specified in the PCI standard. This register does not need to be used in the embedded host.

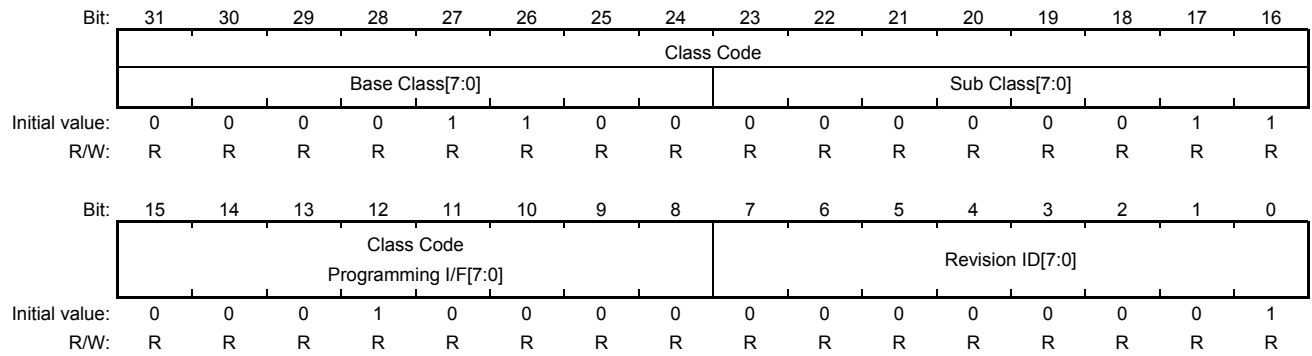
## 51.6.3.2 Offset H'04 (Command, Status)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Detected Parity Error	Signaled System Error	Received Master Abort	Received Target Abort	Signaled Target Abort	Devsel Timing[1:0]		Data Parity Error Detected	Fast Back to Back Capable	—	—	Capabilities List	—	—	—	—
Initial value:	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	Fast Back to Back Enable	SERR Enable	Wait Cycle Control	Parity Error Response	VGA Palette Snoop	Memory Write and Invalidate	Special Cycle	Bus Master	Memory Space	I/O Space
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R	R/W	R	R/W	R	R/W	R/W	R

Bit	Bit Name	Initial Value	R/W	Description
31	Detected Parity Error	0	R/W	This is a status bit for parity error. This bit is set when an address or data parity error is detected. Writing 1 from the PCI bus clears this bit.
30	Signaled System Error	0	R/W	This is a status bit for SERR. This bit is set to 1 when a system error occurs. Writing 1 from the PCI bus clears this bit.
29	Received Master Abort	0	R/W	This is a status bit for Master/Master Abort. This bit is set to 1 in master operation when the bus cycle being executed by the host logic is terminated through Master Abort. Writing 1 from the PCI bus clears this bit.
28	Received Target Abort	0	R/W	This is a status bit for Master/Target Abort. This bit is set to 1 in master operation when the bus cycle being executed by the host logic is terminated through Target Abort. Writing 1 from the PCI bus clears this bit.
27	Signaled Target Abort	0	R/W	This is a status bit for Slave/Target Abort. This bit is set to 1 in slave operation when the host logic has terminated, through Target Abort, the bus cycle in which the host logic is accessed. Writing 1 from the PCI bus clears this bit.
26, 25	Devsel Timing[1:0]	01	R	These bits indicate the DEVSEL response speed. The value is fixed to B'01 (medium-speed response).
24	Data Parity Error Detected	0	R/W	This bit is set when a parity error is detected in master operation. Writing 1 from the PCI bus clears this bit. The value is fixed to 0 while the Parity Error Response bit is set as disabled.
23	Fast Back to Back Capable	0	R	This bit indicates whether Fast Back to Back transactions are supported. As the host logic does not support Fast Back to Back transactions, this value is fixed to 0.
22, 21	—	0	R	Reserved The write value should be 0.
20	Capabilities List	1	R	This value is fixed to 1, which indicates that the power management mode is supported.
19 to 10	—	All 0	R	Reserved The write value should be 0.
9	Fast Back to Back Enable	0	R	This bit enables Fast Back to Back transactions. As the host logic does not support Fast Back to Back transactions, this value is always 0.

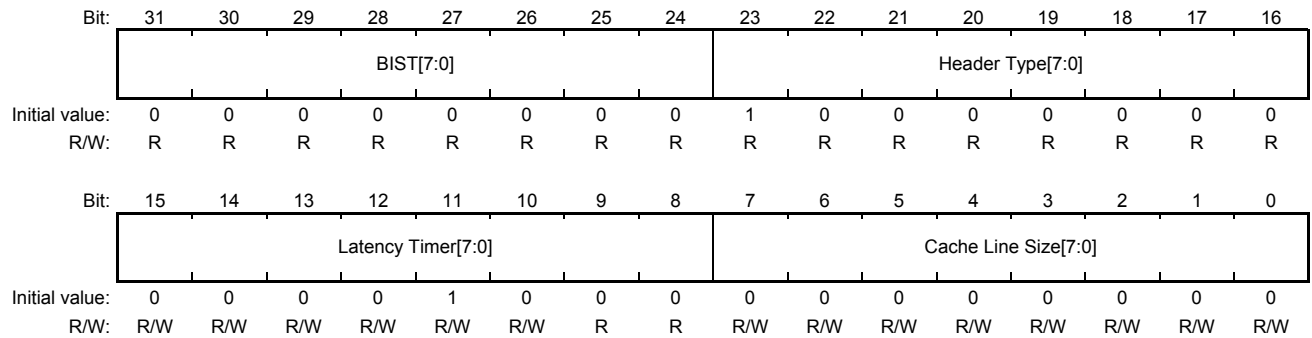
Bit	Bit Name	Initial Value	R/W	Description
8	SERR Enable	0	R/W	This bit enables system error response. 0: SERR0 is not asserted. 1: SERR0 is asserted. To notify of a system error through the SERR signal, set this bit to 1.
7	Wait Cycle Control	0	R	This bit enables wait cycle control. As the host logic does not support address/data stepping, this value is always 0.
6	Parity Error Response	0	R/W	This bit enables parity error response. 0: PERR0 is not asserted. 1: PERR0 is asserted. When a parity error is detected, the Detected Parity Error bit is set to 1 even if this bit is cleared to 0.
5	VGA Palette Snoop	0	R	This bit enables VGA palette snooping. As the host logic does not support VGA palette snooping, this value is always 0.
4	Memory Write and Invalidate Enable	0	R/W	This bit enables the Memory Write and Invalidate command. In this module, do not change this from the initial value (0). 0: Memory write and invalidate command is disabled. 1: Memory write and invalidate command is enabled.
3	Special Cycle	0	R	This bit enables Special Cycle operation. As the host logic does not support the Special Cycle operation, this value is always 0.
2	Bus Master	0	R/W	This bit enables bus master operation. This is an enable signal for master access to the PCI bus. Set to 1 when accessing the SRAM on the system bus. Set this bit to 1 during initial setting of the host logic.
1	Memory Space	0	R/W	This bit enables access to the memory space. This is an enable signal for memory access specified in the PCI standard. Set to 1 when accessing registers. Set this bit to 1 during initial setting of the host logic.
0	I/O Space	0	R	This bit enables access to the I/O space. As the host logic does not accept I/O access, this value is always 0.

**51.6.3.3 Offset H'08 (Revision ID, Class Code)**



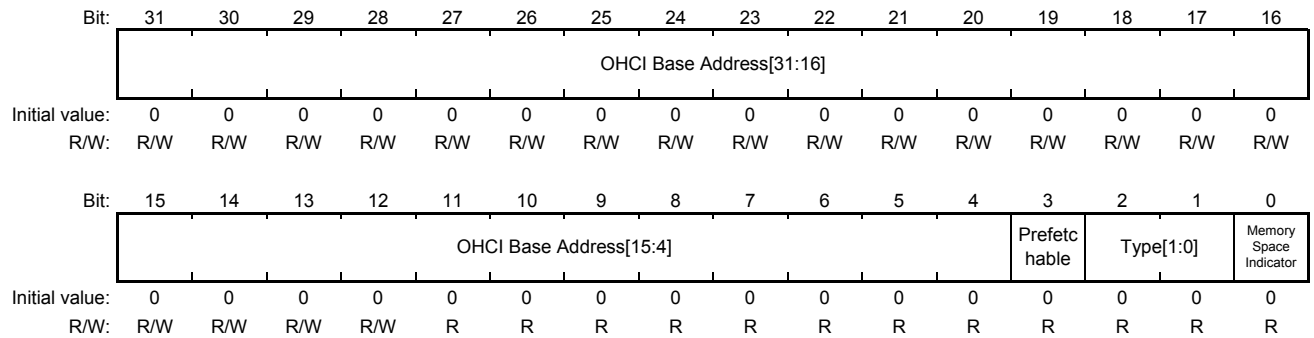
Bit	Bit Name	Initial Value	R/W	Description
31 to 24	Base Class[7:0]	H'0C	R	These bits indicate the base class specified in the PCI standard. The value is H'0C, which indicates a serial peripheral bus controller.
23 to 16	Sub Class[7:0]	H'03	R	These bits indicate the subclass specified in the PCI standard. The value is H'03, which indicates a USB device.
15 to 8	Programming I/F[7:0]	H'10	R	These bits indicate the program interface specified in the PCI standard. The value is H'10, which indicates OHCI.
7 to 0	Revision ID[7:0]	H'01	R	These bits indicate the revision of the host logic. The value is fixed to H'01.

**51.6.3.4 Offset H'0C (Cache Line Size, Latency Timer, Header Type, BIST)**



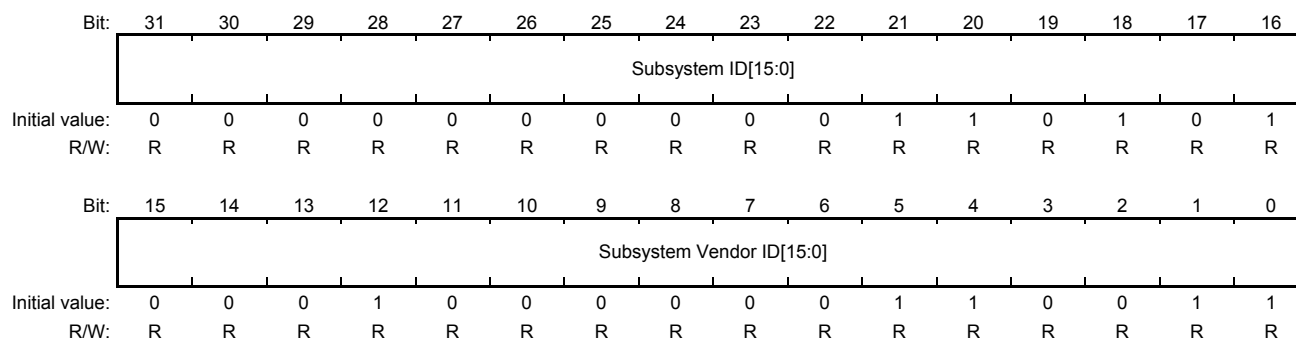
Bit	Bit Name	Initial Value	R/W	Description
31 to 24	BIST[7:0]	H'00	R	These bits are used for self testing. As the host logic does not support the self test function, this value is always H'00.
23 to 16	Header Type[7:0]	H'80	R	These bits notify the system of the header type. As the header type is Type 0, bits [22:16] are fixed to H'00. As this is a multifunction device, bit 23 is fixed to 1.
15 to 8	Latency Timer[7:0]	H'08	R/W	These bits notify the system of the latency timer. The lowest two bits are fixed to B'00.
7 to 0	Cache Line Size[7:0]	H'00	R/W	These bits notify the system of the cache line size.

**51.6.3.5 Offset H'10 (OHCI Base Address)**



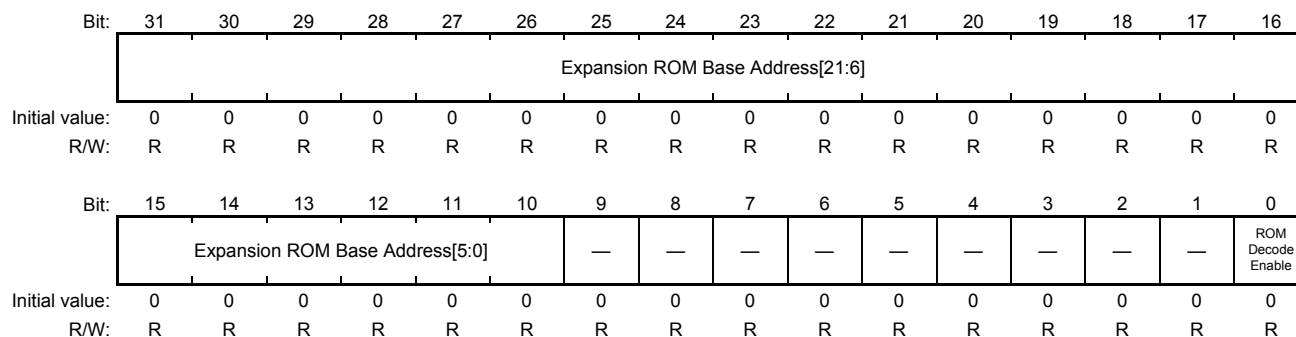
Bit	Bit Name	Initial Value	R/W	Description
31 to 4	OHCI Base Address[31:12]	H'0000 0	R/W	Bits [31:12] specify the base address of the operational registers. Specify the base address of the operational registers determined by the system during initialization. Bits [11:4] are fixed to H'00, which indicates that the operational registers are allocated to a 4-Kbyte address space.
	OHCI Base Address[11:4]	H'00	R	
3	Prefetchable	0	R	As the host logic does not support prefetching in memory read cycles, this bit is fixed to 0.
2, 1	Type[1:0]	00	R	These bits are fixed to B'00, which indicates that the base address of the OHCI operational registers has a 32-bit width and can be allocated to any location in a 32-bit memory space.
0	Memory Space Indicator	0	R	This bit is fixed to 0, which indicates that the OHCI operational registers are mapped to the system memory space.

### 51.6.3.6 Offset H'2C (Subsystem Vendor ID, Subsystem ID)



Bit	Bit Name	Initial Value	R/W	Description
31 to 16	Subsystem ID[15:0]	H'0035	R	This register indicates the device type. This is used to select a driver that operates the device as specified in the PCI standard. This register does not need to be used in the embedded host.
15 to 0	Subsystem Vendor ID [15:0]	H'1033	R	This register indicates the vendor of the device. This is used to select a driver that operates the device as specified in the PCI standard. This register does not need to be used in the embedded host.

### 51.6.3.7 Offset H'30 (Expansion ROM Base Address)



Bit	Bit Name	Initial Value	R/W	Description
31 to 10	Expansion ROM Base Address[21:0]	H'000000	R	As decoding of expansion ROM is prohibited, these bits are always read as H'000000. These bits cannot be written to.
9 to 1	—	All 0	R	Reserved (Don't care)
0	ROM Decode Enable	0	R	As decoding of expansion ROM is prohibited, this bit is always read as 0. This bit cannot be written to.



**51.6.3.8 Offset H'34 (Capability Pointer)**

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	Capability Pointer[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved (Don't care)
7 to 0	Capability Pointer[7:0]	H'40	R	These bits hold the pointer to the capability identifier. As the pointer is set to H'40 in the host logic, this value is set to H'40.

**51.6.3.9 Offset H'3C (Interrupt Line, Interrupt Pin, Min gnt, Max Latency)**

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Max Latency[7:0]								Min Gnt[7:0]							
Initial value:	0	0	1	0	1	0	1	0	0	0	0	0	0	0	0	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Interrupt Pin[7:0]								Interrupt Line[7:0]							
Initial value:	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	Max Latency[7:0]	H'2A	R	These bits indicate the maximum frequency of PCI bus acquisition. As the maximum frequency is set to H'2A in the host logic, this value is set to H'2A.
23 to 16	Min Gnt[7:0]	H'01	R	These bits indicate the minimum burst transfer time. As the minimum time is set to H'01 in the host logic, this value is set to H'01.
15 to 8	Interrupt Pin[7:0]	H'01	R	These bits indicate the pin for outputting interrupts. As INTA is used, this value is fixed to H'01.
7 to 0	Interrupt Line[7:0]	H'00	R/W	These bits indicate the interrupt line. In this module, do not change this from the initial value (H'00).

### 51.6.3.10 Offset H'40 (Capability Identifier, Next Item Pointer, Power Management Capabilities)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Power Management Capabilities															
	PME Support[4:0]				D2 Support	D1 Support	AUX Current[2:0]			DSI	—	PME CLK	Version[2:0]			
Initial value:	0	1	1	1	1	1	1	0	0	0	0	0	0	0	1	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Next Item Pointer[7:0]							Capability Identifier[7:0]								
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31	PME Support[4:0]	0	R	This bit indicates whether the D3 cold state is supported. As the D3 cold state is not supported, this value is fixed to 0.
30 to 27		1111	R	These bits are fixed to B'1111, which indicates that PME interrupt generation is supported in all PCI power states (D0 to D3).
26	D2 Support	1	R	This bit is fixed to 1, which indicates that PCI power state D2 is supported.
25	D1 Support	1	R	This bit is fixed to 1, which indicates that PCI power state D1 is supported.
24 to 22	AUX Current[2:0]	000	R	These bits indicate the necessary current for 3.3-V auxiliary power supply. As PME interrupt generation from the D3 cold state is not supported, this value is fixed to B'000.
21	DSI	0	R	This bit is fixed to 0, which indicates that special initialization is not necessary for power management.
20	—	0	R	Reserved (Don't care)
19	PMECLK	0	R	This bit is fixed to 0, which indicates that PCLK is not necessary for PME interrupt generation.
18 to 16	Version[2:0]	010	R	These bits are fixed to B'010, which indicates that the host logic conforms to "PCI power management interface specification release 1.1".
15 to 8	Next Item Pointer[7:0]	H'00	R	These bits are fixed to H'00, which indicates that the next item does not exist.
7 to 0	Capability Identifier[7:0]	H'01	R	These bits indicate the PCI power management register ID. The value is fixed to H'01.

### 51.6.3.11 Offset H'44 (Power Management Control/Status, PMCSR Bridge Support Extensions)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Data								PMCSR Bridge Support Extensions							
	Data[7:0]								BPCC Enable	B2_B3	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Power Management Control/Status															
	PME Status	Data Scale[1:0]	Data Select[3:0]			PME Enable	—	—	—	—	—	—	—	—	Power State[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R	R	R	R	R/W	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	Data[7:0]	H'00	R/W	The value of these bits is H'00. This is an optional field in the PCI standard, and the host logic does not support it.
23	BPCC Enable	0	R	The value of this bit is 0. This is a bit for the bridge, and the host logic does not support it.
22	B2_B3	0	R	The value of this bit is 0. This is a bit for the bridge, and the host logic does not support it.
21 to 16	—	All 0	R	Reserved The write value should always be 0.
15	PME Status	0	R/W	This bit indicates the PME interrupt state. It is set to 1 when the following condition for PME generation is satisfied. [PME generation condition] Bit 3 (RD) in the HcInterruptStatus register is set to 1 while bit 10 (RWE) in the HcControl register is 1. Writing 1 from the PCI bus clears this bit to 0.
14, 13	Data Scale[1:0]	00	R	The value of these bits is B'00. This is an optional field in the PCI standard, and the host logic does not support it.
12 to 9	Data Select[3:0]	H'0	R	The value of these bits is H'0. This is an optional field in the PCI standard, and the host logic does not support it.
8	PME Enable	0	R/W	This bit specifies whether to use PME. Setting this bit to 1 generates a PME interrupt when operation returns from the power management state.
7 to 2	—	All 0	R	Reserved The write value should always be 0.
1, 0	Power State[1:0]	00	R/W	These bits indicate the power state of the PCI as follows. 00: D0 state 01: D1 state 10: D2 state 11: D3 hot state

### 51.6.3.12 Offset H'E0 (EXT1)

This register is the same as the EXT1 register located in the EHCI configuration space.

Therefore, this register can be accessed also by using the offset address on the EHCI configuration register side.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Potpgt								Hyper Speed transfer Control #2				—	—	—	
Initial value:	0	0	0	0	1	1	1	1	0	0	0	1	0	1	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	Hyper Speed transfer Control #1	—	—	—	—	—	ID_Write	—	—	—	—	Ppcnt	Port_no	
Initial value:	0	0	1	1	0	0	1	1	0	0	0	1	1	1	0	1
R/W:	R	R	R/W	R	R	R	R	R	R/W	R	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	Potpgt[7:0]	H'0F	R/W	These bits specify the value for bits [31:24] (PPOTPGT) in the OHCI HcRhDescriptorA register. POTPGT is the time that software should wait before accessing a root hub port after power supply to the port is started.
23 to 19	Hyper Speed transfer Control #2	H'02	R/W	Do not specify any value other than H'02 (HS asynchronous FIFO threshold = 64 bytes).
18 to 14	—	10000	R	Reserved Do not change this from the initial value.
13	Hyper Speed transfer Control #1 (HS Async OUT advance Mode)	1	R/W	This bit specifies the hyper-speed transfer mode for asynchronous OUT transfer. Setting to 1 enables this function (transfer rate improvement).
12 to 8	—	10011	R	Reserved Do not change this from the initial value.
7	ID_Write_Enable	0	R/W	This bit write-protects the Subsystem ID, Subsystem Vendor ID, Max Latency, and Min Gnt bits. 0: Write-protected. 1: Can be written to.
6 to 3	—	0011	R	Reserved Do not change this from the initial value.
2	Ppcnt	1	R/W	This bit specifies a value for bit 4 (PPC) in the EHCI HCSPARAMS register. 0: The PPC bit is cleared to 0. This indicates that the system incorporating this host logic does not provide a port power control switch and the port power is always active. 1: The PPC bit is set to 1. This indicates that the system incorporating this host logic provides a port power control switch. When the port power is always active, set this bit to 0 and bit 9 (NPS) in the OHCI HcRhDescriptor A register to 1.

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Bit	Bit Name	Initial Value	R/W	Description
1, 0	Port_no	01	R/W	<p>These bits specify the number of valid USB downstream ports.</p> <p>Setting   Valid Ports</p> <p>01:       Port1</p> <p>10:       Port1 and Port2</p> <p>Others:   Reserved</p> <p>In this module, do not change this from the initial value (B'01).</p>

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### 51.6.3.13 Offset H'E4 (EXT2)

This register is the same as the EXT2 register located in the EHCI configuration space. Therefore, this register can be accessed also by using the offset address on the EHCI configuration register side. However, note that bit 0 (EHCI\_mask) can be written to only on the OHCI side.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	PLL Unlock Register Access Mode	—	—	—	—	—	RAM Connect Check Result	RAM Connect Check END Flag	RUN RAM Connect Check
Initial value:	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R	R	R	R	R	R	R	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	Hyper Speed transfer Control #3	EHCI_mask
Initial value:	0	1	1	0	1	1	0	0	0	0	0	0	0	0	1	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

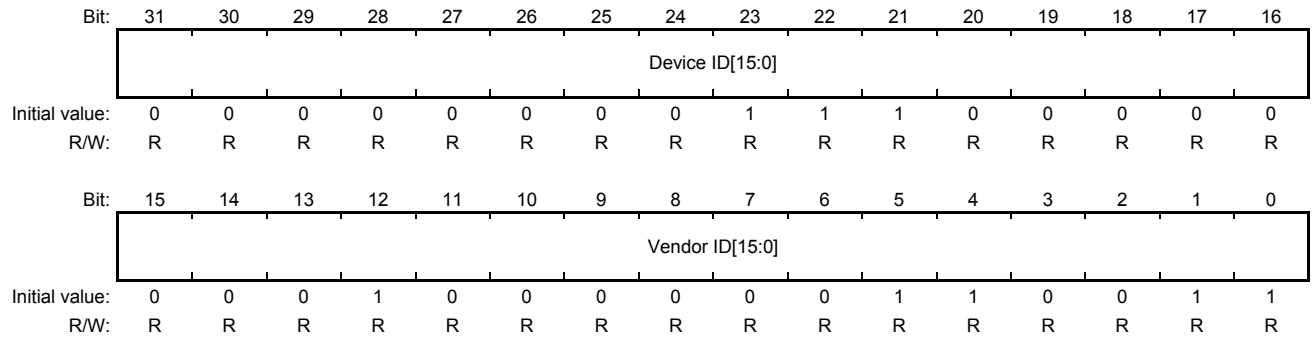
Bit	Bit Name	Initial Value	R/W	Description
31 to 25	—	All 0	R	Reserved Do not change this from the initial value.
24	PLL Unlock Register Access Mode	1	R/W	This bit specifies how to respond to register access in the PLL unlocked state. 0: If a register access request is received in the PLL unlocked state, a correct access response is not returned. Access is delayed until the PLL is locked. 1: If a register access request is received in the PLL unlocked state, a correct access response is returned but the read or written data is not guaranteed.
23 to 19	—	All 0	R	Reserved Do not change this from the initial value.
18	RAM Connect Check Result	0	R	This bit indicates the result of RAM connection check. 0: Connection check result is NG. 1: Connection check result is OK. This value is valid when the RAM Connect Check END Flag bit is 1. Once the connection check is done, this value is not cleared until the RUN RAM Connect Check bit changes from 0 to 1.
17	RAM Connect Check END Flag	0	R	This bit indicates the end of RAM connection check. 0: Connection check has not been done or ended. 1: Connection check has ended. This bit is set when a specified time (about 2 μs) has passed after the RAM connection check is started by modifying the RUN RAM check bit from 0 to 1.
16	RUN RAM Connect Check	0	R/W	This bit activates the RAM connection check circuit. Set this bit to 1 to start the RAM connection check. This bit is not cleared even after the check is completed. To check again, write 0 to this bit to clear it, and then write 1 again to start the check. When this bit changes from 0 to 1, the connection check circuit is reset and the RAM Connect Check END Flag bit and RAM Connect Check Result bit are cleared.
15 to 2	—	All 0	R	Reserved Do not change this from the initial value.

Bit	Bit Name	Initial Value	R/W	Description
1	Hyper Speed transfer Control #3	1	R/W	This bit specifies the hyper-speed transfer mode for asynchronous IN/OUT transfer. Setting to 1 enables this function (transfer rate improvement).
0	EHCI_mask	0	R/W	This bit enables or disables the EHCI host logic. 0: EHCI host logic is enabled. 1: EHCI host logic is disabled. When this bit is set to 1, register access in the EHCI PCI configuration space and memory space is disabled and the EHCI host logic does not operate.

**51.6.4 PCI Configuration Registers for EHCI**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

**51.6.4.1 Offset H'00 (Vendor ID, Device ID)**



Bit	Bit Name	Initial Value	R/W	Description
31 to 16	Device ID [15:0]	H'00E0	R	This register indicates the device type. This is used to select a driver that operates the device as specified in the PCI standard. This register does not need to be used in the embedded host.
15 to 0	Vendor ID [15:0]	H'1033	R	This register indicates the vendor of the device. This is used to select a driver that operates the device as specified in the PCI standard. This register does not need to be used in the embedded host.



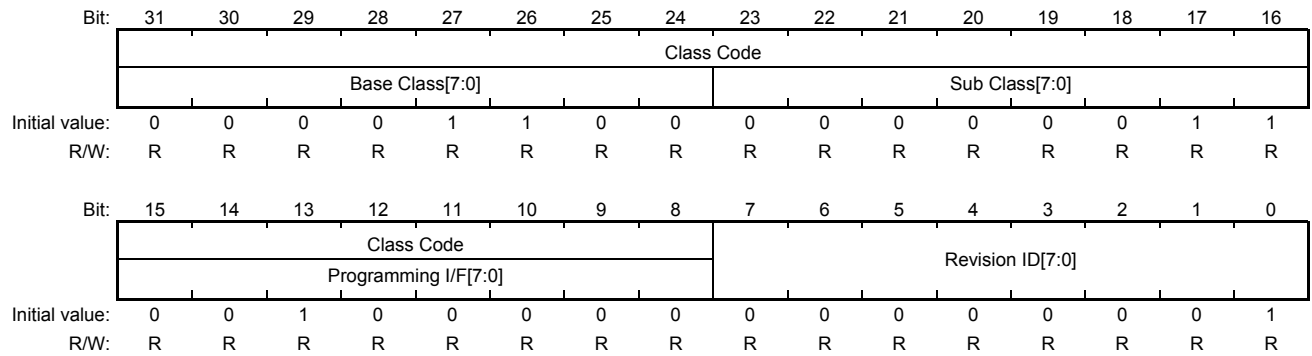
## 51.6.4.2 Offset H'04 (Command, Status)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Detected Parity Error	Signaled System Error	Received Master Abort	Received Target Abort	Signaled Target Abort	Devsel Timing[1:0]	Data Parity Error Detected	Fast Back to Back Capable	—	66 MHz Capable	Capabilities List	—	—	—	—	
Initial value:	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	Fast Back to Back Enable	SERR Enable	Wait Cycle Control	Parity Error Response	VGA Palette Snoop	Memory Write and Invalidate Enable	Special Cycle	Bus Master	Memory Space	I/O Space
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R	R/W	R	R/W	R	R/W	R/W	R

Bit	Bit Name	Initial Value	R/W	Description
31	Detected Parity Error	0	R/W	This is a status bit for parity error. This bit is set when an address or data parity error is detected. Writing 1 from the PCI bus clears this bit.
30	Signaled System Error	0	R/W	This is a status bit for SERR. This bit is set when a system error occurs. Writing 1 from the PCI bus clears this bit.
29	Received Master Abort	0	R/W	This is a status bit for Master/Master Abort. This bit is set to 1 in master operation when the bus cycle being executed by the host logic is terminated through Master Abort. Writing 1 from the PCI bus clears this bit.
28	Received Target Abort	0	R/W	This is a status bit for Master/Target Abort. This bit is set to 1 in master operation when the bus cycle being executed by the host logic is terminated through Target Abort. Writing 1 from the PCI bus clears this bit.
27	Signaled Target Abort	0	R	This is a status bit for Slave/Target Abort. This bit is set to 1 in slave operation when the host logic has terminated, through Target Abort, the bus cycle in which the host logic is accessed. Writing 1 from the PCI bus clears this bit.
26, 25	Devsel Timing[1:0]	01	R	These bits indicate the DEVSEL response speed. The value is fixed to B'01 (medium-speed response).
24	Data Parity Error Detected	0	R/W	This bit is set when a parity error is detected in master operation. Writing 1 from the PCI bus clears this bit. The value is fixed to 0 when the Parity Error Response bit is set as disabled.
23	Fast Back to Back Capable	0	R	This bit indicates whether Fast Back to Back transactions are supported. As the host logic does not support Fast Back to Back transactions, this value is fixed to 0.
22	—	0	R	Reserved The write value should always be 0.
21	66 MHz Capable	0	R	This bit indicates whether 66-MHz operation is available. As the host logic operates only at 33-MHz, this value is fixed to 0.
20	Capabilities List	1	R	This value is fixed to 1, which indicates that the power management mode is supported.
19 to 10	—	All 0	R	Reserved The write value should always be 0.
9	Fast Back to Back Enable	0	R	This bit enables Fast Back to Back transactions. As the host logic does not support Fast Back to Back transactions, this value is always 0.

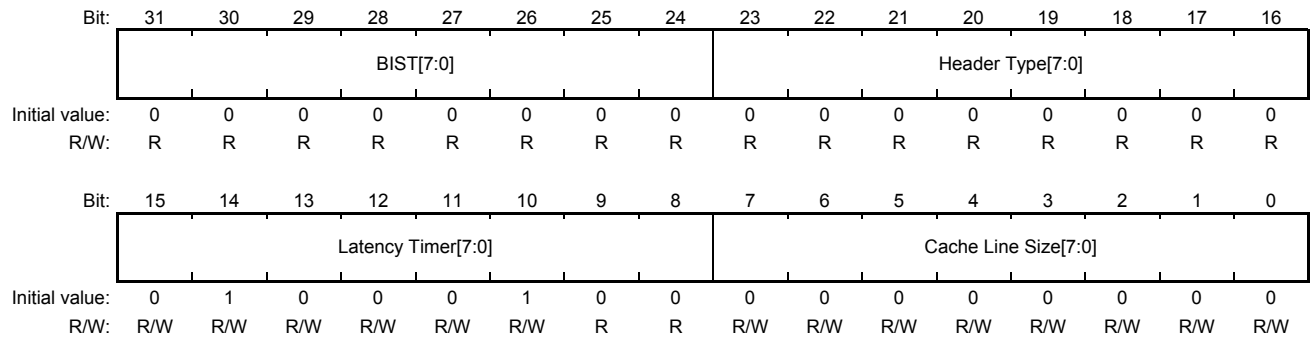
Bit	Bit Name	Initial Value	R/W	Description
8	SERR Enable	0	R/W	This bit enables system error response. 0: SERR0 is not asserted. 1: SERR0 is asserted. To notify of a system error through the SERR signal, set this bit to 1.
7	Wait Cycle Control	0	R	This bit enables wait cycle control. As the host logic does not support address/data stepping, this value is always 0.
6	Parity Error Response	0	R/W	This bit enables parity error response. 0: PERR0 is not asserted. 1: PERR0 is asserted. When a parity error is detected, the Detected Parity Error bit is set to 1 even if this bit is cleared to 0.
5	VGA Palette Snoop	0	R	This bit enables VGA palette snooping. As the host logic does not support VGA palette snooping, this value is always 0.
4	Memory Write and Invalidate Enable	0	R/W	This bit enables the Memory Write and Invalidate command. In this module, do not change this from the initial value (0). 0: Memory write and invalidate command is disabled. 1: Memory write and invalidate command is enabled.
3	Special Cycle	0	R	This bit enables Special Cycle operation. As the host logic does not support the Special Cycle operation, this value is always 0.
2	Bus Master	0	R/W	This bit enables bus master operation. This is an enable signal for master access to the PCI bus. Set to 1 when accessing the SRAM on the system bus. Set this bit to 1 during initial setting of the host logic.
1	Memory Space	0	R/W	This bit enables access to the memory space. This is an enable signal for memory access specified in the PCI standard. Set to 1 when accessing registers. Set this bit to 1 during initial setting of the host logic.
0	I/O Space	0	R	This bit enables access to the I/O space. As the host logic does not accept I/O access, this value is always 0.

**51.6.4.3 Offset H'08 (Revision ID, Class Code)**



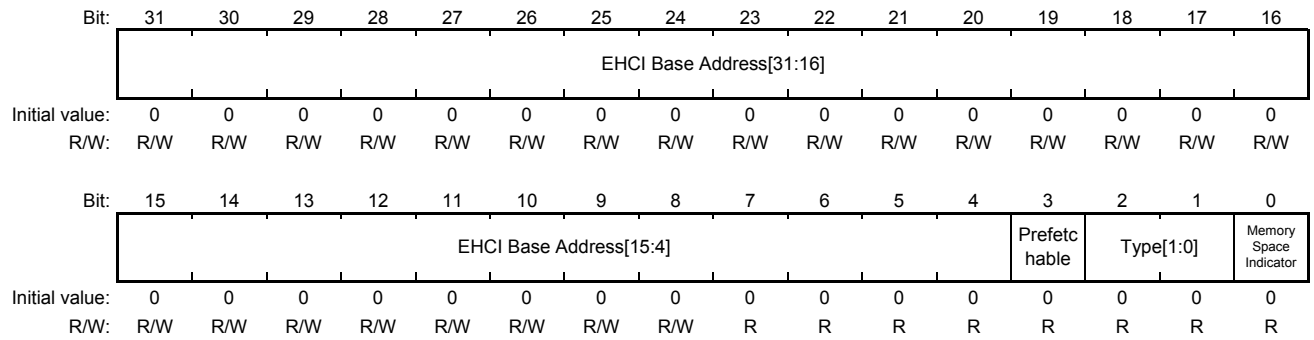
Bit	Bit Name	Initial Value	R/W	Description
31 to 24	Base Class [7:0]	H'0C	R	These bits indicate the base class specified in the PCI standard. The value is H'0C, which indicates a serial peripheral bus controller.
23 to 16	Sub Class [7:0]	H'03	R	These bits indicate the subclass specified in the PCI standard. The value is H'03, which indicates a USB device.
15 to 8	Programming I/F [7:0]	H'20	R	These bits indicate the program interface specified in the PCI standard. The value is H'20, which indicates EHCI.
7 to 0	Revision ID [7:0]	H'01	R	These bits indicate the revision of the host logic. The value is fixed to H'01.

#### 51.6.4.4 Offset H'0C (Cache Line Size, Latency Timer, Header Type, BIST)



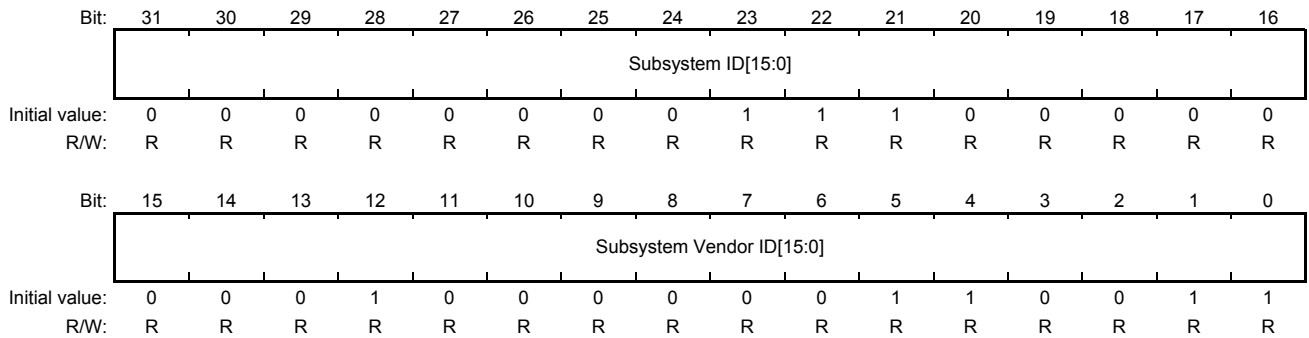
Bit	Bit Name	Initial Value	R/W	Description
31 to 24	BIST[7:0]	H'00	R	These bits are used for self testing. As the host logic does not support the self test function, this value is always H'00.
23 to 16	Header Type [7:0]	H'00	R	These bits notify the system of the header type. As the header type is Type 0, bits [22:16] are fixed to H'00. As the multifunction capability is not supported, bit 23 is fixed to 0.
15 to 8	Latency Timer [7:0]	H'44	R/W[7:2] R[1:0]	These bits notify the system of the latency timer. The lowest two bits are fixed to B'00.
7 to 0	Cache Line Size [7:0]	H'00	R/W	These bits notify the system of the cache line size.

**51.6.4.5 Offset H'10 (EHCI Base Address)**



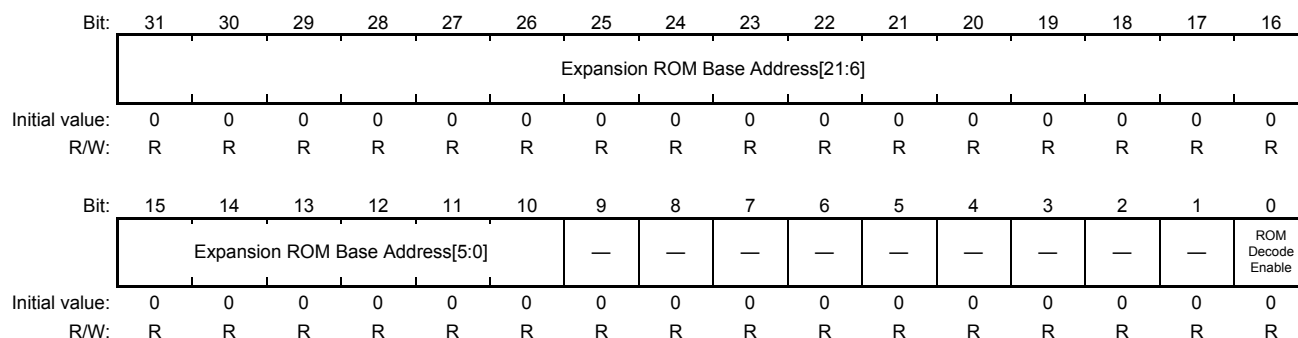
Bit	Bit Name	Initial Value	R/W	Description
31 to 4	EHCI Base Address[31:4]	H'000 000	R/W[31:8] R[7:4]	Bits [31:8] specify the base address of the operational registers. Specify the base address of the operational registers determined by the system during initialization. Bits [7:4] are fixed to H'0, which indicates that the operational registers are allocated to a 256-byte address space.
3	Prefetchable	0	R	As the host logic does not support prefetching in memory read cycles, this bit is fixed to 0.
2, 1	Type[1:0]	00	R	These bits are fixed to B'00, which indicates that the base address of the EHCI operational registers has a 32-bit width and can be allocated to any location in a 32-bit memory space.
0	Memory Space Indicator	0	R	This bit is fixed to 0, which indicates that the EHCI operational registers are mapped to the system memory space.

**51.6.4.6 Offset H'2C (Subsystem Vendor ID, Subsystem ID)**



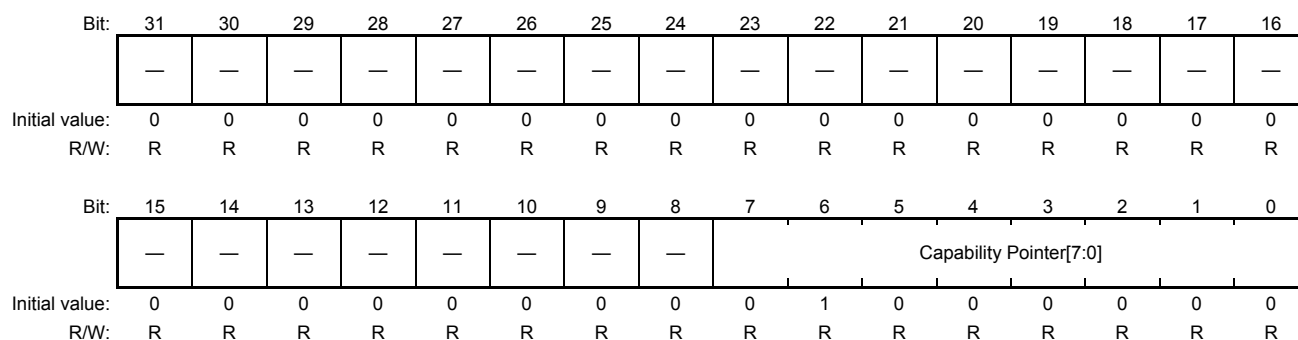
Bit	Bit Name	Initial Value	R/W	Description
31 to 16	Subsystem ID [15:0]	H'00C0	R	This register indicates the device type. This is used to select a driver that operates the device as specified in the PCI standard. This register does not need to be used in the embedded host.
15 to 0	Subsystem Vendor ID [15:0]	H'1033	R	This register indicates the vendor of the device. This is used to select a driver that operates the device as specified in the PCI standard. This register does not need to be used in the embedded host.

**51.6.4.7 Offset H'30 (Expansion ROM Base Address)**



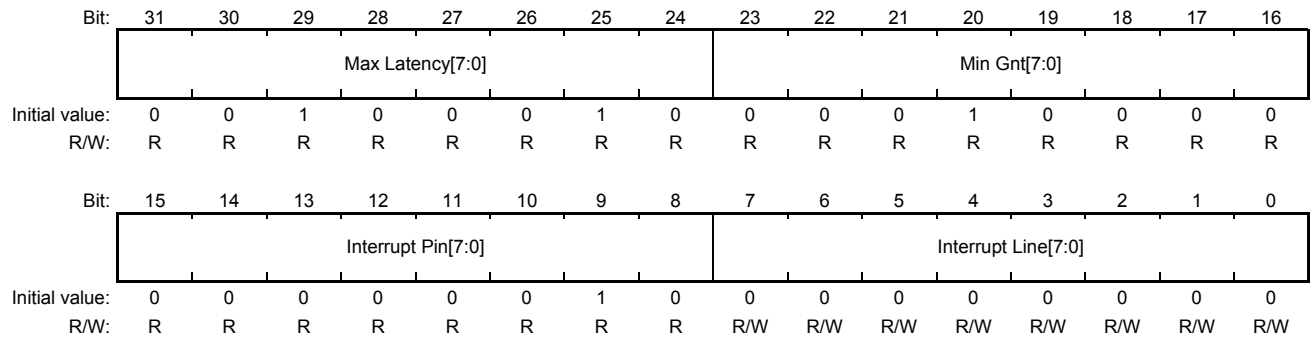
Bit	Bit Name	Initial Value	R/W	Description
31 to 10	Expansion ROM Base Address[21:0]	H'000000	R	As decoding of expansion ROM is prohibited, these bits are always read as H'000000. These bits cannot be written to.
9 to 1	—	All 0	R	Reserved (Don't care)
0	ROM Decode Enable	0	R	As decoding of expansion ROM is prohibited, this bit is always read as 0. This bit cannot be written to.

**51.6.4.8 Offset H'34 (Capability Pointer)**



Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved (Don't care)
7 to 0	Capability Pointer[7:0]	H'40	R	These bits hold the pointer to the capability identifier. As the pointer is set to H'40 in the host logic, this value is set to H'40.

**51.6.4.9 Offset H'3C (Interrupt Line, Interrupt Pin, Min gnt, Max Latency)**



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	Max Latency [7:0]	H'22	R	These bits indicate the maximum frequency of PCI bus acquisition. As the maximum frequency is set to H'22 in the host logic, this value is set to H'22.
23 to 16	Min Gnt[7:0]	H'10	R	These bits indicate the minimum burst transfer time. As the minimum time is set to H'10 in the host logic, this value is H'10.
15 to 8	Interrupt Pin [7:0]	H'02	R	These bits indicate the pin for outputting interrupts. As INTB is used, this value is fixed to H'02.
7 to 0	Interrupt Line [7:0]	H'00	R/W	These bits indicate the interrupt line. In this module, do not change this from the initial value (H'00).



### 51.6.4.10 Offset H'40 (Capability Identifier, Next Item Pointer, Power Management Capabilities)

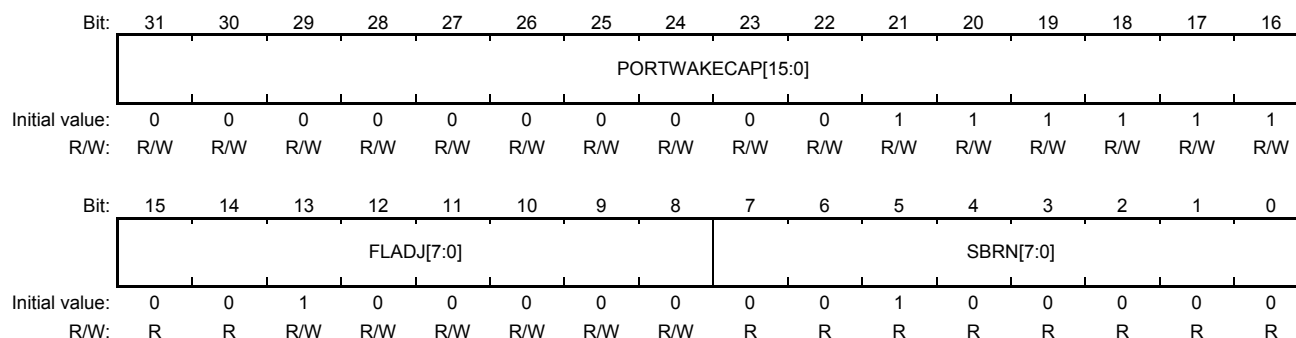
Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Power Management Capabilities															
	PME Support[4:0]				D2 Support	D1 Support	AUX Current[2:0]		DSI	—	PME CLK	Version[2:0]				
Initial value:	0	1	1	1	1	1	1	0	0	0	0	0	0	0	1	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Next Item Pointer[7:0]							Capability Identifier[7:0]								
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31	PME Support[4:0]	0	R	This bit indicates whether the D3 cold state is supported. As the D3 cold state is not supported, this value is fixed to 0.
30 to 27		1111	R	These bits are fixed to B'1111, which indicates that PME interrupt generation is supported in all PCI power states (D0 to D3).
26	D2 Support	1	R	This bit is fixed to 1, which indicates that PCI power state D2 is supported.
25	D1 Support	1	R	This bit is fixed to 1, which indicates that PCI power state D1 is supported.
24 to 22	AUX Current[2:0]	000	R	These bits indicate the necessary current for 3.3-V auxiliary power supply. As PME interrupt generation from the D3 cold state is not supported, this value is fixed to B'000.
21	DSI	0	R	This bit is fixed to 0, which indicates that special initialization is not necessary for power management.
20	—	0	R	Reserved
19	PME CLK	0	R	This bit is fixed to 0, which indicates that PCLK is not necessary for PME interrupt generation.
18 to 16	Version[2:0]	010	R	These bits are fixed to B'010, which indicates that the host logic conforms to "PCI power management interface specification release 1.1".
15 to 8	Next Item Pointer[7:0]	H'00	R	These bits are fixed to H'00, which indicates that the next item does not exist.
7 to 0	Capability Identifier[7:0]	H'01	R	These bits indicate the power management register ID. The value is fixed to H'01.

### 51.6.4.11 Offset H'44 (Power Management Control/Status, PMCSR Bridge Support Extensions)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Data								PMCSR Bridge Support Extensions							
	Data[7:0]								BPCC Enable	B2_B3	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Power Management Control/Status															
	PME Status	Data Scale[1:0]	Data Select[3:0]			PME Enable	—	—	—	—	—	—	—	Power State[1:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R	R	R	R	R/W	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	Data[7:0]	H'00	R	The value of these bits is H'00. This is an optional field in the PCI standard, and the host logic does not support it.
23	BPCC Enable	0	R	The value of this bit is 0. This is a bit for the bridge and the host logic does not support it.
22	B2_B3	0	R	The value of this bit is 0. This is a bit for the bridge and the host logic does not support it.
21 to 16	—	All 0	R	Reserved The write value should always be 0.
15	PME Status	0	R/W	This bit indicates the PME interrupt state. It is set to 1 when the PME generation condition is satisfied. Writing 1 from the PCI bus clears this bit to 0.
14, 13	Data Scale[1:0]	00	R	The value of these bits is B'00. This is an optional field in the PCI standard, and the host logic does not support it.
12 to 9	DSEL[3:0]	H'0	R	Data Select The value of these bits is H'0. This is an optional field in the PCI standard, and the host logic does not support it.
8	PME Enable	0	R/W	This bit specifies whether to use external pin PME. Setting this bit to 1 generates a PME interrupt when operation returns from the power management state.
7 to 2	—	All 0	R	Reserved The write value should always be 0.
1, 0	Power State[1:0]	00	R/W	These bits indicate the power state of the PCI as follows. 00: D0 state 01: D1 state 10: D2 state 11: D3 hot state

**51.6.4.12 Offset H'60 (SBRN, FLADJ, PORTWAKECAP)**

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	PORTWAKECAP[15:0]	H'003F	R/W	These bits specify a mask to select from the connected devices the port to be used for a wakeup event. This setting does not affect the actual operation of the host logic. This module has only one port and this register does not need to be used.
15 to 8	FLADJ[7:0]	H'20	R[7:6] R/W[5:0]	These bits adjust the length of a micro-frame in 16-HS bit time units. The initial value is H'20 (60000d HS bit time).
7 to 0	SBRN[7:0]	H'20	R	These bits indicate the serial bus release number. The value is fixed to H'20.

**51.6.4.13 Offset H'E0 (EXT1)**

This register is the same as the EXT1 register located in the OHCI configuration space. Refer to the description of the OHCI configuration register.

**51.6.4.14 Offset H'E4 (EXT2)**

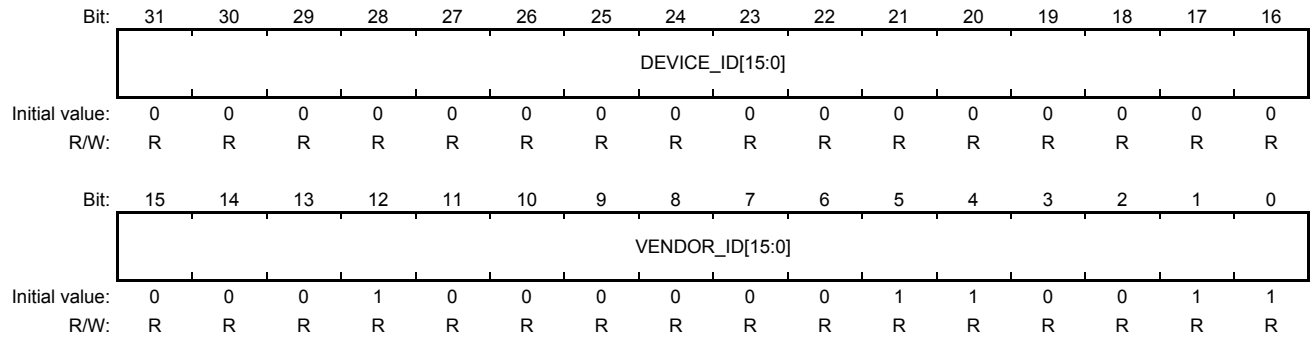
This register is the same as the EXT2 register located in the OHCI configuration space. Refer to the description of the OHCI configuration register.

Note that bit 0 (EHCI\_mask) cannot be accessed from the EHCI side.

### 51.6.5 PCI Configuration Registers for AHB-PCI Bridge

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

#### 51.6.5.1 Offset H'00 (Vendor ID, Device ID)



Bit	Bit Name	Initial Value	R/W	Description
31 to 16	DEVICE_ID [15:0]	H'0000	R	This register indicates the device type. This is used to select a driver that operates the device as specified in the PCI standard. This register does not need to be used in the embedded host.
15 to 0	VENDOR_ID [15:0]	H'1033	R	This register indicates the vendor of the device. This is used to select a driver that operates the device as specified in the PCI standard. This register does not need to be used in the embedded host. It is always read as H'1033.

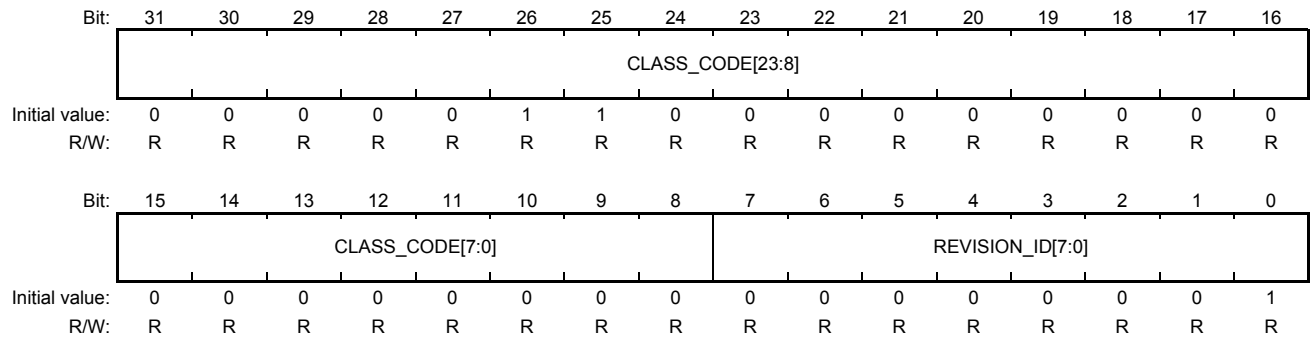
## 51.6.5.2 Offset H'04 (Command, Status)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DETPERR	SIGSERR	REMAPORT	RETABORT	SIGTABORT	DEVTIM[1:0]		MDPERR	FBTB CAP	—	66M CAP	CAP LIST	—	—	—	—
Initial value:	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	FBTB EN	SERR EN	STEP CTR	PERR EN	VGA PSNP	MWINV EN	SPECI ALC	MASTE REN	MEME N	IOEN
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R	R/W	R	R	R	R/W	R/W	R

Bit	Bit Name	Initial Value	R/W	Description
31	DETPERR	0	R/W	This is a status bit for parity error. This bit is set when an address or data parity error is detected. Writing 1 clears this bit. 0: Parity error has not been detected. 1: Parity error has been detected.
30	SIGSERR	0	R/W	This is a status bit for SERR. This bit is set when a system error occurs. Writing 1 clears this bit. 0: SERR# has not been asserted. 1: SERR# has been asserted.
29	REMAPORT	0	R/W	This is a status bit for Master Abort. This bit is set when Master Abort is received. Writing 1 clears this bit. 0: Master Abort has not been received. 1: Master Abort has been received.
28	RETABORT	0	R/W	This is a status bit for Master Target Abort. This bit is set when Target Abort is received. Writing 1 clears this bit. 0: Target Abort has not been received. 1: Target Abort has been received.
27	SIGTABORT	0	R/W	This is a status bit for Slave Target Abort. This bit is set when Target Abort is transmitted. Writing 1 clears this bit. 0: Target Abort has not been transmitted. 1: Target Abort has been transmitted.
26, 25	DEVTIM[1:0]	01	R	These bits indicate the DEVSEL response speed. The value is fixed to B'01 (Medium Mode).
24	MDPERR	0	R/W	This bit is set when a parity error is detected in master operation. Writing 1 clears this bit. 0: Parity error has not been detected. 1: Parity error has been detected.

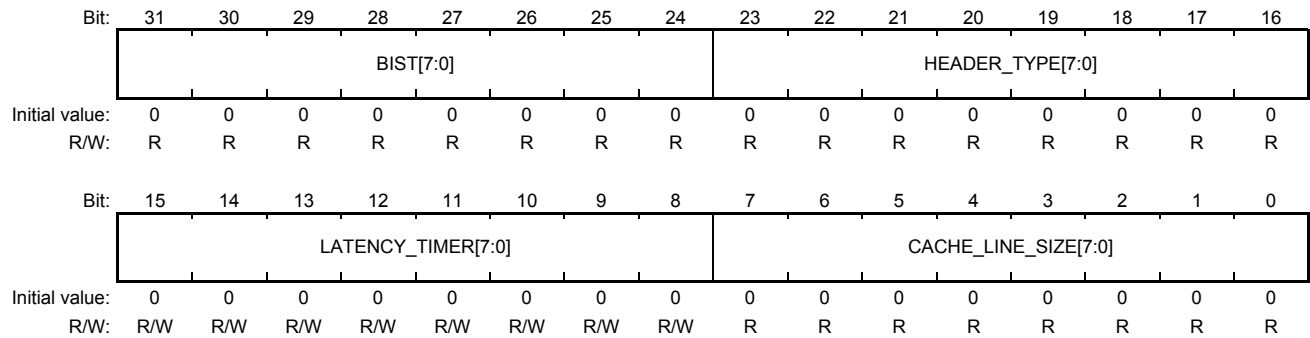
Bit	Bit Name	Initial Value	R/W	Description
23	FBTBCAP	0	R	This bit indicates whether Fast Back to Back transactions are supported. The value is fixed to 0. (Fast Back to Back transactions are not supported.)
22	—	0	R	Reserved The write value should always be 0.
21	66MCAP	0	R	This bit indicates whether 66-MHz operation is supported. The value is fixed to 0. (66-MHz operation is not supported.)
20	CAPLIST	0	R	This bit indicates whether the capabilities list is supported. The value is fixed to 0. (The capabilities list is not supported.)
19 to 10	—	All 0	R	Reserved The write value should always be 0.
9	FBTBEN	0	R	This bit enables Fast Back to Back transactions. The value is fixed to 0.
8	SERREN	0	R/W	This bit specifies the operation when a system error is detected. In this module, set to 1 during initial setting. 0: Ignored (initial value) 1: SERR# is asserted.
7	STEPCTR	0	R	This bit controls address stepping. The value is fixed to 0. (Address stepping is not done.)
6	PERREN	0	R/W	This bit specifies the operation when a parity error is detected. In this module, set to 1 during initial setting. 0: Ignored (initial value) 1: PERR# is asserted.
5	VGAPSNP	0	R	This bit enables VGA palette snooping. The value is fixed to 0.
4	MWINVEN	0	R	This bit enables the Memory Write and Invalidate command. The value is fixed to 0.
3	SPECIALC	0	R	This bit enables the Special Cycle operation. The value is fixed to 0.
2	MASTEREN	0	R/W	This bit specifies the PCI master operation. In this module, set to 1 during initial setting. 0: Master operation is disabled (initial value). 1: Master operation is enabled.
1	MEMEN	0	R/W	This bit specifies the PCI slave operation. In this module, set to 1 during initial setting. 0: Memory cycles cannot be accepted (initial value) 1: Memory cycles can be accepted.
0	IOEN	0	R	This bit enables access to the I/O space. The value is fixed to 0.

**51.6.5.3 Offset H'08 (Revision ID, Class Code)**



Bit	Bit Name	Initial Value	R/W	Description
31 to 8	CLASS_CODE [23:0]	H'060000	R	The value of these bits is H'060000.
7 to 0	REVISION_ID [7:0]	H'01	R	The value of these bits is H'01.

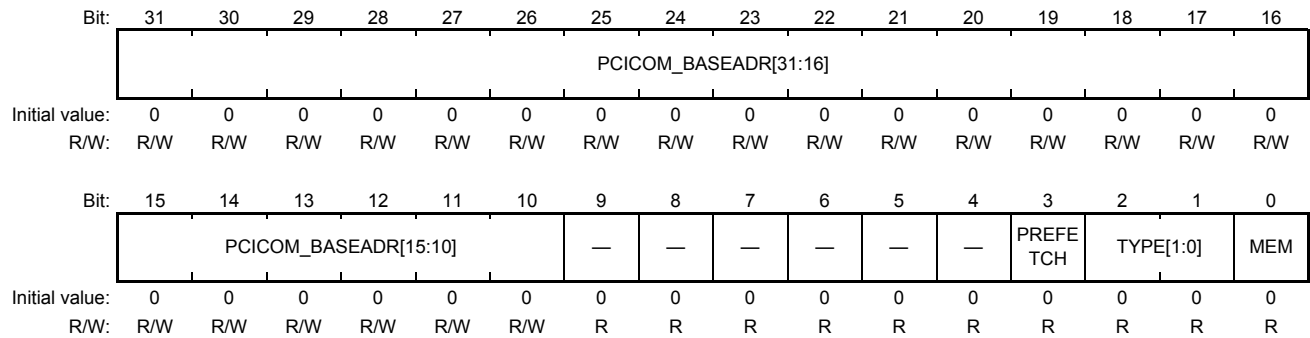
#### 51.6.5.4 Offset H'0C (Cache Line Size, Latency Timer, Header Type, BIST)



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	BIST[7:0]	H'00	R	The value of these bits is H'00 (BIST is not implemented).
23 to 16	HEADER_TYPER[7:0]	H'00	R	The value of these bits is H'00 (single function device).
15 to 8	LATENCY_TIMER[7:0]	H'00	R/W	These bits notify the system of the latency timer. This module does not use the latency timer; do not change this from the initial value (H'00).
7 to 0	CACHE_LINE_SIZE[7:0]	H'00	R	The value of these bits is H'00 (cache is not supported).



### 51.6.5.5 Offset H'10 (AHB-PCI Bridge Base Address)



Bit	Bit Name	Initial Value	R/W	Description
31 to 10	PCICOM_BA SEADR [31:10]	All 0	R/W	These bits specify the base address of the AHB-PCI bridge PCI communication register area. A 1-Kbyte area is necessary and the upper 24 bits specify the base address.
9 to 4	—	All 0	R	Reserved The write value should always be 0.
3	PREFETCH	0	R	This bit indicates whether data can be prefetched. The value is fixed to 0. (Data cannot be prefetched.)
2, 1	TYPE[1:0]	00	R	These bits indicate the base address type. The value is B'00. (The base address can be allocated to any location in a 4-Gbyte space.)
0	MEM	0	R	This bit indicates that the bits specified by the base address are in the memory space. The value is fixed to 0.

## 51.6.5.6 Offset H'14 (PCI-AHB WIN1 Base Address)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PCI_WIN1_				—	—	—	—	—	—	—	—	—	—	—	—
	BASEADR[31:28]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	PREFE	TYPE[1:0]		MEM
													TCH			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

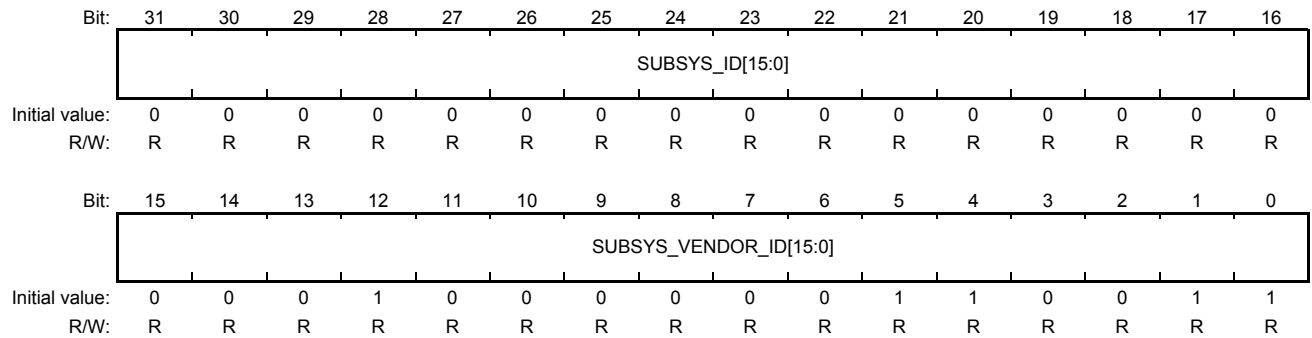
Bit	Bit Name	Initial Value	R/W	Description										
31 to 28	PCI_WIN1_B ASEADR [31:28]	H'0	R/W	<p>These bits specify the base address of PCI-AHB Window 1.</p> <p>For the PCI-AHB Window 1 space, a 256-Mbyte, 512-Mbyte, 1-Gbyte, or 2-Gbyte area can be made accessible through the setting of bits [11:10] (PCI_AHB_WIN1_SIZE) in the USBCTR register.</p> <table border="1"> <thead> <tr> <th>PCI-AHB Window 1 Space</th><th>AHB_BASEADR[31:28]</th></tr> </thead> <tbody> <tr> <td>256 Mbytes</td><td>The upper four bits (bits [31:28]) specify the base address.</td></tr> <tr> <td>512 Mbytes</td><td>The upper three bits (bits [31:29]) specify the base address.</td></tr> <tr> <td>1 Gbyte</td><td>The upper two bits (bits [31:30]) specify the base address.</td></tr> <tr> <td>2 Gbytes</td><td>The upper one bit (bit [31]) specifies the base address.</td></tr> </tbody> </table> <p>For details of register setting, refer to section 51.7, Register Accesses.</p>	PCI-AHB Window 1 Space	AHB_BASEADR[31:28]	256 Mbytes	The upper four bits (bits [31:28]) specify the base address.	512 Mbytes	The upper three bits (bits [31:29]) specify the base address.	1 Gbyte	The upper two bits (bits [31:30]) specify the base address.	2 Gbytes	The upper one bit (bit [31]) specifies the base address.
PCI-AHB Window 1 Space	AHB_BASEADR[31:28]													
256 Mbytes	The upper four bits (bits [31:28]) specify the base address.													
512 Mbytes	The upper three bits (bits [31:29]) specify the base address.													
1 Gbyte	The upper two bits (bits [31:30]) specify the base address.													
2 Gbytes	The upper one bit (bit [31]) specifies the base address.													
27 to 4	—	All 0	R	<p>Reserved</p> <p>The write value should always be 0.</p>										
3	PREFETCH	1	R	<p>This bit indicates whether data can be prefetched.</p> <p>The value is fixed to 1. (Data can be prefetched.)</p>										
2, 1	TYPE[1:0]	00	R	<p>These bits indicate the base address type.</p> <p>The value is B'00. (The base address can be allocated to any location in a 4-Gbyte space.)</p>										
0	MEM	0	R	<p>This bit indicates that the field specified by the base address is in the memory space.</p> <p>The value is fixed to 0.</p>										

## 51.6.5.7 Offset H'18 (PCI-AHB WIN2 Base Address)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PCI_WIN2_				—	—	—	—	—	—	—	—	—	—	—	—
	BASEADR[31:28]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	PREFE	TYPE[1:0]		MEM
													TCH			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

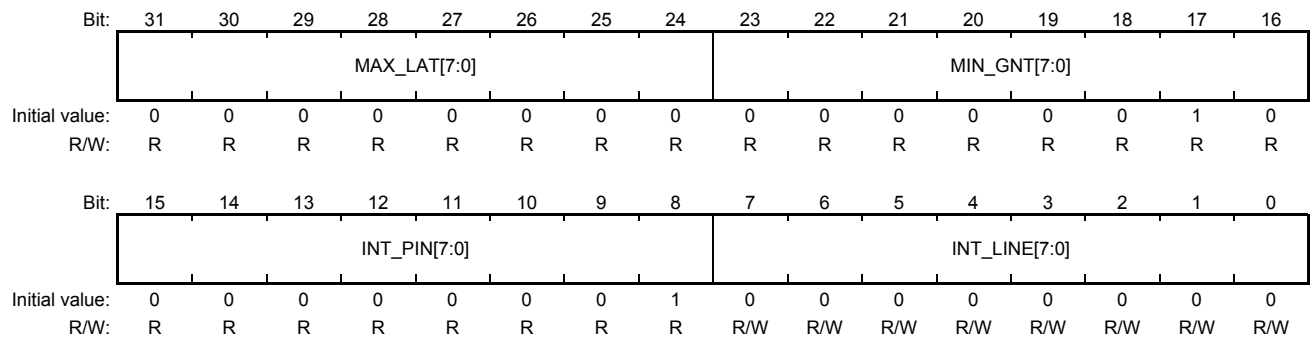
Bit	Bit Name	Initial Value	R/W	Description
31 to 28	PCI_WIN2_B ASEADR [31:28]	H'0	R/W	These bits specify the base address of PCI-AHB Window 2. In this module, a 256-Mbyte area is necessary, and the upper four bits specify the base address.
27 to 4	—	All 0	R	Reserved The write value should always be 0.
3	PREFETCH	0	R	This bit indicates whether data can be prefetched.
2, 1	TYPE[1:0]	00	R	These bits indicate the base address type. The value is B'00. (The base address can be allocated to any location in a 4-Gbyte space.)
0	MEM	0	R	This bit indicates that the bits specified by the base address are in the memory space. The value is fixed to 0.

**51.6.5.8 Offset H'2C (Subsystem Vendor ID, Subsystem ID)**



Bit	Bit Name	Initial Value	R/W	Description
31 to 16	SUBSYS_ID [15:0]	H'00	R	The value of these bits is H'0000.
15 to 0	SUBSYS_VENDOR_ID [15:0]	H'1033	R	The value of these bits is H'1033.

**51.6.5.9 Offset H'3C (Interrupt Line, Interrupt Pin, Min gnt, Max Latency)**



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	MAX_LAT[7:0]	H'00	R	The value of these bits is H'00. (No value is specified for the bus use frequency.)
23 to 16	MIN_GNT[7:0]	H'02	R	The value of these bits is H'02. (Requested latency timer: 16 burst).
15 to 8	INT_PIN[7:0]	H'01	R	The value of these bits is H'01. (INTA# is used).
7 to 0	INT_LINE[7:0]	H'00	R/W	These bits specify the interrupt line. In this module, do not change this from the initial value (H'00).

### 51.6.6 AHB-PCI Bridge PCI Communication Registers

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

#### 51.6.6.1 PCIAHB\_WIN1\_CTR Register

This register is used to make settings for access from the host logic to AHB.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	AHB_BASEADR[31:28]				—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	ENDIAN_CTR[2:0]			—	—	—	—	PREFETCH[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R/W	R/W	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description										
31 to 28	AHB_BASEADR[31:28]	H'0	R/W	<p>These bits specify the base address of the AHB bus for access from the host logic to PCI-AHB Window 1.</p> <p>For the PCI-AHB Window 1 space, a 256-Mbyte, 512-Mbyte, 1-Gbyte, or 2-Gbyte area can be made accessible through the setting of bits [11:10] (PCI_AHB_WIN1_SIZE) in the USBCTR register.</p> <table border="1"> <thead> <tr> <th>PCI-AHB Window 1 Space</th> <th>AHB_BASEADR[31:28]</th> </tr> </thead> <tbody> <tr> <td>256 Mbytes</td> <td>The upper four bits (bits [31:28]) specify the base address.</td> </tr> <tr> <td>512 Mbytes</td> <td>The upper three bits (bits [31:29]) specify the base address.</td> </tr> <tr> <td>1 Gbyte</td> <td>The upper two bits (bits [31:30]) specify the base address.</td> </tr> <tr> <td>2 Gbytes</td> <td>The upper one bit (bit [31]) specifies the base address.</td> </tr> </tbody> </table> <p>For details of register setting, refer to section 51.7, Register Accesses.</p>	PCI-AHB Window 1 Space	AHB_BASEADR[31:28]	256 Mbytes	The upper four bits (bits [31:28]) specify the base address.	512 Mbytes	The upper three bits (bits [31:29]) specify the base address.	1 Gbyte	The upper two bits (bits [31:30]) specify the base address.	2 Gbytes	The upper one bit (bit [31]) specifies the base address.
PCI-AHB Window 1 Space	AHB_BASEADR[31:28]													
256 Mbytes	The upper four bits (bits [31:28]) specify the base address.													
512 Mbytes	The upper three bits (bits [31:29]) specify the base address.													
1 Gbyte	The upper two bits (bits [31:30]) specify the base address.													
2 Gbytes	The upper one bit (bit [31]) specifies the base address.													
27 to 9	—	All 0	R	<p>Reserved</p> <p>The write value should always be 0.</p>										
8 to 6	ENDIAN_CTR[2:0]	000	R/W	<p>These bits specify how to convert endian for the AHB bus. Do not modify this value except for initial setting.</p> <p>To use little endian : B'000                      To use big endian : B'010                      000: No conversion                      001: Access type data swap                      010: Byte data swap                      011: Halfword swap                      100: Address conversion                      Others: Setting prohibited</p>										

Bit	Bit Name	Initial Value	R/W	Description
5 to 2	—	All 0	R	Reserved The write value should always be 0.
1, 0	PREFETCH [1:0]	00	R/W	These bits specify whether to prefetch data in the AHB bus when the host logic issues a read request. In this module, set to B'11 during initial setting and do not modify this value. 00: Prefetch is disabled. 01: Prefetch is enabled (up to 4 burst). 10: Prefetch is enabled (up to 8 burst) 11: Prefetch is enabled (up to 16 burst)

### 51.6.6.2 PCIAHB\_WIN2\_CTR Register

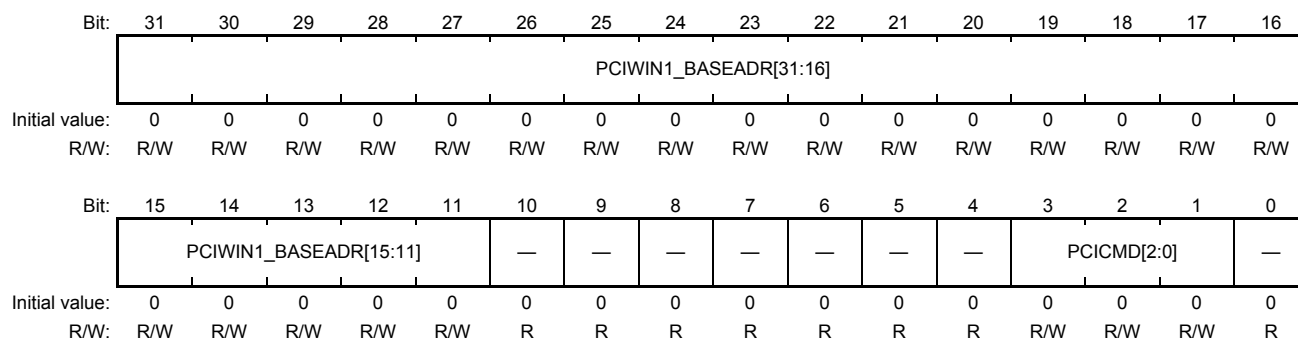
This register is used to make settings for access from the host logic to AHB.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	AHB_BASEADR[31:28]				—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	ENDIAN_CTR[2:0]			—	—	—	—	PREFETCH[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R/W	R/W	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 28	AHB_BASEADR[31:28]	H'0	R/W	<p>These bits specify the base address of the AHB bus for access from the host logic to PCI-AHB Window 2.</p> <p>For the PCI-AHB Window 2 space, a 256-Mbyte area is accessible when bit 9 (PCI_AHB_WIN2_EN) in the USBCTR register is 1, and the upper four bits specify the base address.</p> <p>For details of register setting, refer to section 51.7, Register Accesses.</p>
27 to 9	—	All 0	R	<p>Reserved</p> <p>The write value should always be 0.</p>
8 to 6	ENDIAN_CTR [2:0]	000	R/W	<p>These bits specify how to convert endian for the AHB bus.</p> <p>Do not modify this value except for initial setting.</p> <p>To use little endian: B'000</p> <p>To use big endian: B'010</p> <p>000: No conversion</p> <p>001: Access type data swap</p> <p>010: Byte data swap</p> <p>011: Halfword swap</p> <p>100: Address conversion</p> <p>Others: Setting prohibited</p>
5 to 2	—	All 0	R	<p>Reserved</p> <p>The write value should always be 0.</p>
1, 0	PREFETCH [1:0]	00	R/W	<p>These bits specify whether to prefetch data in the AHB bus when the host logic issues a read request.</p> <p>In this module, set to B'11 during initial setting and do not modify this value.</p> <p>00: Prefetch is disabled.</p> <p>01: Prefetch is enabled (up to 4 burst).</p> <p>10: Prefetch is enabled (up to 8 burst).</p> <p>11: Prefetch is enabled (up to 16 burst).</p>

### 51.6.6.3 AHBPCI\_WIN1\_CTR Register

This register is used to make necessary settings for access to the PCI configuration space.

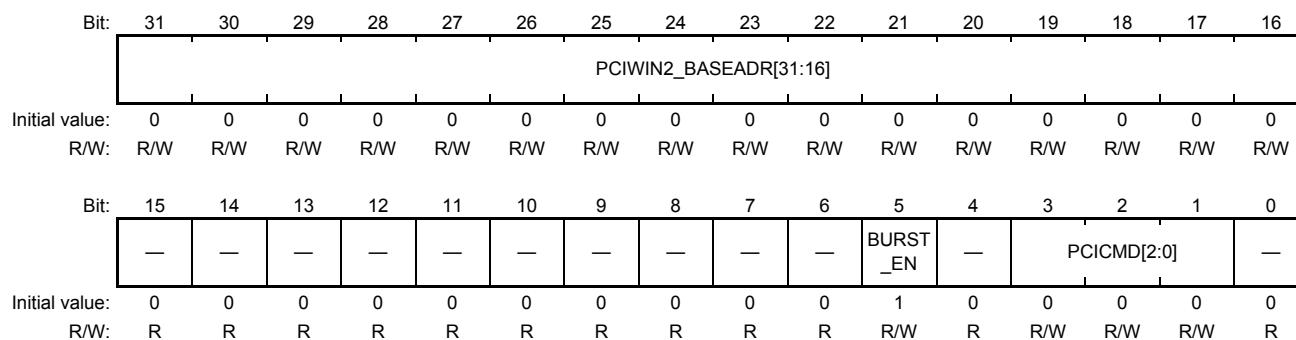


Bit	Bit Name	Initial Value	R/W	Description
31 to 11	PCIWIN1_BA SEADR [31:11]	All 0	R/W	These bits specify the base address of the PCI bus for access from AHB to AHB-PCI Window 1.  This register should be set when the PCI configuration space for the host logic or for the AHB-PCI bridge is accessed. For details of settings, refer to section 51.7, Register Accesses.
10 to 4	—	All 0	R	Reserved  The write value should always be 0.
3 to 1	PCICMD[2:0]	000	R/W	These bits specify the type of PCI bus cycle.  In this module, set to B'101 during initial setting and do not modify this value.  000: Interrupt Acknowledge or Special Cycle 001: I/O Read or I/O Write 011: Memory Read or Memory Write 101: Configuration Read or Configuration Write 110: Memory Read Multiple or Memory Write 111: Memory Read Line or Memory Write Others: Setting prohibited
0	—	0	R	Reserved  The write value should always be 0.



### 51.6.6.4 AHBPCI\_WIN2\_CTR Register

This register is used to make necessary settings for access to the OHCI operational register area.



Bit	Bit Name	Initial Value	R/W	Description
31 to 16	PCIWIN2_BA SEADR [31:16]	H'0000	R/W	These bits specify the base address of the PCI bus for access from AHB to AHB-PCI Window 2.  This register is used for access to the OHCI operational register area. For details of settings, refer to section 51.7, Register Accesses.
15 to 6	—	All 0	R	Reserved  The write value should always be 0.
5	BURST_EN	1	R/W	This bit enables burst transfer to the PCI bus  In this module, clear to 0 during initial setting and do not modify this value.  0: Burst transfer is disabled. 1: Burst transfer is enabled.
4	—	0	R	Reserved  The write value should always be 0.
3 to 1	PCICMD[2:0]	000	R/W	These bits specify the type of PCI bus cycle.  In this module, set to B'011 during initial setting and do not modify this value.  001: I/O Read or I/O Write 011: Memory Read or Memory Write 110: Memory Read Multiple or Memory Write 111: Memory Read Line or Memory Write Others: Setting prohibited
0	—	0	R	Reserved  The write value should always be 0.

### 51.6.6.5 PCI\_INT\_ENABLE Register

This register enables or disables each interrupt source indicated in the PCI\_INT\_STATUS register. When an interrupt source is disabled, the interrupt signal is not asserted even when the interrupt source is generated and the corresponding bit in the PCI\_INT\_STATUS register is set to 1.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	USBH_P MEEN	—	USBH_I NTBEN	USBH_I NTAEN
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	PCIAHB _WIN2_I NTEN	PCIAHB _WIN1_I NTEN	—	—	—	—	—	—	RESERR _INTEN	SIGSER R_INTE N	PERR_I NTEN	REMA ORT_IN TEN	RETA BO RT_IN TEN	SIGTAB ORT_IN TEN
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 20	—	All 0	R	Reserved The write value should always be 0.
19	USBH_PMEEN	0	R/W	This bit enables or disables the interrupt source indicated in bit 19 (USBH_PME) in PCI_INT_STATUS. 0: Disabled 1: Enabled
18	—	0	R	Reserved The write value should always be 0.
17	USBH_INTBEN	0	R/W	This bit enables or disables the interrupt source indicated in bit 17 (USBH_INTB) in PCI_INT_STATUS. 0: Disabled 1: Enabled
16	USBH_INTAEN	0	R/W	This bit enables or disables the interrupt source indicated in bit 16 (USBH_INTA) in PCI_INT_STATUS. 0: Disabled 1: Enabled
15, 14	—	All 0	R	Reserved The write value should always be 0.
13	PCIAHB_WIN2_INTEN	0	R/W	This bit enables or disables the interrupt source indicated in bit 13 (PCIAHB_WIN2_INT) in PCI_INT_STATUS. 0: Disabled 1: Enabled
12	PCIAHB_WIN1_INTEN	0	R/W	This bit enables or disables the interrupt source indicated in bit 12 (PCIAHB_WIN1_INT) in PCI_INT_STATUS. 0: Disabled 1: Enabled
11 to 6	—	All 0	R	Reserved The write value should always be 0.
5	RESERR_INTEN	0	R/W	This bit enables or disables the interrupt source indicated in bit 5 (RESERR_INT) in PCI_INT_STATUS. 0: Disabled 1: Enabled

Bit	Bit Name	Initial Value	R/W	Description
4	SIGSERR_IN TEN	0	R/W	This bit enables or disables the interrupt source indicated in bit 4 (SIGSERR_INT) in PCI_INT_STATUS. 0: Disabled 1: Enabled
3	PERR_INTE N	0	R/W	This bit enables or disables the interrupt source indicated in bit 3 (PERR_INT) in PCI_INT_STATUS. 0: Disabled 1: Enabled
2	REMARBOR T_INTEN	0	R/W	This bit enables or disables the interrupt source indicated in bit 2 (REMABOOT_INT) in PCI_INT_STATUS. 0: Disabled 1: Enabled
1	RETARBORT _INTEN	0	R/W	This bit enables or disables the interrupt source indicated in bit 1 (RETABORT_INT) in PCI_INT_STATUS. 0: Disabled 1: Enabled
0	SIGTARBOR T_INTEN	0	R/W	This bit enables or disables the interrupt source indicated in bit 0 (SIGTABORT_INT) in PCI_INT_STATUS. 0: Disabled 1: Enabled

**51.6.6.6 PCI\_INT\_STATUS Register**

This register indicates the state of interrupt sources in the AHB-PCI bridge and the state of interrupt signals from the host logic.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	USBH_PME	—	USBH_INTB	USBH_INTA
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	PCIAHB_WIN2_INT	PCIAHB_WIN1_INT	—	—	—	—	—	—	RESER_R_INT	SIGSER_R_INT	PERR_INT	REMAORT_INT	RETAORT_INT	SIGTABORT_INT
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 20	—	All 0	R	Reserved The write value should always be 0.
19	USBH_PME	0	R	This bit indicates the state of the PME# interrupt from the host logic. The interrupt can be cleared from the host logic. 0: PME interrupt has not occurred. 1: PME interrupt has occurred.
18	—	0	R	Reserved The write value should always be 0.
17	USBH_INTB	0	R	This bit indicates the state of the INTB# interrupt from the host logic. The interrupt can be cleared from the host logic. 0: INTB interrupt has not occurred. 1: INTB interrupt has occurred.
16	USBH_INTA	0	R	This bit indicates the state of the INTA# interrupt from the host logic. The interrupt can be cleared from the host logic. 0: INTA interrupt has not occurred. 1: INTA interrupt has occurred.
15, 14	—	All 0	R	Reserved The write value should always be 0.
13	PCIAHB_WIN2_INT	0	R/W	This bit indicates that an AHB bus error has occurred in PCIAHB Window 2. Writing 1 clears this bit. 0: AHB bus error has not occurred. 1: AHB bus error has occurred.
12	PCIAHB_WIN1_INT	0	R/W	This bit indicates that an AHB bus error has occurred in PCIAHB Window 1. Writing 1 clears this bit. 0: AHB bus error has not occurred. 1: AHB bus error has occurred.

Bit	Bit Name	Initial Value	R/W	Description
11 to 6	—	All 0	R	Reserved The write value should always be 0.
5	RESERR_IN T	0	R/W	This bit indicates the state of the interrupt source caused by SERR# input. Writing 1 clears this bit. 0: SERR# assertion has not been detected. 1: SERR# assertion has been detected.
4	SIGSERR_IN T	0	R/W	This bit indicates the state of the interrupt source caused by SERR# output. Writing 1 clears this bit. 0: SERR# has not been asserted. 1: SERR# has been asserted.
3	PERR_INT	0	R/W	This bit indicates the state of the interrupt source caused by PERR# input/output. Writing 1 clears this bit. 0: PERR# has not been asserted. 1: PERR# has been asserted.
2	REMABORT_ INT	0	R/W	This bit indicates that Master Abort has been received in PCI master operation. Writing 1 clears this bit. 0: Master Abort has not been received. 1: Master Abort has been received.
1	RETABORT_ INT	0	R/W	This bit indicates that Target Abort has been received in PCI master operation. Writing 1 clears this bit. 0: Target Abort has not been received. 1: Target Abort has been received.
0	SIGTABORT_ INT	0	R/W	This bit indicates that Target Abort has been sent in PCI target operation. Writing 1 clears this bit. 0: Target Abort has not been sent. 1: Target Abort has been sent.

### 51.6.6.7 AHB\_BUS\_CTR Register

This register specifies the AHB master and slave functions of the host logic.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SMODE_READY_CTR	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	MMODE_HBUSREQ	—	—	—	—	MMODE_WR_INCR	MMODE_BYTEBURST	MMODE_HTRANS
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 18	—	All 0	R	Reserved The write value should always be 0.
17	SMODE_READY_CTR	1	R/W	This bit controls the wait operation in AHB slave operation. Set this bit to 0 in a system that uses RETRY or SPLIT. Do not modify this value except for initial setting. 0: Wait is controlled with HRESP = RETRY. 1: Wait is controlled with HREADY = 0.
16 to 8	—	All 0	R	Reserved The write value should always be 0.
7	MMODE_HBUSREQ	0	R/W	This bit specifies the timing of HBUSREQ deassertion in AHB master operation. In this module, set to 1 during initial setting and do not modify this value. 0: Deasserted in the last address phase of the cycle. 1: Deasserted with the first timing of HGRANT = 1 and HREADY = 1.
6 to 3	—	0	R	Reserved The write value should always be 0.
2	MMODE_WR_INCR	0	R/W	This bit specifies the condition of using an undefined-length burst for write transfer in AHB master operation. In this module, set to 1 during initial setting and do not modify this value. 0: INCR is always used except when the transfer count is 4, 8, or 16. 1: INCR4, INCR8, and INCR16 are generally used, and INCR is used only when the remaining data is two to three beats.
1	MMODE_BYTEBURST	0	R/W	This bit controls burst transfer for 16-bit or 8-bit transfer in AHB master operation. In this module, set to 1 during initial setting and do not modify this value. 0: Burst transfer is enabled for 16-bit or 8-bit transfer. 1: Burst transfer is disabled for 16-bit or 8-bit transfer.

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Bit	Bit Name	Initial Value	R/W	Description
0	MMODE_HTRANS	0	R/W	<p>This bit specifies the operating mode for the HTRANS signal in AHB master operation.</p> <p>In this module, set to 1 during initial setting and do not modify this value.</p> <p>0: For divided cycles, NONSEQ is output continuously.</p> <p>1: For divided cycles, IDLE is inserted and the bus is requested again through HBUSREQ.</p>

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### 51.6.6.8 USBCTR Register

This register is used to make settings of the host logic.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	PCI_AHB_WIN1_SIZE[1:0]	PCI_AHB_WIN2_EN	DIRPD	—	—	—	—	—	—	PLL_RST	PCICLK_MASK	USBH_RST
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R	R	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 12	—	All 0	R	Reserved The write value should always be 0.
11, 10	PCI_AHB_WIN1_SIZE[1:0]	0	R/W	These bits control the PCI-AHB Window 1 area. For details, refer to section 51.7, Register Accesses. Do not modify this value except for initial setting. 00: 256 Mbytes 01: 512 Mbytes 10: 1 Gbyte 11: 2 Gbytes
9	PCI_AHB_WIN2_EN	0	R/W	This bit enables operation of PCI-AHB Window 2. For details, refer to section 51.7, Register Accesses. Do not modify this value except for initial setting. In this module, the PCI-AHB Window 2 area is fixed to 256 Mbytes. 0: PCI-AHB Window 2 is not available. 1: PCI-AHB Window 2 is available.
8	DIRPD	0	R/W	When this bit is set to 1, the host logic enters the direct power-down state. When 0 is written while this bit is 1, the host logic returns from the direct power-down state. For the setting of and return from the direct power-down state, refer to section 51.10.3, Direct Power-Down.  As well as this register, bit 12 (DIRPD) in the EPCTR register and the DIRPD input pin can be used to control the direct power-down state. 0: Normal operation 1: Direct power-down state
7 to 3	—	0	R	Reserved The write value should always be 0.



Bit	Bit Name	Initial Value	R/W	Description
2	PLL_RST	1	R/W	<p>This bit controls the reset signal supplied to the PLL.</p> <p>The PLL is used in common for the host logic and the UTMI+ logic. To stop the PLL operation, set this bit to 1.</p> <p>When both this bit and the PLL_RESET pin in the host logic are 1, a reset signal is issued to the PLL.</p> <p>Clearing (0) for either this bit or the PLL_RESET pin in the host logic cancels the reset signal for the PLL.</p> <p>0: PLL reset is canceled. 1: PLL reset is issued.</p>
1	PCICLK_MAS K	1	R/W	<p>This bit stops the PCI clock supply in the host logic.</p> <p>Note that the host logic cannot be accessed when this bit is set to 1.</p> <p>0: PCI clock is supplied. 1: PCI clock is stopped.</p>
0	USBH_RST	1	R/W	<p>This bit controls the reset signal supplied to the host logic.</p> <p>The host logic can be accessed a maximum of three PCLK clock cycles after the reset is canceled.</p> <p>0: Host logic reset is canceled. 1: Host logic reset is issued.</p>

### 51.6.6.9 PCI\_ARBITER\_CTR Register

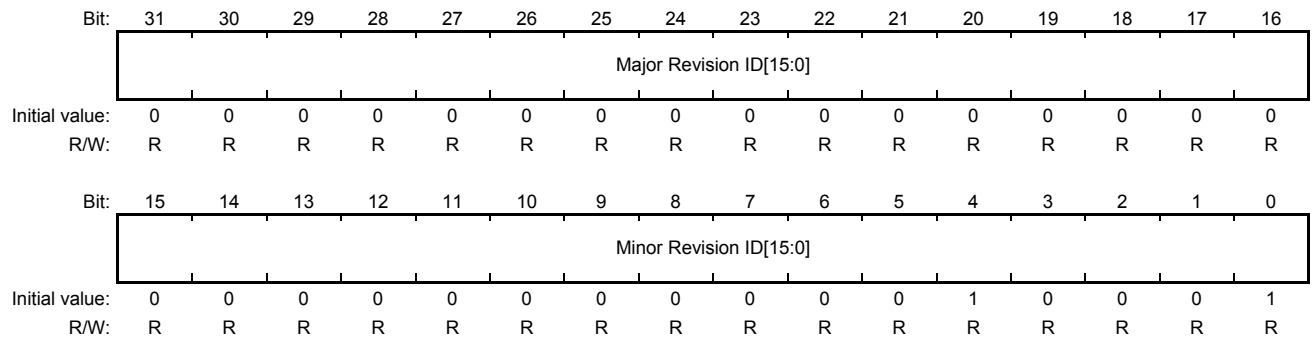
This register is used to make settings of the PCI bus arbitration function.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	—	—	—	PCIBP_MODE	—	—	—	—	—	—	—	—	—	—	PCIREQ1	PCIREQ0	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
R/W:	R	R	R	R/W	R	R	R	R	R	R	R	R	R	R	R/W	R/W	

Bit	Bit Name	Initial Value	R/W	Description
31 to 13	—	—	R	Reserved Do not change this from the initial value.
12	PCIBP_MODE	0	R/W	This bit specifies the master while the PCI bus is in the parking state. In this module, set to 1 during initial setting and do not modify this value. 0: This unit is the master in the bus parking state. 1: The master that made the last access is the master in the bus parking state.
11 to 2	—	All 0	R	Reserved The write value should always be 0.
1	PCIREQ1	0	R/W	This bit enables or disables the PCI bus request signal from the host logic. In this module, set to 1 during initial setting and do not modify this value. 0: Request signal is disabled. 1: Request signal is enabled.
0	PCIREQ0	0	R/W	This bit enables or disables the PCI bus request signal from this unit. In this module, set to 1 during initial setting and do not modify this value. 0: Request signal is disabled. 1: Request signal is enabled.

**51.6.6.10 PCI\_UNIT\_REV Register**

This register indicates the version of the AHB-PCI bridge macro.



Bit	Bit Name	Initial Value	R/W	Description
31 to 16	Major Revision ID [15:0]	H'0000	R	These bits indicate the major revision ID of this unit.
15 to 0	Minor Revision ID [15:0]	H'0011	R	These bits indicate the minor revision ID of this unit.

<b>RZ/G1H</b>	<b>RZ/G1N</b>
<b>RZ/G1M</b>	<b>RZ/G1E</b>

### 51.7 Register Accesses

The registers are accessed through the internal PCI bus. Thus, to provide accesses correctly through the AHB bus, the AHB bus memory space and PCI bus memory space in the USB should be mapped correctly. The PCI has two spaces: PCI configuration space to set the PCI bus transfer settings and base address settings in the PCI memory space and the PCI memory space to perform actual data transfers.

The accesses from the AHB to the host logic or master accesses from the host logic to the AHB are performed through the window area included in the AHB-PCI bridge. Figure 51.2 and Table 51.5 show the relationship between the register areas and window areas.

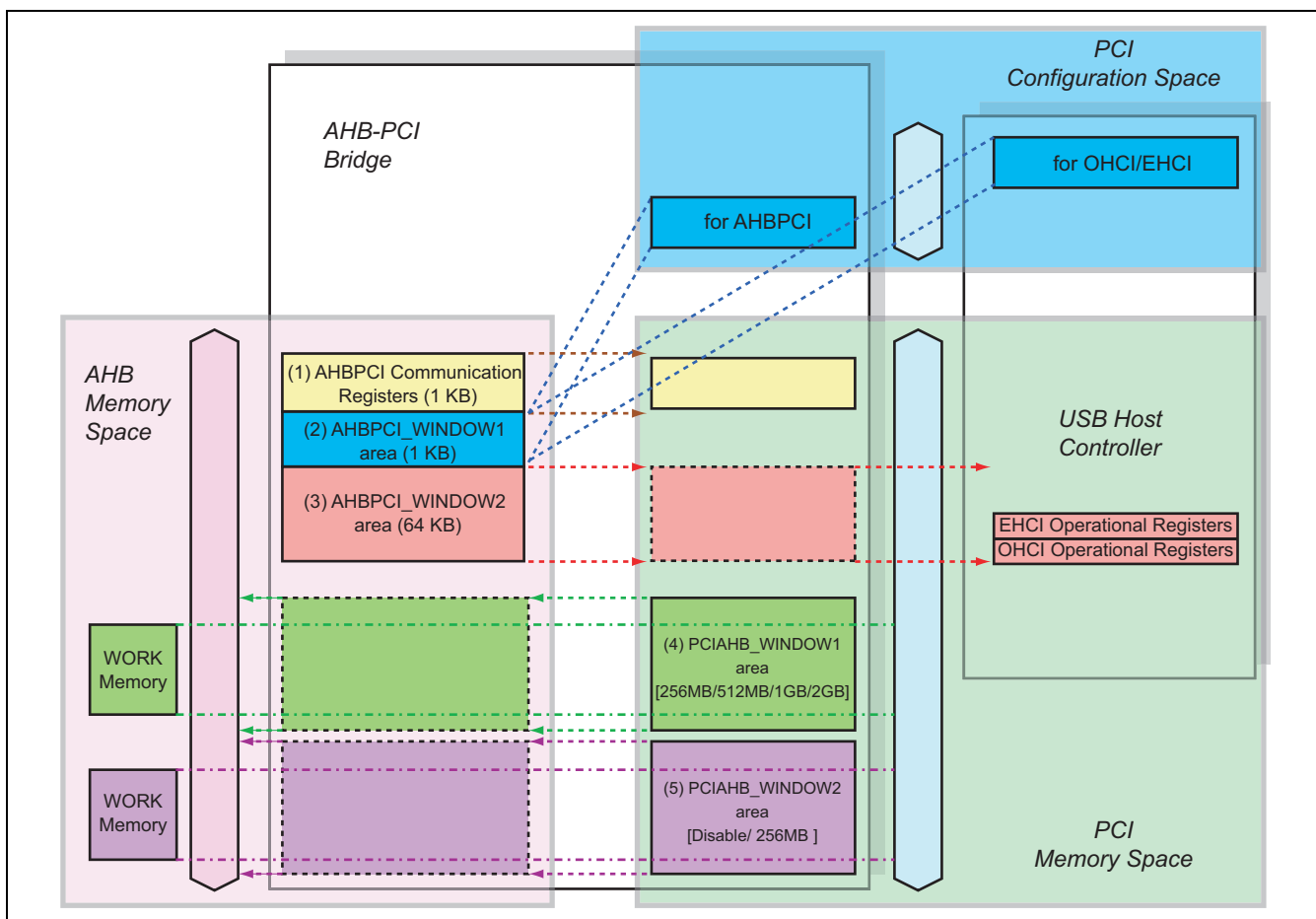


Figure 51.2 Mapping in AHB and PCI Spaces

**Table 51.5 Description of Each Area**

<b>AHB Areas</b>	<b>Size</b>	<b>Description</b>
(1) AHBPCI Communication Registers area	1 KB	Used for various AHB settings and base address settings for WINDOW areas. Since this area is also allocated in the PCI memory space, map this area so that it should not overlap with the other areas.
(2) AHBPCI WINDOW1 area	1 KB	The PCI configuration registers are accessed through this area. Whether to access the OHCI/EHCI configuration registers or AHBPCI bridge registers is switched using the AHBPCI_WIN1_CTR register.
(3) AHBPCI WINDOW2 area	64 KB	The OHCI/EHCI operational registers are accessed through this area.
(4) PCIAHB WINDOW1 area	256 MB, 512 MB, 1 GB and 2 GB	The host logic accesses the work memory on the AHB bus through this area. The size of this area can be changed using the USBCTR register.
(5) PCIAHB WINDOW2 area	Disable, 256 MB	The host logic accesses the work memory on the AHB bus through this area. Whether to use this area or not can be selected using the USBCTR register.

The AHBPCI Communication Registers and AHBPCI WINDOW2 (OHCI/EHCI operational registers) areas and the PCIAHB WINDOW1 and PCIAHB WINDOW2 areas must not overlap each other.

Usually, the AHB memory space and PCI memory space can be allocated in the same address. However, if an overlap occurs between the above areas by the AHB bus memory mapping, set the base addresses so that they should not overlap with the PCIAHB WINDOW1/2 areas using the PCI configuration register (OHCI/EHCI/AHBPCI Base Address). This is shown in Figure 51.3.

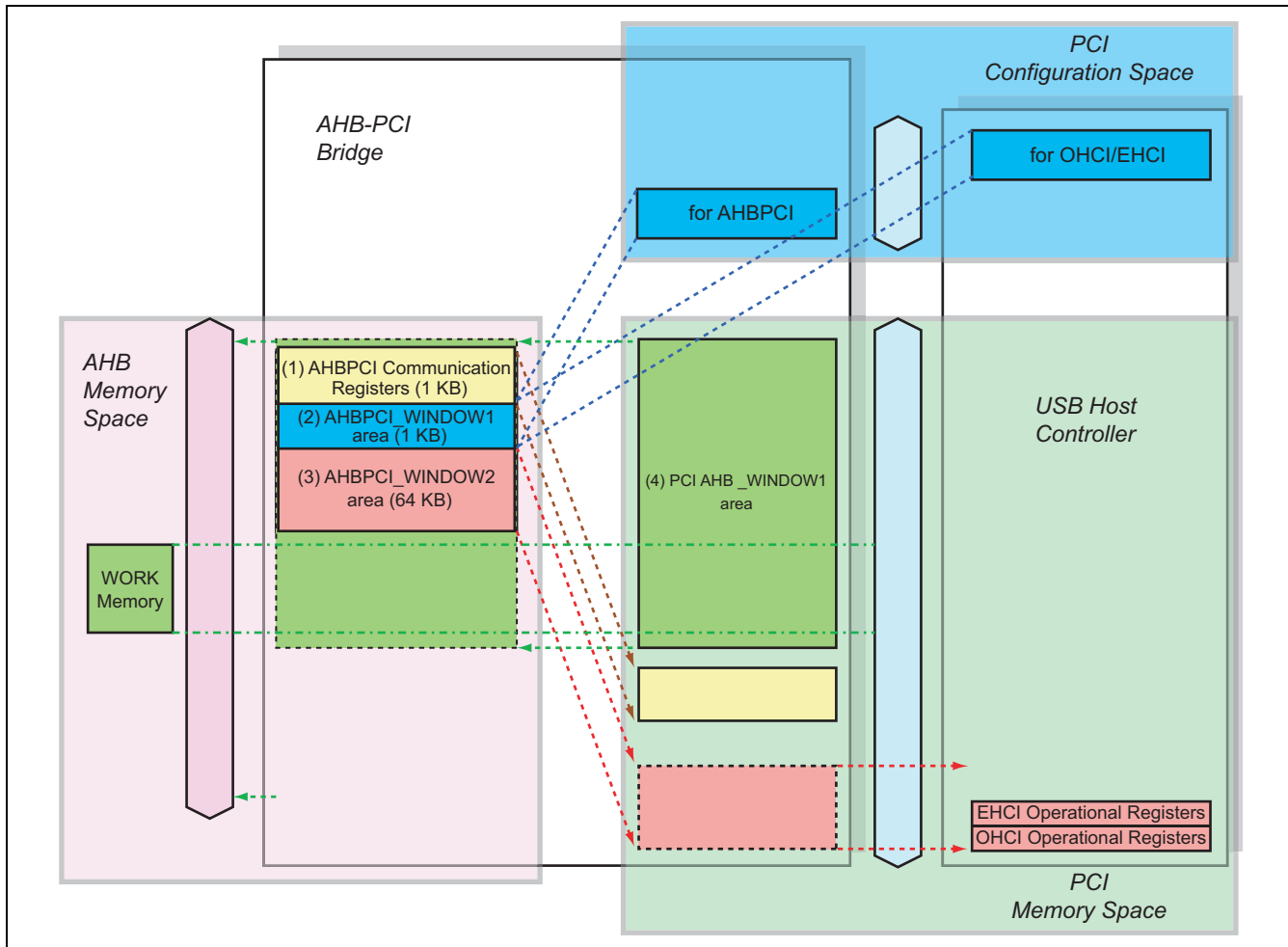


Figure 51.3 Mapping AHB and PCI Spaces (Spaces Overlapped)

Figure 51.4 shows the registers for AHB and PCI space mapping and Table 51.6 shows the relationship between the registers and the settings. In addition, the base address of Figure 51.4 AHB Memory Space is Ch.0. Please refer to a right note address for Ch.0/Ch.1/Ch.2. "Ch.0: H'EE08 / Ch.1: H'EE0A / Ch.2: H'EE0C"

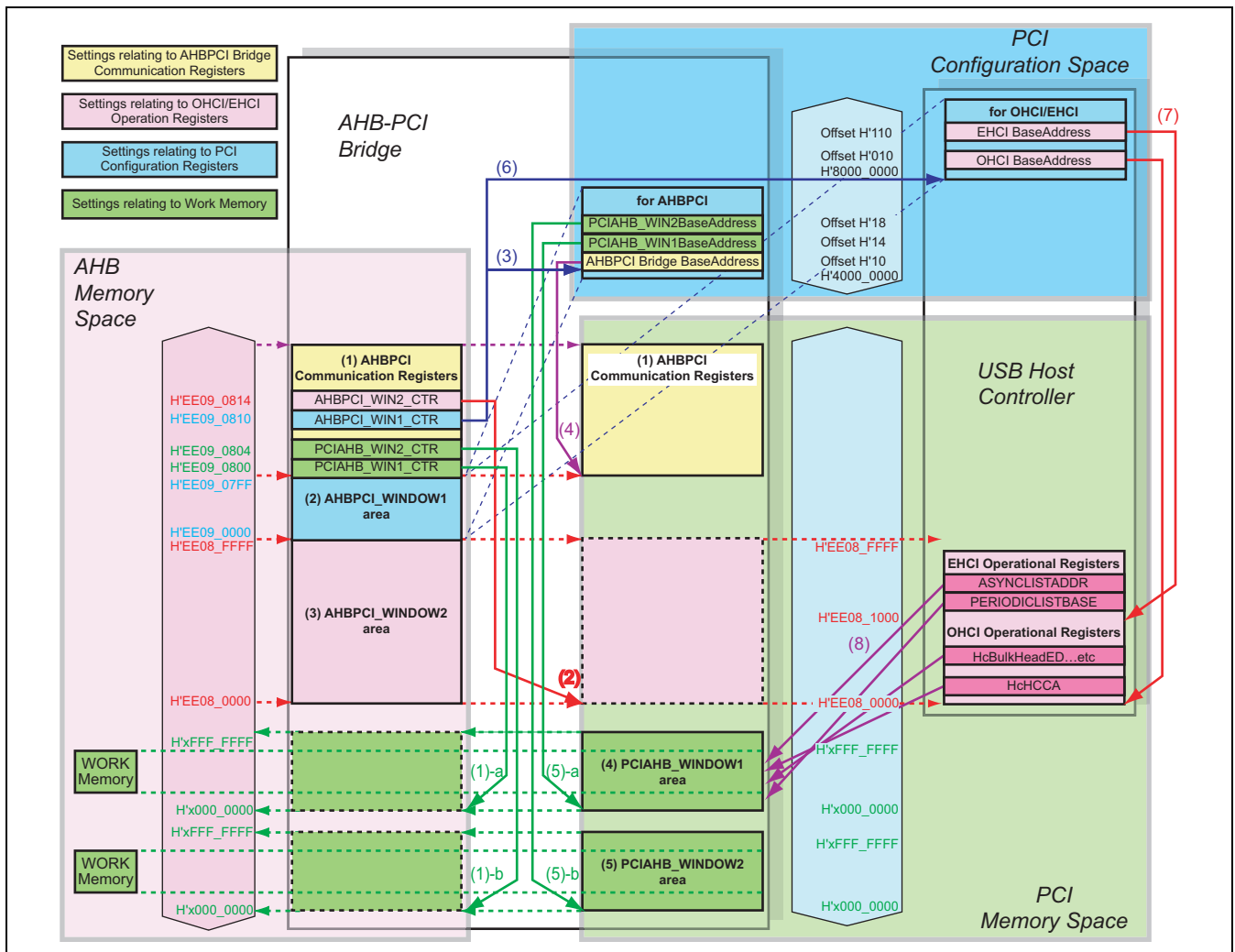


Figure 51.4 Address Setting Registers and AHB and PCI Space Mapping

**Table 51.6 Descriptions of Address Setting Register Values**

Register	Description
(1)-a PCIAHB_WIN1_CTR	When the host logic performs master-access to the ACIPHB WINDOW1 area, the AHB bus address is translated to the base address set in this register. Usually, set the area including the work memory to be used.
(1)-b PCIAHB_WIN2_CTR	When the host logic performs master-access to ACIPHB WINDOW2 area, the AHB bus address is translated to the base address set in this register. Usually, set the area including the work memory to be used.
(2) AHBPCI_WIN2_CTR	When the AHBPCI WINDOW2 area is accessed, the PCI bus address is translated to the base address set in this register. Although the same value as the AHBPCI WINDOW2 area can be set usually, if an overlap occurs with the area including the work memory set in (1), set the address so that it can prevent overlapping.
(3) AHBPCI_WIN1_CTR	When the base address is set to H'4000 0000 in this register, the PCI Configuration Registers area for AHBPCI is accessed.
(4) AHBPCI Bridge base address	Specifies a base address for the AHB-PCI bridge in the PCI space. Set this register so that it should not overlap with the other areas though this register is not accessed from the PCI bus,
(5)-a PCIAHB_WIN1 base address	Specifies a base address for the PCIAHB WINDOW1 area in the PCI space. Usually, the same base address as (1)-a should be set. Areas (5)-a and (5)-b must not overlap each other.
(5)-b	Specifies a base address for the PCIAHB WINDOW2 area in the PCI space. Usually, the same base address as (1)-b should be set. Areas (5)-a and (5)-b must not overlap with each other.
(6)	When the base address is set to H'8000 0000 in this register, the PCI Configuration Registers area for OHCI/EHCI Operational Registers is accessed.
(7)	Specifies a base address for the OHCI/EHCI Operational Registers in the PCI space. Usually, the OHCI base address should be set as the same base address set in (2). The EHCI base address is calculated by adding the base address set in (2) and offset H'1000.
(8) OHCI/EHCI operational registers	On completion of settings (1) to (7), the host logic can access data, such as a descriptor, expanded on the AHB work RAM through the PCI. The following registers are used to specify addresses for data in the work RAM: OHCI/EHCI operational registers HcHCCA HcPeriodicCurrentED HcControlHeadED HcControlCurrentED HcBulkHeadED HcBulkCurrentED HcDoneHead EHCI operational registers PERIODICLISTBASE ASYNCLISTADDR



### 51.7.1 PCI Configuration Register Accesses

The registers in the PCI Configuration Space can be accessed through the AHB-PCI WINDOW1 area (addresses H'10000 to H'107FF: 2-Kbytes). For the access, the AHBPCI\_WIN1\_CTR register should be set correctly. Table 51.7 shows the AHBPCI\_WIN1\_CTR settings to access the PCI Configuration Space areas for the OHCI/EHCI and AHB-PCI Bridge.

**Table 51.7 AHBPCI WIN1 CTR Register Settings**

Access to	AHBPCI_WIN1_CTR Setting	
	PCIWIN1_BASEADR[31:11]	PCICMD[2:0]
OHCI/EHCI PCI Configuration Space	Only set bit 31 to 1.	B'101
AHB-PCI Bridge PCI Configuration Space	Only set bit 30 to 1.	

### 51.7.2 OHCI/EHCI Operational Register Accesses

To access the OHCI/EHCI Operational Registers area, set the PCI space addresses and also set the OHCI/EHCI PCI Configuration Space and AHBPCI\_WIN2\_CTR register. Table 51.8 shows the required settings.

**Table 51.8 Settings Required for Accessing OHCI/EHCI Operational Registers Area**

Bit	Setting
OHCI/EHCI PCI Configuration Space offset H'04 (Command Status) Memory Space (bit 1)	1 (access to memory space enabled)
PCICMD (bits 3 to 1) in AHBPCI WIN2 CTR register	B'011 (memory read/memory write)

## 51.8 Reset System

### 51.8.1 Reset Configuration

This USB host controller is reset by the HRESET signal. When the HRESET signal is asserted, all the circuits within the USB host controller are reset. The HRESET is a power-on reset, and assumes that the HRESET signal of the AHB is connected. The reset signal of this USB host controller is an asynchronous reset that is directly connected to the F/F reset signal. The table lists the reset signals of this USB host controller.

Table 51.9 lists the reset signals for the USB host controller.

**Table 51.9 Reset Signals**

Reset Signal	Supplied From	Description
HRESETn	CPG	Power-on Reset Signal of the USB host controller. Resets the entire USB host controller. HRESETn is controlled from CPB as software reset.
PLL_RST	Internal	PLL in Transceiver Reset signal. This signal reset the Transceiver circuit too. Do not assert this signal when USB Host controller or Function Controller is active.
USBH_RST	Internal	USB Host Controller Reset Signal

When the HRESET is asserted, the USBH\_RST is also asserted. The internal reset can be operated from the AHB-PCI Bridge register. After the HRESET assertion, use the same register to cancel the reset state. For the reset sequence, refer to section 51.11.1, Reset Sequence.

### 51.8.2 Reset System Diagram

Figure 51.5 shows the reset system in the USB host controller.

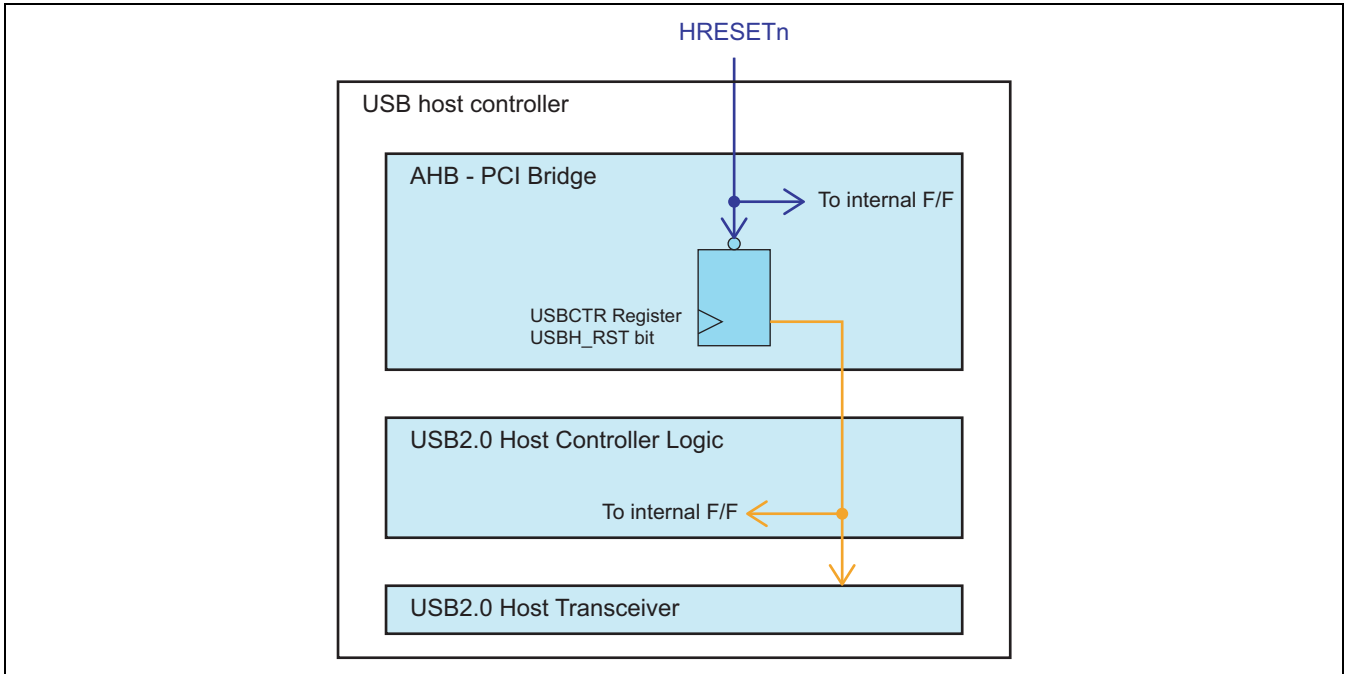


Figure 51.5 Reset System Diagram

## 51.9 Interrupts

### 51.9.1 Interrupt Signals

This USB host controller has the interrupt signals listed below. These signals are used as level-triggered interrupts. The interrupt lines can be reduced by the U2H\_BIND\_INT register if required (e.g., due to insufficient system resources). The U2H\_BIND\_INT register is not used when these interrupts are used individually.

**Table 51.10 Interrupt Signals**

Interrupt Signals	Synchronization Clock	Active Level	Description
USB_INTH	HCLK	High	Interrupt signal generated from the AHB-PCI Bridge
U2H_OHCI_INT	HCLK	High	INTA interrupt signal generated from the host controller
U2H_EHCI_INT	HCLK	High	INTB interrupt signal generated from the host controller
U2H_PME_INT	PMCLK	High	PME interrupt signal generated from the host controller
U2H_BIND_INT	HCLK/PMCLK	High	OR of the interrupt signals (Bridge + OHCI + EHCI + PME)

### 51.9.2 Interrupt Control Registers

#### (1) USB\_INTH Control Register

USB\_INTH is an interrupt that is generated by the AHB-PCI Bridge. The status check, interrupt clear, and interrupt enable are performed by the AHB-PCI Bridge registers.

**Table 51.11 USB\_INTH Control Register**

Function	Register
Interrupt status check and clear	PCI_INT_STATUS Register
Interrupt enable	PCI_INT_ENABLE Register

#### (2) U2H\_OHCI\_INT Control Register

U2H\_OHCI\_INT is an INTA interrupt that is generated by the host controller. This interrupt is controlled by the host controller registers; however, for this interrupt signal assertion, the interrupt enable bit of the AHB-PCI Bridge must be set to Enabled.

**Table 51.12 U2H\_OHCI\_INT Control Register**

Function	Register
Interrupt status check and clear	HcInterruptStatus Register
Interrupt enable	HcInterruptEnable Register
	HcInterruptDisable Register
	PCI_INT_ENABLE Register (bit[16] USBH_INTAEN)

**(3) U2H\_EHCI\_INT Control Register**

U2H\_EHCI\_INT is an INTB interrupt that is generated by the host controller. This interrupt is controlled by the host controller register. To assert this interrupt signal, the interrupt enable bit of the AHB-PCI Bridge must be valid.

**Table 51.13 U2H\_EHCI\_INT Control Register**

Function	Register
Interrupt status check and clear	USBSTS Register
Interrupt enable	USBINTR Register PCI_INT_ENABLE Register (bit[17] USBH_INTBEN)

**(4) U2H\_PME\_INT Control Register**

U2H\_PME\_INT is a PME interrupt that is generated by the host controller. This interrupt is controlled by the host controller register. To assert this interrupt signal, the interrupt enable bit of the AHB-PCI Bridge must be valid.

**Table 51.14 U2H\_PME\_INT Control Register**

Function	Register
Interrupt status check and clear	PCI Configuration Register for OHCI/EHCI offset H'44
Interrupt enable	PCI Configuration Register for OHCI/EHCI offset H'44 PCI_INT_ENABLE Register (bit[19] USBH_PMEEN)

### 51.9.3 U2H\_BIND\_INT

The U2H\_BIND\_INT interrupt signal is generated by an OR of the interrupt source signals (USB\_INTH, U2H\_OHCI\_INT, U2H\_EHCI\_INT, and U2H\_PME\_INT). The signal states of the U2H\_PME\_INT, U2H\_OHCI\_INT and U2H\_EHCI\_INT are reflected to the PCI\_INT\_STATUS register. Reading the PCI\_INT\_STATUS register enables the user to check the interrupt source.

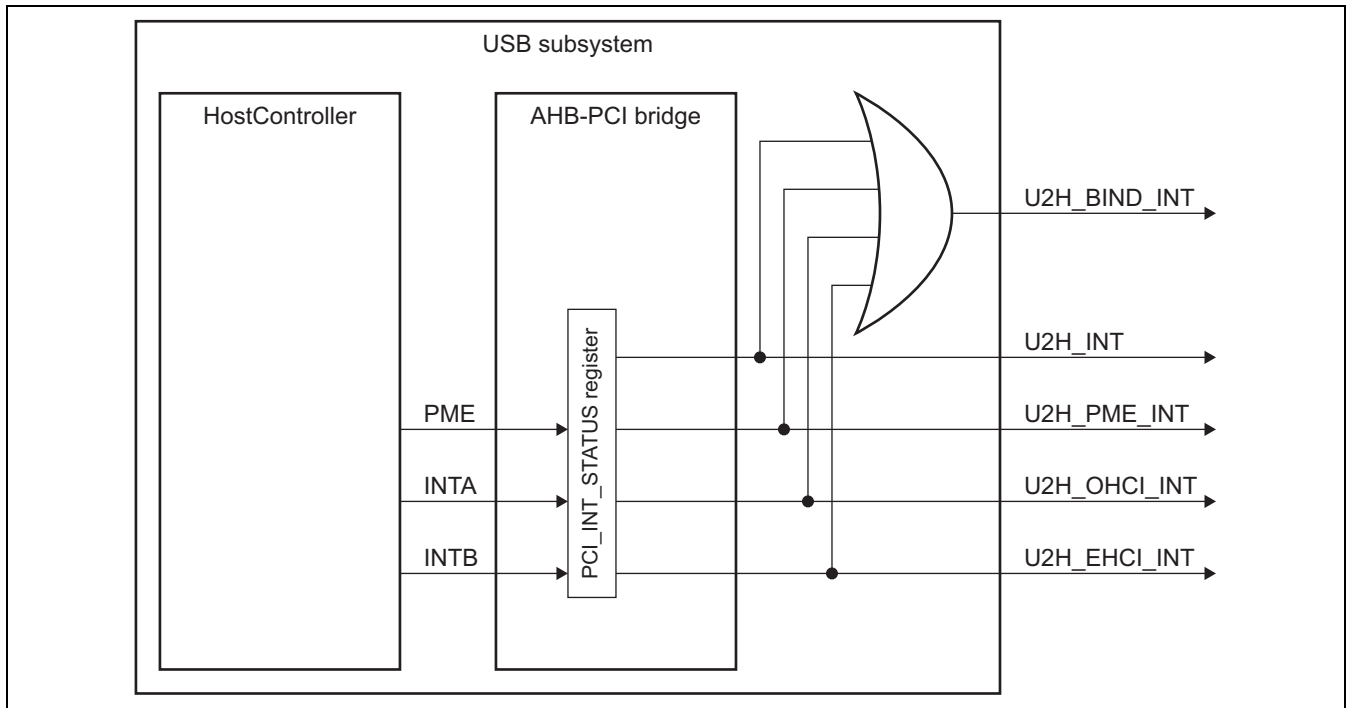


Figure 51.6 Interrupt Signals Aggregation Image

### 51.9.4 Interrupt Signal Clear Time

The AHB-PCI Bridge implements a posted write; therefore, an interrupt generated by the host controller may not be cleared soon after setting the clear register and same interrupt state may be recognized many times. (See the Figure 51.7) The user must take a countermeasure to avoid such false recognition.

For example; access to the host controller register (2) after accessing to an Interrupt Clear Register (1). The operation of (2) is waited (SHREADY = 0 or Retry response) until the operation of (1) is completed. As the result, the interrupt is cleared without fail at the completion of the access of (2).

The U2H\_OHCI\_INT, U2H\_EHCI\_INT, and U2H\_PME\_INT may not be cleared soon after setting the clear register. When HCLK = 150 MHz and PCICLK = 25 MHz, the interrupt is cleared in about 300 ns after setting the clear register. When the host controller is executing a transfer as a master on the internal PCI-bus, it takes about 1.6 μs (35CLK@PCICLK + 3CLK@HCLK + 2CLK@12 MHz) at worst to clear the interrupt.

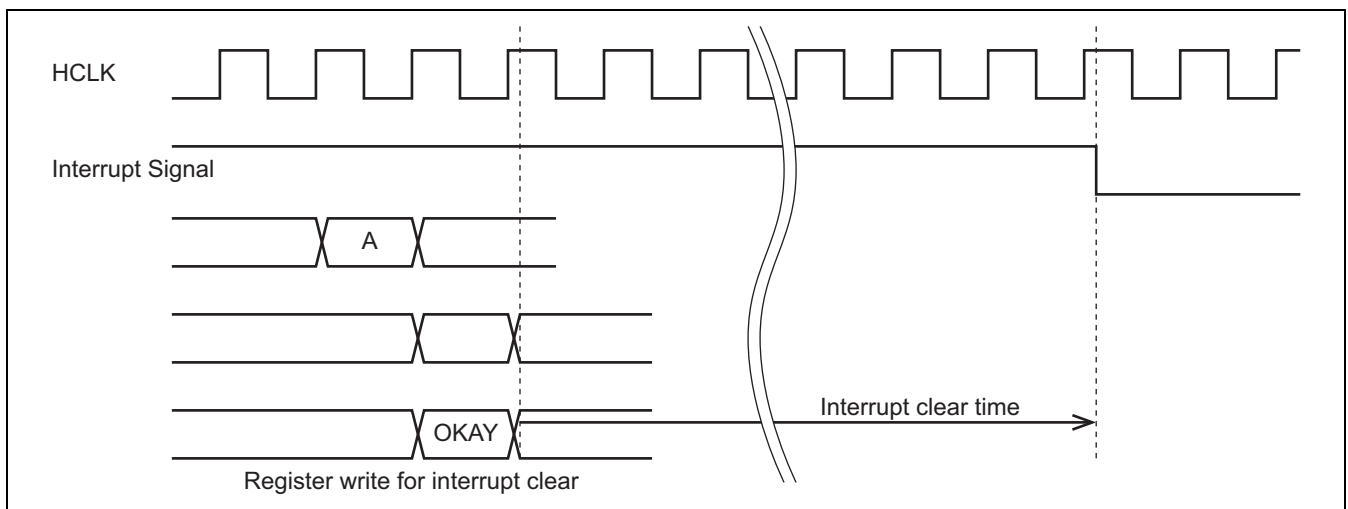


Figure 51.7 Interrupt Clear Time

## 51.10 Power Management

This chapter describes the power management function of the USB Host controller V1 Type-H2.

When the USB is not used, hold the power state in a reset state after cancellation of the AHB bus reset (USBCTR Register, USBH\_RST = 1). The subsequent sections describe a power-off operation that temporarily powers down (suspend) the USB host.

### 51.10.1 Power-Off Sequence

When the USB Host function is temporarily stopped, the power consumption can be reduced by powering down the host controller and stopping the internal PCI bus clock (PCICLK) of the USB host controller.

The USB host controller has a gating circuit for the PCICLK, and the circuit can be controlled from the AHB-PCI Bridge register. The following figure shows the power-off sequence.

#### 51.10.1.1 OHCI Mode

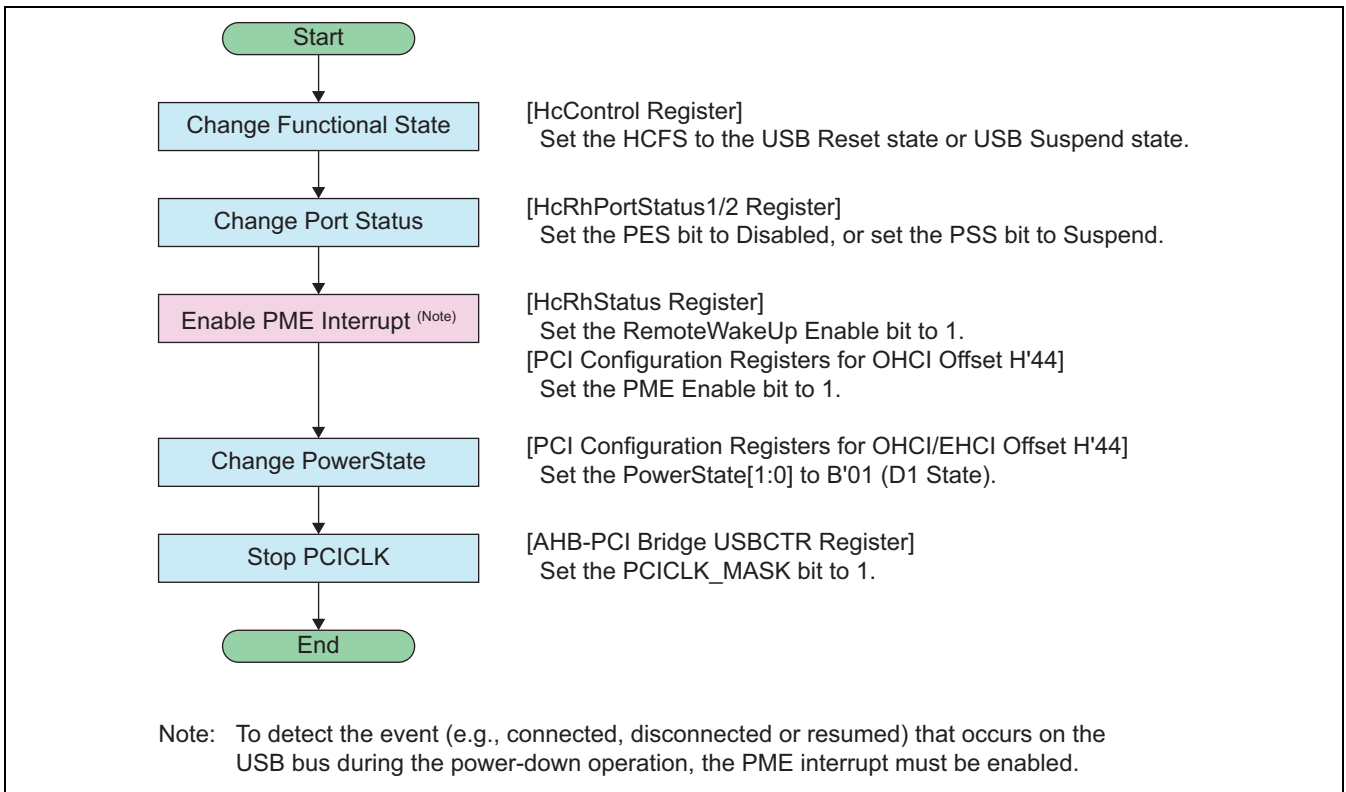
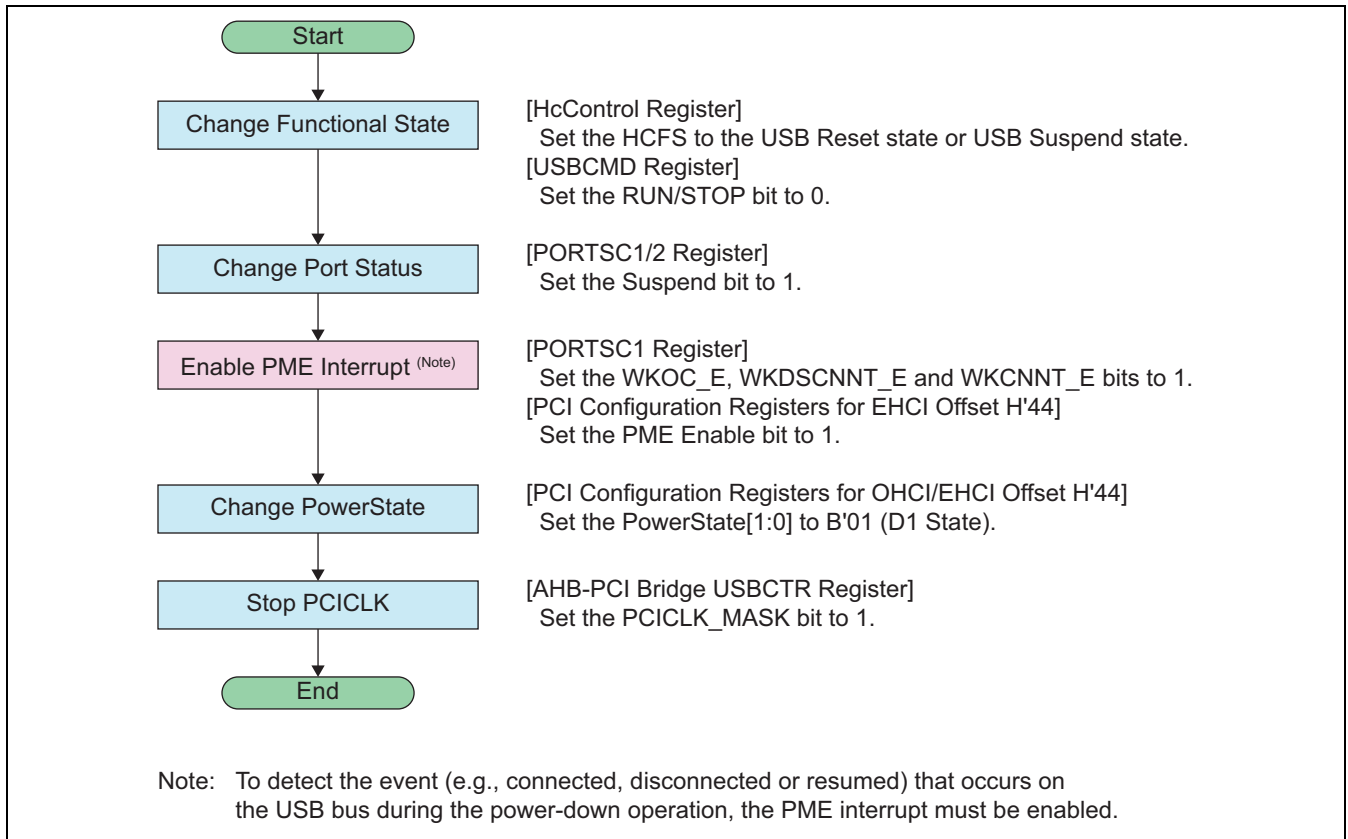


Figure 51.8 Power-Off Sequence



**51.10.1.2 EHCI Mode**



**Figure 51.9 Power-Off Sequence**

### 51.10.2 Power On Sequence

The recovery from the power-down state is performed in the opposite procedure of the power-down operation.

#### 51.10.2.1 OHCI Mode

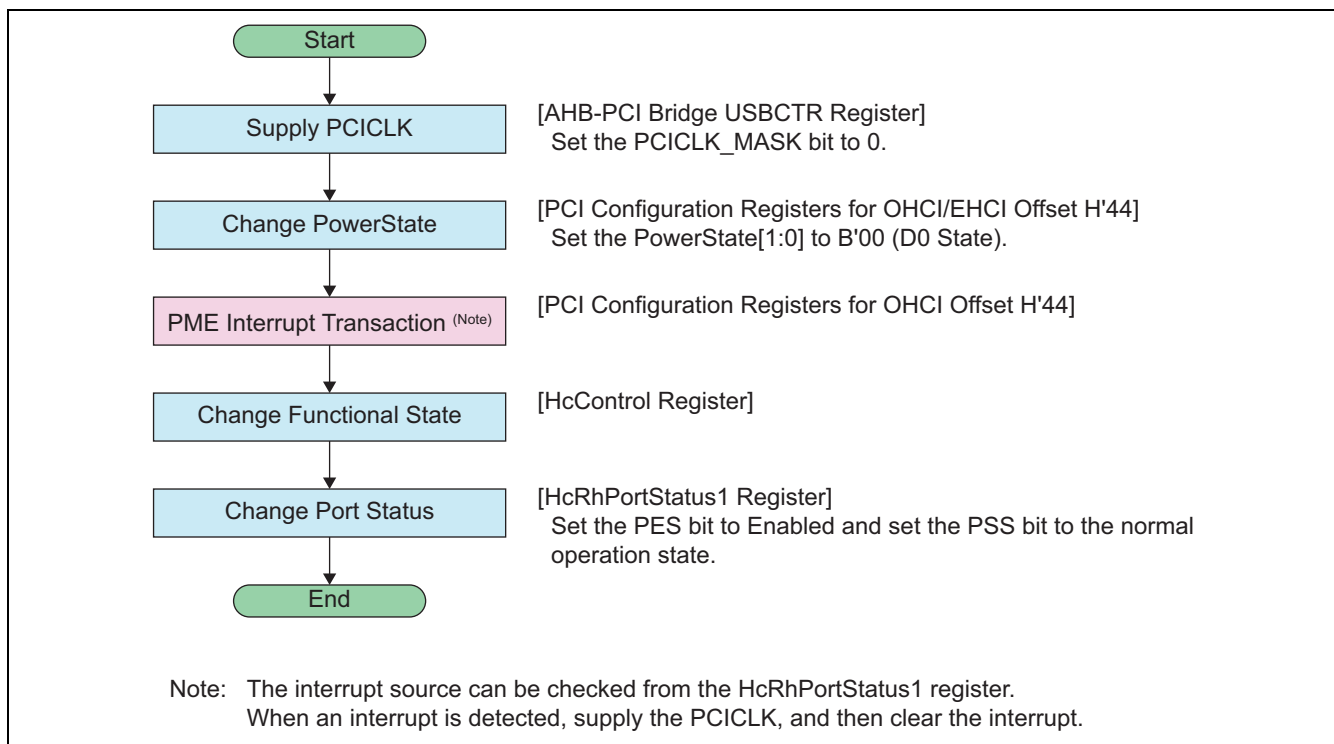


Figure 51.10 Power-On Sequence

#### 51.10.2.2 EHCI Mode

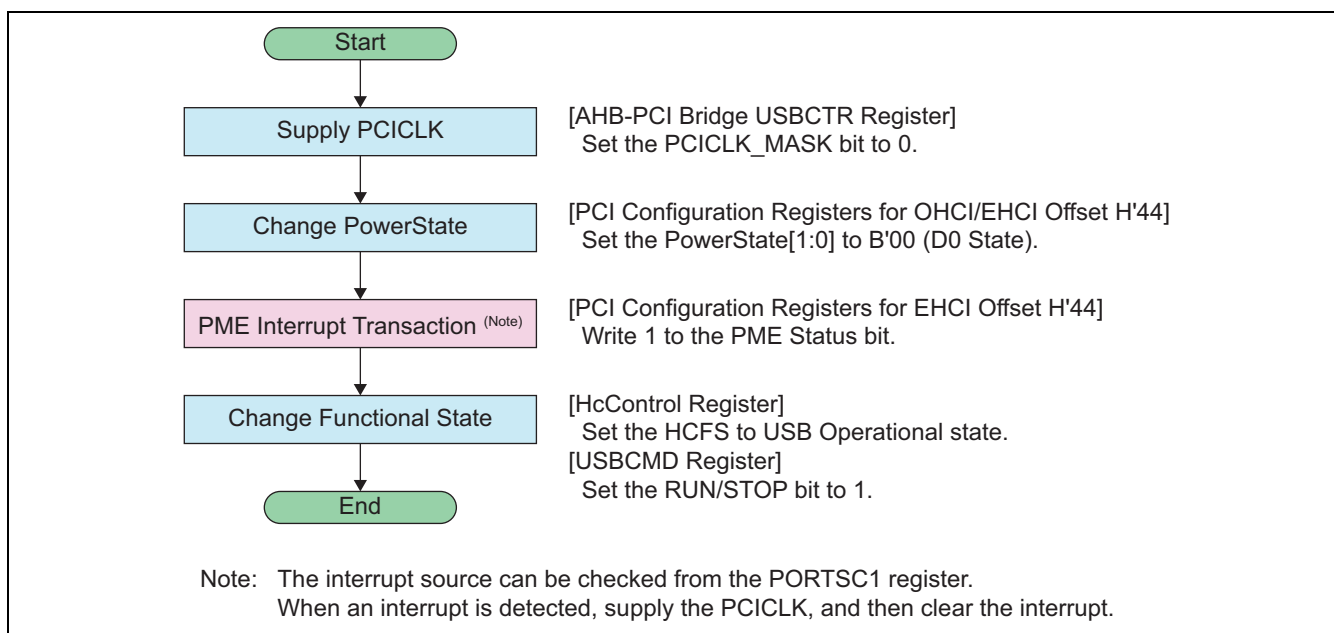


Figure 51.11 Power-On Sequence

### 51.10.3 Direct Power-Down Feature

When the whole USB host controller is not used, power consumption of the USB host controller can be reduced using the direct power-down function. Recovery from the direct power-down state is not performed in this USB host controller.

#### 51.10.3.1 Direct Power-Down Setting

The figure below shows how to set the direct power-down mode. It is recommended that the PCICLK be masked from the PCICLK\_MASK register to minimize power consumption.

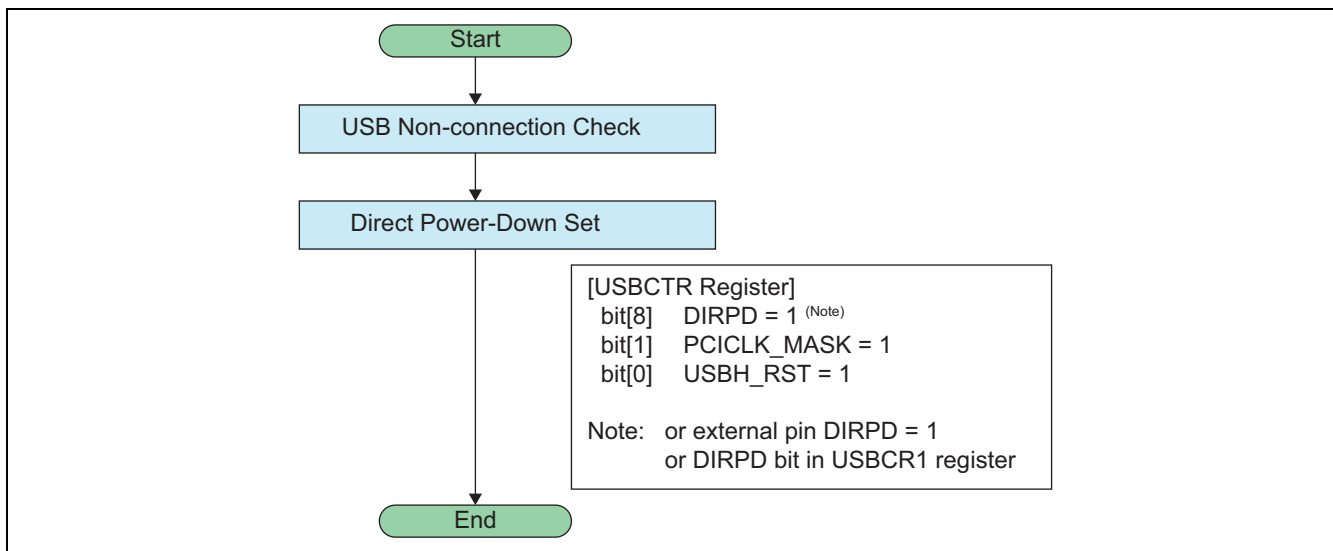
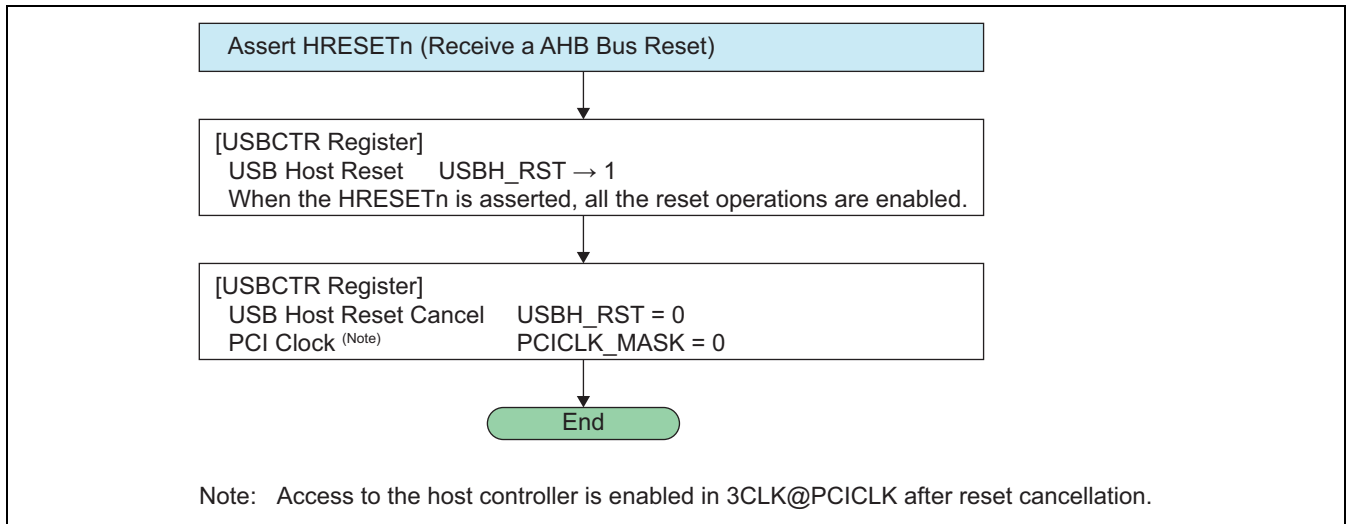


Figure 51.12 Direct Power-Down Setting

## 51.11 Operating Procedures

### 51.11.1 Reset Sequence



**Figure 51.13 Reset Sequence**

51.11.2 Initial Setup Sequence

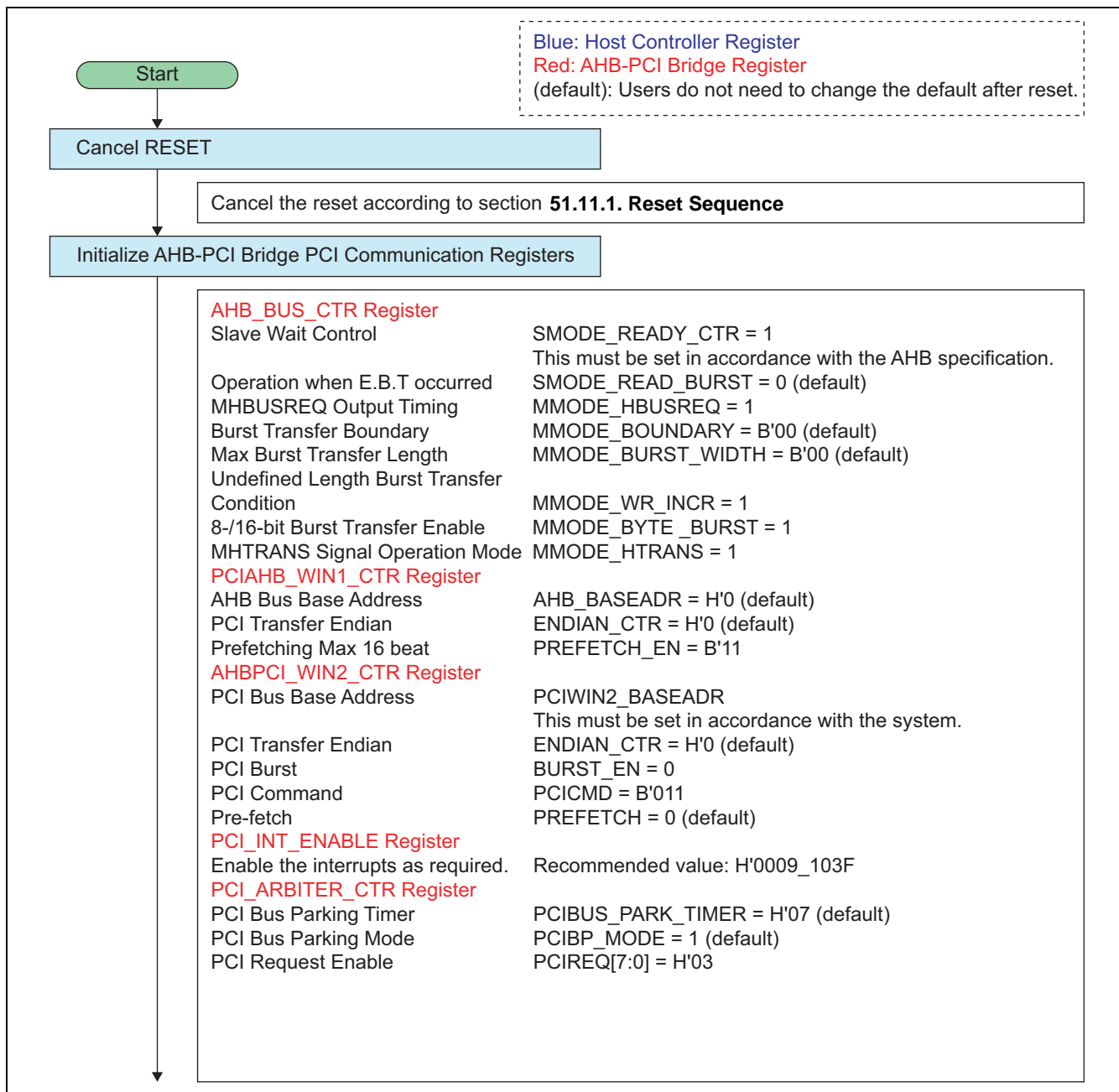
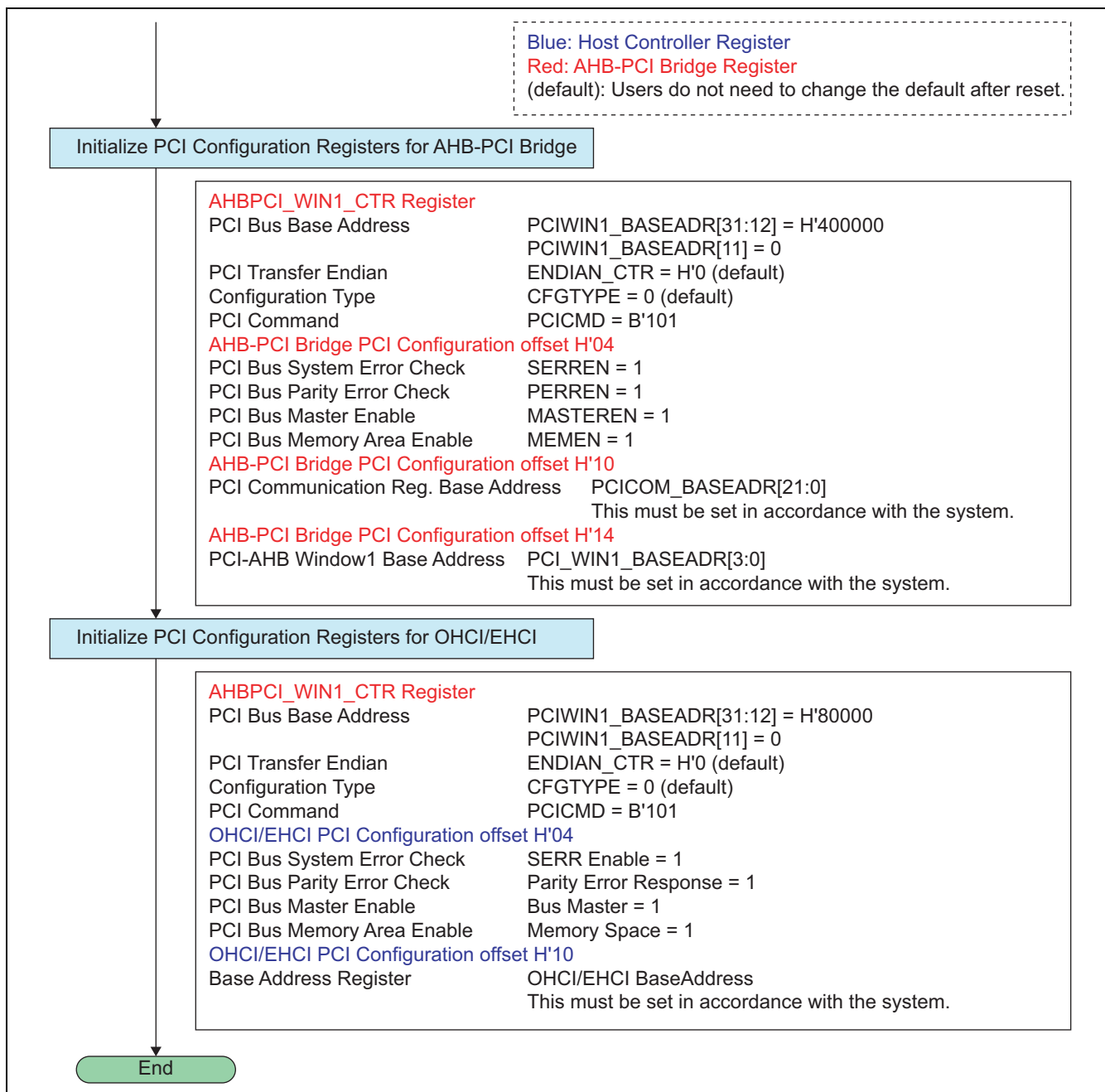


Figure 51.14 USB Host Initial Setup Sequence (1)



**Figure 51.15 USB Host Initial Setup Sequence (2)**

The above settings enable the following operations.

- Access to the OHCI and EHCI Operation Registers via the AHB-PCI Window2 register
- Data transfer to the AHB from the host controller

### 51.11.3 Transfer Overview

Transfer by the host controller must be performed in compliance with the following OHCI and EHCI specifications.

Open Host Controller Interface Specification for USB Rev 1.0a

Enhanced Host Controller Interface Specification for Universal Serial Bus Revision 1.0

This section provides supplementary note about the DMA stop.

#### 51.11.3.1 DMA Transfer Stop

The AHB-PCI Bridge does not have a control bit that turns on or off DMA mode. When the host controller initiates a PCI bus cycle as a master, the AHB-PCI Bridge performs DMA transfer to the AHB. DMA transfer of the host controller is performed: (1) to write the current frame number into memory; and (2) to write or read the descriptor and data loaded into memory to perform a list transaction.

Writing of the frame number (1) is performed per frame cycle when the USB is in the Operational state; therefore, the USB must be put into the Suspend or Reset state before stopping the DMA transfer. In this case, the list transaction of (2) is stopped at the same time.

The list transaction of (2) is stopped when the enable bit (HcControl Register, BLE bit, CLE bit, IE bit, PLE bit) of the list transaction is cleared. The transaction is stopped from the next frame when the bit is cleared. In this case, a writing of the frame number of (1) is not stopped.

## 51.12 Over Current and Vbus Control

### 51.12.1 Over Current Control

This chapter describes the over current detection of USB port and OCI/PPON operation which controls VBUS. OCI is connected to external input pin USB\*\_OVC, PPON is connected to external output pin USB\*\_PWEN.

#### 51.12.1.1 Description of OCI/PPON

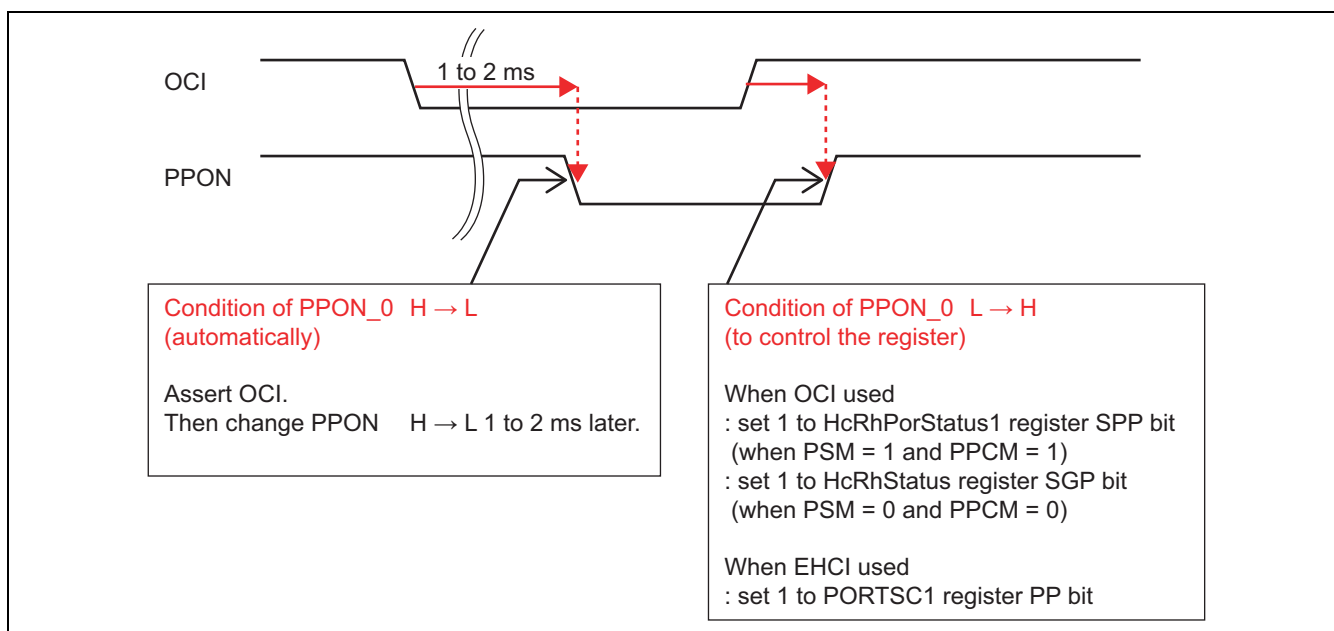
The function of OCI/PPON is described in the following table.

**Table 51.15 OCI/PPON**

Pin	IO	Level	Description
OCI	IN	1	Not detect over current
		0	Detect over current
PPON	OUT	1	Power supply to VBUS ON
		0	Power supply to VBUS OFF

#### 51.12.1.2 Condition of PPON Assertion

The timing chart of OCI / PPON assertion is described following figure.



**Figure 51.16 Timing chart of OCI / PPON assertion and deassertion**

PPON are not asserted automatically when OCI is changed from L to H. Assert PPON by setting the port power bit from software after OCI are changed L → H.



### 51.12.2 VBUS Control

Power supply to VBUS can be stopped by connecting OCI and PPON to highside switch when USB port is not used. It can reduce power consumption.

Note : It depends on the external circuit attached to RZ/G.

The configuration of this operation is described in the following table.

**Table 51.16 PPON setting for VBUS control**

PPON setting	State of VBUS
PPON = 0	VBUS stopped
PPON = 1	VBUS is supplied

The operation of PPON for OCI assertion is changed by the setting of PCI configuration register and OHCI Operation register. The description of this operation is described in following table.

**Table 51.17 PPON operation**

PCI Configuration Register		OHCI Operation Register				PPON operation
EXT1 register	HcRhDescitporA register	HcRhDescriptorB register		PPCM	PPON	
Ppcnt bit	NOCP bit	NPS bit	PSM bit	Bit 1		
0	—	—	—	—	—	Fixed 1
—	1	—	—	—	—	Fixed 1
—	—	1	—	—	—	Fixed 1
1	0	0	0	—	PPON is changed H → L by asserting OCI to 0.	
			1	0		
				1		

Note: If NPS is 1, Host controller detects the over current, but it not change PPON H → L.

51.12.3 Over current detection flow

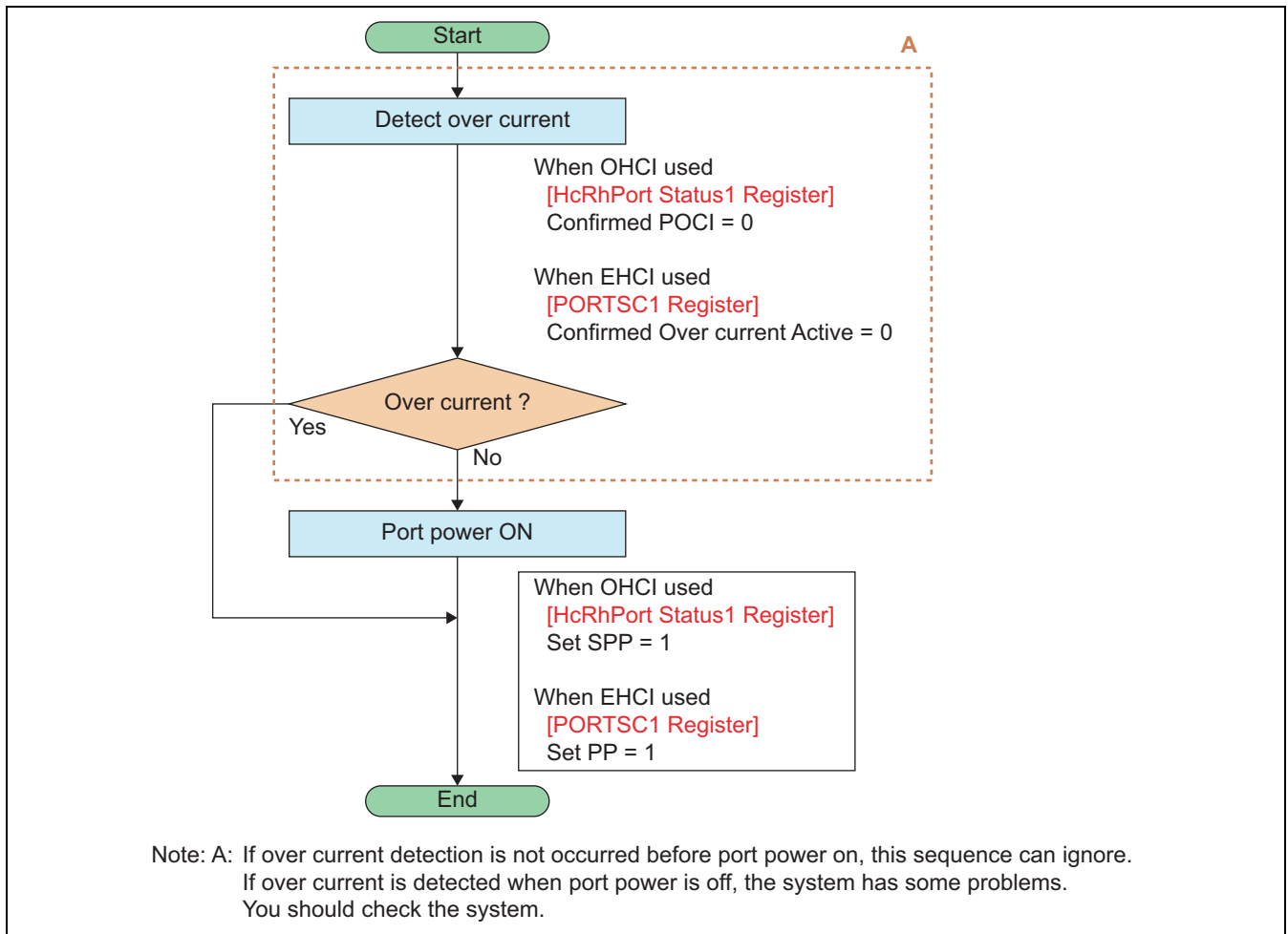
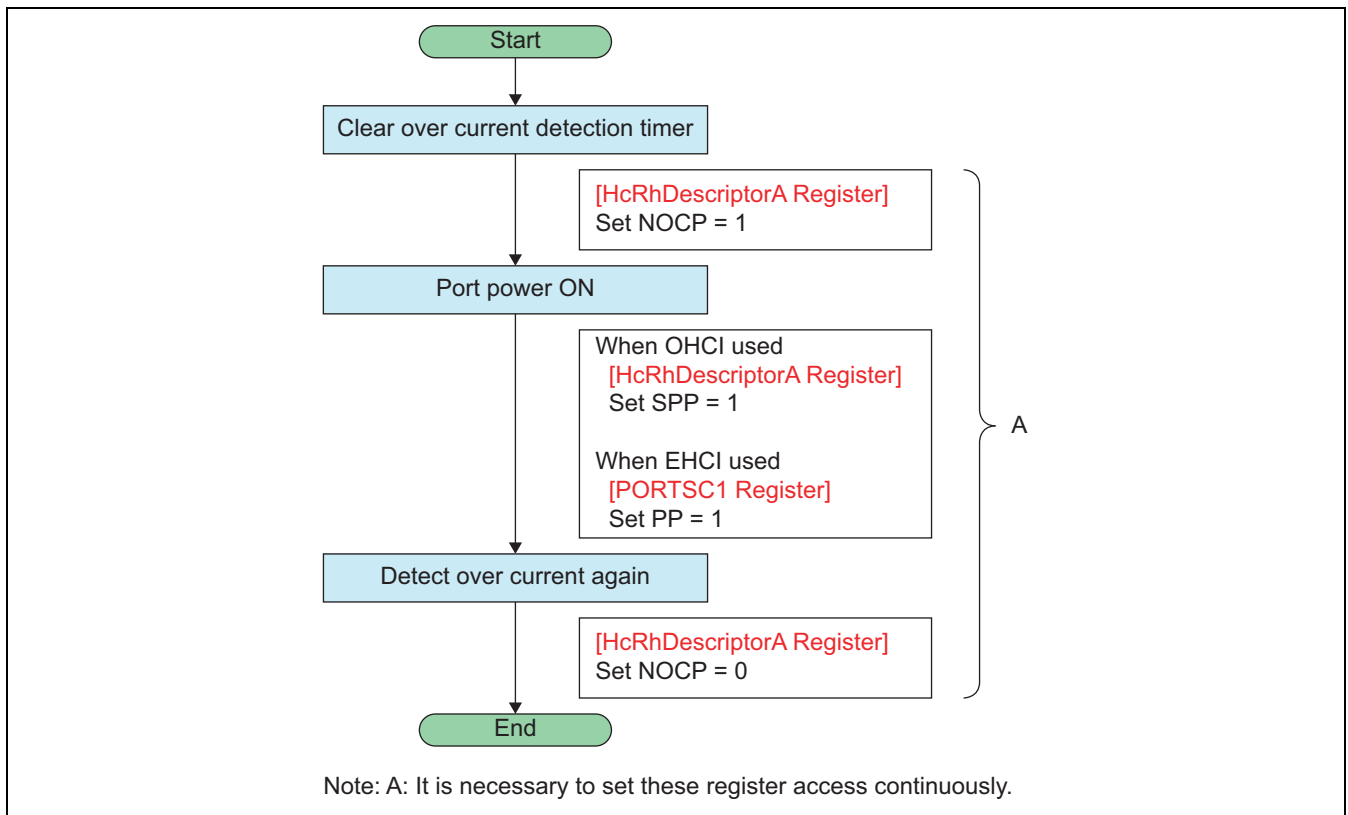


Figure 51.17 Over current detection flow

**51.12.4 PPON setting flow**

PPON setting flow that the case of OCI is active (B'0) when the system is started is described the following figure.



**Figure 51.18 PPON Setting Flow**

If OCI is active when system is started, you should set that OCI detect function is OFF before setting PPON.

OCI detect timer becomes OFF when the OCI detect function is disabled.

If the OCI detect function is set ON after PPON setting, OCI detection value that detected when system is started is cleared.

## 51.13 Usage Note

### 51.13.1 EXT1 register bit 12 (current: reserved bit) should be specified as 0 (default: 1) under some conditions

Problem: The size of the short packet may become the maximum size with the undefined padding data when all of the following conditions are satisfied.

- 1) The transfer type is Control or Bulk Out and transfer is at high speed mode.
- 2) Asynchronous schedule park mode is enabled (USBCMD.ASPME =1).
- 3) Periodic list processing is disabled (USBCMD.PSE = 0).
- 4) Bit 12 of EXT1 register is 1 (this bit is reserved and its initial value is 1).
- 5) Time taken to transfer a fetched QH exceeds the uFrame limit.
- 6) The amount of data remaining to be transferred once the uFrame boundary is exceeded is "maximum packet size  $\times$  n + short packet". n represents a positive integer more than 1.

Note 1. It is most likely harmless for the typical use case. The following cases are some example not to occur this problem.

- Only HS asynchronous out transfer, such as BULK out write transaction to a USB memory from a navigation system cause this issue. The issue does not occur for read operations. Isochronous transfer to transmit audio data or interrupt transfer can avoid this issue even if it is OUT transaction because these are not asynchronous transfer.
- The recent Linux device driver set the asynchronous schedule park mode to disabled by default though it prevent the host controller from achieving the maximum transfer performance. The asynchronous schedule park mode is possibly disabled if the system is based on Linux. In this case the issue does not occur.
- The periodic schedule enable bit is set as enabled for the system which use periodic transfer, isochronous or interrupt transfer. For example a HUB require interrupt transfer so that the USB ports through hubs does not show this issue.
- If the data length does not match with the condition, MAX packet size  $\times$  N + short packet, then the issue does not occur. The file systems for HDD or USB memory use the transfer size multiple of 512-byte. In this case the issue does not occur.

Note 2. The condition 5) is controlled by the host controller hardware therefore it is uncontrollable from user. Linux BSP driver enable or disable the periodic schedule depends on the USB device connected but the park mode is disabled by default. The issue does not occur by default because of condition 2). Applying the workaround is recommended if the park mode is enabled by user and condition 6) are met.

## [Workaround]

The recommended workaround for this problem is the following, which prevent the condition 4).

1. Write 0 to bit 12 in the EXT1 register\*<sup>1</sup> during the initialization sequence.

Notes: \*1. See section 51.6.3.12, Offset H'E0 (EXT1).

## Function of the bit 12 in EXT1

This bit enables or disables fetching of QH at the beginning of the next uFrame once processing for packet transfer exceeds the uFrame time limit; this bit is initially set to 1, but clearing it to 0 (workaround 1) disables the fetching.

Disabling of this function does not cause any problems during packet transfer.

## 52. USB High-Speed Module (HS-USB)

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

This module is a USB controller provided with the function controller function, and high-speed transfer and full-speed transfer are available. Provided with an on-chip USB transceiver, this module also supports all transfer types defined by the USB Specification.

This module can use up to 16 pipes. Furthermore, for pipes 1 to F, arbitrary endpoint numbers can be allocated according to peripheral devices to be communicated and user systems.

### 52.1 Features

#### (1) On-chip USB transceiver

#### (2) Achieves space-saving mount with less external elements

- On-chip D+ pull-up resistor (function operation mode)
- On-chip D+/D- terminating resistors (high-speed operation mode)
- On-chip D+/D- output resistors (full-speed operation mode)

#### (3) All Types of USB Transfers Supported

- Control transfer
- Bulk transfer
- Interrupt transfer (except for high bandwidth)
- Isochronous transfer (except for high bandwidth)

#### (4) Dedicated DMA interface

- On-chip 4-channel DMA interface

#### (5) Pipe configuration

- Up to 16 pipes are selectable (including the default control pipe)
- Programmable pipe configuration
- Arbitrary endpoint numbers can be allocated to pipes 1 to F.
- Settable transfer conditions for each pipe are as follows:

Pipe 0: A pipe only for control transfer with a 64-byte (fixed) single buffer

Pipes 1 and 2: Bulk transfers/isochronous transfer, continuous transfer mode, programmable buffer size (up to 2-Kbytes: double buffer can be specified)

Pipes 3 to 5 and B to F: Bulk transfer, continuous transfer mode, programmable buffer size (up to 2-Kbytes: double buffer can be specified)

Pipes 6 to 8: Interrupt transfer, 64-byte fixed single buffer

Pipes 9 to A: Interrupt transfer, Bulk transfer, continuous transfer mode, programmable buffer size (up to 2-Kbytes: double buffer can be specified)

#### (6) Other functions

- Transfer ending function using transaction count
- SOF pulse output function
- BRDY interrupt event notification timing change function (BFRE)
- Function that automatically clears the buffer memory after the data for the pipe specified at the DnFIFO (n = 0 to 3) port has been read (DCLRM)

- NAK setting function (SHTNAK) for the response PID due to the transfer end
- The suspend and resume of whole LSI can be done by using USBHS.

### (7) Embedded USB PHY

The embedded USB PHY consists of the following features.

- Contains the USB functions drivers and receivers for D+ and D- signaling

The embedded USB PHY does not support ID pin detection and VBUS detection. This function is exported to the external device (for example, MAX3355E). This product support only OVC signals for vbus detection.

This USB subsystem support external device interface for external device control. These signals inform the vbus status, vbus valid and the OTG SRP.

#### 52.1.1 Input/Output Pins

Table 52.1 lists the input and output pins of the USB.

**Table 52.1 Pin Configuration of USB**

Classification	Pin Name	Name	I/O	Description
USB bus interface	DP	USB D+ data	I/O	D+ Input/output of the on-chip transceiver Connect this pin to the D+ pin of the USB bus.
	DM	USB D- data	I/O	D- Input/output of the on-chip transceiver Connect this pin to the D- pin of the USB bus.
Reference resistance	RREF	Reference input	Input	Reference resistance connecting pin Connect this pin to the ground through a 1.8 kΩ ±1% resistor.

## 52.2 Register Descriptions

<b>RZ/G1H</b>	<b>RZ/G1N</b>
<b>RZ/G1M</b>	<b>RZ/G1E</b>

Table 52.2 lists the registers used in this module. Table 52.3 lists the register states in each processing mode.

**Table 52.2 Register Configuration**

Register Name	Abbreviation	R/W	Address	Access Size	RZ/G Series Products			
					RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
System configuration control register	SYSCFG	R/W	H'E659_0000	16	√	√	√	√
CPU bus wait register	BUSWAIT	R/W	H'E659_0002	16	√	√	√	√
System configuration status register	SYSSTS	R	H'E659_0004	16	√	√	√	√
Device state control register	DVSTCTR	R/W	H'E659_0008	16	√	√	√	√
Test mode register	TESTMODE	R/W	H'E659_000C	16	√	√	√	√
CFIFO port register	CFIFO	R/W	H'E659_0014	32	√	√	√	√
CFIFO port select register	CFIFOSEL	R/W	H'E659_0020	16	√	√	√	√
CFIFO port control register	CFIFOCTR	R/W	H'E659_0022	16	√	√	√	√
D0FIFO port select register	D0FIFOSEL	R/W	H'E659_0028	16	√	√	√	√
D0FIFO port control register	D0FIFOCTR	R/W	H'E659_002A	16	√	√	√	√
D1FIFO port select register	D1FIFOSEL	R/W	H'E659_002C	16	√	√	√	√
D1FIFO port control register	D1FIFOCTR	R/W	H'E659_002E	16	√	√	√	√
Interrupt enable register 0	INTENB0	R/W	H'E659_0030	16	√	√	√	√
BRDY interrupt enable register	BRDYENB	R/W	H'E659_0036	16	√	√	√	√
NRDY interrupt enable register	NRDYENB	R/W	H'E659_0038	16	√	√	√	√
BEMP interrupt enable register	BEMPENB	R/W	H'E659_003A	16	√	√	√	√
SOF output configuration register	SOFCFG	R/W	H'E659_003C	16	√	√	√	√
Interrupt status register 0	INTSTS0	R/W	H'E659_0040	16	√	√	√	√
BRDY interrupt status register	BRDYSTS	R/W	H'E659_0046	16	√	√	√	√
NRDY interrupt status register	NRDYSTS	R/W	H'E659_0048	16	√	√	√	√
BEMP interrupt status register	BEMPSTS	R/W	H'E659_004A	16	√	√	√	√
Frame number register	FRMNUM	R/W	H'E659_004C	16	√	√	√	√
μ frame number register	UFRMNUM	R/W	H'E659_004E	16	√	√	√	√
USB address register	USBADDR	R	H'E659_0050	16	√	√	√	√
USB request type register	USBREQ	R	H'E659_0054	16	√	√	√	√
USB request value register	USBVAL	R	H'E659_0056	16	√	√	√	√
USB request index register	USBINDX	R	H'E659_0058	16	√	√	√	√
USB request length register	USBLENG	R	H'E659_005A	16	√	√	√	√
DCP maximum packet size register	DCPMAXP	R/W	H'E659_005E	16	√	√	√	√
DCP control register	DCPCTR	R/W	H'E659_0060	16	√	√	√	√
Pipe window select register	PIPESEL	R/W	H'E659_0064	16	√	√	√	√



Register Name	Abbreviation	R/W	Address	Access Size	RZ/G Series Products			
					RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Pipe configuration register	PIPECFG	R/W	H'E659_0068	16	√	√	√	√
Pipe buffer register	PIPEBUF	R/W	H'E659_006A	16	√	√	√	√
Pipe maximum packet size register	PIPEMAXP	R/W	H'E659_006C	16	√	√	√	√
Pipe cycle control register	PIPEPERI	R/W	H'E659_006E	16	√	√	√	√
Pipe 1 control register	PIPE1CTR	R/W	H'E659_0070	16	√	√	√	√
Pipe 2 control register	PIPE2CTR	R/W	H'E659_0072	16	√	√	√	√
Pipe 3 control register	PIPE3CTR	R/W	H'E659_0074	16	√	√	√	√
Pipe 4 control register	PIPE4CTR	R/W	H'E659_0076	16	√	√	√	√
Pipe 5 control register	PIPE5CTR	R/W	H'E659_0078	16	√	√	√	√
Pipe 6 control register	PIPE6CTR	R/W	H'E659_007A	16	√	√	√	√
Pipe 7 control register	PIPE7CTR	R/W	H'E659_007C	16	√	√	√	√
Pipe 8 control register	PIPE8CTR	R/W	H'E659_007E	16	√	√	√	√
Pipe 9 control register	PIPE9CTR	R/W	H'E659_0080	16	√	√	√	√
Pipe A control register	PIPEACTR	R/W	H'E659_0082	16	√	√	√	√
Pipe B control register	PIPEBCTR	R/W	H'E659_0084	16	√	√	√	√
Pipe C control register	PIPECCTR	R/W	H'E659_0086	16	√	√	√	√
Pipe D control register	PIPEDCTR	R/W	H'E659_0088	16	√	√	√	√
Pipe E control register	PIPEECTR	R/W	H'E659_008A	16	√	√	√	√
Pipe F control register	PIPEFCTR	R/W	H'E659_008C	16	√	√	√	√
Pipe 1 transaction counter enable register	PIPE1TRE	R/W	H'E659_0090	16	√	√	√	√
Pipe 1 transaction counter register	PIPE1TRN	R/W	H'E659_0092	16	√	√	√	√
Pipe 2 transaction counter enable register	PIPE2TRE	R/W	H'E659_0094	16	√	√	√	√
Pipe 2 transaction counter register	PIPE2TRN	R/W	H'E659_0096	16	√	√	√	√
Pipe 3 transaction counter enable register	PIPE3TRE	R/W	H'E659_0098	16	√	√	√	√
Pipe 3 transaction counter register	PIPE3TRN	R/W	H'E659_009A	16	√	√	√	√
Pipe 4 transaction counter enable register	PIPE4TRE	R/W	H'E659_009C	16	√	√	√	√
Pipe 4 transaction counter register	PIPE4TRN	R/W	H'E659_009E	16	√	√	√	√
Pipe 5 transaction counter enable register	PIPE5TRE	R/W	H'E659_00A0	16	√	√	√	√
Pipe 5 transaction counter register	PIPE5TRN	R/W	H'E659_00A2	16	√	√	√	√
Pipe B transaction counter enable register	PIPEBTRE	R/W	H'E659_00A4	16	√	√	√	√

Register Name	Abbreviation	R/W	Address	Access Size	RZ/G Series Products			
					RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Pipe B transaction counter register	PIPEBTRN	R/W	H'E659_00A6	16	√	√	√	√
Pipe C transaction counter enable register	PIPECTRE	R/W	H'E659_00A8	16	√	√	√	√
Pipe C transaction counter register	PIPECTRN	R/W	H'E659_00AA	16	√	√	√	√
Pipe D transaction counter enable register	PIPEDTRE	R/W	H'E659_00AC	16	√	√	√	√
Pipe D transaction counter register	PIPEDTRN	R/W	H'E659_00AE	16	√	√	√	√
Pipe E transaction counter enable register	PIPEETRE	R/W	H'E659_00B0	16	√	√	√	√
Pipe E transaction counter register	PIPEETRN	R/W	H'E659_00B2	16	√	√	√	√
Pipe F transaction counter enable register	PIPEFTRE	R/W	H'E659_00B4	16	√	√	√	√
Pipe F transaction counter register	PIPEFTRN	R/W	H'E659_00B6	16	√	√	√	√
Pipe 9 transaction counter enable register	PIPE9TRE	R/W	H'E659_00B8	16	√	√	√	√
Pipe 9 transaction counter register	PIPE9TRN	R/W	H'E659_00BA	16	√	√	√	√
Pipe A transaction counter enable register	PIPEATRE	R/W	H'E659_00BC	16	√	√	√	√
Pipe A transaction counter register	PIPEATRAN	R/W	H'E659_00BE	16	√	√	√	√
D2FIFO port select register	D2FIFOSEL	R/W	H'E659_00F0	16	√	√	√	√
D2FIFO port control register	D2FIFOCTR	R/W	H'E659_00F2	16	√	√	√	√
D3FIFO port select register	D3FIFOSEL	R/W	H'E659_00F4	16	√	√	√	√
D3FIFO port control register	D3FIFOCTR	R/W	H'E659_00F6	16	√	√	√	√
Low power status register	LPSTS	R/W	H'E659_0102	16	√	√	√	√
USB general control register	UGCTRL	R/W	H'E659_0180	32	√	√	√	√
USB general control register 2	UGCTRL2	R/W	H'E659_0184	32	√	√	√	√
USB general status register	UGSTS	R	H'E659_0188	32	√	√	√	√

**Table 52.3 Register States in Each Processing Mode**

<b>Abbreviation</b>	<b>Power-On Reset</b>	<b>Module Standby</b>
SYSCFG	Initialized	Retained
BUSWAIT	Initialized	Retained
SYSSTS	Initialized	Retained
DVSTCTR	Initialized	Retained
TESTMODE	Initialized	Retained
CFIFO	Initialized	Retained
CFIFOSEL	Initialized	Retained
CFIFOCTR	Initialized	Retained
D0FIFOSEL	Initialized	Retained
D0FIFOCTR	Initialized	Retained
D1FIFOSEL	Initialized	Retained
D1FIFOCTR	Initialized	Retained
INTENB0	Initialized	Retained
BRDYENB	Initialized	Retained
NRDYENB	Initialized	Retained
BEMPENB	Initialized	Retained
SOFCFG	Initialized	Retained
INTSTS0	Initialized	Retained
BRDYSTS	Initialized	Retained
NRDYSTS	Initialized	Retained
BEMPSTS	Initialized	Retained
FRMNUM	Initialized	Retained
UFRMNUM	Initialized	Retained
USBADDR	Initialized	Retained
USBREQ	Initialized	Retained
USBVAL	Initialized	Retained
USBINDX	Initialized	Retained
USBLENG	Initialized	Retained
DCPMAXP	Initialized	Retained
DCPCTR	Initialized	Retained
PIPESEL	Initialized	Retained
PIPECFG	Initialized	Retained
PIPEBUF	Initialized	Retained
PIPEMAXP	Initialized	Retained
PIPEPERI	Initialized	Retained
PIPE1CTR	Initialized	Retained
PIPE2CTR	Initialized	Retained
PIPE3CTR	Initialized	Retained
PIPE4CTR	Initialized	Retained
PIPE5CTR	Initialized	Retained
PIPE6CTR	Initialized	Retained
PIPE7CTR	Initialized	Retained

<b>Abbreviation</b>	<b>Power-On Reset</b>	<b>Module Standby</b>
PIPE8CTR	Initialized	Retained
PIPE9CTR	Initialized	Retained
PIPEACTR	Initialized	Retained
PIPEBCTR	Initialized	Retained
PIPECCTR	Initialized	Retained
PIPEDCTR	Initialized	Retained
PIPEECTR	Initialized	Retained
PIPEFCTR	Initialized	Retained
PIPE1TRE	Initialized	Retained
PIPE1TRN	Initialized	Retained
PIPE2TRE	Initialized	Retained
PIPE2TRN	Initialized	Retained
PIPE3TRE	Initialized	Retained
PIPE3TRN	Initialized	Retained
PIPE4TRE	Initialized	Retained
PIPE4TRN	Initialized	Retained
PIPE5TRE	Initialized	Retained
PIPE5TRN	Initialized	Retained
PIPEBTRN	Initialized	Retained
PIPEBTRN	Initialized	Retained
PIPECTRN	Initialized	Retained
PIPECTRN	Initialized	Retained
PIPEDTRN	Initialized	Retained
PIPEDTRN	Initialized	Retained
PIPEETRN	Initialized	Retained
PIPEETRN	Initialized	Retained
PIPEFTRN	Initialized	Retained
PIPEFTRN	Initialized	Retained
PIPE9TRE	Initialized	Retained
PIPE9TRN	Initialized	Retained
PIPEATRE	Initialized	Retained
PIPEATRN	Initialized	Retained
D2FIFOSEL	Initialized	Retained
D2FIFOCTR	Initialized	Retained
D3FIFOSEL	Initialized	Retained
D3FIFOCTR	Initialized	Retained
LPSTS	Initialized	Retained
UGCTRL	Initialized	Retained
UGCTRL2	Initialized	Retained
UGSTS	Initialized	Retained

### 52.2.1 System Configuration Control Register (SYSCFG)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SYSCFG enables or disables high-speed operation, controls DP\_0 and DM\_0 pins, and enables or disables the operation of this module.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	HSE	—	—	DPRPU	—	—	—	USBE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R	R	R/W	R	R	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 11	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
10	—	0	R/W	Reserved This bit is always read as 0. Writes have no effect.
9, 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7	HSE	0	R/W	High-Speed Operation Enable 0: High-speed operation is disabled. When the function controller function is selected: Full-speed operation only 1: High-speed operation is enabled. (This module detects the transmission rate.) When HSE is 0, this module performs full-speed operation. When HSE is 1, this module executes the reset handshake protocol, and according to the result, this module automatically performs high-speed or full-speed operation. Change this bit while the DPRPU bit is 0.
6, 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	DPRPU	0	R/W	D+ Line Resistance Control Enables or disables pull-up of the D+ line when the function controller function is selected. 0: Pull-up is disabled. 1: Pull-up is enabled. When this bit is set to 1 with the function controller function selected, this module pulls up the D+ line at 3.3V, and informs the USB host of ATTACH. Clearing this bit to 0 cancels the pull-up of the D+ line, and informs the USB host of DETACH. Set this bit to 1 before using this module.
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
0	USBE	0	R/W	<p>USB Module Operation Enable</p> <p>Enables or disables the USB module operation.</p> <p>0: The USB module operation is disabled.</p> <p>1: The USB module operation is enabled.</p> <p>Table 52.4 lists the registers and bit names initialized when this bit is cleared to 0.</p>

**Table 52.4 Registers Initialized by Writing 0 in the USBE Bit**

Register Name	Bit Name
SYSSTS	LNST
DVSTCTR	RHST
INTSTS0	DVSQ
USBADDR	USBADDR
USEREQ	BRequest, bmRequestType
USBVAL	wValue
USBINDX	wIndex
USBLENG	wLength

### 52.2.2 CPU Bus Wait Register (BUSWAIT)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

BUSWAIT specifies the number of access waits from the CPU to this module.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	BWAIT[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3 to 0	BWAIT[3:0]	1111	R/W	<p>CPU Bus Wait</p> <p>Specify the number of access waits to this module.</p> <p>0000: 0 waits (2 access cycles)</p> <p>0001: 1 wait (3 access cycles)</p> <p>0010 to 1110: 2 to 14 waits (4 to 16 access cycles)</p> <p>1111: 15 waits (17 access cycles) initial value</p> <p>The following restriction is provided for access cycles to the registers of addresses beginning with H'04 of this controller.</p> <p>Restriction for wait: The cycle of continuous accesses to the registers of this controller must be 80 ns or more.</p> <p>To satisfy this restriction, control waits using the frequency of system clock HP<math>\phi</math>. Choose the best value within the initial value of 17 clock cycles (maximum).</p> <p>This setting is the same as the waits in accesses to the FIFO port register. The maximum speed of accesses to the FIFO port is as follows:</p> <p>MBW = B'10 (32-bit width) : Max. 48 Mbytes/s</p> <p>MBW = B'01 (16-bit width) : Max. 24 Mbytes/s</p> <p>MBW = B'00 (8-bit width) : Max. 12 Mbytes/s</p>

### 52.2.3 System Configuration Status Register (SYSSTS)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SYSSTS monitors the USB data bus line status (D+ and D- lines).

This register is initialized by a power-on reset or a USB reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	LINE[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1, 0	LNST[1:0]	Undefined*	R	USB Data Line Status Monitor Indicate the USB data bus line (D+ and D- lines) status. Table 52.5 shows the USB data bus line status. Read these bits after the attach processing (DPRPU = 1).

Note: \* These bits depend on the state of the DP, DM, OVC, and IDIN pins.

**Table 52.5 USB Data Bus Line Status**

LNST[1]	LNST[0]	Full-Speed Operation	High-Speed Operation	Chirp Operation
0	0	SE0	Squelch	Squelch
0	1	J-State	UnSquelch	Chirp J
1	0	K-State	Invalid	Chirp K
1	1	SE1	Invalid	Invalid

Legend:

Chirp:	The reset handshake protocol (RHSP) is being executed with high-speed operation is enabled (HSE = 1 in SYSCFG).
Squelch:	SE0 or idle state
UnSquelch:	High-speed J-State or high-speed K-State
Chirp J:	Chirp J-State
Chirp K:	Chirp K-State
Invalid:	Invalid



### 52.2.4 Device State Control Register (DVSTCTR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

DVSTCTR controls and monitors the USB data bus state.

This register is initialized by a power-on reset. The WKUP bit is initialized and the RESUME bit becomes undefined by a USB bus reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	WKUP	—	—	—	—	—	RHST[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	WKUP	0	R/W*	Wakeup Output Enables or disables the remote wakeup (resume signal output) to the USB bus when the function controller function is selected. 0: The remote wakeup signal is not output. 1: The remote wakeup signal is output. This module controls the remote wakeup signal output time. When this bit is set to 1, this module outputs 10 ms K-State and then clears this bit. The USB Specification requires the USB bus idle state to be maintained for at least 5 ms before transmitting the remote wakeup signal. For this reason, this module outputs K-State after waiting for 2 ms even if 1 is written in this bit immediately after the suspended state is detected. Write 1 in this bit only when the device is in the suspended state (DVSQ = 1xx in INTSTS0) and remote wakeup is enabled by the USB host. When setting this bit to 1, do not stop the internal clock even in the suspended state.
7 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2 to 0	RHST[2:0]	000	R	Reset Handshake Indicate the reset handshake state. 000: Transmission rate is undefined. 100: The reset handshake processing is in progress. 010: Full-speed connection 011: High-speed connection When this module detects a USB bus reset with the HSE bit set to 1 for the port, these bits become B'100. After that, when this module outputs ChirpK and detects ChirpJK from the USB host three times, these bits become B'011. Unless high-speed mode is fixed within 2.5 ms after the ChirpK output, these bits become B'010. When this module detects a USB bus reset with the HSE bit set to 0 for the port, these bits become B'010. When the RHST bits are fixed to B'010 or B'011 after this module detected a USB bus reset, the DVST interrupt occurs.

### 52.2.5 Test Mode Register (TESTMODE)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

TESTMODE controls the USB test signal output in high-speed operation mode.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	UTST[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3 to 0	UTST[3:0]	0000	R/W	Test Mode Table 52.6 shows the test mode operation of this module. Control the USB test signal output in high-speed operation mode. These bits are valid only in high-speed operation mode. Use this test mode when the RHST bits in DVSTCTR are B'011. After the test with these bits, cancel this test mode by a power-on reset. Set these bits according to the SetFeature request from the USB host during high-speed communication. While these bits are B'0001 to B'0100, this module does not enter the suspended state.

**Table 52.6 Test Mode Operation**

Test Mode	UTST Bits Setting
Normal operation	B'0000
Test_J	B'0001
Test_K	B'0010
Test_SE0_NAK	B'0011
Test_Packet	B'0100
Test_Force_Enable	—
Reserved	B'0101 to B'0111

### 52.2.6 CFIFO Port Register

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

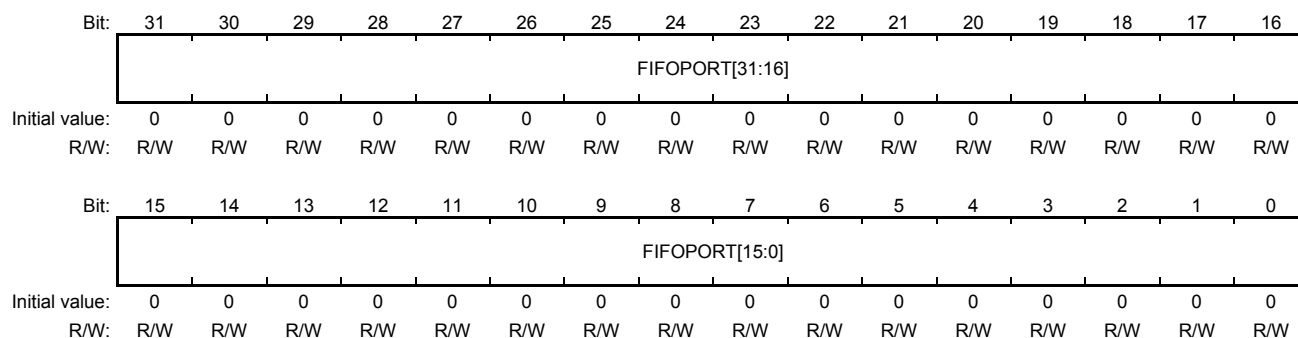
CFIFO is a port register to read data from or write data to the FIFO buffer memory.

Each FIFO port consists of this register (CFIFO) for data read/write from/to the FIFO buffer memory, the select registers (CFIFOSEL, D0FIFOSEL, D1FIFOSEL, D2FIFOSEL and D3FIFOSEL) to select pipes to be allocated to a FIFO port, and the control registers (CFIFOCTR, D0FIFOCTR, D1FIFOCTR, D2FIFOCTR and D3FIFOCTR).

Each FIFO port provides the following features.

- Make accesses to the FIFO buffer for DCP through the CFIFO port.
- Make accesses to the FIFO buffer with DMA transfers through the DMAC module for USB high-speed only.
- When using a function specific to FIFO ports (DMA transfer function, etc.), the pipe number (selected pipe) specified by the CURPIPE bits cannot be changed.
- Register groups of a FIFO port do not affect other FIFO ports.
- Do not allocate the same pipe number to different FIFO ports.
- There are two FIFO buffer states where the access mastership is on the CPU side and on the SIE side. When the FIFO buffer access mastership is on the SIE side, the CPU cannot make an access to the FIFO buffer.

This register is initialized by a power-on reset.



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	FIFOPORT [31:0]	All 0	R/W	<p>FIFO Port</p> <p>Read receive data from the FIFO buffer or write transmit data to the FIFO buffer using these bits.</p> <p>Access to this register is enabled only when the FRDY bit in each control register (CFIFOCTR, D0FIFOCTR, D1FIFOCTR, D2FIFOCTR and D3FIFOCTR) is set to 1.</p> <p>Valid bits in this register vary with the value of the MBW bits. Table 52.7 shows the valid bits in this register.</p>

**Table 52.7 Operation of This Register when Accessed**

Access Size	Bits 31 to 24	Bits 23 to 16	Bits 15 to 8	Bits 7 to 0
32 bits	N + 3 address	N + 2 address	N + 1 address	N + 0 address
16 bits	Write: Invalid, Read: Prohibited*		N + 1 address	N + 0 address
8 bits	Write: Invalid, Read: Prohibited*			N + 0 address

Note: \* Reading an invalid register with word access or byte access is prohibited.

### 52.2.7 FIFO Port Select Registers (CFIFOSEL, D0FIFOSEL, D1FIFOSEL, D2FIFOSEL, D3FIFOSEL)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CFIFOSEL, D0FIFOSEL, D1FIFOSEL, D2FIFOSEL and D3FIFOSEL select pipes to be allocated to FIFO ports and control accesses to each FIFO port.

Do not specify the same pipe number for the CURPIPE bits in CFIFOSEL, D0FIFOSEL, D1FIFOSEL, D2FIFOSEL and D3FIFOSEL. When the CURPIPE bits in D0FIFOSEL, D1FIFOSEL, D2FIFOSEL and D3FIFOSEL are set to B'000, no pipe is specified.

Do not change any pipe number when DMA transfer is enabled.

This register is initialized by a power-on reset.

#### (1) CFIFOSEL

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RCNT	REW	—	—	MBW[1:0]	—	—	—	—	ISEL	—	CURPIPE[3:0]				
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R	R	R/W	R/W	R	R	R	R	R/W	R	R/W	R/W	R/W	R/W

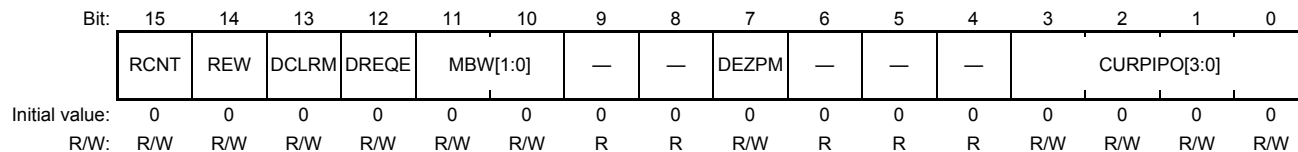
Bit	Bit Name	Initial Value	R/W	Description
15	RCNT	0	R/W	<p>Read Count Mode</p> <p>Specifies read mode of the DTLN bits in CFIFOCTR.</p> <p>0: Clears the DTLN bits after reading all receive data in the CFIFO (or after reading receive data of one side of the double buffer).</p> <p>1: Counts down the DTLN bits at each reading of CFIFO receive data.</p>
14	REW	0	R/W	<p>Buffer Pointer Rewind</p> <p>Specifies whether to rewind the buffer pointer or not.</p> <p>0: The buffer pointer is not rewind.</p> <p>1: The buffer pointer is rewind.</p> <p>When the selected pipe is in the receive direction and this bit is set to 1 during FIFO buffer reading, the FIFO buffer can be read from the first data. (In the case of a double buffer, the first data of one side that is being read can be read again.)</p> <p>Do not set this bit to 1 concurrently with the CURPIPE setting change. Be sure to confirm that the FRDY bit is 1 when setting this bit to 1.</p> <p>To rewrite the FIFO buffer data from the first data for a pipe in the transmit direction, use the BCLR bit.</p>
13, 12	—	All 0	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>

Bit	Bit Name	Initial Value	R/W	Description
11, 10	MBW[1:0]	00	R/W	<p>CFIFO Port Access Bit Width</p> <p>Specify the bit width for accesses to the CFIFO port.</p> <p>00: 8 bits 01: 16 bits 10: 32 bits 11: Setting prohibited</p> <p>When the selected pipe is in the receive direction and data read is started after these bits are set, do not change these bits until all data is completely read.</p> <p>When the selected pipe is in the receive direction, set the CURPIPE and MBW bits at the same time.</p> <p>When the selected pipe is in the transmit direction, no bit width can be changed (from 8 bits to 16/32 bits or from 16 bits to 32 bits) during data write to the buffer memory.</p> <p>When 8-bit width or 16-bit width is selected, data of odd bytes can also be written by controlling the byte access.</p>
9 to 6	—	All 0	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>
5	ISEL	0	R/W	<p>CFIFO Port Access Direction when DCP is Selected</p> <p>0: Buffer memory read is selected. 1: Buffer memory write is selected.</p> <p>To change this bit when the selected pipe is DCP, write 1 or 0 in this bit, read the value of this bit, confirm that the write value equals the read value, and then proceed with the next processing.</p> <p>If this bit is changed in the middle of access to the FIFO buffer, accesses made before that time are retained, the value of this bit is rewritten, and then further access is enabled.</p> <p>Set this bit concurrently with the CURPIPE bits.</p>
4	—	0	R	<p>Reserved</p> <p>This bit is always read as 0. The write value should always be 0.</p>

Bit	Bit Name	Initial Value	R/W	Description
3 to 0	CURPIPE [3:0]	0000	R/W	<p>CFIFO Port Access Pipe Select</p> <p>Set the number of pipe to be used for data read or write through the CFIFO port.</p> <p>0000: DCP</p> <p>0001: Pipe 1</p> <p>0010: Pipe 2</p> <p>0011: Pipe 3</p> <p>0100: Pipe 4</p> <p>0101: Pipe 5</p> <p>0110: Pipe 6</p> <p>0111: Pipe 7</p> <p>1000: Pipe 8</p> <p>1001: Pipe 9</p> <p>1010: Pipe A</p> <p>1011: Pipe B</p> <p>1100: Pipe C</p> <p>1101: Pipe D</p> <p>1110: Pipe E</p> <p>1111: Pipe F</p> <p>To change these bits, write a value in these bits, read the value of these bits, confirm that the write value equals the read value, and then proceed with the next processing.</p> <p>Do not write the same pipe number in the CURPIPE bits in CFIFOSEL, D0FIFOSEL, D1FIFOSEL, D2FIFOSEL and D3FIFOSEL.</p> <p>If these bits are changed in the middle of access to the FIFO buffer, accesses made before that time are retained, the value of these bits is rewritten, and then further access is enabled.</p>

Note: \* Only reading 0 is enabled.

(2) D0FIFOSEL, D1FIFOSEL, D2FIFOSEL, D3FIFOSEL



Bit	Bit Name	Initial Value	R/W	Description
15	RCNT	0	R/W	<p>Read Count Mode</p> <p>Specifies read mode of the DTLN bits in DnFIFOCTR.</p> <p>0: Clears the DTLN bits after reading all receive data in the DnFIFO (or after reading receive data of one side of the double buffer).</p> <p>1: Counts down the DTLN bits at each reading of DnFIFO receive data.</p> <p>When making an access to the DnFIFO with the BFRE bit set to 1, set this bit to 0.</p>
14	REW	0	R/W*	<p>Buffer Pointer Rewind</p> <p>Specifies whether to rewind the buffer pointer or not.</p> <p>0: The buffer pointer is not rewound.</p> <p>1: The buffer pointer is rewound.</p> <p>When the selected pipe is in the receive direction and this bit is set to 1 during FIFO buffer reading, the FIFO buffer can be read from the first data. (In the case of a double buffer, the first data of one side that is being read can be read again.)</p> <p>Do not set this bit to 1 concurrently with the CURPIPE setting change. Be sure to confirm that the FRDY bit is 1 when setting this bit to 1.</p> <p>When making an access to the DnFIFO with the BFRE bit set to 1, do not set this bit to 1 when the short packet data is completely read.</p> <p>To rewrite the FIFO buffer data from the first data for a pipe in the transmit direction, use the BCLR bit.</p>
13	DCLRM	0	R/W	<p>Buffer Memory Auto-Clear Mode after Reading Data of Selected Pipe</p> <p>Enables or disables buffer memory auto-clear mode after reading data of the selected pipe.</p> <p>0: Buffer memory auto-clear mode is disabled.</p> <p>1: Buffer memory auto-clear mode is enabled.</p> <p>When this bit is 1 and a Zero-Length packet is received while the FIFO buffer allocated to the selected pipe is empty or when a short packet is received with the BFRE bit set to 1 and the packet data is completely read, this module performs buffer clear (BCLR = 1 processing) of the FIFO buffer.</p> <p>When using this module with the BRDYM bit set to 1, be sure to set this bit to 0.</p>
12	DREQE	0	R/W	<p>DMA Transfer Request Enable</p> <p>Enables or disables making a DMA transfer request.</p> <p>0: DMA transfer request is disabled.</p> <p>1: DMA transfer request is enabled.</p> <p>To enable a DMA transfer request, set the CURPIPE bits and then set this bit to 1.</p> <p>Set this bit to 0 before changing the CURPIPE setting.</p>



Bit	Bit Name	Initial Value	R/W	Description
11, 10	MBW[1:0]	00	R/W	<p>FIFO Port Access Bit Width</p> <p>Specify the bit width for accesses to the DnFIFO port.</p> <p>00: 8 bits 01: 16 bits 10: 32 bits 11: Setting prohibited</p> <p>When the selected pipe is in the receive direction and data read is started after these bits are set, do not change these bits until all data is completely read.</p> <p>When the selected pipe is in the receive direction, set the CURPIPE and MBW bits at the same time.</p> <p>When the selected pipe is in the transmit direction, no bit width can be changed (from 8 bits to 16/32 bits or from 16 bits to 32 bits) during data write to the buffer memory.</p> <p>When 8-bit width or 16-bit width is selected, data of odd bytes can also be written by controlling the byte access.</p>
9, 8	—	All 0	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>
7	DEZPM	0	R/W	<p>DEZPM: Zero-Length Packet Addition Mode</p> <p>If the DMA transfer size that is set for the USBHS-DMAC modules is an integral multiple of the maximum packet size, a null packet is added after all of the data has been sent.</p> <p>0: Disables addition of packets. 1: Enables addition of packets.</p> <p>This bit is applied to pipes used to write to the FIFO buffer.</p> <p>DEZPM must be set before starting DMA transfers.</p> <p>If the DEZPM bit is set after DMA transfers complete, no null packets are added.</p> <p>Note: This mode depends on the buffer size (PIPEBUF.BUFSIZE[4:0]).</p> <p>A null packet is added after transferring data up to buffer size which is defined by PIPEBUF.BUFSIZE[4:0].</p> <p>When transfer data size is over 2Kbytes, this mode must not be used because max size of buffer is 2Kbytes.</p> <p>In that case, please add the null packet by SW with BVAL bit of FIFO Port Control Registers.</p>
6 to 4	—	All 0	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>

Bit	Bit Name	Initial Value	R/W	Description
3 to 0	CURPIPE [3:0]	0000	R/W	<p>FIFO Port Access Pipe Select</p> <p>Set the number of pipe to be used for data read or write through the DnFIFO ports.</p> <p>0000: No pipe 0001: Pipe 1 0010: Pipe 2 0011: Pipe 3 0100: Pipe 4 0101: Pipe 5 0110: Pipe 6 0111: Pipe 7 1000: Pipe 8 1001: Pipe 9 1010: Pipe A 1011: Pipe B 1100: Pipe C 1101: Pipe D 1110: Pipe E 1111: Pipe F</p> <p>To change these bits, write a value in these bits, read the value of these bits, confirm that the write value equals the read value, and then proceed with the next processing.</p> <p>Do not write the same pipe number in the CURPIPE bits in CFIFOSEL, DnFIFOSEL (n = 0 to 3).</p> <p>If these bits are changed in the middle of access to the FIFO buffer, accesses made before that time are retained, the value of these bits is rewritten, and then further access is enabled.</p>

Note: \* Only reading 0 is enabled.

### 52.2.8 FIFO Port Control Registers (CFIFOCTR, D0FIFOCTR, D1FIFOCTR, D2FIFOCTR, D3FIFOCTR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CFIFOCTR and D0FIFOCTR, D1FIFOCTR, D2FIFOCTR and D3FIFOCTR specify buffer memory write end and CPU buffer clear, as well as indicate whether the FIFO port is accessible or not. These registers correspond to each FIFO port.

These registers are initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BVAL	BCLR	FRDY	—	DTLN[11:0]											
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15	BVAL	0	R/W*1	<p><b>Buffer Memory Enable Flag</b></p> <p>This flag is set to 1 upon completion of data write in the FIFO buffer of the CPU of the pipe selected by the CURPIPE bits.</p> <p>0: Invalid 1: Write end</p> <p>When the selected pipe is in the transmit direction, set this bit to 1 in the following cases. This module sets the FIFO buffer of the CPU to the SIE side to enable data transmission.</p> <p>To send a short packet, set this bit to 1 upon completion of data write.</p> <p>To send a Zero-Length packet, set this bit to 1 before writing data to the FIFO buffer.</p> <p>For pipes of continuous transfer mode, set this bit to 1 after writing data that is a positive integer multiple of MaxPacketSize and less than the BufferSize value.</p> <p>When data with the size specified by MaxPacketSize is written to a pipe of continuous transfer mode, this module writes 1 in this bit and sets the FIFO buffer of the CPU to the SIE side to enable data transmission.</p> <p>Set this bit to 1 when this module shows FRDY = 1.</p> <p>When the selected pipe is in the receive direction, do not set this bit to 1.</p>

Bit	Bit Name	Initial Value	R/W	Description
14	BCLR	0	R/W*2	<p>CPU buffer clear</p> <p>Clears the CPU side FIFO buffer of the selected pipe.</p> <p>0: Invalid</p> <p>1: Clears the CPU side FIFO buffer.</p> <p>When the FIFO buffer assigned to the selected pipe is set to a double buffer, and even when both sides of the buffer are readable, this module clears only one side of the FIFO buffer.</p> <p>When the selected pipe is DCP, this module clears the FIFO buffer when this bit is set to 1 irrespective of whether the FIFO buffer is on the CPU side or SIE side. When clearing the SIE side FIFO buffer, be sure to set the PID bits in DCP to NAK and then set the BCLR bit to 1.</p> <p>When the selected pipe is in the transmit direction, and if 1 is written in the BVAL and BCLR bits at the same time, this module clears the previously written data, and makes a Zero-Length packet transmittable.</p> <p>When the selected pipe is not DCP, write 1 in this bit while the FRDY flag indicates 1.</p>
13	FRDY	0	R	<p>FIFO Port Ready</p> <p>Indicates whether the CPU (DMAC) can access the FIFO port.</p> <p>0: The FIFO port is not accessible.</p> <p>1: The FIFO port is accessible.</p> <p>This module indicates FRDY = 1 in the following cases. However, since there is no data to read, no data can be read from the FIFO port. In these cases, set the BCLR bit to 1 to clear the FIFO buffer to make transmission/reception of the next data available.</p> <p>When a Zero-Length packet is received with the FIFO buffer assigned to the selected pipe empty</p> <p>When a short packet is received with BFRE set to 1 and the packet data is completely read</p>
12	—	0	R	<p>Reserved</p> <p>This bit is always read as 0. The write value should always be 0.</p>
11 to 0	DTLN[11:0]	H'000	R	<p>Receive Data Length</p> <p>Indicate the receive data length.</p> <p>The value of these bits during FIFO buffer reading varies as follows depending on the setting of the RCNT bit.</p> <p>When RCNT = 0:</p> <p>This module indicates the receive data length with these bits until the CPU (DMAC) finishes reading one side of the FIFO buffer.</p> <p>When BFRE is 1, this module retains the receive data length until the BCLR bit is set to 1 after the FIFO buffer read is completed.</p> <p>When RCNT = 1:</p> <p>This module decrements the value of the DTLN bits in each read cycle (-1 when MBW = 0, and -2 when MBW = 1)</p> <p>When reading out from a single FIFO buffer is complete, DTLN = 0 for this module. However, the behavior is different when double-buffering has been specified. If reading out of data from one side is not finished before the other side is full of received data, when all data have been read out from the first side, the DTLN bits reflect the amount of data received in the other side.</p> <p>When reading these bits during FIFO buffer reading while the RCNT bit is 1, note that this module updates the value in these bits within 150 ns after each FIFO port read cycle.</p>

- Notes:
1. Only writing 1 is enabled.
  2. Only reading 0 and writing 1 are enabled.

### 52.2.9 Interrupt Enable Register 0 (INTENB0)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

INTENB0 specifies masking of each interrupt when selection for function controller. When this module detects an interrupt for which 1 is written in the corresponding bit in this register by the software, this module generates a USB interrupt.

When interrupt source detection conditions are satisfied irrespective of the register setting (interrupt enable/disable), this module sets the corresponding status bit in INTSTS0.

When the software changes an interrupt enable bit (0 to 1) whose interrupt source status bit in INTSTS0 is set to 1, this module generates a USB interrupt.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VBSE	RSME	SOFE	DVSE	CTRE	BEMPE	NRDYE	BRDYE	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15	VBSE	0	R/W	VBUS_0 and VBUSIN_0 Interrupt Enable Enables or disables USB interrupt outputs when the VBINT interrupt is detected. 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
14	RSME	0	R/W	Resume Interrupt Enable Enables or disables USB interrupt outputs when the RESM interrupt is detected. 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
13	SOFE	0	R/W	Frame Number Update Interrupt Enable Enables or disables USB interrupt outputs when the SOFR interrupt is detected. 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
12	DVSE	0	R/W	Device State Transition Interrupt Enable* Enables or disables USB interrupt outputs when the DVST interrupt is detected. 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
11	CTRE	0	R/W	Control Transfer Stage Transition Interrupt Enable* Enables or disables USB interrupt outputs when the CTRT interrupt is detected. 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.

Bit	Bit Name	Initial Value	R/W	Description
10	BEMPE	0	R/W	<b>Buffer Empty Interrupt Enable</b> Enables or disables USB interrupt outputs when the BEMP interrupt is detected. 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
9	NRDYE	0	R/W	<b>Buffer Not Ready Response Interrupt Enable</b> Enables or disables USB interrupt outputs when the NRDY interrupt is detected. 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
8	BRDYE	0	R/W	<b>Buffer Ready Interrupt Enable</b> Enables or disables USB interrupt outputs when the BRDY interrupt is detected. 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
7 to 0	—	All 0	R	<b>Reserved</b> These bits are always read as 0. The write value should always be 0.

**52.2.10 BRDY Interrupt Enable Register (BRDYENB)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

BRDYENB enables or disables the BRDY bit to be set to 1 when the BRDY interrupt of a pipe is detected.

When this module detects the BRDY interrupt of a pipe for which the software sets the corresponding bit in this register to 1, this module sets the PIPEBRDY bit of the pipe in BRDYSTS and also sets the BRDY bit in INTSTS0 and generates the BRDY interrupt.

When one or more PIPEBRDY bits in BRDYSTS are 1 and the software changes the corresponding interrupt enable bit(s) in this register from 0 to 1, this module generates the BRDY interrupt.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PIPEF BRDYE	PIPEE BRDYE	PIPED BRDYE	PIPEC BRDYE	PIPEB BRDYE	PIPEA BRDYE	PIPE9 BRDYE	PIPE8 BRDYE	PIPE7 BRDYE	PIPE6 BRDYE	PIPE5 BRDYE	PIPE4 BRDYE	PIPE3 BRDYE	PIPE2 BRDYE	PIPE1 BRDYE	PIPE0 BRDYE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	PIPEF BRDYE	0	R/W	Pipe F BRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
14	PIPEE BRDYE	0	R/W	Pipe E BRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
13	PIPED BRDYE	0	R/W	Pipe D BRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
12	PIPEC BRDYE	0	R/W	Pipe C BRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
11	PIPEB BRDYE	0	R/W	Pipe B BRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
10	PIPEA BRDYE	0	R/W	Pipe A BRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
9	PIPE9 BRDYE	0	R/W	Pipe 9 BRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
8	PIPE8 BRDYE	0	R/W	Pipe 8 BRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.



Bit	Bit Name	Initial Value	R/W	Description
7	PIPE7 BRDYE	0	R/W	Pipe 7 BRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
6	PIPE6 BRDYE	0	R/W	Pipe 6 BRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
5	PIPE5 BRDYE	0	R/W	Pipe 5 BRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
4	PIPE4 BRDYE	0	R/W	Pipe 4 BRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
3	PIPE3 BRDYE	0	R/W	Pipe 3 BRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
2	PIPE2 BRDYE	0	R/W	Pipe 2 BRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
1	PIPE1 BRDYE	0	R/W	Pipe 1 BRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
0	PIPE0 BRDYE	0	R/W	Pipe 0 BRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.

**52.2.11 NRDY Interrupt Enable Register (NRDYENB)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

NRDYENB enables or disables the NRDY bit to be set to 1 when the NRDY interrupt of a pipe is detected.

When this module detects the NRDY interrupt of a pipe for which the software sets the corresponding bit in this register to 1, this module sets the PIPENRDY bit of the pipe in NRDYSTS and also sets the NRDY bit in INTSTS0 and generates an NRDY interrupt.

When one or more PIPENRDY bits in NRDYSTS are 1 and the software changes the corresponding interrupt enable bit(s) in this register from 0 to 1, this module generates an NRDY interrupt.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PIPEF NRDYE	PIPEE NRDYE	PIPED NRDYE	PIPEC NRDYE	PIPEB NRDYE	PIPEA NRDYE	PIPE9 NRDYE	PIPE8 NRDYE	PIPE7 NRDYE	PIPE6 NRDYE	PIPE5 NRDYE	PIPE4 NRDYE	PIPE3 NRDYE	PIPE2 NRDYE	PIPE1 NRDYE	PIPE0 NRDYE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	PIPEF NRDYE	0	R/W	Pipe F NRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
14	PIPEE NRDYE	0	R/W	Pipe E NRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
13	PIPED NRDYE	0	R/W	Pipe D NRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
12	PIPEC NRDYE	0	R/W	Pipe C NRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
11	PIPEB NRDYE	0	R/W	Pipe B NRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
10	PIPEA NRDYE	0	R/W	Pipe A NRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
9	PIPE9 NRDYE	0	R/W	Pipe 9 NRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
8	PIPE8 NRDYE	0	R/W	Pipe 8 NRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.

Bit	Bit Name	Initial Value	R/W	Description
7	PIPE7 NRDYE	0	R/W	Pipe 7 NRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
6	PIPE6 NRDYE	0	R/W	Pipe 6 NRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
5	PIPE5 NRDYE	0	R/W	Pipe 5 NRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
4	PIPE4 NRDYE	0	R/W	Pipe 4 NRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
3	PIPE3 NRDYE	0	R/W	Pipe 3 NRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
2	PIPE2 NRDYE	0	R/W	Pipe 2 NRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
1	PIPE1 NRDYE	0	R/W	Pipe 1 NRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
0	PIPE0 NRDYE	0	R/W	Pipe 0 NRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.

**52.2.12 BEMP Interrupt Enable Register (BEMPENB)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

BEMPENB enables or disables the BEMP bit to be set to 1 when the BEMP interrupt of a pipe is detected.

When this module detects the BEMP interrupt of a pipe for which the software sets the corresponding bit in this register to 1, this module sets the PIPEBEMP bit of the pipe in BEMPSTS and the BEMP bit in INTSTS0 and generates the BEMP interrupt.

When one or more PIPEBEMP bits in BEMPSTS are 1 and the software changes the corresponding interrupt enable bit(s) in this register from 0 to 1, this module generates the BEMP interrupt.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PIPEF BEMPE	PIPEE BEMPE	PIPED BEMPE	PIPEC BEMPE	PIPEB BEMPE	PIPEA BEMPE	PIPE9 BEMPE	PIPE8 BEMPE	PIPE7 BEMPE	PIPE6 BEMPE	PIPE5 BEMPE	PIPE4 BEMPE	PIPE3 BEMPE	PIPE2 BEMPE	PIPE1 BEMPE	PIPE0 BEMPE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	PIPEF BEMPE	0	R/W	Pipe F BEMP Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
14	PIPEE BEMPE	0	R/W	Pipe E BEMP Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
13	PIPED BEMPE	0	R/W	Pipe D BEMP Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
12	PIPEC BEMPE	0	R/W	Pipe C BEMP Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
11	PIPEB BEMPE	0	R/W	Pipe B BEMP Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
10	PIPEA BEMPE	0	R/W	Pipe A BEMP Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
9	PIPE9 BEMPE	0	R/W	Pipe 9 BEMP Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
8	PIPE8 BEMPE	0	R/W	Pipe 8 BEMP Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.

Bit	Bit Name	Initial Value	R/W	Description
7	PIPE7 BEMPE	0	R/W	Pipe 7 BEMP Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
6	PIPE6 BEMPE	0	R/W	Pipe 6 BEMP Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
5	PIPE5 BEMPE	0	R/W	Pipe 5 BEMP Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
4	PIPE4 BEMPE	0	R/W	Pipe 4 BEMP Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
3	PIPE3 BEMPE	0	R/W	Pipe 3 BEMP Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
2	PIPE2 BEMPE	0	R/W	Pipe 2 BEMP Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
1	PIPE1 BEMPE	0	R/W	Pipe 1 BEMP Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
0	PIPE0 BEMPE	0	R/W	Pipe 0 BEMP Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.

### 52.2.13 SOF Output Configuration Register (SOFCFG)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

SOFCFG specifies an effective period of transactions, the BRDY interrupt status clear timing, and others.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	BRDY M	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R/W	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15 to 7	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
6	BRDYM	0	R/W	Status Clear Timing of Each Pipe BRDY Interrupt Specifies the timing to clear the BRDY interrupt status of each pipe. 0: The software clears the status. 1: This module clears the status by reading or writing the FIFO buffer.
5 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

### 52.2.14 Interrupt Status Register 0 (INTSTS0)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

INTSTS0 can know the interrupt generation by referring to the register when the function controller is selected.

Please permit interrupt by the status change that each bit of this register shows only when you select the function.

This register is initialized by a power-on reset. The DVSQ2 to DVSQ0 bits are also initialized by a USB bus reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VBINT	RESM	SOFR	DVST	CTRTR	BEMP	NRDY	BRDY	VBSTS	DVSQ[2:0]			VALID	CTSQ[2:0]		
Initial value:	0	0	0	0/1	0	0	0	0	0/1	0	0	0/1	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R/W	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15	VBINT	0	R/W*6	<p>VBUS_0 and VBUSIN_0 Interrupt Status*4*5</p> <p>0: No VBUS_0 and VBUSIN_0 interrupt is generated. 1: A VBUS_0 and VBUSIN_0 interrupt is generated.</p> <p>This bit indicates 1 when this module detects a change in the VBUS_0 and VBUSIN_0 pin input level (high to low or low to high level). This module indicates the VBUS_0 and VBUSIN_0 pin input value using the VBSTS bit. When a VBINT interrupt occurs, read the VBSTS bit several times by the software and confirm that the read value is equal each time to eliminate chattering.</p>
14	RESM	0	R/W*6	<p>Resume Interrupt Status*4*5</p> <p>0: No resume interrupt is generated. 1: A resume interrupt is generated.</p> <p>This bit indicates 1 when this module detects a falling of the DP_0 pin level in the suspended state (DVSQ = 1XX) with the function controller function selected.</p>
13	SOFR	0	R/W*6	<p>Frame Number Update Interrupt Status*4</p> <p>0: No SOF interrupt is generated. 1: An SOF interrupt is generated.</p> <p>This module indicates SOFR = 1 at the frame number update timing (This interrupt is detected every millisecond).</p> <p>Even when an SOF packet from the USB host is corrupted, this module detects an SOFR interrupt using the internal interpolation.</p>
12	DVST	0/1*1	R/W*6	<p>Device State Transition Interrupt Status*4</p> <p>0: No device state transition interrupt is generated. 1: A device state transition interrupt is generated.</p> <p>When this module detects a change in device state, this module updates the DVSQ value and set this bit to 1.</p> <p>When this interrupt occurred, clear the status before this module detects the next device state transition.</p>

Bit	Bit Name	Initial Value	R/W	Description
11	CTRT	0	R/W*6	<p>Control Transfer Stage Transition Interrupt Status*4</p> <p>0: No control transfer stage transition interrupt is generated. 1: A control transfer stage transition interrupt is generated.</p> <p>When this module detects a control transfer stage transition, this module updates the CTSQ value and set this bit to 1.</p> <p>When this interrupt occurred, clear the status before this module detects the next stage transition in control transfers.</p>
10	BEMP	0	R	<p>Buffer Empty Interrupt Status</p> <p>0: No BEMP interrupt is generated. 1: A BEMP interrupt is generated.</p> <p>This module indicates BEMP = 1 when at least one of the PIPEBEMP bits in BEMPSTS corresponding to the pipes for which 1 is set in the PIPEBEMPE bits in BEMPENB is set to 1 (when this module detects a BEMP interrupt of one or more pipes for which BEMP interrupts are enabled by the software).</p> <p>For PIPEBEMP status assertion conditions, see section 52.3.2 (3), BEMP Interrupt.</p> <p>When the software writes 0 to all PIPEBEMP bits corresponding to the pipes for which interrupts are enabled by the PIPEBEMPE bits, this module clears this bit to 0.</p> <p>This bit cannot be cleared to 0 by writing 0 by the software.</p>
9	NRDY	0	R	<p>Buffer Not Ready Interrupt Status</p> <p>0: No NRDY interrupt is generated. 1: An NRDY interrupt is generated.</p> <p>This module indicates NRDY = 1 when at least one of the PIPENRDY bits in NRDYSTS corresponding to the pipes for which 1 is set in the PIPENRDYE bits in NRDYENB is set to 1 (when this module detects an NRDY interrupt of one or more pipes for which NRDY interrupts are enabled by the software).</p> <p>For PIPENRDY status assertion conditions, see section 52.3.2 (2), NRDY Interrupt.</p> <p>When the software writes 0 to all PIPENRDY bits corresponding to the pipes for which interrupts are enabled by the PIPENRDYE bits, this module clears this bit to 0.</p> <p>This bit cannot be cleared to 0 by writing 0 by the software.</p>
8	BRDY	0	R	<p>Buffer Ready Interrupt Status</p> <p>Indicates the BRDY interrupt status.</p> <p>0: No BRDY interrupt is generated. 1: A BRDY interrupt is generated.</p> <p>This module indicates BRDY = 1 when at least one of the PIPEBRDY bits in BRDYSTS corresponding to the pipes for which 1 is set in the PIPEBRDYE bits in BRDYENB is set to 1 (when this module detects a BRDY interrupt of one or more pipes for which BRDY interrupts are enabled by the software).</p> <p>For PIPEBRDY status assertion conditions, see section 52.3.2 (1), BRDY Interrupt.</p> <p>When the software writes 0 to all PIPEBRDY bits corresponding to the pipes for which interrupts are enabled by the PIPEBRDYE bits, this module clears this bit to 0.</p> <p>This bit cannot be cleared to 0 by writing 0 by the software.</p>



Bit	Bit Name	Initial Value	R/W	Description
7	VBSTS	0/1* <sup>3</sup>	R	VBUS Input Status 0: The VBUS pin is low level. 1: The VBUS pin is high level.
6 to 4	DVSQ[2:0]	000/001* <sup>2</sup>	R	Device State 000: Powered state 001: Default state 010: Address state 011: Configuration state 1xx: Suspended state
3	VALID	0	R/W* <sup>6</sup>	USB Request Receive 0: Not detected 1: A setup packet is received.
2 to 0	CTSQ[2:0]	000	R	Control Transfer Stage 000: Idle stage or setup stage 001: Control read data stage 010: Control read status stage 011: Control write data stage 100: Control write status stage 101: Control write (NoData) status stage 110: Control transfer sequence error 111: Setting prohibited

- Notes:
1. The initial value is B'0 after a power-on reset, and B'1 after a USB bus reset.
  2. The initial value is B'000 after a power-on reset, and B'001 after a USB bus reset.
  3. The initial value is 1 when the VBUS pin is high level, and is 0 when the VBUS pin is low level.
  4. To clear the VBINT, RESM, SOFR, DVST, or CTRT bit, write 0 only to bits to be cleared and write 1 to the other bits. Do not write 0 to status bits that indicate 0.
  5. Only writing 0 is enabled.

**52.2.15 BRDY Interrupt Status Register (BRDYSTS)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

BRDYSTS indicates the BRDY interrupt status of each pipe.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PIPEF BRDY	PIPEE BRDY	PIPED BRDY	PIPEC BRDY	PIPEB BRDY	PIPEA BRDY	PIPE9 BRDY	PIPE8 BRDY	PIPE7 BRDY	PIPE6 BRDY	PIPE5 BRDY	PIPE4 BRDY	PIPE3 BRDY	PIPE2 BRDY	PIPE1 BRDY	PIPE0 BRDY
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	PIPEFBRDY	0	R/W*1	Pipe F BRDY Interrupt Status*2 0: No interrupt is generated. 1: An interrupt is generated.
14	PIPEEBRDY	0	R/W*1	Pipe E BRDY Interrupt Status*2 0: No interrupt is generated. 1: An interrupt is generated.
13	PIPEDBRDY	0	R/W*1	Pipe D BRDY Interrupt Status*2 0: No interrupt is generated. 1: An interrupt is generated.
12	PIPECBRDY	0	R/W*1	Pipe C BRDY Interrupt Status*2 0: No interrupt is generated. 1: An interrupt is generated.
11	PIPEBBDY	0	R/W*1	Pipe B BRDY Interrupt Status*2 0: No interrupt is generated. 1: An interrupt is generated.
10	PIPEABRDY	0	R/W*1	Pipe A BRDY Interrupt Status*2 0: No interrupt is generated. 1: An interrupt is generated.
9	PIPE9BRDY	0	R/W*1	Pipe 9 BRDY Interrupt Status*2 0: No interrupt is generated. 1: An interrupt is generated.
8	PIPE8BRDY	0	R/W*1	Pipe 8 BRDY Interrupt Status*2 0: No interrupt is generated. 1: An interrupt is generated.
7	PIPE7BRDY	0	R/W*1	Pipe 7 BRDY Interrupt Status*2 0: No interrupt is generated. 1: An interrupt is generated.
6	PIPE6BRDY	0	R/W*1	Pipe 6 BRDY Interrupt Status*2 0: No interrupt is generated. 1: An interrupt is generated.

Bit	Bit Name	Initial Value	R/W	Description
5	PIPE5BRDY	0	R/W*1	Pipe 5 BRDY Interrupt Status*2 0: No interrupt is generated. 1: An interrupt is generated.
4	PIPE4BRDY	0	R/W*1	Pipe 4 BRDY Interrupt Status*2 0: No interrupt is generated. 1: An interrupt is generated.
3	PIPE3BRDY	0	R/W*1	Pipe 3 BRDY Interrupt Status*2 0: No interrupt is generated. 1: An interrupt is generated.
2	PIPE2BRDY	0	R/W*1	Pipe 2 BRDY Interrupt Status*2 0: No interrupt is generated. 1: An interrupt is generated.
1	PIPE1BRDY	0	R/W*1	Pipe 1 BRDY Interrupt Status*2 0: No interrupt is generated. 1: An interrupt is generated.
0	PIPE0BRDY	0	R/W*1	Pipe 0 BRDY Interrupt Status*2 0: No interrupt is generated. 1: An interrupt is generated.

- Notes: 1. To clear the status of each bit in this register when BRDYM is 0, write 0 only to bits to be cleared and write 1 to the other bits.
2. When BRDYM is 0, be sure to clear this interrupt before making an access to the FIFO.

### 52.2.16 NRDY Interrupt Status Register (NRDYSTS)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

NRDYSTS indicates the NRDY interrupt status of each pipe.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PIPEF NRDY	PIPEE NRDY	PIPED NRDY	PIPEC NRDY	PIPEB NRDY	PIPEA NRDY	PIPE9 NRDY	PIPE8 NRDY	PIPE7 NRDY	PIPE6 NRDY	PIPE5 NRDY	PIPE4 NRDY	PIPE3 NRDY	PIPE2 NRDY	PIPE1 NRDY	PIPE0 NRDY
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	PIPEFNDRDY	0	R/W*	Pipe F NRDY Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
14	PIPEENRDY	0	R/W*	Pipe E NRDY Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
13	PIPEDNRDY	0	R/W*	Pipe D NRDY Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
12	PIPECNRDY	0	R/W*	Pipe C NRDY Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
11	PIPEBNRDY	0	R/W*	Pipe B NRDY Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
10	PIPEANRDY	0	R/W*	Pipe A NRDY Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
9	PIPE9NRDY	0	R/W*	Pipe 9 NRDY Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
8	PIPE8NRDY	0	R/W*	Pipe 8 NRDY Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
7	PIPE7NRDY	0	R/W*	Pipe 7 NRDY Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
6	PIPE6NRDY	0	R/W*	Pipe 6 NRDY Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.

Bit	Bit Name	Initial Value	R/W	Description
5	PIPE5NRDY	0	R/W*	Pipe 5 NRDY Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
4	PIPE4NRDY	0	R/W*	Pipe 4 NRDY Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
3	PIPE3NRDY	0	R/W*	Pipe 3 NRDY Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
2	PIPE2NRDY	0	R/W*	Pipe 2 NRDY Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
1	PIPE1NRDY	0	R/W*	Pipe 1 NRDY Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
0	PIPE0NRDY	0	R/W*	Pipe 0 NRDY Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.

Note: \* To clear the status of each bit in this register, write 0 only to bits to be cleared and write 1 to the other bits.

### 52.2.17 BEMP Interrupt Status Register (BEMPSTS)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

BEMPSTS indicates the BEMP interrupt status of each pipe.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PIPEF BEMP	PIPEE BEMP	PIPED BEMP	PIPEC BEMP	PIPEB BEMP	PIPEA BEMP	PIPE9 BEMP	PIPE8 BEMP	PIPE7 BEMP	PIPE6 BEMP	PIPE5 BEMP	PIPE4 BEMP	PIPE3 BEMP	PIPE2 BEMP	PIPE1 BEMP	PIPE0 BEMP
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	PIPEFBEMP	0	R/W*	Pipe F BEMP Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
14	PIPEEBEMP	0	R/W*	Pipe E BEMP Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
13	PIPEDBEMP	0	R/W*	Pipe D BEMP Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
12	PIPECBEMP	0	R/W*	Pipe C BEMP Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
11	PIPEBBEMP	0	R/W*	Pipe B BEMP Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
10	PIPEABEMP	0	R/W*	Pipe A BEMP Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
9	PIPE9BEMP	0	R/W*	Pipe 9 BEMP Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
8	PIPE8BEMP	0	R/W*	Pipe 8 BEMP Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
7	PIPE7BEMP	0	R/W*	Pipe 7 BEMP Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
6	PIPE6BEMP	0	R/W*	Pipe 6 BEMP Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.

Bit	Bit Name	Initial Value	R/W	Description
5	PIPE5BEMP	0	R/W*	Pipe 5 BEMP Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
4	PIPE4BEMP	0	R/W*	Pipe 4 BEMP Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
3	PIPE3BEMP	0	R/W*	Pipe 3 BEMP Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
2	PIPE2BEMP	0	R/W*	Pipe 2 BEMP Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
1	PIPE1BEMP	0	R/W*	Pipe 1 BEMP Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
0	PIPE0BEMP	0	R/W*	Pipe 0 BEMP Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.

Note: \* To clear the status of each bit in this register, write 0 only to bits to be cleared and write 1 to the other bits.

### 52.2.18 Frame Number Register (FRMNUM)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

FRMNUM indicates the sources of isochronous errors and a frame number.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OVRN	CRCE	—	—	—	FRNM[10:0]										
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15	OVRN	0	R/W*	<p>Overrun/Underrun Detect Status</p> <p>Indicates whether an overrun or underrun error is detected or not in a pipe that is performing isochronous transfer.</p> <p>0: No error is detected.</p> <p>1: An error is detected.</p> <p>Writing 0 to this bit by the software clears this bit to 0. At this time, write 1 to the other bits in this register.</p> <p>This module indicates OVRN =1 in any of the following cases.</p> <p>When the IN token is received when transmit data write to the FIFO buffer is not completed in a transmit direction pipe of isochronous transfer type</p> <p>When the OUT token is received with no side of the FIFO buffer empty in a receive direction pipe of isochronous transfer type</p>
14	CRCE	0	R/W*	<p>Receive Data Error</p> <p>Indicates whether a CRC error or bit stuffing error is detected or not in a pipe that is performing isochronous transfer.</p> <p>0: No error is detected.</p> <p>1: An error is detected.</p> <p>Writing 0 to this bit by the software clears this bit to 0. At this time, write 1 to the other bits in this register.</p> <p>When a CRC error is detected, this module does not generate an internal NRDY interrupt request.</p>
13 to 11	—	All 0	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>
10 to 0	FRNM [10:0]	H'000	R	<p>Frame Number</p> <p>This module modifies this bit when an SOF is received and indicates the latest frame number.</p> <p>Read these bits twice and confirm that the read value is equal each time.</p>

Note: \* Only writing 0 is enabled.



**52.2.19  $\mu$  Frame Number Register (UFRMNUM)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

UFRMNUM indicates a  $\mu$  frame number.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	UFRNM[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

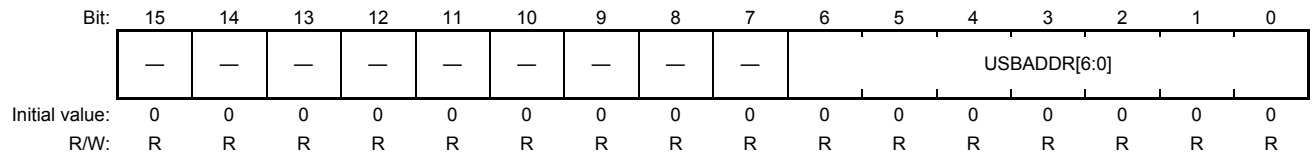
Bit	Bit Name	Initial Value	R/W	Description
15 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2 to 0	UFRNM[2:0]	000	R	$\mu$ Frame Indicate a $\mu$ frame number. In high-speed operating mode, these bits indicate a $\mu$ frame number. In other operating modes, these bits indicate B'000. Read these bits twice and confirm that the read value is equal each time.

**52.2.20 USB Address Register (USBADDR)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

USBADDR indicates a USB address.

This register is initialized by a power-on reset or USB bus reset.



Bit	Bit Name	Initial Value	R/W	Description
15 to 7	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
6 to 0	USBADDR[6:0]	H'00	R	USB Address Indicate the USB address allocated by the host when the SET_ADDRESS request is successfully processed. When this module detects a USB reset, these bits indicate H'00.

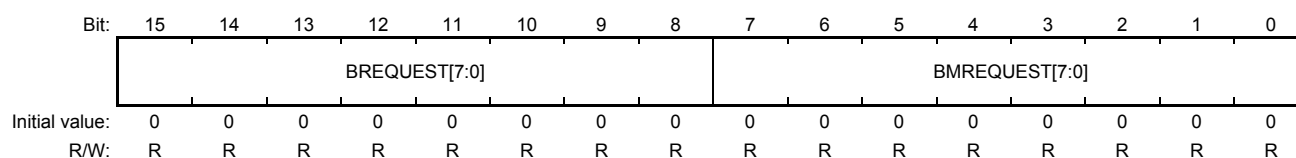
### 52.2.21 USB Request Type Register (USBREQ)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

USBREQ stores the setup request for control transfers.

USBREQ stores the values of received bRequest and bmRequestType.

This register is initialized by a power-on reset or USB bus reset.



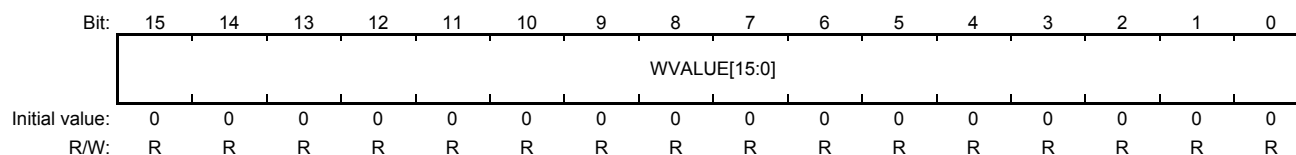
Bit	Bit Name	Initial Value	R/W	Description
15 to 8	BREQUEST [7:0]	H'00	R	Request Store the value of USB request bRequest. Indicate the USB request data received in the SETUP transaction. These bits cannot be modified.
7 to 0	BMREQUEST TYPE[7:0]	H'00	R	Request Type Store the value of USB request bmRequestType. Indicate the USB request data received in the SETUP transaction. These bits cannot be modified.

### 52.2.22 USB Request Value Register (USBVAL)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

USBVAL stores the value of received wValue.

This register is initialized by a power-on reset or USB bus reset.



Bit	Bit Name	Initial Value	R/W	Description
15 to 0	WVALUE [15:0]	H'0000	R	Value Store the value of USB request wValue. Indicate the value of USB request wValue received in the SETUP transaction. These bits cannot be modified.

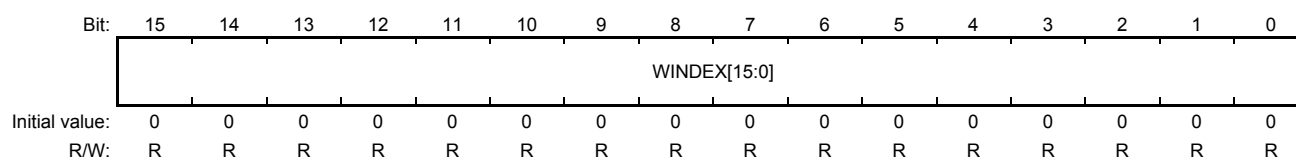
### 52.2.23 USB Request Index Register (USBINDX)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

USBINDX stores the setup request for control transfers.

USBINDX stores the value of received wIndex.

This register is initialized by a power-on reset or USB bus reset.



Bit	Bit Name	Initial Value	R/W	Description
15 to 0	WINDEX [15:0]	H'0000	R	Index Store the value of USB request wIndex. Indicate the value of USB request wIndex received in the SETUP transaction. These bits cannot be modified.

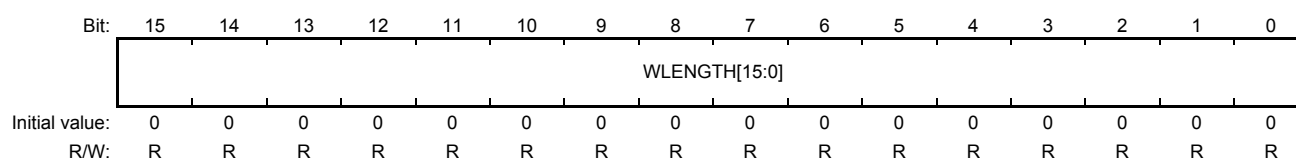
### 52.2.24 USB Request Length Register (USBLENG)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

USBLENG stores the setup request of control transfers.

USBLENG stores the value of received wLength.

This register is initialized by a power-on reset or USB bus reset.



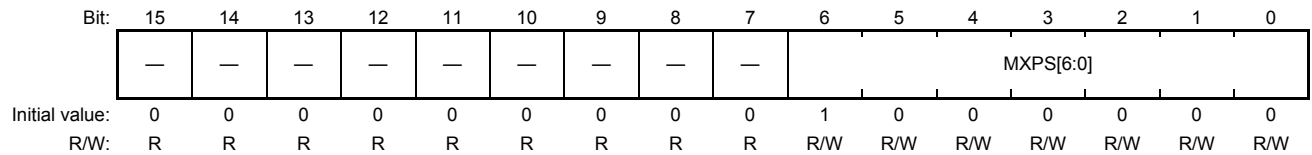
Bit	Bit Name	Initial Value	R/W	Description
15 to 0	WLENGTH [15:0]	H'0000	R	Length Store the value of USB request wLength. Indicate the value of USB request wLength received in the SETUP transaction. These bits cannot be modified.

**52.2.25 DCP Maximum Packet Size Register (DCPMAXP)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

DCPMAXP specifies the maximum packet size of the DCP.

This register is initialized by a power-on reset.



Bit	Bit Name	Initial Value	R/W	Description
15 to 7	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
6 to 0	MXPS [6:0]	H'40	R/W	Maximum Packet Size Set the payload of DCP data (maximum DCP packet size) in these bits. The initial value of these bits is H'40 (64 bytes). Set a value in the MXPS bits based on the USB Specification. Set the MXPS bits when PID = NAK, and the CURPIPE bits are not set. When setting these bits to 1 after changing the PID bits for the pipe from BUF to NAK, check that PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK. Do not write the FIFO buffer when the MXPS bits are 0 or set the PID bits to BUF.

### 52.2.26 DCP Control Register (DCPCTR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

DCPCTR is used to monitor the buffer memory status, change/check the data PID sequence bit, and set the response PID for a DCP.

This register is initialized by a power-on reset. The PID2 to PID0 bits in CCPL are also initialized by a USB bus reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BSTS	—	—	—	—	—	—	SQCLR	SQSET	SQMON	PBUSY	—	—	CCPL	PID[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R/W	R	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	BSTS	0	R	<p>Buffer Status</p> <p>Indicates whether the DCP FIFO buffer is accessible or not.</p> <p>0: The buffer is not accessible.</p> <p>1: The buffer is accessible.</p> <p>This bit indicates as follows depending on the ISEL value.</p> <p>When ISEL = 0, this bit indicates whether the buffer is ready to read receive data.</p> <p>When ISEL = 1, this bit indicates whether the buffer is ready to write transmit data.</p>
14 to 9	—	All 0	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>
8	SQCLR	0	R/W*	<p>Toggle Bit Clear</p> <p>The expected value of the sequence toggle bit for the next transaction in DCP transfer can be set in DATA0.</p> <p>0: Invalid</p> <p>1: The expected value is set in DATA0.</p> <p>This bit always indicates 0.</p> <p>Do not set the SQCLR and SQSET bits to 1 at the same time.</p> <p>Set this bit to 1 when PID = NAK, and the CURPIPE bits are not set.</p> <p>When setting this bit to 1 after changing the PID bits for the pipe from BUF to NAK, check that PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK.</p>

Bit	Bit Name	Initial Value	R/W	Description
7	SQSET	0	R/W*	<p>Toggle Bit Set</p> <p>The expected value of the sequence toggle bit for the next transaction in DCP transfer can be set in DATA1.</p> <p>0: Invalid</p> <p>1: The expected value is set in DATA1.</p> <p>Do not set the SQCLR and SQSET bits to 1 at the same time.</p> <p>Set this bit to 1 when PID = NAK, and the CURPIPE bits are not set.</p> <p>When setting this bit to 1 after changing the PID bits for the pipe from BUF to NAK, check that PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK.</p>
6	SQMON	1	R	<p>Sequence Toggle Bit Monitor</p> <p>Indicates the expected value of the sequence toggle bit for the next transaction in DCP transfer.</p> <p>0: DATA0</p> <p>1: DATA1</p> <p>When the transaction is successfully completed, this module toggles this bit. However, when a DATA-PID mismatch occurs in the receive direction transfer, this bit is not toggled.</p> <p>When the function controller function is selected, this module sets this bit to 1 (sets the expected value in DATA1) when the setup packet is successfully received.</p> <p>When the function controller function is selected, this module does not read this bit in IN transactions or OUT transactions in the status stage.</p>
5	PBUSY	0	R	<p>Pipe Busy</p> <p>Indicates whether the DCP communication state is shifted to the NAK state or not when the DCP changed the PID bits from BUF to NAK.</p> <p>0: Transition to the NAC state is not completed.</p> <p>1: Transition to the NAC state is completed.</p> <p>When this module starts the USB transaction for the corresponding pipe, this module sets this bit to 1. This module clears this bit to 0 upon completion of each transaction.</p> <p>After the software sets PID = NAK, read this bit to check whether changing the pipe setting is enabled or not.</p>
4, 3	—	All 0	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>

Bit	Bit Name	Initial Value	R/W	Description
2	CCPL	0	R/W*	<p>Control Transfer End Enable</p> <p>0: Invalid</p> <p>1: The control transfer end is enabled.</p> <p>When the software sets this bit to 1 while the corresponding PID bits are set to BUF, this module finishes the control transfer stage.</p> <p>That is, this module sends an ACK handshake in response to OUT transactions from the USB host in the control read transfer, and sends a Zero-Length packet in response to IN transactions from the USB host in control write and no-data control transfers. However, a SET_ADDRESS request is detected, this module automatically sends responses from the SETUP stage until the end of the status stage irrespective of the setting of this bit.</p> <p>When this module receives the next setup packet, this module clears this bit to 0.</p> <p>When VALID = 1, the software cannot write 1 to this bit.</p>
1, 0	PID[1:0]	00	R/W	<p>Response PID</p> <p>Control responses of this module in control transfers.</p> <p>00: NAK response</p> <p>01: BUF response (depending on buffer state)</p> <p>10: STALL response</p> <p>11: STALL response</p> <p>This module modifies these bits in the following cases.</p> <p>This module changes these bits to NAK upon receiving a SETUP packet. At this time, this module indicates VALID = 1. The software cannot modify these bits until the software sets VALID = 0.</p> <p>When this module receives data with a size exceeding the MaxPacketSize value while these bits are set to BUF by the software, this module indicates PID = STALL (11).</p> <p>When this module detects a control transfer sequence error, this module indicates PID = STALL (1x).</p> <p>When this module detects a USB bus reset, this module indicates PID = NAK.</p> <p>This module does not read the value of these bits during the SET_ADDRESS request processing (auto processing).</p>

Notes: \* These bits are always read as 0. Only writing 1 is enabled.



**52.2.27 Pipe Window Select Register (PIPESEL)**

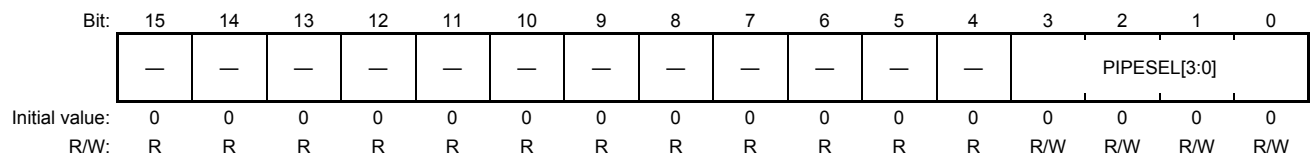
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Make settings for pipes 1 to F using PIPESEL, PIPECFG, PIPEBUF, PIPEMAXP, PIPEPERI, PIPEnCTR, PIPEnTRE, and PIPEnTRN.

Specify a pipe to be used with PIPESEL, and then make function settings for each pipe in PIPECFG, PIPEBUF, PIPEMAXP, and PIPEPERI. The PIPEnCTR, PIPEnTRE, and PIPEnTRN registers can be set independently from pipe selection using PIPESEL.

Not only the selected pipe but also the corresponding bits in registers for all pipes are initialized by a power-on reset or USB bus reset.

This register is initialized by a power-on reset.



Bit	Bit Name	Initial Value	R/W	Description
15 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3 to 0	PIPESEL [3:0]	0000	R/W	Pipe Window Select Specify a pipe number corresponding to PIPECFG, PIPEBUF, PIPEMAXP, and PIPEPERI to be read or written. 0000: No pipe is selected. 0001: Pipe 1 0010: Pipe 2 0011: Pipe 3 0100: Pipe 4 0101: Pipe 5 0110: Pipe 6 0111: Pipe 7 1000: Pipe 8 1001: Pipe 9 1010: Pipe A 1011: Pipe B 1100: Pipe C 1101: Pipe D 1110: Pipe E 1111: Pipe F PIPECFG, PIPEBUF, PIPEMAXP, and PIPEPERI corresponding to the pipe number specified by these bits can be read and written. When these bits are set to B'0000, all bits in PIPECFG, PIPEBUF, PIPEMAXP, and PIPEPERI are read as 0 and cannot be modified.

### 52.2.28 Pipe Configuration Register (PIPECFG)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

PIPECFG specifies the transfer type, buffer memory access direction, and endpoint number for pipes 1 to F, selects continuous transfer mode or discontinuous transfer mode, and single buffer or double buffer, and also specifies whether to disable the operation of each pipe when data transfer finishes.

This register is initialized by a power-on reset. The TYPE1 and TYPE0 bits are also initialized by a USB bus reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TYPE[1:0]		—	—	—	BFRE	DBLB	CNTM D	SHTNA K	—	—	DIR	EPNUM[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R	R	R	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15, 14	TYPE[1:0]	00	R/W	<p>Transfer Type</p> <p>Select the transfer type of the pipe specified by the PIPESEL bits (selected pipe).</p> <p>Pipes 1 and 2</p> <p>00: No pipe is used.</p> <p>01: Bulk transfer</p> <p>10: Setting prohibited</p> <p>11: Isochronous transfer</p> <p>Pipes 3 to 5, B to F</p> <p>00: No pipe is used.</p> <p>01: Bulk transfer</p> <p>10: Setting prohibited</p> <p>11: Setting prohibited</p> <p>Pipes 6 to 8</p> <p>00: No pipe is used.</p> <p>01: Setting prohibited</p> <p>10: Interrupt transfer</p> <p>11: Setting prohibited</p> <p>Pipes 9 to A</p> <p>00: No pipe is used.</p> <p>01: Bulk transfer</p> <p>10: Interrupt transfer</p> <p>11: Setting prohibited</p> <p>Before setting the selected pipe for PID = BUF (before starting USB communication using the selected pipe), be sure to set these bits to a value other than B'00.</p> <p>Modify these bits when the PID bits of the selected pipe are set to NAK. When changing the setting of these bits after changing the PID bits for the selected pipe from BUF to NAK, check that and PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK.</p>

Bit	Bit Name	Initial Value	R/W	Description
13 to 11	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
10	BFRE	0	R/W	<p>BRDY Interrupt Operation</p> <p>Specifies the BRDY interrupt output timing from this module to the CPU for the selected pipe.</p> <p>0: At a BRDY interrupt timing during data transmission or reception 1: At a BRDY interrupt timing after reading data</p> <p>When this bit is set to 1 by the software and the selected pipe is used in the receive direction, this module detects the transfer end and outputs a BRDY interrupt when the packet is completely read.</p> <p>When a BRDY interrupt occurs with this setting, the software must set BCLR = 1. Unless BCLR = 1 is set, the FIFO buffer allocated to the selected pipe does not enter the receive ready state.</p> <p>When this bit is set to 1 by the software and the selected pipe is used in the transmit direction, this module generates no BRDY interrupt.</p> <p>For details, see section 52.3.2 (1), BRDY Interrupt.</p> <p>Modify this bit when PID = NAK, and no pipe number is specified by the CURPIPE bits.</p> <p>Furthermore, when changing the setting of this bit after USB communication using the selected pipe, set the ACLRM bit to 1 and clear it to 0 continuously by the software to clear the FIFO buffer allocated to the selected pipe, in addition to the three register states above.</p> <p>When changing the setting of this bit after changing the PID bits for the selected pipe from BUF to NAK, check that PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK.</p>

Bit	Bit Name	Initial Value	R/W	Description
9	DBLB	0	R/W	<p>Double Buffer Mode</p> <p>Specifies a single buffer or double buffer for the FIFO buffer used in the selected pipe.</p> <p>0: Single buffer 1: Double buffer</p> <p>This bit is valid when pipes 1 to 5, 9 to F are selected.</p> <p>When this bit is set to 1 by the software, this module allocates the FIFO buffer size specified by the BUFSIZE bits in PIPEBUF to the selected pipe for two sides.</p> <p>Thus the size of the FIFO buffer that this module allocates to the selected pipe is as follows: (BUFSIZE + 1) × 64 × (DBLB + 1) [bytes]</p> <p>When this bit is set to 1 by the software and the selected pipe is used in the transmit direction, this module generates no BRDY interrupt.</p> <p>For details, see section 52.3.2 (1), BRDY Interrupt.</p> <p>Modify this bit when PID = NAK, and no pipe number is specified by the CURPIPE bits.</p> <p>Furthermore, when changing the setting of this bit after USB communication using the selected pipe, set the ACLRM bit to 1 and clear it to 0 continuously by the software to clear the FIFO buffer allocated to the selected pipe, in addition to the three register states above.</p> <p>When changing the setting of this bit after changing the PID bits for the selected pipe from BUF to NAK, check that PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK.</p>
8	CNTMD	0	R/W	<p>Continuous Transfer Mode</p> <p>Selects continuous transfer mode or discontinuous transfer mode to be used in communication for the selected pipe.</p> <p>0: Discontinuous transfer mode 1: Continuous transfer mode</p> <p>This bit is valid when pipes 1 to 5, 9 to F are selected by the PIPESEL bits and bulk transfer is selected (TYPE = 01).</p> <p>Modify this bit when PID = NAK, and no pipe number is specified by the CURPIPE bits.</p> <p>Furthermore, when changing the setting of this bit after USB communication using the selected pipe, set the ACLRM bit to 1 and clear it to 0 continuously by the software to clear the FIFO buffer allocated to the selected pipe, in addition to the three register states above.</p> <p>When changing the setting of this bit after changing the PID bits for the selected pipe from BUF to NAK, check that PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK.</p>

Bit	Bit Name	Initial Value	R/W	Description
7	SHTNAK	0	R/W	<p>Pipe Disable at the Time of Transfer End</p> <p>Specifies whether to change the setting of the PID bits to NAK at the end of transfer when the selected pipe is in the receive direction.</p> <p>0: The pipe is continued at the end of transfer. 1: The pipe is disabled at the end of transfer.</p> <p>This bit is valid when the selected pipe is either of pipes 1 to 5, 9 to F and is in the receive direction.</p> <p>When the software sets this bit to 1 for a receive direction pipe, this module changes the setting of the PID bits corresponding to the selected pipe to NAK for the selected pipe when this module determines the transfer end. When the following conditions are satisfied, this module determines the transfer end.</p> <p>When short packet data (including a Zero-Length packet) is correctly received.</p> <p>When the transaction counter is used and packets with a size of the transaction counter are correctly received.</p> <p>Modify this bit when PID = NAK.</p> <p>When changing the setting of this bit after changing the PID bits for the selected pipe from BUF to NAK, check that PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK.</p> <p>For transmit direction pipes, set this bit to 0.</p>
6, 5	—	All 0	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>
4	DIR	0	R/W	<p>Transfer Direction</p> <p>Selects the transfer direction of the selected pipe.</p> <p>0: Receive direction 1: Transmit direction</p> <p>When this bit is set to 0 by the software, this module uses the selected pipe in the receive direction. When this bit is set to 1, this module uses the selected pipe in the transmit direction.</p> <p>Modify this bit when PID = NAK, and no pipe number is specified by the CURPIPE bits.</p> <p>Furthermore, when changing the setting of this bit after USB communication using the selected pipe, set the ACLRM bit to 1 and clear it to 0 continuously by the software to clear the FIFO buffer allocated to the selected pipe, in addition to the three register states above.</p> <p>When changing the setting of this bit after changing the PID bits for the selected pipe from BUF to NAK, check that PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK.</p>

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Bit	Bit Name	Initial Value	R/W	Description
3 to 0	EPNUM [3:0]	0000	R/W	<p>Endpoint Number</p> <p>Specify the endpoint number of the selected pipe.</p> <p>The setting of B'0000 means an unused pipe.</p> <p>Modify these bits when PID = NAK.</p> <p>When changing the setting of these bits after changing the PID bits for the selected pipe from BUF to NAK, check that PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK.</p> <p>Set these bits so that the combination of the DIR setting and the EPNUM setting does not overlap the setting of other pipes (EPNUM = B'0000 is allowed in this case.)</p>

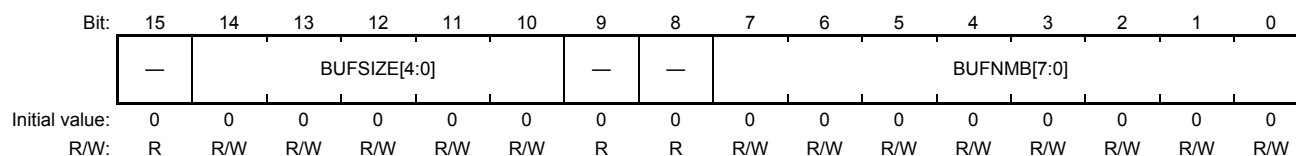
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### 52.2.29 Pipe Buffer Register (PIPEBUF)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

PIPEBUF specifies the buffer size and buffer number for pipes 1 to F.

This register is initialized by a power-on reset.



Bit	Bit Name	Initial Value	R/W	Description
15	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
14 to 10	BUFSIZE [4:0]	H'00	R/W	<p>Buffer Size</p> <p>Specify the buffer size of the pipe specified by the PIPESEL bits (selected pipe) in units of blocks. One block is 64 bytes.</p> <p>00000 (H'00): 64 bytes</p> <p>00001 (H'01): 128 bytes</p> <p>:</p> <p>11111 (H'1F): 2 Kbytes</p> <p>When DBLB = 1 is set by the software, this module allocates the FIFO buffer size specified by these bits to the selected pipe for two sides.</p> <p>Thus the size of the FIFO buffer that this module allocates to the selected pipe is as follows:</p> $(BUFSIZE + 1) \times 64 \times (DBLB + 1) \text{ [bytes]}$ <p>A value that can be set in these bits varies depending on pipes selected.</p> <p>For pipes 1 to 5, 9 to F: Set BUFSIZE to H'00 to H'1F.</p> <p>For pipes 6 to 8: Set BUFSIZE to H'00.</p> <p>When using the buffer with CNTMD = 1, set a value in multiples of MaxPacketSize in these bits.</p> <p>Modify these bits when PID = NAK, and no pipe number is specified by the CURPIPE bits.</p> <p>When changing the setting of this bit after changing the PID bits for the selected pipe from BUF to NAK, check that PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK.</p>
9, 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
7 to 0	BUFNMB [7:0]	H'00	R/W	<p>Buffer Number</p> <p>Specify the FIFO buffer number of the selected pipe with a value from H'04 to H'FF.</p> <p>When the selected pipe is either of pipes 1 to 5, 9 to F, these bits can be set to a value according to user systems. Set BUFNMB to H'06 to H'4F.</p> <p>BUFNMB = 0 to 3 are for DCP only.</p> <p>BUFNMB = 4 is for pipe 6 only.</p> <p>However, when pipe 6 is not used, this is available for other pipes.</p> <p>When pipe 6 is selected, these bits cannot be modified and this module automatically allocates BUFNMB = 4.</p> <p>BUFNMB = 5 is for pipe 7 only.</p> <p>However, when pipe 7 is not used, this is available for other pipes.</p> <p>When pipe 7 is selected, these bits cannot be modified and this module automatically allocates BUFNMB = 5.</p> <p>BUFNMB = 6 is for pipe 8 only.</p> <p>However, when pipe 8 is not used, this is available for other pipes.</p> <p>When pipe 8 is selected, these bits cannot be modified and this module automatically allocates BUFNMB = 6.</p> <p>Modify these bits when PID = NAK, and no pipe number is set in the CURPIPE bits.</p> <p>When changing the setting of these bits after changing the PID bits for the selected pipe from BUF to NAK, check that PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK.</p>

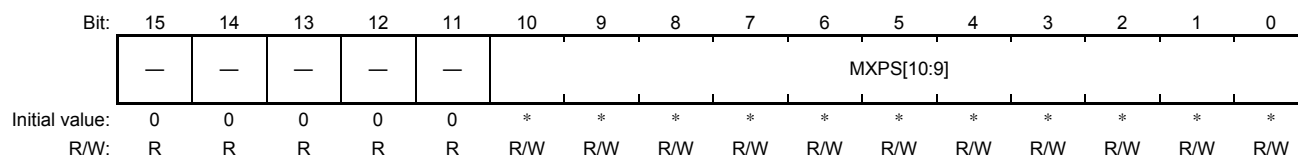


### 52.2.30 Pipe Maximum Packet Size Register (PIPEMAXP)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

PIPEMAXP specifies the maximum packet size for pipes 1 to F.

This register is initialized by a power-on reset.



Bit	Bit Name	Initial Value	R/W	Description
15 to 11	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
10 to 0	MXPS[10:0]	*	R/W	Maximum Packet Size Specify the payload of data (maximum packet size) of the selected pipe. The settable value range for each pipe is as follows: Pipes 1 and 2: 1 byte (H'001) to 1024 bytes (H'400) Pipes 3 to 5, 9 to F: 8 (H'008), 16 (H'010), 32 (H'020), 64 (H'040), or 512 bytes (H'200) (MXPS2 to MXPS0 bits are not provided.) Pipes 6 to 8: 1 byte (H'001) to 64 bytes (H'040) Set a value in the MXPS bits based on the USB Specification for each transfer type. To transmit an isochronous pipe in split transactions, set a value of 188 bytes or less in the MXPS bits. When changing the setting of this bit after changing the PID bits for the selected pipe from BUF to NAK, check that PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK. Do not write the FIFO buffer when the MXPS = 0 or set the PID bits to BUF.

Note: \* The initial value is H'000 (when no pipe is selected by the PIPESEL bits in PIPESEL) or H'040 (when a pipe is selected).

### 52.2.31 Pipe Cycle Control Register (PIPEPERI)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

PIPEPERI specifies whether to activate the buffer flush function or not at the time of an interval error during the isochronous IN transfer, and also specifies the interval error detection interval for pipes 1 to F.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	IFIS	—	—	—	—	—	—	—	—	—	IITV[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12	IFIS	0	R/W	<p>Isochronous IN Buffer Flush</p> <p>Specifies whether to flush the FIFO buffer when the pipe specified by the PIPESEL bits (selected pipe) is isochronous IN transfer type.</p> <p>0: The FIFO buffer is not flushed. 1: The FIFO buffer is flushed.</p> <p>Buffer flush is a function that this module automatically clears the FIFO buffer when this module does not receive IN-Token from the USB host in a (<math>\mu</math>) frame for each interval specified in the IITV bits when the function controller function is selected and the selected pipe is isochronous IN transfer type.</p> <p>When double buffer is selected (DBLB = 1), this module clears data of only the older side.</p> <p>The FIFO buffer is cleared when an SOF packet is received immediately after the (<math>\mu</math>) frame where IN-Token is to be received. Even if the SOF packet is corrupted, the FIFO buffer is cleared at the time when the SOF packet is to be received using the internal interpolation.</p> <p>When the selected pipe is not isochronous transfer type, set this bit to 0.</p>
11 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2 to 0	IITV[2:0]	000	R/W	<p>Interval Error Detection Interval</p> <p>Specify the interval error detection interval of the selected pipe with a value of 2's n-th power of the frame timing.</p> <p>Set these bits when PID = NAK, and no pipe number is specified by the CURPIPE bits.</p> <p>When changing the setting of these bits after changing the PID bits for the selected pipe from BUF to NAK, check that PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK.</p> <p>To change the setting of these bits after USB communication, set PID = NAK and then set ACLRM = 1 to initialize the interval timer.</p> <p>These bits are not provided for pipes 3 to F. Set B'000 in the position of these bits corresponding to pipes 3 to F.</p>

### 52.2.32 Pipe n Control Register (PIPEnCTR) (n = 1 to F)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

PIPEnCTR monitors the buffer memory status, changes/checks the data PID sequence bits, selects whether to use auto-response mode and buffer auto-clear mode, and specifies a response PID for pipes 1 to F. This register can be set independently of the pipe selection using PIPESEL.

This register is initialized by a power-on reset. The PID1 and PID0 bits are also initialized by a USB bus reset.

#### (1) PIPEnCTR (n = 1 to 5, 9 to F)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BSTS	INBUFM	—	—	—	ATREPM	ACLRM	SQCLR	SQSET	SQMON	PBUSY	—	—	—	PID[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W	R/W	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	BSTS	0	R	<b>Buffer Status</b> Indicates the FIFO buffer status of the pipe. 0: The buffer is not accessible from the CPU. 1: The buffer is accessible from the CPU. The meaning of this bit differs depending on the settings of the DIR, BFRE, and DCLRM bits as shown in Table 52.8.
14	INBUFM	0	R	<b>Transmit Buffer Monitor</b> Indicates the FIFO buffer status of the selected pipe in the transmit direction. 0: The buffer memory contains no transmittable data. 1: The buffer memory contains transmittable data. When transmit direction (DIR = 1) is set for the pipe, this module sets this bit to 1 when the software (or DMAC) finishes writing data to the FIFO buffer for at least one register set. When this module finishes sending all data on the register set (writing is completed) of the FIFO buffer, this bit indicates 0. In the case of a double buffer (DBLB = 1), when this module finishes sending all data on both register sets and the software (or DMAC) has not completed writing of data for one register set, this bit indicates 0. When receive direction (DIR = 0) is set for the selected pipe, this bit indicates the same value as the BSTS bit.
13 to 11	—	All 0	R	<b>Reserved</b> These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
10	ATREPM	0	R/W	<p><b>Auto-Response Mode</b></p> <p>Enables or disables auto-response for the selected pipe.</p> <p>0: Auto-response is disabled.</p> <p>1: Auto-response is enabled.</p> <p>When the transfer type of the selected pipe is set to bulk transfer, this bit can be set to 1.</p> <p>When this bit is 1, this module sends responses to tokens from the USB host as follows:</p> <p>(1) When the selected pipe is set for Bulk-IN transfer (TYPE = B'01 and DIR = 1)</p> <p>When ATREPM = 1 and PID = BUF, this module sends a Zero-Length packet in response to the IN-Token.</p> <p>Each time this module receives ACK from the USB host (flow of one transaction: receiving IN-Token -&gt; sending Zero Length packet -&gt; receiving ACK), this module updates the sequence toggle bit (DATA-PID) by toggling it.</p> <p>No BRDY interrupt or BEMP interrupt is generated.</p> <p>(2) When the selected pipe is set for Bulk-OUT transfer (TYPE = B'01 and DIR = 0)</p> <p>When ATREPM = 1 and PID = BUF, this module sends NAK in response to the OUT-Token (or PING-Token) and generates an NRDY interrupt.</p> <p>Modify this bit when PID = NAK.</p> <p>When setting this bit to 1 after changing the PID bits for the pipe from BUF to NAK, check that PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK.</p> <p>Be sure to set this bit to 1 for USB communication when the FIFO buffer is empty. Do not write data to the FIFO buffer during USB communication with this bit set to 1.</p> <p>When the selected pipe is set for isochronous transfer, be sure to set this bit to 0.</p>
9	ACLRM	0	R/W	<p><b>Buffer Auto-Clear Mode</b></p> <p>Enables or disables buffer auto-clear mode for the selected pipe.</p> <p>0: Buffer auto-clear mode is disabled.</p> <p>1: Buffer auto-clear mode is enabled. (All buffers are initialized.)</p> <p>To completely delete the data in the FIFO buffer allocated to the pipe, write 1 and then 0 continuously to the ACLRM bit.</p> <p>Table 52.9 shows data cleared by this module when this bit is set to 1 and then 0 and cases where such data is cleared.</p> <p>Modify this bit when PID = NAK.</p> <p>When setting this bit to 1 after changing the PID bits for the pipe from BUF to NAK, check that PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK.</p>

Bit	Bit Name	Initial Value	R/W	Description
8	SQCLR	0	R/W*	<p>Toggle Bit Clear</p> <p>Set this bit to 1 to clear the expected value (in DATA0) of the sequence toggle bit for the next transaction of the selected pipe.</p> <p>0: Invalid</p> <p>1: The expected value is cleared in DATA0.</p> <p>When the software sets this bit to 1, this module sets the expected value of the sequence toggle bit of the pipe in DATA0. This module always indicates SQCLR = 0.</p> <p>Set the SQCLR bit to 1 when PID = NAK.</p> <p>When setting this bit to 1 after changing the PID bits for the selected pipe from BUF to NAK, check that PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK.</p>
7	SQSET	0	R/W*	<p>Toggle Bit Set</p> <p>Set this bit to 1 to set the expected value of the sequence toggle bit for the next transaction of the selected pipe.</p> <p>0: Invalid</p> <p>1: The expected value is set in DATA1.</p> <p>When the software sets this bit to 1, this module sets the expected value of the sequence toggle bit of the pipe in DATA1. This module always indicates SQSET = 0.</p> <p>Set the SQSET bit to 1 when PID = NAK.</p> <p>When setting this bit to 1 after changing the PID bits for the pipe from BUF to NAK, check that PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK.</p>
6	SQMON	0	R	<p>Toggle Bit Check</p> <p>Indicates the expected value of the sequence toggle bit for the next transaction of the selected pipe.</p> <p>0: DATA0</p> <p>1: DATA1</p> <p>If the pipe is not the isochronous transfer type, when a transaction is successfully processed, this module toggles this bit. However, when a DATA-PID mismatch occurs in the receive direction transfer, this bit is not toggled.</p>
5	PBUSY	0	R	<p>Pipe Busy</p> <p>Indicates whether the pipe is currently used in the USB bus or not.</p> <p>0: The selected pipe is not used in the USB bus.</p> <p>1: The selected pipe is being used in the USB bus.</p> <p>When this module starts the USB transaction for the selected pipe, this module sets this bit to 1. This module clears this bit to 0 upon completion of each transaction.</p> <p>After the software sets PID = NAK, read this bit to see if changing the pipe setting is enabled or not.</p>
4 to 2	—	All 0	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>

Bit	Bit Name	Initial Value	R/W	Description
1, 0	PID[1:0]	00	R/W	<p>Response PID</p> <p>Specify a response used in the next transaction for the selected pipe.</p> <p>00: NAK response</p> <p>01: BUF response (depending on buffer state)</p> <p>10: STALL response</p> <p>11: STALL response</p> <p>These bits are set to NAK by default. To perform USB transfer with the selected pipe, change the setting of these bits to BUF. Table 52.10 shows the basic operation (with no error in packets) of this module in each setting of the PID bits.</p> <p>When changing these bits from BUF to NAK by the software while the pipe is in USB communication, write 00 (NAK) to these bits and then check PBUSY = 1 to confirm that the USB transfer of the pipe entered the NAK state. However, when this module changed these bits to NAK, the software does not have to check the PBUSY bit.</p> <p>This module modifies these bits in the following cases.</p> <ul style="list-style-type: none"> <li>When the pipe is in the receive direction and the software sets the SHTNAK bit of the selected pipe to 1, this module indicates PID = NAK when this module recognizes the transfer end.</li> <li>When this module receives data with a payload exceeding the MaxPacketSize value for the pipe, this module indicates PID = STALL (11).</li> <li>When this module detects a USB bus reset, this module indicates PID = NAK.</li> </ul> <p>Set these bits as follows:</p> <ul style="list-style-type: none"> <li>To change the state from NAK (00) to STALL, write B'10.</li> <li>To change the state from BUF (01) to STALL, write B'11.</li> <li>To change the state from STALL (11) to NAK, write B'10 then B'00.</li> <li>To change the state from STALL to BUF, set these bits to NAK and then to BUF.</li> </ul>

Notes: \* Only reading 0 and writing 1 are enabled.

**Table 52.8 Operations of BSTS Bit**

DIR Bit	BFRE Bit	DCLRM Bit	Meaning of BSTS Bit
0	0	0	Indicates 1 when the FIFO buffer becomes ready to read receive data from the buffer, and indicates 0 upon completion of the data read.
		1	Setting prohibited
	1	0	Indicates 1 when the FIFO buffer becomes ready to read receive data from the buffer, and indicates 0 when the software sets BCLR = 1 after the buffer data read.
		1	Indicates 1 when the FIFO buffer becomes ready to read receive data from the buffer, and indicates 0 upon completion of the data read.
1	0	0	Indicates 1 when the FIFO buffer becomes ready to write transmit data to the buffer, and indicates 0 upon completion of the data write.
		1	Setting prohibited
	1	0	Setting prohibited
		1	Setting prohibited

**Table 52.9 Data Cleared by This Module when ACLRM = 1**

No.	Data Cleared by the ACLRM Bit	Clearing Timing
1	All data in the FIFO buffer (both sides for double FIFO buffer) allocated to the pipe	
2	Interval count value when the pipe is isochronous transfer type	When resetting the interval count value
3	Internal flags related to the BFRE bit	When changing the BFRE setting
4	FIFO buffer toggle control	When changing the DBLB setting
5	Internal flags related to the transaction count	When forcibly terminating the transaction count function

**Table 52.10 Operations of This Module in Each Setting of PID Bits**

PID Bits	Transfer Type	Transfer Direction (DIR Bit)	Operation of This Module
B'00 (NAK)	Bulk or interrupt	Independent of the setting	Sends a NAK response to a token from the USB host.
	Isochronous	Independent of the setting	Sends no response to a token from the USB host.
B'01 (BUF)	Bulk	Receive direction (DIR = 0)	Receives data and sends an ACK response to the OUT token from the USB host when the FIFO buffer for the pipe is ready to receive. Otherwise, sends a NAK response.  Sends an ACK response to the PING token from the USB host when the FIFO buffer for the selected pipe is ready to receive. Otherwise, sends a NYET response.
		Interrupt	Receive direction (DIR = 0)
	Bulk or interrupt	Transmit direction (DIR = 1)	Sends data in response to a token from the USB host when the FIFO buffer for the pipe is ready to transmit. Otherwise, sends a NAK response.
		Isochronous	Receive direction (DIR = 0)
	Transmit direction (DIR = 1)		Sends data in response to a token from the USB host when the FIFO buffer for the pipe is ready to transmit. Otherwise, sends a Zero-Length packet.
B'10 (STALL) or	Bulk or interrupt	Independent of the setting	Sends a STALL response to a token from the USB host.
B'11 (STALL)	Isochronous	Independent of the setting	Sends no response to a token from the USB host.

(2) PIPE<sub>n</sub>CTR (n = 6 to 8)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BSTS	—	—	—	—	—	ACLRM	SQCLR	SQSET	SQMON	PBUSY	—	—	—	PID[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R/W	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	BSTS	0	R	<p>Buffer Status</p> <p>Indicates the state of the FIFO buffer of the selected pipe.</p> <p>0: The buffer is not accessible.</p> <p>1: The buffer is accessible.</p> <p>The meaning of this bit differs as shown in Table 52.8 depending on the settings of the DIR, BFRE, and DCLRM bits.</p>
14 to 10	—	All 0	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>
9	ACLRM	0	R/W	<p>Buffer Auto-Clear Mode*2*3</p> <p>Enables or disables buffer auto-clear mode for the selected pipe.</p> <p>0: Buffer auto-clear mode is disabled.</p> <p>1: Buffer auto-clear mode is enabled. (All buffers are initialized.)</p> <p>To completely delete the data in the FIFO buffer allocated to the pipe, write 1 and then 0 continuously to the ACLRM bit.</p> <p>Table 52.11 shows data cleared by this module when this bit is set to 1 and then 0 and cases where such data is cleared.</p> <p>Modify this bit when PID = NAK, and the pipe is not set in the CURPIPE bits.</p> <p>When setting this bit to 1 after changing the PID bits for the pipe from BUF to NAK, check that PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK.</p>
8	SQCLR	0	R/W*1	<p>Toggle Bit Clear*2*3</p> <p>Set this bit to 1 to clear the expected value (in DATA0) of the sequence toggle bit for the next transaction of the selected pipe.</p> <p>0: Invalid</p> <p>1: The expected value is cleared in DATA0.</p> <p>When the software sets this bit to 1, this module sets the expected value of the sequence toggle bit of the pipe in DATA0. This module always indicates SQCLR = 0.</p> <p>Set the SQCLR bit to 1 when PID = NAK.</p> <p>When setting this bit to 1 after changing the PID bits for the pipe from BUF to NAK, check that PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK.</p>



Bit	Bit Name	Initial Value	R/W	Description
7	SQSET	0	R/W*1	<p>Toggle Bit Set*2*3</p> <p>Set this bit to 1 to set the expected value of the sequence toggle bit for the next transaction of the selected pipe.</p> <p>0: Invalid</p> <p>1: The expected value is set in DATA1.</p> <p>When the software sets this bit to 1, this module sets the expected value of the sequence toggle bit of the selected pipe in DATA1. This module always indicates SQSET = 0.</p> <p>Set the SQSET bit to 1 when PID = NAK.</p> <p>When setting this bit to 1 after changing the PID bits for the selected pipe from BUF to NAK, check that PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK.</p>
6	SQMON	0	R	<p>Toggle Bit Check</p> <p>Indicates the expected value of the sequence toggle bit for the next transaction of the pipe.</p> <p>0: DATA0</p> <p>1: DATA1</p> <p>If the selected pipe that is not the isochronous transfer type, when a transaction is successfully processed, this module toggles this bit. However, when a DATA-PID mismatch occurs in the receive direction transfer, this bit is not toggled.</p>
5	PBUSY	0	R	<p>Pipe Busy</p> <p>Indicates whether the selected pipe is currently used in the USB bus or not.</p> <p>0: The selected pipe is not used in the USB bus.</p> <p>1: The selected pipe is being used in the USB bus.</p> <p>When this module starts the USB transaction for the selected pipe, this module sets this bit to 1. This module clears this bit to 0 upon completion of each transaction.</p> <p>After the software sets PID = NAK, read this bit to see if changing the pipe setting is enabled or not.</p>
4 to 2	—	All 0	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>

Bit	Bit Name	Initial Value	R/W	Description
1, 0	PID[1:0]	00	R/W	<p>Response PID</p> <p>Specify a response used in the next transaction for the selected pipe.</p> <p>00: NAK response</p> <p>01: BUF response (depending on buffer state)</p> <p>10: STALL response</p> <p>11: STALL response</p> <p>These bits are set to NAK by default. To perform USB transfer with the selected pipe, change the setting of these bits to BUF. Table 52.10 shows the basic operation (with no error in packets) of this module in each setting of the PID bits.</p> <p>When changing these bits from BUF to NAK by the software while the pipe is in USB communication, write 00 (NAK) to these bits and then check PBUSY = 1 to confirm that the USB transfer of the selected pipe entered the NAK state. However, when this module changed these bits to NAK, the software needs not check the PBUSY bit.</p> <p>This module modifies these bits in the following cases.</p> <ul style="list-style-type: none"> <li>• When the selected pipe is in the receive direction and the software sets the SHTNAK bit of the selected pipe to 1, this module indicates PID = NAK when this module recognizes the transfer end.</li> <li>• When this module receives data with a payload exceeding the MaxPacketSize value for the pipe, this module indicates PID = STALL (11).</li> <li>• When this module detects a USB bus reset, this module indicates PID = NAK.</li> </ul> <p>Set these bits as follows:</p> <ul style="list-style-type: none"> <li>• To change the state from NAK (00) to STALL, write B'10.</li> <li>• To change the state from BUF (01) to STALL, write B'11.</li> <li>• To change the state from STALL (11) to NAK, write B'10 then B'00.</li> <li>• To change the state from STALL to BUF, set these bits to NAK and then to BUF.</li> </ul>

- Notes:
1. Only reading 0 and writing 1 are enabled.
  2. Set the ACLRM, SQCLR, or SQSET bit when PID = NAK, and the selected pipe is not set in the CURPIPE bits.
  3. When setting the ACLRM, SQCLR, or SQSET bit after changing the PID bits from BUF to NAK, check that PBUSY = 0 for the pipe. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK.

**Table 52.11 Data Cleared by This Module when ACLRM = 1**

No.	Data Cleared by the ACLRM Bit	Clearing Timing
1	All data in the FIFO buffer allocated to the selected pipe	
2	Not Support	
3	Internal flags related to the BFRE bit	When changing the BFRE setting
4	Internal flags related to the transaction count	When forcibly terminating the transaction count function

### 52.2.33 Pipe n Transaction Counter Enable Register (PIPnTRE) (n = 1 to 5, 9 to F)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

PIPnTRE enables or disables the transaction counter function and clears the counter for pipes 1 to 5, 9 to F.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	TRENB	TRCLR	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9	TRENB	0	R/W	Transaction Counter Enable Enables or disables the transaction counter function. 0: The transaction counter function is disabled. 1: The transaction counter function is enabled. When the software sets the number of total packets in the TRNCNT bits in PIPEnTRN for the receive pipe and then sets this bit to 1, this module controls the following when it received the same number of packets as the setting of the TRNCNT bits. When continuous communication mode is used (CNTMD = 1), this module toggles the received data to the CPU even if the FIFO buffer is not full at the end of reception. When SHTNAK = 1, this module changes the PID bits for the corresponding pipe to NAK when this module received the same number of packets as the setting of the TRNCNT bits. When BFRE = 1, this module asserts the BRDY interrupt when this module received the same number of packets as the setting of the TRNCNT bits and read the receive data completely. For transmit pipes, set this bit to 0. When the transaction counter function is not used, set this bit to 0. When using the transaction counter function, set the TRNCNT bits and then set this bit to 1. Furthermore, set this bit to 1 before receiving the first packet that is included in the transaction count range.
8	TRCLR	0	R/W	Transaction Counter Clear Clears the current count value of the transaction counter for the pipe and indicates TRCLR = 0. 0: Invalid 1: The current count value is cleared.
7 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Note: Change the bits in this register when CSSTS = 0 and PID = NAK.

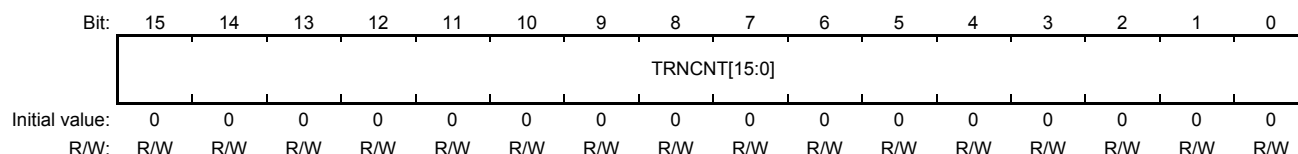
When changing the bits in this register after changing the PID bits for the pipe from BUF to NAK, check that CSSTS = 0 and PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK.

### 52.2.34 Pipe n Transaction Counter Register (PIPEnTRN) (n = 1 to 5, 9 to F)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

PIPEnTRE is a transaction counter for pipes 1 to 5, 9 to F.

This register is initialized by a power-on reset, but the setting of this register is retained through a USB bus reset.



Bit	Bit Name	Initial Value	R/W	Description
15 to 0	TRNCNT [15:0]	All 0	R/W	<p>Transaction Counter</p> <p>Writing:</p> <p>Specify the number of transactions of DMA transfer.</p> <p>Reading:</p> <p>When TRENb = 0, the set number of transactions is indicated.</p> <p>When TRENb = 1, the number of current transactions is indicated.</p> <p>This module increments (+1) the value of these bits when the following conditions are all satisfied.</p> <p>TRENb = 1</p> <p>TRCNT value ≠ current count value +1 when a packet is received.</p> <p>The payload of the received packet equals the value of the MXPS bits.</p> <p>This module clears these bits to 0 when any of the following is satisfied.</p> <p>When the following conditions are all satisfied</p> <ul style="list-style-type: none"> <li>— TRENb = 1</li> <li>— TRCNT value = current count value +1 when a packet is received.</li> <li>— The payload of the received packet equals the value of the MXPS bits.</li> </ul> <p>When the following conditions are all satisfied</p> <ul style="list-style-type: none"> <li>— TRENb = 1</li> <li>— A short packet is received.</li> </ul> <p>When the following conditions are all satisfied</p> <ul style="list-style-type: none"> <li>— TRENb = 1</li> <li>— The software sets the TRCLR bit to 1.</li> </ul> <p>For transmit pipes, set these bits to all 0.</p> <p>When the transaction counter function is not used, set these bits to all 0.</p> <p>Change these bits when CSSTS = 0, PID = NAK, and TRENb = 0.</p> <p>When setting these bits to 1 after changing the PID bits for the pipe from BUF to NAK, check that CSSTS = 0 and PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK.</p> <p>When changing these bits, set TRCNT = 1 and then set TRENb = 1.</p>

**52.2.35 Low Power Status register (LPSTS)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

This register provide low power management control.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	SUSPM	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
14	SUSPM	0	R/W	SuspendM control 0: UTMI suspend mode 1: UTMI normal mode This bit should set to 1 when normal operating. UTMI clock is halted if this bit set to 0. Note: This controller deny register access without as follow registers if this bit set to 0. SYSCFG0 BUSWAIT INTENB1 LPSTS BCCTRL UGCTRL UGSTS
13 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

**52.2.36 USB General Control Register (UGCTRL)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

This register provide embedded USB PHY control.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	CONNECT	—	PLL RESET
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 3	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
2	CONNECT	0	R/W	USB connect control 0: PHY receiver halted 1: PHY receiver enabled
1	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	PLLRESET	1	R/W	PLL Reset 0: PLL reset release 1: PLL reset assert

**52.2.37 USB General Control Register 2 (UGCTRL2)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

This register provide embedded USB PHY control.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	USB2SEL	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	USB0SEL	—	—	—	—	
Initial value:	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31	USB2SEL	0	R/W	USB2.0 Ch.2 [RZ/G1H]/Ch1 [M, N] Selection 0: Select EHCI/OHCI host module for USB2.0 ch2 (PHY) 1: Select USB3.0 module for USB2.0 ch2 (PHY)
30 to 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5, 4	USB0SEL	11	R/W	USB2.0 Ch.0 Selection 01: Select EHCI/OHCI host module for USB2.0 ch0 (PHY) 11: Select HS USB module for USB2.0 ch0 (PHY) Other than above: Setting prohibited
3 to 0	—	0001	R	Reserved These bits are always read as B'0001. The write value should always be B'0001.

### 52.2.38 USB General Status Register (UGSTS)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

This register provide Embedded USB PHY status.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	LOCK	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 9	—	All 0	R	Reserved
8	LOCK	0	R	Embedded USB PHY PLL Lock status 0: Embedded USB PHY PLL clock halted 1: Embedded USB PHY PLL Lock completed
7 to 0	—	All 0	R	Reserved



## 52.3 Operation

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

### 52.3.1 System Control and Oscillation Control

This section describes register operations required for the initial settings of this module and the registers required for the power consumption control.

#### (1) Power control and Initialization

The following is the initialize power on procedure of USB subsystem.

1. Turn on the power domain of HS-USB
2. Supply 1.8 V (VD181)
3. Supply 3.3 V (VD331) (Note: Do not supply 3.3 V when 1.8 V is not supplied.)
4. Wait 100  $\mu$ s for USB PHY power stable.
5. Power Isolation control disable
6. HS-USB and EHCI module stop release and module reset assert.
7. PLLRESET release
8. LPSTS.SUSPM set to normal mode.
9. Check PLL Lock status by USB General status register
10. Starting normal operation after PLL Lock status enabled.
11. UGCTRL.CONNECT bit set to 1

The following is the power off procedure of USB subsystem

1. Normal operation finished
2. UGCTRL.CONNECT bit set to 0
3. PLL disable by PLLRESET assert
4. Power Isolation control enable
5. Shut off 3.3V (VD331)
6. Shut off 1.8V (VD181) (Note: Do not shut off 1.8 V while 3.3 V is being supplied.)
7. Module stop enable and shut off power domain of HS-USB if needed.

#### (2) Enabling High-Speed Operation

This module can set the USB transmission rate (communication bit rate) by the software.

When the function controller function is selected, high-speed operation or full-speed operation is selectable. To enable high-speed operation with this module, set the HSE bit in SYSCFG to 1. When high-speed operation is enabled, this module executes the reset handshake protocol and automatically sets the USB transmission rate. The reset handshake result can be checked by the RHST bits in DVSTCTR.

When high-speed operation is disabled, this module operates only in full speed when the function controller function is selected.

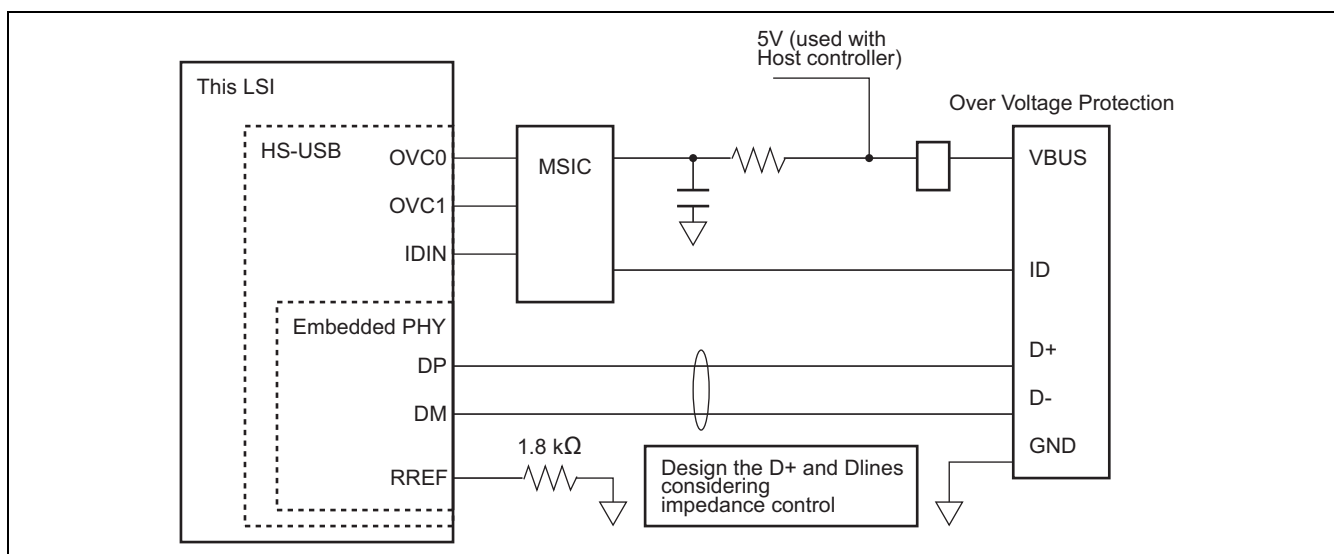
### (3) USB Data Bus Resistor Control

Figure 52.1 shows the connection between this module and the USB connector.

This module incorporates a pull-up resistor of the D+ signal. Specify pull-up using the DPRPU bits in SYSCFG.

Furthermore, this module controls the terminating resistors of the D+ and D- signals in high-speed operation, and the output resistors in full-speed operation. This module automatically switches the on-chip resistors after connection to the host controller detecting a reset handshake, suspended state, or resume.

When the DPRPU bit in SYSCFG is set to 0 during communication with the host controller, this module disables the pull-up resistors (or terminating resistors) of the USB data line. Therefore, the USB host can be notified of a disconnection from the device.



**Figure 52.1 Connection to the USB Connector**

### (4) Software reset when the USB disconnection is detected

Issue a software reset of the USBHS module when the USB disconnection is detected. If the DMA interface is being used, issue a software reset of the USB-DMAC module as well. A software reset can be issued via a register in the CPG

Whether or not the USB disconnection is detected can be determined by the VBSTS in the INTSTS0 register when the function controller function is selected.

Note: USB-PHY might become inoperable to use by the instantaneous interruption of VBUS. As a result S/W on the LSI side (driver) becomes a state of the connection, and USB-PHY becomes a state of power cutoff. It's possible to cancel this state by putting the next way into effect by software.

- 1) When detecting a bus reset or cutoff of VBUS, please refer to the state bit of USB - PHY (USB\_OFF bit of USB\_CR2 register in GPIO) and in case of USB\_OFF=1, set USB\_START bit.
- 2) When 1) is performed and USB - PHY is started, USB\_PHY\_ON interrupt occurs, so please perform a soft reset to USBHS,USB-DMAC and do the setting by which USBHS,USB-DMAC is initialization and DP pull up --, etc. by this timing.

### 52.3.2 Interrupt Function

Table 52.12 lists the interrupt generating conditions of this module.

When any of the following interrupt generating conditions are satisfied and the interrupt output is enabled by the corresponding interrupt enable register, this module outputs a USB interrupt request to the interrupt controller (INTC).

**Table 52.12 Interrupt Generating Conditions**

Bit	Interrupt Name	Interrupt Generating Conditions	Function	Related Status
VBINT	VBUS interrupt	When VBUS input pin state change is detected (both L to H and H to L)		VBSTS
RESM	Resume interrupt	When a USB bus state change is detected in the suspended state (J-State to K-State or J-State to SE0)		—
SOFR	Frame number update interrupt	SOFRM = 0: When an SOF packet with a different frame number is received SOFRM = 1: When an SOF packet with a $\mu$ frame number of 0 cannot be received due to damage, etc.		—
DVST	Device state transition interrupt	When a device state transition is detected USB bus reset detected Suspended state detected SET_ADDRESS request received SET_CONFIGURATION request received		DVSQ
CTRT	Control transfer stage transition interrupt	When a control transfer stage transition is detected Setup stage completed Control write transfer status stage shifted Control read transfer status stage shifted Control transfer completed Control transfer sequence error occurred		CTSQ
BEMP	Buffer empty interrupt	When the buffer becomes empty after sending all buffer memory data When a packet with a size exceeding the maximum packet size is received		BEMPSTS.PIPEBEMP
NRDY	Buffer not ready interrupt	When NAK is sent in response to IN token, OUT token, or PING token When a CRC error or bit stuffing error occurred during data reception in isochronous transfer When an overrun or underrun error occurred during data reception in isochronous transfer		NRDYSTS.PIPENRDY
BRDY	Buffer ready interrupt	When the buffer becomes ready for reading or writing		BRDYSTS.PIPEBRDY
OVRRCR	OVRRCR interrupt	When an OVC input pin state change is detected		OVCMON

Note: These bits in this table are those of INTSTS0 if any register's name is not indicated.

Figure 52.2 shows a block diagram of the interrupt circuit of this module.

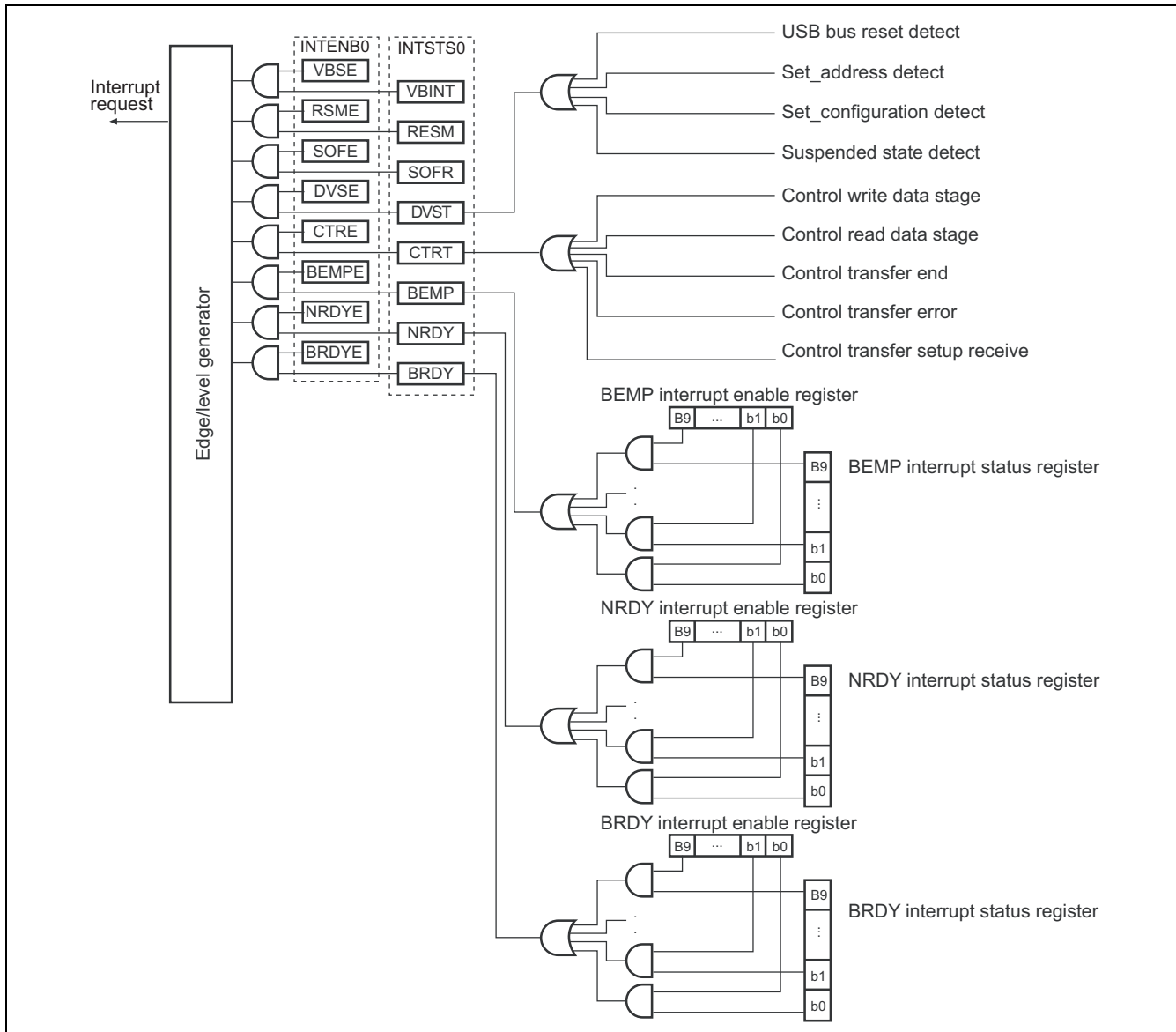


Figure 52.2 Block Diagram of Interrupt Circuit

**(1) BRDY Interrupt**

A BRDY interrupt can be generated when the following conditions in each pipe are satisfied, this module sets the corresponding bit in BRDYSTS to 1. At this time, when the PIPEBRDYE bit for the pipe in BRDYENB is set to 1 and the BRDYE bit in INTENB0 is set to 1 by the software, this module generates a BRDY interrupt.

BRDY interrupt generating conditions and clearing method depend on the settings of the BRDYM bit and the BFRE bit for each pipe.

**(a) When BRDY interrupt disable (BRDYM = 0) and BRDY interrupt output enable (BFRE = 0) at data reception/transmission are specified**

With this setting, a BRDY interrupt indicates that the FIFO port is accessible.

This module generates an internal BRDY interrupt request trigger when the following conditions are satisfied, and sets the PIPEBRDY bit corresponding to the request trigger pipe to 1.

## 1. Pipes set for the transmit direction

- When the software changes the DIR bit from 0 to 1
- When this module finishes sending a packet of the pipe while data write from the CPU to the FIFO buffer allocated to the pipe is disabled (BSTS = 0)
- When continuous communication mode is selected, this module generates a BRDY interrupt request trigger upon completion of sending data for one side of the FIFO buffer.
- When a double FIFO buffer is specified and one side of the FIFO buffer is empty when data write to the other side of the FIFO buffer is completed.  
Even if one side of the FIFO buffer becomes empty while the other side is in data write processing, no BRDY interrupt is generated until the ongoing data write finishes.
- When this module generates a buffer flush for a pipe of isochronous transfer type
- When the FIFO buffer becomes write enable state by writing 1 to the ACLRM bit

No BRDY interrupt request trigger is generated for the DCP (in data transmission of control transfer).

## 2. Pipes set for the receive direction

- When this module receives a packet successfully and the FIFO buffer becomes ready for reading while data read access from the CPU to the FIFO buffer allocated to the pipe is disabled (BSTS = 0)
- No BRDY interrupt request trigger is generated in transactions with incorrect data PID.
- When continuous communication mode is selected, no BRDY interrupt request trigger is generated for packets with a MaxPacketSize data size and when the FIFO buffer still has available space.
- When this module receives a short packet, this module generates a BRDY interrupt request trigger even if the buffer has available space.
- When a transaction counter is used, this module generates a BRDY interrupt request trigger when this module receives a packet with a size of the set value even if the FIFO buffer still has available space.
- When a double FIFO buffer is specified and one side of the FIFO buffer is ready for reading when data read from the other side of the FIFO buffer is completed  
Even if data read for one side of the FIFO buffer is completed while the other side is undergoing data read, no BRDY interrupt request trigger is generated until the ongoing data read finishes.

This interrupt is not generated in communication in the control transfer status stage.

The software can clear the PIPEBRDY interrupt status of the pipe by writing 0 to the PIPEBRDY bit for the pipe in BRDYSTS. At this time, write 1 to the bits corresponding to other pipes.

Be sure to clear the BRDY interrupt status before accessing the FIFO buffer.

**(b) When BRDY interrupt disable (BRDYM = 0) and BRDY interrupt output enable (BFRE = 1) at the end of data read are specified**

With this setting, this module determines that a BRDY interrupt is generated upon completion of reading all data of one transfer in a receive pipe, and sets the bit for the pipe in this register to 1.

This module determines that the last data of a transfer was received in either of the following cases.

- A Zero-Length packet or another short packet is received.
- A transaction counter (TRNCNT bits) is used and a packet with a size of the value of the TRNCNT bits is received.

When either of these conditions is satisfied and the data read is completed, this module determines that reading all data for one transfer is completed.

When this module receives a Zero-Length packet with the FIFO buffer empty, this module determines that reading all data for one transfer is completed when the Zero-Length packet data is toggled to the CPU. In this case, write 1 to the BCLR bit in the corresponding FIFOCTR register by the software to start the next transfer.

With this setting, this module generates no BRDY interrupt for transmit pipes.

The software can clear the PIPEBRDY interrupt status of the pipe to 0 by writing 0 to the PIPEBRDY bit for the pipe. At this time, write 1 to the bits corresponding to other pipes.

When using this mode, do not change the BFRE setting until the processing for one transfer is completed.

To change the BFRE bit during processing, clear all FIFO buffers for the pipe by the ACLRM bit.

**(c) When BRDY interrupt enable (BRDYM = 1) and BRDY interrupt output enable (BFRE = 0) at data reception/transmission are specified**

With this setting, the value of the PIPEBRDY bit varies with the value of the BSTS bit for each pipe. That is, this module indicates 1 or 0 of the BRDY interrupt status according to the FIFO buffer status.

1. Pipes set for the transmit direction

When the FIFO port is ready to write data, the PIPEBRDY bit indicates 1. When the FIFO port is not ready to write data, the PIPEBRDY bit indicates 0.

However, even if the transmit pipe of the DCP is ready to write data, no BRDY interrupt is asserted.

2. Pipes set for the receive direction

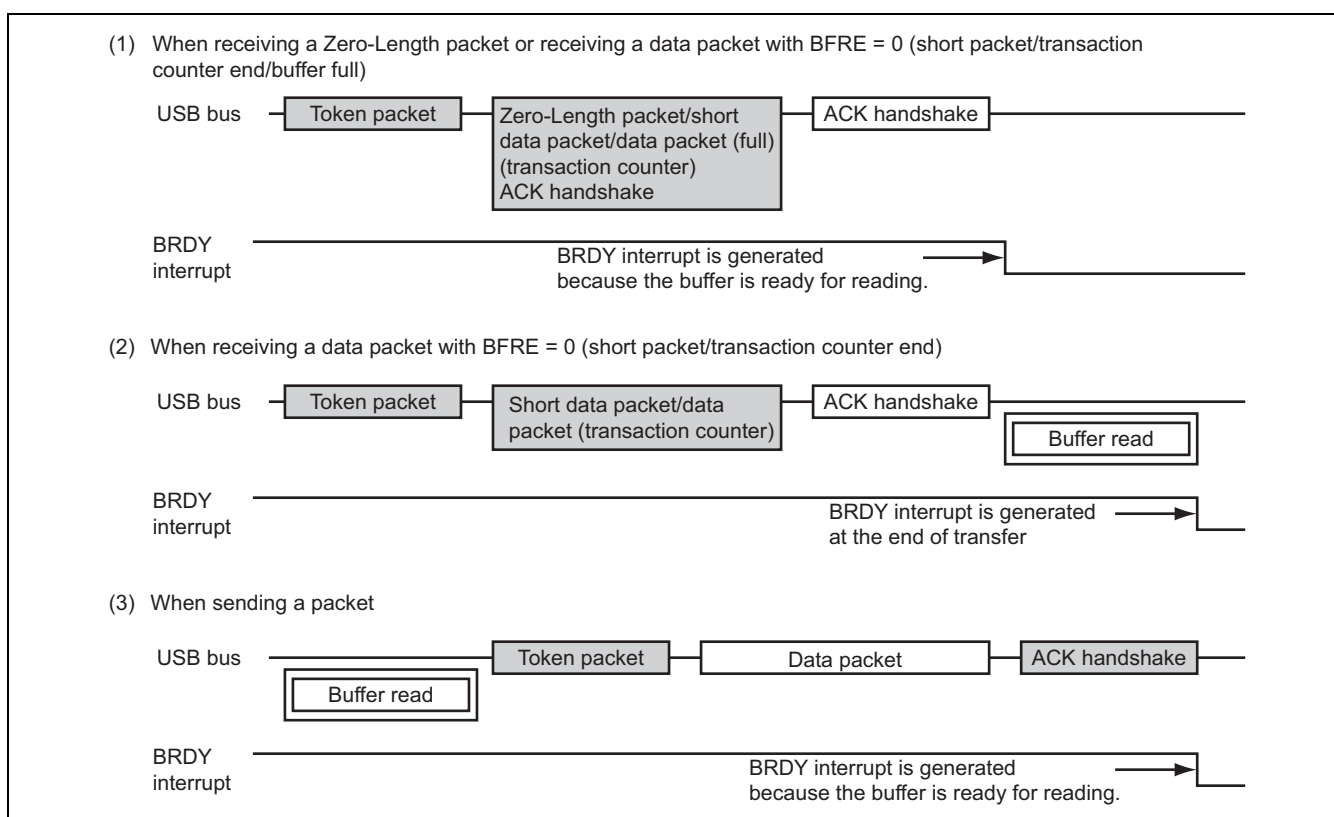
When the FIFO port is ready to read data, the PIPEBRDY bit indicates 1. When all data is read from the FIFO port (reading disabled), the PIPEBRDY bit indicates 0.

When this module receives a Zero-Length packet with the FIFO buffer empty, this module indicates 1 with the corresponding bit until 1 is written to BCLR by the software, and continues to assert the BRDY interrupt.

With this setting, the software cannot clear the PIPEBRDY bit to 0.

When BRDYM = 1, set the BFRE bit to 0 for all pipes.

Figure 52.3 shows the BRDY interrupt generation timing.



**Figure 52.3 BRDY Interrupt Generation Timing**

## (2) NRDY Interrupt

When this module generates an internal NRDY interrupt request for the pipe in which PID = BUF is set by the software, this module indicates PIPENRDY = 1 for the pipe in NRDYSTS. At this time, when 1 is set in the corresponding bit in NRDYENB by the software, this module indicates NRDY = 1 in INTSTS0 and generates a USB interrupt.

The following shows the conditions for this module to generate an internal NRDY interrupt request for a pipe.

Furthermore, when executing the control transfer status stage, this module generates no interrupt request.

### 1. Pipes in the transmit direction

— When this module receives an IN token with no transmit data in the FIFO buffer

This module generates an NRDY interrupt request and indicates PIPENRDY = 1.

— When the pipe in which the interrupt is generated is isochronous transfer type, this module sends a Zero-Length packet and indicates OVRN = 1.

### 2. Pipes in the receive direction pipe

— When this module receives an OUT token with the FIFO buffer occupied

— When the pipe in which the interrupt is generated is isochronous transfer type, this module generates an NRDY interrupt request when this module receives an OUT token, and indicates PIPENRDY = 1 and OVRN = 1.

— When the pipe in which the interrupt is generated is not isochronous transfer type, this module generates an NRDY interrupt request when this module sends an NAK handshake response after receiving data following the OUT token, and indicates PIPENRDY = 1.

However, this module generates no NRDY interrupt when resending data (in the case of DATA-PID mismatch) or when an error occurs in a data packet.

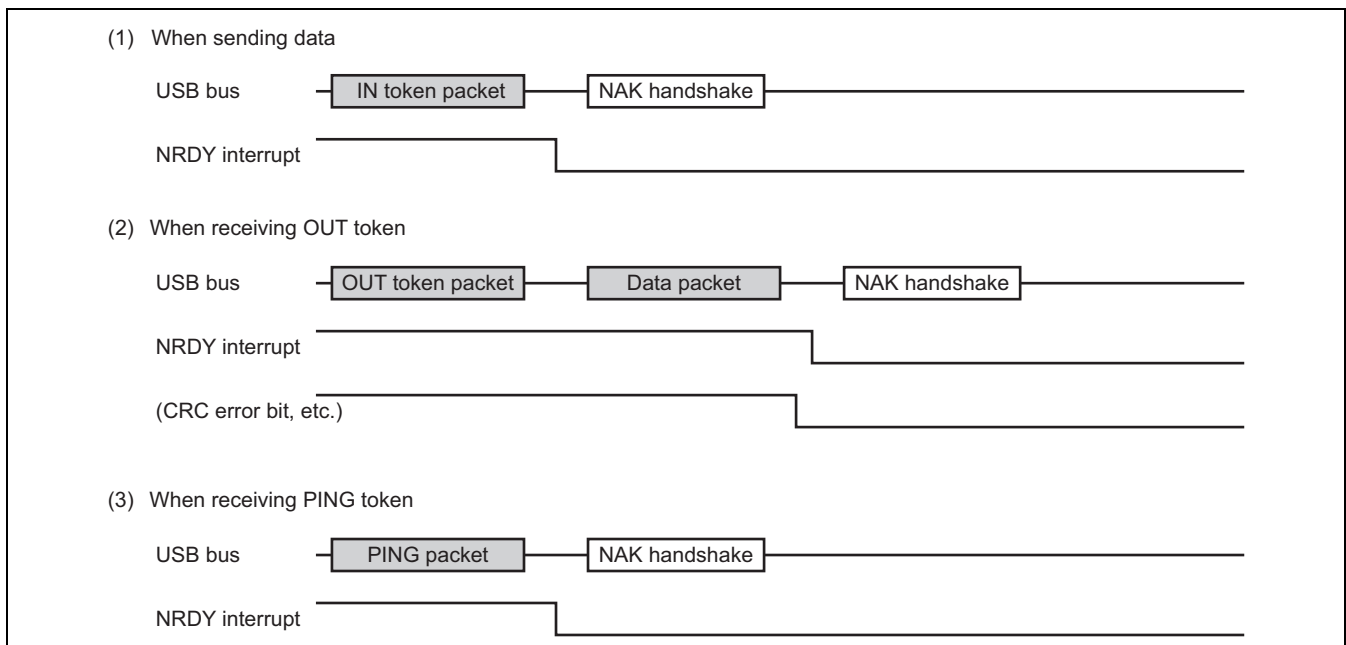
— When this module receives a PING token with the FIFO buffer occupied

This module generates an NRDY interrupt request when this module receives a PING token and indicates PIPENRDY = 1.

— When a packet is not received correctly within the interval frame in an isochronous transfer-type pipe

This module generates an NRDY interrupt request when this module receives SOF and indicates PIPENRDY = 1.

Figure 52.4 shows the NRDY interrupt generation timing when the function controller function is selected.



**Figure 52.4 NRDY Interrupt Generation Timing when the Function Controller Function is Selected**



### (3) BEMP Interrupt

When this module detects a BEMP interrupt for the pipe in which PID = BUF is set by the software, this module indicates PIPEBEMP = 1 for the pipe in BEMPSTS. At this time, when 1 is set in the corresponding bit in BEMPENB by the software, this module indicates BEMP = 1 in INTSTS0 and generates a USB interrupt.

This module generates an internal BEMP interrupt request in the following cases.

#### 1. Transmit direction pipes

- When the FIFO buffer for the pipe is empty at the end of transmission (including transmission of a Zero-Length packet)
- When single buffer is set for the FIFO buffer, this module generates an internal BEMP interrupt request concurrently with a BRDY interrupt for pipes other than DCP.

However, this module generates no internal BEMP interrupt request in the following cases.

- In the case of double buffer, when the software (DMAC) already started writing data to the FIFO buffer of the CPU at the end of transmission for one-side data
- When the buffer is cleared (empty) by writing 1 to the ACLRM or BCLR bit.
- When sending a Zero-Length packet (IN transfer) of the control transfer status stage

#### 2. Receive direction pipes

- When this module receives a packet with a data size exceeding the MaxPacketSize value
- In this case, this module generates a BEMP interrupt request and indicates the PIPEBEMP = 1 for the pipe, ignores the received data, and changes the PID bits for the pipe to STALL (11).

At this time, this module sends a STALL response.

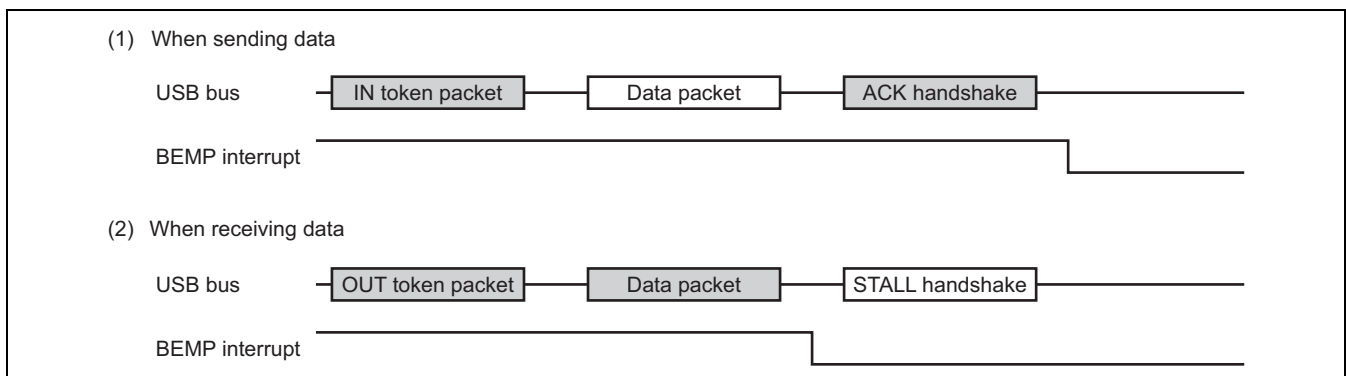
However, this module generates no BEMP interrupt request in the following cases.

- When this module detects a CRC error or bit stuffing error in the receive data
- When executing the SETUP transaction

Writing 0 to the PIPEBEMP bits clears the status.

Writing 0 to the PIPEBEMP bits has no effect on the operation of this module.

Figure 52.5 shows the BEMP interrupt generation timing when the function controller function is selected.

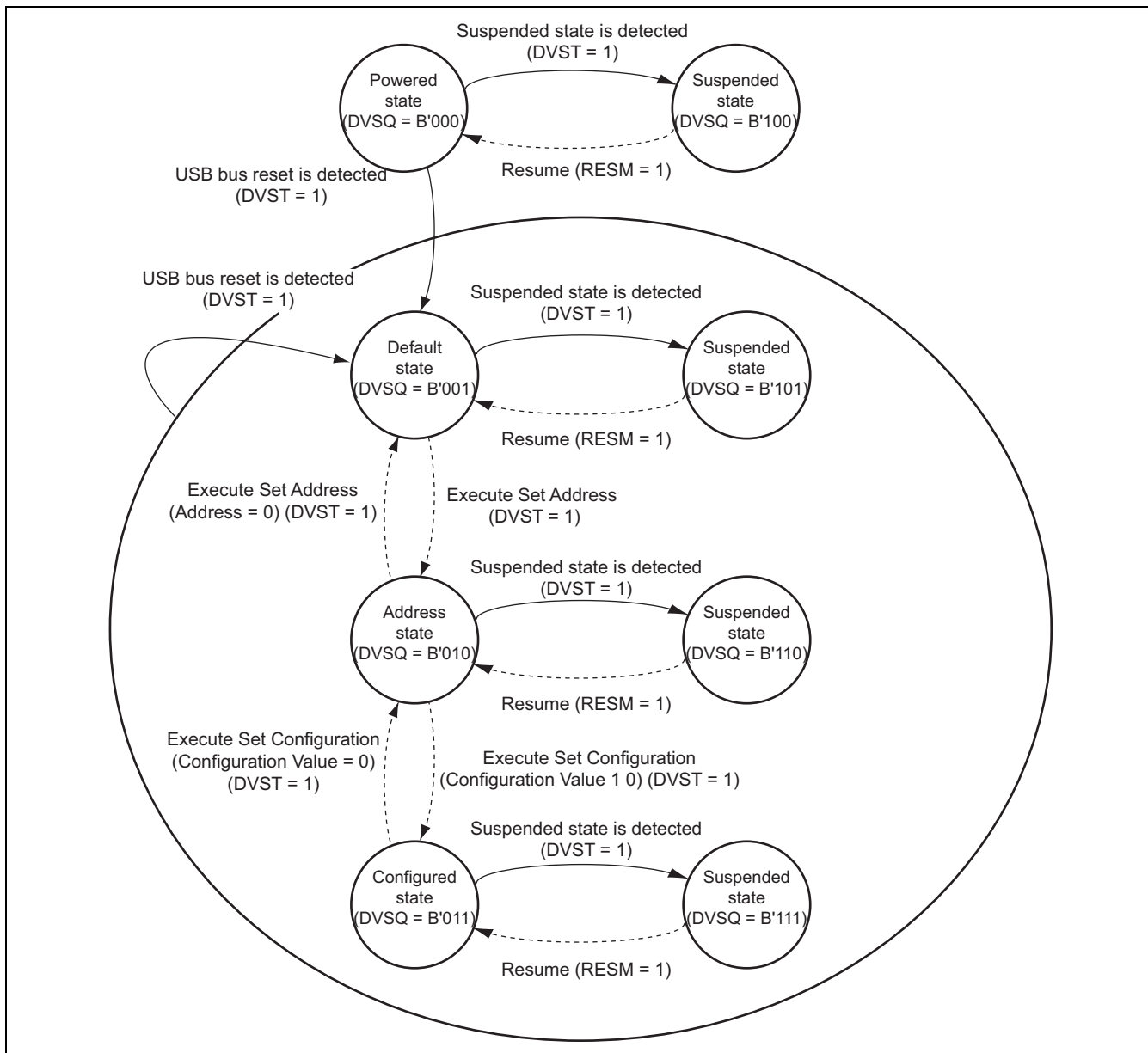


**Figure 52.5 BEMP Interrupt Generation Timing when the Function Controller Function is Selected**

**(4) Device State Transition Interrupt**

Figure 52.6 shows the device state transitions of this module. This module controls device states and generates device state transition interrupts. However, when returning from the suspended state (detecting the resume signal), this module detects the transition with a resume interrupt. The device state transition interrupt is enabled or disabled by setting INTENB0. The current device state can be monitored using the DVSQ bits in INTSTS0.

When this module shifts to the default state, a device state transition interrupt occurs after executing the reset handshake protocol.



**Figure 52.6 Device State Transitions**

**(5) Control Transfer Stage Transition Interrupt**

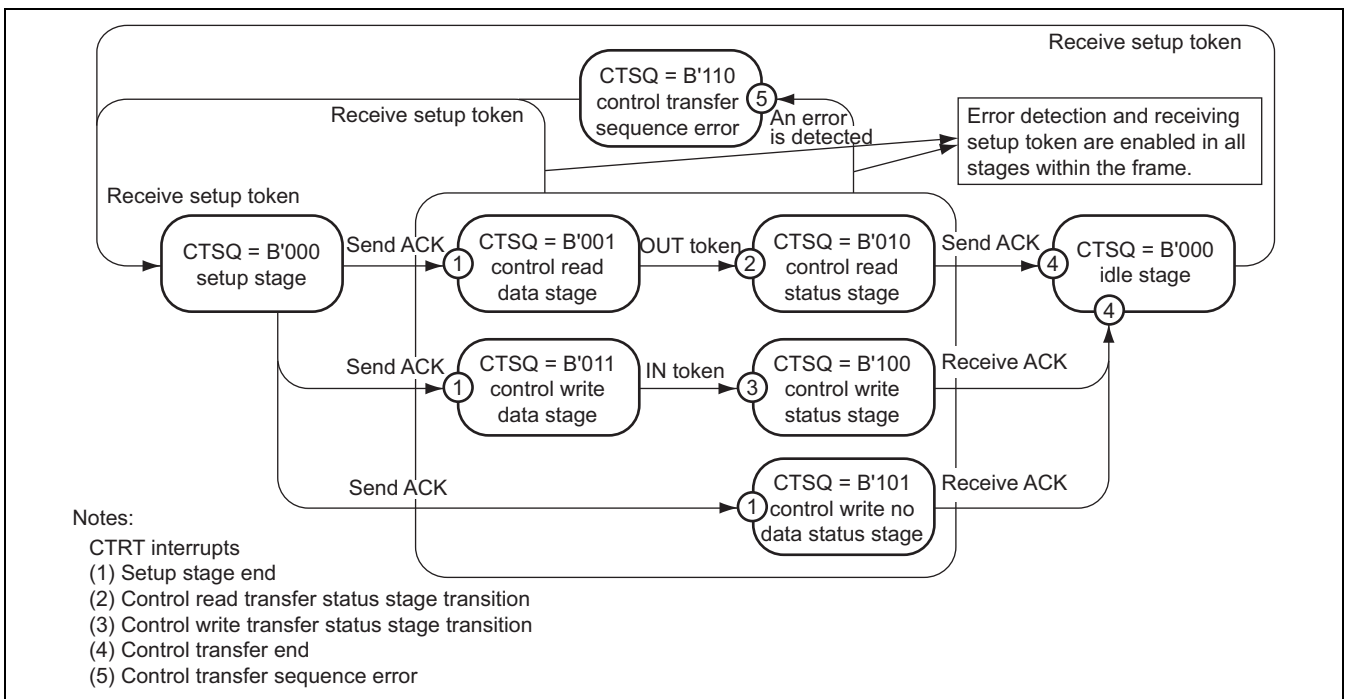
Figure 52.7 shows control transfer stage transitions of this module. This module manages the sequence of control transfers and generates control transfer stage transition interrupts. Enabling or disabling each control transfer stage transition interrupt can be set by INTENB0. The current transfer stage after transition can be checked by the CTSQ bits in INTSTS0.

The following describes control transfer sequence errors. When an error occurs, the PID bits in DCPCTR indicate B'1x (STALL response).

1. Control read transfer
  - This module receives an OUT or PING token in response to the IN token in the data stage before starting data transfer.
  - This module receives an IN token in the status stage.
  - This module receives a packet with a data packet of DATAPID = DATA0 in the status stage.
2. Control write transfer
  - This module receives an IN token in response to the OUT token in the data stage before sending an ACK response.
  - This module receives a packet with the first data packet of DATAPID = DATA0.
  - This module receives an OUT or PING token in the status stage.
3. Control write no-data control transfer
  - This module receives an OUT or PING token in the status stage.

If the size of the receive data exceeds the wLength value of the USB request in the control write transfer data stage, this is not treated as a control transfer sequence error. This module sends ACK for normal end in response to a packet other than Zero-Length packet in the control read transfer status stage.

When a CTRT interrupt is generated (SERR = 1) due to a sequence error, CTSQ = B'110 is retained until the interrupt status is cleared (CTRT = 0) by the system. For this reason, while CTSQ = B'110, even if a new USB request is received, a CTRT interrupt at the end of the setup stage is not generated. (This module retains the setup stage end status and generates a setup stage end interrupt after the interrupt status is cleared by the software.)



**Figure 52.7 Control Transfer Stage Transitions**

### (6) Frame Update Interrupt

Figure 52.8 shows an example of the SOFR interrupt output timing of this module.

An SOFR interrupt is generated immediately after the frame number is updated.

When this module detects a new SOF packet during the full-speed operation, this module updates the frame number and generates an SOFR interrupt. In the high-speed operation, however, the frame number is not updated or no SOFR interrupt is generated unless the module enters the  $\mu$  SOF lock state. Furthermore, the SOF interpolation function is not activated. The  $\mu$  SOF lock state occurs when this module receives a  $\mu$  SOF packet twice in a row with different frame numbers without an error.

The  $\mu$  SOF lock monitoring start and stop conditions are as follows:

1.  $\mu$  SOF lock monitoring start conditions  
USBE = 1
2.  $\mu$  SOF lock monitoring stop conditions  
USBE = 0, receiving USB bus reset, or detection of suspended state

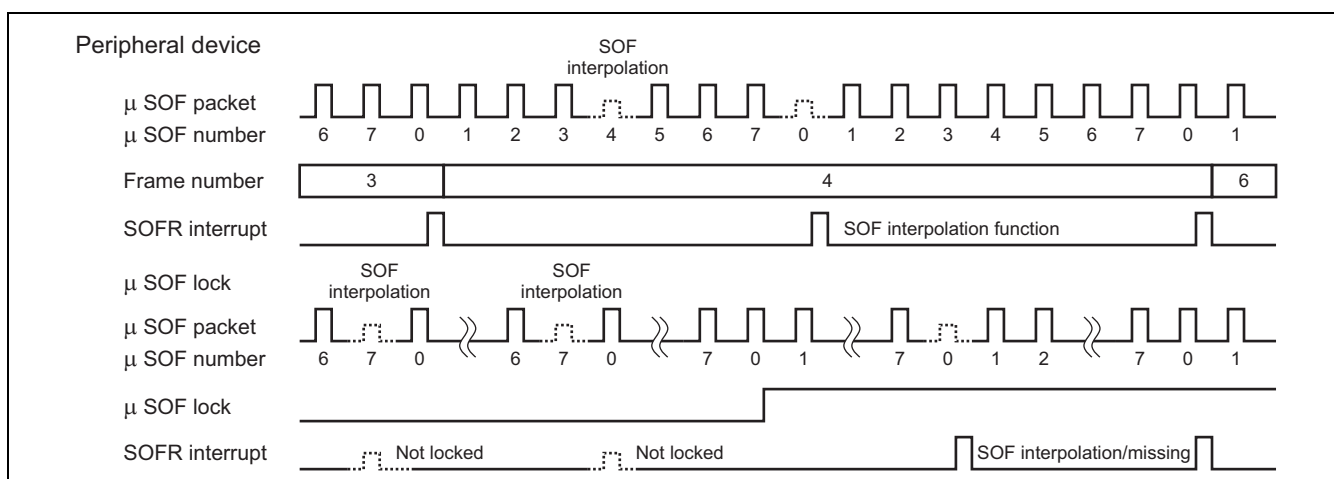


Figure 52.8 Example of SOFR Interrupt Output Timing

### (7) VBUS Interrupt

When the VBUSIN\_0 pin state changes, a VBUS interrupt is generated. The VBUSIN\_0 pin level can be checked by the VBSTS bit in INTSTS0. The VBUS interrupt is used to check connection or disconnection to the host controller.

However, when the system starts up with the host controller connected, the VBUSIN\_0 pin state remains unchanged, and therefore the first VBUS interrupt is not generated.

### (8) Resume Interrupt

When the function controller function is selected and the USB bus state changes (J-State to K-State or J-State to SE0) with the device state suspended, a resume interrupt is generated. The resume interrupt is used to detect the return from the suspended state.

### 52.3.3 Pipe Control

Table 52.13 lists the pipe settings of this module. In the USB data transfer, data must be transmitted or received using virtual pipes called “endpoint.” This module is provided with ten pipes for data transfer. Set each pipe according to system specifications.

**Table 52.13 Pipe Settings**

Register Name	Bit Name	Setting	Remarks
DCPCFG	TYPE	Transfer type	Pipes 1 to F: Setting allowed
PIPECFG	BFRE	BRDY interrupt mode	Pipes 1 to 5, 9 to F: Setting allowed
	DBLB	Double buffer	Pipes 1 to 5, 9 to F: Setting allowed
	CNTMD	Continuous transfer or discontinuous transfer	Pipes 1, 2, 9, A: Setting allowed only when bulk transfer is selected
			Pipes 3 to 5, B to F: Setting allowed
	DIR	Transfer direction	IN or OUT selectable
	EPNUM	Endpoint number	Pipes 1 to F: Setting allowed Set a value other than 0000 when using pipes
PIPEBUF	BUFSIZE	Buffer memory size	DCP: Setting disallowed (256 bytes fixed)
			Pipes 1 to 5, 9 to F: Setting allowed (up to 2 Kbytes) Pipes 6 to 8: Setting disallowed (64 bytes fixed)
PIPEBUF	BUFNMB	Buffer memory number	DCP: Setting disallowed (H'0 to H'3 fixed)
			Pipes 1 to 5, 9 to F: Setting allowed (H'8 to H'7F) Pipes 6 to 8: Setting disallowed (H'4 to H'7 fixed)
DCPMAXP PIPEMAXP	MXPS	Maximum packet size	Setting conforming to the USB Specification
PIPEPERI	IFIS	Buffer flush	Pipes 1, 2: Setting allowed only when isochronous transfer is selected
			Pipes 3 to F: Setting disallowed
PIPEPERI	IITV	Interval counter	Pipes 1, 2: Setting allowed only when isochronous transfer is selected
			Pipes 3 to F: Setting disallowed
DCPCTR PIPECTR	BSTS	Buffer status	For DCP, receive buffer status and transmit buffer status are switched by the ISEL bit.
	INBUFM	IN buffer monitor	Provided only for pipes 3 to 5, 9 to F.
	ATREPM	Auto-response mode	Pipes 1 to 5, 9 to F Setting allowed only when the function controller function is selected.
	ACLRM	Buffer auto-clear	Pipes 1 to F Setting allowed
	SQCLR	Sequence clear	Data toggle bit clear

Register Name	Bit Name	Setting	Remarks
DCPCTR	SQSET	Sequence setting	Data toggle bit setting
PIPEnCTR	SQMON	Sequence check	Data toggle bit check
	PBUSY	Pipe busy check	
	PID	Response PID	See section 52.3.3 (6), Response PID.
	TRENB	Transaction count enable	Pipes 1 to 5, 9 to F: Setting allowed
PIPEnTRE	TRCLR	Current transaction counter clear	Pipes 1 to 5, 9 to F: Setting allowed
	TRNCNT	Transaction counter	Pipes 1 to 5, 9 to F: Setting allowed

### (1) Pipe Control Registers Switching Procedure

The following bits in the pipe control registers can be modified only when USB communication is set to disabled (PID = NAK).

Bits/registers that cannot be modified when USB communication is set to enabled (PID = BUF)

- Each bit in DCPCFG and DCPMAXP
- SQCLR and SQSET bits in DCPCTR
- Each bit in PIPECFG, PIPEBUF, PIPEMAXP, and PIPEPERI
- ATREPM, ACLRM, SQCLR, and SQSET bits in PIPEXCTR
- Each bit in PIPEXTRE and PIPEXTRN

When changing these bits from the state where USB communication is enabled (PID = BUF), follow the steps below.

1. Generate a pipe control register bit change request.
2. Change the PID bits for the pipe to NAK.
3. Wait until the PBUSY bit for the pipe is cleared to 0.
4. Change the bits in the pipe control registers.

The following bits in the pipe control registers can be modified only for pipe information that is not set in any of the CURPIPE bits in CFIFOSEL, D0FIFOSEL, D1FIFOSEL, D2FIFOSEL and D3FIFOSEL.

Bits/registers that cannot be modified while the CURPIPE bits in FIFO-PORT are being set

- Each bit in DCPCFG and DCPMAXP
- Each bit in PIPECFG, PIPEBUF, PIPEMAXP, and PIPEPERI

Before changing the pipe information, set the CURPIPE bits to a pipe other than that to be changed. For the DCP, clear the buffer by the BCLR bit after modifying the pipe information.

### (2) Transfer Type

Specify the transfer type of each pipe by the TYPE bits in PIPECFG as follows:

- DCP: Setting is not required (fixed to control transfer).
- Pipes 1, 2: Set bulk transfer or isochronous transfer.
- Pipes 3 to 5, B to F: Set bulk transfer.
- Pipes 6 to 8 Set interrupt transfer.
- Pipes 9 to A: Set bulk transfer or interrupt transfer.

### (3) Endpoint Number

Specify the endpoint number of each pipe by the EPNUM bits in PIPEPCFG. The endpoint number of the DCP is always 0. For other pipes, endpoint 1 to endpoint 15 are selectable.

- DCP: Setting is not required (fixed to endpoint 0).
- Pipes 1 to F Set an endpoint number by selecting a number 1 to 15.  
However, set an endpoint number so that combinations of the DIR bit and the EPNUM bits do not overlap.

### (4) Maximum Packet Size

Specify the maximum packet size of each pipe by the MXPS bits in DCPMAXP and PIPEMAXP. For the DCP and pipes 1 to 5, 9 to F, any of the maximum packet sizes defined in the USB Specification can be set. For pipes 6 to 8a maximum packet size up to 64 bytes can be set. Specify a maximum packet size as follows before starting transfer (PID = BUF):

- DCP: Set 64 for high-speed operation.
- DCP: Set 8, 16, 32, or 64 for full-speed operation.
- Pipes 1 to 5, 9 to F: Set 512 for high-speed bulk transfer.
- Pipes 1 to 5, 9 to F: Set 8, 16, 32, or 64 for full-speed bulk transfer.
- Pipes 1, 2: Set a value from 1 to 1024 for high-speed isochronous transfer.
- Pipes 1, 2: Set a value from 1 to 1023 for full-speed isochronous transfer.
- Pipes 6 to 8 Set a value from 1 to 64.
- Pipes 9 to A: Set a value from 1 to 64 for interrupt transfer.

High Bandwidth in interrupt and isochronous transfers is not supported.

### (5) Transaction Counter (Pipes 1 to 5, 9 to F: Read Direction)

When the specified number of transactions with data packet in the receive direction are completed, this module recognizes this as a transfer end. The transaction counter works when the pipe selected for the D0FIFOSEL, D1FIFOSEL, D2FIFOSEL and D3FIFOSEL ports is set for the data read (from the buffer memory) direction. The transaction counter is provided with the TRNCNT register to specify the number of transactions and the current counter to count transactions internally. When the current counter reaches the specified value, the buffer memory becomes ready for reading. The current counter of the transaction counter function can be initialized by the TRCLR bit to count transactions again from the beginning. The TRNCNT read data varies depending on the TRENb setting.

- TRENb = 0: The set transaction counter value is read.
- TRENb = 1: The internally counted current counter value is read.
- Change the CURPIPE bits according to the following.
- Do not change the CURPIPE bits until the transaction for the specified pipe finishes.
- Change the CURPIPE bits when the current counter is cleared.
- Control the TRCLR bit according to the following.
- Do not clear the current counter during transaction count and PID = BUF.
- Do not clear the current counter while data is remaining in the buffer.

## (6) Response PID

Specify the response PID for each pipe by the PID bits in DCPCTR and PIPEnCTR.

This module operates as follows according to the response PID setting.

The response PID specifies a response to transactions from the host.

- NAK setting: NAK is always sent in response to a transaction.
- BUF setting: A response is sent to a transaction according to the buffer memory status.
- STALL setting: STALL is always sent in response to a transaction.

Note: This module always sends ACK in response to a setup transaction irrespective of the PID setting, and stores a USB request in the register.

This module modifies the PID bits in the following cases depending on transaction results.

- When the response PID is set by the hardware
  - NAK setting: This module sets PID to NAK in the following cases and always sends NAK in response to a transaction.
- When a SETUP token is successfully received (DCP only)
- When the SHTNAK bit in PIPECFG is set to 1 in a bulk transfer and the transaction counter stops counting or this module receives a short packet
  - BUF setting: This module does not set the PID bits to BUF.
  - STALL setting: This module sets PID to STALL in the following cases and always sends STALL in response to a transaction.
- When a maximum packet size exceeded error is detected in a receive data packet
- When a control transfer sequence error is detected (DCP only)

## (7) Data PID Sequence Bit

When data is successfully transferred in the control transfer data stage, bulk transfer, or interrupt transfer, this module automatically toggles the data PID sequence bit. The sequence bit of the data PID transmitted next can be monitored by the SQMON bit in DCPCTR and PIPEnCTR. In a data transmission period, the sequence bit switches at the ACK handshake receive timing. In a data reception period, the sequence bit switches at the ACK handshake transmit timing. The data PID sequence bit can also be changed by the SQCLR and SQSET bits in DCPCTR and PIPEnCTR.

In control transfers when the function controller function is selected, this module automatically sets the sequence bit during a stage transition. DATA0 is indicated at the end of the setup stage, and DATA1 is used for responses in the status stage. This does not require the setting of the sequence bit by the software.

Note that, the software must also set the data PID sequence bit when sending or receiving a ClearFeature request.

The sequence bit cannot be modified by the SQSET bit for isochronous transfer pipes.



### (8) Response PID = NAK Function

This module has a function to disable the pipe operation (Response PID = NAK) at the last data packet receive timing in a transfer (this module automatically identifies the last data packet receive timing at the short packet receive timing or using the transaction counter) by setting the SHTNAK bit in PIPECFG to 1.

This function allows reception of data packets in transfer units when the buffer memory is used as a double buffer. Furthermore, when the pipe operation is disabled, the software must set the response PID to BUF to enable the pipe operation.

This function is available only for bulk transfers.

### (9) Auto-Response Mode

When the ATREPM bit in PIPEnCTR is set to 1 in a bulk transfer pipe (pipes 1 to 5, 9 to F), this module enters auto-response mode: OUT-NAK mode in OUT transfers (DIR = 0) or null auto-response mode in IN transfers (DIR = 1).

#### 1. OUT-NAK mode

When the ATREPM bit is set to 1 in a bulk OUT transfer pipe, this module sends NAK in response to an OUT token or PING token and outputs an NRDY interrupt. To change response mode from normal mode to OUT-NAK mode, specify OUT-NAK mode with the pipe operation disabled (Response PID = NAK), and then enable the pipe operation (Response PID = BUF). After that, OUT-NAK mode is enabled. However, if an OUT token is received immediately before the pipe operation is disabled, this module receives the data of the token correctly and sends ACK to the host.

To change response mode from OUT-NAK mode to normal mode, reset OUT-NAK mode with the pipe operation disabled (Response PID = NAK), and then enable the pipe operation (Response PID = BUF). In normal mode, this module can receive OUT data and sends ACK in response to a PING token when the buffer is ready for receiving.

#### 2. Null auto-response mode

When the ATREPM bit is set to 1 in a bulk IN transfer pipe, this module continues to send Zero-Length packets. To change response mode from normal mode to null auto-response mode, specify null auto-response mode with the pipe operation disabled (Response PID = NAK), and then enable the pipe operation (Response PID = BUF). After that, null auto-response mode is enabled. However, specify null auto-response mode while the buffer is empty. Verify this by checking INBUFM = 0. Since INBUFM = 1 indicates that the buffer contains data, clear the buffer by setting the ACLRM bit. Do not write data to the buffer from the FIFO port during setting to null auto-response mode.

To change response mode from null auto-response mode to normal mode, delay the pipe operation disabled state (Response PID = NAK) for a time period for sending a Zero-Length packet (full-speed: 10  $\mu$ s, high-speed: 3  $\mu$ s), and then reset null auto-response mode. Normal mode allows writing from the FIFO port, and also allows sending packets to the host by enabling the pipe operation (Response PID = BUF).

### 52.3.4 FIFO Buffer Memory

#### (1) Allocating FIFO Buffer Memory

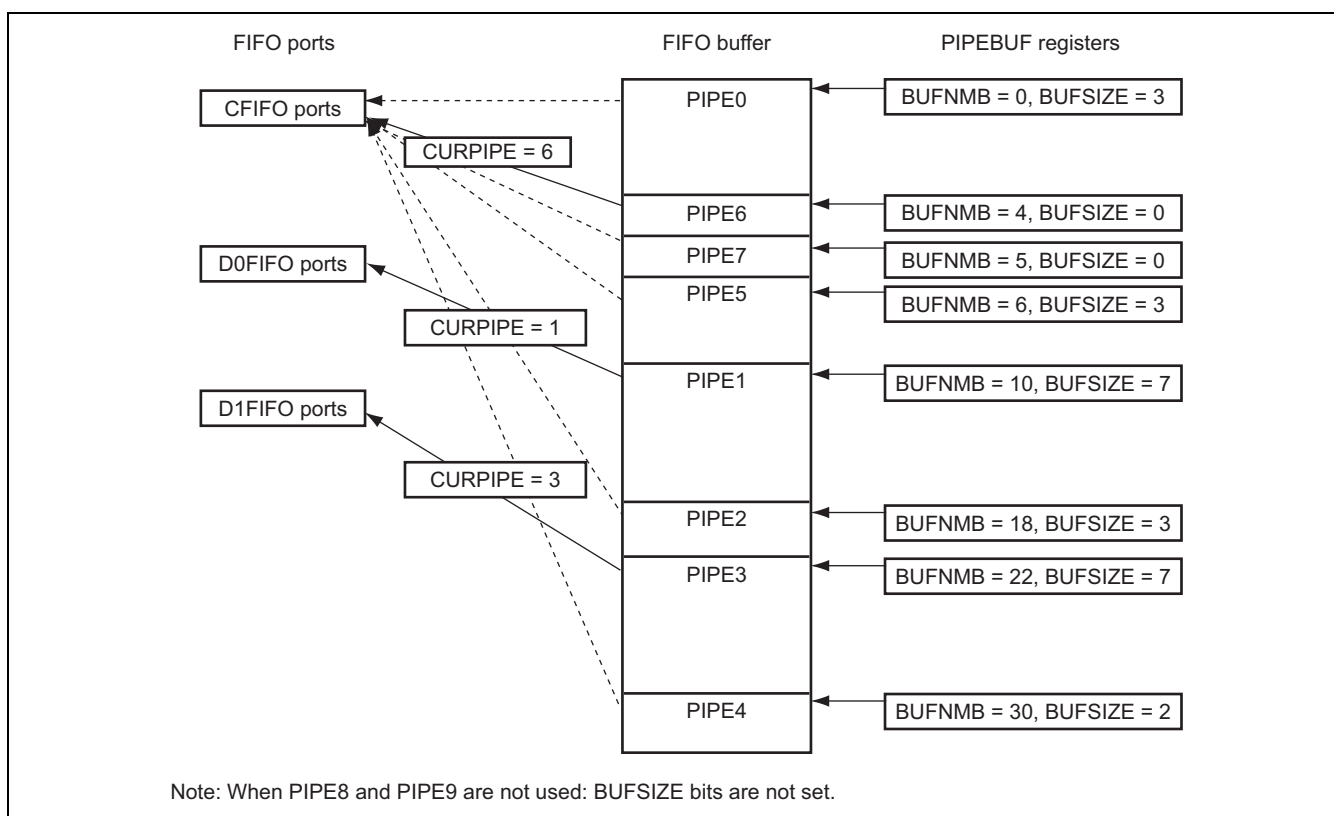
Figure 52.9 shows an example of the FIFO buffer memory map of this module. The FIFO buffer memory is an area shared by the CPU and this module. There are two FIFO buffer memory states where the access right is given to the system (CPU) or to this module (SIE).

The FIFO buffer memory provides independent areas for each pipe. A memory area is set with the block start number and the number of blocks (BUFNMB and BUFSIZE bits in PIPEBUF) in 64-byte units as one block.

When continuous transfer mode is selected by the CNTMD bit in PIPECFG, be sure to set the BUFSIZE bits to a value in integral multiples of the maximum packet size. When double buffer is selected by the DBLB bit in PIPECFG, two sides of the memory area specified by the BUFSIZE bits in PIPEBUF are provided for the same pipe.

Furthermore, three FIFO ports are used for accesses (data read/write) to the buffer memory. The number of a pipe to be allocated to the FIFO ports is specified by the CURPIPE bits in CFIFOSEL and DnFIFOSEL.

The buffer status of each pipe can be monitored by the BSTS and INBUFM bits in DCPCTR and PIPECTR. The access right to the FIFO ports can be checked by the FRDY bit in CFIFOCTR and DnFIFOCTR.



**Figure 52.9 Example of Buffer Memory Map**

- Buffer status

Tables 52.14 and 52.15 show the buffer memory status of this module. The buffer memory status can be monitored by the BSTS bit in DCPCTR and the INBUFM bit in PIPECTR. The buffer memory access direction is specified by the DIR bit in PIPECFG or the ISEL bit in CFIFOSEL (when DCP is selected).

The INBUFM bit is valid only for pipes 1 to 5, 9 to F in the transmit direction.

When a transfer pipe in the transmit direction is set to double buffer, the BSTS bit is used to monitor the buffer status on the CPU side, and the INBUFM bit is used to monitor the buffer status on the SIE side. When data write to the FIFO port by the CPU (DMAC) takes time and buffer empty cannot be checked by the BEMP interrupt, the INBUFM bit is available to check completion of transmission.

**Table 52.14 Buffer Memory Status That Varies Depending on the BSTS Bit**

ISEL or DIR	BSTS	Buffer Memory Status
0 (receive direction)	0	No receive data in the buffer memory or data is being received. Data cannot be read from the FIFO port.
0 (receive direction)	1	Receive data in the buffer memory or a Zero-Length packet is received. Data can be read from the FIFO port. However, the buffer must be cleared because the FIFO port cannot be read when this module receives a Zero-Length packet.
1 (transmit direction)	0	Transmission of data is not completed. Data cannot be written to the FIFO port.
1 (transmit direction)	1	Transmission of data is completed. The CPU can write data to the buffer memory.

**Table 52.15 Buffer Memory Status That Varies Depending on the INBUFM Bit**

DIR	INBUFM	Buffer Memory Status
0 (receive direction)	Invalid	Invalid
1 (transmit direction)	0	Transmittable data is completely sent. No transmittable data is in the buffer memory.
1 (transmit direction)	1	Transmittable data is written from the FIFO port. The buffer memory contains transmittable data.

- FIFO buffer clear

Table 52.16 shows clearing of the FIFO buffer memory of this module. The buffer memory can be cleared by the BCLR, DCLRM, and ACLRM bits.

**Table 52.16 Buffer Clear**

Bit Name	BCLR	DCLRM	ACLRM
Register	CFIFOCTR DnFIFOCTR	DnFIFOSEL	PIPEnCTR
Function	Clears the buffer memory of the CPU.	Automatically clears the buffer memory after reading data of the specified pipe.	Automatically clears the buffer memory by ignoring all received packets.
Clearing method	Writing 1 to this bit clears the buffer memory.	1: This mode is enabled. 0: This mode is disabled.	1: This mode is enabled. 0: This mode is disabled.

- Buffer area

Table 52.17 shows a buffer memory map of this module. The buffer memory includes a dedicated areas reserved beforehand for pipes and user areas provided for user settings.

The buffer for DCP is a dedicated area commonly used in control read transfers and control write transfers.

Areas for pipes 6 to 8 are allocated respectively in advance. However, when none of pipes 6 to 9 is used, the areas are available for pipes 1 to 5, 9 to F as user areas.

Allocate different areas of the buffer memory to each pipe. Note that, when double buffer is specified, the size of an area is twice of the set value.

Do not set the buffer size to a value smaller than the maximum packet size.

**Table 52.17 Buffer Memory Map**

Buffer Memory Number	Buffer Size	Pipe Setting	Remarks
H'0	64 bytes	Fixed only for DCP	Single buffer
H'1 to H'3	—	Unavailable	—
H'4	64 bytes	Fixed only for pipe 6	Single buffer
H'5	64 bytes	Fixed only for pipe 7	Single buffer
H'6	64 bytes	Fixed only for pipe 8	Single buffer
H'7 to H'7F	Max. 7616 bytes	User area for pipes 1 to 5, 9 to F	Double buffer and continuous transfer can be set

- Buffer auto-clear mode function

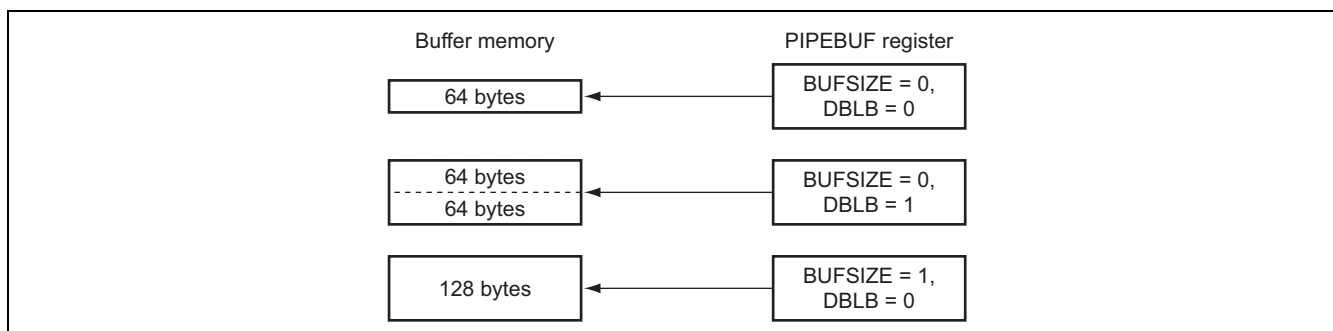
When the ACLRM bit PIPEnCTR is set to 1, this module discards all data packets received. However, when this module receives a data packet successfully, it sends ACK to the host controller. This function is available only for the buffer memory read direction.

Writing 1 and then 0 continuously to the ACLRM bit clears the buffer memory of the selected pipe irrespective of the access direction.

Take at least 100 ns between writing 1 and writing 0 for the sequence execution time of the hardware.

- Buffer memory specifications (single buffer/double buffer setting)

Single buffer or double buffer is selectable for pipes 1 to 5, 9 to F with the DBLB bit in PIPEnCFG. Double buffer is a function to provide two sides of the memory area specified by the BUFSIZE bits in PIPEBUF for the same pipe. Figure 52.10 shows an example of setting for the buffer memory of this module.



**Figure 52.10 Example of Buffer Memory Setting**

- Buffer memory operation (continuous transfer setting)

Continuous transfer mode or discontinuous transfer mode is selectable with the CNTMD bit in PIPEnCFG. This selection is enabled for pipes 1 to 5, 9 to F.

The continuous transfer mode function allows continuous transmission/reception of multiple transactions. When continuous transfer mode is selected, data up to the buffer size allocated to each pipe can be transferred without outputting an interrupt to the CPU.

In continuous transmission mode, data in the buffer is divided by the maximum packet size and is then transmitted. To send data less than the buffer size (a short packet or a packet with a size of integral multiples of the maximum packet size and less than the buffer size), set BVAL = 1 after writing transmit data to the buffer.

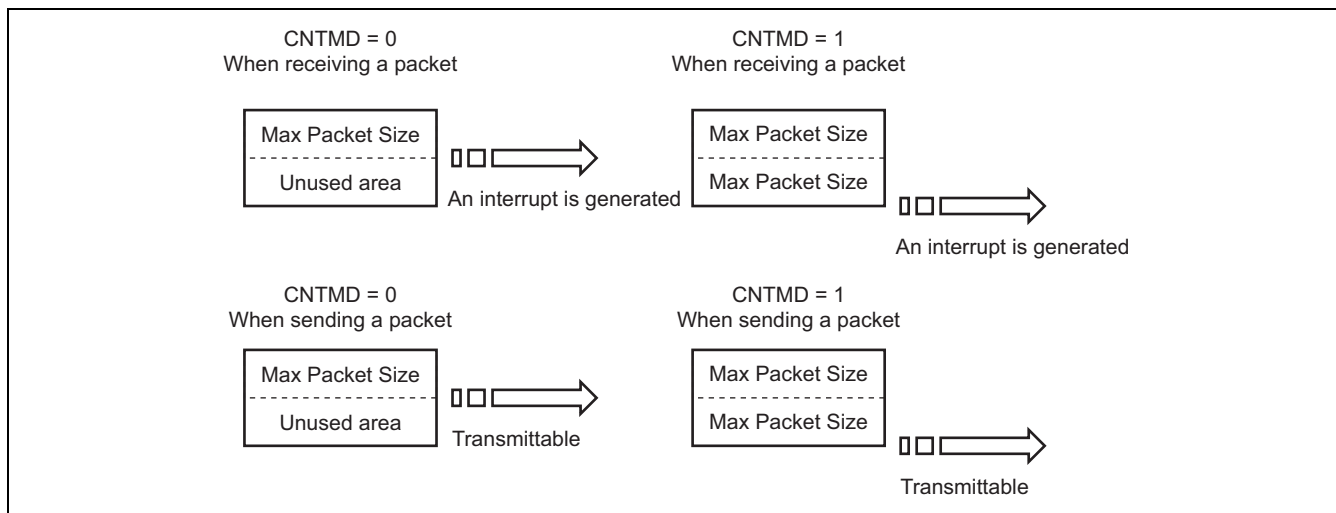
In continuous reception mode, no interrupt is generated until this module receives packets to the buffer size, the transaction count ends, or this module receives a short packet.

Table 52.18 shows the relationship between the CNTMD setting and determination of transmission/reception end of the FIFO buffer.

**Table 52.18 Relationship between CNTMD Setting and Determination of Transmission/Reception End of FIFO Buffer**

Transfer Mode	Determination of Buffer Readable State and Data Transmittable State
Discontinuous transfer (CNTMD = 0)	Conditions for FIFO buffer readable state when data receive direction is selected (DIR = 0): When this module receives one packet
	Conditions for FIFO buffer data transmittable state when data transmit direction is selected (DIR = 1): Any of the following cases: The software (or DMAC) writes data of the maximum packet size to the FIFO buffer. The software (or DMAC) writes data of a short packet (including 0 bytes) to the FIFO buffer, and then sets BVAL = 1.
Continuous transfer (CNTMD = 1)	Conditions for FIFO buffer readable state when data receive direction is selected (DIR = 0): When the bytes of data received in the FIFO buffer for the selected pipe equals the allocated bytes ((BUFSIZE + 1) × 64) When this module receives a short packet other than a Zero-Length packet When this module receives a Zero-Length packet when data is already stored in the FIFO buffer for the selected pipe When this module receives packets as large as the transaction counter value specified for the selected pipe by the software
	Conditions for FIFO buffer data transmittable state when data transmit direction is selected (DIR = 1): Any of the following cases: The volume of data written by the software (or DMAC) equals the size of one side of the FIFO buffer for the selected pipe. The software (or DMAC) writes data less than the size of one side of the FIFO buffer for the selected pipe to the FIFO buffer, and then sets BVAL = 1.

Figure 52.11 shows an example of buffer memory operation of this module.



**Figure 52.11 Example of Buffer Memory Operation**

## (2) FIFO Port Function

Table 52.19 lists the settings for the FIFO port functions of this module. During a data write access, when data up to buffer full (or up to the maximum packet size in discontinuous transfer) is written, the FIFO port automatically enters the data transmittable state. To make data less than buffer full (or the maximum packet size in discontinuous transfer) transmittable, set the BVAL bit in CFIFOCTR and DnFIFOCTR to 1 to set write end. For transmission of a Zero-Length packet, clear the buffer using the BCLR bit in these registers and then set the BVAL bit to 1.

During a data read access, when all data is read, the FIFO port automatically enters the new packet receivable state. However, when receiving a Zero-Length packet (DTLN = 0), no data can be read. Therefore, clear the buffer using the BCLR bit in these registers. The receive data length can be checked by the DTLN bits in CFIFOCTR and DnFIFOCTR.

**Table 52.19 FIFO Port Function Settings**

Register Name	Bit Name	Function	Remarks
CFIFOSEL	RCNT	Selects DTLN read mode.	
DnFIFOSEL	REW	Rewinds the buffer memory (reread/rewrite).	
	DCLRM	Reads and clears receive data of the specified pipe.	DnFIFO only
	DREQE	Enables DMA transfer.	DnFIFO only
	MBW	Specify FIFO port access bit width.	
	BIGEND	Selects FIFO port endian.	
	ISEL	Selects FIFO port access direction.	DCP only
	CURPIPE	Select the current pipe.	
CFIFOCTR	BVAL	Specifies buffer memory write end.	
DnFIFOCTR	BCLR	Clears the buffer memory of the CPU.	
	DTLN	Check receive data length.	

### (a) FIFO Port Selection

Table 52.20 shows pipes that can be selected in each FIFO port. Select a pipe to be accessed by the CURPIPE bits in CFIFOSEL and DnFIFOSEL. After selecting a pipe, confirm that the set CURPIPE value is read correctly, check FRDY = 1, and then make an access to the FIFO port. (If the previous pipe number is read, this controller is changing a pipe.)

Also select the bus width to be accessed by the MBW bits. The buffer memory access direction is specified by the DIR bit in PIPECFG. However, only the access direction of DCP is determined by the ISEL bit.

**Table 52.20 FIFO Port Access**

Pipe	Access	Available port
DCP	CPU access	CFIFO port register
Pipes 1 to F	CPU access	CFIFO port register
	DMA access	D0FIFO and D1FIFO port

### (b) REW Bit

The current access to a pipe can be suspended temporarily, and it is also possible to make an access to another pipe to continue the ongoing pipe processing. This processing is allowed by using the REW bit in CFIFOSEL and DnFIFOSEL.

When the REW bit is set to 1 together with the CURPIPE bits in CFIFOSEL and DnFIFOSEL and a pipe is selected, the reading or writing pointer of the buffer memory is reset, which allows reading or writing data from the first byte. Furthermore, when a pipe is selected with the REW bit set to 0, data can be read or written following the data at the previous selection without resetting the reading or writing pointer of the buffer memory.

To make accesses to the FIFO port, select a pipe and check  $FRDY = 1$ .

### (3) DMA Transfer (Dedicated DMA Interface)

#### (a) Overview of DMA Transfer

The FIFO port can be accessed by the DMAC for pipes 1 to F. When the buffer of a pipe specified for DMA transfer becomes accessible, this module outputs a DMA transfer request.

Specify the data transfer unit to the FIFO port by the MBW bits in  $DnFIFOSEL$ , and select a pipe used for DMA transfer by the CURPIPE bits in  $DnFIFOSEL$ . Do not change the selected pipe during a DMA transfer.

#### (b) DMA Transfer End Auto-Recognition

This module can terminate writing of data by DMA transfer to the FIFO buffer by controlling the DMA transfer end signal input. After sampling the transfer end signal, this module drives the buffer memory into the transmittable state (same state as  $BVAL = 1$ ).

#### (c) DnFIFO Auto-Clear Mode (D0FIFO, D1FIFO, D2FIFO and D3FIFO Port Read Direction)

By setting the DCLRM bit in  $DnFIFOSEL$  to 1, this module automatically clears the buffer memory for the selected pipe upon completion of data read from the buffer memory.

Table 52.21 shows the relationship between packet reception and buffer memory clear by the software. As shown in the table, buffer clearing conditions vary with the BFRE setting. However, in any state that needs clearing, using the DCLRM bit makes buffer clearing by the software unnecessary. Thus DMA transfer is enabled without requiring any software control.

- This function is available only for the buffer memory read direction.

**Table 52.21 Relationship between Packet Reception and Buffer Memory Clear by the Software**

Buffer Status When Receiving a Packet	Register Setting			
	DCLRM = 0		DCLRM = 1	
	BFRE = 0	BFRE = 1	BFRE = 0	BFRE = 1
Buffer full	Clearing not required	Clearing not required	Clearing not required	Clearing not required
Zero-Length packet reception	Clearing required	Clearing required	Clearing not required	Clearing not required
Normal short packet reception	Clearing not required	Clearing required	Clearing not required	Clearing not required
Transaction count end	Clearing not required	Clearing required	Clearing not required	Clearing not required

### 52.3.5 Control Transfer (DCP)

The default control pipe (DCP) is used for data transfer in the control transfer data stage. The buffer memory for the DCP is a 256-byte single buffer of a fixed area used for both control read and control write. The buffer memory can be accessed only by the CFIFO ports.

#### (1) Setup Stage

1. This module always sends ACK in response to a normal setup packet to this module. The following describes the operation of this module in the setup stage.

When this module receives a new setup packet, this module sets the following bits.

- The VALID bit in INTSTS0 to 1
  - The PID bits in DCPCTR to NAK
  - The CCPL bit in DCPCTR to 0
2. When this module receives a data packet following a setup packet, this module stores the USB request parameters in USBREQ, USBVAL, USBINDEX, and USBLENG.

Be sure to process responses to control transfers while VALID = 0. The PID bits cannot be set to BUF when VALID = 1, and therefore the data stage cannot be completed.

With the VALID bit function, this module can suspend the ongoing request processing if this module receives a new USB request during a control transfer, and send a response to the latest request.

This module also determines the direction bit (bit 8 of bmRequestType) of the received USB request and the request data length (wLength), identifies a control read transfer, control write transfer, and control write no-data transfer, and controls stage transitions. For an incorrect sequence, a sequence error of the control transfer stage transition interrupt occurs, and the error is reported to the software. For the stage control of this module, see Figure 52.7.

#### (2) Data Stage

Transfer data in response to the received USB request using the DCP. Before making an access to the DCP buffer memory, specify the access direction by the ISEL bit in CFIFOSEL.

When the transfer data size is larger than the DCP buffer memory size, use a BRDY interrupt for control write transfers and a BEMP interrupt for control read transfers.

In the high-speed control write transfer, this module sends responses using the NYET handshake according to the buffer memory status.

#### (3) Status Stage

Setting the CCPL bit to 1 with the PID bits in DCPCTR set to BUF finishes a control transfer.

After these settings, this module executes the status stage as follows according to the data transfer direction determined in the setup stage:

- Control read transfer  
This module sends a Zero-Length packet and receives an ACK response from the USB host.
- Control write transfer, no-data control transfer  
This module receives a Zero-Length packet from the USB host and sends an ACK response.



#### (4) Control Transfer Auto-Response Function

This module automatically responds to a correct SET\_ADDRESS request. If any of the following errors occurs in the SET\_ADDRESS request, the software must respond to the error.

- Other than control read transfer: bmRequestType ≠ H'00
- Request errors: wIndex ≠ H'00
- Other than no-data control transfer: wLength ≠ H'00
- Request errors: wValue > H'7F
- Control transfer of device state errors: DVSQ = B'011 (configured)

All requests other than SET\_ADDRESS require a response made by the software.

#### 52.3.6 Bulk Transfer (Pipes 1 to 5, 9 to F)

The buffer memory usage (single buffer/double buffer setting or continuous/discontinuous transfer mode setting) can be selected for bulk transfers. The buffer memory size can be set to up to 2 Kbytes. This module manages the buffer memory status and automatically responds to a PING packet and an NYET handshake.

##### (1) NYET Handshake Control

Table 52.22 lists NYET handshake responses of this module. This module sends a NYET response under the following conditions. However, when this module receives a short packet, this module sends ACK instead of NYET. The same is true of the control write transfer data stage.

**Table 52.22 NYET Handshake Responses**

Setting of PID Bits in DCPCTR	Buffer Memory Status	Token	Response	Remarks
NAK/STALL	—	SETUP	ACK	—
	—	IN/OUT/PING	NAK/STALL	—
BUF	—	SETUP	ACK	—
	RCV-BRDY1	OUT/PING	ACK	Receives a data packet when receiving an OUT token.
	RCV-BRDY2	OUT	NYET	Receives a data packet. Sends a “reception disable” response.
	RCV-BRDY2	OUT (Short)	ACK	Receives a data packet. Sends a “reception enable” response.
	RCV-BRDY2	PING	ACK	Sends a “reception enable” response.
	RCV-NRDY	OUT/PING	NAK	Sends a “reception disable” response.
	TRN-BRDY	IN	DATA0/1	Sends a data packet.
TRN-NRDY	IN	NAK	TRN-NRDY	

[Legend]

RCV-BRDY1: The buffer memory has available space for two packets or more when receiving an OUT or PING token.

RCV-BRDY2: The buffer memory has available space for only one packet when receiving an OUT token.

RCV-NRDY: The buffer memory is occupied when receiving an PING token.

TRN-BRDY: The buffer memory contains transmit data when receiving an IN token.

TRN-NRDY: The buffer memory contains no transmit data when receiving an IN token.

### 52.3.7 Interrupt Transfer (Pipes 6 to A)

This module performs interrupt transfer following the cycles controlled by the host controller. In interrupt transfers, this module ignores PING packets (no response), sends no NYET handshake, and sends ACK, NAK, and STALL responses.

This module does not support the High-Bandwidth interrupt transfer.

### 52.3.8 Isochronous Transfer (Pipes 1, 2)

This module is provided with the following functions for isochronous transfers.

- Reporting isochronous transfer error information
- Interval counter (IITV bits)
- Isochronous IN transfer data setup control (IDLY function)
- Isochronous IN transfer buffer flush function (IFIS bit)

This module does not support the isochronous High-Bandwidth transfer.

#### (1) Isochronous Transfer Error Detection

This module is provided with a function to detect the following error information so that the software can manage isochronous transfer errors. Tables 52.23 and 52.24 show the error detection priority of this module and interrupts generated as a result of error detection.

1. PID error
  - When the PID in a receive packet is invalid
2. CRC error, bit stuffing error
  - When a CRC error is found in a receive packet or bit stuffing is invalid
3. Maximum packet size exceeded error
  - When the data size of a receive packet is over the maximum packet size setting
4. Overrun/underrun error
  - When the buffer memory contains no data when this module receives an IN token in the IN direction (transmission) transfer
  - When the buffer memory is occupied when this module receives an OUT token in the OUT direction (reception) transfer
5. Interval error
  - This module generates an interval error in the following cases.
  - When no IN token can be received in interval frames in the isochronous IN transfer
  - When this module receives an OUT token other than interval frames in the isochronous OUT transfer

**Table 52.23 Error Detection when Receiving Tokens**

Priority for Error Detection	Error	Interrupt and Status
1	PID error	This module generates no interrupt (ignores as a damaged packet).
2	CRC error, bit stuffing error	This module generates no interrupt (ignores as a damaged packet).
3	Overrun error, underrun error	This module generates an NRDY interrupt and sets the OVRN bit. This module sends a Zero-Length packet in response to the IN token. This module receives no data packet in response to the OUT token.
4	Interval error	This module generates an NRDY interrupt.

**Table 52.24 Error Detection when Receiving Data Packets**

Priority for Error Detection	Error	Interrupt and Status
1	PID error	This module generates no interrupt (ignores as a damaged packet).
2	CRC error, bit stuffing error	This module generates an NRDY interrupt and sets the CRCE bit.
3	Maximum packet size exceeded error	This module generates a BEMP interrupt and sets the PID bits to STALL.

**(2) DATA-PID**

This module does not support the High-Bandwidth transfer. The following lists responses to received PIDs when the function controller function is selected.

1. IN direction
  - DATA0: Sent correctly as the PID of data packet.
  - DATA1: Not sent
  - DATA2: Not sent
  - mData: Not sent
2. OUT direction (full-speed operation)
  - DATA0: Received correctly as the PID of a data packet.
  - DATA1: Received correctly as the PID of a data packet.
  - DATA2: The packet is ignored.
  - mData: The packet is ignored.
3. OUT direction (high-speed operation)
  - DATA0: Received correctly as the PID of a data packet.
  - DATA1: Received correctly as the PID of a data packet.
  - DATA2: Received correctly as the PID of a data packet.
  - mData: Received correctly as the PID of a data packet.

### (3) Interval Counter

Intervals for isochronous transfers can be set by the IITV bits in PIPEPERI. The functions shown in Table 52.25 are made available with the interval counter.

**Table 52.25 Interval Counter Functions**

Transfer Direction	Function	Detection Conditions
IN	Transmit buffer flush	No IN token can be successfully received in the interval frame during the isochronous IN transfer.
OUT	Reporting reception of no token	No OUT token can be successfully received in the interval frame during the isochronous OUT transfer.

Since the interval counter is counted upon receiving an SOF or using the interpolated SOF, the isochronism can be maintained even if the SOF is damaged. The specifiable frame interval is  $2^{\text{IITV}}$  frames or  $2^{\text{IITV}}$   $\mu$  frames.

#### (a) Counter initialization

This module initializes the interval counter as follows:

- Power-on reset  
The IITV bits are initialized.
- Initializing buffer memory by ACLRM  
The IITV bits are not initialized but the interval counter is initialized. Clearing the ACLRM bit to 0 causes the counter to start counting from the set IITV value.

After the interval counter is initialized, the interval counter starts counting in either of the following cases after a packet is correctly transferred.

1. When this module receives an SOF after sending data in response to the IN token with PID = BUF
2. When this module receives an SOF after receiving the OUT token data with PID = BUF

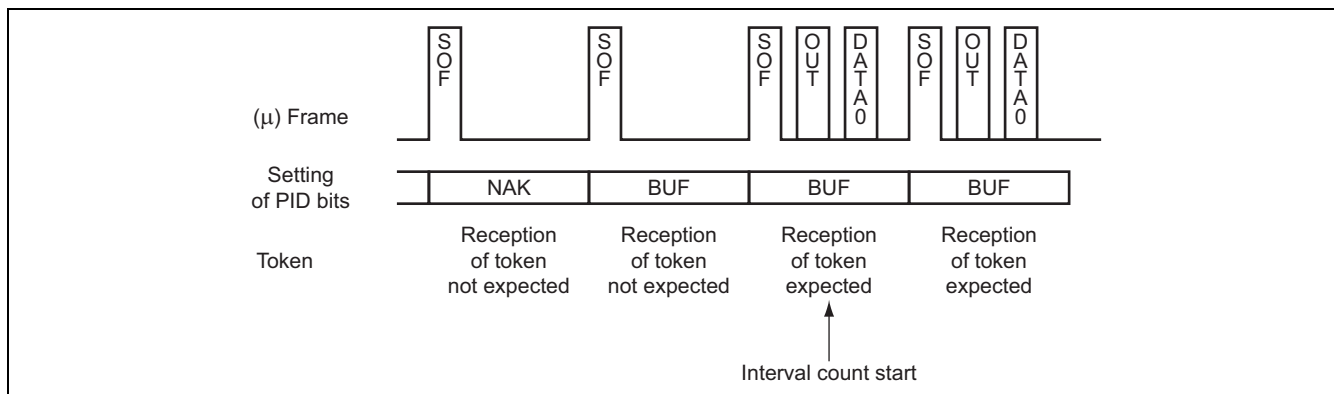
The interval counter is not initialized under the following conditions.

1. When PID = NAK or STALL  
The interval timer does not stop. Try to execute the transaction in the next interval.
2. USB bus reset and USB suspended  
The IITV bits are not initialized. When this module receives an SOF, the interval counter starts counting from the value before receiving the SOF.

#### (b) Interval count and transfer control

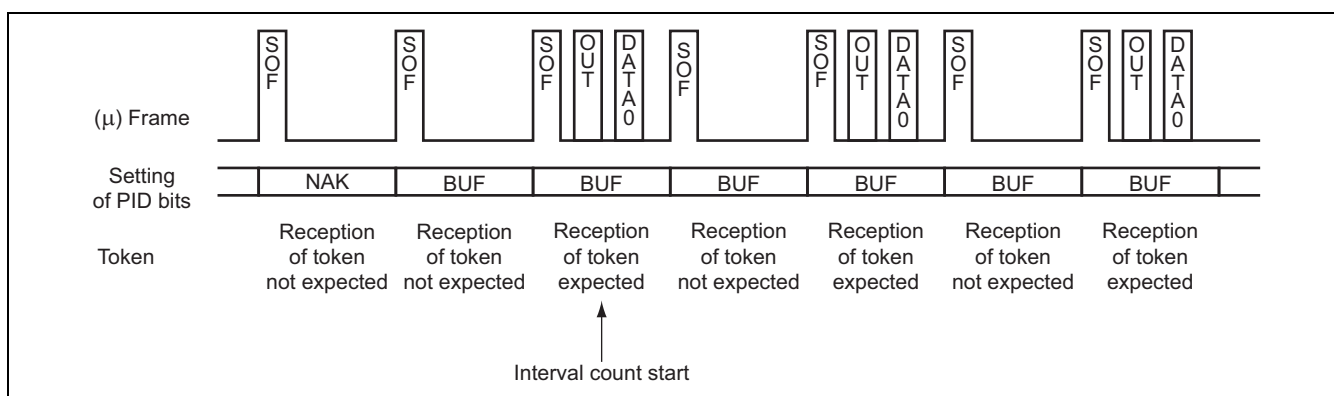
1. When the selected pipe is Isochronous-OUT transfer pipe  
When this module receives no data packet in ( $\mu$ ) frames at the intervals specified by the IITV bits, this controller generates an NRDY interrupt.  
When this module cannot receive data due to a CRC error in the data packet, FIFO buffer full, or other reasons, this module also generates an NRDY interrupt.  
An NRDY interrupt is generated at the SOF packet receive timing. Even if the SOF packet is damaged, this module generates an NRDY interrupt at the SOF packet receive timing using the internal interpolation function.  
When  $\text{IITV} \neq 0$ , however, this module generates an NRDY interrupt at the SOF packet receive timing in each interval after the interval count starts.  
When PID = NAK is set by the software after the interval timer is activated, this module generates no NRDY interrupt even when this module receives an SOF packet.  
The interval count start conditions vary with the set IITV value.

— When IITV = 0: The interval count starts from the next ( $\mu$ ) frame where the PID bits for the selected pipe is changed to BUF.



**Figure 52.12 ( $\mu$ ) Frames and Expectation of Receiving a Token when IITV = 0**

— When IITV  $\neq$  0: The interval count starts from the time when this module successfully receives the first data packet after the PID bits for the selected pipe is changed to BUF.



**Figure 52.13 ( $\mu$ ) Frames and Expectation of Receiving a Token when IITV  $\neq$  0**

2. When the selected pipe is Isochronous-IN transfer pipe

Use the selected pipe by combining with the setting of IFIS = 1. When IFIS = 0, this module sends data packets in response to received tokens irrespective of the IITV value.

When this module receives no IN-Token in ( $\mu$ ) frames at the intervals specified by the IITV bits with transmittable data stored in the FIFO buffer with IFIS = 1, this module clears the FIFO buffer.

When this module cannot receive data due to a CRC error or another bus error in the IN-Token, this module also clears the FIFO buffer.

The FIFO buffer is cleared at the SOF packet receive timing. Even if the SOF packet is damaged, this module clears the FIFO buffer at the SOF packet receive timing using the internal interpolation function.

The interval count start conditions vary with the set IITV value (same as Isochronous-OUT transfer).

When the function controller function is selected, the interval count start conditions are as follows:

- When this module is reset by the hardware (The set IITV value is also cleared to 0.)
- When ACLRM is set to 1 by the software
- When this module detects a USB reset

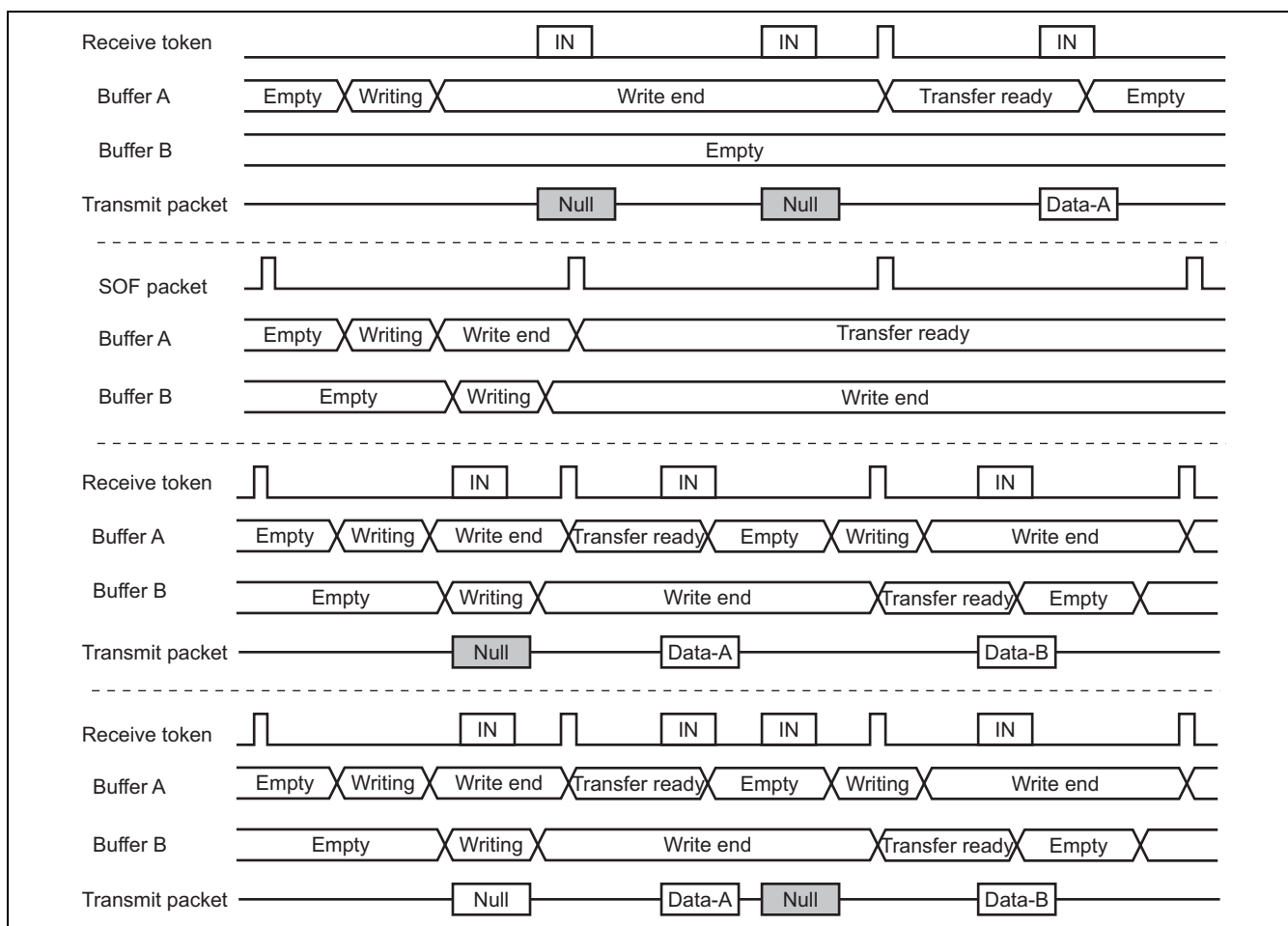
**(4) Transmit Data Setup in Isochronous Transfer**

In isochronous data transmission is selected, this module can send a data packet in the next frame after this module detects an SOF packet after writing data to the buffer. This function is referred to as the isochronous transfer transmit data setup function. With this function, the frame that started data transmission can be identified.

When the buffer memory is used as a double buffer, even if writing data to both buffers is completed, only one side that finished writing earlier becomes transferable. For this reason, even if multiple IN tokens are received in the same frame, only one packet of the buffer memory is sent.

When the buffer memory is ready for transmission in the IN token reception cycle, this module sends data and an ACK response. However, when the buffer memory is not ready for transmission, this module sends a Zero-Length packet and generates an underrun error.

Figure 52.14 shows an example of transmission using the isochronous transfer transmit data setup function of this module when IITV = 0 (each frame). Transmission of a Zero-Length packet is indicated as hatched “Null” in the figure.



**Figure 52.14 Example of Transmit Data Setup Function**

### (5) Transmit Buffer Flush in Isochronous Transfer

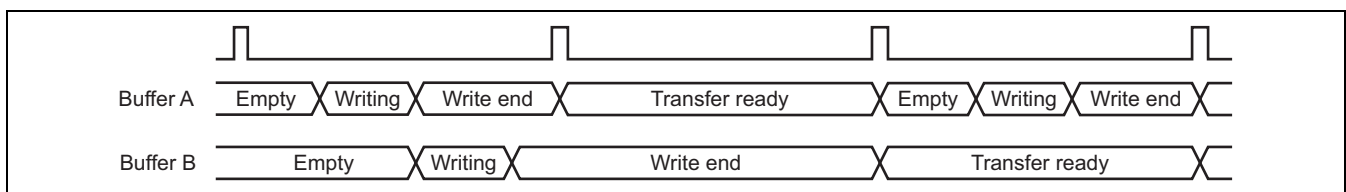
In isochronous data transmission is selected, this module receives no IN token in the interval frame. When this module receives the SOF or  $\mu$  SOF packet of the next frame, this module regards the IN token as damaged and clears the buffer that is ready for transmission to make it writable.

At this time, when the buffer memory is used as a double buffer and writing data to both buffers is completed, this module regards the discarded buffer memory data as transmitted in the same interval frame, and drives the buffer memory that is not discarded due to the reception of an SOF or  $\mu$  SOF packet into the transmission ready state.

The buffer flush function activation timing varies depending on the IITV value.

- When IITV = 0  
This module activates the buffer flush function from the next frame after the pipe is enabled.
- When IITV  $\neq$  0  
This module activates the buffer flush function from the first normal transaction.

Figure 52.15 shows an example of the buffer flush function of this module. For tokens before the interval frame (outside the specified interval), however, this module sends the data stored in the buffer according to the data setup state or sends a Zero-Length packet as an underrun error.



**Figure 52.15 Example of Buffer Flush Function**

Figure 52.16 shows an example of an interval error of this module. Interval errors are the following five. An interval error occurs at timing [1] in the figure, and the buffer flush function is activated.

When an interval error occurs, the buffer flush function is activated in the IN transfer and an NRDY interrupt occurs in the OUT transfer. Discriminate an NRDY interrupt (including a receive packet error) from an overrun error with the OVRN bit.

This module sends a response to the hatched tokens in the figure according to the buffer memory status.

1. IN direction
  - When the buffer is ready to transmit data, this module sends the data and an ACK response.
  - When the buffer is not ready to transmit data, this module sends a Zero-Length packet and generates an underrun error.
2. OUT direction
  - When the buffer is ready to receive data, this module receives data and sends an ACK response.
  - When the buffer is not ready to receive data, this module discards the data and generates an overrun error.

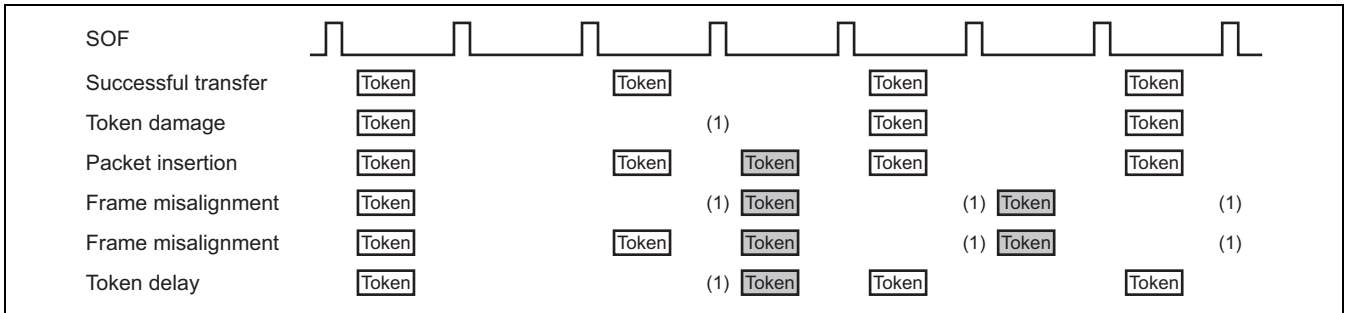


Figure 52.16 Example of Interval Error when IITV = 1



### 52.3.9 SOF Interpolation Function

In case this module cannot receive SOF packets at intervals of 1 ms (full-speed operation) or 125  $\mu$ s (high-speed operation) due to damage or missing of SOF packets, this module interpolates the SOF. The SOF interpolation starts functioning when SYSCFG.USBE = 1 and at the SOF packet receive timing. Furthermore, the interpolation function is initialized in the following cases.

- Power-on reset
- USB bus reset
- When the suspended state is detected

The SOF interpolation functions with the following specifications.

- The frame intervals (125  $\mu$ s or 1 ms) conform to the result of the reset handshake protocol.
- The SOF interpolation does not function until this module receives an SOF packet.
- After receiving the first SOF packet, 125  $\mu$ s or 1 ms is counted by the internal 48-MHz clock to interpolate the SOF.
- After receiving the second SOF packet or a following packet, the SOF is interpolated using the previous receive intervals.
- The SOF interpolation does not function in the suspended state and during a USB bus reset.  
(When this module enters the suspended state in high-speed operation, the SOF interpolation continues for 3 ms from the final packet.)

This module activates the following functions based on the reception of SOF packets. When one or more SOF packets are lost, normal operation can be continued to perform the SOF interpolation.

- Updating frame numbers and  $\mu$  frame numbers
- SOFR interrupt timing and  $\mu$  SOF lock
- Isochronous transfer interval count

When one or more SOF packets are lost in full-speed operation, the FRNM bits in FRMNUM are not updated. When one or more  $\mu$  SOF packets are lost in high-speed operation, the FRNM bits are updated. However, when a  $\mu$  SOF packet with UFRNM = B'000 is lost, the FRNM bits are not updated even if following  $\mu$  SOF packets with UFRNM  $\neq$  B'000 are successfully received.

## 52.4 Guidelines for Designing USB2.0 Hi-Speed Boards

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

### 52.4.1 USB Transmission Line

The USB transmission line indicates the pattern that connects the USB connector and the USB transceiver with built-in this LSI.

The USB2.0 has three communication modes: Hi-Speed, Full-Speed and Low-Speed modes. The transmission speed in the Hi-Speed mode is 480 Mbps. Therefore, the USB transmission line must be designed as a high-frequency circuit. Impedance control is required for the USB transmission line.

- The characteristic impedance required for the USB Hi-Speed transmission line is differential impedance  $90\ \Omega$  ( $\pm 15\%$ ).
- The pattern width and pattern pitch for impedance control vary depending on the board thickness, material and layer configuration. For details, consult the board manufacturer.
- A maximum delay of 1 ns is allowed from the USB connector to this LSI. Therefore it is recommended that the pattern length from the USB device to the USB connector is less than 50 mm and the difference between the pattern lengths for D+ and D- is less than 2.5 mm for a generic PCB.
- The lower layer of the USB transmission line must be a solid ground plane. The ground must be wider than the USB transmission line by 2 mm or more. The power supply for a solid ground plane is DG33.
- Do not allocate other signal lines near to the USB transmission line. In particular, lines carrying widely fluctuating signals, such as clock and data bus lines, must be assigned far from the USB transmission line. Furthermore, layout of the USB transmission lines must be such that they do not cross with other signal lines.
- Locate the USB transmission line on the same layer without passing it through a through-hole. Do not create stubs.
- Place the USB transmission lines so that they are equally spaced from each other.
- Locate the USB transmission line as far as possible from the oscillator, power supply circuit, and other I/O connectors.
- Try to avoid bending the USB transmission line as far as possible. If it is absolutely necessary to bend it, do not bend it at acute or right angles. Bend it moderately, at not more than 45 degrees, or bend it into an arc.
- It is recommended to guard ring the clock, reset, read, write and chip select signals with grounds.

When a resistance is connected to the USB transmission line, locate it near to the USB transmission line. The connecting wire must be as short as possible.

### 52.4.2 Power Supply and Ground Pattern

Analog power supply: AVDD (1.8 V)

Digital power supply: DV181 (1.8 V), DV331 (3.3 V)

Analog ground: PVSS, AVSS

Digital ground: GND1, GND2

- It is recommended to separate power supplies and ground patterns into digital and analog.
- Connect the power supplies and grounds firmly on wide areas.
- Tantalum solid electrolytic capacitors or ceramic capacitors having excellent high-frequency characteristics are recommended as capacitors for power supplies.
- Aluminum electrolytic capacitors affect the jitter value during measurement of EYE diagram. Use the capacitors after adequately designing and testing them.
- It is recommended to place decoupling capacitors with values of 0.1  $\mu\text{F}$ , 0.01  $\mu\text{F}$ , and 0.001  $\mu\text{F}$  as close as possible to the USB power supply.

### 52.4.3 Oscillation

- USB clock is supplied by the internal PLL.
- Provide an oscillation circuit near the clock input pin for USB (EXTAL). It is recommended to guard ring EXTAL with a ground.
- When using a crystal resonator, consult its manufacturer to determine the circuit constant.

### 52.4.4 VBUS

- This HS-USB subsystem cannot connect 5 V signals so that vbus status is informed by ovc0 and ovc1 status.

### 52.4.5 RREF Pin

- Provide a resistor (hereafter called reference resistor) of  $1.8\text{ k}\Omega \pm 1\%$ , between the RREF pin and AVSS, PVSS.
- Locate the reference resistor as close as possible to this LSI.
- The RREF pin, the reference resistor, PVSS and AVSS should be wired on wide areas and the shortest length.
- Use a wiring pattern for and only for the reference resistor, PVSS and AVSS. The pattern should be connected to the analog ground. The pattern should be designed avoiding the possibility for common impedance between RREF and other signals.
- To prevent cross talk, very-frequently switched signals such as DP, DM, clocks, and control signals for addresses and data, should not be placed near to the reference resistor, and their patterns should neither get across nor go parallel to the wiring pattern between the reference resistor and the RREF pin.

It is recommended to guard ring the reference resistor and its wiring pattern with ground.

## 53. USB High-Speed DMAC (USB-DMAC)

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

### 53.1 Features

- Three types of clock: ZS $\phi$ , HP $\phi$  and HS-USB local bus clock (48 MHz), which are asynchronously absorbed in the local bus bridge and AXI bus bridge.
- The AXI bus interface functions are implemented.  
The AXI bus interface handles data transfer with the memory and register settings.
- Data communication is performed using the local DMA protocol.
- Supports two channels that can work concurrently.
- Interrupts
  - Setting count end interrupt
  - USB-DMAC is composed of USB-DMAC0 and USB-DMAC1. There are 2 channels in USB-DMAC0 and 2 channels in USB-DMAC1.
  - Transfer end interrupt upon receiving a short packet from the USB-IP  
This function allows generation of an interrupt even in the case where DMA transfer ends after receiving data less than the transfer size set in the DMAC.
  - Timeout interrupt  
A timeout interrupt can be generated after the specified cycles after the last HS-USB transfer request. (This interrupt is used for the timeout when the final packet received is Max packet.)
  - Interrupts can also be generated when a NULL packet is received or an address error is detected.

**Table 53.1 Main Functions of This Module**

Item	Description
Application	Transfer between USB-IP (FIFO) and AXI bus (4-Gbyte arbitrary space)
Purpose of DMA transfer	High-speed data transfer between USB-IP and AXI bus
DMA transfer end notification to the software	Interrupt signals (transfer count end, USB-IP short packet reception, timeout, etc.)
Transfer space/transfer address direction	4-Gbyte arbitrary space (forward direction) to 4-Gbyte arbitrary space (forward direction)
Maximum transfer count	16,777,216
Transfer unit	8, 16, or 32 bytes
Control signals generated	Address/data read/data write conforming to the USB-IP local bus interface and AXI bus protocols
Number of channels	2 (parallel operation enabled)
Bus specification	AXI bus, local bus (USB-IP local bus)
Clock	AXI bus clock (ZS $\phi$ : 260 MHz), HPB bus clock (HP $\phi$ : 130 MHz) USB local bus clock (48 MHz) Note: The restrictions of ratio of the clock $ZS\phi \geq HP\phi \geq 48 \text{ MHz}$ Please don't change the clock frequency during USB-DMAC0 or USB-DMAC1 transferring.
Maximum transfer rate	IN transfer: About 350 Mbps (USB-DMAC0) OUT transfer: About 340 Mbps (USB-DMAC0) IN transfer: About 175 Mbps (USB-DMAC1) OUT transfer: About 170 Mbps (USB-DMAC1)

**Table 53.2 Bus Access Type**

	Supported Access Type
AXI bus access (USB-DMAC master)	8-byte read/write 16-byte read/write 32-byte read/write
USB-DMAC register setting	4-byte read/write 8-byte read/write

The configuration of this module is shown below.

This module is provided with buffers and bus bridges and controls transfers between the AXI bus and USB High-Speed module (HS-USB).

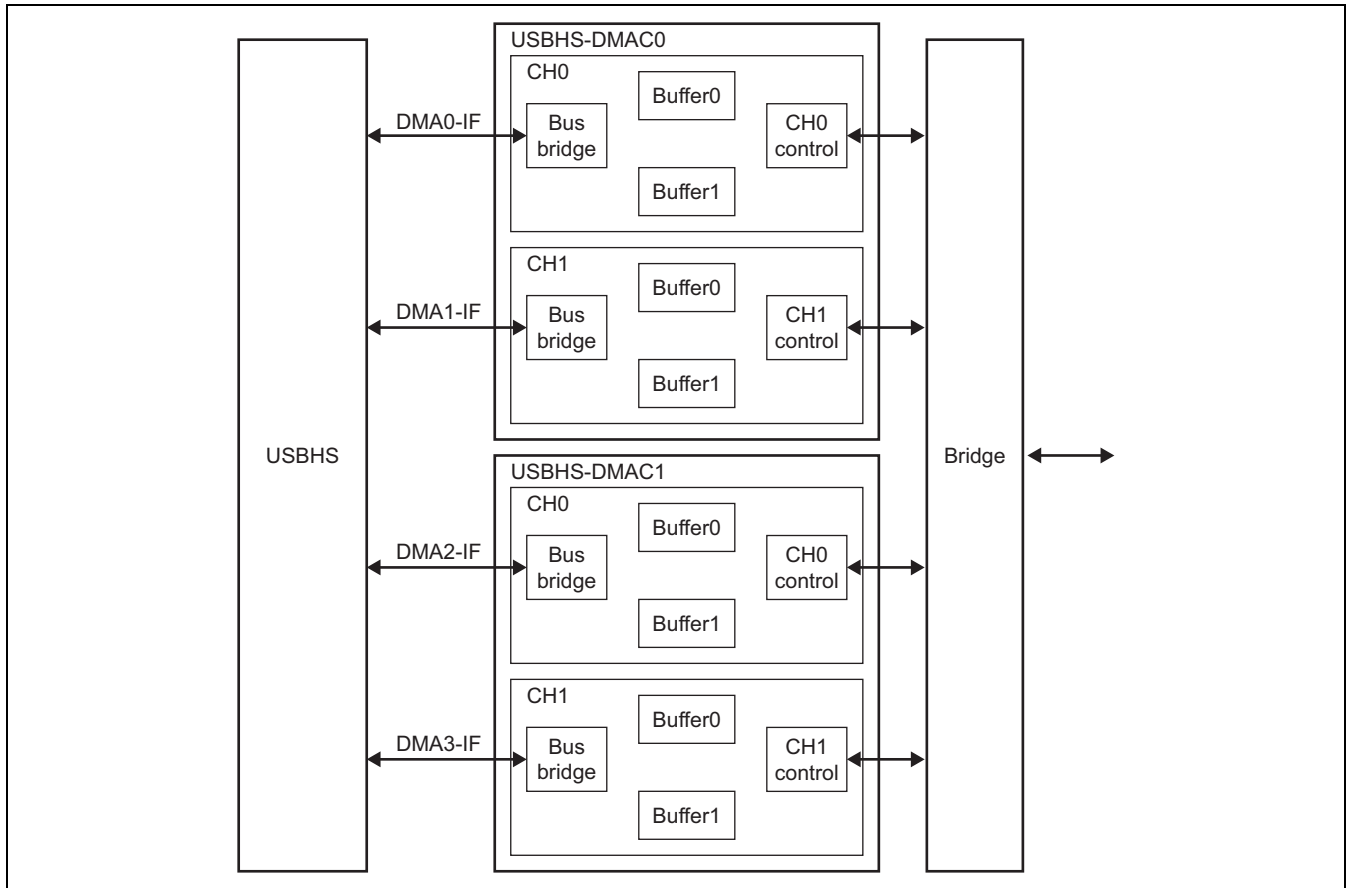


Figure 53.1 USB-DMAC Configuration

## 53.2 Register Descriptions

Table 53.3 shows the register configuration. Table 53.4 shows the register states in each processing mode.

**Table 53.3 Register Configuration**

Register Name	Abbreviation	R/W	Address	Access Size	RZ/G Series Products			
					RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
DMA0 VCR register	USBDMA0_VCR	R/W	H'E65A 0000	32	√	√	√	√
DMA0 Software reset register	USBDMA0_SWR	R/W	H'E65A 0008	32	√	√	√	√
DMA0 interrupt source register	USBDMA0_DMICR	R	H'E65A 0010	32	√	√	√	√
DMA0 source address register_0	USBDMA0_SAR_0	R/W	H'E65A 0020	32	√	√	√	√
DMA0 destination address register_0	USBDMA0_DAR_0	R/W	H'E65A 0024	32	√	√	√	√
DMA0 transfer count register_0	USBDMA0_TCR_0	R/W	H'E65A 0028	32	√	√	√	√
DMA0 timeout count register_0	USBDMA0_TOCNTR_0	R	H'E65A 002C	32	√	√	√	√
DMA0 timeout constant register_0	USBDMA0_TOCSTR_0	R/W	H'E65A 0030	32	√	√	√	√
DMA0 channel control register_0	USBDMA0_CHCR_0	R/W	H'E65A 0034	32	√	√	√	√
DMA0 final transaction valid data transfer enable register_0	USBDMA0_TEND_0	R/W	H'E65A 0038	32	√	√	√	√
DMA0 source address register_1	USBDMA0_SAR_1	R/W	H'E65A 0040	32	√	√	√	√
DMA0 destination address register_1	USBDMA0_DAR_1	R/W	H'E65A 0044	32	√	√	√	√
DMA0 transfer count register_1	USBDMA0_TCR_1	R/W	H'E65A 0048	32	√	√	√	√
DMA0 timeout count register_1	USBDMA0_TOCNTR_1	R	H'E65A 004C	32	√	√	√	√
DMA0 timeout constant register_1	USBDMA0_TOCSTR_1	R/W	H'E65A 0050	32	√	√	√	√
DMA0 channel control register_1	USBDMA0_CHCR_1	R/W	H'E65A 0054	32	√	√	√	√
DMA0 final transaction valid data transfer enable register_1	USBDMA0_TEND_1	R/W	H'E65A 0058	32	√	√	√	√
DMA0 operation register	USBDMA0_DMAOR	R/W	H'E65A 0060	32	√	√	√	√
DMA1 VCR register	USBDMA1_VCR	R/W	H'E65B 0000	32	√	√	√	√
DMA1 Software reset register	USBDMA1_SWR	R/W	H'E65B 0008	32	√	√	√	√
DMA1 interrupt source register	USBDMA1_DMICR	R	H'E65B 0010	32	√	√	√	√
DMA1 source address register_0	USBDMA1_SAR_0	R/W	H'E65B 0020	32	√	√	√	√
DMA1 destination address register_0	USBDMA1_DAR_0	R/W	H'E65B 0024	32	√	√	√	√
DMA1 transfer count register_0	USBDMA1_TCR_0	R/W	H'E65B 0028	32	√	√	√	√
DMA1 timeout count register_0	USBDMA1_TOCNTR_0	R	H'E65B 002C	32	√	√	√	√
DMA1 timeout constant register_0	USBDMA1_TOCSTR_0	R/W	H'E65B 0030	32	√	√	√	√
DMA1 channel control register_0	USBDMA1_CHCR_0	R/W	H'E65B 0034	32	√	√	√	√
DMA1 final transaction valid data transfer enable register_0	USBDMA1_TEND_0	R/W	H'E65B 0038	32	√	√	√	√

Register Name	Abbreviation	R/W	Address	Access Size	RZ/G Series Products			
					RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
DMA1 source address register_1	USBDMA1_SAR_1	R/W	H'E65B 0040	32	√	√	√	√
DMA1 destination address register_1	USBDMA1_DAR_1	R/W	H'E65B 0044	32	√	√	√	√
DMA1 transfer count register_1	USBDMA1_TCR_1	R/W	H'E65B 0048	32	√	√	√	√
DMA1 timeout count register_1	USBDMA1_TOCNTR_1	R	H'E65B 004C	32	√	√	√	√
DMA1 timeout constant register_1	USBDMA1_TOCSTR_1	R/W	H'E65B 0050	32	√	√	√	√
DMA1 channel control register_1	USBDMA1_CHCR_1	R/W	H'E65B 0054	32	√	√	√	√
DMA1 final transaction valid data transfer enable register_1	USBDMA1_TEND_1	R/W	H'E65B 0058	32	√	√	√	√
DMA1 operation register	USBDMA1_DMAOR	R/W	H'E65B 0060	32	√	√	√	√



**Table 53.4 Register States in Each Processing Mode**

<b>Abbreviation</b>	<b>Power-On Reset</b>	<b>Module Standby</b>
USBDMA0_VCR	Initialized	Retained
USBDMA0_SWR	Initialized	Retained
USBDMA0_DMICR	Initialized	Retained
USBDMA0_SAR_0	Initialized	Retained
USBDMA0_DAR_0	Initialized	Retained
USBDMA0_TCR_0	Initialized	Retained
USBDMA0_TOCNTR_0	Initialized	Retained
USBDMA0_TOCSTR_0	Initialized	Retained
USBDMA0_CHCR_0	Initialized	Retained
USBDMA0_TEND_0	Initialized	Retained
USBDMA0_SAR_1	Initialized	Retained
USBDMA0_DAR_1	Initialized	Retained
USBDMA0_TCR_1	Initialized	Retained
USBDMA0_TOCNTR_1	Initialized	Retained
USBDMA0_TOCSTR_1	Initialized	Retained
USBDMA0_CHCR_1	Initialized	Retained
USBDMA0_TEND_1	Initialized	Retained
USBDMA0_DMAOR	Initialized	Retained
USBDMA1_VCR	Initialized	Retained
USBDMA1_SWR	Initialized	Retained
USBDMA1_DMICR	Initialized	Retained
USBDMA1_SAR_0	Initialized	Retained
USBDMA1_DAR_0	Initialized	Retained
USBDMA1_TCR_0	Initialized	Retained
USBDMA1_TOCNTR_0	Initialized	Retained
USBDMA1_TOCSTR_0	Initialized	Retained
USBDMA1_CHCR_0	Initialized	Retained
USBDMA1_TEND_0	Initialized	Retained
USBDMA1_SAR_1	Initialized	Retained
USBDMA1_DAR_1	Initialized	Retained
USBDMA1_TCR_1	Initialized	Retained
USBDMA1_TOCNTR_1	Initialized	Retained
USBDMA1_TOCSTR_1	Initialized	Retained
USBDMA1_CHCR_1	Initialized	Retained
USBDMA1_TEND_1	Initialized	Retained
USBDMA1_DMAOR	Initialized	Retained

**53.2.1 DMA0/1 VCR Register (USBDMA0\_VCR/USBDMA1\_VCR)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ERR_S NT	ERR_R CV
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	ERR_SNT	0	R/W	Send Error Response 0: No error is generated. [Clearing condition] Writing 0 after reading 1. 1: An error is generated.
0	ERR_RCV	0	R/W	Receive Error Response 0: No error is generated. [Clearing condition] Writing 0 after reading 1. 1: An error is generated.

**53.2.2 DMA0/1 Software Reset Register (USBDMA0\_SWR/USBDMA1\_SWR)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SWR
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	SWR	0	R/W	Software Reset 0: Cancels reset. 1: Resets entire system. (No effect for register setting) Note: On software reset, this bit should be held high for long enough until the internal circuit stabilizes. When this bit is set to 1, it is recommended to allow several tens of clocks if operating at 260 MHz for a reset period before clearing the reset (setting this bit to 0) as a precaution.

## 53.2.3 DMA0/1 Interrupt Source Register (USBDMA0\_DMICR/USBDMA1\_DMICR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

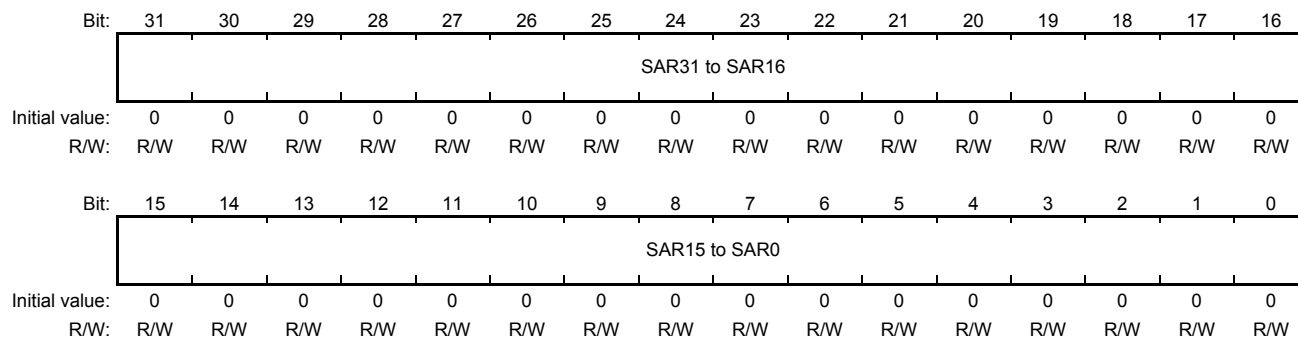
Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SHBSY 1	—	—	—	—	—	—	—	SHBSY 0	—	—	—	—	—	—	AE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	TR1	BUF1	RW1	NULL1	TO1	SP1	TE1	—	TR0	BUF0	RW0	NULL0	TO0	SP0	TE0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31	SHBSY1	0	R	CH1 AXI Bus Busy Flag Monitor 0: The AXI bus is idle. 1: The AXI bus is busy.
30 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23	SHBSY0	0	R	CH0 AXI Bus Busy Flag Monitor 0: The AXI bus is idle. 1: The AXI bus is busy.
22 to 17	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
16	AE	0	R	Address Error Interrupt Source 0: No interrupt is generated. 1: An interrupt is generated. (AE in the DMA operation register is reflected.)
15	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
14	TR1	0	R	CH1 Transaction End: Receive Interrupt Source 0: No interrupt is generated. 1: An interrupt is generated. (TR in the channel 1 control register is reflected.)
13	BUF1	0	R	CH1 Buffer End Detect Interrupt Source 0: No interrupt is generated. 1: An interrupt is generated. (BUF in the channel 1 control register is reflected.)
12	RW1	0	R	CH1 Final Buffer Access Detect Interrupt Source 0: No interrupt is generated. 1: An interrupt is generated. (RW in the channel 1 control register is reflected.)

Bit	Bit Name	Initial Value	R/W	Description
11	NULL1	0	R	CH1 NULL Packet Receive Interrupt Source 0: No interrupt is generated. 1: An interrupt is generated. (NULL in the channel 1 control register is reflected.)
10	TO1	0	R	CH1 Timeout Interrupt Source 0: No interrupt is generated. 1: An interrupt is generated. (TO in the channel 1 control register is reflected.)
9	SP1	0	R	CH1 Short Packet Receive Interrupt Source 0: No interrupt is generated. 1: An interrupt is generated. (SP in the channel 1 control register is reflected.)
8	TE1	0	R	CH1 Transfer End Interrupt Source 0: No interrupt is generated. 1: An interrupt is generated. (TE in the channel 1 control register is reflected.)
7	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
6	TR0	0	R	CH0 Transaction End Detect Interrupt Source 0: No interrupt is generated. 1: An interrupt is generated. (TR in the channel 0 control register is reflected.)
5	BUF0	0	R	CH0 Buffer End Detect Interrupt Source 0: No interrupt is generated. 1: An interrupt is generated. (BUF in the channel 0 control register is reflected.)
4	RW0	0	R	CH0 RWEND Receive Interrupt Source 0: No interrupt is generated. 1: An interrupt is generated. (RW in the channel 0 control register is reflected.)
3	NULL0	0	R	CH0 NULL Receive Interrupt Source 0: No interrupt is generated. 1: An interrupt is generated. (NULL in the channel 0 control register is reflected.)
2	TO0	0	R	CH0 Timeout Interrupt Source 0: No interrupt is generated. 1: An interrupt is generated. (TO in the channel 0 control register is reflected.)
1	SP0	0	R	CH0 Short Packet Receive Interrupt Source 0: No interrupt is generated. 1: An interrupt is generated. (SP in the channel 0 control register is reflected.)
0	TE0	0	R	CH0 Transfer End Interrupt Source 0: No interrupt is generated. 1: An interrupt is generated. (TE in the channel 0 control register is reflected.)

**53.2.4 DMA0/1 Source Address Registers 0 and 1 (USBDMA0\_SAR\_0/USBDMA1\_SAR\_1)**

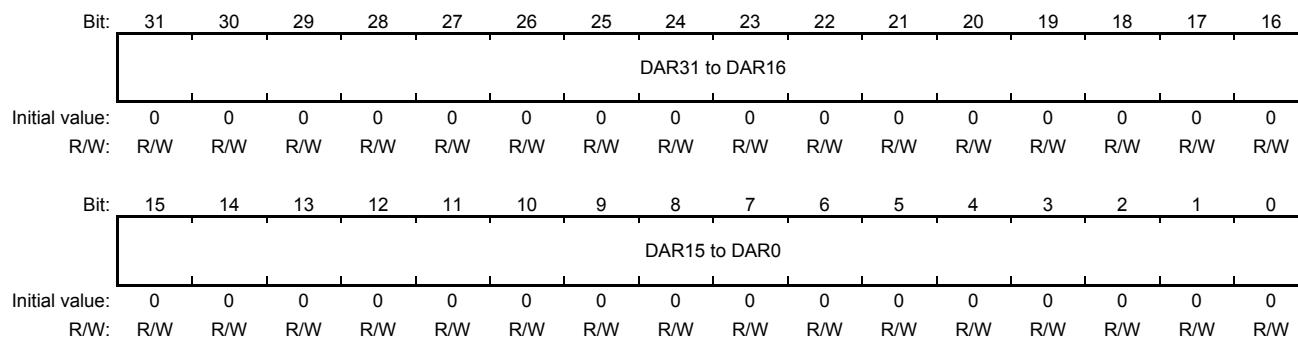
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	SAR31 to SAR0	H'0000 0000	R/W	Source Address (H'00000000 to H'FFFFFFFF (4 Gbytes)) Set a value of 8-byte, 16-byte, or 32-byte boundary. Indicate the next transfer source address during a DMA transfer.

**53.2.5 DMA0/1 Destination Address Registers 0 and 1 (USBDMA0\_DAR\_0/USBDMA1\_DAR\_1)**

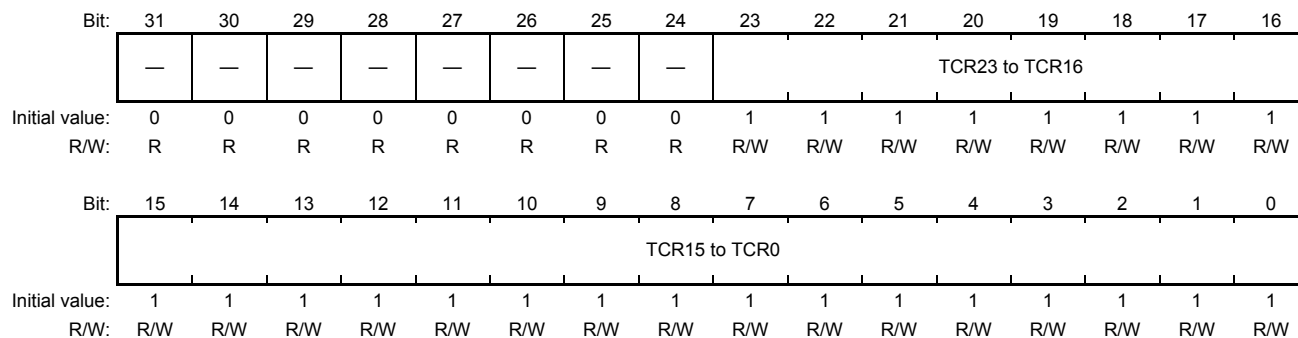
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	DAR31 to DAR0	H'0000 0000	R/W	Destination Address (H'00000000 to H'FFFFFFFF (4 Gbytes)) Set a value of 8-byte, 16-byte, or 32-byte boundary. Indicate the next transfer destination address during a DMA transfer.

**53.2.6 DMA0/1 Transfer Count Registers 0 and 1 (USBDMA0\_TCR\_0/USBDMA1\_TCR\_1)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

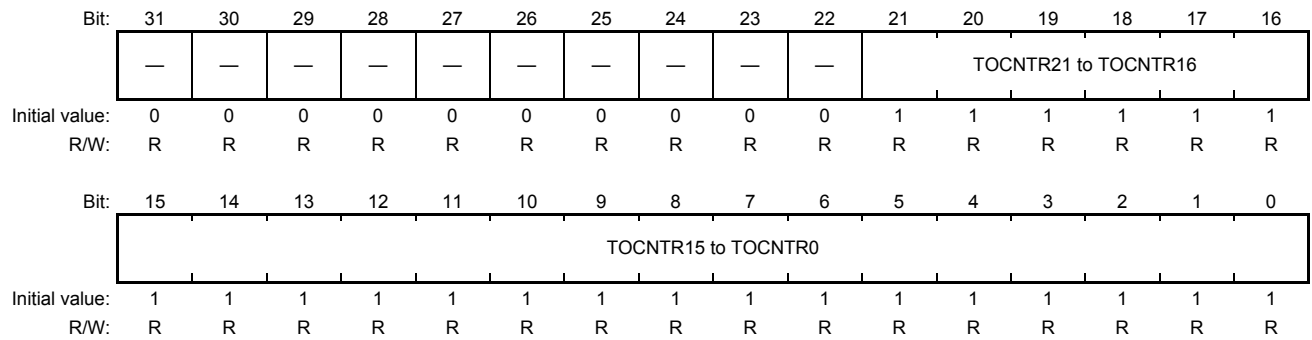


Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	TCR23 to TCR0	H'FF FFFF*	R/W	Transfer Count <ul style="list-style-type: none"> <li>When H'000001 is set, total transfer volume is as follows: Transfer size = 32 bytes: 32 × 1 bytes Transfer size = 16 bytes: 16 × 1 bytes Transfer size = 8 bytes: 8 × 1 bytes</li> <li>When H'FFFFFF is set, 16,777,215 times</li> <li>When H'000000 is set, 16,777,216 times (maximum)</li> <li>Indicate 0 when a DMA transfer completes successfully.</li> </ul>

Note: \* To read this register, read the internal transfer counter value (the TCR counter value) directly. This register is read as all 1 after a reset is cleared because the initial value of the TCR counter is all 1 (H'FFFFFF). When DMA is enabled (DE in USBDMA0/1\_CHCR is asserted), the TCR counter is loaded with the value set in this register and decrements during DMA transfers. This means that the remaining transfer count is read back. Note that the read value may be different from the one set in this register due to this reason.

**53.2.7 DMA0/1 Timeout Count Registers 0 and 1 (USBDMA0\_TOCNTR\_0/USBDMA1\_TOCNTR\_1)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

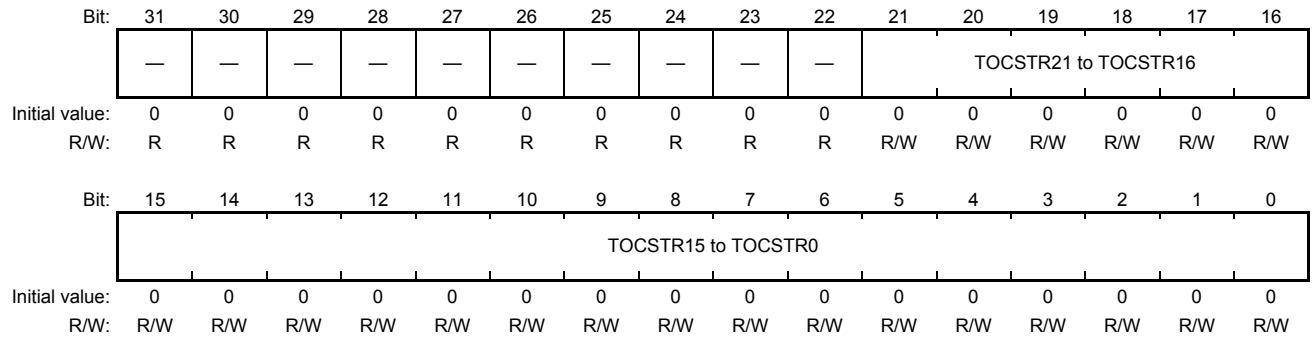


Bit	Bit Name	Initial Value	R/W	Description
31 to 22	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
21 to 0	TOCNTR21 to TOCNTR0	H'3F FFFF	R	Timeout Counter Value (H'000000 to H'27AC40) Indicate the remaining timeout count during timeout counting. (Countable up to H'3FFFFFF (approximately 21 ms) by the hardware. See the descriptions of the USBDMA0/1_TOCSTR register.)



**53.2.8 DMA0/1 Timeout Constant Registers 0 and 1  
(USBDMA0\_TOCSTR\_0/USBDMA1\_TOCSTR\_1)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√



Bit	Bit Name	Initial Value	R/W	Description
31 to 22	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
21 to 0	TOCSTR21 to TOCSTR0	H'00 0000	R/W	Timeout Constant Value (H'000000 to H'27AC40) Set a timeout value (at 200 MHz cycle). The maximum timeout time is approximately 13ms. (Setting up to H'3FFFFFF (approximately 21 ms) is allowed by the hardware.)

## 53.2.9 DMA0/1 Channel Control Registers 0 and 1 (USBDMA0\_CHCR\_0/USBDMA1\_CHCR\_1)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	FTE	—	—	—	SPIM	TRE	BUFE	RWE	NULLE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R	R	R	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TR	BUF	RW	NULL	—	—	—	—	TS1	TS0	IE	TOE	TO	SP	TE	DE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 25	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
24	FTE	0	(R)/W	Forced TE Set Register When a NULL packet is received, the TE bit is forced to 1 to terminate the transfer by setting 1 in this register. (The DREQE bit of the USB-IP should also be controlled accordingly. For details on the control procedure and restrictions, see section 53.3.2 (3), DMA transfer flow.) This bit is always read as 0. 0: No effect (nothing happens). 1: Forces the TE bit to 1.
23 to 21	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
20	SPIM	0	R/W	Short Packet Receive Interrupt Mask Enables or disables the reflection of the short packet (SP) receive flag in the interrupt signal. If this bit is set to 1, no interrupts are generated when an SP is received. However, the SP receive flag (the SP bit) is set regardless of this register setting. 0: The short packet receive interrupt is enabled (default). 1: The short packet receive interrupt is disabled.
19	TRE	0	R/W	Transaction End Detect Interrupt Flag Enable Enables or disables the reflection of TR in the interrupt signal and the DMA stop/restart control. (When this bit is set to 0, the TR bit is always 0.) 0: The TR flag is disabled. 1: The TR flag is enabled.
18	BUFE	0	R/W	Buffer End Detect Interrupt Flag Enable Enables or disables the reflection of BUF in the interrupt signal and the DMA stop/restart control. (When this bit is set to 0, the BUF bit is always 0.) 0: The BUF flag is disabled. 1: The BUF flag is enabled.

Bit	Bit Name	Initial Value	R/W	Description
17	RWE	0	R/W	<p>Final Buffer Access Detect Interrupt Flag Enable</p> <p>Enables or disables the reflection of RW in the interrupt signal and the DMA stop/restart control. (When this bit is set to 0, the RW bit is always 0.)</p> <p>0: The RW flag is disabled. 1: The RW flag is enabled.</p>
16	NULLE	0	R/W	<p>NULL Receive Interrupt Flag Enable</p> <p>Enables or disables the reflection of the NULL receive interrupt flag (NULL) in the interrupt signal.</p> <p>0: The NULL receive interrupt flag is disabled. 1: The NULL receive interrupt flag is enabled.</p>
15	TR	0	R/W*	<p>Transaction End Detect Interrupt Flag</p> <p>When the transaction end is detected, an interrupt is generated.</p> <p>0: DMA transfer is in progress or suspended. [Clearing condition] Writing 0 after reading 1. 1: A transaction end receive interrupt is generated.</p>
14	BUF	0	R/W*	<p>Buffer End Detect Interrupt Flag</p> <p>When the end of the buffer is detected, an interrupt is generated.</p> <p>0: DMA transfer is in progress or suspended. [Clearing condition] Writing 0 after reading 1. 1: A buffer end detect interrupt is generated.</p>
13	RW	0	R/W*	<p>Final Buffer Access Detect Interrupt Flag</p> <p>When the final access to the buffer is detected, an interrupt is generated.</p> <p>0: DMA transfer is in progress or suspended. [Clearing condition] Writing 0 after reading 1. 1: A final buffer access detect interrupt is generated.</p>
12	NULL	0	R/W*	<p>NULL Receive Interrupt Flag</p> <p>When NULL packet is received, an interrupt is generated.</p> <p>0: DMA transfer is in progress or suspended. [Clearing condition] Writing 0 after reading 1. 1: A NULL packet receive interrupt is generated.</p>
11 to 8	—	All 0	R	<p>Reserved</p> <p>The bits should always be written as 0.</p>

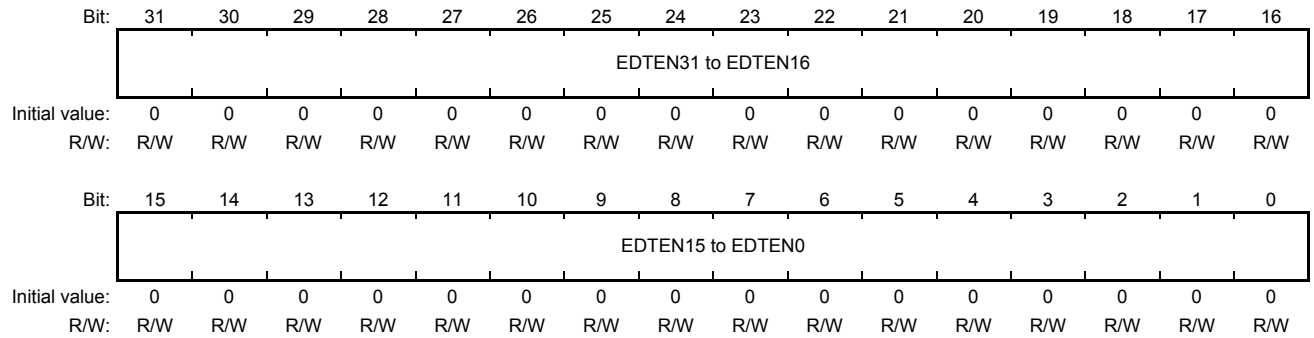
Bit	Bit Name	Initial Value	R/W	Description
7, 6	TS1 to TS0	00	R/W	<p>DMA Transfer Size</p> <p>00: 8 bytes 01: 16 bytes 10: 32 bytes 11: Setting prohibited</p> <p>Specify the same transfer size and address boundary when setting addresses in USBDMA0/1_SAR and USBDMA0/1_DAR as a transfer source and transfer destination.</p> <p>If TS = 11 is set, an address error is generated and DMA transfer is disabled.</p>
5	IE	0	R/W	<p>Interrupt Enable</p> <p>Enables or disables an interrupt request to the CPU when DMA transfer ends. When AE, TE, SP, TO, NULL, RW, BUF, or TR bit is set with this bit set to 1, an interrupt request is output to the CPU.</p> <p>However, when the TRE, BUFE, RWE, NULLE, or TOE bit is set to disabled, no interrupt due to TR, BUF, RW, NULL, or TO is generated.</p> <p>0: An interrupt request is disabled. 1: An interrupt request is enabled.</p>
4	TOE	0	R/W	<p>Timeout Enable</p> <p>Enables or disables the reflection of the timeout flag (TO) in the interrupt.</p> <p>0: Timeout flag is disabled. 1: Timeout flag is enabled.</p>
3	TO	0	R/W*	<p>Timeout Flag</p> <p>After a transfer request REQ is negated, a timeout interrupt is generated after the specified cycles. (Used for timeout when the final packet is Max packet.)</p> <p>0: DMA transfer is in progress or suspended. [Clearing condition] Writing 0 after reading 1. 1: Timeout is generated.</p>
2	SP	0	R/W*	<p>Short Packet Receive Flag</p> <p>A transfer end interrupt is generated upon receiving a short packet from the USB-IP. For example, if DMA transfer size is set to 1 MB but actual data transfer is 900 KB, this interrupt is generated when transfer of 900 KB finishes.</p> <p>0: DMA transfer is in progress or suspended. [Clearing condition] Writing 0 after reading 1. 1: A short packet is received.</p>

Bit	Bit Name	Initial Value	R/W	Description
1	TE	0	R/W*	<p>Transfer End Flag</p> <p>When a DMA transfer ends with USBDMA0/1_TCR = 0, the TE bit is set to 1. When a DMA address error occurs before USBDMA0/1_TCR is cleared to 0 and the transfer is suspended by clearing the DE bit and the DME bit in USBDMA0/1_DMAOR, the TE bit is not set to 1. To clear the TE bit, write 0 after reading 1. When TE = 1, DMA transfer is disabled even if the DE bit is set to 1.</p> <p>0: DMA transfer is in progress or suspended.            [Clearing condition]            Writing 0 after reading 1.</p> <p>1: DMA transfer end (TCR = 0)</p>
0	DE	0	R/W	<p>DMA Enable</p> <p>Enables or disables DMA transfer. Setting the DME bit in USBDMA0/1_DMAOR and the DE bit for the corresponding channel to 1 starts a DMA transfer, provided that all interrupt flags are 0. Clearing the DE bit to 0 suspends the ongoing transfer after the transfer of one transaction is completed.</p> <p>0: DMA transfer is disabled.            1: DMA transfer is enabled.</p>

Note: \* Only writing 0 to clear the flag is enabled.

**53.2.10 DMA0/1 Final Transaction Valid Data Transfer Enable Registers 0 and 1 (USBDMA0\_TEND\_0/USBDMA1\_TEND\_1)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	EDTEN31 to EDTEN0	H'00000000	R/W	<p>Final Transaction Valid Data Transfer Enable (valid only for IN transfers)</p> <p>Specify valid data size in units of bytes in the final transaction of data transfer (see section 53.3.2, DMA Transfer Function).</p> <p>H'80000000: 32 bytes × (n-1) + 1 byte</p> <p>H'C0000000: 32 bytes × (n-1) + 2 bytes</p> <p>:</p> <p>H'FFFFFFF: 32 bytes × (n-1) + 32 bytes</p> <p>Notes: 1. n: Transfer count setting (TCR)</p> <p>2. For the 8-byte transfer, set EDTEN23 to EDTEN0 to 0. For the 16-byte transfer, set EDTEN15 to EDTEN0 to 0.</p>

**53.2.11 DMA0/1 Operation Register (USBDMA0\_DMAOR/USBDMA1\_DMAOR)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	TID1 and TID0	RM	PR1 and PR0	AE	DME		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R/W*	R/W*	R/W	R/W	R/W	R/W*	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 7	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
6, 5	TID1 and TID0	00	R/W*	Response Error Channel Identity Information TID1 indicates the channel 1 error information, and TID0 indicates the channel 0 error information. TID1 0: No error 1: Channel 1 response packet error TID0 0: No error 1: Channel 0 response packet error [Setting condition] When a CH0 (1) response error occurs [Clearing condition] Clearing ERR_RCV in USBDMA0/1_VCR (Channel 0/channel 1 concurrent clear)
4	RM	0	R/W	Response Error Mask Mode 0: A response error is output. 1: A response error is masked.
3, 2	PR1 and PR0	00	R/W	Priority Mode Specify the priority of channels to execute transactions when transfer requests are made simultaneously in both channel 0 and channel 1 as follows: 00: Channel 0 > Channel 1 01: Channel 1 > Channel 0 10: Setting prohibited (If PR = 10 is set, channel 0 > channel 1) 11: Setting prohibit

Bit	Bit Name	Initial Value	R/W	Description
1	AE	0	R/W*	<p>Address Error Flag</p> <p>Indicates that an address error interrupt occurred when setting USBDMA0/1_SAR or USBDMA0/1_DAR. This flag is set to 1 when the value of USBDMA0/1_SAR or USBDMA0/1_DAR differs from the transfer size (TS) boundary, and when the TS bits are set to 11 (setting prohibited).</p> <p>When the AE bit is set to 1, DMA transfer is not enabled even if the DE bit in DMACHCR and the DME bit in USBDMA0/1_DMAOR are set to 1.</p> <p>0: No address error interrupt is generated by the DMAC.</p> <p>[Clearing condition]</p> <p>Setting USBDMA0/1_SAR and USBDMA0/1_DAR to values that match the transfer size boundary.</p> <p>1: An address error interrupt is generated.</p>
0	DME	0	R/W	<p>DMA Master Enable</p> <p>Enables or disables DMA transfers for all channels. When the DME bit and the DE bit in USBDMA0/1_CHCR are set to 1, DMA transfer is enabled, provided that all interrupt flags in USBDMA0/1_CHCR of the transfer channel are 0. Clearing the DME bit suspends the DMA transfer for all channels.</p> <p>0: DMA transfer for all channels is disabled.</p> <p>1: DMA transfer for all channels is enabled.</p>

Note: \* Only writing 0 to clear the flag is enabled.



## 53.3 Operation

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

### 53.3.1 Interrupt/Error Detection Function

This section describes the interrupt/error detection function that is implemented in this module.

Table 53.5 lists the mask, source, and flag registers for each interrupt type.

**Table 53.5 Registers by Interrupts/Errors**

	Interrupt Generation	Interrupt Mask Register	Interrupt Mask Register (Individual Mask)	Source Register	Flag Register
Transfer count end	√	X*1_CHCR_x.IE	—	X*1_DMICR.TEx	X*1_CHCR_x.TE
Short packet receive	√	X*1_CHCR_x.IE	X*1_CHCR_x.SPIM	X*1_DMICR.SPx	X*1_CHCR_x.SP
NULL packet receive	√	X*1_CHCR_x.IE	X*1_CHCR_x.NULLE	X*1_DMICR.NULLx	X*1_CHCR_x.NULL
Timeout	√	X*1_CHCR_x.IE	X*1_CHCR_x.TOE	X*1_DMICR.TOx	X*1_CHCR_x.TO
Transaction end detect	√	X*1_CHCR_x.IE	X*1_CHCR_x.TRE*	X*1_DMICR.TRx	X*1_CHCR_x.TR
Buffer end detect	√	X*1_CHCR_x.IE	X*1_CHCR_x.BUFE*	X*1_DMICR.BUFx	X*1_CHCR_x.BUF
Final buffer access detect	√	X*1_CHCR_x.IE	X*1_CHCR_x.RWE*	X*1_DMICR.RWx	X*1_CHCR_x.RW
Address error	√	X*1_CHCR_x.IE	—	X*1_DMICR.AE	X*1_DMAOR.AE
Response packet error	—	—	—	—	X*1_VCR.ERR_SNT X*1_VCR.ERR_RCV

Legend: X\*1: USBDMA0/USBDMA1

Note: These registers not only mask interrupt generation but also disable error processing (flag sources and flag clearing).

Table 53.6 shows the processing to be executed when different interrupts occur. DMA transfer control is not affected when the NULL packet receive, timeout, or response packet error interrupt occurs. When the transfer count end interrupt occurs, processing is restarted. Processing can be resumed or restarted after interrupts occur from other sources.

**Table 53.6 Processing to be Executed When Interrupts Occur (Suspend/Resume/Restart)**

	Suspend/Resume	Terminate/Restart	Suspend/Resume/Restart Control Mask Register
Transfer count end	—	√	—
Short packet receive	√	√	—
NULL packet receive	—	√*	—
Timeout	—	√	—
Transaction end detect	√	√	USBDMA0/1_CHCR_x.TRE
Buffer end detect	√	√	USBDMA0/1_CHCR_x.BUFE
Final buffer access detect	√	√	USBDMA0/1_CHCR_x.RWE
Address error	√	√	—
Response packet error	—	—	—

Note: \* When a NULL packet is received, processing is forced to be terminated and restarted by the FTE bit (see section 53.3.2 (3), DMA transfer flow.).

The internal circuit is reloaded register values when restarted, but not when resumed.

Table 53.7 lists the interrupt generating conditions.

**Table 53.7 Interrupt Generating Conditions**

<b>Interrupt Name</b>	<b>Interrupt Conditions</b>
Transfer count end interrupt	When the final data transfer of the specified transfer count (in the USBDMA0/1_TCR register) completes IN transfer: When the final access to USB-IP completes OUT transfer: When the data transmission to the AXI completes
Short packet receive interrupt	When the data transfer at the time the end of a transaction is detected completes
NULL packet receive interrupt	When a NULL packet is detected or the forced TE register is set
Timeout interrupt	When the specified time elapses after the last transfer request
Transaction end detect interrupt	When the end of a transaction is detected
Buffer end detect interrupt	When the end of the buffer is detected
Final buffer access detect interrupt	When the final access to the buffer is detected
Address error interrupt	When invalid access to the DMAC register is attempted (With invalid USBDMA0/1_SAR/USBDMA0/1_DAR values or invalid transfer size (TS) specified)
Response packet error	Error Transmission (ERR_SNT) When accessed by a transaction that is not supported Error Reception (ERR_RCV) When received a response packet error from the system

Figure 53.2 shows a block diagram of the interrupt circuit.

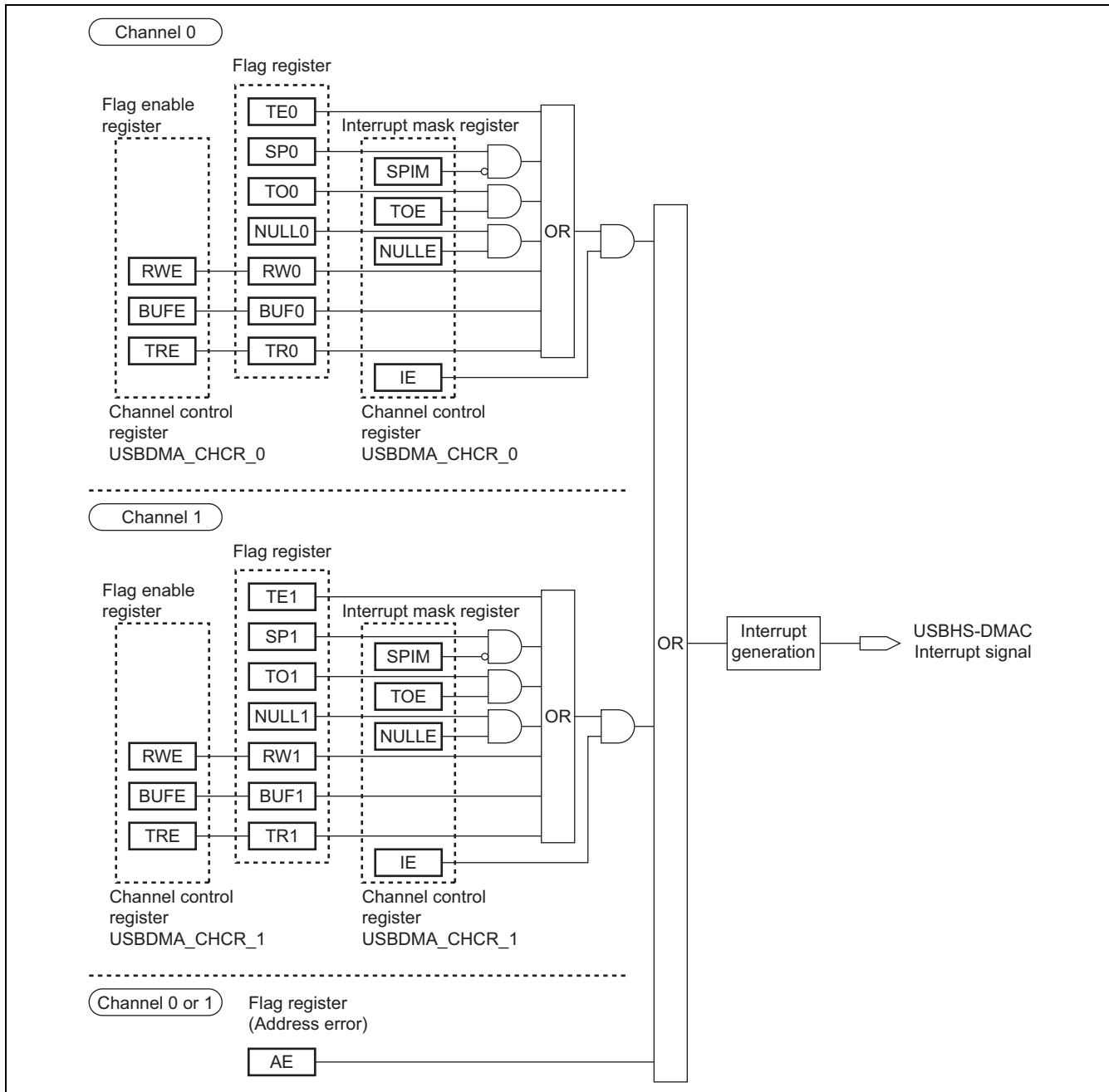
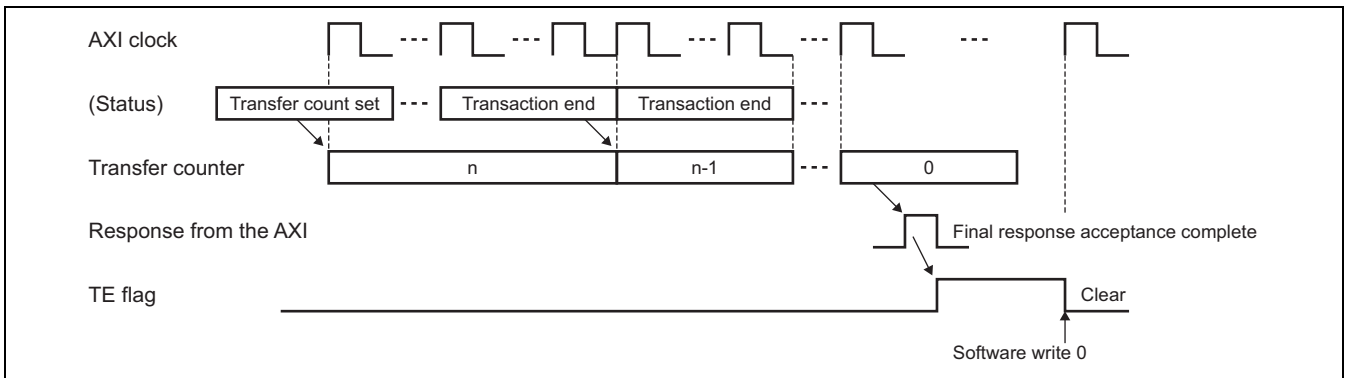


Figure 53.2 Block Diagram of Interrupt Circuit

**(1) Transfer count end interrupt (TE flag)**

Can be generated when the specified number of transfers complete or the FTE bit in the channel control register (USBDMAC0/1\_CHCR\_0 to USBDMAC0/1\_CHCR\_1) is set to 1. When the IE bit in the USBDMAC0/1\_CHCR\_0 to USBDMAC0/1\_CHCR\_1 is set to 0, no interrupts are generated. However, the TE bit in USBDMAC0/1\_CHCR\_0 to USBDMAC0/1\_CHCR\_1 and the TE0 or TE1 bit in the interrupt source register (USBDMAC0/1\_DMICR) are set to 1 regardless of the IE bit setting.

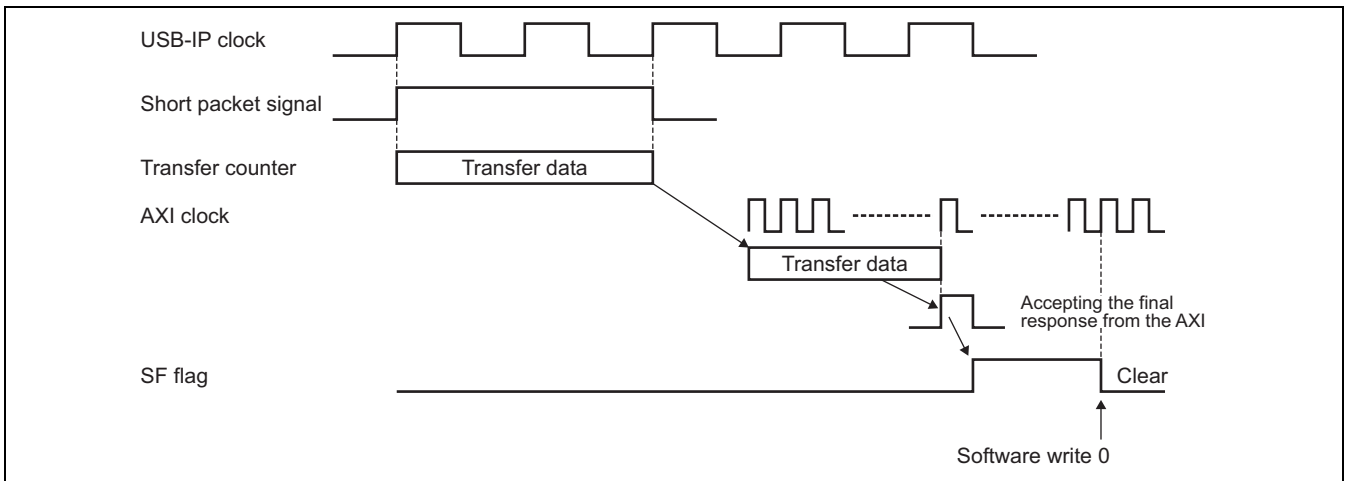
The internal transfer counter is loaded with the value set in the USBDMAC0/1\_TCR\_x register and decrements based on the AXI clock every time one transaction (8-/16-/32-byte) completes. When the transfer count value reaches 0 (the end of a transfer count), the counter sets the TE (transfer end) flag from 0 to 1 (when the FTE bit is set, it is reflected on the TE flag immediately). The TE bit is cleared by writing 0 to it after reading it as 1 by software.



**Figure 53.3 Transfer Count End Interrupt (TE) Generation Timing**

**(2) Short packet receive interrupt (SP flag)**

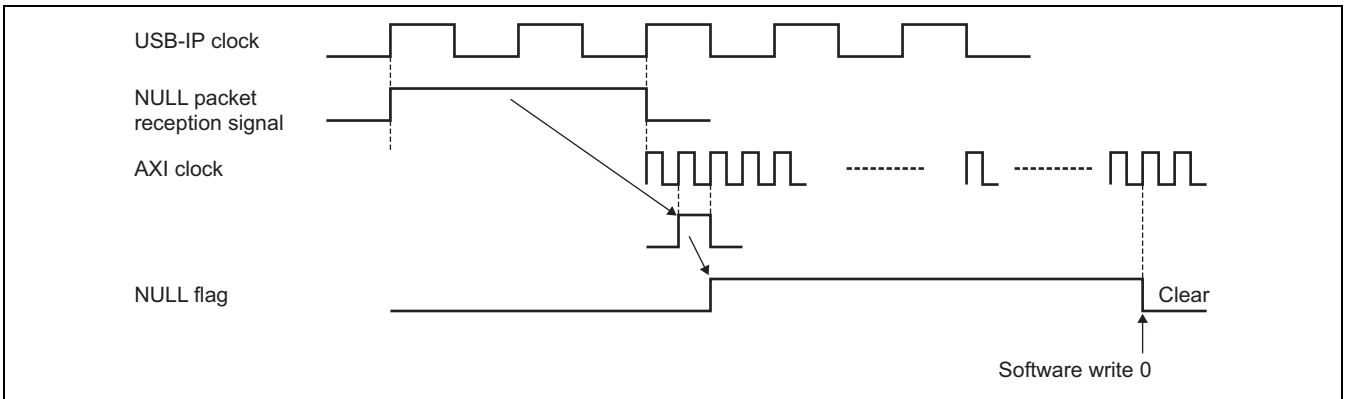
Can be generated when a short packet is detected. When the SPIM bit in the USBDMAC0/1\_CHCR\_x register is set to 1, no interrupts are generated. However, the SP bit (SP flag) in the USBDMAC0/1\_CHCR\_x register and the SP0 or SP1 bit in the USBDMAC0/1\_DMICR register are set to 1, regardless of the SPIM bit setting. The SP bit is cleared by writing 0 to it after reading it as 1 by software.



**Figure 53.4 Short Packet Receive Interrupt (SP) Generation Timing**

**(3) NULL packet receive interrupt (NULL flag)**

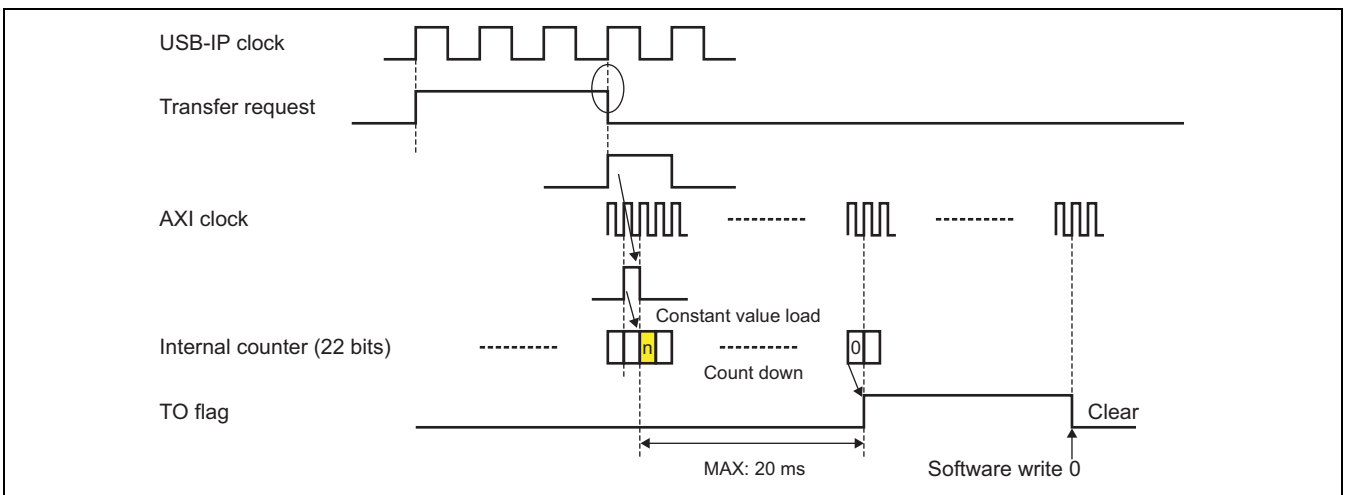
Can be generated when a NULL packet is detected. When the NULLE bit in the USBDMA0/1\_CHCR\_x register is set to 0, no interrupts are generated. However, the NULL bit (NULL flag) in the USBDMA0/1\_CHCR\_x register and the NULL0 or NULL1 bit in the USBDMA0/1\_DMICR register are set to 1, regardless of the NULLE bit setting. Note also that the DMA transfer control in this module, such as stop, suspend, or resume, is not affected when a NULL packet is received. The software is responsible for implementing special processing if necessary since in this module this interrupt is designed only to signal the software that a NULL packet is received.



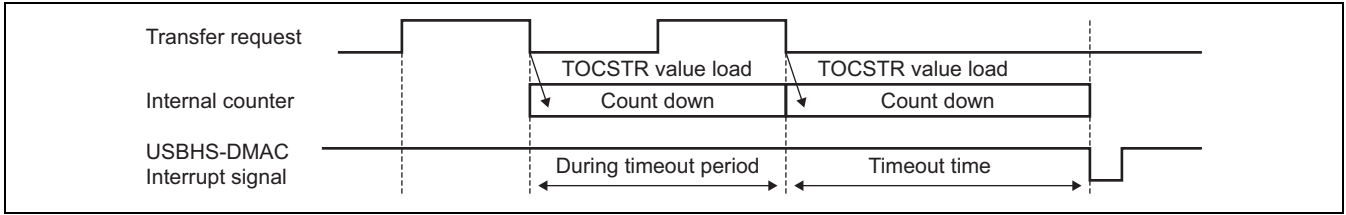
**Figure 53.5 NULL Packet Receive Interrupt (NULL) Generation Timing**

**(4) Timeout interrupt (TO flag)**

Can be generated when the time period that is specified in the timeout constant register (USBDMA0/1\_TOCSR\_0 or USBDMA0/1\_TOCSR\_1) elapses after the final transfer request is received from the USB-IP. On detecting the final transfer request, the internal counter is loaded with the value set in the USBDMA0/1\_TOCSR\_x register and starts counting down. When the counter reaches 0, it generates a timeout interrupt. Note that the DMA transfer control in this module, such as stop, suspend, or resume, is not affected when a timeout interrupt occurs. The TO bit is cleared by writing 0 to it after reading it as 1 by software. Figures 53.6 and 53.7 show the timeout interrupt generation timing.



**Figure 53.6 Timeout Interrupt (TO) Generation Timing**

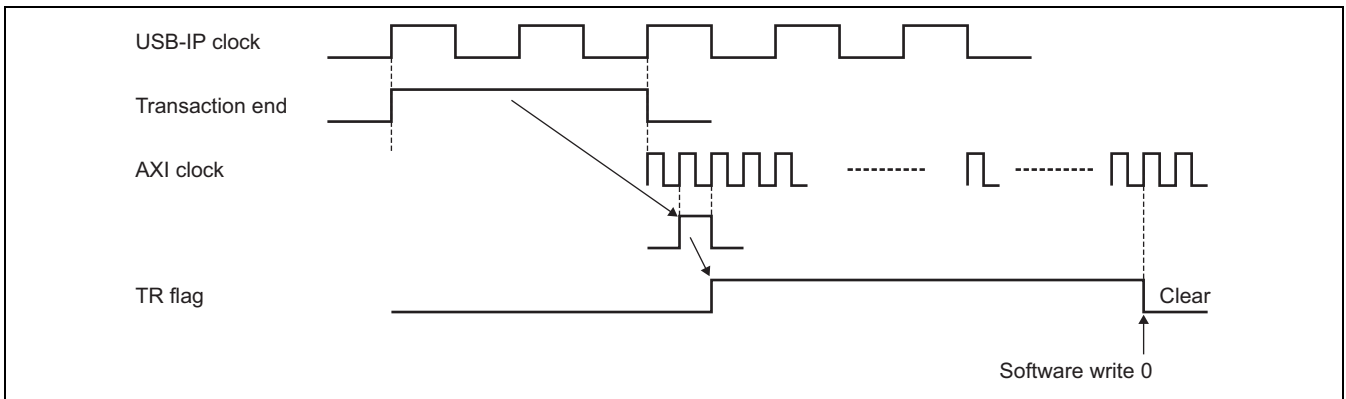


**Figure 53.7 Timeout Interrupt Timing**

The functions described in section 53.3.1 (5) to 53.3.1 (9) are added to detect and notify the transitions on an individual signal line to the software, but no use is defined. They can be used as required.

**(5) Transaction end detect interrupt (TR flag)**

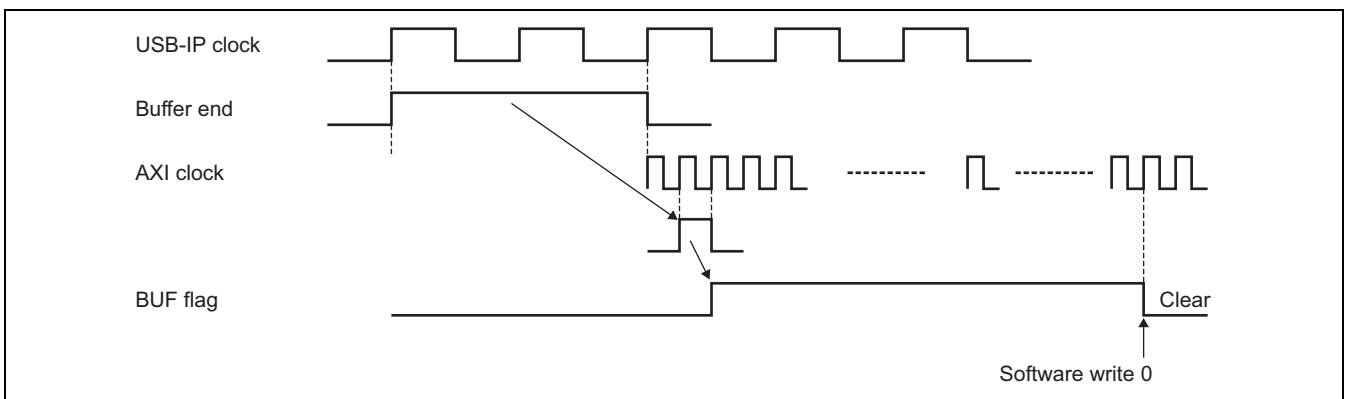
Can be generated when the end of a transaction is detected within the USB-IP. Note that the TR bit in the USBDMA0/1\_CHCR\_x register and the TR0 or TR1 bit in the USBDMA0/1\_DMICR register are not reflected in the interrupt signal when the TRE bit in the USBDMA0/1\_CHCR\_x register is set to 0.



**Figure 53.8 Transaction End Detect Interrupt Timing**

**(6) Buffer end detect interrupt (BUF flag)**

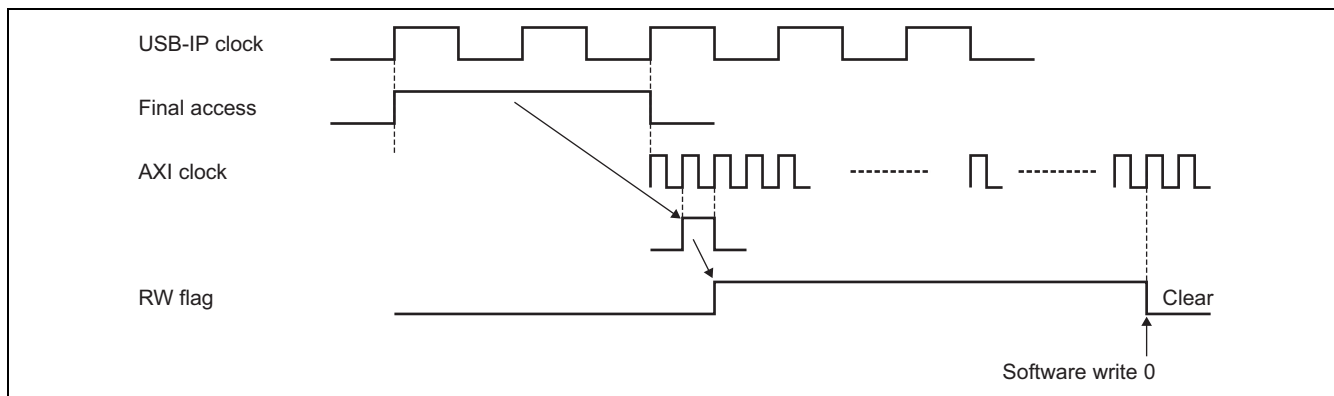
Can be generated when the end of the buffer in the USB-IP is detected. Note that the BUF bit in the USBDMA0/1\_CHCR\_x register and the BUF0 or BUF1 bit in the USBDMA0/1\_DMICR register are not reflected in the interrupt signal when the BUFE bit in the USBDMA0/1\_CHCR\_x register is set to 0.



**Figure 53.9 Buffer End Detect Interrupt Timing**

**(7) Final buffer access detect interrupt (RW flag)**

Can be generated when the final access to the buffer in the USB-IP is detected. Note that the RW bit in the USBDMA0/1\_CHCR\_x register and the RW0 or RW1 bit in the USBDMA0/1\_DMICR register are not reflected in the interrupt signal when the RWE bit in the USBDMA0/1\_CHCR\_x register is set to 0.



**Figure 53.10 Final Buffer Access Detect Interrupt Timing**

**(8) Address error detection**

This is a flag that indicates an address error interrupts has occurred when setting the source address register (USBDMA0/1\_SAR0 to USBDMA0/1\_SAR1) and the destination address register (USBDMA0/1\_DAR0 to USBDMA0/1\_DAR1). When the value written to the USBDMA0/1\_SAR or USBDMA0/1\_DAR register differs from the transfer size (TS) boundary, and when the TS bits are set to 11 (setting prohibited), the AE bit in the USBDMA0/1\_DMAOR register is set to 1. There is no distinction between CH0 and CH1 for an address error (the AE bit is set to 1 when an address error occurs on CH0 or CH1).

While the AE is set, no DMA transfer is allowed even if the DE bit in the USBDMA0/1\_CHCR\_x register and the DME bit in the USBDMA0/1\_DMAOR register are set to 1. The address error interrupt is cleared by setting correct addresses in USBDMA0/1\_SAR\_x and USBDMA0/1\_DAR\_x.

**Table 53.8 Address Error Detection Conditions When Setting Transfer Sizes**

Transfer Size	Address Error Detection Conditions
TS = B'00 (8-byte transfer)	When data that is not aligned to 8-byte boundaries is written to the USBDMA0/1_SAR/ USBDMA0/1_DAR registers (Writes to the USBDMA0/1_SAR/ USBDMA0/1_DAR registers are valid.)
TS = B'01 (16-byte transfer)	When data that is not aligned to 16-byte boundaries is written to the USBDMA0/1_SAR/ USBDMA0/1_DAR registers (Writes to the USBDMA0/1_SAR/ USBDMA0/1_DAR registers are valid.)
TS = B'10 (32-byte transfer)	When data that is not aligned to 32-byte boundaries is written to the USBDMA0/1_SAR/ USBDMA0/1_DAR registers (Writes to the USBDMA0/1_SAR/ USBDMA0/1_DAR registers are valid.)
—	When B'11 (setting prohibited) is written to the TS bit (Writes to the TS bit are valid.)

**(9) Response packet error detection**

This function reports response packet errors when the interface between the AXI and this module is accessed in ways that are not listed in Table 53.2.

**(a) Transmitting response packet errors**

When a response packet error occurs during accessing from the AXI to this module, the ERR\_SNT bit in the USBDMA0/1\_VCR register is set to 1.\* The error signal is also sent to the AXI bus if the RM bit in the USBDMA0/1\_DMAOR register is 0. If the RM bit is set to 1, the error signal is masked (0 is signaled).

Note: \* When a response packet error occurs, the ERR\_SNT bit is set to 1 regardless of the RM bit setting. The ERR\_SNT bit is cleared by writing 0 after reading 1.

**Table 53.9 Response Packet Error Generation**

USBDMA0_DMAOR		
(RM bit) Setting	1 (Mask Mode)	0 (Normal Mode)
Response packet error signal notification to AXI	Signals the fixed value (0) to the AXI bus without determining if there is a response packet error.	Reports a response packet error to the AXI bus when it is accessed with a transfer size other than those supported in this module (4-byte read/write and 8-byte read).

**(b) Receiving response packet errors**

When a response packet error occurs during accessing from this module to the AXI, the ERR\_RCV bit in the USBDMA0/1\_VCR register is set to 1. The TID bit in the USBDMA0/1\_DMAOR register indicates on which channel of this module the error has occurred (TID[1]=1 means it has occurred on CH1 and TID[0]=1 on CH0).

The ERR\_RCV bit is cleared by writing 0 after reading 1.



### 53.3.2 DMA Transfer Function

#### (1) Operating mode

The following operating modes (a) to (b) are supported according to the setting of the PR bit in the DMA operation register (USBDMA0/1\_DMAOR).

##### (a) CH0 first control

Forces CH1 to wait to start a DMA transfer until a DMA transfer completes on CH0.

When there is a timing conflict in starting a DMA transfer between CH0 and CH1, CH0 takes precedence over CH1. If a DMA transfer is in progress on CH1 when CH0 tries to start a DMA transfer, CH0 waits to start it until the ongoing DMA transfer completes on CH1.

##### (b) CH1 first control

Forces CH0 to wait to start a DMA transfer until a DMA transfer completes on CH1.

When there is a timing conflict in starting a DMA transfer between CH1 and CH0, CH1 takes precedence over CH0. If a DMA transfer is in progress on CH0 when CH1 tries to start a DMA transfer, CH1 waits to start it until the ongoing DMA transfer completes on CH0.

Figure 53.11 shows an overview of the processing of the AXI bridge in each operating mode.

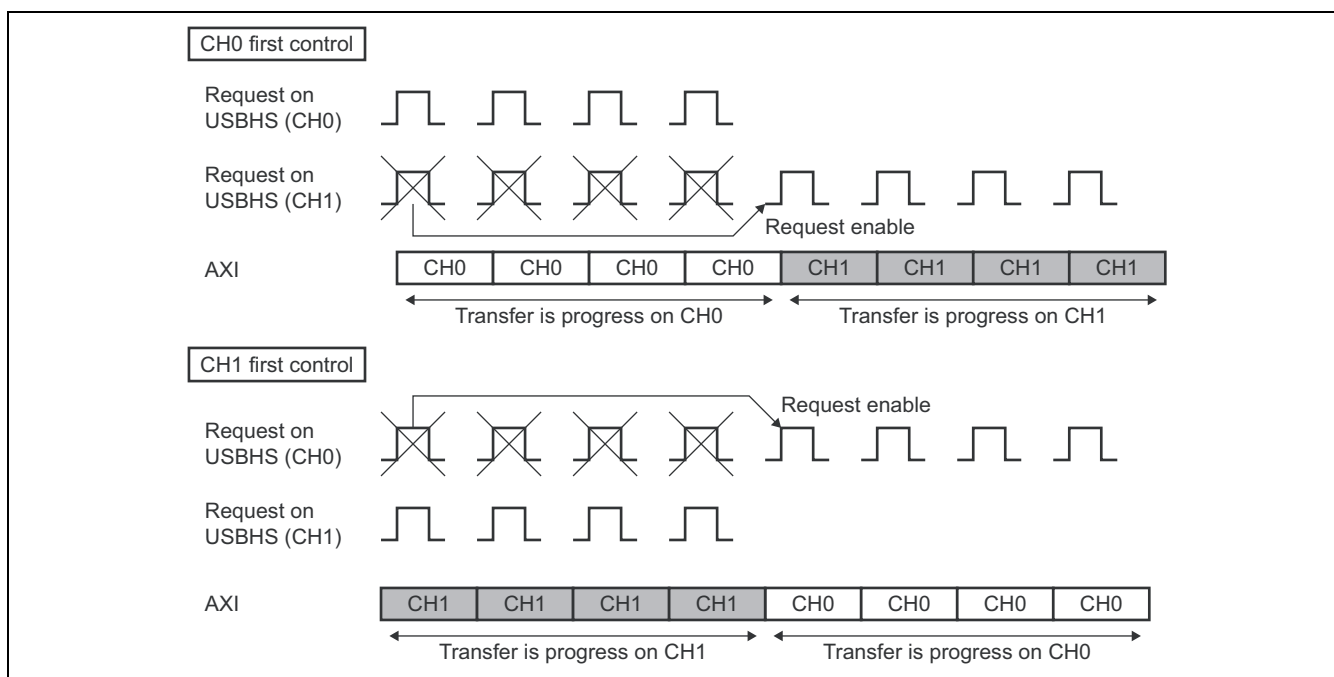


Figure 53.11 Overview of AXI Bridge Processing in Each Mode

**(2) Transfer size**

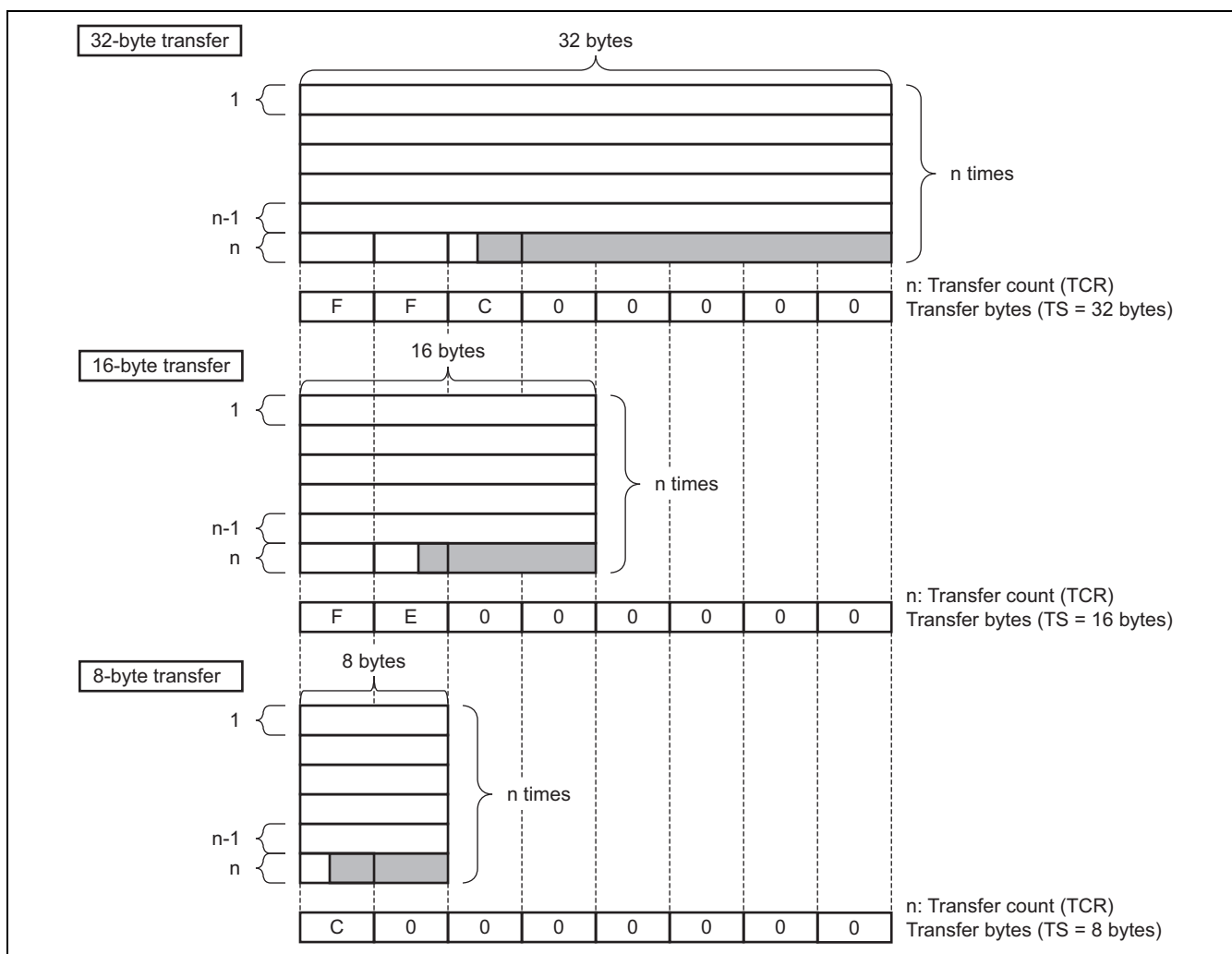
The transfer size on the AXI can be selected by setting the channel control register (the TS bit).

8-, 16-, and 32-byte can be set for each channel independently.

The following consideration should be observed during IN transfers.

The minimum transfer size that can be set to the TS bit is 8 bytes while the USB-IP can control transfers in 1-byte units. For example, if valid transfer data that is  $8 \times (n - 1) + \alpha$  ( $\alpha$  is less than 7 bytes) in size is to be transferred to the USB-IP with the transfer size set to 8 bytes and the transfer count set to  $n$ ,  $\alpha$  is transferred as a valid transfer unit by controlling byte enables according to the DMA final transaction valid data transfer enable register (the EDTEN bits) setting. Likewise, data is transferred in "transfer size x transfer count" (the final transaction is controlled by EDTEN) for 16- and 32-byte transfer sizes. The EDTEN setting is valid only for IN transfer and is don't care for OUT transfer.

Figure 53.12 shows an example of EDTEN setting. When only EDTEN31 in EDTEN31 to EDTEN0 is 1, one byte is enabled. When only EDTEN31 and EDTEN30 in EDTEN31 to EDTEN0 are 1, two bytes are enabled. Therefore, the total transfer volumes in the example shown above are calculated as "(32 bytes x (n - 1)) bytes + 10 bytes" for 32-byte transfer, "(16 bytes x (n - 1)) bytes + 7 bytes" for 16-byte transfer, and "(8 bytes x (n - 1)) bytes + 2 bytes" for 8-byte transfer. EDTEN15 to EDTEN0 in 16-byte transfer, EDTEN23 to EDTEN0 in 8-byte transfer are invalid (their values are ignored).



**Figure 53.12 Example of Final Transaction Valid Data Transfer Enable (EDTEN) Setting**

### (3) DMA transfer flow

After the DMA source address register (USBDMA0/1\_SAR), DMA destination address register (USBDMA0/1\_DAR), DMA transfer count register (USBDMA0/1\_TCR), DMA channel control register (USBDMA0/1\_CHCR), final valid data transfer enable register (USBDMA0/1\_TEND), and DMA operation register (USBDMA0/1\_DMAOR) are set appropriately, the DMAC starts data transfer in the following sequence. The DMA timeout constant register (USBDMA0/1\_TOCSTR) may also need to be set.

If the transfer enabling conditions are set as DE = 1, DME = 1, TE = 0, AE = 0, SP = 0, and (TR = 0, BUF = 0, RW = 0), transfers are performed according to the transfer request enables and transfer requests from the USB-IP. The transfer direction (IN/OUT transfer) is determined by the direction signal from the USB-IP. The transfer size is determined by the setting of TS1 to TS0.

Every time one AXI transaction (in the transfer size specified in the TS bit) completes, the internal counter of this module decrements the USBDMA0/1\_TCR value by one. When the specified transfer count ends (the USBDMA0/1\_TCR value reaches 0), it means all transfers complete. At this time, an USB-DMAC interrupt is generated if the IE bit in the USBDMA0/1\_CHCR register is set to 1.

When a NULL packet is received, transfer can be stopped or restarted by setting FTE = 1 after negating the DREQE bit of the HS-USB module. Follow the steps described later in "Control when a NULL packet is received".

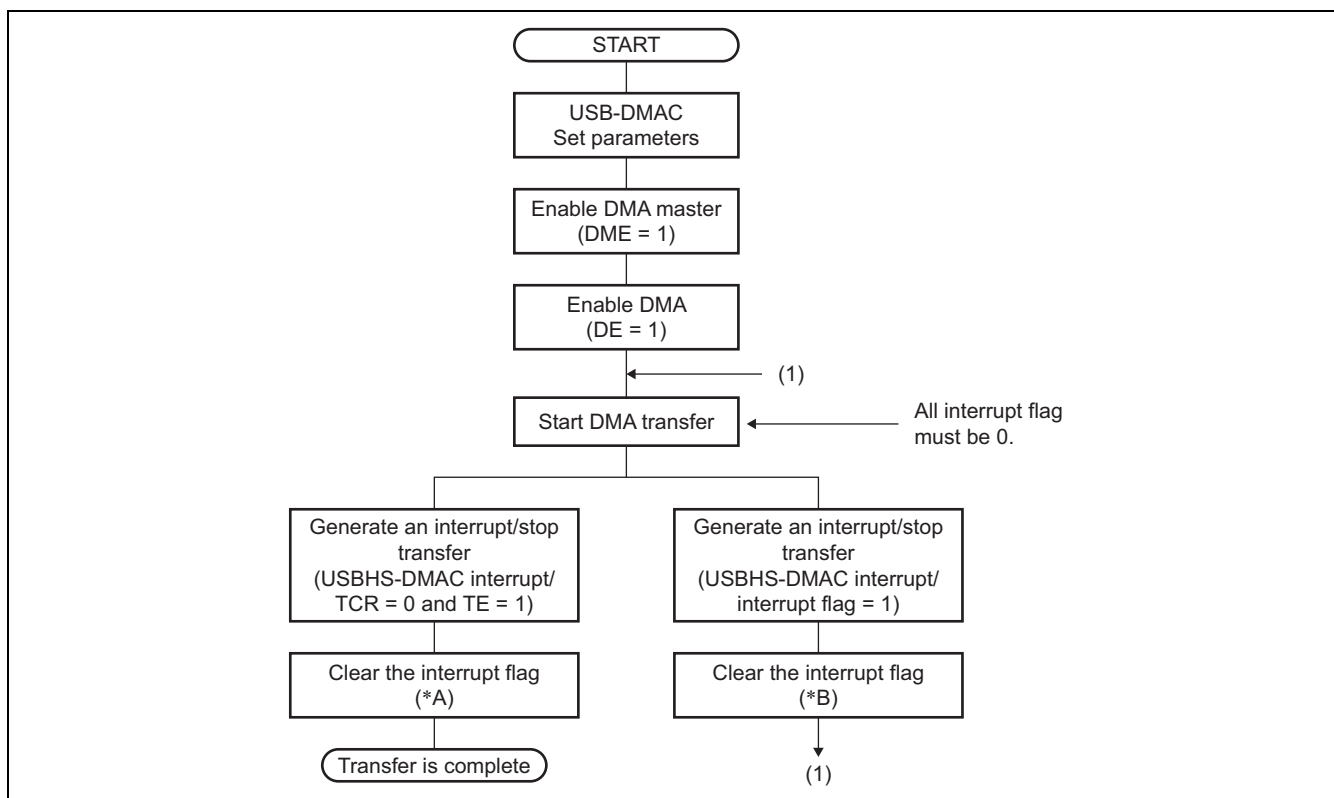
Table 53.10 shows the conditions for each DMA transfer.

**Table 53.10 DMA Transfer Conditions**

Transfer enabling condition	TE = 0, SP = 0, (*TR = 0, BUF = 0, RW = 0)
Transfer (starting) condition	When a transfer request is enabled by the USB-IP When a transfer request is issued by the USB-IP
Transfer completing (then restarting) condition	When the transfer count ends (the TE flag is set to 1), (can be restarted by setting DE and DME to 1.) When FTE = 1 (when DREQE = 1 in the HS-USB module is also set), and the steps described later should be followed. When reset (can enter into standby state by releasing the reset.)
Transfer suspending (then resuming) condition	When DE = 0 or DME = 0 (can be resumed by setting DE = 1 or DME = 1.) When SP = 1 (can be resumed by clearing the SP flag.) When RW = 1, BUF = 1, and TR = 1 (can be resumed by clearing the RW, BUF, and TR flag.)* When the module stops (can be resumed by resuming the module.)

Note: \* Can be ignored when the RWE, BUFE, and TRE bits are disabled (set to 0).

Figure 53.13 illustrates the high-level DMA transfer flow.



**Figure 53.13 DMA Transfer Flow Overview**

Where A and B apply to the following flags:

(Note that RW, BUF, and TR are not set when RWE, BUFE, and TRE are disabled, respectively.)

\* A: TE flag

\* B: SP, (RW, BUF, TR) flags

#### **When to change USBDMAC parameters**

USB-DMAC parameters (such as destination address or transfer count) should be changed while all interrupt flags are cleared and DE = 0 and DME = 0 are set (a transfer is started with the latest parameters when DME = 1 and DE = 1 are set). Furthermore, USB-DMAC parameters should not be changed while the DMA is enabled (DME = 1 and DE = 1).

#### **What to do if freeze**

If a transfer should freeze during operation, issue a software reset after setting DE = 0 and DME = 0 and clearing all interrupt flags. All hardware except configuration registers is initialized. Restart by setting DME and DE to 1 after updating USB-DMAC parameters if necessary.

#### **Control when a timeout occurs**

Since this module assumes bus access in the transfer units listed in Table 53.2, it cannot be restarted when a timeout occurs in an irregular case where it is being accessed with any size that are not in the table. This irregular case should be handled by software, such as by issuing a software reset (to both CH0 and CH1).

**Control when a NULL packet is received**

When a NULL packet is received during a DMA transfer, the DMA transfer can be suspended and resumed on each channel independently by controlling the FTE bit of this module and the DREQE bit of the HS-USB module in the following sequence.

[Control sequence]

During a DMA transfer (A)

- (1) A NULL packet is received (an interrupt is generated and the NULL flag is detected).
- (2) The DREQE bit of the HS-USB module is negated (= 0).
- (3) Wait for the internal bus to be stabilized.
- (4) Perform three actions at the same time; setting the FTE bit, clearing the NULL bit and negating the DE bit.

An interrupt is generated due to TE.

- (5) Clear the interrupt caused by TE.
- (6) Set the parameters (such as TCR or DAR) for the next transfer.
- (7) Assert the DE bit (= 1). The DMA is restarted.
- (8) Assert the DREQE bit (= 1).

Start a DMA transfer (B).

[Restrictions]

1) FTE bit set timing

If this module is accessing the AXI (SHBSYx bit = 1) when setting the FTE bit, you need to wait to set the FTE bit until this module's internal buffer is empty and the AXI bus access is complete (SHBSYx bit = 0). Note that if you accidentally set the FTE bit while an AXI bus access is in progress, the transfer fails and transfer data may be lost or the transfer may be unable to be restarted.

2) DREQE bit assert (negate clear) timing

It is necessary to allow at least  $20\text{clk}@ZS\phi$  after the DE bit is asserted and before the DREQE is asserted. This is because DREQE needs to be asserted after transfers enabled by the DE bit are ready internally to be started. Asserting DREQE immediately after DE may cause malfunction such as initiating unnecessary bus access.

3) Fractional byte and NULL packet reception

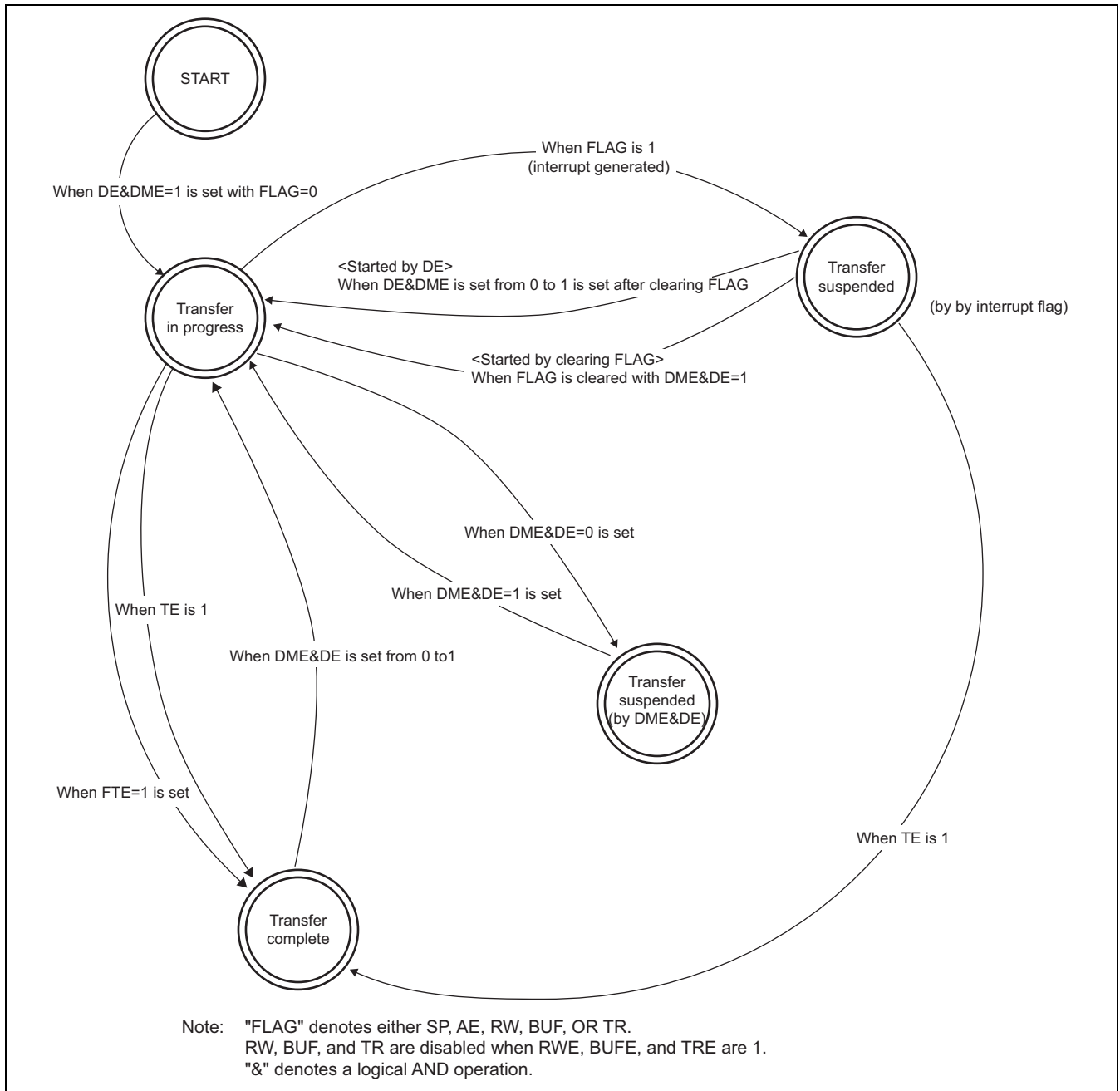
This module assumes bus access in the transfer units listed in Table 53.2 and goes out of control when it receives a NULL packet in an unsupported transfer unit. Therefore, data transfer in any transfer unit that is not in the table is prohibited.

4) IN/OUT switching after NULL packet reception

After a NULL is received, transfers cannot be restarted with the transfer direction switched from OUT to IN. This is because this module still considers the terminated transfer as an OUT transfer until the transfer count reaches its end. Note that if you switch the transfer direction to IN transfer accidentally after a NULL packet is received, a conflict occurs between an IN and an OUT transfers, which may cause illegal bus access.

Use CH0 and CH1 with their transfer direction fixed, or if the transfer direction needs to be switched on the same channel, make sure to do it every time a transfer completes successfully due to the end of transfer count or is terminated by software reset.

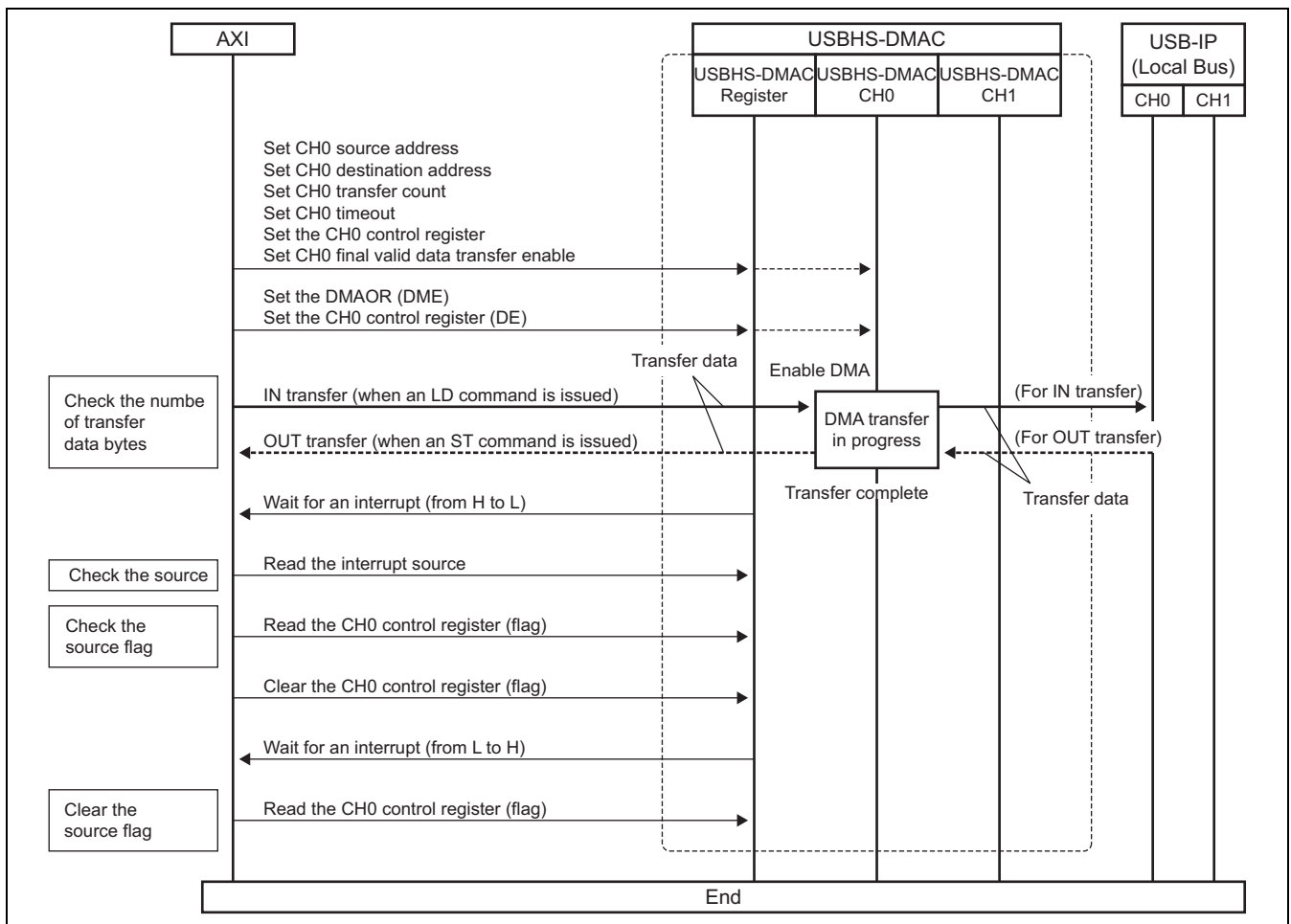
Figure 53.14 shows the state transitions for DMA transfers.



**Figure 53.14 State Transitions for DMA Transfer**

**(4) Control sequence**

Figure 53.15 shows an outline of the control sequence of this module.



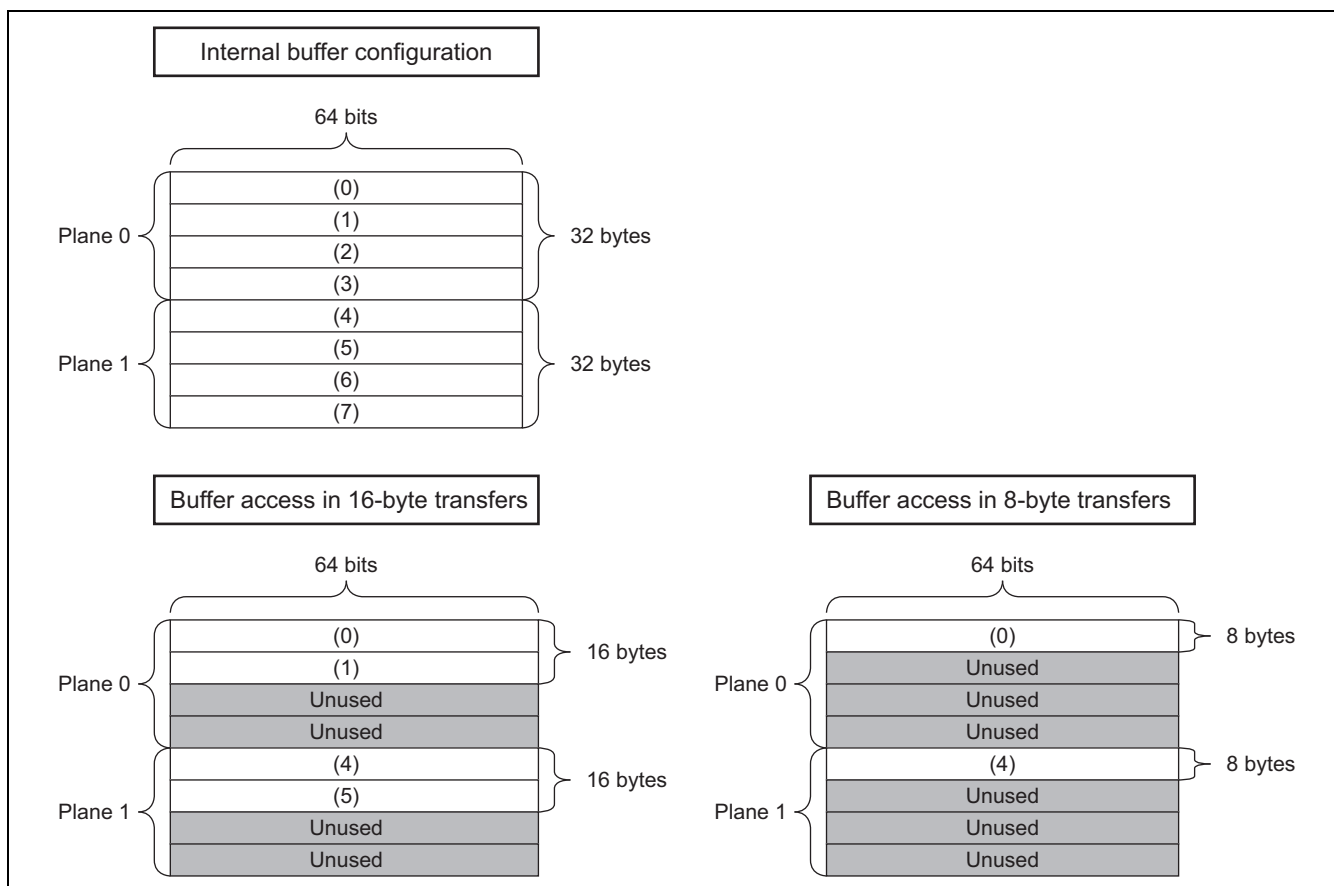
**Figure 53.15 Control Sequence Overview**

**(5) Internal buffer configuration**

This module has 64 bytes (64 bits × 8 words) of internal buffer for each of two channels. Thus, the total capacity of this module's internal buffers is 128 bytes (1,024 bits).

The internal buffers are composed of two planes each of which is organized as 64 bits × 4 words and are readable /writable on per-plane basis from the USB-IP local bus or AXI bus (plane 1 is writable when plane 0 is readable or vice versa). For 16-byte transfers, only 2 words in plane 0 and 2 words in plane 1 are used. For 8-byte transfers, only 1 word in plane 0 and 1 word in plane 1 are used.

Note that these internal buffers cannot be accessed directly by software.



**Figure 53.16 Internal Buffer Configuration and Used Area for Each Transfer Size**



**(6) Internal buffer control (hardware control, for reference)**

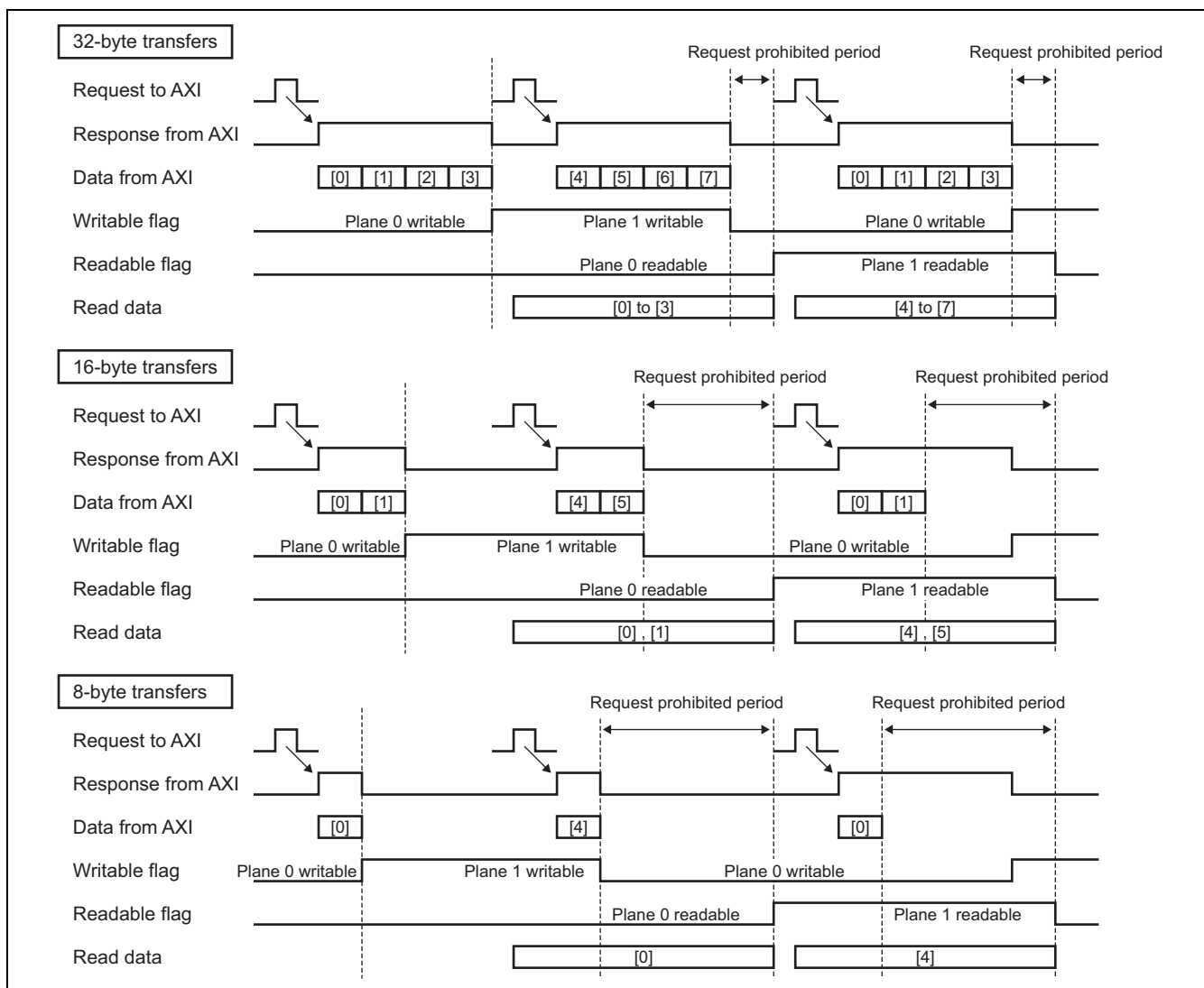
**(a) IN transfer (from AXI to USB)**

Retrieves transfer data from a source on the AXI bus and writes it to this module's internal buffer. Reads the written data from the internal buffer and writes it to the USB-IP.

Figure 53.17 shows how the planes of this module's internal buffers are controlled during an IN transfer. In this figure, "read" and "write" indicate read/write operations to this module's internal buffers.

When a write to plane 0 or plane 1 is complete, the writable plane flag is toggled (every time 2 words\* and 1 word\* are written for 16-byte and 8-byte transfers, respectively). When a read from plane 0 or plane 1 and a transfer the read data to the USB-IP are complete, the readable plane flag is toggled (every time 2 words\* and 1 word\* are read for 16-byte and 8-byte transfers, respectively). Access to the AXI is prohibited during the period when both the writable plane flag and readable plane flag are set on the same plane as a read/write access conflict may occur.

Note: \* 1 word = 64 bits



**Figure 53.17 Read/Write Control for Internal Buffer: From AXI to USB (IN Transfer)**

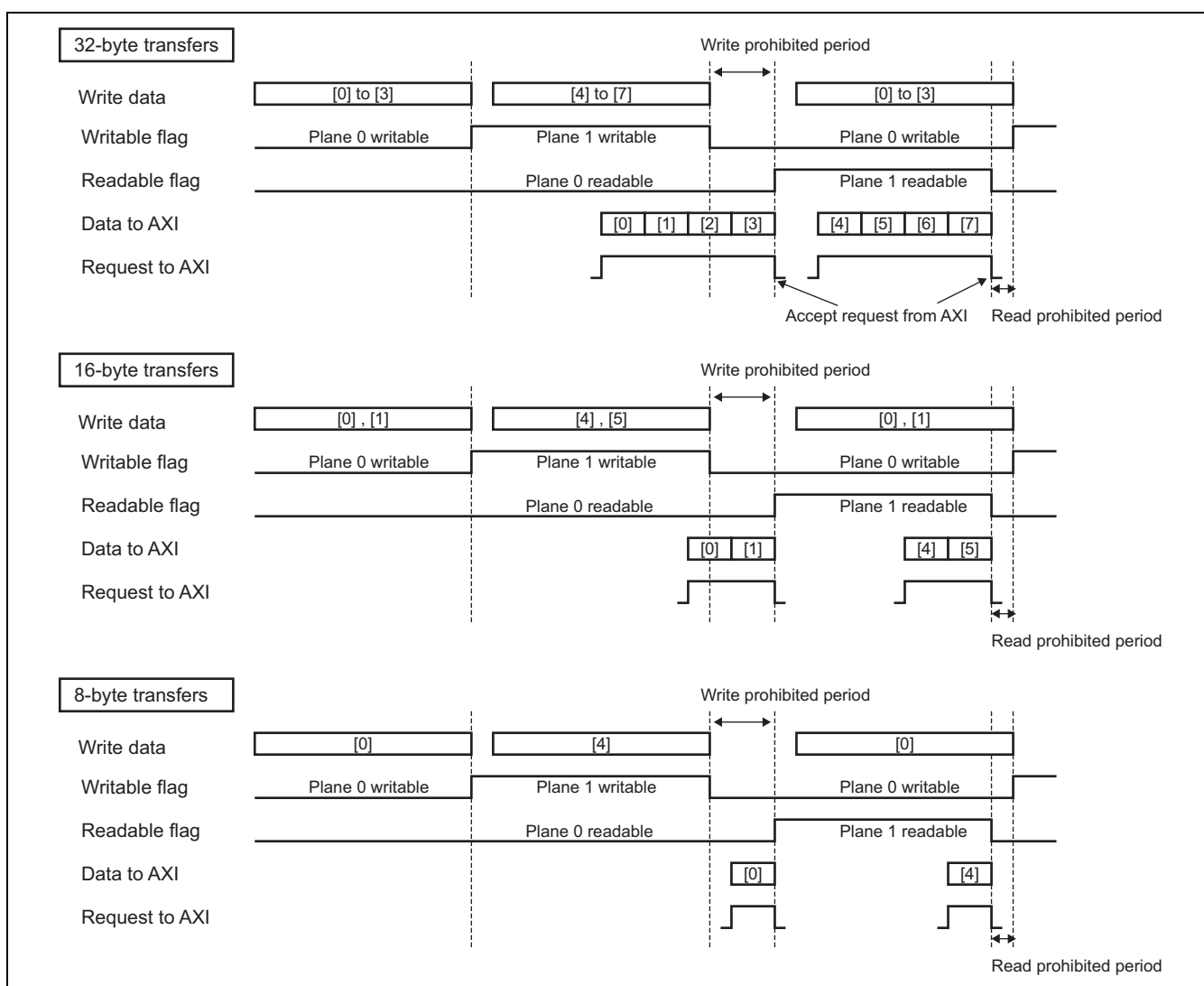
**(b) OUT transfer (from USB to AXI)**

Writes data read from the USB-IP to the internal buffers. Reads the written data from this module's internal buffers and writes it to the destination on the AXI bus (OUT transfer).

Figure 53.18 shows how the planes of this module's internal buffers are controlled during an OUT transfer. In this figure, "read" and "write" indicate read/write operations to this module's internal buffers.

When a write to plane 0 or plane 1 is complete, the writable plane flag is toggled (every time 2 words\* and 1 word\* are written for 16-byte and 8-byte transfers, respectively). When a read from plane 0 or plane 1 is complete, the readable plane flag is toggled (every time 2 words\* and 1 word\* are read for 16-byte and 8-byte transfers, respectively). Access to the AXI is prohibited during the period when both the writable plane flag and readable plane flag are set the same plane as a read/write access conflict may occur.

Note: \* 1 word = 64 bits



**Figure 53.18 Read/Write Control for Internal Buffer: From USB to AXI (OUT Transfer)**

RZ/G1H	RZ/G1N
RZ/G1M	RZ/G1E

### 53.4 DDM (Descriptor DMAC)

The DDM is a module that reconfigures the DMAC and USBDMAC. The OS on the main CPU is highly sophisticated and the overhead from interrupt notification to reconfiguration increases. To solve this problem, the DDM reconfigures the DMAC and USBDMAC in a fast response time on behalf of the CPU.

Figure 53.19 shows the relationship diagram of DDM DMAC USBDMAC connection.

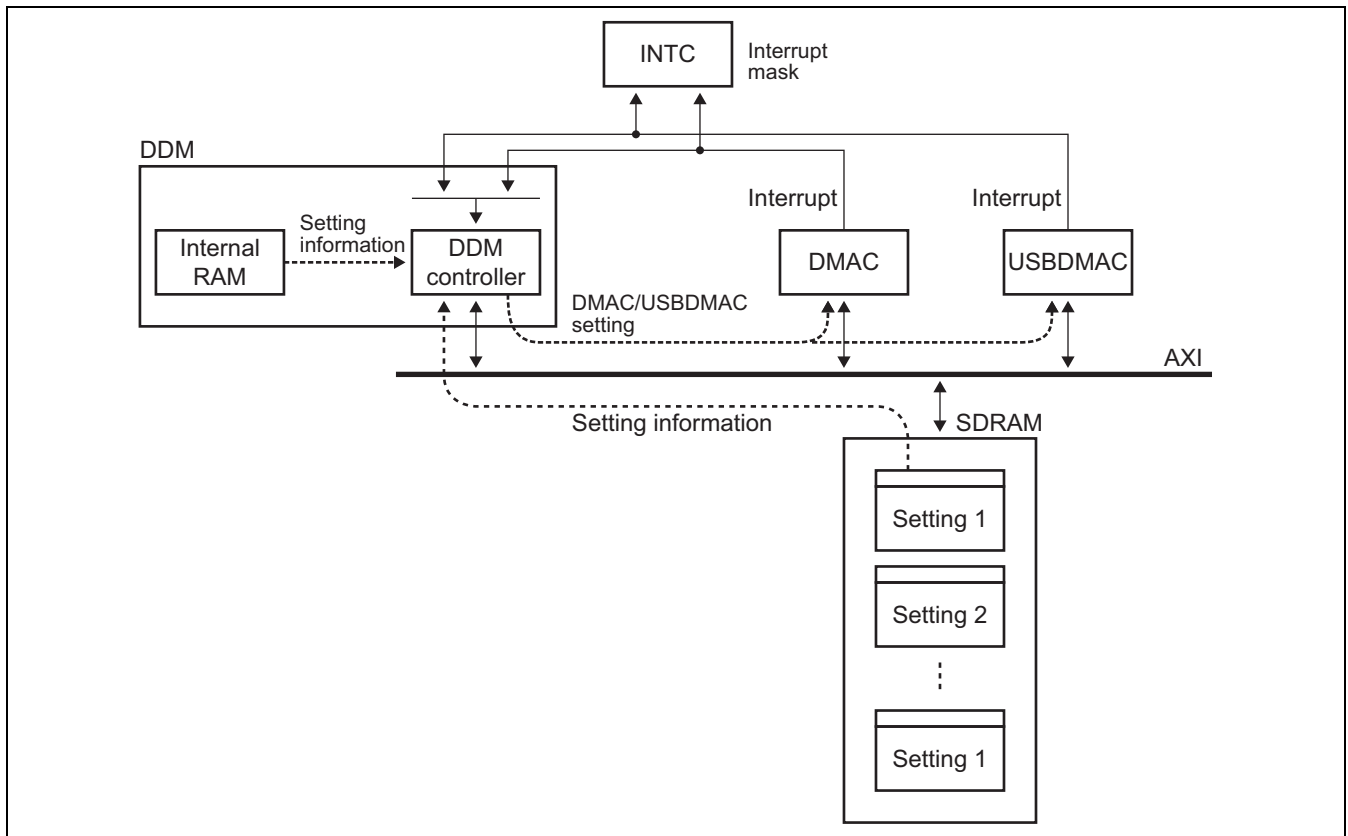


Figure 53.19 Relationship Diagram of DDM Connection

### 53.4.1 DDM Register Descriptions

Table 53.11 shows the DDM register configuration. Table 53.12 shows the register states in each operating mode.

**Table 53.11 DDM Control Registers**

Name	Register Abbreviation	R/W	Initial Value	Address	Access Size (Bits)	RZ/G Series Products			
						RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
DDM interrupt source mask register	DDIREQMSK	R/W	H'00000000	H'E65C0008	32	√	√	√	√
DDM interrupt source register	DDIREQSTA	R	H'00000000	H'E65C000C	32	√	√	√	√
DDM CH1 start source mask register 1	DDINTMSK11	R/W	H'00000000	H'E65C0038	32	√	√	√	√
DDM CH1 start source mask register 2	DDINTMSK12	R/W	H'00000000	H'E65C003C	32	√	√	√	√
DDM CH1 descriptor pointer	DDPTR1	R/W	H'00000000	H'E65C0050	32	√	√	√	√
DDM CH1 control register	DDCTRL1	R/W	H'80000000	H'E65C0054	32	√	√	√	√
DDM CH2 start source mask register 1	DDINTMSK21	R/W	H'00000000	H'E65C0068	32	√	√	√	√
DDM CH2 start source mask register 2	DDINTMSK22	R/W	H'00000000	H'E65C006C	32	√	√	√	√
DDM CH2 descriptor pointer	DDPTR2	R/W	H'00000000	H'E65C0080	32	√	√	√	√
DDM CH2 control register	DDCTRL2	R/W	H'80000000	H'E65C0084	32	√	√	√	√
DDM CH3 start source mask register 1	DDINTMSK31	R/W	H'00000000	H'E65C0098	32	√	√	√	√
DDM CH3 start source mask register 2	DDINTMSK32	R/W	H'00000000	H'E65C009C	32	√	√	√	√
DDM CH3 descriptor pointer	DDPTR3	R/W	H'00000000	H'E65C00B0	32	√	√	√	√
DDM CH3 control register	DDCTRL3	R/W	H'80000000	H'E65C00B4	32	√	√	√	√
DDM CH4 start source mask register 1	DDINTMSK41	R/W	H'00000000	H'E65C00C8	32	√	√	√	√
DDM CH4 start source mask register 2	DDINTMSK42	R/W	H'00000000	H'E65C00CC	32	√	√	√	√
DDM CH4 descriptor pointer	DDPTR4	R/W	H'00000000	H'E65C00E0	32	√	√	√	√
DDM CH4 control register	DDCTRL4	R/W	H'80000000	H'E65C00E4	32	√	√	√	√
DDM CH5 start source mask register 1	DDINTMSK51	R/W	H'00000000	H'E65C00F8	32	√	√	√	√
DDM CH5 start source mask register 2	DDINTMSK52	R/W	H'00000000	H'E65C00FC	32	√	√	√	√
DDM CH5 descriptor pointer	DDPTR5	R/W	H'00000000	H'E65C0110	32	√	√	√	√
DDM CH5 control register	DDCTRL5	R/W	H'80000000	H'E65C0114	32	√	√	√	√
DDM CH6 start source mask register 1	DDINTMSK61	R/W	H'00000000	H'E65C0128	32	√	√	√	√
DDM CH6 start source mask register 2	DDINTMSK62	R/W	H'00000000	H'E65C012C	32	√	√	√	√
DDM CH6 descriptor pointer	DDPTR6	R/W	H'00000000	H'E65C0140	32	√	√	√	√

Name	Register Abbreviation	R/W	Initial Value	Address	Access Size (Bits)	RZ/G Series Products			
						RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
DDM CH6 control register	DDCTRL6	R/W	H'80000000	H'E65C0144	32	√	√	√	√
DDM CH7 start source mask register 1	DDINTMSK71	R/W	H'00000000	H'E65C0158	32	√	√	√	√
DDM CH7 start source mask register 2	DDINTMSK72	R/W	H'00000000	H'E65C015C	32	√	√	√	√
DDM CH7 descriptor pointer	DDPTR7	R/W	H'00000000	H'E65C0170	32	√	√	√	√
DDM CH7 control register	DDCTRL7	R/W	H'80000000	H'E65C0174	32	√	√	√	√
DDM CH8 start source mask register 1	DDINTMSK81	R/W	H'00000000	H'E65C0188	32	√	√	√	√
DDM CH8 start source mask register 2	DDINTMSK82	R/W	H'00000000	H'E65C018C	32	√	√	√	√
DDM CH8 descriptor pointer	DDPTR8	R/W	H'00000000	H'E65C01A0	32	√	√	√	√
DDM CH8 control register	DDCTRL8	R/W	H'80000000	H'E65C01A4	32	√	√	√	√

**Table 53.12 Register States in Each Operating Mode**

<b>Abbreviation</b>	<b>Power-On Reset</b>	<b>Module Standby</b>
DDIREQMSK	Initialized	Retained
DDIREQSTA	Initialized	Retained
DDINTMSK11	Initialized	Retained
DDINTMSK12	Initialized	Retained
DDPTR1	Initialized	Retained
DDCTRL1	Initialized	Retained
DDINTMSK21	Initialized	Retained
DDINTMSK22	Initialized	Retained
DDPTR2	Initialized	Retained
DDCTRL2	Initialized	Retained
DDINTMSK31	Initialized	Retained
DDINTMSK32	Initialized	Retained
DDPTR3	Initialized	Retained
DDCTRL3	Initialized	Retained
DDINTMSK41	Initialized	Retained
DDINTMSK42	Initialized	Retained
DDPTR4	Initialized	Retained
DDCTRL4	Initialized	Retained
DDINTMSK51	Initialized	Retained
DDINTMSK52	Initialized	Retained
DDPTR5	Initialized	Retained
DDCTRL5	Initialized	Retained
DDINTMSK61	Initialized	Retained
DDINTMSK62	Initialized	Retained
DDPTR6	Initialized	Retained
DDCTRL6	Initialized	Retained
DDINTMSK71	Initialized	Retained
DDINTMSK72	Initialized	Retained
DDPTR7	Initialized	Retained
DDCTRL7	Initialized	Retained
DDINTMSK81	Initialized	Retained
DDINTMSK82	Initialized	Retained
DDPTR8	Initialized	Retained
DDCTRL8	Initialized	Retained

### 53.4.2 DDM Interrupt Source Mask Register (DDIREQMSK)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

The DDM Interrupt Source Mask Register enables and disables interrupt sources from the DDM.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	CM8	CM7	CM6	CM5	CM4	CM3	CM2	CM1
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ERR8	END8	ERR7	END7	ERR6	END6	ERR5	END5	ERR4	END4	ERR3	END3	ERR2	END2	ERR1	ENS1
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 24	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
23	CM8	0	R/W	Interrupt Output by CH8 Counter consistent 0: Disables interrupt output. 1: Enables interrupt output.
22	CM7	0	R/W	Interrupt Output by CH7 Counter consistent 0: Disables interrupt output. 1: Enables interrupt output.
21	CM6	0	R/W	Interrupt Output by CH6 Counter consistent 0: Disables interrupt output. 1: Enables interrupt output.
20	CM5	0	R/W	Interrupt Output by CH5 Counter consistent 0: Disables interrupt output. 1: Enables interrupt output.
19	CM4	0	R/W	Interrupt Output by CH4 Counter consistent 0: Disables interrupt output. 1: Enables interrupt output.
18	CM3	0	R/W	Interrupt Output by CH3 Counter consistent 0: Disables interrupt output. 1: Enables interrupt output.
17	CM2	0	R/W	Interrupt Output by CH2 Counter consistent 0: Disables interrupt output. 1: Enables interrupt output.
16	CM1	0	R/W	Interrupt Output by CH1 Counter consistent 0: Disables interrupt output. 1: Enables interrupt output.

Bit	Bit Name	Initial Value	R/W	Descriptions
15	ERR8	0	R/W	Interrupt Output by CH8 DDM_ERR 0: Disables interrupt output. 1: Enables interrupt output.
14	END8	0	R/W	Interrupt Output by CH8 DDM_END 0: Disables interrupt output. 1: Enables interrupt output.
13	ERR7	0	R/W	Interrupt Output by CH7 DDM_ERR 0: Disables interrupt output. 1: Enables interrupt output.
12	END7	0	R/W	Interrupt Output by CH7 DDM_END 0: Disables interrupt output. 1: Enables interrupt output.
11	ERR6	0	R/W	Interrupt Output by CH6 DDM_ERR 0: Disables interrupt output. 1: Enables interrupt output.
10	END6	0	R/W	Interrupt Output by CH6 DDM_END 0: Disables interrupt output. 1: Enables interrupt output.
9	ERR5	0	R/W	Interrupt Output by CH5 DDM_ERR 0: Disables interrupt output. 1: Enables interrupt output.
8	END5	0	R/W	Interrupt Output by CH5 DDM_END 0: Disables interrupt output. 1: Enables interrupt output.
7	ERR4	0	R/W	Interrupt Output by CH4 DDM_ERR 0: Disables interrupt output. 1: Enables interrupt output.
6	END4	0	R/W	Interrupt Output by CH4 DDM_END 0: Disables interrupt output. 1: Enables interrupt output.
5	ERR3	0	R/W	Interrupt Output by CH3 DDM_ERR 0: Disables interrupt output. 1: Enables interrupt output.
4	END3	0	R/W	Interrupt Output by CH3 DDM_END 0: Disables interrupt output. 1: Enables interrupt output.
3	ERR2	0	R/W	Interrupt Output by CH2 DDM_ERR 0: Disables interrupt output. 1: Enables interrupt output.
2	END2	0	R/W	Interrupt Output by CH2 DDM_END 0: Disables interrupt output. 1: Enables interrupt output.



Bit	Bit Name	Initial Value	R/W	Descriptions
1	ERR1	0	R/W	Interrupt Output by CH1 DDM_ERR 0: Disables interrupt output. 1: Enables interrupt output.
0	END1	0	R/W	Interrupt Output by CH1 DDM_END 0: Disables interrupt output. 1: Enables interrupt output.

### 53.4.3 DDM Interrupt Source Register (DDIREQSTA)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

The DDM Interrupt Source Register indicates the currently output interrupt source. This register is read-only. You cannot clear the interrupt source in this register. Clear the interrupt source by using the control register of each channel.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	CM8	CM7	CM6	CM5	CM4	CM3	CM2	CM1
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ERR8	END8	ERR7	END7	ERR6	END6	ERR5	END5	ERR4	END4	ERR3	END3	ERR2	END2	ERR1	ENS1
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 24	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
23	CM8	0	R	Interrupt output by CH8 Counter consistent 0: The interrupt is not output. 1: The interrupt is output.
22	CM7	0	R	Interrupt output by CH7 Counter consistent 0: The interrupt is not output. 1: The interrupt is output.
21	CM6	0	R	Interrupt output by CH6 Counter consistent 0: The interrupt is not output. 1: The interrupt is output.
20	CM5	0	R	Interrupt output by CH5 Counter consistent 0: The interrupt is not output. 1: The interrupt is output.
19	CM4	0	R	Interrupt output by CH4 Counter consistent 0: The interrupt is not output. 1: The interrupt is output.
18	CM3	0	R	Interrupt output by CH3 Counter consistent 0: The interrupt is not output. 1: The interrupt is output.
17	CM2	0	R	Interrupt output by CH2 Counter consistent 0: The interrupt is not output. 1: The interrupt is output.
16	CM1	0	R	Interrupt output by CH1 Counter consistent 0: The interrupt is not output. 1: The interrupt is output.

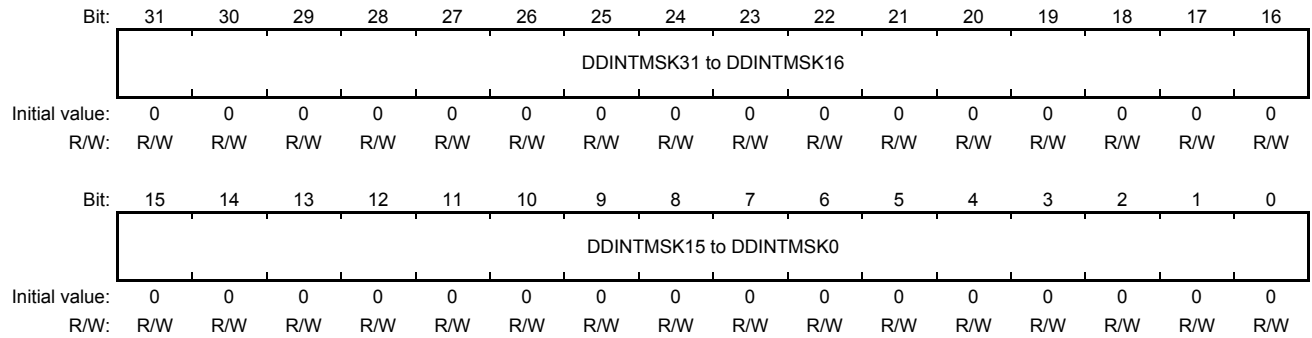
Bit	Bit Name	Initial Value	R/W	Descriptions
15	ERR8	0	R	Interrupt output by CH8 DDM_ERR 0: The interrupt is not output. 1: The interrupt is output.
14	END8	0	R	Interrupt output by CH8 DDM_END 0: The interrupt is not output. 1: The interrupt is output.
13	ERR7	0	R	Interrupt output by CH7 DDM_ERR 0: The interrupt is not output. 1: The interrupt is output.
12	END7	0	R	Interrupt output by CH7 DDM_END 0: The interrupt is not output. 1: The interrupt is output.
11	ERR6	0	R	Interrupt output by CH6 DDM_ERR 0: The interrupt is not output. 1: The interrupt is output.
10	END6	0	R	Interrupt output by CH6 DDM_END 0: The interrupt is not output. 1: The interrupt is output.
9	ERR5	0	R	Interrupt output by CH5 DDM_ERR 0: The interrupt is not output. 1: The interrupt is output.
8	END5	0	R	Interrupt output by CH5 DDM_END 0: The interrupt is not output. 1: The interrupt is output.
7	ERR4	0	R	Interrupt output by CH4 DDM_ERR 0: The interrupt is not output. 1: The interrupt is output.
6	END4	0	R	Interrupt output by CH4 DDM_END 0: The interrupt is not output. 1: The interrupt is output.
5	ERR3	0	R	Interrupt output by CH3 DDM_ERR 0: The interrupt is not output. 1: The interrupt is output.
4	END3	0	R	Interrupt output by CH3 DDM_END 0: The interrupt is not output. 1: The interrupt is output.
3	ERR2	0	R	Interrupt output by CH2 DDM_ERR 0: The interrupt is not output. 1: The interrupt is output.
2	END2	0	R	Interrupt output by CH2 DDM_END 0: The interrupt is not output. 1: The interrupt is output.

Bit	Bit Name	Initial Value	R/W	Descriptions
1	ERR1	0	R	Interrupt output by CH1 DDM_ERR 0: The interrupt is not output. 1: The interrupt is output.
0	END1	0	R	Interrupt output by CH1 DDM_END 0: The interrupt is not output. 1: The interrupt is output.

**53.4.4 DDM CHn Start Source Mask Registers 1 to 2**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

DDM CHn Start Source Mask Registers 1 to 2 mask DDM start sources.



Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 0	DDINTMSK31 to DDINTMSK0	H'0000 0000	R/W	Start Source Mask 0: Does not mask the start source. 1: Masks the start source.

The current source assignment is as follows:

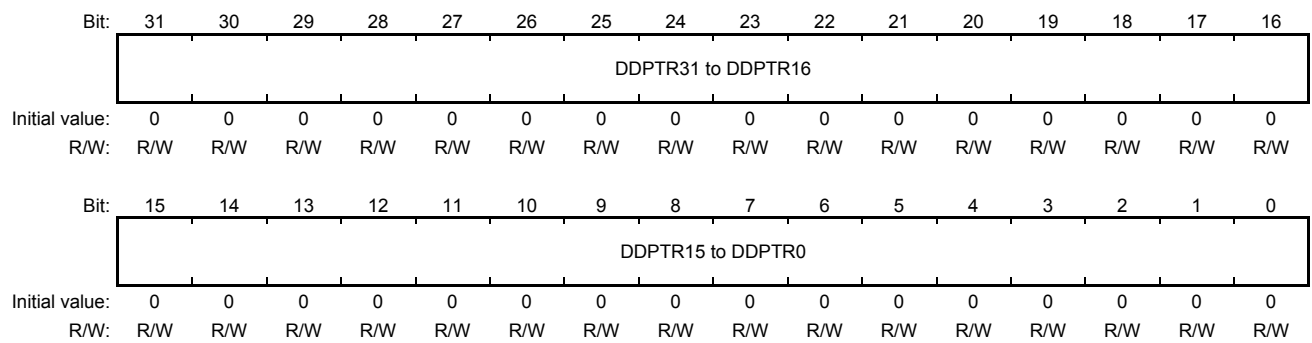
Bit Name	Bit	Assigned Start Source
DDINTMSKn	31 to 20	Reserved
(n=1,2)	19	DMACHCR19 TE bit
	18	DMACHCR18 TE bit
	17	DMACHCR17 TE bit
	16	DMACHCR16 TE bit
	15	DMACHCR15 TE bit
	14	DMACHCR14 TE bit
	13	DMACHCR13 TE bit
	12	DMACHCR12 TE bit
	11	DMACHCR11 TE bit
	10	DMACHCR10 TE bit
	9	DMACHCR9 TE bit
	8	DMACHCR8 TE bit
	7	DMACHCR7 TE bit
	6	DMACHCR6 TE bit
	5	DMACHCR5 TE bit
	4	DMACHCR4 TE bit
	3	DMACHCR3 TE bit
	2	DMACHCR2 TE bit
	1	DMACHCR1 TE bit
	0	DMACHCR0 TE bit

Bit Name	Bit	Assigned Start Source
DDINTMSKn	31 to 2	Reserved
(n=1,2)	1	USBDMAC1 Interrupt
	0	USBDMAC0 Interrupt

**53.4.5 DDM CHn Descriptor Pointer (DDPTRn)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

The DDM CHn Descriptor Pointer indicates the start address of setting code allocated onto memory.



Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 0	DDPTR31 to DDPTR0	H'0000 0000	R/W	Descriptor pointer.

### 53.4.6 DDM CHn Control Register (DDCTRLn)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

The DDM CHn Control Register controls start and stop of DDM.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PRI3 to PRI0				—	—	ENDC M	ENDC MMSK	END_NUM							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	END_CNT							—	—	—	STOP	KICK	DDM_ ERR	DDM_ END	DDE	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R/W	R/W	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 28	PRI3 to PRI0	H'0	R/W	PRI value on the AXI bus.
27, 26	—	00	R	Reserved
25	ENDCM	0	R/W	Descriptor end Counter Consistent Detection Writing 0 is possible to clear the flag. 0: Counter consistent is not detected. 1: Counter consistent is detected.
24	ENDCMMSK	0	R/W	Descriptor end Counter Consistent Detection Mask 0: Masks the ENDCM. (END_CNT is cleared to 0) 1: Does not mask the ENDCM.
23 to 16	END_NUM	All 0	R/W	Number of descriptor ends
15 to 8	END_CNT	All 0	R/W	Descriptor end Counter
7 to 5	—	000	R	Reserved
4	STOP	0	R/W	Forced Stop Function 0: Does not perform forced stop. 1: Performs forced stop.
3	KICK	0	R/W	Forced Start Function without Start Source 0: Does not perform forced start. 1: Performs forced start. This bit is automatically cleared to 0 after 1 is written.
2	DDM_ERR	0	R	Error Occurrence. The error is cleared by setting the DDE bit to 0. 0: No error occurred. 1: An error occurred.
1	DDM_END	0	R	DDM End. DDM end is cleared by setting the DDE bit to 0. 0: The DDM did not end. 1: The DDM ended.
0	DDE	0	R/W	Start Enable 0: Does not enable DDM start. 1: Enables DDM start according to the start source.

### 53.4.7 Internal RAM

Address	Area
H'FE08 0000	Register_area
H'FE08 8000	Code RAM 1 KB
H'FE08 C000	Data RAM 1.5 KB

**Figure 53.20 Internal RAM**

DDM builds in RAM. It is the 2nd page composition of Code RAM and Data RAM. DDM can access without AXI. Access size is arbitrary. In addition, a functional difference is not in both depending on the way of calling depending on which Code RAM and Data RAM were conscious of the use.

### 53.4.8 Principles of Operation

To reconfigure the DMAC by using the DDM, use the following procedure:

1. Describing setting codes
2. Starting and ending the DDM

#### (1) Describing setting codes

##### (a) Data structure

A setting code is fixed-length data consisting of four longwords.

Setting code data consists of the following fields, starting from the beginning:

Field	bit
Operation field	32 bits
Address field	32 bits
Data field	32 bits
Bit mask field	32 bits

Note: Arrange a setting code in 16 bytes boundary.



The following describes the operation field.

### (b) Operation field

The structure of the operation field is as follows:

Bit	Bit Name	Descriptions
31 to 16	HEADER	Indicates DDM setting data. H'DDDD: Normal DDM setting code Usually, set this value. H'EEEE: DDM end code Set this value when ending the channel without starting the DDM the next time. If the HEADER bits have other values, a DDM_ERR interrupt occurs. The channel of the DDM stops immediately.
15 to 8	OPERAND	Operand attribute B'00xyyzz 00: immediately 01: register 10: pointer 11: pointer (Register value) xx: Bit mask field yy: Data field zz: Address field
7 to 4	SIZE	Specify the data access size to be set. 0000: Bytes 0001: Words 0010: Longwords
3	ENDFLG	End Flag of Setting Processing Based on This Start Source 0: Continuation 1: Setting end. The DDM waits for the next start source.
2 to 0	OPC	Operation Code 000: read (cmp/eq) (read) 001: write (write) 010: rmodw (read modify write) 011: add (addition) 100: jmp/eq (branch) 101:ror (rotate right) Others: DDM_ERR interrupt occurs

The address field, data field, and bit mask field each consist of 32 bits. The data field and bit mask field use the LSB side for word- and byte-size access.

Four of register R0-R3 of longword size can be used for every Ch.

**(c) read (cmp/eq)**

The read (cmp/eq) code reads the target address and compares the address with the expected values written in the data field and bit mask field.

When the comparison result becomes true, the TFLG internal variable is set to 1. TFLG is cleared to 0 when jmp/eq is executed or operation with ENDFLG is performed.

Description example1:

The read (cmp/eq) code in this example reads the H'FE00 802C address in longwords and checks if bit 1 is set to 1.

```
H'DDDD 0020
H'FE00 802C
H'0000 0002
H'0000 0002
```

Description example2:

The read (cmp/eq) code in this example reads the R1 in longwords and checks if bit 1 is set to 1.

```
H'DDDD 0120
H'0000 0001
H'0000 0002
H'00000002
```

**(d) write**

The write code writes data to the target address.

Description example1:

The write code in this example accesses the H'FE00 802C address in longwords and writes H'0010 5400.

```
H'DDDD 0021
H'FE00 802C
H'0010 5400
H'FFFF FFFF (don't care)
```

Description example2:

The write code in this example accesses the H'FE00802C address in longwords and writes the value of H'00000001 address to H'FE00802C address.

```
H'DDDD 0821
H'FE00 802C
H'0000 0001
H'FFFF FFFF (don't care)
```

**(2) Description example3:**

The write code in this example accesses the H'FE00 802C address in longwords and writes the value of pointer of R1 to the H'FE00 802C address.

```
H'DDDD 0C21
H'FE00 802C
H'0000 0001
H'FFFF FFFF (don't care)
```

**(a) rmodw**

The rmodw code reads the target address and performs modify-write according to the values of the bit mask field.

Description example:

The rmodw code in this example reads the H'FE00 802C address in longwords and applies H'54 modify-write to bits 11 to 4.

```
H'DDDD 0022
H'FE00 802C
H'0000 0540
H'0000 0FF0
```

**(b) add**

The add code reads the target address and performs add-modify-write according to the values of the bit mask field.

Description example:

The add code in this example reads the H'FE00 802C address in longwords and applies H'200 add-modify-write to bits 11 to 0.

```
H'DDDD 0023
H'FE00 802C
H'0000 0200
H'0000 0FFF
```

Use 0 as the addition data corresponding to the area where the bit mask is 0.

**(c) jmp/eq**

If TFLG is set to 1 by the cmp/eq code, jmp/eq changes the descriptor pointer to the values of the data field. Descriptor pointer change by jmp/eq is not reflected in execution based on the next start source. Changing the descriptor pointer for the next start requires that the CHn descriptor pointer be reconfigured.

Description example:

The jmp/eq code in this example changes the descriptor pointer when TFLG is 1 to H'E558 000E.

```
H'DDDD 0024
H'0000 0000 (don't care)
H'E558 000E
H'0000 0000 (don't care)
```

**(d) ror**

The ror code reads the target address and performs rotate-right-write according to the values of the bit mask field. The shifted lower bits are rotated to higher bits. The ror command shifts according to the value of the data field.

Description example:

The ror code in this example reads the H'FE00 802C address in longwords and applies 8-bits right-shift.

```
H'DDDD 0025
H'FE00 802C
H'0000 0008
H'00FF FFFF
```

**(e) Settings description order**

Describe settings in the following order:

- (1) Clearing the start source (source output side, not the DDM start source mask register)
- (2) Changing the DDM source mask setting as required
- (3) Reconfiguring registers such as DMAC
- (4) Reconfiguring the next descriptor pointer

If several start sources are set, the last write may be unable to catch up with the next start. In such a case, end next descriptor pointer setting in (4) in read after write (do not end it in write).

**(f) Example of setting DMAC restart**

Use DDM CH1. The following shows an example of describing setting codes for reconfiguration when the TE bit of the DMAC1 CH0 channel control register is HI.

```
//TE bit read
H'DDDD 0020
H'FE00 802C
H'0000 0002
H'0000 0002
//TE bit clear
H'DDDD 0021
H'FE00 802C
H'0010 5400
H'FFFF FFFF
//SAR setting
H'DDDD 0021
H'FE00 8020
H'5800 0000
H'FFFF FFFF
//DAR setting
H'DDDD 0021
H'FE00 8024
H'0000 0000
H'FFFF FFFF
//TCR setting
H'DDDD 0021
```

```

H'FE00 8028
H'0000 0010
H'FFFF FFFF
//DE bit write. DMA start
H'DDDD 0021
H'FE00 802C
H'0010 5401
H'FFFF FFFF
//Next descriptor pointer write.
H'DDDD 0021
H'E65C 0050
H'5800 02D0
H'FFFF FFFF
// Setting end by this start. (dummy read)
H'DDDD 0028
H'E65C 0050
H'0000 0000
H'0000 0000

```

### (3) Start and end

#### (a) Starting the DDM

Make necessary settings in the DDM.

- Enabling interrupt output as required
  - Setting a DDM start source
    - Setting a descriptor pointer

After setting the above, set the DDM Enable bit of the DDM control register to 1 to enable DDM start.

Setting example:

```

Enable the interrupt by DDM CH1 end.
  Address: H'E65C 0008 Write data: H'0000 0001
Enable DDM CH1 start when the DMAC1 TE bit is changed.
  Address: H'E65C 0030 Write data: H'0000 1000
Set the DDM CH1 descriptor pointer to H'5800 0210.
  Address: H'E65C 0050 Write data: H'5800 0210
Enable DDM CH1 start.
  Address: H'E65C 0054 Write data: H'0000 0001

```

Set the KICK bit to forced start after setting the DDM Enable bit to 1. Do not set these bits at the same time.

#### (b) Ending the DDM

When the DDM ends, the DDM\_END bit is set to 1. DDM end is cleared by setting the DDE bit to 0. To restart the DDM, you must clear the DDM\_END bit by setting the DDE bit to 0.

Procedure for stopping the DDM by the STOP bit

```

Set the STOP bit to 1. Keep the DDE bit at 1.
Check that the DDM_END bit is 1.
Set the DDE bit to 0.

```

## 54. USB3.0 Host Controller

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

### 54.1 Introduction

The USB3.0 host controller is compliant with the Universal Serial Bus (USB) 3.0 Specifications.

It uses AXI interconnection, which is a system interface that is based on the AMBA® AXI Protocol v1.0 Specification.

The USB3.0 host controller supports super speed (5 Gbps), high speed (480 Mbps), full speed (12 Mbps) and low speed (1.5 Mbps).

**Table 54.1 Supported Speed Type**

Speed Type	High Speed	Full Speed	Low Speed
Super Speed	√	√	√

Also, the USB3.0 host controller is compliant with battery charging.

It is based on the eXtensible Host Controller Interface for the Universal Serial Bus (xHCI) Specification as a host controller interface.

The USB3.0 host controller requires to download FW to operate as a host (see section 54.4.1, FW Download). Contact Renesas to obtain the FW.

#### 54.1.1 Features

The functions of the USB3.0 host controller are listed below.

The USB3.0 host controller has one USB port, one AXI master, and one AXI slave.

##### (1) USB3.0 Host Controller Function

###### [USB Function]

###### Compliant with Universal Serial Bus 3.0 Specification Revision 1.0

- Supports one downstream port. USB2.0 port implements a 50-ohm resistance.
- Supports control, bulk, interrupt, and isochronous transfers.
- Supports all USB bus speeds, USB 3.0 super speed (5 Gbps), high speed (480 Mbps), full speed (12 Mbps) and low speed (1.5 Mbps).
- Supports power control and overcurrent detection
- Supports BIOS USB.
  - Pre-OS and OS hand-off
  - xHCI legacy support control
- Implements the USB2.0ECN USB 2.0 Link Power Management Addendum and LPM function that is compliant with the xHCI specification.
- Supports polarity inversion of USB3.0 SS differential data pin pair.

**Has the following capabilities that are compliant with the eXtensible host controller interface for Universal Serial Bus Specification Revision 1.0.**

- 64-bit addressing capability
- BW negotiation capability
- Port power control
- Latency tolerance message capability
- xHCI host capability
  - Number of device slots (MaxSlots): 32
  - Number of total endpoints: 128
  - Number of stream IDs (MaxPSASize): 32 per endpoint (1 EP for reserved bit)
  - Number of event ring segment tables: 2 (max. 512 events/ring) (ERST Max = 1)
  - Supported page size: 4 Kbytes
  - Context size: 64 bytes
- Debug Port
  - Supports debug port compliant with xHCI debug capability

**[Battery Charging]**

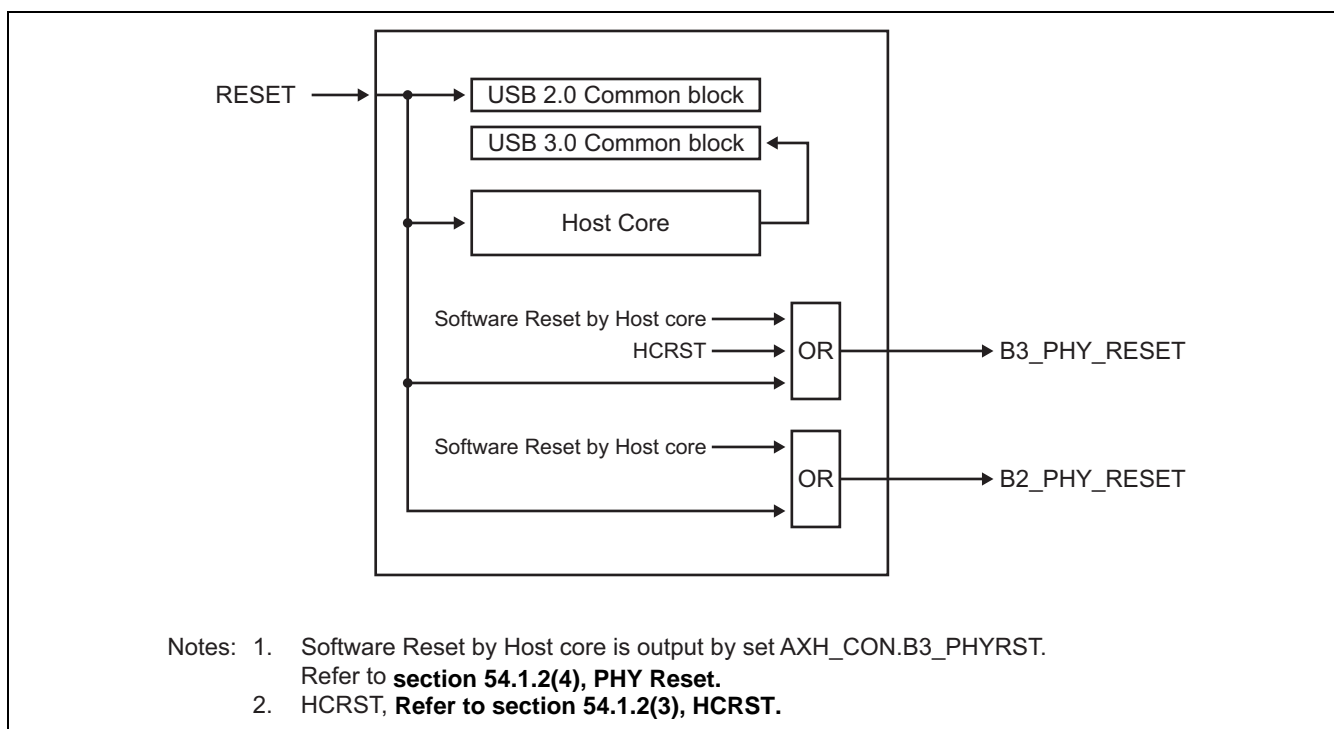
Supports the following modes that are compliant with Battery Charging Specification Revision 1.2

**Charging port device**

- Standard downstream port mode (SDP)
- Charging downstream port mode (CDP)
- Dedicated charging port mode (DCP)

### 54.1.2 Reset

The USB3.0 host controller reset diagram is provided below.



**Figure 54.1 Reset Diagram**

#### (1) Reset Operation

- When the power is on or host core is reset, RESET is asserted.
- The reset is deasserted when USB2.0PLL becomes stable because reset synchronization is cleared.

#### (2) Reset in Cold Boot

- During cold boot and when the power is on, RESET is asserted.
- The reset is deasserted when USB2.0 PLL becomes stable because reset synchronization is cleared.

#### (3) HCRST

- The host controller reset (HCRST) is operated when the USBCMD.HCRST bit is set to 1 by Driver, after which the USBSTS.HCH bit (HCHalted bit) will be 0.
- When HCRST is set, Host core is reset by FW, and initialized.

#### (4) PHY Reset

The B3\_PHY\_RESET is used for a reset of USB3.0 PHY, and the B2\_PHY\_RESET is used for a reset of USB2.0 PHY. Each PHY reset signal is generated by reset signals from the host core.

When Host role, if the bit [16] B3\_PHYRST/ [0] B2\_PHYRST of AXI host control register [H'100 to H'104] is set, B3\_PHY\_RESET/ B2\_PHY\_RESET is output to USB3.0PHY/ USB2.0PHY.



**Table 54.2 B3\_PHY\_RESET and B2\_PHY\_RESET**

USB3.0 Host Controller	Register Setting	Reset Signal Behavior
Host core	AXH_CON.B3_PHYRST = 1	The value of B3_PHYRST is output to B3_PHY_RESET signal.
	AXH_CON.B2_PHYRST = 1	The value of B2_PHYRST is output to B2_PHY_RESET signal.

**Table 54.3 Resources of B3\_PHY\_RESET and B2\_PHY\_RESET**

	(1) Software Reset	(2) HCRST	RESET
B3_PHY_RESET	√	√	√
B2_PHY_RESET	√	—	√

### 54.1.3 Shared Port Configuration

USB3.0 host controller share HS/FS/LS transceiver with USB2.0 Ch.2. Set USB2SEL bit in UGCTRL2 register to enable USB3.0. Refer to section 52.2.38, USB General Control Register 2 (UGCTRL2).

USB 3.0's external pins shares SATA0's ones. When mode pin is selected the following value, USB 3.0 is enabled.

- In the case of RZ/G1H or RZ/G1M, MD23 = 1.
- In the case of RZ/G1N, MD23 =1, MD24 = 0

**Table 54.4 External Pins**

Pin Name	I/O	Description	RZ/G Series Products			
			RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
RIDP0_USB3	Differential Input	SuperSpeed receiver serial data inputs (pos)	√	√	√	—
RIDN0_USB3	Differential Input	SuperSpeed receiver serial data inputs (neg)	√	√	√	—
TODP0_USB3	Differential Output	SuperSpeed transmitter serial data outputs (pos)	√	√	√	—
TODN0_USB3	Differential Output	SuperSpeed transmitter serial data outputs (neg)	√	√	√	—
CICREFP0_USB3	Differential Input	100 MHz Reference Clock (pos)	√	√	√	—
CICREFN0_USB3	Differential Input	100 MHz Reference Clock (neg)	√	√	√	—

## 54.2 Register Specification

RZ/G1H	RZ/G1N
RZ/G1M	RZ/G1E

### 54.2.1 Register Attributes

**Table 54.5 Register Bit-field types**

Register Attribute	Description
R/W	Register bits can be read and written.
RW1C	Register bits can be read. A clear bit may be set by writing "1"; writing 0 to RW1C bits has no effect.
RWT	Register bits can be read. An inversion bit may be set by writing "1"; writing 0 to RWT bits has no effect.
RW1S	Register bits can be read and written. A bit may be set to 1 by writing "1"; writing 0 to RW1S bits has no effect.
R	Register bits can only be read.
W	Register bits can only be written.
Reserved	Reserved bits are Read Only field.

### 54.2.2 Register Overview

Register groups in host cores are consisted of following registers.

- AXI Register
- xHCI Register

CLK60 shall be supplied to host core when user reads or writes valid value at host register.

### 54.2.3 USB3.0 Address Mapping

#### 54.2.3.1 Address Mapping

Base address is H'EE00 0000. Following sections describe only offset address from the base address.

AXI Address	Register Name	Reference Section
H'0000	xHCI Capability Register	54.2.3.3 xHCI Register Overview
H'0020	xHCI Operational Register	
H'005C	Reserved	
H'0100	AXI Host Control Register	54.2.3.2 AXI Register Overview
H'0108 to H'01FF	Reserved	
H'0200 to H'029F	AXI Register	54.2.3.2 AXI Register Overview
H'02A0 to H'041F	Reserved	
H'0420	PORT Status&Control Register	54.2.3.3 xHCI Register Overview
H'0438 to H'04FF	Reserved	
H'0500	Extended Capability Register	54.2.3.3 xHCI Register Overview
H'0598 to H'05FF	Reserved	
H'0600	xHCI Runtime Register	54.2.3.3 xHCI Register Overview
H'0644 to H'07FF	Reserved	
H'0800	Host ControllerDoorbell Register	54.2.3.3 xHCI Register Overview
H'0884 to H'09FF	Reserved	
H'0A00 to H'0BFF	AXI Host Control Register	54.2.3.2 AXI Register Overview

**Figure 54.2 Address Map**

**54.2.3.2 AXI Register Overview**

AXI Offset

H'100  
H'104  
H'108  
...  
H'200  
H'204  
H'208  
H'20C  
H'210  
H'214  
H'218  
H'21C  
H'220  
H'224  
H'228  
H'22C  
H'230  
H'234  
H'238  
H'23C  
H'240  
H'244  
H'248  
H'24C  
H'250  
H'254  
H'258  
H'25C  
H'260 to H'284  
H'288  
H'28C  
H'290  
H'294  
H'298  
H'29C  
H'A00 to H'A40  
H'A44  
H'A48  
H'A4C to H'A58  
H'A5C  
H'A60 to H'AA4  
H'AA8  
H'AAC  
H'AB0  
H'AB4  
H'AB8  
H'ABC to H'BFF

AXI Host Control Register		
AXI Host Control Status Register		
Reserved		
Reserved		
Class Code		Revision ID
Reserved		
Reserved		
Reserved	FLADJ	SBRN
Reserved		
Reserved		
Reserved		
Reserved		Interrupt
Reserved		Enable
LTR		
Reserved		
Battery Charging		
Reserved		
Reserved		
Reserved		
FW Version		
Reserved		
Reserved		
Reserved		
FW DOWNLOAD Control & Status		
Reserved		
FW Data0		
FW Data1		
Reserved		
Renesas Private Register		
Renesas Private Register		
Core Control3		
Renesas Private Register		
VENDOR_CON_SET		
VENDOR_CON_STA		
Reserved		
LCLK Select Register		
USB3.0 Configuration1		
Reserved		
USB3.0 Configuration2		
Reserved		
USB3.0 Configuration3		
Reserved		
USB3.0 RX Polarity		
Reserved		
USB3.0 TX Polarity		
Reserved		

**Figure 54.3 AXI Register Overview**

## 54.2.3.3 xHCI Register Overview

		Offset	3	2	1	0	HW default value		
eXtensible Host Controller Capability		H'000	HCIVERSION		Reserved	CAPLENGTH	0100_0020		
		H'004	HCSPARAMS1					0200_0120	
		H'008	HCSPARAMS2					2400_0011	
		H'00C	HCSPARAMS3					0000_0000	
		H'010	HCCPARAMS					0140_51CF	
		H'014	DBOFF					0000_0800	
		H'018	RTSOFF					0000_0600	
		H'01C	Reserved						
	Host Controller Operational		H'020	USBCMD					0000_0000
			H'024	USBSTS					0000_0801
		H'028	PAGESIZE					0000_0001	
		H'02C	Reserved						
		H'030	Reserved						
		H'034	DNCTRL					0000_0000	
		H'038	CRCRL					0000_0000	
		H'03C	CRCRH					0000_0000	
		H'040	Reserved						
		H'044	Reserved						
		H'048	Reserved						
		H'04C	Reserved						
		H'050	DCBAAPL					0000_0000	
		H'054	DCBAAPH					0000_0000	
		H'058	CONFIG					0000_0000	
		H'05C	Reserved						
Port Status and Control		Port1(SS)	H'420	PORTSC					0000_02A0
	Port1(SS)	H'424	PORTPMSC					0000_0000	
	Port1(SS)	H'428	PORTLI					0000_0000	
		H'42C	Reserved						
	Port2(U2)	H'430	PORTSC					0000_02A0	
	Port2(U2)	H'434	PORTPMSC					0000_0000	
		H'438	Reserved						
		H'43C	Reserved						
xHCI Extended Capabilities		H'500	USBLEGSUP					0000_0401	
		H'504	USBLEGCTLSTS					0000_0000	
		H'508	Reserved						
		H'50C	Reserved						
		H'510	xHCI Supported Protocol Capability (USB 3.0)					0300_0602	
		H'514						2042_5355	
		H'518						0000_0101	
		H'51C	Reserved						

	Offset	3	2	1	0	HW default value	
xHCI Extended Capabilities	H'520	PSI (SuperSpeed)				0000_0000	
	H'524	Reserved					
	H'528	xHCI Supported Protocol Capability (USB 2.0)				0200_0802	
	H'52C					2042_5355	
	H'530					0000_0102	
	H'534	Reserved					
	H'538	PSI (Full-Speed)				0000_0000	
	H'53C	PSI (Low-Speed)				0000_0000	
	H'540	PSI (High-Speed)				0000_0000	
	H'544	Reserved					
	Extended Power Management Capability	H'548	PMC		Nextlte mPtr	Cap_ID	4803_0203
		H'54C	Reserved		PMCSR		0000_0008
H'550		Vender Defined Capability				0000_04C0	
H'554		Command Enable				0000_0000	
H'558		Reserved					
H'55C		Reserved					
H'560		DCID				0000_000A	
H'564		DCDB				0000_0000	
H'568		DCERSTSZ				0000_0000	
H'56C		Reserved					
H'570		DCERSTBA0				0000_0000	
H'574		DCERSTBA1				0000_0000	
H'578		DCERDP0				0000_0000	
H'57C		DCERDP1				0000_0000	
H'580		DCCTRL				0000_0000	
H'584		DCST				0000_0000	
H'588		DCPORTSC				0000_0080	
H'58C		Reserved					
H'590		DCCP0				0000_0000	
H'594		DCCP1				0000_0000	
H'598		Reserved					
H'59C		Reserved					
Host Controller Runtime		H'600	MFINDEX				0000_0000
		H'604	Reserved				
		H'608	Reserved				
		H'60C	Reserved				
		H'610	Reserved				
		H'614	Reserved				
	H'618	Reserved					
	H'61C	Reserved					
	INT #0	H'620	IMAN				0000_0000
	INT #0	H'624	IMOD				0000_0FA0
	INT #0	H'628	ERSTSZ				0000_0000

			3	2	1	0	HW default value
Host Controller Runtime	INT #0	H'62C	Reserved				
	INT #0	H'630	ERSTBA				0000_0000
		H'634					0000_0000
	INT #0	H'638	ERDP				0000_0000
		H'63C					0000_0000
Host Controller Doorbell		H'800	Doorbell Registers (CmdRing)				0000_0000
		H'804	Doorbell Registers (Slot #0)				0000_0000
		H'808	Doorbell Registers (Slot #1)				0000_0000
		H'80C	Doorbell Registers (Slot #2)				0000_0000
		H'810	Doorbell Registers (Slot #3)				0000_0000
		H'814	Doorbell Registers (Slot #4)				0000_0000
		H'818	Doorbell Registers (Slot #5)				0000_0000
		H'81C	Doorbell Registers (Slot #6)				0000_0000
		H'820	Doorbell Registers (Slot #7)				0000_0000
		H'824	Doorbell Registers (Slot #8)				0000_0000
		H'828	Doorbell Registers (Slot #9)				0000_0000
		H'82C	Doorbell Registers (Slot #10)				0000_0000
		H'830	Doorbell Registers (Slot #11)				0000_0000
		H'834	Doorbell Registers (Slot #12)				0000_0000
		H'838	Doorbell Registers (Slot #13)				0000_0000
		H'83C	Doorbell Registers (Slot #14)				0000_0000
		H'840	Doorbell Registers (Slot #15)				0000_0000
		H'844	Doorbell Registers (Slot #16)				0000_0000
		H'848	Doorbell Registers (Slot #17)				0000_0000
		H'84C	Doorbell Registers (Slot #18)				0000_0000
		H'850	Doorbell Registers (Slot #19)				0000_0000
		H'854	Doorbell Registers (Slot #20)				0000_0000
		H'858	Doorbell Registers (Slot #21)				0000_0000
		H'85C	Doorbell Registers (Slot #22)				0000_0000
		H'860	Doorbell Registers (Slot #23)				0000_0000
		H'864	Doorbell Registers (Slot #24)				0000_0000
		H'868	Doorbell Registers (Slot #25)				0000_0000
		H'86C	Doorbell Registers (Slot #26)				0000_0000
		H'870	Doorbell Registers (Slot #27)				0000_0000
		H'874	Doorbell Registers (Slot #28)				0000_0000
		H'878	Doorbell Registers (Slot #29)				0000_0000
		H'87C	Doorbell Registers (Slot #30)				0000_0000
	H'880	Doorbell Registers (Slot #31)				0000_0000	
		H'884	Reserved				
		H'888	Reserved				
		H'88C	Reserved				

Figure 54.4 xHCI Register Map



### 54.3 Register Description

#### 54.3.1 AXI Register

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

##### 54.3.1.1 AXI Host Control Register

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	B3_PHYRST
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	SYS_SUSPEND	—	—	—	—	—	—	—	B2_PHYRST
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 17	—	All 0	R	Reserved
16	B3_PHYRST	0	R/W	Bit for reset USB3.0 PHY. 0: Normal condition 1: Reset condition
15 to 9	—	All 0	R	Reserved
8	SYS_SUSPEND	0	R/W	Bit for setting Suspend USB2.0 PHY (PLL stops) by system. 0: Normal condition 1: Suspend condition (USB2PHY PLL stops)
7 to 1	—	All 0	R	Reserved
0	B2_PHYRST	0	R/W	Bit for reset USB2.0 PHY. 0: Normal condition 1: Reset condition

### 54.3.1.2 AXI Host Control Status Register

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	SS_DISABLE	—	—	—	—	—	—	—	B3_PLL_ACTIVE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	B2_PLL_ACTIVE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 25	—	All 0	R	Reserved
24	SS_DISABLE	0	R	Bit for showing SuperSpeed (SS) Port is disabled. The USB3.0 host controller core doesn't support SS port when this bit is 1.
23 to 17	—	All 0	R	Reserved
16	B3_PLL_ACTIVE	0	R	Bit for showing that USB3PHY PLL is locked or not. When this bit is 0, it means USB3.0 function is not able to use because valid clock is not output from USB3.0 PHY during USB3PHY PLL is unlocked. 0: PLL Unlock (USB3PHY Clock is invalid) 1: PLL Lock (USB3PHY Clock is valid)
15 to 1	—	All 0	R	Reserved
0	B2_PLL_ACTIVE	0	R	Bit for showing that USB2PHY PLL is locked or not. When this bit is 0, it means USB2.0 function is not able to use because valid clock is not output from USB2.0 PHY during USB2PHY PLL is unlocked. 0: PLL Unlock (USB2PHY Clock is invalid) 1: PLL Lock (USB2PHY Clock is valid)

### 54.3.1.3 Revision ID

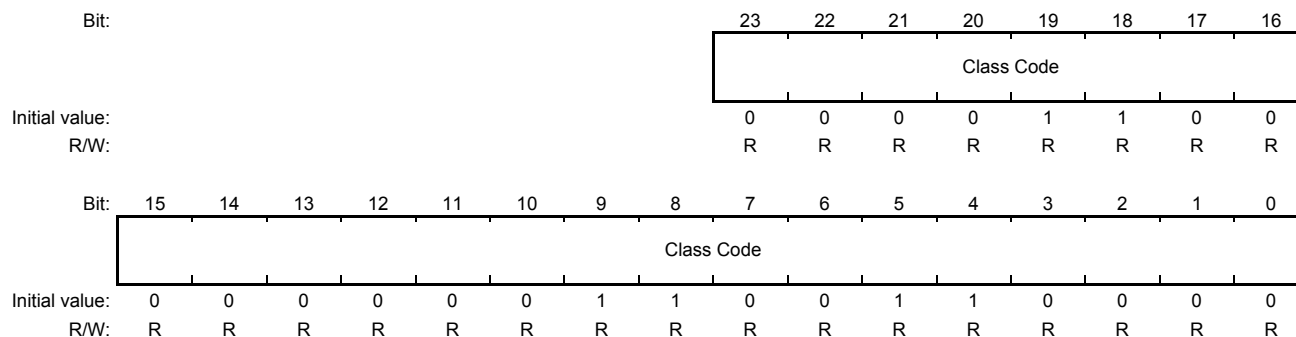
Register displaying Revision ID.

Bit:	7	6	5	4	3	2	1	0
	Revision ID							
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
7 to 0	Revision ID	—	R	Renesas management number

#### 54.3.1.4 Pseudo PCI Class Code

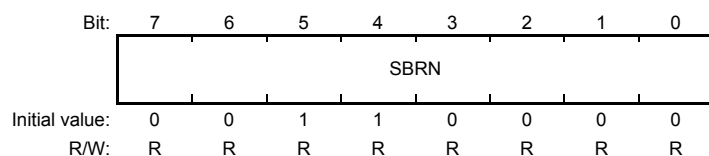
Pseudo register corresponding to PCI class code. This register's value doesn't influence the performance of the AXH block or USB3.0 host controller core.



Bit	Bit Name	Initial Value	R/W	Description
23 to 0	Class Code	H'0C 0330	R	Device Type and Function Base Class: Serial Bus Controller (H'0C) Sub Class: Universal Serial Bus Host Controller (H'03) Program Interface: USB3.0 Host Controller (H'30)

#### 54.3.1.5 Serial Bus Release Number

Register corresponding to the Serial Bus Release Number Register specified in the xHCI specification.

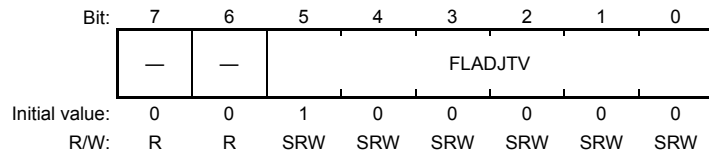


Bit	Bit Name	Initial Value	R/W	Description
7 to 0	SBRN	H'30	R	Serial Bus Release Number Version of universal serial bus specification that is compliant with host controller. H'30: Release 3.0

### 54.3.1.6 Frame Length Adjustment

Register corresponding to the frame length adjustment register specified in the xHCI specification.

This register is used for adjustment of the frame length in USB3.0 host controller core. Only in the HC halted state, write is valid.



Bit	Bit Name	Initial Value	R/W	Description
7, 6	—	All 0	R	Reserved
5 to 0	FLADJTV	H'20	SRW	Frame Length Adjustment Register (FLADJ) Timing Value Adjust SOF counter Clock. H'20: Frame Length 60,000 $SOF\ cycle\ time = 59,488 + (Register\ setting\ value \times 16\ high\ speed\ bit)$

54.3.1.7 Host Interrupt

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	SMI_S TA	LTM_S TA	HSE_S TA	PME_S TA	XHC_S TA
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	RWC	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 5	—	All 0	R	Reserved
4	SMI_STA	0	R	SMI Interrupt Status bit. When an SMI interrupt occurs, this bit is set to 1.
3	LTM_STA	0	RWC	LTM Interrupt status bit. When an LTM interrupt occurs, this bit is set to 1 by FW. AXI sets 1 to clear the bit.
2	HSE_STA	0	R	HSE Interrupt Status bit. When USBSTS.HSE = 1 & USBCMD.HSEE = 1, this bit is set to 1. AXI sets 1 to clear the bit.
1	PME_STA	0	R	PME Interrupt Status bit. When PME_STA = 1 & PME_ENA = 1, this bit is set to 1.
0	XHC_STA	0	R	xHCI Interrupt Status bit. When EventRing is updated and then the INT signal, which indicates asserting of the interrupt in the core, is detected, this bit is set to 1.  When the INT signal, which indicates deasserting of the interrupt in the core, is detected, this bit is set to 0 and cleared.

## 54.3.1.8 Host Interrupt Enable

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	SMI_E NA	LTM_E NA	HSE_E NA	PME_E NA	XHC_E NA
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 5	—	All 0	R	Reserved
4	SMI_ENA	0	R/W	When this bit is set to 1, SMI_STA interrupt is valid.
3	LTM_ENA	0	R/W	When this bit is set to 1, LTM_STA interrupt is valid.
2	HSE_ENA	0	R/W	When this bit is set to 1, HSE_STA interrupt is valid.
1	PME_ENA	0	R/W	When this bit is set to 1, PME_STA interrupt is valid.
0	XHC_ENA	0	R/W	When this bit is set to 1, XHC_STA interrupt is valid.

## 54.3.1.9 LTR

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Requirement	—	—	Latency Scale			Maximum No-Snoop Latency Value									
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Requirement	—	—	Latency Scale			Maximum Snoop Latency Value									
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31	Requirement	0	R	Requirement (No-Snoop)
30, 29	—	All 0	R	Reserved
28 to 26	Latency Scale	000	R	Latency Scale (No-Snoop)
25 to 16	Maximum No-Snoop Latency Value	H'000	R	Latency Value (No-Snoop)
15	Requirement	0	R	Requirement (No-Snoop)
14, 13	—	All 0	R	Reserved
12 to 10	Latency Scale	000	R	Latency Scale (No-Snoop)
9 to 0	Maximum Snoop Latency Value	H'000	R	Latency Value (No-Snoop)

### 54.3.1.10 Battery

Register for setting Battery Charging operational Mode.

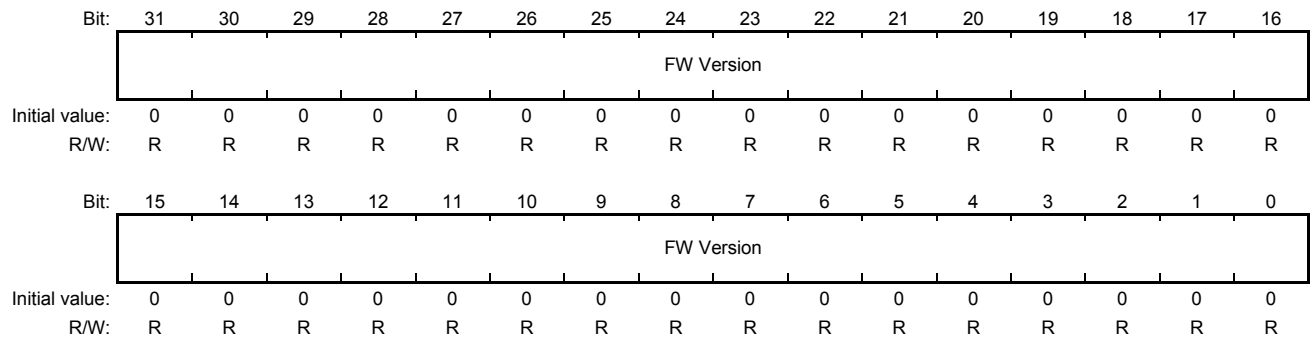
Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	PTPWE R_CTRL	—	—	—	—	—	—	Renesas Private field	
Initial value:	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R	R	R	R	R	R	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	LCLK_NONSTOP_FREQ		—	—	—	—	BC_MODE				
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 25	—	All 0	R	Reserved
24	PTPWER_CTL	1	R/W	Set value of PortPowerControl (PPC) at HCCPARAMS in xHCI register.  The bit is set to 1 when there is an external Power Switch for control VBUS.
23 to 18	—	All 0	R	Reserved
17, 16	Renesas Private field	00	R/W	Renesas Private bit.  This bit can be written only "0". Don't write "1".
15 to 11	—	All 0	R	Reserved
10 to 8	LCLK_NONSTOP_FREQ	000	R/W	Showing a frequency of NONSTOP_CLK entered in USB3.0 host controller core.  000: Default value. Following users shall set this value to 000. <ul style="list-style-type: none"> <li>User who can supply clock (12, 24, 30, 48-MHz) as NONSTOP_CLK to core but don't want to use low-power function.</li> <li>User who can't supply clock (12, 24, 30, 48-MHz) as NONSTOP_CLK to core.</li> </ul> 001: User can supply LCLK_NOSTOP:12 MHz (+/-10%), and uses the function. 010: User can supply LCLK_NOSTOP:24 MHz (+/-10%), and uses the function. 011: User can supply LCLK_NOSTOP:30 MHz (+/-10%), and uses the function. 100: User can supply LCLK_NOSTOP:48 MHz (+/-10%), and uses the function.
7 to 4	—	All 0	R	Reserved
3 to 0	BC_MODE	0000	R/W	Set mode of Battery Charge function.



**54.3.1.11 FW Version**

Register displaying FW Version.



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	FW Version	H'0000_0000	R	FW Version is showed here. After FW downloading, FW Version can be read. Before FW download: H'0020 0000 After FW download: H'0020 XX00

### 54.3.1.12 FW Download Control & Status

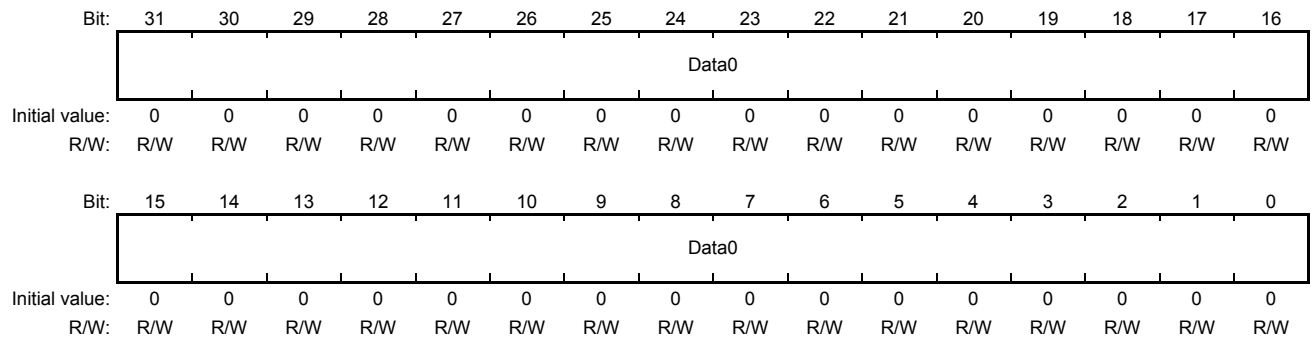
Register displaying Status and Control for writing FW via AXI Bus.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	Set_Data1	Set_Data0	—	Result_Code			—	—	BIOS Download Lock	BIOS Download Enable
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	RW1S	RW1S	R	R	R	R	R	R	RW1S	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 10	—	All 0	R	Reserved
9	Set_Data1	0	RW1S	When this bit is 1, the value of AXICNF05C register is set by the system.
8	Set_Data0	0	RW1S	When this bit is 1, the value of AXICNF058 register is set by the system.
7	—	0	R	Reserved
6 to 4	Result_Code	000	R	This field presents the results of BIOS Download. 000: Invalid 001: Success 010: Error Others: Reserved
3, 2	—	All 0	R	Reserved
1	BIOS Download Lock	0	RW1S	When this bit is 1, the BIOS download function is locked.
0	BIOS Download Enable	0	R/W	When this bit is 1, the BIOS download function is enabled.

**54.3.1.13 FW Data0**

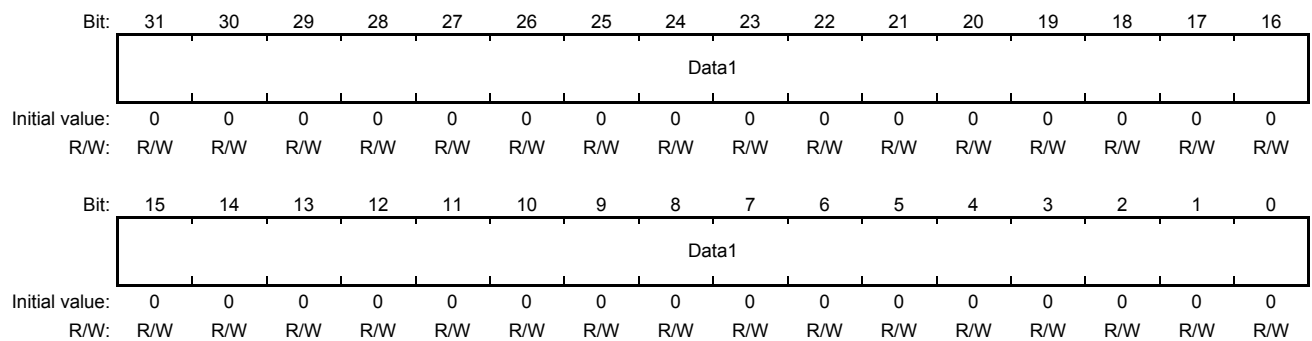
Data Register for writing FW via AXI Bus.



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	Data0	H'0000_0000	R/W	Data register 0 for writing FW

**54.3.1.14 FW Data1**

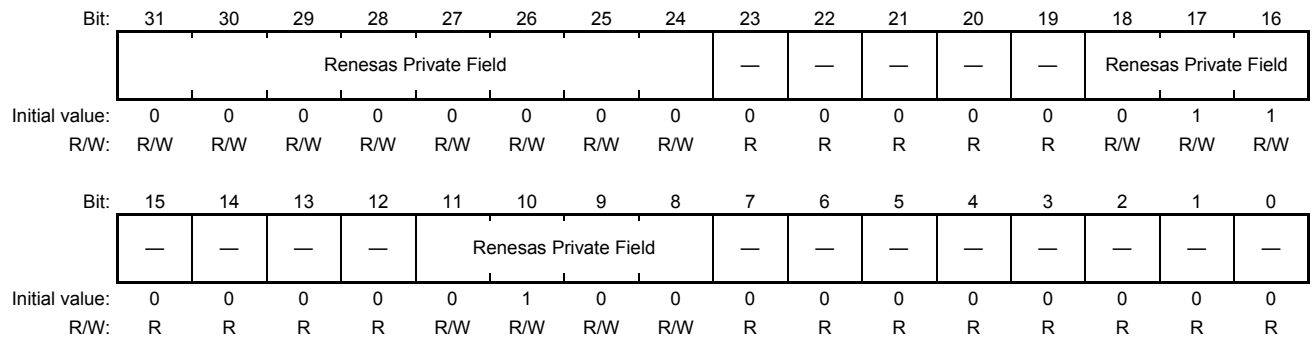
Data Register for writing FW via AXI Bus.



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	Data1	H'0000_0000	R/W	Data register 1 for writing FW

### 54.3.1.15 Renesas Private Register

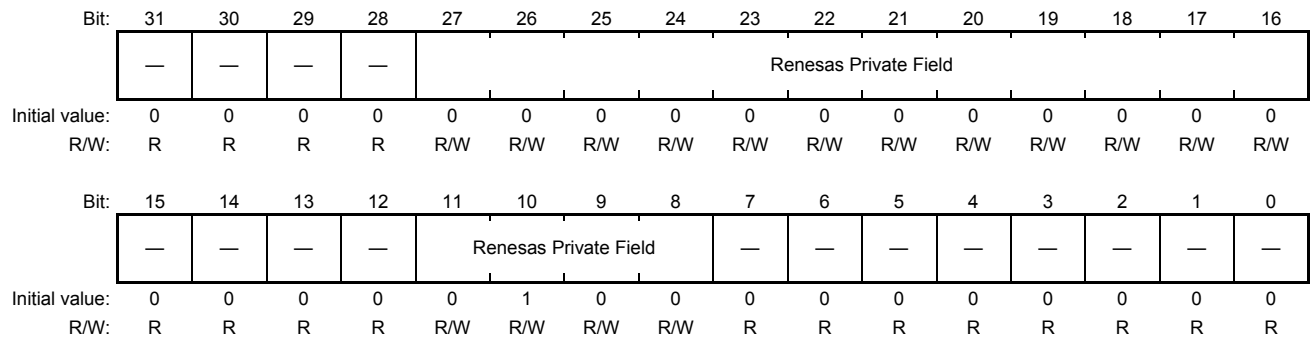
This register is Write inhibit.



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	Renesas Private field	H'00	R/W	Renesas Private field. This is write inhibit field.
23 to 19	—	All 0	R	Reserved
18 to 16	Renesas Private field	011	R/W	Renesas Private field. This is write inhibit field.
15 to 12	—	All 0	R	Reserved
11 to 8	Renesas Private field	H'4	R/W	Renesas Private field. This is write inhibit field.
7 to 0	—	All 0	R	Reserved

### 54.3.1.16 Renesas Private Register

This register is Write inhibit.



Bit	Bit Name	Initial Value	R/W	Description
31 to 28	—	All 0	R	Reserved
27 to 16	Renesas Private Field	H'000	R/W	Renesas Private field. This is write inhibit field.
15 to 12	—	All 0	R	Reserved
11 to 8	Renesas Private field	H'4	R/W	Renesas Private field. This is write inhibit field.
7 to 0	—	All 0	R	Reserved

## 54.3.1.17 Core Control 3

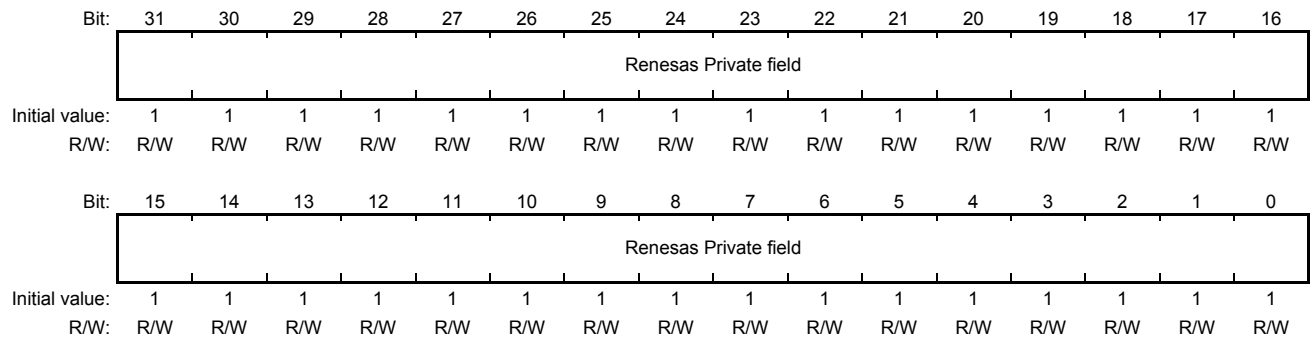
Register for other setting.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	Renesas Private bit	—	—	—	—	—	—	—	Renesas Private bit
Initial value:	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1
R/W:	R	R	R	R	R	R	R	R/W	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PMC_MODE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 25	—	All 0	R	Reserved
24	Renesas Private bit	1	R/W	Renesas Private bit. Do not write 0 to this bit.
23 to 17	—	All 0	R	Reserved
16	Renesas Private bit	1	R	Renesas Private bit This is write inhibit bit.
15 to 2	—	All 0	R	Reserved
1, 0	PMC_MODE	00	R/W	Sets control of HO_CACTIVE at Low Power Interface. When Bit[0] is 0, it is kept HO_CACTIVE at 1 even if system requests to stop ACLK_H. When Bit[1] is 0, it is kept HO_CACTIVE at 1 and is not to be 0 voluntarily. Bit[0] 1: 0 Control of HO_CACTIVE is valid when HI_CSYSREQ/HI_CSYSACK handshake 0: 0 Control of HO_CACTIVE is invalid when HI_CSYSREQ/HI_CSYSACK handshake Bit[1] 1: 0 Control of HO_CACTIVE is valid when not HI_CSYSREQ/HI_CSYSACK handshake 0: 0 Control of HO_CACTIVE is invalid when not HI_CSYSREQ/HI_CSYSACK handshake

### 54.3.1.18 Renesas Private Register

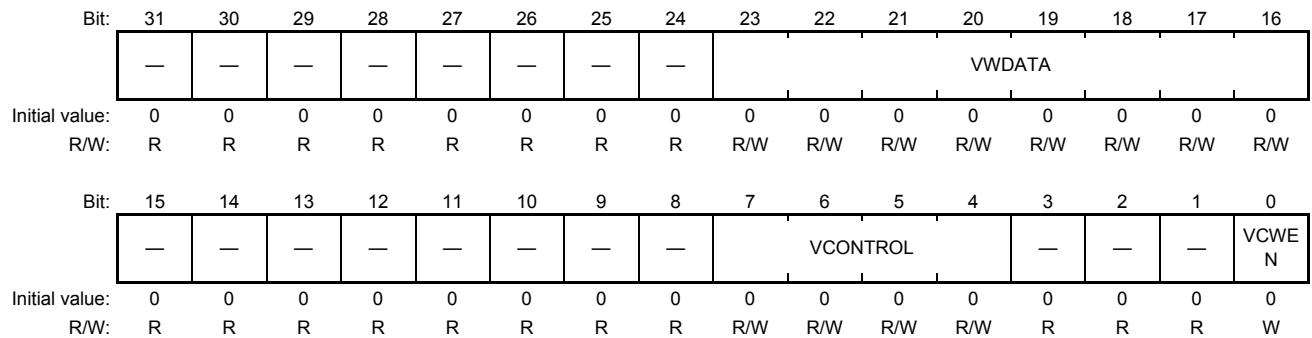
This is write inhibit register.



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	Renesas Private field	H'FFFF FFFF	R/W	Renesas Private field. This is write inhibit field.

### 54.3.1.19 UTMI Plus Vendor Control Interface Set Register (VENDOR\_CON\_SET)

The register for Vendor Control Interface signal setting.



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved
23 to 16	VWDATA	H'00	R/W	Signal for Vendor Write Data. It is write data signal to vendor control register write field.
15 to 8	—	All 0	R	Reserved
7 to 4	VCONTROL	H'0	R/W	Signal for Vendor Control. It is able to select vendor control register that user wants to use.
3 to 1	—	All 0	R	Reserved
0	VCWEN	0	W	Signal for enabling write VWDATA for Vendor Control Address. If this bit is set to 1, it is enabled to write the value of VWDATA for vendor control address.

### 54.3.1.20 UTMI Plus Vendor Control Interface Status Register (VENDOR\_CON\_STA)

The register for status of Vendor Control Interface signal.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R		
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
	—	—	—	—	—	—	—	—	VSTATUS								—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R		

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved
7 to 0	VSTATUS	H'00	R	Signal for Vendor Status. It is read data signal from vendor control register read field.

### 54.3.1.21 LCLK Select Register (LCLKSEL)

The register configure LCLK. Write H'0103\_0001 to enable LCLK operation.

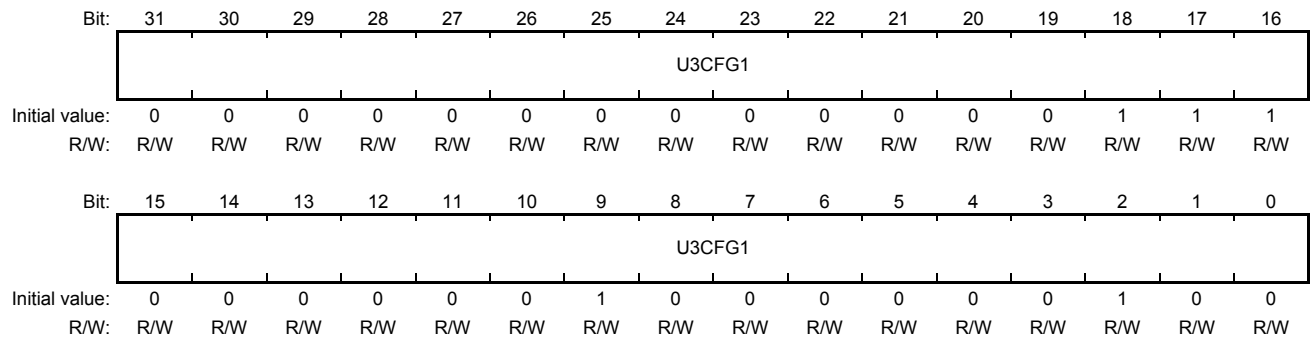
Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	LSEL	—	—
Initial value:	0	0	0	0	0	0	0	1	0	0	0	0	0	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 19	—	H'0020	R/W	Reserved This field should be set to H'0020.
18	LSEL	1	R/W	LCLK selection This bit control LCLK selection. This bit should be set to 0 when this IP operating. 0: LCLK enabled 1: LCLK disabled
17 to 0	—	H'3 0001	R/W	Reserved This field should be set to H'3 0001.



### 54.3.1.22 USB3.0 Configuration1

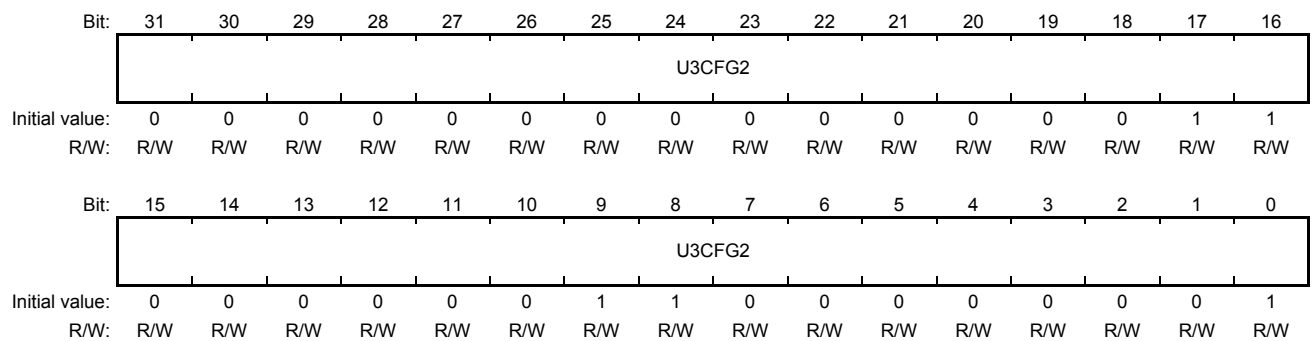
The register controls initial configuration of USB3.0.



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	U3CFG1	H'0007 0204	R/W	Must be set to H'0003 0204.

### 54.3.1.23 USB3.0 Configuration2

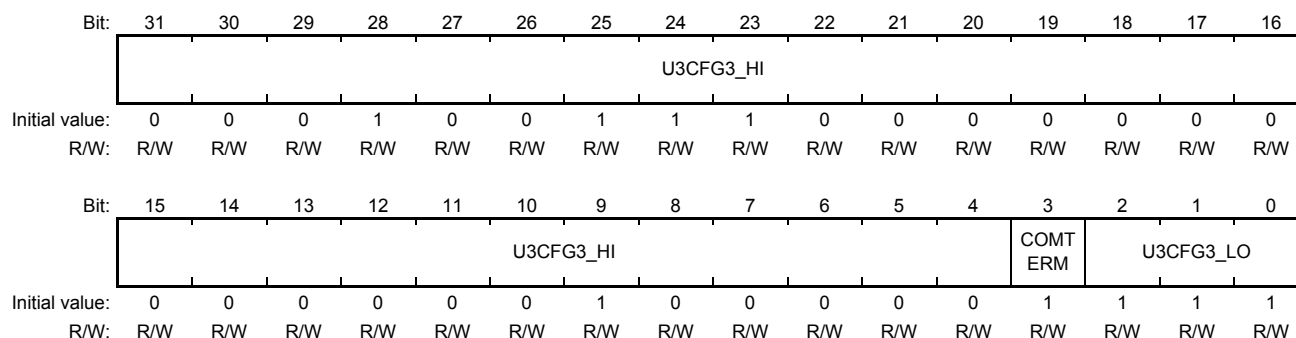
The register controls initial configuration of USB3.0.



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	U3CFG2	H'0003 0301	R/W	Must be set to H'0003 0300.

### 54.3.1.24 USB3.0 Configuration3

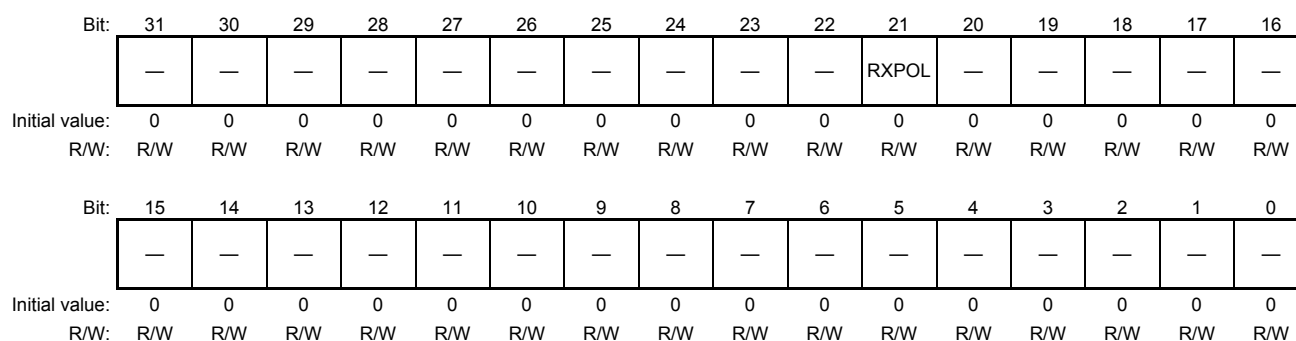
The register controls initial configuration of USB3.0.



Bit	Bit Name	Initial Value	R/W	Description
31 to 4	U3CFG3_HI	H'1380 200	R/W	Must be set to H'1380 200.
3	COMTERM	1	R/W	Internal reference clock terminator control. 0: OFF 1: ON
2 to 0	U3CFG3_LO	111	R/W	Must be set to 111

### 54.3.1.25 USB3.0 RX Polarity

The register controls polarity inversion of SS USB3.0 RX.



Bit	Bit Name	Initial Value	R/W	Description
31 to 22	—	All 0	R/W	Reserved The write value should be 0.
21	RXPOL	0	R/W	Polarity inversion setting of RX. 0: Normal operation 1: Polarity Inversion enable
20 to 0	—	All 0	R/W	Reserved The write value should be 0.

### 54.3.1.26 USB3.0 TX Polarity

The register controls polarity inversion of SS USB3.0 TX.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	TXPOL	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 5	—	All 0	R/W	Reserved The write value should be 0.
4	TXPOL	0	R/W	Polarity inversion setting of TX. 0: Normal operation 1: Polarity Inversion enable
3 to 0	—	All 0	R/W	Reserved The write value should be 0.

### 54.3.2 xHCI Register

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

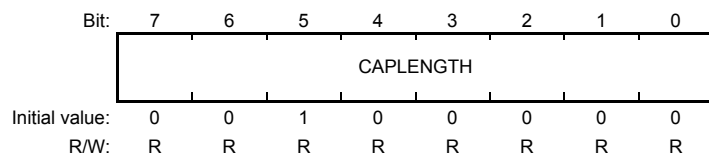
#### 54.3.2.1 Host Controller Capability Registers

Host controller capability registers constitute a register group indicating capability information that shows the host controller interface component.

No.	Offset	Base Offset	Register	Default Value (H)	Function
1	H'00	H'000	CAPLENGTH	H'20	Capability register length
2	H'01	H'001	—	H'00	Reserved
3	H'02	H'002	HCIVERSION	H'0100	Host controller interface version number
4	H'04	H'004	HCSPARAMS1	H'0200 0120	Structural parameters 1
5	H'08	H'008	HCSPARAMS2	H'2400 0011	Structural parameters 2
6	H'0C	H'00C	HCSPARAMS3	H'0000 0000	Structural parameters 3
7	H'10	H'010	HCCPARAMS	H'0140 51CF	Capability parameters
8	H'14	H'014	DBOFF	H'0000 0800	Doorbell offset
9	H'18	H'018	RTSOFF	H'0000 0600	Runtime register space offset
CAPLENGTH-H'01C					Reserved

#### (1) CAPLENGTH

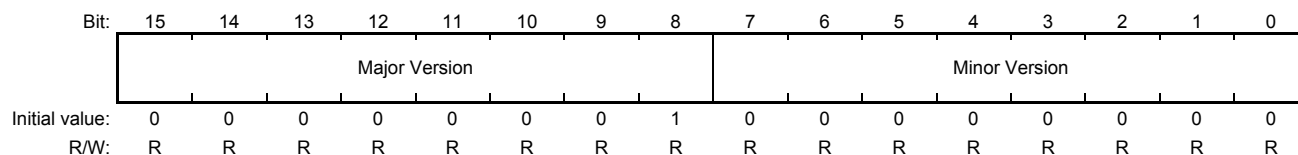
Register specifying capability register size



Bit	Bit Name	Initial Value	R/W	Description
7 to 0	CAPLENGTH	H'20	R	Displays Capability Register Size

#### (2) HCIVERSION

Register storing revision of xHCI Specification supported by the host controller.

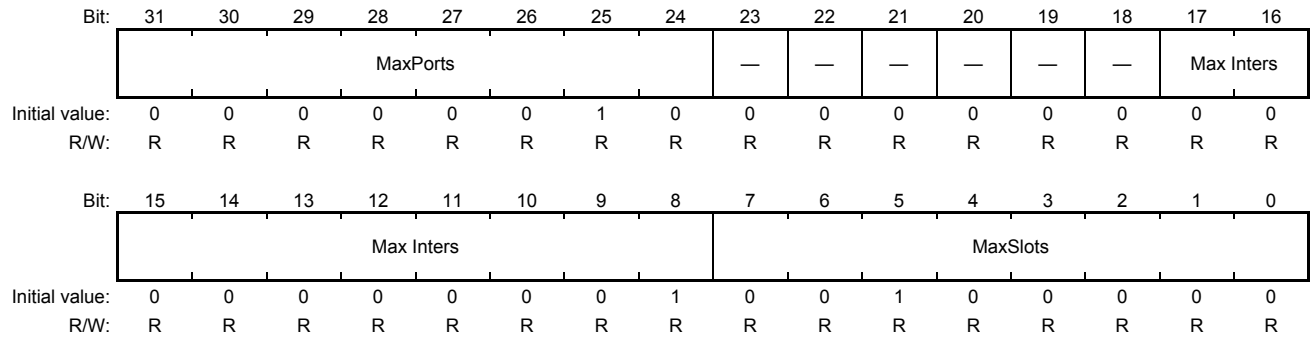


Bit	Bit Name	Initial Value	R/W	Description
15 to 8	Major Version	H'01	R	Displays Major version of xHCI Specification
7 to 0	Minor Version	H'00	R	Displays Minor version of xHCI Specification

**(3) HCSPARAMS1**

Register storing basic architectural parameters supported by the host controller core.

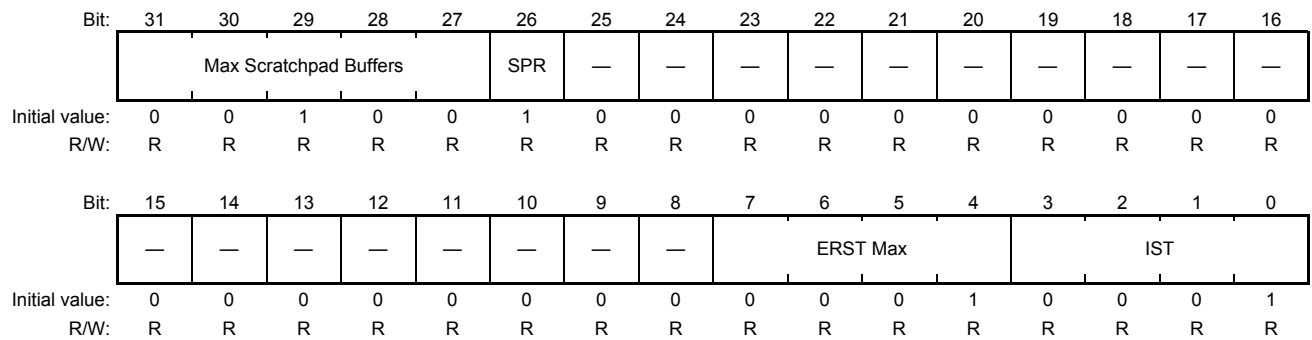
For MaxPorts, the total number of ports for USB3 port and USB2 port is set. The host core has 1 port for each of USB3 and USB2, so the maxports value is 2. For MaxInters, the total number of Interrupters supported by the host controller is set. The host core has 1 interrupter, so bit is set to 1.



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	MaxPorts	H'02	R	Number of Ports Total number of downstream ports implemented by host controller
23 to 18	—	All 0	R	Reserved
17 to 8	Max Inters	H'001	R	Number of Interrupters Total number of Interrupters implemented by host controller
7 to 0	MaxSlots	H'20	R	Number of Device Slots Maximum number of device context structures and doorbell array entries that can be supported

**(4) HCSPARAMS2**

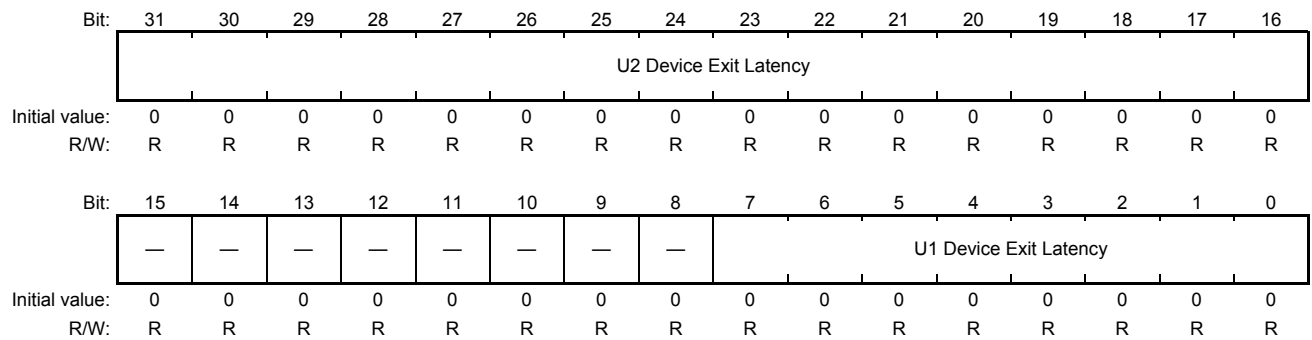
Register storing basic architectural parameters supported by the host controller core.



Bit	Bit Name	Initial Value	R/W	Description
31 to 27	Max Scratchpad Buffers	H'04	R	Displays the number of scratchpad buffers that the system software reserves for xHC. Valid: 0 to 31
26	SPR	1	R	Scratchpad Restore Indicates whether xHC uses a scratchpad buffer or not to save the state when max scratchpad buffers > 0 and save and restore operations are performed. If Max Scratchpad Buffer = 0, this bit is set to 0.
25 to 8	—	All 0	R	Reserved
7 to 4	ERST Max	H'1	R	Event Ring Segment Table Max Determines the maximum supported value for the event ring segment table base size register. The maximum number of event ring segment table entries = $2^{ERST\ Max}$
3 to 0	IST	H'1	R	Isochronous Scheduling Threshold Specifies the number of frames/microframes. Until bit[3] 0: IST[2:0] microframes, TRB can be added. Until bit[3] 1: IST[2:0] frames, TRB can be added.

**(5) HCSPARAMS3**

Register specifying link exit latency.



Bit	Bit Name	Initial Value	R/W	Description
31 to 16	U2 Device Exit Latency	H'0000	R	Worst case latency during transition from U2 to U0. H'0000: zero H'0001: less than 1 $\mu$ s. H'0002: less than 2 $\mu$ s ... H'07FF: less than 2,047 $\mu$ s. H'0800 to H'FFFF: reserved
15 to 8	—	All 0	R	Reserved
7 to 0	U1 Device Exit Latency	H'00	R	Worst case latency during transition from U1 to U0. H'00: zero H'01: less than 1 $\mu$ s. H'02: less than 2 $\mu$ s ... H'0A: less than 10 $\mu$ s. H'0B to H'FF: reserved

**(6) HCCPARAMS**

Register specifying optional capability supported by xHCI.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	xECP															
Initial value:	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MaxPSASize				—	—	—	PAE	NSS	LTC	LHRC	PIND	PPC	CSZ	BNC	AC64
Initial value:	0	1	0	1	0	0	0	1	1	1	0	0	1	1	1	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

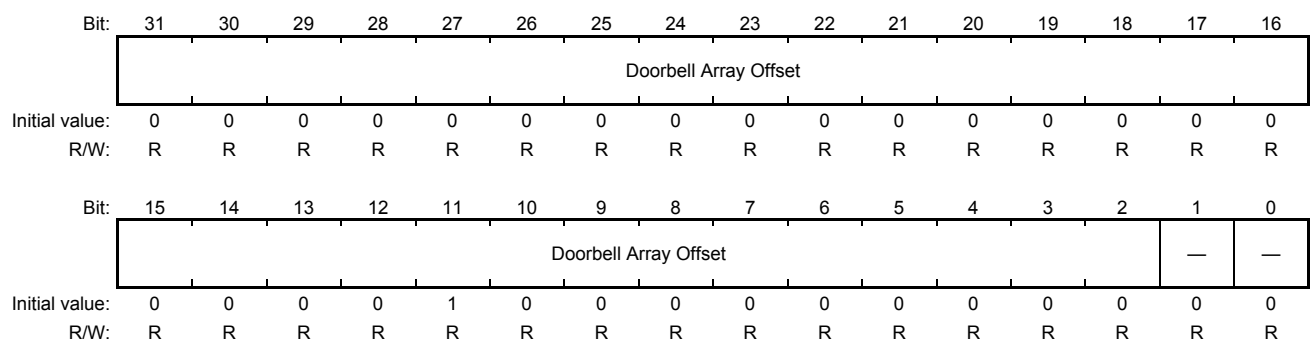
Bit	Bit Name	Initial Value	R/W	Description
31 to 16	xECP	H'0140	R	xHCI Extended Capabilities Pointer Presence or absence of capabilities list H'0000: No extended capabilities Other: Indicates offset from BASE to extended capability. USB Legacy Supported Protocol Capability is at offset H'500.
15 to 12	MaxPSASize	H'5	R	Maximum Primary Stream Array Size Maximum size of primary stream array supported by host. Primary Stream Array size = $2^{\text{MaxPSASize}+1}$ Valid: 1 to 15 Default value is 5 as stream number HSP supports 63.
11 to 9	—	All 0	R	Reserved
8	PAE	1	R	Parse All Event Data Indicates whether host controller parses event data TRB that is found while skipping next TD after receiving short packet in aTD. 0: Just parse first 1: Parse all
7	NSS	1	R	No Secondary SID Support Indicates whether host controller supports secondary stream IDs. 0: Supported 1: Not supported
6	LTC	1	R	Latency Tolerance Messaging Capability Indicates whether host controller supports latency tolerance messaging. 0: Not supported 1: Supported
5	LHRC	0	R	Light HC Reset Capability Indicates whether host controller supports light host controller reset. 0: Not supported 1: Supported



Bit	Bit Name	Initial Value	R/W	Description
4	PIND	0	R	Port Indicators Indicates whether xHCI root hub port supports port indicator control. 0: Not contained 1: Port status/control register contains a field that can be read and written to control port indicator condition.
3	PPC	1	R	Port Power Control Indicates whether host controller contains port power control. 0: Port doesn't contain port power switch. 1: Port contains port power switch
2	CSZ	1	R	Context Size 0: xHC uses 32-byte Context data structure 1: xHC uses 64-byte Context data structure
1	BNC	1	R	BW Negotiation Capability Indicates whether xHC supports bandwidth negotiation 0: Does not support BW negotiation 1: Supports BW negotiation
0	AC64	1	R	64-bit Addressing Capability Addressing range 0: 32-bit address memory pointers 1: 64-bit address memory pointers

**(7) DBOFF**

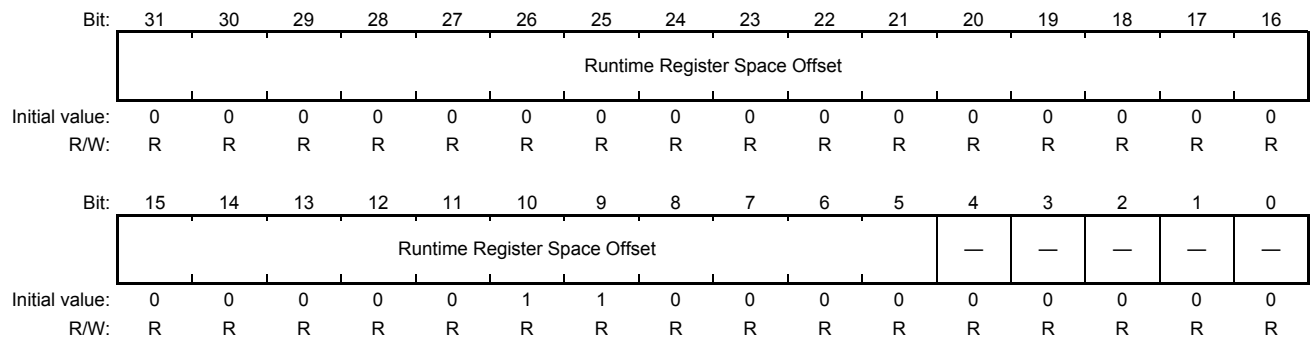
Register specifying Offset from Base Address of Doorbell Array.



Bit	Bit Name	Initial Value	R/W	Description
31 to 2	Doorbell Array Offset	H'0000 0200	R	Dword Offset from Base of Doorbell Array base address. Doorbell array's offset is H'800
1, 0	—	All 0	R	Reserved

**(8) RSTOFF**

Register specifying Offset from Base Address of Runtime Register Space.



Bit	Bit Name	Initial Value	R/W	Description
31 to 5	Runtime Register Space Offset	H'000 0030	R	64-byte offset from Base, for xHCI Runtime Register. Address = Base + runtime register set offset runtime register's offset is H'600
4 to 0	—	All 0	R	Reserved

### 54.3.2.2 Host Controller Operational Registers

Host controller operational registers constitute a register group for monitoring and controlling the operational state of the host controller. The beginning address (Operational BASE) of the host controller operational registers is specified as follows;

Base address = Capability base address + CAPLENTH

No.	Offset	Base Offset	Register	Default Value (H)	Function
1	H'00	H'020	USBCMD	H'0000_0000	USB command
2	H'04	H'024	USBSTS	H'0000_0801	USB status
3	H'08	H'028	PAGESIZE	H'0000_0001	Page size
4	H'10 to H'0C	H'030 to H'02C	—		Reserved
5	H'14	H'034	DNCTRL	H'0000_0000	Device notification control
6	H'18	H'038	CRCRL	H'0000_0000	Command ring control lo
7	H'1C	H'03C	CRCRH	H'0000_0000	Command ring control hi
8	H'2C to H'20	H'04C to H'040	—		Reserved
9	H'30	H'050	DCBAAPL	H'0000_0000	Device context bass address array pointer lo
10	H'34	H'054	DCBAAPH	H'0000_0000	Device context bass address array pointer hi
11	H'38	H'058	CONFIG	H'0000_0000	Configure

Host Controller Port Register Set

Beginning Address is Operational Base + CAPLENTH + (H'400 + H'10 × (n - 1))

“n” indicates Port Number of Host Controller and the maximum value is the value of MaxPorts.

This Host Control Core's MaxPorts is 2. The Register group is as follows.

No.	Offset	Base Offset	Register	Default Value (H)	Function
1	H'00	H'420	PORTSC1	H'0000 02A0	Port Status and Control 1 (USB3)
2	H'04	H'424	PORTPMSC1	H'0000 0000	Port PM Status and Control 1 (USB3)
3	H'08	H'428	PORTLI1	H'0000 0000	Port Link Info 1 (USB3)
—	H'0C	H'40C	—		Reserved
4	H'10	H'430	PORTSC2	H'0000 02A0	Port Status and Control 2 (USB2)
5	H'14	H'434	PORTPMSC2	H'0000 0000	Port PM Status and Control 2 (USB2)
—	H'18	H'438	—		Reserved
—	H'1C	H'43C	—		Reserved

**(1) USBCMD**

Register indicating command to be executed by host controller. The host controller writes the register after which the Command is executed.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	EU3S	EWE	CRS	CSS	LHCRST	—	—	—	HSEE	INTE	HCRST	R/S
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 12	—	All 0	R	Reserved
11	EU3S	0	R/W	Enable U3 MFINDEX stop 0: If all root hub ports are in the disconnected, disabled, or powered-off state, xHC can stop count of MFINDEX. 1: If all root hub ports are in the U3, disconnected, disabled, or powered-off state, xHC can stop count of MFINDEX.
10	EWE	0	R/W	Enable Wrap Event 0: Do not generate MFINDEX wrap event 1: Every time MFINDEX register changes from H'03FFF to H'0, xHC generates MFINDEX wrap event.
9	CRS	0	R/W	Controller Restore State <ul style="list-style-type: none"> <li>CRS bit = 1, Run/Stop bit = 0 and Save State bit = 1: xHC executes restore state operation to restore the internal state.</li> <li>CRS bit = 0: Restore state operation not executed</li> <li>CRS bit = 1, Run/Stop bit = 1 or Save State bit = 0: Restore state operation not executed read value from AXI is 0. If this bit is set to 1 by AXI, H/W sets USBSTS bit 9 to 1, bit 10 to 0 clear.</li> </ul>
8	CSS	0	R/W	Controller Save State <ul style="list-style-type: none"> <li>CSS bit = 1, Run/Stop bit = 0: xHC saves internal state that is restored at next restore state operation</li> <li>CSS bit = 1, Run/Stop bit = 1: Save state operation is not executed. read value from AXI is 0. If this bit is set to 1 by AXI, H/W sets USBSTS bit 8 to 1, bit 10 to 0 clear.</li> </ul>
7	LHCRST	0	R	Light Host Controller Reset If Light HC Reset Capability bit of HCCPARAMS register is 1, this bit is enabled. Read 0: Reset completed Read 1: Reset not completed
6 to 4	—	All 0	R	Reserved

Bit	Bit Name	Initial Value	R/W	Description
3	HSEE	0	R/W	Host System Error Enable HSEE bit = 1, HSE bit = 1: xHC asserts out-of-band error signal to host. Software clears HSE bit, after which its notice signal is received.
2	INTE	0	R/W	Interrupt Enable If this bit is 1, host system interrupt is enabled.
1	HCRST	0	R/W	Host Controller Reset Used to reset host controller. Write 1: Reset Does not influence AXI register. Host controller sets 0, then resetting process completes. Software continues resetting process until this bit changes to 0. Software shall not set 1 when HCHalted bit = 0.
0	R/S	0	R/W	Run/Stop 0: Stop 1: Run During 1, scheduling is being continued. During 0, completes USB transaction and transits to halted state. xHC shall goes to halted state during the 16 microframes after bit clearing. Software shall not set 1 except when xHC is in halted state.

**(2) USBSTS**

Register displaying condition of host controller. If a bit is set to 1, the bit is cleared to 0. If a bit is set 0, the set value is ignored.

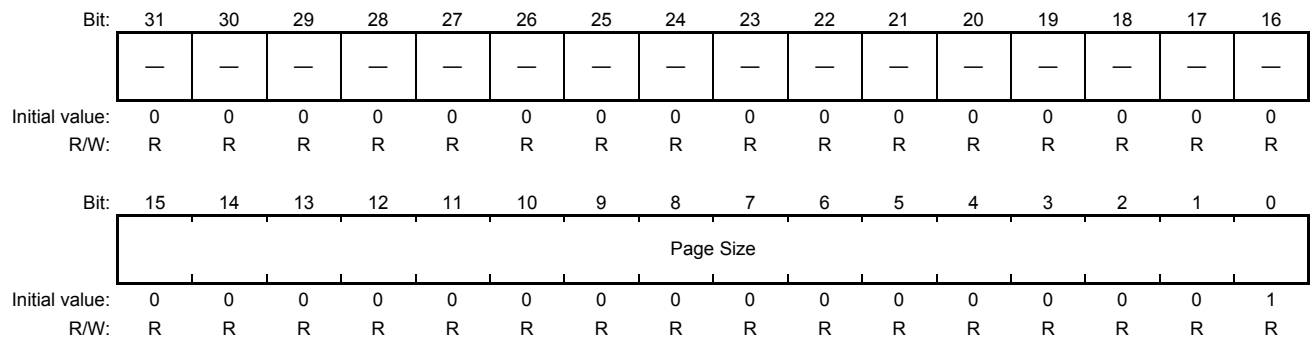
Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	HCE	CNR	SRE	RSS	SSS	—	—	—	PCD	EINT	HSE	—	HCH
Initial value:	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1
R/W:	R	R	R	R	R	RW1C	R	R	R	R	R	RW1C	RW1C	RW1C	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 13	—	All 0	R	Reserved
12	HCE	0	R	Host Controller Error 0: No internal xHC error condition exists 1: Internal xHC error condition
11	CNR	1	R	Controller Not Ready 0: Ready 1: Not ready Software shall not set any doorbell and xHC operational registers except USBSTS until CNR = 0. This flag is set by Chip HW reset and cleared when writing is enabled. This flag remains set to 0 until next HW reset.
10	SRE	0	RW1C	Save/Restore Error When error occurs in save or restore operation, this bit is set to 1. This bit is cleared when save or restore operation starts or when the bit is written with 1.
9	RSS	0	R	Restore State Status When controller restore state flag in USBCMD is set to 1, this bit is set to 1. During restoring, this bit remains set to 1. When restore state operation finishes, this bit is set to 0.
8	SSS	0	R	Save State Status This bit is set to 1 when controller save state flag bit in USBCMD is set to 1. Maintains a value of 1 during saving. This bit is set to 0 when save state operation finishes.
7 to 5	—	All 0	R	Reserved
4	PCD	0	RW1C	Port Change Detect This bit is set to 1 when port change bit changes from 0 to 1 and Force Port Resume bit changes from 0 to 1. 1: Detects resuming of suspended port
3	EINT	0	RW1C	Event interrupt xHC sets 1 when interrupt pending bit is set. 1 write clear

Bit	Bit Name	Initial Value	R/W	Description
2	HSE	0	RW1C	Host System Error 1: Fatal error occurs when xHC accesses host system. And also DMA transfer error. When these errors occur xHC sets Run/Stop bit to 0 and stops command and event after errors.
1	—	0	R	Reserved
0	HCH	1	R	HCHalted If Run/Stop bit is 1, this bit is set to 0. If Run/Stop bit is set to 0 to stop operation, Software or xHC hardware sets this bit to 1.

**(3) PAGESIZE**

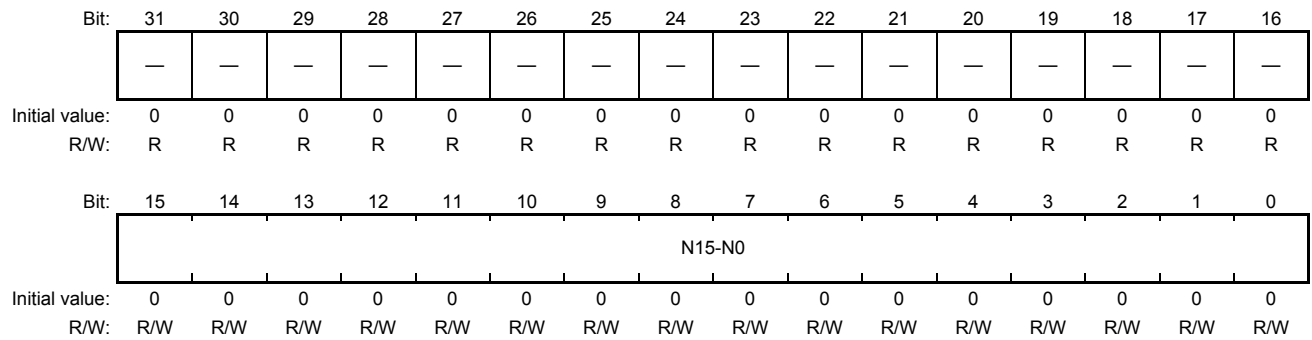
Page size that is supported by xHC implementation is defined.



Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved
15 to 0	Page Size	H'0001	R	xHC's system page size. 4 KB page size

**(4) DNCTRL**

This register is used by host controller to set notification of whether USB device notification Transaction Packet in DNCTRL register is enabled or disabled. Device notification event is permitted by bit setting. It is presupposed that bits are written in units of one word (4 bytes).

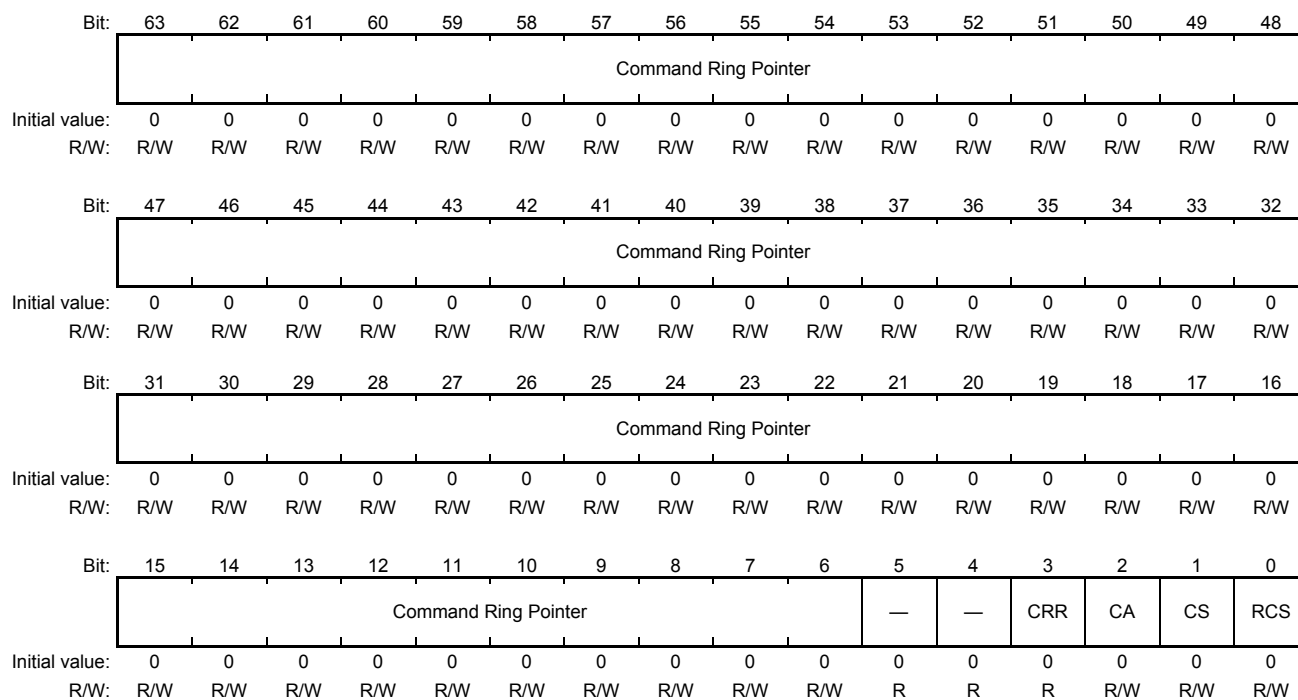


Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved
15 to 0	N15-N0	H'0000	R/W	<p>Notification Enable</p> <p>When the Notification Enable bit is set, and the device notification transaction packet has the same value in the notification type field, a device notification event occurs.</p> <p>EX) When N3 is set, and the device notification TP with its notification type field set to 3 (FUNCTION_WAKE) is received, a device notification event occurs.</p>



**(5) CRCR**

Register indicating base address of first segment of command ring.

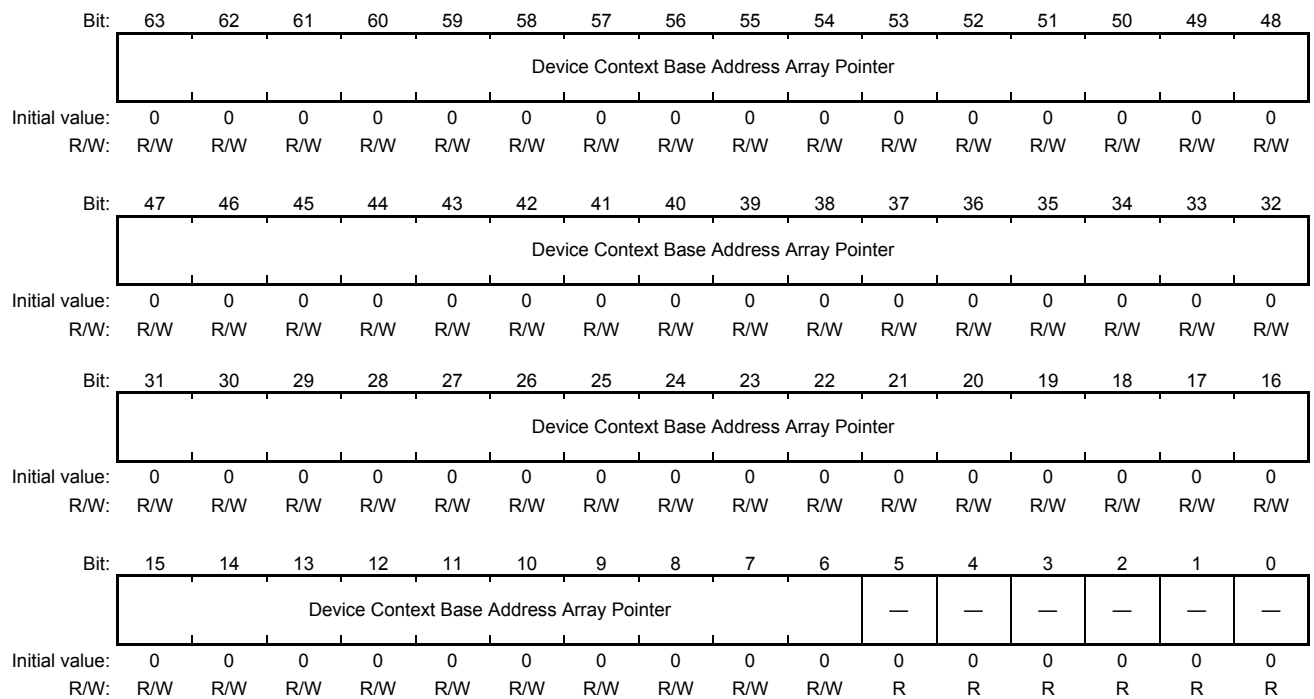


Bit	Bit Name	Initial Value	R/W	Description
63 to 6	Command Ring Pointer	H'0000 0000 0000 000	R/W	Defines a 64-bit Command Ring Dequeue Pointer default value. When Command Ring Running (CRR) is 1, any writing to this bit is ignored. The read value from AXI is 0.
5, 4	—	All 0	R	Reserved
3	CRR	0	R	Command Ring Running This bit is set when the Run/Stop bit is 1 and the DB reason field in the host controller doorbell register is set to 1 by the host controller command. This bit is cleared to 0 when the command ring stops after command stop or command abort is set to 1, or when Run/Stop bit is cleared to 0.
2	CA	0	R/W	Command Abort When this bit is set to 1, stops all commands and stops command ring, changes completion code to “Command Ring Stop”, and sends command completion with the completion code set to current command ring dequeue pointer value. When Command Ring Running (CRR) is 0, xHC ignores any writing to this field. The read value is 0.
1	CS	0	R/W	Command Stop Writing 1 causes command ring operation to be stopped after the command’s completion, then the completion code is changed to command ring stop. Command completion with the command TRB pointer set to the current command ring dequeue pointer value is sent. When Command Ring Running (CRR) is 0, xHC ignores any writing to this field. The read value is 0.

Bit	Bit Name	Initial Value	R/W	Description
0	RCS	0	R/W	Ring Cycle State Defines the xHC Consumer Cycle State (CCS) referred to by the command ring pointer. When Command Ring Running (CRR) is 1, any writing to this field is ignored. The read value is 0.

**(6) DCBAPP**

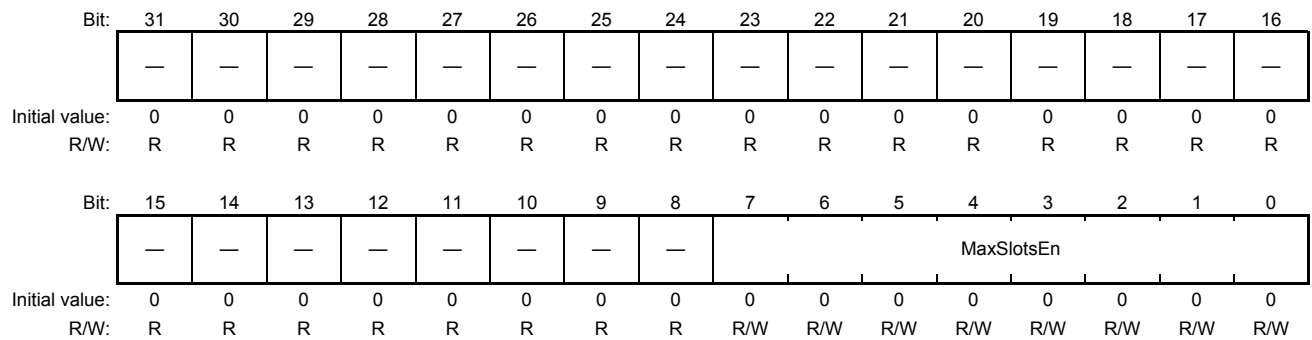
Registers indicating base address of device context bass address array.



Bit	Bit Name	Initial Value	R/W	Description
63 to 6	Device Context Base Address Array Pointer	H'0000 0000 0000 000	R/W	Defines 64-bit base address of device context pointer array table.
5 to 0	—	All 0	R	Reserved

**(7) CONFIG**

Register defining numeric xHC configuration parameters.



Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved
7 to 0	MaxSlotsEn	H'00	R/W	<p>Max Device Slots Enable</p> <p>Indicates maximum number of enabled device slots. The valid range is 0 to MaxSlots.</p> <p>Enabled device slots are allocated continuously.</p> <p>EX) When 16 is defined, Device Slots 1-16 constitute the active range.</p> <p>0: Disable Device slots</p> <p>While xHC is running, (Run/Stop bit = 1), it is not possible to write to this field.</p>

**(8) PORTSC1**

This register controls port status of USB3.0.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	WPR	DR	—	—	WOE	WDE	WCE	CAS	CEC	PLC	PRC	OCC	WRC	PEC	CSC	LWS
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	RW1S	R	R	R	R/W	R/W	R/W	R	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PIC	Port Speed				PP	PLS				PR	OCA	—	PED	CCS	
Initial value:	0	0	0	0	0	0	1	0	1	0	1	0	0	0	0	0
R/W:	R/W	R/W	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R	RW1C	R

Bit	Bit Name	Initial Value	R/W	Description
31	WPR	0	RW1S	Warm Port Reset Write 1: Starts warm reset sequence, and sets PR bit to 1. Conformity with the warm reset sequence, is reflected in the PR bit setting of PR, PRC, and WRC.
30	DR	0	R	Device Removable 0: Device connected to this Port is removable 1: Device connected to this Port is non-removable
29, 28	—	All 0	R	Reserved
27	WOE	0	R/W	Wake on Over-current Enable Write 1: Enables over-current condition as system wake-up event. If Port Power is 0, this bit is set to 0.
26	WDE	0	R/W	Wake on Disconnect Enable Write 1: Enables device disconnect as system wake-up event. If Port Power is 0, this bit is set to 0.
25	WCE	0	R/W	Wake on Connect Enable Write 1: Enables device connect as system wake-up event If Port Power is 0, this bit is set to 0.
24	CAS	0	R	Cold Attach Status 1: Far-end receiver Termination is detected but port status cannot transition to enabled state. If PP is 0 or at USB2.0 Port, this bit is set to 0.
23	CEC	0	RW1C	Port Config Error Change This bit is set when configuration with link partner fails.
22	PLC	0	RW1C	Port Link State Change This bit is set when link transitions from U3 to U0 state. 0: No Change 1: Link state Changed If a port status change event occurs, this bit is cleared to 0 automatically. Software writes 1 and then the bit is cleared.

Bit	Bit Name	Initial Value	R/W	Description
21	PRC	0	RW1C	<p>Port Reset Change</p> <p>This bit is set when port reset process completes. (Port Reset Change from 1 to 0 )</p> <p>0: No change 1: Reset complete</p> <p>If a port status change event occurs, this bit is cleared to 0 automatically. Software writes 1 and then the bit is cleared.</p>
20	OCC	0	RW1C	<p>Over-current Change</p> <p>When over-current active changes, this bit is set to 1. If a port status change event occurs, this bit is cleared to 0 automatically. Software writes 1 and then the bit is cleared.</p>
19	WRC	0	RW1C	<p>Warm Port Reset Change</p> <p>This bit is set to 1 when a warm reset is completed.</p>
18	PEC	0	RW1C	<p>Port Enable/Disable Change</p> <p>0: No change 1: Port enabled/disabled status has changed</p> <p>This bit is set when USB2 protocol port is disabled due to exiting from appropriate conditions at EO2 point. If a port status change event occurs, this bit is cleared to 0 automatically. Software writes 1 and then this bit is cleared. If Port Reset is 0, this bit is set to 0.</p>
17	CSC	0	RW1C	<p>Connect Status Change</p> <p>0: No change 1: Change in current connect status</p> <p>xHC sets this bit to 1 at change of port device connect status. If a port status change event occurs, this bit is cleared to 0 automatically. Software writes 1 and then this bit is cleared. If Port Reset is 0, this bit is set to 0.</p>
16	LWS	0	R/W	<p>Port Link State Write Strobe</p> <p>Write 0: Writing to PLS field is ignored. 1: Writing to PLS field is enabled.</p> <p>The read value is 0</p>
15, 14	PIC	00	R/W	<p>Port Indicator Control</p> <p>If Port Indicator (PIND) bit in HCCPRAMS register is 0, writing to this field has no effect. If Port Indicator (PIND) bit is 1;</p> <p>00: Port indicators are off 01: Amber 10: Green 11: Undefined</p> <p>If Port Reset is 0, this field is set to 0.</p>

Bit	Bit Name	Initial Value	R/W	Description
13 to 10	Port Speed	H'0	R	<p>Speed type of USB device connected to the port.</p> <p>This is enabled only when a device is connected to the port. (Current Connect Status is 1)</p> <p>After a port reset, this field indicates the speed of the device connected to the port. If the reset or speed detection fails, this field indicates Unknown Speed. When the Current Connect Status changes from 0 to 1, this field indicates Undefined Speed.</p> <p>H'0: Undefined Speed (Before Speed detection)</p> <p>H'1: Full-speed device attached</p> <p>H'2: Low-speed device attached</p> <p>H'3: High-speed device attached</p> <p>H'4: SuperSpeed device attached</p> <p>H'5 to H'E: Reserved</p> <p>H'F: Unknown Speed</p> <p>(Error detected during speed detection or Port Reset.)</p>
9	PP	1	R/W	<p>Port Power</p> <p>This field reflects a port's logical power state.</p> <p>0: This port is in the Powered-off state.</p> <p>1: This port is not in the Powered-off state.</p> <p>When the Port Power Control (PPC) bit in the HCSPATAMS1 register is 1, xHC has a port power control switch and this bit shows the current state of the switch. (0:off, 1:on)</p> <p>When the Port Power Control (PPC) bit in the HCSPATAMS1 register is 0, xHC has no port power control switch and each port is hard wired to power and not affected by this bit.</p> <p>If an over-current condition is detected at a powered port, the PP bit of each port is changed from 1 to 0.</p>

Bit	Bit Name	Initial Value	R/W	Description
8 to 5	PLS	H'5	R/W	<p>Port Link State</p> <p>This field is used for port power management and shows the Current Link state. When PED is 1, System software sets this bit then sets Link U state.</p> <p>Port Link State is not set to Disabled, RxDetect, or Inactive State.</p> <p>H'0: The link shall transition to the U0 state from any of the U states.</p> <p>H'1: The link should transition to the U1 State.</p> <p>H'2: The link should transition to the U2 State.</p> <p>H'3: The link shall transition to the U3 state from any of the U states.</p> <p>H'4 to H'F: Ignored.</p> <p>To write to this field, the Port Link State Write strobe should be 1.</p> <p>For USB2 Protocol port, writing 2 requests LPM.</p> <p>Software reads this field to determine success/failure of transition to U2 state.</p> <p>Write 0: Deasserts L1 signal</p> <p>Write 1: No influence</p> <p>Read Value Meaning</p> <p>H'0: Link is in the U0 State</p> <p>H'1: Link is in the U1 State</p> <p>H'2: Link is in the U2 State</p> <p>H'3: Link is in the U3 State (Device Suspended)</p> <p>H'4: Link is in the Disabled State</p> <p>H'5: Link is in the RxDetect State</p> <p>H'6: Link is in the Inactive State</p> <p>H'7: Link is in the Polling State</p> <p>H'8: Link is in the Recovery State</p> <p>H'9: Link is in the Hot Reset State</p> <p>H'A: Link is in the Compliance Mode State</p> <p>H'B: Link is in the Loopback State</p> <p>H'C to H'F: Reserved</p> <p>If Port Reset is 0, this field is ambiguous.</p>
4	PR	0	R/W	<p>Port Reset</p> <p>0: port is not in reset</p> <p>1: port reset assert</p> <p>When software sets this bit from 0 to 1, the bus reset sequence is started.</p> <p>Port Enable/Disable bit is 0.</p> <p>Port Enable bit is 0.</p> <p>This bit remains set to 1 until reset by root hub is completed.</p> <p>When error is detected during resetting, Port Speed bits indicate Unknown Speed.</p> <p>If Port Power is 0, this field is set to 0.</p>

Bit	Bit Name	Initial Value	R/W	Description
3	OCA	0	R	Over-current Active 0: Over-current condition 1: Not over-current condition When an over-current condition is removed, this bit changes from 1 to 0 automatically.
2	—	0	R	Reserved
1	PED	0	RW1C	Port Enable/Disable 0: Disable 1: Enable After detecting a connection at a port, if SS port initialization or reset by the system software is successful, this bit is automatically enabled by xHC. Port is disabled by fault condition (disconnect event or other fault condition), or USB System Software. Bit status doesn't change until port status changes. If Port Power is 0, this field is set to 0.
0	CCS	0	R	Current Connect Status 0: No device is present 1: Device is present on port Reflects current port status. If Port Power is 0, this field is set to 0.



**(9) PORTSC2**

Register controlling Port Status of USB2.0.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	DR	—	—	WOE	WDE	WCE	CAS	—	PLC	PRC	OCC	—	PEC	CSC	LWS
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R	R	RW1C	RW1C	RW1C	R	RW1C	RW1C	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PIC		Port Speed				PP	PLS				PR	OCA	—	PED	CCS
Initial value:	0	0	0	0	0	0	1	0	1	0	1	0	0	0	0	0
R/W:	R/W	R/W	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R	RW1C	R

Bit	Bit Name	Initial Value	R/W	Description
31	—	0	R	Reserved
30	DR	0	R	Device Removable 0: Device connected to this Port is removable 1: Device connected to this Port is non-removable
29 to 28	—	All 0	R	Reserved
27	WOE	0	R/W	Wake on Over-current Enable Write 1: Enables over-current condition as System Wake-up Event If Port Power is 0, this bit is set to 0.
26	WDE	0	R/W	Wake on Disconnect Enable Write 1: Enables device disconnect as System Wake-up Event If Port Power is 0, this bit is set to 0.
25	WCE	0	R/W	Wake on Connect Enable Write 1: Enables device connect as System Wake-up Event If Port Power is 0, this bit is set to 0.
24	CAS	0	R	Cold Attach Status 1: Far-end Receiver Termination is detected but Port Status cannot transition to Enabled State. If PP is 0 or at USB2.0 Port, this bit is set to 0.
23	—	0	R	Reserved
22	PLC	0	RW1C	Port Link State Change This bit is set when Link transitions from U3 to U0 state. 0: No change 1: Link state changed If a Port Status Change Event occurs, this bit is cleared to 0 automatically. Software writes 1 and then the bit is cleared.
21	PRC	0	RW1C	Port Reset Change This bit is set when Port reset process completes. (Port Reset changes from 1 to 0) 0: No change 1: Reset complete If a Port Status Change Event occurs, this bit is cleared to 0 automatically. Software writes 1 and then the bit is cleared.

Bit	Bit Name	Initial Value	R/W	Description
20	OCC	0	RW1C	<p>Over-current Change</p> <p>When Over-current Active changes, this bit is set to 1.</p> <p>If a Port Status Change Event occurs, this bit is cleared to 0 automatically.</p> <p>Software writes 1 and then the bit is cleared.</p>
19	—	0	R	Reserved
18	PEC	0	RW1C	<p>Port Enable/Disable Change</p> <p>0: No change</p> <p>1: Port enabled/disabled status has changed</p> <p>This bit is set when USB2 protocol port is disabled due to exiting from appropriate conditions at EO2 point.</p> <p>If a Port Status Change Event occurs, this bit is cleared to 0 automatically.</p> <p>Software writes 1 and then this bit is cleared.</p> <p>If Port Power is 0, this bit is set to 0.</p>
17	CSC	0	RW1C	<p>Connect Status Change</p> <p>0: No change</p> <p>1: Change in Current Connect Status</p> <p>xHC sets this bit to 1 at change of port device connect status.</p> <p>If a Port Status Change Event occurs, this bit is cleared to 0 automatically.</p> <p>Software writes 1 and then this bit is cleared.</p> <p>If Port Power is 0, this bit is set to 0.</p>
16	LWS	0	R/W	<p>Port Link State Write Strobe</p> <p>Write 0: Writing to PLS field is ignored.</p> <p>1: Writing to PLS field is enabled.</p> <p>The read value is 0</p>
15 to 14	PIC	00	R/W	<p>Port Indicator Control</p> <p>If Port Indicator (PIND) bit in HCCPRAMS Register is 0, writing to this field has no effect.</p> <p>If Port Indicator (PIND) bit is 1;</p> <p>00: Port indicators are off</p> <p>01: Amber</p> <p>10: Green</p> <p>11: Undefined</p> <p>If Port Power is 0, this field is set to 0.</p>

Bit	Bit Name	Initial Value	R/W	Description
13 to 10	Port Speed	H'0	R	<p>Speed type of USB device connected to the port.</p> <p>This is enabled only when a device is connected to the port. (Current Connect Status is 1)</p> <p>After a port reset, this field indicates the speed of the device connected to the port. If the reset or speed detection fails, this field indicates Unknown Speed. When the Current Connect Status changes from 0 to 1, this field indicates Undefined Speed.</p> <p>H'0: Undefined Speed (Before Speed detection)</p> <p>H'1: Full-speed device attached</p> <p>H'2: Low-speed device attached</p> <p>H'3: High-speed device attached</p> <p>H'4: SuperSpeed device attached</p> <p>H'5 to H'E: Reserved</p> <p>H'F: Unknown Speed (Error detected during speed detection or Port Reset.)</p>
9	PP	1	R/W	<p>Port Power</p> <p>This field reflects a port's logical power state.</p> <p>0: This port is in the Powered-off state.</p> <p>1: This port is not in the Powered-off state.</p> <p>When the Port Power Control (PPC) bit in the HCSPATAMS1 register is 1, xHC has a port power control switch and this bit shows the current state of the switch. (0: off, 1: on)</p> <p>When the Port Power Control (PPC) bit in the HCSPATAMS1 register is 0, xHC has no port power control switch and each port is hard wired to power and not affected by this bit.</p> <p>If an over-current condition is detected at a powered port, the PP bit of each port is changed from 1 to 0.</p>

Bit	Bit Name	Initial Value	R/W	Description
8 to 5	PLS	H'5	R/W	<p>Port Link State</p> <p>This field is used for port power management and shows the Current Link state.</p> <p>When PED is 1, System software sets this bit then sets Link U state.</p> <p>Port Link State is not set to Disabled, RxDetect, or Inactive State</p> <p>Write Value: Description</p> <p>H'0: The link shall transition to the U0 state from any of the U states.</p> <p>H'1: The link should transition to the U1 State.</p> <p>H'2: The link should transition to the U2 State.</p> <p>H'3: The link shall transition to the U3 state from any of the U states.</p> <p>H'4 to H'F: Ignored.</p> <p>To write to this field, the Port Link State Write strobe should be 1.</p> <p>For USB2 Protocol port, writing 2 requests LPM.</p> <p>Software reads this field to determine success/failure of transition to U2 state.</p> <p>Write 0: Deasserts L1 signal</p> <p>Write 1: No influence</p> <p>Read Value Meaning</p> <p>H'0: Link is in the U0 State</p> <p>H'1: Link is in the U1 State</p> <p>H'2: Link is in the U2 State</p> <p>H'3: Link is in the U3 State (Device Suspended)</p> <p>H'4: Link is in the Disabled State</p> <p>H'5: Link is in the RxDetect State</p> <p>H'6: Link is in the Inactive State</p> <p>H'7: Link is in the Polling State</p> <p>H'8: Link is in the Recovery State</p> <p>H'9: Link is in the Hot Reset State</p> <p>H'A: Link is in the Compliance Mode State</p> <p>H'B: Link is in the Loopback State</p> <p>H'C to H'F: Reserved</p> <p>If Port Power is 0, this field is ambiguous.</p>
4	PR	0	R/W	<p>Port Reset</p> <p>0: Port is not in reset</p> <p>1: Port reset assert</p> <p>When software sets this bit from 0 to 1, the bus reset sequence is started.</p> <p>Port Enable/Disable bit is 0.</p> <p>Port Enable bit is 0.</p> <p>This bit remains set to 1 until reset by root hub is completed.</p> <p>When error is detected during resetting, Port Speed field indicates Unknown Speed.</p> <p>If Port Power is 0, this field is set to 0.</p>

Bit	Bit Name	Initial Value	R/W	Description
3	OCA	0	R	Over-current Active 0: Over-current condition 1: Not over-current condition When an over-current condition is removed, this bit changes from 1 to 0 automatically.
2	—	0	R	Reserved
1	PED	0	RW1C	Port Enable/Disable 0: Disable 1: Enable After detecting a connection at a port, if SS port initialization or reset by the system software is successful, this bit is automatically enabled by xHC. Port is disabled by fault condition (disconnect event or other fault condition), or USB System Software. Bit status doesn't change until port status changes. If Port Power is 0, this field is set to 0.
0	CCS	R	R	Current Connect Status 0: No device is present 1: Device is present on port Reflects current port status. If Port Power is 0, this field is set to 0.

**(10) PORTMSC1**

Register setting value of SuperSpeed USB link U-State timeout.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FLA
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	U2 Timeout								U1 Timeout							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 17	—	All 0	R	Reserved
16	FLA	0	R/W	Force Link PM Accept Write 1: Set Link Function LMP with Force_LinkPM_Accept bit set is generated This bit is set to 0 when PR is 1 or CCS changes from 0 to 1.
15 to 8	U2 Timeout	H'00	R/W	U2 inactivity timer Timeout value. If H'FF, port is in the U2 entry disabled state. H'00: Zero (default) H'01: 256 $\mu$ s H'02: 512 $\mu$ s ... H'FE: 65.28 ms H'FF: Infinite
7 to 0	U1 Timeout	H'00	R/W	U1 inactivity timer Timeout value. If H'FF, port is in the U1 entry disabled state. H'00: Zero (default) H'01: 1 $\mu$ s H'02: 2 $\mu$ s ... H'7F: 127 $\mu$ s H'80 to H'FE: Reserved H'FF: Infinite

**(11) PORTMSC2**

Register setting LPM information and controlling USB2.0 port test mode.

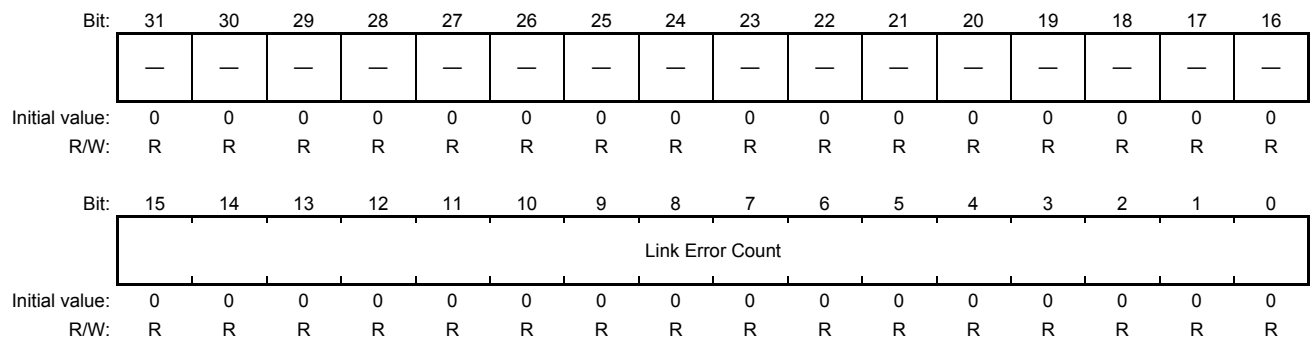
Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Port Test Control												—	—	—	HLE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R	R	R	R	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	L1 Device Slot								HIRD				RWE	L1S		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 28	Port Test Control	H'0	R/W	0: port is not operating in test mode Non-zero: port is operating in test mode A non-zero Port Test Control value is valid when the port is in the Disabled, Disconnected, or Suspend State. <USB2 protocol port> Value    Test Mode H'0:     Test mode not enabled H'1:     Test J_STATE H'2:     Test K_STATE H'3:     Test SE0_NAK H'4:     Test Packet H'5:     Test FORCE_ENABLE H'6 to H'E: Reserved H'F:     Port Test Control Error
27 to 17	—	All 0	R	Reserved
16	HLE	0	R/W	Hardware LPM Enable Writing 1 enables hardware controlled LPM. If Hardware LMP is not supported, this bit is reserved.
15 to 8	L1 Device Slot	H'00	R/W	Device Slot ID of Device directly connected to Root Hub Port. 0: No device
7 to 4	HIRD	H'0	R/W	Host Initiated Resume Duration Duration of Resume that xHC drives to start resume from L1 state.
3	RWE	0	R/W	Remote Wake Enable This bit is set to enable or disable device for Remote Wakeup from L1.

Bit	Bit Name	Initial Value	R/W	Description
2 to 0	L1S	000	R	<p>L1 Status</p> <p>Software uses this field to determine whether L1-based suspend request is successful.</p> <p>Value Meaning</p> <p>000: Invalid</p> <p>001: Success - Port succeed in transition to L1 during resume request (ACK)</p> <p>010: Not Yet - Device fails to transition to L1 (NYET)</p> <p>011 Not Supported - Device doesn't support L1 transitions (STALL)</p> <p>100: Timeout/Error - Device fails LPM Transaction or error occurs</p> <p>101 to 111: Reserved</p> <p>This field is valid when port is in either L0 or L1 state (PLS = 0 or 2).</p>

**(12) PORTLI**

Register indicating Link Error Count of USB3.0 SuperSpeed Port.



Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved
15 to 0	Link Error Count	H'0000	R	Shows Link Error detected Port.



### 54.3.2.3 USB Legacy Support Capability Register

Register set used for supporting System Legacy operation.

Beginning address of USB Legacy Support Capability Register is directed as follows by the Extended Capability Pointer.

Base Address = {Extended Capability Pointer[15:0], B'00 }

No.	Offset	Base Offset	Register	Default Value (H)	Function
1	H'00	H'500	USBLEGSUP	H'0000 0401	USB Legacy Support Capability Register
2	H'04	H'504	USBLEGCTLSTS	H'0000 0000	USB Legacy Support Control and Status Register

#### (1) USBLEGSUP

Register for control of xHC ownership by pre-OS software (BIOS) and operating system (OS).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	HC OS Owned Semaphore	—	—	—	—	—	—	—	HC BIOS Owned Semaphore
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R	R	R	R	R	R	R	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Next Capability Pointer								Capability ID							
Initial value:	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 25	—	All 0	R	Reserved
24	HC OS Owned Semaphore	0	R/W	System Software sets this bit to request xHC ownership. When this bit is 1 and the HC BIOS Owned Semaphore bit is 0, then the OS gets ownership.
23 to 17	—	All 0	R	Reserved
16	HC BIOS Owned Semaphore	0	R/W	BIOS sets this bit to establish xHC ownership. If there is an ownership request from the System Software, the BIOS sets this bit to 0.
15 to 8	Next Capability Pointer	H'04	R	Location of next Capability
7 to 0	Capability ID	H'01	R	Extended Capability This field is fixed to H'01 due to the Legacy Support Capability.

**(2) USBLEGCTLSTS**

Register for enabling System Management Interrupts (SMIs).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SMI on BAR	SMI on PCI Command	SMI on OS Ownership Change	—	—	—	—	—	—	—	—	SMI on Host System Error	—	—	—	SMI on Event Interrupt
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	RW1C	RW1C	RW1C	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SMI on BAR Enable	SMI on PCI Command Enable	SMI on OS Ownership Change Enable	—	—	—	—	—	—	—	—	SMI on Host System Error	—	—	—	USB SMI Enable
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R	R	R	R	R	R	R	R	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	SMI on BAR	0	RW1C	This bit is set to 1 when the Bass Address Register is written.
30	SMI on PCI Command	0	RW1C	This bit is set to 1 when the PCI Command Register is written.
29	SMI on OS Ownership Change	0	RW1C	This Bit is set to 1 when the HC OS Owned Semaphore bit in the USBLEGSUP register changes from 1 to 0, or from 0 to 1.
28 to 21	—	All 0	R	Reserved
20	SMI on Host System Error	0	R	Shadow bit of the Host System Error Interrupt bit in the USBSTS register. If this bit is set to 0, the System Software shall set the Host System Error Interrupt bit in the USBSTS register to 1.
19 to 17	—	All 0	R	Reserved
16	SMI on Event Interrupt	0	R	Shadow bit of the Event Interrupt (EINT) bit in USBSTS register. If EINT is set, this bit is also set. If EINT is cleared, this bit is also cleared.
15	SMI on BAR Enable	0	R/W	If this bit is 1 and SMI on the BAR bit is 1, the Host controller issues SMI.
14	SMI on PCI Command Enable	0	R/W	If this bit is 1 and SMI of the PCI Command bit is 1, the Host controller issues SMI.
13	SMI on OS Ownership Change Enable	0	R/W	If this bit is 1 and SMI of the OS Ownership Change bit is 1, the Host controller issues SMI.
12 to 5	—	All 0	R	Reserved
4	SMI on Host System Error Enable	0	R/W	If this bit is 1 and SMI of the Host System Error bit is 1, the Host controller issues SMI immediately.
3 to 1	—	All 0	R	Reserved
0	USB SMI Enable	0	R/W	If this bit is 1 and SMI of the SMI Event Interrupt bit is 1, the Host controller issues SMI immediately.

### 54.3.2.4 xHCI Supported Protocol Capability Register

The xHCI Supported Protocol Capability is defined in the xHCI specification.

The beginning address of the xHCI Supported Protocol Capability Register is;

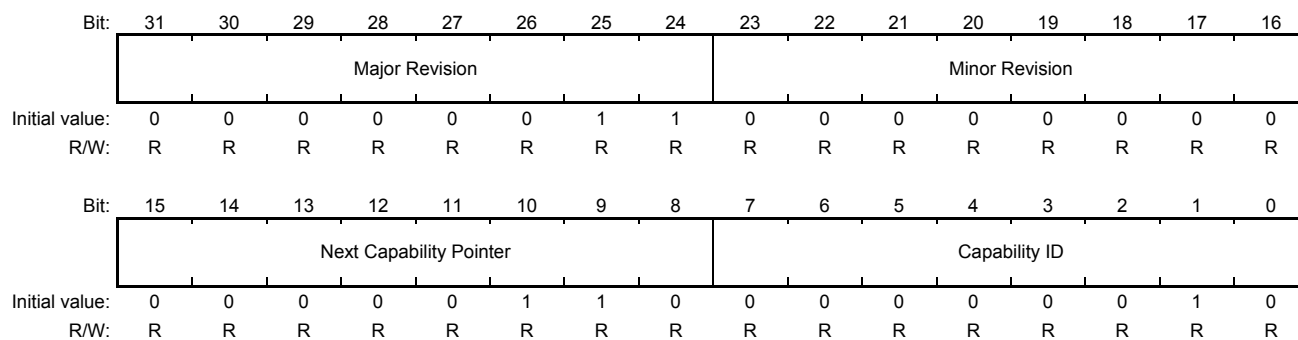
The beginning address of the USB Legacy Support Capability Register + USB Legacy Support Capability

Register's Next Item Pointer (relative DW Offset)

No.	Offset	Base Offset	Default Value (H)	Function
1	H'00	H'510	H'0300 0602	xHCI Supported Protocol Capability
2	H'04	H'514	H'2042 5355	(USB3.0)
3	H'08	H'518	H'0000 0101	
4	H'10	H'520	H'0000 0000	PSI (SuperSpeed)
5	H'18	H'528	H'0200 0802	xHCI Supported Protocol Capability
6	H'1C	H'52C	H'2042 5355	(USB2.0)
7	H'20	H'530	H'0000 0102	
8	H'28	H'538	H'0000 0000	PSI (Full-Speed)
9	H'2C	H'53C	H'0000 0000	PSI (Low-Speed)
10	H'30	H'540	H'0000 0000	PSI (High-Speed)

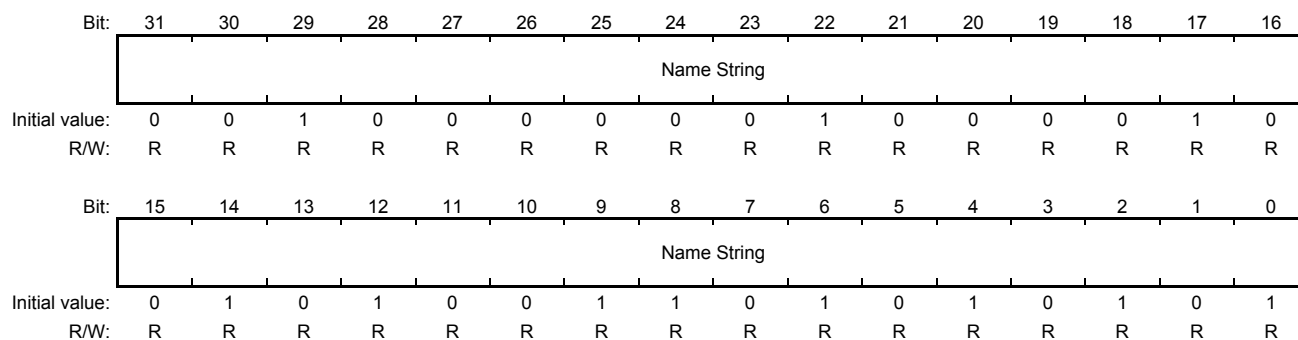
#### (1) xHCI Supported Protocol Capability (USB3.0)

##### (a) AXI Offset H'00



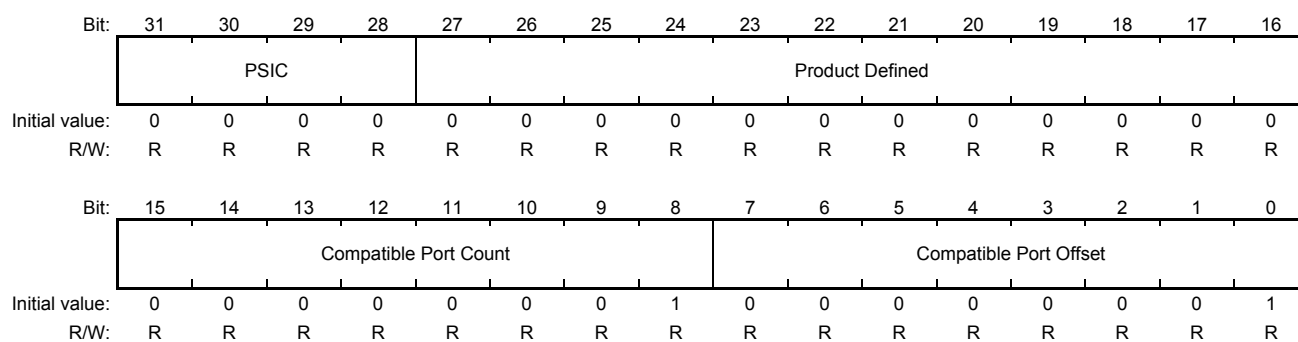
Bit	Bit Name	Initial Value	R/W	Description
31 to 24	Major Revision	H'03	R	Major release number compliant with xHC specification.
23 to 16	Minor Revision	H'00	R	Minor release number compliant with xHC specification.
15 to 8	Next Capability Pointer	H'06	R	Next Capability Location
7 to 0	Capability ID	H'02	R	Extended Capability Fixed to H'02 due to xHCI Supported Protocol Capability

**(b) AXI Offset H'04**



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	Name String	H'2042 5355	R	Mnemonic name string compliant with xHC specification

**(c) AXI Offset H'08**



Bit	Bit Name	Initial Value	R/W	Description
31 to 28	PSIC	H'0	R	Product Speed ID Count Number of the Product Speed IDs that this protocol supports.
27 to 16	Product Defined	H'000	R	Reserved
15 to 8	Compatible Port Count	H'01	R	Number of the Root Hub Ports that this protocol supports.
7 to 0	Compatible Port Offset	H'01	R	Starting Port Number of the Root Hubs that this protocol supports.

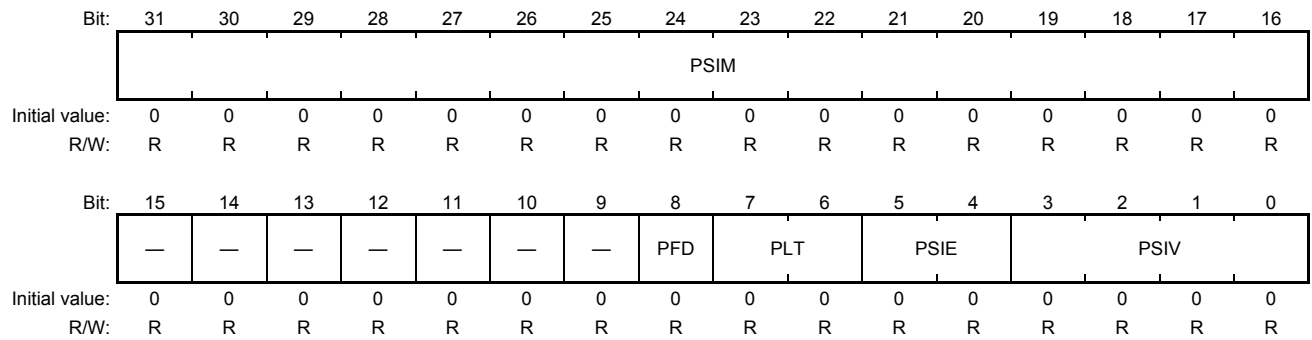
Compatible Port Offset is the starting port number of the ports that this protocol supports.

Compatible Port Count is the number of ports that this protocol supports.

In the case of the Host Core, the number of the USB3.0 (Super Speed) Port starts from 1, and the port number is indicated as 1.

PSIC (31:28) is the PSI number that the protocol supports.

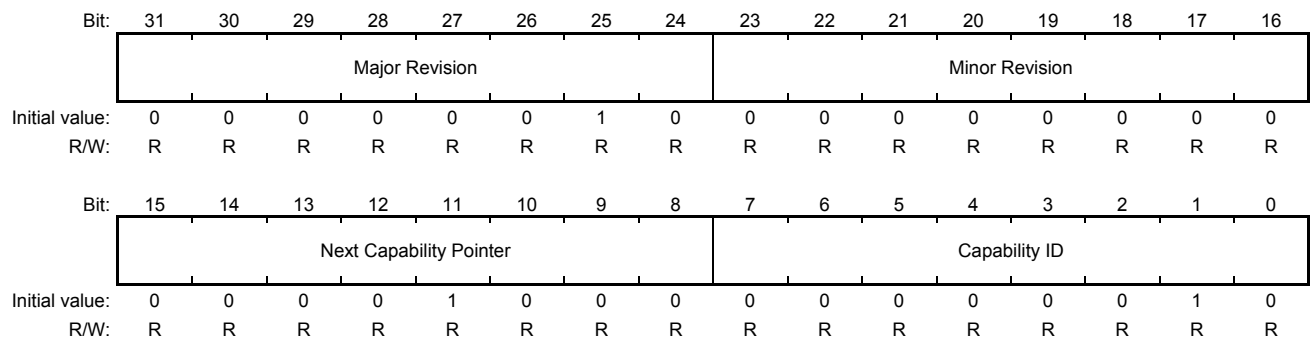
**(d) AXI Offset H'10 (PSI: SuperSpeed)**



Bit	Bit Name	Initial Value	R/W	Description
31 to 16	PSIM	H'0000	R	Product Speed ID Mantissa Maximum bit rate defined in this PSI register. Used with the PSIE field.
15 to 9	—	All 0	R	Reserved
8	PFD	0	R	PSI Full-duplex 0: Link is half-duplex. 1: Link is full-duplex.
7, 6	PLT	00	R	PSI Type Shows whether Symmetric or Asymmetric bit rate is defined for this PSI Register. 00: Symmetric 01: Reserved 10: Asymmetric Rx (Used with Tx PSI Dword) 11: Asymmetric Tx
5, 4	PSIE	00	R	Protocol Speed ID Exponent Unit indicated in PSIM. Value Bit Rate 00: Bits per second 01: Kb/s 10: Mb/s 11: Gb/s
3 to 0	PSIV	0000	R	Protocol Speed ID Value Used for reporting the Bit rate defined in the PSI register of the Port Speed bits in PORTSC.

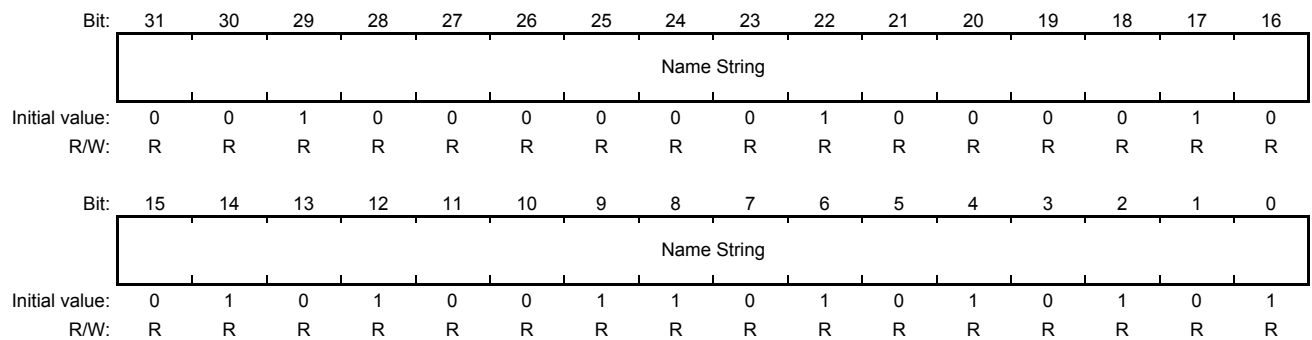
**(2) xHCI Supported Protocol Capability (USB2.0)**

**(a) AXI Offset H'00**



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	Major Revision	H'02	R	Major release number compliant with xHC specification.
23 to 16	Minor Revision	H'00	R	Minor release number compliant with xHC specification.
15 to 8	Next Capability Pointer	H'08	R	Next Capability Location
7 to 0	Capability ID	H'02	R	Extended Capability Fixed to H'02 due to xHCI Supported Protocol Capability

**(b) AXI Offset H'04**



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	Name String	H'2042 5355	R	Mnemonic name string compliant with xHC specification

(c) AXI Offset H'08

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PSIC				—	—	—	—	—	—	—	—	HLC	IHI	HSO	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Compatible Port Count								Compatible Port Offset							
Initial value:	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 28	PSIC	H'0	R	Product Speed ID Count Number of Product Speed IDs that this protocol supports.
27 to 20	—	All 0	R	Reserved
19	HLC	0	R	Hardware LPM Capability 1: Indicates whether hardware controlled LPM is supported
18	IHI	0	R	Integrated Hub Implemented 1: Root Hub and Port mapping of External xHC port are not compliant with default mapping specified in 4.24.2.1 in xHCI Spec.
17	HSO	0	R	High-speed Only 1: USB2 Port indicated with this Capability is HS Only
16	—	0	R	Reserved
15 to 8	Compatible Port Count	H'01	R	Number of Root Hub Ports that this protocol supports.
7 to 0	Compatible Port Offset	H'02	R	Starting Port Number of Root Hubs that this protocol supports.

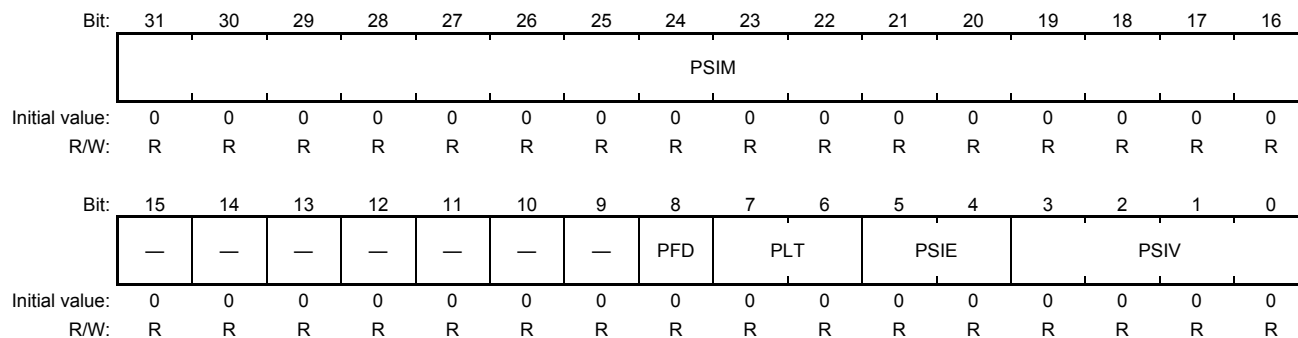
Compatible Port Offset is the starting port number of the ports that this protocol supports.

Compatible Port Count is the number of ports that this protocol supports.

In the case of the Host Core, the number of the USB2.0 Port starts from 2, and the port number is indicated as 1.

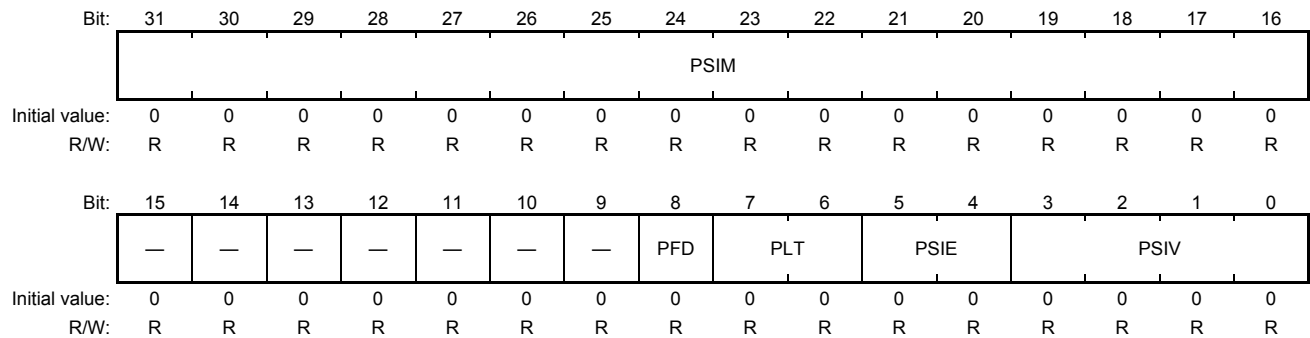
PSIC (31:28) is the PSI number that the protocol supports.

**(d) AXI Offset H'10 (PSI: Full-Speed)**



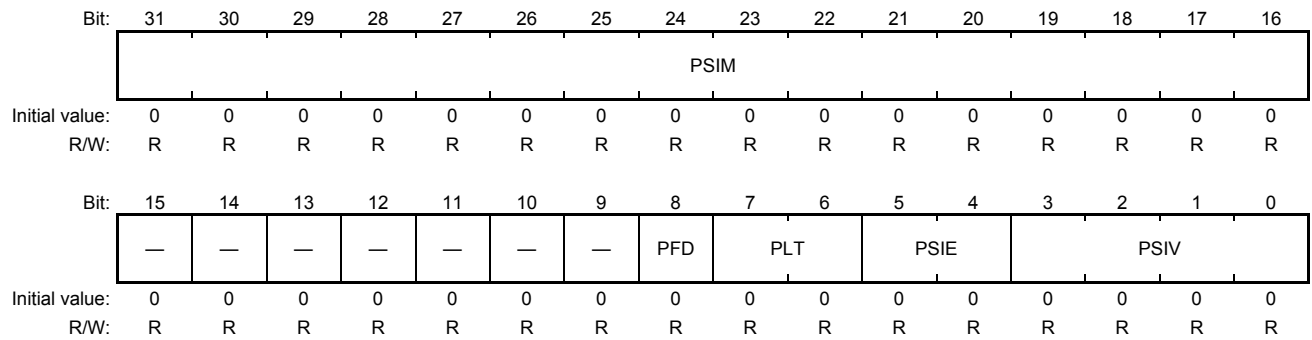
Bit	Bit Name	Initial Value	R/W	Description
31 to 16	PSIM	H'0000	R	Product Speed ID Mantissa Maximum bit rate defined in this PSI register. Used with the PSIE field.
15 to 9	—	All 0	R	Reserved
8	PFD	0	R	PSI Full-duplex 0: Link is half-duplex. 1: Link is full-duplex.
7, 6	PLT	00	R	PSI Type Shows whether Symmetric or Asymmetric bit rate is defined for this PSI Register. 00: Symmetric 01: Reserved 10: Asymmetric Rx (Used with Tx PSI Dword) 11: Asymmetric Tx
5, 4	PSIE	00	R	Protocol Speed ID Exponent Unit indicated in PSIM. Value Bit Rate 00: Bits per second 01: Kb/s 10: Mb/s 11: Gb/s
3 to 0	PSIV	0000	R	Protocol Speed ID Value Used for reporting the Bit rate defined in the PSI Register of the Port Speed field in PORTSC.



**(e) AXI Offset H'14 (PSI: Low-Speed)**

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	PSIM	H'0000	R	Product Speed ID Mantissa Maximum bit rate defined in this PSI register. Used with the PSIE field.
15 to 9	—	All 0	R	Reserved
8	PFD	0	R	PSI Full-duplex 0: Link is half-duplex. 1: Link is full-duplex.
7, 6	PLT	00	R	PSI Type Shows whether Symmetric or Asymmetric bit rate is defined for this PSI Registers. 00: Symmetric 01: Reserved 10: Asymmetric Rx (Used with Tx PSI Dword) 11: Asymmetric Tx
5, 4	PSIE	00	R	Protocol Speed ID Exponent Unit indicated in PSIM. Value    Bit Rate 00:     Bits per second 01:     Kb/s 10:     Mb/s 11:     Gb/s
3 to 0	PSIV	0000	R	Protocol Speed ID Value Used for reporting the Bit rate defined in the PSI Register of the Port Speed field in PORTSC.

**(f) AXI Offset H'18 (PSI: High-Speed)**



Bit	Bit Name	Initial Value	R/W	Description
31 to 16	PSIM	H'0000	R	Product Speed ID Mantissa Maximum bit rate defined in this PSI register. It is used with PSIE field.
15 to 9	—	All 0	R	Reserved
8	PFD	0	R	PSI Full-duplex 0: Link is half-duplex. 1: Link is full-duplex.
7, 6	PLT	00	R	PSI Type Shows Symmetric or Asymmetric bit rate is defined for this PSI Register. 00: Symmetric 01: Reserved 10: Asymmetric Rx (Used with Tx PSI Dword) 11: Asymmetric Tx
5, 4	PSIE	00	R	Protocol Speed ID Exponent Unit indicated in PSIM. Value Bit Rate 00: Bits per second 01: Kb/s 10: Mb/s 11: Gb/s
3 to 0	PSIV	0000	R	Protocol Speed ID Value Used for reporting the Bit rate defined in the PSI Register of the Port Speed field in PORTSC.

If PSIC is 0 in both the USB2.0 and USB3.0 protocol, the following are used as default values.

Default Speed ID Value	Definition	Bit Rate	Protocol	Equivalent PSI Dword value			
				PLT	PFD	PSIE	PSIM
1	Full-Speed	12 Mb/s	USB2.0	0	0	2	12
2	Low-Speed	1.5 Mb/s	USB2.0	0	0	1	1500
3	High-Speed	480 Mb/s	USB2.0	0	0	2	480
4	Super-Speed	5 Gb/s	USB3.0	0	1	3	5

### 54.3.2.5 xHCI Extended Power Management Capability Register

This Capability is equivalent to the PCI Power Management Capability in AXI Configuration.

This Capability is needed when the xHC System Interface is other than PCI.

However the value set for the Next Capability Pointer is compliant with the xHCI specification.

#### (a) AXI Offset H'00

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PMES D3cold	PMES D3hot	PMES D2	PMES D1	PMES D0	D2 Support	D1 Support	AUX Current			DSI	—	PME Clock	Version		
Initial value:	0	1	0	0	1	0	0	0	0	0	0	0	0	0	1	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Next Capability Pointer							Capability ID								
Initial value:	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31	PMESD3cold	0	R	PME Support D3cold Window for accessing contents of AXI Register Power Management Capability Register
30	PMESD3hot	1	R	PME Support D3hot Window for accessing contents of AXI Register Power Management Capability Register
29	PMESD2	0	R	PME Support D2 Window for accessing contents of AXI Register Power Management Capability Register
28	PMESD1	0	R	PME Support D1 Window for accessing contents of AXI Register Power Management Capability Register
27	PMESD0	1	R	PME Support D0 Window for accessing contents of AXI Register Power Management Capability Register
26	D2 Support	0	R	Window for accessing contents of AXI Register Power Management Capability Register
25	D1 Support	0	R	Window for accessing contents of AXI Register Power Management Capability Register
24 to 22	AUX Current	000	R	Window for accessing contents of AXI Register Power Management Capability Register
21	DSI	0	R	Window for accessing contents of AXI Register Power Management Capability Register
20	—	0	R	Reserved
19	PME Clock	0	R	Window for accessing contents of AXI Register Power Management Capability Register
18 to 16	Version	011	R	Window for accessing contents of AXI Register Power Management Capability Register

Bit	Bit Name	Initial Value	R/W	Description
15 to 8	Next Capability Pointer	H'02	R	Relative Pointer to next Capability Fixed to H'02
7 to 0	Capability ID	H'03	R	Capability ID H'03: Extended Power Management Capability Fixed to H'03

**(b) AXI Offset H'04**

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PME Status	Data Scale	Data Select				PME Enable	—	—	—	—	No Soft Reset	—	Power State		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
R/W:	RW1CS	R	R	R	R	R	R	RWS	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved
15	PME Status	0	RW1CS	Window for accessing contents of AXI Register Power Management Status/Control Register
14 to 13	Data Scale	00	R	Window for accessing contents of AXI Register Power Management Status/Control Register
12 to 9	Data Select	0000	R	Window for accessing contents of AXI Register Power Management Status/Control Register
8	PME Enable	0	RWS	Window for accessing contents of AXI Register Power Management Status/Control Register
7 to 4	—	All 0	R	Reserved
3	No Soft Reset	1	R	Window for accessing contents of AXI Register Power Management Status/Control Register
2	—	0	R	Reserved
1 to 0	Power State	00	R/W	Window for accessing contents of AXI Register Power Management Status/Control Register

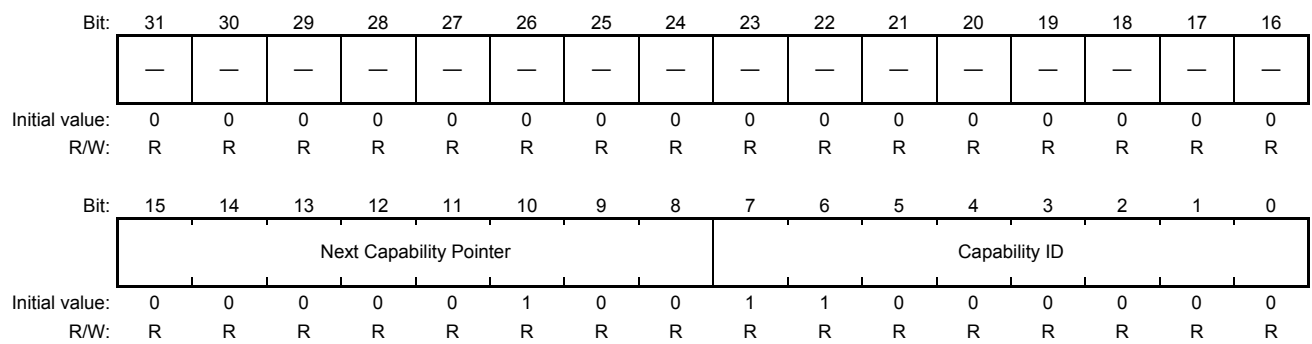
**54.3.2.6 xHCI Vender Defined Capability Register**

According to the xHCI specification, when using and defining the Vender Defined Command, the following conditions are specified. This capability is prepared for them.

- Create xHCI Extended Capability Register(Vender Defined)
- Permit enable/disable setting for Vender Defined function by Driver with Create xHCI Extended Capability Register.
- Do not use this function until validation.

No.	Offset	Base Offset	Default Value (H)	Function
1	H'00	H'550	H'0000 04C0	xHCI Vender Defined Capability
2	H'04	H'554	H'0000 0000	Command Enable

**(a) AXI Offset H'00**



Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved
15 to 8	Next Capability Pointer	H'04	R	Relative Pointer to next Capability Fixed to H'04
7 to 0	Capability ID	H'C0	R	Capability ID H'C0: Extended Power Management Capability Fixed to H'C0

**(b) AXI Offset H'04**

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	Command Enable
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

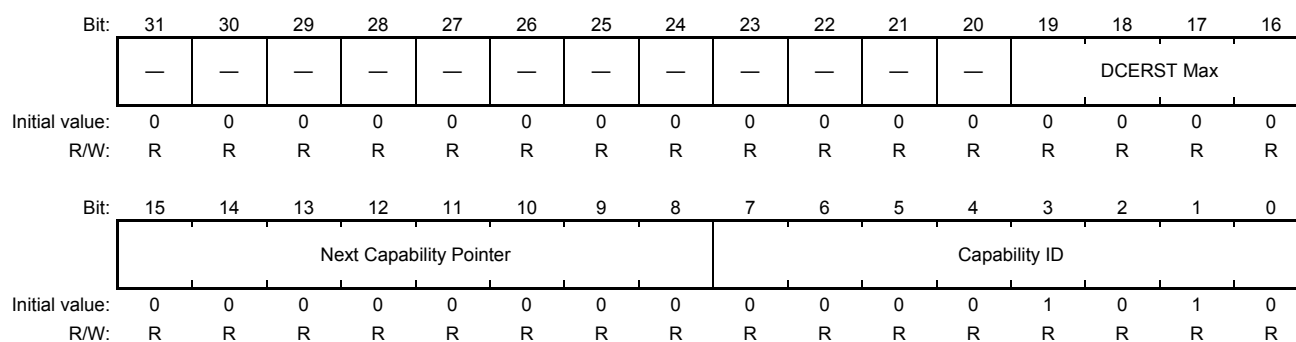
Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved
0	Command Enable	0	R/W	0: Disable Vender Defined Command 1: Enable Vender Defined Command

### 54.3.2.7 Debug Capability Register

Capability for Debug Port Function.

No.	Offset	Base Offset	Default Value (H)	Function
1	H'00	H'560	H'0000 000A	Debug Capability (DCID)
2	H'04	H'564	H'0000 0000	DCDB
3	H'08	H'568	H'0000 0000	DCERSTSZ
4	H'10	H'570	H'0000 0000	DCERSTBAL
5	H'14	H'574	H'0000 0000	DCERSTBAH
6	H'18	H'578	H'0000 0000	DCERDPL
7	H'1C	H'57C	H'0000 0000	DCERDPH
9	H'20	H'580	H'0000 0000	DCCTRL
10	H'24	H'584	H'0000 0000	DCST
11	H'28	H'588	H'0000 0080	DCPORTSC
12	H'30	H'590	H'0000 0000	DCCP0
13	H'34	H'594	H'0000 0000	DCCP1

#### (a) AXI Offset H'00 (DCID)



Bit	Bit Name	Initial Value	R/W	Description
31 to 20	—	All 0	R	Reserved
19 to 16	DCERST Max	0000	R	Maximum number of the debug capability event ring segment table base size register that this debug capability has. Maximum number of Event Ring Segment Table entries = $2^{\text{DCERST Max}}$ .
15 to 8	Next Capability Pointer	H'00	R	Relative pointer to next capability. Fixed to H'00 due to there being no next capability.
7 to 0	Capability ID	H'0A	R	Capability ID H'0A: Debug capability Fixed to H'0A

**(b) AXI Offset H'04 (DCDB)**

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Doorbell Target								—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved
15 to 8	Doorbell Target	H'00	R/W	Doorbell Target Value Definition H'00: Data EP 1 OUT Enqueue Pointer Update H'01: Data EP 1 IN Enqueue Pointer Update H'02 to H'FF: Reserved
7 to 0	—	All 0	R	Reserved

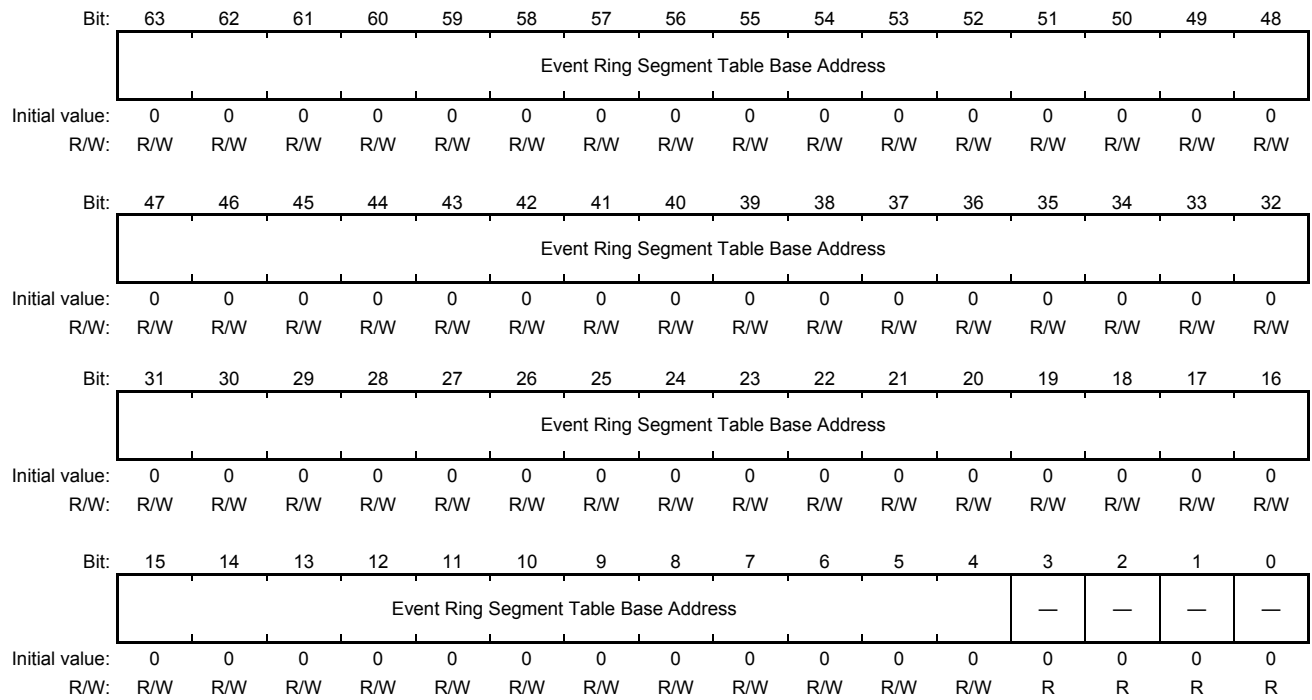
**(c) AXI Offset H'08 (DCERSTSZ)**

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Event Ring Segment Table Size															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved
15 to 0	Event Ring Segment Table Size	H'0000	R/W	Indicates the number of valid Debug Capability Event Ring Segment Table Entries. The maximum number is defined by the DCERST Max field.

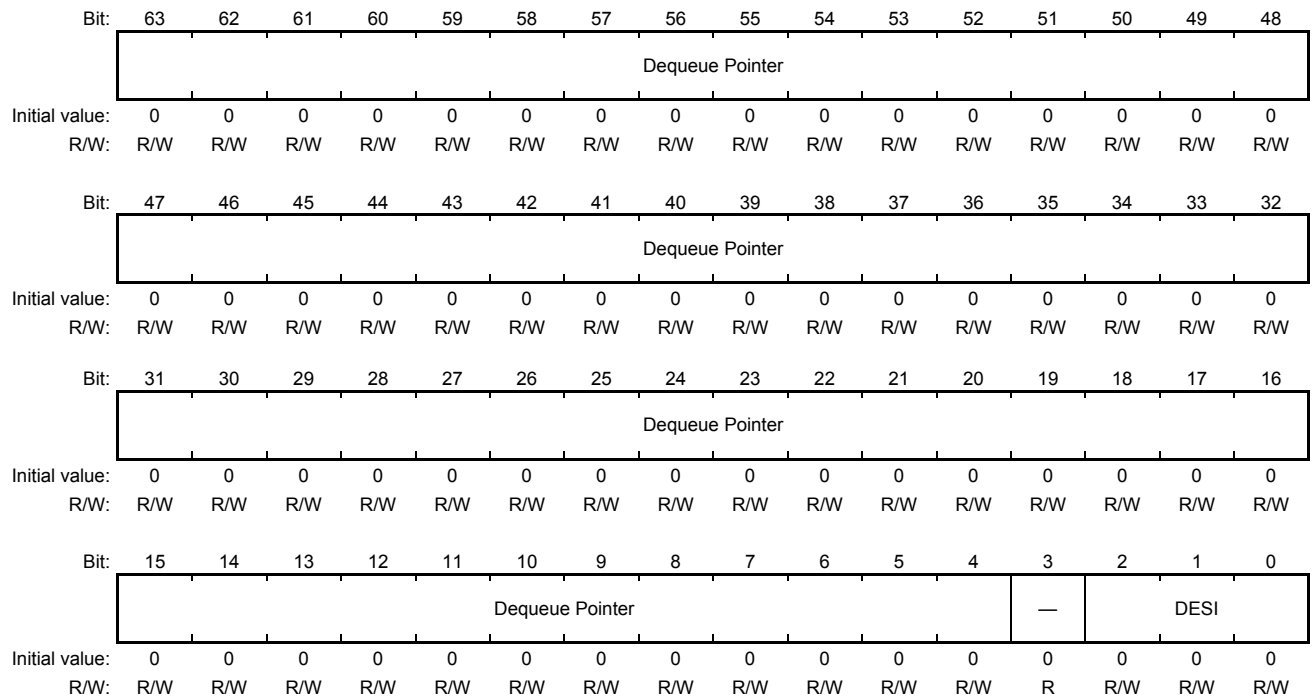


**(d) AXI Offset H'10 (DCERSTBA)**



Bit	Bit Name	Initial Value	R/W	Description
63 to 4	Event Ring Segment Table Base Address	H'000 0000 0000 0000	R/W	Start Address of Debug Capability Event Ring Segment Table. When define AXI_MASTER_ADDRESS_WIDTH_64 is not set, address Hi is fixed to 0.
3 to 0	—	All 0	R	Reserved

(e) AXI Offset H'18 (DCERDP)



Bit	Bit Name	Initial Value	R/W	Description
63 to 4	Dequeue Pointer	H'000 0000 0000 0000	R/W	Address of Debug Capability Event Ring Dequeue Pointer. When define AXI_MASTER_ADDRESS_WIDTH_64 is not set, address Hi is fixed to 0.
3	—	All 0	R	Reserved
2 to 0	DESI	000	R/W	Dequeue ERST Segment Index The field is used for the confirmation of the Event Ring full condition by xHC.

**(f) AXI Offset H'20 (DCCTRL)**

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DCE	Device Address							Debug Max Burst Size							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	DRC	HIT	HOT	LSE	DCR
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	RW1C	RW1S	RW1S	R/W	R

Bit	Bit Name	Initial Value	R/W	Description
31	DCE	0	R/W	Debug Capability Enable If this bit is set to 1, then the xHCI USB Debug Capability is enabled.
30 to 24	Device Address	H'00	R	USB device address when debug device is enumerated
23 to 16	Debug Max Burst Size	H'00	R	Max Burst Size of Bulk Endpoint in DBC
15 to 5	—	All 0	R	Reserved
4	DRC	0	RW1C	DbC Run Change This bit is set to 1 when DCR is set to 0. Cannot be accessed while this bit is 1.
3	HIT	0	RW1S	Halt IN TR When this bit changes from 0 to 1, the HIT_SET bit in the DTU.STS2 register is set to 1. This bit status doesn't influence EP1 OUT Endpoint. This bit is fixed to 0 while DCR is 0.
2	HOT	0	RW1S	Halt OUT TR When this bit changes from 0 to 1, the HOT_SET bit in the DTU.STS2 register is set to 1. This bit status doesn't influence EP1 OUT Endpoint. This bit is fixed to 0 while DCR is 0.
1	LSE	0	R/W	Link Status Event Enable This bit is set to 1 when the Port Link Status Change bit changes from 0 to 1, after which a Port Status Change Event is generated.
0	DCR	0	R	DbC Run 0: Debug Device is not in Configured State 1: Debug Device is in Configured State

**(g) AXI Offset H'24 (DCST)**

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Debug Port Number								—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ER
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	Debug Port Number	H'00	R	Root Hub Port Number when Debug Capability is connected.
23 to 1	—	All 0	R	Reserved
0	ER	0	R	Event Ring Not Empty 0: Debug Capability Event Ring is empty 1: There is a Transfer Event in the Debug Capability Event Ring

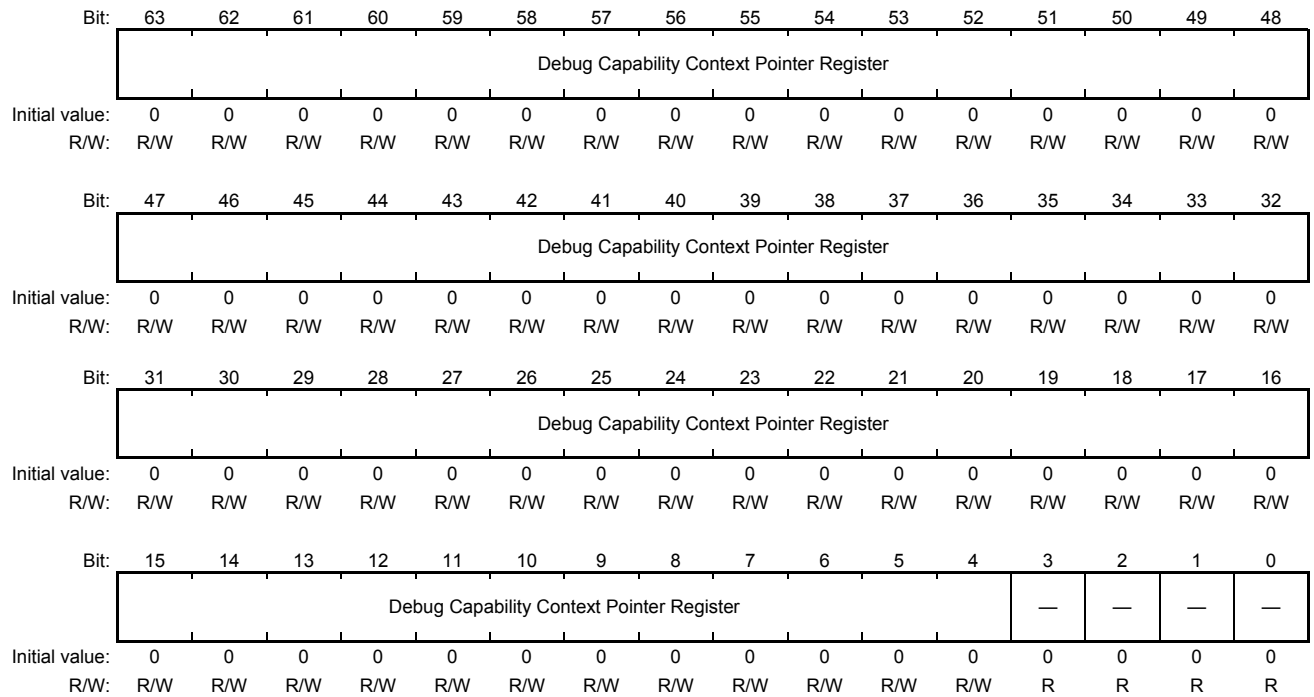
**(h) AXI Offset H'28 (DCPORTSC)**

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	CEC	PLC	PRC	—	—	—	CSC	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	RW1C	RW1C	RW1C	R	R	R	RW1C	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	Port Speed			—	PLS				PR	—	—	PED	CC	
Initial value:	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved
23	CEC	0	RW1C	Port Config Error Change This bit is set to 1 when configuration with Link Partner fails.
22	PLC	0	RW1C	Port Link Status Change This bit is set to 1 when PLC performs the following transition; <Transition Condition> U0 → U3 Suspend signaling detected from Debug Host U3 → U0 Resume complete Polling → Disabled Training Error Ux or Recovery → Inactive Error When DCE is 0, this bit is set to 0.
21	PRC	0	RW1C	Port Reset Change After Port Reset status finishes, this bit is set to 1 (PR 1 → 0) When DCE is 0, this bit is set to 0.
20 to 18	—	All 0	R	Reserved
17	CSC	0	RW1C	Connect Status Change This bit is set to 1 when the CCS bit is changed. When DCE is 0, this bit is set to 0.
16 to 14	—	All 0	R	Reserved
13 to 10	Port Speed	0000	R	CCS = 1: 4 (SuperSpeed) CCS = 0: fixed to 0
9	—	0	R	Reserved
8 to 5	PLS	H'4	R	Port Link Status DCE = 0: fixed to H'4 (Disabled) DCE = 1 and Debug Port Number = 0: fixed to H'5 (RxDetect)
4	PR	0	R	Port Reset When this bit is 1, Port is in Reset.
3, 2	—	All 0	R	Reserved
1	PED	0	R/W	Port Enable/Disable 0: Disabled 1: Enabled When DCE is 0 or CCS is 0, this bit is set to 0.

Bit	Bit Name	Initial Value	R/W	Description
0	CC	0	R	Current Connect Status If Debug Port Number is other than 0, this bit is 1.

(i) AXI Offset H'30 (DCCP)



Bit	Bit Name	Initial Value	R/W	Description
63 to 4	Debug Capability Context Pointer Register	H'000 0000 0000 0000	R/W	Beginning address of Debug Capability Context Pointer When define AXI_MASTER_ADDRESS_WIDTH_64 is not set, address Hi is fixed to 0.
3 to 0	—	All 0	R	Reserved

### 54.3.2.8 Host Controller Runtime Register

Register group for using Runtime during Host Controller operation.

The beginning Address of the Host Controller Runtime Registers is defined as the Runtime Register Space Offset field in the RTSOFF Register and Capability Base Address.

Base Address = Capability Base Address + Runtime Register Space Offset

No.	Offset	Base Offset	Register	Default Value (H)	Function
1	H'00	H'600	MFINDEX	H'0000 0000	Runtime Microframe Index
—	H'1C to H'04	H'604 to H'61F	—	—	Reserved
—	H'20	H'620	IR #0	H'0000 0000	Interrupter Register Set #0

#### (1) MFINDEX

Indicates the current periodic frame.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	Microframe Index													
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 14	—	All 0	R	Reserved
13 to 0	Microframe Index	H'0000	R	Incremented at the end of every microframe (125 μs) Bits [13:3] are used to define the current 1 ms. Frame Index

#### (2) Interrupter Register Set #0

Register controlling Interrupter #0.

No.	Offset	Register	Default Value (H)	Function
—	H'00	IMAN	H'0000 0000	Interrupter Management
—	H'04	IMOD	H'0000 0FA0	Interrupter Moderation
—	H'08	ERSTSZ	H'0000 0000	Event Ring Segment Table Size
—	H'0C	—	H'0000 0000	Reserved
—	H'10	ERSTBA	H'0000 0000 0000 0000	Event Ring Segment Table Base Address
—	H'18	ERDP	H'0000 0000 0000 0000	Event Ring Dequeue Pointer

**(a) AXI Offset H'00 (IMAN)**

This register shows the status of an interrupt and controls enable/disable of Interrupter.

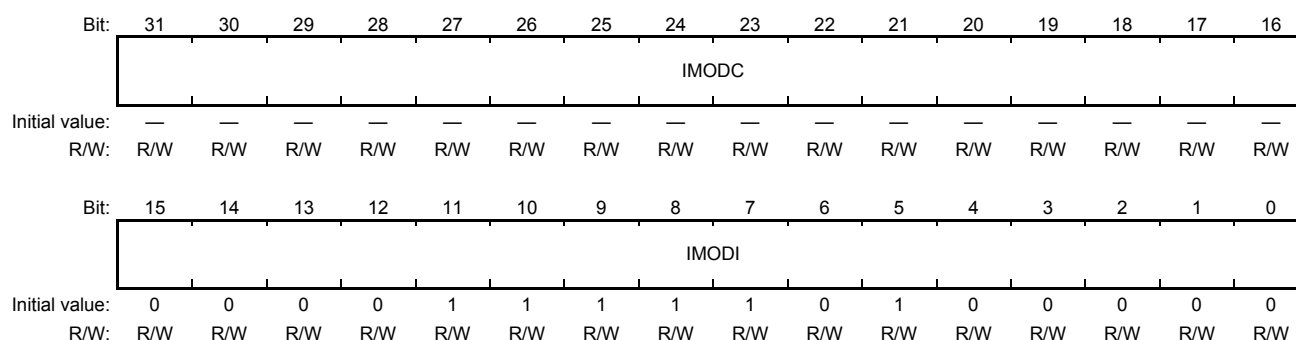
Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IE	IP
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	RWC

Bit	Bit Name	Initial Value	R/W	Description
31 to 2	—	All 0	R	Reserved
1	IE	0	R/W	Interrupt Enable Indicates whether Interrupter can generate an interrupt or not. 0: Does not generate an Interrupt. 1: IP bit is 1, Interrupter Moderation Counter changes to 0 then Interrupter generates an interrupt.
0	IP	0	RWC	Interrupt Pending Current status of Interrupter. 0: Event Ring for Interrupter is empty. There is no pending interrupt. 1: Event Ring for Interrupter is not empty. For interrupter 0, interrupt is pending.



**(b) AXI Offset H'04 (IMOD)**

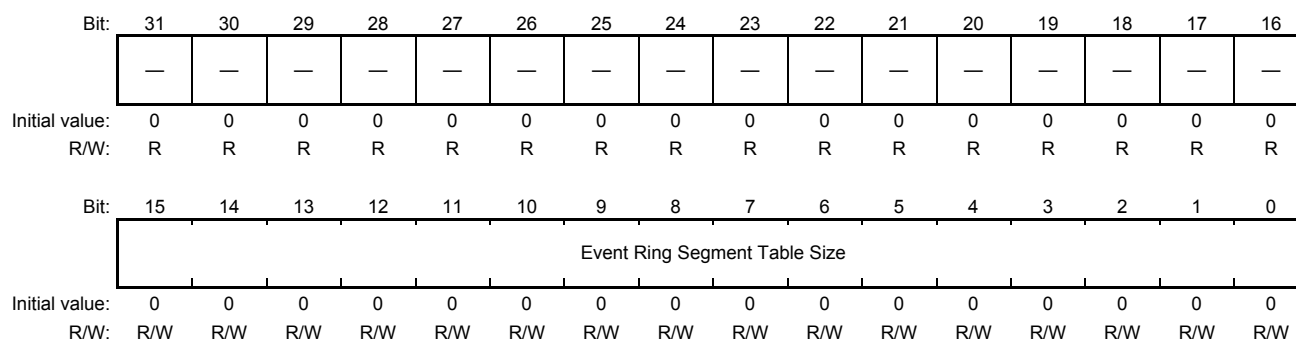
Register for controlling cycle of Moderation of Interrupter.



Bit	Bit Name	Initial Value	R/W	Description
31 to 16	IMODC	undefined	R/W	Down Counter: If IP is cleared to 0, the interval value is loaded and then counted down until 0, at which point the 0 counter will stop. An interrupt is generated when the counter is 0 but Event Ring is not empty and IM and IP bits are 1. Anytime Software can write this counter to change the interrupt rate.
15 to 0	IMODI	H'0FA0	R/W	Minimum value for the inter-interrupt interval. This interval can be set in increments of 250 ns. 0 is not permitted.

**(c) AXI Offset H'08 (ERSTSZ)**

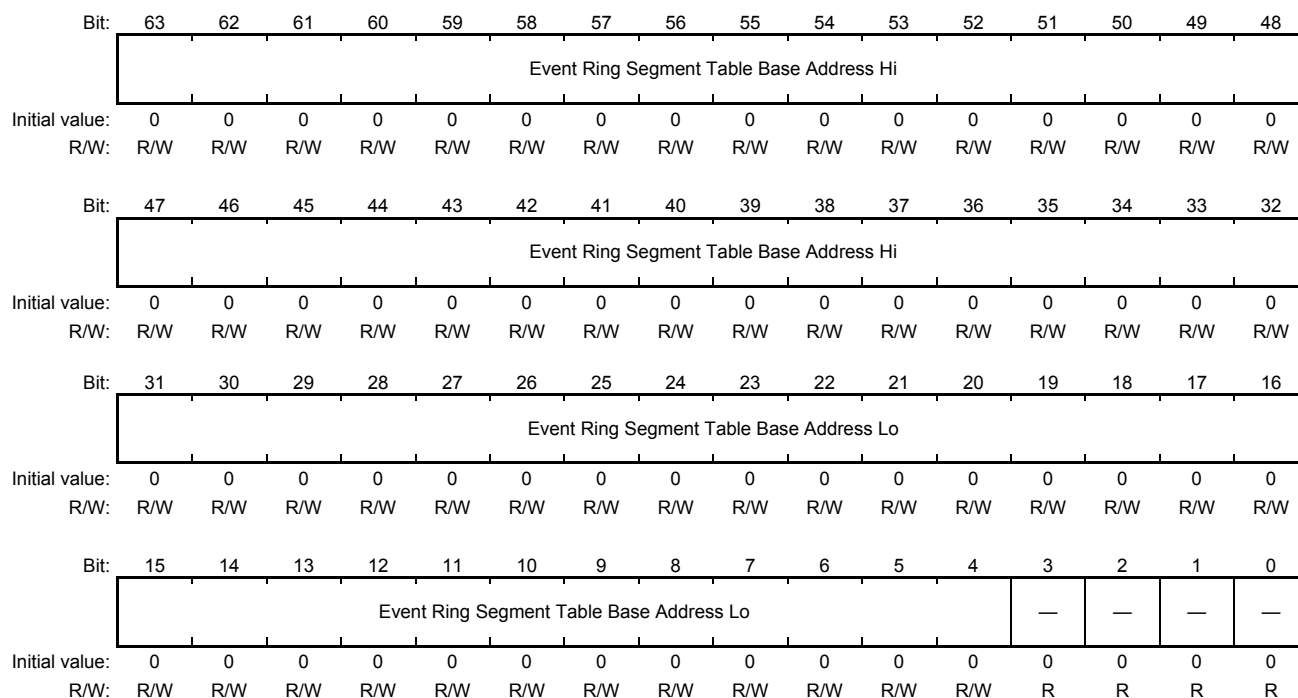
Register for setting number of Event Ring Segment Table entries.



Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved
15 to 0	Event Ring Segment Table Size	H'0000	R/W	Defines the number of valid Event Ring Segment Table entries in the Event Ring Segment Table indicated by Event Ring Segment Table Base Address register. The maximum value supported by xHC is defined by ERST Max field in HSCPARAMS2 Register. xHC ignores bit writing when the Run/Stop bit is set to 1.

**(d) AXI Offset H'10 (ERSTBA)**

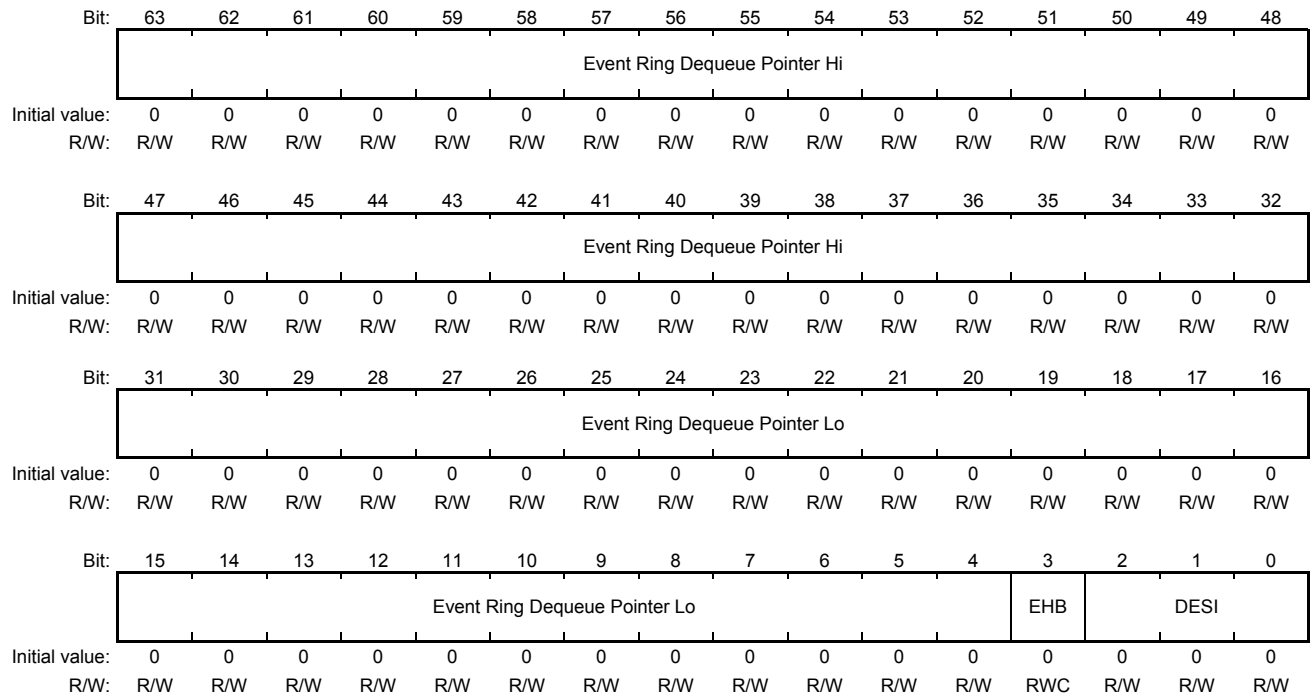
Register for setting the Base Address of the Event Ring Segment Table.



Bit	Bit Name	Initial Value	R/W	Description
63 to 32	Event Ring Segment Table Base Address Hi	H'0000 0000	R/W	Defines the Start Address (Hi) of the Event Ring Segment Table. Upon a write to this Register, the Event Ring State Machine transitions to the Start State. When define AXI_MASTER_ADDRESS_WIDTH_64 is not set, address Hi is fixed to 0.
31 to 4	Event Ring Segment Table Base Address Lo	H'000 0000	R/W	Defines the Start Address (Lo) of the Event Ring Segment Table. Upon a write to this Register, the Event Ring State Machine transitions to the Start State.
3 to 0	—	All 0	R	Reserved

**(e) AXI Offset H'18 (ERDP)**

Register for notification of Event Ring Dequeue Pointer by software



Bit	Bit Name	Initial Value	R/W	Description
63 to 32	Event Ring Dequeue Pointer Hi	H'0000 0000	R/W	Defines the Address (Hi) of Current Dequeue Pointer. Software initializes this Register before the Run/Stop bit is set to 1. When define AXI_MASTER_ADDRESS_WIDTH_64 is not set, address Hi is fixed to 0.
31 to 4	Event Ring Dequeue Pointer Lo	H'000 0000	R/W	Defines the Address (Lo) of the Current Dequeue Pointer. Software initializes the Register before the Run/Stop bit is set to 1.
3	EHB	0	RWC	Event Handler Busy This flag shall be set to '1' when the IP bit is set to '1' and cleared to '0' by software when the Dequeue Pointer register is written.
2 to 0	DESI	000	R/W	Dequeue ERST Segment Index This field is used for confirmation of the Event Ring full condition by xHC.

### 54.3.2.9 Doorbell Register

The Doorbell Register is used for notification of a Device Slot in processing execution on the Host Controller by System Software.

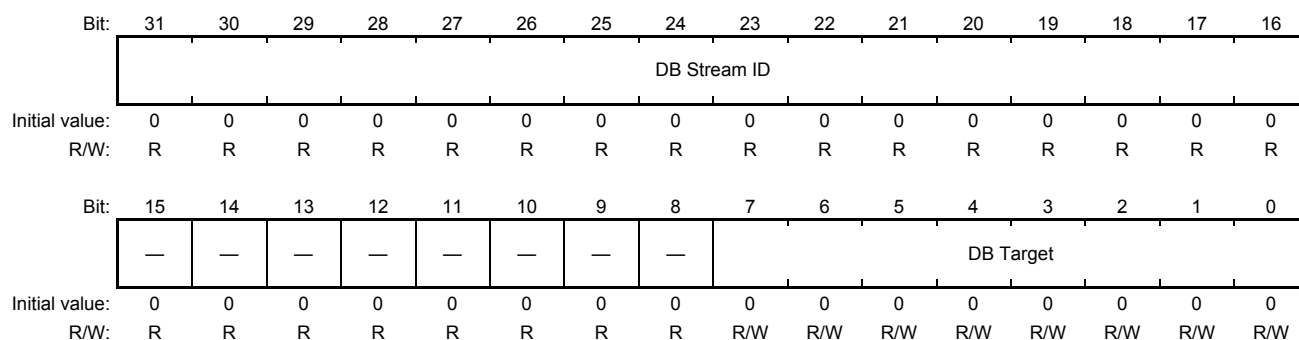
This Register is configured from 33 registers: 1 Host Controller Doorbell and 32 Device Context Doorbells.

The Doorbell Base Address is Dword Align, and provides the Doorbell Array Offset in the Doorbell Offset Register and the Base Address in the xHCI operational register address.

Base Address = Operational Base address + Doorbell Array Offset

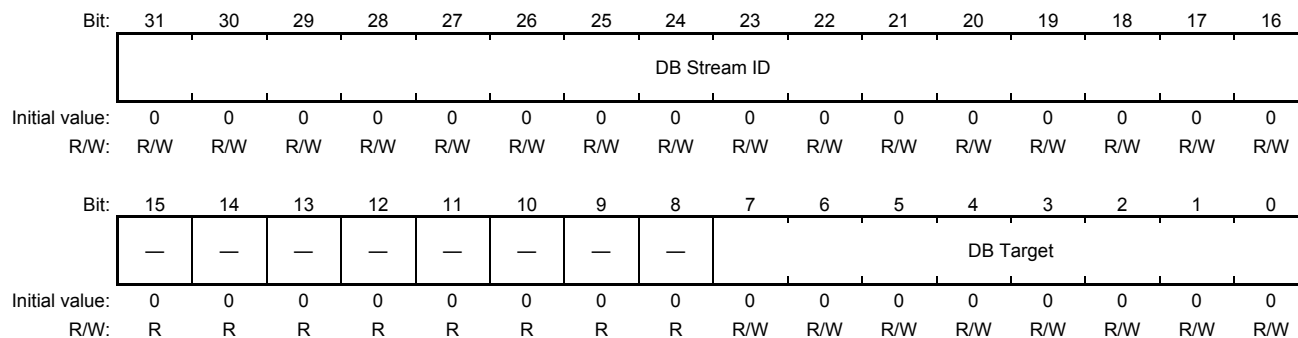
No.	Offset	Base Offset	Register	Default Value (H)	Function
1	H'00	H'800	DOORBELL0	H'0000 0000	Host Controller Doorbell
2	H'80 to H'04	H'880 to H'804	DOORBELL1 to 32	H'0000 0000	Device Context Doorbell (#1 to #32)

#### (1) Doorbell 0



Bit	Bit Name	Initial Value	R/W	Description
31 to 16	DB Stream ID	H'0000	R	Fixed to H'0000
15 to 8	—	All 0	R	Reserved
7 to 0	DB Target	H'00	R/W	Doorbell Target. For Device Context. Command Ring Host Controller Doorbell (0) Value Definition H'00: Host Controller Command H'01 to H'F7: Reserved H'F8 to H'FF: Vendor Defined If the set value is other than 0, it is ignored. The read Value is 0. When the Host Controller Doorbell (0) is set, DB Stream ID field is set to 0.

(2) Doorbell 1-32



Bit	Bit Name	Initial Value	R/W	Description
31 to 16	DB Stream ID	H'0000	R/W	Indicates targeted Endpoint's Stream when Endpoint defines Stream. If Endpoint doesn't define Stream (Max PStream = 0), but this bit is not set to 0, then this setting is ignored. The read Value is 0.
15 to 8	—	All 0	R	Reserved
7 to 0	DB Target	H'00	R/W	Doorbell Target. For Device Context Device Context Doorbells (1 to 255) Value            Definition H'00:            Reserved H'01:            Control EP 0 Enqueue Pointer Update H'02:            EP 1 OUT Enqueue Pointer Update H'03:            EP 1 IN Enqueue Pointer Update H'04:            EP 2 OUT Enqueue Pointer Update H'05:            EP 2 IN Enqueue Pointer Update ...                ... H'1E:            EP 15 OUT Enqueue Pointer Update H'1F:            EP 15 IN Enqueue Pointer Update H'20 to H'F7: Reserved H'F8 to H'FF: Vendor Defined The read Value is 0.

## 54.4 Description of Functions

RZ/G1H	RZ/G1N
RZ/G1M	RZ/G1E

### 54.4.1 FW Download

The USB3.0 host controller requires to download FW via AXI to operate as a host.

FW Download is realized by writing FW image data to a specific area in the AXI Register space. Upon the completion of FW Download, there is no need to write or reload FW.

#### 54.4.1.1 Download Data Format

The following format is used for FW Download.

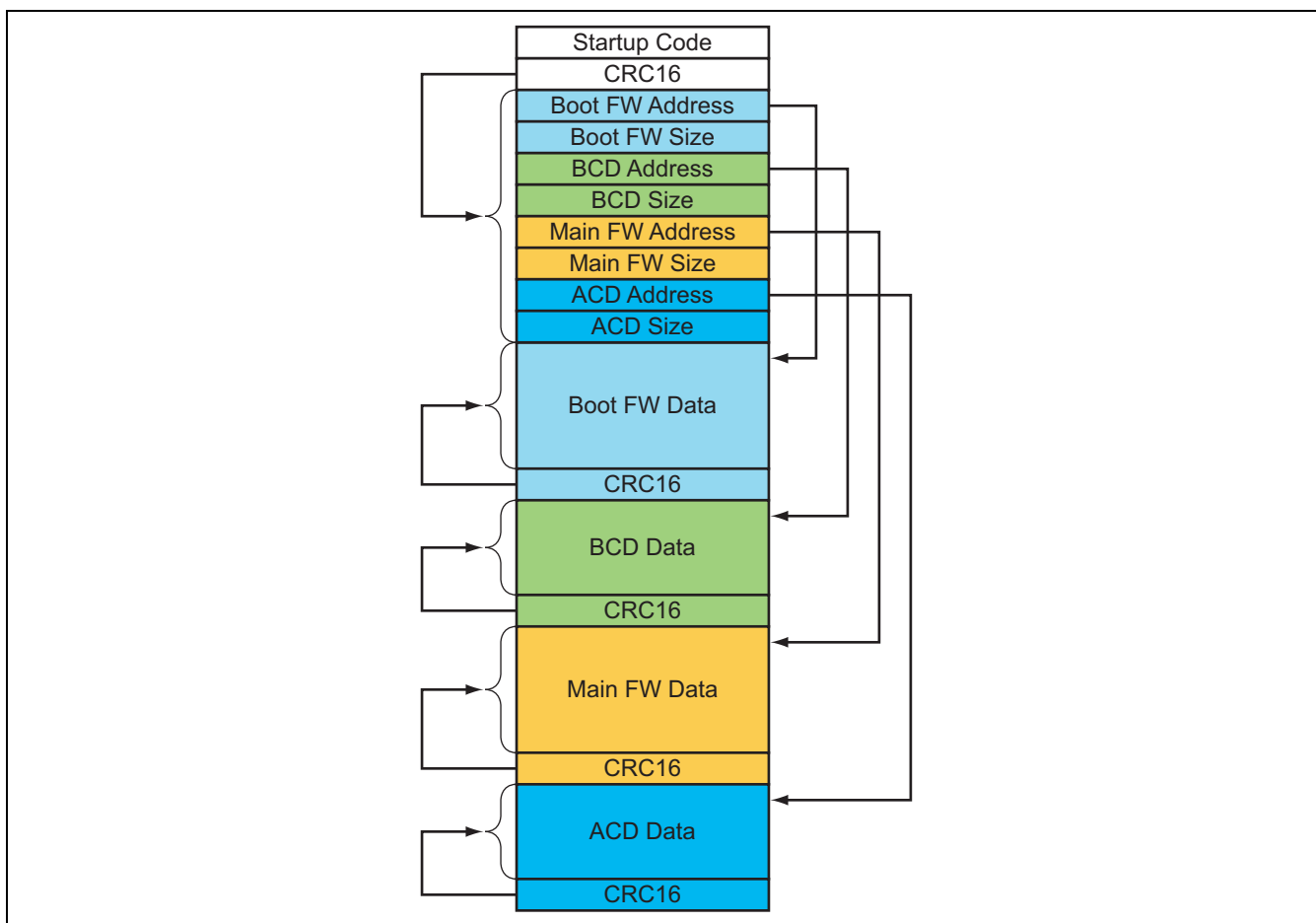


Figure 54.5 The Format of FW Download

Offset (Byte)	Size (Byte)	Field	Field Explanation
H'0000	2	Startup Code	Flag bit to show the storing of ROM Data. H'55AA is set.
H'0002	2	Header CRC16	CRC16 value from BCD Address to ACD size.
H'0004	2	Boot FW Address	Offset from the beginning of ROM Data in Boot FW Data field.
H'0006	2	Boot FW Size	Size of Boot FW field. (L)
H'0008	2	BCD Address	Offset from the beginning of Start Code in BCD Data field.
H'000A	2	BCD Size	Size of BCD Data field. (M)
H'000C	2	Main FW Address	Offset from the beginning of Startup Code in Main FW Data field. (N)
H'000E	2	Main FW Size	Size of Main FW field.
H'0010	2	ACD Address	Offset from the beginning of Startup Code in ACD Data field. (P)
H'0012	2	ACD Size	Size of ACD Data field.
H'0014	L	Boot FW Data	Bootstrap Code
(H'0014+L)	l	Boot FW CRC16	CRC16 of Boot FW Data field. If Boot FW Size field value is 0, it doesn't exist.
(H'0014+L+l)	pl	Padding	Padding to assign the beginning of BCD Data to 2-byte boundary.
(H'0014+L+l+pl)	M	BCD Data	BCD Data (Boot conf)
(H'0014+L+M+l+pl)	m	BCD CRC16	CRC16 of BCD Data field. If BCD Size field value is 0, it doesn't exist.
(H'0014+L+M+l+m+pl)	pm	Padding	Padding to assign the beginning of Main FW Data to 2-byte boundary.
(H'0014+L+M+l+m+pl+pm)	N	Main FW Data	Main FW
(H'0014+L+M+N+l+m+pl+pm)	n	Main FW CRC16	CRC16 of Main FW Data field. If Main FW Size field value is 0, it doesn't exist.
(H'0014+L+M+N+l+m+n+pl+pm)	pn	Padding	Padding to assign the beginning of ACD to 2-byte boundary.
(H'0014+L+M+N+l+m+n+pl+pm+pn)	P	ACD Data	ACD Data (Application conf)
(H'0014+L+M+N+P+l+m+n+pl+pm+pn)	p	ACD CRC16	CRC16 of ACD Data field. If ACD Size field value is 0, it doesn't exist.

Note: If "l", "m", "n", and "p" exist in each CRC16 field then the value is 2.  
If they do not exist, then the value is 0.

### 54.4.1.2 System Interface

The USB3.0 host controller delivers data through the AXI Register.

A register for delivering FW data has no specified data length, so data is always delivered at a 4-byte rate.

If delivered data cannot be allocated to a 4-byte boundary, Host calculates a length of necessary data and discards extra data.

Register	Bit	Field	Default	Attributes	Explanation										
AXICNF050	0	FW Download Enable	0	R/W	Flag bit to show that BIOS indicates execution of FW Download.  The System sets this bit to 1 when FW writing starts, and 0 when the last data is set to FW Data0/1.										
	1	FW Download Lock	0	RW1S	Flag for lock of FW Download.  When this bit is 1, FW Download is not done even when FW Download Enable is 1.										
	6 to 4	Result Code	0	RO	Execution result of BIOS Download.  <table border="1"> <thead> <tr> <th>Value</th> <th>Meaning</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Invalid</td> </tr> <tr> <td>1</td> <td>Success</td> </tr> <tr> <td>2</td> <td>Error</td> </tr> <tr> <td>others</td> <td>Reserved</td> </tr> </tbody> </table>	Value	Meaning	0	Invalid	1	Success	2	Error	others	Reserved
	Value	Meaning													
	0	Invalid													
1	Success														
2	Error														
others	Reserved														
8	Set Data0	0	RW1S	Showing that FW Data0 at AXICNF058 is enabled.											
9	Set Data1	0	RW1S	Showing that FW Data1 at AXICNF05C is enabled.											
AXICNF058	31 to 0	FW Data0	H'00000 0000	R/W	Write data.										
AXICNF05C	31 to 0	FW Data1	H'00000 0000	R/W	Write data.										

When starting FW Download, the System first sets AXICNF050.FW Download Enable to 1, and then starts delivering data to the Host.

After writing a value to AXICNF058 or AXICNF05C, and setting value 1 to the corresponding bit of AXICNF050.SetData0/1, the System shall put the data delivery on hold until the bit changes to 0.

FW Data0/1 can be used in either of the following ways.

- Use FW Data0 and FW Data1 alternately.
- Use only FW Data0

After writing the last data to FW Data, the System sets AXICNF050.FW Download Enable to 0 and notifies the Host that Data transfer completes.

After the System makes a notification and confirms that AXICNF050.Result Code is 1 (Success), the flow completes.

Then if Result Code is 2 (Error), it indicates that Host cannot be used due to some error in FW Download.

(Almost caution is illegally data load.)



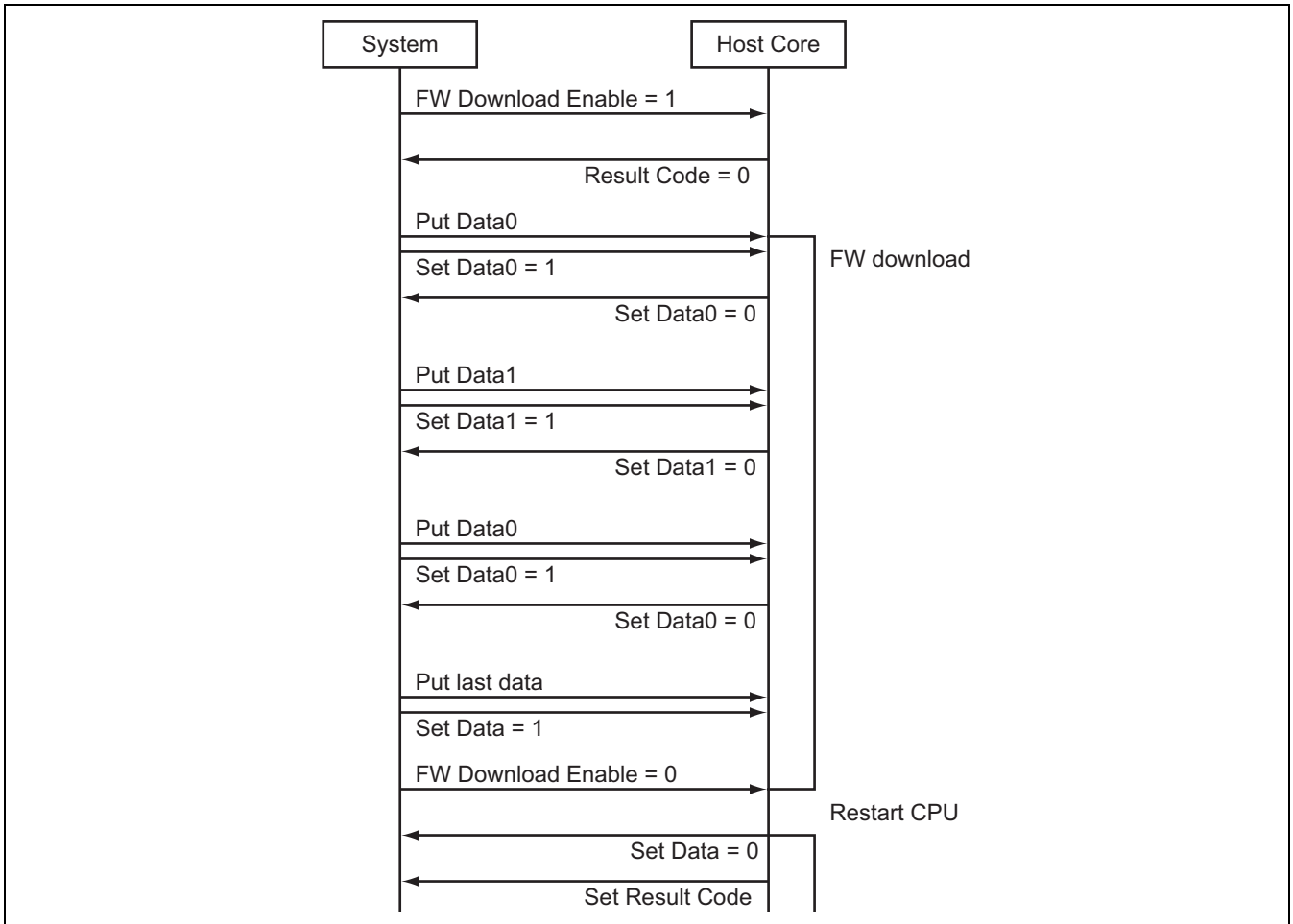


Figure 54.6 The Flow of FW Download

### 54.4.2 Battery Charging

The USB3.0 host controller supports the Battery Charging function of A-Device, which is on the supply side.

In the A-Device, the function is controlled by HW/FW of Host Core.

And it is required that CLk60 is working before starting Battery Charging flow.

Note: For details, refer to Battery Charging Specification Revision1.2.

#### 54.4.2.1 A-Device side (Charging Port Device)

The Battery Charging function is used to pull more current from VBUS than specified in USB specification.

Following Port Modes are supported in A-Device;

- Standard Downstream Port (SDP)
- Charging Downstream Port (CDP)
- Dedicated Charging Port (DCP)

##### (1) Setting BC\_MODE

At first for HW preparing, it shall be set Battery Charging Mode at BC\_MODE[3:0] at Battery Charging Register in AXI Register.

(Refer to section 54.2.3.2, AXI Register Overview, H'230 to H'233)

Battery Charging								
H'233	—	—	—	—	—	—	—	PTPWR_CTRL
H'232	—	—	—	—	—	—	Renesas Private field	
H'231	—	—	—	—	—	LCLK_NOSTOP_FREQ		
H'230	—	—	—	—	BC_MODE			

**Table 54.6 Setting Value for Battery Charging**

Setting Value	BC_MODE	Description
0	Always SDP Mode	Default value after resetting HW. A-Device operates in the “SDP” mode both normal function state and D3 state.
1	Always CDP Mode	A-Device operates in the “CDP” mode both normal function state and D3 state.
2	SDP-DCP Auto-change Mode	A-Device operates in the “SDP” mode in a normal function state and operates in the “DCP” mode in the D3 state.
3	CDP-DCP Auto-change Mode	A-Device operates in the “CDP” mode in a normal function state and operates in the “DCP” mode in the D3 state.

**Table 54.7 BC Mode and Port Type in D0 and D3 State**

<b>BC_MODE</b>	<b>Normal Operation (D0) Port Type</b>	<b>Suspended (D3) Port Type</b>
Always SDP Mode	SDP	SDP
Always CDP Mode	CDP	CDP
SDP-DCP Auto-change Mode	SDP	DCP <b>(Note1)</b>
CDP-DCP Auto-change Mode	CDP	DCP <b>(Note1)</b>

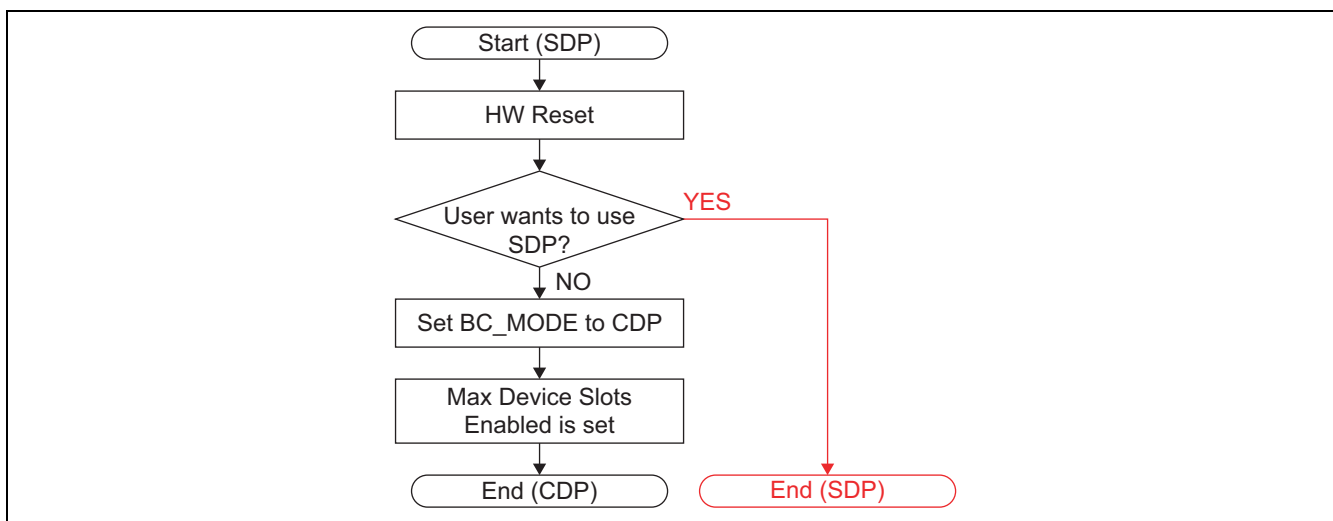
Notes: 1. If WakeOnConnect/WakeOnDisconnect is valid, it shall be kept Port type in Normal Operation A-Device has the following operation modes and can change these modes dynamically in the D0 state (Normal operation) and the D3 state (Suspended).  
 2. For the description of D0 and D3, refer to section 54.4.3.1, Power Management Capability).

**(2) Each case of changing BC\_MODE**

**Case-1)** After Host HW Reset, BC\_MODE is set “Always SDP Mode”.

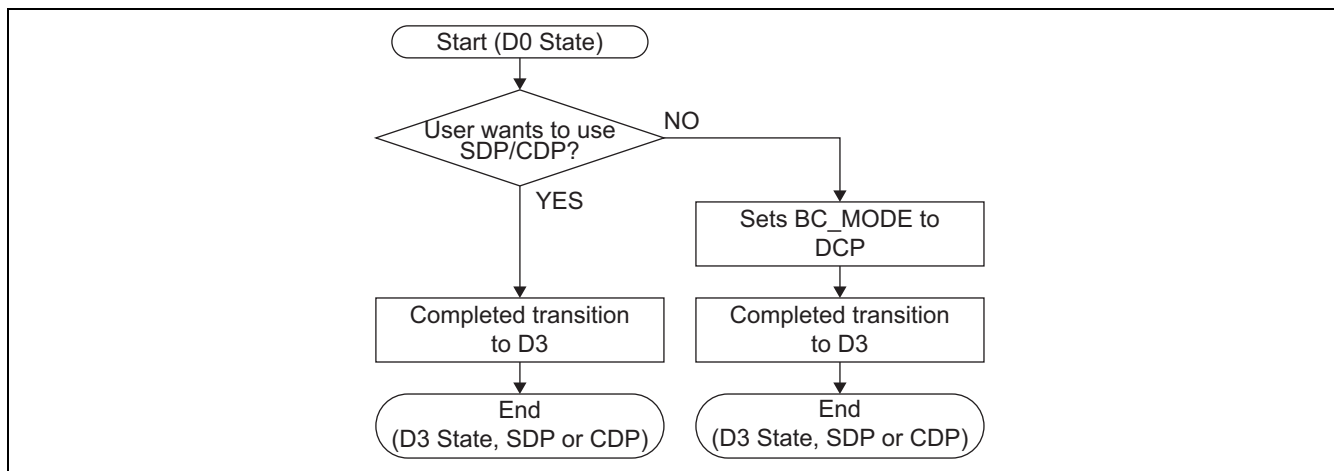
SDP is a default Mode.

Red-colored flow in Figure 54.7 is for default setting.



**Figure 54.7 Default Setting**

**Case-2)** If user wants to change Mode from SDP/CDP to DCP Mode during A-device working, BC\_MODE shall be changed when transition from D0 to D3.

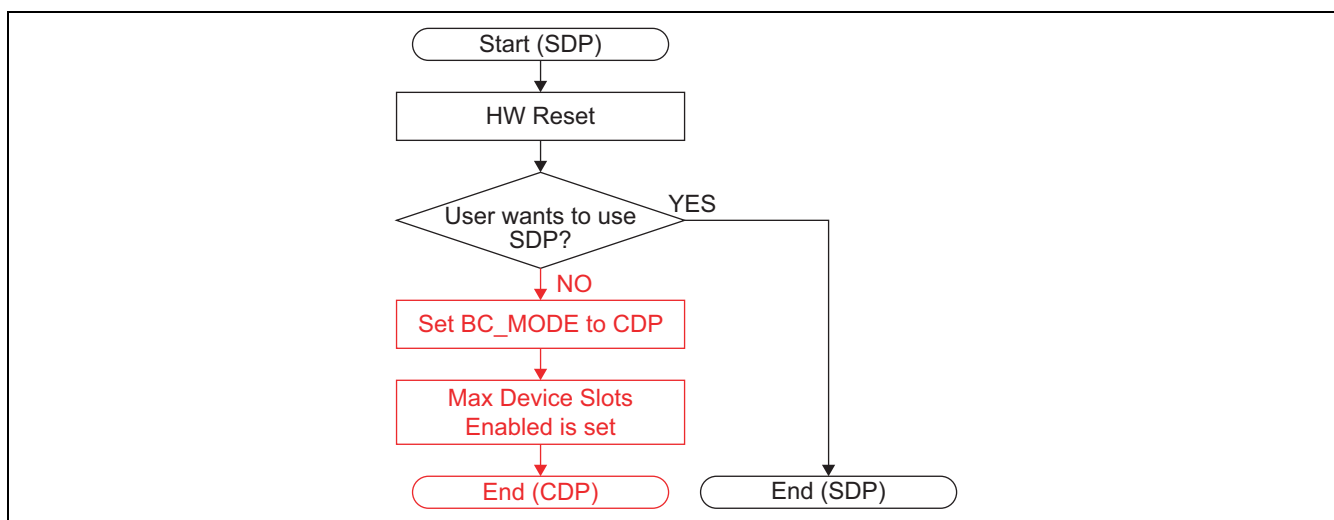


**Figure 54.8 Changing BC\_MODE during Transition between D0 and D3 States**

**Case-3)** When user wants to use A-Device with except default (SDP) Mode after Host HW Reset, BC\_MODE shall be changed before setting value of “Max Device Slots Enabled” in xHCI CONFIG register [H'058].

For the selectable modes, refer to Table 54.7.

Red-colored flow in Figure 54.9 is for BC\_MODE setting.



**Figure 54.9 Changing BC\_MODE**

**[Caution]**

- On the port in which WakeOnConnect/WakeOnDisconnect is enabled, a transition to DCP is not allowed because the port shall detect connect/disconnect of Device.
- When going D3 state with connecting USB device, current Mode shall be kept up setting because that any USB communication doesn't continue with setting DCP.

When changing Battery Charging type, it is required by Battery Charging Specification that VBUS shall be off more than 100-ms and prompting reconnection of device. Host FW operates this process.

### 54.4.3 Power Management

#### 54.4.3.1 Power Management Capability

USB3.0 host controller Host Core sets pseudo D3 state.

It is controlled by Extended Power Management Capability register.

- Extended Power Management Capability

This register controls pseudo PCIe Power State.

Bit 15: PME Status: Showing which there was a Wakeup event during pseudo D3 state

Bit 8: PME Enable: It asserts an interrupt from pseudo D3 state at Wakeup.

When this bit is set to 1, if PME Status is changed 1 then the interrupt occurs.

Bit [1:0]: Power State: Setting pseudo Power state.

The valid value is as follows.

0: D0 (Do not save power)

3: D3 (Do power save)

Note: In the after section, D3 means pseudo D3 state which is described here.

#### 54.4.3.2 Low Power Management of Receiver Detection

It is intended to saving power of Receiver Detection circuit at PHY Hard Macro (PHYHM).

There are two ways, setting initial value in define file and changing value at field of Register.

For changing value, the field shall be set before starting FW download when occurs after reset.

##### (1) D3

USB3.0 Common Block operates periodically Receiver Detection with LCLK during RxDetect state of LTSSM and P3 of PHY state.

However if a system is in Suspend and WakeOnConnect is disabled, there is no need to do Receiver Detection.

To reduce power consumption of PHY by above discarded Receiver Detection, FW can halt the process.

##### (2) D0

Receiver Detection at opened Port in D0 shall be operated.

HW operates reducing power at interval of Receiver Detection.

TimeMax is that decides operational interval of Detection in P3.

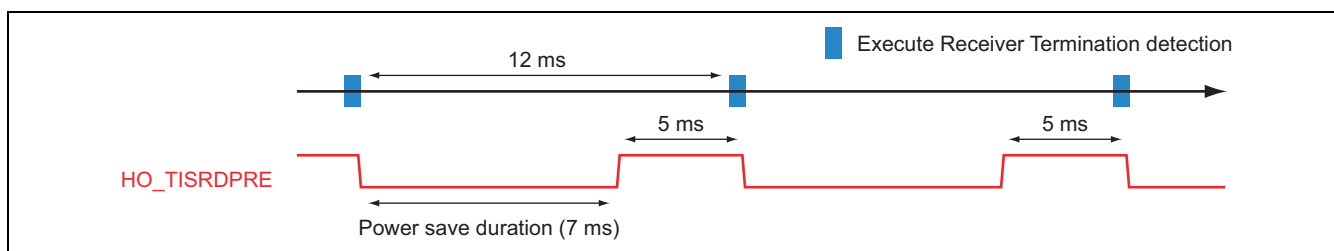


Figure 54.10 Low-Power of Receiver Detection

54.4.3.3 Power Control for Each State

The overview of power control state flow is shown as below.

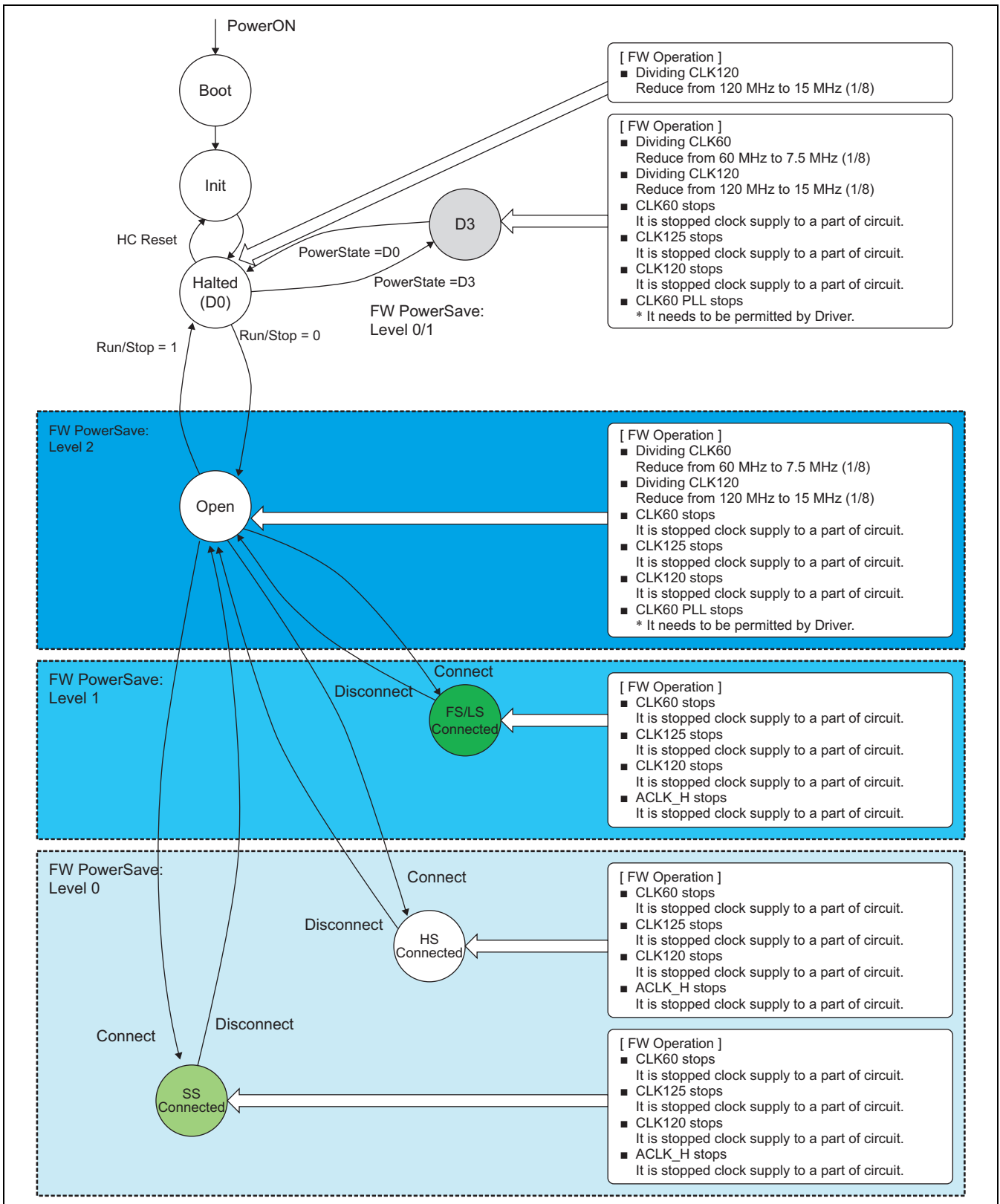


Figure 54.11 Overview of Power Control State Flow

#### 54.4.3.4 Clock Termination by USB3PHY and LTSSM State

USB3PHY may stop PLL which generates CLK125 by USB3PHY's power state.

**Table 54.8 LTSSM State and USB3PHY Condition**

LTSSM State	USB3PHY		Supplement
	POWERDOWN	PLL Operation	
SS.Disabled	P2	Run	
Rx.Detect	P2	Run	Default
	P0	Run	
	P3	Stop	
U0	P0	Run	
U1	P1	Run	
U2	P2	Run	
U3	P0	Run	
	P3	Stop	
U3 → U3_Wakeup, Reset	P0	Run	Transition by receiving LFPS
U3 → RemoteWakeup	P0	Run	Transition is required by PLS (Need Register operation)
Other	P0	Run	

#### 54.4.3.5 Flow of System Suspend and Resume

When following all permission for suspend are met, system goes to suspend.

- Host system sets AXH\_CON.SYS\_SUSPEND to 1 and completes host core's preparations for suspend.

When host core resumes from System Suspend, user shall confirm the bit of B2\_PLL\_ACTIVE at AXH\_STA register [H'104 to H'107] in AXI register is set to 1 before accessing register.

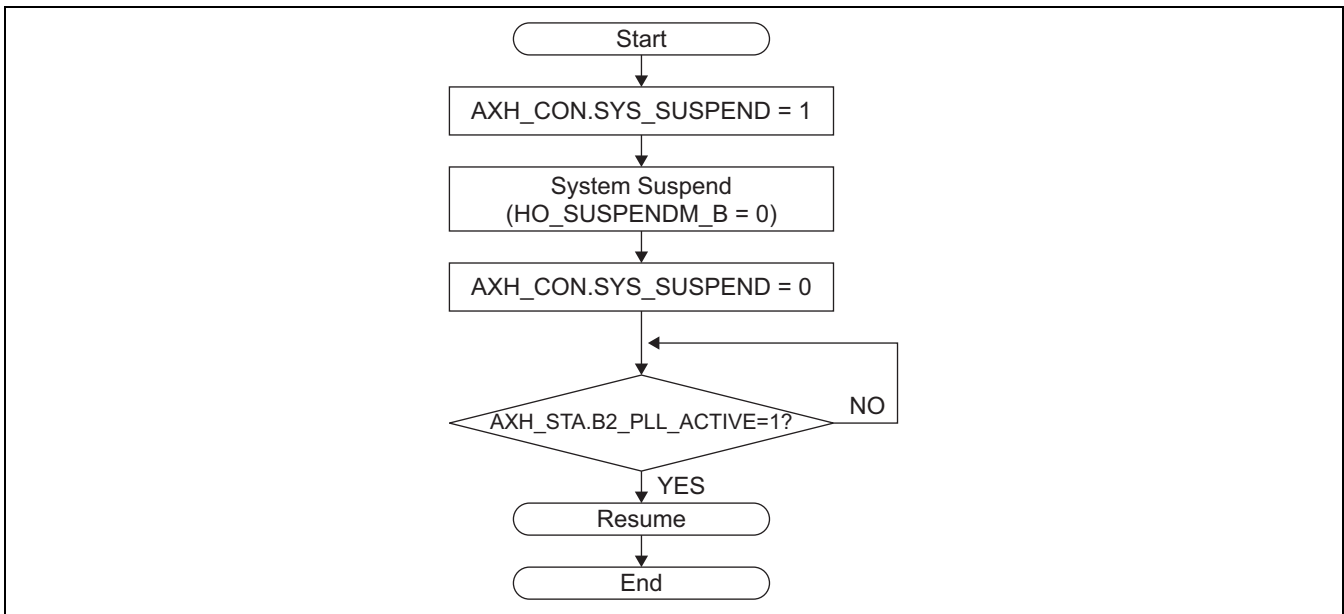


Figure 54.12 System Suspend and Resume Flow



### 54.4.4 Power Control

The process of VBUS ON/OFF and Over Current detection are described below.

#### 54.4.4.1 VBUS On

When VBUS will be on, at first host driver shall execute processes as below.

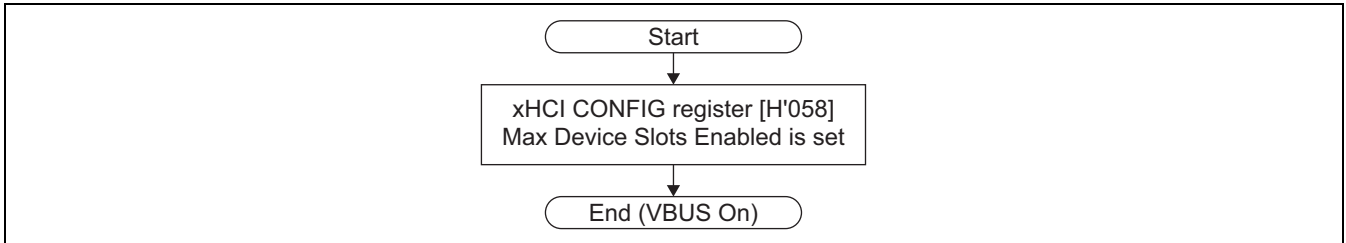


Figure 54.13 Flow of VBUS On

#### 54.4.4.2 VBUS Off

When port power will be off, at first host driver shall execute processes as below.

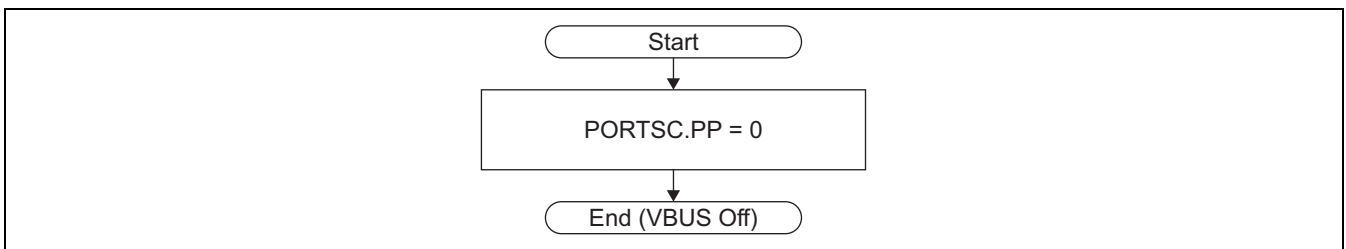
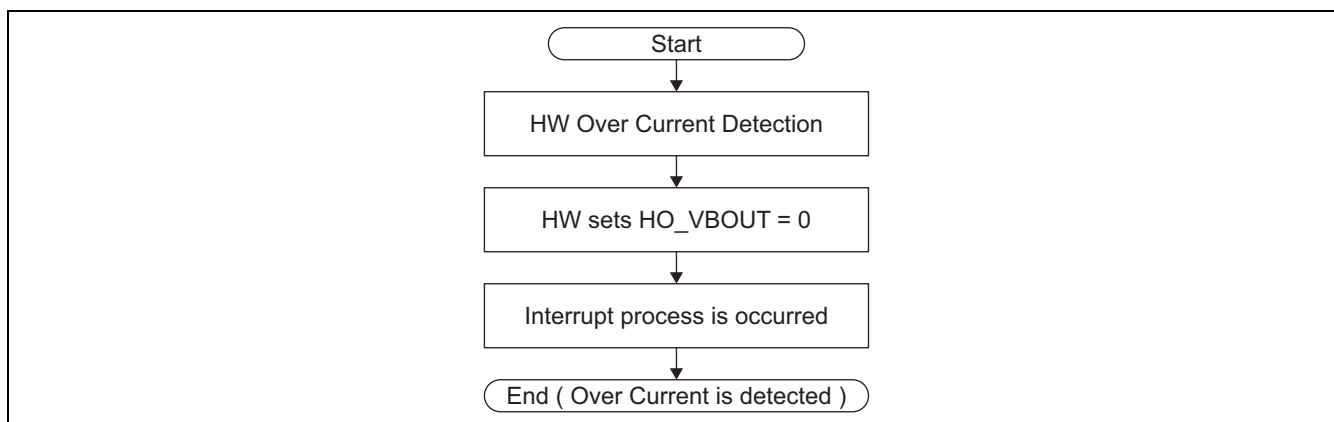


Figure 54.14 Flow of VBUS Off

#### 54.4.4.3 Over Current Detection

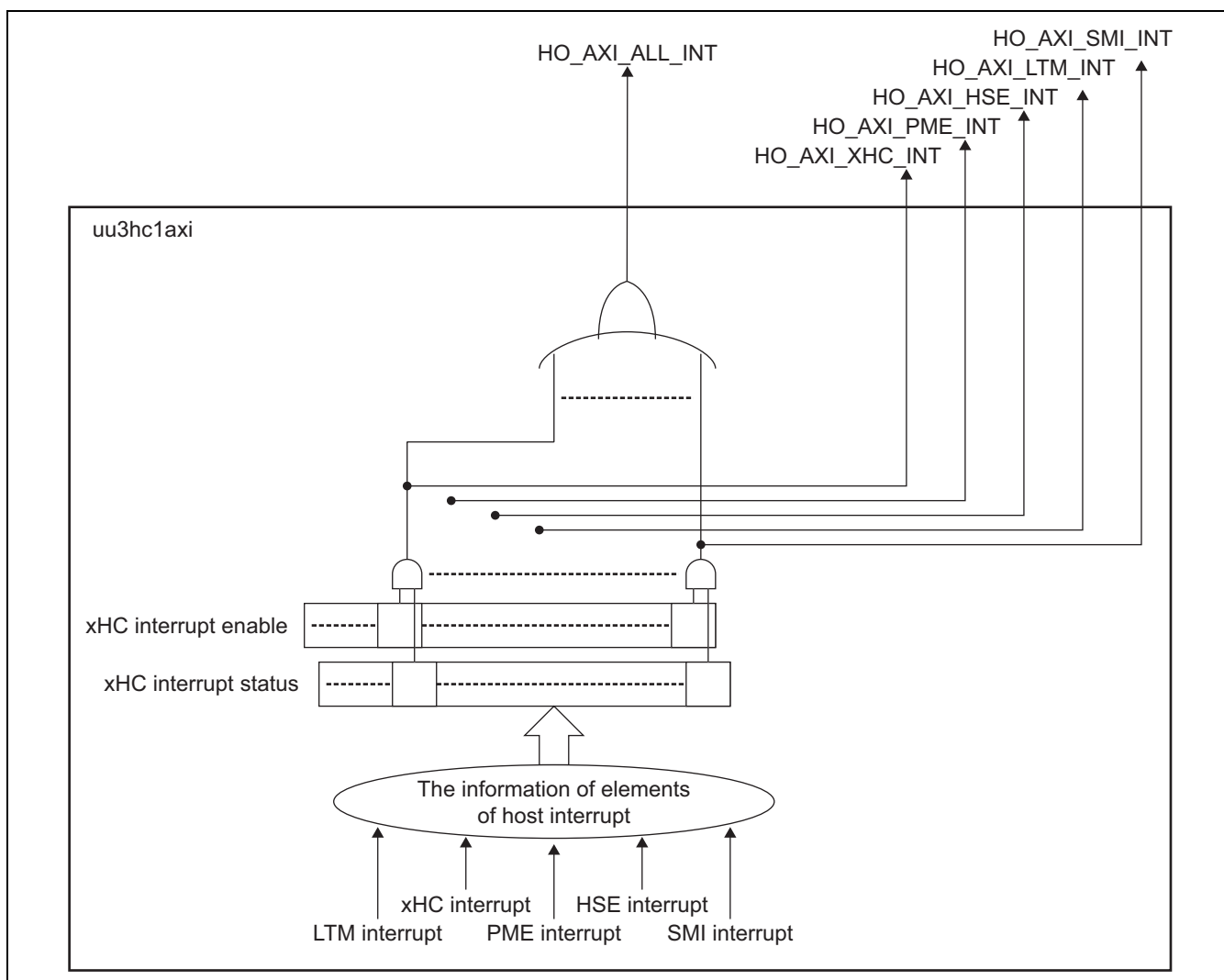
When port will detect over current during the core working, following flow is executed on host.



**Figure 54.15 Flow of Over Current Detection**

### 54.4.5 Structure of Notification for Elements of Interrupt

In USB3.0 host controller, the elements of interrupt are noticed by following layered structure.



**Figure 54.16 Interrupt Layered Structure**

- This Host core doesn't use WAKEB but PME. Interrupt pin by PME is HO\_AXI\_INT\_PME.

Note: About occurrence factor of PME interrupt, refer to xHCI Specification.

- Interrupt occurrence factor of xHCI shall be switched its meaning as PCIINT.
- The abstract of Interrupt signals from Figure 54.16 are below.

**Table 54.9 Function of Interrupt Signals**

Signal Name	Function
HO_AXI_INT_XHC	xHCI Interrupt
HO_AXI_INT_PME	PME Interrupt
HO_AXI_INT_HSE	HSE Interrupt
HO_AXI_INT_LTM	LTM Interrupt
HO_AXI_INT_SMI	SMI Interrupt
HO_AXI_INT_ALL	All Interrupt Signals from Host Core are logical ORed.

#### 54.4.6 Implementation Constraint of Host Core

The USB3.0 host controller core has implementation constraint.

- 1 Packet shall be composed of 8TRB or less.

RZ/G1H	RZ/G1N
RZ/G1M	RZ/G1E

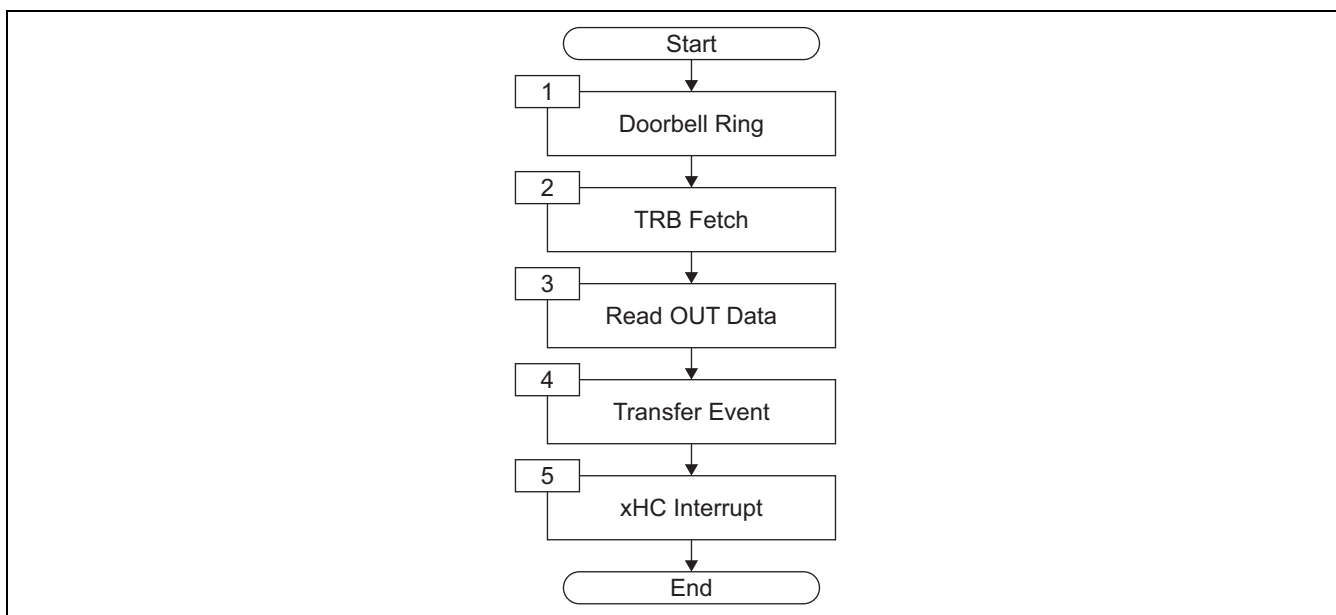
## 54.5 Example of Transaction

This section describes transaction when using Host core. As examples, Bulk OUT and Bulk IN transactions are described. The USB3.0 host controller core complies with xHCI Specification.

Refer to xHCI Specification for details.

### 54.5.1 Bulk OUT Transaction

Bulk OUT transaction flow is shown as below.

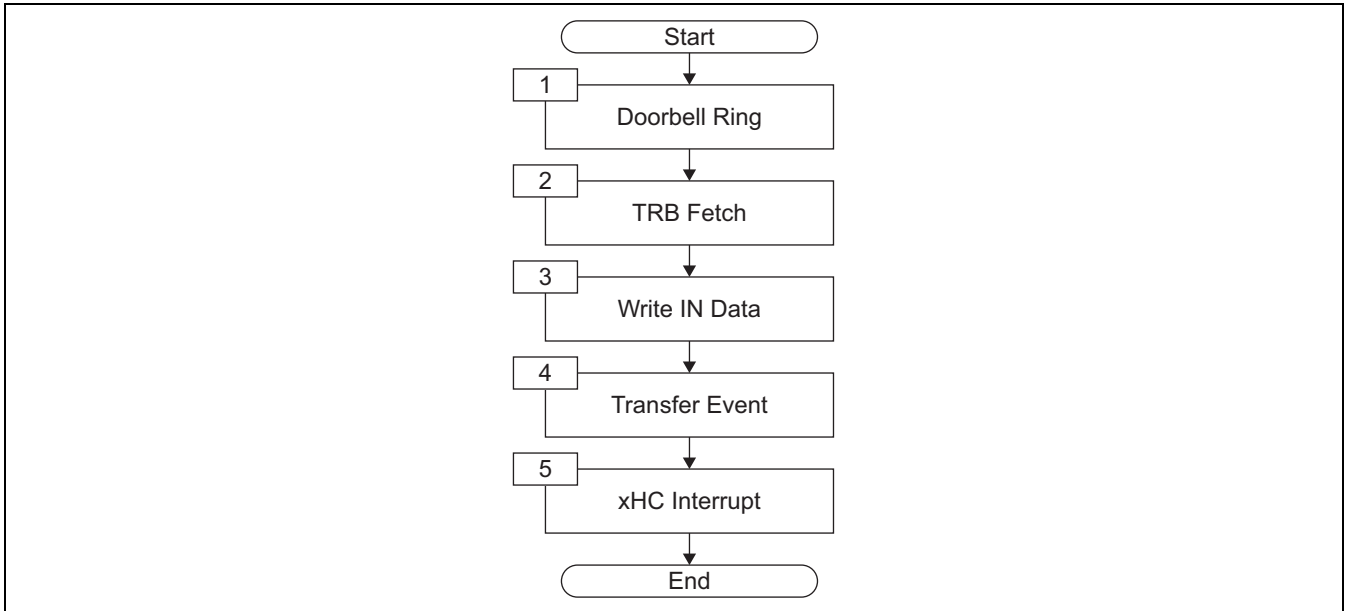


**Figure 54.17 Example of Bulk OUT Transaction Flow**

- 1) Doorbell Ring  
System rings Doorbell to prepare Transfer Data.
- 2) TRB Fetch  
Host core fetches TRB from OUT Transfer Ring,
- 3) Read OUT Data  
Host reads OUT Data from Data Buffer Pointer.
- 4) Transfer Event  
Host writes Transfer Event TRB to Event Ring.
- 5) xHC Interrupt  
Host sends Interrupt to System.

### 54.5.2 Bulk IN Transaction

Bulk IN transaction flow is shown as below.



**Figure 54.18 Example of Bulk IN Transaction Flow**

- 1) Doorbell Ring  
System rings Doorbell to prepare Transfer Data.
- 2) TRB Fetch  
Host core fetches TRB from OUT Transfer Ring,
- 3) Write IN Data  
Host writes IN Data to Data Buffer Pointer.
- 4) Transfer Event  
Host writes Transfer Event TRB to Event Ring.
- 5) xHC Interrupt  
Host sends Interrupt to System.

## 54.6 Power IC Interface Connection

RZ/G1H	RZ/G1N
RZ/G1M	RZ/G1E

The USB3.0 host controller core has power signal detection.

- Power IC has Outputting Over Current Flag signal and the USB3.0 host controller can detect the signal.
- Battery Charging function is able to use at the USB3.0 host controller.

### 54.6.1 Usable Power IC type

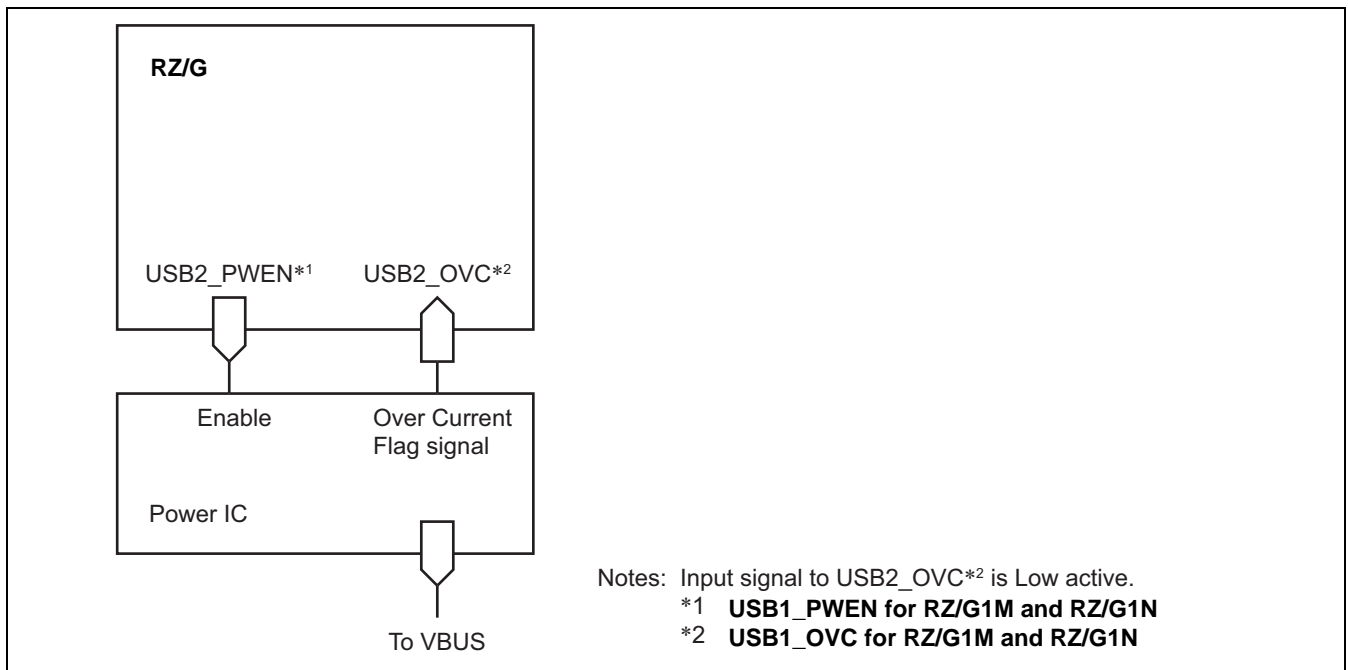


Figure 54.19 Usable Power IC Type

Table 54.10 Setting Registers and Signals for Power IC

Signal	
USB2_OVC*2	USB2_PWEN*1
Connecting to Over Current Flag signal	Connecting to Enable

Notes: 1. USB1\_PWEN for RZ/G1M and RZ/G1N.  
 2. USB1\_OVC for RZ/G1M and RZ/G1N.

• **Restriction**

Do not use another type of Power IC.

# 55. RCLK Watchdog Timer

RZ/G1H	RZ/G1N
RZ/G1M	RZ/G1E

This LSI includes the RCLK watchdog timer (RWDT).

This LSI can be reset by the overflow of the counter when the value of the counter has not been updated because of a system runaway.

The RWDT is a single-channel timer that uses the RCLK as an input and can be used as a watchdog timer.

In RZ/G1H, M, N and E, RCLK is a clock, which is generated by the clock pulse generator (CPG).

## 55.1 Features

- One channel is provided.
- Can be used as a watchdog timer. Reset is generated when the counter overflows.
- A counter input clock can be chosen from:  
Clocks (RCLK/1 to RCLK/(128 × 60 × 30)) that are obtained by dividing the RCLK.

Figure 55.1 shows block diagrams of the RWDT.

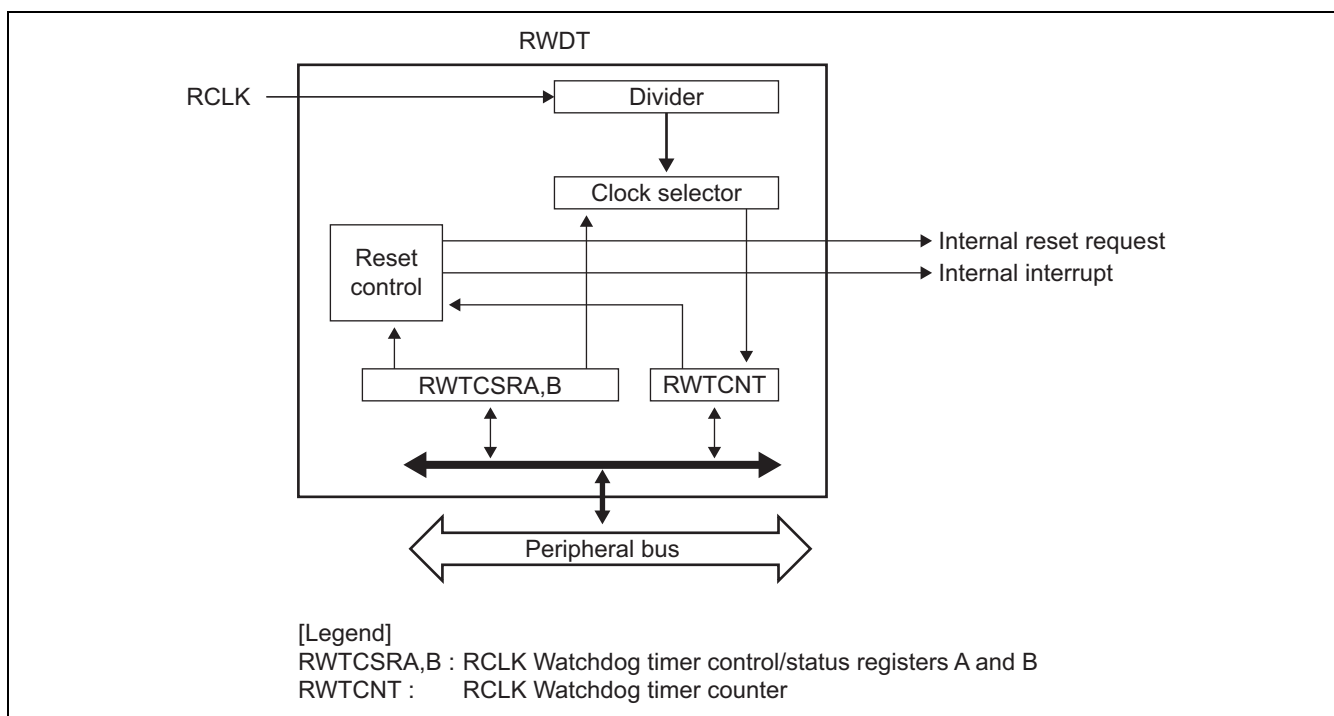


Figure 55.1 Block Diagram of RWDT



## 55.2 Register Descriptions for RWDT

Table 55.2 shows the RWDT register configuration. Table 55.3 shows the register state in each processing mode.

**Table 55.2 Register Configuration of RWDT**

Name	Abbreviation	R/W	Address	Access Size	RZ/G Series Products			
					RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
RCLK watchdog timer counter	RWTCNT	R/W	H'E602 0000	16/32*	√	√	√	√
RCLK watchdog timer control/status register A	RWTCSRA	R/W	H'E602 0004	8/32*	√	√	√	√
RCLK watchdog timer control/status register B	RWTCSR B	R/W	H'E602 0008	8/32*	√	√	√	√

Note: \* Write is performed in 32 bits and read in 16 or 8 bits.

**Table 55.3 Register State of RWDT in Each Processing Mode**

Register Abbreviation	Reset Caused by Other than Overflow	Reset Caused by Overflow*
<b>Register</b>	<b>Bit</b>	
RWTCNT	All	Initialized
RWTCSRA	WOVF	Retained
	Other than WOVF	Initialized
RWTCSR B	All	Initialized

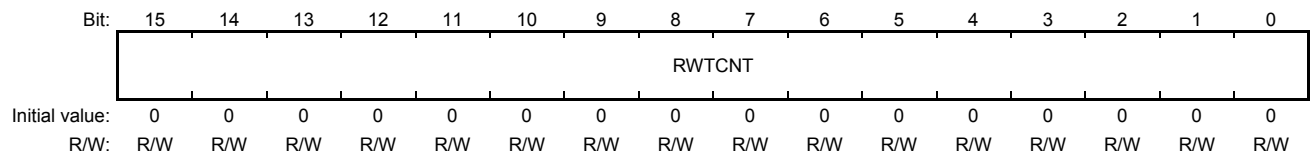
Note: \* RWDT overflow reset.

### 55.2.1 RCLK Watchdog Timer Counter (RWTCNT)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

RWTCNT is a 16-bit readable/writable register that increments on the selected clock. When an overflow occurs, it generates a Reset. The RWTCNT counter is initialized to H'0000 by a power-on reset and RWDT software reset.

Use a long word access to write to the RWTCNT counter, with H'5A5A in the upper byte. Use a word access to read RWTCNT.



### 55.2.2 RCLK Watchdog Timer Control/Status Register A (RWTCRA)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

RWTCRA is an 8-bit readable/writable register composed of bits to select the clock used for the count, overflow flag, and enable bit.

Use a long word access to write to RWTCRA, with H'A5A5A5 in the upper byte. Use a byte access to read RWTCRA.

Bit:	7	6	5	4	3	2	1	0
	TME	—	WRFLG	WOVF	WOVFE	CKS0[2:0]		
Initial value:	0	0	0	0	1	1	1	1
R/W:	R/W	R	R	R/(W)	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7	TME	0	R/W	Starts and stops timer operation. 0: Timer disabled: Count-up stops and RWTCNT value is retained 1: Timer enabled
6	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
5	WRFLG	0	R	Write Status Flag When this bit is 1, write access to RWTCNT is prohibited. If it isn't maintained, operation isn't secured. This bit indicates the period that the writing to RWTCNT is masked for synchronization after the writing to RWTCNT. Confirm that this flag is 0 when RWTCNT is written to continuously.
4	WOVF	0	R/(W)	Indicates that the RWTCNT has overflowed. This bit isn't initialized by a generated reset by an overflow of RWDT. Write 0 to this bit before using the RWDT. 0: No overflow 1: RWTCNT has overflowed Note: Only 0 can be written to clear the flag.
3	WOVFE	1	R/W	Overflow Interrupt Disable/Enable 0: Disables interrupts due to overflow 1: Enables interrupts due to overflow

Bit	Bit Name	Initial Value	R/W	Description
2 to 0	CKS0[2:0]	111	R/W	<p>RTC Clock Select</p> <p>These bits select the clock to be used for the RWTCNT count from the eight types obtainable by dividing the RCLK. The overflow period that is shown inside the parenthesis in the table is the value when the RCLK is 31.7 kHz*.</p> <p>Note. * 1560 MHz/(1024 × 48) = 31.73828125 kHz</p> <p>000: R<math>\phi</math> (2.1 s (RWTCNT: H'FF00 = 8.06 ms))</p> <p>001: R<math>\phi</math>/4 (8.2 s (RWTCNT: H'FF00 = 32.2 ms))</p> <p>010: R<math>\phi</math>/16 (33.0 s (RWTCNT: H'FF00 = 129.0 ms))</p> <p>011: R<math>\phi</math>/32 (66.0 s (RWTCNT: H'FF00 = 258.0 ms))</p> <p>100: R<math>\phi</math>/64 (132.0 s (RWTCNT: H'FF00 = 516.0 ms))</p> <p>101: R<math>\phi</math>/128 (264.0 s (RWTCNT: H'FF00 = 1.03 s))</p> <p>110: R<math>\phi</math>/1024 (2112.0 s (RWTCNT: H'FF00 = 8.25 s))</p> <p>111: RCLK select expanded mode</p> <p>The clock cycle varies depending on the CKS1 bit in RWTCSR B. Its initial value is R<math>\phi</math>/4096 (8438.0 s (RWTCNT: H'FF00 = 33.0 s)).</p>

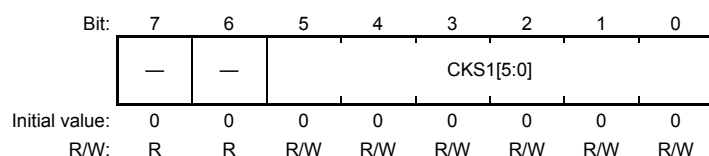
Note: These overflow periods are calculated from the rounded value of R $\phi$ =31.7 kHz.

### 55.2.3 RCLK Watchdog Timer Control/Status Register B (RWTCSR B)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

RWTCSR B is an 8-bit readable/writable register composed of bits to select the clock used for the count.

Use a word access to write to RWTCSR B, with H'A5A5A5 in the upper byte. Use a byte access to read RWTCSR B.



Bit	Bit Name	Initial Value	R/W	Description
7, 6	—	0	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>

Bit	Bit Name	Initial Value	R/W	Description
5 to 0	CKS1[5:0]	All 0	R/W	RCLK Select for RCLK Select Expanded Mode Selects the clock used for the RWTCNT count when the CKS0 bit in RWTCSCRA is B'111. The following table shows the time values used to cause an overflow from the counter H'0000(Overflow time from counter H'FF00). Assuming that $R\phi/128 = 264 \text{ s}$ (1.01 s), the overflow cycle in the table is calculated for the case when the RCLK is 31.7 kHz.

CKS1[3:0]	CKS1[5:4]			
	B'00	B'01	B'10	B'11
H'0	8438 s (33 s)	—	—	—
H'1	264 s (1.01 s)	1320 s (5.05 s)	264 min (1.01 min)	— (5.05 min)
H'2	528 s (2.02 s)	2640 s (10.1 s)	528 min (2.02 min)	— (10.1 min)
H'3	1055 s (3.03 s)	5280 s (15.2 s)	1056 min (3.03 min)	— (15.2 min)
H'4	4219 s (4.04 s)	— (20.2 s)	— (4.04 min)	— (20.2 min)
H'5	— (5.05 s)	— (25.3 s)	— (5.05 min)	— (25.3 min)
H'6	— (6.06 s)	— (30.3 s)	— (6.06 min)	— (30.3 min)
H'7	— (7.07 s)	— (35.4 s)	— (7.07 min)	— (—)
H'8	— (8.08 s)	— (40.4 s)	— (8.08 min)	— (—)
H'9	— (9.09 s)	— (45.5 s)	— (9.09 min)	— (—)
H'A	— (10.1 s)	— (50.5 s)	— (10.1 min)	— (—)
H'B	— (—)	— (55.6 s)	— (—)	— (—)
H'C	— (—)	— (60.6 s)	— (—)	— (—)
from H'D	— (—)	— (—)	— (—)	— (—)

Note: - (-): Reserved, - (xxx): Not recommendable  
These overflow periods are calculated from the rounded value of  $R\phi = 31.7 \text{ kHz}$ .

**55.2.4 Notes on Register Access**

RWTCSRA: Bits TME, CKS0

RWTCSRБ: Bits CKS1

After writing a value in this register, it is possible to read that value immediately, but it is not reflected in operation. 2 cycles of RCLK need to be inputted until the set-up value is reflected.

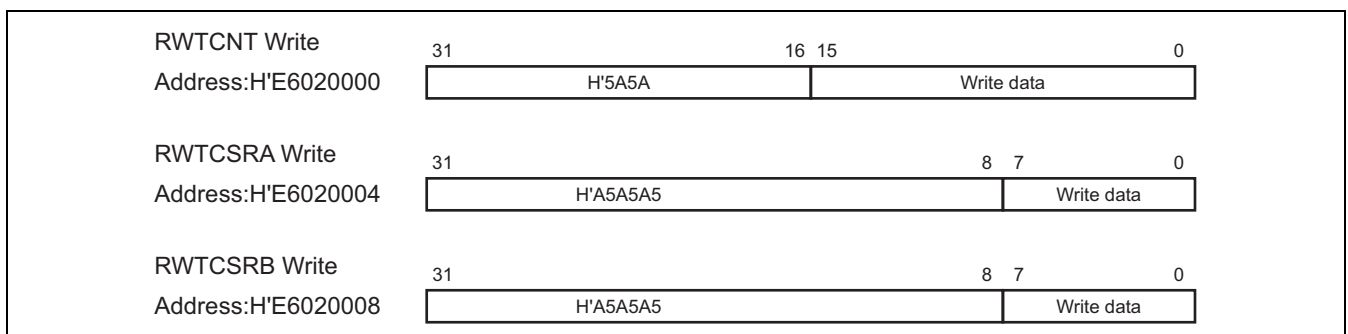
RWTCNT: Bits 15 to 0

After writing a value in this register, it is possible to read that value immediately, but it is not reflected in operation. 2 cycles of RCLK need to be inputted until the set-up value is reflected. Writing to this register, once started, is protected from further write operations until the writing operation has been completed. Read RWTCSRA. If WRFLG is 0, the next value can be written in RWTCNT.

The writing procedure to RWTCNT, RWTCSRA, and RWTCSRБ differs from that of other registers with the purpose of preventing an unintended write. The procedure for writing to these registers is given below.

**Writing to RWTCNT, RWTCSRA, and RWTCSRБ:**

- These registers must be written by a long word transfer instruction. They cannot be written by a byte or word transfer instruction.
- When writing to RWTCNT, set the upper byte to H'5A5A and transfer the lower byte as the write data. When writing to RWTCSRA and RWTCSRБ, set the upper byte to H'A5A5A5 and transfer the lower byte as the write data.



**Figure 55.2 Writing to RWTCNT, RWTCSRA, and RWTCSRБ**

## 55.3 RWDT Usage

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

### 55.3.1 Control of System Runaway

After a reset, RWDT is disabled. When the counter overflow occurs after the counter starts, an internal reset is again generated. By this function, a reset can be automatically generated even when this LSI has caused a system runaway. While this LSI is operating correctly, write H'0000 (or the set value) to RWTCNT periodically so that RWTCNT does not overflow.

Take the following steps to use the RWDT.

1. Clear the TME bit in RWTCSSRA to 0 to temporarily stop counting.  
(Confirm that RCLK was input more than 2 cycles.)
2. Write H'0000 or the set value in RWTCNT.
3. Clear the WOVF bit in RWTCSSRA to 0.
4. Set the kind of count clock to the CKS0[2:0] bits in RWTCSSRA, and CKS1[5:0] bits in RWTCSSRB.
5. Confirm that RWTCSSRA.WRFLG becomes 0.  
If WRFLG is 1, wait until it'll be 0.
6. Start the counting by setting the TME bit in RWTCSSRA to 1.  
(TME and CKS0 can't be set at the same time. When setting that at the same time, behavior isn't guaranteed.)
7. While this LSI is operating correctly, write H'0000 (or the set value) to RWTCNT periodically so that RWTCNT does not overflow.
8. When RWTCNT overflows, Reset is generated because the RWDT sets the WOVF flag in RWTCSSRA to 1. At this time, RWTCNT, RWTCSSRA (excluding the WOVF bit), and RWTCSSRB are initialized.

Execute a power-on reset or a software reset at that time and initialize RWDT.

When not initializing and using RWDT, behavior isn't guaranteed.

### 55.3.2 Module Stop

A setup of a stop of the Clock by a Module Stop signal is possible when RWDT is an Idle state. The Idle state of RWDT is when the condition of following all was satisfied.

- When RWTCSSRA.TME bit is 0
- When RWTCSSRA.WRFLG is 0
- When 3 or more cycles have passed in RCLK since the last Register access

### 55.3.3 Debugging Operation

When debugging the CPU core, stop counting up RWTCNT and retain the value of RWTCNT.

## 56. 16-Bit Timer Pulse Unit (TPU)

RZ/G1H	RZ/G1N
RZ/G1M	RZ/G1E

This LSI has a 16-bit timer pulse unit (TPU), which consists of four 16-bit timers.

### 56.1 Features

The TPU0 has the following features.

- Four timers are incorporated.
- Four pulse outputs are possible.
- Each timer of the TPU0 has four general registers (TGRA, TGRB, TGRC, and TGRD) for each timer. TGRA enables an output compare setting. TGRB, TGRC and TGRD in each timer can be used as timer-counter clearing registers. TGRC and TGRD can also be used as buffer registers.
- The following operations can be set for each timer.
  - Waveform output on compare match: output of a 0 or 1 or toggling of output is selectable.
  - Counter clearing operation: Counters can be cleared in response to a compare match.
  - PWM mode allows the output of a PWM waveform with any duty cycle.
  - The four outputs can be used to produce PWM output in up to four phases.
- A stepping motor control mode is available for timer 0.
- Buffer operation can be set for each timer.
- Automatic rewriting of values in output compare registers is possible.
- One interrupt request from TPU0
  - Enabling or disabling of compare match and counter overflows as interrupt sources can be set independently for each timer.
  - In stepping motor control mode, enabling or disabling of state transitions, requests for data, and overflows of data as interrupt sources is possible for timer 0.

Table 56.1 shows the TPU0 functions.

**Table 56.1 TPU0 Functions**

Item		Timer 0	Timer 1	Timer 2	Timer 3
Counter clock		CP $\phi$ /1	CP $\phi$ /1	CP $\phi$ /1	CP $\phi$ /1
		CP $\phi$ /4	CP $\phi$ /4	CP $\phi$ /4	CP $\phi$ /4
		CP $\phi$ /16	CP $\phi$ /16	CP $\phi$ /16	CP $\phi$ /16
		CP $\phi$ /64	CP $\phi$ /64	CP $\phi$ /64	CP $\phi$ /64
General registers		TPU0_TGRA0 TPU0_TGRB0	TPU0_TGRA1 TPU0_TGRB1	TPU0_TGRA2 TPU0_TGRB2	TPU0_TGRA3 TPU0_TGRB3
General and registers/ Buffer register		TPU0_TGRC0 TPU0_TGRD0	TPU0_TGRC1 TPU0_TGRD1	TPU0_TGRC2 TPU0_TGRD2	TPU0_TGRC3 TPU0_TGRD3
Output pins	Normal operation	TPU0TO0	TPU0TO1	TPU0TO2	TPU0TO3
	Stepping motor control mode	TPU0TO0 to TPU0TO3	None	None	None
Counter clearing		Compare match with TPU0_TGR	Compare match with TPU0_TGR	Compare match with TPU0_TGR	Compare match with TPU0_TGR
Output in response to compare match	0	√	√	√	√
	1	√	√	√	√
	Toggling	√	√	√	√
PWM mode		√	√	√	√
Buffer operation		√	√	√	√
Interrupt		5 sources Compare match/ overflow  6 more sources added in stepping motor control mode/ Transition to acceleration state /transition to normal state /transition to deceleration state /transition to stop state /data request /data overflow			



56.1.1 Block Diagram

Figure 56.1 is a block diagram of the TPU.

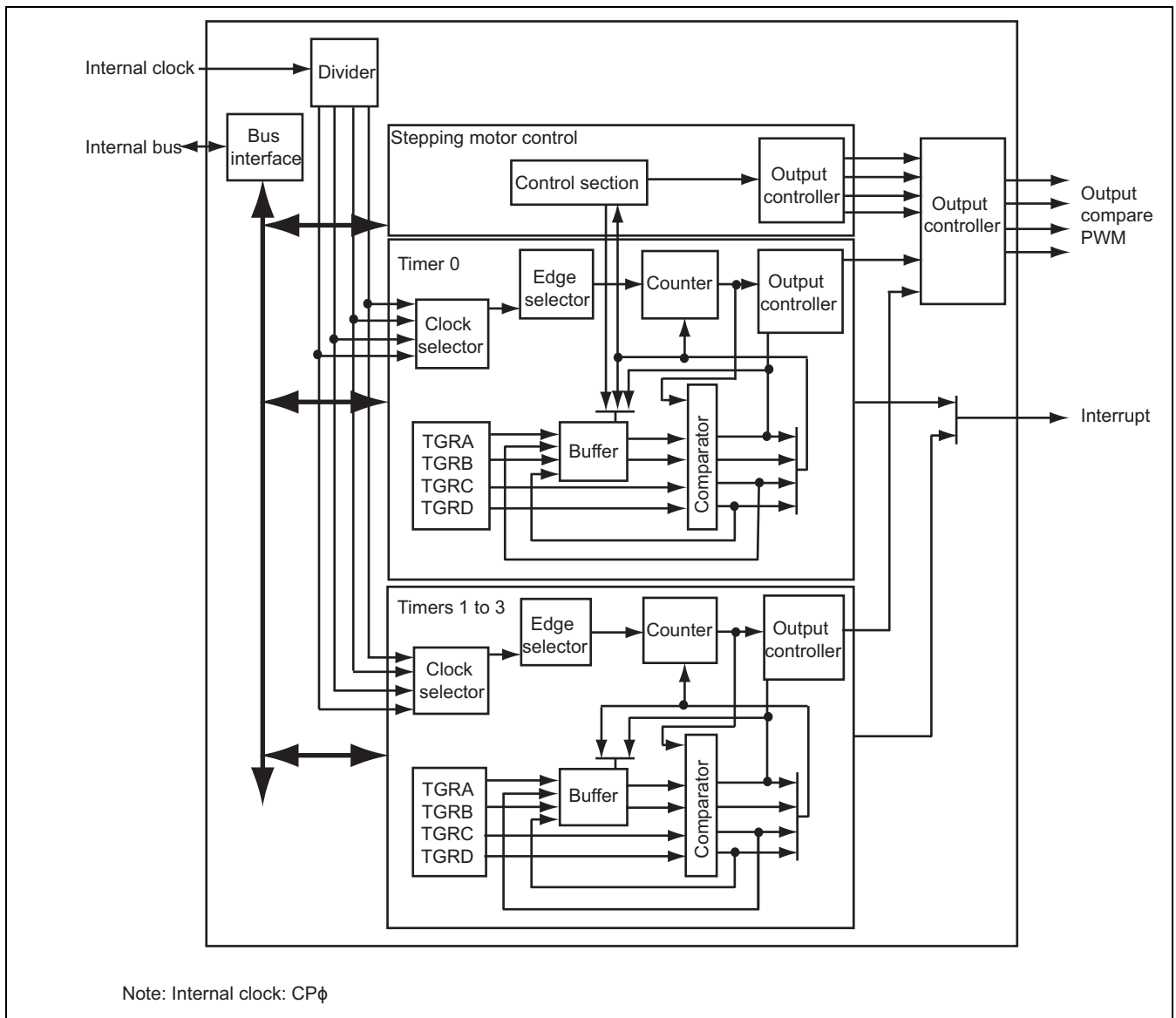


Figure 56.1 Block Diagram of the TPU

### 56.1.2 Input/Output Pins

Table 56.2 shows the pin configuration of the TPU0.

**Table 56.2 Pin Configuration**

Module	Timer	Pin Name	Function	I/O	Description	RZ/G Series Products			
						RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
TPU0	0	TPU0TO0	TPU0 output compare match 0	Output	TPU0_TGRA0 output compare output/ PWM output pin/pattern output pin 0 in stepping motor control mode	√	√	√	√
	1	TPU0TO1	TPU0 output compare match 1	Output	TPU0_TGRA1 output compare output/ PWM output pin/pattern output pin 1 in stepping motor control mode	√	√	√	√
	2	TPU0TO2	TPU0 output compare match 2	Output	TPU0_TGRA2 output compare output/ PWM output pin/pattern output pin 2 in stepping motor control mode	√	√	√	√
	3	TPU0TO3	TPU0 output compare match 3	Output	TPU0_TGRA3 output compare output/ PWM output pin/pattern output pin 3 in stepping motor control mode	√	√	√	√

## 56.2 Register Descriptions

Table 56.3 shows the TPU0 register configuration. Table 56.4 shows the register states in each operating mode.

**Table 56.3 Register Configuration**

Register Name	Abbreviation	R/W	Address	Access Size	RZ/G Series Products			
					RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Timer start register	TPU0_TSTR	R/W	H'E60F 0000	16	√	√	√	√
Timer control register 0	TPU0_TCR0	R/W	H'E60F 0010	16	√	√	√	√
Timer mode register 0	TPU0_TMDR0	R/W	H'E60F 0014	16	√	√	√	√
Timer I/O control register 0	TPU0_TIOR0	R/W	H'E60F 0018	16	√	√	√	√
Timer interrupt enable register 0	TPU0_TIER0	R/W	H'E60F 001C	16	√	√	√	√
Timer status register 0	TPU0_TSR0	R/W	H'E60F 0020	16	√	√	√	√
Timer counter 0	TPU0_TCNT0	R/W	H'E60F 0024	16	√	√	√	√
Timer general register A0	TPU0_TGRA0	R/W	H'E60F 0028	16	√	√	√	√
Timer general register B0	TPU0_TGRB0	R/W	H'E60F 002C	16	√	√	√	√
Timer general register C0	TPU0_TGRC0	R/W	H'E60F 0030	16	√	√	√	√
Timer general register D0	TPU0_TGRD0	R/W	H'E60F 0034	16	√	√	√	√
Timer control register 1	TPU0_TCR1	R/W	H'E60F 0050	16	√	√	√	√
Timer mode register 1	TPU0_TMDR1	R/W	H'E60F 0054	16	√	√	√	√
Timer I/O control register 1	TPU0_TIOR1	R/W	H'E60F 0058	16	√	√	√	√
Timer interrupt enable register 1	TPU0_TIER1	R/W	H'E60F 005C	16	√	√	√	√
Timer status register 1	TPU0_TSR1	R/W	H'E60F 0060	16	√	√	√	√
Timer counter 1	TPU0_TCNT1	R/W	H'E60F 0064	16	√	√	√	√
Timer general register A1	TPU0_TGRA1	R/W	H'E60F 0068	16	√	√	√	√
Timer general register B1	TPU0_TGRB1	R/W	H'E60F 006C	16	√	√	√	√
Timer general register C1	TPU0_TGRC1	R/W	H'E60F 0070	16	√	√	√	√
Timer general register D1	TPU0_TGRD1	R/W	H'E60F 0074	16	√	√	√	√
Timer control register 2	TPU0_TCR2	R/W	H'E60F 0090	16	√	√	√	√
Timer mode register 2	TPU0_TMDR2	R/W	H'E60F 0094	16	√	√	√	√
Timer I/O control register 2	TPU0_TIOR2	R/W	H'E60F 0098	16	√	√	√	√
Timer interrupt enable register 2	TPU0_TIER2	R/W	H'E60F 009C	16	√	√	√	√
Timer status register 2	TPU0_TSR2	R/W	H'E60F 00A0	16	√	√	√	√
Timer counter 2	TPU0_TCNT2	R/W	H'E60F 00A4	16	√	√	√	√
Timer general register A2	TPU0_TGRA2	R/W	H'E60F 00A8	16	√	√	√	√
Timer general register B2	TPU0_TGRB2	R/W	H'E60F 00AC	16	√	√	√	√
Timer general register C2	TPU0_TGRC2	R/W	H'E60F 00B0	16	√	√	√	√
Timer general register D2	TPU0_TGRD2	R/W	H'E60F 00B4	16	√	√	√	√
Timer control register 3	TPU0_TCR3	R/W	H'E60F 00D0	16	√	√	√	√
Timer mode register 3	TPU0_TMDR3	R/W	H'E60F 00D4	16	√	√	√	√
Timer I/O control register 3	TPU0_TIOR3	R/W	H'E60F 00D8	16	√	√	√	√

Register Name	Abbreviation	R/W	Address	Access Size	RZ/G Series Products			
					RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Timer interrupt enable register 3	TPU0_TIER3	R/W	H'E60F 00DC	16	√	√	√	√
Timer status register 3	TPU0_TSR3	R/W	H'E60F 00E0	16	√	√	√	√
Timer counter 3	TPU0_TCNT3	R/W	H'E60F 00E4	16	√	√	√	√
Timer general register A3	TPU0_TGRA3	R/W	H'E60F 00E8	16	√	√	√	√
Timer general register B3	TPU0_TGRB3	R/W	H'E60F 00EC	16	√	√	√	√
Timer general register C3	TPU0_TGRC3	R/W	H'E60F 00F0	16	√	√	√	√
Timer general register D3	TPU0_TGRD3	R/W	H'E60F 00F4	16	√	√	√	√
Motor control setting register	TPU0_TMIR	R/W	H'E60F 0100	16	√	√	√	√
Motor deceleration (stop) transition register	TPU0_TMRR	R/W	H'E60F 0104	16	√	√	√	√
Motor control status register	TPU0_TMSR	R	H'E60F 0108	16	√	√	√	√
Motor operation pattern storing register 0	TPU0_TMMPR0	R/W	H'E60F 0110	16	√	√	√	√
Motor operation pattern storing register 1	TPU0_TMMPR1	R/W	H'E60F 0114	16	√	√	√	√
Motor stop pattern storing register 0	TPU0_TMSPR0	R/W	H'E60F 0118	16	√	√	√	√
Motor stop pattern storing register 1	TPU0_TMSPR1	R/W	H'E60F 011C	16	√	√	√	√
Motor output pattern storing register	TPU0_TMOPR	R/W	H'E60F 0120	16	√	√	√	√
Motor acceleration the number of steps register	TPU0_TMASR	R/W	H'E60F 0130	16	√	√	√	√
Motor normal the number of steps register	TPU0_TMTSR	R/W	H'E60F 0134	16	√	√	√	√
Motor deceleration the number of steps register	TPU0_TMRSR	R/W	H'E60F 0138	16	√	√	√	√
Motor control sequence counter register	TPU0_TMSCR	R/W	H'E60F 0140	16	√	√	√	√
Motor control normal counter register	TPU0_TMTCR	R	H'E60F 0144	16	√	√	√	√

**Table 56.4 Register States in Each Operating Mode**

<b>Register Abbreviation</b>	<b>Reset *</b>	<b>Module Standby</b>
TPU0_TSTR	Initialized	Retained
TPU0_TCR0 to TPU0_TCR3	Initialized	Retained
TPU0_TMDR0 to TPU0_TMDR3	Initialized	Retained
TPU0_TIOR0 to TPU0_TIOR3	Initialized	Retained
TPU0_TIER0 to TPU0_TIER3	Initialized	Retained
TPU0_TSR0 to TPU0_TSR3	Initialized	Retained
TPU0_TCNT0 to TPU0_TCNT3	Initialized	Retained
TPU0_TGRA0 to TPU0_TGRA3	Initialized	Retained
TPU0_TGRB0 to TPU0_TGRB3	Initialized	Retained
TPU0_TGRC0 to TPU0_TGRC3	Initialized	Retained
TPU0_TGRD0 to TPU0_TGRD3	Initialized	Retained
TPU0_TMIR	Initialized	Retained
TPU0_TMRR	Initialized	Retained
TPU0_TMSR	Initialized	Retained
TPU0_TMMPR0	Initialized	Retained
TPU0_TMMPR1		
TPU0_TMSPR0	Initialized	Retained
TPU0_TMSPR1		
TPU0_TMOPR	Initialized	Retained
TPU0_TMASR	Initialized	Retained
TPU0_TMTSR	Initialized	Retained
TPU0_TMRSR	Initialized	Retained
TPU0_TMSCR	Initialized	Retained
TPU0_TMTCR	Initialized	Retained

Note: \* Refer to section 8, Reset (RST).

### 56.2.1 Timer Control Register (TPU0\_TCR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

TPU0\_TCR is provided for each of timers 0 to 3 and is used to control TPU0\_TCNT. TPU0\_TCR is initialized to H'0000 by a reset.

Writing to TPU0\_TCR is only allowed only when TPU0\_TCNT is stopped.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	CCLR[2:0]			CKEG[1:0]		TPSC[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 8	—	All 0	R	Reserved These bits are always read as 0 and cannot be modified.
7 to 5	CCLR[2:0]	000	R/W	Counter Clear Specify the TPU0_TCNT clearing source. 000: TPU0_TCNT clearing disabled 001: TPU0_TCNT cleared in response to TPU0_TGRA compare match 010: TPU0_TCNT cleared in response to TPU0_TGRB compare match 011: Setting prohibited 100: TPU0_TCNT clearing disabled 101: TPU0_TCNT cleared in response to TPU0_TGRC compare match 110: TPU0_TCNT cleared in response to TPU0_TGRD compare match 111: Setting prohibited
4, 3	CKEG[1:0]	00	R/W	Clock Edge Select the input clock edge for counting up. Counting of both edges by the internal clock has the same effect as halving the cycle of the input clock (e.g., the rate of counting both edges of $CP\phi/4$ is same as the rate of counting rising edges of $CP\phi/2$ ). When the phase coefficient mode is selected, this setting is ignored. 00: Count rising edges 01: Count falling edges* 1X: Count both edges* [Legend] X: Don't care Note: * If the input clock is $CP\phi/1$ , the timer does not operate with this setting.
2 to 0	TPSC[2:0]	000	R/W	Timer Prescaler Select the clock for counting by TPU0_TCNT. The clock source can be selected independently for each timer. Table 56.5 shows the clock sources that can be set for each timer. For more information on count clock selection, see Table 56.6.

**Table 56.5 TPU Clock Sources**

Timer	Internal Clock: CP $\phi$			
	Clock $\phi/1$	Clock $\phi/4$	Clock $\phi/16$	Clock $\phi/64$
0	√	√	√	√
1	√	√	√	√
2	√	√	√	√
3	√	√	√	√

[Legend]

√: Setting

**Table 56.6 Count Clock Selection by the TPSC[2:0] Bits**

Timer	TPSC[2]	TPSC[1]	TPSC[0]	Description
0 to 3	0	0	0	Internal clock $\phi/1$ (initial value)
			1	Internal clock $\phi/4$
			0	Internal clock $\phi/16$
			1	Internal clock $\phi/64$
1	*	*		Setting prohibited

[Legend]

\*: Don't care.

Note: Internal clock: CP $\phi$

### 56.2.2 Timer Mode Register (TPU0\_TMDR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

TPU0\_TMDR is provided for each of timers 0 to 3, and is used to specify the operating mode of the corresponding timer. TPU0\_TMDR is initialized to H'0000 by a reset.

Writing to TPU0\_TMDR is only allowed when TPU0\_TCNT is stopped.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	BFWT	BFB	BFA	—	MD[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 7	—	All 0	R	Reserved These bits are always read as 0 and cannot be modified.
6	BFWT	0	R/W	Buffer Write Timing Specifies when to update TPU0_TGRA and TPU0_TGRB when TPU0_TGRC and TPU0_TGRD are in use as compare match buffers. When TPU0_TGRC and TPU0_TGRD are not in use as compare match buffer registers, this has no effect. 0: TPU0_TGRA and TPU0_TGRB are rewritten on a compare match with the counters. 1: TPU0_TGRA and TPU0_TGRB are rewritten on clearing of the counter.
5	BFB	0	R/W	Buffer Operation B Specifies operation mode of TPU0_TGRB. 0: TPU0_TGRB is in normal operation. 1: TPU0_TGRB and TPU0_TGRD are used for buffered operation.
4	BFA	0	R/W	Buffer Operation A Specifies operation mode of TPU0_TGRA. 0: TPU0_TGRA normal operation. 1: TPU0_TGRA and TPU0_TGRC are used for buffered operation.
3	—	0	R	Reserved This bit is always read as 0 and cannot be modified.
2 to 0	MD[2:0]	000	R/W	Timer Operating Mode Specifies the timer operating mode. 000: Normal operation 001: Setting prohibited 010: PWM mode 011 to 111: Setting prohibited



**56.2.3 Timer I/O Control Register (TPU0\_TIOR)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

TPU0\_TIOR is provided for each of timers 0 to 3, and is used to control the corresponding TPU0TO0 to TPUTO3 pins. TPU0\_TIOR is initialized to H'0000 by a reset.

Writing to TPU0\_TIOR is only allowed when TPU0\_TCNT is stopped. Note that the setting of TPU0\_TMDR may affect TPU0\_TIOR.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	IOA[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 3	—	All 0	R	Reserved These bits are always read as 0 and cannot be modified.
2 to 0	IOA[2:0]	000	R/W	I/O Control Bits IOA2 to IOA0 specify the functions of TPU0_TGRA and the TPU0TO0 to TPUTO3 pins. For details, see Table 56.7.

**Table 56.7 Settings for Bits IOA[2:0], Initial States of Pins TPUTO0 to TPUTO3, and Results of Matching with TPU0\_TGRA**

Timer	IOA[2]	IOA[1]	IOA[0]	Description
0 to 3	0	0	0	Always output 0 (initial value)
			1	Initial output from the TPU0TO0 to TPUTO3 pins is 0
			0	Output 0 on compare match with TPU0_TGRA.*
			1	Output 1 on compare match with TPU0_TGRA.
0 to 3	0	1	0	Toggle output on compare match with TPU0_TGRA.*
			1	Always output 1
			0	Initial output from the TPU0TO0 to TPUTO3 pins is 1
			1	Output 0 on compare match with TPU0_TGRA.
0 to 3	1	0	0	Output 1 on compare match with TPU0_TGRA.*
			1	Output 1 on compare match with TPU0_TGRA.*
			0	Toggle output on compare match with TPU0_TGRA.*
			1	Toggle output on compare match with TPU0_TGRA.*

Note: \* This setting is prohibited in PWM mode.

### 56.2.4 Timer Interrupt Enable Register (TPU0\_TIER)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

TPU0\_TIER is provided for each of timers 0 to 3 and is used to enable or disable the sources of interrupt requests for the corresponding timer. TPU0\_TIER is initialized to H'0000 by a reset. Bits 8 to 13 are only present in timer 0.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	TMD OFE	TMD RFE	TMS 1ER	TMS 1ET	TMS 1EA	TMS 1ES	—	—	—	TC1EV	TG1ED	TG1EC	TG1EB	TG1EA
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15, 14	—	All 0	R	Reserved These bits are always read as 0 and cannot be modified.
13	TMDOFE	0	R/W	Motor Control Data Transfer Overflow Detection Enable This bit enables or disables interrupt request in response to the state of the TMDOFS flag in the stepping motor control mode of timer 0. This bit is reserved in timers 1 to 3, is always read as 0, and cannot be modified. 0: Interrupt request in response to the TMDOFS flag disabled 1: Interrupt request in response to the TMDOFS flag enabled
12	TMDRFE	0	R/W	Motor Control Data Transfer Request Detection Enable This bit enables or disables interrupt request in response to the state of the TMDRFS flag in the stepping motor control mode of timer 0. This bit is reserved in timers 1 to 3, is always read as 0, and cannot be modified. 0: Interrupt request in response to the TMDRFS flag disabled 1: Interrupt request in response to the TMDRFS flag enabled
11	TMS1ER	0	R/W	Motor Control Deceleration Transition Detection Enable This bit enables or disables interrupt request in response to the state of the TMCFR flag in the stepping motor control mode of timer 0. This bit is reserved in timers 1 to 3, is always read as 0, and cannot be modified. 0: Interrupt request in response to the TMCFR flag disabled 1: Interrupt request in response to the TMCFR flag enabled
10	TMS1ET	0	R/W	Motor Control Normal Transition Detection Enable This bit enables or disables interrupt request in response to the state of the TMCFT flag in the stepping motor control mode of timer 0. This bit is reserved in timers 1 to 3, is always read as 0, and cannot be modified. 0: Interrupt request in response to the TMCFT flag disabled 1: Interrupt request in response to the TMCFT flag enabled

Bit	Bit Name	Initial Value	R/W	Description
9	TMS1EA	0	R/W	<p>Motor Control Acceleration Transition Detection Enable</p> <p>This bit enables or disables interrupt request in response to the state of the TMCFA flag in the stepping motor control mode of timer 0.</p> <p>This bit is reserved in timers 1 to 3, is always read as 0, and cannot be modified.</p> <p>0: Interrupt request in response to the TMCFA flag disabled 1: Interrupt request in response to the TMCFA flag enabled</p>
8	TMS1ES	0	R/W	<p>Motor Control Stop Transition Detection Enable</p> <p>This bit enables or disables interrupt request in response to the state of the TMCFS flag in the stepping motor control mode of timer 0.</p> <p>This bit is reserved in timers 1 to 3, is always read as 0, and cannot be modified.</p> <p>0: Interrupt request in response to the TMCFS flag disabled 1: Interrupt request in response to the TMCFS flag enabled</p>
7 to 5	—	All 0	R	<p>Reserved</p> <p>These bits are always read as 0 and cannot be modified.</p>
4	TC1EV	0	R/W	<p>Overflow Interrupt Enable</p> <p>This bit enables or disables the interrupt request in response to the state of the TCFV flag.</p> <p>0: Interrupt request in response to the TCFV flag disabled 1: Interrupt request in response to the TCFV flag enabled</p>
3	TG1ED	0	R/W	<p>TPU0_TGR Interrupt Enable D.</p> <p>This bit enables or disables interrupt request in response to the state of the TGFD bit.</p> <p>0: Interrupt request in response to the TGFD bit disabled 1: Interrupt request in response to the TGFD bit enabled</p>
2	TG1EC	0	R/W	<p>TPU0_TGR Interrupt Enable C</p> <p>This bit enables or disables interrupt request in response to the state of the TGFC bit.</p> <p>0: Interrupt request in response to the TGFC bit disabled 1: Interrupt request in response to the TGFC bit enabled</p>
1	TG1EB	0	R/W	<p>TPU0_TGR Interrupt Enable B</p> <p>This bit enables or disables interrupt request in response to the state of the TGFB bit.</p> <p>0: Interrupt request in response to the TGFB bit disabled 1: Interrupt request in response to the TGFB bit enabled</p>
0	TG1EA	0	R/W	<p>TPU0_TGR Interrupt Enable A</p> <p>This bit enables or disables interrupt request in response to the state of the TGFA bit.</p> <p>0: Interrupt request in response to the TGFA bit disabled 1: Interrupt request in response to the TGFA bit enabled</p>

### 56.2.5 Timer Status Registers (TPU0\_TSR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

TPU0\_TSR is provided for each of timers 0 to 3 and indicates the state of the corresponding timer. TPU0\_TSR is initialized to H'0000 by a reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	TMD OFS	TMD RFS	TMCFR	TMCFT	TMCFA	TMCFS	—	—	—	TCFV	TGFD	TGFC	TGFB	TGFA
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R	R	R	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*

Bit	Bit Name	Initial Value	R/W	Description
15, 14	—	All 0	R	Reserved These bits are always read as 0 and cannot be modified.
13	TMDOFS	0	R/(W)*	Motor Control Data Transfer Overflow Detection This flag indicates that a data transfer overflow has been detected in the stepping motor control mode of timer 0. This bit is reserved in timers 1 to 3, is always read as 0, and cannot be modified. [Clearing condition] Writing 0 to the TMDOFS bit after reading the TMDOFS bit while TMDOFS is set to 1 [Setting condition] When the DMA transfer overflow occurs
12	TMDRFS	0	R/(W)*	Motor Control Data Transfer Request Detection This flag indicates that a data transfer request interrupt has been detected in the stepping motor control mode of timer 0. If DMA transfer is not in use, data are written to TPU0_TGRD0 in response to this interrupt. This bit is reserved in timers 1 to 3, is always read as 0, and cannot be modified. [Clearing condition] Writing 0 to the TMDRFS bit after reading the TMDRFS bit while TMDRFS is set to 1 [Setting condition] When data transfer request occurs
11	TMCFR	0	R/(W)*	Motor Control Deceleration Transition Detection This flag indicates that the current sequence state of timer 0 in the stepping motor control mode is the deceleration state. This bit is reserved in timers 1 to 3, is always read as 0, and cannot be modified. [Clearing condition] Writing 0 to the TMCFR bit after reading TMCFR bit = 1 [Setting condition] When the sequence state is shifted to the deceleration state

Bit	Bit Name	Initial Value	R/W	Description
10	TMCFT	0	R/(W)*	<p>Motor Control Normal Transition Detection</p> <p>This flag indicates that the current sequence state of timer 0 in the stepping motor control mode is the normal state.</p> <p>This bit is reserved in timers 1 to 3, is always read as 0, and cannot be modified.</p> <p>[Clearing condition]</p> <p>Writing 0 to the TMCFT bit after reading TMCFT bit = 1</p> <p>[Setting condition]</p> <p>When the sequence state is shifted to the normal state</p>
9	TMCFA	0	R/(W)*	<p>Motor Control Acceleration Transition Detection</p> <p>This flag indicates that the current sequence state of timer 0 in the stepping motor control mode is the acceleration state.</p> <p>This bit is reserved in timers 1 to 3, is always read as 0, and cannot be modified.</p> <p>[Clearing condition]</p> <p>Writing 0 to the TMCFA bit after reading TMCFA bit = 1</p> <p>[Setting condition]</p> <p>When the sequence state is shifted to the acceleration state</p>
8	TMCFS	0	R/(W)*	<p>Motor Control Stop Transition Detection</p> <p>This flag indicates that the current sequence state of timer 0 in the stepping motor control mode is the stop state.</p> <p>This bit is reserved in timers 1 to 3, is always read as 0, and cannot be modified.</p> <p>[Clearing condition]</p> <p>Writing 0 to the TMCFS bit after reading TMCFS bit = 1</p> <p>[Setting condition]</p> <p>When the sequence state is shifted to the stop state</p>
7 to 5	—	All 0	R	<p>Reserved</p> <p>These bits are always read as 0 and cannot be modified.</p>
4	TCFV	0	R/(W)*	<p>Overflow</p> <p>This flag indicates that TPU0_TCNT has overflowed.</p> <p>[Clearing condition]</p> <p>Writing 0 to the TCFV bit after reading TCFV bit = 1</p> <p>[Setting condition]</p> <p>When the value of TPU0_TCNT overflows (when its value changes from H'FFFF to H'0000)</p>
3	TGFD	0	R/(W)*	<p>Compare Flag D</p> <p>This flag indicates that the values of TPU0_TCNT and TPU0_TGRD have matched (a compare match).</p> <p>[Clearing condition]</p> <p>Writing 0 to the TGFD bit after reading TGFD bit = 1</p> <p>[Setting condition]</p> <p>When the values of TPU0_TCNT and TPU0_TGRD have matched</p>

Bit	Bit Name	Initial Value	R/W	Description
2	TGFC	0	R/(W)*	<p>Compare Flag C</p> <p>This flag indicates that the values of TPU0_TCNT and TPU0_TGRC have matched (a compare match).</p> <p>[Clearing condition]</p> <p>Writing 0 to the TGFC bit after reading TGFC bit = 1</p> <p>[Setting condition]</p> <p>When the values of TPU0_TCNT and TPU0_TGRC have matched</p>
1	TGFB	0	R/(W)*	<p>Compare Flag B</p> <p>This flag indicates that the values of TPU0_TCNT and TPU0_TGRB have matched (a compare match).</p> <p>[Clearing condition]</p> <p>Writing 0 to the TGFB bit after reading TGFB bit = 1</p> <p>[Setting condition]</p> <p>When the values of TPU0_TCNT and TPU0_TGRB have matched</p>
0	TGFA	0	R/(W)*	<p>Output Compare Flag A</p> <p>This flag indicates that the values of TPU0_TCNT and TPU0_TGRA have matched (a compare match).</p> <p>[Clearing condition]</p> <p>Writing 0 to the TGFA bit after reading TGFA bit = 1</p> <p>[Setting condition]</p> <p>When the values of TPU0_TCNT and TPU0_TGRA are matched</p>

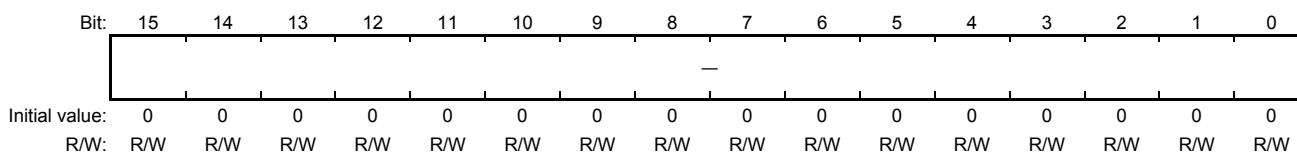
Note: \* Only 0 can be written to clear the flag.

### 56.2.6 Timer Counter (TPU0\_TCNT)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

TPU0\_TCNT is a 16-bit counter, and is provided for each of timers 0 to 3.

TPU0\_TCNT is initialized to H'0000 by a reset.



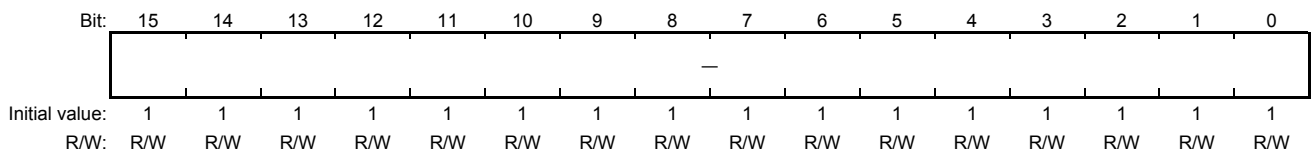
Bit	Bit Name	Initial Value	R/W	Description
15 to 0	—	All 0	R/W	Timer Counter Bits

**56.2.7 Timer General Register A to D (TPU0\_TGRA/TPU0\_TGRB/TPU0\_TGRC/TPU0\_TGRD)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

TPU0\_TGRA, TPU0\_TGRB, TPU0\_TGRC and TPU0\_TGRD are 16 bits general registers that are provided for each of timers 0 to 3. TPU0\_TGRC and TPU0\_TGRD can be designated for operation as buffer registers\*. TPU0\_TGR is initialized to H'FFFF by a reset.

Note: \* The combinations of TPU0\_TGR registers and buffer registers are TPU0\_TGRA with TPU0\_TGRC and TPU0\_TGRB with TPU0\_TGRD.



Bit	Bit Name	Initial Value	R/W	Description
15 to 0	—	All 1	R/W	Timer General Register Bits

### 56.2.8 Timer Start Register (TPU0\_TSTR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

TPU0\_TSTR is used to start or stop the timer counter (TCNT) of timers 0 to 3.

TPU0\_TSTR is initialized to H'0000 by a reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	TMST	CST3	CST2	CST1	CST0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 5	—	All 0	R	Reserved These bits are always read as 0 and cannot be modified.
4	TMST	0	R/W	Motor Control Sequence Start Selects whether to start or stop the motor control sequence. This bit is cleared to 0 when the timer has shifted to the stop state after motor control operation was started. 0: Stops motor control sequence 1: Starts motor control sequence
3	CST3	0	R/W	Counter Start Selects whether to start or stop the TPU0_TCNT3 operation. 0: Stops the TPU0_TCNT3 counting operation 1: Starts the TPU0_TCNT3 counting operation
2	CST2	0	R/W	Counter Start Selects whether to start or stop the TPU0_TCNT2 operation. 0: Stops the TPU0_TCNT2 counting operation 1: Starts the TPU0_TCNT2 counting operation
1	CST1	0	R/W	Counter Start Selects whether to start or stop the TPU0_TCNT1 operation. 0: Stops the TPU0_TCNT1 counting operation 1: Starts the TPU0_TCNT1 counting operation
0	CST0	0	R/W	Counter Start Selects whether to start or stop the TPU0_TCNT0 operation. 0: Stops the TPU0_TCNT0 counting operation 1: Starts the TPU0_TCNT0 counting operation



### 56.2.9 Motor Control Setting Register (TPU0\_TMIR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

TPU0\_TMIR is used to configure operation in the motor control mode.

TPU0\_TMIR is initialized to H'0000 by a reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	TDMAE	MTRPAT DOWN	MTRPATKING [1:0]	MTRON	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 5	—	All 0	R	Reserved These bits are always read as 0 and cannot be modified.
4	TDMAE	0	R/W	Selection of DMA Use Selects whether to use DMA for step interval input (writing to TPU0_TGRD0) in the motor control mode. 0: DMA is not used. 1: DMA is used.
3	MTRPAT DOWN	0	R/W	Operation and Stop Patterns Transition Ascending/Descending Select Selects the direction of transitions within operation and stop patterns as ascending or descending in the motor control mode. 0: Ascending 1: Descending
2, 1	MTRPAT KIND[1:0]	00	R/W	Operation and Stop Pattern Type Select Selects the number of patterns in the cycles of stop and start patterns in the motor control mode. 00: Four 01: Eight 10: Setting prohibited 11: Setting prohibited
0	MTRON	0	R/W	TPU Mode/Stepping Motor Control Mode Select 0: TPU mode 1: Stepping motor control mode  Note: This bit also controls a selecting signal to switch TPU0TO0 to TPU0TO 3 outputs. Set this bit to 1 after making initial settings for the pattern cycle. Do not modify this bit during the counter operation.

### 56.2.10 Motor Deceleration (Stop) Transition Register (TPU0\_TMRR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

TPU0\_TMRR is used to place timer 0 in to the deceleration state from the normal state, in the motor control mode.

TPU0\_TMRR is initialized to H'0000 by a reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	REDU ON0	REDU ON
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 2	—	All 0	R	Reserved These bits are always read as 0 and cannot be modified.
1	REDUON0	0	R/W	This bit is used to force a transition of timer 0 to the deceleration (or stop) state from the normal state in motor control mode. Note that the state transition only proceeds when pattern 0 is the currently specified pattern. Setting this bit has no effect if timer 0 is not in the normal state. This bit is automatically cleared to 0 when the state of timer 0 shifts to the stop state. 0: No operation 1: Timer 0 is forcibly placed in the deceleration (or stop) state from the normal state.
0	REDUON	0	R/W	This bit is used to force a transition of timer 0 to the deceleration (or stop) state from the normal state in motor control mode. Setting this bit has no effect if timer 0 is not in the normal state. This bit is automatically cleared to 0 when the state of timer 0 shifts to the stop state. 0: No operation 1: Timer 0 is forcibly placed in the deceleration (or stop) state from the normal state.

### 56.2.11 Motor Control Status Register (TPU0\_TMSR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

TPU0\_TMSR is a read-only register that indicates the sequence state in motor control mode.

TPU0\_TMSR is initialized to H'0001 by a reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	SITR	SITT	SITA	SITS
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15 to 4	—	All 0	R	Reserved These bits are always read as 0 and cannot be modified.
3	SITR	0	R	This bit indicates the sequence state in motor control mode. 1: The sequence state is deceleration. 0: The sequence state is not deceleration.
2	SITT	0	R	This bit indicates the sequence state in motor control mode. 1: The sequence state is normal. 0: The sequence state is not normal.
1	SITA	0	R	This bit indicates the sequence state in motor control mode. 1: The sequence state is acceleration. 0: The sequence state is not acceleration.
0	SITS	1	R	This bit indicates the sequence state in motor control mode. 1: The sequence state is stop. 0: The sequence state is not stop.

### 56.2.12 Motor Operation Pattern Storing Register 0 (TPU0\_TMMPR0)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

TPU0\_TMMPR0 is used to set motor operation patterns [3] to [0] in motor control mode.

TPU0\_TMMPR0 is initialized to H'0000 by a reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MP33	MP32	MP31	MP30	MP23	MP22	MP21	MP20	MP13	MP12	MP11	MP10	MP03	MP02	MP01	MP00
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	MP33	0	R/W	Motor Operation Pattern [3] in Motor Control Mode
14	MP32	0	R/W	MP33: TPU0TO3 output value in motor operation pattern [3]
13	MP31	0	R/W	MP32: TPU0TO2 output value in motor operation pattern [3]
12	MP30	0	R/W	MP31: TPU0TO1 output value in motor operation pattern [3] MP30: TPU0TO0 output value in motor operation pattern [3]
11	MP23	0	R/W	Motor Operation Pattern [2] in Motor Control Mode
10	MP22	0	R/W	MP23: TPU0TO3 output value in motor operation pattern [2]
9	MP21	0	R/W	MP22: TPU0TO2 output value in motor operation pattern [2]
8	MP20	0	R/W	MP21: TPU0TO1 output value in motor operation pattern [2] MP20: TPU0TO0 output value in motor operation pattern [2]
7	MP13	0	R/W	Motor Operation Pattern [1] in Motor Control Mode
6	MP12	0	R/W	MP13: TPU0TO3 output value in motor operation pattern [1]
5	MP11	0	R/W	MP12: TPU0TO2 output value in motor operation pattern [1]
4	MP10	0	R/W	MP11: TPU0TO1 output value in motor operation pattern [1] MP10: TPU0TO0 output value in motor operation pattern [1]
3	MP03	0	R/W	Motor Operation Pattern [0] in Motor Control Mode
2	MP02	0	R/W	MP03: TPU0TO3 output value in motor operation pattern [0]
1	MP01	0	R/W	MP02: TPU0TO2 output value in motor operation pattern [0]
0	MP00	0	R/W	MP01: TPU0TO1 output value in motor operation pattern [0] MP00: TPU0TO0 output value in motor operation pattern [0]

### 56.2.13 Motor Operation Pattern Storing Register 1 (TPU0\_TMMPR1)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

TPU0\_TMMPR1 is used to set motor operation pattern [7] to [4] in motor control mode.

TPU0\_TMMPR1 is initialized to H'0000 by a reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MP73	MP72	MP71	MP70	MP63	MP62	MP61	MP60	MP53	MP52	MP51	MP50	MP43	MP42	MP41	MP40
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	MP73	0	R/W	Motor Operation Pattern [7] in Motor Control Mode
14	MP72	0	R/W	MP73: TPU0TO3 output value in motor operation pattern [7]
13	MP71	0	R/W	MP72: TPU0TO2 output value in motor operation pattern [7]
12	MP70	0	R/W	MP71: TPU0TO1 output value in motor operation pattern [7] MP70: TPU0TO0 output value in motor operation pattern [7]
11	MP63	0	R/W	Motor Operation Pattern [6] in Motor Control Mode
10	MP62	0	R/W	MP63: TPU0TO3 output value in motor operation pattern [6]
9	MP61	0	R/W	MP62: TPU0TO2 output value in motor operation pattern [6]
8	MP60	0	R/W	MP61: TPU0TO1 output value in motor operation pattern [6] MP60: TPU0TO0 output value in motor operation pattern [6]
7	MP53	0	R/W	Motor Operation Pattern [5] in Motor Control Mode
6	MP52	0	R/W	MP53: TPU0TO3 output value in motor operation pattern [5]
5	MP51	0	R/W	MP52: TPU0TO2 output value in motor operation pattern [5]
4	MP50	0	R/W	MP51: TPU0TO1 output value in motor operation pattern [5] MP50: TPU0TO0 output value in motor operation pattern [5]
3	MP43	0	R/W	Motor Operation Pattern [4] in Motor Control Mode
2	MP42	0	R/W	MP43: TPU0TO3 output value in motor operation pattern [4]
1	MP41	0	R/W	MP42: TPU0TO2 output value in motor operation pattern [4]
0	MP40	0	R/W	MP41: TPU0TO1 output value in motor operation pattern [4] MP40: TPU0TO0 output value in motor operation pattern [4]

### 56.2.14 Motor Stop Pattern Storing Register 0 (TPU0\_TMSPR0)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

TPU0\_TMSPR0 is used to set motor stop pattern [3] to [0] in motor control mode.

TPU0\_TMSPR0 is initialized to H'0000 by a reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SP33	SP32	SP31	SP30	SP23	SP22	SP21	SP20	SP13	SP12	SP11	SP10	SP03	SP02	SP01	SP00
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	SP33	0	R/W	Motor Stop Pattern [3] in Motor Control Mode
14	SP32	0	R/W	SP33: TPU0TO3 output value in motor stop pattern [3]
13	SP31	0	R/W	SP32: TPU0TO2 output value in motor stop pattern [3]
12	SP30	0	R/W	SP31: TPU0TO1 output value in motor stop pattern [3] SP30: TPU0TO0 output value in motor stop pattern [3]
11	SP23	0	R/W	Motor Stop Pattern [2] in Motor Control Mode
10	SP22	0	R/W	SP23: TPU0TO3 output value in motor stop pattern [2]
9	SP21	0	R/W	SP22: TPU0TO2 output value in motor stop pattern [2]
8	SP20	0	R/W	SP21: TPU0TO1 output value in motor stop pattern [2] SP20: TPU0TO0 output value in motor stop pattern [2]
7	SP13	0	R/W	Motor Stop Pattern [1] in Motor Control Mode
6	SP12	0	R/W	SP13: TPU0TO3 output value in motor stop pattern [1]
5	SP11	0	R/W	SP12: TPU0TO2 output value in motor stop pattern [1]
4	SP10	0	R/W	SP11: TPU0TO1 output value in motor stop pattern [1] SP10: TPU0TO0 output value in motor stop pattern [1]
3	SP03	0	R/W	Motor Stop Pattern [0] in Motor Control Mode
2	SP02	0	R/W	SP03: TPU0TO3 output value in motor stop pattern [0]
1	SP01	0	R/W	SP02: TPU0TO2 output value in motor stop pattern [0]
0	SP00	0	R/W	SP01: TPU0TO1 output value in motor stop pattern [0] SP00: TPU0TO0 output value in motor stop pattern [0]

### 56.2.15 Motor Stop Pattern Storing Register 1 (TPU0\_TMSPR1)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

TPU0\_TMSPR1 is used to set motor stop pattern [7] to [4] in motor control mode.

TPU0\_TMSPR1 is initialized to H'0000 by a reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SP73	SP72	SP71	SP70	SP63	SP62	SP61	SP60	SP53	SP52	SP51	SP50	SP43	SP42	SP41	SP40
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	SP73	0	R/W	Motor Stop Pattern [7] in Motor Control Mode
14	SP72	0	R/W	SP73: TPU0TO3 output value in motor stop pattern [7]
13	SP71	0	R/W	SP72: TPU0TO2 output value in motor stop pattern [7]
12	SP70	0	R/W	SP71: TPU0TO1 output value in motor stop pattern [7] SP70: TPU0TO0 output value in motor stop pattern [7]
11	SP63	0	R/W	Motor Stop Pattern [6] in Motor Control Mode
10	SP62	0	R/W	SP63: TPU0TO3 output value in motor stop pattern [6]
9	SP61	0	R/W	SP62: TPU0TO2 output value in motor stop pattern [6]
8	SP60	0	R/W	SP61: TPU0TO1 output value in motor stop pattern [6] SP60: TPU0TO0 output value in motor stop pattern [6]
7	SP53	0	R/W	Motor Stop Pattern [5] in Motor Control Mode
6	SP52	0	R/W	SP53: TPU0TO3 output value in motor stop pattern [5]
5	SP51	0	R/W	SP52: TPU0TO2 output value in motor stop pattern [5]
4	SP50	0	R/W	SP51: TPU0TO1 output value in motor stop pattern [5] SP50: TPU0TO0 output value in motor stop pattern [5]
3	SP43	0	R/W	Motor Stop Pattern [4] in Motor Control Mode
2	SP42	0	R/W	SP43: TPU0TO3 output value in motor stop pattern [4]
1	SP41	0	R/W	SP42: TPU0TO2 output value in motor stop pattern [4]
0	SP40	0	R/W	SP41: TPU0TO1 output value in motor stop pattern [4] SP40: TPU0TO0 output value in motor stop pattern [4]

### 56.2.16 Motor Output Pattern Storing Register (TPU0\_TMOPR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

TPU0\_TMOPR is used to specify the motor output pattern in motor control mode. When read, it indicates the pattern currently being output. Writing to this register while the sequence is in the stop state leads to output of the pattern with the corresponding number. TPU0\_TMOPR is initialized to H'0000 by a reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	NOWPAT[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 3	—	All 0	R	Reserved These bits are always read as 0 and cannot be modified.
2 to 0	NOWPAT [2:0]	000	R/W	In motor control mode, Reading: The pattern number currently being output is read. Writing: If the sequence is in the stop state, the pattern corresponding to the written pattern number is output.

### 56.2.17 Motor Acceleration Step Count Register (TPU0\_TMASR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

TPU0\_TMASR is used to set the number of steps in the acceleration state of motor control mode. TPU0\_TMASR is initialized to H'0000 by a reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	AS[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

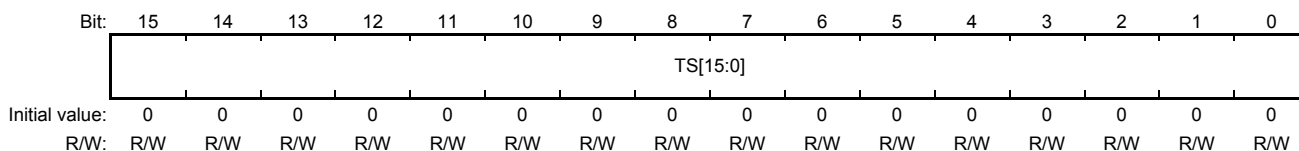
Bit	Bit Name	Initial Value	R/W	Description
15 to 0	AS[15:0]	H'0000	R/W	Specify the number of steps in the acceleration state of motor control mode. When the setting is H'0000, the acceleration state is skipped.



### 56.2.18 Motor Normal the Number of Steps Register (TPU0\_TMTSR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

TPU0\_TMTSR is used to set the number of steps in the normal state of motor control mode. TPU0\_TMTSR is initialized to H'0000 by a reset.

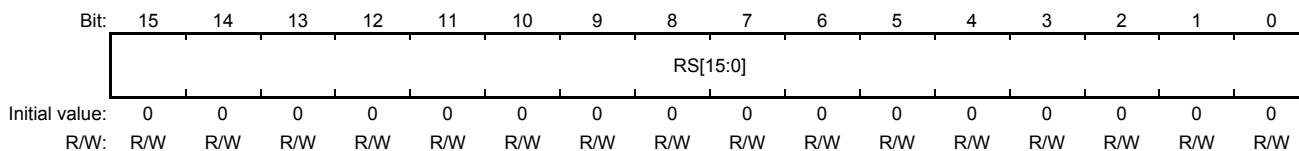


Bit	Bit Name	Initial Value	R/W	Description
15 to 0	TS[15:0]	H'0000	R/W	Specify the number of steps in the normal state of motor control mode.  When the setting is H'0000, the normal state is maintained until 1 is written to the REDUON0 bit or REDUON bit in TPU0_TMRR.

### 56.2.19 Motor Deceleration the Number of Steps Register (TPU0\_TMRSR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

TPU0\_TMRSR is used to set the number of steps in the deceleration state of motor control mode. TPU0\_TMRSR is initialized to H'0000 by a reset.



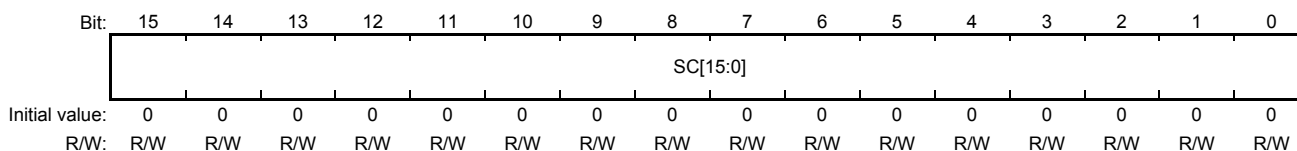
Bit	Bit Name	Initial Value	R/W	Description
15 to 0	RS[15:0]	H'0000	R/W	Specify the number of steps in the deceleration state of motor control mode.  When the setting is H'0000, the deceleration state is skipped.

### 56.2.20 Motor Control Sequence Counter Register (TPU0\_TMSCR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

TPU0\_TMSCR indicates or controls the value of the sequence counter in motor control mode. Writing to this register is only allowed when the motor control mode is in use and the current state is the normal state.

TPU0\_TMSCR is initialized to H'0000 by a reset.



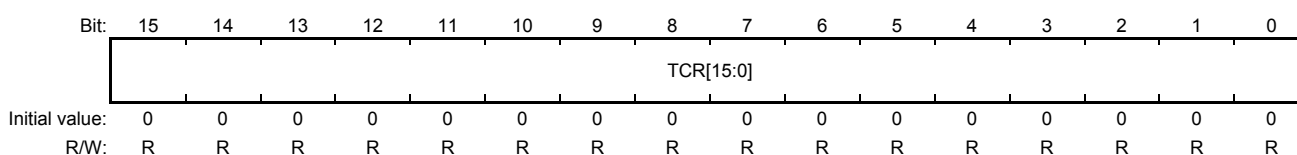
Bit	Bit Name	Initial Value	R/W	Description
15 to 0	SC[15:0]	H'0000	R/W	Value of Sequence Counter in Motor Control Mode Reading: The value of the sequence counter is read. Writing: Writing is only allowed in the normal state. The written value is directly stored in the sequence counter.

### 56.2.21 Motor Control Normal Counter Register (TPU0\_TMTCR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

TPU0\_TMTCR is a read-only register that indicates the number of steps in the normal state of motor control mode.

TPU0\_TMTCR is initialized to H'0000 by a reset.



Bit	Bit Name	Initial Value	R/W	Description
15 to 0	TCR[15:0]	H'0000	R	Indicate the number of steps in the normal state of motor control mode.

## 56.3 Operation

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

### 56.3.1 Overview

An overview of operation in the various modes is given below.

#### (1) Ordinary Operation

Each timer has TPU0\_TCNT and TPU0\_TGR registers. TPU0\_TCNT counts up, and is capable of free-running operation and counting to define periods corresponding to register settings.

#### (a) Buffered Operation

When a compare match occurs, the buffer register value in the corresponding timer is transferred to TPU0\_TGR. Either a compare match or clearing of the counter can be selected as the trigger that defines the timing of updating from a buffer register.

#### (b) PWM Mode

In PWM mode, a PWM waveform is output. The duty cycle can be set by TPU0\_TGR. PWM waveforms with duty cycles in the range from 0 to 100% can be output in accord with the settings of TPU0\_TGRA and TPU0\_TGRB.

#### (c) Stepping Motor Control Mode

Pre-defined patterns can be output from TPU0TO3 to TPU0TO0 by placing timer 0 to stepping motor control mode.

### 56.3.2 Basic Functions

#### (1) Counter Operation

When a bit from among CST3 to CST0 in TPU0\_TSTR is set to 1, the TPU0\_TCNT for the corresponding timer starts counting. A TPU0\_TCNT can operate as a free-running counter, periodic counter, and so on.

#### (a) Example of Procedure for Setting up Counter Operations

Figure 56.2 shows an example of the procedure for setting up counter operation.

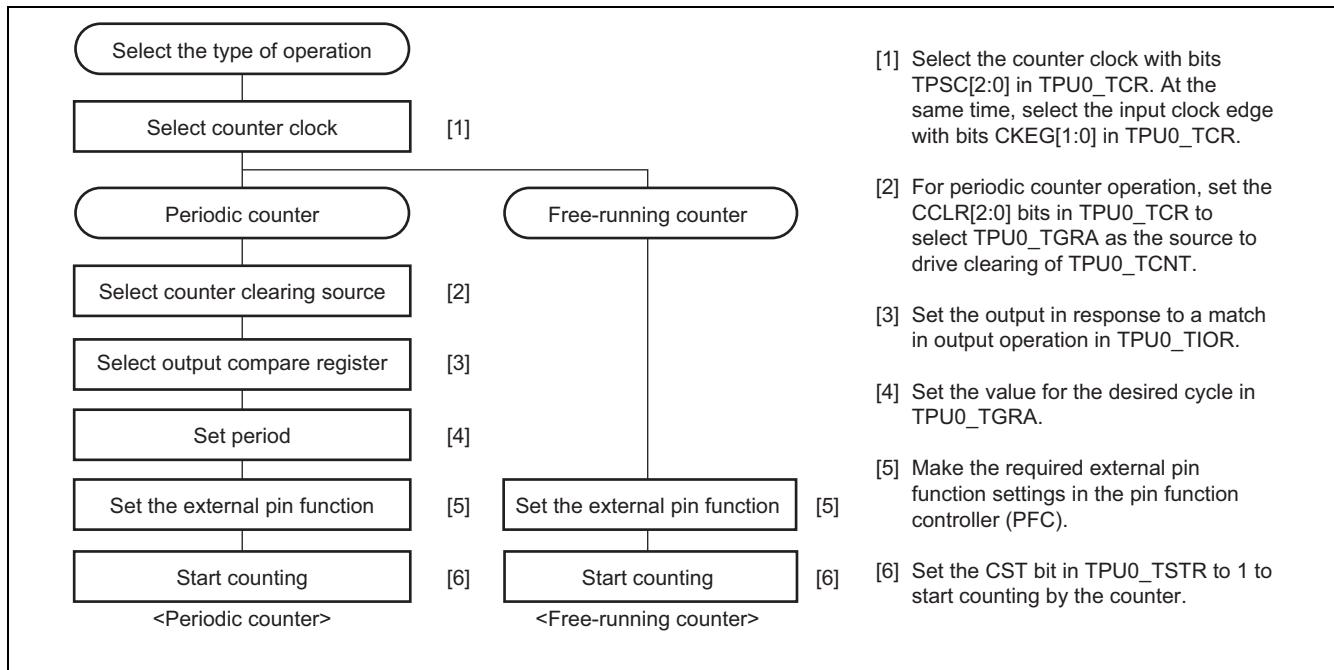
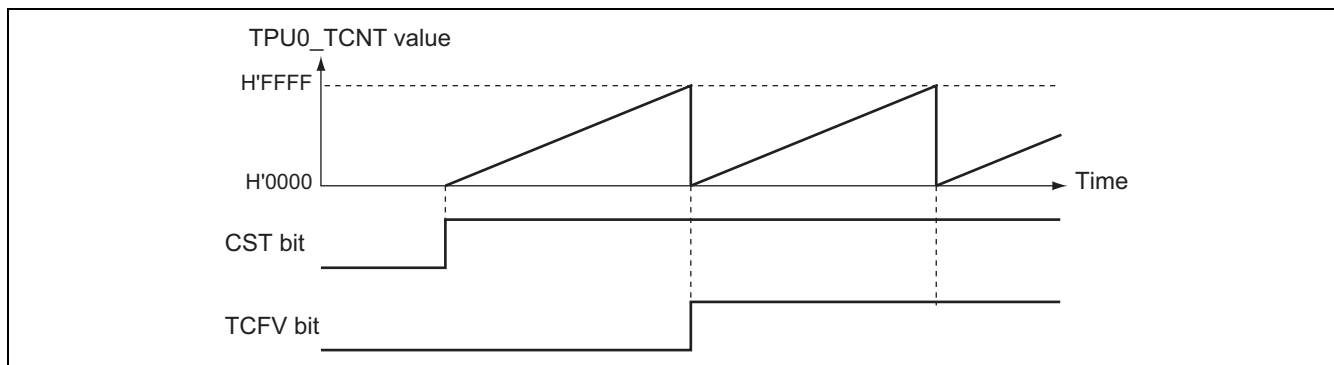


Figure 56.2 Example of Procedure for Setting up Counter Operation

**(b) Free-Running Counter Operation and Periodic Counter Operation**

Immediately after a reset, the TPU0\_TCNT counters are all designated as free-running counters. When the relevant bit in TPU0\_TSTR is set to 1, the corresponding TPU0\_TCNT starts counting up as a free-running counter. When TPU0\_TCNT has overflowed (when its value changes from H'FFFF to H'0000), the TCFV bit in TPU0\_TSR is set to 1. After it overflows, TPU0\_TCNT starts counting up again from H'0000.

Figure 56.3 illustrates free-running counter operation.

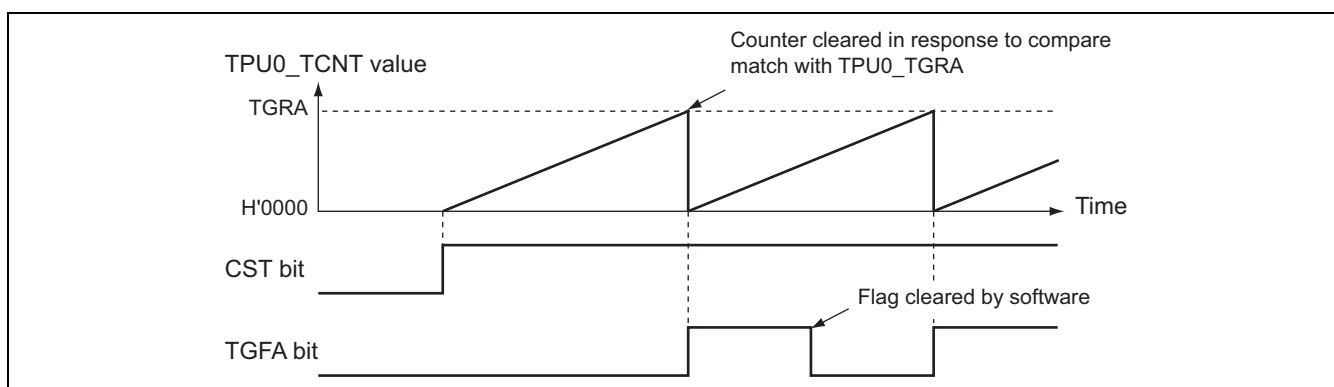


**Figure 56.3 Free-Running Counter Operation**

When a compare match is selected as the source to drive clearing of TPU0\_TCNT, the TPU0\_TCNT counter for the relevant timer operates as a periodic counter (counting a period defined by a general register). The TPU0\_TGR register for setting the period is designated as the output compare register, and counter clearing in response to a compare match is selected by means of bits CCLR[2:0] in TPU0\_TCR. After the settings have been made, TPU0\_TCNT starts counting as a periodic counter when the corresponding bit in TPU0\_TSTR is set to 1. When the counted value matches the value in the selected TPU0\_TGR, the TGF bit in TPU0\_TSR is set to 1 and TPU0\_TCNT is cleared to H'0000.

After a compare match, TPU0\_TCNT starts counting up again from H'0000.

Figure 56.4 illustrates periodic counter operation.



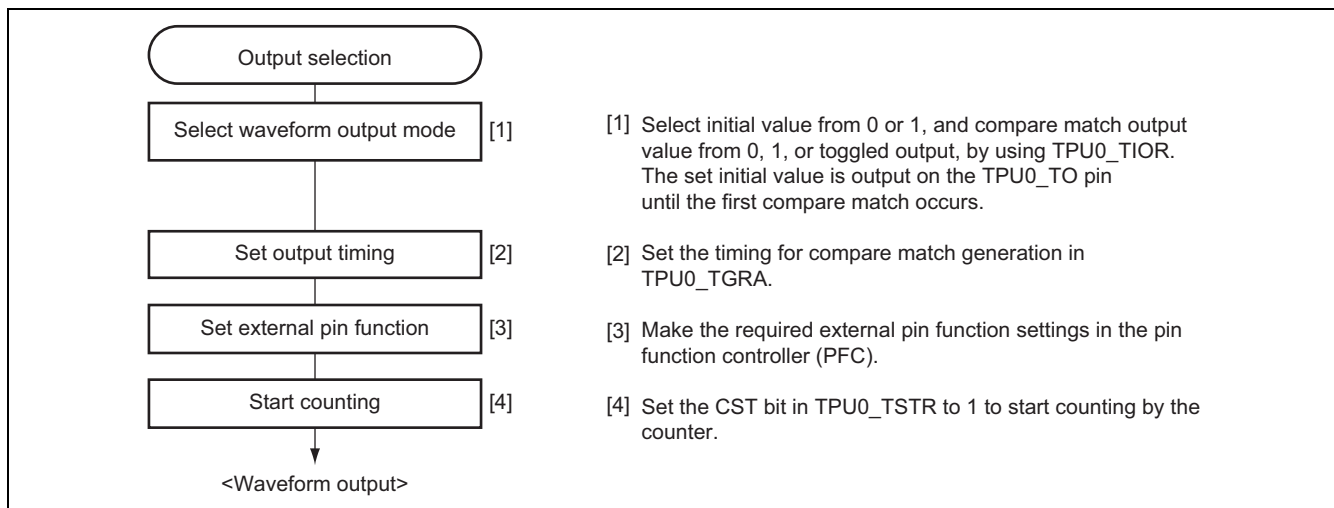
**Figure 56.4 Periodic Counter Operation**

**(2) Waveform Output by Compare Match**

The TPU can be set for the output of logical 0 or 1, or toggling of the output on the output pin in response to a compare match with TPU0\_TGRA.

**(a) Example of Procedure for Setting up Waveform Output under Compare Match Control**

Figure 56.5 shows an example of the procedure for setting up waveform output under compare match control.

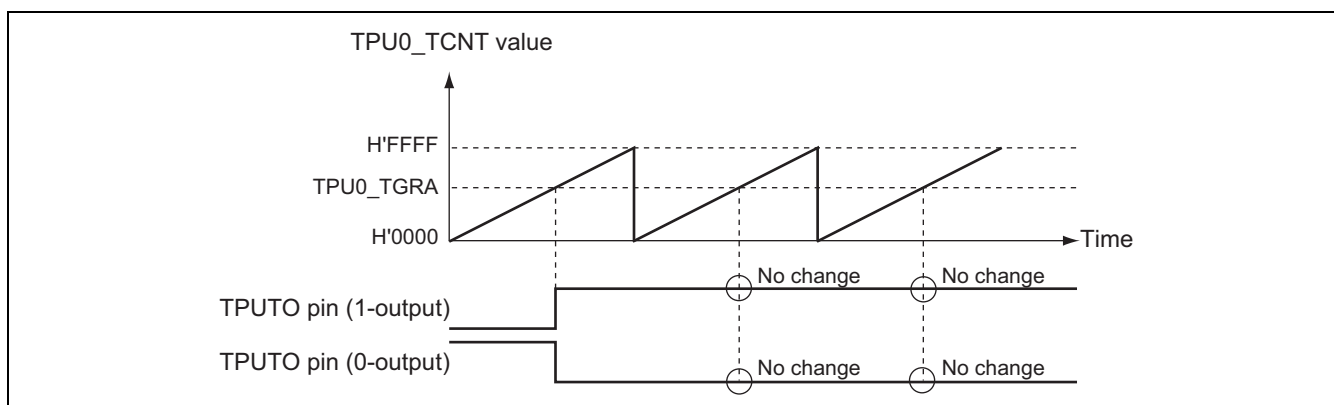


**Figure 56.5 Example of Procedure for Setting up Waveform Output under Compare Match Control**

**(b) Examples of Waveform Output Operation**

Figure 56.6 shows an example of the output of 0 or 1.

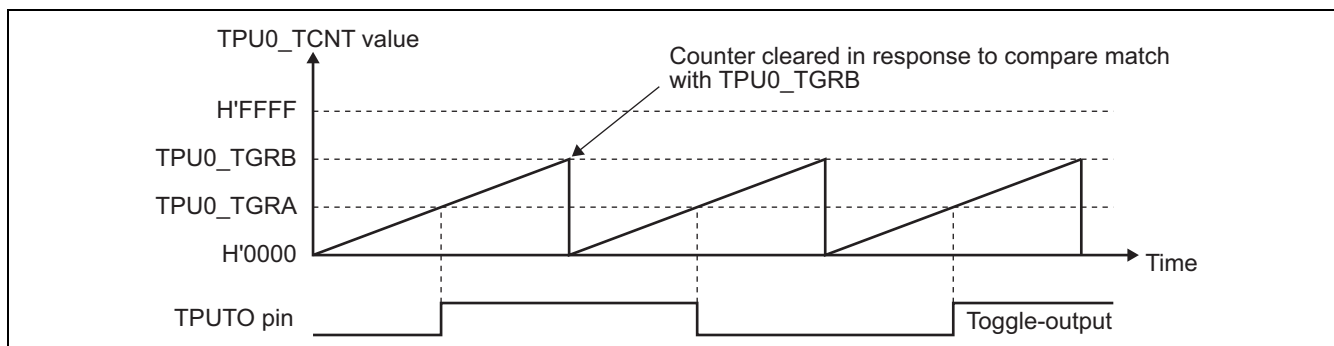
In this example, TPU0\_TCNT has been designated as a free-running counter, and settings have been made so that 1 or 0 is output in response to compare match A. When the set level is the same as the level on the pin, the level on the pin does not change.



**Figure 56.6 Example of Output of 0 or 1**

Figure 56.7 shows an example of toggled output.

In this example, TPU0\_TCNT has been designated as a periodic counter (with counter clearing handled by compare match B), and settings have been made so that the output is toggled in response to compare match A.



**Figure 56.7 Example of Toggled Output Operation**

### 56.3.3 Buffered Operation

TPU0\_TGRC and TPU0\_TGRD can be used as buffer registers.

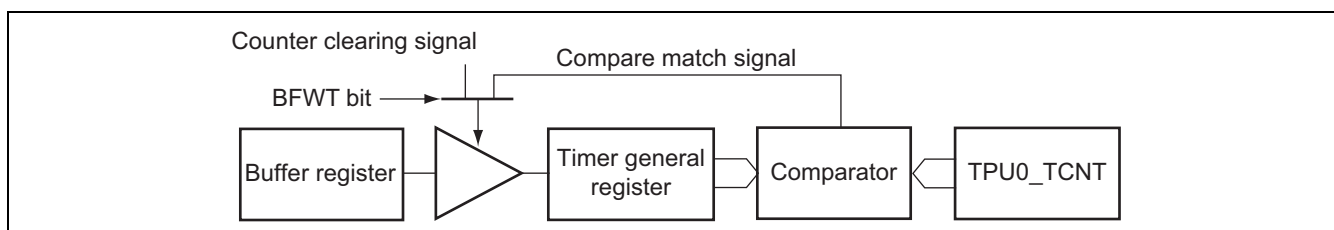
Table 56.8 shows the register combinations used in buffered operation.

**Table 56.8 Register Combinations in Buffered Operation**

Timer General Register	Buffer Register
TPU0_TGRA	TPU0_TGRC
TPU0_TGRB	TPU0_TGRD

When a compare match occurs, the value in the buffer register for the corresponding timer is transferred to the timer general register. Either a compare match or clearing of the counter can be selected as the trigger that defines the timing of updating from a buffer register.

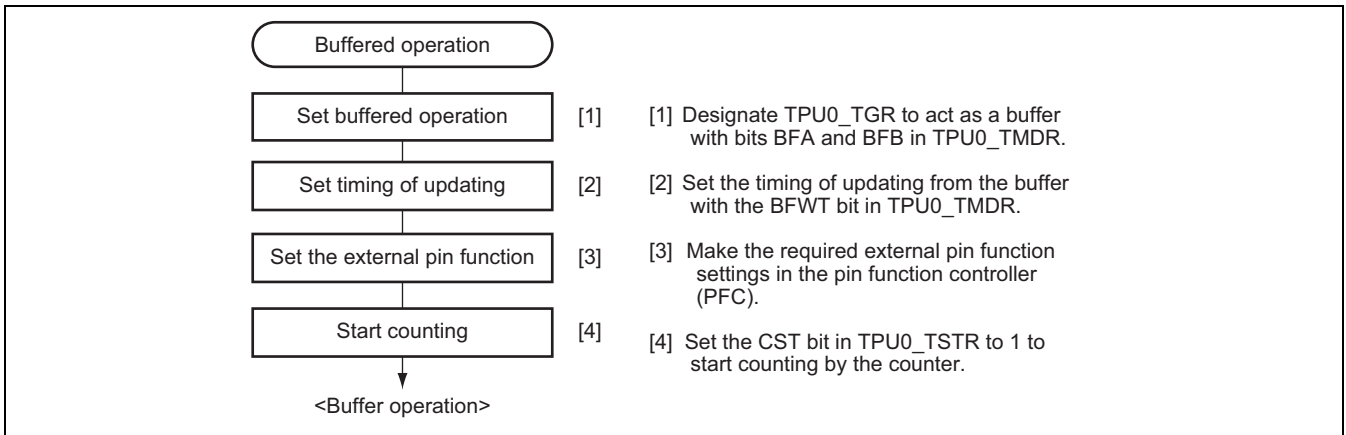
This operation is illustrated in Figure 56.8.



**Figure 56.8 Buffered Compare Match Operation**

**(1) Example of Procedure for Setting up Buffered Operation**

Figure 56.9 shows an example of the procedure for setting up buffered operation.



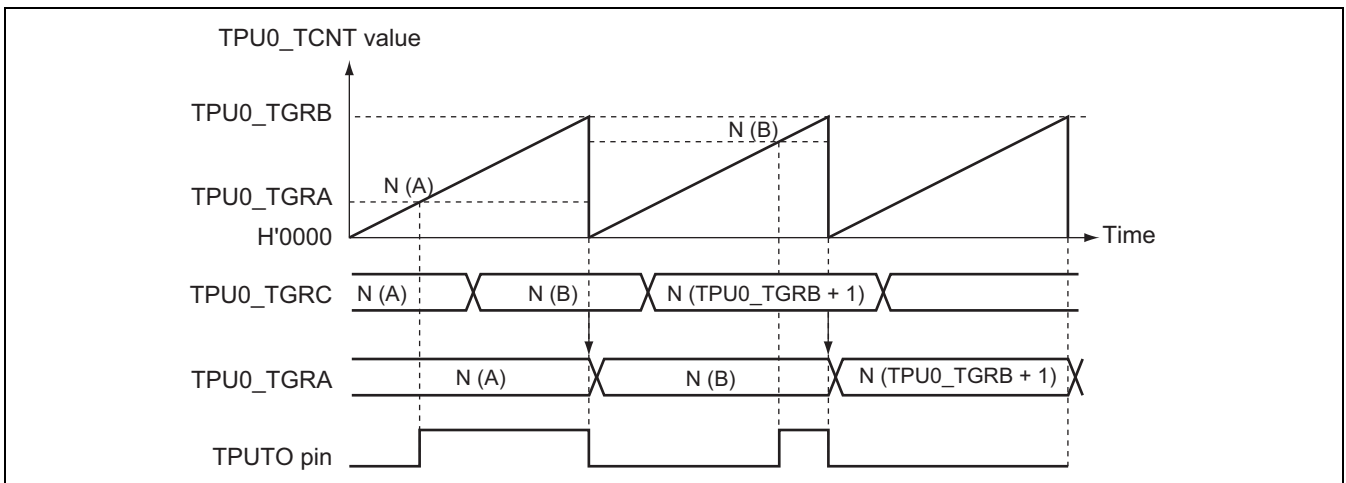
**Figure 56.9 Example of Procedure for Setting up Buffered Operation**

**(2) Examples of Buffered Operation**

Figure 56.10 shows an example of operation in which PWM mode has been designated for timer 0, and buffered operation has been designated for TPU0\_TGRA and TPU0\_TGRC. The settings used in this example are for clearing of TPU0\_TCNT in response to compare match B, output of 1 (on the TPU0TO0 to 3 for the selected timer) on compare match A, output of 0 as the initial value by clearing the counter, and the timing for updating from the buffer register as clearing of the counter.

When compare match A occurs, the output changes. When counter clearing is generated by a match with TPU0\_TGRB, the output changes and the value in buffer register TPU0\_TGRC is simultaneously transferred to the timer general register TPU0\_TGRA. This operation is repeated every time compare match A occurs.

For details on the PWM mode, see section 56.3.4, PWM Mode.



**Figure 56.10 Example of Buffer Operation**



### 56.3.4 PWM Mode

In PWM mode, PWM waveforms are output from the output pins. The output of 0 or 1 can be selected as the response to a compare match with the given TPU0\_TGRA.

Designating TPU0\_TGRB compare match as the counter clearing source enables setting of the overall cycle in that register. All timers can be independently placed in PWM mode.

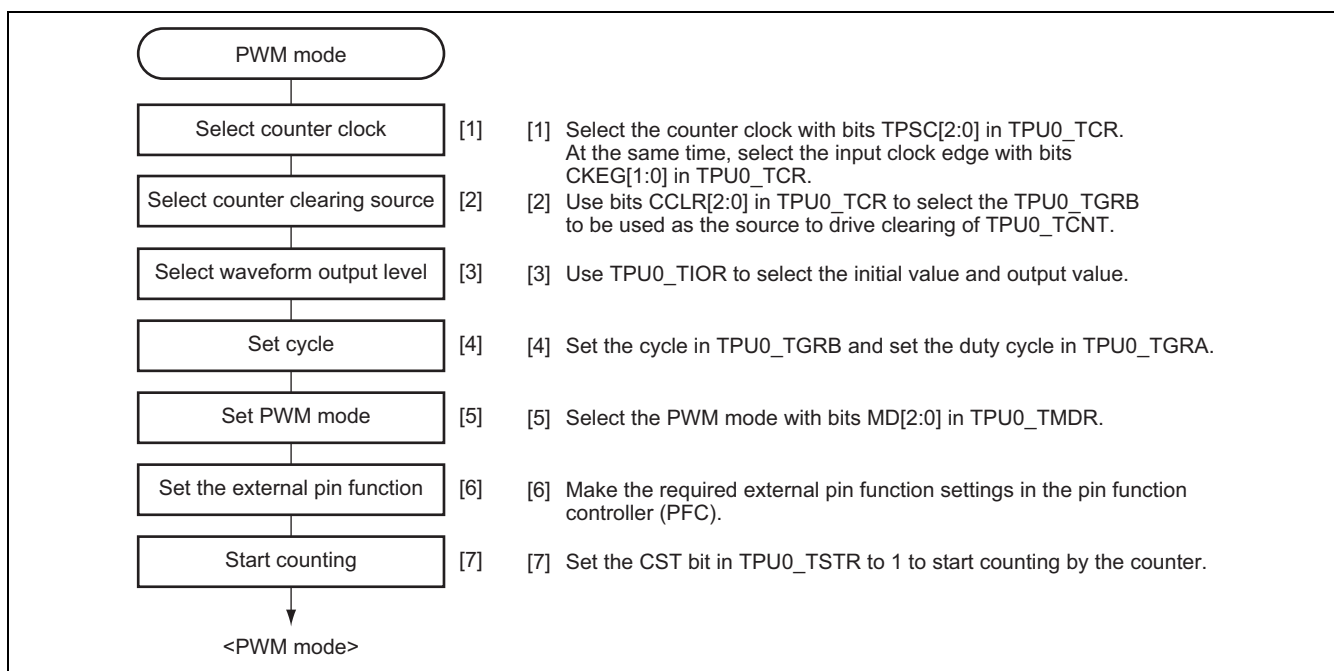
PWM output is generated from the output pins by using TPU0\_TGRA and TPU0\_TGRB to control the duty cycle and period, respectively. The initial output specified by TPU0\_TIOR is output on the output pin by counter clearing in response to a compare match with the period register. Be sure to set TPU0\_TIOR so that the initial output level is different from the compare match output. Selecting the same level or toggled output leads to no operation.

Conditions for 0% and 100% duty cycles are shown below.

- 0% duty cycle: The setting of the duty-cycle register (TPU0\_TGRA) being equal to that of the period register plus one (TPU0\_TGRB + 1)
- 100% duty cycle: The setting of the duty-cycle register (TPU0\_TGRA) being 0

#### (1) Example of Procedure for Setting up PWM Mode Operation

Figure 56.11 shows an example of the procedure for setting up the PWM mode operation.



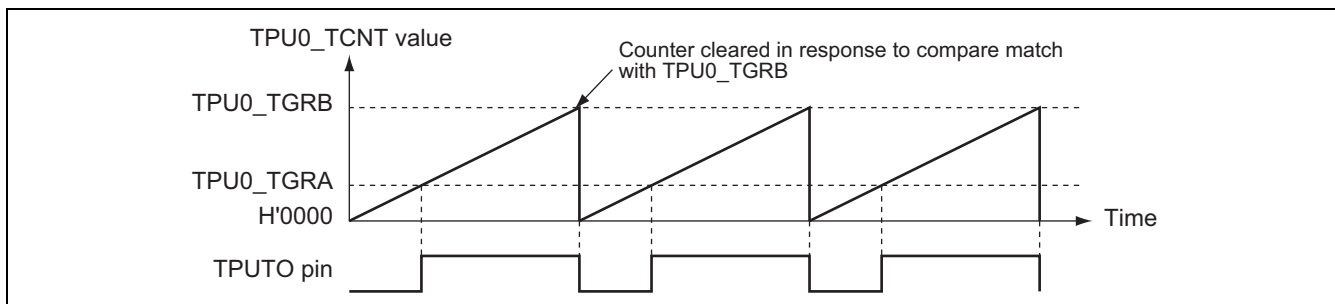
**Figure 56.11 Example of Procedure for Setting up PWM Mode Operation**

**(2) Examples of PWM Mode Operation**

Figure 56.12 shows an example of PWM mode operation.

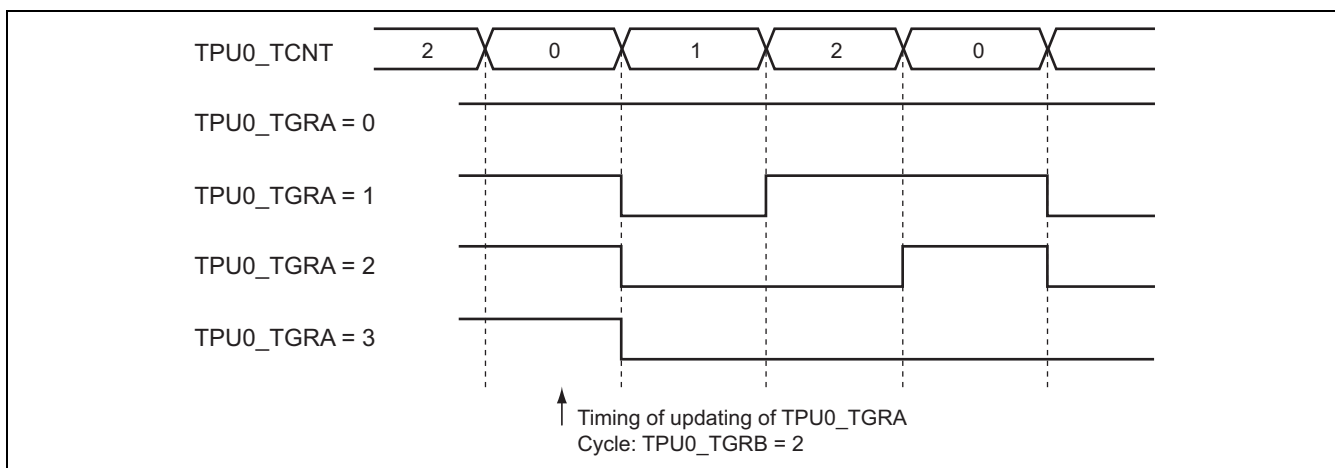
In this example, compare match with TPU0\_TGRB is set as the source to drive clearing of TPU0\_TCNT, 0 is set as the initial output value for TPU0\_TGRA, and 1 is set as the output value on a compare match with TPU0\_TGRA.

In this case, the value set in TPU0\_TGRB defines the cycle time (period), and the value set in TPU0\_TGRA defines the duty cycle.



**Figure 56.12 Example of PWM Mode Operation (1)**

Figure 56.13 shows an example of PWM waveform output with 0% and 100% duty cycles in PWM mode.



**Figure 56.13 Example of PWM Mode Operation (2)**

### 56.3.5 Stepping-Motor Control Mode

#### (1) Features of Stepping-Motor Control Mode

- This mode is for the output of signals for stepping-motor control on four pins and is only available for timer 0.
- States of the output pins change in response to compare matches with the counter of timer 0.
- By using the DMAC or an interrupt to rewrite the values of the compare-match registers, the intervals between transitions of the states of the output pins can be specified as desired.
- Specified patterns are output on the output pins.
- Four or eight patterns can be selected.
- The pattern-number counter is incremented or decremented by 1 on every compare match with the counter on timer 0. When the pattern-number counter overflows in normal mode, its value returns to 0. When the pattern-number counter underflows, its value becomes 3 (for a four-pattern cycle) or 7 (for an eight-pattern cycle).
- Patterns consist of stop patterns and operating patterns. Operating patterns are output while the counter is running, and stop patterns are output while the counter is stopped.
- While the counter is running, operation is in three states (the acceleration, deceleration, and normal states). Only for acceleration and deceleration, the interval between changes of pattern can be controlled.
- The acceleration or deceleration state can be skipped by writing H'0000 to TPU0\_TMASR and TPU0\_TMRSR.
- TPU0\_TMRR can be used to force a transition from the normal to the deceleration state.

#### (2) Glossary

Sequence State:	The four states in the sequence, i.e. the acceleration, normal, deceleration, and stop states
Sequence Counter:	Counter to control transitions to next sequence states The sequence counter is decremented with every compare match with the counter of timer 0 and, when the value reaches 1, the control state will make the transition to the next state in the sequence on a further compare match with the counter of timer 0.
Auto Mode:	Mode of operation when a value other than H'0000 has been written to TPU0_TMTSR The number of pattern transitions in the normal state corresponding to the setting of TPU0_TMTSR, and this is followed by an automatic transition to the deceleration state (or, if TPU0_TMRSR = H'0000, a transition to the stop state).
Manual Mode:	Mode of operation when H'0000 has been written to TPU0_TMTSR. In this case, the transition from the normal to the deceleration state (or the stop state if TPU0_TMRSR = H'0000) is not made unless 1 is written to the REDUON0 and REDUON bits in TPU0_TMRR.
Pulse Mode:	Mode of operation when H'0000 has been written to TPU0_TMASR and TPU0_TMRSR. Operation is only in the normal state, so the output pattern is changed with a constant interval.
Step:	The pattern is changed with every compare match with the counter of timer 0. Step refers to the interval of time between the change to one pattern and the change to the next.
Operation Pattern:	The four-bit patterns for output in the acceleration, normal, and deceleration states.
Stop Pattern:	The four-bit patterns for output in the stop state.

### (3) Setting up Basic Motor Control Operation

An example of operation in stepping motor control is shown in Figure 56.14.

Stepping-motor control mode allows the output of patterns with a variable step interval.

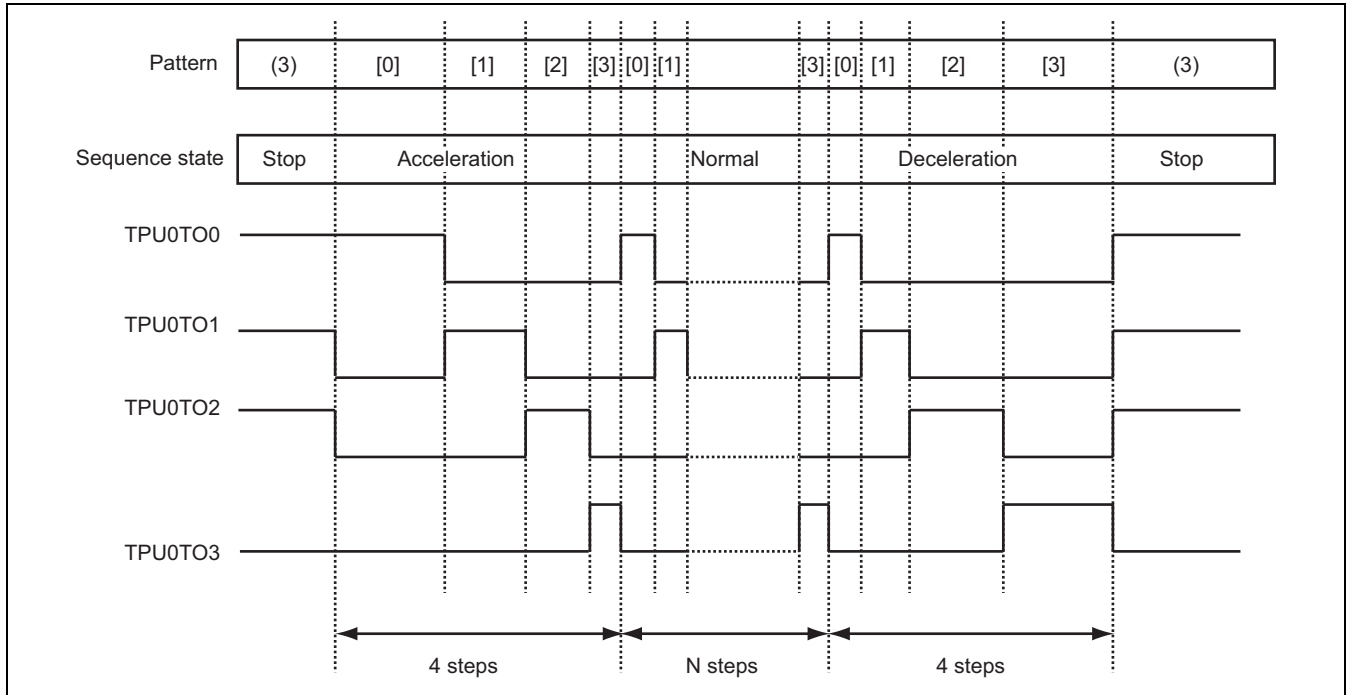


Figure 56.14 Example of Stepping-Motor Control

**(a) Compare Match Settings for Timer 0**

For stepping motor control, set TPU0\_TCR0 and TPU0\_TMDR0 as follows:

**Table 56.9 Compare Match Settings for Timer 0**

Register	Setting	Description
TPU0_TCR0	B'0000 0000 0100 0xxx	CCLR[2:0] bits = B'010 CKEG[1:0] bits = B'00 TPSC[2:0] bits = B'xxx (optional)
TPU0_TMDR0	B'0000 0000 0110 0000	BFWT bit = 1 BFB bit = 1 BFA bit = 0 MD[2:0] bits = B'000

[Legend]

x: Don't care.

With the above settings, TPU0\_TGRD0 is used as a buffer register for TPU0\_TGRB0, and the contents of the general register are rewritten when the timer counter is cleared. The step interval can be changed by using DMA transfer or interrupt control to write a desired value to TPU0\_TGRD0.

The TPSC[2:0] bits in TPU0\_TCR0 are for a timer prescaler setting. The step interval is calculated from the following formula.

**[For RZ/G1H, RZ/G1M, and RZ/G1N]**

With  $CP\phi$  at 15 MHz, B'011 as the value of TPSC[2:0] in TPU0\_TCR0, H'1425 as the value of TPU0\_TGRD0, the result is  $66.7 \text{ ns} \times 64 \times 5157 \text{ (H'1425)} = 25,380,691.2 \text{ ns} \cong 22 \text{ ms}$ . That is, the pattern will change after approximately 22 ms.

**[RZ/G1E]**

With  $CP\phi$  at 32.5 MHz, B'011 as the value of TPSC[2:0] in TPU0\_TCR0, H'1425 as the value of TPU0\_TGRD0, the result is  $30.8 \text{ ns} \times 64 \times 5157 \text{ (H'1425)} = 10,165,478.4 \text{ ns} \cong 10 \text{ ms}$ . That is, the pattern will change after approximately 10 ms.

**(b) Sequence State and the Number of Steps**

In stepping-motor control mode, operation is in three states (acceleration, normal, and deceleration) while the counter is running. In the acceleration and deceleration states, the step interval can be changed. Accordingly, the value of TPU0\_TGRD0 must be changed the same number of times as the patterns are changed.

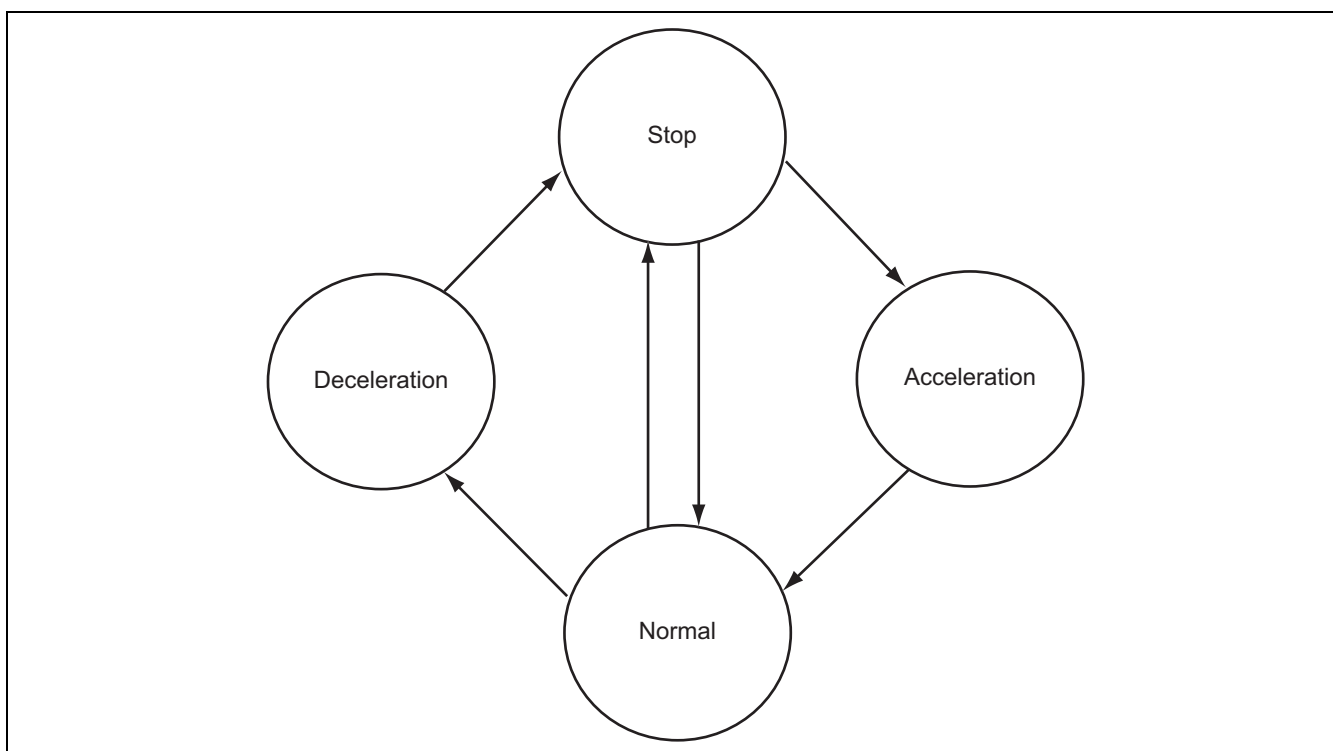
In the normal state, the step interval cannot be changed. So, TPU0\_TGRD0 is only set once for a period in the normal state.

The numbers of steps in the acceleration, normal, and deceleration states are set in TPU0\_TMASR, TPU0\_TMTSR, and TPU0\_TMRSR, respectively. If H'0000 is written to TPU0\_TMASR or TPU0\_TMRSR, the corresponding state is skipped. Furthermore, the manual mode can be selected by writing H'0000 to TPU0\_TMTSR. In this mode, the transition from normal mode can only be initiated by changing the value in TPU0\_TMRR.

Table 56.10 gives descriptions of the sequence states and Figure 56.15 shows the transitions between sequence states.

**Table 56.10 Description of Sequence States**

Start/Stop	State	Description	
		Step Interval	Definition in TPU0_TGRD0
Start	Acceleration	Variable	The number of steps specified for this state
	Normal	Fixed	Only once
	Deceleration	Variable	The number of steps specified for this state
Stop	Stop	—	—



**Figure 56.15 Sequence State Transition**

**(c) Setting of the Step Interval**

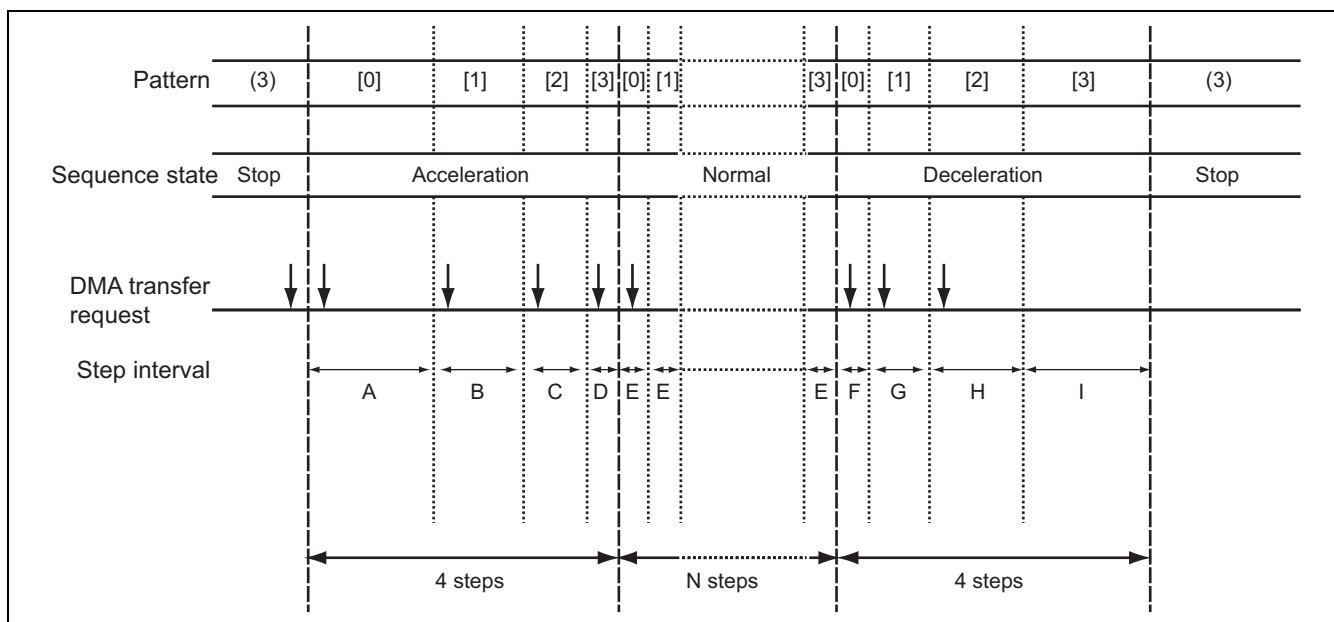
Direct memory access or interrupt-driven transfer can be used to set the step interval

- DMA transfer

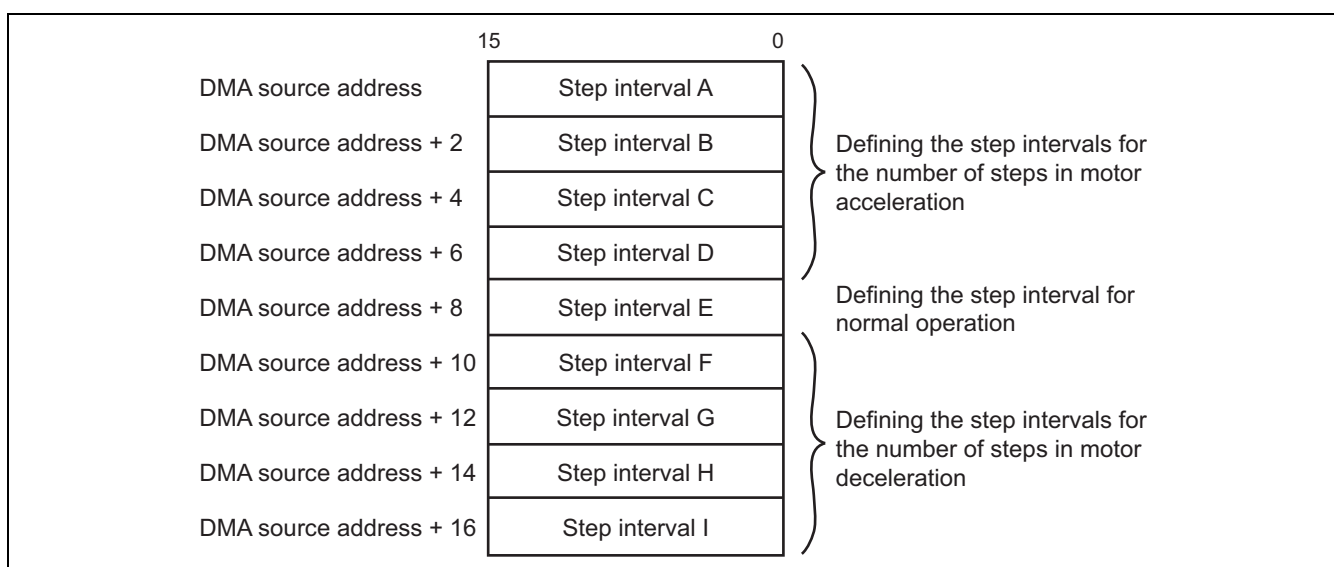
Setting the TDMAE bit in TPU0\_TMIR to 1 selects the use of DMA transfer to modify the step interval.

The number of requests for DMA transfer is given by  $TPU0\_TMASR + 1$  (to transfer the step interval for the normal state) +  $TPU0\_TMRSR$ . The step intervals must be defined in sequence from the address indicated by the DMA source address register. Figure 56.16 shows an example of timing in operation with DMA transfer requests used to set the step intervals. Figure 56.17 shows the corresponding definitions of step intervals in the address map.

Table 56.11 lists an example of the DMA settings.



**Figure 56.16 Operation with DMA Transfer Requests Used to Adjust the Step Interval**



**Figure 56.17 Address Map of Step Interval Definitions for the Example of Operation**

**Table 56.11 DMA Settings**

DMA Register	Setting	Description
DMA source address register	H'XXXX XXXX	Address where the table of step intervals starts
DMA destination address register	H'E70F 0034	Address of TPU0_TGRD0
DMA transfer count register	H'0000 0000	(Setting for the maximum number of transfer operations) *
DMA transfer count register B	H'XXXX XXXX	The number of DMA transfer requests is set in the higher- and lower-order 16 bits. (for Figure 56.16, H'0009 0009)
DMA channel control register	H'E670 80*C	Reload mode: Use source address registers (SARs) as the source for reloading. Fixed destination address. Incrementation of source addresses. The DMA extension resource selector is used. DMA transfer is in word (two-byte) units. The other bits are in the default settings.
DMA extension resource selector	H'F1 in the bit field for the selected DMA channel	Select TPU0
DMA operation register	H'0001	Permits DMA transfer on all channels. The other bits are in the default settings

Note: \* Transfer is stopped when the value of the DMA transfer counter reaches 0, so change the value of the DMA transfer counter back to 1 after TPU-related operations are finished.

- Interrupt-driven transfer

Setting the TMDRFE bit in TPU0\_TIER0 to 1 allows the use of interrupt-driven transfer to change the step interval.

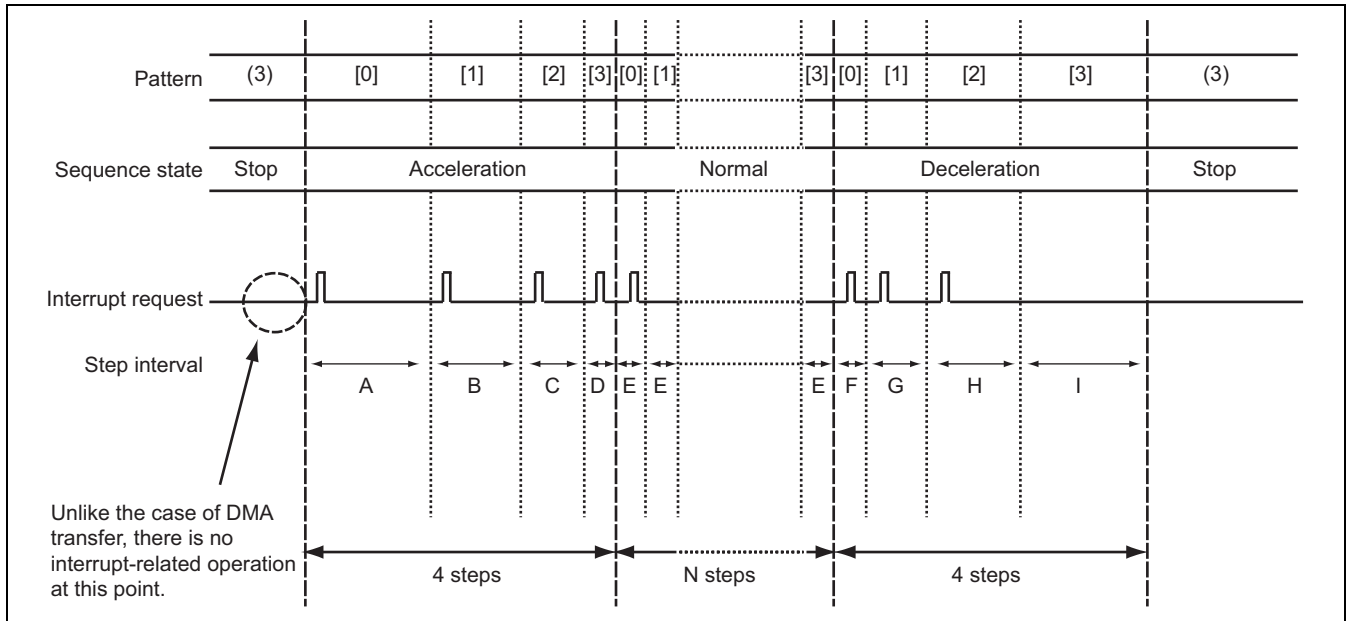
$TPU0\_TMASR-1 + 1$  (to transfer the step interval in the normal state) + TPU0\_TMRSR gives the number of times TPU0\_TGRD0 must be written to by interrupt-driven transfer.

This method is unlike DMA transfer in that an interrupt is not generated when the initial transfer is required. The initial value should thus be written to TPU0\_TGRD0 before counter operation starts.

Once interrupt generation starts, the interrupt handler writes the step intervals to TPU0\_TGRD0 and writes 0 to the TMDRFS bit after reading it as 1.

Figure 56.18 shows an example of timing in operation with interrupt-driven transfer used to set the step intervals.





**Figure 56.18 Interrupt-Driven Adjustment of the Step Interval**

The step-intervals in the example of operation shown in Figure 56.18 are defined in the following stages.

- Write step interval A to TPU0\_TGRD0 before starting the counter.
  - Write step interval B to TPU0\_TGRD0 in response to the first interrupt.
  - Write step interval C to TPU0\_TGRD0 in response to the second interrupt.
  - Write step interval D to TPU0\_TGRD0 in response to the third interrupt.
  - Write step interval E to TPU0\_TGRD0 in response to the fourth interrupt.
  - Write step interval F to TPU0\_TGRD0 in response to the fifth interrupt.
  - Write step interval G to TPU0\_TGRD0 in response to the sixth interrupt.
  - Write step interval H to TPU0\_TGRD0 in response to the seventh interrupt.
  - Write step interval I to TPU0\_TGRD0 in response to the eighth interrupt.
- } Defining the step intervals for the number of steps in motor acceleration
- } Defining the step interval for normal operation
- } Defining the step intervals for the number of steps in motor deceleration

**(d) Pattern Setting**

In stepping-motor control mode, each four-bit value for output on pins TPU0TO0 to TPU0TO3 is regarded as a single pattern. The patterns are in a sequence, and a compare match with the timer counter triggers each transition to the next pattern.

The following rules apply to pattern transfer.

- Either a four- or an eight-pattern cycle may be used. The number is determined by the MTRPATKIND bit in TPU0\_TMIR0.
- Each pattern is indicated by a pattern number. The current pattern number is either incremented or decremented on each compare match with the timer counter. Incrementation or decrementation of the pattern numbers is determined by the MTRPATDOWN bit in TPU0\_TMIR0.
- The pattern-number counter returns to 0 when it overflows. When it underflows, the pattern number becomes three (for a four-pattern cycle) or seven (for an eight-pattern cycle).
- Operating patterns are defined as the output patterns in the acceleration, normal, and deceleration states, and stop patterns are defined as the output patterns in the stop state. In transitions from an operating pattern to a stop pattern, the pattern number remains the same. In transitions from a stop pattern to an operating pattern, the current pattern number changes to that of the next pattern.

The operating patterns are set in TPU0\_TMMPR0 and TPU0\_TMMPR1, and the stop patterns are set in TPU0\_TMSPR0 and TPU0\_TMSPR1.

Table 56.12 lists the order of patterns for different settings of the MTRPATDOWN and MTRPATKIND bits in TPU0\_TMIR.

**Table 56.12 Settings of the MTRPATDOWN and MTRPATKIND Bits in TPU0\_TMIR and Orders of Patterns**

TPU0_TMIR		Example of Pattern Order (Operating Pattern [ ], Stop Pattern ( ))
MTRPATDOWN Bit	MTRPATKIND Bits	
0	B'00	[0] → [1] → [2] → [3] → [0] → [1] → [2] → [3] → (3) → [0]
1		[0] → [3] → [2] → [1] → [0] → [3] → [2] → [1] → (1) → [0]
0	B'01	[0] → [1] → [2] → [3] → [4] → [5] → [6] → [7] → (7) → [0]
1		[0] → [7] → [6] → [5] → [4] → [3] → [2] → [1] → (1) → [0]

**(e) Specifying the Output Pattern in the Stop State**

Specifying a pattern number in the NOWPAT[2:0] bits of TPU0\_TMOPR while output is in the stop state leads to output of the corresponding pattern on pins TPU0TO3 to TPU0TO0. The initial value is 0.

**(f) Selecting the Stepping-Motor Control Mode**

Stepping-motor control by the TPU circuit is selected by setting the MTRON bit in TPU0\_TMIR to 1. The output on pins TPU0TO3 to TPU0TO0 is switched to the output corresponding to stepping-motor control.

Switching should proceed while the motor is stopped.

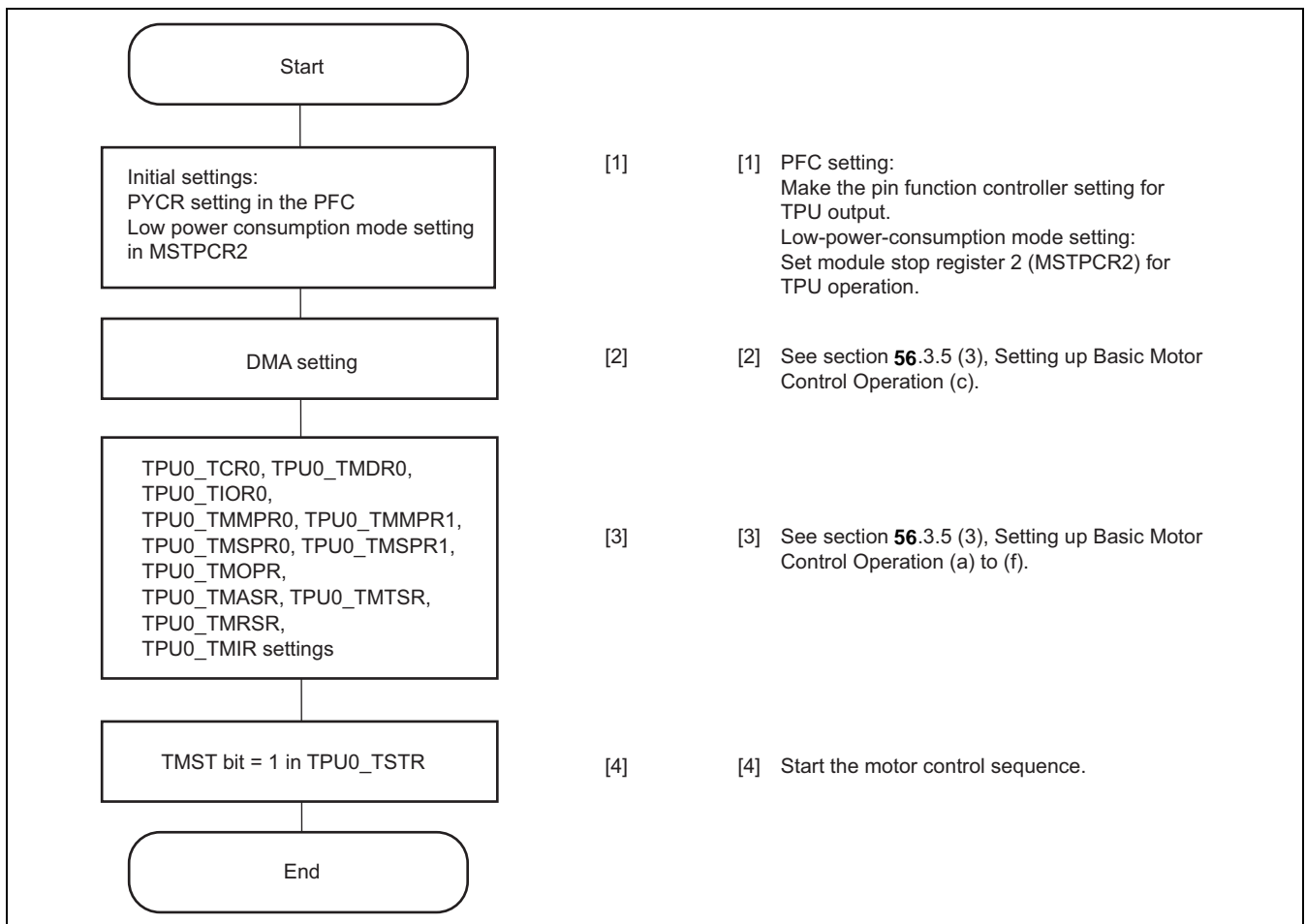
The stop pattern specified as pattern 0 in TPU0\_TMOPR is output after switching. Therefore, verify the value in TPU0\_TMOPR or write the desired pattern to TPU0\_TMOPR.

**(g) Starting Stepping-Motor Control**

Stepping-motor control is started by setting the TMST bit in TPU0\_TSTR to 1. This bit is automatically cleared (to 0) in the stop state after motor-control operations are over.

**(h) Example of the Procedure for Setting up Stepping-Motor Control**

Figure 56.19 is a flowchart of stepping-motor control.



**Figure 56.19 Flowchart**

#### (4) Changing the Number of Steps in the Normal State.

The number of steps in the normal state is set in TPU0\_TMTSR. The operations for changing the number of steps are described under (a) and (b) below.

In manual mode (TPU0\_TMTSR = H'0000), the operation under (a) is the only way of switching from the normal state.

##### (a) Changes by TPU0\_TMRR

Writing 1 to the REDUON0 bit or the REDUON bit in TPU0\_TMRR initiates the transition to the deceleration state (or, if TPU0\_TMRSR = H'0000, to the stop state).

Table 56.13 describes how operation in response to the writing of 1 to the REDUON0 bit varies with the operating state. Table 56.14 describes how operation in response to the writing of 1 to the REDUON bit varies with the operating state.

**Table 56.13 Timing of Writing 1 to the REDUON0 Bit and Operation**

Timing of Writing 1 to the REDUON0 Bit	Operation
Acceleration	Operation continues normally until the end of acceleration. Control then enters the normal state.
Normal	Control remains in the normal state until the pattern number becomes [0]. The transition to the deceleration state (or the stop state if TPU0_TMRSR is H'0000) follows the end of this step in the normal state.
Deceleration	Writing 1 to the bit has no effect on deceleration.
Stop	TPU0_TMRR is cleared to H'0000 after control has made the transition from the normal or deceleration state to the stop state. When 1 is written to the REDUON0 bit after control is in the stop state, the sequence in the next round of motor control continues until the pattern number in the normal state becomes [0]. The transition to the deceleration state (or the stop state if TPU0_TMRSR is H'0000) is made at the end of this step in the normal state.

**Table 56.14 Timing of Writing 1 to the REDUON Bit and Operation**

Timing to Write 1 in REDUON Bit	Operation
Acceleration	Operation continues normally until the end of acceleration.
Normal	The transition to the deceleration state (or the stop state if TPU0_TMRSR is H'0000) is made after a single step in the normal state.
Deceleration	Writing 1 to the bit has no effect on deceleration.
Stop	TPU0_TMRR is cleared to H'0000 after control has made the transition from the normal or deceleration state to the stop state. When 1 is written to the REDUON0 bit after control is in the stop state, the sequence in the next round of motor control continues until it enters the normal state. The transition to the deceleration state (or the stop state if TPU0_TMRSR is H'0000) is made at the end of a single step in the normal state.

**(b) Changing the Number of Steps by Changing the Value in TPU0\_TMSCR**

In auto mode (i.e. when TPU0\_TMTSR  $\neq$  H'0000), TMSCR indicates the remaining number of steps in the current state.

When the control sequence is in the normal state, the number of steps can be changed by writing the desired number of steps. Writing is ineffective in states other than the normal state.

Do not write to this register when control is in manual mode (TPU0\_TMTSR = H'0000).

**(5) Acquiring the Number of Steps in the Normal State**

In the stop state, TPU0\_TMTCR can be read to acquire the number of steps in the normal state of the immediately preceding sequence.

**(6) Pulse Mode**

Writing H'0000 to TPU0\_TMASR and TPU0\_TMRSR selects operation in the normal state alone, with a constant step interval. That is, operation starts with the step interval defined for the normal mode and the interval does not subsequently change. This is referred to as pulse mode operation.

Examples of pulse-mode operation are described below.

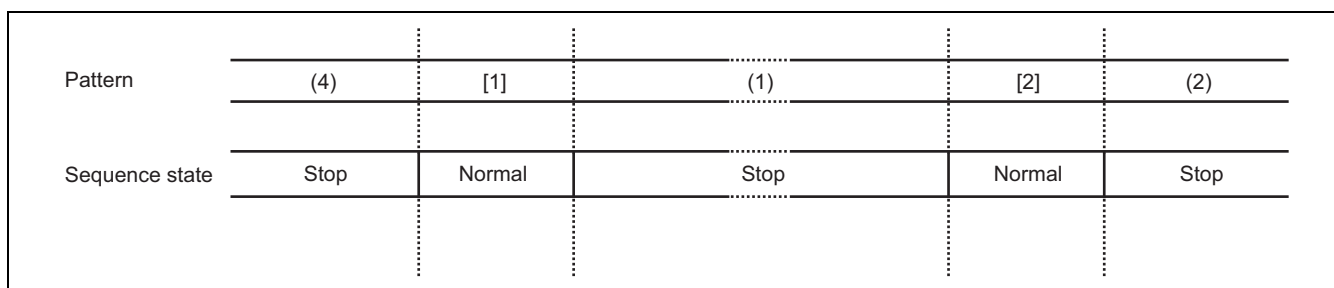
**(a) Single-Pulse Shifts in Pulse Mode and Auto Mode**

Table 56.15 gives an example of register settings for single-pulse steps in auto mode.

Figure 56.20 is a timing chart for single-pulse shifts in auto mode.

**Table 56.15 Register Settings to Select One Pulse as the Number of Steps in Auto Mode**

Register Setting Value	Contents
TPU0_TMASR: H'0000	No acceleration state
TPU0_TMTSR: H'0001	Only one step in the normal state
TPU0_TMRSR: H'0000	No deceleration state



**Figure 56.20 Timing of Single-Pulse Shifts in Auto Mode**

### (b) Single-Pulse Shifts in Pulse Mode and Manual Mode

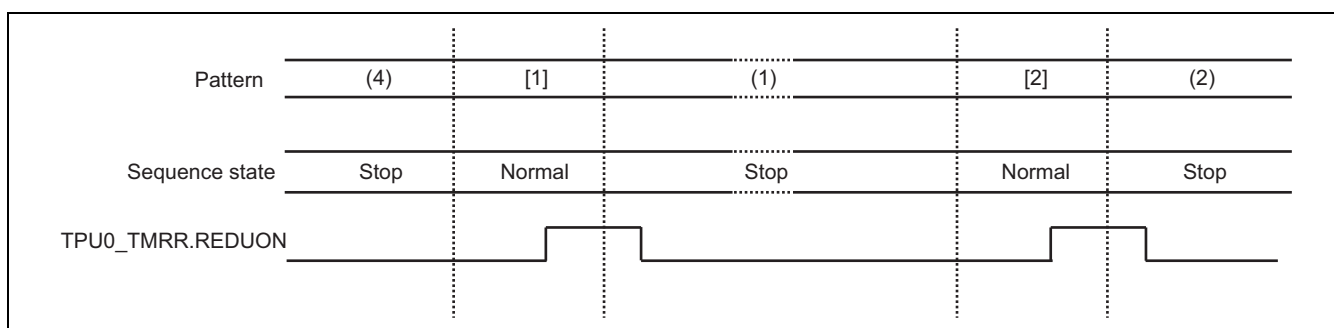
In manual mode, setting the REDUON0 or REDUON bit in TPU0\_TMRR to 1 while the sequence is in the normal state enables a single pulse shift.

Table 56.16 gives an example of register settings for single-pulse steps in manual mode.

Figure 56.21 is a timing chart for single-pulse shifts in manual mode.

**Table 56.16 Register Settings to Select One Pulse as the Number of Steps in Manual Mode**

Register Setting Value	Contents
TPU0_TMASR: H'0000	No acceleration state
TPU0_TMTSR: H'0000	Looping in the normal state
TPU0_TMRSR: H'0000	No deceleration state



**Figure 56.21 Timing of Single-Pulse Shifts in Manual Mode**

### (7) Interrupts

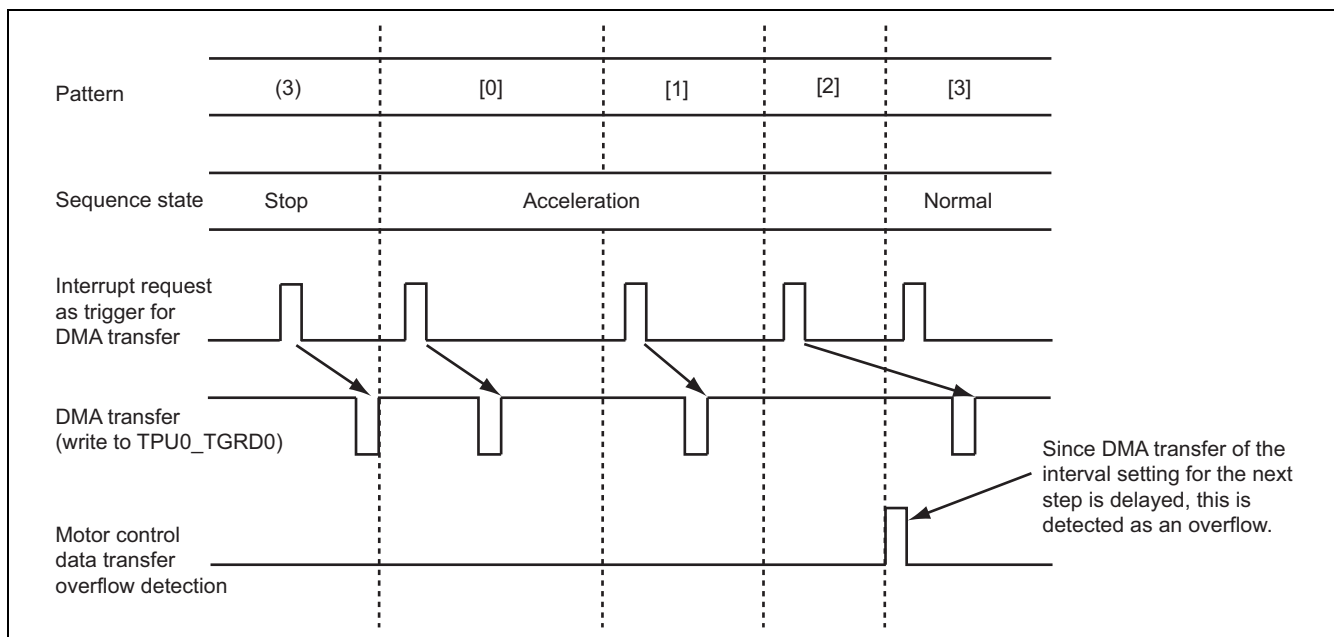
Timer 0 has six added interrupt conditions for use with stepping-motor control mode.

The interrupt conditions are described below.

#### (a) Detection of Overflows of Data Transferred for Motor Control

Setting the TMDOFE bit in TPU0\_TIER0 to 1 selects the detection of overflows of data transferred for motor control (motor control data transfer overflows). Here, overflow refers to the condition where buffer-related operation, i.e. the transfer of the data from TPU0\_TGRD0, is delayed; that is, when the operation TPU0\_TGRD0→TPU0\_TGRB0 is delayed. To cancel this interrupt, write 0 to the TMDOFS bit of TPU0\_TSR0 after having read it as 1.

Figure 56.22 shows an example of DMA transfer where an overflow in data transfer for motor control occurs and detection of overflows has been enabled.



**Figure 56.22 DMA Transfer with Detection of Motor Control Data Transfer Overflows Enabled**

Since this interrupt is for use in the debugging of defective operation, normal operation will not be restored even if it is detected.

#### (b) Detection of Requirement for Transfer of Motor control Data

Detection of requirements for the transfer of motor control data (detect motor control data transfer request) is enabled by setting the TMDRFE bit of TPU0\_TIER0. This interrupt is generated when the next pattern interval is to be changed from the current interval. On detection of this interrupt, the handler should write the setting for the next interval to TPU0\_TGRD0 and then write 0 to the TMDRFS bit of TPU0\_TSR0 after having read it as 1.

This interrupt is not available if DMA transfer has been selected (the TDMAE bit in TPU0\_TMIR = 1).

See Figure 56.18 for an example of usage of this interrupt.

#### (c) Detecting the Transition to Deceleration

Setting the TMS1ER bit in TPU0\_TIER0 to 1 enables detection of the transition to deceleration. The handler should clear the TMCFR flag of TPU0\_TSR0 by writing 0 to the bit after having read it as 1.

#### (d) Detecting the Transition to the Normal State

Setting the TMS1ET bit in TPU0\_TIER0 to 1 enables detection of the transition to the normal state. The handler should clear the TMCFT flag of TPU0\_TSR0 by writing 0 to the bit after having read it as 1.

#### (e) Detecting the Transition to Acceleration

Setting the TMS1EA bit in TPU0\_TIER0 to 1 enables detection of the transition to acceleration. The handler should clear the TMCFA flag of TPU0\_TSR0 by writing 0 to the bit after having read it as 1.

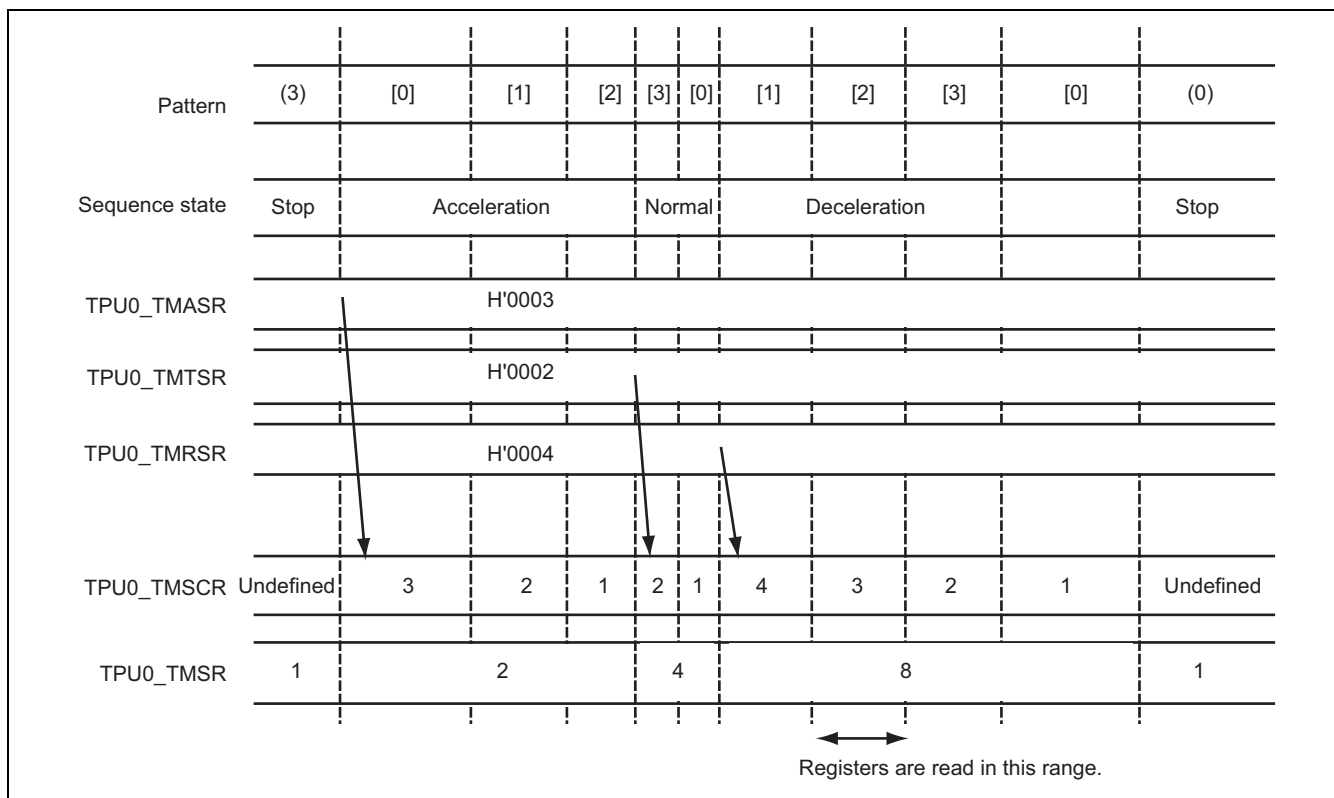
#### (f) Detecting the Transition to the Stop State

Setting the TMS1ES bit in TPU0\_TIER0 to 1 enables detection of the transition to the stop state. The handler should clear the TMCFS flag of TPU0\_TSR0 by writing 0 to the bit after having read it as 1.

**(8) Checking the State of Operation**

Read TPU0\_TMSR and TPU0\_TMSCR to check the current state of operations. TPU0\_TMSCR indicates the value resulting from decrementation (on every compare match with the timer counter) from the values in the number of steps register (TPU0\_TMASR, TPU0\_TMTSR, or TPU0\_TMRSR) during sequence transitions.

Figure 56.23 shows how the values in TPU0\_TMSR and TPU0\_TMSCR vary through the four states. As is shown in the figure, the current step within the overall sequence of state transitions can be estimated by, for example, reading TPU0\_TMSR = H'0008 and TPU0\_TMSCR = H'0003 in the interval indicated in the figure below.



**Figure 56.23 Values of TPU0\_TMSR and TPU0\_TMSCR**



# 57A. Compare Match Timer 0 (CMT0)

RZ/G1H	RZ/G1N
RZ/G1M	RZ/G1E

## 57A.1 Features

- Two channels
- 16 bits/32 bits can be selected as counter size (bit-width).
- Provided with 32-bit constant registers and 32-bit up counters that can be written or read at any time.
- Following four clocks can be selected as counter clocks:
  - RCLK: 1/1, 1/8, 1/32, and 1/128
- One-shot operation or free-running operation is selectable.
- Compare match or overflow can be selected as interrupt source.
- Counter operation can be enabled or disabled at the time of debugging of CPU core using the debugging mode operation selector.

Figure 57A.1 shows a block diagram of the CMT0.

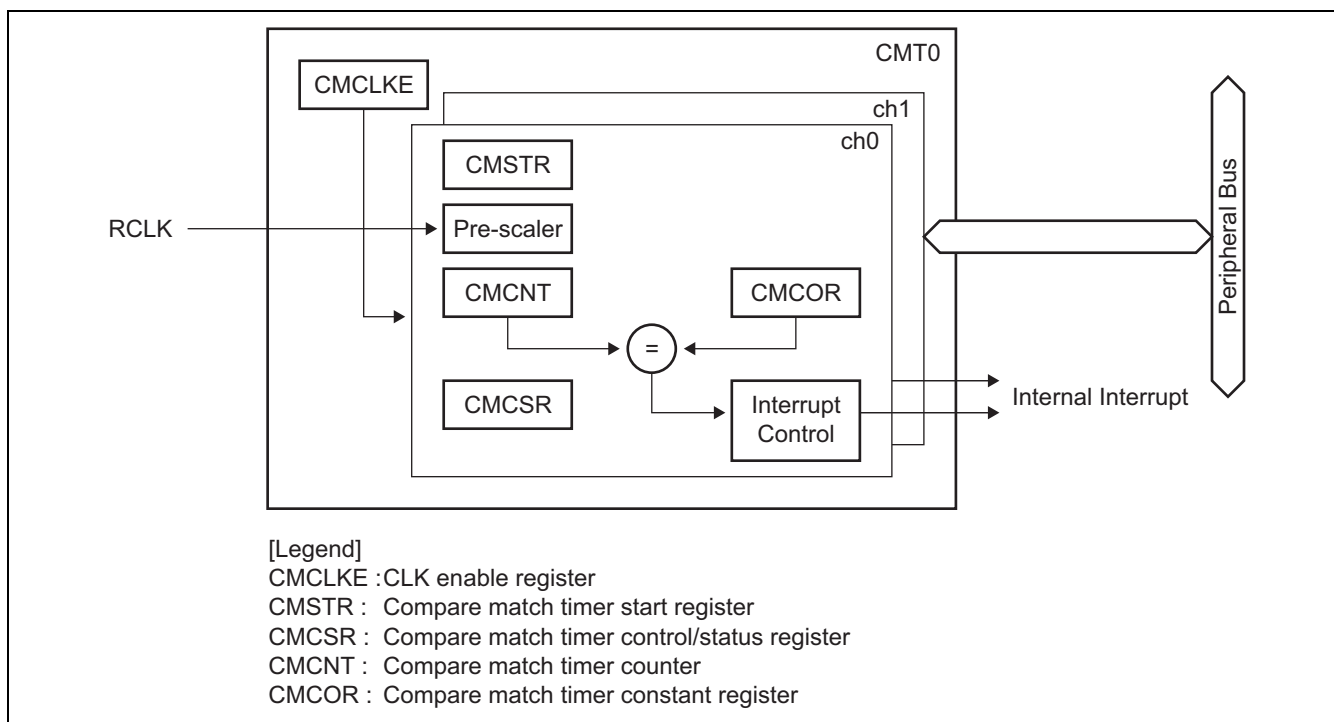


Figure 57A.1 Block Diagram of CMT0

## 57A.2 Register Descriptions

Table 57A.1 shows the CMT0 register configuration. Table 57A.2 shows the register states in each operating mode.

**Table 57A.1 Register Configuration**

Register Name	Abbreviation	R/W	Address	Access Size	RZ/G Series Products			
					RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
CLK enable register	CMCLKE	R/W	H'FFCA 1000	32	√	√	√	√
Compare match timer start register 0	CMSTR0	R/W	H'FFCA 0500	32	√	√	√	√
Compare match timer control/status register 0	CMCSR0	R/W	H'FFCA 0510	32	√	√	√	√
Compare match timer counter 0	CMCNT0	R/W	H'FFCA 0514	32	√	√	√	√
Compare match timer constant register 0	CMCOR0	R/W	H'FFCA 0518	32	√	√	√	√
Compare match timer start register 1	CMSTR1	R/W	H'FFCA 0600	32	√	√	√	√
Compare match timer control/status register 1	CMCSR1	R/W	H'FFCA 0610	32	√	√	√	√
Compare match timer counter 1	CMCNT1	R/W	H'FFCA 0614	32	√	√	√	√
Compare match timer constant register 1	CMCOR1	R/W	H'FFCA 0618	32	√	√	√	√

**Table 57A.2 Register States in Each Operating Mode**

Register Abbreviation	Power-On Reset	Module Standby
CMCLKE	Initialized	Retained
CMSTR0	Initialized	Retained
CMCSR0	Initialized	Retained
CMCNT0	Initialized	Retained
CMCOR0	Initialized	Retained
CMSTR1	Initialized	Retained
CMCSR1	Initialized	Retained
CMCNT1	Initialized	Retained
CMCOR1	Initialized	Retained

### 57A.2.1 CLK Enable Register (CMCLKE)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CMCLKE is a 32-bit register, which specifies clock supply to each channel. When there are unused channels, set 0 to this register, for stop supplying clock to the channel. It is prohibited to stop clock supply, while counter is working.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	Ch1 clke	Ch0 clke	—	—	—	—	—
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R	R	R	R	R	R	R	R	R	R/W	R/W	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 7	—	All 1	R	Reserved These bits are always read as 1. The write value should always be 1.
6	Ch1clke	1	R/W	0: Clock isn't supplied to ch1. 1: Clock is supplied to ch1.
5	Ch0clke	1	R/W	0: Clock isn't supplied to ch0. 1: Clock is supplied to ch0.
4 to 0	—	All 1	R	Reserved These bits are always read as 1. The write value should always be 1.

**57A.2.2 Compare Match Timer Start Registers 0 and 1 (CMSTR0, CMSTR1)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CMSTRn (n = 0/1) is a 32-bit register which specifies the operation of compare match timer counters (CMCNTn).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	STR0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	STR0	1	R/W	Count Start These bits specify start/halt of compare match timer counter (CMCNTn). 0: CMCNTn halts 1: CMCNTn starts counting

### 57A.2.3 Compare Match Timer Control/Status Registers 0 and 1 (CMCSR0, CMCSR1)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CMCSRn (n = 0/1) is a 32-bit register that indicates the occurrence of compare matches, enables interrupts, and sets the counter input clocks.

Do not change bits other than the CMF and OVF bits, while compare match timer counter (CMCNTn) is under counting.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CMF	OVF	WRFLG	—	—	—	CMS	CMM	—	—	CMR[1:0]	DBGIV D	CKS[2:0]			
Initial value:	0	0	0	0	0	0	0	1	0	0	0	0	1	1	1	1
R/W:	R/(W)	R/(W)	R	R	R	R	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15	CMF	0	R/(W)	Compare Match Flag This flag indicates whether values of the compare match timer counter (CMCNTn) and compare match timer constant register (CMCORn) have matched or not. Software cannot write 1 to the bit. When one-shot is selected for the counter operation, counting resumes by clearing this bit. 0: CMCNTn and CMCORn values have not matched. [Clearing condition] Write 0 to CMF 1: CMCNTn and CMCORn values have matched. Note: Only 0 can be written to clear the flag.
14	OVF	0	R/(W)	Overflow Flag This flag indicates whether the compare match timer counter (CMCNTn) has overflowed or not. Software cannot write 1 to this bit. 0: CMCNTn has not overflowed. [Clearing condition] Write 0 to OVF 1: CMCNTn has overflowed. Note: Only 0 can be written to clear the flag.
13	WRFLG	0	R	Write State Flag Write access to CMCNTn is prohibited, while this bit is 1. Further behavior is not guaranteed, if data is written while this bit is 1. This bit indicates CMCNTn is in synchronization period for setting previously written data. Confirm that this flag is 0, before writing to CMCNTn.

Bit	Bit Name	Initial Value	R/W	Description
12 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9	CMS	0	R/W	Compare Match Timer Counter Size Specify whether the compare match timer counter (CMCNTn) is used as a 16-bit counter or a 32-bit counter. This bit specifies the valid size of compare match timer constant register (CMCORn). 0: Operates as a 32-bit counter. 1: Operates as a 16-bit counter. Note: Refer to section 57A.3.5, CMT0 Register Access, for the note regarding writing to or reading from this bit.
8	CMM	1	R/W	Compare Match Mode Specify counter operation mode. 0: One-shot operation 1: Free-running operation Note: Refer to section 57A.3.5, CMT0 Register Access, for the note regarding writing to or reading from this bit.
7, 6	—	All 0	R	Reserved This bit is always read as 0. The write value should always be 0.
5, 4	CMR[1:0]	00	R/W	Compare Match Request These bits enable or disable an internal interrupt request in a compare match. 00: Disables an internal interrupt request. 01: Setting prohibited 10: Enables an internal interrupt request. 11: Setting prohibited Note: Refer to section 57A.3.5, CMT0 Register Access, for the note regarding writing to or reading from this bit.
3	DBGIVD	1	R/W	Debug Mode Operation Select Sets the counter operation in debug mode. 0: Stops the counter operation in debug mode. 1: Enables the counter operation even in debug mode. Note: Refer to section 57A.3.5, CMT0 Register Access, for the note regarding writing to or reading from this bit.

Bit	Bit Name	Initial Value	R/W	Description
2 to 0	CKS[2:0]	111	R/W	<p>Clock Select</p> <p>These bits select the input clock to CMCNTn. When the count start bit (STRO) in CMSTRn is set to 1, CMCNTn begins incrementing with the clock selected by these bits.</p> <p>000: Setting prohibited                      001: Setting prohibited                      010: Setting prohibited                      011: Setting prohibited                      100: RCLK/8                      101: RCLK/32                      110: RCLK/128                      111: RCLK/1</p> <p>Note: Refer to section 57A.3.5, CMT0 Register Access, for the note regarding writing to or reading from this bit.</p>

**57A.2.4 Compare Match Timer Counters 0 and 1 (CMCNT0, CMCNT1)**

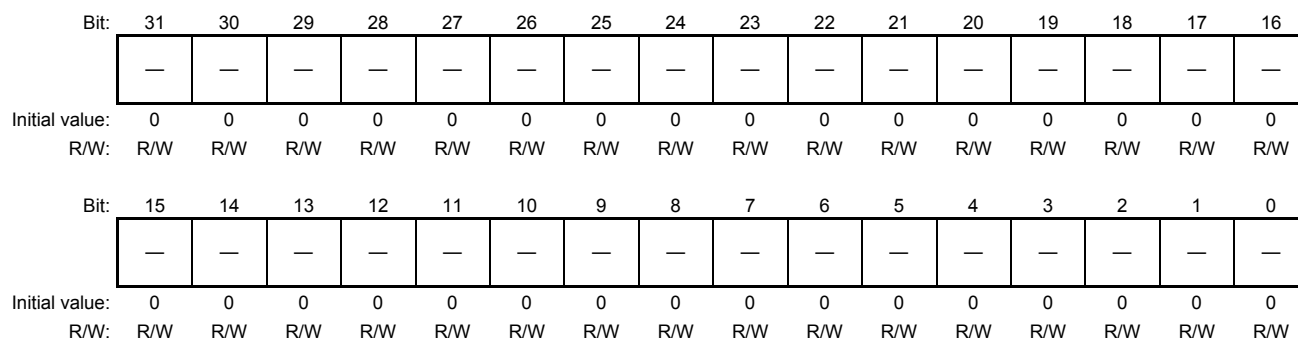
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CMCNTn (n = 0 to 1) is a 32-bit register that is used as an up-counter.

To specify counter operation, set compare match timer control/status register n (CMCSRn), before starting operation of corresponding channel.

When the 16-bit counter operation is selected by the CMS bit, bits 31 to 16 of this register become invalid. When data is written to this register in 16-bit mode, write H'0000 to the upper 16 bits.

When CMCNTn is read during the counter operation, the read value may be wrong because different clock is used between counter and bus-interface. For exact value, read this register continuously, until same values are read from this register.



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	—	All 0	R/W	<p>Compare match timer counter bit31 to 0</p> <p>Note: Refer to section 57A.3.5, CMT0 Register Access, for the note regarding writing to or reading from this bit.</p>

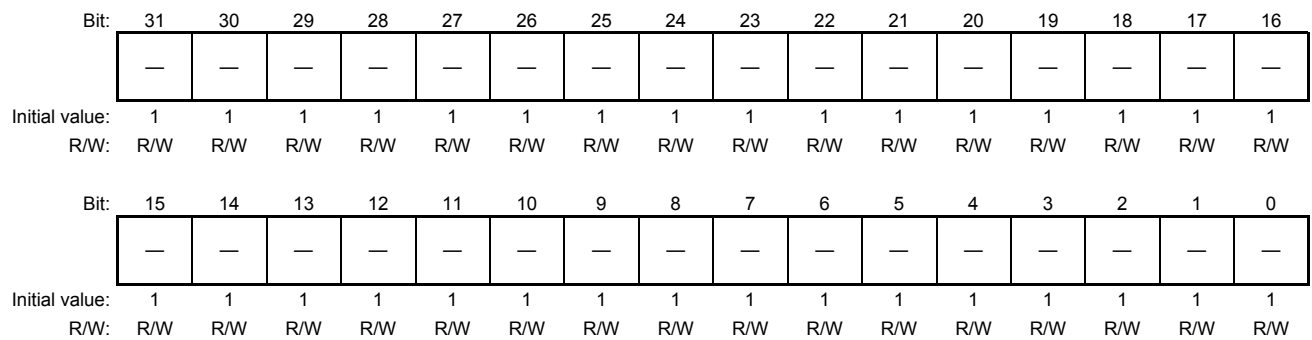
**57A.2.5 Compare Match Timer Constant Registers 0 and 1 (CMCOR0, CMCOR1)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CMCORn (n = 0/1) is a 32-bit register that sets the compare match period with CMCNTn.

When the 16-bit counter operation is selected by the CMS bit in CMCSRn, bits 15 to 0 of this register become valid. Write H'0000 to upper 16bits in 16-bit counter operation.

An overflow is detected when CMCNTn is cleared to 0 and this register is H'FFFFFFFF.



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	—	All 1	R/W	Compare match timer constant register bit31 to 0 Note: Refer to section 57A.3.5, CMT0 Register Access, for the note regarding writing to or reading from this bit.



RZ/G1H	RZ/G1N
RZ/G1M	RZ/G1E

### 57A.3 Operation

#### 57A.3.1 Counter Operation

The CMT0 starts the operation of the counter by writing 1 to the STR0 bit in CMSTRn after each register has been set. Complete all of the settings before starting the operation. Do not change the register settings other than clearing flag bits, during the compare match timer n (CMCNTn) is under operation.

The counter operates in one of two ways.

- One-Shot Operation

One-shot operation is selected by setting the CMM bit in CMCSRn to 0. When the value in CMCNTn matches the value in CMCORn, the value in CMCNTn is cleared to H'00000000 and the CMF bit in CMCSRn is set to 1. Counting by CMCNTn stops after it has been cleared.

To detect an overflow interrupt, set the value in CMCORn to H'FFFFFFFF. When the value in CMCNTn matches the value in CMCORn, CMCNTn is cleared to H'00000000 and the CMF and OVF bits in CMCSRn are set to 1.

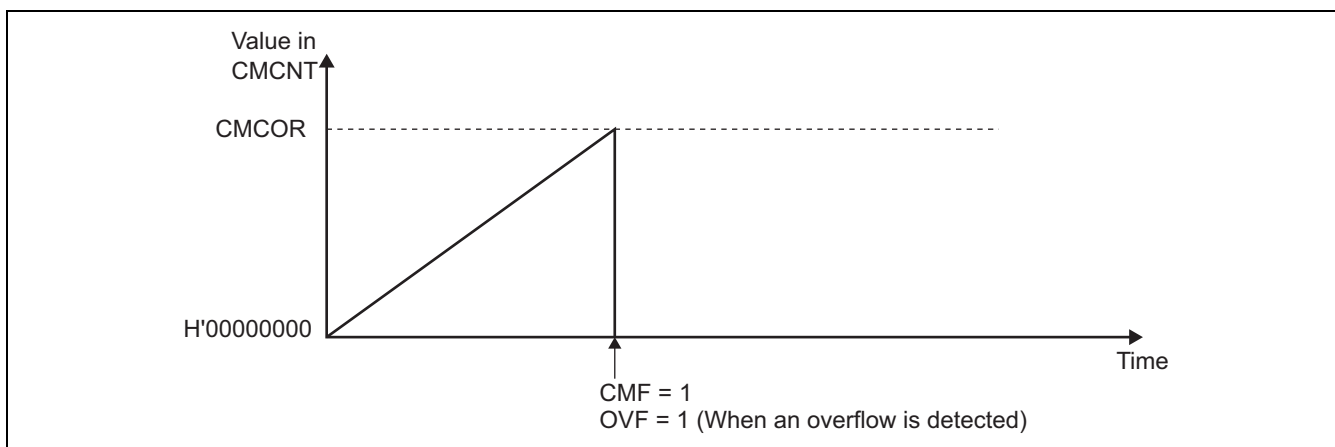


Figure 57A.2 Counter Operation (One-Shot Operation)

- Free-Running Operation

Free-running operation is selected by setting the CMM bit in CMCSRn to 1. When the value in CMCNTn matches the value in CMCORn, CMCNTn is cleared to H'00000000 and the CMF bit in CMCSRn is set to 1. CMCNTn resumes counting-up after it has been cleared.

To detect an overflow interrupt, set CMCORn to H'FFFFFFF. When the values in CMCNTn and CMCORn match, CMCNTn is cleared to H'00000000 and the CMF and OVF bits in CMCSRn are set to 1.

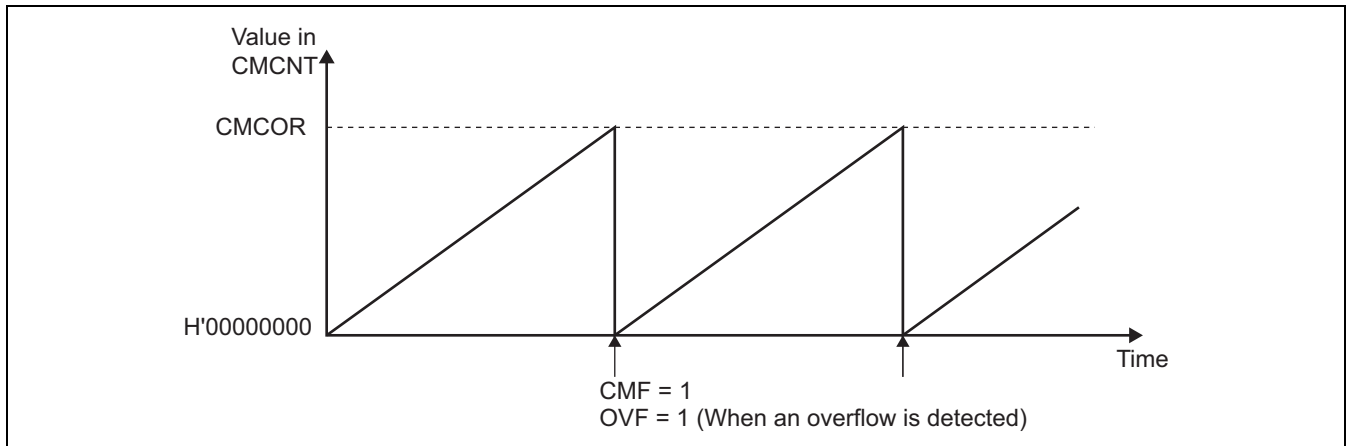


Figure 57A.3 Counter Operation (Free-Running Operation)

### 57A.3.2 Counter Size

In this module, the size of the counter can be selected from 16, or 32 bits. This is selected by the CMS bit in CMCSRn.

When the 16-bit size is selected, H'0000 should be used as upper 16 bits of write data to CMCORn. To detect an overflow interrupt, CMCORn must be set to H'0000FFFF.

### 57A.3.3 Timing for Counting by CMCNTn

In this module, the clock for the counter can be selected from among the following:

- RCLK: 1/1, 1/8, 1/32, and 1/128

The clock for the counter is selected by the CKS bits in CMCSRn. CMCNTn is incremented at the rising edge of the selected clock.

### 57A.3.4 Internal Interrupt Request to CPU

By CMR bits in CMCSRn, internal interrupt request to the CPU at a compare match can be asserted.

To clear the internal interrupt request to the CPU, the CMF bit should be set to 0. Set the CMF bit to 0 in the handling routine for the CMT0 interrupt.

### 57A.3.5 CMT0 Register Access

After writing to following registers, written data can be read after writing has finished. However, it takes 2 cycles in counter input clock (RCLK), for reflecting written data to counter behavior.

CMCSRn: Bits CKS, CMM, CMS, CMR, DBGIVD

CMCORn: Bits 31 to 0

CMSTRn: Bit STR0

After writing to following registers, written data can be read after writing has finished. However, it takes 2 cycles in counter input clock (RCLK), for reflecting written data to counter behavior.

And for following registers, write access is prohibited, while previously written data is under writing. Do not perform next write access, while CMCSRn.WRFLG is 1.

CMCNT\*: Bits 31 to 0

### 57A.3.6 Compare Match Flag Set/Clear Timing

The CMF bit in CMCSRn is set to 1 by the compare match signal generated when CMCORn and CMCNTn match. The compare match signal is generated upon the final state of the match (timing at which the CMCNTn value is updated to 0). Consequently, after CMCORn and CMCNTn match, a compare match signal will not be generated until a CMCNTn counter clock is input. Figure 57A.4 shows the set timing of the CMF bit.

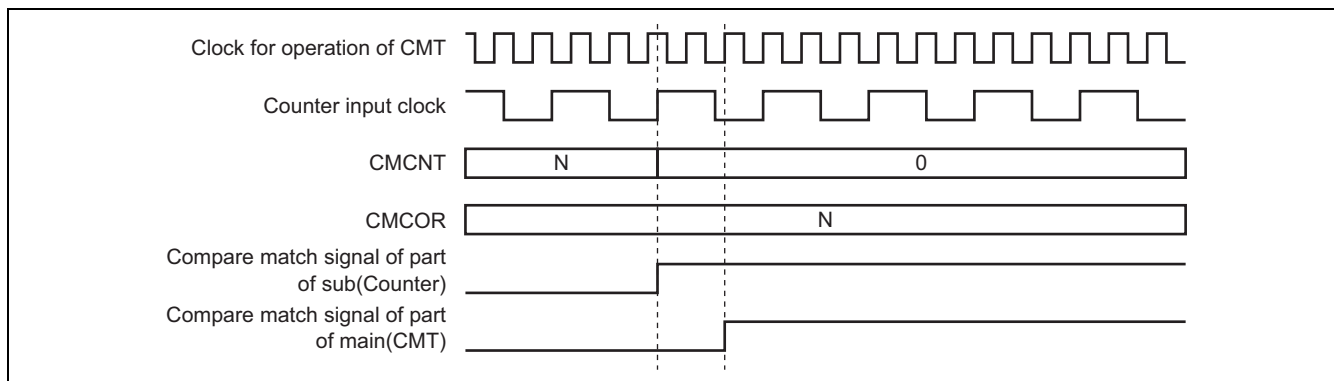


Figure 57A.4 CMF Set Timing

Set the CMF bit as 0. The CMF flag is cleared immediately.

### 57A.3.7 CMT0 Usage

Take the following steps to use the CMT0.

1. Clear the STR0 bit in CMSTRn to 0 to temporarily stop counting.  
(Confirm that RCLK was input more than 2 cycles.)
2. Write H'00000000 on CMCNTn.
3. Set counter size, compare match mode, type of counter clock and interrupt request and clear the bit of OVF and CMF in CMCSRn.
4. Set the value on CMCORn.
5. Confirm that CMCSRn.WRFLG is 0.  
If WRFLG is 1, wait until it'll be 0.
6. Start the counting by setting the STR0 bit in CMSTRn to 1.  
(Refer to section 57A.3.5, CMT0 Register Access)

### 57A.3.8 Module Stop/ CMCLKE Setting

When counter is not used, clock of this module can be stopped by CMCLKE register. Please confirm that, following conditions are satisfied, before stopping counter's clock.

- CMSTRn.STR0 bit is 0
- CMCSRn.WRFLG is 0
- 3 or more cycles have passed in RCLK, since the last Register access

## 57B. Compare Match Timer 1 (CMT1)

RZ/G1H	RZ/G1N
RZ/G1M	RZ/G1E

### 57B.1 Features

- Eight channels
- 16 bits/32 bits/48 bits can be selected as counter size (bit-width).
- 48-bit constant registers and 48-bit up counters that can be written or read at any time.
- For channel 0 to 4, following twelve clocks can be selected as counter clock.
  - CP $\phi$  (CPEX $\phi$ )\*: 1/8, 1/32, 1/128, and 1/1
    - Note: Clock name CP $\phi$  is for RZ/G1H, M and N, CPEX $\phi$  is for RZ/G1E; Both CP $\phi$  and CPEX $\phi$  are divided-by-2 of the EXTAL clock.
  - RCLK: 1/1, 1/8, 1/32, and 1/128
  - Pseudo 32 kHz: 1/1, 1/8, 1/32, and 1/128
- For channel 5 to 7, following four clocks can be selected as counter clock.
  - RCLK: 1/1, 1/8, 1/32, and 1/128
- One-shot operation or free-running operations are selectable.
- Compare match can be used as interrupt source.
- Support Module standby mode.
- RCLK-synchronous counter start/stop mode for channel 0
- Counter operation can be enabled or disabled at the time of debugging of CPU core using the debugging mode operation selector.

Figure 57B.1 shows a block diagram of the CMT1.

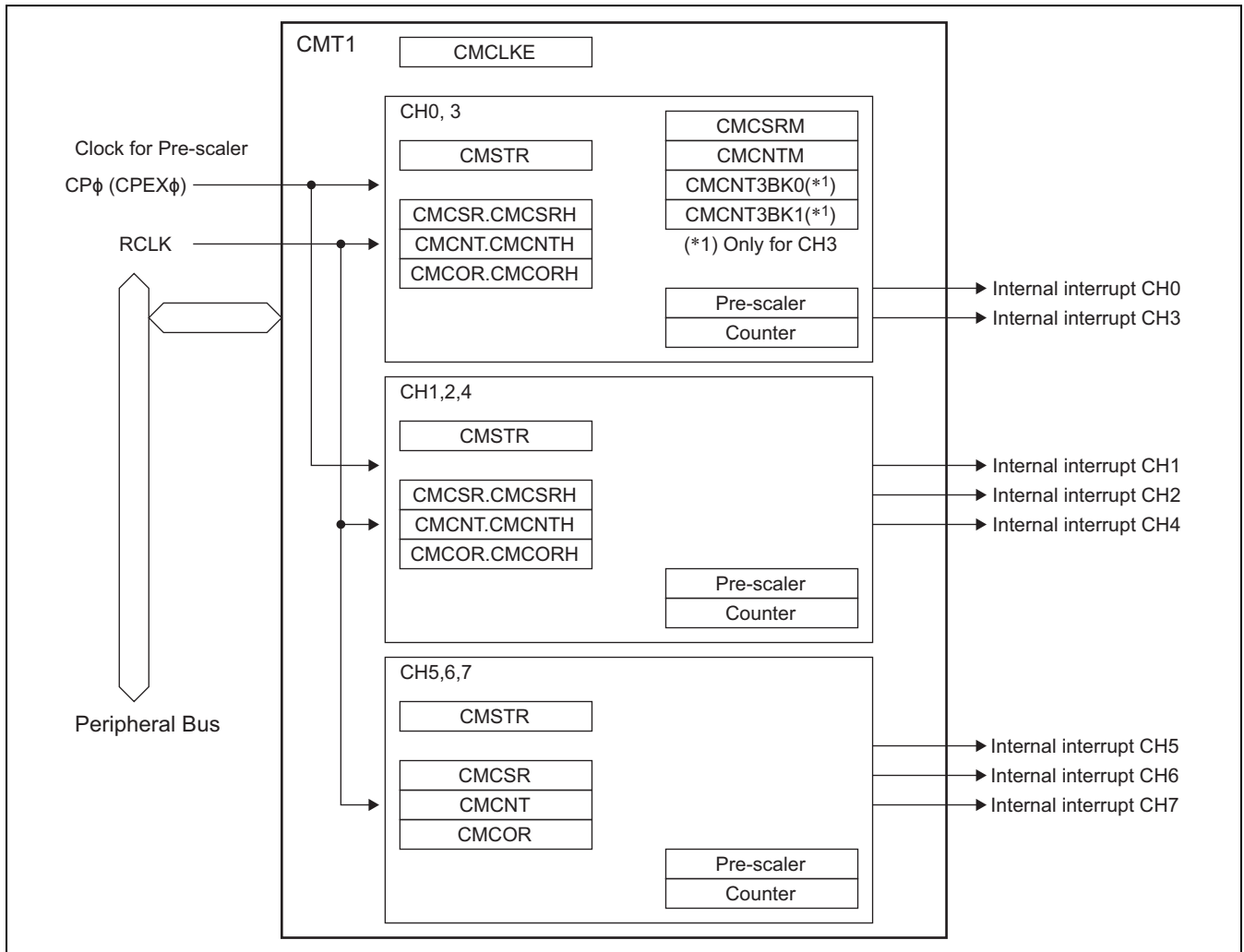


Figure 57B.1 Block Diagram of CMT1

## 57B.2 Register Descriptions

Table 57B.1 shows the CMT1 register configuration. Table 57B.2 shows the register states in each operating mode.

**Table 57B.1 Register Configuration**

Register Name	Abbreviation	R/W	Address	Access Size	RZ/G Series Products			
					RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
CLK enable register	CMCLKE	R/W	H'E613 1000	32	√	√	√	√
Compare match timer start register 0	CMSTR0	R/W	H'E613 0000	32	√	√	√	√
Compare match timer control/status register 0	CMCSR0	R/W	H'E613 0010	32	√	√	√	√
Compare match timer counter 0	CMCNT0	R/W	H'E613 0014	32	√	√	√	√
Compare match timer constant register 0	CMCOR0	R/W	H'E613 0018	32	√	√	√	√
Compare match timer control/status register H0	CMCSRH0	R/W	H'E613 0020	32	√	√	√	√
Compare match timer counter H0	CMCNTH0	R/W	H'E613 0024	32	√	√	√	√
Compare match timer constant register H0	CMCORH0	R/W	H'E613 0028	32	√	√	√	√
Compare match timer match control/status register 0	CMCSRM0	R/W	H'E613 0040	32	√	√	√	√
Compare match timer match counter 0	CMCNTM0	R	H'E613 0044	32	√	√	√	√
Compare match timer start register 1	CMSTR1	R/W	H'E613 0100	32	√	√	√	√
Compare match timer control/status register 1	CMCSR1	R/W	H'E613 0110	32	√	√	√	√
Compare match timer counter 1	CMCNT1	R/W	H'E613 0114	32	√	√	√	√
Compare match timer constant register 1	CMCOR1	R/W	H'E613 0118	32	√	√	√	√
Compare match timer control/status register H1	CMCSRH1	R/W	H'E613 0120	32	√	√	√	√
Compare match timer counter H1	CMCNTH1	R/W	H'E613 0124	32	√	√	√	√
Compare match timer constant register H1	CMCORH1	R/W	H'E613 0128	32	√	√	√	√
Compare match timer start register 2	CMSTR2	R/W	H'E613 0200	32	√	√	√	√
Compare match timer control/status register 2	CMCSR2	R/W	H'E613 0210	32	√	√	√	√
Compare match timer counter 2	CMCNT2	R/W	H'E613 0214	32	√	√	√	√
Compare match timer constant register 2	CMCOR2	R/W	H'E613 0218	32	√	√	√	√
Compare match timer control/status register H2	CMCSRH2	R/W	H'E613 0220	32	√	√	√	√
Compare match timer counter H2	CMCNTH2	R/W	H'E613 0224	32	√	√	√	√
Compare match timer constant register H2	CMCORH2	R/W	H'E6130228	32	√	√	√	√
Compare match timer start register 3	CMSTR3	R/W	H'E613 0300	32	√	√	√	√

Register Name	Abbreviation	R/W	Address	Access Size	RZ/G Series Products			
					RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Compare match timer control/status register 3	CMCSR3	R/W	H'E613 0310	32	√	√	√	√
Compare match timer counter 3	CMCNT3	R/W	H'E613 0314	32	√	√	√	√
Compare match timer constant register 3	CMCOR3	R/W	H'E613 0318	32	√	√	√	√
Compare match timer control/status register H3	CMCSRH3	R/W	H'E613 0320	32	√	√	√	√
Compare match timer counter H3	CMCNTH3	R/W	H'E613 0324	32	√	√	√	√
Compare match timer constant register H3	CMCORH3	R/W	H'E6130328	32	√	√	√	√
Compare match timer counter 3 backup 0	CMCNT3BK0	R	H'E613 0330	32	√	√	√	√
Compare match timer counter 3 backup 1	CMCNT3BK1	R	H'E613 0334	32	√	√	√	√
Compare match timer match control/status register 3	CMCSR3M3	R/W	H'E613 0340	32	√	√	√	√
Compare match timer match counter 3	CMCNTM3	R	H'E613 0344	32	√	√	√	√
Compare match timer start register 4	CMSTR4	R/W	H'E613 0400	32	√	√	√	√
Compare match timer control/status register 4	CMCSR4	R/W	H'E613 0410	32	√	√	√	√
Compare match timer counter 4	CMCNT4	R/W	H'E613 0414	32	√	√	√	√
Compare match timer constant register 4	CMCOR4	R/W	H'E613 0418	32	√	√	√	√
Compare match timer control/status register H4	CMCSRH4	R/W	H'E613 0420	32	√	√	√	√
Compare match timer counter H4	CMCNTH4	R/W	H'E613 0424	32	√	√	√	√
Compare match timer constant register H4	CMCORH4	R/W	H'E613 0428	32	√	√	√	√
Compare match timer start register 5	CMSTR5	R/W	H'E613 0500	32	√	√	√	√
Compare match timer control/status register 5	CMCSR5	R/W	H'E613 0510	32	√	√	√	√
Compare match timer counter 5	CMCNT5	R/W	H'E613 0514	32	√	√	√	√
Compare match timer constant register 5	CMCOR5	R/W	H'E613 0518	32	√	√	√	√
Compare match timer start register 6	CMSTR6	R/W	H'E613 0600	32	√	√	√	√
Compare match timer control/status register 6	CMCSR6	R/W	H'E613 0610	32	√	√	√	√
Compare match timer counter 6	CMCNT6	R/W	H'E613 0614	32	√	√	√	√
Compare match timer constant register 6	CMCOR6	R/W	H'E613 0618	32	√	√	√	√
Compare match timer start register 7	CMSTR7	R/W	H'E613 0700	32	√	√	√	√
Compare match timer control/status register 7	CMCSR7	R/W	H'E613 0710	32	√	√	√	√
Compare match timer counter 7	CMCNT7	R/W	H'E613 0714	32	√	√	√	√



Register Name	Abbreviation	R/W	Address	Access Size	RZ/G Series Products			
					RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Compare match timer constant register 7	CMCOR7	R/W	H'E613 0718	32	√	√	√	√

Table 57B.2 Register States in Each Operating Mode

Register Abbreviation	Power-On Reset	Module Standby
CMCLKE	Initialized	Retained
CMSTR0	Initialized	Retained
CMCSR0	Initialized	Retained
CMCNT0	Initialized	Retained
CMCOR0	Initialized	Retained
CMCSRH0	Initialized	Retained
CMCNTH0	Initialized	Retained
CMCORH0	Initialized	Retained
CMCSR0M0	Initialized	Retained
CMCNTM0	Initialized	Retained
CMSTR1	Initialized	Retained
CMCSR1	Initialized	Retained
CMCNT1	Initialized	Retained
CMCOR1	Initialized	Retained
CMCSRH1	Initialized	Retained
CMCNTH1	Initialized	Retained
CMCORH1	Initialized	Retained
CMSTR2	Initialized	Retained
CMCSR2	Initialized	Retained
CMCNT2	Initialized	Retained
CMCOR2	Initialized	Retained
CMCSRH2	Initialized	Retained
CMCNTH2	Initialized	Retained
CMCORH2	Initialized	Retained
CMSTR3	Initialized	Retained
CMCSR3	Initialized	Retained
CMCNT3	Initialized	Retained
CMCOR3	Initialized	Retained
CMCSRH3	Initialized	Retained
CMCNTH3	Initialized	Retained
CMCORH3	Initialized	Retained
CMCNT3BK0	Initialized	Retained
CMCNT3BK1	Initialized	Retained
CMCSR0M3	Initialized	Retained

<b>Register Abbreviation</b>	<b>Power-On Reset</b>	<b>Module Standby</b>
CMCNTM3	Initialized	Retained
CMSTR4	Initialized	Retained
CMCSR4	Initialized	Retained
CMCNT4	Initialized	Retained
CMCOR4	Initialized	Retained
CMCSRH4	Initialized	Retained
CMCNTH4	Initialized	Retained
CMCORH4	Initialized	Retained
CMSTR5	Initialized	Retained
CMCSR5	Initialized	Retained
CMCNT5	Initialized	Retained
CMCOR5	Initialized	Retained
CMSTR6	Initialized	Retained
CMCSR6	Initialized	Retained
CMCNT6	Initialized	Retained
CMCOR6	Initialized	Retained
CMSTR7	Initialized	Retained
CMCSR7	Initialized	Retained
CMCNT7	Initialized	Retained
CMCOR7	Initialized	Retained

### 57B.2.1 CLK Enable Register (CMCLKE)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CMCLKE is a 32bits register, which specify clock supply to each channel. When there are unused channels, set '0' as this register, to stop supplying clock to the channel. It is prohibited to stop clock supply, while counter is working.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	Ch7 clke	Ch6 clke	Ch5 clke	Ch4 clke	Ch3 clke	Ch2 clke	Ch1 clke	Ch0 clke
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 8	—	All 1	R	Reserved These bits are always read as 1. The write value should always be 1.
7	Ch7clke	1	R/W	0: Clock isn't supplied to ch7 1: Clock is supplied to ch7
6	Ch6clke	1	R/W	0: Clock isn't supplied to ch6 1: Clock is supplied to ch6
5	Ch5clke	1	R/W	0: Clock isn't supplied to ch5 1: Clock is supplied to ch5
4	Ch4clke	1	R/W	0: Clock isn't supplied to ch4 1: Clock is supplied to ch4
3	Ch3clke	1	R/W	0: Clock isn't supplied to ch3 1: Clock is supplied to ch3
2	Ch2clke	1	R/W	0: Clock isn't supplied to ch2 1: Clock is supplied to ch2
1	Ch1clke	1	R/W	0: Clock isn't supplied to ch1 1: Clock is supplied to ch1
0	Ch0clke	1	R/W	0: Clock isn't supplied to ch0 1: Clock is supplied to ch0

### 57B.2.2 Compare Match Timer Start Registers 0 to 7 (CMSTRn)

CMSTRn (n = 0 to 7) is a 32-bit register which specify the operation of compare match timer counter (CMCNTn). Refer to section 57B.3.5, Register Access, for register value update timing.

#### (1) CMSTR0

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	STRORS	—	—	—	—	—	—	—	STR0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	STRORS	0	R/W	RCLK-Synchronous Counter Start/Stop Mode Select 0: Normal operation Channel 0 starts or stops counting, immediately after data is written to STR0. 1: RCLK-synchronous counter start/stop mode Channel 0 starts or stops counting on detecting an RCLK rising edge, after data is written to STR0.
7 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	STR0	0	R/W	Count Start 0 These bits specify start/halt of compare match timer counter 0 (CMCNT0). 0: CMCNT0 halts 1: CMCNT0 start counting

(2) CMSTRn (n = 1 to 4)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	STR0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	STR0	0	R/W	Count Start 0 These bits specify start/halt of compare match timer counter (CMCNTn). 0: CMCNTn halts 1: CMCNTn starts counting

**(3) CMSTRn (n = 5 to 7)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	STR0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	STR0	1	R/W	Count Start 0 These bits specify start/halt of compare match timer counter (CMCNTn). 0: CMCNTn halts 1: CMCNTn starts counting

### 57B.2.3 Compare Match Timer Control/Status Registers 0 to 7 (CMCSRn)

CMCSRn (n = 0 to 7) is a 32-bit register that indicates the occurrence of compare match, enable interrupt and set the counter input clock.

Do not change bits other than the CMF and OVF bits, while compare match timer counter (CMCNTn) is under counting.

#### (1) CMCSR0

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CMF	OVF	WRFLG	CH0STTF	CH0STPF	CH0STPF	CMS	CMM	—	—	CMR[1:0]	DBGIVD	CKS[2:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
R/W:	R/(W)	R/(W)	R	R/(W)	R/(W)	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15	CMF	0	R/(W)	Compare Match Flag This flag indicates whether values of the compare match timer counter (CMCNT0) and compare match timer constant register (CMCOR0) have matched or not. Software cannot write 1 to the bit. When one-shot is selected for the counter operation, counting resumes by clearing this bit. 0: CMCNT0 and CMCOR0 values have not matched [Clearing conditions] • Write 0 to this bit 1: CMCNT0 and CMCOR0 values have matched Note: Only 0 can be written to clear the flag.
14	OVF	0	R/(W)	Overflow Flag This flag indicates whether the compare match timer counter (CMCNT0) has overflowed or not. Software cannot write 1 to this bit. 0: CMCNT0 has not overflowed [Clearing conditions] • Write 0 to this bit 1: CMCNT0 has overflowed Note: Only 0 can be written to clear the flag.

Bit	Bit Name	Initial Value	R/W	Description
13	WRFLG	0	R	<p>Write State Flag</p> <p>Write access to CMCNT0 is prohibited, while this bit is 1. Further behavior is not guaranteed, if data is written while this bit is 1.</p> <p>This bit indicates CMCNT0 is in synchronization period for setting previously written data.</p> <p>Confirm that this flag is 0, before writing to CMCNT0.</p>
12	CH0STTF	0	R/(W)	<p>Channel 0 Start Flag</p> <p>When RCLK-synchronous channel 0 counter start/stop mode is selected, this flag indicates whether the counter in channel 0 started on detecting an RCLK rising edge after 1 was written to the STR0 bit in CMSR.</p> <p>0: Channel 0 counter has not started.</p> <p>[Clearing condition]</p> <ul style="list-style-type: none"> <li>Write 0 to CH0STTF.</li> </ul> <p>1: Channel 0 counter has started.</p> <p>Note: Only 0 can be written to clear the flag.</p>
11	CH0STPF	0	R/(W)	<p>Channel 0 Stop Flag</p> <p>When RCLK-synchronous channel 0 counter start/stop mode is selected, this flag indicates whether the counter in channel 0 stopped on detecting an RCLK rising edge after 1 was written to the STR0 bit in CMSR.</p> <p>0: Channel 0 counter has not stopped.</p> <p>[Clearing condition]</p> <ul style="list-style-type: none"> <li>Write 0 to CH0STPF.</li> </ul> <p>1: Channel 0 counter has stopped.</p> <p>Note: Only 0 can be written to clear the flag.</p>
10	CH0SSIE	0	R/W	<p>Channel 0 Start/Stop Interrupt Enable</p> <p>When RCLK-synchronous channel 0 counter start/stop mode is selected, this bit enables or disables an interrupt due to the start or stop of the counter in channel 0.</p> <p>0: Disables an interrupt due to start or stop of channel 0 counter.</p> <p>1: Enables an interrupt due to start or stop of channel 0 counter.</p>
9	CMS	0	R/W	<p>Compare Match Timer Counter Size</p> <p>This bit and CMCSRH0.CMSH select whether the compare match timer counter 0 (CMCNTH0[15:0], and CMCNT0[31:0]) is used as a 16-bit counter, a 32-bit counter, or a 48-bit counter.</p> <p>This bit also specifies valid size of the compare match timer constant register 0 (CMCORH0[15:0], and CMCOR0[31:0]).</p> <p>CMCSRH0[9].CMSH, and CMCSR0[9].CMS:</p> <p>1x: Operates as a 48-bit counter</p> <p>00: Operates as a 32-bit counter</p> <p>01: Operates as a 16-bit counter</p>
8	CMM	0	R/W	<p>Compare Match Mode</p> <p>Specify operation mode of the counter.</p> <p>0: One-shot operation</p> <p>1: Free-running operation</p>
7	—	0	R	<p>Reserved</p> <p>This bit is always read as 0. The write value should always be 0.</p>



Bit	Bit Name	Initial Value	R/W	Description
6	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
5, 4	CMR[1:0]	00	R/W	Compare Match Request These bits enable or disable internal interrupt request in a compare match. 00: Disables internal interrupt request 01: Setting prohibited 10: Enables an internal interrupt request 11: Setting prohibited
3	DBGIVD	1	R/W	Debug Mode Operation Select Sets the counter operation in debugging mode. 0: Stops the counter operation in debugging mode. 1: Continues the counter operation even in debugging mode.
2 to 0	CKS[2:0]	111	R/W	Clock Select These bits and CMCSRH0.CKSH select the clock input to CMCNT0. When the count start bit (STR0) for the corresponding channel is set to 1, CMCNT0 begins incrementing with the clock selected by these bits. CMCSRH0.CKSH[0]+CMCSR0.CKS[2:0]: x000: CP $\phi$ (CPEX $\phi$ )/8 x001: CP $\phi$ (CPEX $\phi$ )/32 x010: CP $\phi$ (CPEX $\phi$ )/128 x011: CP $\phi$ (CPEX $\phi$ )/1 0100: RCLK/8 0101: RCLK/32 0110: RCLK/128 0111: RCLK/1 1100: Pseudo 32 kHz/8 1101: Pseudo 32 kHz/32 1110: Pseudo 32 kHz/128 1111: Pseudo 32 kHz/1

## (2) CMCSRn (n = 1 to 4)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CMF	OVF	WRFLG	—	—	—	CMS	CMM	—	—	CMR[1:0]	DBG IVD	CKS[2:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
R/W:	R/(W)	R/(W)	R	R	R	R	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15	CMF	0	R/(W)	Compare Match Flag This flag indicates whether values of the compare match timer counter (CMCNTn) and compare match timer constant register (CMCORn) have matched or not. Software cannot write 1 to the bit. When one-shot is selected for the counter operation, counting resumes by clearing this bit. 0: CMCNTn and CMCORn values have not matched [Clearing conditions] • Write 0 to this bit 1: CMCNTn and CMCORn values have matched Note: Only 0 can be written to clear the flag.
14	OVF	0	R/(W)	Overflow Flag This flag indicates whether the compare match timer counter (CMCNTn) has overflowed or not. Software cannot write 1 to this bit. 0: CMCNTn has not overflowed [Clearing conditions] • Write 0 to this bit 1: CMCNTn has overflowed Note: Only 0 can be written to clear the flag.
13	WRFLG	0	R	Write State Flag Write access to CMCNTn is prohibited, while this bit is 1. Further behavior is not guaranteed, if data is written while this bit is 1. This bit indicates CMCNTn is in synchronization period for setting previously written data. Confirm that this flag is 0, before writing to CMCNTn.
12 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
9	CMS	0	R/W	<p>Compare Match Timer Counter Size</p> <p>This bit and CMCSRn.CMSH specify whether the compare match timer counter (CMCNTHn[15:0] and CMCNTn[31:0]) is used as a 16-bit counter, a 32-bit counter, or a 48-bit counter.</p> <p>This setting becomes the valid size for the compare match timer constant register (CMCORHn[15:0], CMCORn[31:0]).</p> <p>CMCSRn[9].CMSH+CMCSRn[9].CMS:</p> <p>1x: Operates as a 48-bit counter 00: Operates as a 32-bit counter 01: Operates as a 16-bit counter</p>
8	CMM	0	R/W	<p>Compare Match Mode</p> <p>Specify counter operation mode.</p> <p>0: One-shot operation 1: Free-running operation</p>
7, 6	—	All 0	R	<p>Reserved</p> <p>This bit is always read as 0. The write value should always be 0.</p>
5, 4	CMR[1:0]	00	R/W	<p>Compare Match Request</p> <p>These bits enable or disable internal interrupt request in a compare match.</p> <p>00: Disables internal interrupt request 01: Setting prohibited 10: Enables an internal interrupt request 11: Setting prohibited</p>
3	DBGIVD	1	R/W	<p>Debug Mode Operation Select</p> <p>Sets the counter operation in debugging mode.</p> <p>0: Stops the counter operation in debugging mode. 1: Continues the counter operation even in debugging mode.</p>
2 to 0	CKS[2:0]	111	R/W	<p>Clock Select</p> <p>These bits and CMCSRn.CKSH specify the input clock to CMCNTn. When the count start bit (STR0) for the corresponding channel is set to 1, CMCNTn begins incrementing with the clock selected by these bits.</p> <p>CMCSRn.CKSH[0], CMCSRn.CKS[2:0]:</p> <p>x000: CP<math>\phi</math> (CPEX<math>\phi</math>)/8 x001: CP<math>\phi</math> (CPEX<math>\phi</math>)/32 x010: CP<math>\phi</math> (CPEX<math>\phi</math>)/128 x011: CP<math>\phi</math> (CPEX<math>\phi</math>)/1 0100: RCLK/8 0101: RCLK/32 0110: RCLK/128 0111: RCLK/1 1100: Pseudo 32 kHz/8 1101: Pseudo 32 kHz/32 1110: Pseudo 32 kHz/128 1111: Pseudo 32 kHz/1</p>

## (3) CMCSRn (n = 5 to 7)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CMF	OVF	WRFLG	—	—	—	CMS	CMM	—	—	CMR[1:0]	DBG IVD	CKS[2:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
R/W:	R/(W)	R/(W)	R	R	R	R	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15	CMF	0	R/(W)	Compare Match Flag This flag indicates whether values of the compare match timer counter (CMCNTn) and compare match timer constant register (CMCORn) have matched or not. Software cannot write 1 to the bit. When one-shot is selected for the counter operation, counting resumes by clearing this bit. 0: CMCNTn and CMCORn values have not matched [Clearing conditions] <ul style="list-style-type: none"> <li>Write 0 to this bit</li> </ul> 1: CMCNTn and CMCORn values have matched Note: Only 0 can be written to clear the flag.
14	OVF	0	R/(W)	Overflow Flag This flag indicates whether the compare match timer counter (CMCNTn) has overflowed or not. Software cannot write 1 to this bit. 0: CMCNTn has not overflowed [Clearing conditions] <ul style="list-style-type: none"> <li>Write 0 to this bit</li> </ul> 1: CMCNTn has overflowed Note: Only 0 can be written to clear the flag.
13	WRFLG	0	R	Write State Flag Write access to CMCNTn is prohibited, while this bit is 1. Further behavior is not guaranteed, if data is written while this bit is 1. This bit indicates CMCNTn is in synchronization period for setting previously written data. Confirm that this flag is 0, before writing to CMCNTn.
12 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
9	CMS	0	R/W	<p>Compare Match Timer Counter Size</p> <p>Selects whether the compare match timer counter (CMCNTn) is used as a 16-bit counter or a 32-bit counter.</p> <p>This setting becomes the valid size for the compare match timer constant register (CMCORn).</p> <p>0: Operates as a 32-bit counter.</p> <p>1: Operates as a 16-bit counter.</p>
8	CMM	1	R/W	<p>Compare Match Mode</p> <p>Specify counter operation mode.</p> <p>0: One-shot operation</p> <p>1: Free-running operation</p>
7, 6	—	All 0	R	<p>Reserved</p> <p>This bit is always read as 0. The write value should always be 0.</p>
5, 4	CMR[1:0]	00	R/W	<p>Compare Match Request</p> <p>These bits enable or disable internal interrupt request in a compare match.</p> <p>00: Disables internal interrupt request</p> <p>01: Setting prohibited</p> <p>10: Enables an internal interrupt request</p> <p>11: Setting prohibited</p>
3	DBGIVD	1	R/W	<p>Debug Mode Operation Select</p> <p>Sets the counter operation in debugging mode.</p> <p>0: Stops the counter operation in debugging mode.</p> <p>1: Continues the counter operation even in debugging mode.</p>
2 to 0	CKS[2:0]	111	R/W	<p>Clock Select</p> <p>These bits select the clock input to CMCNTn. When the count start bit (STRO) in CMSTRn is set to 1, CMCNTn begins incrementing with the clock selected by these bits.</p> <p>000: Setting prohibited</p> <p>001: Setting prohibited</p> <p>010: Setting prohibited</p> <p>011: Setting prohibited</p> <p>100: RCLK/8</p> <p>101: RCLK/32</p> <p>110: RCLK/128</p> <p>111: RCLK/1</p>

Notes: 1. CMCSR 0 to CMCSR7

2. Refer to section 57B.3.5, Register Access, for the note regarding writing to or reading from the following bits.

**57B.2.4 Compare Match Timer Control/Status Registers H0 to 4 (CMCSRHn)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CMCSRHn is a 32-bit register which specify the counter size and input clocks.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	CMSH	—	—	—	—	—	—	—	—	CKSH
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 10	—	All 0	R	Reserved This bit is always read as 0. The write value should always be 0.
9	CMSH	0	R/W	Compare Match Timer Counter Size This bit and CMCSRn.CMS specify whether the compare match timer counter (CMCNTHn[15:0] and CMCNTn[31:0]) is used as a 16-bit counter, a 32-bit counter, or a 48-bit counter. This bit also specify valid size for the compare match timer constant register (CMCORHn[15:0], CMCORn[31:0]). CMCSRHn.CMSH[9], CMCSRn.CMS[9]: 1x: Operates as a 48-bit counter 00: Operates as a 32-bit counter 01: Operates as a 16-bit counter
8 to 1	—	All 0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
0	CKSH	0	R/W	<p>Clock Select</p> <p>This bit and CMCSRn.CKS[2:0] select the clock input to CMCNT. When the count start bit (STR0) for the corresponding channel is set to 1, CMCNTn begins incrementing with the clock selected by these bits.</p> <p>CMCSRHn.CKSH[0], CMCSRn.CKS[2:0]:</p> <p>x000: CP<math>\phi</math> (CPEX<math>\phi</math>)/8  x001: CP<math>\phi</math> (CPEX<math>\phi</math>)/32  x010: CP<math>\phi</math> (CPEX<math>\phi</math>)/128  x011: CP<math>\phi</math> (CPEX<math>\phi</math>)/1  0100: RCLK/8  0101: RCLK/32  0110: RCLK/128  0111: RCLK/1  1100: Pseudo 32 kHz/8  1110: Pseudo 32 kHz/32  1101: Pseudo 32 kHz/128  1111: Pseudo 32 kHz/1</p>

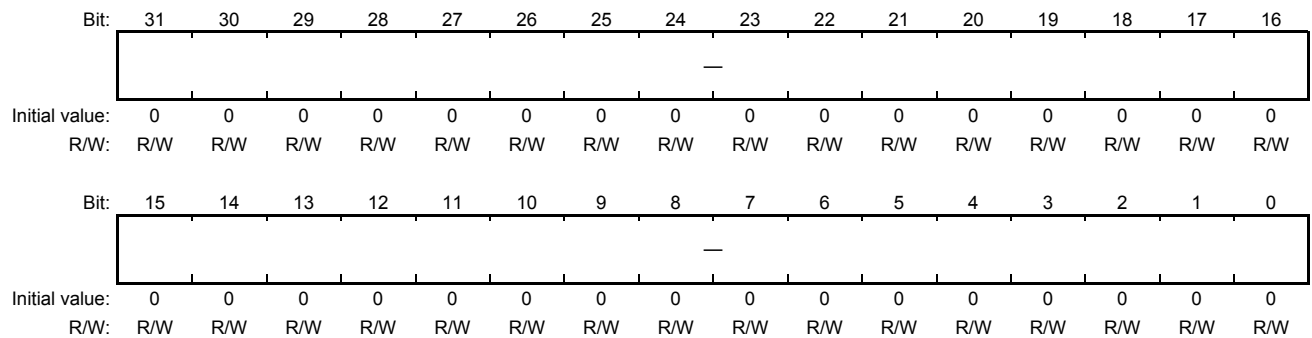
Note: CMSH, CKSH For write or read, refer to section 57B.3.5, Register Access.

**57B.2.5 Compare Match Timer Counters 0 to 7 (CMCNTn)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CMCNTn (n = 0 to 7) is a 32-bit register which is used as an up-counter of each channel.

To specify counter operation, set compare match timer control/status register n (CMCSRn), before starting operation of corresponding channel. When the 16-bit counter operation is selected by the CMCSRH.CMSH and CMCSR.CMS bits, bits 31 to 16 of this register is invalid. When data is written to this register in 16-bit mode, write H'0000 to the upper 16 bit.



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	—	All 0	R/W	Compare match timer counter bit31 to 0

Note: For access to this register, refer to section 57B.3.5, Register Access.



**57B.2.6 Compare Match Timer Counters H 0 to 4 (CMCNTHn)**

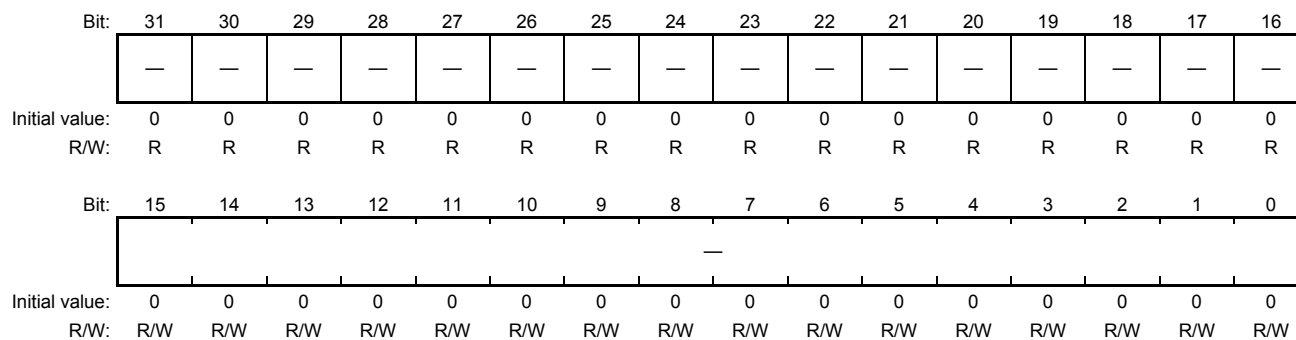
RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CMCNTHn (n = 0 to 4) is a 32-bit register which is used as an up-counter for channel0 to 4.

To specify counter operation, set compare match timer control/status register n (CMCSRn/CMCSRHn), before starting operation of corresponding channel. When the 48-bit counter operation is selected by the CMCSRHn.CMSH and CMCSRn.CMS bits, bits 15 to 0 of this register become valid as the upper 16-bit of 48-bit counter. The value written to this register is reflected to counter behavior, when lower data is written to CMCNTn. Write the upper data to this register first. The value is not reflected to counter’s behavior, if data is not written to CMCNTn later.

When reading the value of 48-bit counter, upper 16-bit can be read out by reading bits 15 to 0 of this register. At the same time of the reading, the value of 48-bit counter is stored to the read-buffer. After reading CMCNTHn, lower 32-bit can be read out by reading CMCNTn.

Note: If CMCNTn is read out before reading CMCNTHn, the read out value of 48-bit counter may not be correct.



Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved This bit is always read as 0. The write value should always be 0.
15 to 0	—	All 0	R/W	Compare match timer counter H bit15 to 0 Note: For access to this register, refer to section 57B.3.5, Register Access.

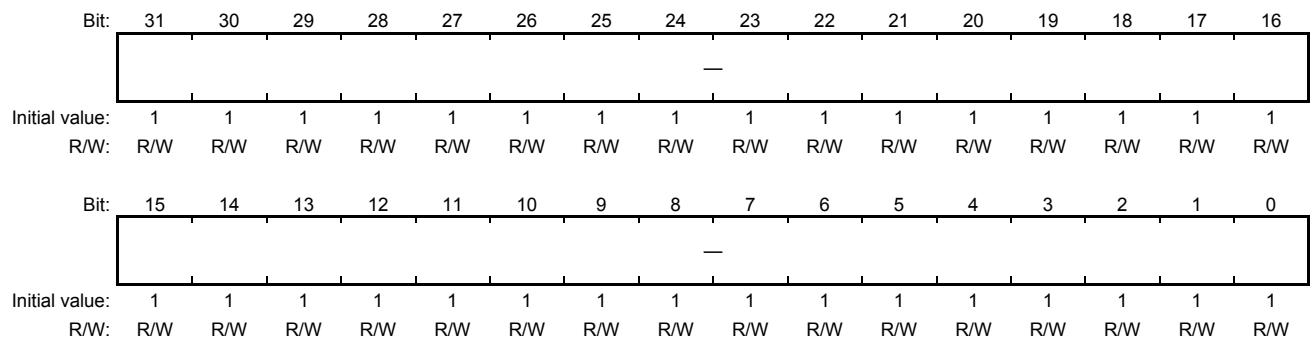
**57B.2.7 Compare Match Timer Constant Registers 0 to 7 (CMCORN)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CMCORN is a 32-bit register which specify the compare match period of CMCNTn for each channel.

When the 16-bit counter operation is selected by the CMCSRHn.CMSH and CMCSRn.CMS bits, bits 31 to 16 of this register is invalid. When data is written to this register in 16-bit operation mode, write H'0000 as upper 16bit.

An overflow is detected when CMCNTn is cleared to 0 and this register is H'FFFFFFFF (when the 16-bit counter operation it is H'0000 FFFF).



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	—	All 1	R/W	Compare match timer constant register bit31 to 0 Note: For access to this register, refer to section 57B.3.5, Register Access.

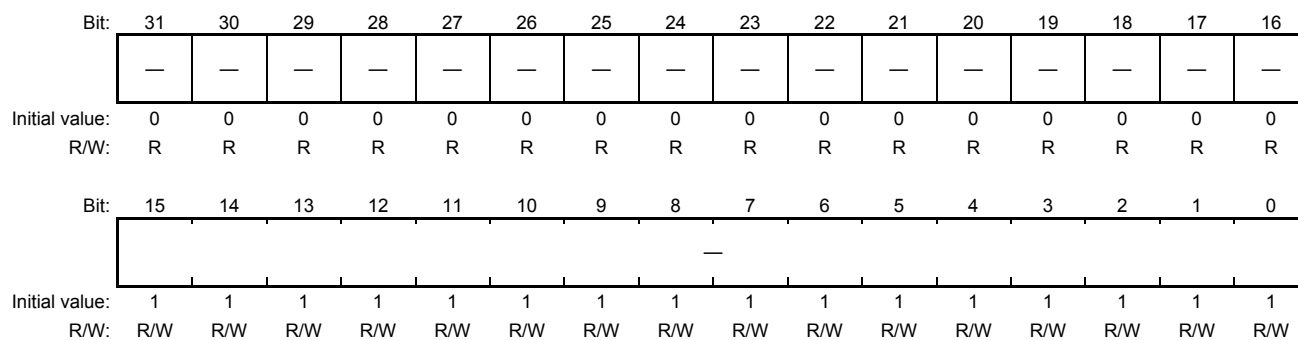
**57B.2.8 Compare Match Timer Constant Registers H0 to 4 (CMCORHn)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CMCORHn is a 32-bit register which specify the compare match period with CMCNTHn for channel0 to 4.

When the 48-bit counter operation is selected by the CMCSRHn.CMSH and CMCSRn.CMS bits, bits 15 to 0 of this register become valid as the upper 16-bit of 48-bit counter.

An overflow is detected when CMCNTHn is cleared to 0 and this register is H'FFFF.

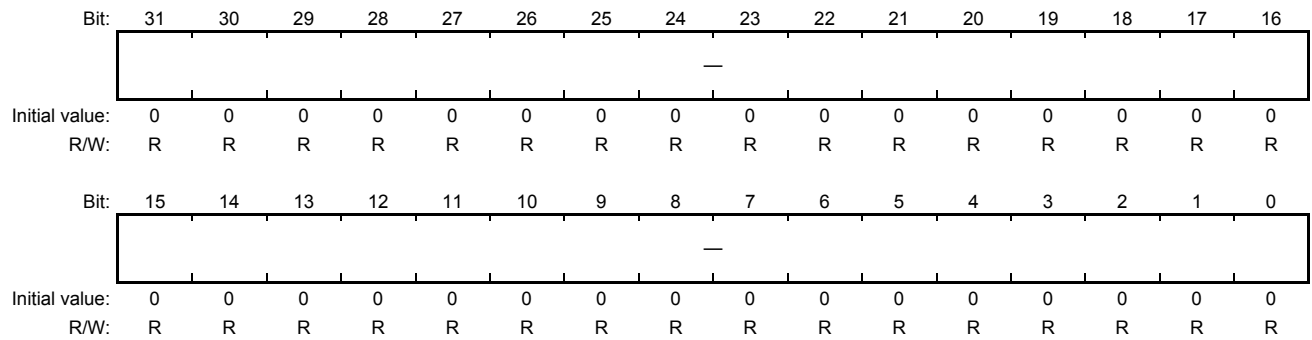


Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved This bit is always read as 0. The write value should always be 0.
15 to 0	—	All 1	R/W	Compare match timer constant register H bit15 to 0 Note: For access to this register, refer to section 57B.3.5, Register Access.

**57B.2.9 Compare Match Timer Counter 3 Backup 0 (CMCNT3BK0)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CMCNT3BK0 is a 32-bit register which stores a copy of the CMCNT3 value immediately after the counter in channel 0 stops in RCLK-synchronous channel 0 counter start/stop mode.

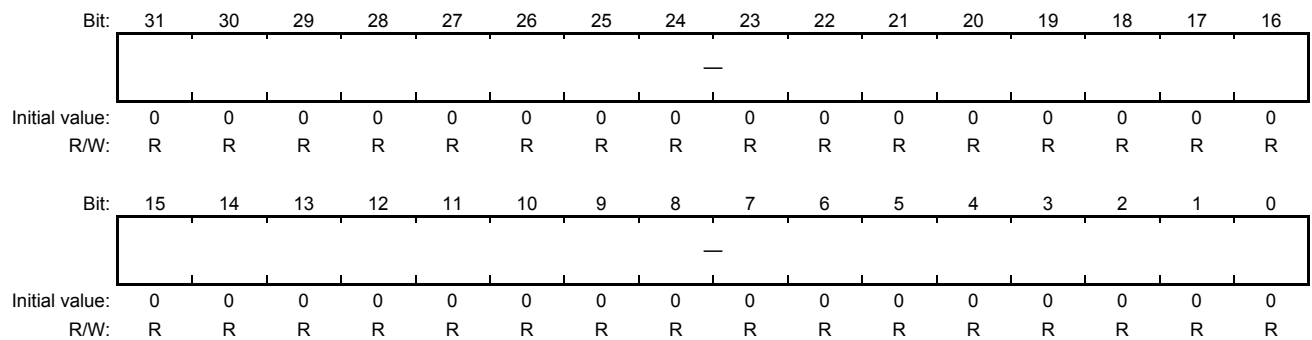


Bit	Bit Name	Initial Value	R/W	Description
31 to 0	—	All 0	R	Compare match timer counter 3 backup 0 bit31 to 0

**57B.2.10 Compare Match Timer Counter 3 Backup 1 (CMCNT3BK1)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CMCNT3BK1 is a 32-bit register which stores a copy of the CMCNT3 value immediately after the counter in channel 0 starts in RCLK-synchronous channel 0 counter start/stop mode.



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	—	All 0	R	Compare match timer counter 3 backup 1 bit31 to 0

**57B.2.11 Compare Match Timer Match Control/Status Registers 0 and 3 (CMCSRm)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CMCSRm is a 32-bit register which resets to compare match timer match counter, and sets the counter start/halt. This register is only present in channels 0 and 3.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	WRFLG	—	—	—	—	—	—	—	—	—	—	—	—	—	CMPCLR	CMPSTART
	G														R	ART
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

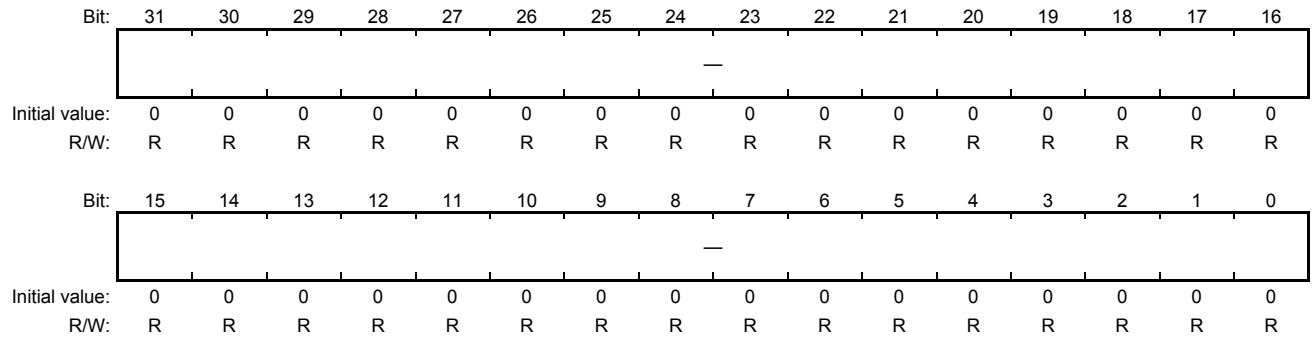
Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved This bit is always read as 0. The write value should always be 0.
15	WRFLG	0	R	Write state flag. When this Bit is 1, CMCNTMn cannot be cleared. After CMCNTMn is cleared, this bit become 1 for a while (*), for indicating synchronization period. Needs to confirm this flag is 0 or wait the period enough when continuously clearing. Note: * In the maximum, "Counter input clock 6 cycle " <ul style="list-style-type: none"> <li>Counter input clock CMCSRn.CKS2 = 0: CPφ (CPEXφ) CMCSRn.CKS2 = 1: RCLK</li> </ul>
14 to 2	—	All 0	R	Reserved This bit is always read as 0. The write value should always be 0.
1	CMPCLR	0	R/W	Counter Clear [When writing] 0: No operation 1: Clears counter When CMPCLR and CMPSTART are written 1 at the same time, the counter starts after clearing the counter. [When reading] This bit is always read as 0.
0	CMPSTART	0	R/W	Count Start This bit specifies start/halt of the compare match timer match counter (CMCNTMn) of each channel. 0: CMCNTMn Halts 1: CMCNTMn Starts counting

**57B.2.12 Compare Match Timer Match Counters 0 and 3 (CMCNTMn)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

CMCNTMn is a 32-bit register which is used as an up-counter. This register is only present in channels 0 and 3.

A counter operation is set by the compare match timer match control/status register (CMCSRm). After the counter CMCNTn starts, this counter increases whenever at a compare match.



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	—	All 0	R	Compare match timer match counter bit31 to 0

RZ/G1H	RZ/G1N
RZ/G1M	RZ/G1E

### 57B.3 Operation

#### 57B.3.1 Counter Operation

The CMT1 starts the operation of the counter by writing H'1 to the STR0 bit in CMSTRn after each register has been set. Complete all of the settings before starting the operation. Do not change the register settings other than clearing flag bits, while the compare match timer (CMCNTn) is under operation.

The counter operates in one of two ways.

- One-Shot Operation

One-shot operation is selected by setting the CMM bit in CMCSRn to H'0. When the value in CMCNTn matches the value in CMCORn, the value in CMCNTn is cleared to H'0000 0000 and the CMF bit in CMCSRn is set to H'1. Counting by CMCNTn stops after it has been cleared.

To detect an overflow interrupt, set the value in CMCORn to H'FFFF FFFF. When the value in CMCNTn matches the value in CMCORn, CMCNTn is cleared to H'0000 0000 and the CMF and OVF bits in CMCSRn are set to H'1.

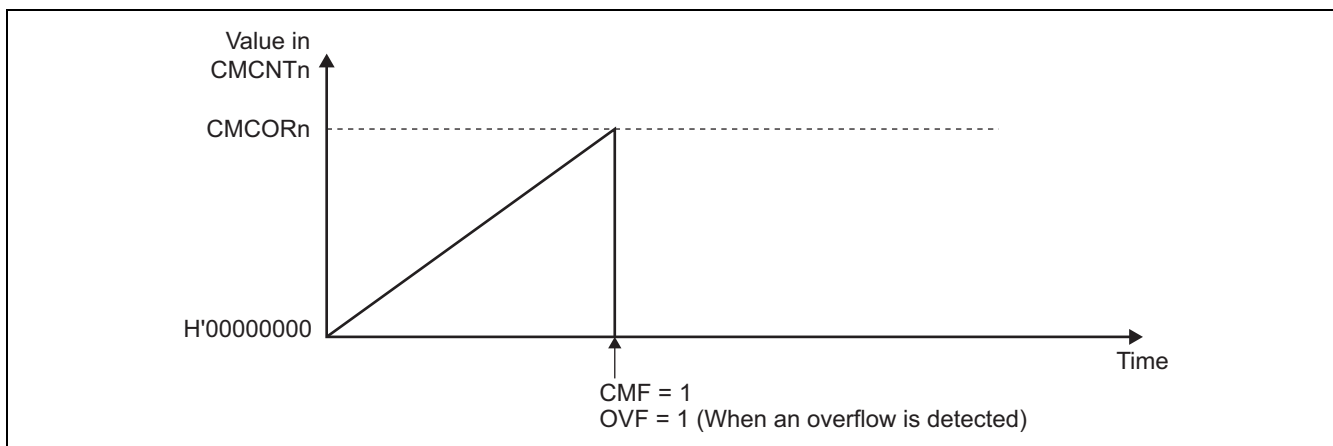
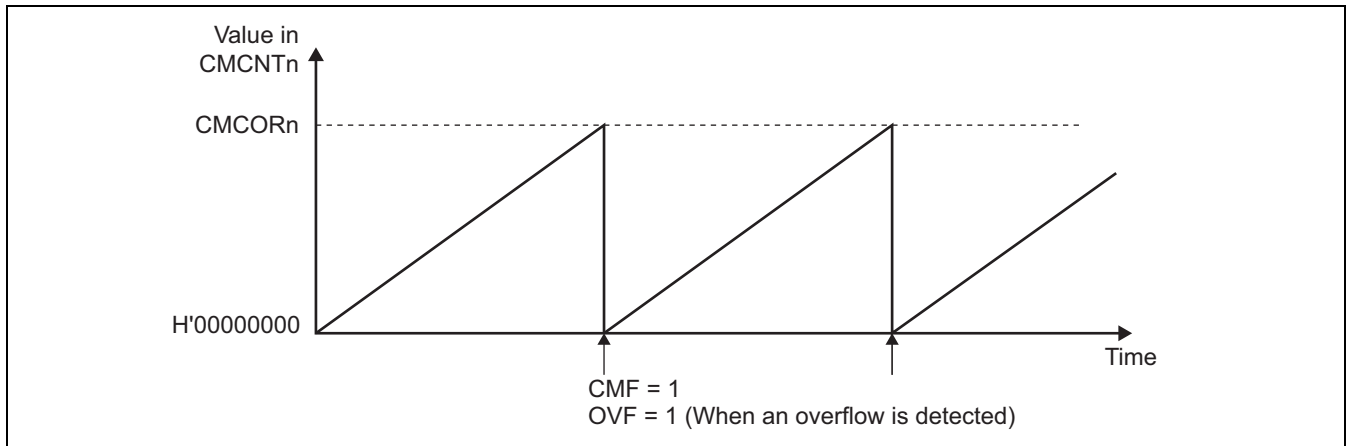


Figure 57B.2 Counter Operation (One-Shot Operation)

- Free-Running Operation

Free-running operation is selected by setting the CMM bit in CMCSRn to H'1. When the value in CMCNTn matches the value in CMCORn, CMCNTn is cleared to H'0000 0000 and the CMF bit in CMCSRn is set to H'1. CMCNTn resumes counting-up after it has been cleared.

To detect an overflow interrupt, set CMCORn to H'FFFF FFFF. When the values in CMCNTn and CMCORn match, CMCNTn is cleared to H'0000 0000 and the CMF and OVF bits in CMCSRn are set to H'1.



**Figure 57B.3 Counter Operation (Free-Running Operation)**



### 57B.3.2 Counter Size

In this module, the size of the counter can be selected from 16, 32, or 48 bits. This is selected by the CMS bit in CMCSRn and CMSH bit in CMCSRHn.

When the 16-bit/32-bit size is selected, upper 32 bits/16 bits of CMCORn is ignored. To detect an overflow interrupt, the value 1 must be set to valid bits of CMCORn.

(for example, H'00000000FFFF, H'0000FFFFFFFF)

### 57B.3.3 Timing for Counting by CMCNTn

In this module, the clock for the counter can be selected from among the following:

Channels 0 to 4:	CP $\phi$ (CPEX $\phi$ ) clock:	1/1, 1/8, 1/32, and 1/128
	RCLK:	1/1, 1/8, 1/32, and 1/128
	Pseudo 32-kHz:	1/1, 1/8, 1/32 and 1/128
Channel 5 to 7:	RCLK:	1/1, 1/8, 1/32, and 1/128

CP $\phi$  (CPEX $\phi$ ) for RZ/G1H/M/N is a clock, which is generated based on EXTAL, and divided by 2; for RZ/G1E is a clock from PLL1 via common divider. For details of these clocks, refer to section 7, Clock Pulse Generator (CPG).

Pseudo 32-kHz is a clock, which is generated inside this module. Refer to section 57B.3.8, Pseudo 32-kHz Counter.

The clock for the counter is selected by the CKS bits in CMCSRn and CKSH bit in CMCSRHn. CMCNTn is incremented at the rising edge of the selected clock.

### 57B.3.4 Internal Interrupt Request to CPU

By CMR bits in CMCSRn, internal interrupt request to the CPU at a compare match can be asserted.

To clear the internal interrupt request to the CPU, the CMF bit should be set to H'0. Set the CMF bit to 0 in the handling routine for the CMT1 interrupt.

### 57B.3.5 Register Access

After writing to following registers, written data can be read after writing has finished. However, it takes 2 cycles in counter input clock (RCLK), for reflecting written data to counter behavior.

- CMCSRn: Bits CH0SSIE(ch0), CMS, CMM, CMR[1:0], DBGIVD, CKS[2:0]
- CMCORn, CMCORHn
- CMSTRn: Bit STR0RS, STR0
- CMCSRMn: Bit CMPCLR, CMPSTART

After writing to following registers, written data can be read after writing has finished. However, it takes 2 cycles in counter input clock (RCLK or CP $\phi$  (CPEX $\phi$ )), for reflecting written data to counter behavior. After writing data to this register, next write access is prohibited, until CMCSRn.WRFLG become 0.

- CMCNTn, CMCNTHn

### 57B.3.6 Compare Match Flag Set/Clear Timing

The CMF bit in CMCSRn is set to 1 by the compare match signal generated when CMCORn and CMCNTn match. The compare match signal is generated upon the final state of the match (timing at which the CMCNTn value is updated to H'0000). Consequently, after CMCORn and CMCNTn match, a compare match signal will not be generated until a CMCNTn counter clock is input. Figure 57B.4 shows the set timing of the CMF bit.

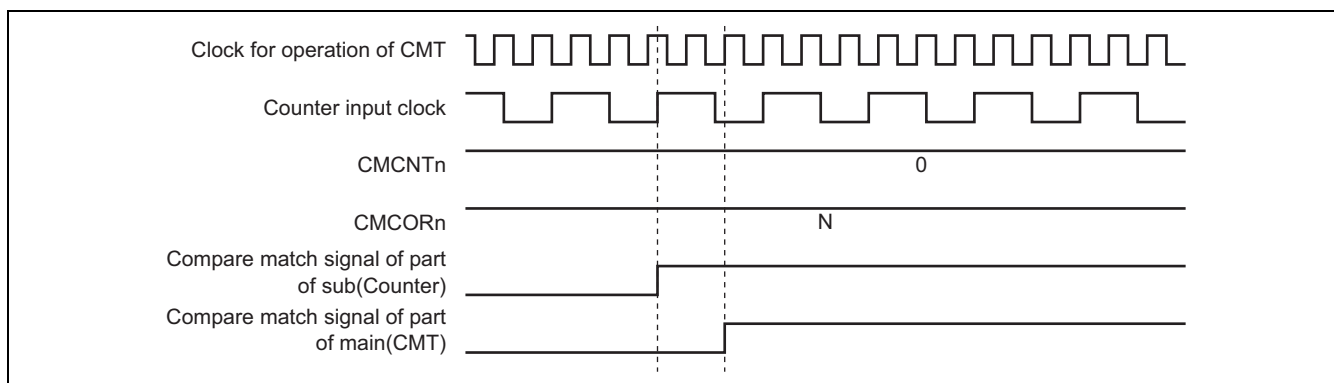


Figure 57B.4 CMF Set Timing

Set the CMF bit to 0. The CMF flag is cleared immediately.

### 57B.3.7 RCLK-Synchronous Counter Start/Stop Mode in Channel 0

The CMT1 provides the RCLK-synchronous counter start/stop mode in channel 0, in which channels 0 and 3 can be used together for time measurement.

Figure 57B.5 shows a flow chart for preparation.

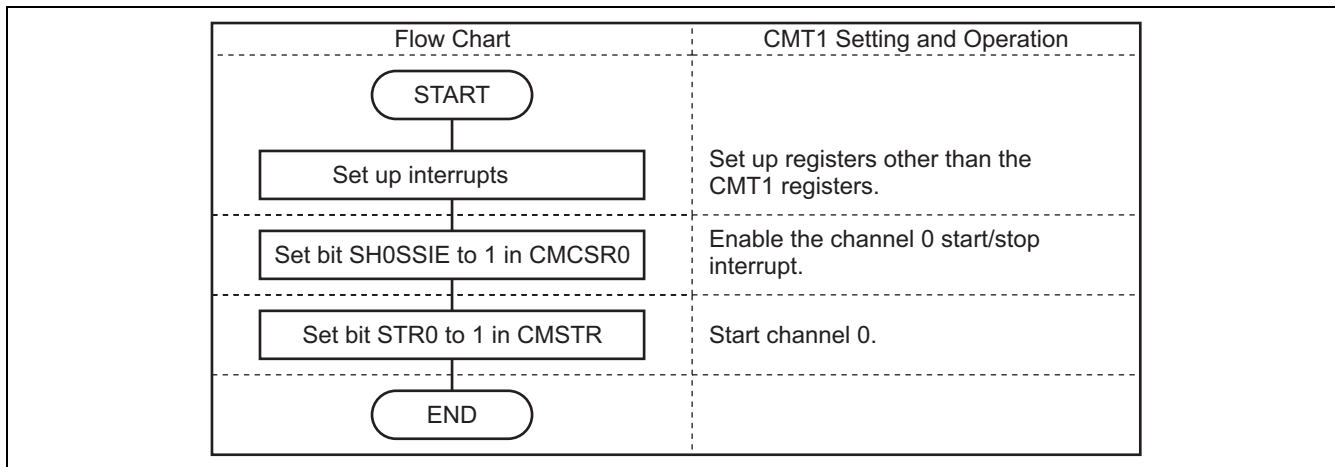
Figure 57B.6 shows a flow chart for starting measurement.

Figure 57B.7 shows a flow chart for stopping measurement.

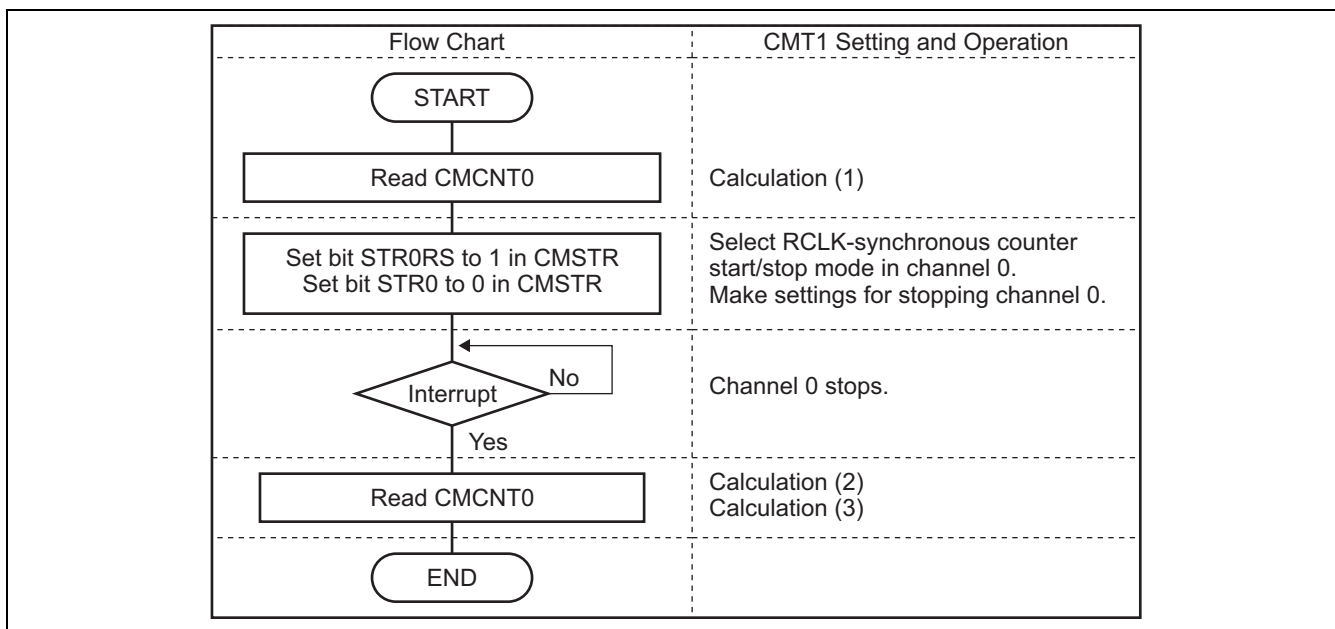
Figure 57B.8 shows a timing chart when measurement starts.

Figure 57B.9 shows a timing chart when measurement stops.

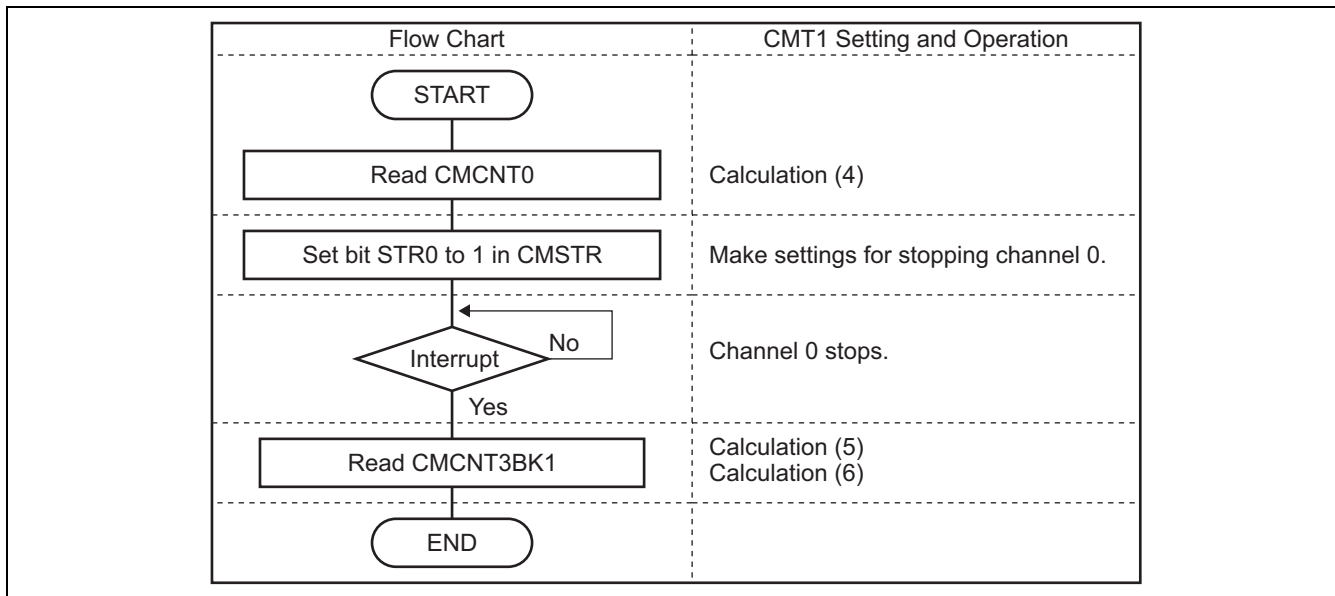
Figure 57B.10 shows how to calculate the time measured by the counters.



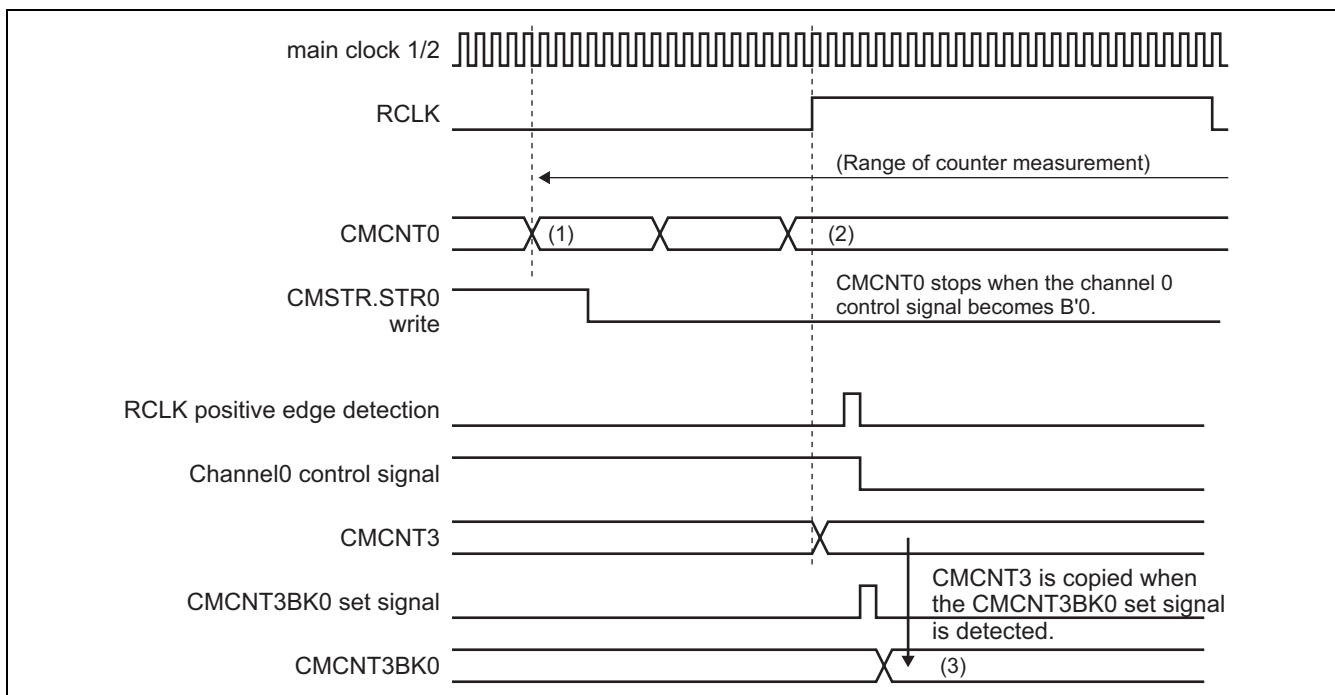
**Figure 57B.5 Flow Chart for Preparation**



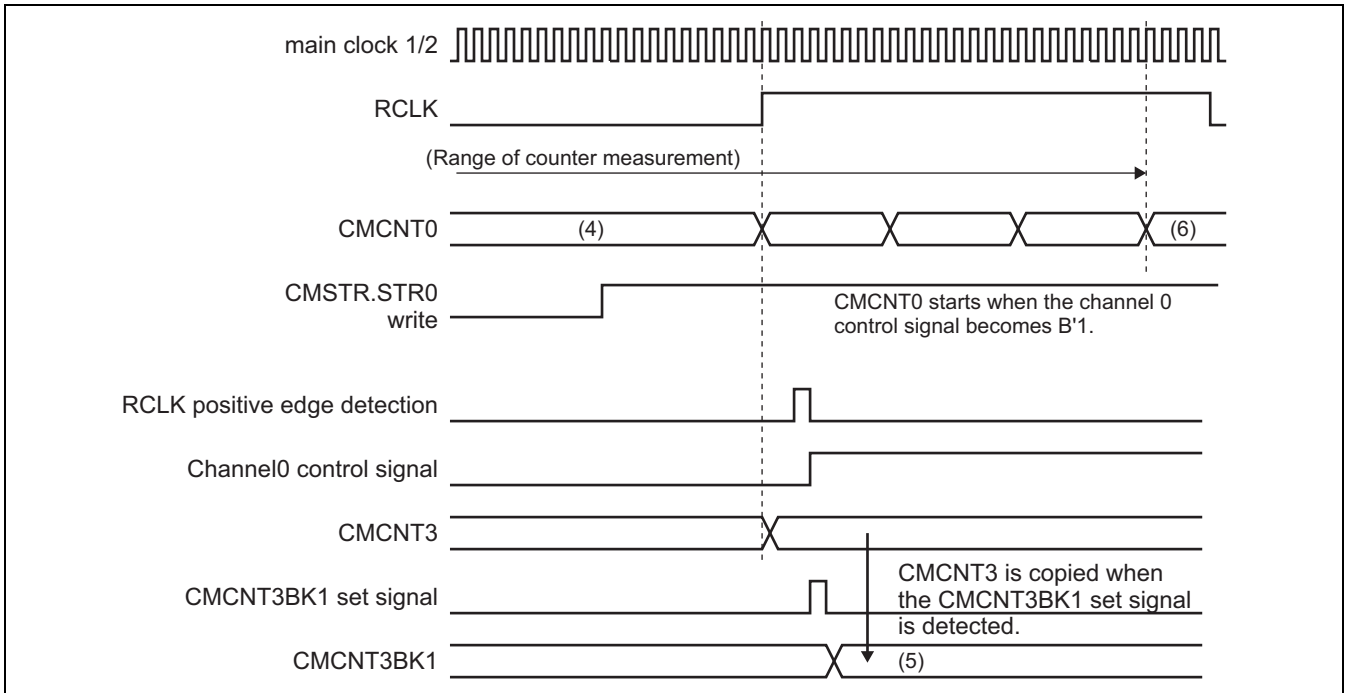
**Figure 57B.6 Flow Chart for Starting Measurement**



**Figure 57B.7 Flow Chart for Stopping Measurement**



**Figure 57B.8 Timing Chart When Measurement Starts**



**Figure 57B.9 Timing Chart When Measurement Stops**

$$(((2) - (1)) + ((6) - (4) - 1)) \times \text{Tapc} + ((5) - (3)) \times \text{Tr}$$

Tapc : Cycle of main clock 1/2  
 Tr : Cycle of RCLK

**Figure 57B.10 Calculation of Time Measured by Counters**

### 57B.3.8 Pseudo 32-kHz Counter

Pseudo 32-kHz clock is created inside this module, based on RCLK by Pseudo 32-kHz Counter. By removing 3 edge of RCLK every 128 cycle, Pseudo 32-kHz clock is generated. By this edge removing, frequency of this clock becomes 128/131 of RCLK.

### 57B.3.9 CMT1 Usage

Take the following steps to use the CMT1.

1. Clear the STR0 bit in CMSTRn to 0 to temporarily stop counting.  
(Confirm that Counter input clock was input more than 2 cycles.)
2. Write H'00000000 on CMCNTn.
3. Set counter size, compare match mode, kind of count clock and interrupt request and clear the bit of OVF and CMF in CMCSRn.
4. Set the value on CMCORn.
5. Confirm that CMCSRn.WRFLG is 0.  
If WRFLG is 1, wait until it'll be 0.
6. Start the counting by setting the STR0 bit in CMSTRn to 1 (refer to section 57B.3.5, Register Access).

### 57B.3.10 Module Stop/ CMCLKE Setting

When counter is not used, clock of this module can be stopped by CMCLKE register. Please confirm that, following conditions are satisfied, before stopping counter's clock.

- CMSTRn.STR0 bit is 0
- CMCSRn.WRFLG is 0
- 3 or more cycles have passed in Counter input clock since the last Register access

## 58. Timer Unit (TMU)

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

This LSI includes a 32-bit timer unit (TMU) with 12 channels (channels 0 to 11).

Channels 0 to 2, 3 to 5, 6 to 8, and 9 to 11 are grouped into timers 0, 1, 2 and 3, respectively.

For channels 0 to 2, CP $\phi$  is provided as a base clock. For channels 3 to 11, P $\phi$  is provided.

### 58.1 Features

TMU has the following features:

- Auto-reload type 32-bit down counter is provided for each channel
- Input capture function provided: Channels 5 and 8
- Selection of rising edge or falling edge as external clock input edge when external clock is selected or input capture function is used: Channels 3 to 8
- 32-bit timer constant register for auto-reload use, readable/writable at any time, and 32-bit down-counter are provided for each channel
- Selection of five counter input clocks: Channels 0 to 2  
Five peripheral clocks (CP $\phi$ /4, CP $\phi$ /16, CP $\phi$ /64, CP $\phi$ /256, and CP $\phi$ /1024)
- Selection of six counter input clocks: Channels 3 to 8  
External clock (TCLK1/2), and five peripheral clocks (P $\phi$ /4, P $\phi$ /16, P $\phi$ /64, P $\phi$ /256, and P $\phi$ /1024)
- Selection of five counter input clocks: Channels 9 to 11  
Five peripheral clocks (P $\phi$ /4, P $\phi$ /16, P $\phi$ /64, P $\phi$ /256, and P $\phi$ /1024)
- Two interrupt sources  
One underflow source (each channel) and one input capture source (channels 5 and 8)

Figure 58.1 show block diagrams of TMU.

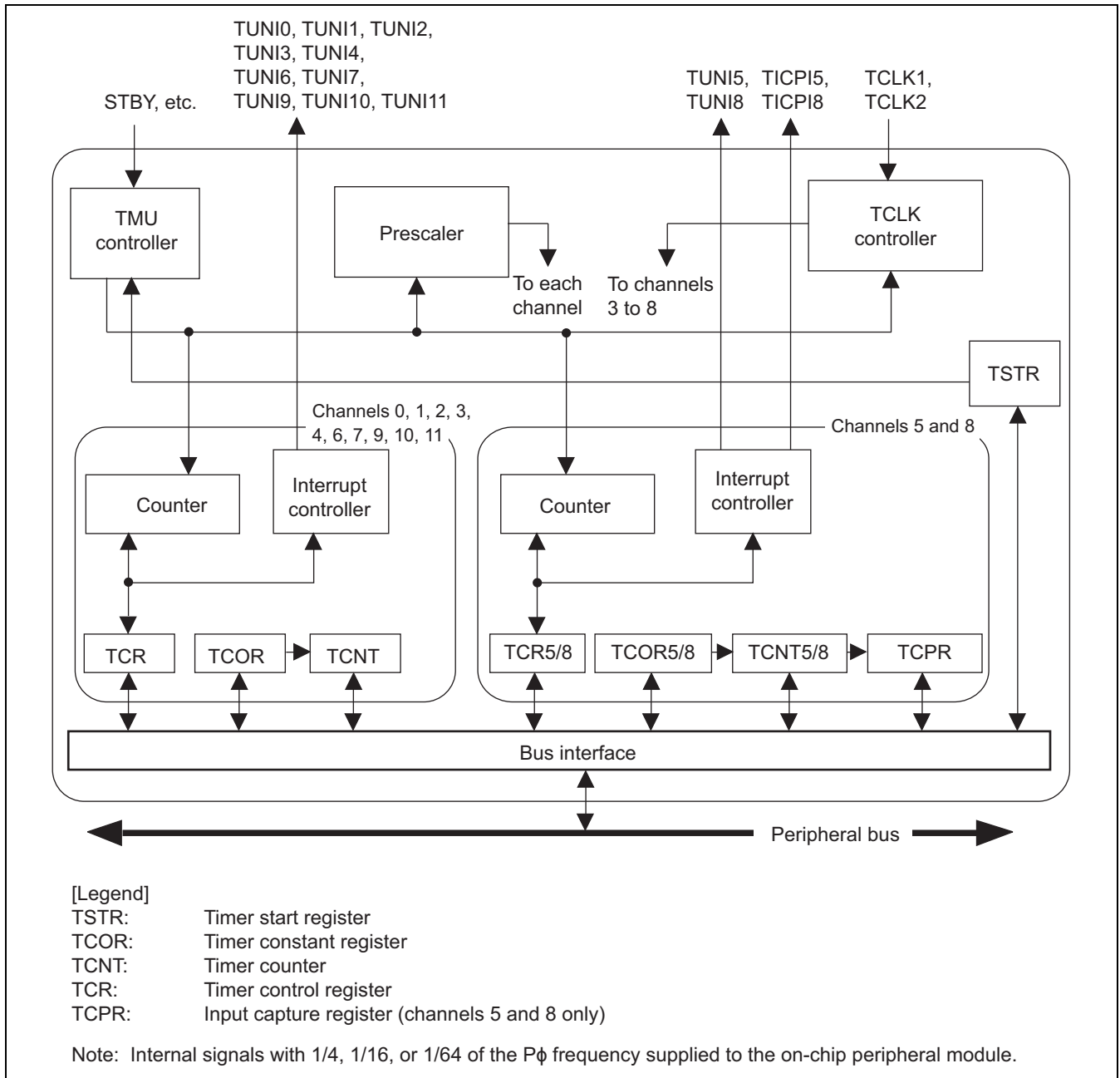


Figure 58.1 Block Diagram of TMU



## 58.2 Input/Output Pins

Table 58.1 shows the pin configuration of the TMU.

**Table 58.1 Pin Configuration**

Name	Abbreviation	I/O	Function	RZ/G Series Products			
				RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Clock input 1	TCLK1	Input	External clock input pin for channels 3 to 5/ input capture control input pin for channel 5	√	√	√	√
Clock input 2	TCLK2	Input	External clock input pin for channels 6 to 8/ input capture control input pin for channel 8	√	√	√	√

### 58.3 Register Descriptions

The TMU has the following registers. Do not write to any addresses other than listed below. Operations cannot be guaranteed if writing is attempted. Values read from addresses other than those listed below are undefined.

**Table 58.2 Register Configuration (1)**

Channel	Name	Abbreviation	R/W	Address	Size	RZ/G Series Products			
						RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Common to 0 to 2	Timer start register 0	TSTR0	R/W	H'E61E 0004	8	√	√	√	√
0	Timer constant register 0	TCOR0	R/W	H'E61E 0008	32	√	√	√	√
	Timer counter 0	TCNT0	R/W	H'E61E 000C	32	√	√	√	√
	Timer control register 0	TCR0	R/W	H'E61E 0010	16	√	√	√	√
1	Timer constant register 1	TCOR1	R/W	H'E61E 0014	32	√	√	√	√
	Timer counter 1	TCNT1	R/W	H'E61E 0018	32	√	√	√	√
	Timer control register 1	TCR1	R/W	H'E61E 001C	16	√	√	√	√
2	Timer constant register 2	TCOR2	R/W	H'E61E 0020	32	√	√	√	√
	Timer counter 2	TCNT2	R/W	H'E61E 0024	32	√	√	√	√
	Timer control register 2	TCR2	R/W	H'E61E 0028	16	√	√	√	√
Common to 3 to 5	Timer start register 1	TSTR1	R/W	H'FFF6 0004	8	√	√	√	√
3	Timer constant register 3	TCOR3	R/W	H'FFF6 0008	32	√	√	√	√
	Timer counter 3	TCNT3	R/W	H'FFF6 000C	32	√	√	√	√
	Timer control register 3	TCR3	R/W	H'FFF6 0010	16	√	√	√	√
4	Timer constant register 4	TCOR4	R/W	H'FFF6 0014	32	√	√	√	√
	Timer counter 4	TCNT4	R/W	H'FFF6 0018	32	√	√	√	√
	Timer control register 4	TCR4	R/W	H'FFF6 001C	16	√	√	√	√
5	Timer constant register 5	TCOR5	R/W	H'FFF6 0020	32	√	√	√	√
	Timer counter 5	TCNT5	R/W	H'FFF6 0024	32	√	√	√	√
	Timer control register 5	TCR5	R/W	H'FFF6 0028	16	√	√	√	√
	Input capture register 5	TCPR5	R	H'FFF6 002C	32	√	√	√	√

Channel	Name	Abbreviation	R/W	Address	Size	RZ/G Series Products			
						RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Common to 6 to 8	Timer start register 2	TSTR2	R/W	H'FFF7 0004	8	√	√	√	√
6	Timer constant register 6	TCOR6	R/W	H'FFF7 0008	32	√	√	√	√
	Timer counter 6	TCNT6	R/W	H'FFF7 000C	32	√	√	√	√
	Timer control register 6	TCR6	R/W	H'FFF7 0010	16	√	√	√	√
7	Timer constant register 7	TCOR7	R/W	H'FFF7 0014	32	√	√	√	√
	Timer counter 7	TCNT7	R/W	H'FFF7 0018	32	√	√	√	√
	Timer control register 7	TCR7	R/W	H'FFF7 001C	16	√	√	√	√
8	Timer constant register 8	TCOR8	R/W	H'FFF7 0020	32	√	√	√	√
	Timer counter 8	TCNT8	R/W	H'FFF7 0024	32	√	√	√	√
	Timer control register 8	TCR8	R/W	H'FFF7 0028	16	√	√	√	√
	Input capture register 8	TCPR8	R	H'FFF7 002C	32	√	√	√	√
Common to 9 to 11	Timer start register 3	TSTR3	R/W	H'FFF8 0004	8	√	√	√	√
9	Timer constant register 9	TCOR9	R/W	H'FFF8 0008	32	√	√	√	√
	Timer counter 9	TCNT9	R/W	H'FFF8 000C	32	√	√	√	√
	Timer control register 9	TCR9	R/W	H'FFF8 0010	16	√	√	√	√
10	Timer constant register 10	TCOR10	R/W	H'FFF8 0014	32	√	√	√	√
	Timer counter 10	TCNT10	R/W	H'FFF8 0018	32	√	√	√	√
	Timer control register 10	TCR10	R/W	H'FFF8 001C	16	√	√	√	√
11	Timer constant register 11	TCOR11	R/W	H'FFF8 0020	32	√	√	√	√
	Timer counter 11	TCNT11	R/W	H'FFF8 0024	32	√	√	√	√
	Timer control register 11	TCR11	R/W	H'FFF8 0028	16	√	√	√	√

**Table 58.3 Register Configuration (2)**

Channel	Name	Abbreviation	Power-On Reset	Module Standby	RZ/G Series Products			
					RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Common to 0 to 2	Timer start register	TSTR0	H'00	Retained	√	√	√	√
0	Timer constant register 0	TCOR0	H'FFFF FFFF	Retained	√	√	√	√
	Timer counter 0	TCNT0	H'FFFF FFFF	Retained	√	√	√	√
	Timer control register 0	TCR0	H'0000	Retained	√	√	√	√
1	Timer constant register 1	TCOR1	H'FFFF FFFF	Retained	√	√	√	√
	Timer counter 1	TCNT1	H'FFFF FFFF	Retained	√	√	√	√
	Timer control register 1	TCR1	H'0000	Retained	√	√	√	√
2	Timer constant register 2	TCOR2	H'FFFF FFFF	Retained	√	√	√	√
	Timer counter 2	TCNT2	H'FFFF FFFF	Retained	√	√	√	√
	Timer control register 2	TCR2	H'0000	Retained	√	√	√	√
Common to 3 to 5	Timer start register 1	TSTR1	H'00	Retained	√	√	√	√
3	Timer constant register 3	TCOR3	H'FFFF FFFF	Retained	√	√	√	√
	Timer counter 3	TCNT3	H'FFFF FFFF	Retained	√	√	√	√
	Timer control register 3	TCR3	H'0000	Retained	√	√	√	√
4	Timer constant register 4	TCOR4	H'FFFF FFFF	Retained	√	√	√	√
	Timer counter 4	TCNT4	H'FFFF FFFF	Retained	√	√	√	√
	Timer control register 4	TCR4	H'0000	Retained	√	√	√	√
5	Timer constant register 5	TCOR5	H'FFFF FFFF	Retained	√	√	√	√
	Timer counter 5	TCNT5	H'FFFF FFFF	Retained	√	√	√	√
	Timer control register 5	TCR5	H'0000	Retained	√	√	√	√
	Input capture register 5	TCPR5	Retained	Retained	√	√	√	√

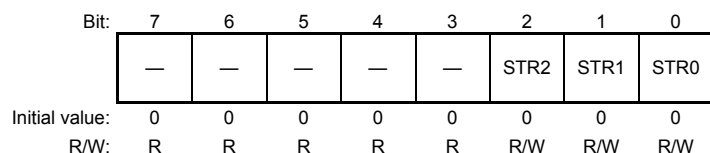
Channel	Name	Abbreviation	Power-On Reset	Module Standby	RZ/G Series Products			
					RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Common to 6 to 8	Timer start register 2	TSTR2	H'00	Retained	√	√	√	√
6	Timer constant register 6	TCOR6	H'FFFF FFFF	Retained	√	√	√	√
	Timer counter 6	TCNT6	H'FFFF FFFF	Retained	√	√	√	√
	Timer control register 6	TCR6	H'0000	Retained	√	√	√	√
7	Timer constant register 7	TCOR7	H'FFFF FFFF	Retained	√	√	√	√
	Timer counter 7	TCNT7	H'FFFF FFFF	Retained	√	√	√	√
	Timer control register 7	TCR7	H'0000	Retained	√	√	√	√
8	Timer constant register 8	TCOR8	H'FFFF FFFF	Retained	√	√	√	√
	Timer counter 8	TCNT8	H'FFFF FFFF	Retained	√	√	√	√
	Timer control register 8	TCR8	H'0000	Retained	√	√	√	√
	Input capture register 8	TCPR8	Retained	Retained	√	√	√	√
Common to 9 to 11	Timer start register 3	TSTR3	H'00	Retained	√	√	√	√
9	Timer constant register 9	TCOR9	H'FFFF FFFF	Retained	√	√	√	√
	Timer counter 9	TCNT9	H'FFFF FFFF	Retained	√	√	√	√
	Timer control register 9	TCR9	H'0000	Retained	√	√	√	√
10	Timer constant register 10	TCOR10	H'FFFF FFFF	Retained	√	√	√	√
	Timer counter 10	TCNT10	H'FFFF FFFF	Retained	√	√	√	√
	Timer control register 10	TCR10	H'0000	Retained	√	√	√	√
11	Timer constant register 11	TCOR11	H'FFFF FFFF	Retained	√	√	√	√
	Timer counter 11	TCNT11	H'FFFF FFFF	Retained	√	√	√	√
	Timer control register 11	TCR11	H'0000	Retained	√	√	√	√

**58.3.1 Timer Start Registers (TSTRn) (n = 0 to 3)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

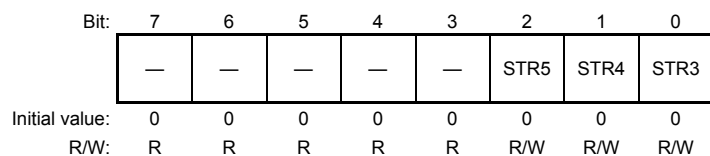
TSTR are 8-bit readable/writable registers that select whether to run or halt the TCNT.

• (TSTR0)



Bit	Bit Name	Initial Value	R/W	Description
7 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2	STR2	0	R/W	Counter Start 2 Selects whether to run or halt TCNT2. 0: TCNT2 count halted 1: TCNT2 counts
1	STR1	0	R/W	Counter Start 1 Selects whether to run or halt TCNT1. 0: TCNT1 count halted 1: TCNT1 counts
0	STR0	0	R/W	Counter Start 0 Selects whether to run or halt TCNT0. 0: TCNT0 count halted 1: TCNT0 counts

• (TSTR1)



Bit	Bit Name	Initial Value	R/W	Description
7 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2	STR5	0	R/W	Counter Start 5 Selects whether to run or halt TCNT5. 0: TCNT5 count halted 1: TCNT5 counts
1	STR4	0	R/W	Counter Start 4 Selects whether to run or halt TCNT4. 0: TCNT4 count halted 1: TCNT4 counts

Bit	Bit Name	Initial Value	R/W	Description
0	STR3	0	R/W	Counter Start 3 Selects whether to run or halt TCNT3. 0: TCNT3 count halted 1: TCNT3 counts

- (TSTR2)

Bit:	7	6	5	4	3	2	1	0
	—	—	—	—	—	STR8	STR7	STR6
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2	STR8	0	R/W	Counter Start 8 Selects whether to run or halt TCNT8. 0: TCNT8 count halted 1: TCNT8 counts
1	STR7	0	R/W	Counter Start 7 Selects whether to run or halt TCNT7. 0: TCNT7 count halted 1: TCNT7 counts
0	STR6	0	R/W	Counter Start 6 Selects whether to run or halt TCNT6. 0: TCNT6 count halted 1: TCNT6 counts

- (TSTR3)

Bit:	7	6	5	4	3	2	1	0
	—	—	—	—	—	STR11	STR10	STR9
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2	STR11	0	R/W	Counter Start 11 Selects whether to run or halt TCNT11. 0: TCNT11 count halted 1: TCNT11 counts
1	STR10	0	R/W	Counter Start 10 Selects whether to run or halt TCNT10. 0: TCNT10 count halted 1: TCNT10 counts

Bit	Bit Name	Initial Value	R/W	Description
0	STR9	0	R/W	Counter Start 9 Selects whether to run or halt TCNT9. 0: TCNT9 count halted 1: TCNT9 counts

### 58.3.2 Timer Constant Registers (TCORn) (n = 0 to 11)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

TCOR are 32-bit readable/writable registers. After underflow has been generated according to the result of the TCNT countdown, the value of TCOR is set to TCNT and TCNT continues countdown from the value.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

### 58.3.3 Timer Counters (TCNTn) (n = 0 to 11)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

TCNT are 32-bit readable/writable registers that count down upon the input clock selected using the bits TPSC2 to TPSC0 in TCR.

When a TCNT countdown results in an underflow, the UNF in TCR of corresponding channel is set. At the same time, the value of TCOR is set to TCNT and TCNT continues countdown from that value.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W



### 58.3.4 Timer Control Registers (TCRn) (n = 0 to 11)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

TCR are 16-bit readable/writable registers that select a count clock and edge when an external clock is selected, and control an interrupt generation when the flag that indicates the generation of a TCNT is set to 1. TCR of channels 5 and 8 control the input capture function and generation of an interrupt during the input capture.

- TCR0, TCR1, TCR2, TCR3, TCR4, TCR6, TCR7, TCR9, TCR10, TCR11

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	UNF	—	—	UNIE	CKEG		TPSC		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W

- TCR5, TCR8

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	ICPF	UNF	ICPE		UNIE	CKEG		TPSC		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9	ICPF*1	0	R/W	Input Capture Interrupt Flag Status flag, provided in channels 5 and 8 only, which indicates the occurrence of input capture. 0: No input capture has occurred [Clearing condition] When 0 is written to ICPF 1: Input capture has occurred [Setting condition] When an input capture occurs*2
8	UNF	0	R/W	Underflow Flag Status flag which indicates the occurrence of a TCNT underflow. 0: TCNT has not underflowed [Clearing condition] When 0 is written to UNF 1: TCNT has underflowed [Setting condition] When TCNT underflows*2

Bit	Bit Name	Initial Value	R/W	Description
7, 6	ICPE* <sup>1</sup>	00	R/W	<p>Input Capture Control</p> <p>A function of channels 5 and 8 only: determines whether the input capture function can be used, and when used, whether or not to enable interrupts.</p> <p>Use the CKEG bits to designate use of either the rising or falling edge of the TCLK pin to set the values of TCNT5 and TCNT8 to TCP5 and TCP8, respectively.</p> <p>Only when the ICPF bits in TCR5 and TCR8 are 0, the values of TCNT5 and TCNT8 are set to TCP5 and TCP8. When the ICPF bit is set to 1, neither TCP5 nor TCP8 is set even when input capture is generated.</p> <p>00: Input capture function is not used.</p> <p>01: Reserved (setting prohibited)</p> <p>10: Input capture function is used. Interrupt due to input capture (TICPI5 and TICPI8) is not enabled.</p> <p>11: Input capture function is used. Interrupt due to input capture (TICPI5 and TICPI8) is enabled.</p>
5	UNIE	0	R/W	<p>Underflow Interrupt Control</p> <p>Controls enabling of interrupt generation when the status flag (UNF) indicating TCNT underflow has been set to 1.</p> <p>0: Interrupt due to underflow (TUNI) is not enabled</p> <p>1: Interrupt due to underflow (TUNI) is enabled</p>
4, 3	CKEG	00	R/W	<p>Clock Edge</p> <p>Select an input edge of the external clock when the external clock is selected, or when the input capture function is used.</p> <p>00: Count/capture register set on rising edge</p> <p>01: Count/capture register set on falling edge</p> <p>1X: Count/capture register set on both rising and falling edge</p>
2 to 0	TPSC	000	R/W	<p>Timer Prescaler 2 to 0</p> <p>Select the TCNT count clock.</p> <p>000: Count on (input-clock)/4</p> <p>001: Count on (input-clock)/16</p> <p>010: Count on (input-clock)/64</p> <p>011: Count on (input-clock)/256</p> <p>100: Count on (input-clock)/1024</p> <p>101: Setting prohibited</p> <p>110: Setting prohibited</p> <p>111: Count on external clock (TCLK) (Not usable in channels 0, 1, 2, 9, 10 and 11)</p> <p>Note: Input-clock is CP<math>\phi</math> for channel 0/1/2, and P<math>\phi</math> for channel 3/4/5/6/7/8/9/10/11.</p>

## [Legend]

X: Don't care

Notes: 1. Reserved in channels 0, 1, 2, 3, 4, 6, 7, 9, 10, and 11 (initial value is 0 and read-only).

2. Writing 1 does not change the value.

### 58.3.5 Input Capture Registers n (TCPRn)

Note: n = 5 and 8

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

TCPR5 and TCPR8 are read-only 32-bit registers used for the input capture function provided only in channels 5 and 8. The ICPE and CKEG bits in TCR5 and TCR8 control the input capture function. When an input capture occurs, the value of TCNT5 is copied to TCPR5, and the value of TCNT8 is copied to TCPR8. The values of TCNT5 and TCNT8 are set in TCPR5 and TCPR8, respectively, only when the ICPF bits in TCR5 and TCR8 are 0.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

RZ/G1H	RZ/G1N
RZ/G1M	RZ/G1E

## 58.4 Operation

Each channel has a 32-bit timer counter (TCNT) and 32-bit timer constant register (TCOR). TCNT counts down. The auto-reload function enables synchronized counting and external-event counting. Channels 5 and 8 have an input capture function.

### 58.4.1 Counter Operation

When the bits STR8 to STR0 in TSTR0 to TSTR3 are set to 1, TCNT of corresponding channel starts counting. When TCNT underflows, the UNF flag of corresponding TCR is set. In this case, if the UNIE bit in TCR is set to 1, an interrupt request is sent to the CPU. Also, the value is copied from TCOR to TCNT and the down-count operation is continued (Auto reload function).

#### (1) Procedure for setting count operation

Figure 58.2 shows an example of the procedure for setting the count operation.

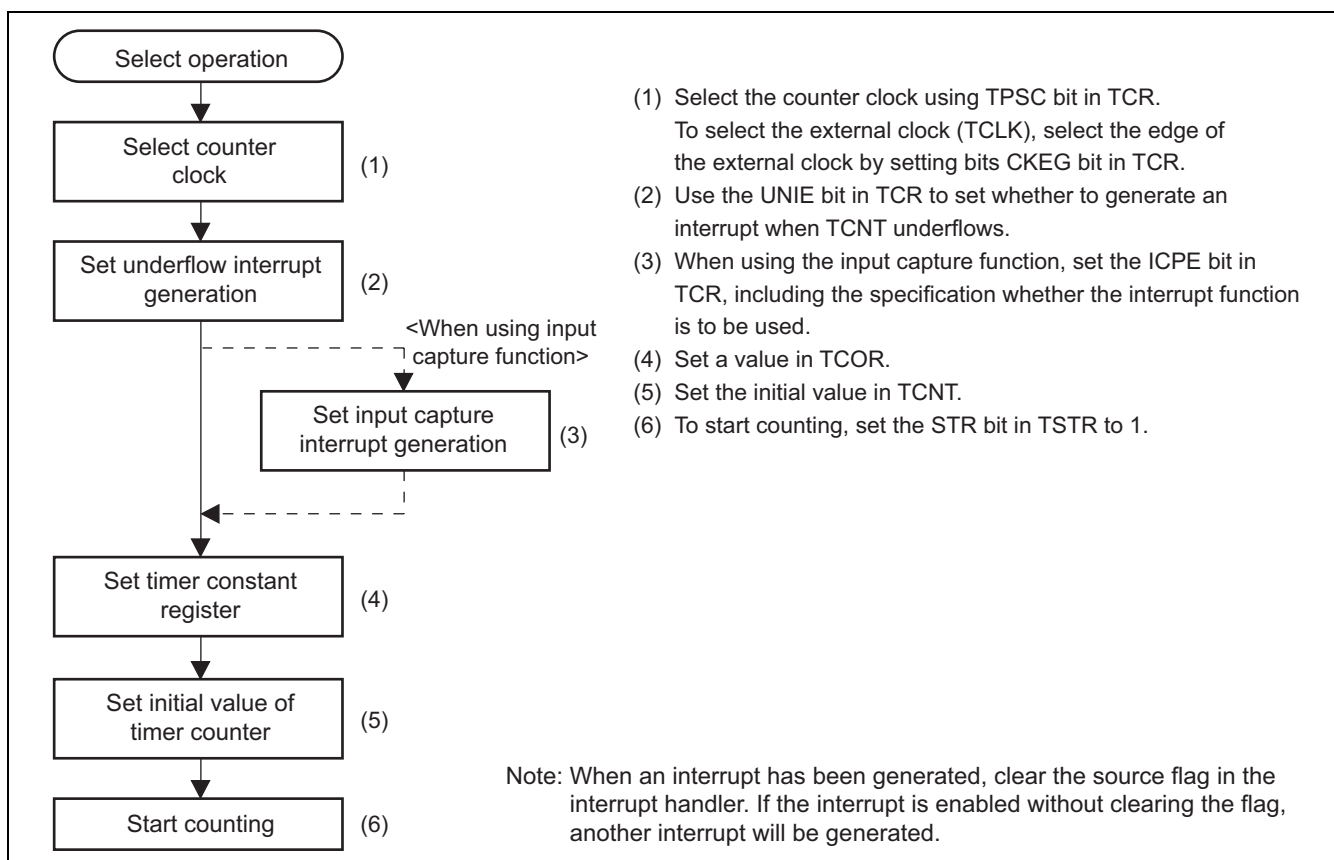
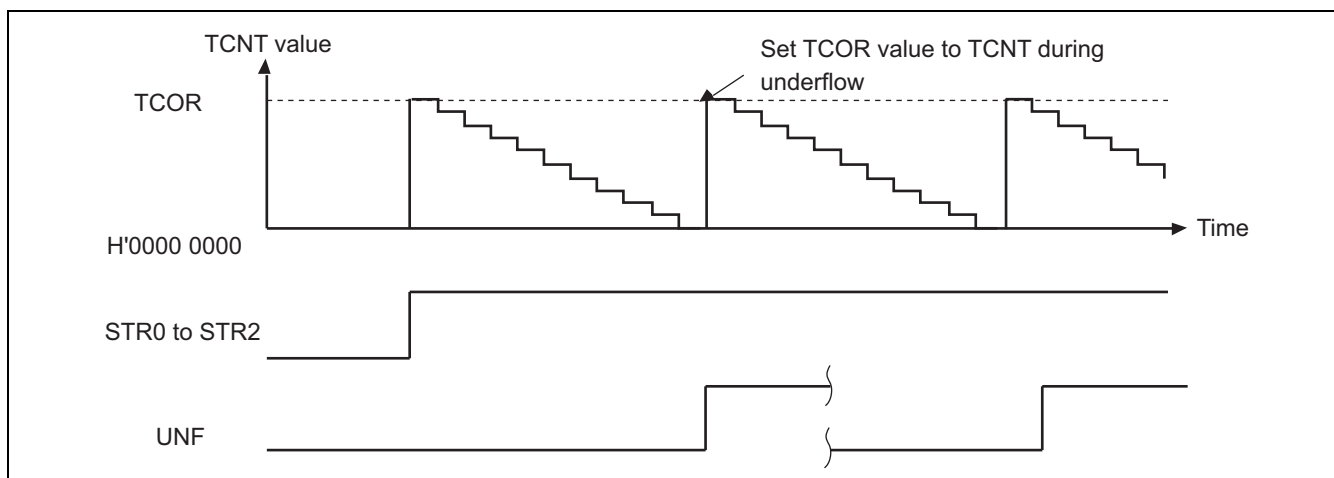


Figure 58.2 Procedure for Setting Count Operation

**(2) Auto-reload count operation**

Figure 58.3 shows the TCNT auto-reload operation.

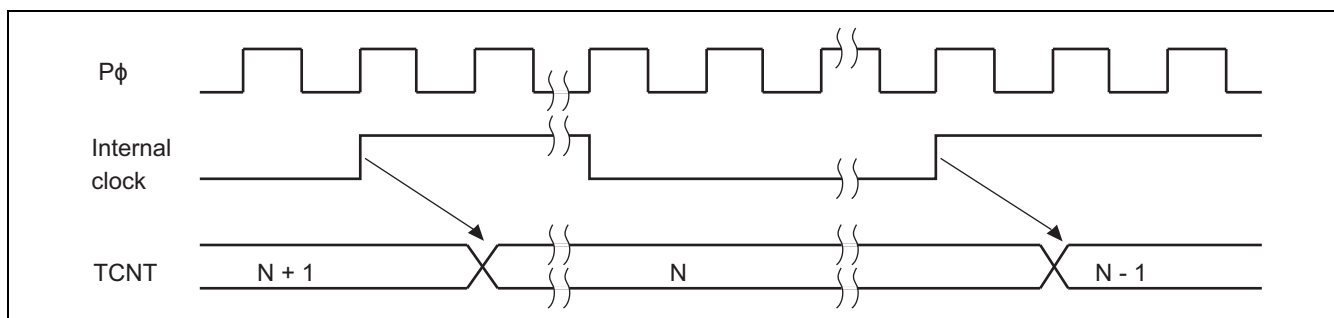


**Figure 58.3 TCNT Auto-Reload Operation**

**(3) TCNT count timing**

- Internal clock operation

Five clocks ( $P\phi/4$ ,  $P\phi/16$ ,  $P\phi/64$ ,  $P\phi/256$ ,  $P\phi/1024$ ) that are created by dividing peripheral clocks are selected as count clocks by setting bits TPSC2 to TPSC0 in TCR. Figure 58.4 shows the timing.

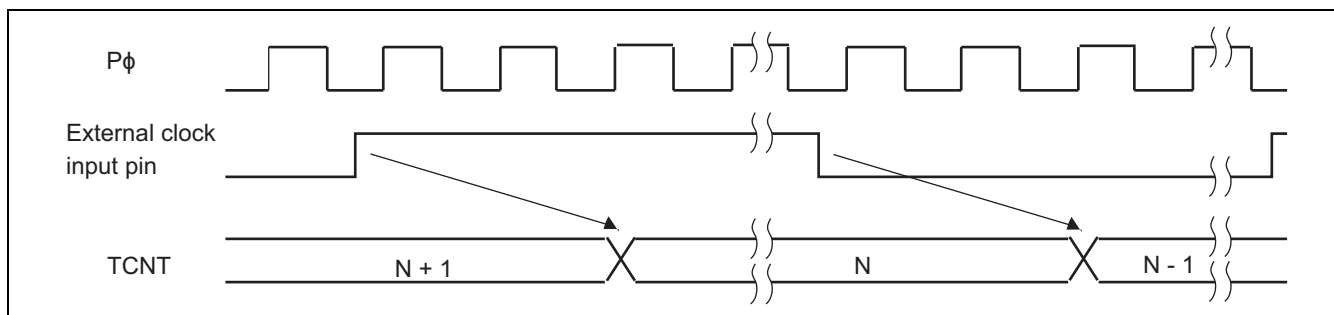


**Figure 58.4 Count Timing when Internal Clock is Operating**

- External clock operation

Set the bits TPSC3 to TPSC0 in TCR to select the external clock pin (TCLK) as the timer clock. Use the bits CKEG1 and CKEG0 in TCR to select the detection edge. Rise, fall, or both can be selected.

Figure 58.5 shows the timing for both-edge detection.



**Figure 58.5 Count Timing when External Clock is Operating**

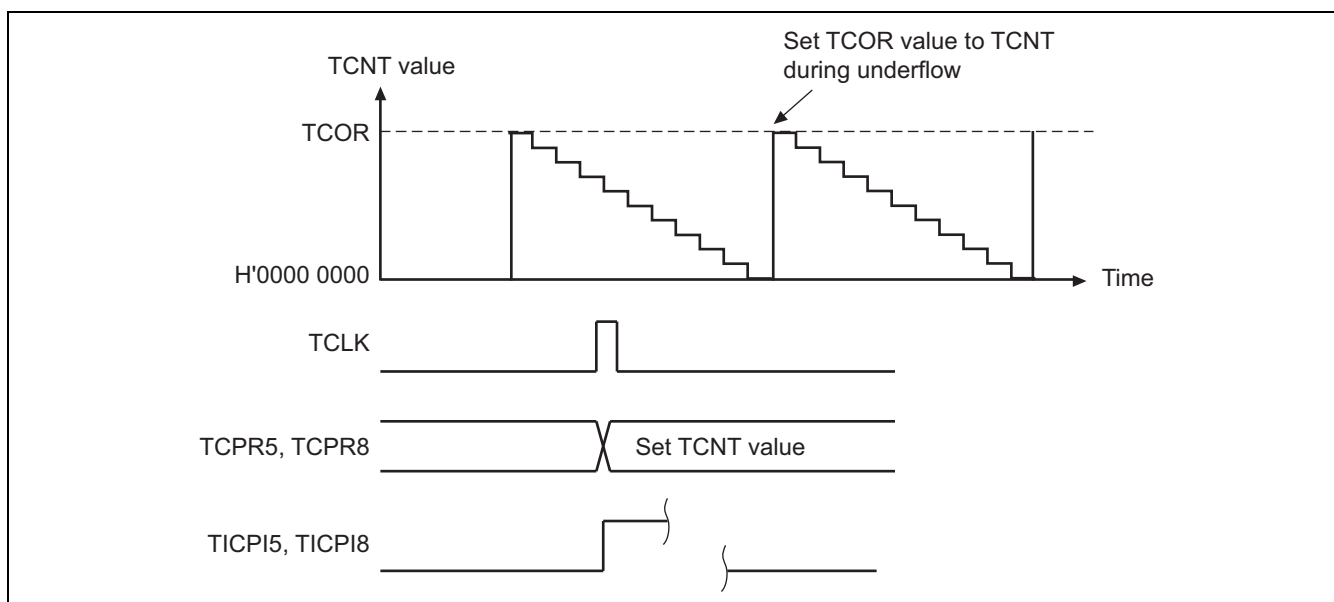
### 58.4.2 Input Capture Function

Channels 5 and 8 have the input capture function. When using the input capture function, follow the procedure shown below.

1. Set the timer operating clock as an internal clock with bits TPSC3 to TPSC0 in TCR.
2. Set use of the input capture function and whether to generate an interrupt on using it with bits ICPE1 and ICPE0 in TCR.
3. Specify either rising edge or falling edge of the TCLK pin to be used to set the value of TCNT to TCPR5 and TCPR8 with bits CKEG1 and CKEG0 in TCR.

Only when an input capture is occurred and the ICPF bits in TCR5 and TCR8 are 0, the values of TCNT5 and TCNT8 are set in TCPR5 and TCPR8, respectively.

Figure 58.6 shows the operating timing when the input capture function is used (the rising edge of TCLK is used).



**Figure 58.6 Operating Timing when Using Input Capture Function**

## 58.5 Interrupt

RZ/G1H	RZ/G1N
RZ/G1M	RZ/G1E

The TMU interrupt sources are underflow interrupt or input capture interrupt when the input capture function is used. The underflow interrupt is generated at each channel. The input capture interrupt is generated at channels 5 and 8 only.

An underflow interrupt request is generated (for each channel) when both the UNF bit and the interrupt enable bit for that channel are set to 1.

When the input capture function is used and the input capture request is generated, an interrupt request is generated if the ICPF bit in TCR5 or TCR8 is 1 and the input capture control bits ICPE1 and ICPE0 in TCR5 and TCR8 are 11.

Table 58.4 shows the TMU interrupt sources.

**Table 58.4 TMU Interrupt Sources**

Channel	Interrupt Sources	Description	RZ/G Series Products			
			RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
0	TUNI0	Underflow interrupt 0	√	√	√	√
1	TUNI1	Underflow interrupt 1	√	√	√	√
2	TUNI2	Underflow interrupt 2	√	√	√	√
3	TUNI3	Underflow interrupt 3	√	√	√	√
4	TUNI4	Underflow interrupt 4	√	√	√	√
5	TUNI5	Underflow interrupt 5	√	√	√	√
	TICPI5	Input capture interrupt 5	√	√	√	√
6	TUNI6	Underflow interrupt 6	√	√	√	√
7	TUNI7	Underflow interrupt 7	√	√	√	√
8	TUNI8	Underflow interrupt 8	√	√	√	√
	TICPI8	Input capture interrupt 8	√	√	√	√
9	TUNI9	Underflow interrupt 9	√	√	√	√
10	TUNI10	Underflow interrupt 10	√	√	√	√
11	TUNI11	Underflow interrupt 11	√	√	√	√

## 58.6 Usage Notes

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

### 58.6.1 Writing to Registers

When writing to the TMU registers, clear the start bits (STR11 to STR0) of the corresponding TSTR channel to stop the timer counting.

Writing to TSTR and clearing bits UNF and ICPF in TCR can be executed during counting. To clear flags UNF and ICPF during counting, do not change the values of bits other than those to be cleared.

### 58.6.2 Reading TCNT Register

Reading from TCNT is performed synchronously with the timer count operation. When timer counting and register read processing are performed simultaneously, the value before TCNT counting down is read.

### 58.6.3 External Clock Frequency

The frequency of external clock (TCLK) for each channel should be  $P\phi/4$  or less.



## 59. PWM Timer

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

### 59.1 Overview

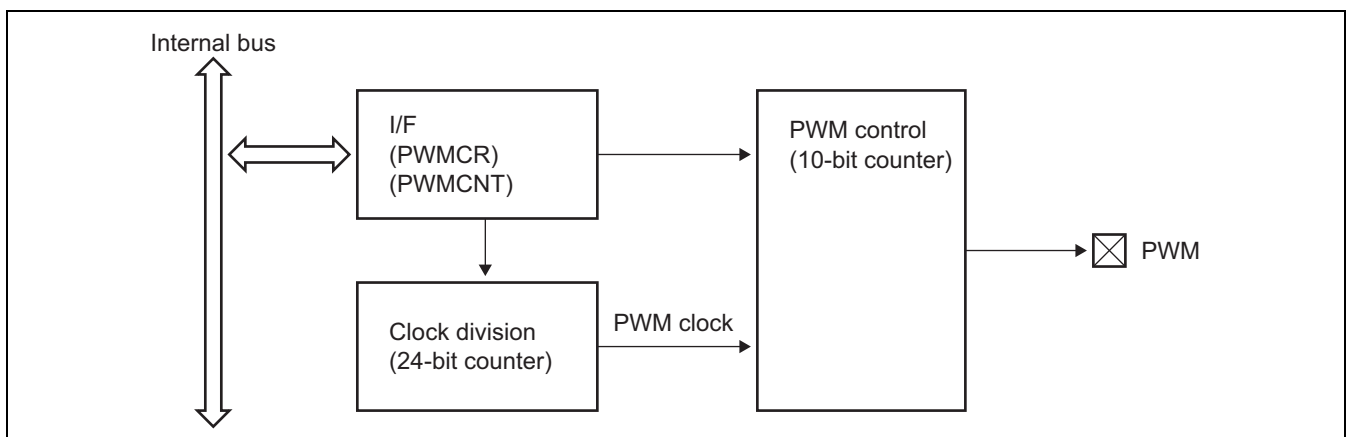
This LSI incorporates a seven-channel pulse width modulation (PWM) timer.

#### 59.1.1 Features

- PWM output cycle settable (10 bits)
- PWM output cycle settable within the range from 2 cycles to  $2^{24} \times 1024$  cycles of internal bus clock  $P\phi$  (i.e. from 30.77 ns to 264 seconds when  $P\phi = 65$  MHz)
- High-level width of the PWM output signal settable (10 bits)
- Continuous pulse output or single pulse output selectable

#### 59.1.2 Block Diagram

Figure 59.1 shows a block diagram of the PWM timer.



**Figure 59.1 Block Diagram of PWM Timer**

### 59.1.3 Input/Output pins

Table 59.1 shows the pin configuration of the PWM timer.

**Table 59.1 Pin Configuration**

Pin Name	I/O	Function	RZ/G Series Products			
			RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
PWM0	Output	PWM0 timer pulse output	√	√	√	√
PWM1	Output	PWM1 timer pulse output	√	√	√	√
PWM2	Output	PWM2 timer pulse output	√	√	√	√
PWM3	Output	PWM3 timer pulse output	√	√	√	√
PWM4	Output	PWM4 timer pulse output	√	√	√	√
PWM5	Output	PWM5 timer pulse output	√	√	√	√
PWM6	Output	PWM6 timer pulse output	√	√	√	√

### 59.1.4 Register Descriptions

Table 59.2 lists the registers of the PWM timer.

**Table 59.2 List of Registers**

Channel	Name	Abbreviation	R/W	Address	Access Size	RZ/G Series Products			
						RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
0	PWM control register	PWMCNT	R/W	H' E6E3 0000	32	√	√	√	√
	PWM count register	PWMCNT	R/W	H' E6E3 0004	32	√	√	√	√
1	PWM control register	PWMCNT	R/W	H' E6E3 1000	32	√	√	√	√
	PWM count register	PWMCNT	R/W	H' E6E3 1004	32	√	√	√	√
2	PWM control register	PWMCNT	R/W	H' E6E3 2000	32	√	√	√	√
	PWM count register	PWMCNT	R/W	H' E6E3 2004	32	√	√	√	√
3	PWM control register	PWMCNT	R/W	H' E6E3 3000	32	√	√	√	√
	PWM count register	PWMCNT	R/W	H' E6E3 3004	32	√	√	√	√
4	PWM control register	PWMCNT	R/W	H' E6E3 4000	32	√	√	√	√
	PWM count register	PWMCNT	R/W	H' E6E3 4004	32	√	√	√	√
5	PWM control register	PWMCNT	R/W	H' E6E3 5000	32	√	√	√	√
	PWM count register	PWMCNT	R/W	H' E6E3 5004	32	√	√	√	√
6	PWM control register	PWMCNT	R/W	H' E6E3 6000	32	√	√	√	√
	PWM count register	PWMCNT	R/W	H' E6E3 6004	32	√	√	√	√

Note: Do not access addresses other than those listed above. If access is attempted, a malfunction may occur.

**Table 59.3 Register States in Each Operating Mode**

<b>Name</b>	<b>Abbreviation</b>	<b>Power-on Reset</b>	<b>Module Standby</b>
PWM control register	PWMCR	H'0000 0000	Retained
PWM count register	PWMCNT	H'0000 0000	Retained

The registers of the PWM timer are mapped into the internal bus address space.

## 59.2 Register Description

Registers in the PWM timer are allocated to and arranged in the address space of the internal bus.

Legend for Register Description

Initial value: Register value after a reset

—: Undefined value

R/W: Readable/writable. The written value can be read.

R/WC0: Readable/writable. Writing 0 initializes the bit. Writing 1 is ignored.

R/WC1: Readable/writable. Writing 1 initializes the bit. Writing 0 is ignored.

R: Read-only. When the bit is reserved, the write value should always be 0.

—/W: Write-only. The read value is undefined.

## 59.2.1 PWM Control Register (PWMCR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	CC0			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CCMD	—	—	—	SYNC	—	—	—	—	—	—	SS0	—	—	—	EN0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R	R/W	R	R	R	R	R	R	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 20	—	All 0	R	Reserved The read value is always 0. The write value should always be 0.
19 to 16	CC0	0000	R/W	<p>Clock Control</p> <p>The clock frequency of the PWM counter is obtained by dividing the frequency of the clock signal P<math>\phi</math>.</p> <p>When the P<math>\phi</math> frequency is f MHz, the following PWM clock frequencies are obtained.</p> <p>0000: f MHz            0001: f MHz/2<sup>2</sup>            0010: f MHz/2<sup>4</sup>            0011: f MHz/2<sup>6</sup>            0100: f MHz/2<sup>8</sup>            0101: f MHz/2<sup>10</sup>            0110: f MHz/2<sup>12</sup>            0111: f MHz/2<sup>14</sup>            1000: f MHz/2<sup>16</sup>            1001: f MHz/2<sup>18</sup>            1010: f MHz/2<sup>20</sup>            1011: f MHz/2<sup>22</sup>            1100: f MHz/2<sup>24</sup></p> <p>When 1101, 1110, or 1111 is set, the PWM clock frequency is f MHz/2<sup>24</sup>.</p>

Bit	Bit Name	Initial Value	R/W	Description
15	CCMD	0	R/W	<p>CC0 Frequency Division Mode</p> <p>Changes the PWM clock frequency set by the clock control (CC0) bits.</p> <p>0: The PWM clock frequency set by CC0 is used.</p> <p>1: The PWM clock frequency set by CC0 is changed as follows:</p> <p>1 - 0000: <math>f \text{ MHz}/2</math></p> <p>1 - 0001: <math>f \text{ MHz}/2^3</math></p> <p>1 - 0010: <math>f \text{ MHz}/2^5</math></p> <p>1 - 0011: <math>f \text{ MHz}/2^7</math></p> <p>1 - 0100: <math>f \text{ MHz}/2^9</math></p> <p>1 - 0101: <math>f \text{ MHz}/2^{11}</math></p> <p>1 - 0110: <math>f \text{ MHz}/2^{13}</math></p> <p>1 - 0111: <math>f \text{ MHz}/2^{15}</math></p> <p>1 - 1000: <math>f \text{ MHz}/2^{17}</math></p> <p>1 - 1001: <math>f \text{ MHz}/2^{19}</math></p> <p>1 - 1010: <math>f \text{ MHz}/2^{21}</math></p> <p>1 - 1011: <math>f \text{ MHz}/2^{23}</math></p> <p>If 1100, 1101, 1110, or 1111 is set for CC0, the PWM clock frequency is <math>f \text{ MHz}/2^{24}</math> irrespective of the CCMD value.</p>
14 to 12	—	All 0	R	<p>Reserved</p> <p>The read value is always 0. The write value should always be 0.</p>
11	SYNC	0	R/W	<p>Specifies whether to allow the set values in the PWM count register (PWMCNT) to be reflected in the timer operation synchronously with setting the PWM control register (PWMCR).</p> <p>0: Allows the PWMCNT set values to be reflected in the timer operation irrespective of PWMCR setting.</p> <p>1: Allows the PWMCNT set values to be reflected in the timer operation synchronously with PWMCR setting.</p> <p>For details, refer to section 59.3, Description of Operation.</p>
10 to 5	—	All 0	R	<p>Reserved</p> <p>The read value is always 0. The write value should always be 0.</p>
4	SS0	0	R/W	<p>Single Pulse Output</p> <p>0: The timer operates in continuous pulse output mode.</p> <p>1: The timer operates only for a single cycle and then stops.</p>
3 to 1	—	All 0	R	<p>Reserved</p> <p>The read value is always 0. The write value should always be 0.</p>
0	EN0	0	R/W	<p>Channel Enable</p> <p>0: The channel is held in the idle state, and outputs a high level.</p> <p>1: The channel outputs high and low levels in a predetermined cycle.</p> <p>This bit is automatically cleared in single pulse output mode.</p>

### 59.2.2 PWM Count Register (PWMCNT)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	CYC0									
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	PH0									
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 26	—	All 0	R	Reserved The read value is always 0. The write value should always be 0.
25 to 16	CYC0	H'000	R/W	PWM Cycle Sets the PWM output cycle. The cycle set by these bits is the sum of the high-level and low-level periods. Setting H'000 is prohibited.
15 to 10	—	All 0	R	Reserved The read value is always 0. The write value should always be 0.
9 to 0	PH0	H'000	R/W	PWM High-Level Period Sets the period for which the PWM timer outputs a high-level signal. Setting H'000 is prohibited.

Note: For the CYC0 and PH0 bits, set the number of cycles to be counted of the PWM clock signal whose frequency has been set by the CC0 and CCMD bits in the PWM control register.

### 59.3 Description of Operation

RZ/G1H

RZ/G1N

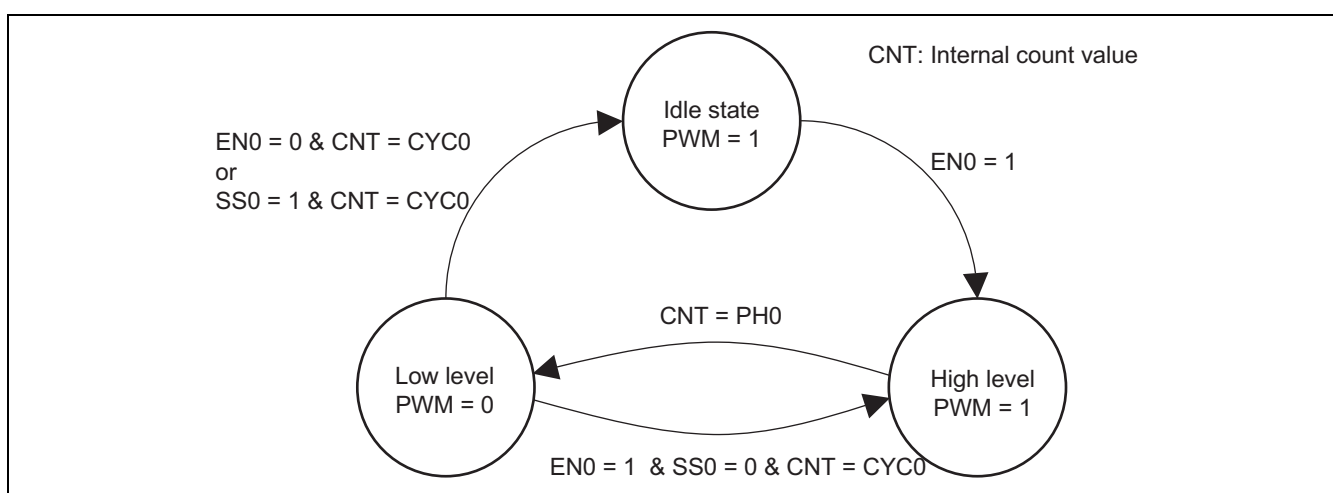
RZ/G1M

RZ/G1E

The duty ratio of a PWM output pulse can be obtained by setting a high-level period and a cycle. The timer channel counts the PWM clock signal pulses using a 10-bit counter to generate the PWM output pulse having the specified period and cycle. When the channel function is enabled ( $EN0 = 1$ ), the timer outputs a high level until the counter value reaches the value set in the PH0 bits of the PWM count register (PWMCNT). The output goes low when the PH0 value is reached, and is held low until the counter value reaches the value set in the CYC0 bits of PWMCNT. When the CYC0 value is reached, the output goes high and the counter is reset.

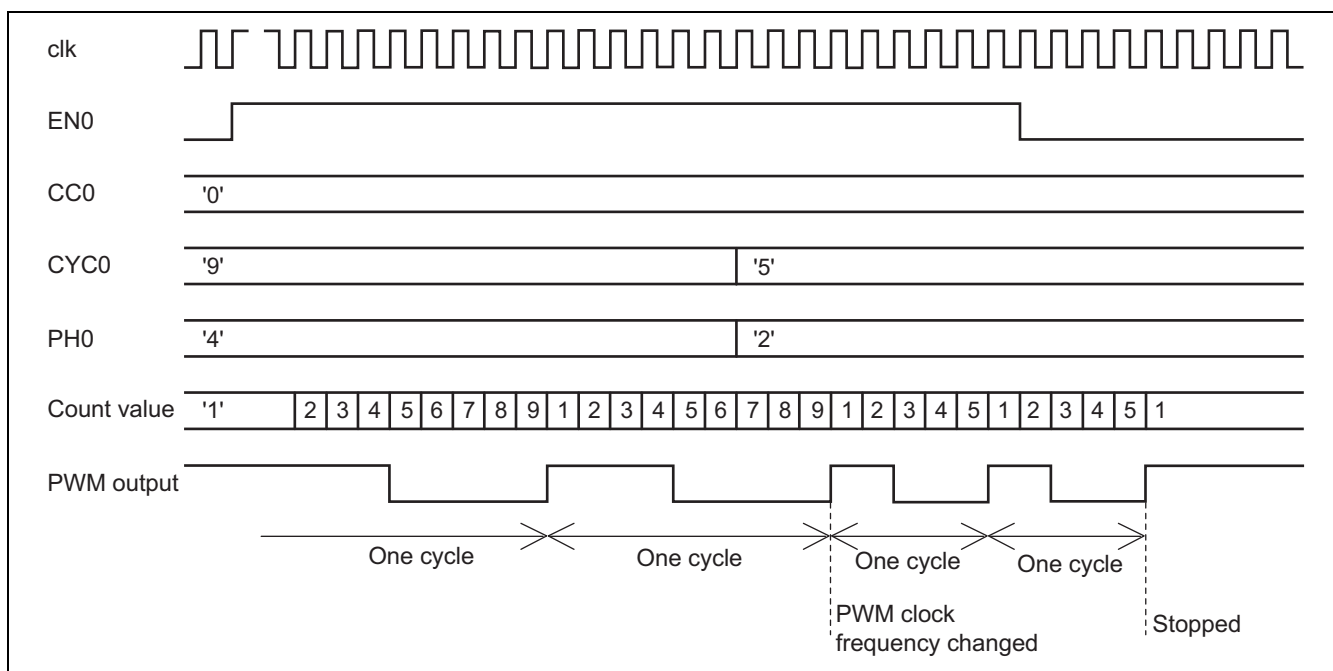
Unless the channel function is enabled, the output is held high, and the counter is held in the reset state.

Figure 59.2 shows the PWM state transition during the operation described above.



**Figure 59.2 PWM Timer State Transition**

Note that after a channel has been enabled by writing 1 to  $EN0$ , the number of clock pulses before output of the first falling edge from a channel is greater than the value set in the PWM control register and PWM count register by up to four cycles of the  $P\phi$  clock. After that, the PWM output rises and falls according to a set timing. Figure 59.3 schematically shows this output timing. This figure shows an internal operation.



**Figure 59.3 PWM Output Timing**

1. The period from enabling the channel to the first falling edge output from the channel is the sum of a set value and up to four cycles of the  $P\phi$  clock.
2. After that, the PWM high and low widths are the same as the set values.
3. When the PWM count register is changed during operation ( $EN0 = 1$ ), timing of the output will be in accord with the new settings after output of the current cycle has been completed.
4. When the CC0 and CCMD bit values in the PWM control register are changed during operation ( $EN0 = 1$ ), timing of the output will be in accord with the new settings after output of the current cycle has been completed.
5. To stop the timer operation, write 0 to the EN0 bit. The timer stops operation after completing the output of the current cycle. Note that, however, if 1 is written to EN0 again before completing the output of the current cycle, the timer does not stop but continues to operate.
6. For the PWM timer output, continuous pulse output mode and single pulse output mode are supported. In continuous pulse output mode, the timer outputs pulses continuously while EN0 is 1. In single pulse output mode, the timer outputs a single pulse. In this mode, EN0 is automatically cleared.
7. To change the values of the clock control bits (CC0) and the CC0 frequency division mode bit (CCMD) in the PWMCR register and of the PWM cycle bits (CYC0) and the PWM high-level period bits (PH0) in the PWMCNT register at the same time during the PWM operation, the following procedure should be followed:
  1. Write 1 to the SYNC bit. (Write the original set values to the other bits in PWMCR.)
  2. Change the PWMCNT value.
  3. Change the CC0 and CCMD values in PWMCR. (Write the original set values to the other bits in PWMCR. The SYNC bit should be held at 1.)

By following the above procedure, the new PWMCNT value is reflected in the timer operation synchronously with PWMCR setting.

When changing only the PWMCNT value while SYNC = 1, writing to PWMCR is required after changing the PWMCNT value. In this case, write the same values as the original set values to the PWMCR bits. On the other hand, when changing only the PWMCR value, writing to PWMCNT is not required.

If PWMCNT and PWMCR values are changed while SYNC = 0, the change to the values might not be completed within a single PWM output cycle but actually take two or more cycles. This may disturb the period or duty cycle of the PWM output.

Note that, when the PWCNT value is changed while SYNC = 1, the new values are read from PWMCNT even before PWMCR is set.



## 59.4 Usage Note

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

When using the PWM timer, note the following points.

When the CYC0 value is equal to or smaller than PH0 value in the PWM count register, the PWM output is held high. In this case, to start pulse output, clear EN0 to 0, set CYC0 to the value greater than the PH0 value, and then set EN0 to 1.

Note that, a maximum period equivalent to  $CYC0 = H'3FF$  at the set PWM clock frequency may be required before pulse output is started.

## 60. Thermal Sensor (THS/TSC)

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

### 60.1 Overview

This LSI provides a thermal sensor module that measures the temperature ( $T_j$ ) inside the LSI.

#### 60.1.1 Features

- (1) Measures temperature  $T_j$  with an accuracy of  $\pm 5^\circ\text{C}$  over the range of temperatures from  $-40^\circ\text{C}$  to  $125^\circ\text{C}$ .
- (2) Provides reference to temperature  $T_j$  as measured from outside the chip with the use of external LSI pins (VTHREF and VTHSENSE).
- (3) Provides reference to the result of measuring the temperature in  $5^\circ\text{C}$  units by access to registers.
- (4) Capable of generating interrupts when the detected temperature  $T_j$  within the LSI rises above or falls below a specified temperature.
- (5) Capable of removing noise due to the detection of rises and falls in the temperature by applying a chattering prevention circuit.

#### 60.1.2 Block Diagram

The block diagram of the thermal sensor module is shown below. The thermal sensor consists of the thermal sensor (THS) which is an analog circuit for measuring temperature and the thermal sensor controller (TSC) which controls the analog circuit.

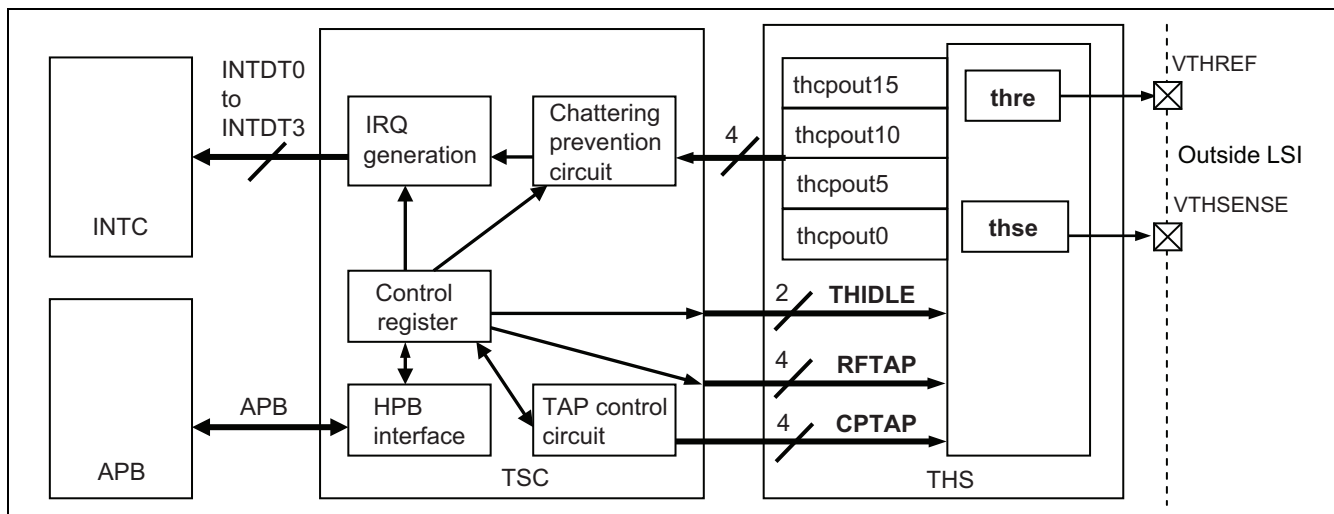


Figure 60.1 THS/TSC Block Diagram

Three signals THIDLE, RFTAP (4 bits) and CPTAP (4 bits) are output from the TSC to the THS. THIDLE stops or starts the THS operation, RFTAP adjusts the analog circuit operation, and CPTAP specifies the temperature range to be measured by the thermal sensor. Setting the CPTAP bits determines the reference temperature for measurement, and the THS determines if the chip temperature is above  $0^\circ\text{C}$ ,  $5^\circ\text{C}$ ,  $10^\circ\text{C}$ , or  $15^\circ\text{C}$  of the reference temperature. For CPTAP, either of the following can be selected: the use of the fixed value specified by the register or the use of the value determined by the TAP control circuit so that the temperatures near the current chip temperature can be measured.

Note: In the RZ/G series products, RFTAP and CPTAP are determined automatically by hardware by setting the CPCTL bit in the THSCR register to 1.

Four signals, thecpout0, thecpout5, thecpout10, and thecpout15, are output from the THS to the TSC. These signals indicate the temperature measured by the thermal sensor; whether or not the chip temperature is above 0°C, 5°C, 10°C, or 15°C of the reference temperature. Through use of the registers in the TSC, the chip temperature calculated from these signals can be read and temperature rise or drop can be notified by generating an interrupt on the rising or falling edge of these signals. In addition, the chattering prevention circuit in the TSC prevents the noise generated in the analog circuit.

The THS is provided with two pins that output voltage to the outside of the LSI. The chip temperature can be measured from outside the chip by measuring the voltages on these pins.

### 60.1.3 External Pins

**Table 60.1 Pin Configuration**

Pin Name	Symbol	I/O	Function
Thermal sensor output voltage	VTHSENSE	Analog I/O	Outputs a voltage correlated with the temperature T <sub>j</sub> in the LSI.
Thermal sensor output reference voltage	VTHREF	Analog I/O	Outputs a reference voltage used to convert the voltage output from the VTHSENSE pin into a digital signal.

For details, refer to section 60.3.4, Temperature Measurement Using External Pins.

### 60.1.4 Register Configuration

Table 60.2 shows the list of registers. The base address is H'E61F 0000.

Any address other than those listed in the table must not be written to. Otherwise, correct operation is not guaranteed. The read value is undefined.

**Table 60.2 Register Configuration**

Register Name	Abbreviation	R/W	Address	Initial Value	Access Size	RZ/G Series Products			
						RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Interrupt status register	STR	R	H'000	H'0000 0000	32	√	√	√	—
Interrupt enable register	ENR	R/W	H'004	H'0000 0000	32	√	√	√	—
Interrupt mask register	INT_MASK	R/W	H'00C	H'000F 0F0F	32	√	√	√	—
Positive/negative logic select register	POSNEG	R/W	H'120	H'0000 0001	32	√	√	√	—
Edge/level sensing select register	EDGLEVEL	R/W	H'124	H'0000 000F	32	√	√	√	—
Chattering prevention ON/OFF setting register	FILONOFF	R/W	H'128	H'0000 000F	32	√	√	√	—
THS control register	THSCR	R/W	H'12C	H'0000 0003	32	√	√	√	—
THS status register	THSSR	R	H'130	H'0xxx 00xx	32	√	√	√	—
Interrupt control register	INTCTRL	R/W	H'134	H'2500 0000	32	√	√	√	—

## 60.2 Register Description

[Legend for register description]

Initial value: Register value after a reset

—: Undefined value

R/W: Readable/writable. The written value can be read.

Data is accessed in longword units.

### 60.2.1 Interrupt Status Register (STR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

Function: When an interrupt signal is input from the THS, 1 is set to this register. To clear the status, 0 should be written to or read from this register.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	PRTFLG	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	Tj03ST	Tj02ST	Tj01ST	Tj00ST
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	—	0	R/W	Reserved
30	PRTFLG	0	R/W	Interrupt Temperature Status Flag 0: Normal operation 1: This bit is set to 1 when the internal temperature in the LSI exceeds the threshold temperature that has been specified in the INTCTLR register. This bit is cleared to 0 by writing 0 after the Tj*ST bit in the STR register has been cleared.
29 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3	Tj03ST	0	R/W	Tj03 Detection Status 0: Not detected. 1: The Tj03 threshold temperature specified by CTEMP3[5:0] in the INTCTLR register is detected. This bit is cleared by writing or reading 0.
2	Tj02ST	0	R/W	Tj02 Detection Status 0: Not detected. 1: The Tj02 threshold temperature specified by CTEMP2[5:0] in the INTCTLR register is detected. This bit is cleared by writing or reading 0.
1	Tj01ST	0	R/W	Tj01 Detection Status 0: Not detected. 1: The Tj01 threshold temperature specified by CTEMP1[5:0] in the INTCTLR register is detected. This bit is cleared by writing or reading 0.
0	Tj00ST	0	R/W	Tj00 Detection Status 0: Not detected. 1: The Tj00 threshold temperature specified by CTEMP0[5:0] in the INTCTLR register is detected. This bit is cleared by writing or reading 0.

### 60.2.2 Interrupt Enable Register (ENR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

Function: ENR controls enabling or disabling the interrupt output from the THS.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	Tj03_EN	Tj02_EN	Tj01_EN	Tj00_EN
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3	Tj03_EN	0	R/W	Enables comparing the CTEMP3[5:0] bits in the INTCTLR register with the CTEMP[5:0] bits in the THSSR register. 0: Disable 1: Enable
2	Tj02_EN	0	R/W	Enables comparing the CTEMP2[5:0] bits in the INTCTLR register with the CTEMP[5:0] bits in the THSSR register. 0: Disable 1: Enable
1	Tj01_EN	0	R/W	Enables comparing the CTEMP1[5:0] bits in the INTCTLR register with the CTEMP[5:0] bits in the THSSR register. 0: Disable 1: Enable
0	Tj00_EN	0	R/W	Enables comparing the CTEMP0[5:0] bits in the INTCTLR register with the CTEMP[5:0] bits in the THSSR register. 0: Disable 1: Enable

### 60.2.3 Interrupt Mask Register (INT\_MASK)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

Function: INT\_MASK masks output of an interrupt request signal to the INTC.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	Tj03INT_MSK	Tj02INT_MSK	Tj01INT_MSK	Tj00INT_MSK
Initial value:	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 20	—	All 0	R/W	Reserved These bits are always read as 0. The write value should always be 0.
19 to 16	—	All 1	R/W	Reserved These bits are always read as 1. The write value should always be 1.
15 to 12	—	All 0	R/W	Reserved These bits are always read as 0. The write value should always be 0.
11 to 8	—	All 1	R/W	Reserved These bits are always read as 1. The write value should always be 1.
7 to 4	—	All 0	R/W	Reserved These bits are always read as 0. The write value should always be 0.
3	Tj03INT_MSK	1	R/W	Selects whether or not the Tj03 interrupt request is masked when Tj03ST in the STR register is 1. 0: Mask is cleared. 1: Masked.
2	Tj02INT_MSK	1	R/W	Selects whether or not the Tj02 interrupt request is masked when Tj02ST in the STR register is 1. 0: Mask is cleared. 1: Masked.
1	Tj01INT_MSK	1	R/W	Selects whether or not the Tj01 interrupt request is masked when Tj01ST in the STR register is 1. 0: Mask is cleared. 1: Masked.
0	Tj00INT_MSK	1	R/W	Selects whether or not the Tj00 interrupt request is masked when Tj00ST in the STR register is 1. 0: Mask is cleared. 1: Masked.

**60.2.4 Positive/Negative Logic Select Register (POSNEG)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

Function: POSNEG selects rising edge detection (positive logic) or falling edge detection (negative logic) of the interrupt input signal. Set this register before setting mode.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	POSNEG3-0			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3 to 0	POSNEG3 to POSNEG0	0001	R/W	Selects the edge polarity of the interrupt input signal. 0: Detects a rising edge. (An interrupt is generated when Tj rises above a specified temperature.) 1: Detects a falling edge. (An interrupt is generated when Tj falls below a specified temperature.)



### 60.2.5 Edge/Level Sensing Select Register (EDGLEVEL)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

Function: EDGLEVEL selects edge detection for the interrupt input ports.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	EDGLEVEL3-0			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3 to 0	EDGLEVEL3 to EDGLEVEL0	1111	R/W	Specifies the method to detect interrupt signal input. Select edge detection. 0: Selects level detection. (Setting prohibited) 1: Selects edge detection. Use the thermal sensor with this field set to the initial value.

**60.2.6 Chattering Prevention ON/OFF Setting Register (FILONOFF)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

Function: FILONOFF turns on or off chattering input prevention.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	FILONOFF3-0			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3 to 0	FILONOFF3 to FILONOFF0	1111	R/W	Turns on or off the chattering prevention circuit. 0: Chattering prevention is off. 1: Chattering prevention is on.

When chattering prevention is on, an interrupt input signal is sampled four times in 25 μs cycles\*. An interrupt is generated only when the same input level is detected four times. When the same input level is detected three or less times of sampling, it is judged as chattering and an interrupt is not generated. Accordingly, when the filtering function is used, an input signal needs to be four or more clock cycles long for 100 μs cycle sampling.

Note: \* Since the clock used is generated by dividing cpck by 335, one cycle is 22 μs when cpck is 15 MHz.

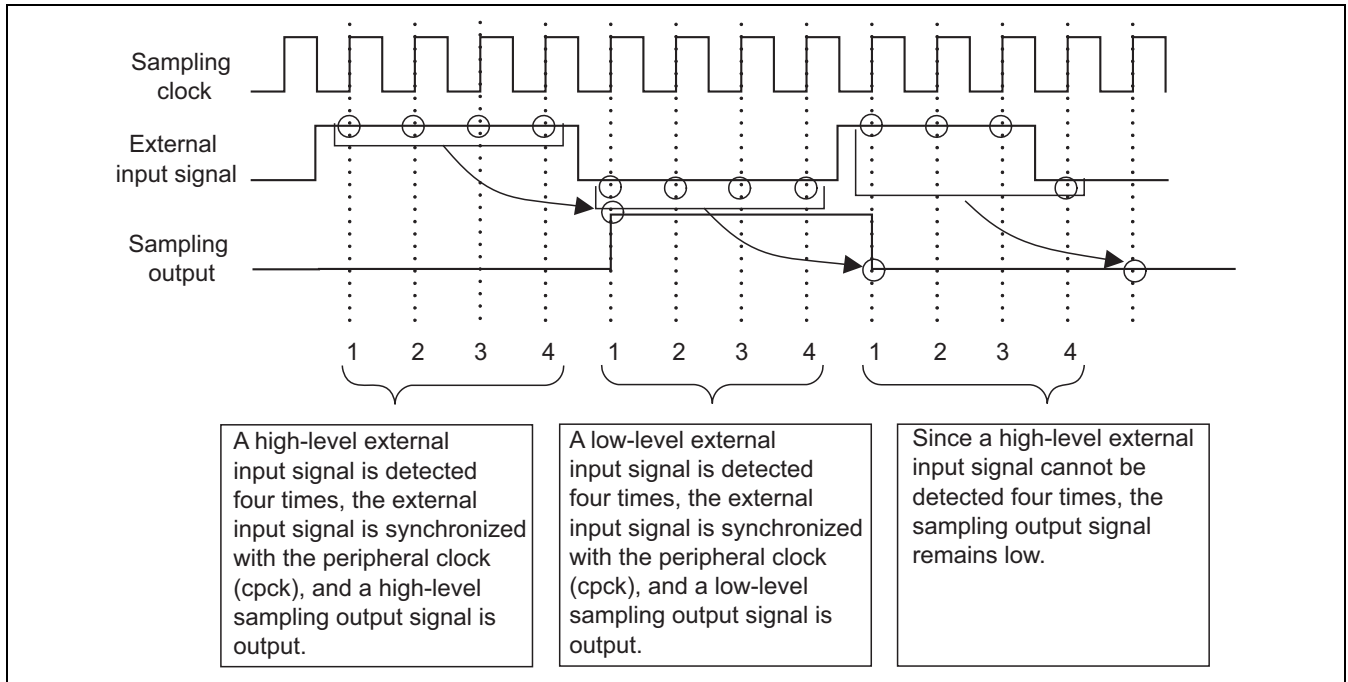


Figure 60.2 Sampling Timing Chart

### 60.2.7 THS Control Register (THSCR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

Function: THSCR specifies the THS operating mode.

The THS is in the operating state in the initial state. When not using the thermal sensor, place it in the idle state by setting this register. This register also selects the method to set the comparator offset, and sets an offset value.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	CPCTL	—	—	THIDLE1-0	RFTAP3-0			CPTAP3-0					
Initial value:	0	0	0	0	0	0	0	0	-	-	-	-	0	0	1	1
R/W:	R	R	R	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12	CPCTL	0	R/W	Specifies the method to set the offset (CPTAP) of the comparator in the THS. 0: Setting prohibited 1: TAP value is determined automatically by hardware. When 1 is set, an offset value appropriate for measuring the current chip temperature is selected by hardware. For details, refer to section 60.3.3, Temperature Measurement Using Register (When CPCTL = 1). Note: Set this bit to 1 when using the thermal sensor.
11, 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9, 8	THIDLE1, THIDLE0	00	R/W	Selects either the normal operating state or the idle state of the THS. 00: Normal operating state 01: Setting prohibited 10: Normal operating state (output from VTHSENSE or VTHREF is stopped) 11: Idle state Set this bit to 11 (idle state) when the thermal sensor is not used.
7 to 4	RFTAP3 to RFTAP0	—	R/W	Sets an offset value (RFTAP) of the op amp in the THS. Note: These bits are determined automatically by hardware. The write value should always be same value with read value just before.
3 to 0	CPTAP3 to CPTAP0	H'3	R/W	Sets the offset value (CPTAP) of the comparator in the THS. Note: These bits have no effect.

**60.2.8 THS Status Register (THSSR)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

Function: THSSR indicates the status of the thermal sensor.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	—	—	—	—	—	—	—	—	0	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	CTEMP5-0					
Initial value:	0	0	0	0	0	0	0	0	0	0	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 28	—	All 0	R	Reserved These bits are always read as the initial value. The write value should always be the initial value.
27 to 24	—	—	R	Reserved The read value is undefined.
23 to 20	—	—	R	Reserved The read value is undefined.
19	—	0	R	Reserved This bit is always read as the initial value. The write value should always be the initial value.
18 to 16	—	—	R	Reserved The read value is undefined.
15 to 6	—	All 0	R	Reserved These bits are always read as the initial value. The write value should always be the initial value.
5 to 0	CTEMP5 to CTEMP0	—	R	Indicates the current temperature. Convert the value of the bits to actual temperature (°C) by the following formula. $T = CTEMP[5:0] \times 5 - 65$

### 60.2.9 Interrupt Control Register (INTCTLR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

Function: INTCTLR controls the interrupts of the thermal sensor.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	CTEMP3						—	—	CTEMP2					
Initial value:	0	0	1	0	0	1	0	1	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	CTEMP1						—	—	CTEMP0					
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31, 30	—	All 0	R	Reserved These bits are always read as the initial value. The write value should always be the initial value.
29 to 24	CTEMP3	H'25	R/W	Indicates the temperature that causes an INTDT3 interrupt. Specify the value calculated by “((interrupt temperature) + 65) / 5.” The INTDT3 interrupt is generated when the CPCTL bit (bit 12) in THSCR is 1 and the following condition is satisfied: CTEMP3 ≥ CTEMP (when POSNEG3 is 1) or CTEMP3 < CTEMP (when POSNEG3 is 0). Here CTEMP is the current chip temperature indicated with bits 5 to 0 in THSSR.
23, 22	—	All 0	R	Reserved These bits are always read as the initial value. The write value should always be the initial value.
21 to 16	CTEMP2	H'00	R/W	Indicates the temperature that causes an INTDT2 interrupt. Specify the value calculated by “((interrupt temperature) + 65) / 5.” The INTDT2 interrupt is generated when the CPCTL bit (bit 12) in THSCR is 1 and the following condition is satisfied: CTEMP2 ≥ CTEMP (when POSNEG2 is 1) or CTEMP2 < CTEMP (when POSNEG2 is 0). Here CTEMP is the current chip temperature indicated with bits 5 to 0 in THSSR.
15, 14	—	All 0	R	Reserved These bits are always read as the initial value. The write value should always be the initial value.

Bit	Bit Name	Initial Value	R/W	Description
13 to 8	CTEMP1	H'00	R/W	<p>Indicates the temperature that causes an INTDT1 interrupt.</p> <p>Specify the value calculated by “((interrupt temperature) + 65) / 5.”</p> <p>The INTDT1 interrupt is generated when the CPCTL bit (bit 12) in THSCR is 1 and the following condition is satisfied:</p> <p>CTEMP1 <math>\geq</math> CTEMP (when POSNEG1 is 1) or            CTEMP1 &lt; CTEMP (when POSNEG1 is 0).</p> <p>Here CTEMP is the current chip temperature indicated with bits 5 to 0 in THSSR.</p>
7, 6	—	All 0	R	<p>Reserved</p> <p>These bits are always read as the initial value. The write value should always be the initial value.</p>
5 to 0	CTEMP0	H'00	R/W	<p>Indicates the temperature that causes an INTDT0 interrupt.</p> <p>Specify the value calculated by “((interrupt temperature) + 65) / 5.”</p> <p>The INTDT0 interrupt is generated when the CPCTL bit (bit 12) in THSCR is 1 and the following condition is satisfied:</p> <p>CTEMP0 <math>\geq</math> CTEMP (when POSNEG0 is 1) or            CTEMP0 &lt; CTEMP (when POSNEG0 is 0).</p> <p>Here CTEMP is the current chip temperature indicated with bits 5 to 0 in THSSR.</p>

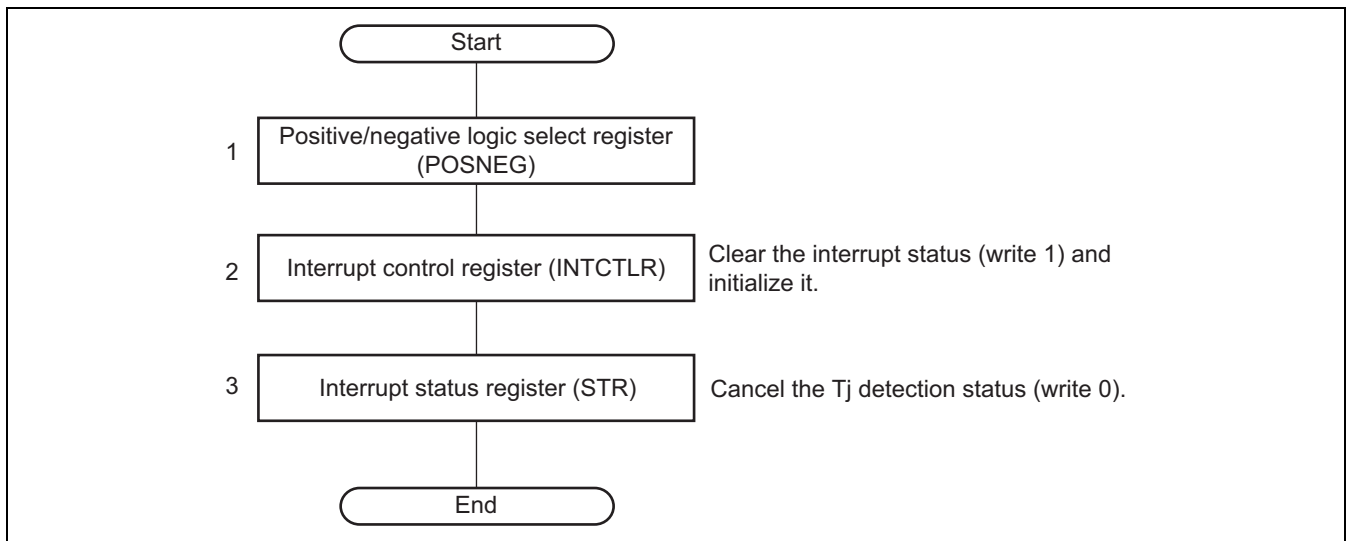
### 60.3 Operation

RZ/G1H	RZ/G1N
RZ/G1M	RZ/G1E

#### 60.3.1 Flow of Register Initialization

Shown below is flow of register initialization for the thermal sensor.

If the settings of (1) are changed, an unexpected interrupt may be generated within the module. In that case, cancel the interrupt with steps (2) and (3) before using the thermal sensor.



**Figure 60.3 Flow of Register Initialization**



### 60.3.2 Temperature Measurement Using Register (When CPCTL = 0)

Setting is prohibited.

### 60.3.3 Temperature Measurement Using Register (When CPCTL = 1)

The following describes the method to measure the chip temperature by using a comparator offset value determined by the TAP control circuit. Setting the CPCTL bit (bit 12) in THSCR to 1 allows an offset value to be determined by the TAP control circuit.

The TAP control circuit increases an offset value by 1 when the chip temperature is determined to rise above the upper limit of the measurable temperature range, and decreases it by 1 when determined to fall below the lower limit. Such determination is performed by detecting a low-to-high transition of thcpout15 or a high-to-low transition of thcpout0. Note that, an offset value cannot be less than 0 or 15 or more.

Once an offset value is changed, the value is not changed again for 300  $\mu$ s.

When reading the temperature measurement result from a register, read the value of the CTEMP5 to CTEMP0 bits in THSSR.

Do not use the value of the CTEMP5 to CTEMP0 bits in THSSR immediately after a change to the offset value for the TAP control circuit because the new offset setting will not yet have been reflected in the value. When CPCTL is 1, hardware automatically updates the offset value but since software is not informed of the timing of updates, consecutively read the value of the CTEMP5 to CTEMP0 bits in THSSR at an interval of at least 300  $\mu$ s and only accept the result when the same value is read twice (since the temperature changes more gradually than the 300  $\mu$ s interval, as long as a change to the offset value is not made during the interval between reading of the CTEMP5 to CTEMP0 bits in THSSR, the same value will be read out.)

By setting 0 or 1 in the positive/negative logic select register (POSNEG) and specifying the temperatures that cause interrupts in the INTCTLR register, the INTDT3 to INTDT0 interrupts can be generated when the chip temperature rises above or falls below the temperatures specified in the INTCTLR register.

However, immediately after a change to the offset value for the TAP control circuit, an interrupt may be generated before completion of the temperature measurement at the changed offset value. If an interrupt is generated at such a time, read out the value of the CTEMP5 to CTEMP0 bits in THSSR a second time after 300  $\mu$ s, check whether or not the interrupt was valid, and if it was, proceed with interrupt processing.

### 60.3.4 Temperature Measurement Using External Pins

For temperature measurement with the external pins, connect the external circuit to the VTHSENSE and VTHREF pins and calculate the temperature based on the output voltages on these pins.

#### (1) External Pins Used for Temperature Measurement

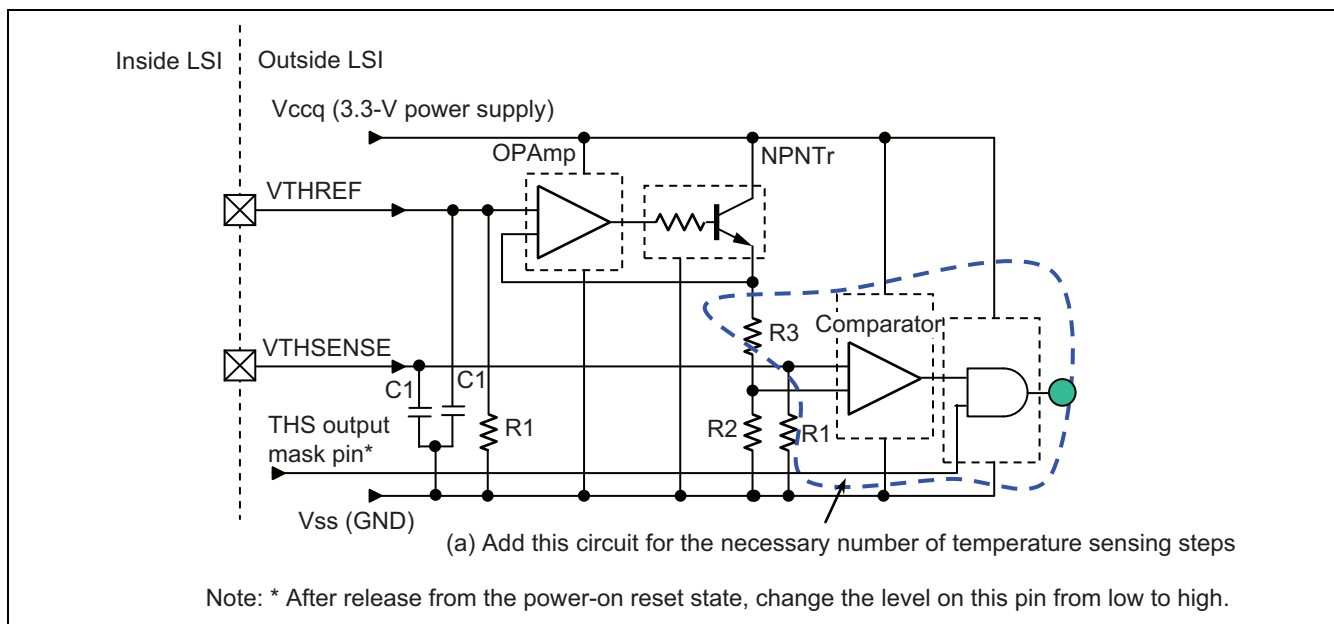
In temperature measurement with the external pins, the pins shown in Table 60.3 are used.

**Table 60.3 External Pins Used for Temperature Measurement**

Pin Name	Output Voltage Range [V]	Maximum Allowed Input/Output Current [ $\mu$ A]	Tj Accuracy
VTHSENSE	360 mV (min.) to 750 mV (max.)	$\pm 8$	The accuracy of Tj is $\pm 5^\circ\text{C}$ max. {(VHTREF - VTHSENSE) specification} (This does not include error such as device accuracy of the recommended external connection circuit).  The temperature range for detection is $-40^\circ\text{C}$ to $125^\circ\text{C}$ .  When Tj is outside the range of $-40^\circ\text{C}$ to $125^\circ\text{C}$ , the operation and accuracy cannot be guaranteed.
VTHREF	1.18 V (min.) to 1.32 V (max.)	$\pm 8$	

#### (2) Recommended External Connection Circuit

Figure 60.4 shows a recommended external connection circuit for the THS used for temperature measurement with the external pins.



**Figure 60.4 Recommended External Connection Circuit for THS**

The recommended external connection circuit outputs a high level at a desired temperature. By using VTHREF, which is affected by the noise equal to the external noise that affects VTHSENSE, the external noise is canceled out, and thus the accuracy of Tj is improved.

In addition, the number of steps for digitizing a measured temperature Tj (the number of temperatures with which an actual temperature is compared) can be increased by adding the circuit part indicated with (a) in the figure.

The followings should be considered for the wiring of VTHSENSE and VTHREF.

1. For jumper wiring use a twisted pair.
2. For substrate wiring, arrange differential lines as close to each other as possible on the board.

To obtain low-to-high output at  $T_j = 125^\circ\text{C}$ , the constants of the circuit components are as follows:

$$R1 = 560 \text{ k}\Omega, C1 = 0.1 \text{ }\mu\text{F}$$

$$\begin{aligned} \text{Reference value: } R2 &= 340 \text{ }\Omega, R3 = 280 \text{ }\Omega \text{ (E96) } T_j \text{ at } 125.0^\circ\text{C} \\ & (R2 = 340 \text{ }\Omega, R3 = 287 \text{ }\Omega \text{ (E96) } T_j \text{ at } 120.3^\circ\text{C}) \end{aligned}$$

For R2 and R3, E96 series resistor with a tolerance of  $\pm 0.1\%$  is recommended. The error of this resistor will be the same value as the error produced when  $T_j$  is digitalized. A material which is little affected by the temperature is recommended for the resistor. Note that, R2 and R3 can be configured from two or more resistors.

The accuracy of R1 is not a problem since R1 is used as a pull-down resistor.

C1 is a bypass capacitor. Be sure to mount this even when the recommended external connection circuit is not to be used.

### (3) Calculation Formula

Temperature  $T_j$  can be calculated from the voltages on VTHSENSE and VTHREF as follows.

$$T_j = (VTHREF - VTHSENSE + \text{temperature coefficient 2}) / \text{temperature coefficient 1} \text{ [}^\circ\text{C]}$$

VTHSENSE, VTHREF: measured voltages [V]

Temperature coefficient 1:  $-1.60 \text{ [mV/}^\circ\text{C]}$

Temperature coefficient 2:  $-761.4 \text{ [mV]}$

Example: When VTHSENSE is  $0.681 \text{ [V]}$  and VTHREF is  $1.243 \text{ [V]}$ ,  $T_j$  is calculated as  $125^\circ\text{C}$  as follows.

$$T_j = ((1.243 - 0.681) \times 1000 - 761.4) / (-1.60) = 124.6 \text{ [}^\circ\text{C]}$$

## 60.4 Usage Notes

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

1. When the THS is not used, connect the VTHSENSE and VTHREF pins to GND or leave them open. The THS operates in the initial state. Accordingly, when the THS is not used, the THIDLE bit in THSCR should be set to 1 to place the THS in the idle state. When connecting the VTHSENSE and VTHREF pins to GND, be sure to place the THS in the idle state in the same manner.
2. The guaranteed accuracy of the outputs on the VTHSENSE and VTHREF pins is {(VHTREF - VTHSENSE) specification guaranteed accuracy  $\pm 5^{\circ}\text{C}$  max.} over the temperature range from  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . Take measurement errors into account in designing the user system. Note that, when the internal registers of the TSC are used for measurement of the chip temperature, the operation of the sensor is not guaranteed outside the range of  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  within which operation of the logic circuit is guaranteed.

**Table 60.4 Accuracy of  $T_j$  in Temperature Detection by the Thermal Sensor**

$T_j$ [ $^{\circ}\text{C}$ ]	$T_j$ Accuracy
$T_j > 125^{\circ}\text{C}$	Operation and accuracy are not guaranteed.
$-40^{\circ}\text{C} \leq T_j \leq 125^{\circ}\text{C}$	$\pm 5^{\circ}\text{C}$ {(VHTREF - VTHSENSE) specification}
$-40^{\circ}\text{C} > T_j$	Operation and accuracy are not guaranteed.

3. When  $T_j$  exceeds  $125^{\circ}\text{C}$ , correct operation and device characteristics are not guaranteed.  
Although this module provides a bit for detecting  $T_j = 135^{\circ}\text{C}$ , this bit should only be used for fail-safe operation where the LSI is stopped on the verge of a thermal runaway condition (but has not yet entered that state) and the power consumption is increasing rapidly.
4. The recommended external connection circuit outputs a digital signal that is used to control the LSI from outside according to the LSI temperature  $T_j$ .  
For instance, this circuit can be used as an external fail-safe circuit to stop the power supply to the LSI when thermal runaway occurs and the LSI becomes uncontrollable because of high temperature. Instead of an external connection circuit, an ADC can be connected to detect  $T_j$  with high resolution.  
The external circuit should be used after the THS output mask pin is determined. An AND gate is included in the recommended circuit to avoid signal transmission to subsequent stages before the THS output mask pin is determined.  
However, when a clock signal is input to the PLL and the LSI is in the state after power-on reset, an output can be obtained on the VTHSENSE and VTHREF pins of the THS even when the THS output mask pin is not determined. In this case, it is recommended that the THS output mask pin of the AND circuit in the recommended circuit should be connected with the power-on reset pin via an inverter (low  $\rightarrow$  high for operation).
5. The result of temperature measurement by using the thermal sensor will not be correct over the  $300\ \mu\text{s}$  period after a change to the TAP offset value. For the reasons explained in the descriptions in sections 60.3.2 and 60.3.3, do not take account of results of measurement immediately after a change to the offset value.

## 61. System Controller (SYSC)

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

### 61.1 Overview

The SYSC module controls the supply of power to CPUs (Cortex-A15\*<sup>1\*2</sup>, and Cortex-A7\*<sup>1\*3</sup>), RGX\*<sup>1</sup>, and SGX\*<sup>2\*3</sup>, with the aim of low leakage power. When a module is not in use, shutting off power to the module further lowers leakage power than just stopping supply of the clock signal.

For the RZ/G1E, only pseudo power off is supported. In pseudo power off mode, clock distribution for target modules are stopped with reset assert, but shutting off power-line for reducing leakage current is not supported. In this section, 'power off' means pseudo power off for the RZ/G1E.

#### 61.1.1 Features

- Support shutoff and resumption of power in the following four\*<sup>2\*3</sup>, or 11\*<sup>1</sup> power domains.

##### [RZ/G1H]

Cortex-A15 CPU0 to CPU3 (including the L1 cache)  
 Cortex-A15 SCU (including the L2 cache)  
 Cortex-A7 CPU0 to CPU3 (including the L1 cache)  
 Cortex-A7 SCU (including the L2 cache)  
 RGX

##### [RZ/G1M/N]

Cortex-A15 CPU0/CPU1 (including the L1 cache)  
 Cortex-A15 SCU (including the L2 cache)  
 SGX

##### [RZ/G1E]

Cortex-A7 CPU0/CPU1 (including the L1 cache)  
 Cortex-A7 SCU (including the L2 cache)  
 SGX

- Only power to the domains listed below is on (i.e. the domains are in the power-resume state) after a power-on reset.

##### [RZ/G1H]

Cortex-A15 CPU0 and Cortex-A15 SCU, if MD6 = 0 and MD7 = 0 (Cortex-A15 boot)  
 Cortex-A7 CPU0 and Cortex-A7 SCU, if MD6 = 1 and MD7 = 0 (Cortex-A7 boot)

##### [RZ/G1M/N]

Cortex-A15 CPU0 and Cortex-A15 SCU, if MD6 = 0 and MD7 = 0 (Cortex-A15 boot)

##### [RZ/G1E]

Cortex-A7 CPU0 and Cortex-A7 SCU, if MD6 = 1 and MD7 = 0 (Cortex-A7 boot)

Other domains are in the shutoff state after a power-on reset.

- Control of supplying and shutting off power is independent for each target domain, with the following exceptions.

##### [RZ/G1H]

SCU for the Cortex-A15s can't be switched off while power to any of Cortex-A15 CPU0/1/2/3 is on.  
 SCU of the Cortex-A7s can't be switched off while power to any of Cortex-A7 CPU0/1/2/3 is on.

##### [RZ/G1M/N]

SCU of the Cortex-A15s can't be switched off while power to either or both of Cortex-A15 CPU0/1 is on.

##### [RZ/G1E]

SCU of the Cortex-A7s can't be switched off while power to either or both of Cortex-A7 CPU0/1 is on.

- Resumption of the supply of power to Cortex-A15s (CPU0 to CPU3\*<sup>1</sup>/CPU1\*<sup>2</sup>, SCU), and Cortex-A7s (CPU0 to CPU3\*<sup>1</sup>/CPU1\*<sup>3</sup> and SCU) is controlled by interrupts in each domain.
- Power for Cortex-A15s (CPU0 to CPU3\*<sup>1</sup>/CPU1\*<sup>2</sup>) or Cortex-A7s (CPU0 to CPU3\*<sup>1</sup>/CPU1\*<sup>3</sup>) can be shut off by WFI instructions

Notes: 1. Applicable to the RZ/G1H  
2. Applicable to the RZ/G1M and N  
3. Applicable to the RZ/G1E

61.1.2 Block Diagram

Figures 61.1 to 61.3 are block diagrams of the SYSC.

Connected to the internal peripheral bus (the APB bus), the SYSC operates in coordination with the CPG, the RESET module, the CPU, and the debugger; it contains a module that controls the objects of power shutoff.

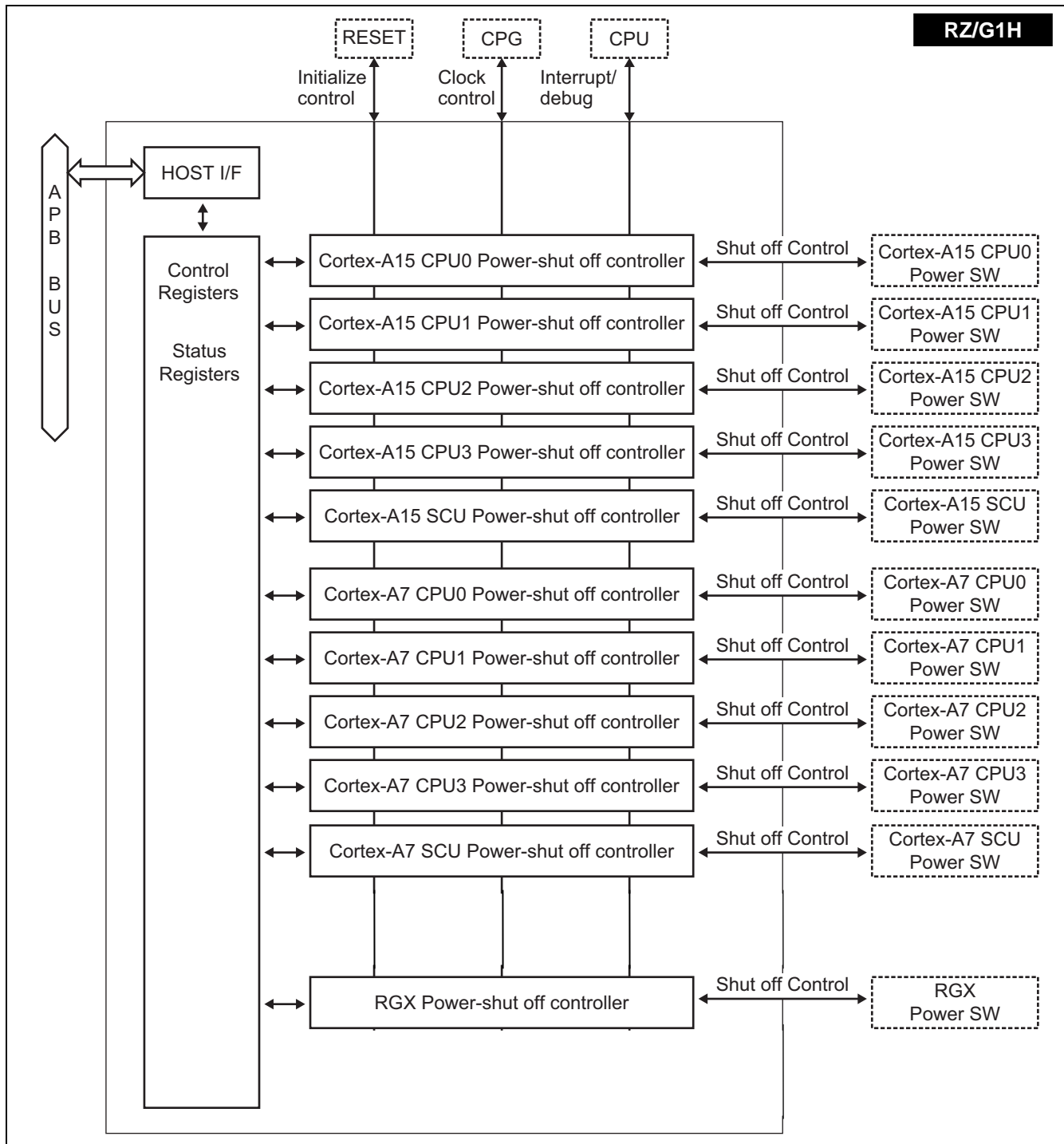


Figure 61.1 Block Diagram [RZ/G1H]

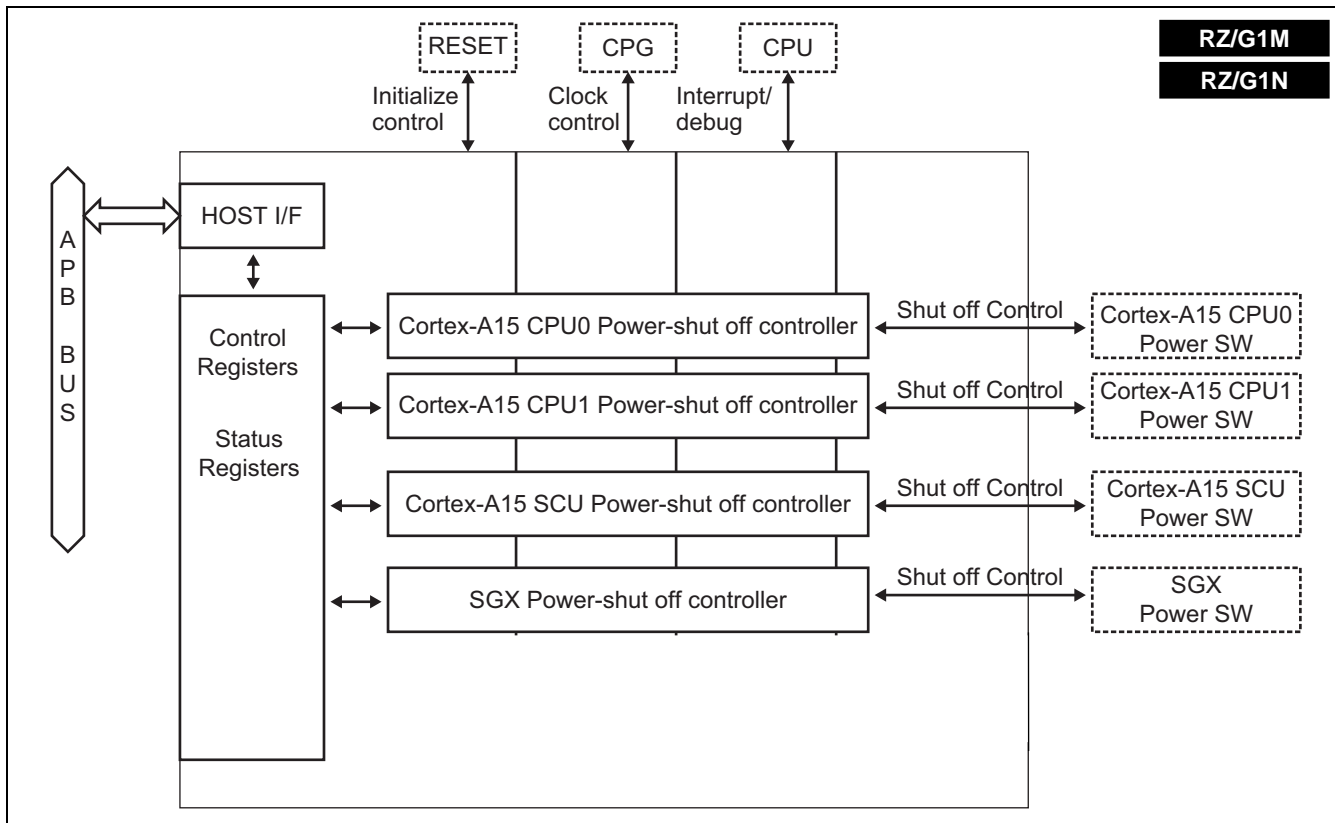


Figure 61.2 Block Diagram [RZ/G1M / N]

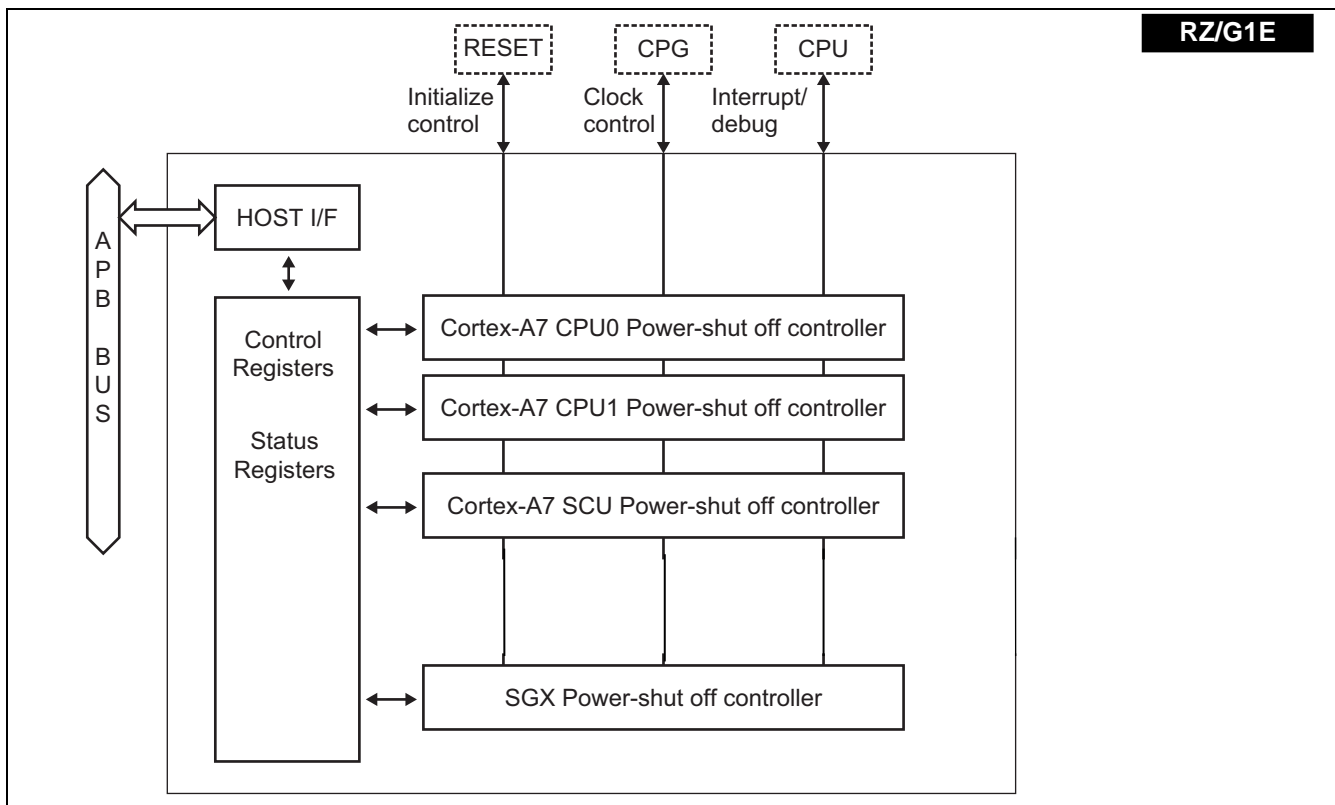


Figure 61.3 Block Diagram [RZ/G1E]



### 61.1.3 Input/Output Pins

The SYSC has no input/output pins.

## 61.2 Register Configuration

Tables 61.1 to 61.2 list the SYSC registers.

Base-address of SYSC is H'E618 0000.

Do not write to addresses other than those listed below, otherwise normal operation cannot be guaranteed. Values read from other addresses are undefined.

[Legend]

Initial value: Register value after a reset

—: Undefined value

R/W: Readable/writable. The written value can be read.

R: Read-only. The write value should always be the initial value.

—/W: Write-only. The read value is undefined.

**Table 61.1 List of Registers (Common Registers)**

Name	Abbreviation	R/W	Initial Value	Address	Access size	RZ/G Series Products			
						RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
SYSC Status Register	SYSCSR	R	H'0000 0003	H'0000	32	√	√	√	√
Interrupt Status Register	SYSCISR	R	H'0000 0000	H'0004	32	√	√	√	√
Interrupt Status Clear Register	SYSCISCR	—/W	—	H'0008	32	√	√	√	√
Interrupt Enable Register	SYSCIER	R/W	H'0000 0000	H'000C	32	√	√	√	√
Interrupt Mask Register	SYSCIMR	R/W	H'0131 11EF	H'0010	32	√	√	√	√
Cortex-A15 Wake Up Mask Register	WUPMSKCA15	R/W	H'0000 0000	H'0014	32	√	√	√	—
Cortex-A7 Wake Up Mask Register	WUPMSKCA7	R/W	H'0000 0000	H'0018	32	√	—	—	√
External Event Request Status Register	SYSCEERSR	R	H'0000 0000	H'0020	32	√	√	√	—
External Event Request Status Clear Register	SYSCEERSCR	—/W	—	H'0024	32	√	√	√	—
External Event Request Status Enable Register	SYSCEERSER	R/W	H'0000 0000	H'0028	32	√	√	√	—
External Event Request Status Register 2	SYSCEERSR2	R	H'0000 0000	H'002C	32	√	—	—	√
External Event Request Status Clear register 2	SYSCEERSCR2	—/W	—	H'0030	32	√	—	—	√
External Event Request Status Enable Register 2	SYSCEERSER2	R/W	H'0000 0000	H'0034	32	√	—	—	√

**Table 61.2 List of Registers (Power Control Registers for each domain)**

Name	Abbreviation	R/W	Initial Value	Address	Access size	RZ/G Series Products			
						RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Power status register 0	PWRSR0	R	H'0000 001E	H'0040	32	√	√	√	—
Power shutoff status register 0	PWROFFSR0	R	H'0000 0000	H'0048	32	√	√	√	—
Power resume status register 0	PWRONSR0	R	H'0000 0000	H'0050	32	√	√	√	—
Power shutoff/resume error register 0	PWRER0	R	H'0000 0000	H'0054	32	√	√	√	—
Power status register 2	PWRSR2	R	H'0000 0001	H'00C0	32	√	√	√	√
Power shutoff control register 2	PWROFFCR2	—/W	—	H'00C4	32	√	√	√	√
Power shutoff status register 2	PWROFFSR2	R	H'0000 0000	H'00C8	32	√	√	√	√
Power resume control register 2	PWRONCR2	—/W	—	H'00CC	32	√	√	√	√
Power resume status register 2	PWRONSR2	R	H'0000 0000	H'00D0	32	√	√	√	√
Power shutoff/resume error register 2	PWRER2	R	H'0000 0000	H'00D4	32	√	√	√	√
Power status register 3	PWRSR3	R	H'0000 0010	H'0100	32	√	—	—	√
Power shutoff control register 3	PWROFFCR3	—/W	—	H'0104	32	√	—	—	√
Power shutoff status register 3	PWROFFSR3	R	H'0000 0000	H'0108	32	√	—	—	√
Power resume control register 3	PWRONCR3	—/W	—	H'010C	32	√	—	—	√
Power resume status register 3	PWRONSR3	R	H'0000 0000	H'0110	32	√	—	—	√
Power shutoff/resume error register 3	PWRER3	R	H'0000 0000	H'0114	32	√	—	—	√
Power status register 5	PWRSR5	R	H'0000 0010	H'0180	32	√	√	√	—
Power shutoff control register 5	PWROFFCR5	—/W	—	H'0184	32	√	√	√	—
Power shutoff status register 5	PWROFFSR5	R	H'0000 0000	H'0188	32	√	√	√	—
Power resume control register 5	PWRONCR5	—/W	—	H'018C	32	√	√	√	—
Power resume status register 5	PWRONSR5	R	H'0000 0000	H'0190	32	√	√	√	—
Power shutoff/resume error register 5	PWRER5	R	H'0000 0000	H'0194	32	√	√	√	—
Power status register 6	PWRSR6	R	H'0000 001E	H'01C0	32	√	—	—	√
Power shutoff status register 6	PWROFFSR6	R	H'0000 0000	H'01C8	32	√	—	—	√

Name	Abbreviation	R/W	Initial Value	Address	Access size	RZ/G Series Products			
						RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Power resume status register 6	PWRONSR6	R	H'0000 0000	H'01D0	32	√	—	—	√
Power shutoff/resume error register 6	PWRER6	R	H'0000 0000	H'01D4	32	√	—	—	√

## 61.2.1 Common Registers

These registers are used to control the shutting off of power to the various modules with respect to the common settings, the interrupts, as well as external events.

### 61.2.1.1 SYSC Status Register (SYSCSR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PONE NB	POFF ENB
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	PONENB	1	R	This bit indicates whether the SYSC is ready to accept power resume requests. Any power resume request issued when the SYSC is disabled from accepting power resume requests will be ignored. 1: Power resume request is acceptable. 0: Power resume request is not accepted.
0	POFFENB	1	R	This bit indicates whether the SYSC is ready to accept power shutoff requests. Any power shutoff request issued when the SYSC is disabled from accepting power shutoff requests will be ignored. 1: Power shutoff request is acceptable. 0: Power shutoff request is not acceptable.

**61.2.1.2 Interrupt Status Register (SYSCISR)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

**[RZ/G1H]**

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	CA7-SCU	RGX	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	CA15-SCU	—	—	—	CA7-CPU[3:0]			—	CA15-CPU[3:0]				
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

**[RZ/G1M/N]**

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	SGX	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	CA15-SCU	—	—	—	—	—	—	—	—	—	—	CA15-CPU[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

**[RZ/G1E]**

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	CA7-SCU	SGX	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	CA7-CPU[3:0]		—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 25	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
24	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
23, 22	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
21	CA7-SCU	0	R	Indicates Cortex-A7 SCU power-processing status. [RZ/G1H/E]  This bit is set to 1 when the CA7-SCU bit in the interrupt enable register is 1 upon completion of the Cortex-A7 SCU power shutoff or power resume processing. If the CA7-SCU bit in the interrupt enable register is 0, this bit is not set to 1 even when the Cortex-A7 SCU power shutoff or power resume processing is completed. An interrupt request is issued when the CA7-SCU bit in the interrupt mask register is 0 and this bit is 1.  0: Power shutoff or power resume processing of CA7-SCU is not completed. 1: Power shutoff or power resume processing of CA7-SCU is completed.
—	—	0	R	Reserved [RZ/G1M/N]  This bit is always read as 0. The write value should always be 0.
20	RGX/ SGX	0	R	Indicates RGX power-processing status. [RZ/G1H] Indicates SGX power-processing status. [RZ/G1M/N/E]  This bit is set to 1 when the RGX/SGX bit in the interrupt enable register is 1 upon completion of the RGX/SGX power shutoff or power resume processing. If the RGX/SGX bit in the interrupt enable register is 0, this bit is not set to 1 even when the RGX/SGX power shutoff or power resume processing is completed. An interrupt request is issued when the RGX/SGX bit in the interrupt mask register is 0 and this bit is 1.  0: Power shutoff or power resume processing of RGX/SGX is not completed. 1: Power shutoff or power resume processing of RGX/SGX is completed.
19 to 17	—	All 0	R	Reserved  These bits are always read as 0. The write value should always be 0.
16	—	0	R	Reserved  This bit is always read as 0. The write value should always be 0.
15 to 13	—	All 0	R	Reserved  These bits are always read as 0. The write value should always be 0.
12	CA15- SCU	0	R	Indicates Cortex-A15 SCU power-processing status. [RZ/G1H/M/N]  This bit is set to 1 when the CA15-SCU bit in the interrupt enable register is 1 upon completion of the Cortex-A15 SCU power shutoff or power resume processing. If the CA15-SCU bit in the interrupt enable register is 0, this bit is not set to 1 even when the Cortex-A15 SCU power shutoff or power resume processing is completed. An interrupt request is issued when the CA15-SCU bit in the interrupt mask register is 0 and this bit is 1.  0: Power shutoff or power resume processing of Cortex-A15 SCU is not completed. 1: Power shutoff or power resume processing of Cortex-A15 SCU is completed.
—	—	0	R	Reserved [RZ/G1E]  This bit is always read as 0. The write value should always be 0.
11 to 9	—	All 0	R	Reserved  These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
8 to 5	CA7-CPU[3:0]/ CA7-CPU[1:0]	All 0	R	<p>Indicates Cortex-A7 CPU3-0 power-processing status. [RZ/G1H]</p> <p>Reserved (bits 8 and 7) and indicates Cortex-A7 CPU1-0 power-processing status (bits 6 and 5). [RZ/G1E]</p> <p>This bit is set to 1 when the CA7-CPU[3:0] / CPU[1:0] bit in the interrupt enable register is 1 upon completion of the Cortex-A7 core CPU3-0 / CPU1-0 power shutoff or power resume processing. If the Cortex-A7 CPU[3:0] / CPU[1:0] bit in the interrupt enable register is 0, this bit is not set to 1 even when power shutoff or power resume processing for the Cortex-A7 core CPU3-0 / CPU1-0 is completed. An interrupt request is issued when the CA7-CPU[3:0] / CPU[1:0] bit in the interrupt mask register is 0 and this bit is 1.</p> <p>0: Power shutoff or power resume processing of Cortex-A7 CPU3-0 / CPU1-0 is not completed.</p> <p>1: Power shutoff or power resume processing of Cortex-A7 CPU3-0 / CPU1-0 is completed.</p> <p>Regarding RZ/G1E, Bit 8/7 of this field is reserved. These bits are always read as 0. The write value should always be 0.</p>
—	—	All 0	R	<p>Reserved [RZ/G1M/N]</p> <p>These bits are always read as 0. The write value should always be 0.</p>
4	—	0	R	<p>Reserved</p> <p>This bit is always read as 0. The write value should always be 0.</p>
3 to 0	CA15-CPU[3:0]/ CA15-CPU[1:0]	All 0	R	<p>Indicates Cortex-A15 CPU3-0 power-processing status. [RZ/G1H]</p> <p>Reserved (Bit 3/2) and indicates Cortex-A15 CPU1-0 power-processing status(Bit 1/0). [RZ/G1M/N]</p> <p>This bit is set to 1 when the CA15-CPU[3:0] / CPU[1:0] bit in the interrupt enable register is 1 upon completion of the Cortex-A15 core CPU3-0 / CPU1-0 power shutoff or power resume processing. If the Cortex-A15 CPU[3:0] / CPU[1:0] bit in the interrupt enable register is 0, this bit is not set to 1 even when power shutoff or power resume processing for the Cortex-A15 core CPU3-0 / CPU1-0 is completed. An interrupt request is issued when the CA15-CPU[3:0] / CPU[1:0] bit in the interrupt mask register is 0 and this bit is 1.</p> <p>0: Power shutoff or power resume processing of Cortex-A15 CPU3-0 / CPU1-0 is not complete.</p> <p>1: Power shutoff or power resume processing of Cortex-A15 CPU3-0 / CPU1-0 is complete.</p> <p>Regarding RZ/G1M/N, Bit 3/2 of this field is reserved. These bits are always read as 0. The write value should always be 0.</p>
—	—	All 0	R	<p>Reserved [RZ/G1E]</p> <p>These bits are always read as 0. The write value should always be 0.</p>



**61.2.1.3 Interrupt Status Clear Register (SYSCISCR)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

**[RZ/G1H]**

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	CA7-SCU	RGX	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	—	—	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	—/W	—/W	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	CA15-SCU	—	—	—	CA7-CPU[3:0]			—	CA15-CPU[3:0]				
Initial value:	0	0	0	—	0	0	0	—	—	—	—	0	—	—	—	—
R/W:	R	R	R	—/W	R	R	R	—/W	—/W	—/W	—/W	R	—/W	—/W	—/W	—/W

**[RZ/G1M/N]**

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	SGX	—	—	—	—
Initial value:	0	0	0	0	0	0	0	—	0	0	—	—	0	0	0	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	—/W	R	R	R	—/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	CA15-SCU	—	—	—	—	—	—	—	—	—	—	CA15-CPU[1:0]	
Initial value:	0	0	0	—	0	0	0	0	0	0	0	0	0	0	—	—
R/W:	R	R	R	—/W	R	R	R	R	R	R	R	R	R	R	—/W	—/W

**[RZ/G1E]**

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	CA7-SCU	SGX	—	—	—	—
Initial value:	0	0	0	0	0	0	0	—	0	0	—	—	0	0	0	0
R/W:	R	R	R	R	R	R	R	—/W	R	R	—/W	—/W	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	CA7-CPU[1:0]		—	—	—	—	—
Initial value:	0	0	0	—	0	0	0	—	—	—	—	0	—	—	—	—
R/W:	R	R	R	—/W	R	R	R	—/W	—/W	—/W	—/W	R	—/W	—/W	—/W	—/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 25	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
24	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
23, 22	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
21	CA7-SCU	—	—/W	Specify clear of Cortex-A7 SCU interrupt status. [RZ/G1H/E] Writing 1 to this bit clears the CA7-SCU bit in the interrupt status register (SYSCISR) to 0. Writing 0 to this bit is ignored.
	—	0	R	Reserved [RZ/G1M/N] This bit is always read as 0. The write value should always be 0.
20	RGX/ SGX	—	—/W	Specify clear of RGX interrupt status. [RZ/G1H] Specify clear of SGX interrupt status. [RZ/G1M/N/E] Writing 1 to this bit clears the RGX/SGX bit in the interrupt status register (SYSCISR) to 0. Writing 0 to this bit is ignored.
	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
16	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
15 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12	CA15-SCU	—	—/W	Specify clear of Cortex-A15 SCU interrupt status. [RZ/G1H/M/N] Writing 1 to this bit clears the CA15-SCU bit in the interrupt status register (SYSCISR) to 0. Writing 0 to this bit is ignored.
	—	0	R	Reserved [RZ/G1E] This bit is always read as 0. The write value should always be 0.
11 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8 to 5	CA7- CPU[3:0]/ CA7- CPU[1:0]	—	—/W	Specify clear of Cortex-A7 CPU3-0 interrupt status. [RZ/G1H] Reserved (Bit 8/7) and Specify clear of Cortex-A7 CPU1-0 interrupt status. [RZ/G1E] Writing 1 to this bit clears the CA7-CPU[3:0] / CPU[1:0] bit in the interrupt status register (SYSCISR) to 0. Writing 0 to this bit is ignored. Regarding RZ/G1E, Bit 8/7 of this field is reserved. These bits are always read as 0. The write value should always be 0.
	—	All 0	R	Reserved [RZ/G1M/N] These bits are always read as 0. The write value should always be 0.
4	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
3 to 0	CA15- CPU[3:0]/ CA15- CPU[1:0]	—	—/W	Specify clear of Cortex-A15 CPU3-0 interrupt status. [RZ/G1H] Writing 1 to this bit clears the CA15-CPU[3:0] bit in the interrupt status register (SYSCISR) to 0. Writing 0 to this bit is ignored. Regarding RZ/G1M/N, Bit 3/2 of this field is reserved. These bits are always read as 0. The write value should always be 0.
	—	All 0	R	Reserved [RZ/G1M/N/E] These bits are always read as 0. The write value should always be 0.

**61.2.1.4 Interrupt Enable Register (SYSCIER)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

**[RZ/G1H]**

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	CA7-SCU	RGX	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	CA15-SCU	—	—	—	CA7-CPU[3:0]			—	CA15-CPU[3:0]				
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R	R	R	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W

**[RZ/G1M/N]**

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	SGX	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	CA15-SCU	—	—	—	—	—	—	—	—	—	—	CA15-CPU[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R	R	R	R	R	R	R	R	R	R	R	R/W

**[RZ/G1E]**

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	CA7-SCU	SGX	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R	R	R/W	R/W	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	CA7-CPU[1:0]		—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R	R	R	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 25	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
24	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
23, 22	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
21	CA7-SCU	0	R/W	Specifies that the status is indicated in the CA7-SCU bit in the interrupt status register (SYSCISR) when the Cortex-A7 SCU power shutoff or power resume processing is complete. [RZ/G1H/E] 0: Does not indicate the status when power shutoff or power resume processing is complete. 1: Indicates the status when power shutoff or power resume processing is complete.
—	—	0	R	Reserved [RZ/G1M/N] This bit is always read as 0. The write value should always be 0.
20	RGX/ SGX	0	R/W	Specifies that the status is indicated in the RGX [RZ/G1H] / SGX [RZ/G1M/N/E] bit in the interrupt status register (SYSCISR) when the RGX/SGX power shutoff or power resume processing is complete. 0: Does not indicate the status when power shutoff or power resume processing is complete. 1: Indicates the status when power shutoff or power resume processing is complete.
19 to 17	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
16	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
15 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12	CA15-SCU	0	R/W	Specifies that the status is indicated in the CA15-SCU bit in the interrupt status register (SYSCISR) when the Cortex-A15 SCU power shutoff or power resume processing is complete. [RZ/G1H/M/N] 0: Does not indicate the status when power shutoff or power resume processing is complete. 1: Indicates the status when power shutoff or power resume processing is complete.
—	—	0	R	Reserved [RZ/G1E] This bit is always read as 0. The write value should always be 0.
11 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8 to 5	CA7-CPU[3:0]/ CA7-CPU[1:0]	All 0	R/W	Specifies that the status is indicated in the CA7-CPU[3:0] [RZ/G1H] / CPU[1:0] [RZ/G1E] bit in the interrupt status register (SYSCISR) when power shutoff or power resume processing for the Cortex-A7 core CPU3-0 / CPU1-0 is complete. 0: Does not indicate the status when power shutoff or power resume processing is complete. 1: Indicates the status when power shutoff or power resume processing is complete. Regarding RZ/G1E , Bit 8/7 of this field is reserved. These bits are always read as 0. The write value should always be 0.
—	—	All 0	R	Reserved [RZ/G1M/N] These bits are always read as 0. The write value should always be 0.
4	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
3 to 0	CA15-CPU[3:0]/ CA15-CPU[1:0]	All 0	R/W	<p>Specifies that the status is indicated in the CA15-CPU[3:0] [RZ/G1H] / CPU[1:0] [RZ/G1M/N] bit in the interrupt status register (SYSCISR) when power shutoff or power resume processing for the Cortex-A15 core CPU3-0 / CPU1-0 is complete.</p> <p>0: Does not indicate the status when power shutoff or power resume processing is complete.</p> <p>1: Indicates the status when power shutoff or power resume processing is complete.</p> <p>Regarding RZ/G1M/N, Bit 3/2 of this field is reserved. These bits are always read as 0. The write value should always be 0.</p>
—	—	All 0	R	<p>Reserved [RZ/G1E]</p> <p>These bits are always read as 0. The write value should always be 0.</p>

**61.2.1.5 Interrupt Mask Register (SYSCIMR)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

**[RZ/G1H]**

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	CA7-SCU	RGX	—	—	—	—
Initial value:	0	0	0	0	0	0	0	1	0	0	1	1	0	0	0	1
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	CA15-SCU	—	—	—	CA7-CPU[3:0]			—	CA15-CPU[3:0]				
Initial value:	0	0	0	1	0	0	0	1	1	1	1	0	1	1	1	1
R/W:	R	R	R	R/W	R	R	R	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W

**[RZ/G1M/N]**

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	SGX	—	—	—	—
Initial value:	0	0	0	0	0	0	0	1	0	0	1	1	0	0	0	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	CA15-SCU	—	—	—	—	—	—	—	—	—	—	—	CA15-CPU[1:0]
Initial value:	0	0	0	1	0	0	0	1	1	1	1	0	1	1	1	1
R/W:	R	R	R	R/W	R	R	R	R	R	R	R	R	R	R	R	R/W

**[RZ/G1E]**

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	CA7-SCU	SGX	—	—	—	—
Initial value:	0	0	0	0	0	0	0	1	0	0	1	1	0	0	0	1
R/W:	R	R	R	R	R	R	R	R/W	R	R	R/W	R/W	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	CA7-CPU[1:0]		—	—	—	—	—
Initial value:	0	0	0	1	0	0	0	1	1	1	1	0	1	1	1	1
R/W:	R	R	R	R/W	R	R	R	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 25	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
24	—	1	R	Reserved [RZ/G1M/N/E] This bit is always read as 1. The write value should always be 1.
23, 22	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
21	CA7-SCU	1	R/W	Controls the interrupt output when the Cortex-A7 SCU power shutoff or power resume processing is complete. If this bit is 1, no interrupt is issued even if the pertinent bit in the interrupt status register (SYSCISR) is set to 1. [RZ/G1H/E]  0: Does not mask the interrupt when the Cortex-A7 SCU power shutoff or power resume processing is complete. 1: Masks the interrupt when the Cortex-A7 SCU power shutoff or power resume processing is complete.
—	—	1	R	Reserved [RZ/G1M/N]  This bit is always read as 1. The write value should always be 1.
20	RGX/ SGX	1	R/W	Controls the interrupt output when the RGX[RZ/G1H] / SGX[RZ/G1M/N/E] power shutoff or power resume processing is complete. If this bit is 1, no interrupt is issued even if the pertinent bit in the interrupt status register (SYSCISR) is set to 1.  0: Does not mask the interrupt when the RGX / SGX power shutoff or power resume processing is complete. 1: Masks the interrupt when the RGX / SGX power shutoff or power resume processing is complete.
19 to 17	—	All 0	R	Reserved  These bits are always read as 0. The write value should always be 0.
16	—	1	R/W	Reserved  This bit is always read as 1. The write value should always be 1.
15 to 13	—	All 0	R	Reserved  These bits are always read as 0. The write value should always be 0.
12	CA15-SCU	1	R/W	Controls the interrupt output when the Cortex-A15 SCU [RZ/G1H/M/N] power shutoff or power resume processing is complete. If this bit is 1, no interrupt is issued even if the pertinent bit in the interrupt status register (SYSCISR) is set to 1.  0: Does not mask the interrupt when the Cortex-A15 SCU power shutoff or power resume processing is complete. 1: Masks the interrupt when the Cortex-A15 SCU power shutoff or power resume processing is complete.
—	—	1	R/W	Reserved [RZ/G1E]  This bit is always read as 1. The write value should always be 1.
11 to 9	—	All 0	R	Reserved  These bits are always read as 0. The write value should always be 0.
8 to 5	CA7-CPU[3:0]/ CA7-CPU[1:0]	All 1	R/W	Controls the interrupt output when power shutoff or power resume processing for the Cortex-A7 core CPU3-0 [RZ/G1H] / CPU[1:0] [RZ/G1E] is complete. If this bit is 1, no interrupt is issued even if the pertinent bit in the interrupt status register (SYSCISR) is set to 1.  0: Does not mask the interrupt when power shutoff or power resume processing for the Cortex-A7 core CPU3-0 is complete. 1: Masks the interrupt when power shutoff or power resume processing for the Cortex-A7 core CPU3-0 is complete.  Regarding RZ/G1E , Bit 8/7 of this field is reserved. These bits are always read as 1. The write value should always be 1.
—	—	All 1	R	Reserved [RZ/G1M/N]  The write value should always be 1.
4	—	0	R	Reserved  This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
3 to 0	CA15-CPU[3:0]/ CA15-CPU[1:0]	All 1	R/W	<p>Controls the interrupt output when power shutoff or power resume processing for the Cortex-A15 core CPU3-0 [RZ/G1H] / CPU[1:0] [RZ/G1M/N] is complete. If this bit is 1, no interrupt is issued even if the pertinent bit in the interrupt status register (SYSCISR) is set to 1.</p> <p>0: Does not mask the interrupt when power shutoff or power resume processing for the Cortex-A15 core CPU3-0 is complete.</p> <p>1: Masks the interrupt when power shutoff or power resume processing for the Cortex-A15 core CPU3-0 is complete.</p> <p>Regarding RZ/G1M/N, Bit 3/2 of this field is reserved. These bits are always read as 1. The write value should always be 1.</p>
—	—	All 1	R	<p>Reserved [RZ/G1E]</p> <p>These bits are always read as 1. The write value should always be 1.</p>



## 61.2.1.6 Cortex-A15 Wake Up Mask Register (WUPMSKCA15)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

## [RZ/G1H]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	CSD[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	FIQ[3:0]			—	—	—	—	IRQ[3:0]				
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R	R	R	R	R/W	R/W	R/W	R/W

## [RZ/G1M/N]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CSD[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	FIQ[1:0]		—	—	—	—	—	—	IRQ[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 20	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
19 to 16	CSD[3:0]/ CSD[1:0]	All 0	R/W	Enable/Disable wake up Cortex-A15 CPU0-3 [RZ/G1H] / CPU0-1 [RZ/G1M/N] + SCU area when receiving CSD[3:0] /CSD [1:0] factor 0: Enable 1: Disable This setting is available only when Cortex-A15 SCU area is in OFF state. Regarding RZ/G1M/N, Bit 11/10 of this field is reserved. These bits are always read as 0. The write value should always be 0.
15 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
11 to 8	FIQ[3:0]/ FIQ[1:0]	All 0	R/W	<p>Enable/Disable wake up Cortex-A15 CPU0-3 [RZ/G1H] / CPU0-1 [RZ/G1M/N] + SCU area when receiving FIQ[3:0] / FIQ[1:0] factor</p> <p>0: Enable 1: Disable</p> <p>This setting is available only when Cortex-A15 SCU area is in OFF state.</p> <p>Regarding RZ/G1M/N, Bit 7/6 of this field is reserved. These bits are always read as 0. The write value should always be 0.</p>
7 to 4	—	All 0	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>
3 to 0	IRQ[3:0]/ IRQ[1:0]	All 0	R/W	<p>Enable/Disable wake up Cortex-A15 CPU0-3 [RZ/G1H] / CPU0-1 [RZ/G1M/N] + SCU area when receiving IRQ[3:0] / IRQ[1:0] factor</p> <p>0: Enable 1: Disable</p> <p>This setting is available only when Cortex-A15 SCU area is in OFF state.</p> <p>Regarding RZ/G1M/N, Bit 3/2 of this field is reserved. These bits are always read as 0. The write value should always be 0.</p>

**61.2.1.7 Cortex-A7 Wake Up Mask Register (WUPMSKCA7)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	—	—	√

[RZ/G1H]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	CSD[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	FIQ[3:0]			—	—	—	—	IRQ[3:0]				
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R	R	R	R	R/W	R/W	R/W	R/W

[RZ/G1E]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CSD[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	FIQ[1:0]		—	—	—	—	—	—	IRQ[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 20	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
19 to 16	CSD[3:0]/ CSD[1:0]	All 0	R/W	Enable/Disable wake up Cortex-A7 CPU0-3 [RZ/G1H] / CPU0-1 [RZ/G1E] + SCU area when receiving CSD[3:0] / CSD[1:0] factor 0: Enable 1: Disable This setting is available only when Cortex-A7 SCU area is in OFF state Regarding RZ/G1E, Bit 11/10 of this field is reserved. These bits are always read as 0. The write value should always be 0.
15 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
11 to 8	FIQ[3:0]/ FIQ[1:0]	All 0	R/W	<p>Enable/Disable wake up Cortex-A7 CPU0-3 [RZ/G1H] / CPU0-1 [RZ/G1E] + SCU area when receiving FIQ[3:0] / FIQ[1:0] factor</p> <p>0: Enable 1: Disable</p> <p>This setting is available only when Cortex-A7 SCU area is in OFF state.</p> <p>Regarding RZ/G1E, Bit 7/6 of this field is reserved. These bits are always read as 0. The write value should always be 0.</p>
7 to 4	—	All 0	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>
3 to 0	IRQ[3:0]/ IRQ[1:0]	All 0	R/W	<p>Enable/Disable wake up Cortex-A7 CPU0-3 [RZ/G1H] / CPU0-1 [RZ/G1E] + SCU area when receiving IRQ[3:0] / IRQ[1:0] factor</p> <p>0: Enable 1: Disable</p> <p>This setting is available only when Cortex-A7 SCU area is in OFF state.</p> <p>Regarding RZ/G1E, Bit 3/2 of this field is reserved. These bits are always read as 0. The write value should always be 0.</p>

## 61.2.1.8 External Event Request Status Register (SYSCEERSR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

## [RZ/G1H]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	FIQ_CA15[3:0]			IRQ_CA15[3:0]			—	—	—	—		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

## [RZ/G1M/N]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	FIQ_CA15[1:0]		—	—	IRQ_CA15[1:0]		—	—	—	—
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11 to 8	FIQ_CA15[3:0]/ FIQ_CA15[1:0]	All 0	R	<p>If the FIQ_CA15[3:0] [RZ/G1H] / FIQ_CA15[1:0] [RZ/G1M/N] bit in the external event request status enable register is 1, this bit is set to 1 when a power resume request due to an FIQ interrupt is accepted by the Cortex-A15 core CPU3-0 / CPU1-0. If the FIQ_CA15[3:0] / FIQ_CA15[1:0] bit in the external event request status enable register is 0, this bit is not set to 1 even when a power resume request due to an FIQ interrupt is accepted. This bit is also set to 1 when the request is accepted when power for the Cortex-A15 core CPU3-0 / CPU1-0 is not shut off.</p> <p>0: The power resume request due to an FIQ interrupt has not been accepted by the Cortex-A15 core CPU3-0.</p> <p>1: The power resume request due to an FIQ interrupt has been accepted by the Cortex-A15 core CPU3-0.</p> <p>This bit is set, only when condition above is satisfied in Cortex-A15 SCU is power-shutoff state.</p> <p>Regarding RZ/G1M/N, Bit 11/10 of this field is reserved. These bits are always read as 0. The write value should always be 0.</p>

Bit	Bit Name	Initial Value	R/W	Description
7 to 4	IRQ_CA15[3:0]/ IRQ_CA15[1:0]	All 0	R	<p>If the IRQ_CA15[3:0] [RZ/G1H] / IRQ_CA15[1:0] [RZ/G1M/N] bit in the external event request status enable register is 1, this bit is set to 1 when a power resume request due to an IRQ interrupt is accepted by the Cortex-A15 core CPU3-0 / CPU1-0. If the IRQ_CA15[3:0] / IRQ_CA15[1:0] bit in the external event request status enable register is 0, this bit is not set to 1 even when a power resume request due to an IRQ interrupt is accepted. This bit is also set to 1 when the request is accepted when power for the Cortex-A15 core CPU3-0 / CPU1-0 is not shut off.</p> <p>0: The power resume request due to an IRQ interrupt has not been accepted by the Cortex-A15 core CPU3-0 / CPU1-0.</p> <p>1: The power resume request due to an IRQ interrupt has been accepted by the Cortex-A15 core CPU3-0 / CPU1-0.</p> <p>This bit is set, only when condition above is satisfied in Cortex-A15 SCU is power-shutoff state.</p> <p>Regarding RZ/G1M/N, Bit 7/6 of this field is reserved. These bits are always read as 0. The write value should always be 0.</p>
3 to 0	—	All 0	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>

## 61.2.1.9 External Event Request Status Clear Register (SYSCEERSCR)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

## [RZ/G1H]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	FIQ_CA15[3:0]			IRQ_CA15[3:0]			—	—	—	—		
Initial value:	0	0	0	0	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	R	R	R	R

## [RZ/G1M/N]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	FIQ_CA15[1:0]		—	—	IRQ_CA15[1:0]		—	—	—	—
Initial value:	0	0	0	0	0	0	—	—	0	0	—	—	0	0	—	—
R/W:	R	R	R	R	R	R	—/W	—/W	R	R	—/W	—/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11 to 8	FIQ_CA15[3:0]/ FIQ_CA15[1:0]	All 0	—/W	Writing 1 to this bit clears the FIQ_CA15[3:0] / FIQ_CA15[1:0] bit in the external event request status register (SYSCOFSR) to 0. If 0 is written to this bit or the pertinent bit in the external event request status register is 0, nothing happens. If the pertinent bit in the external event request status register is set to 1 and 1 is written to this bit simultaneously to clear it to 0, setting the bit to 1 takes precedence. Regarding RZ/G1M/N, Bit 11/10 of this field is reserved. These bits are always read as 0. The write value should always be 0.
7 to 4	IRQ_CA15[3:0]/ IRQ_CA15[1:0]	All 0	—/W	Writing 1 to this bit clears the IRQ_CA15[3:0] [RZ/G1H] / IRQ_CA15[1:0] [RZ/G1M/N] bit in the external event request status register (SYSCOFSR) to 0. If 0 is written to this bit or the pertinent bit in the external event request status register is 0, nothing happens. If the pertinent bit in the external event request status register is set to 1 and 1 is written to this bit simultaneously to clear it to 0, setting the bit to 1 takes precedence. Regarding RZ/G1M/N, Bit 7/6 of this field is reserved. These bits are always read as 0. The write value should always be 0.

---

Bit	Bit Name	Initial Value	R/W	Description
3 to 0	—	All 0	R	Reserved

---

These bits are always read as 0. The write value should always be 0.

---



**61.2.1.10 External Event Request Status Enable Register (SYSCEERSER)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	—

**[RZ/G1H]**

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	FIQ_CA15[3:0]			IRQ_CA15[3:0]			—	—	—	—		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R

**[RZ/G1M/N]**

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	FIQ_CA15[1:0]		—	—	IRQ_CA15[1:0]		—	—	—	—
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R	R	R/W	R/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11 to 8	FIQ_CA15[3:0] / FIQ_CA15[1:0]	All 0	R/W	Specifies that the status be indicated in the FIQ_CA15[3:0] [RZ/G1H] / FIQ_CA15[1:0] [RZ/G1M/N] bit in the external event request status register (SYSCOFSR) when a power resume request due to an FIQ interrupt is accepted by the Cortex-A15 core CPU3-0 / CPU1-0. 0: Does not indicate the status when a power resume request is accepted. 1: Indicates the status when a power resume request is accepted. Regarding RZ/G1M/N, Bit 11/10 of this field is reserved. These bits are always read as 0. The write value should always be 0.
7 to 4	IRQ_CA15[3:0] / IRQ_CA15[1:0]	All 0	R/W	Specifies that the status be indicated in the IRQ_CA15[3:0] [RZ/G1H] / IRQ_CA15[1:0] bit in the external event request status register (SYSCOFSR) when a power resume request due to an FIQ interrupt is accepted by the Cortex-A15 core CPU3-0 / CPU1-0. 0: Does not indicate the status when a power resume request is accepted. 1: Indicates the status when a power resume request is accepted. Regarding RZ/G1M/N, Bit 7/6 of this field is reserved. These bits are always read as 0. The write value should always be 0.

---

<b>Bit</b>	<b>Bit Name</b>	<b>Initial Value</b>	<b>R/W</b>	<b>Description</b>
3 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

---

**61.2.1.11 External Event Request Status Register2 (SYSCEERSR2)**

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	—	—	√

**[RZ/G1H]**

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	FIQ_CA7[3:0]				IRQ_CA7[3:0]				—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

**[RZ/G1E]**

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	FIQ_CA7[1:0]		—	—	IRQ_CA7[1:0]		—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11 to 8	FIQ_CA7[3:0] / FIQ_CA7[1:0]	All 0	R	<p>If the FIQ_CA7[3:0] [RZ/G1H] / FIQ_CA7[1:0] [RZ/G1E] bit in the external event request status enable register is 1, this bit is set to 1 when a power resume request due to an FIQ interrupt is accepted by the Cortex-A7 core CPU3-0 / CPU1-0. If the FIQ_CA7[3:0] / FIQ_CA7[1:0] bit in the external event request status enable register is 0, this bit is not set to 1 even when a power resume request due to an FIQ interrupt is accepted. This bit is also set to 1 when the request is accepted when power for the Cortex-A7 core CPU3-0 / CPU1-0 is not shut off.</p> <p>0: The power resume request due to an FIQ interrupt has not been accepted by the Cortex-A7 core CPU3-0 / CPU1-0. 1: The power resume request due to an FIQ interrupt has been accepted by the Cortex-A7 core CPU3-0 / CPU1-0.</p> <p>This bit is set, only when condition above is satisfied in Cortex-A7 SCU is power-shutoff state.</p> <p>Regarding RZ/G1E, Bit 11/10 of this field is reserved. These bits are always read as 0. The write value should always be 0.</p>

Bit	Bit Name	Initial Value	R/W	Description
7 to 4	IRQ_CA7[3:0] / IRQ_CA7[1:0]	All 0	R	<p>If the IRQ_CA7[3:0] [RZ/G1H] / IRQ_CA7[1:0] [RZ/G1E] bit in the external event request status enable register is 1, this bit is set to 1 when a power resume request due to an IRQ interrupt is accepted by the ARM core CPU3. If the IRQ_CA7[3:0] / IRQ_CA[1:0] bit in the external event request status enable register is 0, this bit is not set to 1 even when a power resume request due to an IRQ interrupt is accepted. This bit is also set to 1 when the request is accepted when power for the Cortex-A7 core CPU3-0 / CPU1-0 is not shut off.</p> <p>0: The power resume request due to an IRQ interrupt has not been accepted by the Cortex-A7 core CPU3-0 / CPU1-0.</p> <p>1: The power resume request due to an IRQ interrupt has been accepted by the Cortex-A7 core CPU3-0 / CPU1-0.</p> <p>This bit is set, only when condition above is satisfied in Cortex-A7 SCU is power-shutoff state.</p> <p>Regarding RZ/G1E, Bit 7/6 of this field is reserved. These bits are always read as 0. The write value should always be 0.</p>
3 to 0	—	All 0	R	<p>Reserved</p> <p>These bits are always read as 0. The write value should always be 0.</p>

### 61.2.1.12 External Event Request Status Clear Register2 (SYSCEERSCR2)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	—	—	√

[RZ/G1H]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	FIQ_CA7[3:0]			IRQ_CA7[3:0]			—	—	—	—		
Initial value:	0	0	0	0	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	R	R	R	R

[RZ/G1E]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	FIQ_CA7[1:0]		—	—	IRQ_CA7[1:0]		—	—	—	—
Initial value:	0	0	0	0	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11 to 8	FIQ_CA7[3:0] / FIQ_CA7[1:0]	—	—/W	Writing 1 to this bit clears the FIQ_CA7[3:0] [RZ/G1H] / FIQ_CA7[1:0] [RZ/G1E] bit in the external event request status register 2 (SYSCEERSR2) to 0. If 0 is written to this bit or the pertinent bit in the external event request status register is 0, nothing happens. If the pertinent bit in the external event request status register is set to 1 and 1 is written to this bit simultaneously to clear it to 0, setting the bit to 1 takes precedence. Regarding RZ/G1E, Bit 11/10 of this field is reserved. These bits are always read as 0. The write value should always be 0.
7 to 4	IRQ_CA7[3:0] / IRQ_CA7[1:0]	—	—/W	Writing 1 to this bit clears the IRQ_CA7[3:0] [RZ/G1H] / IRQ_CA7[1:0] [RZ/G1E] bit in the external event request status register2 (SYSCEERSR2) to 0. If 0 is written to this bit or the pertinent bit in the external event request status register is 0, nothing happens. If the pertinent bit in the external event request status register is set to 1 and 1 is written to this bit simultaneously to clear it to 0, setting the bit to 1 takes precedence. Regarding RZ/G1E, Bit 7/6 of this field is reserved. These bits are always read as 0. The write value should always be 0.

---

Bit	Bit Name	Initial Value	R/W	Description
3 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

---

### 61.2.1.13 External Event Request Status Enable Register2 (SYSCEERSER2)

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

#### [RZ/G1H]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	FIQ_CA7[3:0]			IRQ_CA7[3:0]			—	—	—	—		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R

#### [RZ/G1E]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	FIQ_CA7[1:0]		—	—	IRQ_CA7[1:0]		—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R	R	R/W	R/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11 to 8	FIQ_CA7[3:0] / FIQ_CA7[1:0]	All 0	R/W	Specifies that the status be indicated in the FIQ_CA7[3:0] [RZ/G1H] / FIQ_CA7[1:0] [RZ/G1E] bit in the external event request status register (SYSCOF SR) when a power resume request due to an FIQ interrupt is accepted by the Cortex-A7 core CPU3-0 / CPU1-0. 0: Does not indicate the status when a power resume request is accepted. 1: Indicates the status when a power resume request is accepted. Regarding RZ/G1E, Bit 11/10 of this field is reserved. These bits are always read as 0. The write value should always be 0.
7 to 4	IRQ_CA7[3:0] / IRQ_CA7[1:0]	All 0	R/W	Specifies that the status be indicated in the IRQ_CA7[3:0] [RZ/G1H] / IRQ_CA7[1:0] [RZ/G1E] bit in the external event request status register (SYSCOF SR) when a power resume request due to an FIQ interrupt is accepted by the Cortex-A7 core CPU3-0 / CPU1-0. 0: Does not indicate the status when a power resume request is accepted. 1: Indicates the status when a power resume request is accepted. Regarding RZ/G1E, Bit 7/6 of this field is reserved. These bits are always read as 0. The write value should always be 0.

---

<b>Bit</b>	<b>Bit Name</b>	<b>Initial Value</b>	<b>R/W</b>	<b>Description</b>
3 to 0	—	All 0	R	Reserved

---

These bits are always read as 0. The write value should always be 0.

---



### 61.2.2 Power Control Registers for ARM CPUs

These registers control power status of Cortex-A15 and Cortex-A7 CPUs.

In the detailed description of these registers, the register names corresponding to the modules are denoted as "n (n: 0/6)". The "n" and the module names correspond as follows:

Cortex-A15: n = 0

Cortex-A7: n = 6

#### 61.2.2.1 Power Status Register n (PWRSRn)

Note: n=0/6 [RZ/G1H] , n=0 [RZ/G1M/N] , n=6 [RZ/G1E]

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

##### [RZ/G1H]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	PWRUP_CPU[3:0]			PWRDWN_CPU[3:0]				
Initial value:	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

##### [RZ/G1M/N/E]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	PWRUP_CPU [1:0]		—	—	PWRDWN_CPU [1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
7 to 4	PWRUP_CPU[3:0]/ PWRUP_CPU[1:0]	0 for CPU1/2/3 1 for CPU0	R	Indicates the non-power-shutoff state of CPU3-0 [RZ/G1H] / CPU1-0 [RZ/G1M/N/E].  0: Not in non-power-shutoff state 1: In non-power-shutoff state  Regarding RZ/G1M/N/E, Bit 7/6 of this field is reserved. These bits are always read as 0. The write value should always be 0.
3 to 0	PWRDWN_CPU[3:0]/ PWRDWN_CPU[1:0]	0 for CPU0 1 for CPU1/2/3	R	Indicates the power-shutoff state of CPU3-0 [RZ/G1H] / CPU1-0 [RZ/G1M/N/E].  0: Not in power-shutoff state 1: In power-shutoff state  Regarding RZ/G1M/N/E, Bit 3/2 of this field is reserved. These bits are always read as 1. The write value should always be 1.

### 61.2.2.2 Power Shutoff Status Register n (PWROFFSRn)

Note: n=0/6 [RZ/G1H], n=0 [RZ/G1M/N], n=6 [RZ/G1E]

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

#### [RZ/G1H]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	CPU[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

#### [RZ/G1M/N/E]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CPU[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3 to 0	CPU[3:0]/ CPU[1:0]	All 0	R	Indicates the power shutoff sequence execution status of CPU3-0 [RZ/G1H] / CPU1-0 [RZ/G1M/N/E]. 0: The power shutoff sequence not being executed 1: The power shutoff sequence being executed Regarding RZ/G1M/N/E, Bit 3/2 of this field is reserved. These bits are always read as 0. The write value should always be 0.

### 61.2.2.3 Power Resume Status Register n (PWRONSRn)

Note: n=0/6 [RZ/G1H], n=0 [RZ/G1M/N], n=6 [RZ/G1E]

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

#### [RZ/G1H]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	CPU[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

#### [RZ/G1M/N/E]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CPU[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3 to 0	CPU[3:0]/ CPU[1:0]	All 0	R	Indicates the power resume sequence execution status of CPU3-0 [RZ/G1H] / CPU1-0 [RZ/G1M/N/E]. 0: The power resume sequence not being executed 1: The power resume sequence being executed Regarding RZ/G1M/N/E, Bit 3/2 of this field is reserved. These bits are always read as 0. The write value should always be 0.

### 61.2.2.4 Power Shutoff/Resume Error Register n (PWRErn)

Note: n=0/6 [RZ/G1H], n=0 [RZ/G1M/N], n=6 [RZ/G1E]

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

#### [RZ/G1H]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	CPU[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

#### [RZ/G1M/N/E]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CPU[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3	CPU[3:0]/ CPU[1:0]	All 0	R	Indicates whether a power shutoff or power resume request by a preceding register write to CPU3-0 [RZ/G1H] /CPU1-0 [RZ/G1M/N/E] was accepted or not. 0: Either a preceding power shutoff or power resume request to CPU3-0 / CPU1-0 was accepted. 1: Either a preceding power shutoff or power resume request to CPU3-0 / CPU1-0 was not accepted. Regarding RZ/G1M/N/E, Bit 3/2 of this field is reserved. These bits are always read as 0. The write value should always be 0.

### 61.2.3 Power Control Registers for RGX, and SCU of Cortex-A15

These registers control power shutoff/resume of following modules. In the detailed description of these registers that follows, the register names corresponding to the modules are denoted as "n (n: 2/3/4/5)". The "n" and the module names correspond as follows:

RGX [RZ/G1H] / SGX [RZ/G1M/N/E] : n = 2

Cortex-A7 SCU: n = 3

Cortex-A15 SCU: n = 5

#### 61.2.3.1 Power Status Register n (PWRSRn) (n = 2/3/5)

Note: n = 2/3/5 [RZ/G1H] , n = 2/5 [RZ/G1M/N] , n = 2/3 [RZ/G1E]

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	PWRUP	—	—	—	PWRDWN
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0/1	0	0	0	0/1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	PWRUP	0 for n = 2 1 for n = 3/5	R	Indicates the power non-shutoff status of a given module. 0: The module is not in the power non-shutoff state. 1: The module is in the power non-shutoff state.
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	PWRDWN	0 for n = 3/5 1 for n = 2	R	Indicates the power shutoff status of a given module. 0: The module is not in the power shutoff state. 1: The module is in the power shutoff state.

### 61.2.3.2 Power Shutoff Control Register n (PWROFFCRn) (n = 2/3/5)

Note: n = 2/3/5 [RZ/G1H], n = 2/5 [RZ/G1M/N], n = 2/3 [RZ/G1E]

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PWRD WN
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	—/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	PWRDWN	—	—/W	Specify the start of power-shutoff sequence. <p>Writing 1 to this bit when the POFFENB bit in the SYSC status register is 1 starts the power shutoff sequence for the module. In this case, the ERR bit in the power shutoff/resume error register n is set to 0.</p> <p>Writing 1 to this bit when the POFFENB bit in the SYSC status register is 0 does not start the power shutoff sequence. In this case, the ERR bit in the power shutoff/resume error register n is set to 1.</p> <p>0: Does not shut off power for the module. 1: Starts the power shutoff sequence for the module.</p> <p>When the power shutoff sequence is started, during the execution of the power shutoff sequence the shutoff processing status is indicated in the DWNSTATE bit in the power shutoff status register n. The PWRUP bit in the power status register n is set to 0. Upon completion of the power shutoff sequence, the PWRDWN bit in the power status register n is set to 1. The pertinent bit in the interrupt status register is set to 1 if it is enabled by the setting of the interrupt status enable register.</p> <p>If 1 is written to this bit when the module is in the power shutoff state, such a request is ignored. In this case, too, if 1 is written when the POFFENB bit is 1, the pertinent bit in the power shutoff/resume error register is set to 0, and if 1 is written when the POFFENB bit is 0, the pertinent bit in the power shutoff/resume error register is set to 1.</p>

**61.2.3.3 Power Shutoff Status Register n (PWROFFSRn) (n = 2/3/5)**

Note: n = 2/3/5 [RZ/G1H] , n = 2/5 [RZ/G1M/N] , n = 2/3 [RZ/G1E]

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DWNS TATE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	DWNSTATE	0	R	Indicates the power shutoff sequence execution status for the module. 0: The power shutoff sequence not being executed 1: The power shutoff sequence being executed



### 61.2.3.4 Power Resume Control Register n (PWRONCRn) (n = 2/3/5)

Note: n = 2/3/5 [RZ/G1H], n = 2/5 [RZ/G1M/N], n = 2/3 [RZ/G1E]

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PWRUP
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	—/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	PWRUP	—	—/W	Specify the start of power-resume sequence.  Writing 1 to this bit when the PONENB bit in the SYSC status register is 1 starts the power resume sequence for the module. In this case, the ERR bit in the power shutoff/resume error register n is set to 0.  Writing 1 to this bit when the PONENB bit in the SYSC status register is 0 does not start the power resume sequence. In this case, the ERR bit in the power shutoff/resume error register n is set to 1.  0: Does not resume power for the module. 1: Starts the power resume sequence for the module.  When the power resume sequence is started, during the execution of the power resume sequence the resume processing status is indicated in the UPSTATE bit in the power resume status register n. The PWRDWN bit in the power status register n is set to 0. Upon completion of the power resume sequence, the PWRUP bit in the power status register n is set to 1. The pertinent bit in the interrupt status register is set to 1 if it is enabled by the setting of the interrupt status enable register.  If 1 is written to this bit when the module is in the power non-shutoff state, such a request is ignored. In this case, too, if 1 is written when the PONENB bit is 1, the pertinent bit in the power shutoff/resume error register is set to 0, and if 1 is written when the PONENB bit is 0, the pertinent bit in the power shutoff/resume error register is set to 1.

**61.2.3.5 Power Resume Status Register n (PWRONSRn) (n = 2/3/5)**

Note: n = 2/3/5 [RZ/G1H] , n = 2/5 [RZ/G1M/N] , n = 2/3 [RZ/G1E]

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	UPSTATE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	UPSTATE	0	R	Indicates the power resume sequence execution status for the module. 0: The power resume sequence not being executed 1: The power resume sequence being executed

**61.2.3.6 Power Shutoff/Resume Error Register n (PWRErn) (n = 2/3/5)**

Note: n = 2/3/5 [RZ/G1H] , n = 2/5 [RZ/G1M/N] , n = 2/3 [RZ/G1E]

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ERR
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	ERR	0	R	Indicates that either a power shutoff or power resume request by a preceding register write to the module was issued when such requests were not acceptable. 0: Either a preceding power shutoff or power resume request to the module was accepted. 1: Either a preceding power shutoff or power resume request to the module was not accepted.

## 61.3 Operations

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

### 61.3.1 Power Control of ARM CPUs

The ARM CPUs can be powered off by executing the WFI instruction. Similarly, power of ARM CPU core can be resumed either by controlling the CPG (APMU) registers or by an IRQ or FIQ interrupt.

For detail of power control by CPG (APMU) registers, see section 7B, Advanced Power Management Unit for AP-System Core (APMU).

#### (1) Power Control by WFI Instruction and Interrupts

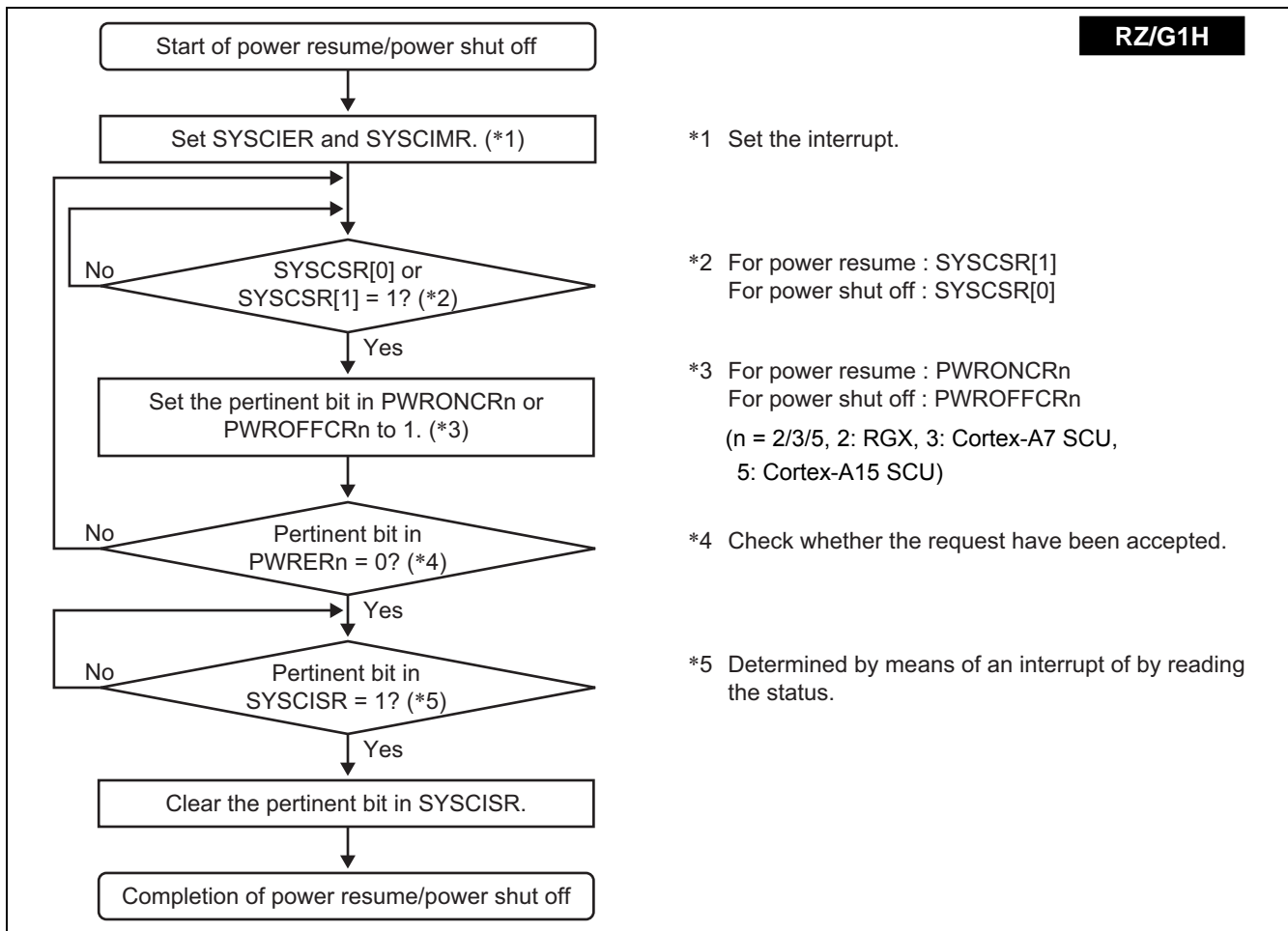
The power shutdown by the WFI instruction is performed only when Cortex-A7\*<sup>2</sup>/ Cortex-A15\*<sup>1</sup> CPU<sup>n</sup>\*<sup>3</sup> power status control register (CA7CPU<sup>n</sup>\*<sup>3</sup>CR\*<sup>1</sup>, CA15CPU<sup>n</sup>\*<sup>3</sup>CR\*<sup>2</sup>) is in the core standby mode. In case of other setting, power shutdown sequence is not activated by the WFI instruction. See section 7B, Advanced Power Management Unit for AP-System Core (APMU).

Power can be resumed by an IRQ or FIQ interrupt on the ARM core. After resuming power of Cortex-A7\*<sup>2</sup>/ Cortex-A15\*<sup>1</sup> CPUs by IRQ/FIQ, read the value of SYSCOFSR/SYSCOFSR2\*<sup>2</sup> registers. Without reading those registers after power-resuming, the shutdown sequence of related CPUs will not start.

- Notes:
1. Applicable to the RZ/G1H, RZ/G1M, and RZ/G1N
  2. Applicable to the RZ/G1H and RZ/G1E
  3. n = 0 to 3 [RZ/G1H]  
n = 0, 1 [RZ/G1M, RZ/G1N, and RZ/G1E]

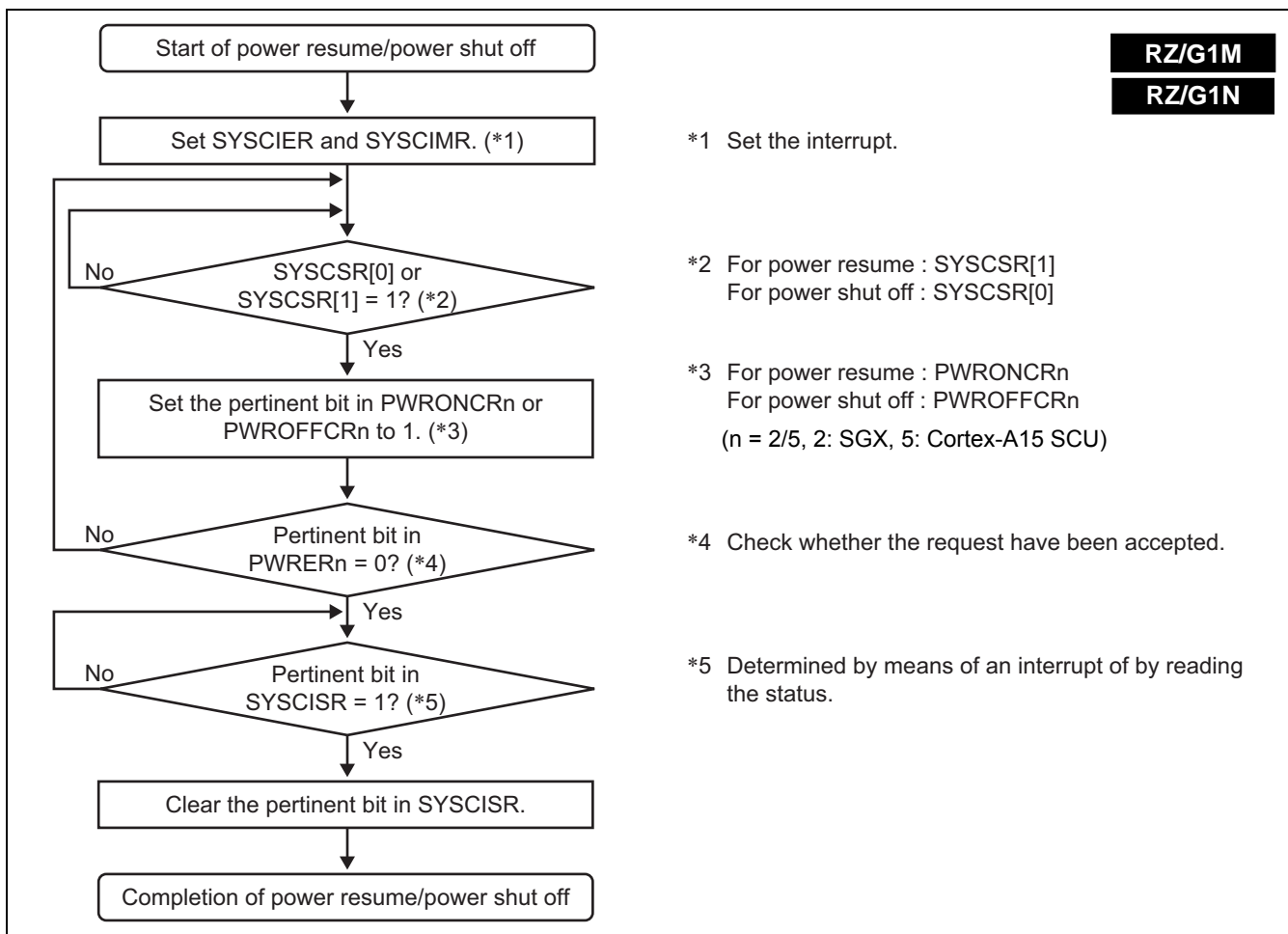
**61.3.2 Power Control of non-ARM-CPU modules**

Power control on modules other than the ARM CPUs can be performed exclusively by means of SYSC registers. Such power control should be performed with reference to the flowchart given below:



**Figure 61.4 Power Resume/Shutoff Flowchart on non-ARM-CPU by Means of SYSC Registers [RZ/G1H]**

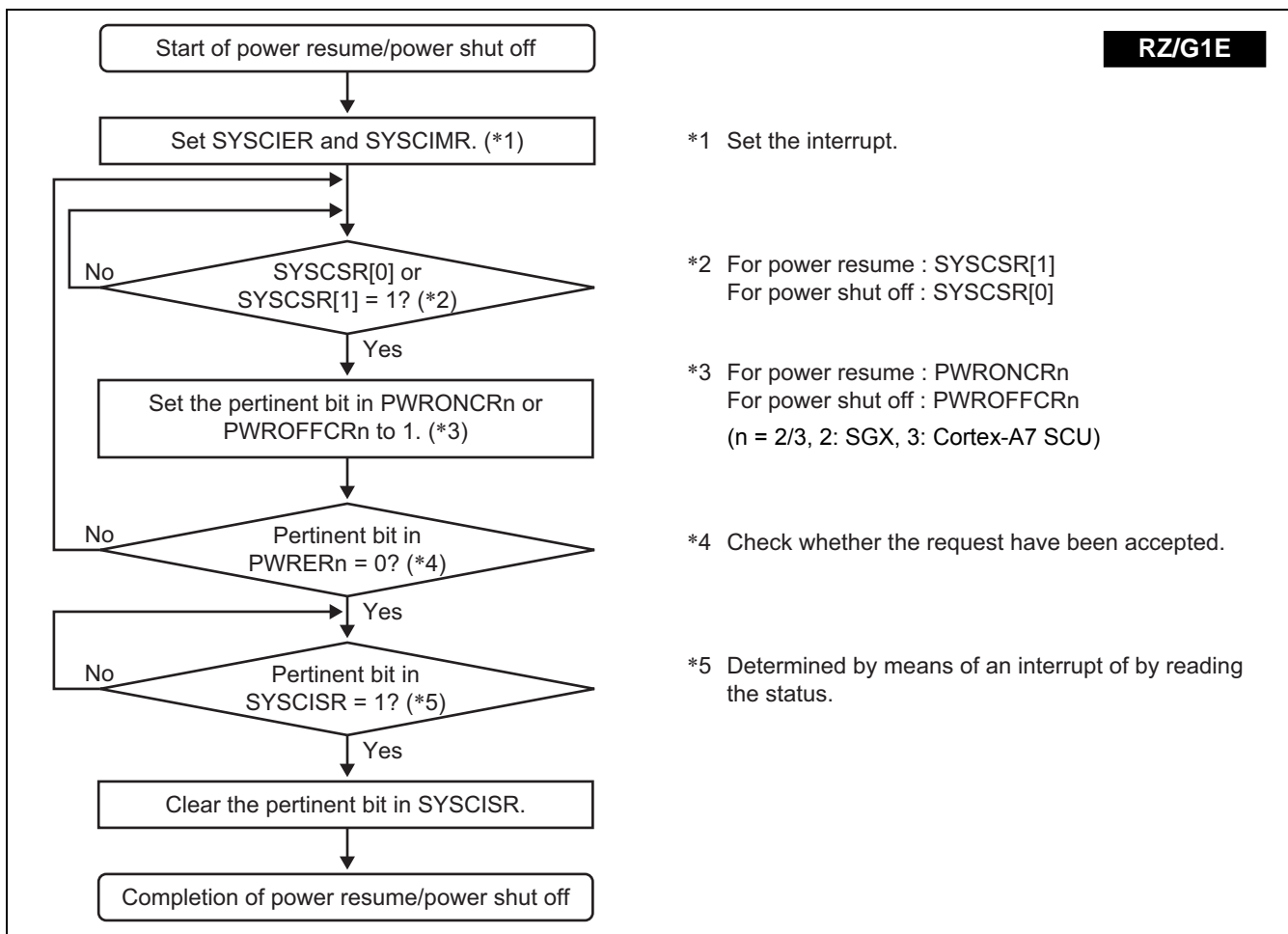
**RZ/G1M**  
**RZ/G1N**



- \*1 Set the interrupt.
- \*2 For power resume : SYSCSR[1]  
For power shut off : SYSCSR[0]
- \*3 For power resume : PWRONCRn  
For power shut off : PWROFFCRn  
(n = 2/5, 2: SGX, 5: Cortex-A15 SCU)
- \*4 Check whether the request have been accepted.
- \*5 Determined by means of an interrupt of by reading the status.

**Figure 61.5 Power Resume/Shutoff Flowchart on non-ARM-CPU by Means of SYSC Registers [RZ/G1M/N]**

**RZ/G1E**



- \*1 Set the interrupt.
- \*2 For power resume : SYSCSR[1]  
For power shut off : SYSCSR[0]
- \*3 For power resume : PWRONCRn  
For power shut off : PWROFFCRn  
(n = 2/3, 2: SGX, 3: Cortex-A7 SCU)
- \*4 Check whether the request have been accepted.
- \*5 Determined by means of an interrupt of by reading the status.

**Figure 61.6 Power Resume/Shutoff Flowchart on non-ARM-CPU by Means of SYSC Registers [RZ/G1E]**

## 61.4 Usage Notes

RZ/G1H	RZ/G1N
RZ/G1M	RZ/G1E

1. For modules other than the ARM CPUs, resume or shutoff sequences on more than one module cannot be executed simultaneously. Whether or not a resume or shutoff sequence can be accepted is indicated in the SYSC status register.
2. The ARM CPUs can simultaneously execute resume or shutoff sequences for the CPU0 to CPU<sup>n</sup>\*1 of the ARM core only if those sequences are simultaneously activated. Resume and shutoff sequences cannot be executed simultaneously even for the CPU0 to CPU<sup>n</sup>\*1 of the ARM core.
3. If power for the ARM core is controlled by the WFI instruction or interrupts, such actions can potentially be in contention with power control by means of the SYSC register at an unexpected timing. Such control should be performed with references to the flowchart shown in Figures 61.4 to 61.6.
4. For a module for which power is shut down, register settings and memory contents are not retained; any necessary information should be saved before power is shut off.
5. Shutting off and resuming power requires several hundreds of microseconds.

Note: CPU0 to CPU3 [RZ/G1H]  
 CPU0, CPU1 [RZ/G1M/N/E]



# 62. CoreSight

RZ/G1H	RZ/G1N
RZ/G1M	RZ/G1E

## 62.1 Features

- JTAG interface
  - Supports dedicated 5-pin JTAG and SWD
- Supports the cross trigger between following IPs.
  - Cortex-A15 CPU. [Only RZ/G1H, RZ/G1M, RZ/G1N]
  - Cortex-A7 CPU. [Only RZ/G1H, RZ/G1E]
  - CoreSight
- Tracing function
  - ETM is installed for each Cortex-A7 CPU
  - PTM is installed for each Cortex-A15 CPU
  - A maximum of 16 bits × 390 Mbps (145-MHz DDR) trace\* data pin output
  - 16-Kbyte embedded trace FIFO (ETF)

Note: \* Design frequency of internal logic. This is limited by IO buffer performance.

## 62.2 Block Diagram

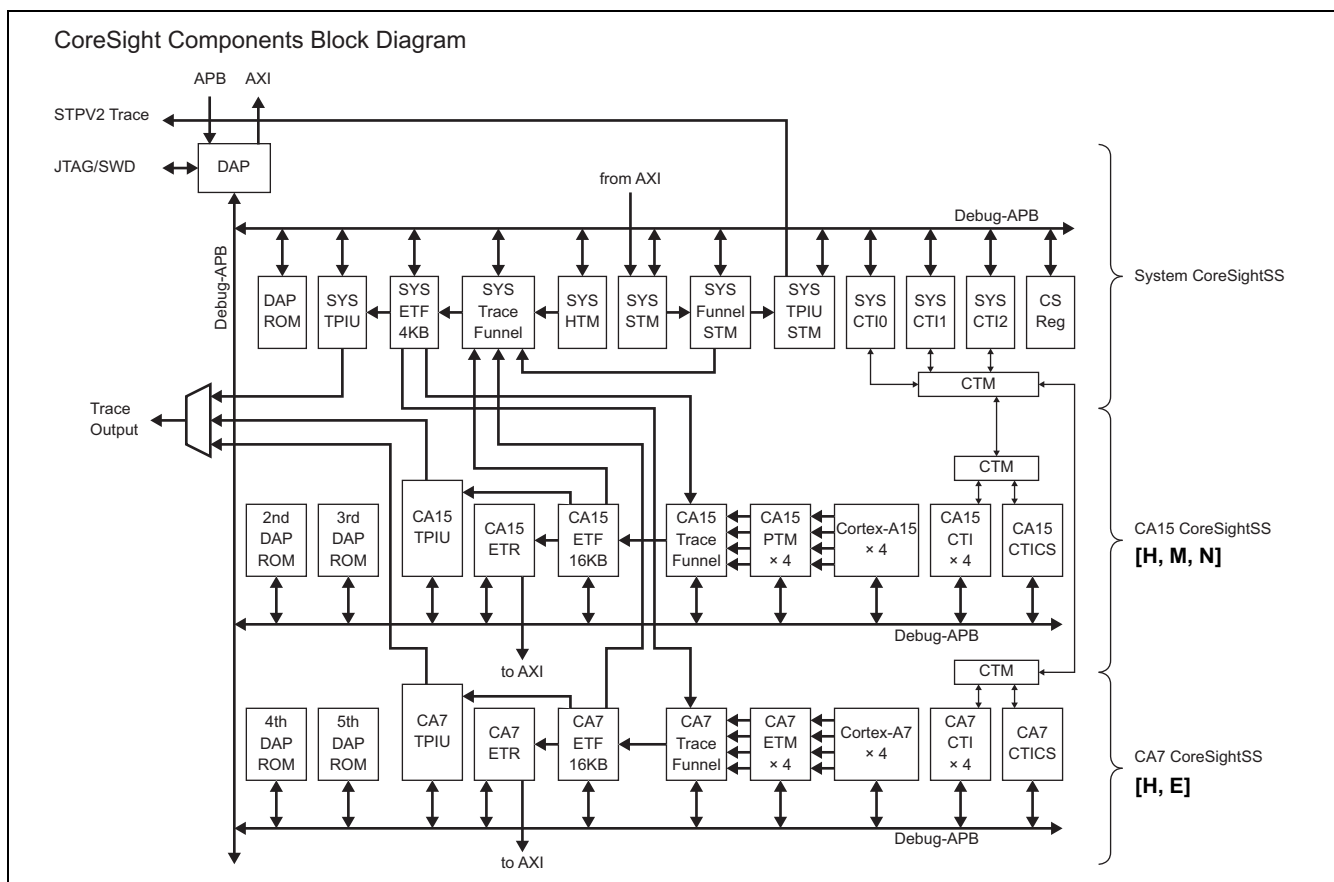


Figure 62.1 CoreSight Block Diagram

## 62.3 Input/Output Pins

### 62.3.1 JTAG Pins

5-pin JTAG and SWD are supported as dedicated pins.

**Table 62.1 RZ/G1H JTAG Pins**

Function Name	JTAG1 1.8V	JTAG2 1.8V	JTAG3 1.8V	I/O
TRST	TRST#	SD0_CMD	SD1_CMD	Input
TCK/SWCLK	TCK	SD0_DAT0	SD1_DAT0	Input
TMS/SWDIO	TMS	SD0_DAT1	SD1_DAT1	Input/output
TDI	TDI	SD0_DAT2	SD1_DAT2	Input
TDO/SWO	TDO	SD0_CLK	SD1_CLK	Output
EDBGREQ	—	SD0_DAT3	SD1_DAT3	IN

**Table 62.2 RZ/G1M/N JTAG Pins**

Function Name	JTAG1 1.8V	JTAG2 1.8V	JTAG3 1.8V	I/O
TRST	TRST#	SD2_CMD	SD3_CMD	Input
TCK/SWCLK	TCK	SD2_DATA0	SD3_DATA0	Input
TMS/SWDIO	TMS	SD2_DATA1	SD3_DATA1	Input/output
TDI	TDI	SD2_DATA2	SD3_DATA2	Input
TDO/SWO	TDO	SD2_CLK	SD3_CLK	Output
EDBGREQ	—	SD2_DATA3	SD3_DATA3	IN

**Table 62.3 RZ/G1E JTAG Pins**

Function Name	JTAG1 1.8V	JTAG2 1.8V	JTAG3 1.8V	I/O
TRST	TRST#	SD1_CMD	MMC_CMD	Input
TCK/SWCLK	TCK	SD1_DATA0	MMC_D0	Input
TMS/SWDIO	TMS	SD1_DATA1	MMC_D1	Input/output
TDI	TDI	SD1_DATA2	MMC_D2	Input
TDO/SWO	TDO	SD1_CLK	MMC_CLK	Output
EDBGREQ	—	SD1_DATA3	MMC_D3	IN

- Notes:
1. Please refer section 5, Pin Function Controller (PFC) to know the initial states of pull-up/down control each pins. Basically, the pull-up control initial states of JTAG2/3 multiplexed with SD/MMC pins are disabled.
  2. If the JTAG Ports are not selected by debug related MD pins (MD[11:10], MD[21:20], MDT[1:0] pins are all low level), TRST# pin of JTAG1 should be set Low level or drove with the same level of PRESET# pin.
  3. JTAG1, JTAG2 and JTAG3 and Trace ports support 1.8 V only.

### 62.3.2 Trace Pins

A maximum of 16-bit trace ports are supported as multiplexed pins.

**Table 62.4 RZ/G1H Trace Pins**

Function Name	Pin Name	Pin Name	I/O
ARM_TRACEDATA_0	SD2_DAT3	SCIFA2_SCK	Output

Function Name	Pin Name	Pin Name	I/O
ARM_TRACEDATA_1	SD3_DAT2	HRTS0#	Output
ARM_TRACEDATA_2	SD3_DAT1	HCTS0#	Output
ARM_TRACEDATA_3	SD3_DAT0	HTX0	Output
ARM_TRACEDATA_4	SD3_CMD	HRX0	Output
ARM_TRACEDATA_5	SD3_CLK	HSCCK0	Output
ARM_TRACEDATA_6	SD2_WP	SCIFA2_TXD	Output
ARM_TRACEDATA_7	SD2_CD	SCIFA2_RXD	Output
ARM_TRACEDATA_8	SD2_DAT1	SCIFA1_CTS#	Output
ARM_TRACEDATA_9	SD2_DAT0	SCIFA1_TXD	Output
ARM_TRACEDATA_10	SD2_CMD	SCIFA1_RXD	Output
ARM_TRACEDATA_11	SD2_CLK	SCIFA0_RTS#	Output
ARM_TRACEDATA_12	SD1_WP	SCIFA0_CTS#	Output
ARM_TRACEDATA_13	SD1_CD	SCIFA0_TXD	Output
ARM_TRACEDATA_14	SD0_WP	SCIFA0_RXD	Output
ARM_TRACEDATA_15	SD0_CD	SCIFA0_SCK	Output
TRACECLK	SD3_WP	MSIOF0_SS1	Output
TRACECTL	SD2_DAT2	SCIFA1_RTS#	Output
CTIREQ	SD3_DAT3	MSIOF0_SCK	Input
CTIACK	SD3_CD	MSIOF0_SYNC	Output

**Table 62.5 RZ/G1M/N Trace Pins**

Function Name	Pin Name	Pin Name	I/O
ARM_TRACEDATA_0	SD0_WP	DU1_DG1	Output
ARM_TRACEDATA_1	SD3_DATA2	DU1_DB0	Output
ARM_TRACEDATA_2	SD3_DATA1	DU1_DG7	Output
ARM_TRACEDATA_3	SD3_DATA0	DU1_DG6	Output
ARM_TRACEDATA_4	SD3_CMD	DU1_DG5	Output
ARM_TRACEDATA_5	SD3_CLK	DU1_DG4	Output
ARM_TRACEDATA_6	SD2_WP	DU1_DG3	Output
ARM_TRACEDATA_7	SD2_CD	DU1_DG2	Output
ARM_TRACEDATA_8	SD2_DATA3	DU1_DR7	Output
ARM_TRACEDATA_9	SD2_DATA2	DU1_DR6	Output
ARM_TRACEDATA_10	SD2_DATA1	DU1_DR5	Output
ARM_TRACEDATA_11	SD2_DATA0	DU1_DR4	Output
ARM_TRACEDATA_12	SD2_CMD	DU1_DR3	Output
ARM_TRACEDATA_13	SD2_CLK	DU1_DR2	Output
ARM_TRACEDATA_14	SD0_DATA3	DU1_DR1	Output
ARM_TRACEDATA_15	SD0_DATA2	DU1_DR0	Output
TRACECLK	SD3_WP	DU1_DB3	Output
TRACECTL	SD0_CD	DU1_DG0	Output
CTIREQ	SD3_DATA3	DU1_DB1	Input
CTIACK	SD3_CD	DU1_DB2	Output

**Table 62.6 RZ/G1E Trace Pins**

Function Name	Pin Name	Pin Name	I/O
ARM_TRACEDATA_0	SD1_CD	MMC_D4	Output
ARM_TRACEDATA_1	SD1_DATA1	MMC_D1	Output
ARM_TRACEDATA_2	SD1_DATA2	MMC_D2	Output
ARM_TRACEDATA_3	SD1_DATA3	MMC_D3	Output
ARM_TRACEDATA_4	MMC_D4	SD1_CD	Output
ARM_TRACEDATA_5	MMC_D5	SD1_WP	Output
ARM_TRACEDATA_6	MMC_CLK	SD1_CLK	Output
ARM_TRACEDATA_7	MMC_CMD	SD1_CMD	Output
ARM_TRACEDATA_8	MMC_D0	SD1_DATA0	Output
ARM_TRACEDATA_9	MMC_D1	SD1_DATA1	Output
ARM_TRACEDATA_10	MMC_D2	SD1_DATA2	Output
ARM_TRACEDATA_11	MMC_D3	SD1_DATA3	Output
ARM_TRACEDATA_12	SD0_CLK	SD0_CLK	Output
ARM_TRACEDATA_13	SD0_CMD	SD0_CMD	Output
ARM_TRACEDATA_14	SD0_DATA0	SD0_DATA0	Output
ARM_TRACEDATA_15	SD0_DATA1	SD0_DATA1	Output
TRACECLK	SD1_CLK	MMC_CLK	Output
TRACECTL	SD1_WP	MMC_D5	Output
CTIREQ	SD1_DATA0	MMC_D0	Input
CTIACK	SD1_CMD	MMC_CMD	Output

## 62.4 Address Map

RZ/G1H	RZ/G1N
RZ/G1M	RZ/G1E

Table 62.7 Coresight Address Map

System Address (CPU View)	Debug-APB address (Debugger View)	module
H'E6F00000 to H'E6F00FFF	H'80000000 to H'80000FFF	DAP ROM
H'E6F01000 to H'E6F01FFF	H'80001000 to H'80001FFF	SYS-ETF
H'E6F02000 to H'E6F02FFF	H'80002000 to H'80002FFF	SYS-CTI0
H'E6F03000 to H'E6F03FFF	H'80003000 to H'80003FFF	SYS-TPIU
H'E6F04000 to H'E6F04FFF	H'80004000 to H'80004FFF	SYS-TraceFunnel
H'E6F05000 to H'E6F06FFF	H'80005000 to H'80006FFF	Reserved
H'E6F07000 to H'E6F07FFF	H'80007000 to H'80007FFF	SYS-HTM
H'E6F08000 to H'E6F08FFF	H'80008000 to H'80008FFF	SYS-CTI2
H'E6F09000 to H'E6F09FFF	H'80009000 to H'80009FFF	SYS-STM
H'E6F0A000 to H'E6F0AFFF	H'8000A000 to H'8000AFFF	SYS-TPIU-STM
H'E6F0B000 to H'E6F0BFFF	H'8000B000 to H'8000BFFF	SYS-TraceFunnel-STM
H'E6F0C000 to H'E6F0CFFF	H'8000C000 to H'8000CFFF	SYS-CTI1
H'E6F0D000 to H'E6F1EFFF	H'8000D000 to H'8001EFFF	Reserved
H'E6F1F000 to H'E6F1FFFF	H'8001F000 to H'8001FFFF	CS-Reg
H'E6F20000 to H'E6F7FFFF	H'80020000 to H'8007FFFF	Reserved
H'E6F80000 to H'E6F80FFF	H'80080000 to H'80080FFF	2nd DAP ROM
H'E6F81000 to H'E6F81FFF	H'80081000 to H'80081FFF	CA15-ETF
H'E6F82000 to H'E6F82FFF	H'80082000 to H'80082FFF	CA15-CTICS
H'E6F83000 to H'E6F83FFF	H'80083000 to H'80083FFF	CA15-TPIU
H'E6F84000 to H'E6F84FFF	H'80084000 to H'80084FFF	CA15-TraceFunnel
H'E6F85000 to H'E6F85FFF	H'80085000 to H'80085FFF	CA15-ETR
H'E6F86000 to H'E6F9FFFF	H'80086000 to H'8009FFFF	Reserved
H'E6FA0000 to H'E6FA0FFF	H'800A0000 to H'800A0FFF	3rd DAPROM
H'E6FA1000 to H'E6FAFFFF	H'800A1000 to H'800AFFFF	Reserved
H'E6FB0000 to H'E6FB0FFF	H'800B0000 to H'800B0FFF	CA15-DBG (CPU0) / Reserved* <sup>1</sup>
H'E6FB1000 to H'E6FB1FFF	H'800B1000 to H'800B1FFF	CA15-PMU (CPU0) / Reserved* <sup>1</sup>
H'E6FB2000 to H'E6FB2FFF	H'800B2000 to H'800B2FFF	CA15-DBG (CPU1) / Reserved* <sup>1</sup>
H'E6FB3000 to H'E6FB3FFF	H'800B3000 to H'800B3FFF	CA15-PMU (CPU1) / Reserved* <sup>1</sup>
H'E6FB4000 to H'E6FB4FFF	H'800B4000 to H'800B4FFF	CA15-DBG (CPU2) / Reserved* <sup>3</sup>
H'E6FB5000 to H'E6FB5FFF	H'800B5000 to H'800B5FFF	CA15-PMU (CPU2) / Reserved* <sup>3</sup>
H'E6FB6000 to H'E6FB6FFF	H'800B6000 to H'800B6FFF	CA15-DBG (CPU3) / Reserved* <sup>3</sup>
H'E6FB7000 to H'E6FB7FFF	H'800B7000 to H'800B7FFF	CA15-PMU (CPU3) / Reserved* <sup>3</sup>
H'E6FB8000 to H'E6FB8FFF	H'800B8000 to H'800B8FFF	CA15-CTI (CPU0) / Reserved* <sup>1</sup>
H'E6FB9000 to H'E6FB9FFF	H'800B9000 to H'800B9FFF	CA15-CTI (CPU1) / Reserved* <sup>1</sup>
H'E6FBA000 to H'E6FBAFFF	H'800BA000 to H'800BAFFF	CA15-CTI (CPU2) / Reserved* <sup>3</sup>
H'E6FBB000 to H'E6FBBFFF	H'800BB000 to H'800BBFFF	CA15-CTI (CPU3) / Reserved* <sup>3</sup>
H'E6FBC000 to H'E6FBCFFF	H'800BC000 to H'800BCFFF	CA15-PTM (CPU0) / Reserved* <sup>1</sup>
H'E6FBD000 to H'E6FBDFFF	H'800BD000 to H'800BDFFF	CA15-PTM (CPU1) / Reserved* <sup>1</sup>

System Address (CPU View)	Debug-APB address (Debugger View)	module
H'E6FBE000 to H'E6FBEFFF	H'800BE000 to H'800BEFFF	CA15-PTM (CPU2) / Reserved* <sup>3</sup>
H'E6FBF000 to H'E6FBFFFF	H'800BF000 to H'800BFFFF	CA15-PTM (CPU3) / Reserved* <sup>3</sup>
H'E6FC0000 to H'E6FC0FFF	H'800C0000 to H'800C0FFF	4th DAP ROM
H'E6FC1000 to H'E6FC1FFF	H'800C1000 to H'800C1FFF	CA7-ETF
H'E6FC2000 to H'E6FC2FFF	H'800C2000 to H'800C2FFF	CA7-CTICS
H'E6FC3000 to H'E6FC3FFF	H'800C3000 to H'800C3FFF	CA7-TPIU
H'E6FC4000 to H'E6FC4FFF	H'800C4000 to H'800C4FFF	CA7-TraceFunnel
H'E6FC5000 to H'E6FC5FFF	H'800C5000 to H'800C5FFF	CA7-ETR
H'E6FC6000 to H'E6FDFFFF	H'800C6000 to H'800DFFFF	Reserved
H'E6FE0000 to H'E6FE0FFF	H'800E0000 to H'800E0FFF	5th DAPROM
H'E6FE1000 to H'E6FEFFFF	H'800E1000 to H'800EFFFF	Reserved
H'E6FF0000 to H'E6FF0FFF	H'800F0000 to H'800F0FFF	CA7-DBG (CPU0) / Reserved* <sup>2</sup>
H'E6FF1000 to H'E6FF1FFF	H'800F1000 to H'800F1FFF	CA7-PMU (CPU0) / Reserved* <sup>2</sup>
H'E6FF2000 to H'E6FF2FFF	H'800F2000 to H'800F2FFF	CA7-DBG (CPU1) / Reserved* <sup>2</sup>
H'E6FF3000 to H'E6FF3FFF	H'800F3000 to H'800F3FFF	CA7-PMU (CPU1) / Reserved* <sup>2</sup>
H'E6FF4000 to H'E6FF4FFF	H'800F4000 to H'800F4FFF	CA7-DBG (CPU2) / Reserved* <sup>3</sup>
H'E6FF5000 to H'E6FF5FFF	H'800F5000 to H'800F5FFF	CA7-PMU (CPU2) / Reserved* <sup>3</sup>
H'E6FF6000 to H'E6FF6FFF	H'800F6000 to H'800F6FFF	CA7-DBG (CPU3) / Reserved* <sup>3</sup>
H'E6FF7000 to H'E6FF7FFF	H'800F7000 to H'800F7FFF	CA7-PMU (CPU3) / Reserved* <sup>3</sup>
H'E6FF8000 to H'E6FF8FFF	H'800F8000 to H'800F8FFF	CA7-CTI (CPU0) / Reserved* <sup>2</sup>
H'E6FF9000 to H'E6FF9FFF	H'800F9000 to H'800F9FFF	CA7-CTI (CPU1) / Reserved* <sup>2</sup>
H'E6FFA000 to H'E6FFAFFF	H'800FA000 to H'800FAFFF	CA7-CTI (CPU2) / Reserved* <sup>3</sup>
H'E6FFB000 to H'E6FFBFFF	H'800FB000 to H'800FBFFF	CA7-CTI (CPU3) / Reserved* <sup>3</sup>
H'E6FFC000 to H'E6FFCFFF	H'800FC000 to H'800FCFFF	CA7-ETM (CPU0) / Reserved* <sup>2</sup>
H'E6FFD000 to H'E6FFDFFF	H'800FD000 to H'800FDFFF	CA7-ETM (CPU1) / Reserved* <sup>2</sup>
H'E6FFE000 to H'E6FFEFFF	H'800FE000 to H'800FEFFF	CA7-ETM (CPU2) / Reserved* <sup>3</sup>
H'E6FFF000 to H'E6FFFFF	H'800FF000 to H'800FFFFF	CA7-ETM (CPU3) / Reserved* <sup>3</sup>

Notes: Do not write to any addresses other than listed above. Operations cannot be guaranteed if writing is attempted.  
Values read from addresses other than those listed above are undefined.

1. Only RZ/G1H, RZ/G1M, RZ/G1N.
2. Only RZ/G1H, RZ/G1E.
3. Only RZ/G1H.

CPU and the product correspondence are as follows.

CortexA-15	CPU0/CPU1	[RZ/G1H, RZ/G1M, RZ/G1N]
CortexA-15	CPU2/CPU3	[RZ/G1H]
CortexA-7	CPU0/CPU1	[RZ/G1H, RZ/G1E]
CortexA-7	CPU2/CPU3	[RZ/G1H]

### 62.5 Cross Trigger Connection

RZ/G1H	RZ/G1N
RZ/G1M	RZ/G1E

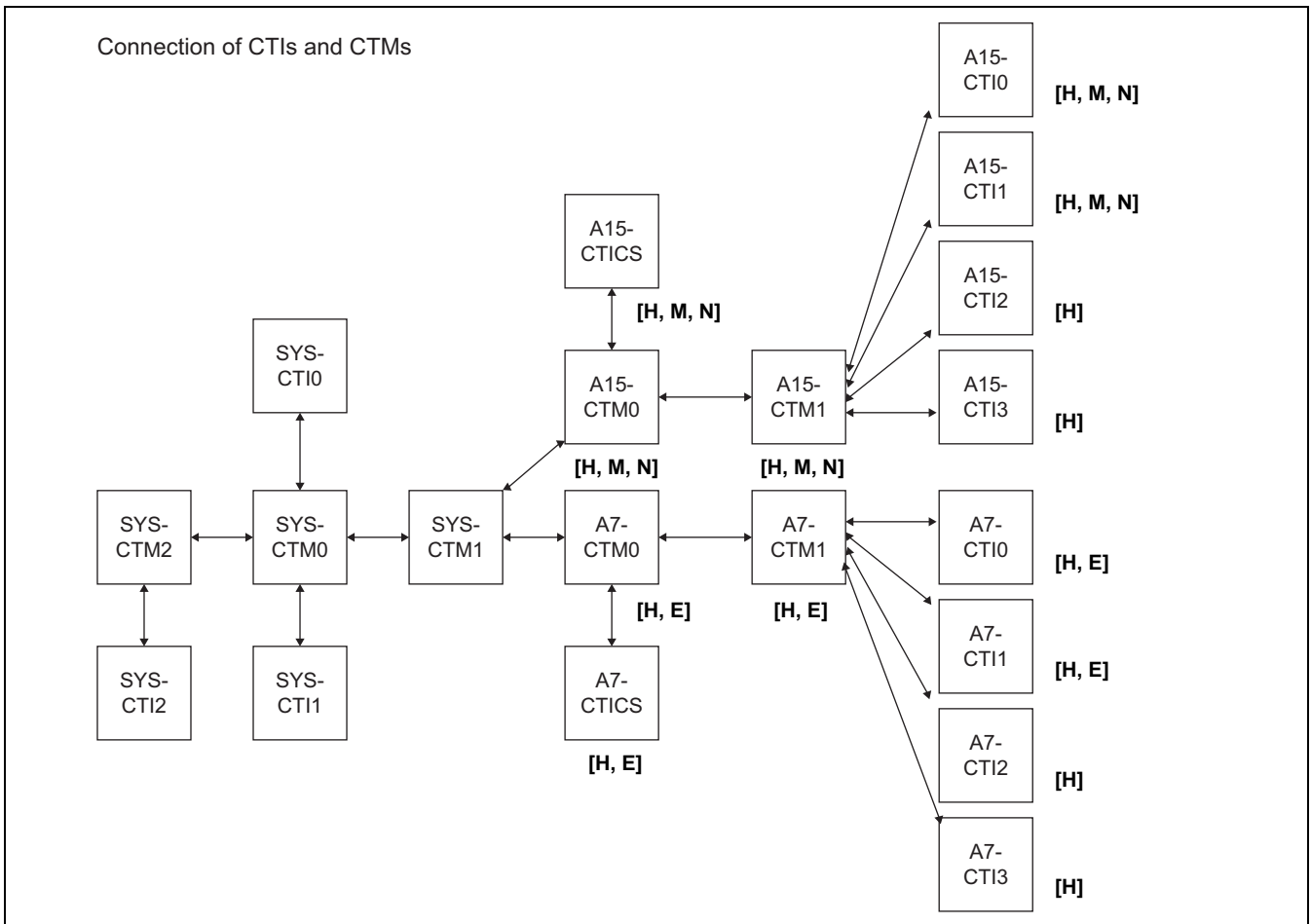


Figure 62.2 Cross Trigger Connection



## 62.6 SYS-CTI0 Trigger Connection

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

**Table 62.8** SYS-CTI0 Trigger Inputs

Trigger Input Bit	Trigger Signal	Source Device
[7]	HTMEXTOUT[1]	SYS-HTM
[6]	HTMEXTOUT[0]	SYS-HTM
[5]	HTMTRIGGER	SYS-HTM
[4]	Not in use	
[3]	ACQCOMP	SYS-ETF
[2]	FULL	SYS-ETF
[1]	Not in use	
[0]	Not in use	

**Table 62.9** SYS-CTI0 Trigger Outputs

Trigger Output Bit	Trigger Signal	Destination Device
[7]	Reserved (not in use)	
[6]	Not in use	
[5]	HTMEXTIN[1]	SYS-HTM
[4]	HTMEXTIN[0]	SYS-HTM
[3]	TRIGIN	SYS-TPIU
[2]	FLUSHIN	SYS-TPIU
[1]	TRIGIN	SYS-ETF
[0]	FLUSHIN	SYS-ETF

## 62.7 SYS-CTI1 Trigger Connection

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

**Table 62.10** SYS-CTI1 Trigger Inputs

Trigger Input Bit	Trigger Signal	Source Device
[7]	ASYNCOUT	SYS-STM
[6]	TRIGOUTHETE	SYS-STM
[5]	TRIGOUTSW	SYS-STM
[4]	TRIGOUTSPTE	SYS-STM
[3]	Not in use	
[2]	Not in use	
[1]	Not in use	
[0]	Not in use	

**Table 62.11** SYS-CTI1 Trigger Outputs

Trigger Output Bit	Trigger Signal	Destination Device
[7]	Not in use	
[5]	HWEVENTS[3:2]	SYS-STM
[4]	HWEVENTS[1:0]	SYS-STM
[3]	TRIGIN	SYS-TPIU-STM
[2]	FLUSHIN	SYS-TPIU-STM
[1]	Not in use	
[0]	Not in use	

## 62.8 SYS-CTI2 Trigger Connection

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

**Table 62.12** SYS-CTI2 Trigger Inputs

Trigger Input Bit	Trigger Signal	Source Device
[7]	Reserved (not in use)	
[6]	spubrkreq	SPU
[5]	Not in use	
[4]	Not in use	
[3]	Not in use	
[2]	Not in use	
[1]	Not in use	
[0]	Not in use	

**Table 62.13** SYS-CTI2 Trigger Outputs

Trigger Output Bit	Trigger Signal	Destination Device
[7]	Reserved (not in use)	
[6]	ctibrkreq	SPU
[5]	Not in use	
[4]	Not in use	
[3]	Not in use	
[2]	Not in use	
[1]	Not in use	
[0]	Not in use	

## 62.9 CA15-CTI[0-3] Trigger Connection

RZ/G1H	RZ/G1N
RZ/G1M	RZ/G1E

Note: CA15-CTI[0, 1] only RZ/G1H, RZ/G1M, RZ/G1N.  
CA15-CTI[2, 3] only RZ/G1H.

**Table 62.14 CA15-CTI[0-3] (CA15-CTI[0, 1]) Trigger Inputs**

Trigger Input Bit	Trigger Signal	Source Device
[7]	Not in use	
[6]	PTMTRIGGER	PTM-A15
[5]	COMMRX	Cortex-A15
[4]	COMMTX	Cortex-A15
[3]	EXTOUT[1]	PTM-A15
[2]	EXTOUT[0]	PTM-A15
[1]	PMUIRQ	Cortex-A15
[0]	DBGTRIGGER	Cortex-A15

**Table 62.15 CA15-CTI[0-3] (CA15-CTI[0, 1]) Trigger Outputs**

Trigger Output Bit	Trigger Signal	Destination Device
[7]	DBGRESTART	Cortex-A15
[6]	nCTIIRQ	INTC for ARM
[5]	Not in use	
[4]	EXTIN[3]	PTM-A15
[3]	EXTIN[2]	PTM-A15
[2]	EXTIN[1]	PTM-A15
[1]	EXTIN[0]	PTM-A15
[0]	EDBGRQ	Cortex-A15

## 62.10 CA15-CTICS Trigger Connection

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

Note: CA15-CTICS only RZ/G1H, RZ/G1M, RZ/G1N.

**Table 62.16 CA15-CTICS Trigger Inputs**

Trigger Input Bit	Trigger Signal	Source Device
[7]	Not in use	
[6]	Not in use	
[5]	Not in use	
[4]	Not in use	
[3]	ACQCOMP	A15-ETF
[2]	FULL	A15-ETF
[1]	ACQCOMP	A15-ETR
[0]	FULL	A15-ETR

**Table 62.17 CA15-CPU-CTICS Outputs**

Trigger Output Bit	Trigger Signal	Destination Device
[7]	TRIGIN	A15-ETR
[6]	FLUSHIN	A15-ETR
[5]	Not in use	
[4]	Not in use	
[3]	TRIGIN	A15-TPIU
[2]	FLUSHIN	A15-TPIU
[1]	TRIGIN	A15-ETF
[0]	FLUSHIN	A15-ETF

## 62.11 CA7-CTI[0-3] Trigger Connection

RZ/G1H	RZ/G1N
RZ/G1M	RZ/G1E

Note: CA7-CTI[0, 1] only RZ/G1H, RZ/G1E.  
CA7-CTI[2, 3] only RZ/G1H.

**Table 62.18 CA7-CTI[0-3] (CA7-CTI[0, 1]) Trigger Inputs**

Trigger Input Bit	Trigger Signal	Source Device
[7]	Not in use	
[6]	ETMTRIGGER	ETM-A7
[5]	COMMRX	Cortex-A7
[4]	COMMTX	Cortex-A7
[3]	EXTOUT[1]	ETM-A7
[2]	EXTOUT[0]	ETM-A7
[1]	nPMUIRQ	Cortex-A7
[0]	DBGTRIGGER	Cortex-A7

**Table 62.19 CA7-CTI[0-3] (CA7-CTI[0, 1]) Trigger Outputs**

Trigger Output Bit	Trigger Signal	Destination Device
[7]	DBGRESTART	Cortex-A7
[6]	nCTIIRQ	INTC for ARM
[5]	Not in use	
[4]	EXTIN[3]	ETM-A7
[3]	EXTIN[2]	ETM-A7
[2]	EXTIN[1]	ETM-A7
[1]	EXTIN[0]	ETM-A7
[0]	DBGRRQ	Cortex-A7

## 62.12 CA7-CTICS Trigger Connection



Note: CA7-CTICS only RZ/G1H, RZ/G1E.

**Table 62.20 CA7-CTICS Trigger Inputs**

Trigger Input Bit	Trigger Signal	Source Device
[7]	Not in use	
[6]	Not in use	
[5]	Not in use	
[4]	Not in use	
[3]	ACQCOMP	A7-ETF
[2]	FULL	A7-ETF
[1]	ACQCOMP	A7-ETR
[0]	FULL	A7-ETR

**Table 62.21 CA7-CPU-CTICS Outputs**

Trigger Output Bit	Trigger Signal	Destination Device
[7]	TRIGIN	A7-ETR
[6]	FLUSHIN	A7-ETR
[5]	Not in use	
[4]	Not in use	
[3]	TRIGIN	A7-TPIU
[2]	FLUSHIN	A7-TPIU
[1]	TRIGIN	A7-ETF
[0]	FLUSHIN	A7-ETF

## 62.13 CSReg

### 62.13.1 ATCLKCR\_CA15 Register

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address CPU view: H'E6F1F100 Debugger view: H'8001F100

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16							
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0							
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W							
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0							
	ATCLK_DIV[7:0]														—	—	—	—	—	—	—	—	ATCLK_DIVEN
Initial value:	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1						
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W						

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	Reserved	All 0	R/W	Reserved
15 to 8	ATCLK_DIV[7:0]	H'01	R/W	
7 to 1	Reserved	All 0	R/W	Reserved
0	ATCLK_DIVEN	1	R/W	

### 62.13.2 LOCKACCESS Register

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address CPU view: H'E6F1FFB0 Debugger view: H'8001FFB0

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	—	—	W	Lock Access Register See CoreSight Architecture Specification



### 62.13.3 LOCKSTATUS Register

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address CPU view: H'E6F1FFB4 Debugger view: H'8001FFB4

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	—	H'0000_0003	R	Lock Status Register See CoreSight Architecture Specification

### 62.13.4 Peripheral ID4 Register

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address CPU view: H'E6F1FFD0 Debugger view: H'8001FFD0

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	4KB count			JEP106 continuation code				
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved
7 to 4	4KB count	H'0	R	
3 to 0	JEP106 continuation code	H'4	R	

### 62.13.5 Peripheral ID0 Register

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address CPU view: H'E6F1FFE0 Debugger view: H'8001FFE0

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	Part No.0							
Initial value:	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	H'0000_00	R	Reserved
7 to 0	Part No.0	H'AA	R	

### 62.13.6 Peripheral ID1 Register

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address CPU view: H'E6F1FFE4 Debugger view: H'8001FFE4

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	JEP106 ID code[3:0]			Part No.1				
Initial value:	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	H'0000_00	R	Reserved
7 to 4	JEP106 ID code[3:0]	H'3	R	
3 to 0	Part No.1	H'F	R	

### 62.13.7 Peripheral ID2 Register

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address CPU view: H'E6F1FFE8 Debugger view: H'8001FFE8

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	Rev			1'b1	JEP106 ID code[6:4]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	H'0000_00	R	Reserved
7 to 4	Rev	H'0	R	
3	1'b1	1	R	
2 to 0	JEP106 ID code[6:4]	H'2	R	

### 62.13.8 Peripheral ID3 Register

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address CPU view: H'E6F1FFEC Debugger view: H'8001FFEC

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	RevAnd			CustomrModified				
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	H'0000_00	R	Reserved
7 to 4	RevAnd	H'0	R	
3 to 0	CustomrModified	H'0	R	

### 62.13.9 Component ID0 Register

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address CPU view: H'E6F1FFF0 Debugger view: H'8001FFF0

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	Preamble							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	H'0000_00	R	Reserved
7 to 0	Preamble	H'0D	R	

### 62.13.10 Component ID1 Register

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address CPU view: H'E6F1FFF4 Debugger view: H'8001FFF4

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	Component class				Preamble			
Initial value:	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	H'0000_00	R	Reserved
7 to 4	Component class	H'F	R	
3 to 0	Preamble	H'0	R	

### 62.13.11 Component ID2 Register

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address CPU view: H'E6F1FFF8 Debugger view: H'8001FFF8

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	Preamble							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	H'0000_00	R	Reserved
7 to 0	Preamble	H'05	R	

### 62.13.12 Component ID3 Register

RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
√	√	√	√

Address CPU view: H'E6F1FFFC Debugger view: H'8001FFFC

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	Preamble							
Initial value:	0	0	0	0	0	0	0	0	1	0	1	1	0	0	0	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	H'0000_00	R	Reserved
7 to 0	Preamble	H'B1	R	

## 63. Electrical Characteristics

### 63.1 Absolute Maximum Ratings

<b>RZ/G1H</b>	<b>RZ/G1N</b>
<b>RZ/G1M</b>	<b>RZ/G1E</b>

**Table 63.1.1 Absolute Maximum Ratings**

Item	Value	Unit	Remarks
Power supply voltage (3.3 V) (VCCQ, VCCQ33_MLBP, VCCQ_SD (SDHI), VD331)	-0.3 to +4.6	V	H, M and N
Power supply voltage (3.3 V) (VCCQ, VCCQ_SD/VCCQ_MMC_SD (SDHI), VD331)			E
Power supply voltage (1.8 V) (AVDD, VCCQ18, VCCQ_ISO, VCCQ_SD (SDR50/SDR104), VDD_CPGPLL, VDDA_SATA0/1, VDDQ_LVDS, VCCQ18_MLBP, VDDQ_M0APLL, VDDQ_M1APLL, VDDQ_M0DPLL, VDDQ_M1DPLL, VDDQ_M1MPLL, DU/DU0_LVDS0/LVDS_PLL1_VCC (H/M), DU_LVDS1_PLL1_VCC (H only), VDD_MLBPPLL, VDD_MLBPPLL0, VDD_MLBPPLL1)	-0.3 to +2.5	V	H, M and N (DU_LVDS1_PLL1_VCC: H only)
Power supply voltage (1.8 V) (AVDD, VCCQ18, VCCQ_SD/VCCQ_MMC_SD (SDR50/SDR104), VDD_CPGPLL, VDD_MLBPPLL, VDDQ_M0APLL, VDDQ_M0DPLL)			E
Power supply voltage (1.5V) (VDDQ_M0)	-0.3 to +1.875	V	—
Power supply voltage (1.5V) (VDDQ_M1, VDDQ_M1A)			H and M
Power supply voltage (1.35 V) (VDDQ_M0)	-0.3 to +1.75	V	—
Power supply voltage (1.35 V) (VDDQ_M1, VDDQ_M1A)			H and M
Power supply voltage (1.0 V) (VDD)	-0.3 to +1.26	V	—
Power supply voltage (1.0 V) (VDD_DVFS, VDDD_SATA0/1)			H, M and N
Input voltage (3.3-V I/O, 3.3-V tolerant I/O)	-0.3 to VCCQ + 0.3	V	*1
Input voltage (3.3-V I/O)	-0.3 to VCCQ33_MLBP + 0.3	V	*1, H, M and N
Input voltage (3.3-V I/O [SDHI])	-0.3 to VCCQ_SD/VCCQ_MMC_ SD + 0.3	V	*1, H, M, N and E
Input voltage (1.8-V I/O)	-0.3 to VCCQ18 + 0.3	V	*2, except for 3.3-V tolerant I/O
Input voltage (1.8-V I/O [SDHI (SDR50/SDR104)])	-0.3 to VCCQ_SD/VCCQ_MMC_ SD + 0.3	V	*2, H, M, N and E
Input voltage (1.8-V I/O)	-0.3 to VCCQ18_MLBP + 0.3	V	*2, H, M and N
Input voltage (1.5-V I/O [DDR3])	-0.3 to VDDQ_M0/M1/M1A + 0.3	V	*3, H and E, M1/M1A: H

Item	Value	Unit	Remarks
Input voltage (1.35-V I/O [DDR3L])	-0.3 to VDDQ_M0/M1/M1A + 0.3	V	*4, M and N, M1/M1A: M
Input voltage (1.0-V I/O [SATA])	-0.3 to VDDD_SATA0/1 + 0.3	V	*5, H, M and N
Input voltage (USB0_OVC/VBUS pin, USB1_OVC pin [USB2.0])	-0.3 to VCCQ + 0.3	V	*1, H, M, N and E
Output voltage (3.3-V I/O, 3.3-V tolerant I/O)	-0.3 to VCCQ + 0.3	V	*1
Output voltage (3.3-V I/O)	-0.3 to VCCQ33_MLBP + 0.3	V	*1, H, M and N
Output voltage (3.3-V I/O [SDHI])	-0.3 to VCCQ_SD/VCCQ_MMC_ SD + 0.3	V	*1, H, M, N and E
Output voltage (1.8-V)	-0.3 to VCCQ18 + 0.3	V	*2, except for 3.3-V tolerant I/O
Output voltage (1.8-V I/O [SDHI (SDR50/SDR104)])	-0.3 to VCCQ_SD/VCCQ_MMC_ SD + 0.3	V	*2, H, M, N and E
Output voltage (1.8-V I/O [DU/LVDS])	-0.3 to VDDQ_LVDS + 0.3	V	*2, H, M and N
Output voltage (1.8-V I/O)	-0.3 to VCCQ18_MLBP + 0.3	V	*2, H, M and N
Output voltage (1.5-V I/O [DDR3])	-0.3 to VDDQ_M0/M1/M1A + 0.3	V	*3, H and E, M1/M1A: H
Output voltage (1.35-V I/O [DDR3L])	-0.3 to VDDQ_M0/M1/M1A + 0.3	V	*4, M and N, M1/M1A: M
Output voltage (1.0-V I/O [SATA])	-0.3 to VDDD_SATA0/1 + 0.3	V	*5, H, M and N
Operating temperature	-40 to +105	°C	Tc (case)
	-40 to +85	°C	Ta (ambient)
Storage temperature	-55 to +125	°C	Ta (ambient)

Notes: Permanent damage to the LSI may result if absolute maximum ratings are exceeded. In normal operation, this LSI should be used within the specifications described in the following descriptions. If this LSI is not used within the specifications, the reliability of this LSI may lower.

Voltages are referenced at GND = VSS = AVSS = 0 V.

Abbreviations in the tables have the following meanings.

SDHI: SDHI does not operate through SDR50/SDR104.

SDHI (SDR50/SDR104): SDHI operates through SDR50/SDR104.

For details of the number of channels or available modules, refer to each manual; SHDI, DU/LVDS, SATA/PCIEC/USB3.0, DBSC3 (DDR) and USB2.0 (AVDD).

1. Do not exceed 4.6 V.
2. Do not exceed 2.5 V.
3. Do not exceed 1.875V.
4. Do not exceed 1.75V.
5. Do not exceed 1.26V.



## 63.2 Power Supply

<b>RZ/G1H</b>	<b>RZ/G1N</b>
<b>RZ/G1M</b>	<b>RZ/G1E</b>

**Table 63.2.1 Power Supply (H, M, N and E)**

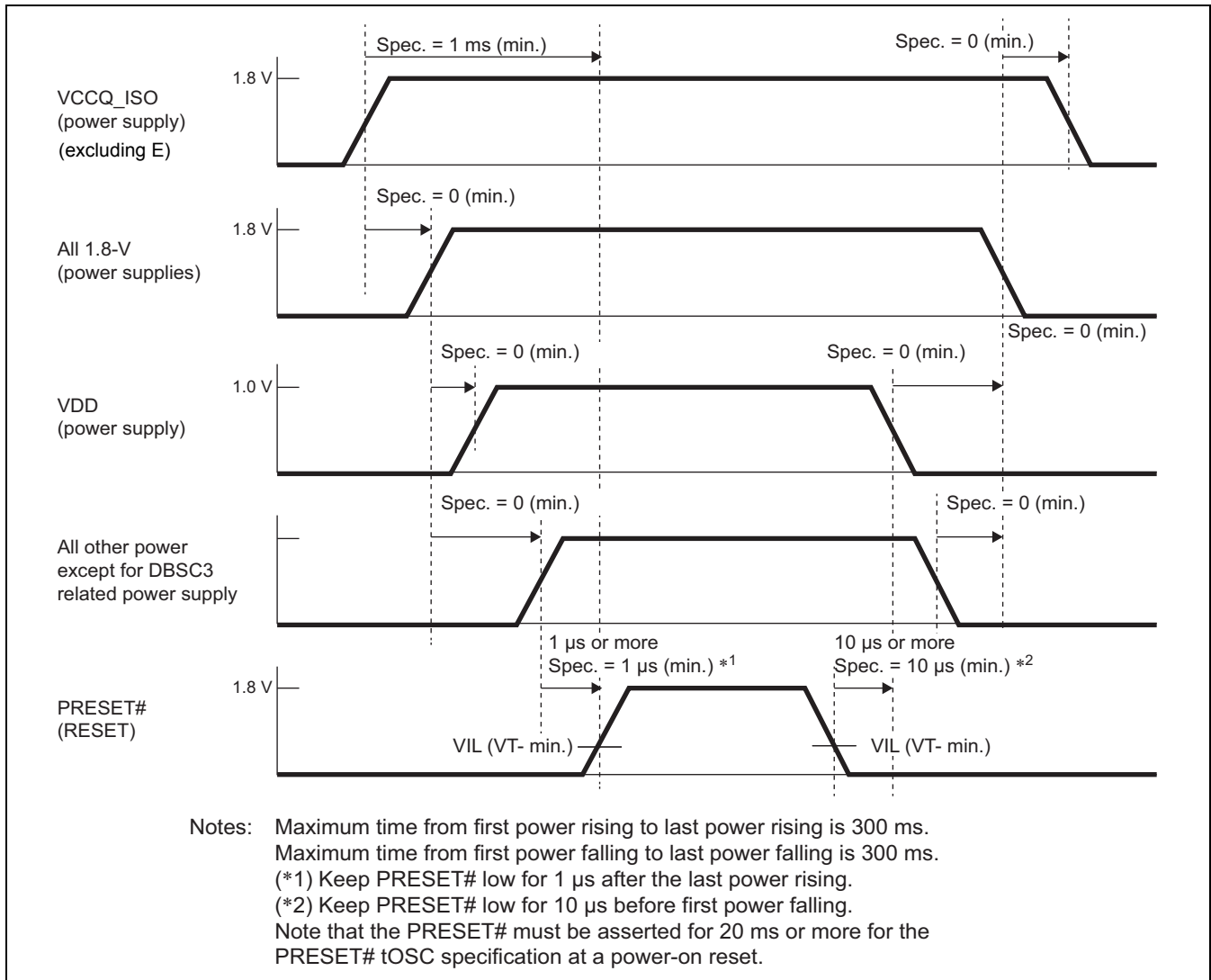
Item	Symbol	Voltage			Unit	Remarks
		Min.	Typ.	Max.		
Power supply (Internal)	VDD	0.98	1.03	1.08	V	VDD for power supply and VSS for ground
Power supply (3.3-V I/O)	VCCQ	3.0	3.3	3.6	V	VCCQ for power supply and VSS for ground
Power supply (3.3-V I/O) (excluding E)	VCCQ33_MLBP	3.0	3.3	3.6	V	VCCQ33_MLBP for power supply and VSS for ground
Power supply (3.3-V I/O [SDHI])	VCCQ_SD0 to VCCQ_SD3, VCCQ_MMC_SD2	3.0	3.3	3.6	V	VCCQ_SD0 to VCCQ_SD3, VCCQ_MMC_SD2 for power supply and VSS for ground
Power supply ([VCCQ_ISO]) (excluding E)	VCCQ_ISO	1.7	1.8	1.9	V	VCCQ_ISO for power supply and VSS for ground
Power supply (1.8-V I/O [VCCQ18])	VCCQ18	1.7	1.8	1.9	V	VCCQ18 for power supply and VSS for ground
Power supply (1.8-V I/O) (excluding E)	VCCQ18_MLBP	1.7	1.8	1.9	V	VCCQ18_MLBP for power supply and VSS for ground
Power supply (1.8-V I/O [SDHI(SDR50/SDR104)])	VCCQ_SD0 to VCCQ_SD3, VCCQ_MMC_SD2	1.7	1.8	1.9	V	VCCQ_SD0 to VCCQ_SD3, VCCQ_MMC_SD2 for power supply and VSS for ground
Power supply (1.8-V I/O [DU/LVDS]) (excluding E)	VDDQ_LVDS	1.7	1.8	1.9	V	VDDQ_LVDS for power supply and VSS for ground
Power supply (1.5-V I/O [DDR3])	VDDQ_M0 (H, M, N, E), VDDQ_M1 (H, M), VDDQ_M1A (H, M)	1.425	1.5	1.575	V	VDDQ_M0, VDDQ_M1 and VDDQ_M1A for power supply and VSS for ground
Power supply (1.35-V I/O [DDR3L])	VDDQ_M1 (H, M), VDDQ_M1A (H, M)	1.283	1.35	1.450	V	
Power supply (USB3.0) (excluding E)	VDDA_SATA0	1.7	1.8	1.9	V	VDDA_SATA0 for power supply and VSS_SATA0 for ground
	VDDD_SATA0	0.98	1.03	1.08	V	VDDD_SATA0 for power supply and VSS_SATA0 for ground
Power supply (PCI-E) (excluding E)	VDDA_SATA1 (H, M)	1.7	1.8	1.9	V	VDDA_SATA1 for power supply and VSS_SATA1 for ground
	VDDA_SATA0 (N)					VDDA_SATA0 for power supply and VSS_SATA0 for ground
	VDDD_SATA1 (H, M)	0.98	1.03	1.08	V	VDDD_SATA1 for power supply and VSS_SATA1 for ground
	VDDD_SATA0 (N)					VDDD_SATA0 for power supply and VSS_SATA0 for ground

Item	Symbol	Voltage			Unit	Remarks
		Min.	Typ.	Max.		
Power supply (SATA) (excluding E)	VDDA_SATA0 (H, M, N)	1.7	1.8	1.9	V	VDDA_SATA0, VDDA_SATA1 for power supply and VSS_SATA0, VSS_SATA1 for ground respectively
	VDDA_SATA1 (H, M)					
	VDDD_SATA0 (H, M, N)	0.98	1.03	1.08	V	VDDD_SATA0, VDDD_SATA1 for power supply and VSS_SATA0, VSS_SATA1 for ground respectively
	VDDD_SATA1 (H, M)					
Power supply (PLL [CPG])	VDD_CPGPLL	1.7	1.8	1.9	V	VDD_CPGPLL for power supply and VSS_CPGPLL for ground
Power supply (PLL [DDR3/DDR3L])	VDDQ_M0DPLL VDDQ_M1DPLL VDDQ_M1MPLL VDDQ_M0APLL VDDQ_M1APLL	1.7	1.8	1.9	V	VDDQ_M0DPLL, VDDQ_M1DPLL, VDDQ_M1MPLL, VDDQ_M0APLL, VDDQ_M1APLL for power supply and VSSQ_M0DPLL, VSSQ_M1DPLL, VSSQ_M1MPLL, VSSQ_M0APLL, VSSQ_M1APLL for ground respectively
Power supply (PLL [DU/LVDS]) (excluding E)	DU/DU0_LVDS0/L VDS_PLL1_VCC (H/M/N), DU_LVDS1_PLL1 _VCC (H)	1.7	1.8	1.9	V	DU/DU0_LVDS0/LVDS_PLL1_V CC, DU_LVDS1_PLL1_VCC for power supply and DU/DU0_LVDS0/LVDS_PLL1_V SS, DU_LVDS1_PLL1_VSS for ground respectively
Power supply (PLL)	VDD_MLBPLL	1.7	1.8	1.9	V	VDD_MLBPLL for power supply and VSS_MLBPLL for ground
	VDD_MLBPPLL0 (H,M,N)	1.7	1.8	1.9	V	VDD_MLBPPLL0 for power supply and VSS_MLBPPLL0 for ground
	VDD_MLBPPLL1 (H,M,N)	1.7	1.8	1.9	V	VDD_MLBPPLL1 for power supply and VSS_MLBPPLL1 for ground
Power supply (USB2.0)	AVDD	1.7	1.8	1.9	V	AVDD for power supply and AVSS for ground
	VD331	3.0	3.3	3.6	V	VD331 for power supply and VSS for ground
	VD181	1.7	1.8	1.9	V	VD181 for power supply and VSS for ground
Power supply (DVFS) (excluding E)	VDD_DVFS	0.98	1.03	1.08	V	VDD_DVFS for power supply and VSS for ground

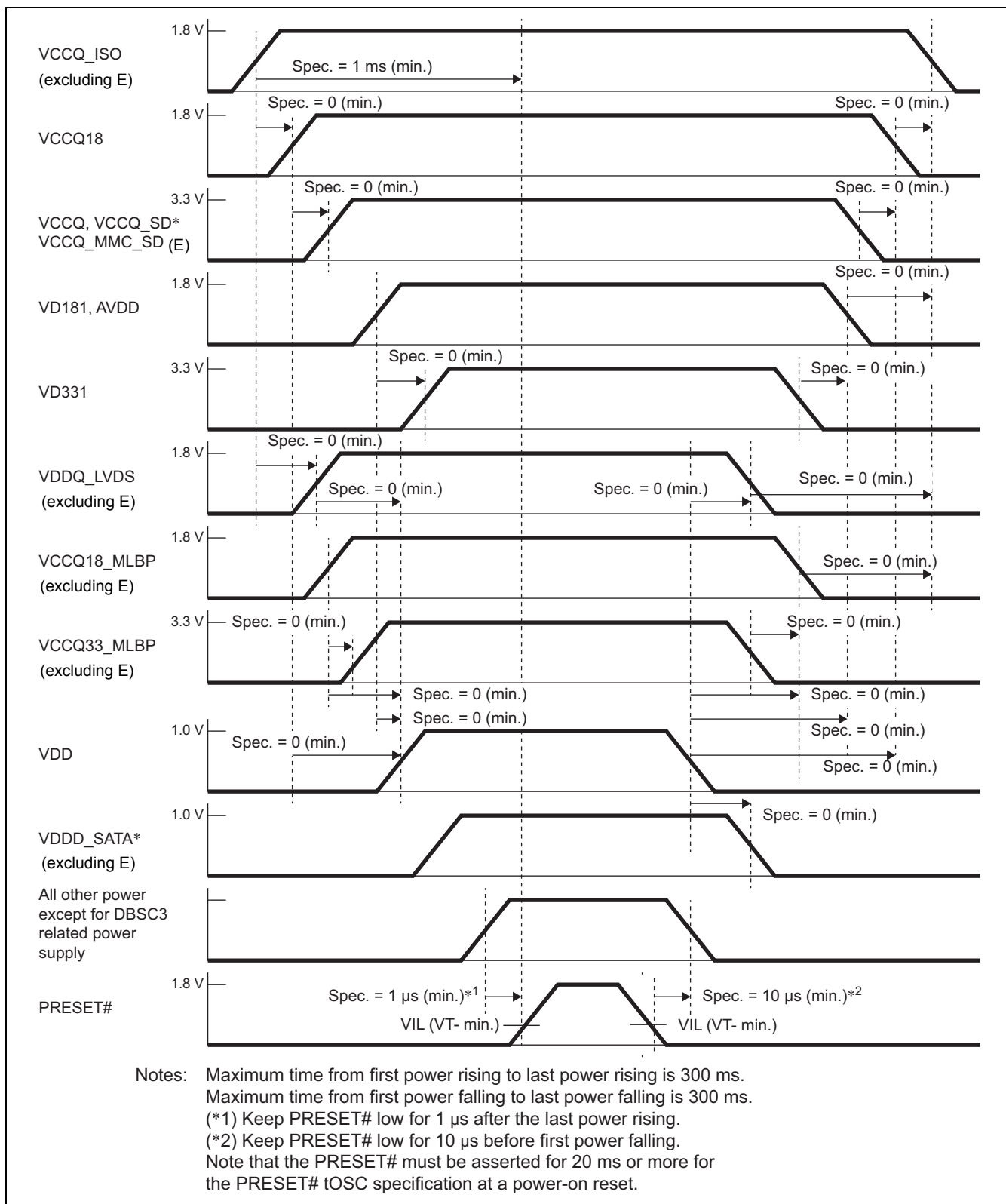
### 63.3 Sequence of Turning On/Off Power Supplies

<b>RZ/G1H</b>	<b>RZ/G1N</b>
<b>RZ/G1M</b>	<b>RZ/G1E</b>

#### (1) Power Sequence (Abstract)



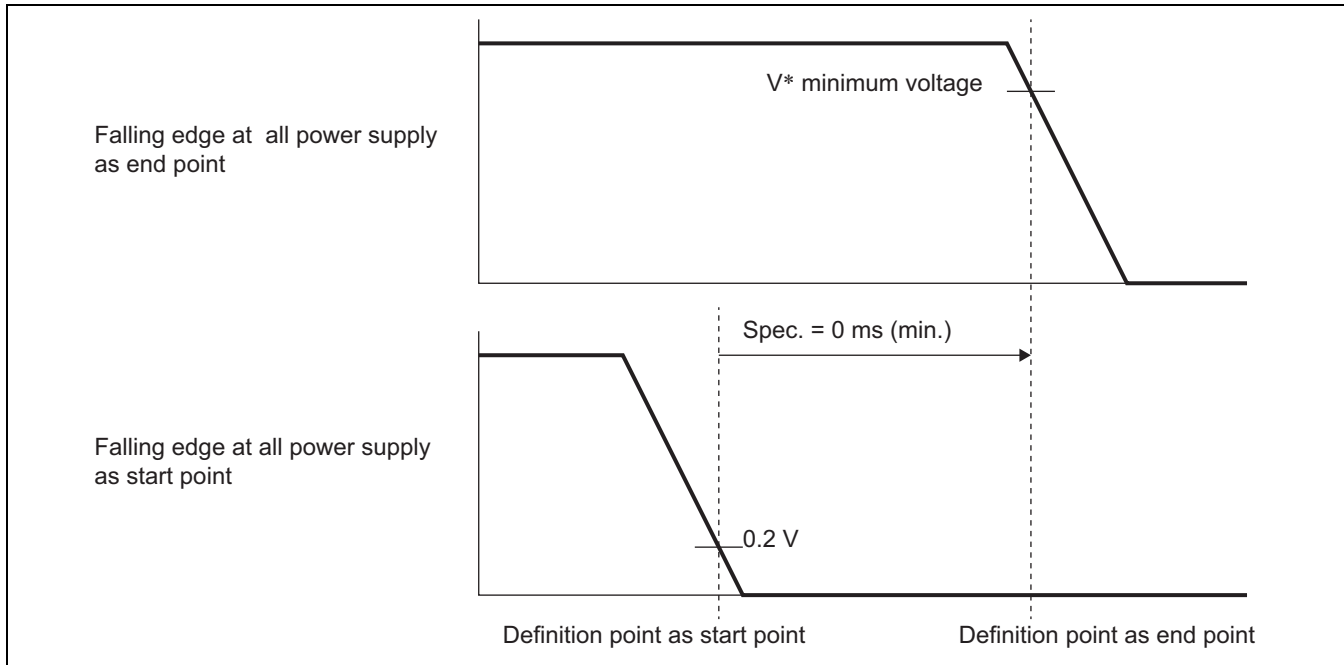
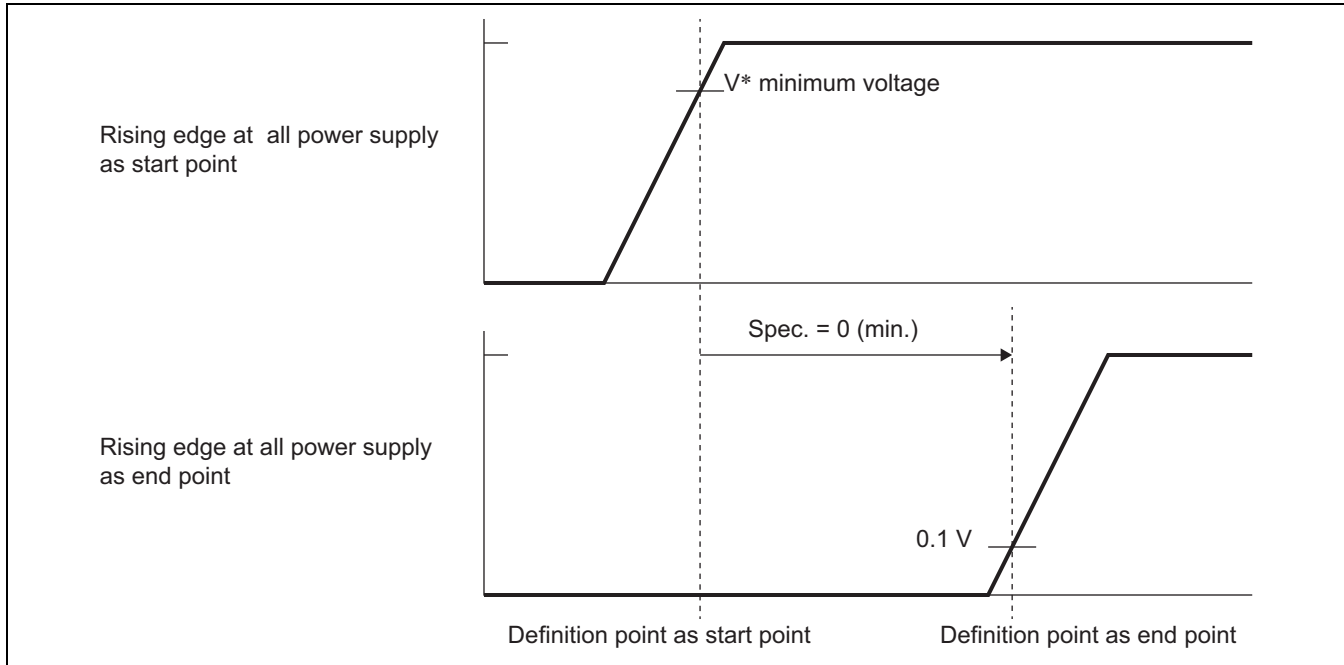
(2) Power Sequence (Details)



63.3.1 Wave form definition for power sequence

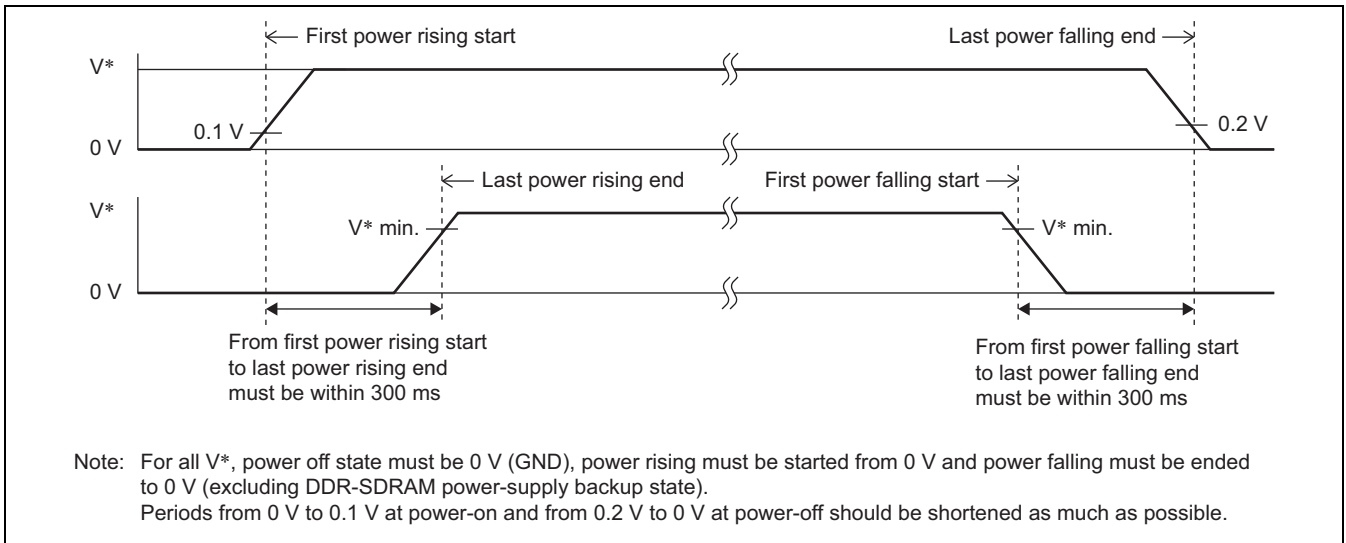
RZ/G1H	RZ/G1N
RZ/G1M	RZ/G1E

This definition is for the different voltage power supply for example between 1.8-V and 3.3-V, it is possible to turn on or off at the same time for the same voltage power supply.



63.3.2 Power On and Power Off Wave Form

<b>RZ/G1H</b>	<b>RZ/G1N</b>
<b>RZ/G1M</b>	<b>RZ/G1E</b>



## 63.4 DC Characteristics

**Table 63.4.1 Supply Current (RZ/G1H and M)**
**RZ/G1H**
**RZ/G1M**

Conditions: Each power supply and ground are separated, ground is 0 V respectively,  
 T<sub>c</sub> = -40 to +105 °C (-20 to +105 °C for SDR104 only).

Item		Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply current (internal)	Normal	IDD	—	—	5300	mA	VDD = 1.08 V [H]
					3600	mA	VDD = 1.08 V [M]
Supply current (internal)	Normal	IDD_DVFS	—	—	11200	mA	VDD_DVFS = 1.08 V [H]
					5500	mA	VDD_DVFS = 1.08 V [M]
Supply current (3.3-V I/O)	Normal	ICCQ	—	—	100	mA	VCCQ = 3.6 V Local bus Access only case Current from/to external load is not included.
Supply current (3.3-V I/O)	Normal	ICCQ33_MLBP	—	—	80.0	mA	VCCQ33_MLBP = 3.6 V
Supply current (3.3-V I/O [SDHI])	Normal	ICCQ_SD0	—	—	18.0	mA	VCCQ_SD = 3.6 V
		ICCQ_SD1 (H only)	—	—	18.0		
		ICCQ_SD2	—	—	18.0		
		ICCQ_SD3	—	—	18.0		
Supply current (1.8-V I/O [VCCQ_ISO])	Normal	ICCQ_ISO	—	—	78	mA	VCCQ_ISO = 1.90 V
Supply current (1.8-V I/O)	Normal	ICCQ18	—	—	30	mA	VCCQ18 = 1.90 V
Supply current (1.8-V I/O)	Normal	ICCQ18_MLBP	—	—	10.0	mA	VCCQ18_MLBP = 1.90 V
Supply current (1.8-V I/O [SDHI] (SDR50, SDR104))	Normal	ICCQ_SD0	—	—	30	mA	VCCQ_SD = 1.90 V T <sub>c</sub> = -20 to +105 °C for SDR104 (SDR104: SD0 only)
		ICCQ_SD1 (H only)	—	—	30		
		ICCQ_SD2	—	—	30		
		ICCQ_SD3	—	—	30		
Supply current (1.8-V I/O [LVDS])	Normal	IDDQ_LVDS	—	—	185.0	mA	VDDQ_LVDS = 1.90 V (H; 2-channel)
					95.0	mA	VDDQ_LVDS = 1.90 V (M; 1-channel)
Supply current (1.8-V I/O [SATA0])	Normal	IDDA_SATA0	—	—	8.0	mA	VDDA_SATA0 = 1.90 V
Supply current (1.0-V [SATA0])	Normal	IDDD_SATA0	—	—	105.0	mA	VDDD_SATA0 = 1.08 V
Supply current (1.8-V I/O [SATA1])	Normal	IDDA_SATA1	—	—	8.0	mA	VDDA_SATA1 = 1.90 V
Supply current (1.0-V [SATA1])	Normal	IDDD_SATA1	—	—	105.0	mA	VDDD_SATA1 = 1.08 V

Item		Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply current (1.5-V I/O [DDR3])	Normal	IDDQ_M0	—	—	840	mA	VDDQ_M0 = 1.575 V (H only)
	DDR power supply backup		—	—	980	μA	VDDQ_M0 = 1.575 V, No Vtt termination channel 0 of 32-bit x 2- channel operation (H only)
	Normal	IDDQ_M1, IDDQ_M1A	—	—	840	mA	VDDQ_M1 = VDDQ_M1A = 1.575 V (H only)
	DDR power supply backup		—	—	980	μA	VDDQ_M1 = VDDQ_M1A = 1.575 V, No Vtt termination channel 1 of 32-bit x 2- channel operation (H only)
Supply current (1.35-V I/O [DDR3L])	Normal	IDDQ_M0	—	—	770	mA	VDDQ_M0 = 1.450 V (M only)
	DDR power supply backup		—	—	880	μA	VDDQ_M0 = 1.450 V, No Vtt termination channel 0 of 32-bit x 2- channel operation (M only)
	Normal	IDDQ_M1, IDDQ_M1A	—	—	770	mA	VDDQ_M1 = VDDQ_M1A = 1.450 V (M only)
	DDR power supply backup		—	—	880	μA	VDDQ_M1 = VDDQ_M1A = 1.450 V, No Vtt termination channel 1 of 32-bit x 2- channel operation (M only)
Supply current (PLL [CPG])		IDD_CPGPLL0	—	—	2.0	mA	VDD_CPGPLLn = 1.90 V (n = 0 to 3)
		IDD_CPGPLL1	—	—	4.0		
		IDD_CPGPLL2	—	—	2.0		
		IDD_CPGPLL3	—	—	2.0		
Supply current (PLL [DDR3/DDR3L])		IDDQ_M0DPLLn	—	—	70.0	mA	VDDQ_M0DPLLn = VDDQ_M1DPLLn = VDDQ_M1MPLL = VDDQ_M0APLL = VDDQ_M1APLL = 1.90 V (n = 0 to 3, total value)
		IDDQ_M1DPLLn	—	—	70.0		
		IDDQ_M1MPLL	—	—	12.0		
		IDDQ_M0APLL	—	—	12.0		
		IDDQ_M1APLL	—	—	12.0		
Supply current (PLL [DU/LVDS])		ICC_DU_LVDS0_ PLL1_VCC	—	—	2.0	mA	DU/DU0_LVDS0/LVDS_ PLL1_VCC = 1.90 V (H/M)
		ICC_DU_LVDS1_ PLL1_VCC	—	—	2.0		DU_LVDS1_PLL1_VCC = 1.90 V (H only)
Supply current (PLL)		IDD_MLBPLL	—	—	4.0	mA	VDD_MLBPLL
		IDD_MLBPPLL0	—	—	4.0		= VDD_MLBPPLL0



Item		Symbol	Min.	Typ.	Max.	Unit	Remarks
		IDD_MLBPPLL1	—	—	4.0		= VDD_MLBPPLL1 = 1.90 V
Supply current (USB2.0)	Normal	IDD_AVDD, IDD_VD181	—	—	102.0	mA	AVDD = VD181 = 1.90 V (total value, M) 3channel [H]
		IDD_VD331	—	—	74.0		VD331 = 3.6 V

**Table 63.4.2 Supply Current (RZ/G1N and E)****RZ/G1N****RZ/G1E**

Conditions: Each power supply and ground are separated, ground is 0 V respectively,  
 Tc = -40 to +105 °C (-20 to +105 °C for SDR104 only).

Item		Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply current (internal)	Normal	IDD	—	—	3200	mA	VDD = 1.08 V [N]
					2600	mA	VDD = 1.08 V [E]
Supply current (internal)	Normal	IDD_DVFS	—	—	5000	mA	VDD_DVFS = 1.08 V (N only)
Supply current (3.3-V I/O)	Normal	ICCQ	—	—	100	mA	VCCQ = 3.6 V Local bus Access only case Current from/to external load is not included.
Supply current (3.3-V I/O)	Normal	ICCQ33_MLBP	—	—	80.0	mA	VCCQ33_MLBP = 3.6 V (N only)
Supply current (3.3-V I/O [SDHI])	Normal	ICCQ_SD0	—	—	18.0	mA	VCCQ_SD = VCCQ_MMC_SD = 3.6 V ([N]/[E])
		ICCQ_SD2/SD1	—	—	18.0		
		ICCQ_SD3/_MMC_C_SD2	—	—	18.0		
Supply current (1.8-V I/O [VCCQ_ISO])	Normal	ICCQ_ISO	—	—	78.0	mA	VCCQ_ISO = 1.90 V (N only)
Supply current (1.8-V I/O)	Normal	ICCQ18	—	—	30.0	mA	VCCQ18 = 1.90 V
Supply current (1.8-V I/O)	Normal	ICCQ18_MLBP	—	—	10.0	mA	VCCQ18_MLBP = 1.90 V (N only)
Supply current (1.8-V I/O [SDHI] (SDR50, SDR104))	Normal	ICCQ_SD0	—	—	30.0	mA	VCCQ_SD = VCCQ_MMC_SD = 1.90 V Tc = -20 to 105 °C for SDR104 ([N]/[E]) (SDR104: SD0 only)
		ICCQ_SD2/ICCQ_SD1	—	—	30.0		
		ICCQ_SD3/ICCQ_MMC_SD2	—	—	30.0		
Supply current (1.8-V I/O [LVDS])	Normal	IDDQ_LVDS	—	—	95.0	mA	VDDQ_LVDS = 1.90 V (N only)
Supply current (1.8-V I/O [SATA0])	Normal	IDDA_SATA0	—	—	8.0	mA	VDDA_SATA0 = 1.90 V (N only)
Supply current (1.0-V [SATA0])	Normal	IDDD_SATA0	—	—	105.0	mA	VDDD_SATA0 = 1.08 V (N only)
Supply current (1.5-V I/O [DDR3])	Normal	IDDQ_M0	—	—	840	mA	VDDQ_M0 = 1.575 V (E only)
	DDR power supply backup		—	—	980	μA	VDDQ_M0 = 1.575 V, No Vtt termination (E only)
Supply current (1.35-V I/O)	Normal	IDDQ_M0	—	—	770	mA	VDDQ_M0 = 1.450 V (N only)

Item		Symbol	Min.	Typ.	Max.	Unit	Remarks
[DDR3L])	DDR power supply backup		—	—	880	μA	VDDQ_M0 = 1.450 V, No Vtt termination (N only)
3Supply current (PLL [CPG])		IDD_CPGPLL0	—	—	2.0	mA	VDD_CPGPLLn = 1.90 V (n = 0, 1, 3)
		IDD_CPGPLL1	—	—	4.0		
		IDD_CPGPLL3	—	—	2.0		
Supply current (PLL [DDR3/DDR3L])		IDDQ_M0DPLLn	—	—	70.0	mA	VDDQ_M0DPLLn = VDDQ_M0APLL = 1.90 V (n = 0 to 3, total value)
		IDDQ_M0APLL	—	—	12.0		
Supply current (PLL [DU/LVDS])		ICC_DU_LVDS0_ PLL1_VCC	—	—	2.0	mA	DU0_LVDS_PLL1_VCC = 1.90 V (N only)
Supply current (PLL)		IDD_MLBPLL	—	—	4.0	mA	VDD_MLBPLL = VDD_MLBPPLL0 = VDD_MLBPPLL1 = 1.90 V (N only)
		IDD_MLBPPLL0	—	—	4.0		
		IDD_MLBPPLL1	—	—	4.0		
Supply current (USB2.0)	Normal	IDD_AVDD, IDD_VD181	—	—	102.0	mA	AVDD = VD181 = 1.90 V (total value)
		IDD_VD331	—	—	74.0		VD331 = 3.6 V

<b>RZ/G1H</b>	<b>RZ/G1N</b>
<b>RZ/G1M</b>	<b>RZ/G1E</b>

**Table 63.4.3 DC Characteristics (3.3-V I/O)**

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement conditions	Remarks
Input high voltage	VIH	2.0	—	VCCQ + 0.3	V	VCCQ = 3.0 to 3.6 V	—
Input low voltage	VIL	-0.3	—	0.8	V		
Output high voltage	VOH	2.4	—	VCCQ + 0.3	V	VCCQ = 3.0 to 3.6 V	IOH = -4 mA
Output low voltage	VOL	-0.3	—	0.4	V		IOL = 4 mA
Pin capacitance	CL	—	—	10	pF	—	All pins*2
Pin capacitance	CL	—	—	15	pF	—	DP/DM only (H, M, N and E)
Input leakage current	ILI	—	—	1	μA	VCCQ = 3.0 to 3.6 V	All input pins*1
Output leakage current	ILO	—	—	1	μA		Hi-Z output*1
Pull-up current	IPU	8	—	250	μA	—	Vin = VSS

Notes: 1. This excludes pins with pull-up resistors, which are off.

2. Except power supply and USB pins.

<b>RZ/G1H</b>	<b>RZ/G1N</b>
<b>RZ/G1M</b>	<b>RZ/G1E</b>

**Table 63.4.4 DC Characteristics (3.3-V I/O [SDHI])**

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement conditions	Remarks
Input high voltage	VIH	0.625 × VCCQ_SD	—	VCCQ_SD + 0.3	V	VCCQ_SD = 3.0 to 3.6 V	—
Input low voltage	VIL	VSS - 0.3	—	0.25 × VCCQ_SD	V		VSS = 0 V
Output high voltage	VOH	0.75 × VCCQ_SD	—	—	V	—	IOH = -2 mA VCCQ_SDmin
Output low voltage	VOL	—	—	0.125 × VCCQ_SD	V	—	IOL = 2 mA VCCQ_SDmin
Pin capacitance	CL	—	—	10	pF	—	—
Input leakage current	ILI	—	—	1	μA	—	—
Output leakage current	ILO	—	—	1	μA	—	Hi-Z output

<b>RZ/G1H</b>	<b>RZ/G1N</b>
<b>RZ/G1M</b>	<b>RZ/G1E</b>

**Table 63.4.5 DC Characteristics (3.3-V I/O [6-pin interface])**

Item	Symbol	Min.	Typ.	Max.	Unit	
Driver Characteristics:						
Differential output voltage(steady-state)	$V_{OD}$	300	—	500	mV	
Difference in differential output voltage between (high/low) steady-states	$\Delta V_{OD}$	-50	—	+50	mV	
Common-mode output voltage	$V_{OCM}$	1.0	—	1.5	V	
Difference in common-mode output between (high/low) steady-states	$\Delta V_{OCM}$	-50	—	+50	mV	
Variations in common-mode output during a logic state transitions	$V_{CMV}$	—	—	150	mV <sub>p-p</sub>	
Short circuit current	$ I_{OS} $	—	—	43	mA	
Differential output impedance	$Z_O$	1.6	—	—	k $\Omega$	
Receiver Characteristics:						
Differential clock input	logic low steady-state	$V_{ILC}$	—	—	-50	mV
	logic high steady-state	$V_{IHC}$	+50	—	—	mV
	hysteresis	$V_{HSC}$	-25	—	+25	mV
Differential signal/data input	logic low steady-state	$V_{ILS}$	—	—	-50	mV
	logic high steady-state	$V_{IHS}$	+50	—	—	mV

<b>RZ/G1H</b>	<b>RZ/G1N</b>
<b>RZ/G1M</b>	<b>RZ/G1E</b>

**Table 63.4.6 DC Characteristics (1.8-V I/O [SDHI (SDR50, SDR104)])**

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement condition	Remarks
Input high voltage	$V_{IH}$	1.27	—	2.00	V	$V_{SS} = 0\text{ V}$	—
Input low voltage	$V_{IL}$	$V_{SS} - 0.3$	—	0.58	V		—
Output high voltage	$V_{OH}$	1.4	—	—	V		$I_{OH} = -2\text{ mA}$
Output low voltage	$V_{OL}$	—	—	0.45	V		$I_{OL} = 2\text{ mA}$
Pin capacitance	$C_L$	—	—	10	pF		—
Input leakage current	$I_{LI}$	—	—	1	$\mu\text{A}$		—
Output leakage current	$I_{LO}$	—	—	1	$\mu\text{A}$		Hi-Z output

<b>RZ/G1H</b>	<b>RZ/G1N</b>
<b>RZ/G1M</b>	<b>RZ/G1E</b>

**Table 63.4.7 DC Characteristics (1.8-V I/O [LVDS])**

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement condition	Remarks
Output high voltage	VOH	—	—	1.475	V	—	—
Output low voltage	VOL	0.925	—	—	V	—	—
Differential output voltage	Vod	0.247	—	0.454	V	—	—
Output offset voltage	Vos	1.125	—	1.375	V	—	—
Output impedance	Ro	—	100	—	Ω	—	—
Output current (vs GND)	Is	—	—	40	mA	—	—
Output short circuit current	Isab	—	—	12	mA	—	—

<b>RZ/G1H</b>	<b>RZ/G1N</b>
<b>RZ/G1M</b>	<b>RZ/G1E</b>

**Table 63.4.8 DC Characteristics (1.8-V I/O)**

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement conditions	Remarks
Schmitt input high voltage	VT+	—	—	VCCQ18 × 0.7	V	VCCQ18=1.7 to 1.9 V	PRESET#, BSMODE, MPMD0, MPMD1, and NMI pins
Schmitt input low voltage	VT-	VCCQ18 × 0.3	—	—	V		
Input high voltage	VIH	VCCQ18 × 0.8	—	VCCQ18 + 0.3	V	—	EXTAL pin
Input low voltage	VIL	-0.3	—	VCCQ18 × 0.2	V	—	—
Input high voltage (1.8-V LVCMOS)	VIH	0.65 × VCCQ18	—	VCCQ18 + 0.3	V	VCCQ18 = 1.7 to 1.9 V	Other pins (excluding I2C/IIC open-drain pins)
Input low voltage (1.8-V LVCMOS)	VIL	-0.3	—	0.35 × VCCQ18	V		
Output high voltage	VOH	0.7 × VCCQ18	—	VCCQ18 + 0.3	V	VCCQ18 = 1.7 to 1.9 V	IOH = -4 mA
Output low voltage	VOL	-0.3	—	0.4	V		IOL = 4 mA
Pin capacitance	CL	—	—	10	pF	—	—
Input leakage current	ILI	—	—	1	μA	VCCQ18 = 1.7 to 1.9 V	All input pins*1
Output leakage current	ILO	—	—	1	μA		—
Pull-up current	IPU	6	—	240	μA	—	Vin = VSS

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

**Table 63.4.9 DC Characteristics (I2C/IIC open-drain 1.8-V I/O)**

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement condition	Remarks
External pull-up voltage	VPU18	1.7	1.8	1.9	V	—	I2Cn_SCL/SDA and IICm_SCL/SDA pins (I2C/IIC open-drain assigned channels)* <sup>1</sup>
	VPU33	3.0	3.3	3.6	V	3.3 V tolerant* <sup>2</sup>	
Input high voltage	VIH	VCCQ18 × 0.7	—	VPU18 + 0.3	V	—	
		VCCQ18 × 0.7	—	VPU33 + 0.3	V	3.3 V tolerant* <sup>2</sup>	
Input low voltage	VIL	-0.3	—	0.3 × VCCQ18	V	—	
Output low voltage	VOL	—	—	0.2 × VCCQ18	V	IOL = 2 mA	
		—	—	0.4	V	IOL = 3 mA, 3.3 V tolerant* <sup>2</sup>	
Output low current	IOL	3	—	—	mA	VOL = 0.4 V 3.3 V tolerant* <sup>2</sup>	

Notes: 1. Available OD channel number of each product is as follows:

[H] n=0 and 3, m=0 and 3

[M, N] n=5, m=3

[E] m=1 (n: not available).

For details of I2C and IIC channel and the output buffer type relation, refer to section 44, I2C and section 45, IIC in the manual.

2. When using 1.8V I2C/IIC pins as 3.3 V tolerant, all the VPU33 power supply for the I2C/IIC of this LSI must keep the same power on/off sequence as the VCCQ of this LSI.

RZ/G1H

RZ/G1E

**Table 63.4.10 DC Characteristics (1.5-V I/O [DDR3])**

DDR3 channel 1 is available for H (VDDQ\_M1, M1xxx signals)

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement conditions	Remarks
Input high voltage (MDQ pin)	VIH	VREF + 0.1	—	—	V	VDDQ_M0 = VDDQ_M1 = 1.425 to 1.575 V	M0DQ, M0DQS, M1DQ, and M1DQS pins
Input low voltage (MDQ pin)	VIL	—	—	VREF - 0.1	V		
Input high voltage	VIH	0.7 × VDDQ_M0, VDDQ_M1	—	—	V	VDDQ_M0 = VDDQ_M1 = 1.425 to 1.575 V	M0BKPRST# and M1BKPRST# pins
Input low voltage	VIL	—	—	0.3 × VDDQ_M0, VDDQ_M1	V		
Differential input reference voltage	VREF	0.49 × VDDQ_M0, VDDQ_M1	0.50 × VDDQ_M0, VDDQ_M1	0.51 × VDDQ_M0, VDDQ_M1	V	VDDQ_M0 = VDDQ_M1 = 1.425 to 1.575 V	*1
DC differential input voltage	VIHD	0.2	—	—	V	M0DQS = M1DQS = H, VIN = VDDQ_M0, VDDQ_M1/2 VDD = 1.0 V <sub>typ</sub> , VDDQ_M0 = VDDQ_M1 = 1.425 to 1.575 V	M0DQS and M1DQS pins
DC differential input voltage	VILD	—	—	-0.2	V	M0DQS = M1DQS = L, VIN = VDDQ_M0, VDDQ_M1/2, VDD = 1.0 V <sub>typ</sub> , VDDQ_M0 = VDDQ_M1 = 1.425 to 1.575 V	
DC differential input voltage	VIN	0.35	—	-0.35	V	VIHD = 200 mV or VILD = -200 mV, VDD = 1.0 V <sub>typ</sub> , VDDQ_M0 = VDDQ_M1 = 1.425 to 1.575 V	
Input high voltage (AC)	VIH (AC)	VREF - 0.175	—	—	V	—	—
Input low voltage (AC)	VIL (AC)	—	—	VREF + 0.175	V	—	—



Item	Symbol	Min.	Typ.	Max.	Unit	Measurement conditions	Remarks
AC differential input cross point voltage	VIX (AC)	0.5 × VDDQ_M0, VDDQ_M1 - 0.15	—	0.5 × VDDQ_M0, VDDQ_M1 + 0.15	V	VDDQ_M0 = VDDQ_M1 = 1.425 to 1.575 V	M0DQS and M1DQS pins *2
AC differential output cross point voltage	VOX (AC)	VREF - 0.125	—	VREF + 0.125	V	—	M0CK, M0DQS, M1CK, and M1DQS pins (PU,PD not used, 5.5kohm used, 500ohm used)
High Hi-Z leak current	IOZH	—	—	4	μA	—	Other than M0ZQ and M1ZQ pins
Low Hi-Z leak current	IOZL	-4	—	—	μA	—	
High Hi-Z leak current	IOZH	—	—	5	μA	—	M0ZQ and M1ZQ pins
Low Hi-Z leak current	IOZL	-5	—	—	μA	—	
Pin capacitance	CL	—	—	15	pF	—	All pins*3
PLL power supply	*4	1.62	1.8	1.98	V	—	—

- Notes: 1. Peak to peak ac noise on VREF may not exceed ±2 % of VREF.  
 2. The VIX (AC) indicates the voltage at which differential input signals cross each other. The typical value of VIX (AC) is expected to be 0.5 × VDDQ\_M0, VDDQ\_M1.  
 3. Except power supply pins.  
 4. VDDQ\_M0APLL, VDDQ\_M1APLL, VDDQ\_M1MPLL, VDDQ\_M0DPLL0 to VDDQ\_M0DPLL3 pins.

RZ/G1H

RZ/G1E

**Table 63.4.11 DDR3 Interface ODT Characteristics**

DDR3 channel 1 is available for H (VDDQ\_M1 signal)

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement conditions	Remarks
Termination voltage	Vtt	VREF - 0.04	VREF	VREF + 0.04	V	VDD = 1.0 V <sub>typ</sub> , VDDQ_M0 = VDDQ_M1	—
ODT resistance (60 Ω)	RTT60	54.0	—	66.0	Ω	= 1.425 to 1.575 V	—
VM deviation	ΔVM	-5	—	+5	%		*

Note: VM is a voltage value measured with the ODT turned on without any load applied to this LSI chip. ΔVM is obtained by the following formula:  

$$\Delta VM = (2 \times VM / VDDQ\_M0, VDDQ\_M1-1) \times 100$$

RZ/G1M

RZ/G1N

**Table 63.4.12 DC Characteristics (1.35-V I/O [DDR3L])**

DDR3 channel 1 is available for M (VDDQ\_M1, M1xxx signals)

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement conditions	Remarks
Input high voltage (MDQ pin)	VIH	VREF + 0.09	—	—	V	VDDQ_M0 = VDDQ_M1 = 1.283 to 1.450 V	M0DQ, M0DQS, M1DQ, and M1DQS pins
Input low voltage (MDQ pin)	VIL	—	—	VREF - 0.09	V		
Input high voltage	VIH	0.7 × VDDQ_M0, VDDQ_M1	—	—	V	VDDQ_M0 = VDDQ_M1 = 1.283 to 1.450 V	M0BKPRST# and M1BKPRST# pins
Input low voltage	VIL	—	—	0.3 × VDDQ_M0, VDDQ_M1	V		
Differential input reference voltage	VREF	0.49 × VDDQ_M0, VDDQ_M1	0.50 × VDDQ_M0, VDDQ_M1	0.51 × VDDQ_M0, VDDQ_M1	V	VDDQ_M0 = VDDQ_M1 = 1.283 to 1.450 V	*1
DC differential input voltage	VIHD	0.18	—	—	V	M0DQS = M1DQS = H, VIN = VDDQ_M0, VDDQ_M1/2 VDD = 1.0 V <sub>typ</sub> , VDDQ_M0 = VDDQ_M1 = 1.283 to 1.450 V	M0DQS and M1DQS pins
DC differential input voltage	VILD	—	—	-0.18	V	M0DQS = M1DQS = L, VIN = VDDQ_M0, VDDQ_M1/2, VDD = 1.0 V <sub>typ</sub> , VDDQ_M0 = VDDQ_M1 = 1.283 to 1.450 V	
DC differential input voltage	VIN	0.32	—	-0.32	V	VIHD = 200 mV or VILD = -200 mV, VDD = 1.0 V <sub>typ</sub> , VDDQ_M0 = VDDQ_M1 = 1.283 to 1.450 V	
Input high voltage (AC)	VIH (AC)	VREF - 0.16	—	—	V	—	—
Input low voltage (AC)	VIL (AC)	—	—	VREF + 0.16	V	—	—

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement conditions	Remarks
AC differential input cross point voltage	VIX (AC)	0.5 × VDDQ_M0, VDDQ_M1 - 0.15	—	0.5 × VDDQ_M0, VDDQ_M1 + 0.15	V	VDDQ_M0 = VDDQ_M1 = 1.283 to 1.450 V	M0DQS and M1DQS pins *2
AC differential output cross point voltage	VOX (AC)	VREF - 0.125	—	VREF + 0.125	V	VDDQ_M0 = VDDQ_M1 = 1.450 V	M0CK, M0DQS, M1CK, and M1DQS pins (PU,PD not used, 5.5kohm used, 500ohm used)
High Hi-Z leak current	IOZH	—	—	4	μA	VDDQ_M0 = VDDQ_M1 = 1.450 V	Other than M0ZQ and M1ZQ pins
Low Hi-Z leak current	IOZL	-4	—	—	μA	VDDQ_M0 = VDDQ_M1 = 1.450 V	
High Hi-Z leak current	IOZH	—	—	5	μA	VDDQ_M0 = VDDQ_M1 = 1.450 V	M0ZQ and M1ZQ pins
Low Hi-Z leak current	IOZL	-5	—	—	μA	VDDQ_M0 = VDDQ_M1 = 1.450 V	
Pin capacitance	CL	—	—	15	pF	—	All pins*3
PLL power supply	*4	1.62	1.8	1.98	V	—	—

- Notes: 1. Peak to peak ac noise on VREF may not exceed ±2 % of VREF.  
2. The VIX (AC) indicates the voltage at which differential input signals cross each other. The typical value of VIX (AC) is expected to be 0.5 × VDDQ\_M0, VDDQ\_M1.  
3. Except power supply pins.  
4. VDDQ\_M0APLL, VDDQ\_M1APLL, VDDQ\_M1MPLL, VDDQ\_M0DPLL0 to VDDQ\_M0DPLL3 pins.

RZ/G1M

RZ/G1N

Table 63.4.13 DDR3L Interface ODT Characteristics

DDR3 channel 1 is available for M (VDDQ\_M1 signal)

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement conditions	Remarks
Termination voltage	Vtt	VREF - 0.04	VREF	VREF + 0.04	V	VDD = 1.0 Vtyp, VDDQ_M0 = VDDQ_M1	—
ODT resistance (60 Ω)	RTT60	54.0	—	66.0	Ω	= 1.283 to 1.450 V	—
VM deviation	ΔVM	-5	—	+5	%		*

Note: VM is a voltage value measured with the ODT turned on without any load applied to this LSI chip. ΔVM is obtained by the following formula:  

$$\Delta VM = (2 \times VM / VDDQ\_M0, VDDQ\_M1-1) \times 100$$

<b>RZ/G1H</b>	<b>RZ/G1N</b>
<b>RZ/G1M</b>	<b>RZ/G1E</b>

**Table 63.4.14 USB High-Speed Transceiver Characteristics**

Item		Symbol	Min.	Typ.	Max.	Unit	Remarks
Input	Common mode voltage range	$V_{HSCM}$	-50	—	500	mV	—
	Differential input sensitivity	$V_{diff}$	150	—	—	mV	
	Squelch threshold	$V_{HSSQ}$	100	—	150	mV	
	Disconnect level	$V_{HSDSC}$	525	—	625	mV	
Output	Idle state	$V_{HSOI}$	-10	—	10	mV	RL = 45 Ω to GND
	High level voltage	$V_{HSOH}$	360	—	440	mV	
	Low level voltage	$V_{HSOL}$	-10	—	10	mV	
	Chirp J state	$V_{CHIRPJ}$	700	—	1100	mV	
	Chirp K state	$V_{CHIRPK}$	-900	—	-500	mV	

<b>RZ/G1H</b>	<b>RZ/G1N</b>
<b>RZ/G1M</b>	<b>RZ/G1E</b>

**Table 63.4.15 USB Low-/full-speed Transceiver Characteristics**

Item		Symbol	Min.	Typ.	Max.	Unit	Remarks
Input	High voltage (driven)	$V_{IH}$	2.0	—	—	V	—
	Low voltage	$V_{IL}$	—	—	0.8	V	
	Differential Input Sensitivity	$V_{DI}$	0.2	—	—	V	DP-DM
	Differential Common Mode Range	$V_{CM}$	0.8	—	2.5	V	—
Output	High voltage (driven)	$V_{OH}$	2.8	—	VCCQ	V	
	Low voltage	$V_{OL}$	—	—	0.3	V	
	Output Signal Crossover Voltage	$V_{CRS}$	1.3	—	2.0	V	

<b>RZ/G1H</b>	<b>RZ/G1N</b>
<b>RZ/G1M</b>	<b>RZ/G1E</b>

**Table 63.4.16 USB High-Speed Output Driver Impedance**

Item		Symbol	Min.	Typ.	Max.	Unit	Remarks
Driver output impedance		$R_O$	40.5	45	49.5	Ω	—
DP pull-up resistor (on-chip)	Idle state	$R_{PU}$	0.9	—	1.575	kΩ	
	Receiving state		1.425	—	3.09	kΩ	
Pull-down resistor (on-chip)		$R_{PD}$	14.25	—	24.80	kΩ	
External reference resistor		$R_{REF}$	1.782	1.8	1.818	kΩ	±1 %

<b>RZ/G1H</b>	<b>RZ/G1N</b>
<b>RZ/G1M</b>	<b>RZ/G1E</b>

**Table 63.4.17 DC Characteristics of VBUS pin**

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
VBUS input voltage	VIH	2.0	—	VCCQ + 0.3	V	—
	VIL	-0.3	—	0.8	V	

### 63.5 Clock and Reset Timings

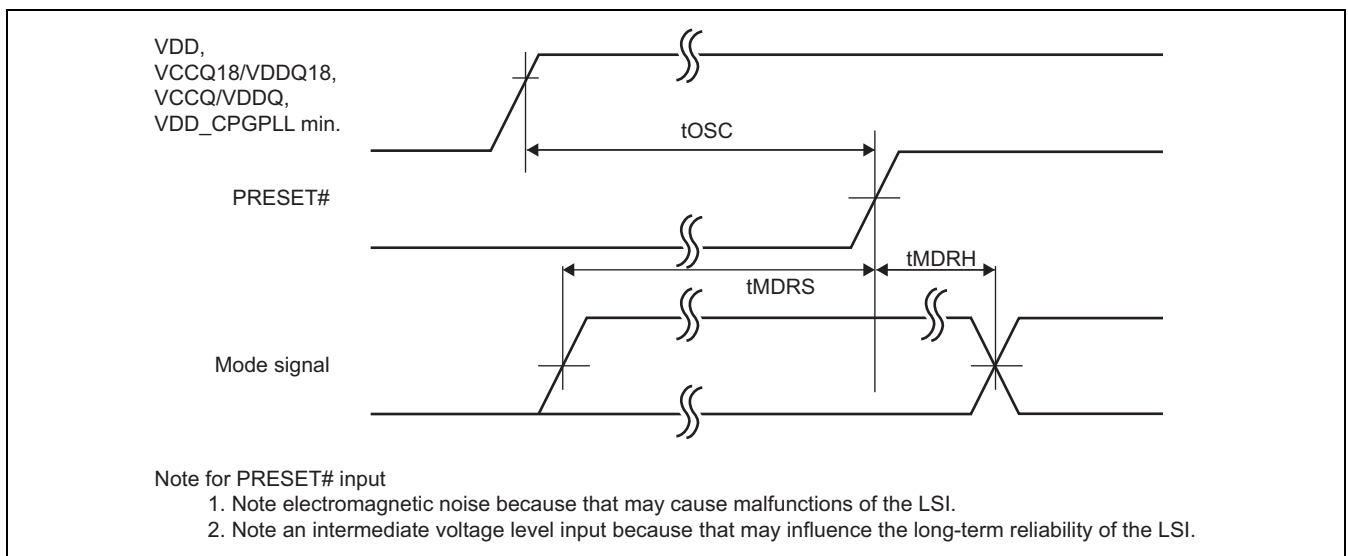
<b>RZ/G1H</b>	<b>RZ/G1N</b>
<b>RZ/G1M</b>	<b>RZ/G1E</b>

**Table 63.5.1 Clock and Reset Timings**

Conditions: VCCQ/VDDQ = 3.3 V ± 0.3 V, VCCQ18/VDDQ18 = 1.8 V ± 0.1 V, GND = VSS = 0 V,  
Tc = -40 to +105 °C

Pin	Item	Symbol	Min.	Max.	Unit	Figures
PRESET#, EXTAL	Power-on oscillation settling time	tOSC	20	—	ms	Figure 63.5.1
Mode signal*	MD reset setup time	tMDRS	20	—	ms	
Mode signal*	MD reset hold time	tMDRH	3	—	ns	

Note: \* MDn (n= 0, 1, 2, ...) and MDT [1:0]. For details of mode signals, refer to section 3.3, Mode Pin Settings.



**Figure 63.5.1 Reset when Turning on Power Supply**

## 63.6 LBSC

### 63.6.1 Normal Read/Write, Burst ROM Read and DMA Access

**Table 63.6.1 Normal Read/Write Access Timing (RZ/G1H, M, N and E)**

Conditions: VCCQ = 3.3 ± 0.3 V, GND = VSSQ = 0 V, Tc = -40 to +105 °C,  
CL = 40 pF

<b>RZ/G1H</b>	<b>RZ/G1N</b>
<b>RZ/G1M</b>	<b>RZ/G1E</b>

Item	Symbol	Min.	Typ.	Max.	Unit	Figures
Address output delay time	tDA	0.0	—	6.0	ns	Figure 63.6.1
CS# output delay time	tDCS	0.0	—	6.0	ns	
BS# output delay time	tDBS	0.0	—	6.0	ns	
RD# output delay time	tDRD	0.0	—	6.0	ns	
RD/WR# output delay time	tDRW	0.0	—	6.0	ns	
Read data setup time	tSD	11.0	—	—	ns	
Read data hold time	tHD	0.0	—	—	ns	
WE# output delay time	tDWE	0.0	—	6.0	ns	
Write data output delay time	tDD	0.0	—	6.0	ns	
External wait signal setup time	tSEW	11.0	—	—	ns	
External wait signal hold time	tHEW	0.0	—	—	ns	
ATADIR# output delay time	tDATAD	0.0	—	6.0	ns	
ATAG# output delay time	tDATAG	0.0	—	6.0	ns	
ATARD# (DIOR#) output delay time	tDDIOR	0.0	—	6.0	ns	
ATAWR# (DIOW#) output delay time	tDDIOW	0.0	—	6.0	ns	

**Table 63.6.2 Burst ROM Read Access Timing**

<b>RZ/G1H</b>	<b>RZ/G1N</b>
<b>RZ/G1M</b>	<b>RZ/G1E</b>

Conditions: VCCQ = 3.3 ± 0.3 V [H, M, N and E],  
 GND = VSSQ = 0 V, Tc = -40 to +105 °C, CL = 40 pF

Item	Symbol	Min.	Typ.	Max.	Unit	Figures
Address output delay time	tDABST	0.0	—	6.0	ns	Figure 63.6.2
CS# output delay time	tDCSBST	0.0	—	6.0	ns	
RD# output delay time	tDRDBST	0.0	—	6.0	ns	
Read data setup time	tSDBST	11.0	—	—	ns	
Read data hold time	tHDBST	0.0	—	—	ns	

**Table 63.6.3 DMA Signal Access Timing**

<b>RZ/G1H</b>	<b>RZ/G1N</b>
<b>RZ/G1M</b>	<b>RZ/G1E</b>

Conditions: VCCQ = 3.3 ± 0.3 V [H, M, N and E],  
 GND = VSSQ = 0 V, Tc = -40 to +105 °C, CL = 40 pF

Item	Symbol	Min.	Typ.	Max.	Unit	Figures
DMA transfer request signal setup time	tSDRQ	11.0	—	—	ns	Figure 63.6.3
DMA transfer request signal hold time	tHDRQ	0.0	—	—	ns	
Delay time for DMA transfer end acknowledge signal output	tDDAK	0.0	—	6.0	ns	
Delay time for DMA acceptance signal output	tDDRK	0.0	—	6.0	ns	



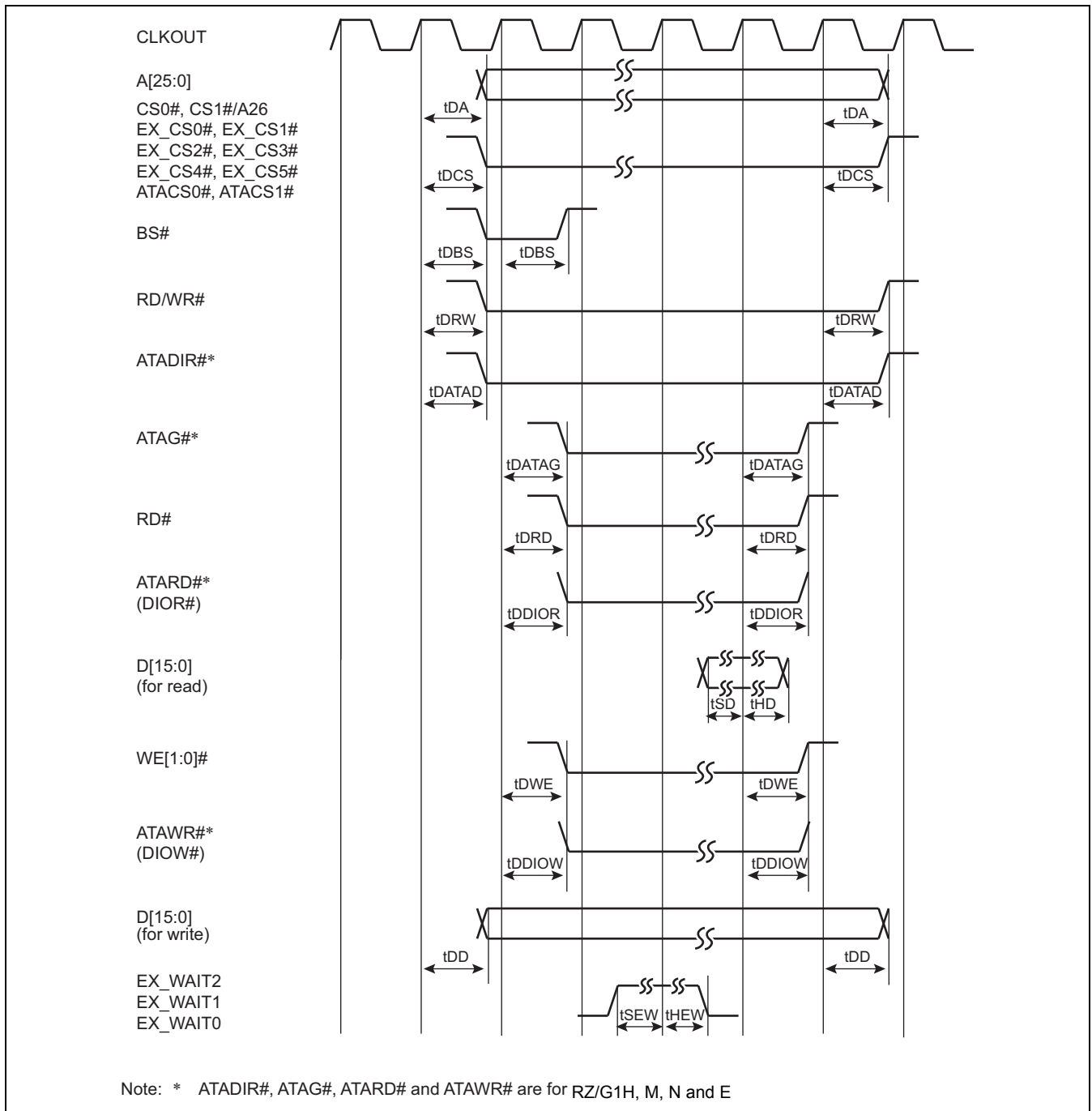


Figure 63.6.1 Normal Read/Write Access Timing

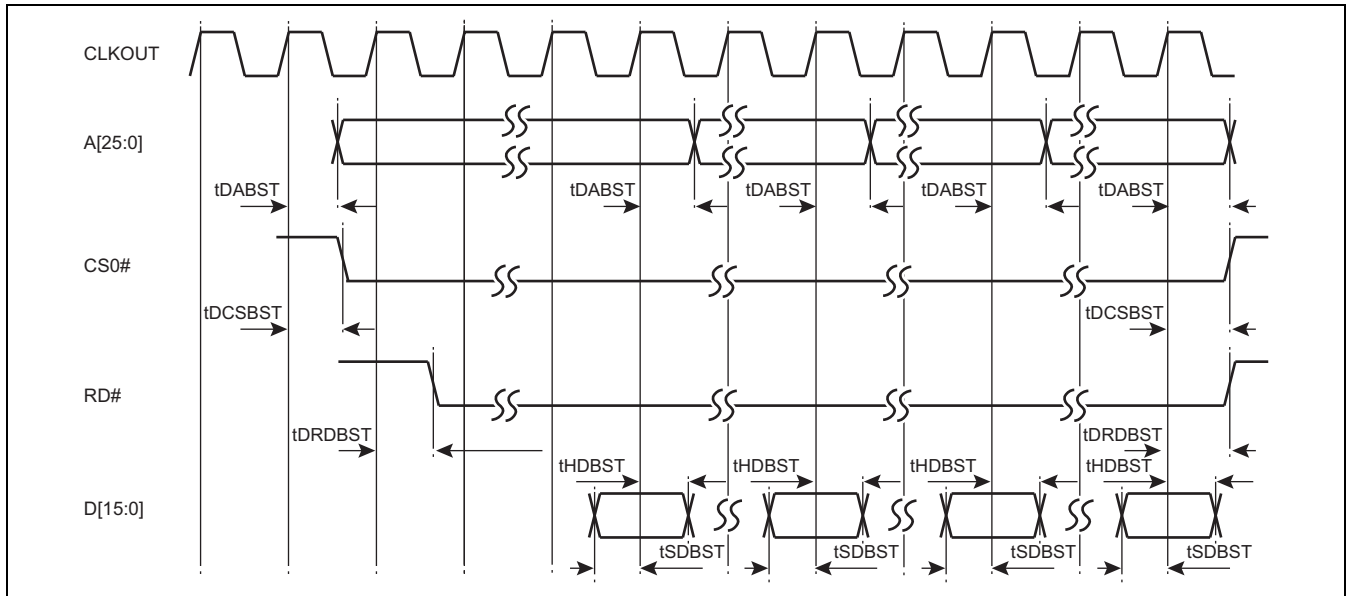


Figure 63.6.2 Burst ROM Read Access Timing

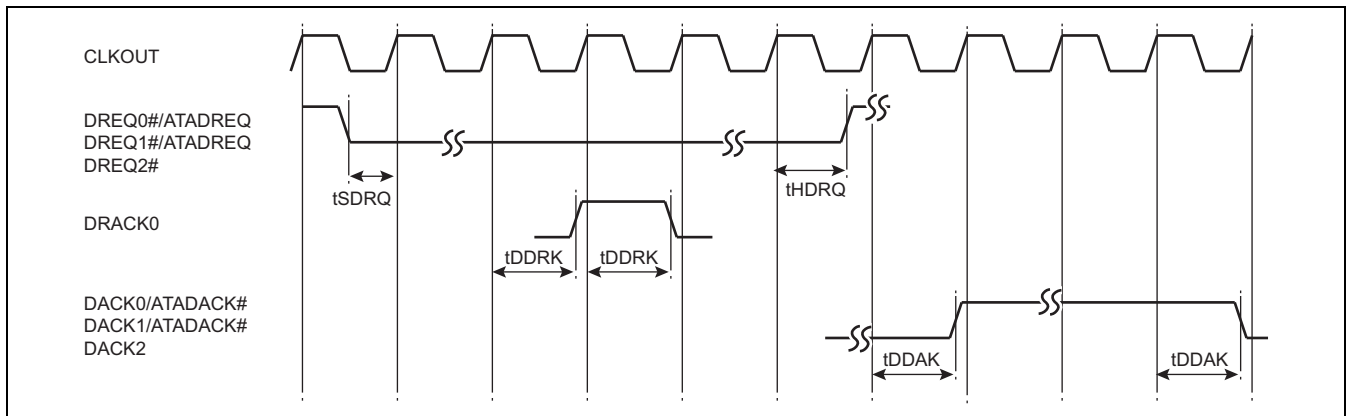


Figure 63.6.3 DMA Signal Access Timing

## 63.6.2 Ultra ATA Transfer for ATA Interface

<b>RZ/G1H</b>	<b>RZ/G1N</b>
<b>RZ/G1M</b>	<b>RZ/G1E</b>

**Table 63.6.4 Timing of Ultra ATA Transfer for ATA Interface  
(RZ/G1H, M, N and E)**

Conditions: VCCQ = 3.3 ± 0.3 V, GND = VSSQ = 0 V, Tc = -40 to +105 °C, CL = 40 pF

Item	Symbol	MODE0		MODE1		MODE2		MODE3		MODE4		Unit	Figures
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Typical average two-cycle time	t2CYCTYP	240	—	160	—	120	—	90	—	60	—	ns	Figures 63.6.4 to 63.6.13
Cycle time	tCYC	112	—	73	—	54	—	39	—	25	—	ns	
Minimum two-cycle time	t2CYC	230	—	153	—	115	—	86	—	57	—	ns	
Data setup time (reception)	tDS	15	—	10	—	7	—	7	—	5	—	ns	
Data hold time (reception)	tDH	5	—	5	—	5	—	5	—	5	—	ns	
Data setup time (transmission)	tDVS	70	—	48	—	31	—	20	—	6.7	—	ns	
Data hold time (transmission)	tDVH	6.2	—	6.2	—	6.2	—	6.2	—	6.2	—	ns	
CRC data setup time (transmission)	tCVS	70	—	48	—	31	—	20	—	6.7	—	ns	
CRC data hold time (transmission)	tCVH	6.2	—	6.2	—	6.2	—	6.2	—	6.2	—	ns	
First DSTROBE time (transmission)	tZFS	0	—	0	—	0	—	0	—	0	—	ns	
Data enabled to the first DSTROBE edge time (transmission)	tDZFS	70	—	48	—	31	—	20	—	6.7	—	ns	
First STROBE time	tFS	—	230	—	200	—	170	—	130	—	120	ns	
Limited interlock time	tLI	0	150	0	150	0	150	0	100	0	100	ns	
Minimum interlock time	tMLI	20	—	20	—	20	—	20	—	20	—	ns	
Unlimited interlock time	tUI	0	—	0	—	0	—	0	—	0	—	ns	
Output release time	tAZ	—	10	—	10	—	10	—	10	—	10	ns	
Output delay time	tZAH	20	—	20	—	20	—	20	—	20	—	ns	
Minimum output assert/negate time (from release timing)	tZAD	0	—	0	—	0	—	0	—	0	—	ns	
Envelope time	tENV	20	70	20	70	20	70	20	55	20	55	ns	
Final STROBE time	tRFS	—	75	—	70	—	60	—	60	—	60	ns	
STOP assertion or DMARQ negation time	tRP	160	—	125	—	100	—	100	—	100	—	ns	
IORDY release time	tIORDYZ	—	20	—	20	—	20	—	20	—	20	ns	
STROBE driven time	tZIORDY	0	—	0	—	0	—	0	—	0	—	ns	
DMACK setup/hold time	tACK	20	—	20	—	20	—	20	—	20	—	ns	
STROBE STOP time	tSS	50	—	50	—	50	—	50	—	50	—	ns	

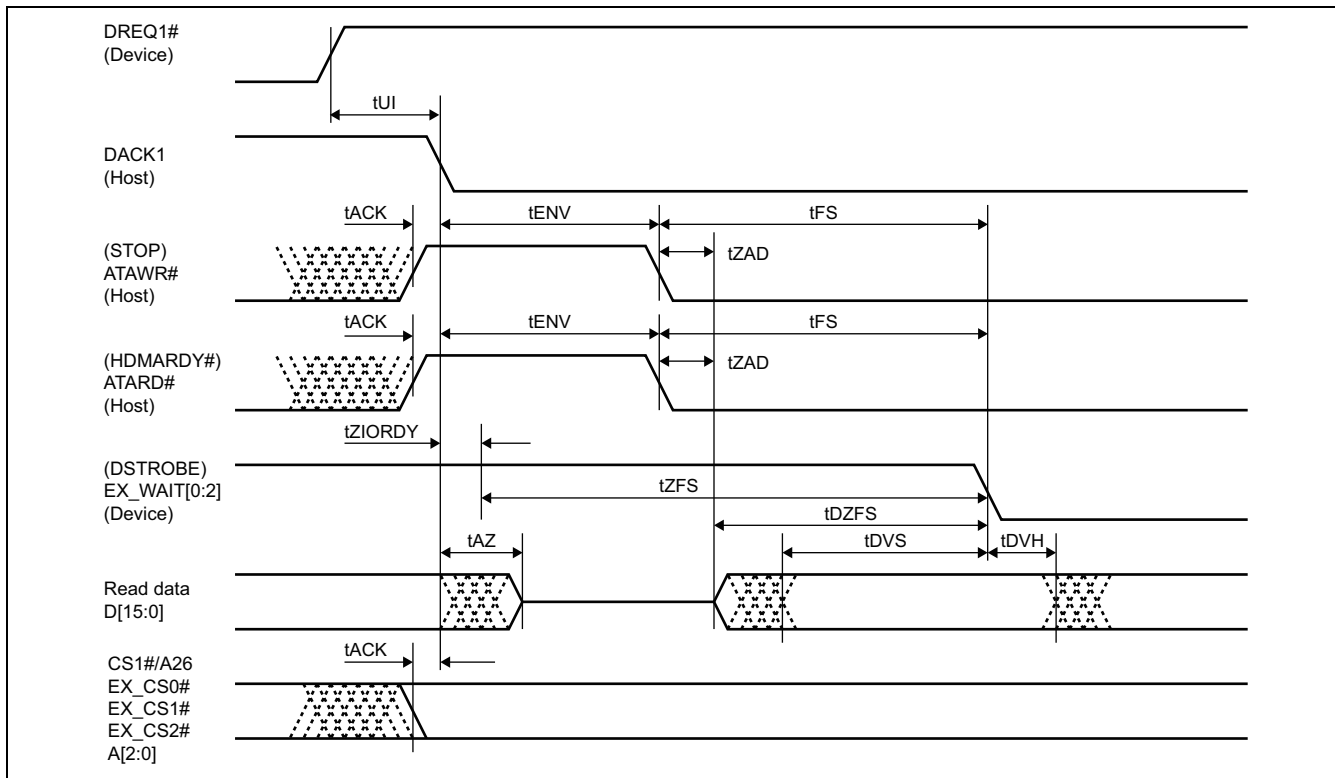


Figure 63.6.4 Initializing Ultra DMA Transfer (for Read) [H, M, N and E]

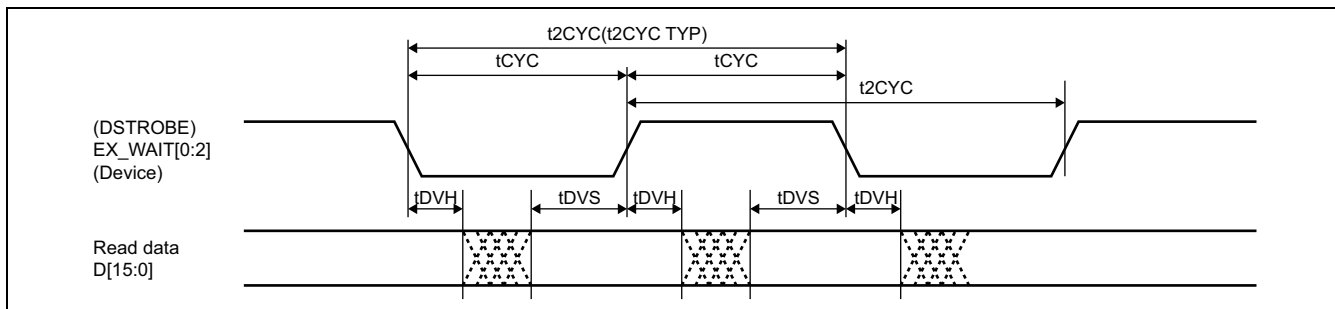


Figure 63.6.5 Ultra DMA Transfer (for Read) [H, M, N and E]

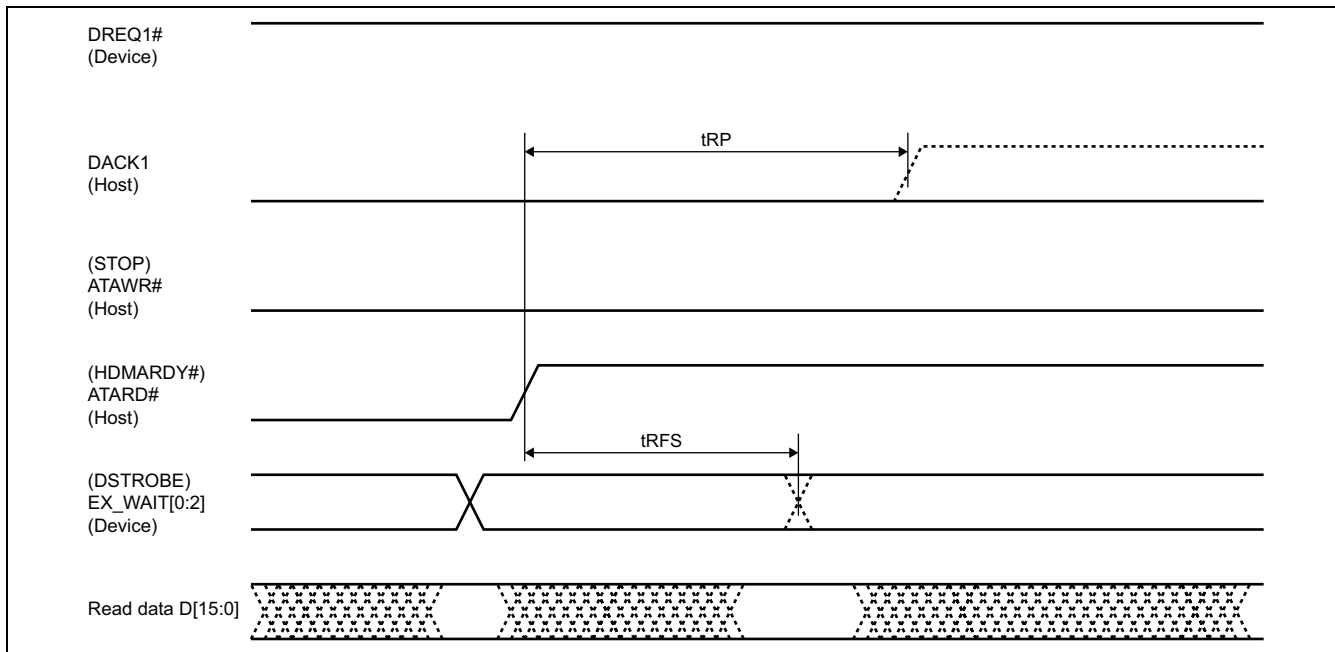


Figure 63.6.6 Host Pausing Ultra DMA (for Read) [H, M, N and E]

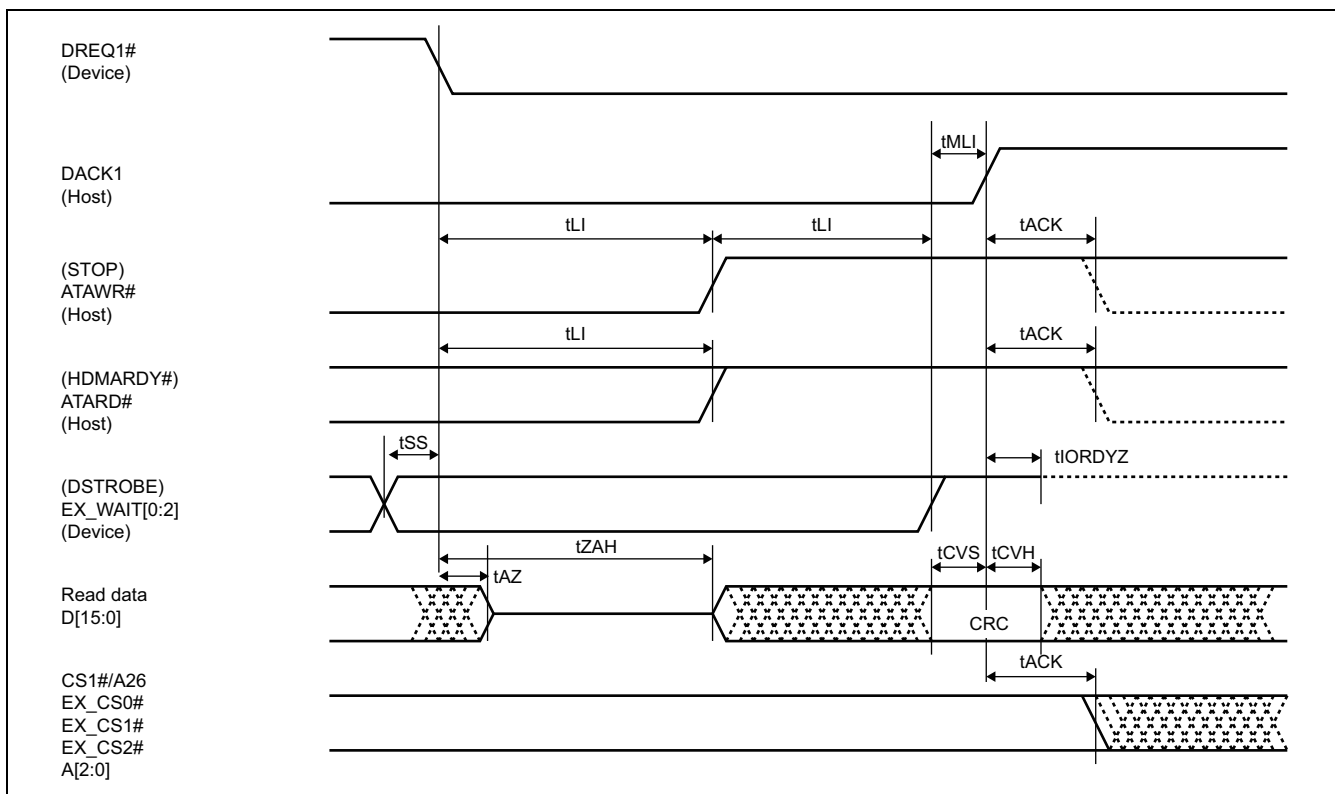


Figure 63.6.7 Device Terminating Ultra DMA Transfer (for Read) [H, M, N and E]

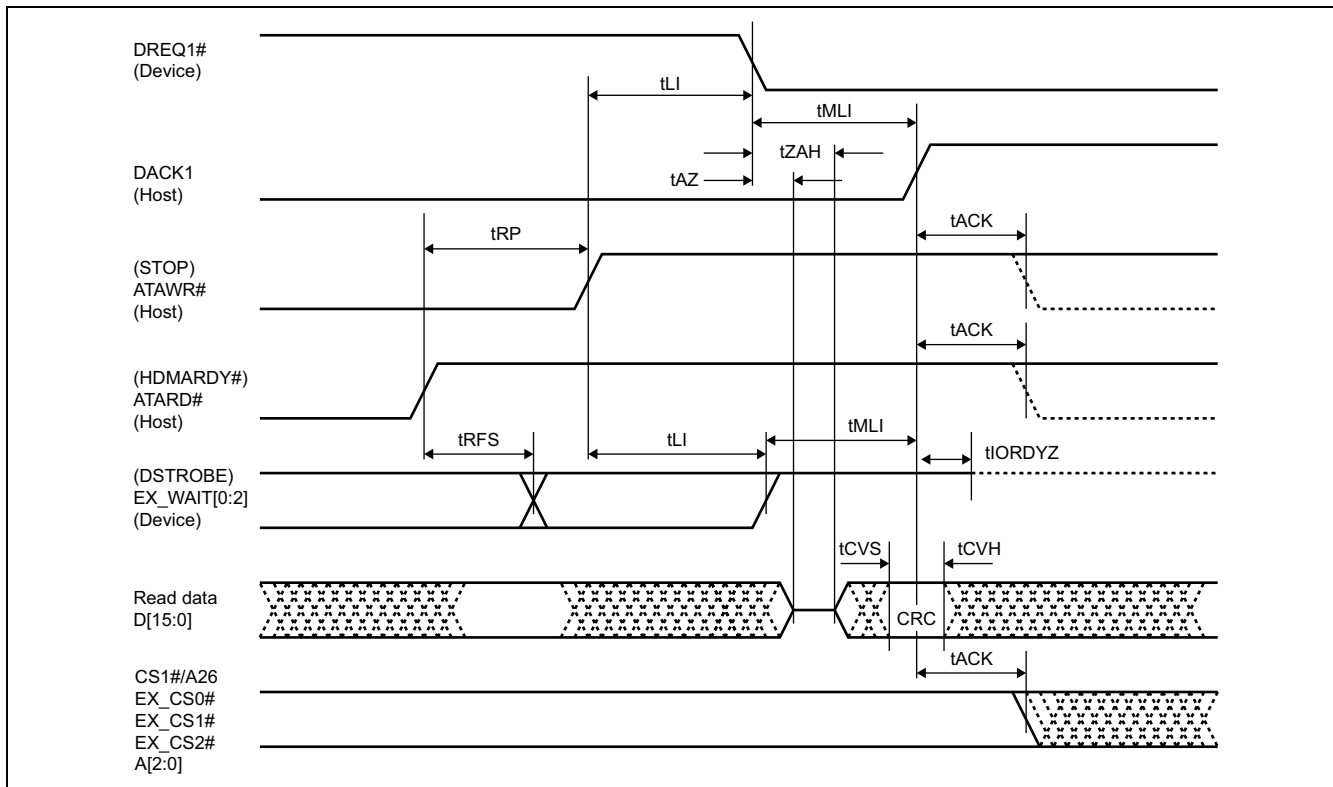


Figure 63.6.8 Host Terminating Ultra DMA Transfer (for Read) [H, M, N and E]

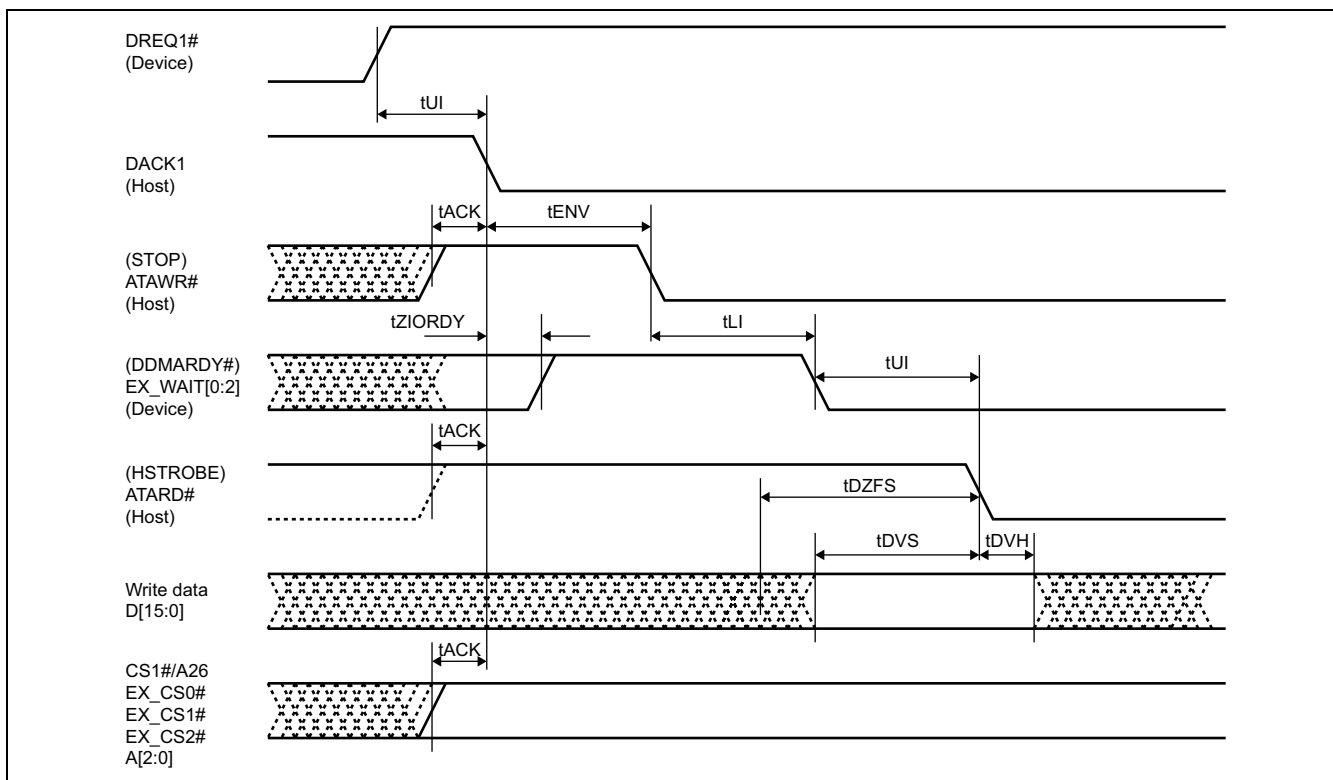


Figure 63.6.9 Initiating Ultra DMA Transfer (for Write) [H, M, N and E]

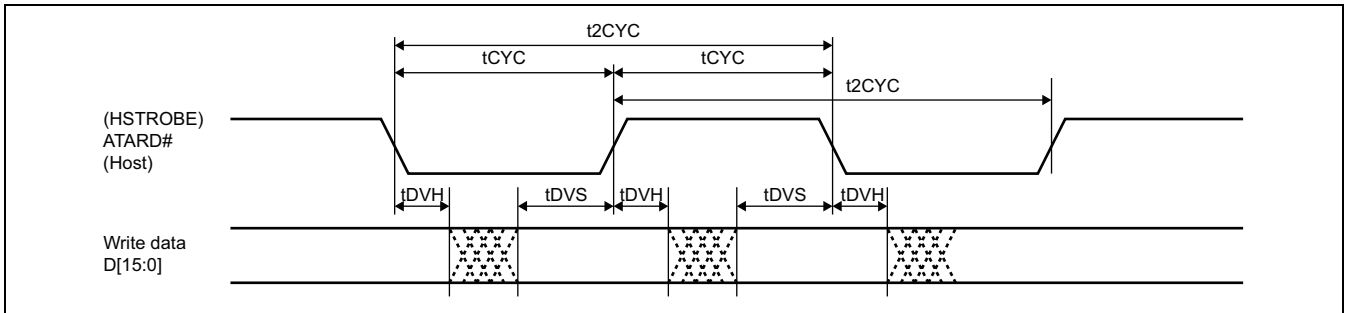


Figure 63.6.10 Ultra DMA Transfer (for Write) [H, M, N and E]

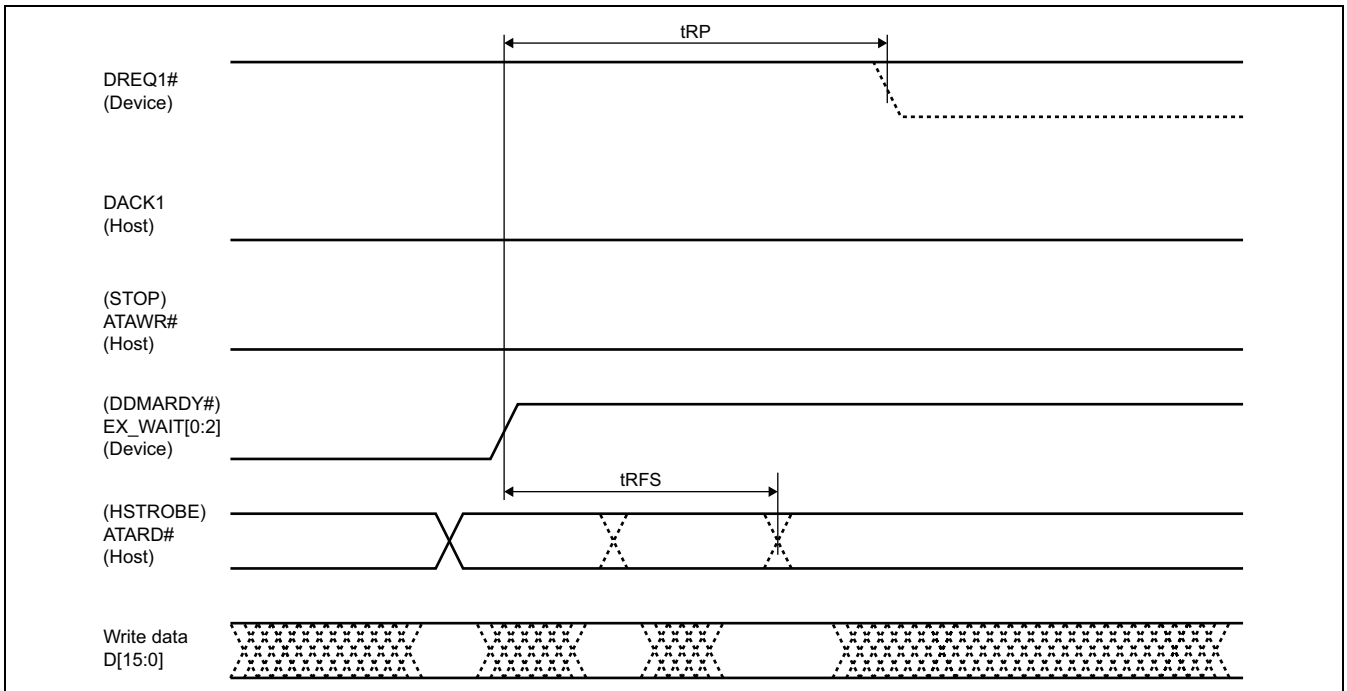


Figure 63.6.11 Device Pausing Ultra DMA (for Write) [H, M, N and E]

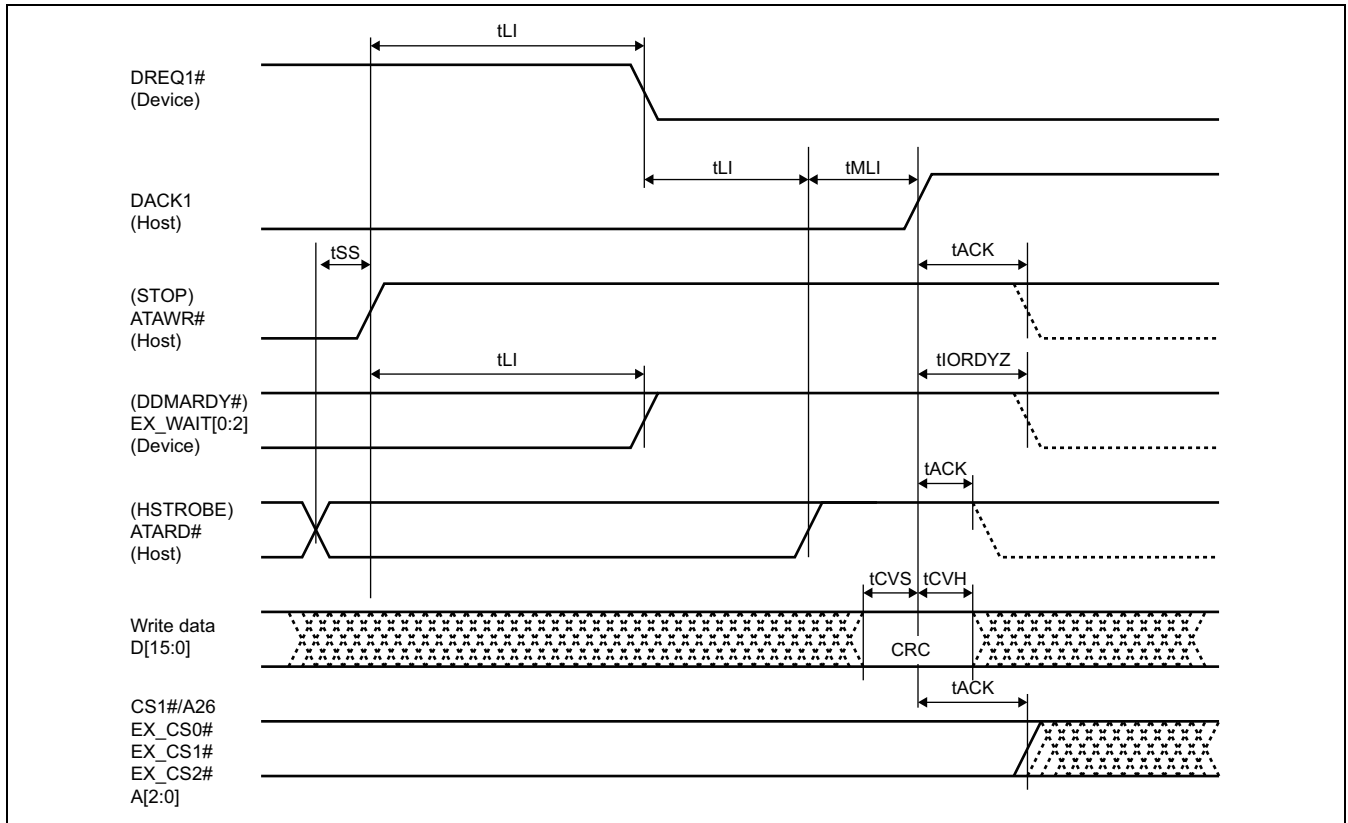


Figure 63.6.12 Host Terminating Ultra DMA Transfer (for Write) [H, M, N and E]

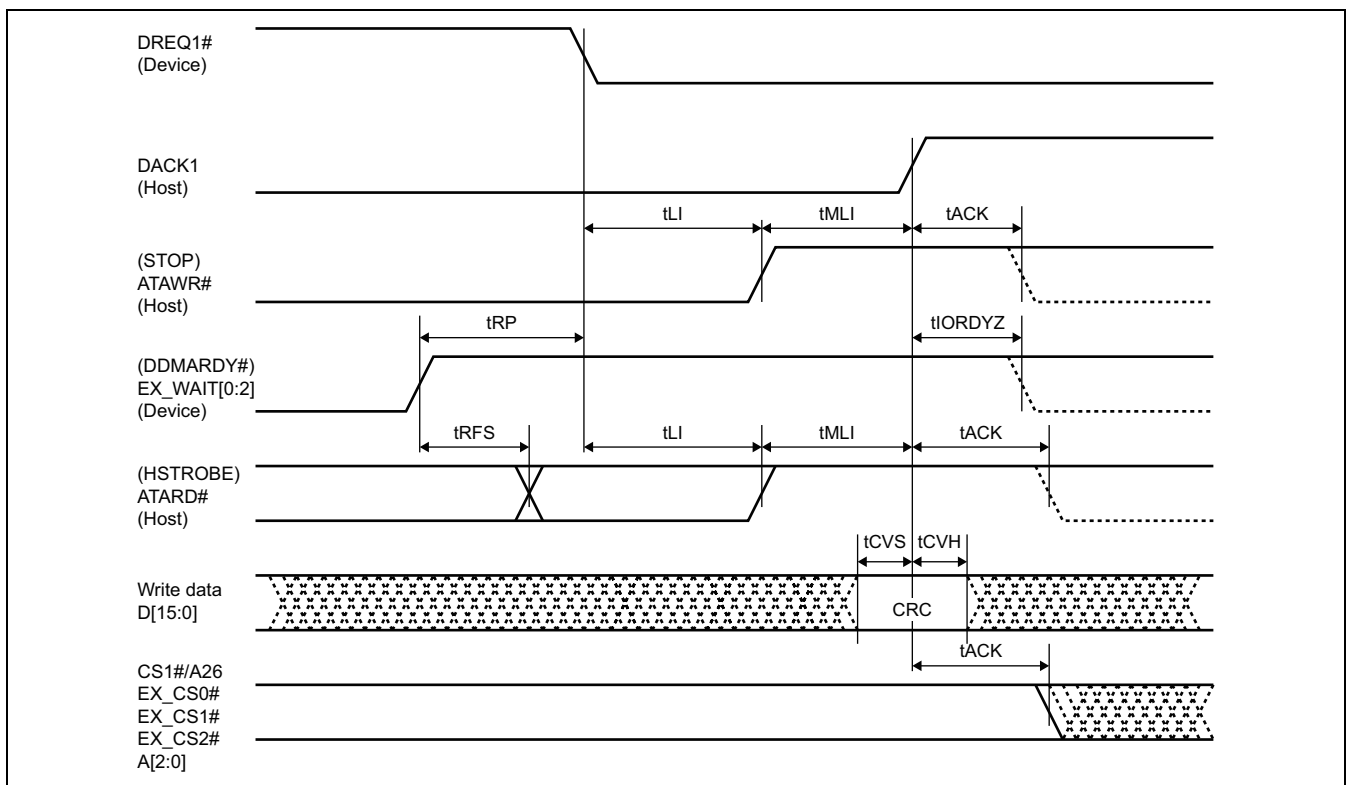


Figure 63.6.13 Device Terminating Ultra DMA Transfer (for Write) [H, M, N and E]



## 63.7 DBSC3 Access Timing

RZ/G1H	RZ/G1N
RZ/G1M	RZ/G1E

Table 63.7.1 DBSC3 Access Timing (DDR3, DDR3L)

Conditions for DDR3\* : VDDQ\_M0 = VDDQ\_M1 = 1.5 V ± 0.075 V, GND = VSS = 0 V, Tc = -40 to +105°C

Conditions for DDR3L\*: VDDQ\_M0 = VDDQ\_M1 = 1.35 V + 0.100/-0.067 V, GND = VSS = 0 V, Tc = -40 to +105°C

Item		Symbol	Min.	Max.	Unit	Figure
MCK average clock period	DDR3-1600*	tCK(avg)	1.25	1.50	ns	Figure 63.7.2
	DDR3-1333		1.50	1.80	ns	
MCK absolute high pulse width		tCH(abs)	0.44	—	tCK(avg)	Figure 63.7.2
MCK absolute low pulse width		tCL(abs)	0.44	—	tCK(avg)	Figure 63.7.2
Command and Address output setup time to MCK, MCK#	DDR3-1600*	tOS(1T)	350	—	ps	Figure 63.7.3
	DDR3-1333		390	—	ps	
	DDR3-1600*	tOS(2T)	1470	—	ps	
	DDR3-1333		1630	—	ps	
Command and Address output hold time from MCK, MCK#	DDR3-1600*	tOH(1T)	350	—	ps	Figure 63.7.3
	DDR3-1333		390	—	ps	
	DDR3-1600*	tOH(2T)	350	—	ps	
	DDR3-1333		390	—	ps	
Control and Address pulse width for each output	DDR3-1600*	tOPW(1T)	700	—	ps	Figure 63.7.3
	DDR3-1333		780	—	ps	
	DDR3-1600*	tOPW(2T)	1820	—	ps	
	DDR3-1333		2020	—	ps	
Write Latency		WL	CWL	—	tCK(avg)	Figure 63.7.4
MDQS, MDQS# rising edge to MCK, MCK# rising edge (write)		tWDQSS	-0.20	0.20	tCK(avg)	Figure 63.7.4
MDQS, MDQS# falling edge setup time to MCK, MCK# rising edge (write)		tWDSS	0.25	—	tCK(avg)	Figure 63.7.4
MDQS, MDQS# falling edge hold time from MCK, MCK# rising edge (write)		tWDSH	0.25	—	tCK(avg)	Figure 63.7.4
MDQS, MDQS# differential high pulse width (write)		tWDQSH	0.45	0.55	tCK(avg)	Figure 63.7.5
MDQS, MDQS# differential low pulse width (write)		tWDQSL	0.45	0.55	tCK(avg)	Figure 63.7.5
MDQS, MDQS# differential WRITE Preamble (write)		tWPRE	0.9	—	tCK(avg)	Figure 63.7.5
MDQS, MDQS# differential WRITE Postamble (write)		tWPST	0.3	—	tCK(avg)	Figure 63.7.5
MDQ and MDM output setup time to MDQS, MDQS# (write)	DDR3-1600*	tWDS	200	—	ps	Figure 63.7.6
	DDR3-1333		220	—	ps	
MDQ and MDM output hold time from DQS, DQS# (write)	DDR3-1600*	tWDH	200	—	ps	Figure 63.7.6
	DDR3-1333		220	—	ps	

Item		Symbol	Min.	Max.	Unit	Figure
MDQ and MDM output pulse width for each output (write)	DDR3-1600*	tWDIPW	400	—	ps	Figure 63.7.6
	DDR3-1333		440	—	ps	
Read latency		RL	CL	—	tCK(avg)	Figure 63.7.7
MDQS, MDQS# rising edge input access time from rising MCK, MCK# (read)	DDR3-1600*	tRDQSCK	-315	2000	ps	Figure 63.7.7
	DDR3-1333		-375	2000	ps	
MDQS, MDQS# differential input high pulse width (read)		tRQSH	0.4	—	tCK(avg)	Figure 63.7.8
MDQS, MDQS# differential input low pulse width (read)		tRQSL	0.4	—	tCK(avg)	Figure 63.7.8
MDQS, MDQS# differential READ Preamble (read)		tRPRE	0.9	—	tCK(avg)	Figure 63.7.8
MDQS, MDQS# differential READ Postamble (read)		tRPST	0.3	—	tCK(avg)	Figure 63.7.8
MDQS, MDQS# to DQ skew, per group, per access (read)	DDR3-1600*	tRDQSQ	—	150	ps	Figure 63.7.9
	DDR3-1333		—	175	ps	
MDQ input hold time from MDQS, MDQS# (read)		tRQH	0.35	—	tCK(avg)	Figure 63.7.9

Note: The signal timing is based on the following electric potential:  
 For MCK output, MDQS input/output: Differential input/output cross point voltage  
 For MDQ input: MVREF  
 For outputs other than MCK or MDQS:  $0.5 \times VDDQ\_M0, VDDQ\_M1$

\* RZ/G1M and N cannot be used for DDR3, RZ/G1H and E cannot be used for DDR3L, and RZ/G1E cannot be used for DDR3-1600.

- Reference Load and VTT Termination of AC Timing  
 Reference Load for AC Timing

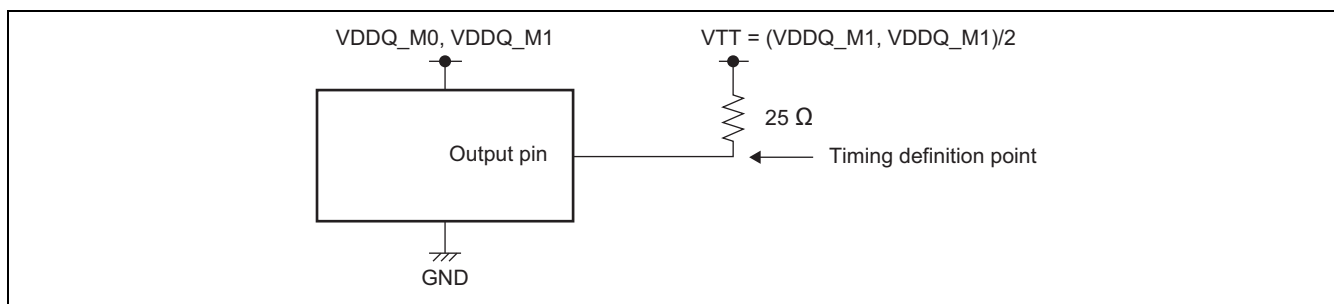


Figure 63.7.1 Reference Load for AC Timing

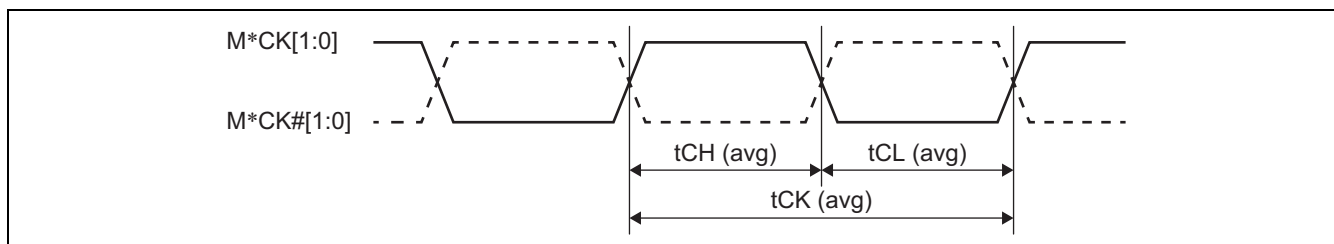


Figure 63.7.2 MCK Clock Output

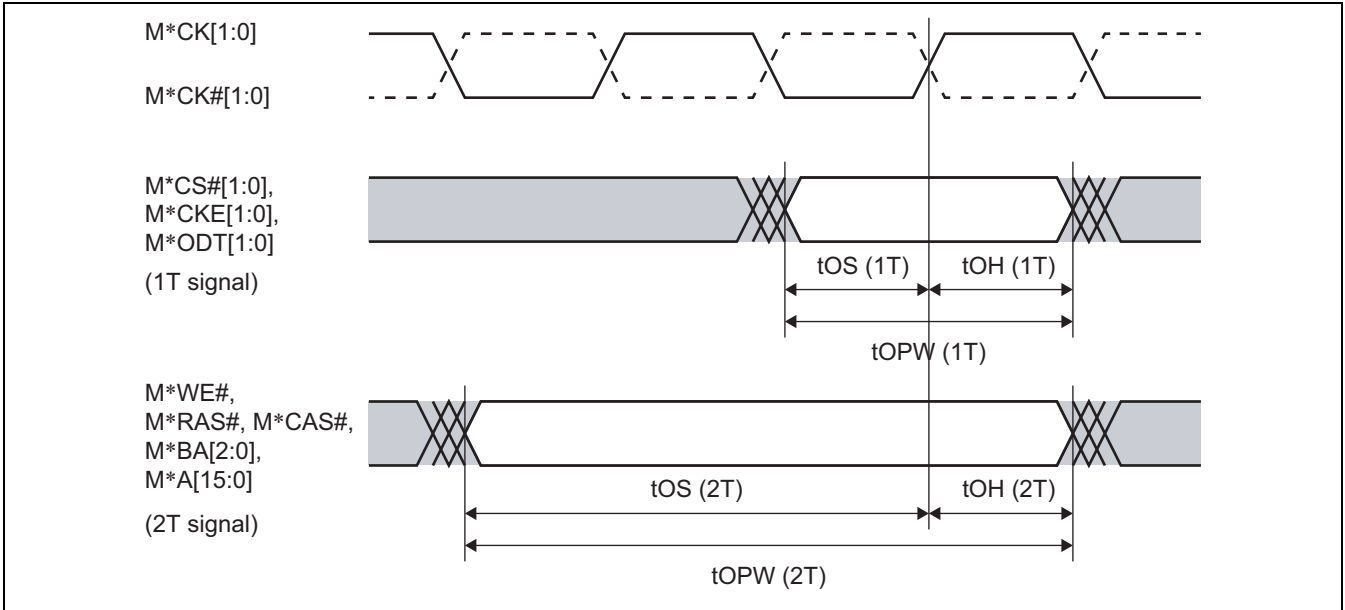


Figure 63.7.3 Address and Command Output Timing relative to MCK Output

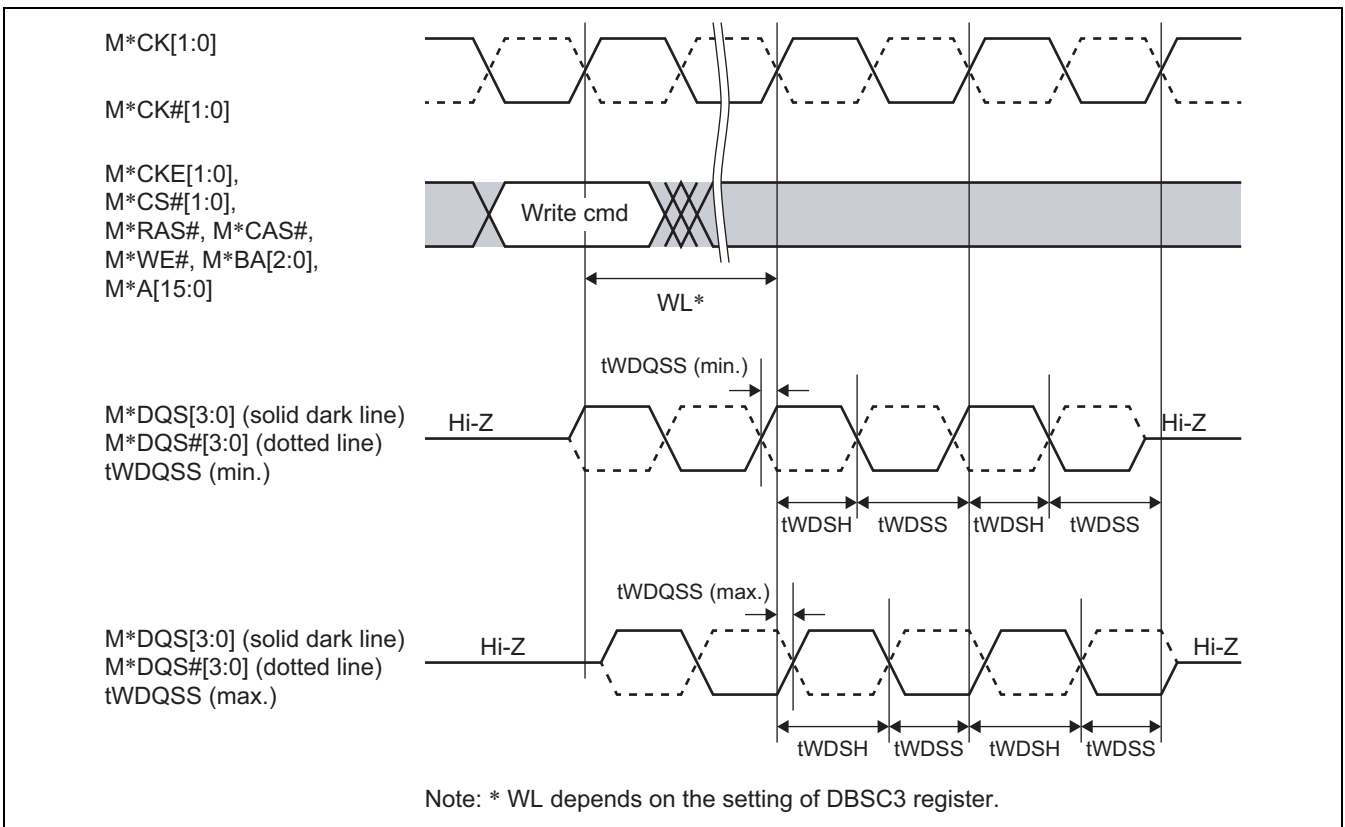


Figure 63.7.4 MDQS Output Timing relative to MCK Output (write)

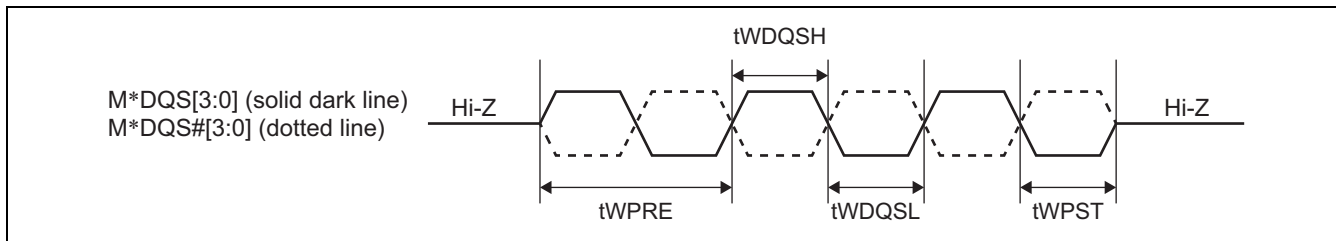


Figure 63.7.5 MDQS Output Timing (write)

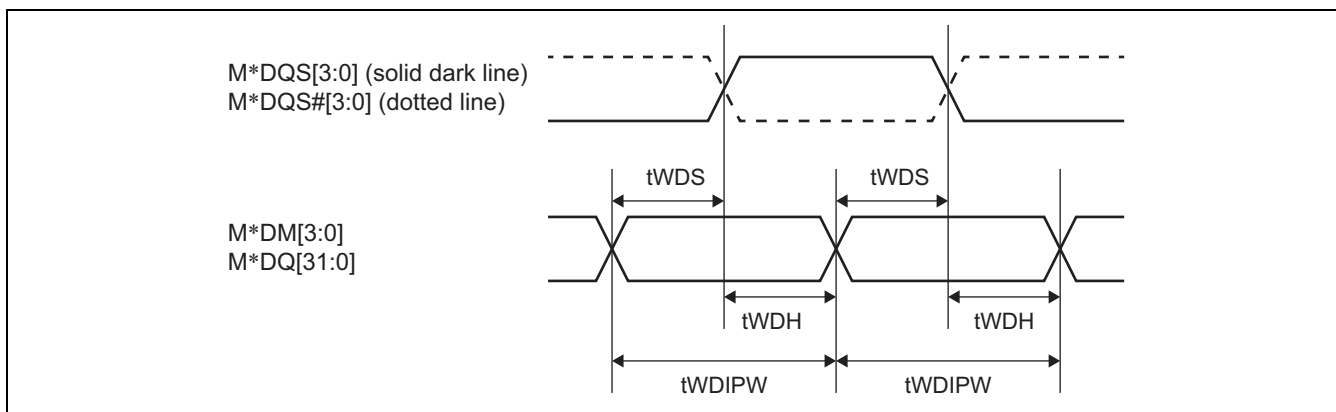


Figure 63.7.6 MDQ/MDM Output Timing relative to MDQ (write)

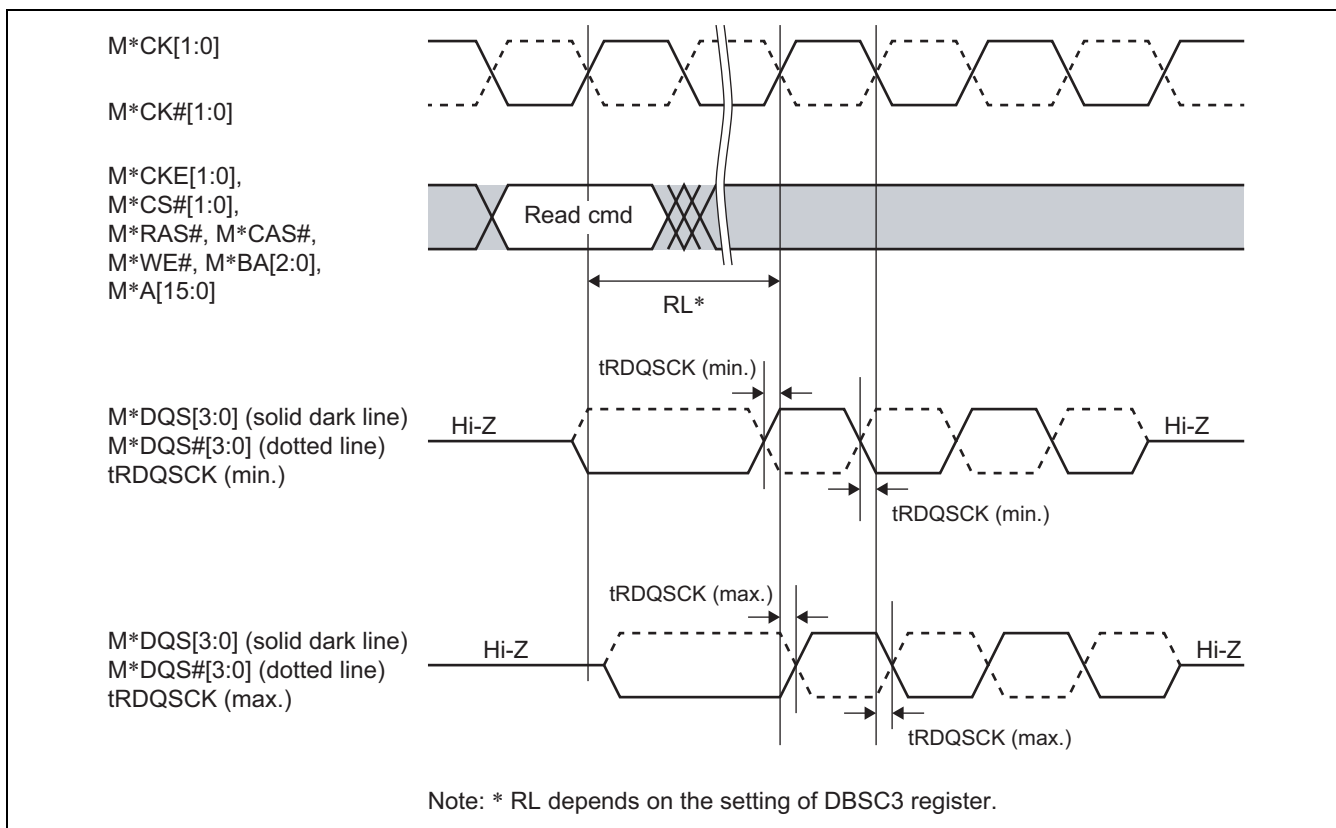


Figure 63.7.7 MDQS Input Timing relative to MCK Output (read)

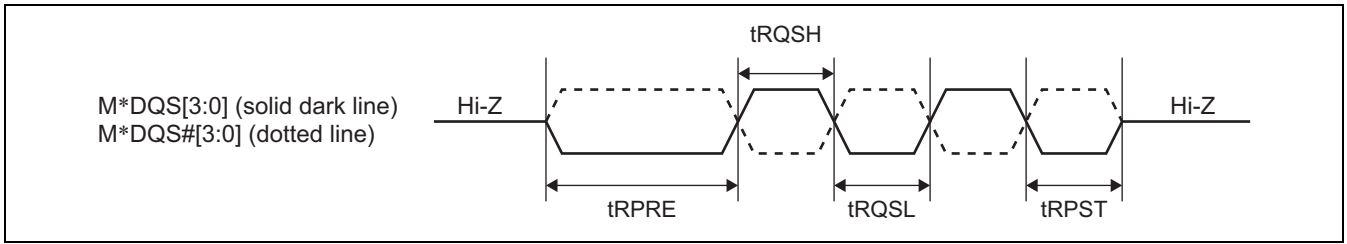


Figure 63.7.8 MDQS Input Timing (read)

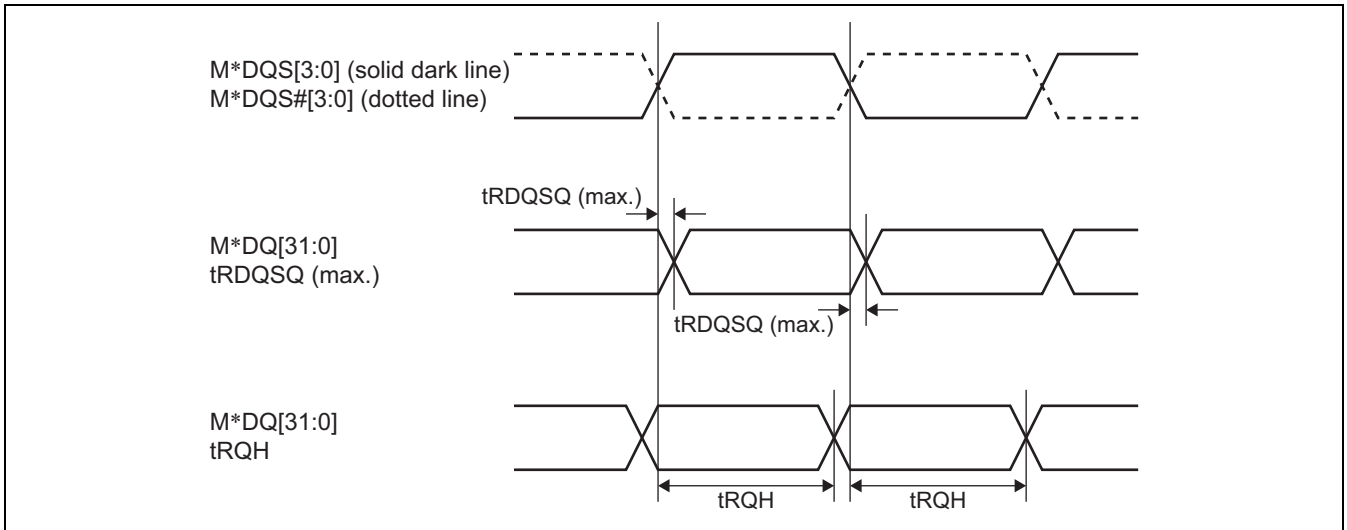


Figure 63.7.9 MDQ Input Timing relative to MDQS (read)

## 63.8 Display Unit (DU)

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

**Table 63.8.1 DOTCLKIN Timing**

Conditions: VCCQ18 = 1.8 V ± 0.1 V (H: DU0-2 and M, N: DU0), VDDQ/VCCQ = 3.3 V ± 0.3 V (M, N: DU1, E), GND = VSS = 0 V, Tc = -40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Figure
DOTCLKIN cycle time	tDICYC	8.4	—	200	ns	Figure 63.8.1
DOTCLKIN High level time	tDCKIH	3	—	—	ns	
DOTCLKIN Low level time	tDCKIL	3	—	—	ns	

**Table 63.8.2 Display Signal Timing**

Conditions: VDDQ/VCCQ = 3.3 V ± 0.3 V, GND = VSS = 0 V, Tc = -40 to +105°C, CL = 20 pF

Item	Symbol	Min.	Typ.	Max.	Unit	Figures
Display input control signal*1 setup time	tDS1	5	—	—	ns	Figure 63.8.2
Display input control signal*1 hold time	tDH1	3	—	—	ns	(relative to DOTCLKIN)
DOTCLKOUT output cycle time	tDCYC	10	—	200	ns	Figure 63.8.3
DOTCLKOUT output high level width	tDCKH	2	—	—	ns	(relative to DOTCLKOUT)
Display input control signal*1 setup time*2	tDS2	13	—	—	ns	
Display input control signal*1 hold time*2	tDH2	-6	—	—	ns	
Display output control signal*1 output delay time	tDD	2	—	8.5	ns	
Display digital data*1 output delay time	tDD	2	—	8.5	ns	
Display digital data 2*1 output delay time*3	tDD2	2	—	8.5	ns	
EXHSYNC# input low level width	tEXHLW	4tDCYC	—	—	ns	Figure 63.8.4
EXHSYNC# input high level width	tEXHHW	4tDCYC	—	—	ns	
EXVSYNC# input low level width	tEXVLW	3HC	—	—	tDCYC	
ODDF# setup time 1*4	tOD1	(ys+yw) × HC	—	—	tDCYC	
ODDF# setup time 2*4	tOD2	1HC	—	—	tDCYC	

Notes: 1. For correspondence between these signals and pin names, refer to Table 63.8.3.

2. Clock signal is input from DOTCLKIN and then output from DOTCLKOUT without being frequency-divided.

3. This electrical characteristic is applicable when the DR0D bit (bit 21) in the display output control register (DORCR) is set to 1. When the DR1D bit is cleared to 0, this characteristic is the same as the display digital data output delay time (tDD). Min value of tDCYC will be twice. This electrical characteristic applies to only DU0 output.

4. ys, yw and HC in Min value of ODDF# setup time 1 and ODDF# setup time 2 (tOD1 and tOD2);

ys: From rise of VSYNC to display start position in the vertical direction of the display screen (unit: raster line)

yw: Vertical display period of display screen (unit: raster line)

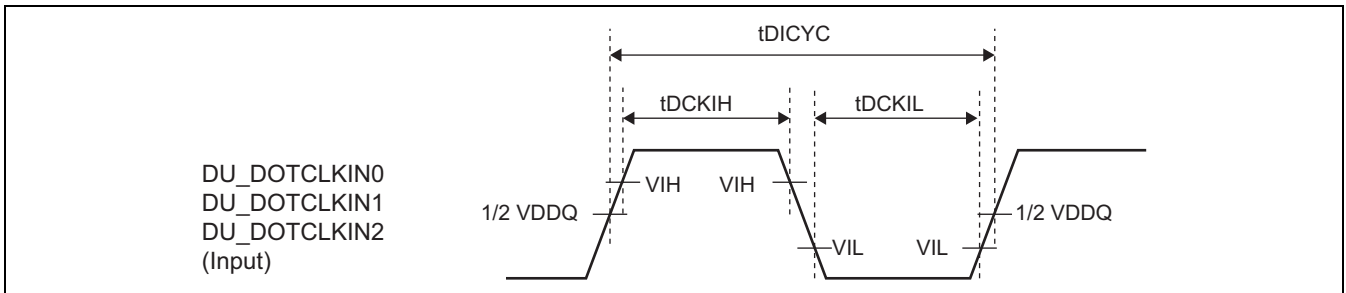
HC: Horizontal scan period (unit: dot clock)

**Table 63.8.3 Correspondence between Signals in Notes and Pin Names**

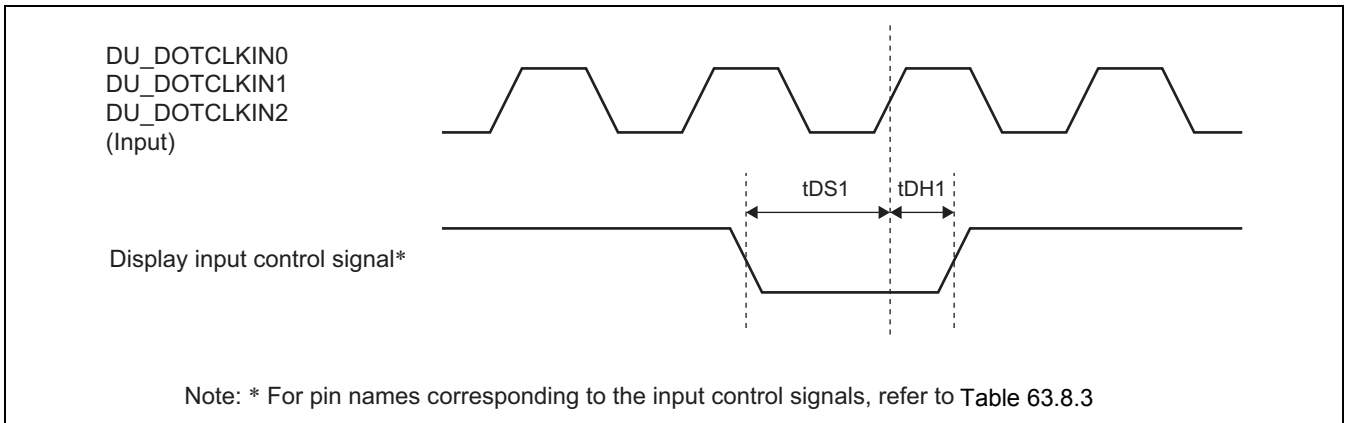
Signal in Note	Pin Name
Display input control signals	DU*_EXVSYNC/DU_VSYNC
	DU*_EXHSYNC/DU_HSYNC

Signal in Note	Pin Name
Display output control signals	DU*_EXODDF/DU_ODDF/DISP/CDE
	DU*_EXVSYNC/DU_VSYNC
	DU*_EXHSYNC/DU_HSYNC
	DU*_EXODDF/DU_ODDF/DISP/CDE
	DU*_DISP
Display digital data/display digital data 2	DU*_CDE
	DU*_DR7(_Yn_DATAm)
	DU*_DR6(_Yn_DATAm)
	DU*_DR5(_Yn_DATAm)
	DU*_DR4(_Yn_DATAm)
	DU*_DR3(_Yn_DATAm)
	DU*_DR2(_Yn_DATAm)
	DU*_DR1(_Yn_DATAm)
	DU*_DR0(_Yn_DATAm)
	DU*_DG7(_C/Yn_DATAm)
	DU*_DG6(_C/Yn_DATAm)
	DU*_DG5(_C/Yn_DATAm)
	DU*_DG4(_C/Yn_DATAm)
	DU*_DG3(_C/Yn_DATAm)
	DU*_DG2(_C/Yn_DATAm)
	DU*_DG1(_C/Yn_DATAm)
	DU*_DG0(_C/Yn_DATAm)
	DU*_DB7(_Cn_DATAm)
	DU*_DB6(_Cn_DATAm)
	DU*_DB5(_Cn_DATAm)
	DU*_DB4(_Cn_DATAm)
	DU*_DB3(_Cn_DATAm)
	DU*_DB2(_Cn_DATAm)
	DU*_DB1(_Cn_DATAm)
	DU*_DB0(_Cn_DATAm)

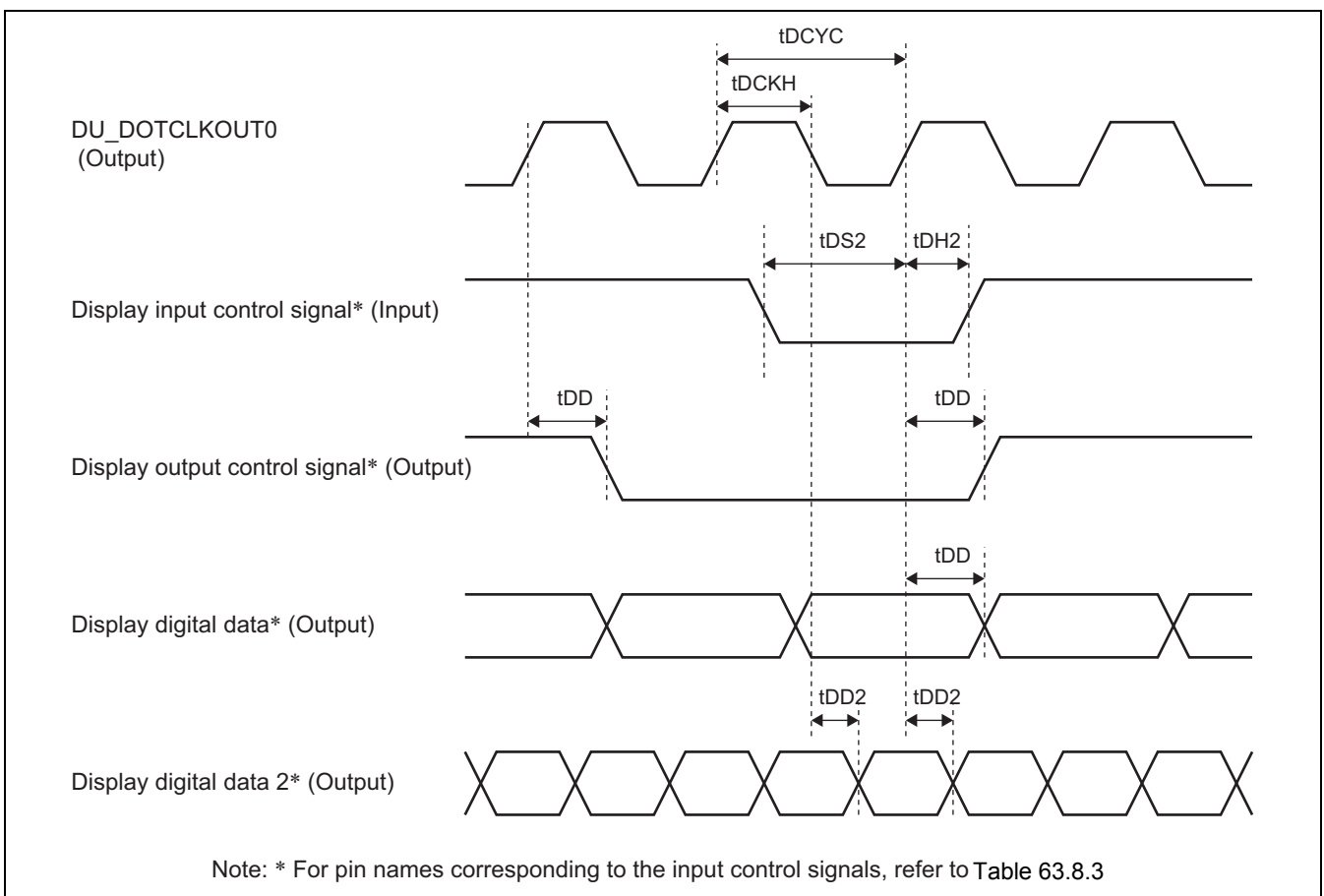
Note: \* Blank, 0, or 1; for details of pin name, refer to section 21, Display Unit (DU).



**Figure 63.8.1 DOTCLKIN Clock Input Timing**



**Figure 63.8.2 Display Signal Timing (Relative to DOTCLKIN)**



**Figure 63.8.3 Display Signal Timing (Relative to DOTCLKOUT)**



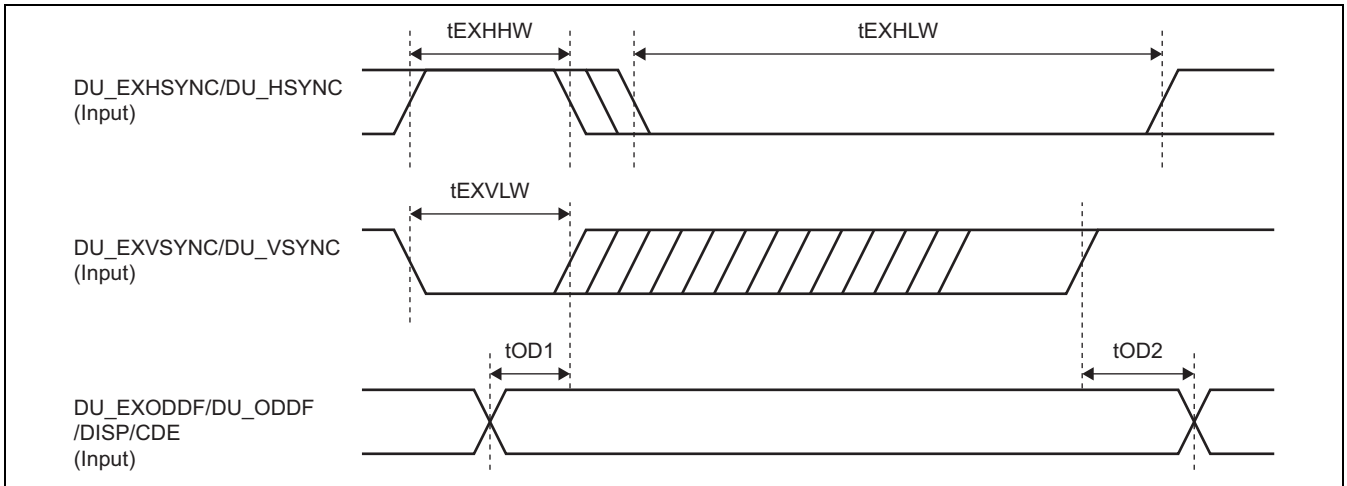


Figure 63.8.4 TV Sync Mode Display Signal Timing

63.9 LVDS

<b>RZ/G1H</b>	<b>RZ/G1N</b>
<b>RZ/G1M</b>	<b>RZ/G1E</b>

**Table 63.9.1 LVDS Dot Clock Input Timing (RZ/G1H, M and N)**

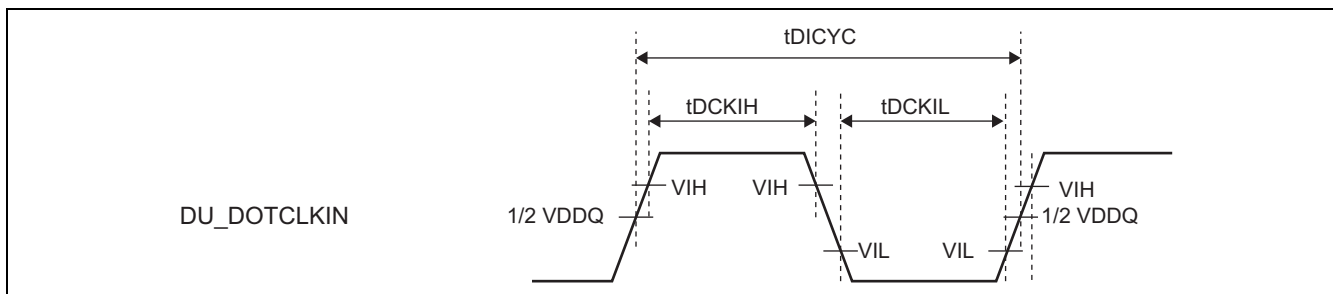
Conditions: VCCQ18 = 1.8 V ± 0.1 V, GND = VSS = 0 V, Tc = -40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Figure
DU_DOTCLKIN cycle time	tDCYC	6.73	—	32.0	ns	Figure 63.9.1
DU_DOTCLKIN high level width	tDCKIH	3.0	—	—	ns	
DU_DOTCLKIN low level width	tDCKIL	3.0	—	—	ns	

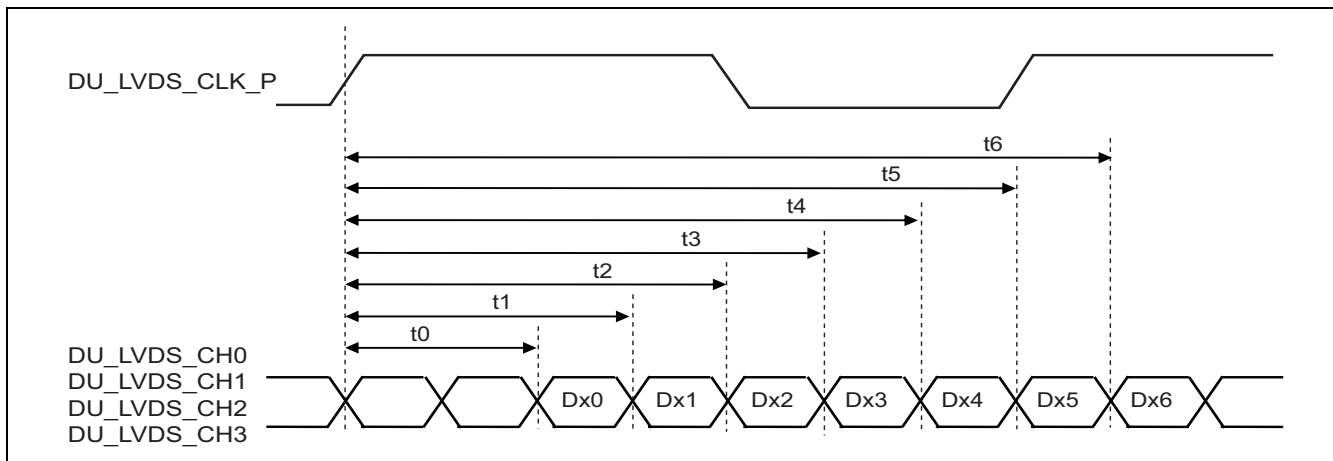
**Table 63.9.2 LVDS Module Signal Timing (RZ/G1H, M and N)**

Conditions: VDDQ\_LVDS = 1.8 V ± 0.1 V, GND = VSS = 0 V, Tc = -40 to +105°C, CL = 5 pF, RL = 100 Ω

Item	Symbol	Min.	Typ.	Max.	Unit	Figure
Data delay time (bit 0 data)	t0	2/7 tDCYC -0.20	—	2/7 tDCYC +0.20	ns	Figure 63.9.2
Data delay time (bit 1 data)	t1	3/7 tDCYC -0.20	—	3/7 tDCYC +0.20	ns	
Data delay time (bit 2 data)	t2	4/7 tDCYC -0.20	—	4/7 tDCYC +0.20	ns	
Data delay time (bit 3 data)	t3	5/7 tDCYC -0.20	—	5/7 tDCYC +0.20	ns	
Data delay time (bit 4 data)	t4	6/7 tDCYC -0.20	—	6/7 tDCYC +0.20	ns	
Data delay time (bit 5 data)	t5	7/7 tDCYC -0.20	—	7/7 tDCYC +0.20	ns	
Data delay time (bit 6 data)	t6	8/7 tDCYC -0.20	—	8/7 tDCYC +0.20	ns	



**Figure 63.9.1 DU\_DOTCLKIN Clock Input Timing**



**Figure 63.9.2 Display Output Timing**

## 63.10 Video Input Module (VIN)

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

Table 63.10.1 VIN Signal Timing

Conditions: VCCQ = VCCQ\_SDn = 3.3 V ± 0.3 V [H, M, N, E], GND = VSS = 0 V, Tc = -40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Figure
VI_CLK cycle time	tVCcyc	10	37	—	ns	Figure 63.10.1
Data setup time	tVCDs	3.5	—	—	ns	
Data/control hold time	tVCDh	1.5	—	—	ns	
Sync signal setup time	tVCCEs	3.5	—	—	ns	
Sync signal hold time	tVCCEh	1.5	—	—	ns	
VI_HSYNC# hold cycle	tVCMcyc	8	—	—	tVCcyc	
VI_HSYNC# Low period	tVCHL	300	—	—	ns	

Table 63.10.2 VIN Signal Timing (double-edge capture mode: RZ/G1H only)

Conditions: VCCQ = VCCQ\_SDn = 3.3 V ± 0.3 V, GND = VSS = 0 V, Tc = -40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks	Figure
VI_CLK cycle time	tVCcyc	12.5	37	—	ns	Max. 80 MHz	Figure 63.10.2
VI_CLK clock duty	tVCdtyH/L	45:55	—	55:45	%	tVCdtyH: tVCdtyL	
Data setup time	tVCDs	1.8	—	—	ns	—	
Data hold time	tVCDh	0.5	—	—	ns	—	
Sync signal setup time	tVCCEs	3.5	—	—	ns	ITU-R BT.601	
Sync signal hold time	tVCCEh	1.5	—	—	ns	ITU-R BT.601	

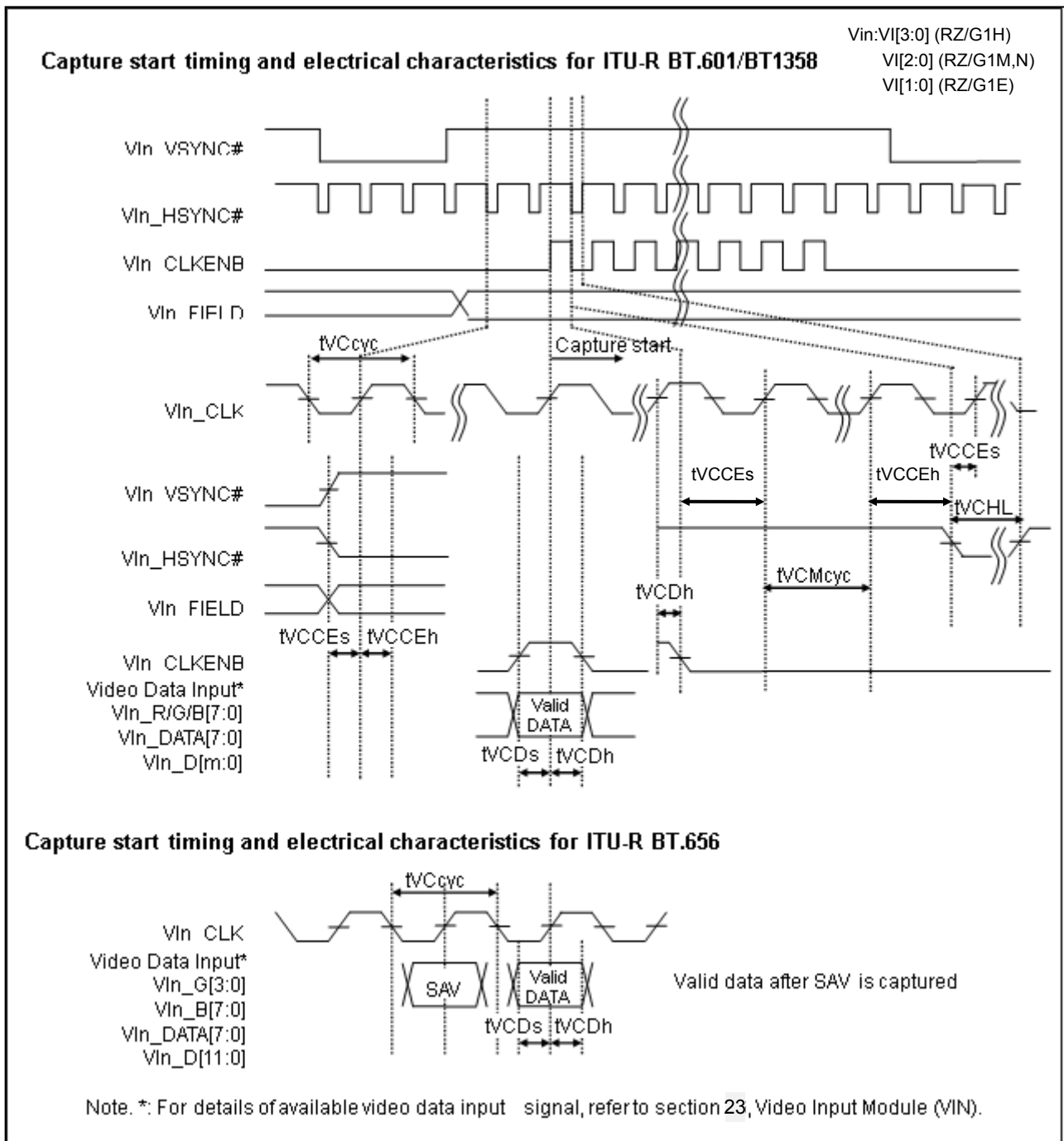
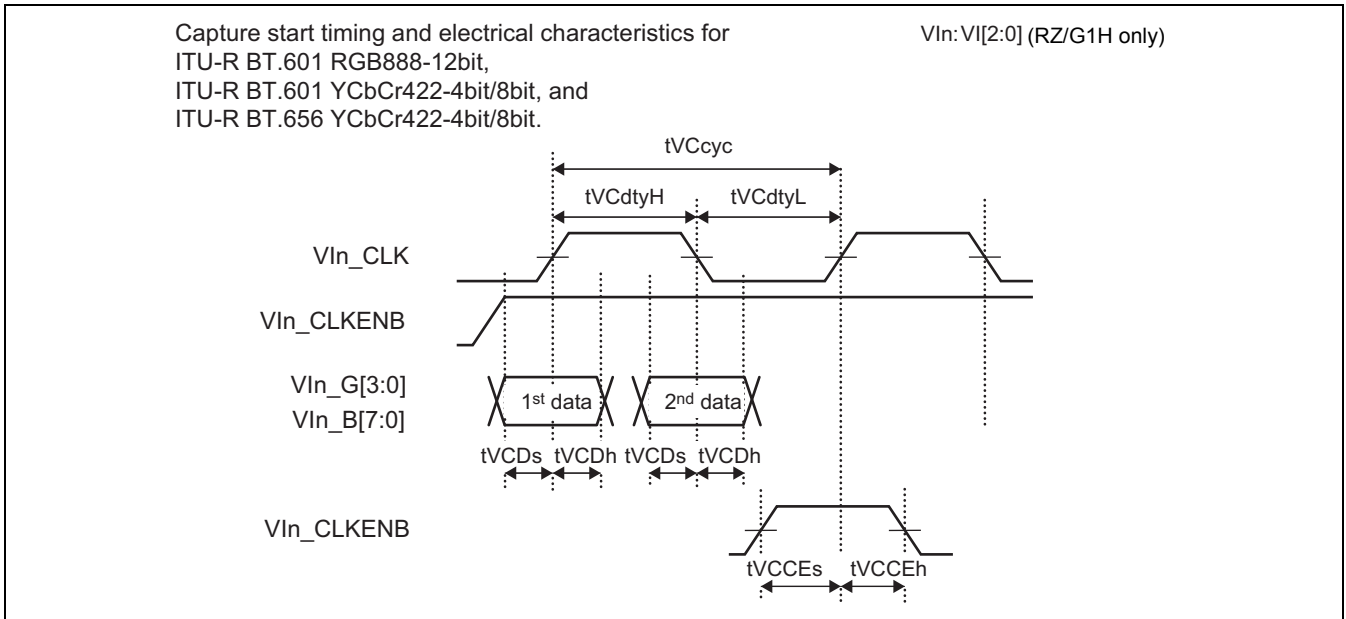


Figure 63.10.1 Capture start timing and electrical characteristics [H, M, N, E]



**Figure 63.10.2 Capture Start Timing and Electrical Characteristics (double-edge capture mode\*) [H]**

Note: \* Double-edge capture mode is available only for the RZ/G1H.

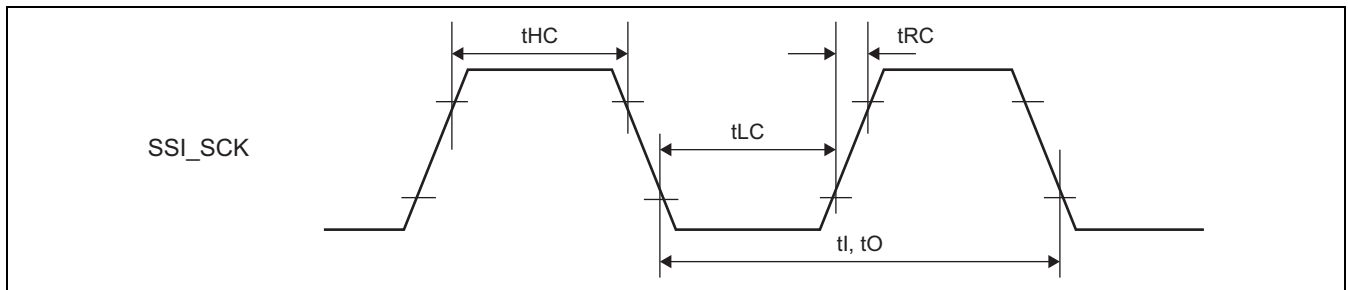
### 63.11 SSI Interface

<b>RZ/G1H</b>	<b>RZ/G1N</b>
<b>RZ/G1M</b>	<b>RZ/G1E</b>

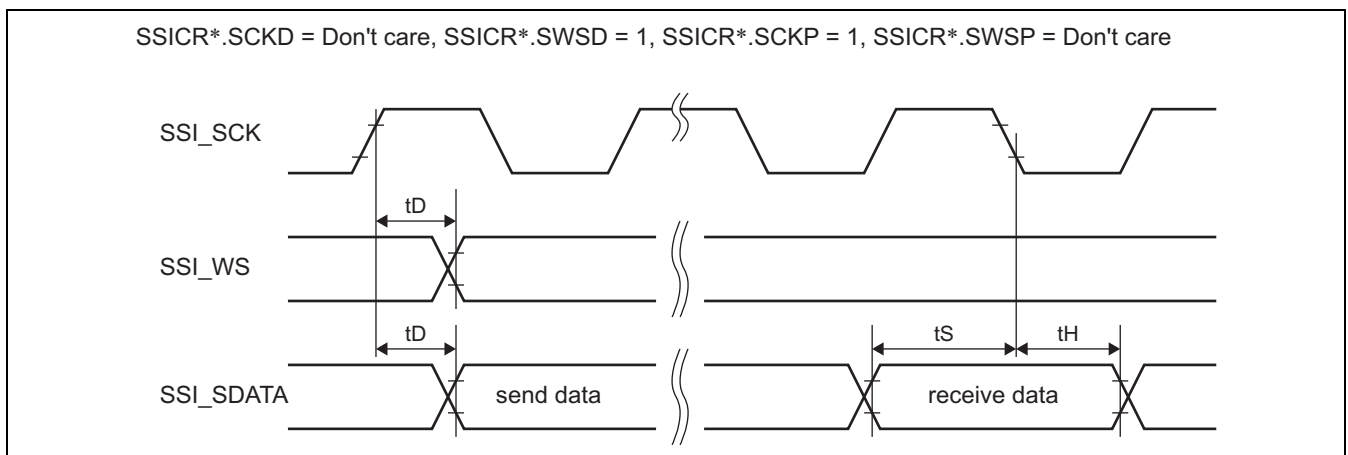
**Table 63.11.1 SSI Interface Signal Timing**

Conditions: VCCQ/VDDQ = 3.3 V ± 0.3 V, GND = VSS = 0 V, Tc = -40 to +105°C,  
 CL = 30 pF (other than tRC: Rise-edge clock timing)

Item	Symbol	Min.	Typ.	Max.	Unit	Note	Figure
Output clock cycle	tO	80	—	15625	ns	—	Figure 63.11.1
Input clock cycle	tI	66	—	15625	ns	—	
Output clock high-cycle	tHC	35	—	—	ns	—	
Output clock low-cycle	tLC	35	—	—	ns	—	
Input clock high-cycle	tHC	28	—	—	ns	—	
Input clock low-cycle	tLC	28	—	—	ns	—	
Rise-edge clock timing	tRC	—	—	20	ns	Output (100pF)	
Output delay	tD	-5	—	19	ns	—	Figures 63.11.2 to 63.11.5
	tD	—	—	22	ns	—	Figure 63.11.6
Setup time	tS	15	—	—	ns	—	Figures 63.11.2 to 63.11.6
Hold time	tH	5	—	—	ns	—	
Audio clock frequency	fAUDIO	3.072	—	25	MHz	—	Figure 63.11.7



**Figure 63.11.1 SCK Clock Input/output Timing**



**Figure 63.11.2 SSI Timing (1)**

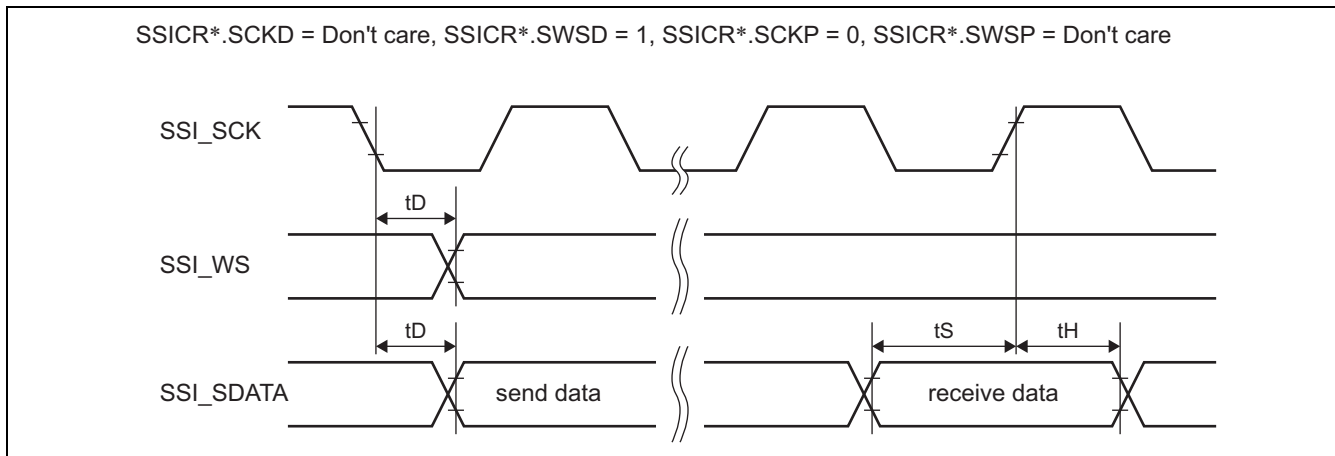


Figure 63.11.3 SSI Timing (2)

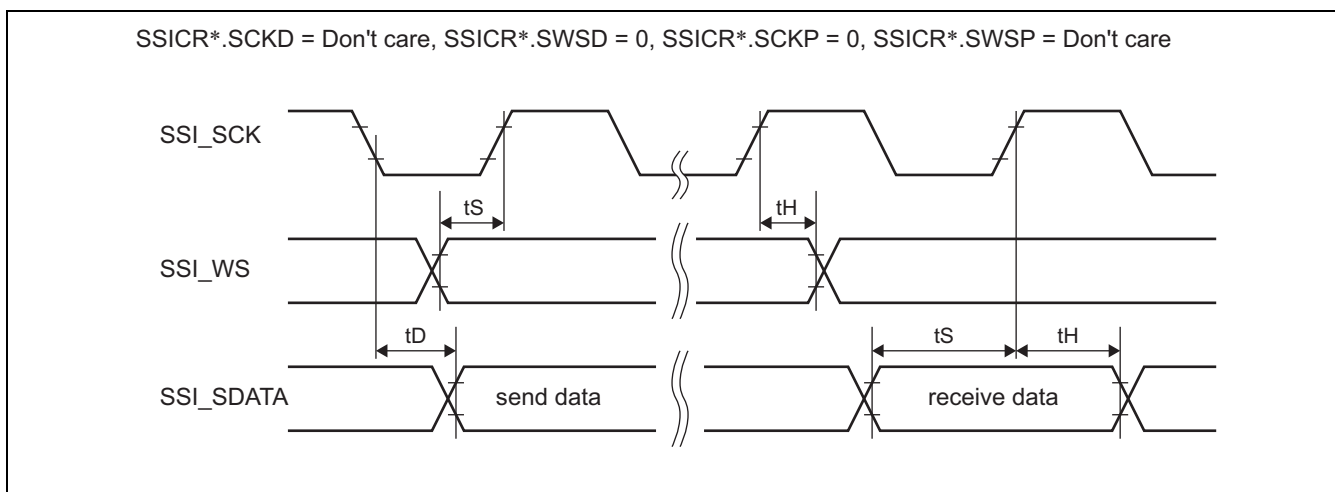


Figure 63.11.4 SSI Timing (3)

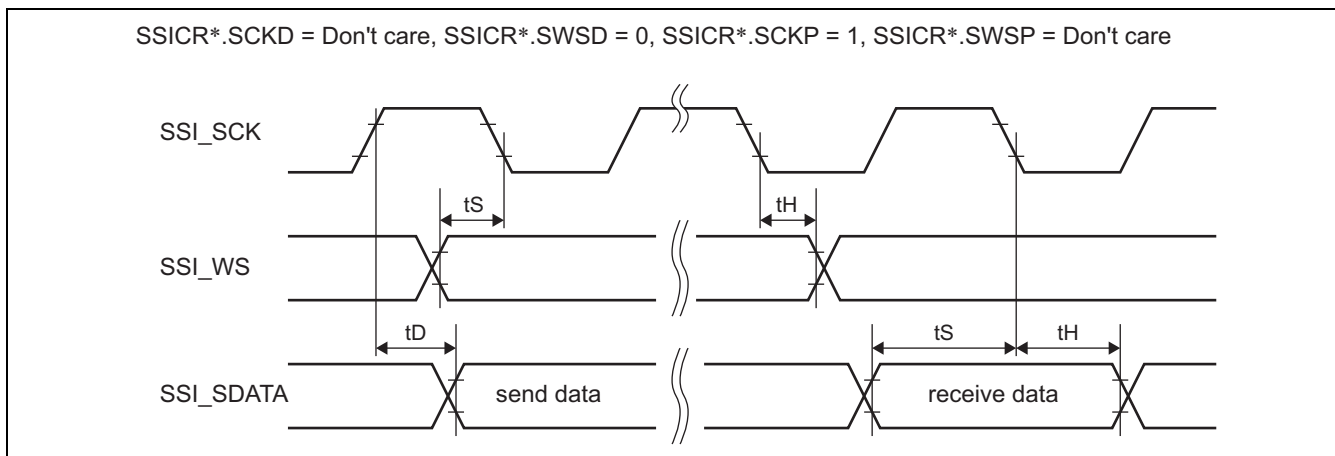


Figure 63.11.5 SSI Timing (4)

The follows are output timings of the MSB bit in the setting of the slave transmission by non-compression.  
 Send data is no padding bit with a left justify format or a right justify format.  
 SSICR\*.SCKD=0, SSICR\*.SWSD=0, SSICR\*.DEL=1, SSICR\*.TRMD=1  
 SSICR\*.SDTA=0 or SSICR\*.SDTA=1 and moreover SSICR\*.SWL=SSICR\*.DWL

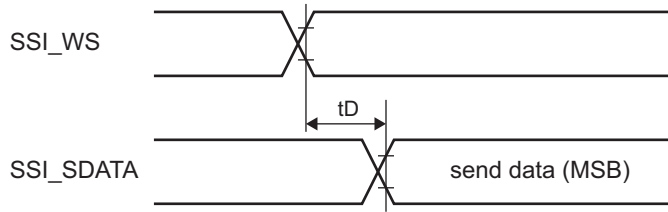


Figure 63.11.6 SSI Timing (5)

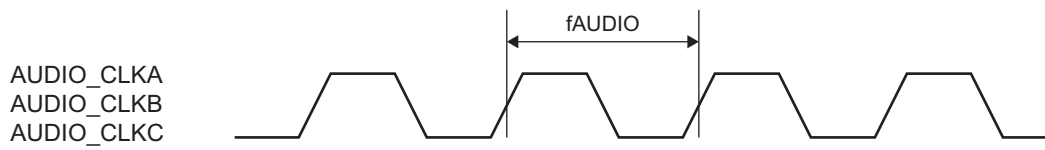


Figure 63.11.7 AUDIO\_CLK Input Timing



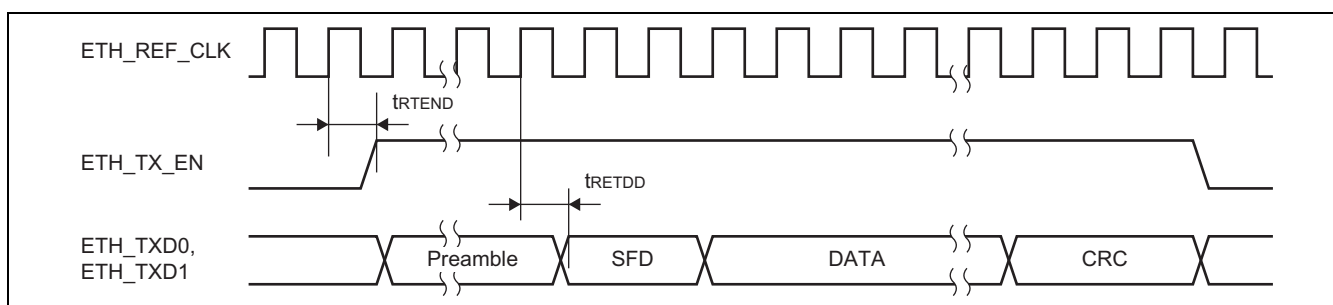
### 63.12 Ethernet MAC Controller Signal Timing

<b>RZ/G1H</b>	<b>RZ/G1N</b>
<b>RZ/G1M</b>	<b>RZ/G1E</b>

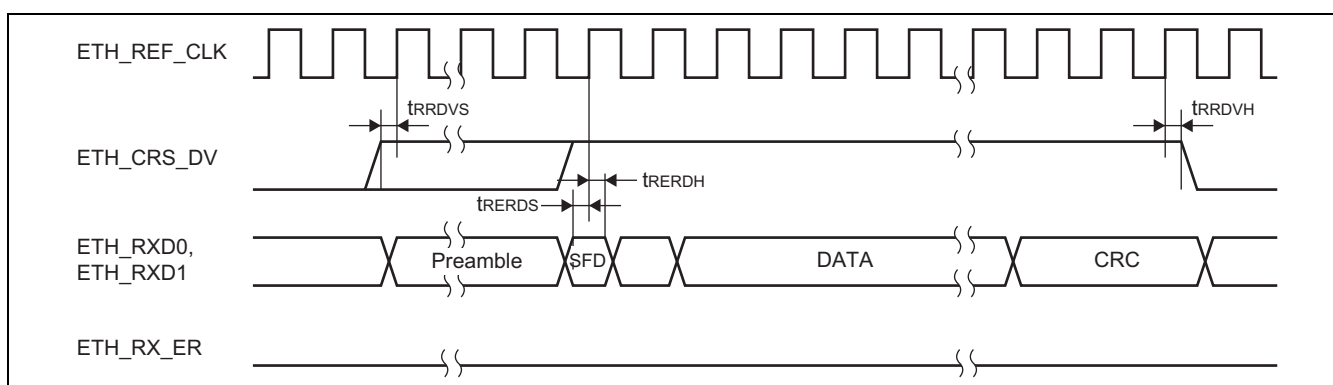
**Table 63.12.1 Ethernet MAC Controller Signal Timing (RMII)**

Conditions: VCCQ = 3.3 ± 0.3 V, GND = VSS = 0 V, Tc = -40 to +105°C, CL = 30 pF

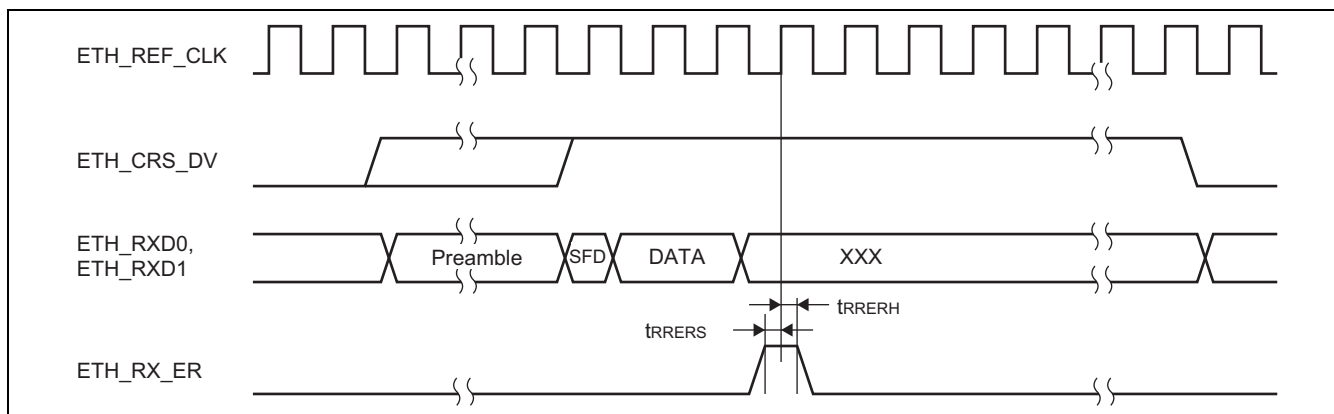
Item	Symbol	Min.	Typ.	Max.	Unit	Figures
ETH_REF_CLK clock input frequency	$f_{RTcyc}$	50 – 50 ppm	—	50 + 50 ppm	MHz	Figure 63.12.1
ETH_TX_EN output delay time	$t_{RTEND}$	2.5	—	12	ns	
ETH_TXD1, ETH_TXD0 output delay time	$t_{RETDD}$	2.5	—	12	ns	
ETH_CRS_DV setup time	$t_{RRDVS}$	4	—	—	ns	Figure 63.12.2
ETH_CRS_DV hold time	$t_{RRDVH}$	2.5	—	—	ns	
ETH_RXD1, ETH_RXD0 setup time	$t_{RERDS}$	4	—	—	ns	
ETH_RXD1, ETH_RXD0 hold time	$t_{RERDH}$	2.5	—	—	ns	
ETH_RX_ER setup time	$t_{RRERS}$	4	—	—	ns	Figure 63.12.3
ETH_RX_ER hold time	$t_{RRERH}$	2.5	—	—	ns	



**Figure 63.12.1 RMII Transmission Timing**



**Figure 63.12.2 RMII Reception Timing (Normal Operation)**



**Figure 63.12.3 RMII Reception Timing (Case When Error Occurs)**

**(1) ETH\_MDC (Management Data Clock) timing specification (setup time and hold time)**

Although ETH\_MDC is a reference clock for the serial management interface (SMI), ETH\_MDC input setup time and ETH\_MDC input hold time are not specified.

**(2) ETH\_MDIO (Management Data Input/Output) timing provision (setup time and hold time)**

The AC specifications for the SMI (PHY side) from the IEEE are as follows:

ETH\_MDC input cycle  $\geq 400$  ns.

ETH\_MDC input pulse width at each level  $\geq 160$  ns

ETH\_MDIO input setup and hold times  $\geq 10$  ns (PHY latches the MAC output on rising edges of ETH\_MDC).

ETH\_MDIO output delay time = 0 to 300 ns (delay time from a rising edge of ETH\_MDC)

The ETH\_MDC output, ETH\_MDIO output, and ETH\_MDIO input latching depend on software adjusting settings in the PHY interface register (PIR). Adjust the ETH\_MDC output (period) and ETH\_MDIO output (timing of changes) to satisfy the AC input specs on the PHY side. To adjust the timing of ETH\_MDIO input latching, consider the AC output specifications on the PHY side.

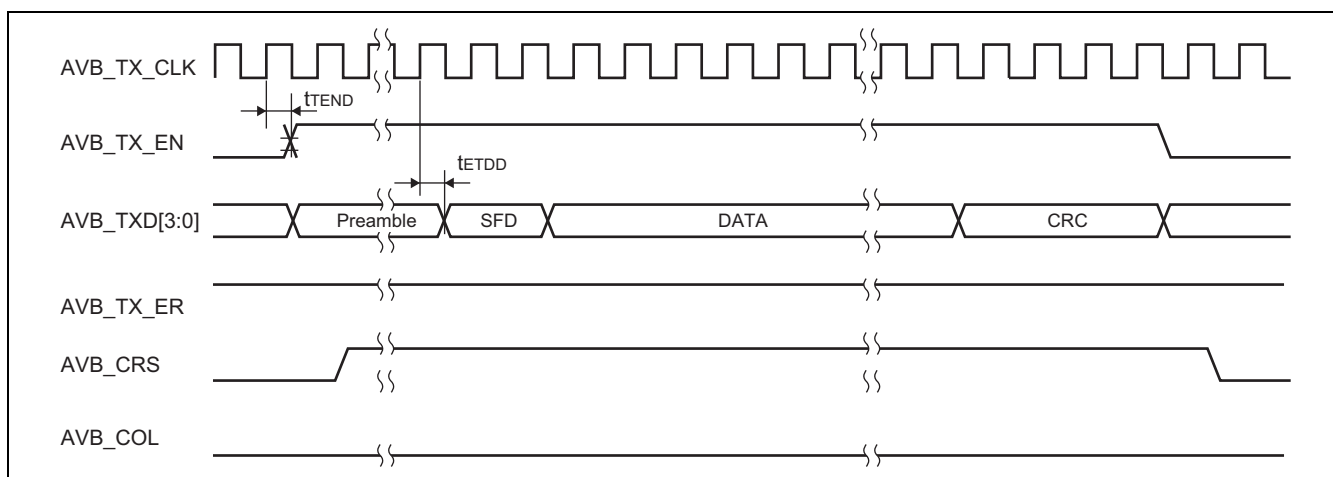
### 63.13 Ethernet AVB Module Signal Timing

<b>RZ/G1H</b>	<b>RZ/G1N</b>
<b>RZ/G1M</b>	<b>RZ/G1E</b>

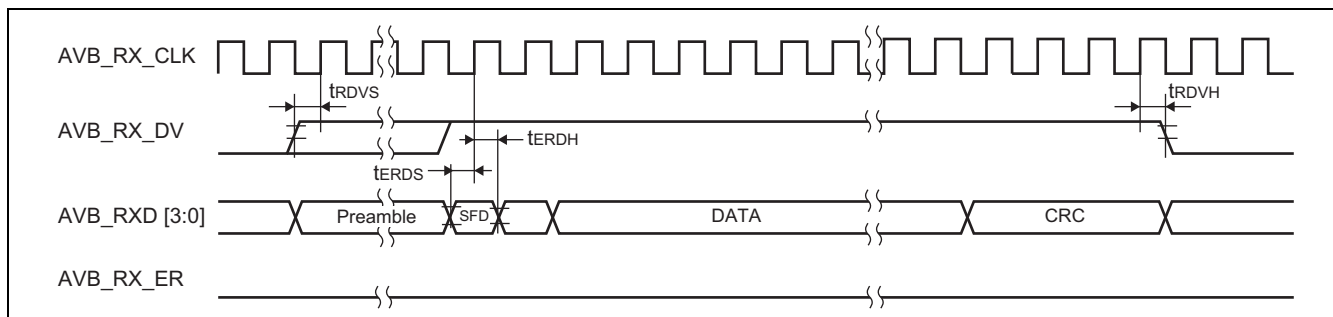
**Table 63.13.1 Ethernet Control Timing (MII)**

Conditions: VCCQ/VDDQ = VCCQ\_SDn = 3.3 ± 0.3 V, Tc = -40 to +105 °C, GND = VSSQ = 0 V, CL = 30 pF

Item	Symbol	Min.	Typ.	Max.	Unit	Figures
AVB_TX_CLK cycle time	t <sub>cyc</sub>	40	—	—	ns	Figure 63.13.1
AVB_TX_EN output delay time	t <sub>TEND</sub>	0	—	25	ns	
AVB_TXD[3:0] output delay time	t <sub>ETDD</sub>	0	—	25	ns	
AVB_RX_CLK cycle time	t <sub>Rcyc</sub>	40	—	—	ns	Figure 63.13.2
AVB_RX_DV setup time	t <sub>RDVS</sub>	10	—	—	ns	
AVB_RX_DV hold time	t <sub>RDVH</sub>	10	—	—	ns	
AVB_RXD[3:0] setup time	t <sub>ERDS</sub>	10	—	—	ns	
AVB_RXD[3:0] hold time	t <sub>ERDH</sub>	10	—	—	ns	
AVB_RX_ER setup time	t <sub>RERS</sub>	10	—	—	ns	Figure 63.13.3
AVB_RX_ER hold time	t <sub>RERH</sub>	10	—	—	ns	
AVB_MAGIC output delay time	t <sub>MAGICD</sub>	0	—	25	ns	Figure 63.13.4



**Figure 63.13.1 MII Transmission Timing (Normal Operation)**



**Figure 63.13.2 MII Reception Timing (Normal Operation)**

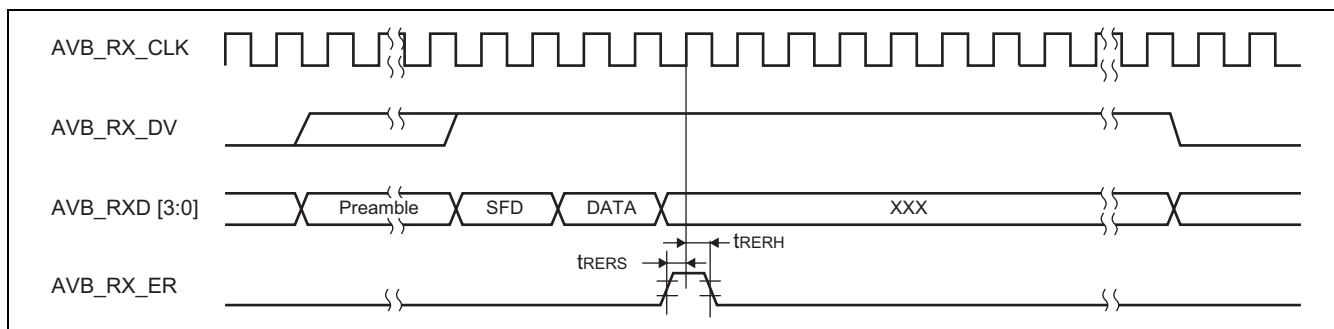


Figure 63.13.3 MII Reception Timing (Case When Error Occurs)

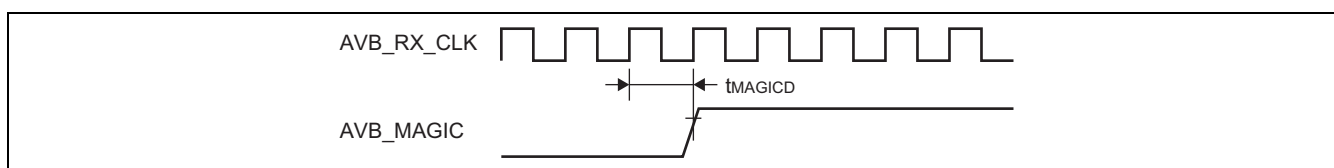


Figure 63.13.4 AVB\_MAGIC Output Timing

Table 63.13.2 Ethernet Control Timing (GMII)

Conditions: VCCQ/VDDQ = VCCQ\_SDn = 3.3 ± 0.3 V, Tc = -40 to +105 °C, GND = VSSQ = 0 V, CL = 30 pF

Item	Symbol	Min.	Typ.	Max.	Unit	Figures
AVB_GTXREFCLK clock input frequency	fREF125CK	125 – 100ppm	—	125 + 100ppm	MHz	—
AVB_GTX_CLK cycle time	tGTcyc	7.5	—	8.5	ns	Figure 63.13.5
AVB_TX_EN output delay time	tGTEND	0.5	—	5.5	ns	
AVB_TXD[7:0] output delay time	tGETDD	0.5	—	5.5	ns	
AVB_RX_CLK cycle time	tGRcyc	8	—	—	ns	Figure 63.13.6
AVB_RX_DV setup time	tGRDVS	2	—	—	ns	
AVB_RX_DV hold time	tGRDVH	0	—	—	ns	
AVB_RXD[7:0] setup time	tGERDS	2	—	—	ns	
AVB_RXD[7:0] hold time	tGERDH	0	—	—	ns	
AVB_RX_ER setup time	tGRERS	2	—	—	ns	Figure 63.13.7
AVB_RX_ER hold time	tGRERH	0	—	—	ns	
AVB_MAGIC output delay time	tMAGICD	0	—	25	ns	Figure 63.13.8

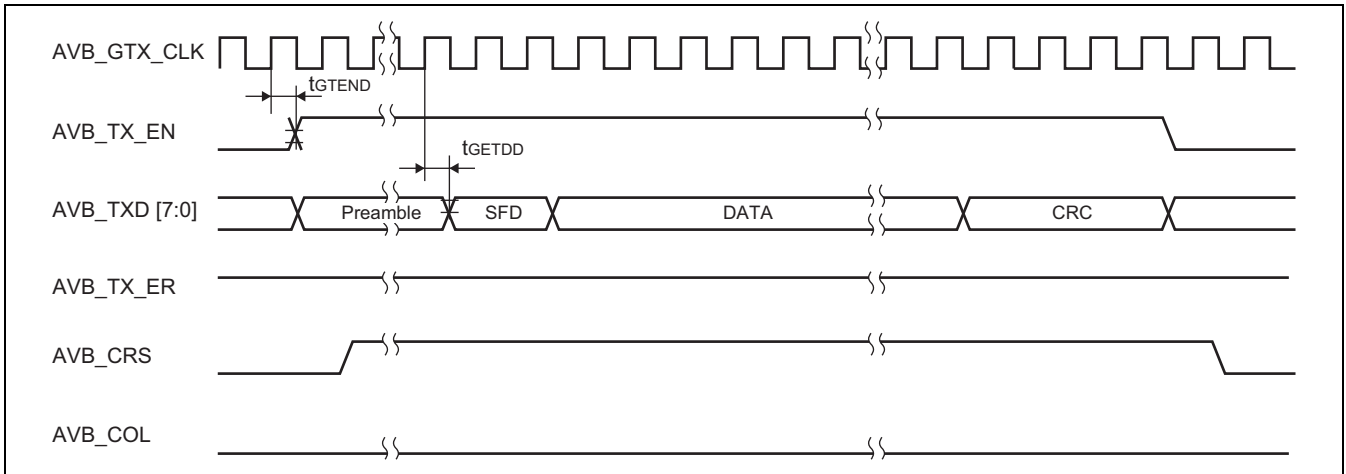


Figure 63.13.5 GmII Transmission Timing (Normal Operation)

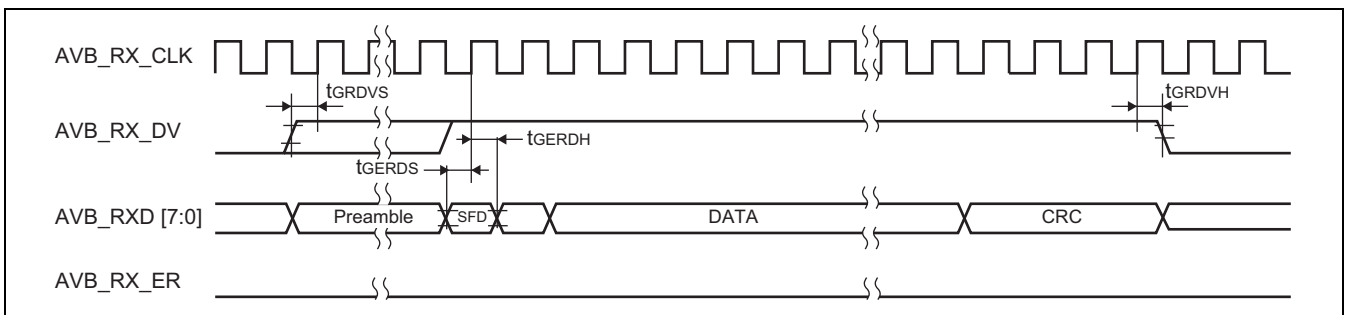


Figure 63.13.6 GmII Reception Timing (Normal Operation)

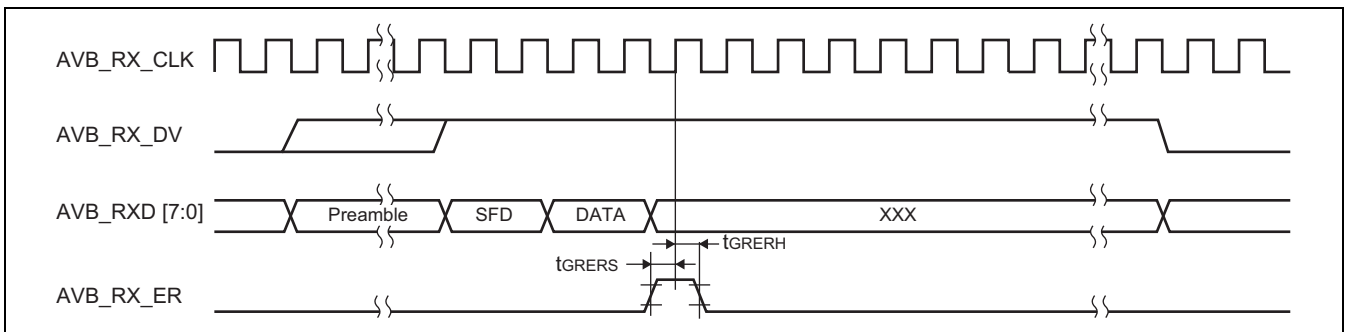


Figure 63.13.7 MII Reception Timing (Case When Error Occurs)

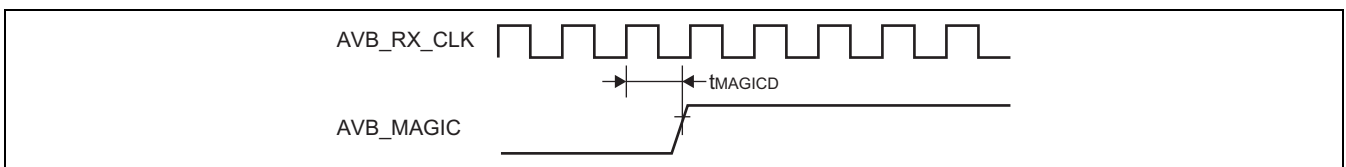


Figure 63.13.8 AVB\_MAGIC Output Timing

### 63.14 PCI Express Interface (Gen2)

<b>RZ/G1H</b>	<b>RZ/G1N</b>
<b>RZ/G1M</b>	<b>RZ/G1E</b>

The description in this section is compliant with the following PCIe standard:  
'PCI Express® Base Specification Revision 2.1, March 4, 2009'.

**Table 63.14.1 PCI Express (Gen2) Interface Characteristics (RZ/G1H, M and N)**

Conditions: VDDA\_SATA1 (VDDA\_PCIe) = 1.8 V, VDDD\_SATA1 (VDDD\_PCIe) = 1.03 V,  
VSS\_SATA1 (VSS\_PCIe) = GND = 0 V, Tc = -40 to +105°C

Test Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Differential Input Peak to Peak Voltage (2.5 GT/s)	VRX-DIFFp-p	0.175	—	1.200	V	*1
Differential Input Peak to Peak Voltage (5 GT/s)	VRX-DIFFp-p	0.120	—	1.200	V	*1
Differential Peak to Peak Output Voltage (2.5 & 5 GT/s)	VTX-DIFFp-p	0.800	—	1.2	V	*2
Absolute Delta of DC Common Mode Voltage between D+ and D- (2.5 & 5 GT/s)	VTX-CM-DC- LINE-DELTA	0	—	25	mV	*2
Unit Interval (2.5 GT/s)	UI	399.88	—	400.12	ps	*3
Unit Interval (5 GT/s)	UI	199.94	—	200.06	ps	*3
DC Differential TX Impedance (2.5 GT/s)	ZTX-DIFF-DC	80	—	120	Ω	—
DC Differential TX Impedance (5 GT/s)	ZTX-DIFF-DC	—	—	120	Ω	—
DC Differential Input Impedance (2.5 GT/s)	ZRX-DIFF-DC	80	—	120	Ω	—
DC Input Impedance (2.5 & 5 GT/s)	ZRX-DC	40	—	60	Ω	—

Notes: \*1. RXP, RXN: DC test

\*2. TXP, TXN: DC test

\*3. Need Reference Clock (Low Voltage Swing, Differential Clocks). The nominal single-ended swing for each clock is 0 to 0.7 V and a nominal frequency of 100 MHz ±100 PPM.

63.15 SCIF

<b>RZ/G1H</b>	<b>RZ/G1N</b>
<b>RZ/G1M</b>	<b>RZ/G1E</b>

Table 63.15.1 SCIF Signal Timing

Conditions: VCCQ/VDDQ = VCCQ\_SDn = 3.3 ± 0.3 V, GND = VSS = 0 V, Tc = -40 to +105 °C, CL = 30 pF

Item	Symbol	Min.	Typ.	Max.	Unit	Figures
Input clock cycle (asynchronous)	tSCYC	4	—	—	tCYC	Figure 63.15.1
Input clock cycle (synchronous)	tSCYC	8	—	—	tCYC	
Input clock pulse width	tSCKW	0.4	—	0.6	tSCYC	
Input clock rise time	tSCKr	—	—	0.8	tCYC	
Input clock fall time	tSCKf	—	—	0.8	tCYC	
Transmit data delay time	tTXD	—	—	4	tCYC	Figure 63.15.2
Receive data setup time (synchronous)	tRXS	5	—	—	tCYC	
Receive data hold time (synchronous)	tRXH	2	—	—	tCYC	

Note: tCYC is for one cycle of the Pφ clock.

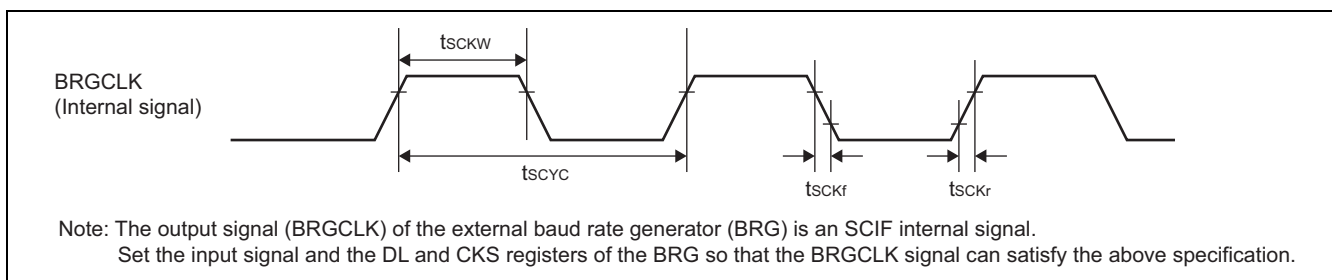


Figure 63.15.1 Input Clock Timing

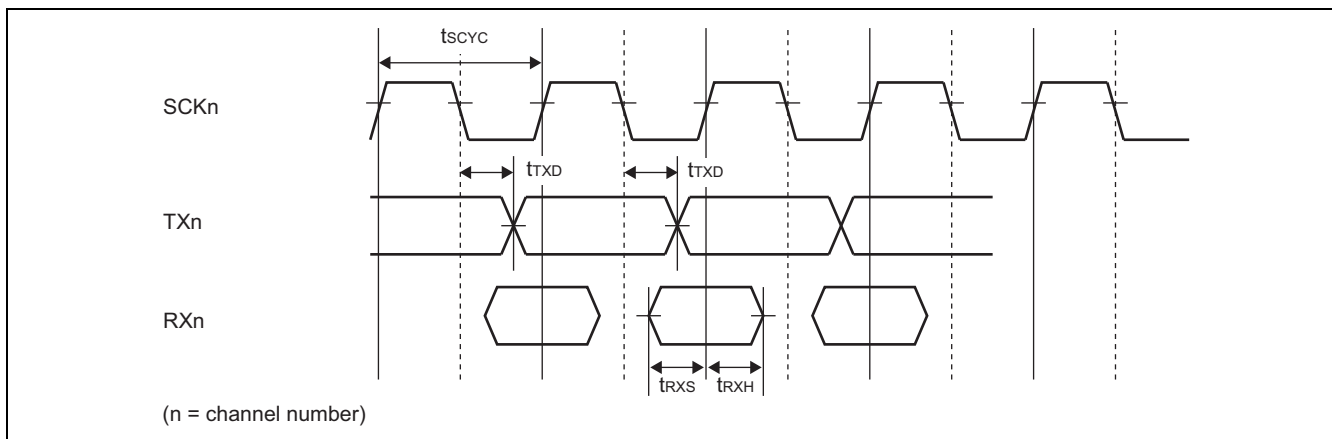


Figure 63.15.2 Input/output Timing in Synchronous Mode

## 63.16 SCIFA/B

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

Table 63.16.1 SCIFA/B Module Signal Timing (Asynchronous mode)

Conditions: VCCQ/VDDQ = VCCQ\_SDn = 3.3 V ± 0.3 V, GND = VSS = 0 V, Tc = -40 to +105°C, CL = 30 pF

Item	Symbol	Min.	Max.	Unit	Figure
SCK input clock cycle time	t <sub>SCYC</sub>	4	—	t <sub>pcyc</sub> *	Figure 63.16.1
SCK input clock high-level width	t <sub>SCWH</sub>	0.4	—	t <sub>scyc</sub>	
SCK input clock low-level width	t <sub>SCWL</sub>	0.4	—	t <sub>scyc</sub>	
SCK input clock rise-time	t <sub>SCKr</sub>	—	1.5	t <sub>pcyc</sub> *	
SCK input clock fall-time	t <sub>SCKf</sub>	—	1.5	t <sub>pcyc</sub> *	
TXD output delay time	t <sub>TXD</sub>	—	3 × t <sub>pcyc</sub> + 50	ns	Figure 63.16.2
RXD input setup time	t <sub>RXS</sub>	2 × t <sub>pcyc</sub>	—	ns	
RXD input hold time	t <sub>RXH</sub>	2 × t <sub>pcyc</sub>	—	ns	
RTS output delay	t <sub>RTSD</sub>	—	100	ns	
CTS setup time	t <sub>CTSS</sub>	100	—	ns	
CTS hold time	t <sub>CTSH</sub>	100	—	ns	

Note: \* t<sub>pcyc</sub> is a cycle time of peripheral clock (MPφ).

Table 63.16.2 SCIFA/B Module Signal Timing (Clock synchronous mode)

Conditions: VCCQ/VDDQ = VCCQ\_SDn = 3.3 V ± 0.3 V, GND = VSS = 0 V, Tc = -40 to +105°C, CL = 30 pF

Item	Symbol	Min.	Max.	Unit	Figure
SCK input/output clock cycle time	t <sub>SCYC</sub>	12	—	t <sub>pcyc</sub> *	Figure 63.16.1
SCK input/output clock high-level width	t <sub>SCWH</sub>	0.4	0.6	t <sub>scyc</sub>	
SCK input/output clock low-level width	t <sub>SCWL</sub>	0.4	0.6	t <sub>scyc</sub>	
SCK input/output synchronous clock rise-time	t <sub>SCKr</sub>	—	1.5	t <sub>pcyc</sub> *	
SCK input/output synchronous clock fall-time	t <sub>SCKf</sub>	—	1.5	t <sub>pcyc</sub> *	
TXD output delay time (when SCK is input)	t <sub>TXD</sub>	—	3 × t <sub>pcyc</sub> + 50	ns	Figure 63.16.2
TXD output delay time (when SCK is output)	t <sub>TXD</sub>	—	50	ns	
RXD input setup time	t <sub>RXS</sub>	4	—	t <sub>pcyc</sub> *	
RXD input hold time	t <sub>RXH</sub>	4	—	t <sub>pcyc</sub> *	

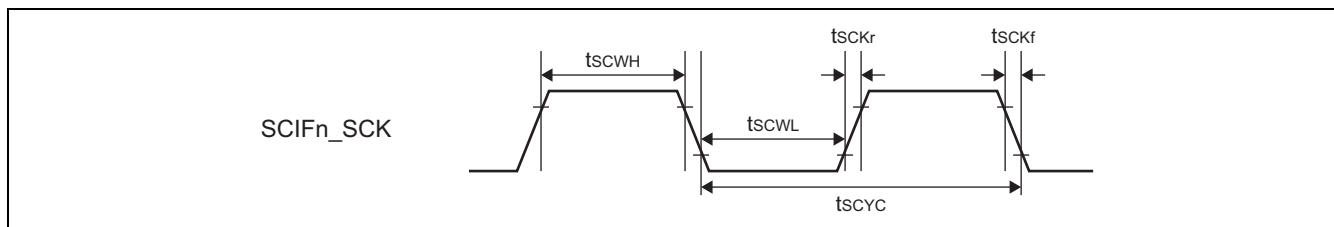
Note: \* t<sub>pcyc</sub> is a cycle time of peripheral clock (MPφ).

Figure 63.16.1 SCIFA/B Module Signal Timing



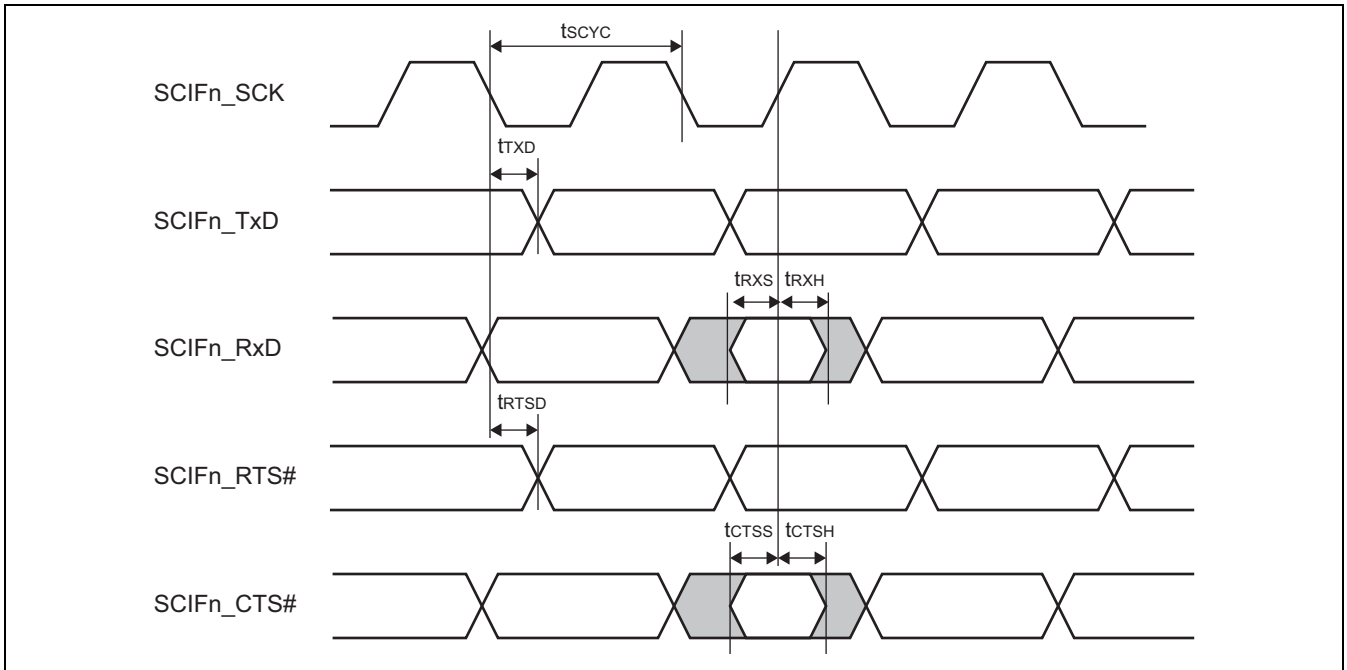


Figure 63.16.2 SCIFA/B Module Signal Timing

**63.17 HSCIF**

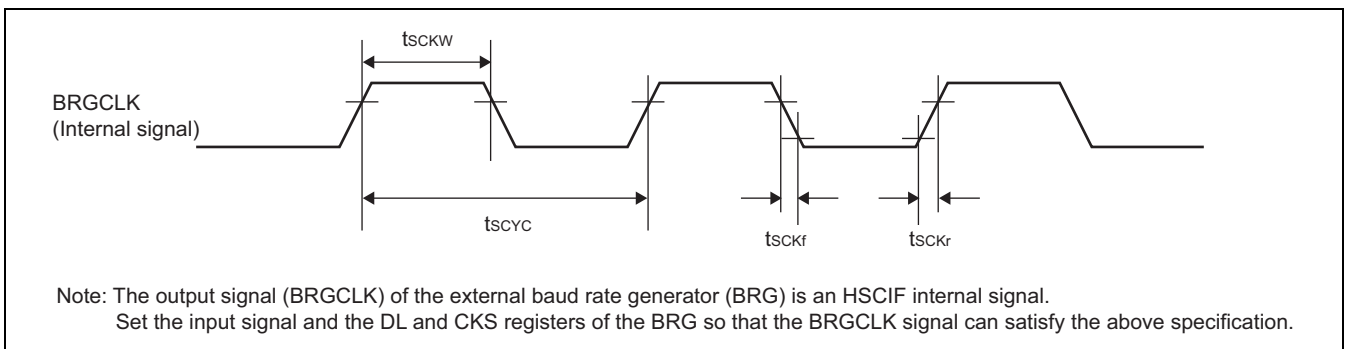
<b>RZ/G1H</b>	<b>RZ/G1N</b>
<b>RZ/G1M</b>	<b>RZ/G1E</b>

**Table 63.17.1 HSCIF Signal Timing**

Conditions: VCCQ/VDDQ = VCCQ\_SDn = 3.3 ± 0.3 V, GND = VSS = 0 V, Tc = -40 to +105 °C, CL = 30 pF

Item	Symbol	Min.	Typ.	Max.	Unit	Figure
Input clock cycle (asynchronous)	tSCYC	4	—	—	tCYC	Figure 63.17.1
Input clock pulse width	tSCKW	0.4	—	0.6	tSCYC	
Input clock rise time	tSCKr	—	—	0.8	tCYC	
Input clock fall time	tSCKf	—	—	0.8	tCYC	

Note: tCYC is for one cycle of the ZSφ clock.



**Figure 63.17.1 Input Clock Timing**

63.18 I2C

RZ/G1H	RZ/G1N
RZ/G1M	RZ/G1E

Table 63.18.1 I2C Signal Timing

Conditions: VCCQ/VDDQ = VCCQ\_SDn = 3.3 ± 0.3 V, VCCQ18/VDDQ18 = 1.8 V ± 0.1 V, GND = VSS = 0 V, Tc = -40 to 105 °C, CL = 400 pF

Item	Symbol	Min.	Typ.	Max.	Unit	Figures
I2C_SCL frequency	tICYC	—	—	400	kHz	Figure 63.18.1
I2C_SCL low level time	tLOW	$1/(2 \times tICYC) - 100$	—	—	ns	
I2C_SCL high level time	tHIGH	600	—	—	ns	
I2C_SCL/I2C_SDA falling time	tICF	—	—	250	ns	
I2C_SDA bus free time	tICBF	1300	—	—	ns	
I2C_SCL start condition hold time	tICH	600	—	—	ns	
I2C_SCL repeat-start condition setup time	tICS	600	—	—	ns	
I2C_SDA stop condition setup time	tICST	600	—	—	ns	
I2C_SDA setup time	tDAS	100	—	—	ns	
I2C_SDA hold time	tICDH	0	—	900	ns	

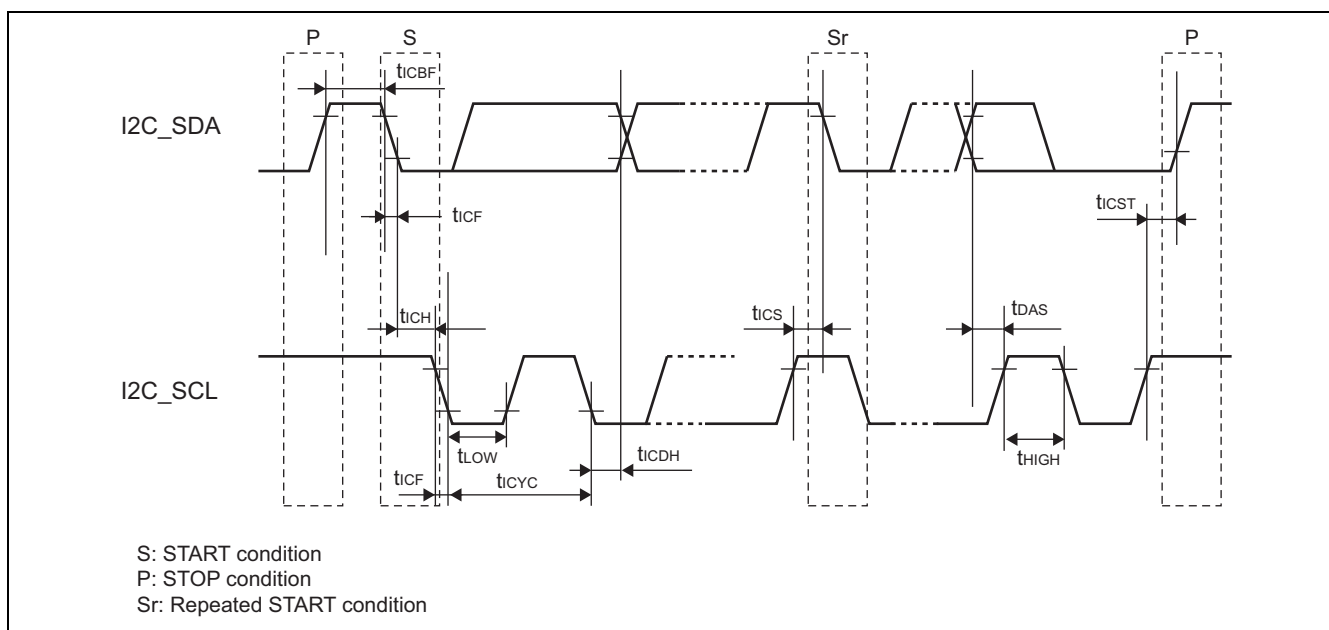


Figure 63.18.1 I2C Signal Timing

## 63.19 IIC Bus Interface

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

Table 63.19.1 IIC Bus Interface Signal Timing

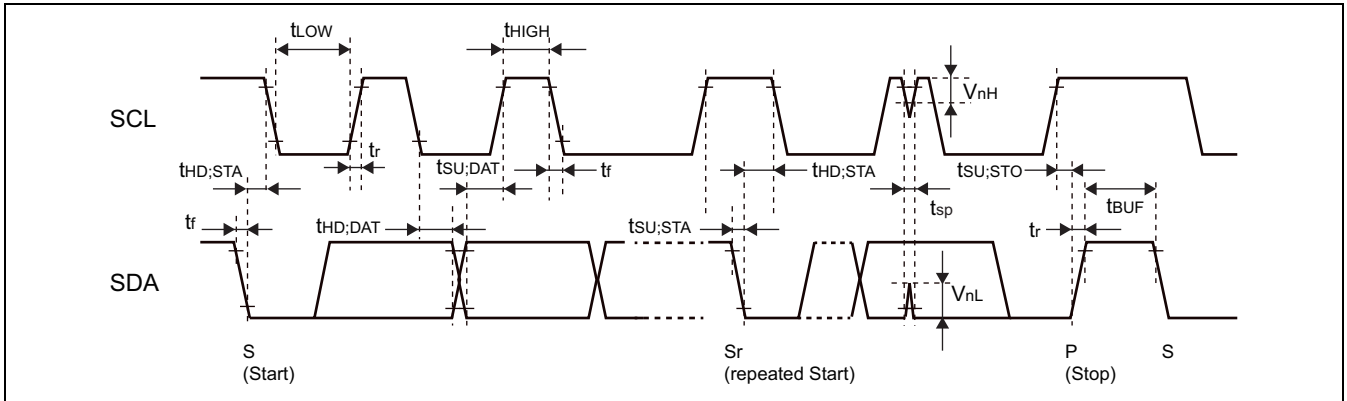
Condition: VCCQ /VDDQ = VCCQ\_SDn = 3.3 V ± 0.3 V or 1.8 V ± 0.1 V, GND = VSS = 0 V, Tc = -40 to +105°C,  
CL = 30 pF

Item	Symbol	Standard-Mode		Fast-Mode		Unit	Figure
		Min.	Max.	Min.	Max.		
SCLclock frequency	f <sub>SCL</sub>	0	100	0	400	kHz	Figure 63.19.1
Hold time (after repeat START condition, first clock pulse is generated)	t <sub>HD;STA</sub>	4.0	—	0.6	—	μs	
L period in SCL clock	t <sub>LOW</sub>	4.7	—	1.3	—	μs	
H period in SCL clock	t <sub>HIGH</sub>	4.0	—	0.6	—	μs	
Setup time for repeat START condition	t <sub>SU;STA</sub>	4.7	—	0.6	—	μs	
Date hold time	t <sub>HD;DAT</sub>	0	3.45	0	0.9	μs	
Data setup time	t <sub>SU;DAT</sub>	250	—	100	—	ns	
SDA and SCLsignal rise time	t <sub>r</sub>	—	1000	—	300	ns	
SDA and SCL signal fall time	t <sub>f</sub>	—	300	—	300	ns	
Setup time for STOP condition	t <sub>SU;STO</sub>	4.0	—	0.6	—	μs	
Bus free time between STOP and START conditions	t <sub>BUF</sub>	4.7	—	1.3	—	μs	
Noise margin at low level of each connected device (including hysteresis)	VnL	0.1 ×VCCQ	—	0.1 ×VCCQ	—	V	
Noise margin at high level of each connected device (including hysteresis)	VnH	0.2 ×VCCQ	—	0.2 ×VCCQ	—	V	
Spike pulse width suppressed by the input filter	t <sub>SP</sub>	—	—	0	50	ns	

- Notes. 1. All values are referenced at VCCQ × 0.3 and VCCQ × 0.7 levels.  
 2. To satisfy the I2C-bus specification, pull-up resistors (R<sub>p</sub>) with the appropriate resistance must be included depending on the total of bus capacitive load of each line.  
 Pull-up resistor range should be following, refer Table 63.19.2.  
 $R_{p(max)} = t_r / (0.8473 \times C_b)$   
 $R_{p(min)} = (VCCQ - V_{OL(max)}) / I_{OL}$   
 3. The total capacity (C<sub>b</sub>) should be less than or equal to 100 pF

**Table 63.19.2 Pull-up Resistor Range of IIC Bus Interface**

Symbol	VCCQ Voltage	Standard-Mode		Fast-Mode		Unit	Remarks
		Min.	Max.	Min.	Max.		
Rp	Vpullup = 1.8 V	517	11802	517	3540	$\Omega$	—
(Cb=100pF)	Vpullup = 3.3 V	1067	11802	1067	3540	$\Omega$	



**Figure 63.19.1 IIC Bus Interface Signal Timing**

## 63.20 MSIOF

**Table 63.20.1 MSIOF Module Signal Timing (RZ/G1H: channels 0, 1 and 3)**
**RZ/G1H**

Conditions: VCCQ = 3.3 V ± 0.3 V, GND = VSS = 0 V, Tc = -40 to +105°C, CL = 30 pF

Item	Symbol	Min.	Max.	Unit	Figures
MSIOF_SCK clock cycle time	tMSCYC	4 × tpcyc*	—	ns	Figures 63.20.1, 63.20.2, 63.20.3, 63.20.4
MSIOF_SCK output clock high-level width	tMSWHO	0.4 × tMSCYC	—	ns	
MSIOF_SCK output clock low-level width	tMSWLO	0.4 × tMSCYC	—	ns	
MSIOF_SCK input high-level width	tMSWHI	0.4 × tMSCYC	—	ns	
MSIOF_SCK input low-level width	tMSWLI	0.4 × tMSCYC	—	ns	
MSIOF_SYNC input setup time in slave mode	tTSFSS	15	—	ns	
MSIOF_SYNC input hold time in slave mode	tTSFSH	8	—	ns	
MSIOF_TXD output delay time1 in slave mode	tTSDD1	0	35	ns	
MSIOF_TXD output delay time2 in slave mode	tTSDD2	0	35	ns	
MSIOF_RXD input setup time in slave mode	tTSRDS	15	—	ns	
MSIOF_RXD input hold time in slave mode	tTSRDH	8	—	ns	
MSIOF_SYNC output delay time in master mode	tTMSFD	-12	25	ns	
MSIOF_TXD output delay time in master mode	tTMDD	-12	25	ns	
MSIOF_RXD input setup time in master mode	tTMRDS	30	—	ns	
MSIOF_RXD input hold time in master mode	tTMRDH	10	—	ns	

Note: \* tpcyc is a cycle time of peripheral clock (MPφ)

**Table 63.20.2 MSIOF Module Signal Timing (RZ/G1H: channel 2 only)**
**RZ/G1H**

Conditions: VCCQ = 3.3 V ± 0.3 V, GND = VSS = 0 V, Tc = -40 to +105°C, CL = 30 pF

Item	Symbol	Min.	Max.	Unit	Figures
MSIOF_SCK clock cycle time	tMSCYC	2 × tpcyc*	—	ns	Figures 63.20.1, 63.20.2, 63.20.3, 63.20.4
MSIOF_SCK output clock high-level width	tMSWHO	0.4 × tMSCYC	—	ns	
MSIOF_SCK output clock low-level width	tMSWLO	0.4 × tMSCYC	—	ns	
MSIOF_SCK input high-level width	tMSWHI	0.4 × tMSCYC	—	ns	
MSIOF_SCK input low-level width	tMSWLI	0.4 × tMSCYC	—	ns	
MSIOF_SYNC input setup time in slave mode	tTSFSS	10	—	ns	
MSIOF_SYNC input hold time in slave mode	tTSFSH	5	—	ns	
MSIOF_TXD output delay time1 in slave mode	tTSDD1	0	30	ns	
MSIOF_TXD output delay time2 in slave mode	tTSDD2	0	30	ns	
MSIOF_RXD input setup time in slave mode	tTSRDS	10	—	ns	
MSIOF_RXD input hold time in slave mode	tTSRDH	5	—	ns	
MSIOF_SYNC output delay time in master mode	tTMSFD	-6	16	ns	
MSIOF_TXD output delay time in master mode	tTMDD	-6	16	ns	
MSIOF_RXD input setup time in master mode	tTMRDS	20	—	ns	
MSIOF_RXD input hold time in master mode	tTMRDH	5	—	ns	

Note: \* tpcyc is a cycle time of peripheral clock (MPφ)

**Table 63.20.3 MSIOF Module Signal Timing (RZ/G1M, N and E)****RZ/G1M****RZ/G1N****RZ/G1E**

Conditions: VCCQ = 3.3 V ± 0.3 V, GND = VSS = 0 V, Tc = -40 to +105°C, CL = 30 pF

Item	Symbol	Min.	Max.	Unit	Figures
MSIOF_SCK clock cycle time	tMSCYC	2 × tpcyc*	—	ns	Figures 63.20.1, 63.20.2, 63.20.3, 63.20.4
MSIOF_SCK output clock high-level width	tMSWHO	0.4 × tMSCYC	—	ns	
MSIOF_SCK output clock low-level width	tMSWLO	0.4 × tMSCYC	—	ns	
MSIOF_SCK input high-level width	tMSWHI	0.4 × tMSCYC	—	ns	
MSIOF_SCK input low-level width	tMSWLI	0.4 × tMSCYC	—	ns	
MSIOF_SYNC input setup time in slave mode	tTSFSS	10	—	ns	
MSIOF_SYNC input hold time in slave mode	tTSFSH	5	—	ns	
MSIOF_TXD output delay time1 in slave mode	tTSDD1	0	30	ns	
MSIOF_TXD output delay time2 in slave mode	tTSDD2	0	30	ns	
MSIOF_RXD input setup time in slave mode	tTSRDS	10	—	ns	
MSIOF_RXD input hold time in slave mode	tTSRDH	5	—	ns	
MSIOF_SYNC output delay time in master mode	tTMSFD	-3	8	ns	
MSIOF_TXD output delay time in master mode	tTMDD	-3	8	ns	
MSIOF_RXD input setup time in master mode	tTMRDS	20	—	ns	
MSIOF_RXD input hold time in master mode	tTMRDH	5	—	ns	

Note: \* tpcyc is a cycle time of peripheral clock (MPφ)

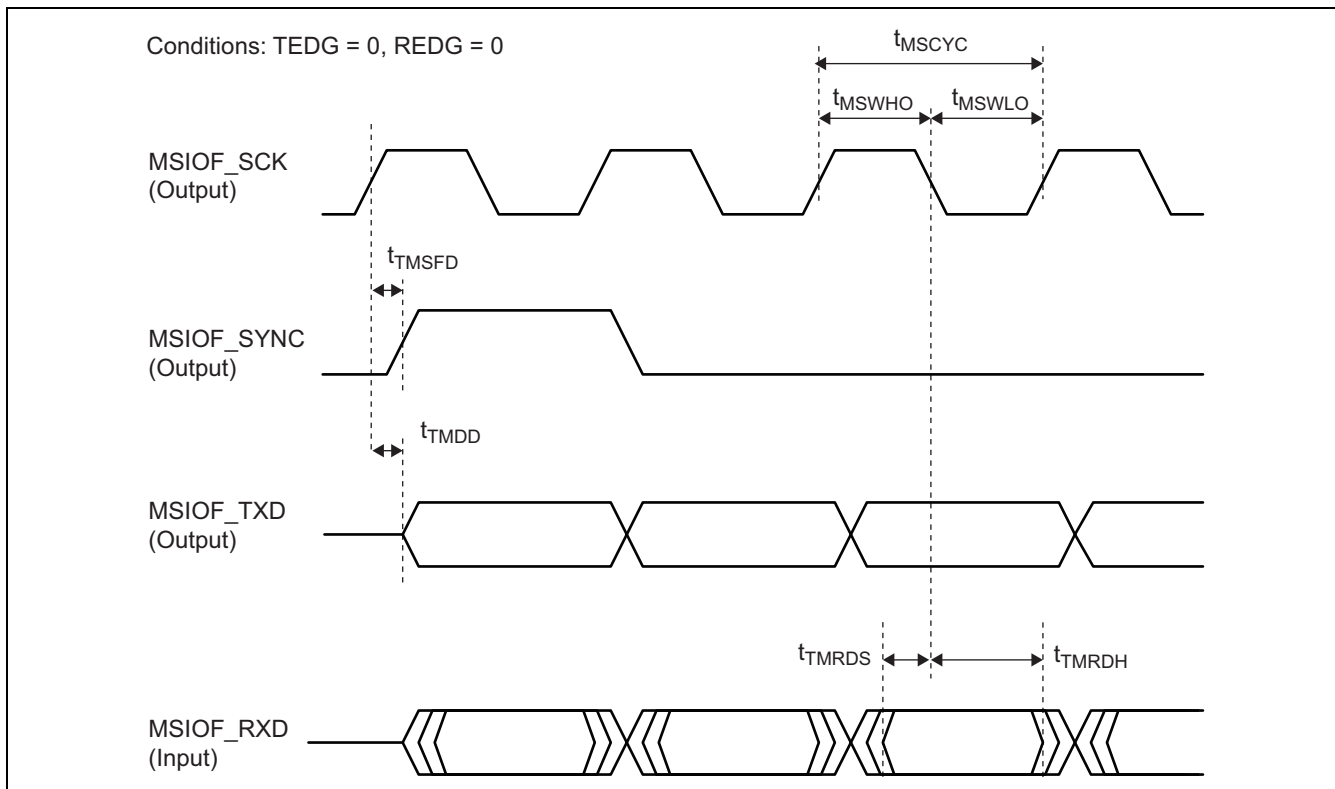


Figure 63.20.1 MSIOF Timing (Master Mode) (TEDG=0, REDG=0)

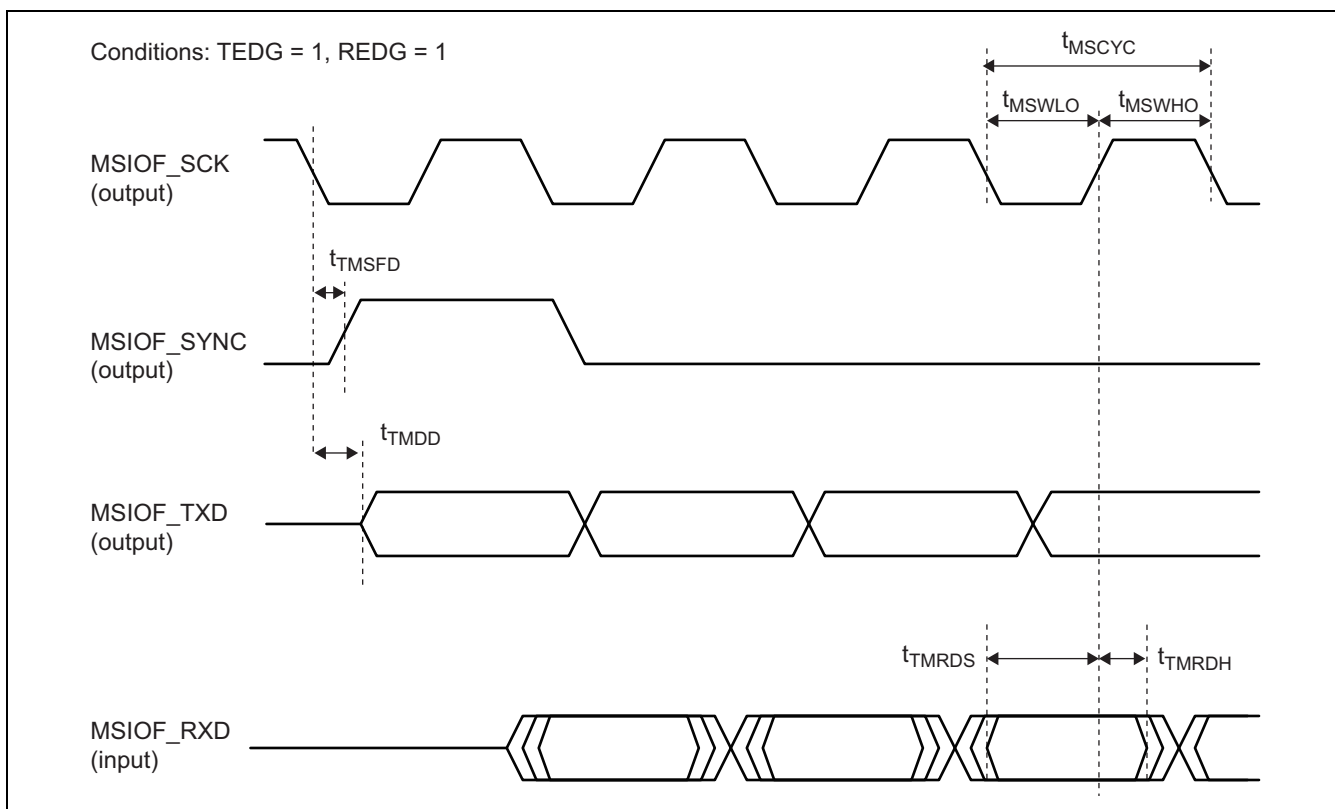


Figure 63.20.2 MSIOF Timing (Master Mode) (TEDG=1, REDG=1)



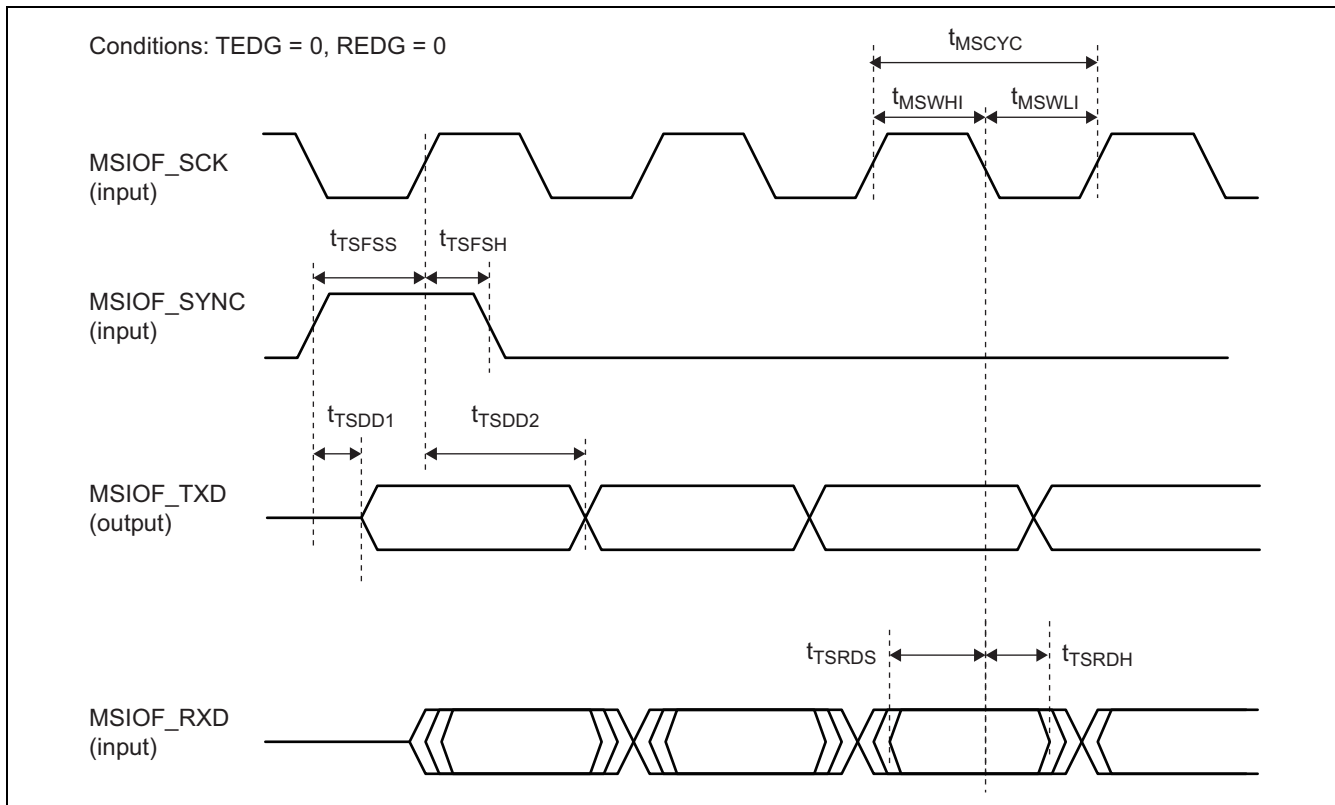


Figure 63.20.3 MSIOF Timing (Slave Mode) (TEDG=0, REDG=0)

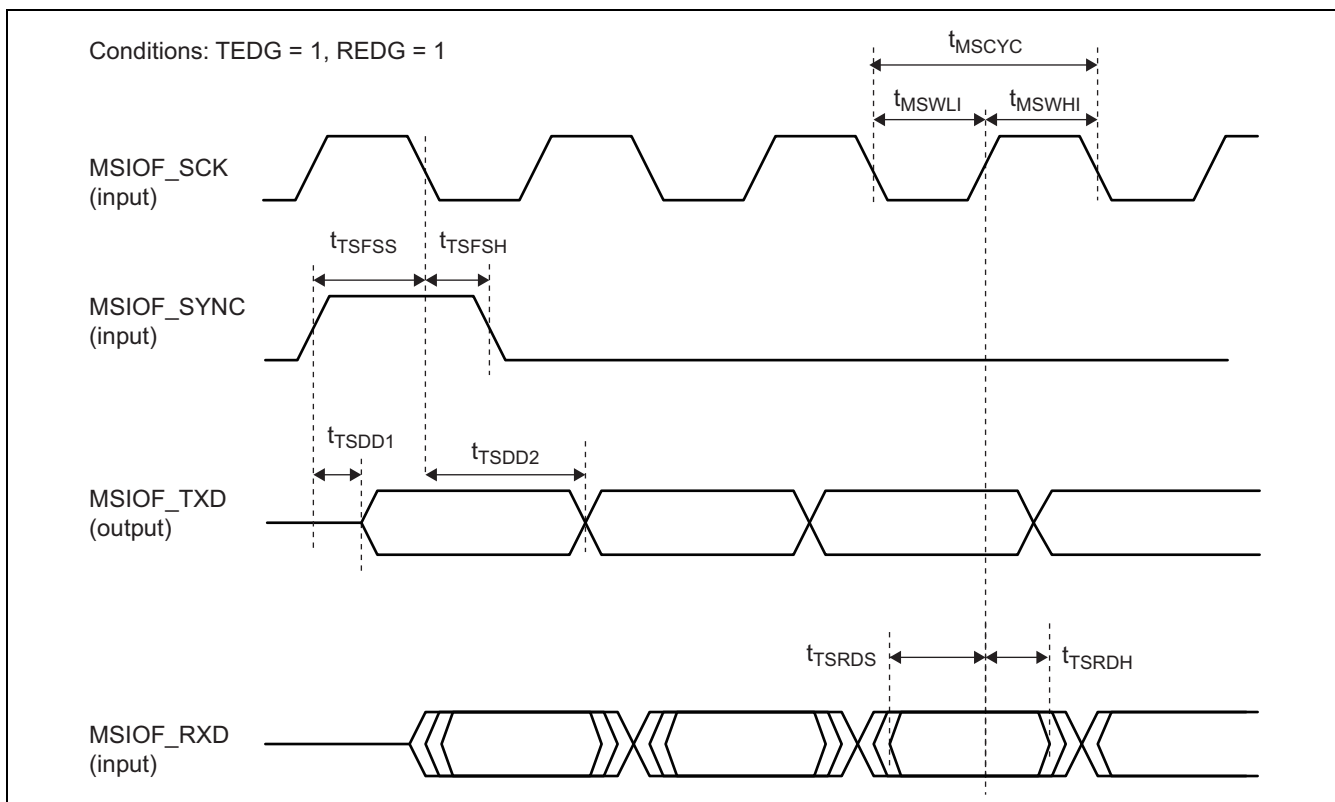


Figure 63.20.4 MSIOF Timing (Slave Mode) (TEDG=1, REDG=1)

## 63.21 QSPI

**Table 63.21.1 QSPI Signal Timing (RZ/G1H)**
**RZ/G1H**

Conditions: VCCQ = 3.3 V ± 0.3 V, GND = VSS = 0 V, Tc = -40 to +105°C, CL = 30 pF

Item	Symbol	Min.	Typ.	Max.	Unit	Figures
QSPICLK clock cycle	tQScyc	1	—	4080	Tcyc	Figures 63.21.1 to 63.21.3
Data input setup time	tSU	4.8	—	—	ns	
Data input hold time	tH	0.0	—	—	ns	
SSL setup time	tLEAD	1 to 8	—	—	tQScyc	
SSL hold time	tLAG	0.5 to 7.5	—	—	tQScyc	
Data output delay time	tOD	—	—	3.05	ns	
Data output hold time	tOH	-1.4	—	—	ns	
Continuous transfer delay time	tTD	1	—	8	tQScyc	

 Note: Tcyc is a cycle time of QSPI clock (QSPI $\phi$ ).

**Table 63.21.2 QSPI Signal Timing (RZ/G1M, N and E)**
**RZ/G1M**
**RZ/G1N**
**RZ/G1E**

Conditions: VCCQ = VCCQ\_SDn = 3.3 V ± 0.3 V, GND = VSS = 0 V, Tc = -40 to +105°C, CL = 30 pF

Item	Symbol	Min.	Typ.	Max.	Unit	Figures
QSPICLK clock cycle	tQScyc	1	—	4080	Tcyc	Figures 63.21.1 to 63.21.3
Data input setup time	tSU	4.8	—	—	ns	
Data input hold time	tH	0.0	—	—	ns	
SSL setup time	tLEAD	1 to 8	—	—	tQScyc	
SSL hold time	tLAG	0.5 to 7.5	—	—	tQScyc	
Data output delay time	tOD	—	—	3.05	ns	
Data output hold time	tOH	-3.0* <sup>1</sup> -1.4* <sup>2</sup>	—	—	ns	
Continuous transfer delay time	tTD	1	—	8	tQScyc	

 Notes: Tcyc is a cycle time of QSPI clock (QSPI $\phi$ ).

1. For RZ/G1M only.
2. For RZ/G1N and E.

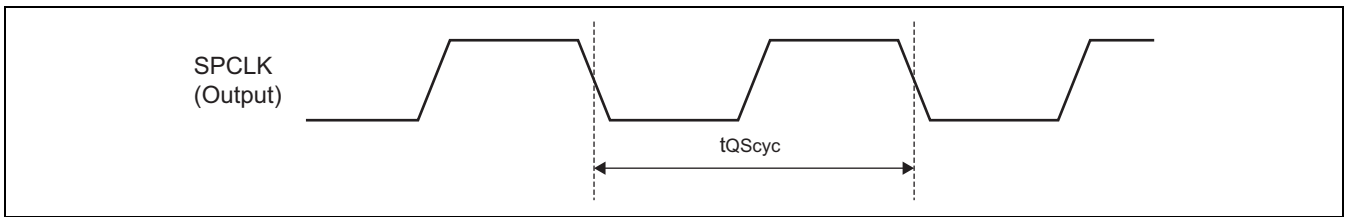


Figure 63.21.1 Clock Timing

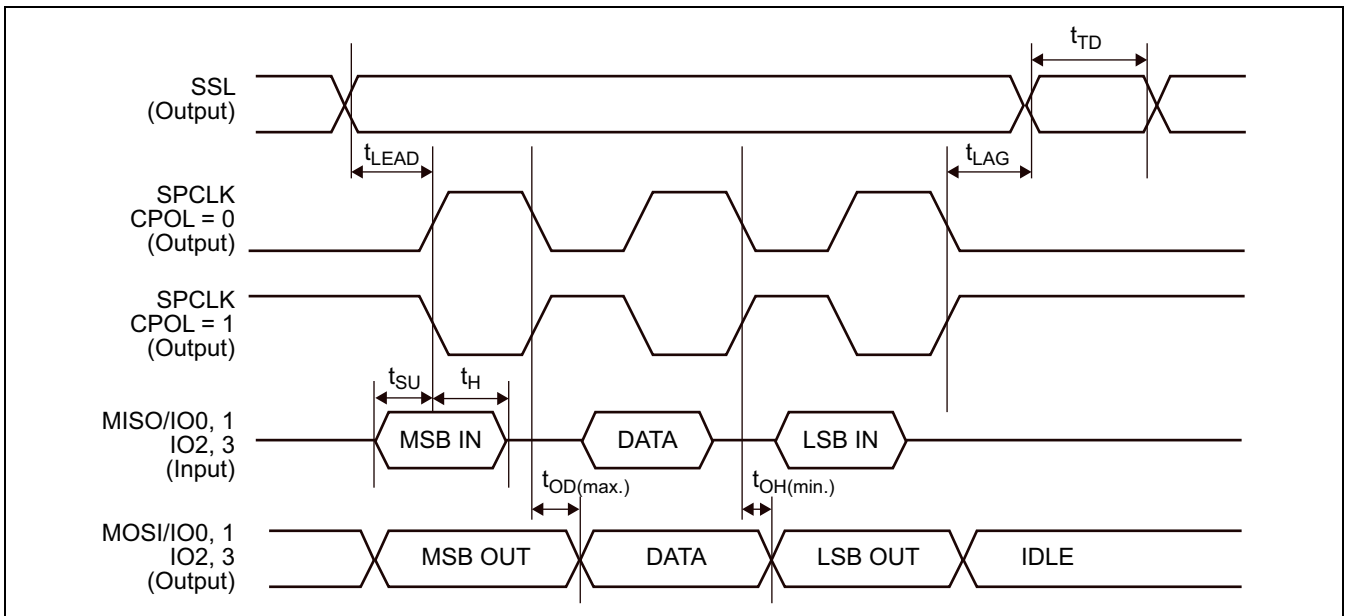


Figure 63.21.2 Sending and Receiving Timing (CPHA=0)

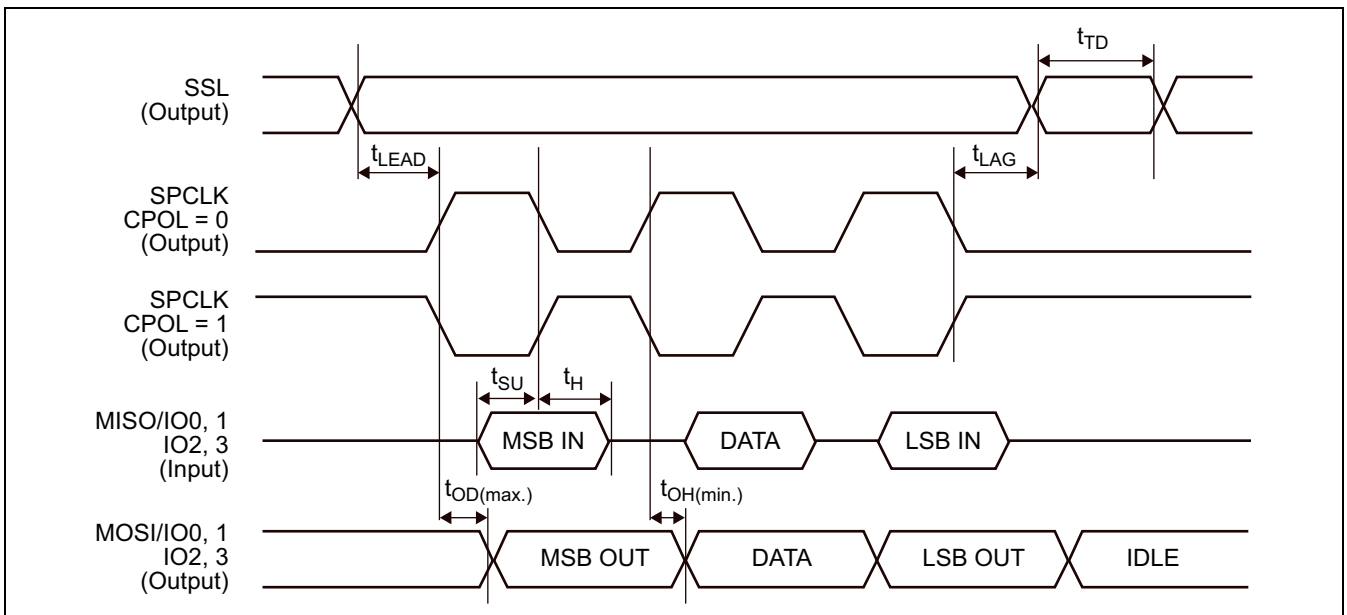


Figure 63.21.3 Sending and Receiving Timing (CPHA=1)

## 63.22 MMC Signal Timing

<b>RZ/G1H</b>	<b>RZ/G1N</b>
<b>RZ/G1M</b>	<b>RZ/G1E</b>

**Table 63.22.1 MMC Signal Timing (RZ/G1H, M, N and E)**

Conditions: VCCQ = VCCQ\_SDn/VCCQ\_MMC\_SD2 = 3.3 ± 0.3 V, GND = VSS = 0 V, Tc = -40 to +105°C, CL = 30 pF

Item		Symbol	Min.	Max.	Unit	Figure
MMC_CLK clock cycle		t <sub>MMCCYC</sub>	2 × t <sub>MMCφ</sub>	—	ns	Figure 63.22.1
MMC_CMD output data delay time		t <sub>MMCCMD</sub>	—	t <sub>MMCCYC</sub> × 1/2 + 1	ns	
MMC_CMD output data hold time		t <sub>MMCCMDH</sub>	4	—	ns	
MMC_D output data delay time 1	H, E: all MMC data pins	t <sub>MMCDADD1</sub>	—	t <sub>MMCCYC</sub> × 3/4 + 1	ns	
	M, N: MMC_D[5:0] pins and MMC_D[7:6]_B pins			t <sub>MMCCYC</sub> × 3/4 + 1	ns	
	MMC_D[7:6] pins			t <sub>MMCCYC</sub> × 3/4 + 3	ns	
MMC_D output data delay time 2*	H, E: all MMC data pins	t <sub>MMCDADD2</sub>	—	t <sub>MMCCYC</sub> × 1/2 + 1	ns	
	M, N: MMC_D[5:0] pins and MMC_D[7:6]_B pins			t <sub>MMCCYC</sub> × 1/2 + 1	ns	
	MMC_D[7:6] pins			t <sub>MMCCYC</sub> × 1/2 + 3	ns	
MMC_D output data hold time		t <sub>MMCDADH</sub>	4	—	ns	
MMC_CMD input data setup time		t <sub>MMCCMS</sub>	4	—	ns	
MMC_CMD input data hold time		t <sub>MMCCMH</sub>	2	—	ns	
MMC_D input data setup time		t <sub>MMCDAS</sub>	4	—	ns	
MMC_D input data hold time		t <sub>MMCDAH</sub>	2	—	ns	

Notes: t<sub>MMCφ</sub> is for one cycle of MMCxφ.

\* Set 1 to the ODTS bit of CE\_ODATSEL (data output phase select register) for this specification.

### Limitation of Transfer Performance for MMC

When the MMC module of the RZ/G series products operates with all of the following condition 1 to 3, the transfer performance of the MMC interface is limited up to 35 MB/s at MMC\_CLK = 48.75 MHz by the internal latency.

#### Condition

- 1) MMC transfer data size is over 1024 bytes.
- 2) MMC dedicated RAM (1024 bytes) all data has been transferred.
- 3) MMC continues data transfer after 1024 bytes of dedicated RAM data transferred.

The MMC\_CLK stops by each 512 bytes transfer. If this becomes a problem for the external device, set the MMC\_CLK frequency less than 35.45 MHz (i.e., 35.45 MB/s) by CE\_CLK\_CTRL.CLKDIV [3:0].

For details, refer to section 49.4.2, Limitation of Transfer Performance.

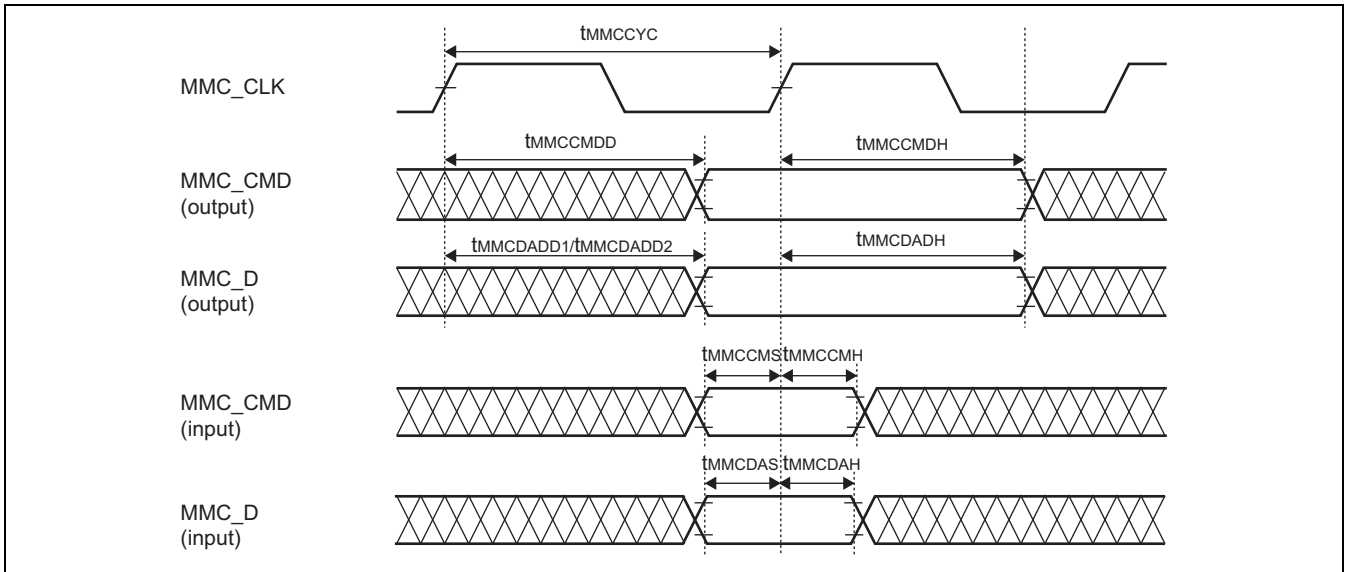


Figure 63.22.1 MMC Signal Timing

## 63.23 Serial ATA (Gen2)

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

The description in this section is compliant with the following Serial ATA standard:  
'Serial ATA International Organization: Serial ATA Revision 3.1, July 18, 2011'.

**Table 63.23.1 Serial ATA (Gen2) Interface Characteristics (RZ/G1H, M and N)**

Conditions: VDDA\_SATA0/1 = 1.8 V, VDDD\_SATA0/1 = 1.03 V, VSS\_SATA0/1 = GND = 0 V, Tc = -40 to +105°C

Test Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
RX Differential Input Voltage (Gen1i)	Vdiff RX	325	—	600	mVppd	*1
RX Differential Input Voltage (Gen2i)	Vdiff RX	275	—	750	mVppd	*1
TX Differential Output Voltage (Gen1i)	Vdiff TX	400	—	600	mVppd	*2
TX Differential Output Voltage (Gen2i)	Vdiff TX	400	—	700	mVppd	*2
DC Coupled Common Mode Voltage (Gen1i)	Vcm dc	200	—	450	mV	*2
Unit Interval (Gen1i)	TUI	666.4333	666.6667	670.2333	ps	*3
Unit Interval (Gen2i)	TUI	333.2167	333.3333	335.1167	ps	*3
COMRESET Transmit Gap Length (Gen1i and Gen2i)	TScmreset	—	480	—	UIOOB	*4
COMWAKE Transmit Gap Length (Gen1i and Gen2i)	TScmwake	—	160	—	UIOOB	*4
TX Differential Impedance (Gen1i)	ZdiffTX	85	—	115	Ω	*2
TX Single-Ended Impedance (Gen1i)	Zs-eTX	40	—	—	Ω	*2
RX Differential Impedance (Gen1i)	ZdiffRX	85	—	115	Ω	*1
RX Single-Ended Impedance (Gen1i)	Zs-eRX	40	—	—	Ω	*1

Notes: \*1. RXP, RXN: DC test

\*2. TXP, TXN: DC test

\*3. Need Reference Clock (Low Voltage Swing, Differential Clocks). The nominal single-ended swing for each clock is 0 to 0.7 V and a nominal frequency of 100 MHz ±100 PPM.

\*4. TXP, TXN: UIOOB (UI During OOB Signaling) = 646.67 to 686.67ps, Not tested.

## 63.24 USB Signal Timing

RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

**Table 63.24.1 USB High-speed Signal Timing**

Conditions: VCCQ = VD331 = 3.3 V ± 0.3 V, AVDD = VD181 = 1.8 V ± 0.1 V, GND = VSS = 0 V,  
Tc = -40 to +105°C

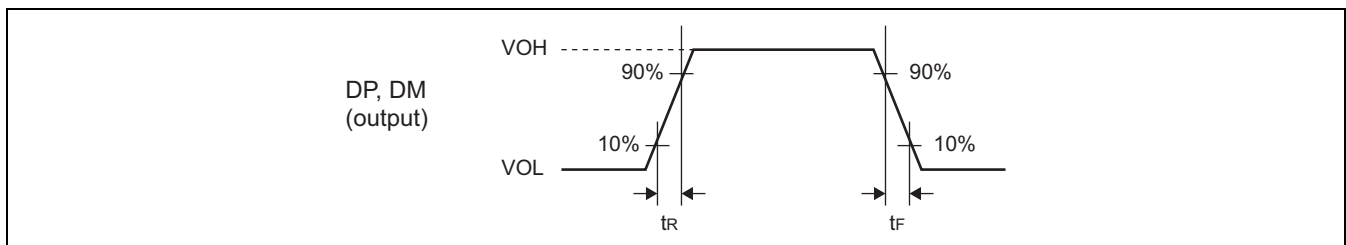
Item	Symbol	Min.	Typ.	Max.	Unit	Figure
High-speed data rate	T <sub>HSDRAT</sub>	479.76	480	480.24	Mb/s	—

**Table 63.24.2 USB Low-/full-speed Signal Timing**

Conditions: VCCQ = VD331 = 3.3 V ± 0.3 V, AVDD = VD181 = 1.8 V ± 0.1 V, GND = VSS = 0 V,  
Tc = -40 to +105°C, CL = 50 pF

Item	Symbol	Min.	Typ.	Max.	Unit	Figure	
Low-speed*	Rise time	t <sub>R</sub>	75	—	300	ns	Figure 63.24.1
	Fall time	t <sub>F</sub>	75	—	300	ns	
	Differential Rise and Fall Time Matching (t <sub>R</sub> /t <sub>F</sub> )	t <sub>RFM</sub>	80	—	125	%	
Full-speed	Rise time	t <sub>R</sub>	4	—	20	ns	
	Fall time	t <sub>F</sub>	4	—	20	ns	
	Differential Rise and Fall Time Matching (t <sub>R</sub> /t <sub>F</sub> )	t <sub>RFM</sub>	90	—	111.11	%	

Note: \* The USB 2.0 Function module does not support Low-speed.



**Figure 63.24.1 USB Low-/Full-Speed Signal Timing**

**Table 63.24.3 USB 2.0 External Clock Accuracy**

Conditions: VCCQ = VD331 = 3.3 V ± 0.3 V, AVDD = VD181 = 1.8 V ± 0.1 V, GND = VSS = 0 V,  
Tc = -40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
External clock accuracy (USBCLK)	—	—	48.000	—	MHz	Frequency deviation: ±100 ppm or less

**63.25 USB 3.0 (Super-Speed)****RZ/G1H****RZ/G1N****RZ/G1M****RZ/G1E**

The description in this section is compliant with the following USB 3.0 standard:  
'Universal Serial Bus 3.0 Specification Revision 1.0, Jun 6, 2011'.

**Table 63.25.1 USB 3.0 (Super-Speed 5GT/s) Interface Characteristics (RZ/G1H, M and N)**

Conditions: VDDA\_SATA0 (VDDA\_USB3) = 1.8 V, VDDD\_SATA0 (VDDD\_USB3) = 1.03 V,  
VSS\_SATA0 (VSS\_USB3) = GND = 0 V, T<sub>c</sub> = -40 to +105°C

Test Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Differential Rx peak to peak voltage	V <sub>RX-DIFFp-p</sub>	0.030	—	—	V	*1
Differential p-p Tx voltage swing	V <sub>TX-DIFFp-p</sub>	0.8	—	1.2	V	*2
Absolute DC Common Mode Voltage between U1 and U0	V <sub>TX-CM-DC- ACTIVEIDLE- DELTA</sub>	—	—	200	mV	*2
Unit Interval	UI	199.94	—	200.06	ps	*3
DC Differential TX Impedance	R <sub>TX-DIFF-DC</sub>	72	—	120	Ω	—
DC Differential Input Impedance	R <sub>RX-DIFF-DC</sub>	72	—	120	Ω	—
DC Input Impedance {DC common mode impedance}	Z <sub>RX-DC</sub> {R <sub>TX-DC</sub> ,R <sub>RX-DC</sub> }	36 {18}	— {-}	60 {30}	Ω {Ω}	—

Notes: \*1. RXP, RXN: DC test

\*2. TXP, TXN: DC test

\*3. Need Reference Clock (Low Voltage Swing, Differential Clocks). The nominal single-ended swing for each clock is 0 to 0.7 V and a nominal frequency of 100 MHz ±100 PPM.



**63.26 TMU**

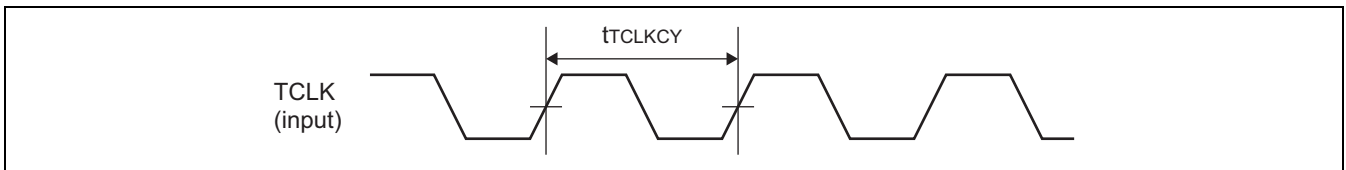
<b>RZ/G1H</b>	<b>RZ/G1N</b>
<b>RZ/G1M</b>	<b>RZ/G1E</b>

**Table 63.26.1 TMU Signal Timing**

Conditions: VCCQ/VDDQ = 3.3 ± 0.3 V, GND = VSS = 0 V, Tc = -40 to +105 °C

Item	Symbol	Min.	Typ.	Max.	Unit	Figure
TCLK clock cycle	tTCLKCY	4	—	16.37	tCYC	Figure 63.26.1

Note: tCYC is for one cycle of the Pφ clock.



**Figure 63.26.1 TMU Signal Timing**

<b>RZ/G1H</b>	<b>RZ/G1N</b>
<b>RZ/G1M</b>	<b>RZ/G1E</b>

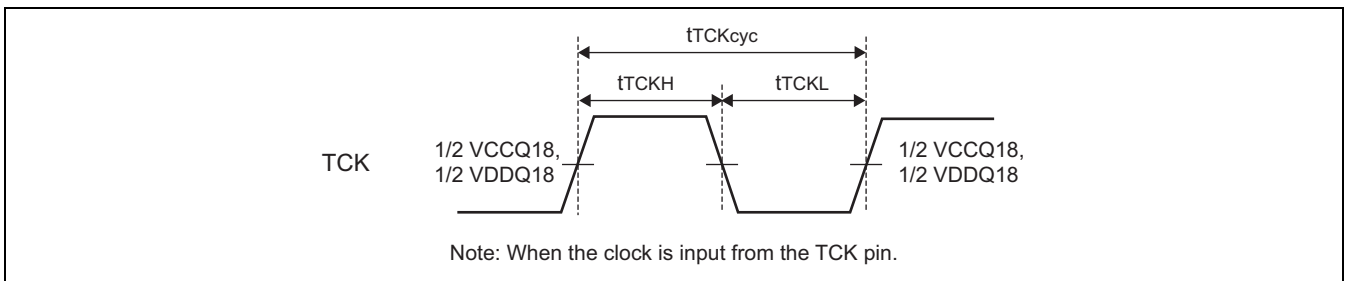
### 63.27 CoreSight

**Table 63.27.1 JTAG Interface Signal Timing**

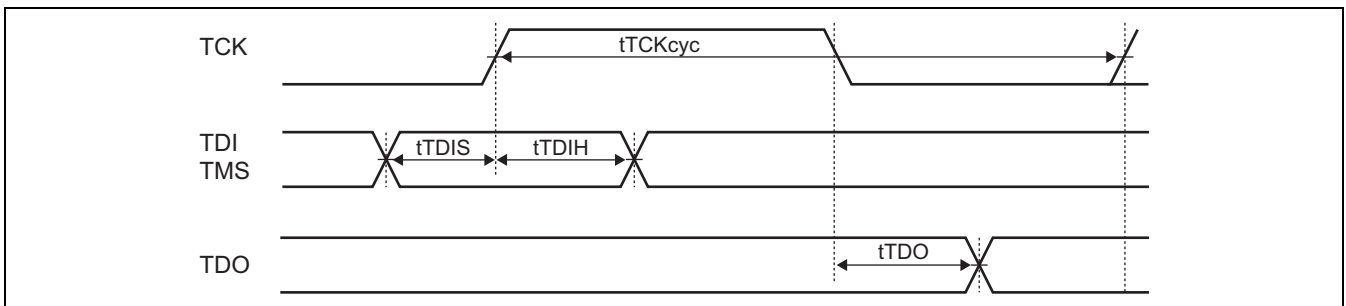
Conditions: VCCQ18/VDDQ18 = 1.8 V ± 0.1 V, GND = VSS = 0 V, Tc = -40 to +105 °C, CL = 30 pF

Item	Symbol	Min.	Typ.	Max.	Unit	Figures
TCK Input clock cycle	tTCKcyc	50*	—	—	ns	Figure 63.27.1
TCK Input clock pulse width (high level)	tTCKH	20	—	—	ns	
TCK Input clock pulse width (low level)	tTCKL	20	—	—	ns	
TDI/TMS setup time	tDIS	15	—	—	ns	Figure 63.27.2
TDI/TMS hold time	tDIH	15	—	—	ns	
TDO output delay time	tDO	0	—	14	ns	

Note: \* The cycle is 500 ns (2 MHz) during boundary scan operation.



**Figure 63.27.1 TCK Input Timing**



**Figure 63.27.2 Data Transfer Timing**

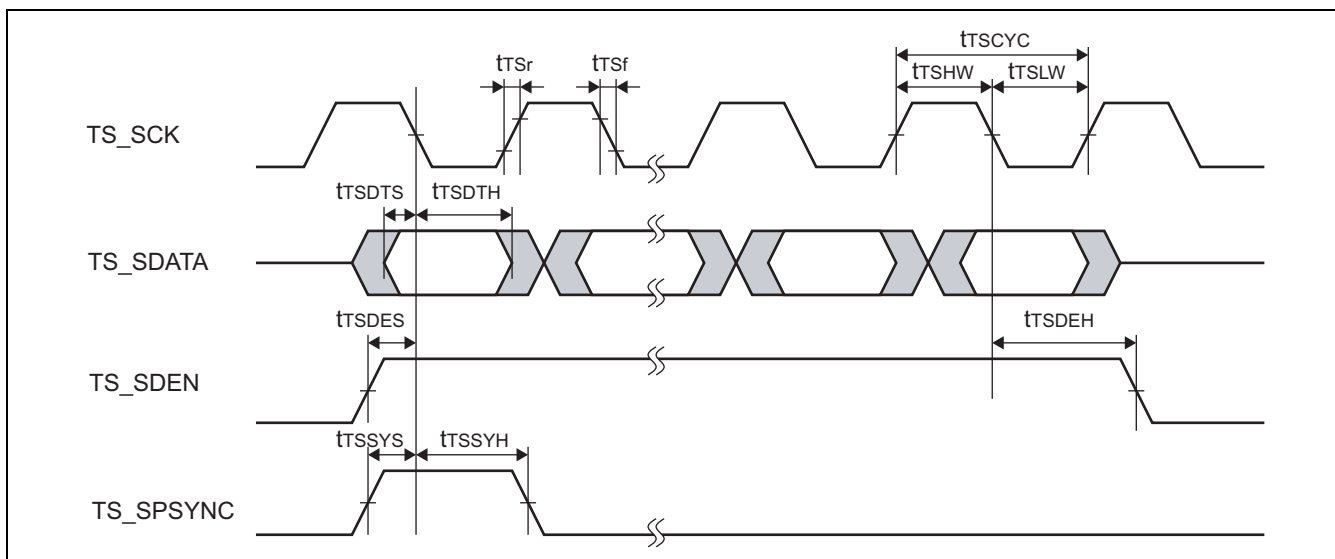
### 63.28 TS Interface (TSIF)

**RZ/G1M**

**Table 63.28.1 TSIF Signal Timing (RZ/G1M)**

Conditions: VCCQ = VCCQ\_SDn = 3.3 V ± 0.3 V, GND = VSS = 0 V, Tc = -40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Figure
TSIF input clock cycle	tTSCYC	15	—	—	ns	Figure 63.28.1
TSIF input clock rise time (from VIL to VIH)	tTSr	—	—	3	ns	
TSIF input clock fall time (from VIH to VIL)	tTSf	—	—	3	ns	
TSIF input clock high-level width	tTSHW	0.4×tTSCYC	—	—	ns	
TSIF input clock low-level width	tTSLW	0.4×tTSCYC	—	—	ns	
TSIF input data setup time	tTSDTS	5	—	—	ns	
TSIF input data hold time	tTSDTH	5	—	—	ns	
TSIF input data enable signal setup time	tTSDES	5	—	—	ns	
TSIF input data enable signal hold time	tTSDEH	5	—	—	ns	
TSIF input data sync signal setup time	tTSSYS	5	—	—	ns	
TSIF input data sync signal hold time	tTSSYH	5	—	—	ns	



**Figure 63.28.1 TSIF Module Signal Timing**  
 (TSCTLR.TSDATP=0, TSCTLR.TSCLKP=1, TSCTLR.TSVLDP=0, TSCTLR.PSYCP=0)

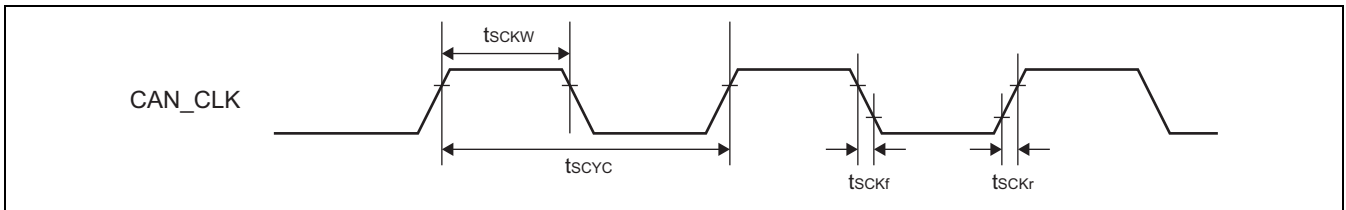
**63.29 CAN**

<b>RZ/G1H</b>	<b>RZ/G1N</b>
<b>RZ/G1M</b>	<b>RZ/G1E</b>

**Table 63.29.1 CAN Signal Timing**

Conditions: VCCQ/VDDQ = VCCQ\_SDn = 3.3 ± 0.3 V, GND = VSS = 0 V, Tc = -40 to +105 °C

Item	Symbol	Min.	Typ.	Max.	Unit	Figure
Input clock cycle (asynchronous)	tSCYC	20	—	—	ns	Figure 63.29.1
Input clock pulse width	tSCKW	0.4	—	0.6	tSCYC	
Input clock rise time	tSCKr	—	—	0.2	tCYC	
Input clock fall time	tSCKf	—	—	0.2	tCYC	



**Figure 63.29.1 Input Clock Timing**

## 63.30 AC Characteristics Test Circuit

### 63.30.1 Single-Ended Push-Pull Output

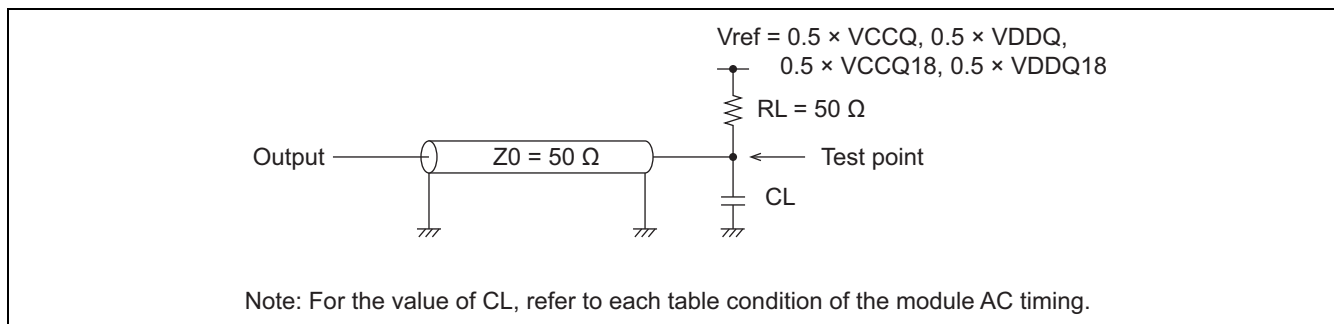
RZ/G1H

RZ/G1N

RZ/G1M

RZ/G1E

3.3 V and 1.8 V single-ended push-pull output test circuit.



**Figure 63.30.1 AC Output Load Equivalent Circuit (VCCQ/VDDQ, VCCQ18/VDDQ18, VCCQ\_SD)**

### 63.30.2 Single-Ended I2C/IIC LVTTL and Open-Drain Output

RZ/G1H

RZ/G1N

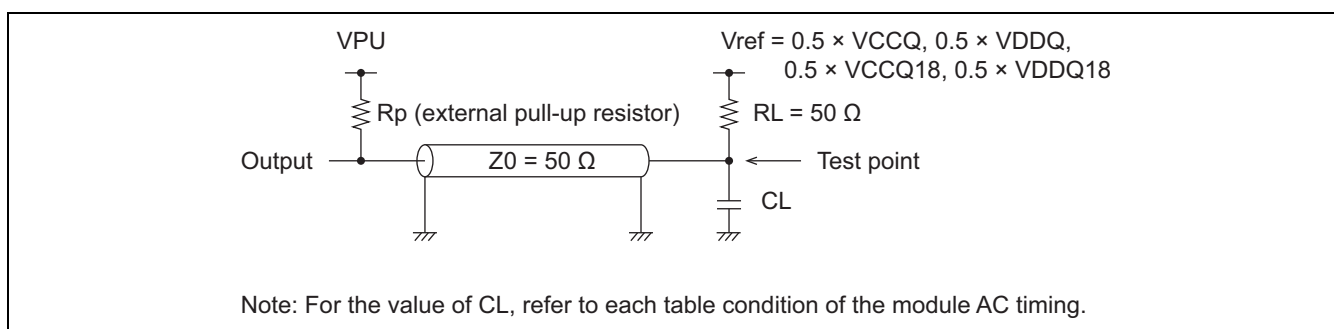
RZ/G1M

RZ/G1E

3.3V and 1.8 V single-ended I2C/IIC LVTTL\* and open-drain output test circuit.  
(3.3 V tolerant)

Note: \* The LVTTL output of the I2C and IIC modules drives low-level only.

When using 1.8V I2C/IIC pins (OD assigned channel) as 3.3 V tolerant, all the external pull-up voltage (VPU) power supply to the I2C/IIC of this LSI must keep the same power on/off sequence as the VCCQ, VDDQ (3.3 V) of this LSI.

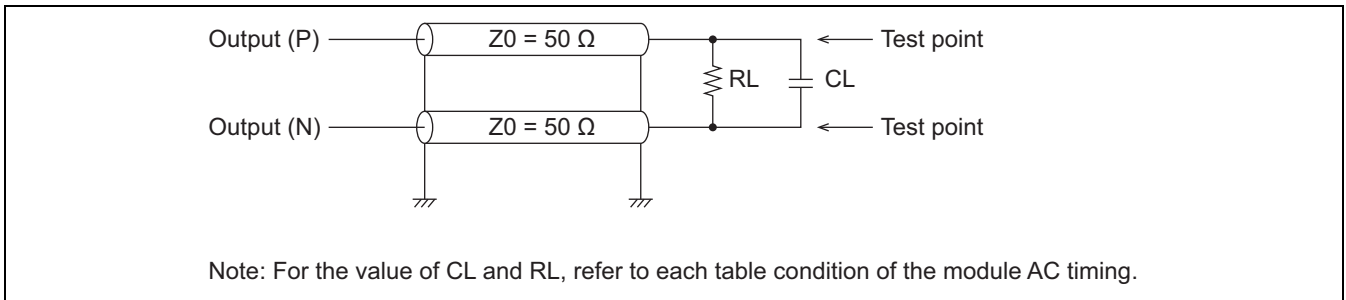


**Figure 63.30.2 AC Output Load Equivalent Circuit (VCCQ, VDDQ, VCCQ18, VDDQ18)**

**63.30.3 Differential Output (LVDS)**

<b>RZ/G1H</b>	<b>RZ/G1N</b>
<b>RZ/G1M</b>	RZ/G1E

1.8 V and 3.3 V differential output test circuit.



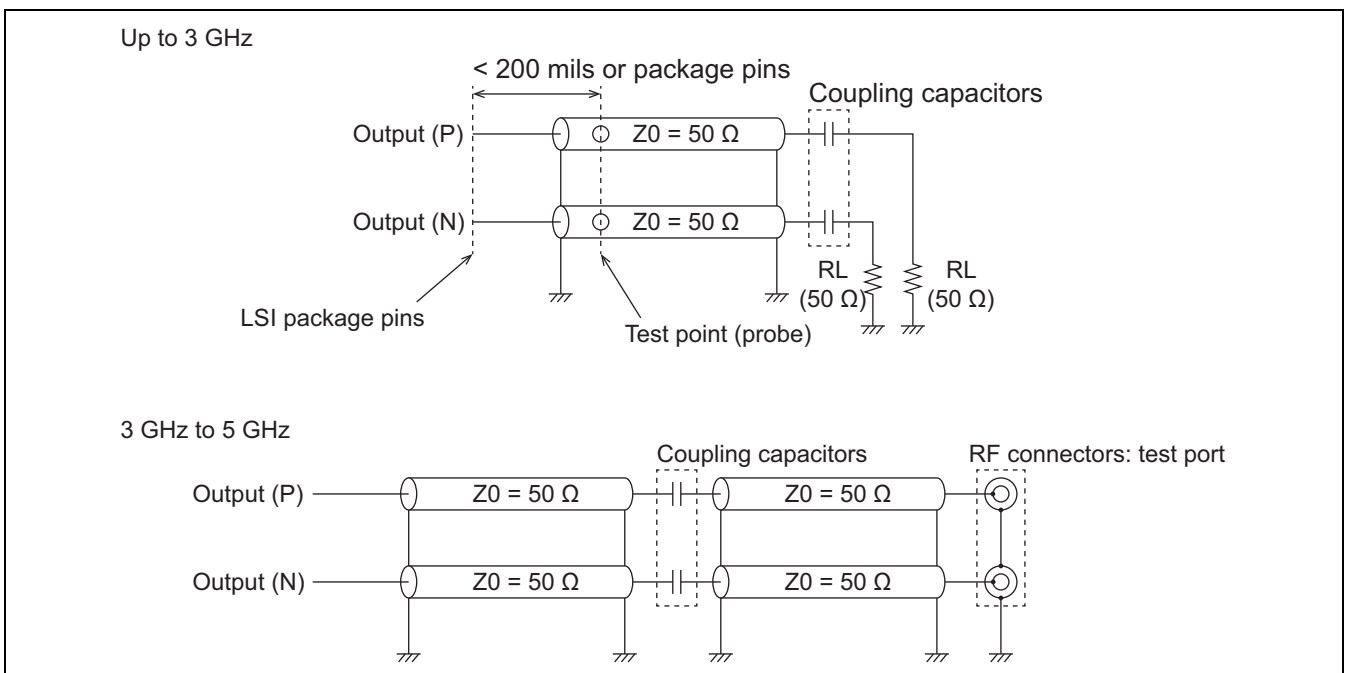
**Figure 63.30.3 AC Output Load Equivalent Circuit (VDDQ\_LVDS, VCCQ33\_MLBP)**

**63.30.4 Differential Output (SATA, PCI Express, USB 3.0)**

<b>RZ/G1H</b>	<b>RZ/G1N</b>
<b>RZ/G1M</b>	RZ/G1E

1.0 V differential output test circuit.

Since the auto-tester uses socket-adaptor for LSI test in mass-production line, following circuits are for evaluation and reference only.

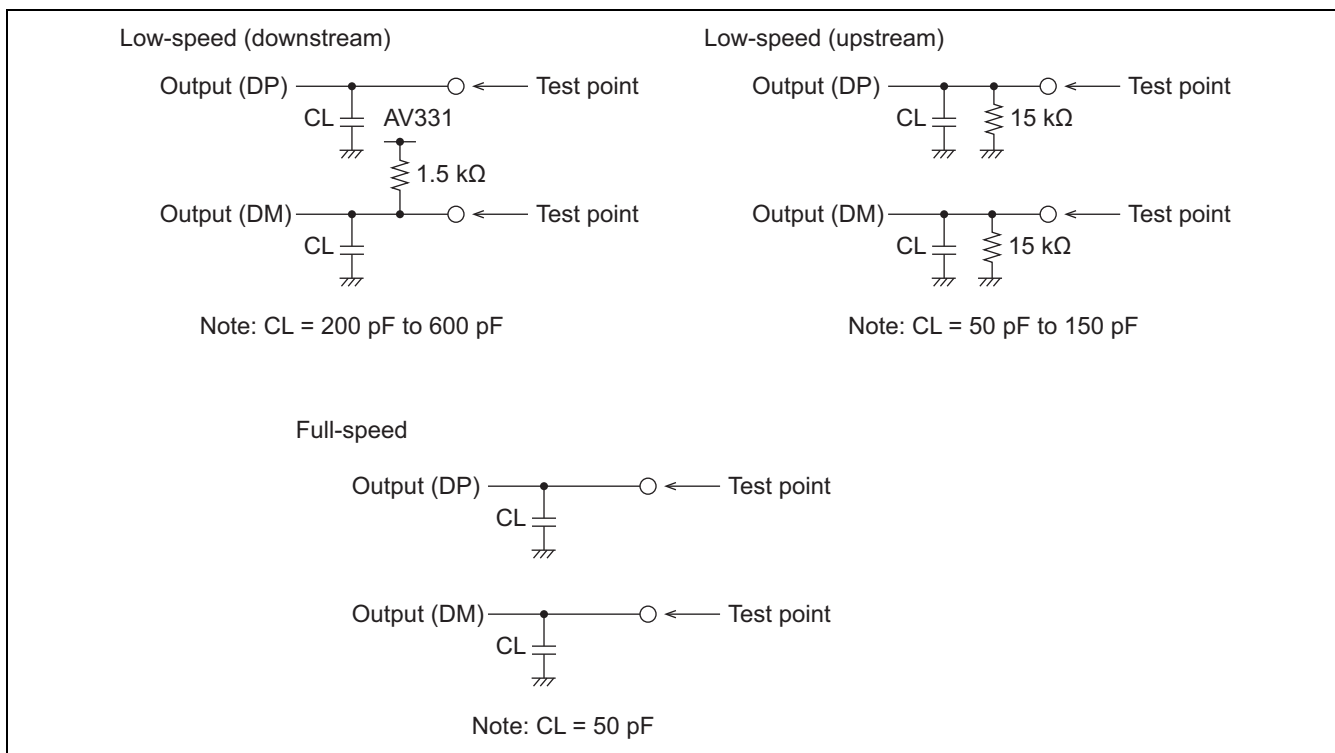


**Figure 63.30.4 AC Output Load Equivalent Circuit (VDDA\_SATA (SATA, PCIEC, USB 3.0))**

**63.30.5 Differential Output USB 2.0 Low-Speed and Full-Speed**

<b>RZ/G1H</b>	<b>RZ/G1N</b>
<b>RZ/G1M</b>	<b>RZ/G1E</b>

3.3 V differential output test circuit (USB 2.0 Low-speed and Full-speed).

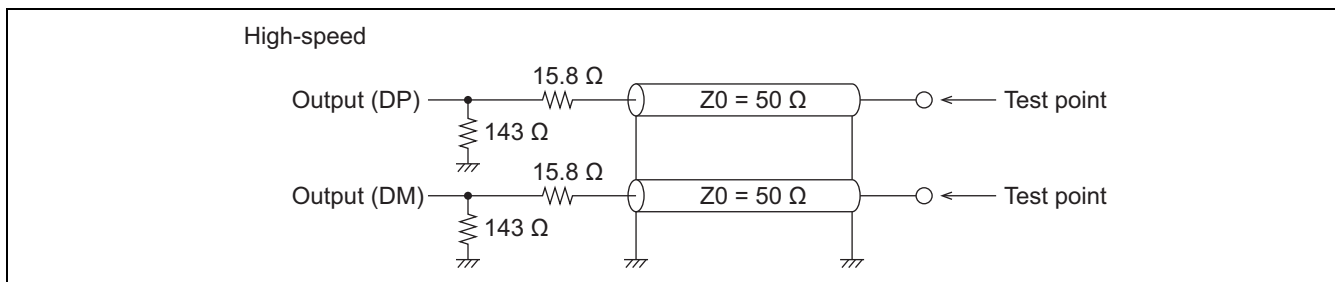


**Figure 63.30.5 AC Output Load Equivalent Circuit (AVDD)**

**63.30.6 Differential Output USB 2.0 High-Speed**

<b>RZ/G1H</b>	<b>RZ/G1N</b>
<b>RZ/G1M</b>	<b>RZ/G1E</b>

3.3 V differential output test circuit (USB 2.0 High-speed).



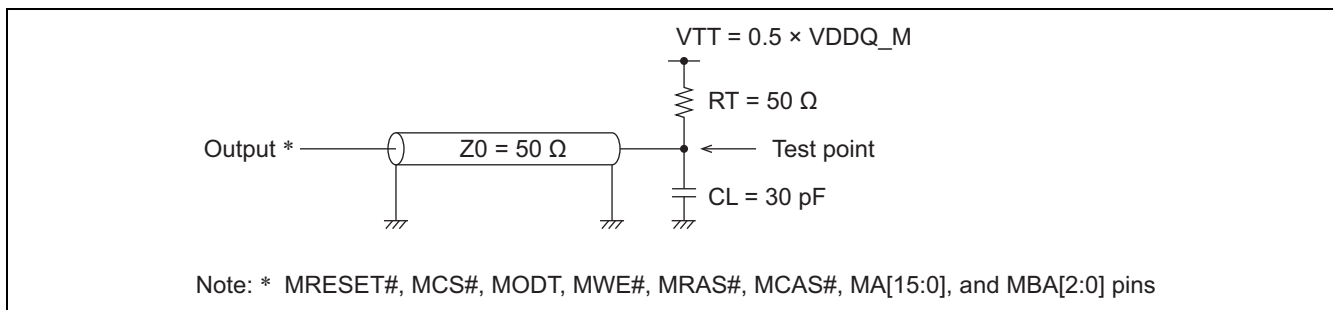
**Figure 63.30.6 AC Output Load Equivalent Circuit (AVDD)**

**63.30.7 SSTL Single-Ended Output (DDR3 Interface)**

<b>RZ/G1H</b>	<b>RZ/G1N</b>
<b>RZ/G1M</b>	<b>RZ/G1E</b>

1.5 V and 1.35 V\* single ended output test circuit (address and control signal).

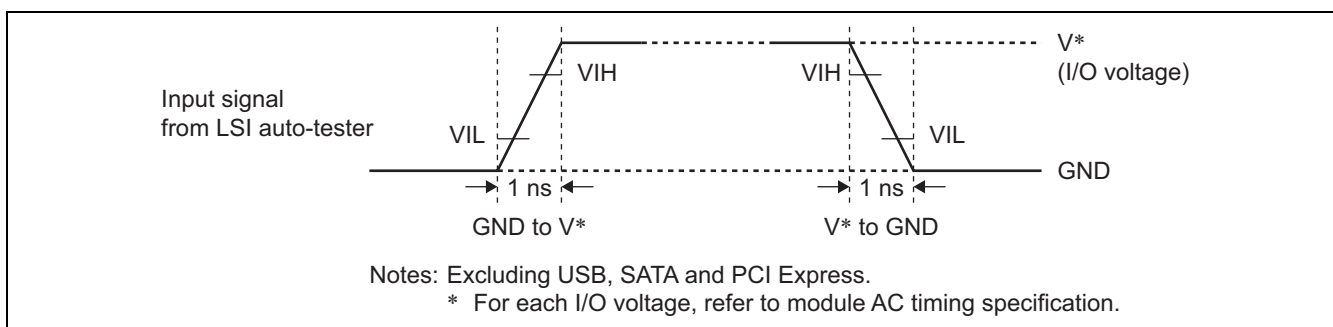
Note: \* 1.5V (DDR3) is available for the RZ/G1H, E.  
 1.35 V (DDR3L) is available for the RZ/G1M, N.



**Figure 63.30.7 AC Output Load Equivalent Circuit (VDDQ\_M)**

**63.30.8 AC Test Input Signal Wave Form**

<b>RZ/G1H</b>	<b>RZ/G1N</b>
<b>RZ/G1M</b>	<b>RZ/G1E</b>



**Figure 63.30.8 AC Test Input Signal Wave Form**



# Appendix A. Product Register (PRR)

RZ/G1H	RZ/G1N
RZ/G1M	RZ/G1E

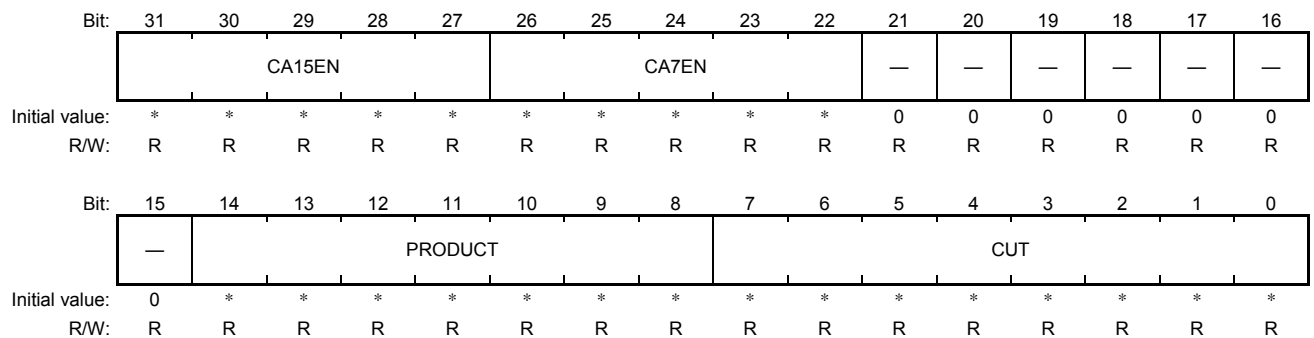
## A.1 Overview

PRR indicates the product version and which of the ARM Cortex cores is present.

## A.2 Register Descriptions

The following describes the details of the product register (PRR).

Register Name	Abbreviation	R/W	Address	Initial Value (Power-On Reset by PRESET# Pin)	Initial Value (Software Reset)	Access Size	RZ/G Series Products			
							RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Product register	PRR	R	H'FF00 0044	*	*	32 bits	√	√	√	√



Note: \* The settings of these bits are explained overleaf. Except in the RZ/G1E, where bits 31 to 27 are fixed, and the RZ/G1M, and N, where bits 26 to 22 are fixed, they depend on the product and the configuration you have ordered. Bits for processors that are never present in a given product are read as 1.

Bit	Bit Name	Initial Value	R/W	Description
31 to 27	CA15EN	It depends on the product. See the description.	R	<p>Cortex-A15 CPU State</p> <p>[RZ/G1H]</p> <p>Bit 31 Cortex-A15 State</p> <p>0: The product has four Cortex-A15 CPUs. 1: The product does not have four Cortex-A15 CPUs.</p> <p>Bit 30 Cortex-A15 CPU3 State</p> <p>0: The product has Cortex-A15 CPU3. 1: The product does not have Cortex-A15 CPU3.</p> <p>Bit 29 Cortex-A15 CPU2 State</p> <p>0: The product has Cortex-A15 CPU2. 1: The product does not have Cortex-A15 CPU2.</p> <p>Bit 28 Cortex-A15 CPU1 State</p> <p>0: The product has Cortex-A15 CPU1. 1: The product does not have Cortex-A15 CPU1.</p> <p>Bit 27 Cortex-A15 CPU0 State</p> <p>0: The product has Cortex-A15 CPU0. 1: The product does not have Cortex-A15 CPU0.</p> <p>[RZ/G1M/N]</p> <p>Bit 31 Cortex-A15 State</p> <p>0: The product has two Cortex-A15 CPUs. 1: The product does not have two Cortex-A15 CPUs.</p> <p>Bit 30 Reserved. The read value is always 1.</p> <p>Bit 29 Reserved. The read value is always 1.</p> <p>Bit 28 Cortex-A15 CPU1 State</p> <p>0: The product has Cortex-A15 CPU1. 1: The product does not have Cortex-A15 CPU1.</p> <p>Bit 27 Cortex-A15 CPU0 State</p> <p>0: The product has Cortex-A15 CPU0. 1: The product does not have Cortex-A15 CPU0.</p> <p>[RZ/G1E]</p> <p>Bit 31 Reserved. The read value is always 1.</p> <p>Bit 30 Reserved. The read value is always 1.</p> <p>Bit 29 Reserved. The read value is always 1.</p> <p>Bit 28 Reserved. The read value is always 1.</p> <p>Bit 27 Reserved. The read value is always 1.</p>

Bit	Bit Name	Initial Value	R/W	Description
26 to 22	CA7EN	It depends on the product. See the description.	R	<p>Cortex-A7 CPU State</p> <p>[RZ/G1H]</p> <p>Bit 26 Cortex-A7 State</p> <p>0: The product has four Cortex-A7 CPUs. 1: The product does not have four Cortex-A7 CPUs.</p> <p>Bit 25 Cortex-A7 CPU3 State</p> <p>0: The product has Cortex-A7 CPU3. 1: The product does not have Cortex-A7 CPU3.</p> <p>Bit 24 Cortex-A7 CPU2 State</p> <p>0: The product has Cortex-A7 CPU2. 1: The product does not have Cortex-A7 CPU2.</p> <p>Bit 23 Cortex-A7 CPU1 State</p> <p>0: The product has Cortex-A7 CPU1. 1: The product does not have Cortex-A7 CPU1.</p> <p>Bit 22 Cortex-A7 CPU0 State</p> <p>0: The product has Cortex-A7 CPU0. 1: The product does not have Cortex-A7 CPU0.</p> <p>[RZ/G1M/N]</p> <p>Bit 26 Reserved. The read value is always 1. Bit 25 Reserved. The read value is always 1. Bit 24 Reserved. The read value is always 1. Bit 23 Reserved. The read value is always 1. Bit 22 Reserved. The read value is always 1.</p> <p>[RZ/G1E]</p> <p>Bit 26 Cortex-A7 State</p> <p>0: The product has two Cortex-A7 CPUs. 1: The product does not have two Cortex-A7 CPUs.</p> <p>Bit 25 Reserved. The read value is always 1. Bit 24 Reserved. The read value is always 1.</p> <p>Bit 23 Cortex-A7 CPU1 State</p> <p>0: The product has Cortex-A7 CPU1. 1: The product does not have Cortex-A7 CPU1.</p> <p>Bit 22 Cortex-A7 CPU0 State</p> <p>0: The product has Cortex-A7 CPU0. 1: The product does not have Cortex-A7 CPU0.</p>
21 to 15	—	All 0	R	Reserved
14 to 8	PRODUCT	See the description.	R	<p>Product ID Number</p> <p>100 0101: RZ/G1H 100 0111: RZ/G1M 100 1011: RZ/G1N 100 1100: RZ/G1E</p>

Bit	Bit Name	Initial Value	R/W	Description
7 to 0	CUT	See the description.	R	Cut Number ES1.0: 0000 0000 ES2.0: 0001 0000 ES3.0: 0010 0000

**Table A.1 Possible Configuration of the ARM Cortex Cores**

Product	RZ/G1H	RZ/G1M	RZ/G1N	RZ/G1E
Cortex-A15 CPU3	√	—	—	—
Cortex-A15 CPU2	√	—	—	—
Cortex-A15 CPU1	√	√	√	—
Cortex-A15 CPU0	√	√	√	—
Cortex-A7 CPU3	√	—	—	—
Cortex-A7 CPU2	√	—	—	—
Cortex-A7 CPU1	√	—	—	√
Cortex-A7 CPU0	√	—	—	√

## Appendix B. Sequence of Activation for RZ/G Series Products

RZ/G1H	RZ/G1N
RZ/G1M	RZ/G1E

The following describes the initialization sequence of a RZ/G series product.

### (1) Selection of Master Boot Processor and External Boot Device

Select the master boot processor by placing the required levels on the MD6 and MD7 pins and external boot device by placing the required levels on the MD1, MD2, and MD3 pins before booting up the LSI. For details, see section 18, Booting.

Note: The following steps from (2) to (6) are not included in the sequence described in section 18, Booting because these steps are not relevant to booting. Note, however, that steps (2) to (6) must be executed before restoring the power supply to modules, including CPUs other than the master boot processor, to which the power has been cut off.

### (2) Stopping the RWDT

To prevent the watchdog timer issuing an unexpected reset or interrupt while the activation sequence is in progress, be sure to disable the RCLK watchdog timer (RDWT). Enable their operation at an appropriate time after the activation sequence is completed. For details, see section 8, Reset (RST), section 11, Interrupt Controller for AP-System Core (INTC-SYS), and section 55, RCLK Watchdog Timer.

Notes: 1. Use the RWTCSSRA register to disable the RWDT.  
2. Currently, the reset and interrupt signals caused by the watchdog timer overflowing are initially masked in RZ/G series products. Accordingly, this step of disabling the watchdog timers within the activation sequence is not mandatory. However, this step is implemented in the sample driver to ensure that they are masked.

### (3) Selecting the Functions of Multiplexed Pins

When a pin function other than that selected by the initial setting is to be used, set the relevant registers in the pin function controller (PFC). Note that, before setting these registers, the LSI multiplexed pin setting register (PMMR) must be appropriately set to prevent incorrect writing to registers. For details, see section 5, Pin Function Controller (PFC).

Note: When a GPIO function different from that selected by the initial setting is to be used, start by setting the GPIO attributes before setting the pin function controller.

### (4) Initial Settings for Operating Frequency Required by the Main Processor, Cache, MMU, and Interrupt Controller

Make initial settings for operating frequency required by the master processor, cache, MMU, and interrupt control. The operating frequencies are set by using the registers FRQCRC (for Cortex-A15), and PLL0CR in the clock pulse generator (CPG). The details of the functional specifications for the CPU required for setting the cache, MMU, and interrupt control are not included in this manual; use the sample driver included in the board support package (BSP).

Note: The FRQCRC register is not present in the RZ/G1E.

### (5) Initial Settings for Local Bus Control

When an external device is to be connected to the local bus (bits MD[3:1] are set to 000), make initial settings for the registers including CSWCR as required before starting access to the external device. For details, see section 14, LBSC within Bus Bridge.

## (6) Initial Settings for Memory Controllers

When a program is to be stored in and run from SDRAM, make initial settings for the required registers in the DBSC3 and S3CTRL modules. For details, see section 15, External Bus Controller for DDR3-SDRAM and section 15A, S3 Cache Controller (S3CTRL).

Note: QoS and split settings in the DBSC3 and S3CTRL modules are also required. For details, use the sample driver included in the board support package (BSP) for reference, as well as referring to the sections of the manual indicated above.

## (7) Settings for Restoring Power Supply to Functional Modules to be Used Immediately after Activation (Other than Cortex-A7 and Cortex-A15)

In the initial state, power may not be supplied to some modules to be used. Accordingly, for modules to be used immediately after activation, set the control registers in the system controller (SYSC) as required and read the status registers to check that the power supply has been restored. For details on the sequence for restoring the power supply, see section 61, System Controller (SYSC).

Note that the power control bits for the snoop control units (SCUs) of Cortex-A15 and Cortex-A7 are available in the SYSC, however, the supply of power to an SCU is automatically restored when the power supply for the respective CPU is separately restored by controlling the registers in the advanced power management unit for AP-system core (APMU). Accordingly, this step in controlling the power supply to the SCUs of Cortex-A15 and Cortex-A7 does not require explicit action.

Notes: 1. Cortex-A15 is not present in the RZ/G1E. Cortex-A7 is not present in the RZ/G1M, and RZ/G1N.  
2. The settings for modules other than those to be used immediately after activation can be made separately before the modules are used.

## (8) Settings for Release from the Module Reset State and the Supply of Clock Signals to Functional Modules to be Used Immediately after Activation (Other than CPUs)

In the initial state, clock signals may not be being supplied to all modules to be used. Accordingly, for modules to be used immediately after activation, set the xxxCKCR registers (xxx represents a module name) for the respective modules in the clock pulse generator (CPG) or set the SMSTPCRn registers (n = 0 to 11) in the module standby and software reset control block of the CPG. For details, see section 7, Clock Pulse Generator (CPG) and section 7A, Module Standby and Software Reset.

Note: The settings for modules other than those to be used immediately after activation can be made separately before the modules are used.

## (9) Setting of Boot Address of the CPU (as Required)

To switch the boot address to an area in the DDR memory to which high-speed access is possible, start by downloading the required program to the specified area and set the starting address for execution in the boot address register (SBAR, or SBAR2) for the relevant CPU. This setting is not required if the boot address is not to be changed. For details, see section 8, Reset (RST).

## (10) Restoring the Power Supply to a CPU Other than the Master Boot Device

Before using a CPU (Cortex-A15 or Cortex-A7) other than the master boot processor, start by checking the PRR register described in Appendix A to confirm which CPU is available for use. If activation of a CPU disabled by the PRR register is attempted, the clock pulse generator may not operate properly.\*<sup>1</sup>

To use a CPU (Cortex-A15 or Cortex-A7) other than the master boot processor, set the Cortex-A7/Cortex-A15 debug resource reset control register (CA7DBGRCR/CA15DBGRCR) in the APMU module and set the relevant control register in the same module to restore the power supply. Then, read the status registers in the APMU and SYSC modules to check whether the power supply has actually been restored. This procedure must be followed for each CPU until restoration of the power supply is confirmed. For details, see section 7B, Advanced Power Management Unit for AP-System Core (APMU), and section 61, System Controller (SYSC).

Notes: Cortex-A15 is not present in the RZ/G1E. Cortex-A7 is not present in the RZ/G1M, and RZ/G1N.

1. This step can be skipped if you already know which CPU is available for use.

#### **(11) Releasing CPUs Other than the Master Boot Processor from the Reset State**

When a CPU (Cortex-A15 or Cortex-A7) other than the master boot processor is to be used, clear the relevant bit in the Cortex-A15/Cortex-A7 reset control register (CA15RESCNT/CA7RESCNT) to 0 to release it from the reset state. To reduce fluctuations in current, release the CPUs from the reset state one at a time.

Note: Cortex-A15 is not present in the RZ/G1E. Cortex-A7 is not present in the RZ/G1M, and RZ/G1N.

This is the end of the required initial settings and all the CPUs to be used will have been activated.

- Notes:
1. There is no particular order for steps (3) to (10) in this sequence, except that the settings in step (5) must be made before step (9).
  2. In consideration of system performance, we recommend making the settings in steps (3) and (4) during the earlier stages of the sequence.
  3. The settings in some steps of this sequence might be re-made by the OS.

<b>Main Revisions and Additions in this Edition</b>
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Minor revisions such as corrections of errors in spelling and modifications of wording are not included in the revision history.

Rev.	Description		
	Page	Contents	Summary
1.00	—	First edition issued	



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RZ/G Series User's Manual: Hardware

Publication Date: Rev.1.00 Sep 30, 2016

Published by: Renesas Electronics Corporation

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