OBSOLETE PRODUCT
POSSIBLE SUBSTITUTE PRODUCT
HFA1113

July 2004 FN3606.5

## 225MHz, Low Power, Output Limiting, Closed Loop Buffer Amplifier

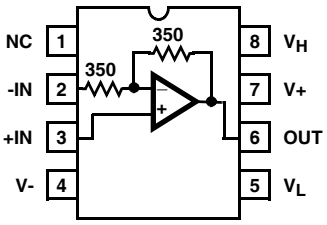
The HFA1115 is a high speed closed loop Buffer featuring both user programmable gain and output limiting. Manufactured on Intersil's proprietary complementary bipolar UHF-1 process, the HFA1115 also offers a wide -3dB bandwidth of 225MHz, very fast slew rate, excellent gain flatness and high output current.

This buffer is the ideal choice for high frequency applications requiring output limiting, especially those needing ultra fast overload recovery times. The limiting function allows the designer to set the maximum positive and negative output levels, thereby protecting later stages from damage or input saturation. The HFA1115 also allows for voltage gains of +2, +1, and -1, without the use of external resistors. Gain selection is accomplished via connections to the inputs, as described in the "Application Information" text. The result is a more flexible product, fewer part types in inventory, and more efficient use of board space.

Compatibility with existing op amp pinouts provides flexibility to upgrade low gain amplifiers, while decreasing component count. Unlike most buffers, the standard pinout provides an upgrade path, should a higher closed loop gain be needed at a future date. For Military product, refer to the HFA1115/883 data sheet.

## Pinout

**HFA1115**
**(PDIP, SOIC)**
TOP VIEW




## Pin Descriptions

| NAME | PIN NUMBER | DESCRIPTION |
|---|---|---|
| NC | 1 | No Connection |
| -IN | 2 | Inverting Input |
| +IN | 3 | Non-Inverting Input |
| V- | 4 | Negative Supply |
| $V_L$ | 5 | Lower Output Limit |
| OUT | 6 | Output |
| V+ | 7 | Positive Supply |
| $V_H$ | 8 | Upper Output Limit |

## Features

- User Programmable Output Voltage Limiting
- High Input Impedance . . . . . 1MΩ
- Differential Gain . . . . . 0.02%
- Differential Phase . . . . . 0.03 Degrees
- Wide -3dB Bandwidth ($A_V$ = +2) . . . . . 225MHz
- Very Fast Slew Rate ($A_V$ = -1) . . . . . 1135V/μs
- Low Supply Current . . . . . 7.1mA
- High Output Current . . . . . 60mA
- Excellent Gain Accuracy . . . . . 0.99V/V
- User Programmable For Closed-Loop Gains of +1, -1 or +2 Without Use of External Resistors
- Fast Overdrive Recovery . . . . . <1ns
- Standard Operational Amplifier Pinout

## Applications

- Flash A/D Drivers
- Video Cable Drivers
- High Resolution Monitors
- Professional Video Processing
- Medical Imaging
- Video Digitizing Boards/Systems
- Battery Powered Communications

## Part # Information

| PART NUMBER (BRAND) | TEMP. RANGE ($^oC$) | PACKAGE | PKG. NO. |
|---|---|---|---|
| HFA1115IP | -40 to 85 | 8 Ld PDIP | E8.3 |
| HFA1115IB (H1115I) | -40 to 85 | 8 Ld SOIC | M8.15 |
| HFA11XXEVAL | High Speed Op Amp DIP Evaluation Board | | |



CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
1-888-INTERSIL or 1-888-468-3774 | Intersil (and design) is a trademark of Intersil Americas Inc.
Copyright Harris Corporation 1998, Copyright Intersil Americas Inc. 2004. All Rights Reserved

## Absolute Maximum Ratings

Voltage Between V+ and V- . . . . . 11V
DC Input Voltage . . . . . $V_{SUPPLY}$
Output Current (Note 2) . . . . . Short Circuit Protected
ESD Rating
Human Body Model (Per MIL-STD-883 Method 3015.7) . . . .600V

## Operating Conditions

Temperature Range . . . . . $-40^oC$ to $85^oC$
Supply Voltage Range (Typical) . . . . . 5V to 10V

## Thermal Information

| Thermal Resistance (Typical, Note 1) | $\theta_{JA}$ ($^oC/W$) |
|---|---|
| PDIP Package | 130 |
| SOIC Package | 170 |

Maximum Junction Temperature (Die) . . . . . $175^oC$
Maximum Junction Temperature (Plastic Packages) . . . . . $150^oC$
Maximum Storage Temperature Range . . . . . $-65^oC$ to $150^oC$
Maximum Lead Temperature (Soldering 10s) . . . . . $300^oC$
(SOIC - Lead Tips Only)

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

NOTES:

1. $\theta_{JA}$ is measured with the component mounted on an evaluation PC board in free air.
2. Output is protected for short circuits to ground. Brief short circuits to ground will not degrade reliability, however, continuous (100% duty cycle) output current should not exceed 30mA for maximum reliability.

## Electrical Specifications

$V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_L = 100\Omega$, Unless Otherwise Specified

| PARAMETER | TEST CONDITIONS | (NOTE 3) TEST LEVEL | TEMP. ($^oC$) | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **INPUT CHARACTERISTICS** | | | | | | | |
| Output Offset Voltage | | A | 25 | - | 2 | 10 | mV |
| | | A | Full | - | 3 | 15 | mV |
| Average Output Offset Voltage Drift | | B | Full | - | 22 | 70 | $\mu V/^oC$ |
| Common-Mode Rejection Ratio | $\Delta V_{CM} = \pm1.8V$ | A | 25 | 42 | 45 | - | dB |
| | $\Delta V_{CM} = \pm1.8V$ | A | 85 | 40 | 44 | - | dB |
| | $\Delta V_{CM} = \pm1.2V$ | A | -40 | 40 | 45 | - | dB |
| Power Supply Rejection Ratio | $\Delta V_{PS} = \pm1.8V$ | A | 25 | 45 | 49 | - | dB |
| | $\Delta V_{PS} = \pm1.8V$ | A | 85 | 43 | 48 | - | dB |
| | $\Delta V_{PS} = \pm1.2V$ | A | -40 | 43 | 48 | - | dB |
| Non-Inverting Input Bias Current | | A | 25 | - | 1 | 15 | $\mu A$ |
| | | A | Full | - | 3 | 25 | $\mu A$ |
| Non-Inverting Input Bias Current Drift | | B | Full | - | 30 | 80 | $nA/^oC$ |
| Non-Inverting Input Bias Current Power Supply Sensitivity | $\Delta V_{PS} = \pm1.25V$ | A | 25 | - | 0.5 | 1 | $\mu A/V$ |
| | | A | Full | - | - | 3 | $\mu A/V$ |
| Non-Inverting Input Resistance | $\Delta V_{CM} = \pm1.8V$ | A | 25 | 0.8 | 1.1 | - | $M\Omega$ |
| | $\Delta V_{CM} = \pm1.8V$ | A | 85 | 0.5 | 1.4 | - | $M\Omega$ |
| | $\Delta V_{CM} = \pm1.2V$ | A | -40 | 0.5 | 1.3 | - | $M\Omega$ |
| Inverting Input Resistance | | C | 25 | 280 | 350 | 420 | $\Omega$ |
| Input Capacitance | | C | 25 | - | 1.6 | - | pF |
| Input Voltage Common Mode Range (Implied by $V_{IO}$ CMRR and $+R_{IN}$ Tests) | | A | 25, 85 | $\pm1.8$ | $\pm2.4$ | - | V |
| | | A | -40 | $\pm1.2$ | $\pm1.7$ | - | V |
| Input Noise Voltage Density (Note 4) | f = 100kHz | B | 25 | - | 7 | - | $nV/\sqrt{Hz}$ |
| Non-Inverting Input Noise Current Density (Note 4) | f = 100kHz | B | 25 | - | 3.6 | - | $pA/\sqrt{Hz}$ |

**Electrical Specifications** $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

| PARAMETER | TEST CONDITIONS | (NOTE 3) TEST LEVEL | TEMP. ($^oC$) | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **TRANSFER CHARACTERISTICS** | | | | | | | |
| Gain | $A_V = -1$ | A | 25 | -0.98 | -0.996 | -1.02 | V/V |
| | | A | Full | -0.975 | -1.000 | -1.025 | V/V |
| | $A_V = +1$ | A | 25 | 0.98 | 0.992 | 1.02 | V/V |
| | | A | Full | 0.975 | 0.993 | 1.025 | V/V |
| | $A_V = +2$ | A | 25 | 1.96 | 1.988 | 2.04 | V/V |
| | | A | Full | 1.95 | 1.990 | 2.05 | V/V |
| **AC CHARACTERISTICS** | | | | | | | |
| -3dB Bandwidth ($V_{OUT} = 0.2V_{P-P}$, Note 4) | $A_V = -1$ | B | 25 | - | 225 | - | MHz |
| | $A_V = +1$, $+R_S = 620\Omega$ | B | 25 | - | 200 | - | MHz |
| | $A_V = +2$ | B | 25 | - | 225 | - | MHz |
| Full Power Bandwidth ($V_{OUT} = 5V_{P-P}$ at $A_V = +2/-1$, $4V_{P-P}$ at $A_V = +1$, Note 4) | $A_V = -1$ | B | 25 | - | 157 | - | MHz |
| | $A_V = +1$, $+R_S = 620\Omega$ | B | 25 | - | 140 | - | MHz |
| | $A_V = +2$ | B | 25 | - | 125 | - | MHz |
| Gain Flatness (to 25MHz, $V_{OUT} = 0.2V_{P-P}$, Note 4) | $A_V = +1$, $+R_S = 620\Omega$ | B | 25 | - | $\pm0.1$ | - | dB |
| | $A_V = +2$ | B | 25 | - | $\pm0.04$ | - | dB |
| Gain Flatness (to 50MHz, $V_{OUT} = 0.2V_{P-P}$, Note 4) | $A_V = +1$, $+R_S = 620\Omega$ | B | 25 | - | $\pm0.25$ | - | dB |
| | $A_V = +2$ | B | 25 | - | $\pm0.1$ | - | dB |
| **OUTPUT CHARACTERISTICS** | | | | | | | |
| Output Voltage Swing (Note 4) | $A_V = -1$, $R_L = 100\Omega$ | A | 25 | $\pm3.0$ | $\pm3.2$ | - | V |
| | | A | Full | $\pm2.8$ | $\pm3.0$ | - | V |
| Output Current (Note 4) | $A_V = -1$, $R_L = 50\Omega$ | A | 25, 85 | 50 | 55 | - | mA |
| | | A | -40 | 28 | 42 | - | mA |
| Output Short Circuit Current | | B | 25 | - | 90 | - | mA |
| Output Resistance (Note 4) | DC, $A_V = +2$ | B | 25 | - | 0.07 | - | $\Omega$ |
| Second Harmonic Distortion ($A_V = +2$, $V_{OUT} = 2V_{P-P}$) | 10MHz | B | 25 | - | -50 | - | dBc |
| | 20MHz | B | 25 | - | -45 | - | dBc |
| Third Harmonic Distortion ($A_V = +2$, $V_{OUT} = 2V_{P-P}$) | 10MHz | B | 25 | - | -50 | - | dBc |
| | 20MHz | B | 25 | - | -45 | - | dBc |
| **TRANSIENT RESPONSE** $A_V = +2$, Unless Otherwise Specified | | | | | | | |
| Rise and Fall Times ($V_{OUT} = 0.5V_{P-P}$, Note 4) | Rise Time | B | 25 | - | 1.7 | - | ns |
| | Fall Time | B | 25 | - | 1.9 | - | ns |
| Overshoot ($V_{OUT} = 0.5V_{P-P}$, $V_{IN}$ $t_{RISE} = 2.5ns$) | +OS | B | 25 | - | 0 | - | % |
| | -OS | B | 25 | - | 0 | - | % |
| Slew Rate ($V_{OUT} = 5V_{P-P}$, $A_V = -1$) | +SR | B | 25 | - | 1660 | - | V/µs |
| | -SR (Note 5) | B | 25 | - | 1135 | - | V/µs |
| Slew Rate ($V_{OUT} = 4V_{P-P}$, $A_V = +1$, $+R_S = 620\Omega$) | +SR | B | 25 | - | 1125 | - | V/µs |
| | -SR (Note 5) | B | 25 | - | 800 | - | V/µs |

**Electrical Specifications** $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

| PARAMETER | TEST CONDITIONS | (NOTE 3) TEST LEVEL | TEMP. ($^oC$) | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Slew Rate ($V_{OUT} = 5V_{P-P}$, $A_V = +2$) | +SR | B | 25 | - | 1265 | - | V/μs |
| | -SR (Note 5) | B | 25 | - | 870 | - | V/μs |
| Settling Time ($V_{OUT}$ = +2V to 0V step, Note 4) | To 0.1% | B | 25 | - | 23 | - | ns |
| | To 0.05% | B | 25 | - | 33 | - | ns |
| | To 0.02% | B | 25 | - | 45 | - | ns |
| **VIDEO CHARACTERISTICS** | | | | | | | |
| Differential Gain | f = 3.58MHz, $A_V = +2$, $R_L = 150\Omega$ | B | 25 | - | 0.02 | - | % |
| Differential Phase | f = 3.58MHz, $A_V = +2$, $R_L = 150\Omega$ | B | 25 | - | 0.03 | - | Degrees |
| **OUTPUT LIMITING CHARACTERISTICS** $A_V = +2$, $V_H = +1V$, $V_L = -1V$, Unless Otherwise Specified | | | | | | | |
| Limit Accuracy (Note 4) | $V_{IN} = \pm1.6V$, $A_V = -1$ | A | Full | -125 | -70 | 125 | mV |
| Overdrive Recovery Time (Note 4) | $V_{IN} = \pm1V$ | B | 25 | - | 0.8 | - | ns |
| Negative Limit Range | | B | 25 | -5.0 to +2.5 | | | V |
| Positive Limit Range | | B | 25 | -2.5 to +5.0 | | | V |
| Limit Input Bias Current | | A | Full | - | 85 | 200 | μA |
| Limit Input Bandwidth | | C | 25 | - | 100 | - | MHz |
| **POWER SUPPLY CHARACTERISTICS** | | | | | | | |
| Power Supply Range | | C | 25 | 4.5 | - | 5.5 | ±V |
| Power Supply Current (Note 4) | | A | 25 | 6.6 | 6.9 | 7.1 | mA |
| | | A | Full | - | 7.1 | 7.3 | mA |

NOTE:

3. Test Level: A. Production Tested; B. Typical or Guaranteed Limit Based on Characterization; C. Design Typical for Information Only.
4. See Typical Performance Curves for more information.
5. Slew rates are asymmetrical if the output swings below GND (e.g., a bipolar signal). Positive unipolar output signals have symmetric positive and negative slew rates comparable to the +SR specification. See the “Application Information” section, and the pulse response graphs for details.

## Application Information

### Relevant Application Notes

The following Application Notes pertain to the HFA1115:

- AN9653-Use and Application of Output Limiting Amplifiers
- AN9752-Sync Stripper and Sync Inserter for Composite Video

These publications may be obtained from Intersil’s web site (http://www.intersil.com).

### HFA1115 Advantages

The HFA1115 features a novel design which allows the user to select from three closed loop gains, without any external components. The result is a more flexible product, fewer part types in inventory, and more efficient use of board space. Implementing a gain of 2, cable driver with this IC eliminates the two gain setting resistors, which frees up board space for termination resistors.

Like most newer high performance amplifiers, the HFA1115 is a current feedback amplifier (CFA). CFAs offer high bandwidth and slew rate at low supply currents, but can be difficult to use because of their sensitivity to feedback capacitance and parasitics on the inverting input (summing node). The HFA1115 eliminates these concerns by bringing the gain setting resistors on-chip. This yields the optimum placement and value of the feedback resistor, while minimizing feedback and summing node parasitics. Because there is no access to the summing node, the PCB parasitics do not impact performance at gains of +2 or -1 (see “Unity Gain Considerations” for discussion of parasitic impact on unity gain performance).

The HFA1115's closed loop gain implementation provides better gain accuracy, lower offset and output impedance, and better distortion compared with open loop buffers.

### *Closed Loop Gain Selection*

This "buffer" operates in closed loop gains of -1, +1, or +2, and gain selection is accomplished via connections to the ±inputs. Applying the input signal to +IN and floating -IN selects a gain of +1 (see next section for layout caveats), while grounding -IN selects a gain of +2. A gain of -1 is obtained by applying the input signal to -IN with +IN grounded through a 50Ω resistor.

The table below summarizes these connections:

| GAIN ($A_V$) | CONNECTIONS | |
|---|---|---|
| | +INPUT (PIN 3) | -INPUT (PIN 2) |
| -1 | 50Ω to GND | Input |
| +1 | Input | NC (Floating) |
| +2 | Input | GND |

### *Unity Gain Considerations*

Unity gain selection is accomplished by floating the -Input of the HFA1115. Anything that tends to short the -Input to GND, such as stray capacitance at high frequencies, will cause the amplifier gain to increase toward a gain of +2. The result is excessive high frequency peaking, and possible instability. Even the minimal amount of capacitance associated with attaching the -Input lead to the PCB results in approximately 3dB of gain peaking. At a minimum this requires due care to ensure the minimum capacitance at the -Input connection.

**TABLE 1. UNITY GAIN PERFORMANCE FOR VARIOUS IMPLEMENTATIONS**

| APPROACH | PEAK-ING (dB) | BW (MHz) | +SR/-SR (V/μs) | ±0.1dB GAIN FLATNESS (MHz) |
|---|---|---|---|---|
| Remove Pin 2 | 2.5 | 400 | 1200/850 | 20 |
| $+R_S$ = 620Ω | 0.6 | 170 | 1125/800 | 25 |
| $+R_S$ = 620Ω and Remove Pin 2 | 0 | 165 | 1050/775 | 65 |
| Short Pins 2, 3 | 0 | 200 | 875/550 | 45 |
| 100pF cap. be-tween pins 2, 3 | 0.2 | 190 | 900/550 | 19 |

Table 1 lists five alternate methods for configuring the HFA1115 as a unity gain buffer, and the corresponding performance. The implementations vary in complexity and involve performance trade-offs. The easiest approach to implement is simply shorting the two input pins together, and applying the input signal to this common node. The amplifier bandwidth drops from 400MHz to 200MHz, but excellent gain flatness is the benefit. Another drawback to this approach is that the amplifier input noise voltage and input offset voltage terms see a gain of +2, resulting in higher noise and output offset voltages. Alternately, a 100pF capacitor between the inputs shorts them only at high frequencies, which prevents the increased output offset voltage but delivers less gain flatness.

Another straightforward approach is to add a 620Ω resistor in series with the positive input. This resistor and the HFA1115 input capacitance form a low pass filter which rolls off the signal bandwidth before gain peaking occurs. This configuration was employed to obtain the datasheet AC and transient parameters for a gain of +1.

### *Non-inverting Input Source Impedance*

For best operation, the DC source impedance seen by the non-inverting input should be ≥50Ω. This is especially important in inverting gain configurations where the non-inverting input would normally be connected directly to GND.

### *Pulse Undershoot and Asymmetrical Slew Rates*

The HFA1115 utilizes a quasi-complementary output stage to achieve high output current while minimizing quiescent supply current. In this approach, a composite device replaces the traditional PNP pulldown transistor. The composite device switches modes after crossing 0V, resulting in added distortion for signals swinging below ground, and an increased undershoot on the negative portion of the output waveform (see Figures 9, 13, and 17). This undershoot isn't present for small bipolar signals, or large positive signals. Another artifact of the composite device is asymmetrical slew rates for output signals with a negative voltage component. The slew rate degrades as the output signal crosses through 0V (see Figures 9, 13, and 17), resulting in a slower overall negative slew rate. Positive only signals have symmetrical slew rates as illustrated in the large signal positive pulse response graphs (see Figures 7, 11, and 15).

## *PC Board Layout*

This amplifier's frequency response depends greatly on the care taken in designing the PC board. **The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!**

Attention should be given to decoupling the power supplies. A large value (10μF) tantalum in parallel with a small value (0.1μF) chip capacitor works well in most cases.

Terminated microstrip signal lines are recommended at the input and output of the device. Capacitance directly on the output must be minimized, or isolated as discussed in the next section.

For unity gain applications, care must also be taken to minimize the capacitance to ground at the amplifier's inverting input. At higher frequencies this capacitance tends to short the -INPUT to GND, resulting in a closed loop gain which increases with frequency. This causes excessive high frequency peaking and potentially other problems as well.

An example of a good high frequency layout is the Evaluation Board shown in Figure 2.

## Driving Capacitive Loads

Capacitive loads, such as an A/D input, or an improperly terminated transmission line degrade the amplifier's phase margin resulting in frequency response peaking and possible oscillations. In most cases, the oscillation can be avoided by placing a resistor ($R_S$) in series with the output prior to the capacitance.

Figure 1 details starting points for the selection of this resistor. The points on the curve indicate the $R_S$ and $C_L$ combinations for the optimum bandwidth, stability, and settling time, but experimental fine tuning is recommended. Picking a point above or to the right of the curve yields an overdamped response, while points below or left of the curve indicate areas of underdamped performance.

$R_S$ and $C_L$ form a low pass network at the output, thus limiting system bandwidth well below the amplifier bandwidth of 200MHz ($A_V$ = +1). By decreasing $R_S$ as $C_L$ increases (as illustrated by the curves), the maximum bandwidth is obtained without sacrificing stability. In spite of this, bandwidth still decreases as the load capacitance increases. For example, at $A_V$ = +1, $R_S$ = 50Ω, $C_L$ = 22pF, the overall bandwidth is 185MHz, but the bandwidth drops to 50MHz at $A_V$ = +1, $R_S$ = 15Ω, $C_L$ = 330pF.

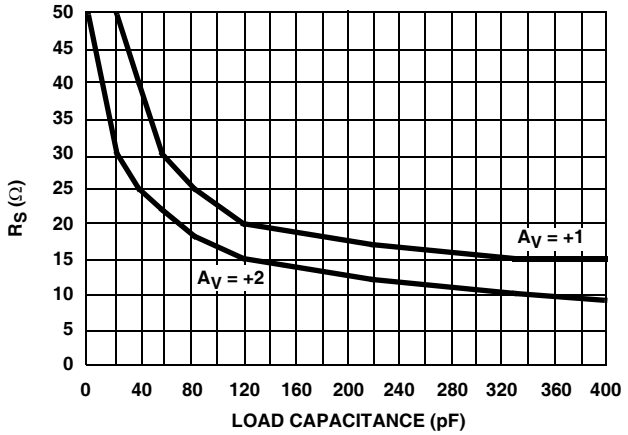



**FIGURE 1. RECOMMENDED SERIES RESISTOR vs LOAD CAPACITANCE**

## Evaluation Board

The performance of the HFA1115 may be evaluated using the HFA11XX Evaluation Board, slightly modified as follows:

1. 1. Remove the 510Ω feedback resistor ($R_2$), and leave the connection open.
2. 2. a. For $A_V$ = +1 evaluation, remove the 510Ω gain setting resistor ($R_1$), and leave pin 2 floating.
   b. For $A_V$ = +2, replace the 510Ω gain setting resistor with a 0Ω resistor to GND.

The layout and modified schematic of the board are shown in Figure 2.

To order evaluation boards (Part Number HFA11XXEVAL), please contact your local sales office.

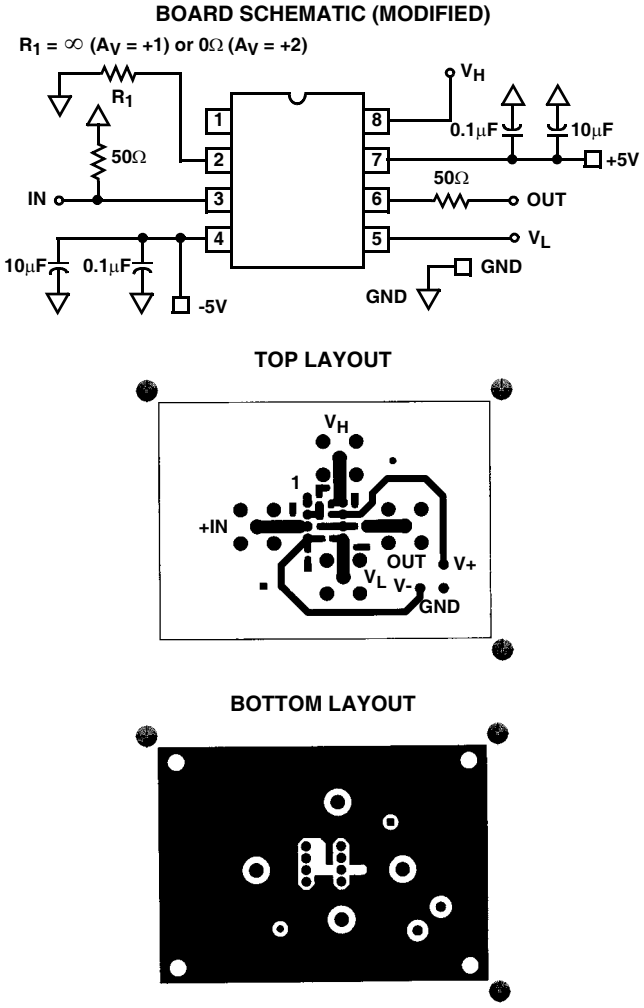



**FIGURE 2. EVALUATION BOARD SCHEMATIC (AFTER MODIFICATION FOR BUFFER USE) AND LAYOUT**

## Limiting Operation

### General

The HFA1115 features user programmable output clamps to limit output voltage excursions. Limiting action is obtained by applying voltages to the $V_H$ and $V_L$ terminals (pins 8 and 5) of the amplifier. $V_H$ sets the upper output limit, while $V_L$ sets the lower limit level. If the amplifier tries to drive the output above $V_H$, or below $V_L$, the clamp circuitry limits the output voltage at $V_H$ or $V_L$ (± the limit accuracy), respectively. The low input bias currents of the limit pins allow them to be driven by simple resistive divider circuits, or active elements such as amplifiers or DACs.

### Limit Circuitry

Figure 3 shows a simplified schematic of the HFA1115 input stage, and the high limit ($V_H$) circuitry. As with all current feedback amplifiers, there is a unity gain buffer ($Q_{X1}$ - $Q_{X2}$) between the positive and negative inputs. This buffer forces -IN to track +IN, and sets up a slewing current of:

$I_{SLEW} = (V_{-IN} - V_{OUT})/R_F + V_{-IN}/R_G$

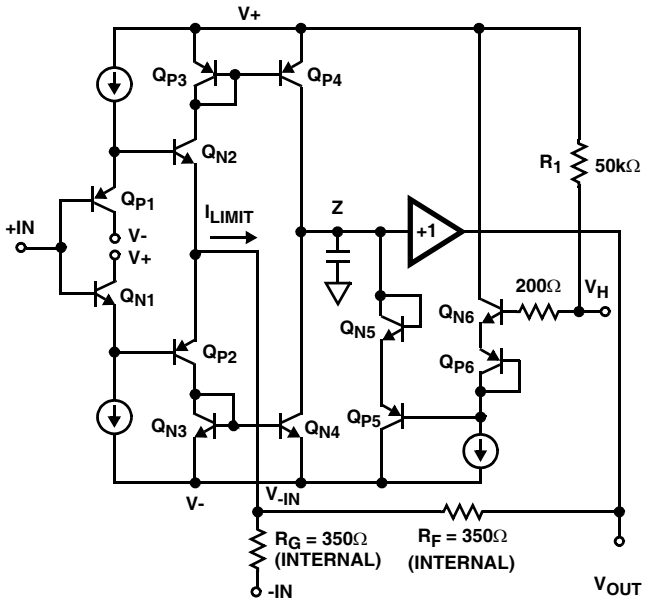



**FIGURE 3. HFA1115 SIMPLIFIED $V_H$ LIMIT CIRCUITRY**

This current is mirrored onto the high impedance node (Z) by $Q_{X3}$-$Q_{X4}$, where it is converted to a voltage and fed to the output via another unity gain buffer. If no limiting is utilized, the high impedance node may swing within the limits defined by $Q_{P4}$ and $Q_{N4}$. Note that when the output reaches its quiescent value, the current flowing through -IN is reduced to only that small current ($-I_{BIAS}$) required to keep the output at the final voltage.

Tracing the path from $V_H$ to Z illustrates the effect of the limit voltage on the high impedance node. $V_H$ decreases by $2V_{BE}$ ($Q_{N6}$ and $Q_{P6}$) to set up the base voltage on $Q_{P5}$. $Q_{P5}$ begins to conduct whenever the high impedance node reaches a voltage equal to $Q_{P5}$'s base voltage + $2V_{BE}$ ($Q_{P5}$ and $Q_{N5}$). Thus, $Q_{P5}$ limits node Z whenever Z reaches $V_H$. $R_1$ provides a pull-up network to ensure functionality with the limit inputs floating. A similar description applies to the symmetrical low limit circuitry controlled by $V_L$.

When the output is limited, the negative input continues to source a slewing current ($I_{Limit}$) in an attempt to force the output to the quiescent voltage defined by the input. $Q_{P5}$ must sink this current while limiting, because the -IN current is always mirrored onto the high impedance node. The limiting current is calculated as:

$$I_{LIMIT} = (V_{-IN} - V_{OUT\ LIMITED})/R_F + V_{-IN}/R_G.$$

As an example, a unity gain circuit with $V_{IN}$ = 2V, and $V_H$ = 1V, would have $I_{LIMIT}$ = (2V - 1V)/350Ω + 2V/∞ = 2.8mA ($R_G = \infty$ because -IN is floated for unity gain applications). Note that $I_{CC}$ increases by $I_{LIMIT}$ when the output is limited.

### *Limit Accuracy*

The limited output voltage will not be exactly equal to the voltage applied to $V_H$ or $V_L$. Offset errors, mostly due to $V_{BE}$ mismatches, necessitate a limit accuracy parameter which is found in the device specifications. Limit accuracy is a function of the limiting conditions. Referring again to Figure 3, it can be seen that one component of limit accuracy is the $V_{BE}$ mismatch between the $Q_{X6}$ transistors, and the $Q_{X5}$ transistors. If the transistors always ran at the same current level there would be no $V_{BE}$ mismatch, and no contribution to the inaccuracy. The $Q_{X6}$ transistors are biased at a constant current, but as described earlier, the current through $Q_{X5}$ is equivalent to $I_{Limit}$. $V_{BE}$ increases as $I_{LIMIT}$ increases, causing the limited output voltage to increase as well. $I_{LIMIT}$ is a function of the overdrive level (($A_V$ x $V_{IN}$ - $V_{LIMIT}$) / $V_{LIMIT}$), so limit accuracy degrades as the overdrive increases (see Figures 28 and 29). For example, accuracy degrades from -20mV to +30mV when the overdrive increases from 100% to 200% ($A_V$ = +2, $V_H$ = 500mV).

Consideration must also be given to the fact that the limit voltages have an effect on amplifier linearity. The "Linearity Near Limit Voltage" curves, Figures 30 and 31, illustrate the impact of several limit levels on linearity.

### *Limit Range*

Unlike some competitor devices, both $V_H$ and $V_L$ have usable ranges that cross 0V. While $V_H$ must be more positive than $V_L$, both may be positive or negative, within the range restrictions indicated in the specifications. For example, the HFA1115 could be limited to ECL output levels by setting $V_H$ = -0.8V and $V_L$ = -1.8V. $V_H$ and $V_L$ may be connected to the same voltage (GND for instance) but the result won't be a DC output voltage from an AC input signal. A 150mV - 200mV AC signal will still be present at the output.

### *Recovery from Overdrive*

The output voltage remains at the limit level as long as the overdrive condition remains. When the input voltage drops below the overdrive level ($V_{LIMIT}/A_V$) the amplifier returns to linear operation. A time delay, known as the Overdrive Recovery Time, is required for this resumption of linear operation. Overdrive recovery time is defined as the difference between the amplifier's propagation delay exiting limiting and the amplifier's normal propagation delay, and it is a strong function of the overdrive level. Figure 32 details the overdrive recovery time for various limit and overdrive levels

### *Benefits of Output Limiting*

The plots of "Pulse Response Without Limiting" and "Pulse Response With Limiting" (Figures 4 and 5) highlight the advantages of output limiting. Besides the obvious benefit of constraining the output swing to a defined range, limiting the output excursions also keeps the output transistors from saturating, which prevents unwanted saturation artifacts from distorting the output signal. Output limiting also takes advantage of the HFA1115's ultra-fast overdrive recovery

time, reducing the recovery time from 2.5ns to 0.5ns, based on the amplifier's normal propagation delay of 1.2ns.

## *Typical Performance Curves* $V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified

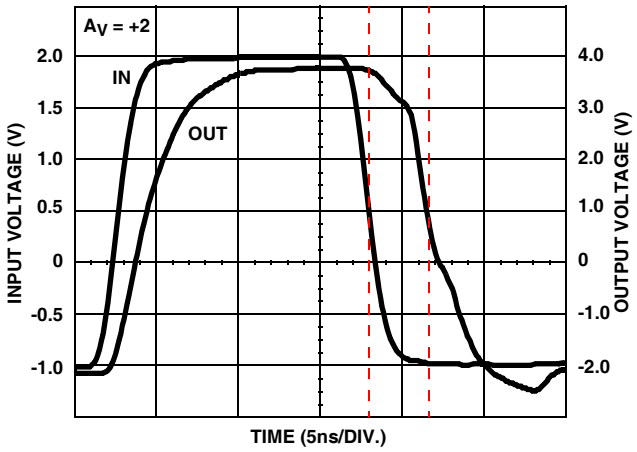



FIGURE 4. PULSE RESPONSE WITHOUT LIMITING

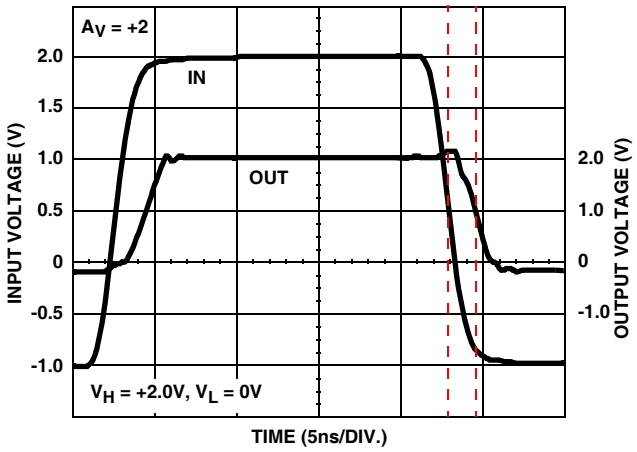



FIGURE 5. PULSE RESPONSE WITH LIMITING

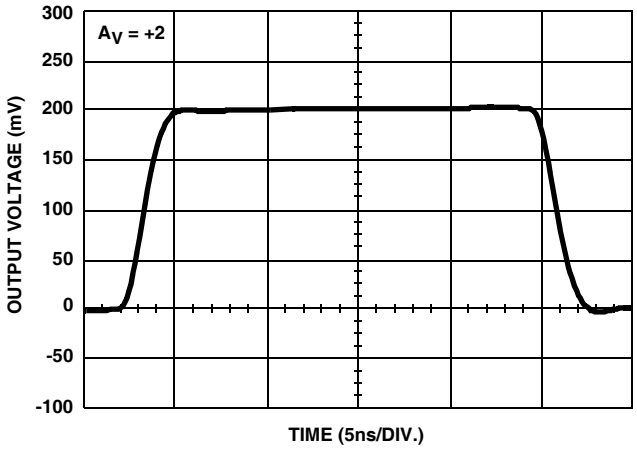



FIGURE 6. SMALL SIGNAL POSITIVE PULSE RESPONSE

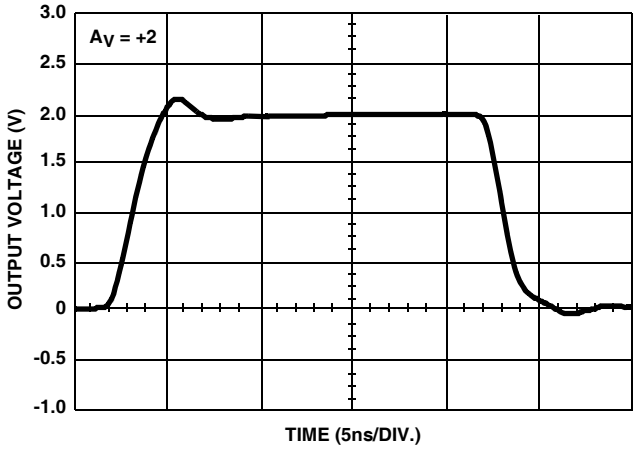



FIGURE 7. LARGE SIGNAL POSITIVE PULSE RESPONSE

## Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

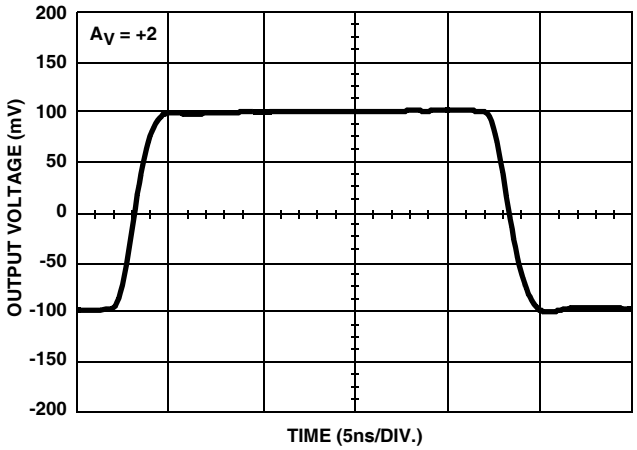



FIGURE 8. SMALL SIGNAL BIPOLAR PULSE RESPONSE

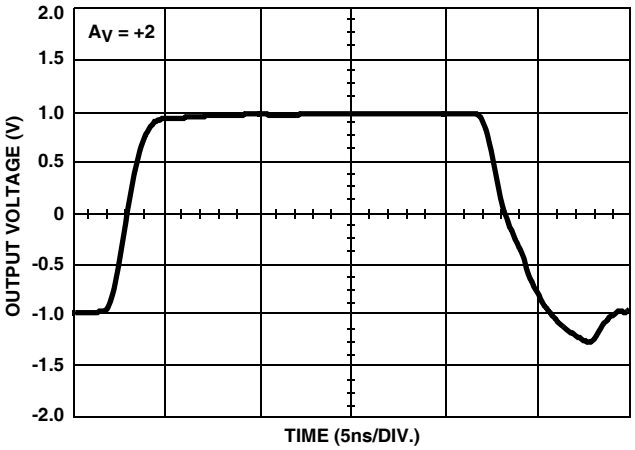



FIGURE 9. LARGE SIGNAL BIPOLAR PULSE RESPONSE

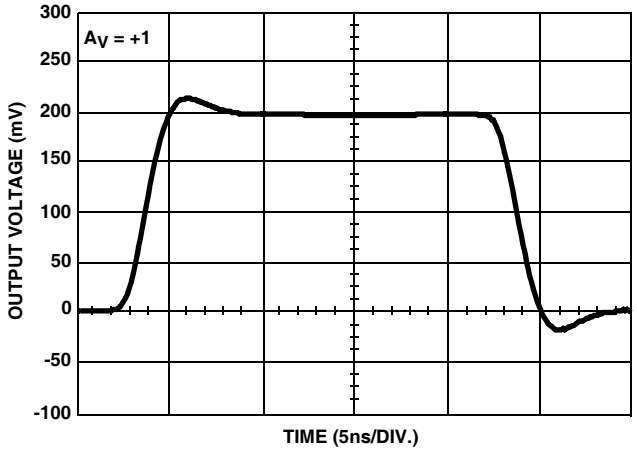



FIGURE 10. SMALL SIGNAL POSITIVE PULSE RESPONSE

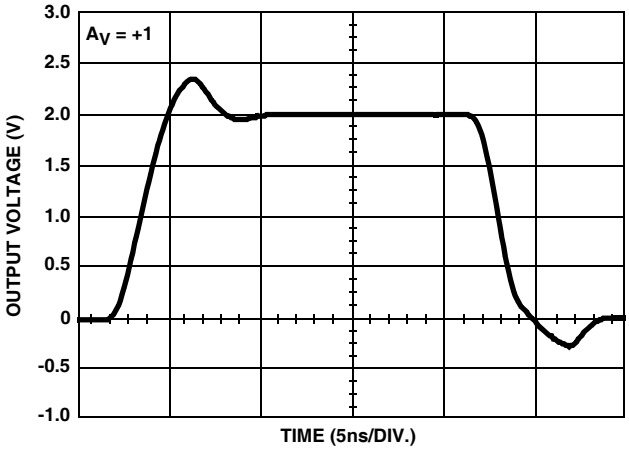



FIGURE 11. LARGE SIGNAL POSITIVE PULSE RESPONSE

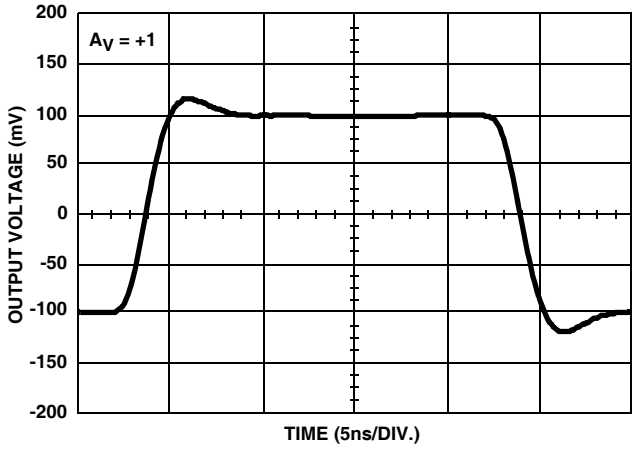



FIGURE 12. SMALL SIGNAL BIPOLAR PULSE RESPONSE

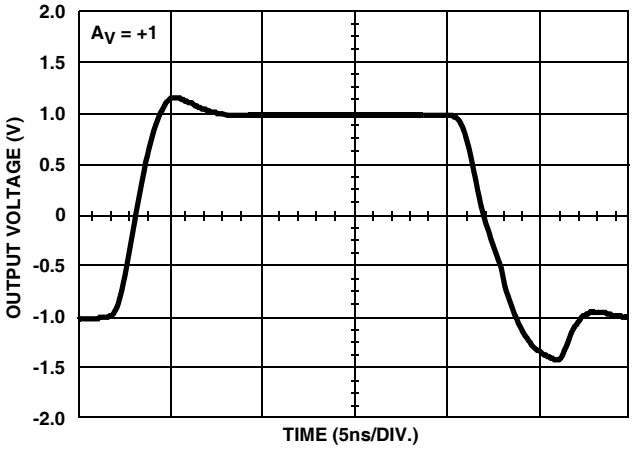



FIGURE 13. LARGE SIGNAL BIPOLAR PULSE RESPONSE

## Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

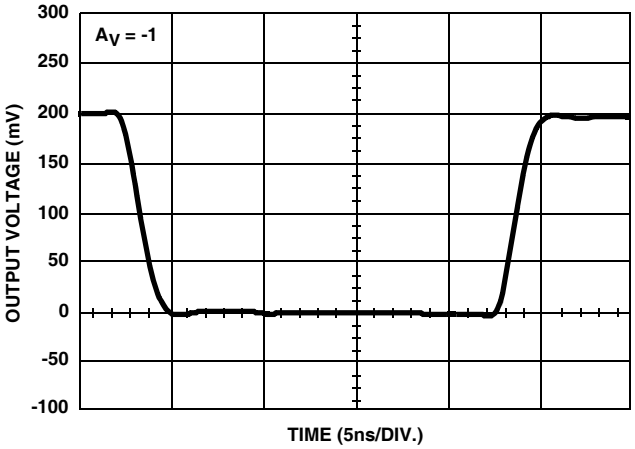



FIGURE 14. SMALL SIGNAL POSITIVE PULSE RESPONSE

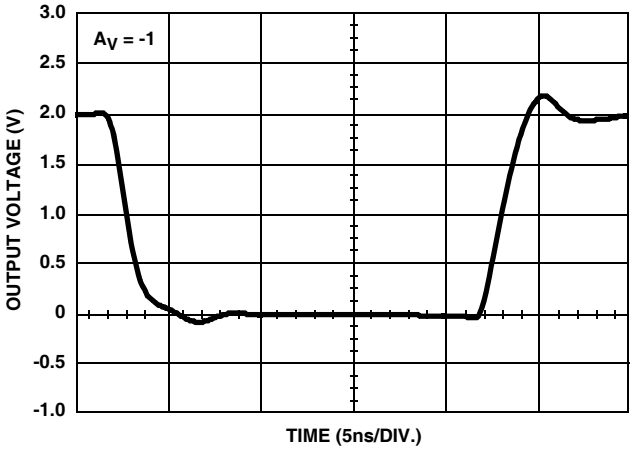



FIGURE 15. LARGE SIGNAL POSITIVE PULSE RESPONSE

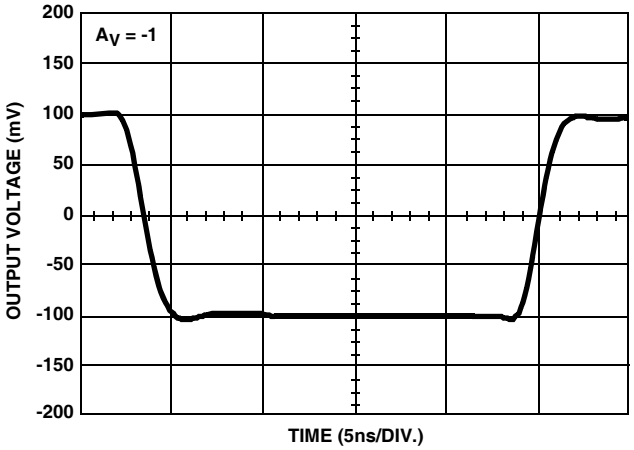



FIGURE 16. SMALL SIGNAL BIPOLAR PULSE RESPONSE

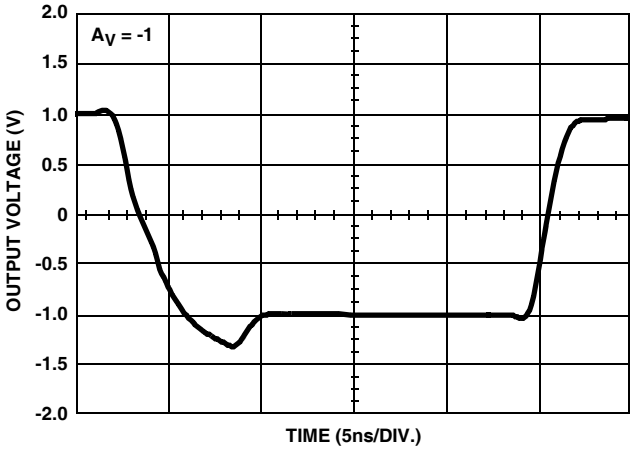



FIGURE 17. LARGE SIGNAL BIPOLAR PULSE RESPONSE

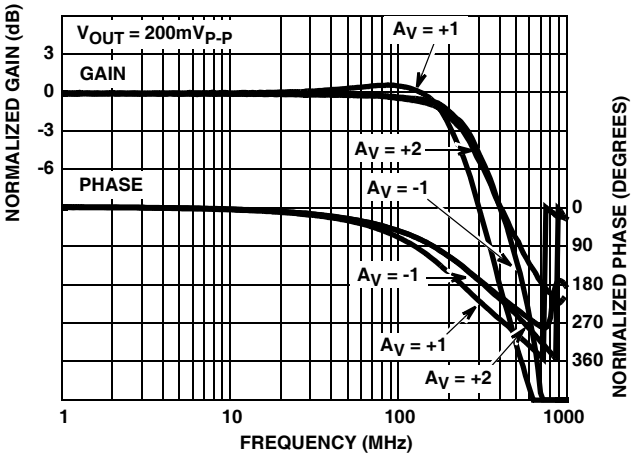



FIGURE 18. FREQUENCY RESPONSE

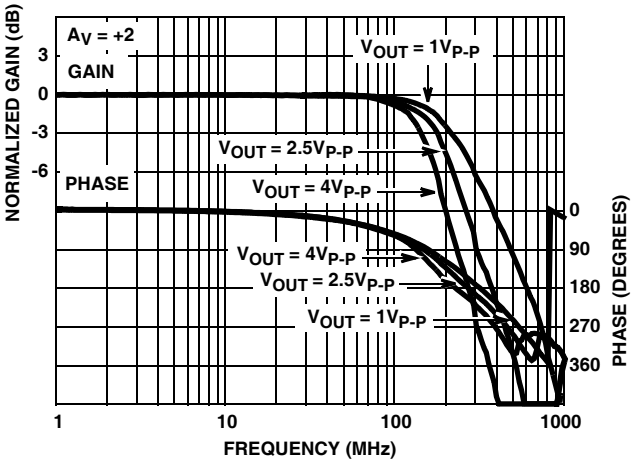



FIGURE 19. FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES

## Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

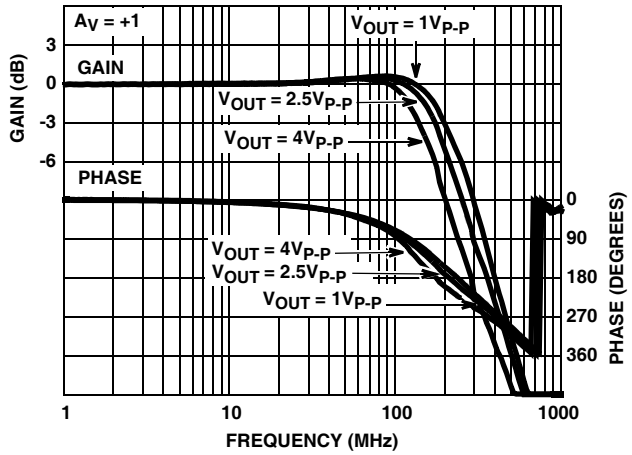



FIGURE 20. FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES

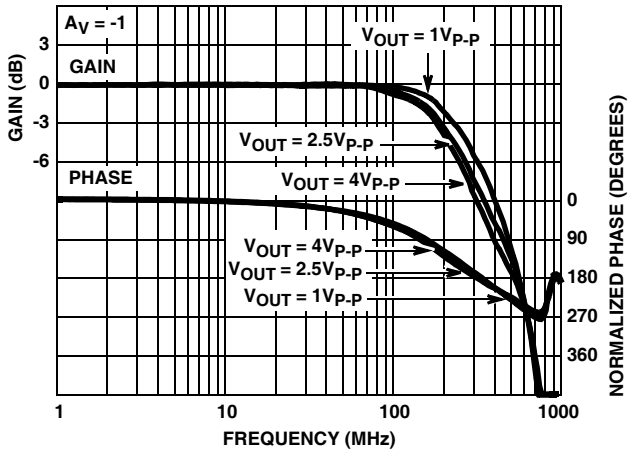



FIGURE 21. FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES

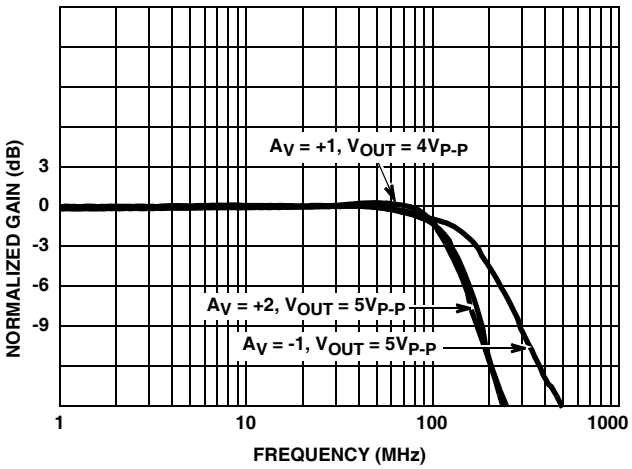



FIGURE 22. FULL POWER BANDWIDTH

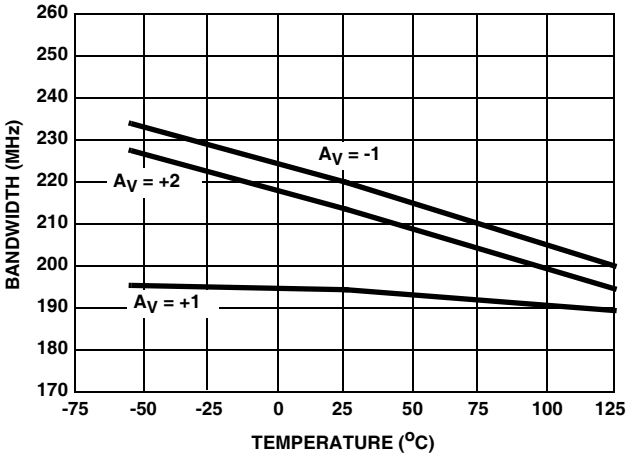



FIGURE 23. -3dB BANDWIDTH vs TEMPERATURE

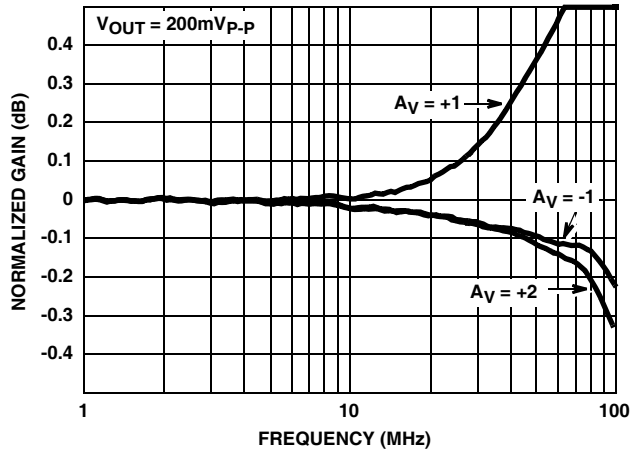



FIGURE 24. GAIN FLATNESS

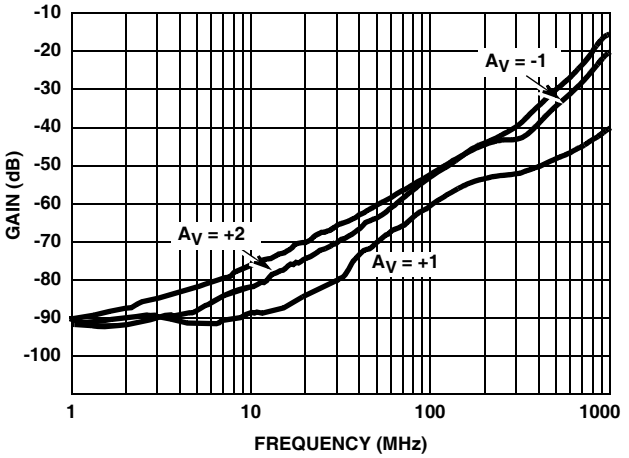



FIGURE 25. REVERSE ISOLATION ($S_{12}$)

## Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

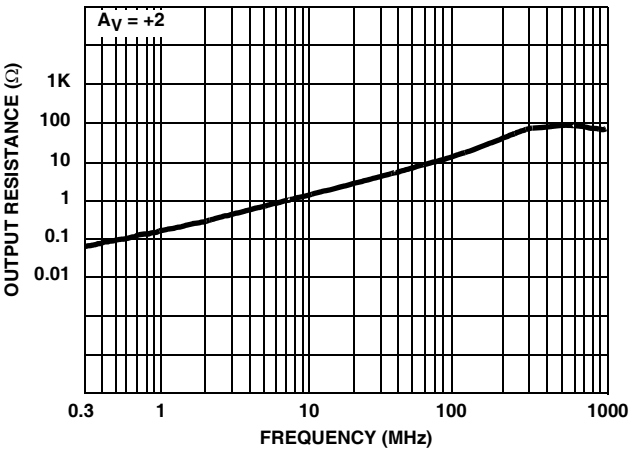



FIGURE 26. OUTPUT RESISTANCE

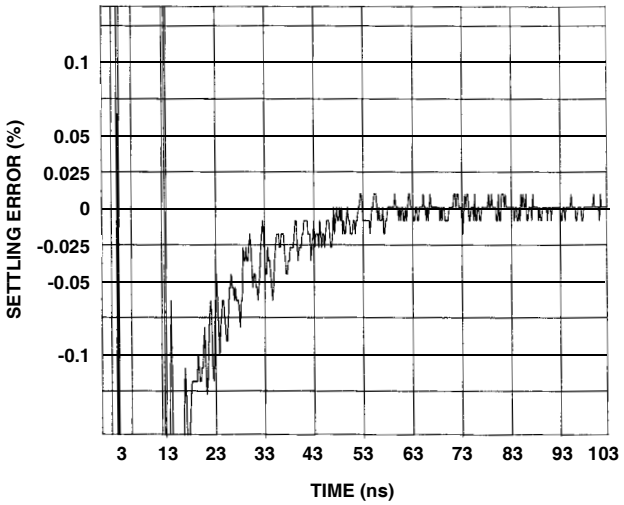



FIGURE 27. SETTLING TIME RESPONSE

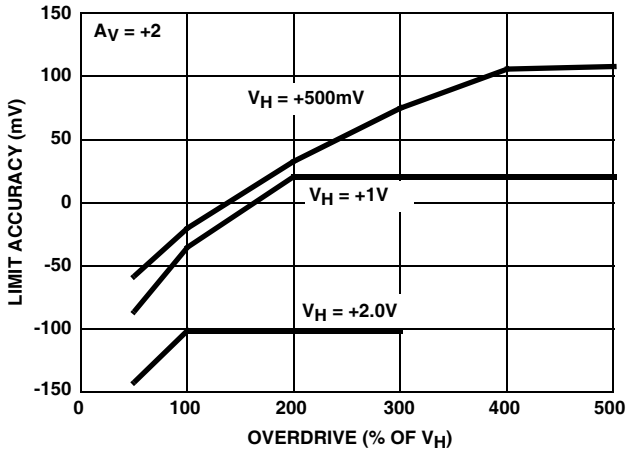



FIGURE 28. $V_H$ LIMIT ACCURACY vs OVERDRIVE

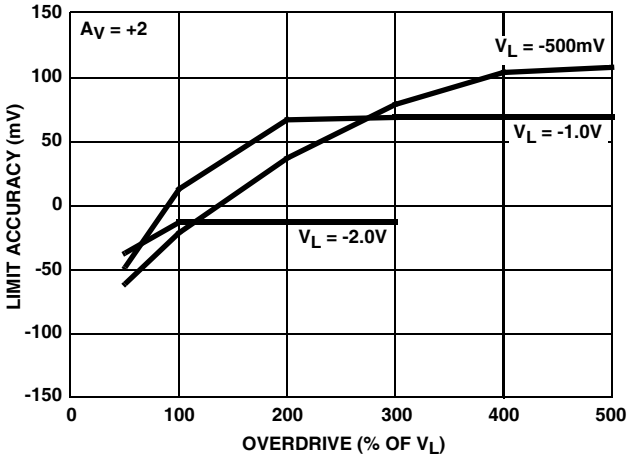



FIGURE 29. $V_L$ LIMIT ACCURACY vs OVERDRIVE

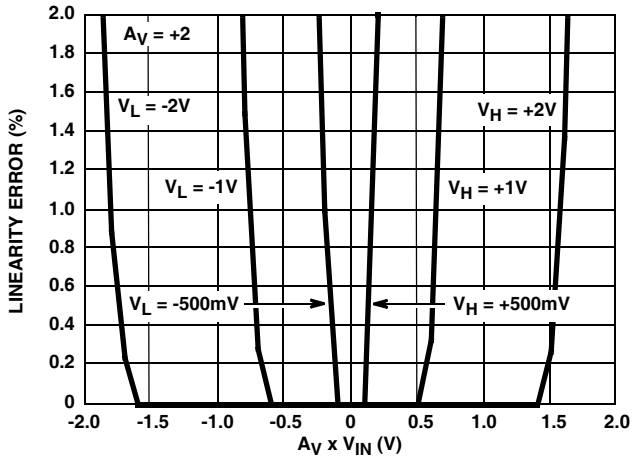



FIGURE 30. LINEARITY NEAR LIMIT VOLTAGE

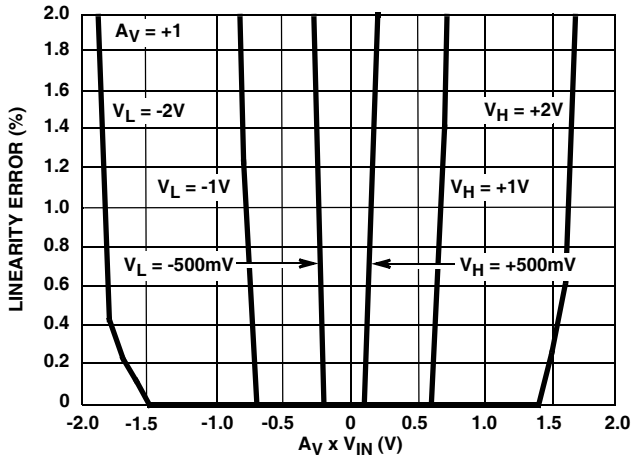



FIGURE 31. LINEARITY NEAR LIMIT VOLTAGE

## Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

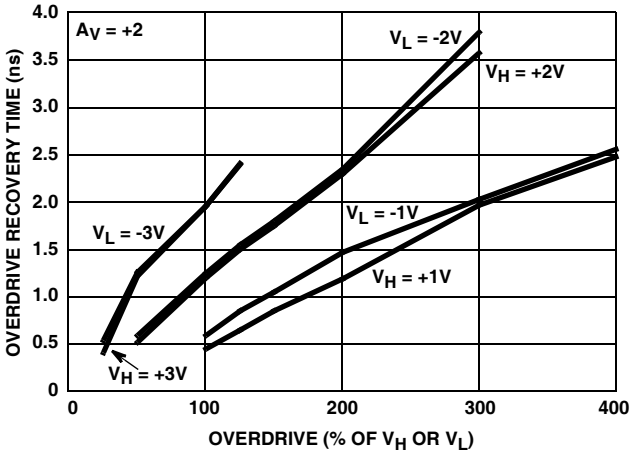



FIGURE 32. OVERDRIVE RECOVERY TIME vs OVERDRIVE

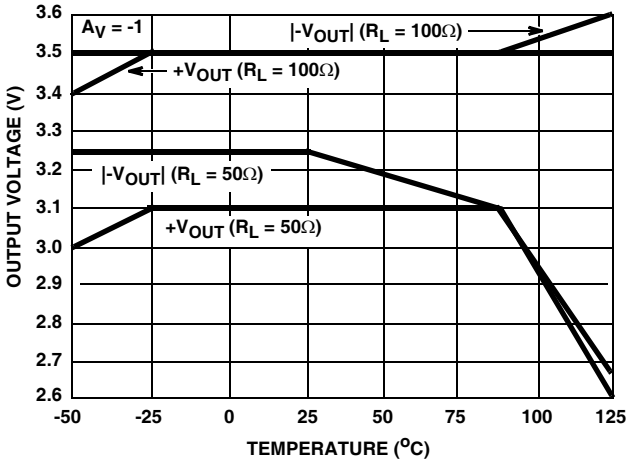



FIGURE 33. OUTPUT VOLTAGE vs TEMPERATURE

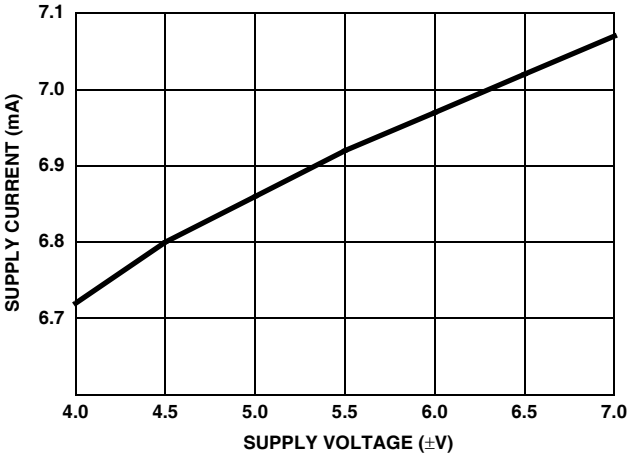



FIGURE 34. SUPPLY CURRENT vs SUPPLY VOLTAGE

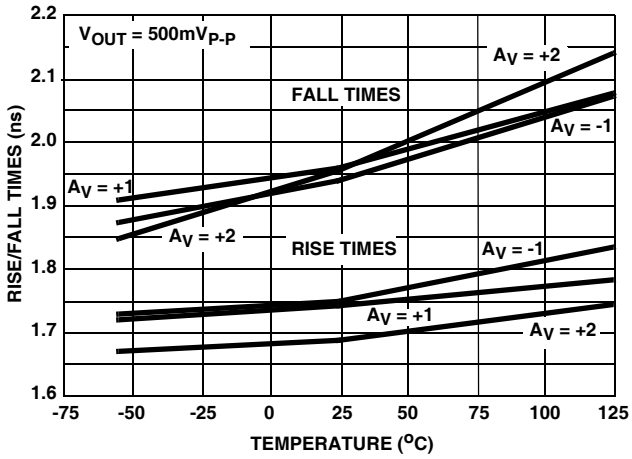



FIGURE 35. RISE AND FALL TIMES vs TEMPERATURE

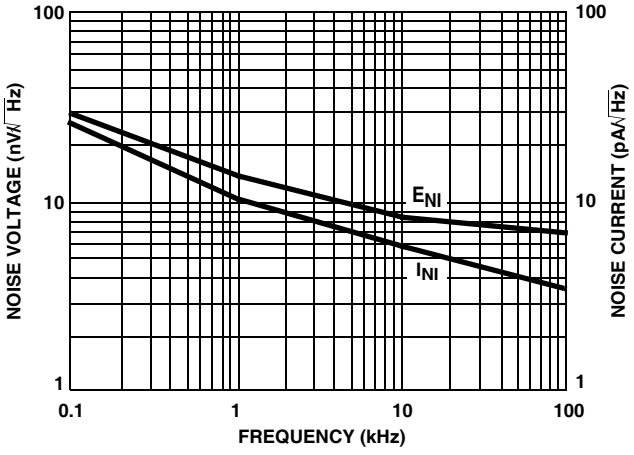



FIGURE 36. INPUT NOISE CHARACTERISTICS

## Die Characteristics

**DIE DIMENSIONS:**

59 mils x 58.2 mils x 19 mils
1500μm x 1480μm x 483μm

**METALLIZATION:**

Type: Metal 1: AlCu(2%)/TiW
Thickness: Metal 1: 8kÅ ±0.4kÅ

Type: Metal 2: AlCu(2%)
Thickness: Metal 2: 16kÅ ±0.8kÅ

**SUBSTRATE POTENTIAL (Powered Up):**

Floating (Recommend Connection to V-)

**PASSIVATION:**

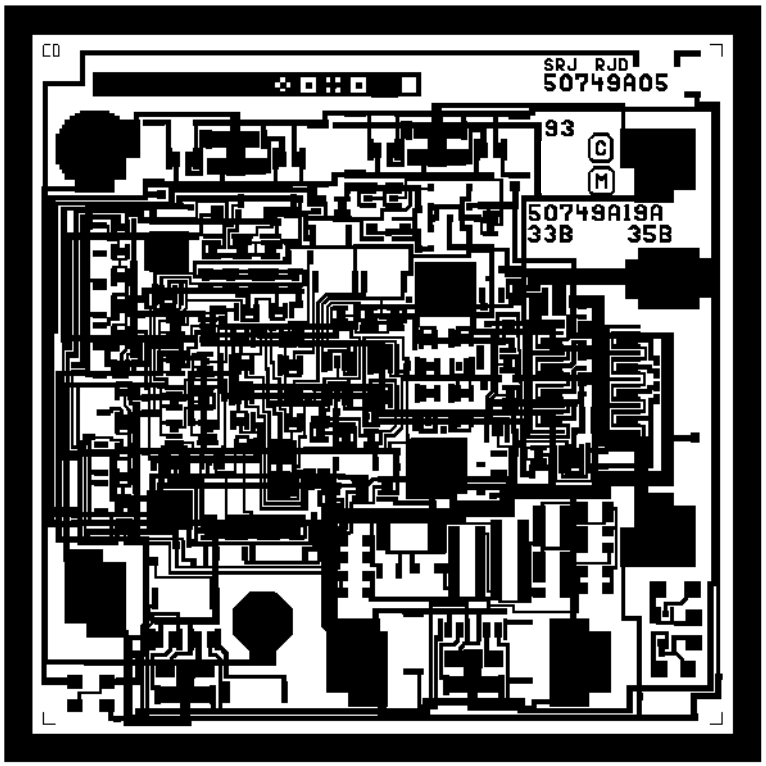
Type: Nitride
Thickness: 4kÅ ±0.5kÅ

**TRANSISTOR COUNT:**

89

## Metallization Mask Layout

**HFA1115**




All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9000 quality systems.
Intersil Corporation's quality certifications can be viewed at www.intersil.com/design/quality

*Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.*

For information regarding Intersil Corporation and its products, see www.intersil.com