

To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

Send any inquiries to <http://www.renesas.com/inquiry>.

Notice

1. All information included in this document is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas Electronics products listed herein, please confirm the latest product information with a Renesas Electronics sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas Electronics such as that disclosed through our website.
2. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
3. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part.
4. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
5. When exporting the products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. You should not use Renesas Electronics products or the technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.
6. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
7. Renesas Electronics products are classified according to the following three quality grades: “Standard”, “High Quality”, and “Specific”. The recommended applications for each Renesas Electronics product depends on the product’s quality grade, as indicated below. You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application categorized as “Specific” without the prior written consent of Renesas Electronics. Further, you may not use any Renesas Electronics product for any application for which it is not intended without the prior written consent of Renesas Electronics. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for an application categorized as “Specific” or for which the product is not intended where you have failed to obtain the prior written consent of Renesas Electronics. The quality grade of each Renesas Electronics product is “Standard” unless otherwise expressly specified in a Renesas Electronics data sheets or data books, etc.
 - “Standard”: Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots.
 - “High Quality”: Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; safety equipment; and medical equipment not specifically designed for life support.
 - “Specific”: Aircraft; aerospace equipment; submersible repeaters; nuclear reactor control systems; medical equipment or systems for life support (e.g. artificial life support devices or systems), surgical implantations, or healthcare intervention (e.g. excision, etc.), and any other applications or purposes that pose a direct threat to human life.
8. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

7300 PIXELS × 3 COLOR CCD LINEAR IMAGE SENSOR

DESCRIPTION

The μ PD8835 is a very high-speed color CCD (Charge Coupled Device) linear image sensor which changes optical images to electrical signal and has the function of color separation. The μ PD8835 has the high speed voltage amplifiers, which have four outputs per color, and the high speed registers, so it is possible that the image of the high density is read at very high speed. Therefore, it is suitable for very high-speed 600dpi/A3 color digital copiers, color scanners and so on, by the package with heat sink that has high heat radiation.

FEATURES

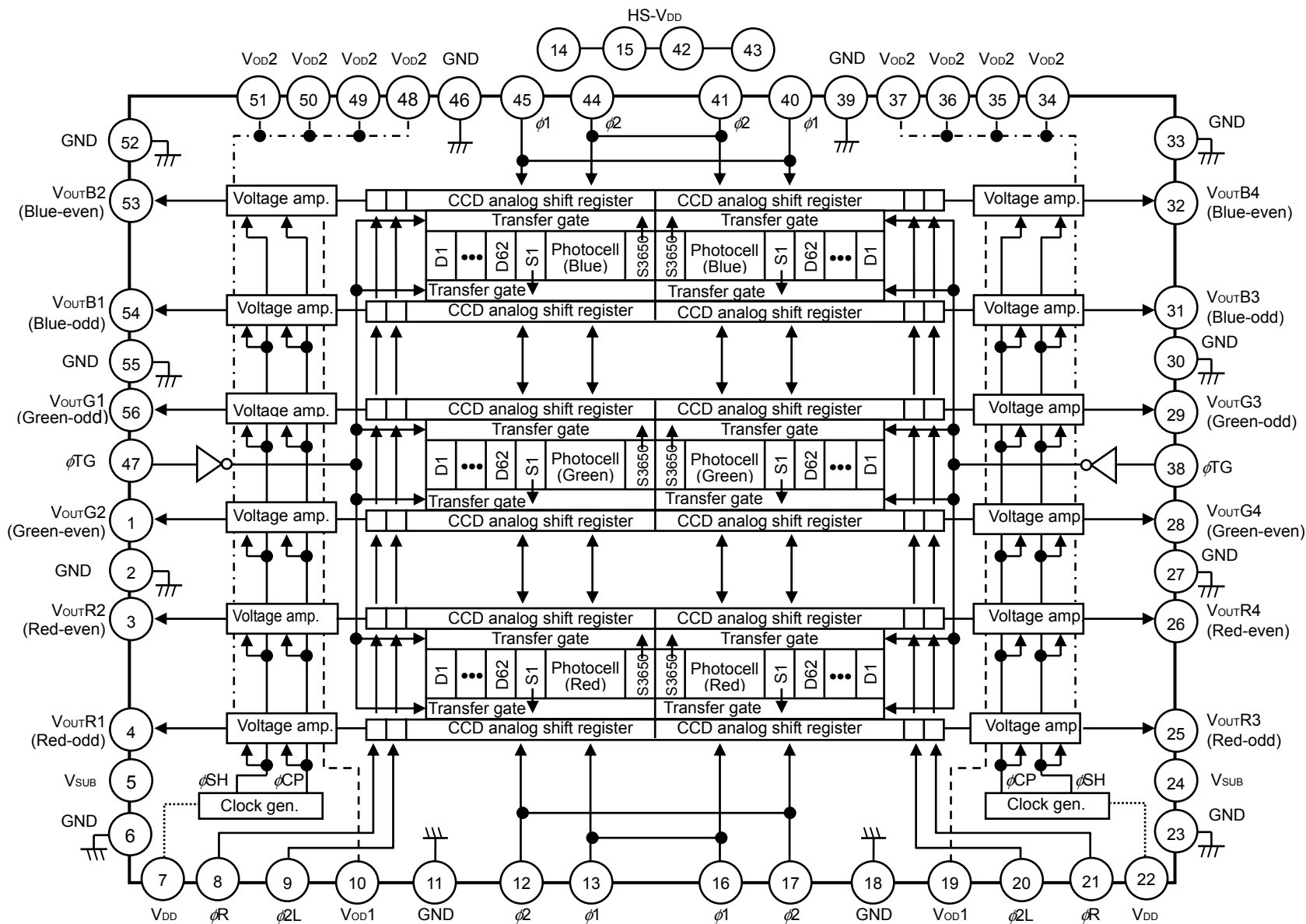
- Valid photocell : 7300 pixels × RGB 3 lines
- Photocell's size : 10 μm
- Line spacing : 40 μm (4 lines) Red line - Green line, Green line - Blue line
- Color filter : Primary colors (Red, Green, and Blue), Pigment filter
Light resistance 10⁷ lx hour with standard sunlight and ultraviolet cut filter (L40)
- Resolution : 24 dot/mm A3 (297 × 420 mm) size (shorter side)
- Data rate : 140 MHz/color max. (35 MHz/ch max.)
- Power supply : +10 V and +5 V
- Drive clock level : CMOS output under 5 V operation
- On-chip circuits : Voltage amplifiers
Reset feed-through level clamp circuit
Clamp clock generation circuit
Sample and Hold circuit
Sample and Hold clock generation circuit
- Output type : 4 outputs / color, Front & Rear separate type
Sample and Hold mode only

ORDERING INFORMATION

Part Number	Package
μPD8835CU-A	CCD linear image sensor 56-pin plastic DIP with heat sink (15.24 mm (600)), 1.778 mm pitch

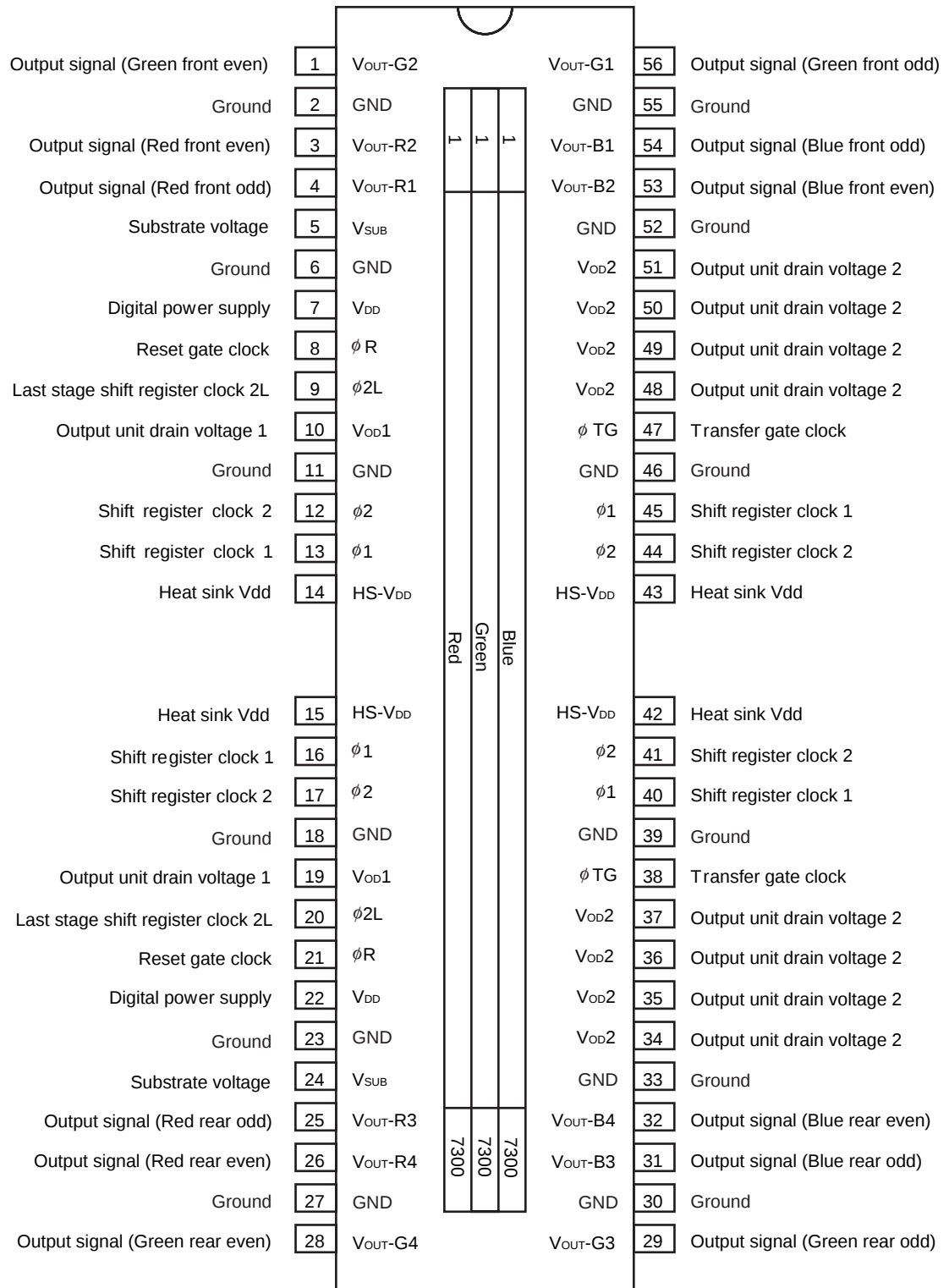
Remark "-A" indicates Pb-free (This product does not contain Pb in external electrode and other parts).

BLOCK DIAGRAM

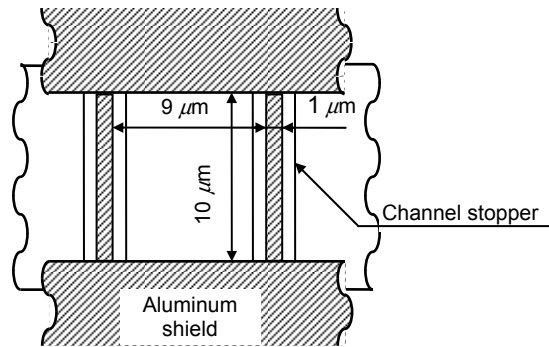


PIN CONFIGURATION (Top View)

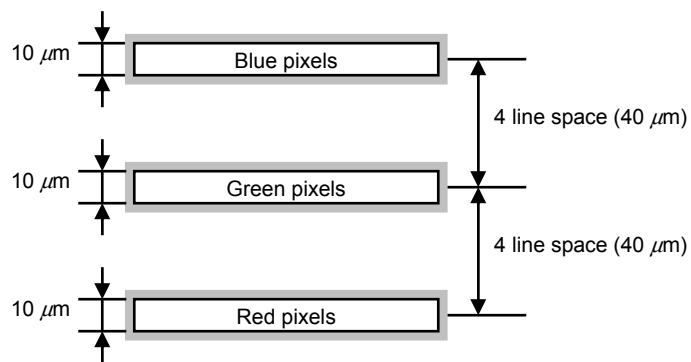
CCD linear image sensor 56-pin plastic DIP with heat sink (15.24 mm (600)) 1.778 mm pitch



PHOTOCELL STRUCTURE DIAGRAM



PHOTOCELL ARRAY STRUCTURE DIAGRAM



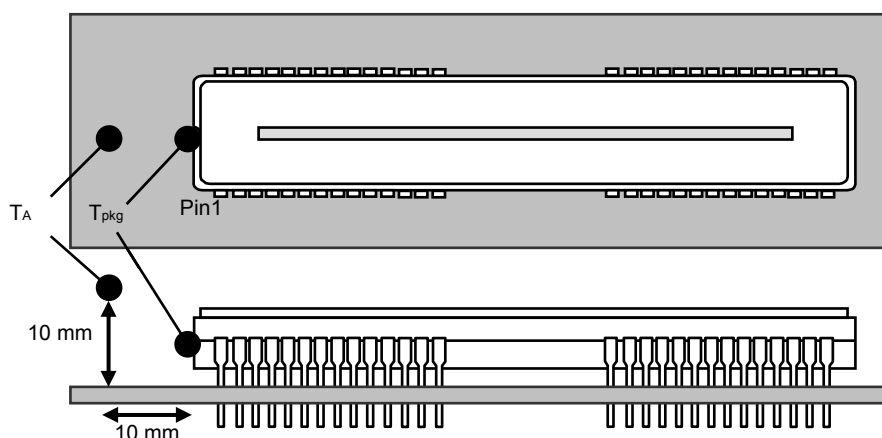
ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Ratings	Unit
Output drain voltage	V_{OD1}, V_{OD2}	-0.3 to +12.0	V
Digital power supply	V_{DD}	-0.3 to +8.0	V
Substrate voltage	V_{SUB}	-0.3 to +8.0	V
Heat sink V_{DD}	HS- V_{DD}	-0.3 to +8.0	V
Voltage difference between V_{DD} and V_{SUB}	$V_{DD}-V_{SUB}$	-0.5 to +0.5	V
Shift register clock voltage	$V_{\phi1}, V_{\phi2}$	-0.3 to +8.0	V
Last stage shift register clock voltage	$V_{\phi2L}$	-0.3 to +8.0 ^{Note 1}	V
Reset gate clock voltage	$V_{\phi R}$	-0.3 to +8.0 ^{Note 1}	V
Transfer gate clock voltage	$V_{\phi TG}$	-0.3 to +8.0	V
Operating ambient temperature ^{Note 2}	T_A	0 to +60	°C
Package surface temperature ^{Note 3}	T_{pkg}	0 to +75	°C
Storage temperature	T_{stg}	-40 to +100	°C

Notes 1. Be careful so that the voltage of $V_{\phi2L}$ and $V_{\phi R}$ are not beyond $V_{DD} + 0.3V$.

2. The operating ambient temperature T_A is defined as an atmosphere temperature in a point 10 mm away on the circuit board, and 10 mm away from the short side of package pin 1. Refer to the below figure.

3. The package surface temperature T_{pkg} is defined as a surface temperature of package short side of pin1. Refer to the below figure.



Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

RECOMMENDED POWER ON/OFF SEQUENCE

The power on/off sequence is not limited. But, when V_{OD1} and V_{OD2} are powered, avoid V_{SUB} and V_{DD} being unsettled (i.e. high impedance).

Prevent V_{DD} and V_{SUB} from being powered on/off separately.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Output drain voltage	V_{OD1}, V_{OD2}	9.5	10.0	10.5	V
Digital power supply	V_{DD}	4.75	5.0	5.4	V
Substrate voltage	V_{SUB}	4.75	5.0	5.4	V
Heat sink V_{DD}	HS- V_{DD}	4.75	5.0	5.4	V
Voltage difference between V_{DD} and V_{SUB}	$V_{DD}-V_{SUB}$	-0.3	0.0	0.3	V
Shift register clock high level	$V_{\phi 1H}, V_{\phi 2H}$	4.75	5.0	6.0	V
Shift register clock low level	$V_{\phi 1L}, V_{\phi 2L}$	-0.3	0.0	0.3	V
Last stage shift register clock high level	$V_{\phi 2LH}$	4.75	5.0	$V_{DD}+0.3$	V
Last stage shift register clock low level	$V_{\phi 2LL}$	-0.3	0.0	0.3	V
Reset gate clock high level	$V_{\phi RH}$	4.75	5.0	$V_{DD}+0.3$	V
Reset gate clock low level	$V_{\phi RL}$	-0.3	0.0	0.3	V
Transfer gate clock high level	$V_{\phi TGH}$	4.75	5.0	6.0	V
Transfer gate clock low level	$V_{\phi TGL}$	-0.3	0.0	0.3	V
Shift register clock amplitude	$V_{p-p\phi 1}, V_{p-p\phi 2}$	4.75	5.0	6.3	V
Transfer gate clock amplitude	$V_{p-p\phi TG}$	4.75	5.0	6.3	V
Signal output data rate	$f_{\phi R}$	0.1	1	35	MHz
Clock rate	$f_{\phi 1}, f_{\phi 2}$	0.1	1	35	MHz

ELECTRICAL CHARACTERISTICS

T_A = +25°C, V_{OD1} = V_{OD2} = +10 V, V_{DD} = V_{SUB} = +5 V, f_{φR} = 1 MHz, Data rate = 1 MHz, Storage time = 10 ms, Input clock = 5 Vp-p

Light source (except Response2): 3200 K halogen lamp + C-500S (Infrared cut filter, t = 1 mm) + HA-50 (Heat absorbing filter, t = 3 mm)

Parameter		Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Saturation voltage		V _{sat}		1.2	1.5	–	V
Saturation exposure	Red	SE(R)		–	0.14	–	lx•s
	Green	SE(G)		–	0.16	–	
	Blue	SE(B)		–	0.3	–	
Photo response non-uniformity		PRNU1(-)	V _{OUT} = 1 V	–	6	18	%
		PRNU1(+)		–	6	11	
Average dark signal		ADS	Light shielding	–	0.1	5.0	mV
Dark signal non-uniformity		DSNU	Light shielding	–	2.0	10.0	mV
	Power consumption (V _{OD1})	P _{OD1}		–	790	950	mW
	Power consumption (V _{OD2})	P _{OD2}		–	960	1150	
	Power consumption (V _{DD})	P _{DD}	f _{φR} = 35 MHz	–	69	90	
	Power consumption (V _{SUB})	P _{SUB}		–	1	20	
Total power consumption		P _W	f _{φR} = 35 MHz	–	1820	2210	
Output impedance		Z _O		–	0.15	0.4	kΩ
Response1	Red	R _R		7.8	10.5	13.2	V/lx•s
	Green	R _G		6.9	9.2	11.5	
	Blue	R _B		3.75	5.0	6.25	
Response2 (Corresponding value from Response1)	Red	R _R	A light source + CM500S	–	(9.8)	–	V/lx•s
	Green	R _G		–	(9.0)	–	
	Blue	R _B		–	(4.5)	–	
Response peak	Red			–	610	–	nm
	Green			–	535	–	
	Blue			–	460	–	
Image lag		IL	V _{OUT} = 1 V	–	1	20	mV
Offset level		V _{OS}		4.0	5.0	6.0	V
Output settling time ^{Note}		ts1	V _{OUT} = 1 V	2	3	4	ns
		ts2		5.5	7	8.5	
Register imbalance		RI	V _{OUT} = 1 V	–	2.0	10.0	%
		RI-FR	V _{OUT} = 1 V	–	2.0	10.0	%
Total transfer efficiency		TTE	V _{OUT} = 1 V, f _{φ1} = 35 MHz	94	98	–	%
Dynamic range		DR1	V _{sat} /DSNU	–	750	–	times
		DR2	V _{sat} /σ _{dark}	–	1875	–	
Light shielding random noise		σ _{dark}		–	0.8	–	mV

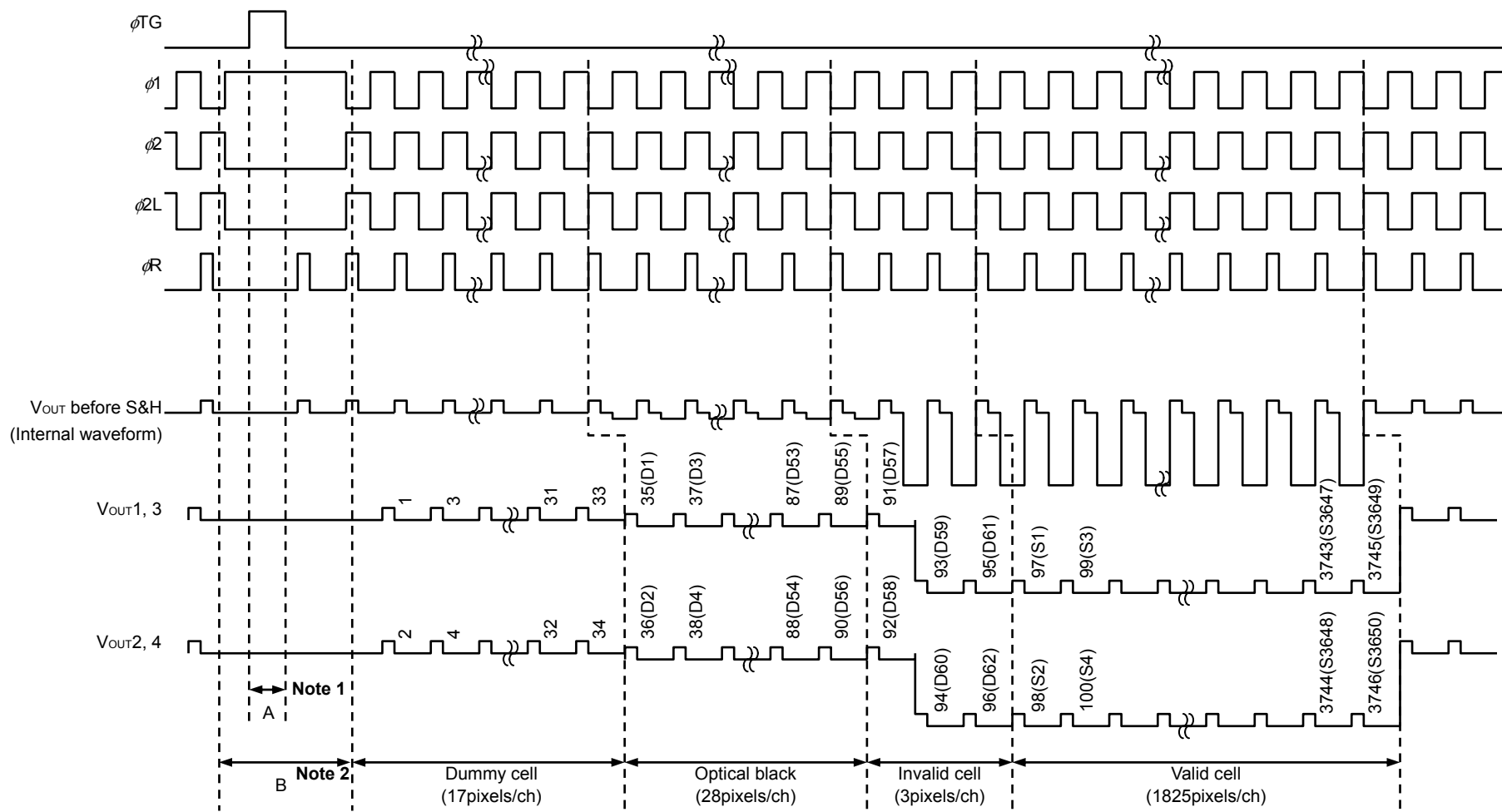
Note Definitions of ts1 and ts2 are indicated in the **TIMING CHART 2**.

INPUT PIN CAPACITANCE ($V_{OD1} = V_{OD2} = +10\text{ V}$, $V_{DD} = V_{SUB} = +5\text{ V}$)

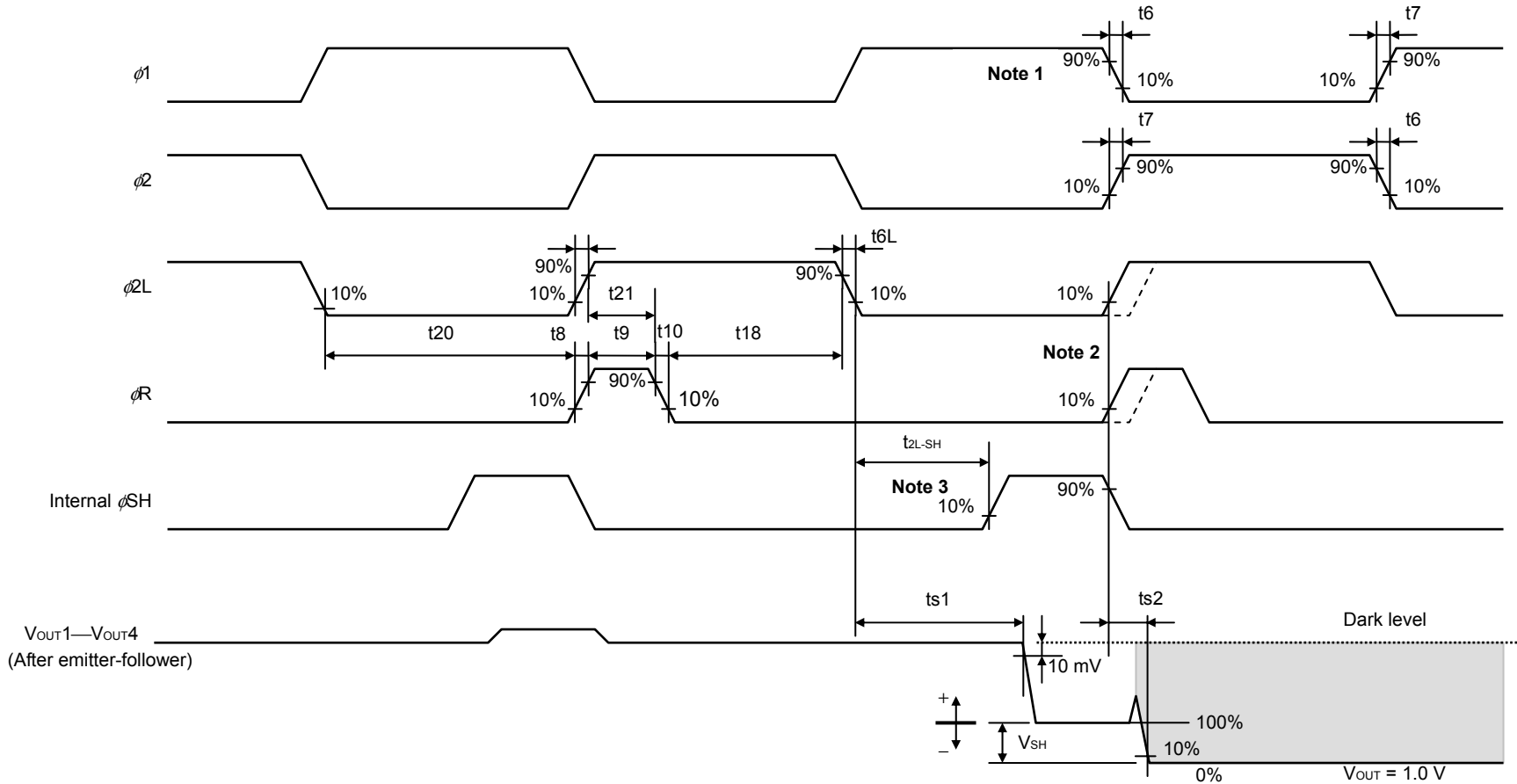
Parameter	Symbol	Pin name	Pin No.	MIN.	TYP.	MAX.	Unit
Shift register clock pin capacitance ^{Note}	$C_{\phi 1}$	$\phi 1$	13	215	240	265	pF
			16	215	240	265	
			40	215	240	265	
			45	215	240	265	
		TOTAL		860	960	1060	
	$C_{\phi 2}$	$\phi 2$	12	215	240	265	pF
			17	215	240	265	
			41	215	240	265	
			44	215	240	265	
		TOTAL		860	960	1060	
Last stage shift register clock pin capacitance	$C_{\phi 2L}$	$\phi 2L$	9	11	12	13	pF
			20	11	12	13	
Reset gate clock pin capacitance	$C_{\phi R}$	ϕR	8	11	12	13	pF
			21	11	12	13	
Transfer gate clock pin capacitance	$C_{\phi TG}$	ϕTG	38	2	3	4	pF
			47	2	3	4	

Note $C_{\phi 1}$ and $C_{\phi 2}$ are equivalent capacitance with driving device, including the co-capacitance between $\phi 1$ and $\phi 2$.
Pin 13, 16, 40 and 45 ($\phi 1$) are connected inside of the device. Pin 12, 17, 41 and 44 ($\phi 2$) are also connected inside of the device.

TIMING CHART 1



TIMING CHART 2

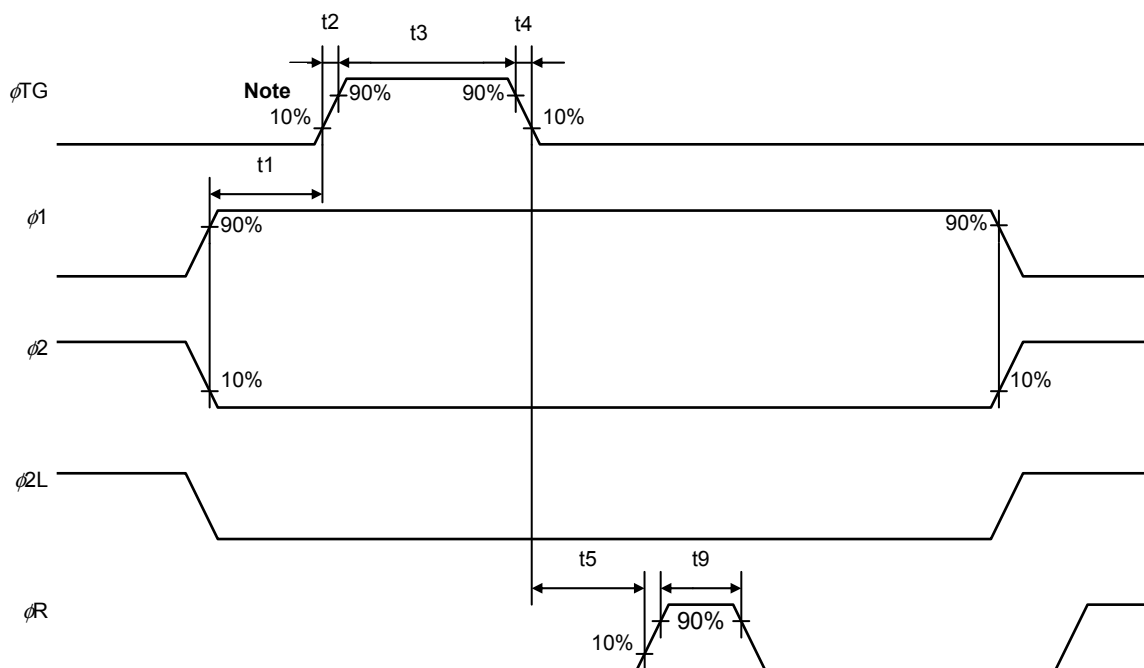


Notes 1. '10%' and '90%' are defined as a ratio against the amplitude of the clock.

2. $ts2$ is defined by earlier timing of either ϕR or $\phi2L$.

3. t_{2L-SH} is a period between external $\phi2L$ and internal ϕSH . The design value of t_{2L-SH} is 0 ns.

TIMING CHART 3 (The period B of TIMING CHART 1)



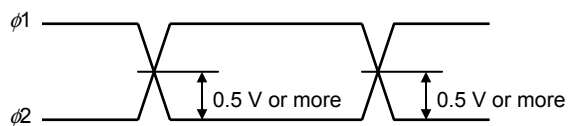
Note '10%' and '90%' are defined as a ratio against the amplitude of the clock.

Symbol	MIN.	TYP.	MAX.	Unit
t1	100	200	1000	ns
t2, t4	0	10	—	ns
t3	1000	2000	5000	ns
t5	300	500	5000	ns
t6, t7	0	10	—	ns
t6L, t7L	0	3	10	ns
t8, t10	0	3	10	ns
t9	2	$T^{\text{Note}}/4$	—	ns
t11	300	500	5000	ns
t18	3	$T^{\text{Note}}/4$	—	ns
t20	10	$T^{\text{Note}}/2$	—	ns
t21	0	t9	—	ns

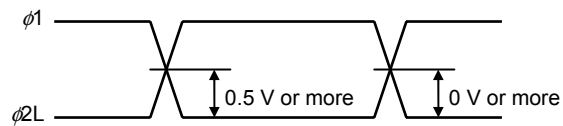
Note 'T' means 1 period.

CROSS POINTS

($\phi 1$, $\phi 2$) CROSS POINTS

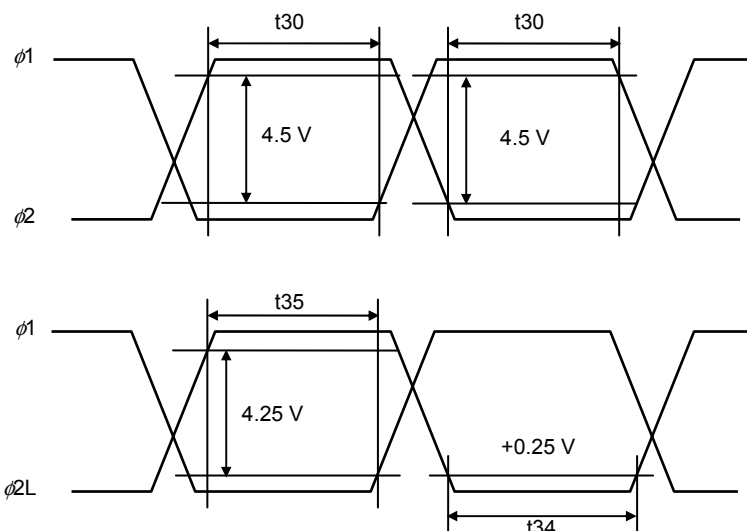


($\phi 1$, $\phi 2L$) CROSS POINTS



Remark Adjust cross points of ($\phi 1$, $\phi 2$) and ($\phi 1$, $\phi 2L$) with an input resistance of each pin.

CLOCK HIGH AND LOW LEVEL WIDTH



Symbol	MIN.	TYP.	MAX.	Unit
t30	3	—	—	ns
t34	10	—	—	ns
t35	3	—	—	ns

DEFINITIONS OF CHARACTERISTICS

1. Saturation voltage: V_{sat}

The output signal voltage at which the response linearity is lost

2. Saturation exposure: SE

Product of intensity of illumination (lx) and storage time (s) when saturation of output voltage occurs

3. Photo response non-uniformity: PRNU1

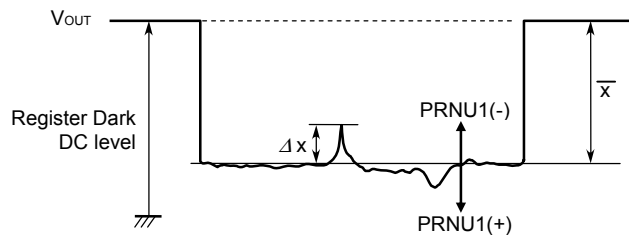
The output signal non-uniformity of all the valid pixels when the photosensitive surface is applied with the light of uniform illumination. This is calculated by the following formula, and it is defined by each twelve of them.

$$\text{PRNU1 (\%)} = \frac{\Delta x}{\bar{x}} \times 100$$

$$\bar{x} = \frac{\sum_{j=1}^{1825} x_j}{1825}$$

Δx : maximum of $|x_j - \bar{x}|$

x_j : Output voltage of valid pixel number j



4. Average dark signal: ADS

Average output signal voltage of all the valid pixels at light shielding. This is calculated by the following formula, and it is defined by each twelve of them.

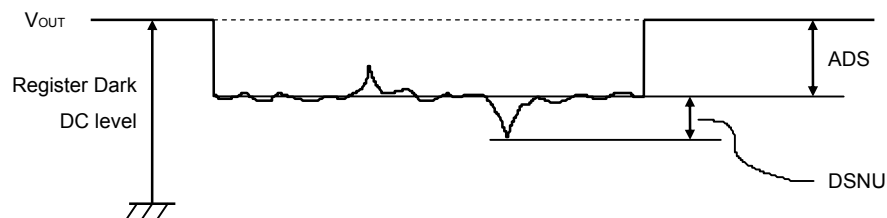
$$\text{ADS (mV)} = \frac{\sum_{j=1}^{1825} d_j}{1825} \quad d_j : \text{Dark signal of valid pixel number } j$$

5. Dark signal non-uniformity: DSNU

Absolute maximum of the difference between ADS and voltage of the highest or lowest output pixel of all the valid pixels at light shielding. This is calculated by the following formula, and it is defined by each twelve of them.

$\text{DSNU (mV)} : \text{maximum of } |d_j - \text{ADS}| \quad j = 1 \text{ to } 1825$

d_j : Dark signal of valid pixel number j



6. Output impedance: Z_o

Impedance of the output pins viewed from outside

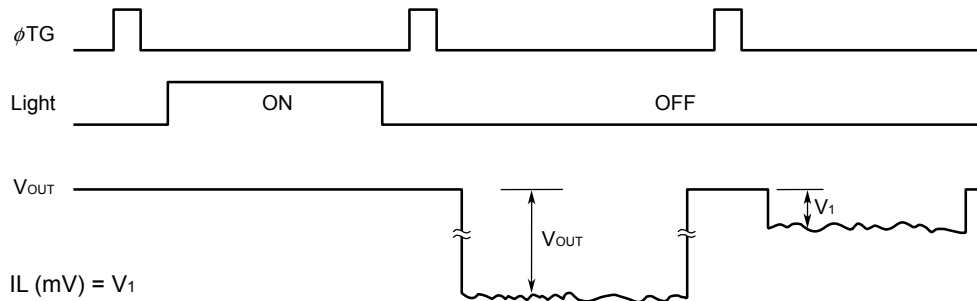
7. Response: R

Output voltage divided by exposure ($I_x \cdot s$)

Note that the response varies with a light source (spectral characteristic).

8. Image lag: IL

The rate between the last output voltage and the next one after read out the data of a line



9. Register imbalance: RI , $RI-FR$

RI is the rate of the difference between the averages of the output voltage of odd pixels and even pixels, against the average output voltage of all the valid pixels. The RI is calculated between V_{OUT1} and V_{OUT2} and between V_{OUT3} and V_{OUT4} . The $RI-FR$ is defined as RI between Front and Rear.

$$RI (\%) = \frac{\frac{2}{n} \left| \sum_{j=1}^{\frac{n}{2}} (V_{2j-1} - V_{2j}) \right|}{\frac{1}{n} \sum_{j=1}^n V_j} \times 100$$

n : Number of valid pixels (1 to 1825)
 V_j : Output voltage of each pixel

$$RI-FR(\%) = \frac{|V_{OUT(F)} - V_{OUT(R)}|}{(V_{OUT(F)} + V_{OUT(R)})/2} \times 100$$

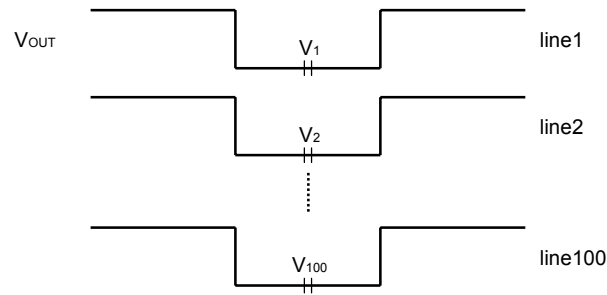
$V_{OUT(F)}$: Average output voltage of V_{OUT1} and V_{OUT2}
 $V_{OUT(R)}$: Average output voltage of V_{OUT3} and V_{OUT4}

10. Random noise (Light shielding): σ_{dark}

Light shielding random noise σ_{dark} is defined as the standard deviation of a valid pixel output signal with 100 times (= 100 lines) data sampling at dark (light shielding). This is measured by the DC level sampling of only the signal level, not by CDS (Correlated Double Sampling).

$$\sigma \text{ (mV)} = \sqrt{\frac{\sum_{i=1}^{100} (V_i - \bar{V})^2}{100}}, \quad \bar{V} = \frac{1}{100} \sum_{i=1}^{100} V_i$$

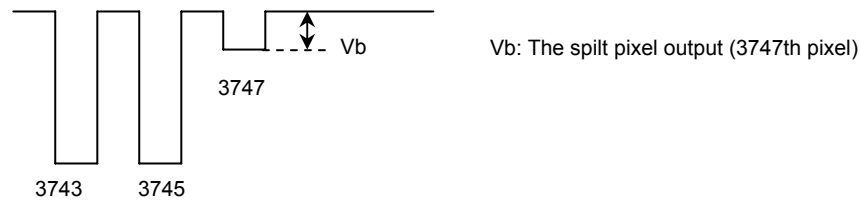
V_i : A valid pixel output signal among all of the valid pixels for each color.



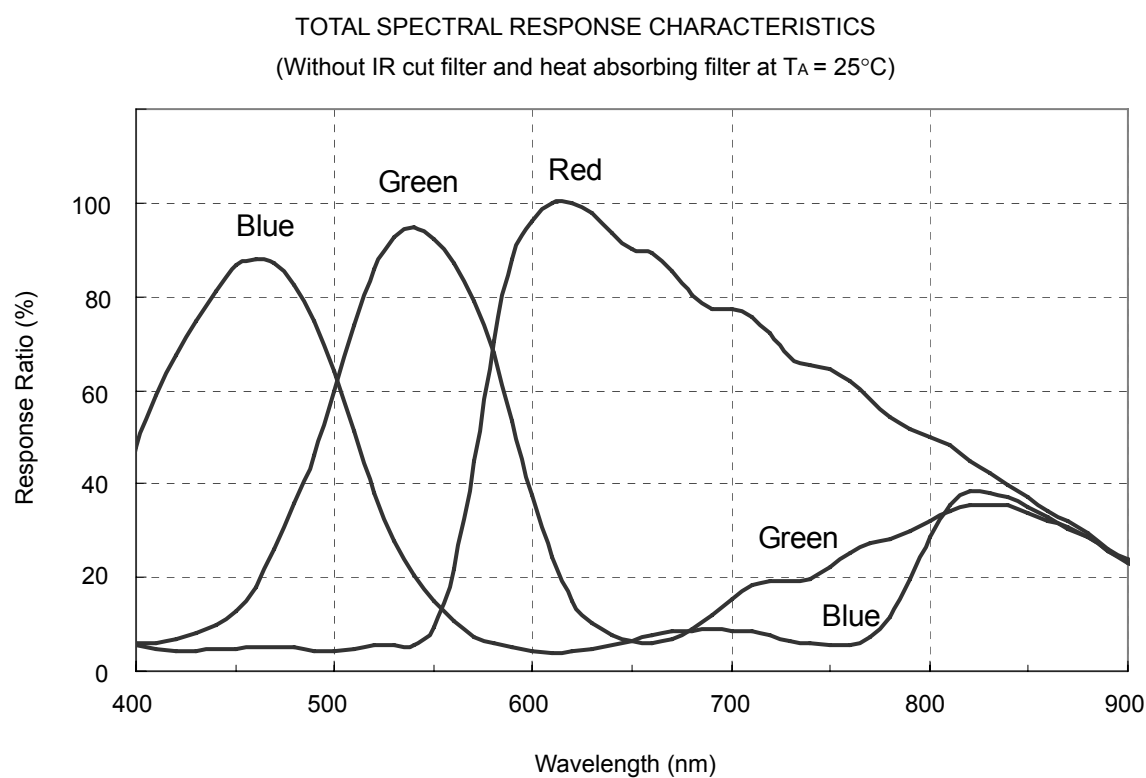
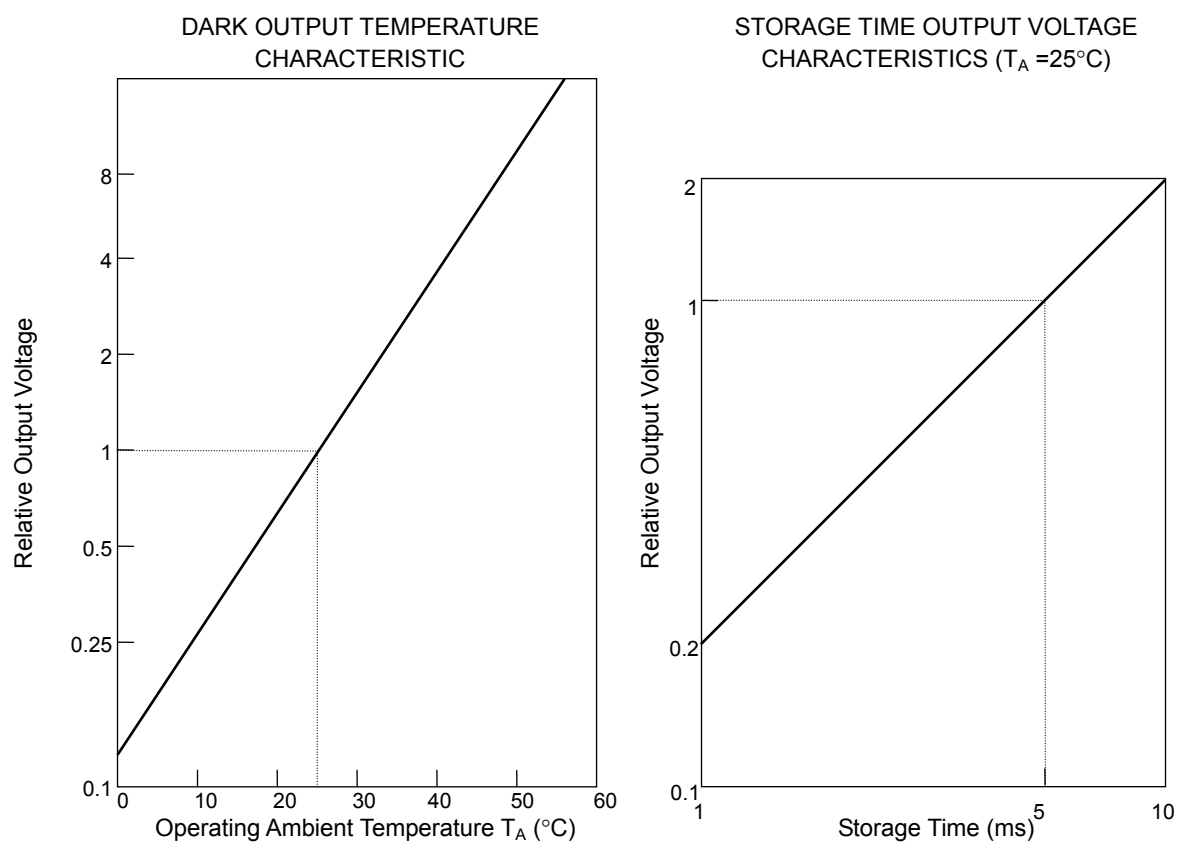
11. Total transfer efficiency: TTE

TTE is the total transfer rate of CCD analog shift register. This is calculated by the following.

$$\text{TTE (\%)} = (1 - V_b / \text{Average output of all the valid pixels}) \times 100$$

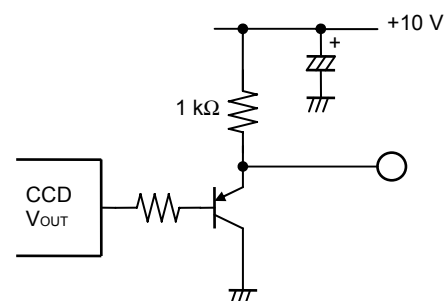


STANDARD CHARACTERISTIC CURVES (Nominal)



[illegible]

- ## B1 to B4, G1 to G4, and R1 to R4 EQUIVALENT CIRCUIT



**CCD LINEAR IMAGE SENSOR 56-PIN PLASTIC DIP
(WITH HEAT SINK) (15.24mm(600)) 1.778 mm pitch**

[illegible]

Name	Dimensions	Refractive index
Glass cap	91.0×11.6×0.7	1.5

- ※1 1st valid pixel ↔ The center of the pin1
- ※2 1st valid pixel ↔ The center of the package
- ※3 The surface of the CCD chip ↔ The top of the cap
- ※4 The bottom of the package ↔ The surface of the CCD chip
- ※5 The draft angle of the shaded portions (4 places) are 1 degree.
- ※6 There is no heat sink exposure from the package.
- ※7 The center of the CCD chip ↔ Package side(shaded portion)

© NEC Electronics Corporation 2009

RECOMMENDED SOLDERING CONDITIONS

When soldering this product, it is highly recommended to observe the conditions as shown below.

If other soldering processes are used, or if the soldering is performed under different conditions, please make sure to consult with our sales offices.

Type of Through-hole Device

μPD8835CU-A: CCD linear image sensor 56-pin plastic DIP with heat sink (15.24 mm (600)) 1.778 mm pitch

Process	Conditions
Partial heating method	Pin temperature: 380°C or below, Heat time: 3 seconds or less (per pin).

- Cautions**
1. During assembly care should be taken to prevent solder or flux from contacting the glass cap. The optical characteristics could be degraded by such contact.
 2. Soldering by the solder flow method may have deleterious effects on prevention of glass cap soiling and heat resistance. So the method cannot be guaranteed.

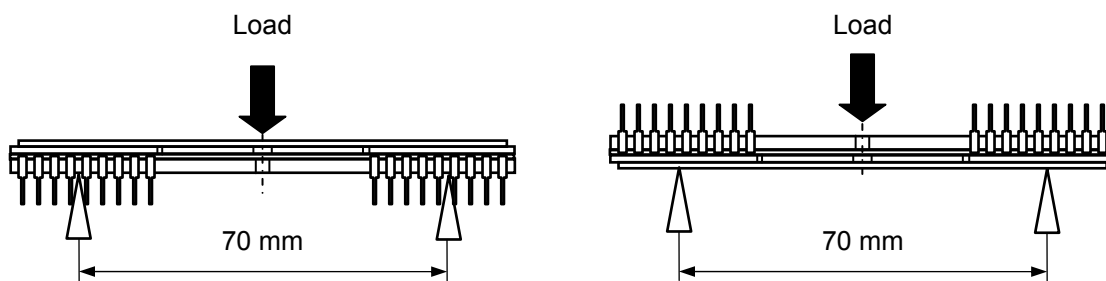
NOTES OF HANDLING THE PACKAGES

The application of an excessive load to the package may cause the package to warp or break, or cause chips to come off internally. Particular care should be taken when mounting the package on the circuit board. You should not reform the lead frame. We recommend to use a IC-inserter when you assemble to PCB.

For this product, the reference value for the three-point bending strength Note is 280[N]. Avoid imposing a load, however, on the inside portion as viewed from the face on which the window (glass) is bonded to the package body.

Note Three-point bending strength test

Distance between supports: 70 mm, Support R: R2 mm, Loading rate: 0.5 mm/min.



NOTES OF HANDLING

1. MOUNTING OF THE PACKAGE

The application of an excessive load to the package may cause the package to warp or break, or cause chips to come off internally. Particular care should be taken when mounting the package on the circuit board. Don't have any object come in contact with glass cap. You should not reform the lead frame. We recommend to use an IC-inserter when you assemble it to PCB.

Also, be care that any of the following can cause the package to crack or dust to be generated.

1. Applying heat to the external leads for an extended period of time with soldering iron.
2. Rapid cooling or heating
3. Applying repetitive bending stress to the external leads.

2. GLASS CAP

Don't either touch glass cap surface by hand or have any object come in contact with glass cap surface. Care should be taken to avoid mechanical or thermal shock because the glass cap is easily to damage. For dirt stuck through electricity ionized air is recommended.

3. OPERATE AND STORAGE ENVIRONMENTS

Operate in clean environments. CCD image sensors are precise optical equipment that should not be subject to mechanical shocks. Exposure to high temperatures or humidity will affect the characteristics. So avoid storage or usage in such conditions.

Keep in a case to protect from dust and dirt. Dew condensation may occur on CCD image sensors when the devices are transported from a low-temperature environment to a high-temperature environment. Avoid such rapid temperature changes.

For more detail, refer to our document "Review of Quality and Reliability Handbook" (C12769E)

4. ELECTROSTATIC BREAKDOWN

CCD image sensor is protected against static electricity, but destruction due to static electricity is something detected. Before handling, be sure to take the following protective measures.

1. Ground the tools such as soldering iron, radio cutting pliers or of pincer.
2. Install a conductive mat or on the floor or working table to prevent the generation of static electricity.
3. Either handle bare handed or use non chargeable gloves, clothes or material.
4. Ionized air is recommended for discharge when handling CCD image sensor.
5. For the shipment of mounted substrates, use box treated for prevention of static charges.
6. Anyone who is handling CCD image sensors, mounting them on PCB or testing or inspecting PCBs on which semiconductor devices have been mounted must wear anti-static bands such as wrist straps and ankle straps which are grounded via a series resistance connection of about 1M Ω .

NOTES FOR CMOS DEVICES

- (1) **VOLTAGE APPLICATION WAVEFORM AT INPUT PIN:** Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).
- (2) **HANDLING OF UNUSED INPUT PINS:** Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.
- (3) **PRECAUTION AGAINST ESD:** A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.
- (4) **STATUS BEFORE INITIALIZATION:** Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.
- (5) **POWER ON/OFF SEQUENCE:** In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.
- (6) **INPUT OF SIGNAL DURING POWER OFF STATE :** Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

- The information in this document is current as of February, 2010. The information is subject to change without notice. For actual design-in, refer to the latest publications of NEC Electronics data sheets or data books, etc., for the most up-to-date specifications of NEC Electronics products. Not all products and/or types are available in every country. Please check with an NEC Electronics sales representative for availability and additional information.
 - No part of this document may be copied or reproduced in any form or by any means without the prior written consent of NEC Electronics. NEC Electronics assumes no responsibility for any errors that may appear in this document.
 - NEC Electronics does not assume any liability for infringement of patents, copyrights or other intellectual property rights of third parties by or arising from the use of NEC Electronics products listed in this document or any other liability arising from the use of such products. No license, express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of NEC Electronics or others.
 - Descriptions of circuits, software and other related information in this document are provided for illustrative purposes in semiconductor product operation and application examples. The incorporation of these circuits, software and information in the design of a customer's equipment shall be done under the full responsibility of the customer. NEC Electronics assumes no responsibility for any losses incurred by customers or third parties arising from the use of these circuits, software and information.
 - While NEC Electronics endeavors to enhance the quality, reliability and safety of NEC Electronics products, customers agree and acknowledge that the possibility of defects thereof cannot be eliminated entirely. To minimize risks of damage to property or injury (including death) to persons arising from defects in NEC Electronics products, customers must incorporate sufficient safety measures in their design, such as redundancy, fire-containment and anti-failure features.
 - NEC Electronics products are classified into the following three quality grades: "Standard", "Special" and "Specific". The "Specific" quality grade applies only to NEC Electronics products developed based on a customer-designated "quality assurance program" for a specific application. The recommended applications of an NEC Electronics product depend on its quality grade, as indicated below. Customers must check the quality grade of each NEC Electronics product before using it in a particular application.
 - "Standard": Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots.
 - "Special": Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support).
 - "Specific": Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems and medical equipment for life support, etc.
- The quality grade of NEC Electronics products is "Standard" unless otherwise expressly specified in NEC Electronics data sheets or data books, etc. If customers wish to use NEC Electronics products in applications not intended by NEC Electronics, they must contact an NEC Electronics sales representative in advance to determine NEC Electronics' willingness to support a given application.
- (Note 1) "NEC Electronics" as used in this statement means NEC Electronics Corporation and also includes its majority-owned subsidiaries.
- (Note 2) "NEC Electronics products" means any product developed or manufactured by or for NEC Electronics (as defined above).

(M8E0909E)