

TOSHIBA Bi-CMOS INTEGRATED CIRCUIT SILICON MONOLITHIC

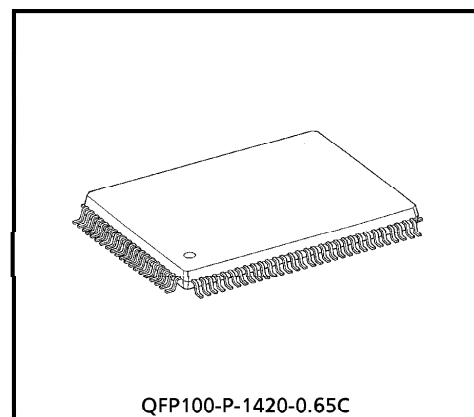
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64BIT SHIFT REGISTER / LATCH DRIVER

The TB62600F is specifically designed for 64bit Thermal Head drivers. And this IC is monolithic integrated circuits designed to be used together with Bi-CMOS (DMOS) integrated circuit. The devices consist of a 64bit shift register, dual 64bit latches, and 64 output DMOS structures.

FEATURE

- Built-in selection circuit : parallel-in parallel-out (8×8) or serial-in parallel-out (1×64)
- CMOS compatible inputs
- Open-drain DMOS outputs
- Low steady-state power consumption
- Built-in mono stable multi-vibrator for head protection
- Package : QFP100-P-1420C

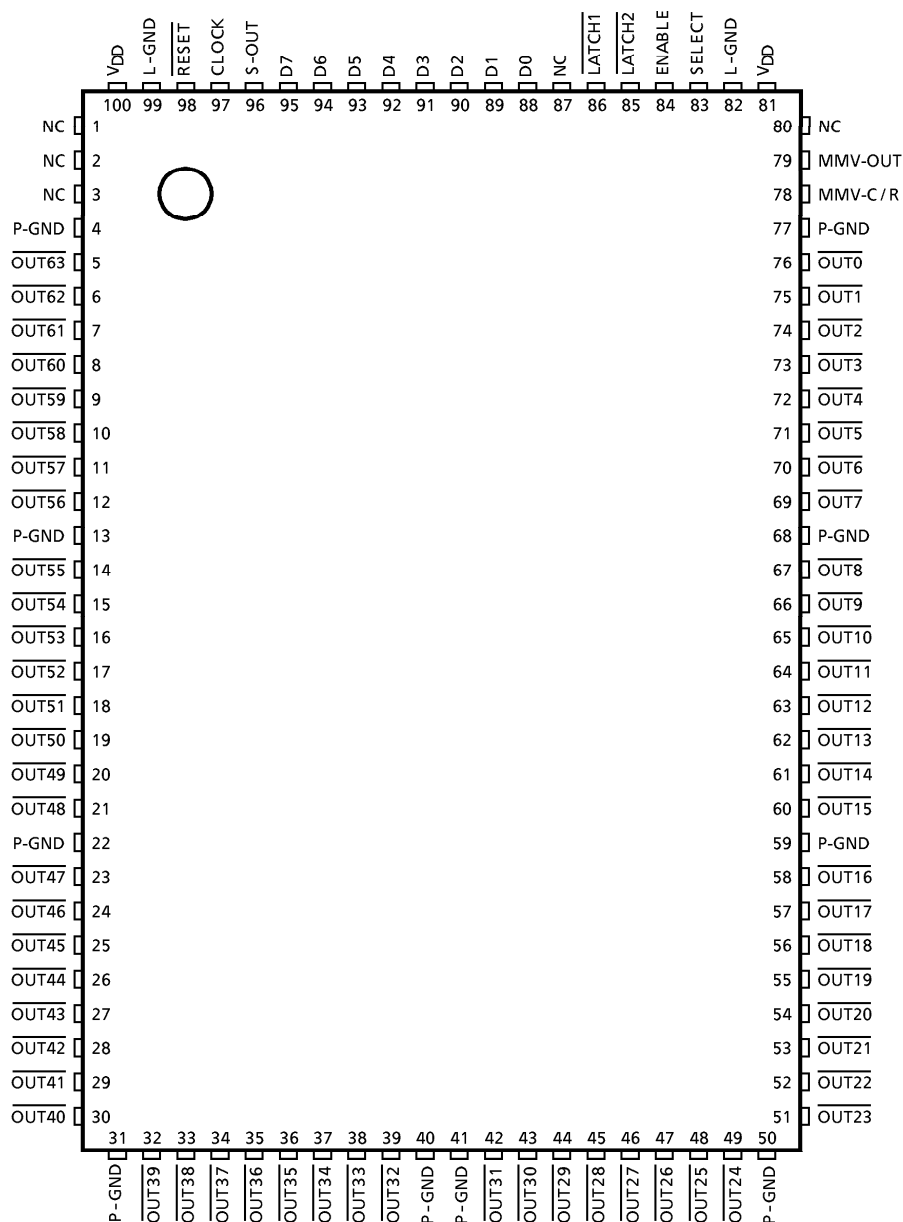


Weight : 1.6g (Typ.)

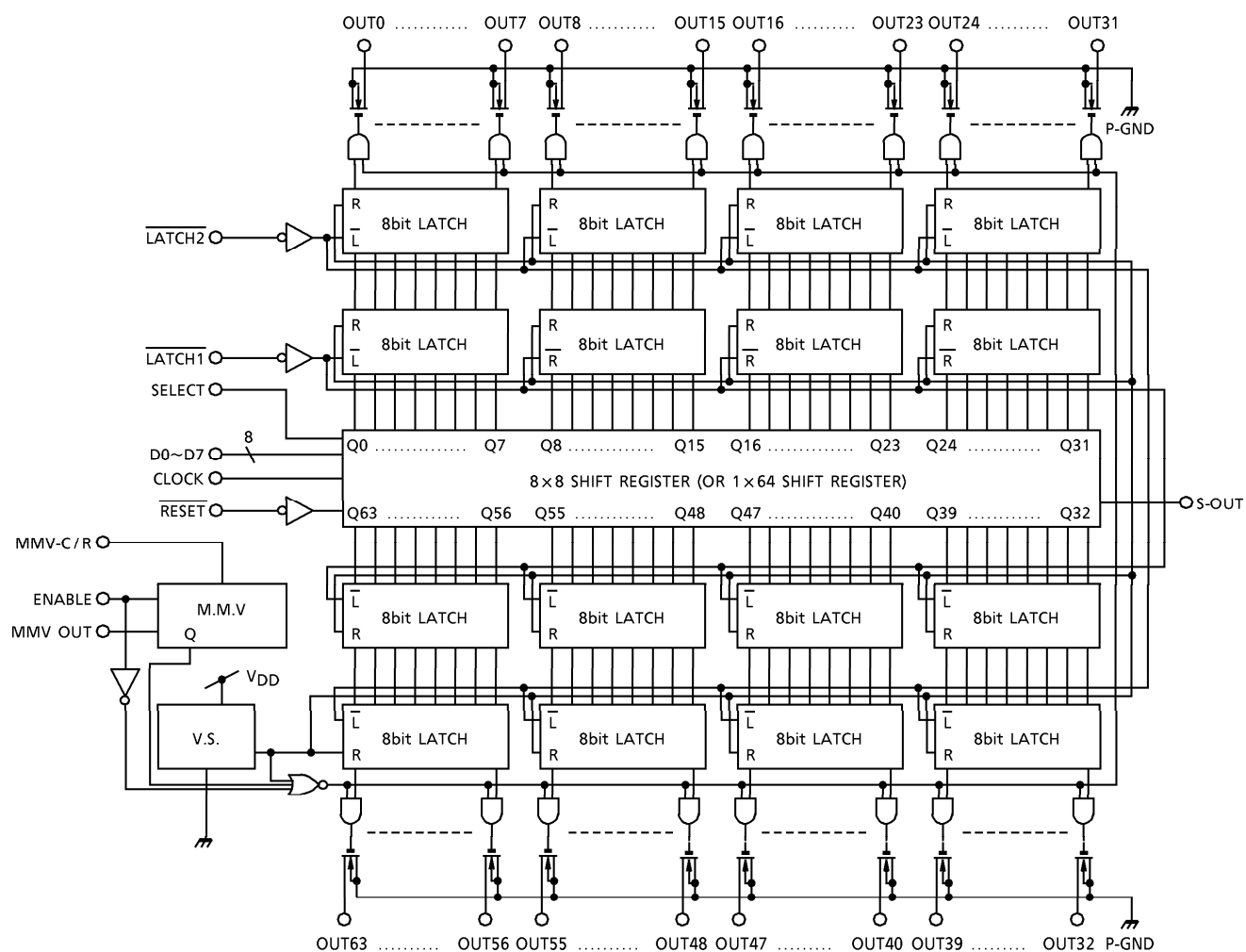
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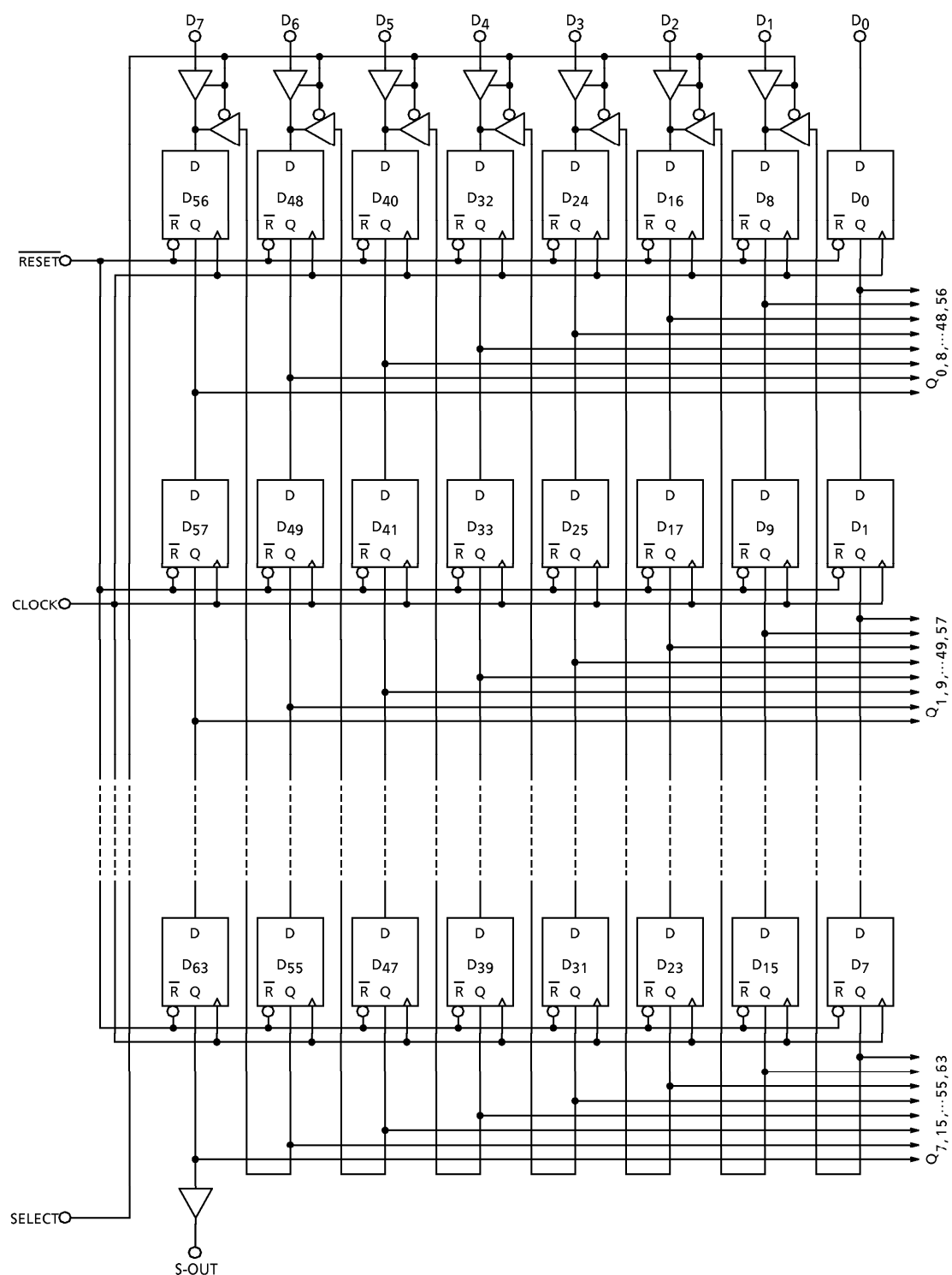
PIN CONNECTION (TOP VIEW)



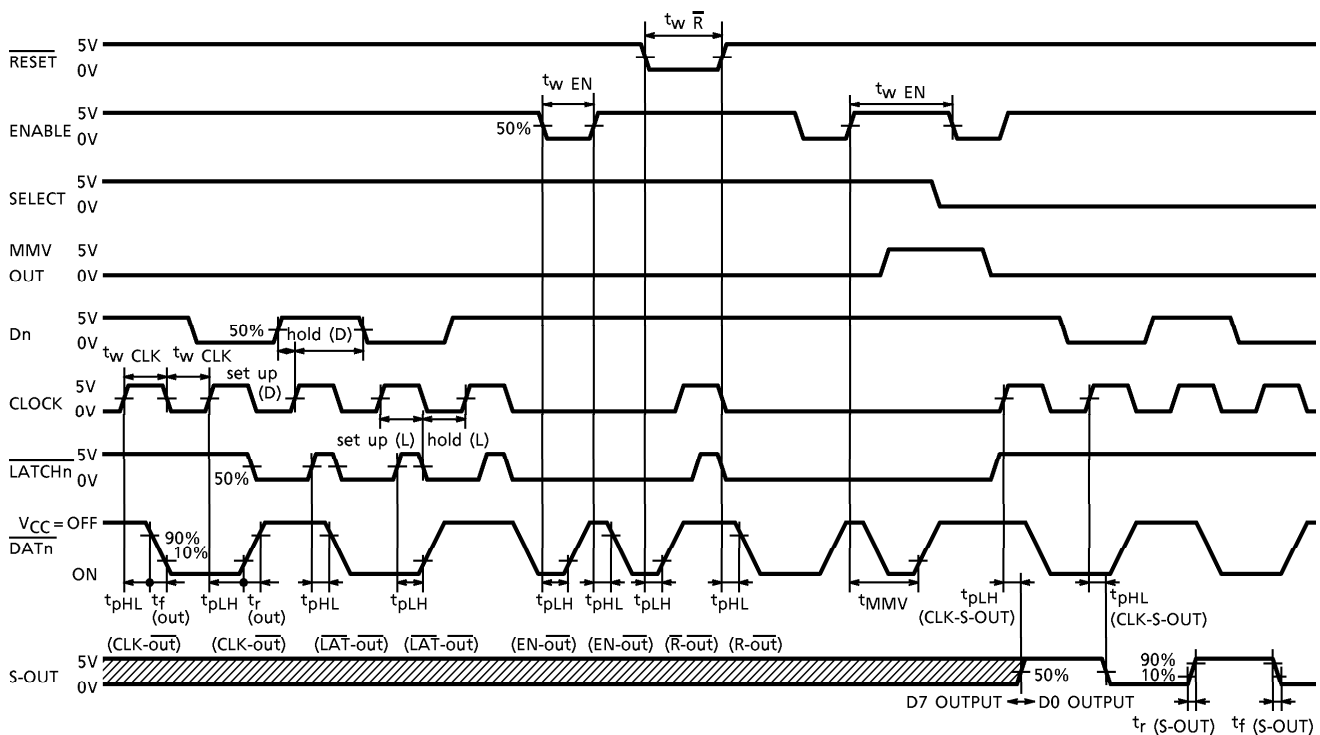
BLOCK DIAGRAM



BLOCK DIAGRAM (8×8, 1×64 shift register)



TIMING WAVEFORM



TERMINAL DESCRIPTION

PIN NAME	PIN No.	FUNCTION
CLOCK	97	Input Terminals for Shift register Clock.
ENABLE	84	"L" : All Outputs "On". Pull-Down Input Terminal.
$\overline{\text{RESET}}$	98	"L" : Reset shift register and latch. Pull-Down Input Terminal.
D0~D7	88~95	Input Terminals for Output Data. "H" : Output On, "L" : Output Off.
MMV-C / R	78	CR Connection Terminal for CR Timer (MMV).
MMV-OUT	79	Output Terminal for CR Timer (MMV).
$\overline{\text{OUT0}}\sim\overline{\text{63}}$	—	Output Terminals. These are Open Drain Outputs.
SELECT	83	Input Terminal for Input Mode Data. "H" : 8bit Parallel Input Mode, "L" : 1bit Serial Input Mode.
S-OUT	96	Output Terminal for Serial Data "D63".
$\overline{\text{LATCH1}}/\overline{\text{LATCH2}}$	86 / 85	Input Terminal for Latch. "H" : Data Through, "L" : Data Latch.
V _{DD}	81, 100	Supply Voltage Terminal for Control Logic.
L-GND	82, 99	Ground Terminal for Control Logic.
P-GND	—	Ground Terminal for Drivers. 10 Terminals.

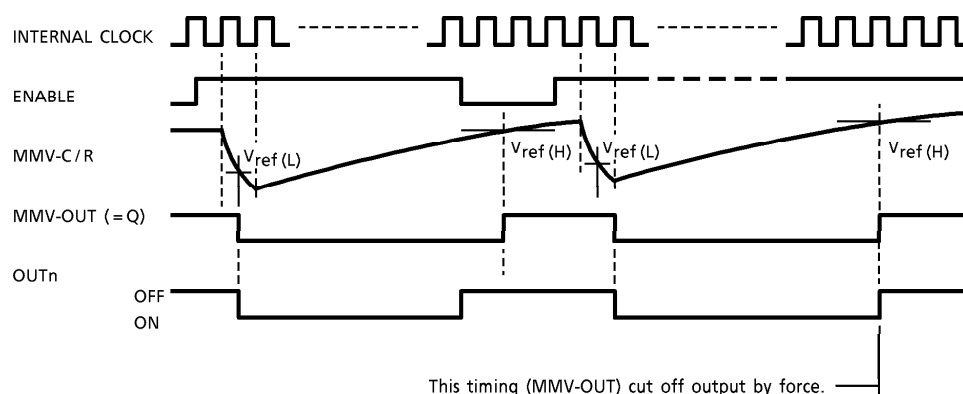
MMV OPERATION

MMV Output of Q becomes "L" when the MMV/E voltage becomes less than $V_{ref}(L)$ after the first rising edge of Internal Clock.

And becomes "H" when the MMV/E voltage above $V_{ref}(H)$ after re-changing of external capacitance connect to MMV/E. The external capacitance and resistor connect to MMV/E control MMV Output "ON" period.

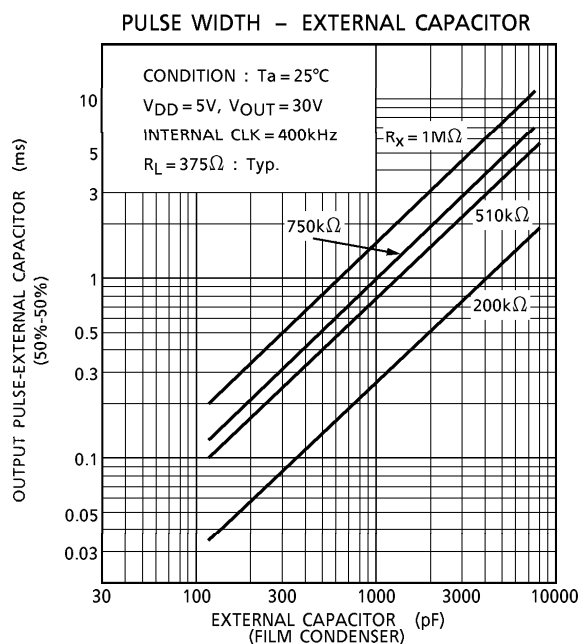
So Output Load is protected from burn-out. It's required enough discharging time (decided by Time period of Internal Clock) of external capacitance.

(Refer to figure below)



PULSE WIDTH OF MMV

See Below



MAXIMUM RATINGS ($T_a = 25^\circ\text{C}$)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Supply Voltage		V_{DD}	$-0.3 \sim 7.0$	V
Output Drain-Source Voltage		V_{DS}	$-0.4 \sim 30$	V
Output Current		I_{DS}	130	mA / ch
Input Current		I_{IN}	± 5	mA
Input Voltage		V_{IN}	$-0.3 \sim V_{DD} \pm 0.3$	V
Power Dissipation	Free Air	P_D	1.0	W
	(Note 1) PCB		1.3	
Operating Temperature		T_{opr}	$-40 \sim 85$	$^\circ\text{C}$
Storage Temperature		T_{stg}	$-55 \sim 150$	$^\circ\text{C}$

(Note 1) $60 \times 60 \times 1.6\text{mm}$ Cu 24% Glass Epoxy PCB**RECOMMENDED OPERATING CONDITIONS** ($T_a = -40 \sim 85^\circ\text{C}$, $V_{SS} = 0\text{V}$)

CHARACTERISTIC		SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Supply Voltage		V _{DD}	—		4.5	5	5.5	V
Input Voltage	“H” LEVEL	V _{IH}	—		0.7 V _{DD}	—	V _{DD}	V
	“L” LEVEL	V _{IL}	—		0	—	0.3 V _{DD}	
Output Drain-Source Voltage		V _{OUT}	—		—	—	24	V
Output Current		I _{OUT}	Duty = 100%	All Output “L” Level	—	—	44	mA / ch
			Duty = 80%		—	—	49	
			Duty = 50%		—	—	62	
External Resistor		R _{EXT}	—		200	—	1000	kΩ
External Capacitance		C _{EXT}	—		100	—	4000	pF
Power Dissipation		P _D	—		—	—	0.67	mW

ELECTRICAL CHARACTERISTICS (Ta = -10~80°C, V_{DD} = 4.5~5.5V, V_{SS} = 0V, "H" = V_{IH}, "L" = V_{IL})

CHARACTERISTIC		SYMBOL	TEST CIR- CUIT	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Output Voltage	“L” LEVEL	V _{DS1}	—	I _{OUT} = 40mA, Ta = 25°C		—	0.16	0.32	V
		V _{DS1}	—	I _{OUT} = 40mA		—	—	0.48	
		V _{DS2}	—	I _{OUT} = 100mA, Ta = 25°C		—	0.40	0.80	
		V _{DS2}	—	I _{OUT} = 100mA		—	—	1.20	
Output Current	“H” LEVEL	I _{OH}	—	S-OUT	V _{OH} = 4.6V Ta = 25°C	—	0.2	0.5	mA
	“L” LEVEL	I _{OL}	—	MMV-OUT	V _{OL} = 0.4V Ta = 25°C	—	0.2	0.5	
Output Resistor		R _{ON}	—	Ta = 25°C		—	4.00	8.00	Ω
Output Leakage Current		I _{OZ1}	—	V _{OUT} = 30V, EN = “L”, 1bit		—	—	10	μA
		I _{OZ2}	—	V _{OUT} = 30V, EN = “L”, 64bit		—	—	100	
Input Current		I _{IN}	—	V _{IN} = V _{DD} or V _{SS}		—	—	± 1	μA
Input Voltage	“H” LEVEL	V _{IH}	—	—		0.7 V _{DD}	—	—	V
	“L” LEVEL	V _{IL}	—	—		—	—	0.3 V _{DD}	
Voltage Supervisor Opating Voltage		V _{VS}	—	—		2.0	—	4.0	V
Supply Current		I _{DD}	—	—		—	—	300	μA
Operating Supply Current		I _{DD1}	—	f _{CLK} = 5MHz, Duty = 50% Data = 1 / 2 f _{CLK} , OUTPUT off LATCH = “L”, LATCH-Data = “L”		—	—	5.0	mA
		I _{DD2}	—	f _{CLK} = 1MHz, Duty = 50% Data = 1 / 64 f _{CLK} All OUTPUT open LATCH = “H”, 1bit ON		—	—	6.0	
Input Pull-Up Resistor		R _{VDD}	—	V _{DD} = 5.0V, Ta = 25°C		150	300	600	kΩ
Input Pull-Down Resistor		R _{VSS}	—	V _{DD} = 5.0V, Ta = 25°C		150	300	600	
Internal Clock Frequency		f _{int}	—	V _{DD} = 5.0V, Ta = 25°C		400	800	—	kHz

RECOMMENDED TIMING CONDITIONS ($T_a = -40 \sim 85^\circ\text{C}$, $V_{DD} = 4.5 \sim 5.5\text{V}$, $V_{SS} = 0\text{V}$)

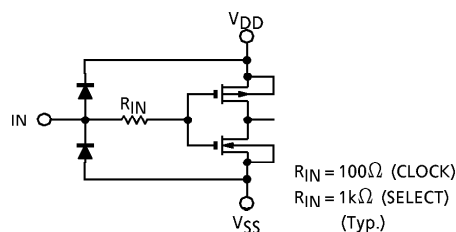
CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Clock Pulse Width	$t_w \text{ CLK}$	—	50	—	—	ns
Enable Pulse Width	$t_w \text{ EN}$	—	0.5	—	—	μs
Latch Pulse Width	$t_w \overline{\text{LAT}}$	—	50	—	—	ns
Clear Pulse Width	$t_w \text{ CLR}$	—	80	—	—	ns
Data Set up Time	t_{setup}	—	37	50	—	ns
Data Hold Time	t_{hold}	—	50	—	—	ns

SWITCHING CHARACTERISTICS ($T_a = 25^\circ\text{C}$, $V_{DD} = 5\text{V}$, $V_{OUT} = 26\text{V}$, $R_1 = 650\Omega$, $C_L = 15\text{pF}$)

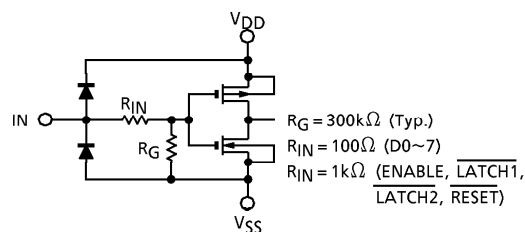
CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay Time (Low-to-High)	CLK-Out _n	t _{pLH}	MMV-C / R = "L"	—	—	1000	ns
	R-Out _n		MMV-C / R = "L"	—	—	1000	
	LAT1-Out _n		MMV-C / R = "L"	—	—	1000	
	LAT2-Out _n		MMV-C / R = "L"	—	—	1000	
	EN-Out _n		R = 750kΩ, C = 2600pF, Ta = 25°C	—	—	2500	
Propagation Delay Time (High-to-Low)	CLK-Out _n	t _{pHL}	MMV-C / R = "L"	—	—	1000	ns
	LAT1-Out _n		MMV-C / R = "L"	—	—	1000	
	LAT2-Out _n		MMV-C / R = "L"	—	—	1000	
	EN-Out _n		R = 750kΩ, C = 2600pF, Ta = 25°C	—	—	2500	
Set up Time	CLK-LAT _n	t _{setup} (L)	—	—	70	120	ns
	CLK-S-IN	t _{setup} (D)	—	—	—	30	
Hold Time	CLK-LAT _n	t _{hold} (L)	—	—	—	0	
	CLK-S-IN	t _{hold} (D)	—	—	—	20	
Clock Pulse Width		t _w CLK	—	—	—	50	ns
Latch Pulse Width		t _w LAT _n	—	—	—	50	ns
Reset Pulse Width		t _w R	—	—	—	50	ns
Enable Pulse Width		t _w EN	—	—	—	400	ns
Output Rise Time		t _{or}	OUT _n	—	200	500	ns
Output Fall Time		t _{of}	OUT _n	—	200	500	ns
Maximum Clock Frequency		f _{MAX}	Duty = 50%	10	15	—	MHz
Voltage Supervisor Operating Pulse Width		t _w VS	V _{DD} (H) = 5V, V _{DD} (L) = 2V	—	200	—	ns
MMV Reset Time		t _{MMV}	R = 750kΩ, C = 2600pF, Ta = 25°C	1	3	5	ms

EQUIVALENT OF INPUTS AND OUTPUT CIRCUIT

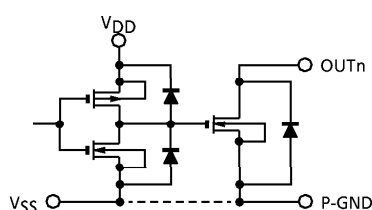
1. CLOCK, SELECT



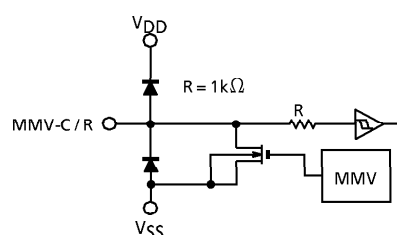
2. ENABLE, $\overline{LATCH1}$, $\overline{LATCH2}$, $\overline{RESET}$, D0~7



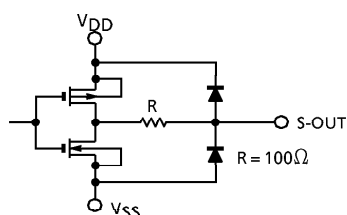
3. $\overline{OUTn}$



4. MMV-C / R



5. S-OUT, MMV-OUT



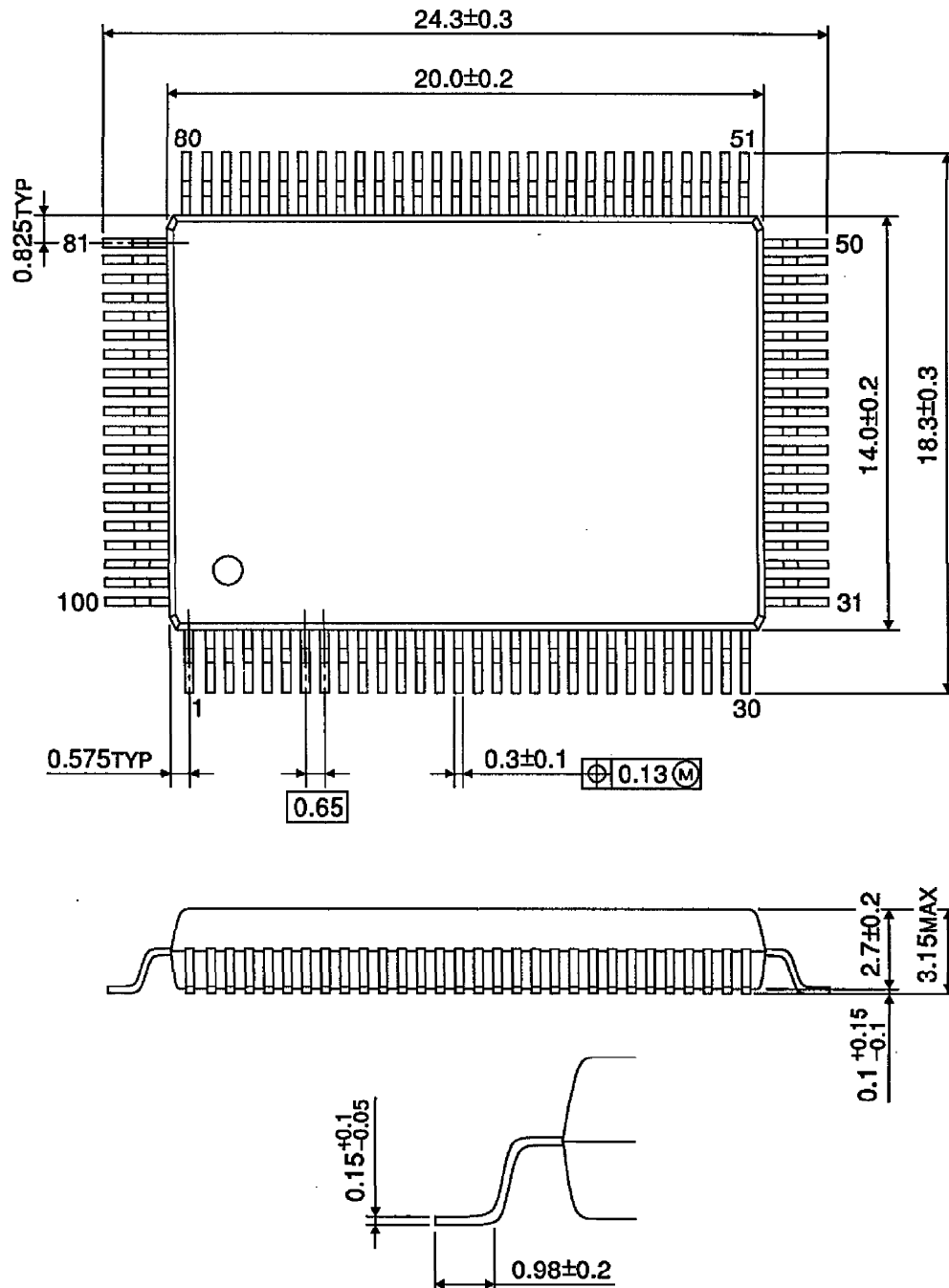
PRECAUTIONS for USING

Utmost care is necessary in the design of the output line, V_{CC} (V_{DD}) and GND (L-GND, P-GND) line since IC may be destroyed due to short-circuit between outputs, air contamination fault, or fault by improper grounding.

OUTLINE DRAWING

QFP100-P-1420-0.65C

Unit : mm



Weight : 1.6g (Typ.)