Seven Degrees of Freedom Inertial Sensor

Data Sheet

ADIS16489

FEATURES

- **Triaxial, digital gyroscope, ±450°/sec dynamic range**
  - **±0.018° axis-to-axis misalignment error**
  - **5.3°/hr in-run bias stability**
  - **0.25°/√hr angular random walk**
  - **0.045°/sec nonlinearity**
- **Triaxial, digital accelerometer, ±18 *g* dynamic range**
- **Barometer, 300 mbar to 1100 mbar**
- **Triaxial, delta angle and delta velocity outputs**
- **Factory calibrated sensitivity, bias, and axial alignment**
  - **Calibration temperature range: −40°C to +85°C**
- **SPI compatible**
- **Programmable operation and control**
  - **Automatic and manual bias correction controls**
  - **4 FIR filter banks, 120 configurable taps**
  - **Digital I/O: data ready alarm indicator, external clock**
  - **Alarms for condition monitoring**
  - **Power-down/sleep mode for power management**
  - **Optional input sync clock: up to 2.4 kHz**
  - **On demand self test of inertial sensors**
  - **On demand flash memory test (checksum)**
- **Single-supply operation: 3.0 V to 3.6 V**
- **2000 *g* shock survivability**
- **Parylene coating (moisture barrier for internal circuitry)**
- **Operating temperature range: −40°C to +105°C**

APPLICATIONS

- **Platform stabilization and control**
- **Navigation**
- **Personnel tracking**
- **Instrumentation**
- **Robotics**

GENERAL DESCRIPTION

The ADIS16489 is a complete inertial system that includes a triaxis gyroscope, a triaxis accelerometer, and a barometer. Each inertial sensor in the ADIS16489 combines industry leading *i*MEMS® technology with signal conditioning that optimizes dynamic performance. The factory calibration characterizes each sensor for sensitivity, bias, alignment, and linear acceleration (gyroscope bias). As a result, each sensor has its own dynamic compensation formulas that provide accurate sensor measurements.

The ADIS16489 provides a simple, cost effective method for integrating accurate, multiaxis inertial sensing into industrial systems, especially when compared with the complexity and investment associated with discrete designs. All necessary motion testing and calibration are part of the production process at the factory, greatly reducing system integration time. Tight orthogonal alignment simplifies inertial frame alignment in navigation systems. The serial peripheral interface (SPI) and register structure provide a simple interface for data collection and configuration control. Parylene coating of all internal circuitry (except the barometer) provides a protective barrier against moisture exposure.

The ADIS16489 uses the same footprint and connector system as the ADIS16375, ADIS16480, ADIS16485, and ADIS16488A, which greatly simplifies the upgrade process. The ADIS16489 is packaged in a module that is approximately 44 mm × 47 mm × 14 mm and includes a standard connector interface.

FUNCTIONAL BLOCK DIAGRAM

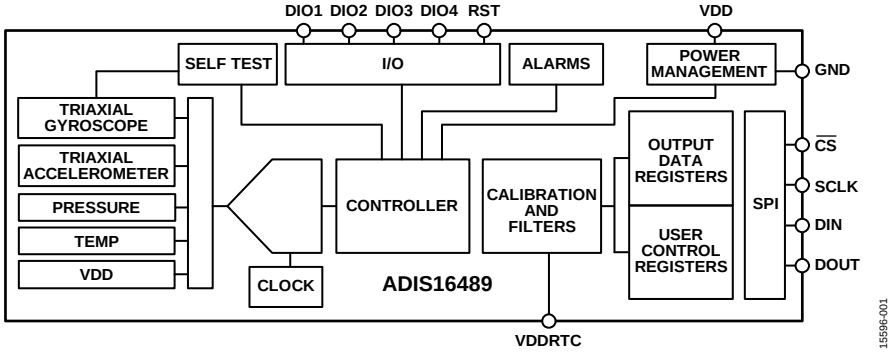


Figure 1.

Rev. B **Document Feedback**

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REVISION HISTORY

8/2020—Rev. A to Rev. B

Changed EVAL-ADIS to EVAL-ADIS2 ..... Throughout
Change to Nonlinearity Parameter, Table 1 4
Changes to Table 6 9
Changes to Introduction Section 11
Changes to Dual Memory Structure Section and Reading Sensor Data Section 12
Changes to Table 10 13
Changes to Table 12 Title, Table 13 Title, Table 14 Title, Table 16 Title, and Table 16 16
Changes to Table 18 17
Changes to Table 92 23
Changes to Table 144 and Table 146 27
Changes to Continuous Bias Estimation (NULL_CNFG) Section, Table 161, and Figure 33 30
Change to Solving for ΔX_ACCL_OUT, ΔZ_GYRO_OUT, ΔY_GYRO_OUT, and ΔX_GYRO_OUT Section 32
Changes to FIR Filters Section 35

11/2018—Rev. 0 to Rev. A

Added Endnote 4, Table 1; Renumbered Sequentially 4
Added X-Ray Sensitivity Section 39

2/2017—Revision 0: Initial Version

SPECIFICATIONS

T_C = 25°C, VDD = 3.3 V, angular rate = 0°/sec, dynamic range = ±450°/sec ± 1 *g*, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
GYROSCOPES					
Dynamic Range		±450		±480	°/sec
Sensitivity	x_GYRO_OUT and x_GYRO_LOW (32-bit)		3.052×10^{-7}		°/sec/LSB
Repeatability[1]	−40°C ≤ T_C ≤ +85°C			±1	%
Sensitivity Temperature Coefficient	−40°C ≤ T_C ≤ +85°C, 1 σ		±25		ppm/°C
Misalignment Error	Axis to axis		±0.018		Degrees
	Axis to frame (package)		±1.0		Degrees
Nonlinearity	Best fit straight line, full scale (FS) = 450°/sec		0.01		% FS
Bias					
Repeatability[1, 2]	−40°C ≤ T_C ≤ +85°C, 1 σ		±0.2		°/sec
In-Run Bias Stability	1 σ		5.3		°/hr
Angular Random Walk	1 σ		0.25		°/√hr
Temperature Coefficient	−40°C ≤ T_C ≤ +85°C, 1 σ		±0.0025		°/sec/°C
Error over Temperature	−15°C ≤ T_C ≤ +65°C, 10°C range		±0.0611		°/sec
Linear Acceleration Effect	Any axis, 1 σ (CONFIG[7] = 1)		0.009		°/sec/*g*
	Any axis, 1 σ (CONFIG[7] = 0)		0.015		°/sec/*g*
Noise					
Output Noise	No filtering		0.16		°/sec rms
Rate Noise Density	f = 10 Hz to 40 Hz, no filtering		0.0068		°/sec/√Hz rms
3 dB Bandwidth			330		Hz
Sensor Resonant Frequency			18		kHz
ACCELEROMETERS[3]	Each axis				
Dynamic Range		±18			*g*
Sensitivity	x_ACCL_OUT and x_ACCL_LOW (32-bit)		1.221×10^{-8}		*g*/LSB
Repeatability[1]	−40°C ≤ T_C ≤ +85°C			±0.5	%
Sensitivity Temperature Coefficient	−40°C ≤ T_C ≤ +85°C, 1 σ		±25		ppm/°C
Misalignment	Axis to axis		±0.035		Degrees
	Axis to frame (package)		±1.0		Degrees
Nonlinearity	Best fit straight line, ±10 *g*		10		m*g*
	Best fit straight line, ±18 *g*		90		m*g*
Bias					
Repeatability[1, 2, 4]	−40°C ≤ T_C ≤ +85°C, 1 σ		±16		m*g*
In-Run Bias Stability	1 σ		70		μ*g*
Velocity Random Walk	1 σ		0.029		m/sec/√hr
Temperature Coefficient	−40°C ≤ T_C ≤ +85°C, 1 σ		±0.1		m*g*/°C
Noise					
Output Noise	No filtering		1.29		m*g* rms
Noise Density	f = 10 Hz to 40 Hz, no filtering		0.063		m*g*/√Hz rms
3 dB Bandwidth			330		Hz
Sensor Resonant Frequency			5.5		kHz
BAROMETER					
Pressure Range		300		1100	mbar
	Extended	10		1200	mbar
Sensitivity	BAROM_OUT and BAROM_LOW (32-bit)		6.1×10^{-7}		mbar/LSB
Error with Supply			0.04		%/V
Total Error			4.5		mbar
Relative Error[5]	−40°C ≤ T_C ≤ +85°C		2.5		mbar
Nonlinearity[6]	Best fit straight line, FS = 1100 mbar		0.1		% of FS
	−40°C ≤ T_C ≤ +85°C		0.2		% of FS
Linear *g* Sensitivity	±1 *g*, 1 σ		0.005		mbar/*g*
Noise			0.025		mbar rms

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
TEMPERATURE SENSOR					
Scale Factor	Output = 0x0000 at 25°C (±5°C)		0.00565		°C/LSB
LOGIC INPUTS[7]					
Input Voltage					
High, V_{IH}		2.0			V
Low, V_{IL}				0.8	V
$\overline{RST}$ Pulse Width		1			µs
$\overline{CS}$ Wake-Up Pulse Width		20			µs
Input Current					
Logic 1 (High), I_{IH}	V_{IH} = 3.3 V			10	µA
Logic 0 (Low), I_{IL}	V_{IL} = 0 V				
All Pins Except $\overline{RST}$				10	µA
$\overline{RST}$ Pin			0.33		mA
Input Capacitance, C_{IN}			10		pF
DIGITAL OUTPUTS					
Output Voltage					
High, V_{OH}	I_{SOURCE} = 0.5 mA	2.4			V
Low, V_{OL}	I_{SINK} = 2.0 mA			0.4	V
FLASH MEMORY	Endurance[8]	100,000			Cycles
Data Retention[9]	T_J = 85°C	20			Years
FUNCTIONAL TIMES[10]	Time until data is available				
Power-On Start-Up Time				600	ms
Back-up			1370	1500	ms
Reset Recovery Time[11]			390	600	ms
Sleep Mode Recovery Time			730	1000	µs
Flash Memory					
Update Time[12]			1.05	6.8	sec
Test Time			50		ms
On Demand Self Test Time	Using internal clock (2460 Hz)		12		ms
CONVERSION RATE			2.46		kSPS
Initial Clock Accuracy			0.02		%
Temperature Coefficient			40		ppm/°C
Sync Input Clock[13]		0.7		2.4	kHz
POWER SUPPLY, VDD	Operating voltage range, VDD = 3.3 V	3.0		3.6	V
Power Supply Current, I_{DD}[14]	Normal mode, µ ± σ		186		mA
	Sleep mode		12.2		mA
	Power-down mode		37		µA
POWER SUPPLY, VDDRTC	Operating voltage range	3.0	3.3	3.6	V
Real-Time Clock Supply Current	Normal mode, VDDRTC = 3.3 V		13		µA

[1] The repeatability specifications represent analytical projections based on the following drift contributions and conditions: temperature hysteresis (−40°C to +85°C), electronics drift (high temperature operating life test: 110°C, 500 hours), drift from temperature cycling (JESD22, Method A104-C, Method N, 500 cycles, −55°C to +85°C), rate random walk (10-year projection), and broadband noise.
[2] Bias repeatability describes a long-term behavior over a variety of conditions. Short-term repeatability relates to the in-run bias stability and noise density specifications.
[3] All specifications associated with the accelerometers relate to the full-scale range of ±18 *g*.
[4] X-ray exposure can degrade this performance metric.
[5] The relative error assumes that the initial error, at 25°C, is corrected in the end application.
[6] Specification assumes a full scale (FS) of 1000 mbar.
[7] The digital I/O signals use a 3.3 V system.
[8] Endurance is qualified as per JEDEC Standard 22, Method A117, measured at −40°C, +25°C, +85°C, and +125°C.
[9] The data retention specification assumes a junction temperature (T_J) of 85°C per JEDEC Standard 22, Method A117. Data retention lifetime decreases with T_J.
[10] These times do not include thermal settling and internal filter response times, which may affect overall accuracy.
[11] The $\overline{RST}$ line must be in a low state for at least 10 µs to ensure a proper reset initiation and recovery.
[12] Monitoring the data ready signal (see Table 153 for FNCTIO_CTRL configuration) for the return of regular pulsing can help minimize system wait times.
[13] The device functions at clock rates below 0.7 kHz but at reduced performance levels.
[14] Supply current transients can reach 600 mA during initial startup or reset recovery.

TIMING SPECIFICATIONS

T_C = 25°C, VDD = 3.3 V, unless otherwise noted.

Table 2.

Parameter	Description	Min[1]	Typ	Max[1]	Unit
f_{SCLK}	Serial clock	0.01		15	MHz
t_{STALL}[2]	Stall period between data	2			µs
t_{CLS}	Serial clock low period	31			ns
t_{CHS}	Serial clock high period	31			ns
$t_{\overline{CS}}$	Chip select to clock edge	32			ns
t_{DAV}	DOUT valid after SCLK edge			10	ns
t_{DSU}	DIN setup time before SCLK rising edge	2			ns
t_{DHD}	DIN hold time after SCLK rising edge	2			ns
t_{DR}, t_{DF}	DOUT rise/fall times, ≤100 pF loading		3	8	ns
t_{DSOE}	$\overline{CS}$ assertion to data out active	0		11	ns
t_{HD}	SCLK edge to data out invalid	0			ns
t_{SFS}	Last SCLK edge to $\overline{CS}$ deassertion	32			ns
t_{DSHI}	$\overline{CS}$ deassertion to data out high impedance	0		9	ns
	Data ready pulse width		11	15	µs
t_1	Input sync pulse width	5			µs
t_2	Input sync to data invalid		560	570	µs
t_3	Input sync period	417			µs

[1] Guaranteed by design and characterization, but not tested in production.
[2] See Table 3 for exceptions to the stall time rating.

Register Specific Stall Times

Table 3.

Parameter	Description	Min[1]	Typ	Max	Unit
STALL TIME					
FNCTIO_CTRL	Configure DIOx functions	15			µs
FILTR_BNK_0	Enable/select finite impulse response (FIR) filter banks	10			µs
FILTR_BNK_1	Enable/select FIR filter banks	10			µs
NULL_CNFG	Configure autonull bias function	10			µs
GLOB_CMD[1]	Self test	12000			µs
GLOB_CMD[2]	Flash memory test	50000			µs
GLOB_CMD[3]	Flash memory update	375000			ms
GLOB_CMD[6]	Factory calibration restore	75000			sec
GLOB_CMD[7]	Software reset	120000			ms

[1] Monitoring the data ready signal (see Table 153 for FNCTIO_CTRL configuration) for the return of regular pulsing can help minimize system wait times.

Timing Diagrams

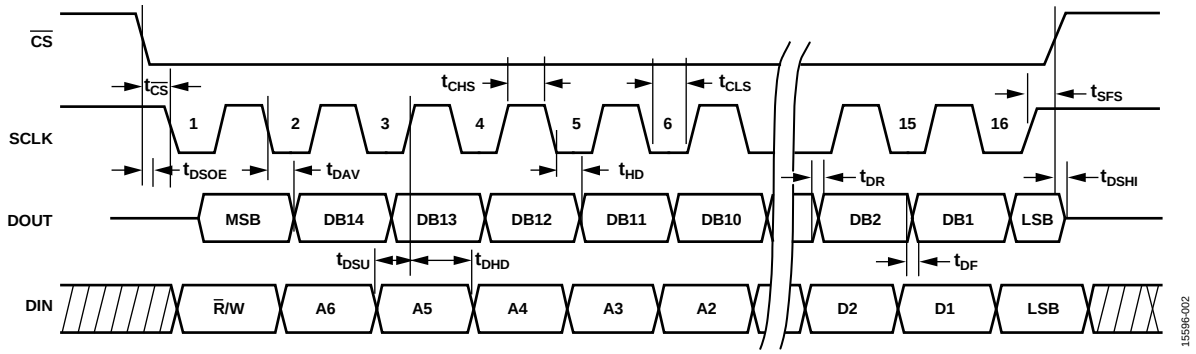


Figure 2. SPI Timing and Sequence

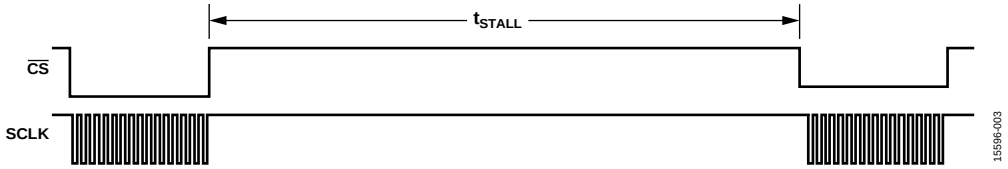


Figure 3. Stall Time and Data Rate

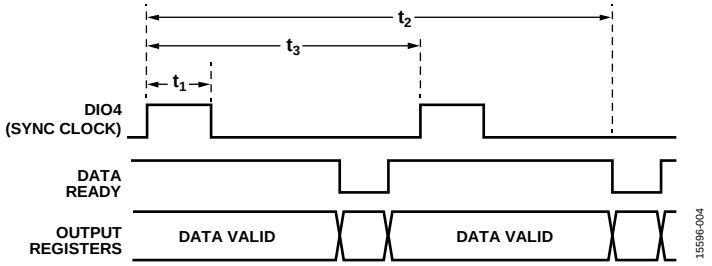


Figure 4. Input Clock Timing Diagram, FNCTIO_CTRL[7:4] = 0xFD

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Shock Survivability	
Any Axis, Unpowered	2000 *g*
Any Axis, Powered	2000 *g*
VDD to GND	−0.3 V to +3.6 V
Digital Input Voltage to GND	−0.3 V to VDD + 0.2 V
Digital Output Voltage to GND	−0.3 V to VDD + 0.2 V
Operating Temperature Range	−40°C to +105°C
Storage Temperature Range[1]	−65°C to +150°C
Barometric Pressure	2 bar

[1] Extended exposure to temperatures that are lower than −55°C or higher than +105°C can adversely affect the accuracy of the factory calibration.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure.

θ_{JC} is the junction to case thermal resistance.

The ADIS16489 is a multichip module, which includes many active components. The values in Table 5 identify the thermal response of the hottest component inside of the ADIS16489 with respect to the overall power dissipation of the module. This approach enables a simple method for predicting the temperature of the hottest junction, based on either ambient or case temperature.

For example, when the ambient temperature is 70°C, the hottest junction inside of the ADIS16489 is 89.1°C.

$$T_J = \theta_{JA} \times VDD \times I_{DD} + 70°C$$

$$T_J = 22.8°C/W \times 3.3\ V \times 0.254A + 70°C$$

$$T_J = 89.1°C$$

Table 5. Package Characteristics

Package Type	θ_{JA}	θ_{JC}	Device Weight
ML-24-6[1]	22.8°C/W	10.1°C/W	48 g

[1] Thermal impedance simulated values come from a case when four M2 × 0.4 mm machine screws (torque = 20 inch ounces) secure the ADIS16489 to the printed circuit board.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

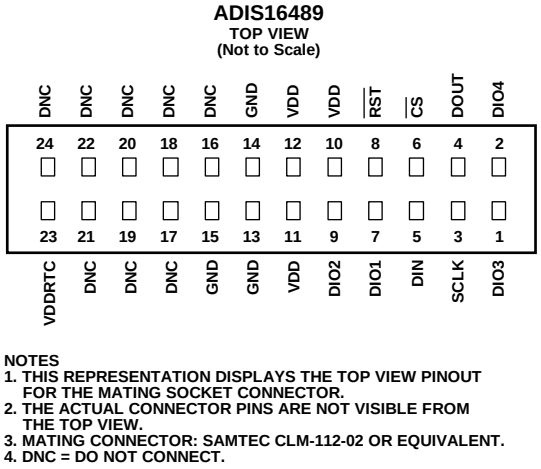


Figure 5. Pin Configuration

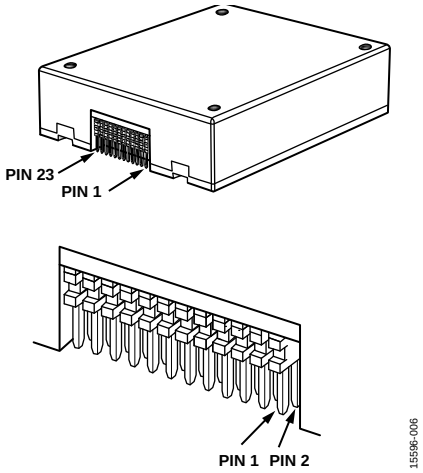


Figure 6. Axial Orientation (Top Side Facing Up)

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
1	DIO3	Input and output	Configurable Digital Input and Output 3.
2	DIO4	Input and output	Configurable Digital Input and Output 4.
3	SCLK	Input	SPI Serial Clock.
4	DOUT	Output	SPI Data Output. Clocks output on the SCLK falling edge.
5	DIN	Input	SPI Data Input. Clocks input on the SCLK rising edge.
6	$\overline{CS}$	Input	SPI Chip Select.
7	DIO1	Input and output	Configurable Digital Input and Output 1.
8	$\overline{RST}$	Input	Reset.
9	DIO2	Input and output	Configurable Digital Input and Output 2.
10, 11, 12	VDD	Supply	Power Supply.
13, 14, 15	GND	Supply	Power Ground.
16 to 22, 24	DNC	Not applicable	Do Not Connect. Do not connect to these pins.
23	VDDRTC	Supply	Real-Time Clock Power Supply. The VDDRTC power supply must be connected, even if the RTC feature is not used.

TYPICAL PERFORMANCE CHARACTERISTICS

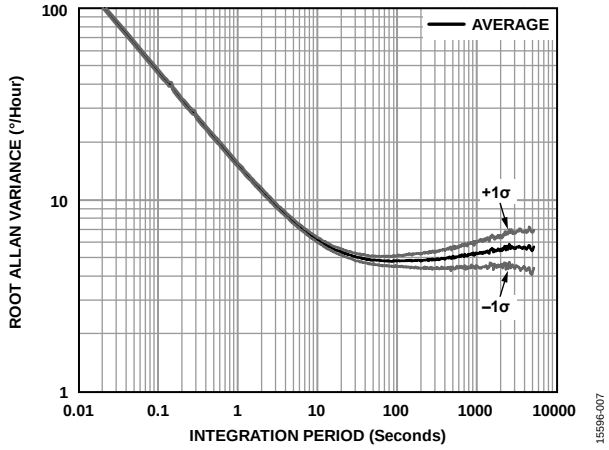


Figure 7. Gyroscope Allan Variance, T_C = 25°C

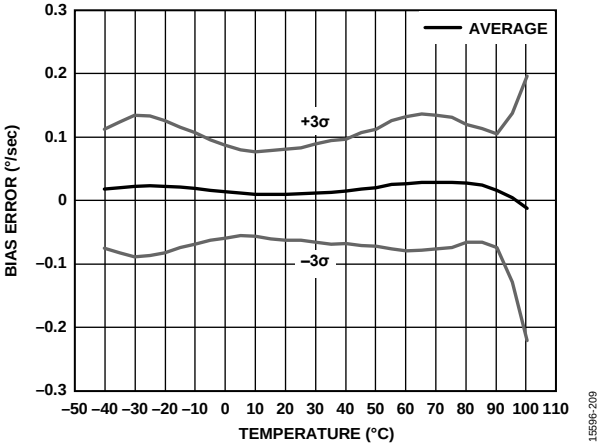


Figure 9. Gyroscope Bias Error vs. Temperature

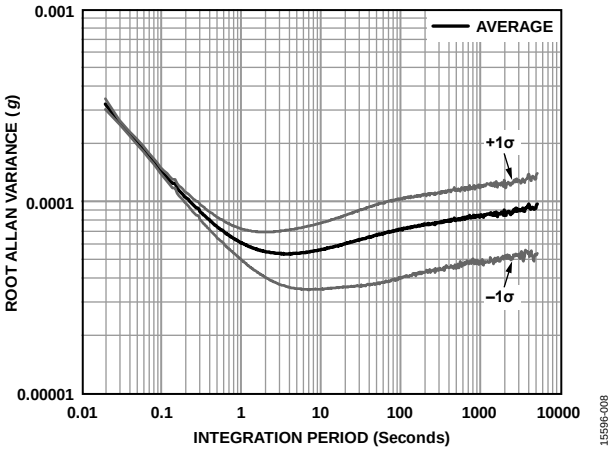


Figure 8. Accelerometer Allan Variance, T_C = 25°C

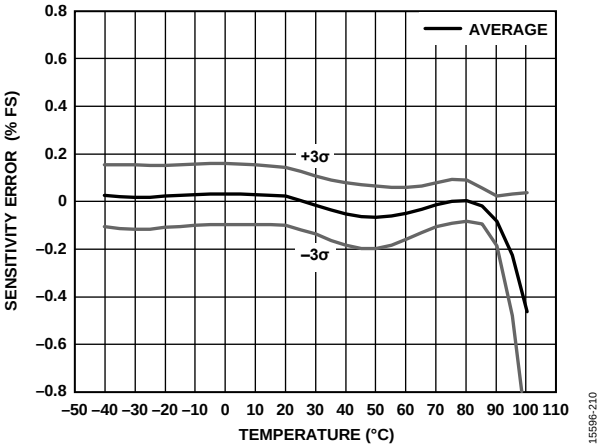


Figure 10. Gyroscope Scale (Sensitivity) Error vs. Temperature

THEORY OF OPERATION

INTRODUCTION

The ADIS16489 is an autonomous sensor system that starts up on its own when it has a valid power supply. After running through its initialization process, the ADIS16489 begins sampling, processing, and loading calibrated sensor data into the output registers, which are accessible using the SPI port. The SPI port typically connects to a compatible port on an embedded processor (see Figure 11). The four SPI signals facilitate synchronous, serial data communication. The factory default configuration provides users with a data ready signal on the DIO2 pin to trigger data acquisition (see Figure 31).

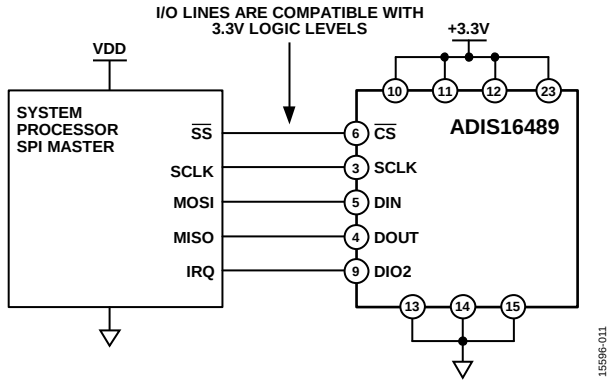


Figure 11. Electrical Connection Diagram

Table 7. Generic Master Processor Pin Names and Functions

Mnemonic	Function
$\overline{SS}$	Slave select
SCLK	Serial clock
MOSI	Master output, slave input
MISO	Master input, slave output
IRQ	Interrupt request

Embedded processors typically use control registers to configure their serial ports for communicating with SPI slave devices such as the ADIS16489. Table 8 contains a list of settings that describe the SPI protocol of the ADIS16489.

Table 8. Generic Master Processor SPI Settings

Processor Setting	Description
Master	The ADIS16489 operates as slave
SCLK ≤ 15 MHz	Maximum serial clock rate
SPI Mode 3	CPOL = 1 (polarity), CPHA = 1 (phase)
MSB First Mode	Bit sequence
16-Bit Mode	Shift register/data length

REGISTER STRUCTURE

The register structure and SPI port support a simple connection between the ADIS16489 and an embedded processor platform. The register structure contains both output data and control registers. The output data registers include the latest sensor data, a real-time clock, error flags, alarm flags, and identification data. The control registers include sample rate, filtering, input and output, alarms, calibration, and diagnostic configuration options. All communication between the ADIS16489 and an external processor involves either reading or writing to one of the user registers.

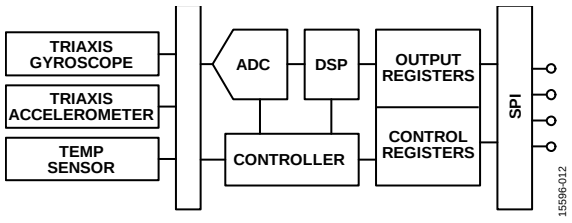


Figure 12. Basic Operation

The register structure uses a paged addressing scheme that contains 13 pages with each page containing 64 register locations. Each register is 16 bits wide and each byte has a unique address within the memory map of that page. The SPI port has access to one page at a time, using the bit sequence in Figure 13. Select the page to activate for SPI access by writing its code to the PAGE_ID register. Read the PAGE_ID register to determine which page is currently active. Table 9 displays the PAGE_ID register contents for each page, along with their basic functions. The PAGE_ID register is located at Address 0x00 on every page.

Table 9. User Register Page Assignments

Page	PAGE_ID	Function
0	0x00	Output data, clock, identification
1	0x01	Reserved
2	0x02	Calibration
3	0x03	Control: sample rate, filtering, input and output, alarms
4	0x04	Serial number
5	0x05	FIR Filter Bank A, Coefficient 0 to Coefficient 59
6	0x06	FIR Filter Bank A, Coefficient 60 to Coefficient 119
7	0x07	FIR Filter Bank B, Coefficient 0 to Coefficient 59
8	0x08	FIR Filter Bank B, Coefficient 60 to Coefficient 119
9	0x09	FIR Filter Bank C, Coefficient 0 to Coefficient 59
10	0x0A	FIR Filter Bank C, Coefficient 60 to Coefficient 119
11	0x0B	FIR Filter Bank D, Coefficient 0 to Coefficient 59
12	0x0C	FIR Filter Bank D, Coefficient 60 to Coefficient 119

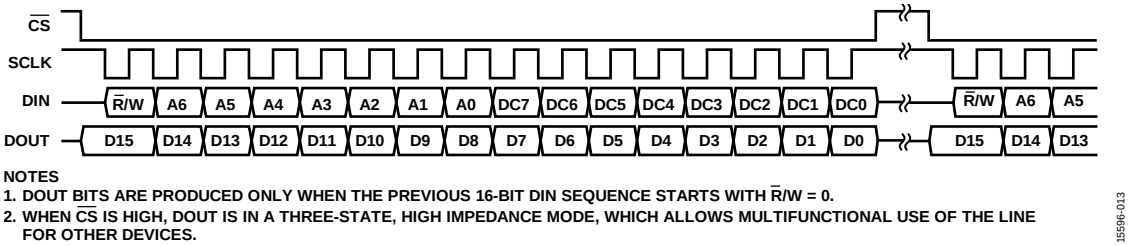


Figure 13. SPI Communication Bit Sequence

SPI COMMUNICATION

Each SPI command and response is 16 bits in length and uses the digital coding from Figure 13.

DEVICE CONFIGURATION

Each register contains 16 bits (two bytes). Bits[7:0] contain the low byte, and Bits[15:8] contain the high byte of each register. Each byte has its own unique address in the user register map (see Table 10). Update the contents of a register by writing to its low byte first and its high byte second. There are three parts to coding a SPI command (see Figure 13), which writes a new byte of data to a register: the write bit ($\overline{R}/W = 1$), the address of the byte, [A6:A0], and the new data for that location, [DC7:DC0]. Figure 14 provides a coding example for writing 0xFEDC to the XG_BIAS_LOW register (see Table 109), assuming the PAGE_ID register already equals 0x0002.

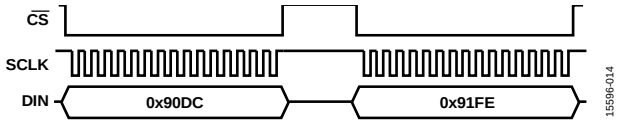


Figure 14. SPI Sequence for Writing 0xFEDC to XG_BIAS_LOW

Dual Memory Structure

The ADIS16489 uses a dual memory structure (see Figure 15) in which the SRAM supports real-time operation and the flash memory provides nonvolatile storage. During the start-up process, the operating code, calibration coefficients, and user register settings load from the flash memory into the SRAM to support normal operation. The manual flash update command (GLOB_CMD[3], see Table 151) provides a simple method for saving user register values to the flash memory. Registers with the flash backup feature are indicated by a yes in the flash backup column of Table 10. This flash backup preserves these settings for automatic recall during the next power-on or reset recovery process.

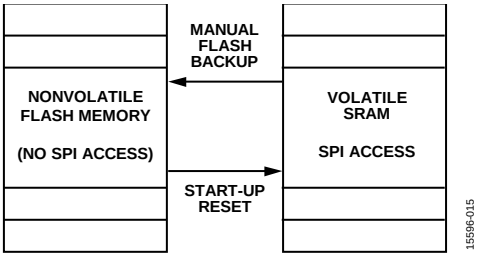


Figure 15. SRAM and Flash Memory Diagram

READING SENSOR DATA

The 16-bit command code (see Figure 13) for a read request on the SPI has three parts: the read bit ($\overline{R}/W = 0$), either address of the register, [A6:A0], and eight don't care bits, [DC7:DC0]. A read command produces the registers contents on the DOUT pin, during the following 16-bit communication cycle. Figure 16 provides an example that includes two register reads in succession. This example starts with DIN = 0x1A00, to request the contents of the Z_GYRO_OUT register, and follows with 0x1800, to request the contents of the Z_GYRO_LOW register (assuming the PROD_ID register already equals 0x0000). This is an example of full duplex operation in which the ADIS16489 receives a new request while transmitting the data response from the prior request (see Figure 16).



Figure 16. SPI Read Example

Figure 17 provides an example of the four SPI signals when reading the PROD_ID register (see Table 93) in a repeating pattern. This pattern is helpful when troubleshooting the SPI interface as it provides a clear expectation for all signals because the register contents involved never change.

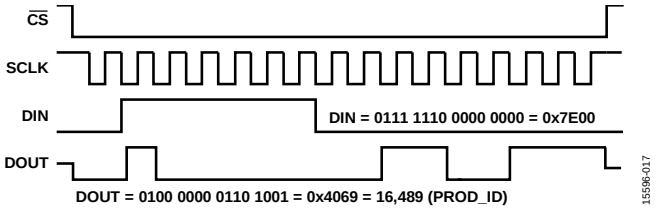


Figure 17. SPI Read Example, Second 16-Bit Sequence

USER REGISTER MEMORY MAP

Table 10. User Register Memory Map (N/A Means Not Applicable)

Name	R/W	Flash Backup	PAGE_ID	Address	Default	Register Description
PAGE_ID	R/W	No	0x00	0x00, 0x01	0x0000	Page identifier
Reserved	N/A	N/A	0x00	0x02 to 0x05	N/A	Reserved
SEQ_CNT	R	No	0x00	0x06, 0x07	N/A	Sample sequence counter
SYS_E_FLAG	R	No	0x00	0x08, 0x09	0x0000	Output, system error flags
DIAG_STS	R	No	0x00	0x0A, 0x0B	0x0000	Output, self test error flags
ALM_STS	R	No	0x00	0x0C, 0x0D	0x0000	Output, alarm error flags
TEMP_OUT	R	No	0x00	0x0E, 0x0F	N/A	Output, temperature
X_GYRO_LOW	R	No	0x00	0x10, 0x11	N/A	Output, x-axis gyroscope, low word
X_GYRO_OUT	R	No	0x00	0x12, 0x13	N/A	Output, x-axis gyroscope, high word
Y_GYRO_LOW	R	No	0x00	0x14, 0x15	N/A	Output, y-axis gyroscope, low word
Y_GYRO_OUT	R	No	0x00	0x16, 0x17	N/A	Output, y-axis gyroscope, high word
Z_GYRO_LOW	R	No	0x00	0x18, 0x19	N/A	Output, z-axis gyroscope, low word
Z_GYRO_OUT	R	No	0x00	0x1A, 0x1B	N/A	Output, z-axis gyroscope, high word
X_ACCL_LOW	R	No	0x00	0x1C, 0x1D	N/A	Output, x-axis accelerometer, low word
X_ACCL_OUT	R	No	0x00	0x1E, 0x1F	N/A	Output, x-axis accelerometer, high word
Y_ACCL_LOW	R	No	0x00	0x20, 0x21	N/A	Output, y-axis accelerometer, low word
Y_ACCL_OUT	R	No	0x00	0x22, 0x23	N/A	Output, y-axis accelerometer, high word
Z_ACCL_LOW	R	No	0x00	0x24, 0x25	N/A	Output, z-axis accelerometer, low word
Z_ACCL_OUT	R	No	0x00	0x26, 0x27	N/A	Output, z-axis accelerometer, high word
Reserved	N/A	N/A	0x00	0x28 to 0x2D	N/A	Reserved
BAROM_LOW	R	No	0x00	0x2E, 0x2F	N/A	Output, barometer, low word
BAROM_OUT	R	No	0x00	0x30, 0x31	N/A	Output, barometer, high word
Reserved	N/A	N/A	0x00	0x32 to 0x3F	N/A	Reserved
X_DELTANG_LOW	R	No	0x00	0x40, 0x41	N/A	Output, x-axis delta angle, low word
X_DELTANG_OUT	R	No	0x00	0x42, 0x43	N/A	Output, x-axis delta angle, high word
Y_DELTANG_LOW	R	No	0x00	0x44, 0x45	N/A	Output, y-axis delta angle, low word
Y_DELTANG_OUT	R	No	0x00	0x46, 0x47	N/A	Output, y-axis delta angle, high word
Z_DELTANG_LOW	R	No	0x00	0x48, 0x49	N/A	Output, z-axis delta angle, low word
Z_DELTANG_OUT	R	No	0x00	0x4A, 0x4B	N/A	Output, z-axis delta angle, high word
X_DELTVEL_LOW	R	No	0x00	0x4C, 0x4D	N/A	Output, x-axis delta velocity, low word
X_DELTVEL_OUT	R	No	0x00	0x4E, 0x4F	N/A	Output, x-axis delta velocity, high word
Y_DELTVEL_LOW	R	No	0x00	0x50, 0x51	N/A	Output, y-axis delta velocity, low word
Y_DELTVEL_OUT	R	No	0x00	0x52, 0x53	N/A	Output, y-axis delta velocity, high word
Z_DELTVEL_LOW	R	No	0x00	0x54, 0x55	N/A	Output, z-axis delta velocity, low word
Z_DELTVEL_OUT	R	No	0x00	0x56, 0x57	N/A	Output, z-axis delta velocity, high word
Reserved	N/A	N/A	0x00	0x58 to 0x77	N/A	Reserved
TIME_MS_OUT	R/W	No	0x00	0x78, 0x79	N/A	Real-time clock: minutes/seconds
TIME_DH_OUT	R/W	No	0x00	0x7A, 0x7B	N/A	Real-time clock: day/hour
TIME_YM_OUT	R/W	No	0x00	0x7C, 0x7D	N/A	Real-time clock: year/month
PROD_ID	R	Yes	0x00	0x7E, 0x7F	0x4069	Output, product identification (16,489)
Reserved	N/A	N/A	0x01	0x00 to 0x7F	N/A	Reserved
PAGE_ID	R/W	No	0x02	0x00, 0x01	0x0000	Page identifier
Reserved	N/A	N/A	0x02	0x02, 0x03	N/A	Reserved
X_GYRO_SCALE	R/W	Yes	0x02	0x04, 0x05	0x0000	Calibration, scale, x-axis gyroscope
Y_GYRO_SCALE	R/W	Yes	0x02	0x06, 0x07	0x0000	Calibration, scale, y-axis gyroscope
Z_GYRO_SCALE	R/W	Yes	0x02	0x08, 0x09	0x0000	Calibration, scale, z-axis gyroscope
X_ACCL_SCALE	R/W	Yes	0x02	0x0A, 0x0B	0x0000	Calibration, scale, x-axis accelerometer
Y_ACCL_SCALE	R/W	Yes	0x02	0x0C, 0x0D	0x0000	Calibration, scale, y-axis accelerometer
Z_ACCL_SCALE	R/W	Yes	0x02	0x0E, 0x0F	0x0000	Calibration, scale, z-axis accelerometer

Name	R/W	Flash Backup	PAGE_ID	Address	Default	Register Description
XG_BIAS_LOW	R/W	Yes	0x02	0x10, 0x11	0x0000	Calibration, offset, gyroscope, x-axis, low word
XG_BIAS_HIGH	R/W	Yes	0x02	0x12, 0x13	0x0000	Calibration, offset, gyroscope, x-axis, high word
YG_BIAS_LOW	R/W	Yes	0x02	0x14, 0x15	0x0000	Calibration, offset, gyroscope, y-axis, low word
YG_BIAS_HIGH	R/W	Yes	0x02	0x16, 0x17	0x0000	Calibration, offset, gyroscope, y-axis, high word
ZG_BIAS_LOW	R/W	Yes	0x02	0x18, 0x19	0x0000	Calibration, offset, gyroscope, z-axis, low word
ZG_BIAS_HIGH	R/W	Yes	0x02	0x1A, 0x1B	0x0000	Calibration, offset, gyroscope, z-axis, high word
XA_BIAS_LOW	R/W	Yes	0x02	0x1C, 0x1D	0x0000	Calibration, offset, accelerometer, x-axis, low word
XA_BIAS_HIGH	R/W	Yes	0x02	0x1E, 0x1F	0x0000	Calibration, offset, accelerometer, x-axis, high word
YA_BIAS_LOW	R/W	Yes	0x02	0x20, 0x21	0x0000	Calibration, offset, accelerometer, y-axis, low word
YA_BIAS_HIGH	R/W	Yes	0x02	0x22, 0x23	0x0000	Calibration, offset, accelerometer, y-axis, high word
ZA_BIAS_LOW	R/W	Yes	0x02	0x24, 0x25	0x0000	Calibration, offset, accelerometer, z-axis, low word
ZA_BIAS_HIGH	R/W	Yes	0x02	0x26, 0x27	0x0000	Calibration, offset, accelerometer, z-axis, high word
Reserved	N/A	N/A	0x02	0x28 to 0x73	0x0000	Reserved
BR_BIAS_LOW	R/W	Yes	0x02	0x40, 0x41	0x0000	Calibration, offset, barometer, low word
BR_BIAS_HIGH	R/W	Yes	0x02	0x42, 0x43	0x0000	Calibration, offset, barometer, high word
Reserved	N/A	N/A	0x02	0x28 to 0x73	0x0000	Reserved
USER_SCR_1	R/W	Yes	0x02	0x74, 0x75	0x0000	User Scratch Register 1
USER_SCR_2	R/W	Yes	0x02	0x76, 0x77	0x0000	User Scratch Register 2
USER_SCR_3	R/W	Yes	0x02	0x78, 0x79	0x0000	User Scratch Register 3
USER_SCR_4	R/W	Yes	0x02	0x7A, 0x7B	0x0000	User Scratch Register 4
FLSHCNT_LOW	R	Yes	0x02	0x7C, 0x7D	N/A	Diagnostic, flash memory count, low word
FLSHCNT_HIGH	R	Yes	0x02	0x7E, 0x7F	N/A	Diagnostic, flash memory count, high word
PAGE_ID	R/W	No	0x03	0x00, 0x01	0x0000	Page identifier
GLOB_CMD	W	No	0x03	0x02, 0x03	N/A	Control, global commands
Reserved	N/A	N/A	0x03	0x04, 0x05	N/A	Reserved
FNCTIO_CTRL	R/W	Yes	0x03	0x06, 0x07	0x000D	Control, I/O pins, functional definitions
GPIO_CTRL	R/W	Yes	0x03	0x08, 0x09	0x00X0[1]	Control, I/O pins, general purpose
CONFIG	R/W	Yes	0x03	0x0A, 0x0B	0x00C0	Control, clock, and miscellaneous correction
DEC_RATE	R/W	Yes	0x03	0x0C, 0x0D	0x0000	Control, output sample rate decimation
NULL_CNFG	R/W	Yes	0x03	0x0E, 0x0F	0x070A	Control, automatic bias correction configuration
SLP_CNT	W	No	0x03	0x10, 0x11	N/A	Control, power-down/sleep mode
Reserved	N/A	N/A	0x03	0x12 to 0x15	N/A	Reserved
FILTR_BNK_0	R/W	Yes	0x03	0x16, 0x17	0x0000	Filter selection
FILTR_BNK_1	R/W	Yes	0x03	0x18, 0x19	0x0000	Filter selection
Reserved	N/A	N/A	0x03	0x1A to 0x1F	N/A	Reserved
ALM_CNFG_0	R/W	Yes	0x03	0x20, 0x21	0x0000	Alarm configuration
ALM_CNFG_1	R/W	Yes	0x03	0x22, 0x23	0x0000	Alarm configuration
ALM_CNFG_2	R/W	Yes	0x03	0x24, 0x25	0x0000	Alarm configuration
Reserved	N/A	N/A	0x03	0x26, 0x27	N/A	Reserved
XG_ALM_MAGN	R/W	Yes	0x03	0x28, 0x29	0x0000	Alarm configuration, x-axis gyroscope
YG_ALM_MAGN	R/W	Yes	0x03	0x2A, 0x2B	0x0000	Alarm configuration, y-axis gyroscope
ZG_ALM_MAGN	R/W	Yes	0x03	0x2C, 0x2D	0x0000	Alarm configuration, z-axis gyroscope
XA_ALM_MAGN	R/W	Yes	0x03	0x2E, 0x2F	0x0000	Alarm configuration, x-axis accelerometer
YA_ALM_MAGN	R/W	Yes	0x03	0x30, 0x31	0x0000	Alarm configuration, y-axis accelerometer
ZA_ALM_MAGN	R/W	Yes	0x03	0x32, 0x33	0x0000	Alarm configuration, z-axis accelerometer
Reserved	N/A	N/A	0x03	0x34 to 0x39	N/A	Reserved
BR_ALM_MAGN	R/W	Yes	0x03	0x3A, 0x3B	0x0000	Alarm configuration, barometer
Reserved	N/A	N/A	0x03	0x3C to 0x77	N/A	Reserved
FIRM_REV	R	Yes	0x03	0x78, 0x79	N/A	Firmware revision
FIRM_DM	R	Yes	0x03	0x7A, 0x7B	N/A	Firmware programming date: day/month
FIRM_Y	R	Yes	0x03	0x7C, 0x7D	N/A	Firmware programming date: year
Reserved	N/A	N/A	0x03	0x7E, 0x7F	N/A	Reserved

Name	R/W	Flash Backup	PAGE_ID	Address	Default	Register Description
PAGE_ID	R/W	No	0x04	0x00, 0x01	0x0000	Page identifier
Reserved	N/A	N/A	0x04	0x02 to 0x1F	N/A	Reserved
PART_ID1	R	N/A	0x04	0x20, 0x21	N/A	Part Identification 1
PART_ID2	R	N/A	0x04	0x22, 0x23	N/A	Part Identification 2
PART_ID3	R	N/A	0x04	0x24, 0x25	N/A	Part Identification 3
PART_ID4	R	N/A	0x04	0x26, 0x27	N/A	Part Identification 4
Reserved	N/A	N/A	0x04	0x28 to 0x7F	N/A	Reserved
PAGE_ID	R/W	No	0x05	0x00, 0x01	0x0000	Page identifier
Reserved	N/A	N/A	0x05	0x02 to 0x07	N/A	Reserved
FIR_COEF_Axxx	R/W	Yes	0x05	0x08 to 0x7F	N/A	FIR Filter Bank A: Coefficient 0 through Coefficient 59
PAGE_ID	R/W	No	0x06	0x00, 0x01	0x0000	Page identifier
Reserved	N/A	N/A	0x06	0x02 to 0x07	N/A	Reserved
FIR_COEF_Axxx	R/W	Yes	0x06	0x08 to 0x7F	N/A	FIR Filter Bank A: Coefficient 60 through Coefficient 119
PAGE_ID	R/W	No	0x07	0x00, 0x01	0x0000	Page identifier
Reserved	N/A	N/A	0x07	0x02 to 0x07	N/A	Reserved
FIR_COEF_Bxxx	R/W	Yes	0x07	0x08 to 0x7F	N/A	FIR Filter Bank B: Coefficient 0 through Coefficient 59
PAGE_ID	R/W	No	0x08	0x00, 0x01	0x0000	Page identifier
Reserved	N/A	N/A	0x08	0x02 to 0x07	N/A	Reserved
FIR_COEF_Bxxx	R/W	Yes	0x08	0x08 to 0x7F	N/A	FIR Filter Bank B: Coefficient 60 through Coefficient 119
PAGE_ID	R/W	No	0x09	0x00, 0x01	0x0000	Page identifier
Reserved	N/A	N/A	0x09	0x02 to 0x07	N/A	Reserved
FIR_COEF_Cxxx	R/W	Yes	0x09	0x08 to 0x7F	N/A	FIR Filter Bank C: Coefficient 0 through Coefficient 59
PAGE_ID	R/W	No	0x0A	0x00, 0x01	0x0000	Page identifier
Reserved	N/A	N/A	0x0A	0x02 to 0x07	N/A	Reserved
FIR_COEF_Cxxx	R/W	Yes	0x0A	0x08 to 0x7F	N/A	FIR Filter Bank C: Coefficient 60 through Coefficient 119
PAGE_ID	R/W	No	0x0B	0x00, 0x01	0x0000	Page identifier
Reserved	N/A	N/A	0x0B	0x02 to 0x07	N/A	Reserved
FIR_COEF_Dxxx	R/W	Yes	0x0B	0x08 to 0x7F	N/A	FIR Filter Bank D: Coefficient 0 through Coefficient 59
PAGE_ID	R/W	No	0x0C	0x00, 0x01	0x0000	Page identifier
Reserved	N/A	N/A	0x0C	0x02 to 0x07	N/A	Reserved
FIR_COEF_Dxxx	R/W	Yes	0x0C	0x08 to 0x7F	N/A	FIR Filter Bank D: Coefficient 60 through Coefficient 119

[1] The GPIO_CTRL[7:4] bits reflect the logic levels on the DIOx lines and do not have a default setting.

USER REGISTER DEFINTIONS

PAGE 0 (PAGE_ID)

Table 11. PAGE_ID Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x00, 0x01	0x0000	R/W	No

Table 12. PAGE_ID Bit Definitions

Bits	Description
[15:0]	Page number, binary numerical format

The contents in the PAGE_ID register (see Table 11 and Table 12) contain the current page setting, and provide a control for selecting another page for SPI access. For example, set DIN = 0x8002 to select Page 2 for SPI-based user access. See Table 10 for the page assignments associated with each user accessible register.

SAMPLE SEQUENCE COUNTER (SEQ_CNT)

When using the internal sampling clock, the barometer output data registers (BAROM_LOW and BAROM_OUT, see Table 53 and Table 55) update at a rate of 51.25 SPS. When using the external clock, the barometers update at a rate that is 1/48th of the input clock frequency. Therefore, the update rates for the barometer does not change with the DEC_RATE register settings. SYS_E_FLAG[9] (see Table 16) offers a new data indicator bit that indicates new, unread data is in the barometer output data registers. The SEQ_CNT register provides a counter function to help determine when there is new data in the barometer registers. When SEQ_CNT = 0x0001, there is new data in the barometer output registers. When beginning a continuous read loop, read SEQ_CNT, then subtract this value from the maximum value of the range (depends on DEC_RATE setting; see Table 14) to predict the number of internal sample cycles until the next sample update in the barometer output data registers.

Table 13. SEQ_CNT Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x06, 0x07	Not applicable	R	No

Table 14. SEQ_CNT Bit Definitions

Bits	Description
[15:7]	Don't care
[6:0]	Binary counter: range = 1 to 48/(DEC_RATE + 1)

STATUS/ERROR FLAG INDICATORS (SYS_E_FLAG)

The SYS_E_FLAG register (see Table 15 and Table 16) provides various error flags. Reading this register causes all of its bits to return to 0, with the exception of Bit 7. If an error condition persists, its flag (bit) automatically returns to an alarm value of 1.

Table 15. SYS_E_FLAG Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x08, 0x09	0x0000	R	No

Table 16. SYS_E_FLAG Bit Definitions

Bits	Description
15	Watch dog timer flag. A 1 indicates that the ADIS16489 automatically reset itself to clear an issue.
[14:13]	Not used.
12	Gyroscope saturation. A 1 indicates that the rate of rotation on one axis is equal to or greater than ±480°/sec (±1 % tolerance).
[11:10]	Not used.
9	Barometer sample update. A 1 indicates that BAROM_OUT (see Table 55) and BAROM_LOW (see Table 53) registers contain new data.
8	Not used.
7	Processing overrun. A 1 indicates the occurrence of a processing overrun. Initiate a reset to recover. Replace the ADIS16489 if this error persists. One possible cause of a processing overrun error is the VDDRTC pin not being connected to a 3.3 V power supply.
6	Flash memory failure. A 1 indicates that the most recent flash memory test (GLOB_CMD[2], see Table 151) failed. Repeat test and replace the ADIS16489 if this error persists.
5	Sensor failure. A 1 indicates the failure of at least one of the self-test processes: continuous or on demand. Run the ODST (GLOB_CMD, Bit 1, see Table 151) when the unit is in not in motion. Replace the ADIS16489 if the error persists.
4	Overrange. A 1 indicates that the digital magnitude of at least one sensor has reached 99% of its maximum value. Initiate a reset to recover and replace the ADIS16489 if this error persists.
3	SPI communication error. A 1 indicates that the total number of SCLK cycles is not equal to an integer multiple of 16. Repeat the previous communication sequence to recover. Persistence in this error may indicate a weakness in the SPI service from the master processor.
[2:1]	Not used.
0	Alarm status flag. A 1 indicates that one of the user-programmable alarms is active. See the ALM_STS register for an indication of which alarm is active.

SELF TEST ERROR FLAGS (DIAG_STS)

Table 17. DIAG_STS Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x0A, 0x0B	0x0000	R	No

Table 18. DIAG_STS Bit Definitions

Bits	Description
[15:12]	Not used
11	Self test failure, barometer (1 = failure)
[10:6]	Not used
5	ODST failure, z-axis accelerometer (1 = failure)
4	ODST failure, y-axis accelerometer (1 = failure)
3	ODST failure, x-axis accelerometer (1 = failure)
2	ODST failure, z-axis gyroscope (1 = failure)
1	ODST failure, y-axis gyroscope (1 = failure)
0	Self test failure, x-axis gyroscope (1 = failure)

SYS_E_FLAG[5] (see Table 16) contains the pass and fail result (0 = pass) for on demand self test (ODST) operations, whereas the DIAG_STS register (see Table 17 and Table 18) contains pass and fail flags (0 = pass) for each inertial sensor. Reading the DIAG_STS register causes all of its bits to restore to 0. The bits in DIAG_STS return to 1 if the error conditions persists.

ALARM ERROR FLAGS (ALM_STS)

Table 19. ALM_STS Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x0C, 0x0D	0x0000	R	No

Table 20. ALM_STS Bit Definitions

Bits	Description
[15:12]	Not used
11	Barometer alarm flag (1 = alarm is active)
[10:6]	Not used
5	Z-axis accelerometer alarm flag (1 = alarm is active)
4	Y-axis accelerometer alarm flag (1 = alarm is active)
3	X-axis accelerometer alarm flag (1 = alarm is active)
2	Z-axis gyroscope alarm flag (1 = alarm is active)
1	Y-axis gyroscope alarm flag (1 = alarm is active)
0	X-axis gyroscope alarm flag (1 = alarm is active)

The ALM_STS register (see Table 19 and Table 20) contains the error flags for the alarm settings in the ALM_CNFG_0 (see Table 170) and ALM_CNFG_1 (see Table 172) registers. Reading the ALM_STS register causes all bits to restore to 0. If the alarm condition is persistent, its bit restores to a 1 in the next sample cycle.

INTERNAL TEMPERATURE (TEMP_OUT)

Table 21. TEMP_OUT Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x0E, 0x0F	Not applicable	R	No

Table 22. TEMP_OUT Bit Definitions

Bits	Description
[15:0]	Temperature data; twos complement, 0.00565°C per LSB, 25°C = 0x0000

The TEMP_OUT register (see Table 21 and Table 22) provides a coarse measurement of the temperature inside of the ADIS16489. This data is most useful for monitoring relative changes that influence the temperature inside of the ADIS16489.

Table 23. TEMP_OUT Data Format Examples

Temperature (°C)	Decimal	Hex	Binary
+85	+10,619	0x297B	0010 1001 0111 1011
+25 + 0.0113	+2	0x0002	0000 0000 0000 0010
+25 + 0.00565	+1	0x0001	0000 0000 0000 0001
+25	0	0x0000	0000 0000 0000 0000
+25 − 0.00565	−1	0xFFFF	1111 1111 1111 1111
+25 − 0.0113	−2	0xFFFE	1111 1111 1111 1110
−40	−11,504	0xD310	1101 0011 0001 0000

GYROSCOPE DATA

The gyroscopes in the ADIS16489 measure the angular rate of rotation around three orthogonal axes (x, y, and z). Figure 18 illustrates the orientation of each gyroscope axis, along with the direction of rotation that produces a positive response in each of their measurements.

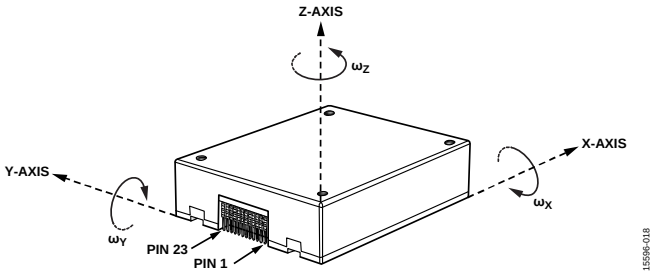


Figure 18. Gyroscope Axis and Polarity Assignments

Each gyroscope has two output data registers. Figure 19 illustrates how these two registers combine to support a 32-bit, twos complement data format for the x-axis gyroscope measurements. This format also applies to the y- and z-axes as well.

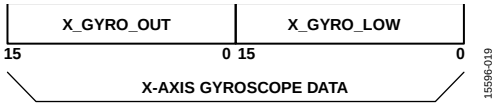


Figure 19. Gyroscope Output Data Structure

X-Axis Gyroscope (X_GYRO_LOW, X_GYRO_OUT)

Table 24. X_GYRO_LOW Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x10, 0x11	Not applicable	R	No

Table 25. X_GYRO_LOW Bit Definitions

Bits	Description
[15:0]	X-axis gyroscope data; low word

Table 26. X_GYRO_OUT Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x12, 0x13	Not applicable	R	No

Table 27. X_GYRO_OUT Bit Definitions

Bits	Description
[15:0]	X-axis gyroscope data; high word; twos complement, ±450°/sec range; 0°/sec = 0x0000, 1 LSB = 0.02°/sec

The X_GYRO_LOW (see Table 24 and Table 25) and X_GYRO_OUT (see Table 26 and

Table 27) registers contain the gyroscope data for the x-axis.

Y-Axis Gyroscope (Y_GYRO_LOW, Y_GYRO_OUT)

Table 28. Y_GYRO_LOW Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x14, 0x15	Not applicable	R	No

Table 29. Y_GYRO_LOW Bit Definitions

Bits	Description
[15:0]	Y-axis gyroscope data; low word

Table 30. Y_GYRO_OUT Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x16, 0x17	Not applicable	R	No

Table 31. Y_GYRO_OUT Bit Definitions

Bits	Description
[15:0]	Y-axis gyroscope data; high word; twos complement, ±450°/sec range; 0°/sec = 0x0000, 1 LSB = 0.02°/sec

The Y_GYRO_LOW (see Table 28 and Table 29) and Y_GYRO_OUT (see Table 30 and Table 31) registers contain the gyroscope data for the y-axis.

Z-Axis Gyroscope (Z_GYRO_LOW, Z_GYRO_OUT)

Table 32. Z_GYRO_LOW Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x18, 0x19	Not applicable	R	No

Table 33. Z_GYRO_LOW Bit Definitions

Bits	Description
[15:0]	Z-axis gyroscope data; additional resolution bits

Table 34. Z_GYRO_OUT Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x1A, 0x1B	Not applicable	R	No

Table 35. Z_GYRO_OUT Bit Definitions

Bits	Description
[15:0]	Z-axis gyroscope data; high word; twos complement, ±450°/sec range; 0°/sec = 0x0000, 1 LSB = 0.02°/sec

The Z_GYRO_LOW (see Table 32 and Table 33) and Z_GYRO_OUT (see Table 34 and Table 35) registers contain the gyroscope data for the z-axis.

Gyroscope Resolution

Table 36 and Table 37 offer various numerical examples that demonstrate the format of the angular rate (gyroscopes) data in both 16-bit and 32-bit formats.

Table 36. 16-Bit Gyroscope Data Format Examples

Rotation Rate (°/sec)	Decimal	Hex	Binary
+450	+22,500	0x57E4	0101 0111 1110 0100
+0.04	+2	0x0002	0000 0000 0000 0010
+0.02	+1	0x0001	0000 0000 0000 0001
0	0	0x0000	0000 0000 0000 0000
−0.02	−1	0xFFFF	1111 1111 1111 1111
−0.04	−2	0xFFFE	1111 1111 1111 1110
−450	−22,500	0xA81C	1010 1000 0001 1100

Table 37. 32-Bit Gyroscope Data Format Examples

Rotation Rate (°/sec)	Decimal	Hex
+450	+1,474,560,000	0x57E40000
$+0.02/2^{15}$	+2	0x00000002
$+0.02/2^{16}$	+1	0x00000001
0	0	0x00000
$-0.02/2^{16}$	−1	0xFFFFFFFF
$-0.02/2^{15}$	−2	0xFFFFFFFE
−450	−1,474,560,000	0x73600000

ACCELERATION DATA

The accelerometers in the ADIS16489 measure both dynamic and static (response to gravity) acceleration along three orthogonal axes (x, y, and z). Figure 20 illustrates the orientation of each accelerometer axis, along with the direction of acceleration that produces a positive response in each of their measurements.

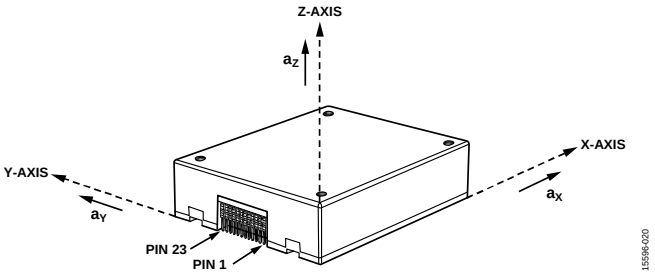


Figure 20. Accelerometer Axis and Polarity Assignments

Each accelerometer has two output data registers. Figure 21 illustrates how these two registers combine to support a 32-bit, twos complement data format for the x-axis accelerometer measurements. This format also applies to the y- and z-axes as well.

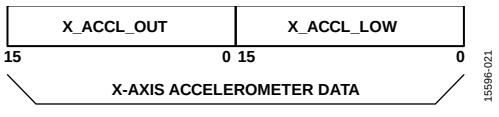


Figure 21. Accelerometer Output Data Structure

X-Axis Accelerometer (X_ACCL_LOW, X_ACCL_OUT)

Table 38. X_ACCL_LOW Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x1C, 0x1D	Not applicable	R	No

Table 39. X_ACCL_LOW Bit Definitions

Bits	Description
[15:0]	X-axis accelerometer data; low word

Table 40. X_ACCL_OUT Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x1E, 0x1F	Not applicable	R	No

Table 41. X_ACCL_OUT Definitions

Bits	Description
[15:0]	X-axis accelerometer data, high word; twos complement, ±18 *g* range; 0 *g* = 0x0000, 1 LSB = 0.8 m*g*

The X_ACCL_LOW (see Table 38 and Table 39) and X_ACCL_ OUT (see Table 40 and Table 41) registers contain the accelerometer data for the x-axis.

Y-Axis Accelerometer (Y_ACCL_LOW, Y_ACCL_OUT)

Table 42. Y_ACCL_LOW Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x20, 0x21	Not applicable	R	No

Table 43. Y_ACCL_LOW Bit Definitions

Bits	Description
[15:0]	Y-axis accelerometer data; low word

Table 44. Y_ACCL_OUT Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x22, 0x23	Not applicable	R	No

Table 45. Y_ACCL_OUT Bit Definitions

Bits	Description
[15:0]	Y-axis accelerometer data; twos complement, ±18 *g* range, 0 *g* = 0x0000, 1 LSB = 0.8 m*g*

The Y_ACCL_LOW (see Table 42 and Table 43) and Y_ACCL_ OUT (see Table 44 and Table 45) registers contain the accelerometer data for the x-axis.

Z-Axis Accelerometer (Z_ACCL_LOW, Z_ACCL_OUT)

Table 46. Z_ACCL_LOW Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x24, 0x25	Not applicable	R	No

Table 47. Z_ACCL_LOW Bit Definitions

Bits	Description
[15:0]	Z-axis accelerometer data; low word

Table 48. Z_ACCL_OUT Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x26, 0x27	Not applicable	R	No

Table 49. Z_ACCL_OUT Bit Definitions

Bits	Description
[15:0]	Z-axis accelerometer data, high word; twos complement, ±18 *g* range; 0 *g* = 0x0000, 1 LSB = 0.8 m*g*

The Z_ACCL_LOW (see Table 46 and Table 47) and Z_ACCL_ OUT (see Table 48 and Table 49) registers contain the accelerometer data for the z-axis.

Accelerometer Resolution

Table 50 and Table 51 offer various numerical examples that demonstrate the format of the linear acceleration data in both 16-bit and 32-bit formats.

Table 50. 16-Bit Accelerometer Data Format Examples

Acceleration	Decimal	Hex	Binary
+18 *g*	+20,000	0x4E20	0100 1110 0010 0000
+1.6 m*g*	+2	0x0002	0000 0000 0000 0010
+0.8 m*g*	+1	0x0001	0000 0000 0000 0001
0 m*g*	0	0x0000	0000 0000 0000 0000
−0.8 m*g*	−1	0xFFFF	1111 1111 1111 1111
−1.6 m*g*	−2	0xFFFE	1111 1111 1111 1110
−18 *g*	−20,000	0xB1E0	1011 0001 1110 0000

Table 51. 32-Bit Accelerometer Data Format Examples

Acceleration (*g*)	Decimal	Hex
+18	+1,310,720,000	0x4E200000
$+0.0008/2^{15}$	+2	0x00000002
$+0.0008/2^{16}$	+1	0x00000001
0	0	0x00000000
$-0.0008/2^{16}$	−1	0xFFFFFFFF
$-0.0008/2^{15}$	−2	0xFFFFFFFE
−18	−1,310,720,000	0xB1E00000

BAROMETER DATA

The barometer measures the atmospheric pressure. The barometer has two output data registers: BAROM_LOW and BAROM_OUT. Figure 22 illustrates how these two registers combine to support 32-bit, twos complement data format for the pressure measurements.

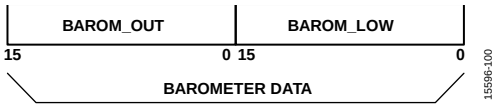


Figure 22. Barometer Output Data Structure

Barometer (BAROM_LOW, BAROM_OUT)

Table 52. BAROM_LOW Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x2E, 0x2F	Not applicable	R	No

Table 53. BAROM_LOW Bit Definitions

Bits	Description
[15:0]	Barometer data; low word

Table 54. BAROM_OUT Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x30, 0x31	Not applicable	R	No

Table 55. BAROM_OUT Bit Definitions

Bits	Description
[15:0]	Barometer data; high word; twos complement, ±1.31 range; 0 bar = 0x0000, 1 LSB = 40µbar

The BAROM_LOW (see Table 52 and Table 53) and BAROM_OUT (see Table 54 and Table 55) registers contain the barometer data.

Barometer Resolution

Table 56 and Table 57 offer various numerical examples that demonstrate the format of the pressure (barometer) data in both 16-bit and 32-bit formats.

Table 56. 16-Bit Barometer Data Format Examples

Pressure	Decimal	Hex	Binary
+1.31068 bar	+32767	0x3FFF	0111 1111 1111 1111
+80 µbar	+2	0x0002	0000 0000 0000 0010
+40 µbar	+1	0x0001	0000 0000 0000 0001
0	0	0x0000	0000 0000 0000 0000
−40 µbar	−1	0xFFFF	1111 1111 1111 1111
−80 µbar	−2	0xFFFE	1111 1111 1111 1110
−1.31072	−32768	0x4000	1000 0000 0000 0000

Table 57. 32-Bit Barometer Data Format Examples

Pressure	Decimal	Hex
+1.31068 bar	+4,294,967,295	0x3FFFFFFF
+80 µbar ÷ 2^{16}	+2	0x00000002
+40 µbar ÷ 2^{16}	+1	0x00000001
0	0	0x00000000
−40 µbar ÷ 2^{16}	−1	0xFFFFFFFF
−80 µbar ÷ 2^{16}	−2	0xFFFFFFFE
−1.31072	−4,294,967,296	0x40000000

DELTA ANGLES

In addition to the angular rate of rotation (gyroscope) measurements around each axis (x, y, and z), the ADIS16489 also provides delta angle measurements that represent a computation of angular displacement between each sample update.

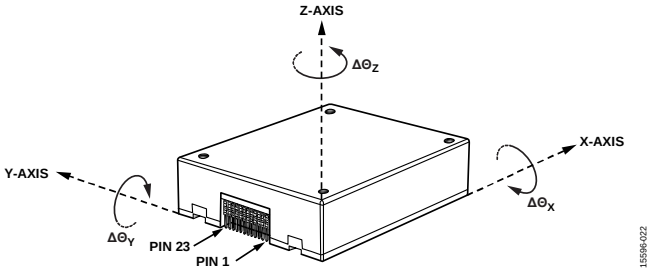


Figure 23. Delta Angle Axis and Polarity Assignments

The delta angle outputs represent an integration of the gyroscope measurements and use the following formula for all three axes (x-axis displayed):

$$\Delta\theta_{x,nD} = \frac{1}{2 f_S} \times \sum_{d=0}^{D-1} \left(\omega_{x,nD+d} + \omega_{x,nD+d-1} \right)$$

where:
D is the decimation rate = DEC_RATE + 1 (see Table 159).
f_S is the sample rate.
d is the incremental variable in the summation formula.
ω_x is the x-axis rate of rotation (gyroscope).
n is the sample time, prior to the decimation filter.

When using the internal sample clock, f_S is equal to 2460 SPS. When using the external clock option, f_S is equal to the frequency of the external clock. The external clock frequency must be at least 700 Hz to prevent overflow in the delta angle data registers at high rotation rates.

Each axis of the delta angle measurements has two output data registers. Figure 24 illustrates how these two registers combine to support a 32-bit, twos complement data format for the x-axis delta angle measurements. This format also applies to the y- and x-axes as well.

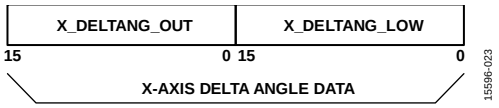


Figure 24. Delta Angle Output Data Structure

X-Axis Delta Angle (X_DELTANG_LOW, X_DELTANG_OUT)

Table 58. X_DELTANG_LOW Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x40, 0x41	Not applicable	R	No

Table 59. X_DELTANG_LOW Bit Definitions

Bits	Description
[15:0]	X-axis delta angle data; low word

Table 60. X_DELTANG_OUT Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x42, 0x43	Not applicable	R	No

Table 61. X_DELTANG_OUT Bit Definitions

Bits	Description
[15:0]	X-axis delta angle data; twos complement, ±720° range, 0° = 0x0000, 1 LSB = 720°/2^{15} = ~0.022°

The X_DELTANG_LOW (see Table 58 and Table 59) and X_DELTANG_OUT (see Table 60 and Table 61) registers contain the delta angle data for the x-axis.

Y-Axis Delta Angle (Y_DELTANG_LOW, Y_DELTANG_OUT)

Table 62. Y_DELTANG_LOW Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x44, 0x45	Not applicable	R	No

Table 63. Y_DELTANG_LOW Bit Definitions

Bits	Description
[15:0]	Y-axis delta angle data; low word

Table 64. Y_DELTANG_OUT Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x46, 0x47	Not applicable	R	No

Table 65. Y_DELTANG_OUT Bit Definitions

Bits	Description
[15:0]	Y-axis delta angle data; twos complement, ±720° range, 0° = 0x0000, 1 LSB = 720°/2^{15} = ~0.022°

The Y_DELTANG_LOW (see Table 62 and Table 63) and Y_DELTANG_OUT (see Table 64 and Table 65) registers contain the delta angle data for the y-axis.

Z-Axis Delta Angle (Z_DELTANG_LOW, Z_DELTANG_OUT)

Table 66. Z_DELTANG_LOW Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x48, 0x49	Not applicable	R	No

Table 67. Z_DELTANG_LOW Bit Definitions

Bits	Description
[15:0]	Z-axis delta angle data; low word

Table 68. Z_DELTANG_OUT Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x4A, 0x4B	Not applicable	R	No

Table 69. Z_DELTANG_OUT Bit Definitions

Bits	Description
[15:0]	Z-axis delta angle data; twos complement, ±720° range, 0° = 0x0000, 1 LSB = 720°/2^{15} = ~0.022°

The Z_DELTANG_LOW (see Table 66 and Table 67) and Z_DELTANG_OUT (see Table 68 and Table 69) registers contain the delta angle data for the z-axis.

Delta Angle Resolution

Table 70 and Table 71 offers various numerical examples that demonstrate the format of the delta-angle data in 16-bit and 32-bit formats.

Table 70. 16-Bit Delta Angle Data Format Examples

Delta Angle (°)	Decimal	Hex	Binary
$+720 \times (2^{15} - 1)/2^{15}$	+32,767	0x7FFF	0111 1111 1110 1111
$+720/2^{14}$	+2	0x0002	0000 0000 0000 0010
$+720/2^{15}$	+1	0x0001	0000 0000 0000 0001
0	0	0x0000	0000 0000 0000 0000
$-720/2^{15}$	−1	0xFFFF	1111 1111 1111 1111
$-720/2^{14}$	−2	0xFFFE	1111 1111 1111 1110
−720	−32,768	0x8000	1000 0000 0000 0000

Table 71. 32-Bit Delta Angle Data Format Examples

Delta Angle (°)	Decimal	Hex
$+720 \times (2^{31} - 1)/2^{31}$	+2,147,483,647	0x7FFFFFFF
$+720/2^{30}$	+2	0x00000002
$+720/2^{31}$	+1	0x00000001
0	0	0x00000000
$-720/2^{31}$	−1	0xFFFFFFFF
$-720/2^{30}$	−2	0xFFFFFFFE
−720	−2,147,483,648	0x80000000

DELTA VELOCITY

In addition to the linear acceleration measurements along each axis (x, y, and z), the ADIS16489 also provides delta velocity measurements that represent a computation of linear velocity change between each sample update.

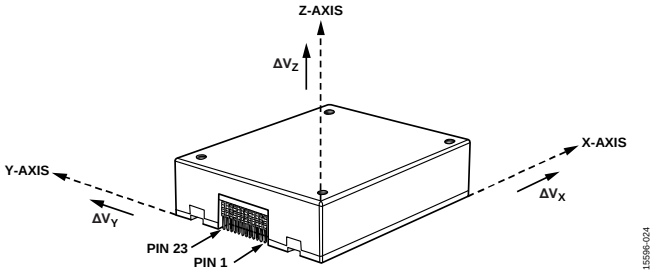


Figure 25. Delta Velocity Axis and Polarity Assignments

The delta velocity outputs represent an integration of the acceleration measurements and use the following formula for all
three axes (x-axis displayed):

$$\Delta V_{x,nD} = \frac{1}{2 f_S} \times \sum_{d=0}^{D-1} \left(a_{x,nD+d} + a_{x,nD+d-1} \right)$$

where:
D is the decimation rate = DEC_RATE + 1 (see Table 159).
f_S is the sample rate.
d is the incremental variable in the summation formula.
a_x is the x-axis acceleration (accelerometer).
n is the sample time, prior to the decimation filter.

When using the internal sample clock, f_S is equal to 2460 SPS. When using the external clock option, f_S is equal to the frequency of the external clock. The frequency external of the clock must be at least 700 Hz to prevent overflow in the delta velocity data registers at high acceleration levels.

Each axis of the delta velocity measurements has two output data registers. Figure 26 illustrates how these two registers combine to support 32-bit, twos complement data format, for the x-axis delta velocity measurements. This format also applies to the y- and z-axes as well.

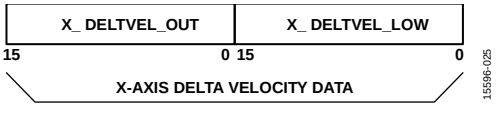


Figure 26. Delta Angle Output Data Structure

X-Axis Delta Velocity (X_DELTVEL_LOW, X_DELTVEL_OUT)

Table 72. X_DELTVEL_LOW Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x4C, 0x4D	Not applicable	R	No

Table 73. X_DELTVEL_LOW Bit Definitions

Bits	Description
[15:0]	X-axis delta angle data; low word

Table 74. X_DELTVEL_OUT Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x4E, 0x4F	Not applicable	R	No

Table 75. X_DELTVEL_OUT Bit Definitions

Bits	Description
[15:0]	X-axis delta velocity data; twos complement, ±200 m/sec range, 0 m/sec = 0x0000; 1 LSB = 200 m/sec ÷ 2^{15} = ~6.104 mm/sec

The X_DELTVEL_LOW (see Table 72 and Table 73) and X_DELTVEL_OUT (see Table 74 and Table 75) registers contain the delta velocity data for the x-axis.

Y-Axis Delta Velocity (Y_DELTVEL_LOW, Y_DELTVEL_OUT)

Table 76. Y_DELTVEL_LOW Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x50, 0x51	Not applicable	R	No

Table 77. Y_DELTVEL_LOW Bit Definitions

Bits	Description
[15:0]	Y-axis delta velocity data; low word

Table 78. Y_DELTVEL_OUT Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x52, 0x53	Not applicable	R	No

Table 79. Y_DELTVEL_OUT Bit Definitions

Bits	Description
[15:0]	Y-axis delta velocity data; twos complement, ±50 m/sec range, 0 m/sec = 0x0000; 1 LSB = 50 m/sec ÷ 2^{15} = ~1.526 mm/sec

The Y_DELTVEL_LOW (see Table 76 and Table 77) and Y_DELTVEL_OUT (see Table 78 and Table 79) registers contain the delta velocity data for the y-axis.

Z-Axis Delta Velocity (Z_DELTVEL_LOW, Z_DELTVEL_OUT)

Table 80. Z_DELTVEL_LOW Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x54, 0x55	Not applicable	R	No

Table 81. Z_DELTVEL_LOW Bit Definitions

Bits	Description
[15:0]	Z-axis delta angle data; low word

Table 82. Z_DELTANG_OUT Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x56, 0x57	Not applicable	R	No

Table 83. Z_DELTVEL_OUT Bit Definitions

Bits	Description
[15:0]	Z-axis delta velocity data; twos complement, ±200 m/sec range, 0 m/sec = 0x0000; 1 LSB = 200 m/sec ÷ 2^{15} = ~6.104 mm/sec

The Z_DELTVEL_LOW (see Table 80 and Table 81) and Z_DELTVEL_OUT (see Table 82 and Table 83) registers contain the delta velocity data for the z-axis.

Delta Velocity Resolution

Table 84 and Table 85 offer various numerical examples that demonstrate the format of the delta velocity data in both 16-bit and 32-bit formats.

Table 84. 16-Bit Delta Velocity Data Format Examples

Velocity (m/sec)	Decimal	Hex	Binary
+200 × (2^{15} − 1)/2^{15}	+32,767	0x7FFF	0111 1111 1110 1111
+200/2^{14}	+2	0x0002	0000 0000 0000 0010
+200/2^{15}	+1	0x0001	0000 0000 0000 0001
0	0	0x0000	0000 0000 0000 0000
−200/2^{15}	−1	0xFFFF	1111 1111 1111 1111
−200/2^{14}	−2	0xFFFE	1111 1111 1111 1110
−200	−32,768	0x8000	1000 0000 0000 0000

Table 85. 32-Bit Delta Velocity Data Format Examples

Velocity (m/sec)	Decimal	Hex
+200 × (2^{31} − 1)/2^{31}	+2,147,483,647	0x7FFFFFFF
+200/2^{30}	+2	0x00000002
+200/2^{31}	+1	0x00000001
0	0	0x00000000
−200/2^{31}	−1	0xFFFFFFFF
−200/2^{30}	−2	0xFFFFFFFE
−200	−2,147,483,648	0x80000000

REAL-TIME CLOCK

The VDDRTC power supply pin (see Table 6, Pin 23) provides a separate supply for the real-time clock (RTC) function. Connecting the VDDTC pin to its own 3.3 V supply enables the RTC to keep track of time, even when the main supply (VDD) is off.

Configure the RTC function by selecting one of two modes in CONFIG[0] (see Table 157). The real-time clock data is available in the TIME_MS_OUT register (see Table 87), TIME_DH_OUT register (see Table 89), and TIME_YM_OUT register (see Table 91). When using the elapsed timer mode, the time data registers start at 0x0000 when the device starts up (or resets) and begin keeping time in a manner that is similar to a stopwatch.

When using the clock/calendar mode, write the current time to the real-time registers in the following sequence: seconds (TIME_ MS_OUT[5:0]), minutes (TIME_ MS_OUT[13:8]), hours (TIME_DH_OUT[5:0]), day (TIME_DH_OUT[12:8]), month (TIME_YM_OUT[3:0]), and year (TIME_YM_OUT[14:8]).

The updates to the timer become active only after a write to the TIME_YM_OUT[14:8] byte is complete.

The real-time clock registers reflect the newly updated values only after the next seconds tick of the clock that follows the write to TIME_YM_OUT[14:8] (year). Writing to TIME_YM_OUT[14:8] activates all timing values; therefore, always write to this location last when updating the timer, even if the year information does not require updating.

Write the current time to each time data register after setting CONFIG[0] = 1 (DIN = 0x8003, DIN = 0x8AC1, DIN = 0x8B00). This sequence preserves the factory default for other bits in the CONFIG register. After configuring the CONFIG register, set GLOB_CMD[3] = 1 (DIN = 0x8003, DIN = 0x8204, DIN = 0x8300) to back up these settings in flash, and use a separate 3.3 V source to supply power to the VDDRTC function. While only VDDRTC needs to have power for time tracking, access to the time data in the TIME_xx_OUT registers requires normal operation (VDD = 3.3 V and full startup).

Real-Time Clock: Minutes/Seconds (TIME_MS_OUT)

Table 86. TIME_MS_OUT Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x78, 0x79	Not applicable	R/W	No

Table 87. TIME_MS_OUT Bit Definitions

Bits	Description
[15:14]	Not used
[13:8]	Minutes, binary data, range = 0 to 59
[7:6]	Not used
[5:0]	Seconds, binary data, range = 0 to 59

Real-Time Clock: Days/Hours (TIME_DH_OUT)

Table 88. TIME_DH_OUT Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x7A, 0x7B	Not applicable	R/W	No

Table 89. TIME_DH_OUT Bit Definitions

Bits	Description
[15:13]	Not used
[12:8]	Day, binary data, range = 1 to 31
[7:6]	Not used
[5:0]	Hours, binary data, range = 0 to 23

Real-Time Clock: Years/Months (TIME_YM_OUT)

Table 90. TIME_YM_OUT Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x7C, 0x7D	Not applicable	R/W	No

Table 91. TIME_YM_OUT Bit Definitions

Bits	Description
[15]	Not used
[14:8]	Year, binary data, range = 0 to 99, relative to 2000 A.D.
[7:4]	Not used
[3:0]	Month, binary data, range = 1 to 12

Product Identification (PROD_ID)

Table 92. PROD_ID Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x7E, 0x7F	0x4069	R	Yes

Table 93. PROD_ID Bit Definitions

Bits	Description
[15:0]	Product identification = 0x4069

The PROD_ID register (see Table 92 and Table 93) contains the numerical portion of the part number (16489). See Figure 17 for an example of how to use a looping read of this register to validate the integrity of the communication.

PAGE 2 (PAGE_ID)

Table 94. PAGE_ID Register Definition

Page	Addresses	Default	Access	Flash Backup
0x02	0x00, 0x01	0x0000	R/W	No

Table 95. PAGE_ID Bit Assignments

Bits	Description
[15:0]	Page number, binary numerical format

The contents in the PAGE_ID register (see Table 94 and Table 95) contain the current page setting, and provide a control for selecting another page for SPI access. For example, set DIN = 0x8002 to select Page 2 for SPI-based user access. See Table 10 for the page assignments associated with each user accessible register.

CALIBRATION

The signal chain of each inertial sensor (accelerometers, gyroscopes) includes application of unique correction formulas, which come from extensive characterization of bias, sensitivity, alignment, and response to linear acceleration (gyroscopes) over a temperature range of −40°C to +85°C for every single ADIS16489. These correction formulas are not accessible, but users do have the opportunity to adjust bias and scale factor, for each sensor individually, through user accessible registers. These correction factors follow immediately after the factory derived correction formulas in the signal chain, which processes at a rate of 2460 Hz when using the internal sample clock (see f_S in Figure 33).

Calibration, Gyroscope Scale (X_GYRO_SCALE)

Table 96. X_GYRO_SCALE Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x02	0x04, 0x05	0x0000	R/W	Yes

Table 97. X_GYRO_SCALE Bit Definitions

Bits	Description
[15:0]	X-axis gyroscope scale correction; twos complement, 0x0000 = unity gain, 1 LSB = $1 \div 2^{15}$ = ~0.003052%

The X_GYRO_SCALE register (see Table 96 and Table 97) provides users with the opportunity to adjust the scale factor for the x-axis gyroscopes. See Figure 27 for an illustration of how this scale factor influences the x-axis gyroscope data.

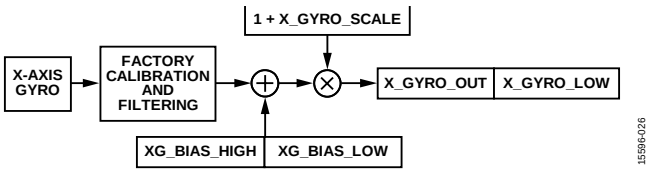


Figure 27. User Calibration Signal Path, Gyroscopes

Calibration, Gyroscope Scale (Y_GYRO_SCALE)

Table 98. Y_GYRO_SCALE Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x02	0x06, 0x07	0x0000	R/W	Yes

Table 99. Y_GYRO_SCALE Bit Definitions

Bits	Description
[15:0]	Y-axis gyroscope scale correction; twos complement, 0x0000 = unity gain, 1 LSB = $1 \div 2^{15}$ = ~0.003052%

The Y_GYRO_SCALE register (see Table 98 and Table 99) allows users to adjust the scale factor for the y-axis gyroscopes. This register influences the y-axis gyroscope measurements in the same manner that X_GYRO_SCALE influences the x-axis gyroscope measurements (see Figure 27).

Calibration, Gyroscope Scale (Z_GYRO_SCALE)

Table 100. Z_GYRO_SCALE Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x02	0x08, 0x09	0x0000	R/W	Yes

Table 101. Z_GYRO_SCALE Bit Definitions

Bits	Description
[15:0]	Z-axis gyroscope scale correction; twos complement, 0x0000 = unity gain, 1 LSB = $1 \div 2^{15}$ = ~0.003052%

The Z_GYRO_SCALE register (see Table 100 and Table 101) allows users to adjust the scale factor for the z-axis gyroscopes. This register influences the z-axis gyroscope measurements in the same manner that X_GYRO_SCALE influences the x-axis gyroscope measurements (see Figure 27).

Calibration, Accelerometer Scale (X_ACCL_SCALE)

Table 102. X_ACCL_SCALE Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x02	0x0A, 0x0B	0x0000	R/W	Yes

Table 103. X_ACCL_SCALE Bit Definitions

Bits	Description
[15:0]	X-axis accelerometer scale correction; twos complement, 0x0000 = unity gain, 1 LSB = $1 \div 2^{15}$ = ~0.003052%

The X_ACCL_SCALE register (see Table 102 and Table 103) allows users to adjust the scale factor for the x-axis accelerometers. See Figure 28 for an illustration of how this scale factor influences the x-axis accelerometer data.

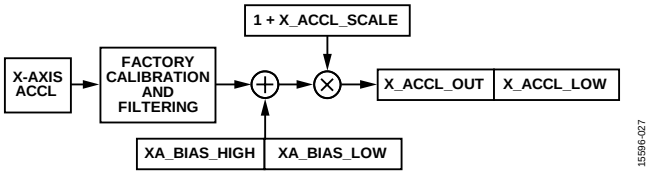


Figure 28. User Calibration Signal Path, Accelerometers

Calibration, Accelerometer Scale (Y_ACCL_SCALE)

Table 104. Y_ACCL_SCALE Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x02	0x0C, 0x0D	0x0000	R/W	Yes

Table 105. Y_ACCL_SCALE Bit Definitions

Bits	Description
[15:0]	Y-axis accelerometer scale correction; twos complement, 0x0000 = unity gain, 1 LSB = $1 \div 2^{15}$ = ~0.003052%

The Y_ACCL_SCALE register (see Table 104 and Table 105) allows users to adjust the scale factor for the y-axis accelerometers. This register influences the y-axis accelerometer measurements in the same manner that the X_ACCL_SCALE influences the x-axis accelerometer measurements (see Figure 28).

Calibration, Accelerometer Scale (Z_ACCL_SCALE)

Table 106. Z_ACCL_SCALE Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x02	0x0E, 0x0F	0x0000	R/W	Yes

Table 107. Z_ACCL_SCALE Bit Definitions

Bits	Description
[15:0]	Z-axis accelerometer scale correction; twos complement, 0x0000 = unity gain, 1 LSB = $1 \div 2^{15}$ = ~0.003052%

The Z_ACCL_SCALE register (see Table 106 and Table 107) allows users to adjust the scale factor for the z-axis accelerometers. This register influences the z-axis accelerometer measurements in the same manner that the X_ACCL_SCALE influences the x-axis accelerometer measurements (see Figure 28).

Calibration, Gyroscope Bias (XG_BIAS_LOW, XG_BIAS_HIGH)

Table 108. XG_BIAS_LOW Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x02	0x10, 0x11	0x0000	R/W	Yes

Table 109. XG_BIAS_LOW Bit Definitions

Bits	Description
[15:0]	X-axis gyroscope offset correction, low word

Table 110. XG_BIAS_HIGH Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x02	0x12, 0x13	0x0000	R/W	Yes

Table 111. XG_BIAS_HIGH Bit Definitions

Bits	Description
[15:0]	X-axis gyroscope offset correction, high word twos complement, 0°/sec = 0x0000, 1 LSB = 0.02°/sec

The XG_BIAS_LOW (see Table 108 and Table 109) and XG_BIAS_HIGH (see Table 110 and Table 111) registers combine to allow users to adjust the bias of the x-axis gyroscopes. Table 36 and Table 37 offer numerous examples of this data format, in both 16-bit and 32-bit formats. See Figure 27 for an illustration of how these two registers combine and influence the x-axis gyroscope measurements.

Calibration, Gyroscope Bias (YG_BIAS_LOW, YG_BIAS_HIGH)

Table 112. YG_BIAS_LOW Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x02	0x14, 0x15	0x0000	R/W	Yes

Table 113. YG_BIAS_LOW Bit Definitions

Bits	Description
[15:0]	Y-axis gyroscope offset correction, low word

Table 114. YG_BIAS_HIGH Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x02	0x16, 0x17	0x0000	R/W	Yes

Table 115. YG_BIAS_HIGH Bit Definitions

Bits	Description
[15:0]	Y-axis gyroscope offset correction, high word; twos complement, 0°/sec = 0x0000, 1 LSB = 0.02°/sec

The YG_BIAS_LOW (see Table 112 and Table 113) and YG_BIAS_HIGH (see Table 114 and Table 115) registers combine to allow users to adjust the bias of the y-axis gyroscopes. Table 36 and Table 37 offer numerous examples of this data format, in both 16-bit and 32-bit formats. See Figure 27 for an illustration of how these two registers combine and influence the y-axis gyroscope measurements.

Calibration, Gyroscope Bias (ZG_BIAS_LOW, ZG_BIAS_HIGH)

Table 116. ZG_BIAS_LOW Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x02	0x18, 0x19	0x0000	R/W	Yes

Table 117. ZG_BIAS_LOW Bit Definitions

Bits	Description
[15:0]	Z-axis gyroscope offset correction, low word

Table 118. ZG_BIAS_HIGH Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x02	0x1A, 0x1B	0x0000	R/W	Yes

Table 119. ZG_BIAS_HIGH Bit Definitions

Bits	Description
[15:0]	Z-axis gyroscope offset correction, high word twos complement, 0°/sec = 0x0000, 1 LSB = 0.02°/sec

The ZG_BIAS_LOW (see Table 116 and Table 117) and ZG_BIAS_HIGH (see Table 118 and Table 119) registers combine to allow users to adjust the bias of the z-axis gyroscopes. Table 36 and Table 37 offer numerous examples of this data format, in both 16-bit and 32-bit formats. See Figure 27 for an illustration of how these two registers combine and influence the z-axis gyroscope measurements.

Calibration, Accelerometer Bias (XA_BIAS_LOW, XA_BIAS_HIGH)

Table 120. XA_BIAS_LOW Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x02	0x1C, 0x1D	0x0000	R/W	Yes

Table 121. XA_BIAS_LOW Bit Definitions

Bits	Description
[15:0]	X-axis accelerometer offset correction, low word

Table 122. XA_BIAS_HIGH Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x02	0x1E, 0x1F	0x0000	R/W	Yes

Table 123. XA_BIAS_HIGH Bit Definitions

Bits	Description
[15:0]	X-axis accelerometer offset correction, high word, twos complement, 0 *g* = 0x0000, 1 LSB = 0.8 m*g*

The XA_BIAS_LOW (see Table 120 and Table 121) and XA_BIAS_HIGH (see Table 122 and Table 123) registers combine to allow users to adjust the bias of the x-axis accelerometers. Table 50 and Table 51 offer numerous examples of data format, in both 16-bit and 32-bit formats. See Figure 28 for an illustration of how these two registers combine and influence the x-axis accelerometer measurements.

Calibration, Accelerometer Bias (YA_BIAS_LOW, YA_BIAS_HIGH)

Table 124. YA_BIAS_LOW Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x02	0x20, 0x21	0x0000	R/W	Yes

Table 125. YA_BIAS_LOW Bit Definitions

Bits	Description
[15:0]	Y-axis accelerometer offset correction, low word

Table 126. YA_BIAS_HIGH Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x02	0x22, 0x23	0x0000	R/W	Yes

Table 127. YA_BIAS_HIGH Bit Definitions

Bits	Description
[15:0]	Y-axis accelerometer offset correction, high word, twos complement, 0 *g* = 0x0000, 1 LSB = 0.8 m*g*

The YA_BIAS_LOW (see Table 124 and Table 125) and YA_BIAS_HIGH (see Table 126 and Table 127) registers combine to allow users to adjust the bias of the y-axis accelerometers. Table 50 and Table 51 offer numerous examples of data format, in both 16-bit and 32-bit formats. See Figure 28 for an illustration

of how these two registers combine and influence the y-axis accelerometer measurements.

Calibration, Accelerometer Bias (ZA_BIAS_LOW, ZA_BIAS_HIGH)

Table 128. ZA_BIAS_LOW Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x02	0x24, 0x25	0x0000	R/W	Yes

Table 129. ZA_BIAS_LOW Bit Definitions

Bits	Description
[15:0]	Z-axis accelerometer offset correction, low word

Table 130. ZA_BIAS_HIGH Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x02	0x26, 0x27	0x0000	R/W	Yes

Table 131. ZA_BIAS_HIGH Bit Definitions

Bits	Description
[15:0]	Z-axis accelerometer offset correction, high word, twos complement, 0 *g* = 0x0000, 1 LSB = 0.8 m*g*

The ZA_BIAS_LOW (see Table 128 and Table 129) and ZA_BIAS_HIGH (see Table 130 and Table 131) registers combine to allow users to adjust the bias of the z-axis accelerometers. Table 50 and Table 51 offer numerous examples of data format, in both 16-bit and 32-bit formats. See Figure 28 for an illustration of how these two registers combine and influence the z-axis accelerometer measurements.

BAROMETERS

Calibration, Barometer Bias (BR_BIAS_LOW, BR_BIAS_HIGH)

The BR_BIAS_LOW (see Table 132 and Table 133) and BR_BIAS_HIGH (see Table 134 and Table 135) registers provide a user configurable, bias correction function for the barometer measurement. See Figure 29 for the location and influence that this correction factor has in the barometer signal chain.

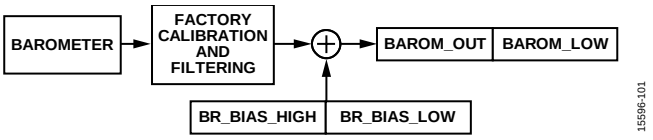


Figure 29. User Calibration Signal Path, Accelerometers

Table 132. BR_BIAS_LOW Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x02	0x40, 0x41	0x0000	R/W	Yes

Table 133. BR_BIAS_LOW Bit Definitions

Bits	Description
[15:0]	Barometric pressure bias correction factor, low word

Table 134. BR_BIAS_HIGH Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x02	0x42, 0x43	0x0000	R/W	Yes

Table 135. BR_BIAS_HIGH Bit Definitions

Bits	Description
[15:0]	Barometric pressure bias correction factor, high word, twos complement, ±1.3 bar measurement range, 0 bar = 0x0000, 1 LSB = 40 µbar

The digital format examples in Table 56 also apply to the BR_BIAS_HIGH register and the digital format examples in Table 57 apply to the 32-bit number that comes from combining BR_BIAS_LOW and BR_BIAS_HIGH.

SCRATCH REGISTERS (USER_SCR_x)

Table 136. USER_SCR_1 Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x02	0x74, 0x75	0x0000	R/W	Yes

Table 137. USER_SCR_1 Bit Definitions

Bits	Description
[15:0]	User defined

Table 138. USER_SCR_2 Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x02	0x76, 0x77	0x0000	R/W	Yes

Table 139. USER_SCR_2 Bit Definitions

Bits	Description
[15:0]	User defined

Table 140. USER_SCR_3 Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x02	0x78, 0x79	0x0000	R/W	Yes

Table 141. USER_SCR_3 Bit Definitions

Bits	Description
[15:0]	User defined

Table 142. USER_SCR_4 Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x02	0x7A, 0x7B	0x0000	R/W	Yes

Table 143. USER_SCR_4 Bit Definitions

Bits	Description
[15:0]	User defined

The USER_SCR_1 (see Table 136 and Table 137), USER_SCR_2 (see Table 138 and Table 139), USER_SCR_3 (see Table 140 and Table 141), and USER_SCR_4 (see Table 142 and Table 143) registers provide four locations for users to store information.

FLASH MEMORY ENDURANCE COUNTER (FLSHCNT_LOW, FLSHCNT_HIGH)

Table 144. FLSHCNT_LOW Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x02	0x7C, 0x7D	Not applicable	R	Yes

Table 145. FLSHCNT_LOW Bit Definitions

Bits	Description
[15:0]	Flash memory write counter, low word

Table 146. FLSHCNT_HIGH Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x02	0x7E, 0x7F	Not applicable	R	Yes

Table 147. FLSHCNT_HIGH Bit Definitions

Bits	Description
[15:0]	Flash memory write counter, high word

The FLSHCNT_LOW (see Table 144 and Table 145) and FLSHCNT_HIGH (see Table 146 and Table 147) registers combine to provide a 32-bit, binary counter that tracks the number of flash memory write cycles. In addition to the number of write cycles, the flash memory has a finite service lifetime, which depends on the junction temperature. Figure 30 provides some guidance for estimating the retention life for the flash memory at specific junction temperatures. The junction temperature is approximately 7°C above the case temperature.

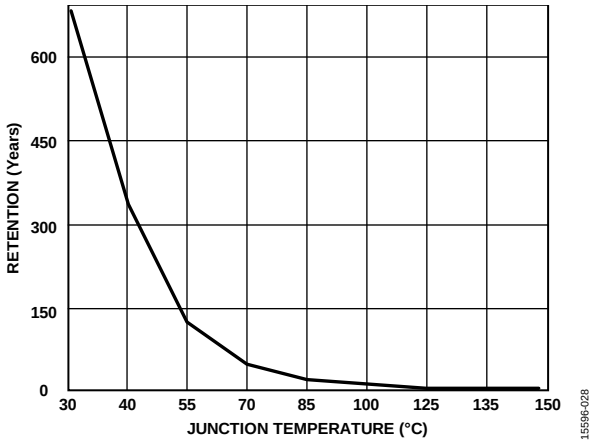


Figure 30. Flash Memory Retention

PAGE 3 (PAGE_ID)

Table 148. PAGE_ID Register Definition

Page	Addresses	Default	Access	Flash Backup
0x03	0x00, 0x01	0x0000	R/W	No

Table 149. PAGE_ID Bit Assignments

Bits	Description
[15:0]	Page number, binary numerical format

The contents in the PAGE_ID register (see Table 148 and Table 149) contain the current page setting, and provide a control for selecting another page for SPI access. For example, set DIN = 0x8002 to select Page 2 for SPI-based user access. See Table 10 for the page assignments associated with each user accessible register.

GLOBAL COMMANDS (GLOB_CMD)

Table 150. GLOB_CMD Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x03	0x02, 0x03	Not applicable	W	No

Table 151. GLOB_CMD Bit Definitions

Bits	Description
[15:8]	Not used
7	Software reset
6	Factory calibration restore
[5:4]	Not used
3	Flash memory update
2	Flash memory test (checksum)
1	Self test
0	Bias correction update

The GLOB_CMD register (see Table 150 and Table 151) provides trigger bits for several operations. Write a 1 to the appropriate bit in GLOB_CMD to start a particular function.

Software Reset

Turn to Page 3 (DIN = 0x8003) and then set GLOB_CMD[7] = 1 (DIN = 0x8280, DIN = 0x8300) to initiate a reset in the operation of the ADIS16489. This reset removes all data, initializes all registers from their flash settings, and restarts data sampling and processing. This function provides a firmware alternative to providing a low pulse on the $\overline{\text{RST}}$ pin (see Table 6, Pin 8).

Factory Calibration Restore

Turn to Page 3 (DIN = 0x8003) and then set GLOB_CMD[6] = 1 (DIN = 0x8240, DIN = 0x8300) to initiate restoration of the factory calibration. This restoration writes 0x0000 to the following registers: X_GYRO_SCALE, Y_GYRO_SCALE, Z_GYRO_SCALE, X_ACCL_SCALE, Y_ACCL_SCALE, Z_ACCL_SCALE, XG_BIAS_LOW, XG_BIAS_HIGH, YG_BIAS_LOW, YG_BIAS_HIGH, ZG_BIAS_LOW, ZG_BIAS_ HIGH, XA_BIAS_LOW, XA_BIAS_HIGH, YA_BIAS_LOW, YA_BIAS_HIGH, ZA_BIAS_LOW, and ZA_BIAS_HIGH.

Flash Memory Update

Turn to Page 3 (DIN = 0x8003) and then set GLOB_CMD[3] = 1 (DIN = 0x8208, DIN = 0x8300) to initiate a manual flash update. SYS_E_FLAG[6] (see Table 16) identifies success (0) or failure (1) in completing this process.

Flash Memory Test

Turn to Page 3 (DIN = 0x8003) and then set GLOB_CMD[2] = 1 (DIN = 0x8204, DIN = 0x8300) to initiate a checksum test on the flash memory bank. SYS_E_FLAG[6] = 0 (see Table 16) indicates a passing condition, which means that the most recent checksum value is the same as the checksum value, which came from the configuration of the units at the factory.

On Demand Self Test (ODST)

Turn to Page 3 (DIN = 0x8003) and then set GLOB_CMD[1] = 1 (DIN = 0x8202, then DIN = 0x8300) to run the ODST routine, which executes the following steps:

1. Measure the output on each sensor.
2. Activate an internal force on the mechanical elements of each sensor, which simulates the force associated with actual inertial motion.
3. Measure the output response on each sensor.
4. Deactivate the internal force on each sensor.
5. Calculate the difference between the force on and normal operating conditions (force off).
6. Compare the difference with internal pass/fail criteria.
7. Report the pass/fail results for each sensor in DIAG_STS (see Table 18) and the overall pass/fail flag in SYS_E_FLAG[5] (see Table 16).

When using an external clock, the self test execution times may vary from the 12 ms listed in Table 1. Also, false positive results are possible when the executing the ODST while the device is in motion.

Bias Correction Update

Turn to Page 3 (DIN = 0x8003) and set GLOB_CMD[0] = 1 (DIN = 0x8201, then DIN = 0x8300) to update the user offset registers with the correction factors of the continuous bias estimator (CBE). Ensure that the inertial platform is stable during the entire average time for optimal bias estimates.

AUXILIARY I/O LINE CONFIGURATION (FNCTIO_CTRL)

Table 152. FNCTIO_CTRL Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x03	0x06, 0x07	0x000D	R/W	Yes

Table 153. FNCTIO_CTRL Bit Definitions

Bits	Description
[15:12]	Not used
11	Alarm indicator: 1 = enabled, 0 = disabled
10	Alarm indicator polarity: 1 = positive, 0 = negative
[9:8]	Alarm indicator line selection: 00 = DIO1, 01 = DIO2, 10 = DIO3, 11 = DIO4
7	Sync clock input enable: 1 = enabled, 0 = disabled
6	Sync clock input polarity: 1 = rising edge, 0 = falling edge
[5:4]	Sync clock input line selection: 00 = DIO1, 01 = DIO2, 10 = DIO3, 11 = DIO4
3	Data ready enable: 1 = enabled, 0 = disabled
2	Data ready polarity: 1 = positive, 0 = negative
[1:0]	Data ready line selection: 00 = DIO1, 01 = DIO2, 10 = DIO3, 11 = DIO4

The FNCTIO_CTRL register (see Table 152 and Table 153) provides configuration control for each input/output pin (DIO1, DIO2, DIO3, and DIO4). Each DIOx pin supports only one function at a time. In cases where a single pin has two assignments, the enable bit for the lower priority function automatically resets to zero (disabling the lower priority function). The order of priority is as follows, from highest priority to lowest priority: data ready, sync clock input, alarm indicator, and general purpose. Changing the FNCTIO_CTRL[5:4] bit settings requires an execution time of 75 ms, whereas changing the settings of the remaining bits in the FNCTIO_CTRL register only takes 3 ms. During this execution time (75 ms or 3 ms), the operational state and the contents of the register remain unchanged, but the SPI interface supports normal communication (for accessing other registers).

Data Ready Indicator

The FNCTIO_CTRL[3:0] bits provide three configuration options for the data ready function: on/off, polarity, and DIOx line. The primary purpose this signal is to drive the interrupt control line of an embedded processor, which can help synchronize data collection and minimize latency. The factory default assigns DIO2 as a positive polarity data ready signal, which means that the data in the output registers is valid when the DIO2 line is high (see Figure 31). This configuration works well when DIO2 drives an interrupt service pin that activates on a low to high pulse.



Figure 31. Data Ready, When FNCTIO_CTRL[3:0] = 1101 (default)

Use the following sequence to change this assignment to DIO1 with a negative polarity:

1. Turn to Page 3 (DIN = 0x8003).
2. Set FNCTIO_CTRL[3:0] = 1000 (DIN = 0x8608, then DIN = 0x8700). The timing jitter on the pulse width of the data ready signal is typically ±1.4 µs.

Input Sync/Clock Control

FNCTIO_CTRL[7:4] provide configuration options for using one of the DIOx lines as an input synchronization signal for sampling inertial sensor data. For example, use the following sequence to establish DIO4 as a positive polarity input clock pin and keep the factory default setting for the data ready function:

1. Turn to Page 3 (DIN = 0x8003).
2. Set FNCTIO_CTRL[7:0] = 0xFD (DIN = 0x86FD).
3. Set FNCTIO_CTRL[15:8] = 0x00 (DIN = 0x8700).

This command also disables the internal sampling clock. Therefore, no data sampling occurs if no input clock signal is present. The best performance is available when using an input clock frequency of 2400 Hz.

Alarm Indicator

FNCTIO_CTRL[11:8] provide three configuration options for using one of the DIOx lines as an alarm indicator: on/off, polarity, and DIOx line. The primary purpose this signal is to provide an output signal that activates when a bit in the SYS_E_FLAG register = 1 (see Table 16). For example, use the following sequence to establish DIO3 as a negative polarity alarm indicator, while preserving the factory default setting for the data ready function:

1. Turn to Page 3 (DIN = 0x8003)
2. Set FNCTIO_CTRL[7:0] = 0x0D (DIN = 0x860D).
3. Set FNCTIO_CTRL[15:8] = 0x0A (DIN = 0x870A).

GENERAL-PURPOSE I/O CONTROL (GPIO_CTRL)

Table 154. GPIO_CTRL Register Definitions[1]

Page	Addresses	Default	Access	Flash Backup
0x03	0x08, 0x09	0x00X0	R/W	Yes

[1] The GPIO_CTRL[7:4] bits reflect the logic levels on the DIOx lines and do not have a default setting.

Table 155. GPIO_CTRL Bit Definitions[1]

Bits	Description
[15:8]	Don't care
7	General-Purpose I/O Line 4 (DIO4) data level
6	General-Purpose I/O Line 3 (DIO3) data level
5	General-Purpose I/O Line 2 (DIO2) data level
4	General-Purpose I/O Line 1 (DIO1) data level
3	General-Purpose I/O Line 4 (DIO4) direction control (1 = output, 0 = input)
2	General-Purpose I/O Line 3 (DIO3) direction control (1 = output, 0 = input)
1	General-Purpose I/O Line 2 (DIO2) direction control (1 = output, 0 = input)
0	General-Purpose I/O Line 1 (DIO1) direction control (1 = output, 0 = input)

[1] The GPIO_CTRL[7:4] bits reflect the logic levels on the DIOx lines and do not have a default setting.

When FNCTIO_CTRL does not configure a DIOx pin, GPIO_CTRL provides register controls for general-purpose use of the pin. GPIO_CTRL[3:0] provide input/output assignment controls for each line. When the DIOx lines are inputs, monitor their level by reading GPIO_CTRL[7:4]. When the DIOx lines are used as outputs, set their level by writing to GPIO_CTRL[7:4]. For example, use the following sequence to set DIO1 and DIO3 as high and low output lines, respectively, and set DIO2 and DIO4 as input lines. Turn to Page 3 (DIN = 0x8003) and set GPIO_CTRL[7:0] = 0x15 (DIN = 0x8815, then DIN = 0x8900).

MISCELLANEOUS CONFIGURATION (CONFIG)

Table 156. CONFIG Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x03	0x0A, 0x0B	0x00C0	R/W	Yes

Table 157. CONFIG Bit Definitions

Bits	Description
[15:8]	Not used
7	Linear *g* compensation for gyroscopes (1 = enabled)
6	Point of percussion alignment (1 = enabled)
[5:2]	Not used
1	Real-time clock, daylight savings time (1: enabled, 0: disabled)
0	Real-time clock control (1: relative/elapsed timer mode, 0: calendar mode)

The CONFIG register (see Table 156 and Table 157) provides configuration options for the linear *g* compensation in the gyroscopes (on/off), point of percussion alignment for the accelerometers (on/off), and the real-time clock function.

Point of Percussion

CONFIG[6] offers a point of percussion alignment function that maps the accelerometer sensors to the corner of the package identified in Figure 32. To activate this feature, turn to Page 3 (DIN = 0x8003), then set CONFIG[6] = 1 (DIN = 0x8A40, DIN = 0x8B00).

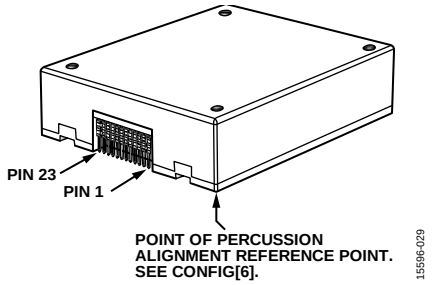


Figure 32. Point of Percussion Reference Point

Linear Acceleration on Effect on Gyroscope Bias

The ADIS16489 includes first-order compensation for the linear *g* effect in the gyroscopes, which uses the following model:

$$\begin{bmatrix} \omega_{XC} \\ \omega_{YC} \\ \omega_{ZC} \end{bmatrix} = \begin{bmatrix} LG_{11} & LG_{12} & LG_{13} \\ LG_{21} & LG_{22} & LG_{23} \\ LG_{31} & LG_{32} & LG_{33} \end{bmatrix} \times \begin{bmatrix} A_X \\ A_Y \\ A_Z \end{bmatrix} + \begin{bmatrix} \omega_{XPC} \\ \omega_{YPC} \\ \omega_{ZPC} \end{bmatrix}$$

The linear *g* correction factors, LG_{XY}, apply correction for linear acceleration in all three directions to the data path of each gyroscope (ω_{XPC}, ω_{YPC}, and ω_{ZPC}) at the rate of the data samples (2460 SPS when using the internal clock). CONFIG[7] provides an on/off control for this compensation. The factory default value for this bit activates this compensation. To turn it off, turn to Page 3 (DIN = 0x8003) and set CONFIG[7] = 0 (DIN = 0x8A40, DIN = 0x8B00). This command sequence also preserves the default setting for the point of percussion alignment function (on).

DECIMATION FILTER (DEC_RATE)

Table 158. DEC_RATE Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x03	0x0C, 0x0D	0x0000	R/W	Yes

Table 159. DEC_RATE Bit Definitions

Bits	Description
[15:11]	Don't care
[10:0]	Decimation rate, binary format, maximum = 2047, see Figure 33 for the impact on sample rate

The DEC_RATE register (see Table 158 and Table 159) provides user control for the final filter stage (see Figure 33), which averages and decimates the accelerometers and gyroscopes data, while also extending the time that the delta angle and delta velocity track between each update. The output sample rate is equal to 2460/(DEC_RATE + 1). When using the external clock option (Bit 7 and Bits[5:4] of the FNCTIO_CTRL register, see Figure 33), replace the 2460 number in this relationship with the input clock frequency. For example, turn to Page 3 (DIN = 0x8003), and set DEC_RATE = 0x18 (DIN = 0x8C18, then DIN = 0x8D00) to reduce the output sample rate to 98.4 SPS (2460 ÷ 25).

CONTINUOUS BIAS ESTIMATION (NULL_CNFG)

Table 160. NULL_CNFG Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x03	0x0E, 0x0F	0x070A	R/W	Yes

Table 161. NULL_CNFG Bit Definitions

Bits	Description
[15:14]	Not used.
13	Z-axis acceleration bias correction enable (1 = enabled).
12	Y-axis acceleration bias correction enable (1 = enabled).
11	X-axis acceleration bias correction enable (1 = enabled).
10	Z-axis gyroscope bias correction enable (1 = enabled).
9	Y-axis gyroscope bias correction enable (1 = enabled).
8	X-axis gyroscope bias correction enable (1 = enabled).
[7:4]	Not used.
[3:0]	Time base control (TBC), range is 0 to 13 (default = 10), time base (t_B) = $2^{TBC}/f_S$, where f_S is the IMU sample rate before decimation and is 2460 SPS if the factory default internal clock is used. The total average time (t_A) required for autonull = 64 × t_B.

The NULL_CNFG register (see Table 160 and Table 161) provides the configuration controls for the CBE, which associates with the bias correction update command in GLOB_CMD[0] (see Table 151). NULL_CNFG[3:0] establish the total average time (t_A) for the bias estimates and NULL_ CNFG[13:8] provide on/off controls for each sensor. The factory default configuration for NULL_CNFG enables the bias null command for the gyroscopes, disables the bias null command for the accelerometers, and sets the average time to ~26.64 sec. This calculation assumes that the internal sample clock (f_S = 2460 SPS) is used. If the user is supplying an external clock by setting Bit 7 of the FNCTIO_CRTL register to 1 (see Table 152 and Table 153), f_S is the IMU sample rate before decimation.

When a sensor bit in NULL_CNFG is active (equal to 1), setting GLOB_CMD[0] = 1 (DIN sequence: 0x8003, 0x8201, 0x8300) causes its bias correction register to automatically update with a value that corrects for its present bias error (from the CBE). For example, setting NULL_CNFG[8] equal to 1 causes an update in the XG_BIAS_LOW (see Table 109) and XG_BIAS_HIGH (see Table 111) registers.

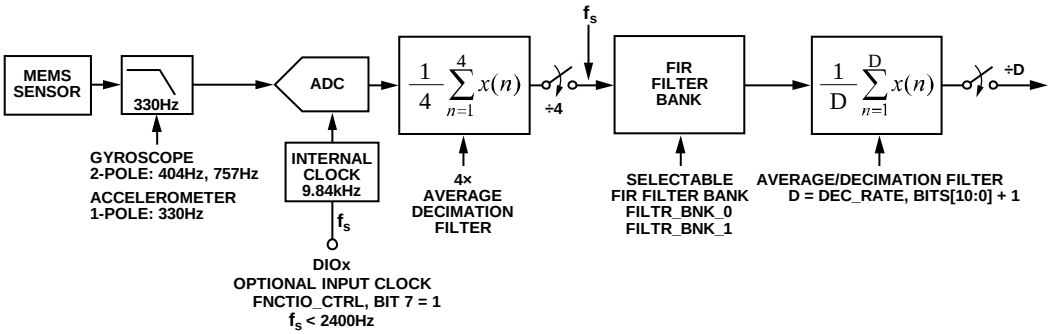


Figure 33. Sampling and Frequency Response Signal Flow

POWER MANAGEMENT (SLP_CNT)

Table 162. SLP_CNT Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x03	0x10, 0x11	Not applicable	W	No

Table 163. SLP_CNT Bit Definitions

Bits	Description
[15:10]	Not used
9	Power-down mode
8	Normal sleep mode
[7:0]	Programmable time bits; 1 sec/LSB; 0x00 = indefinite

The SLP_CNT register (see Table 162 and Table 163) provides controls for both power-down mode and sleep modes. The trade-off between power-down mode and sleep mode is idle power and recovery time. Power-down mode offers the best power consumption but requires the most time to recover. In addition, all volatile settings are lost during power-down, whereas sleep mode preserves these settings.

To initiate a sleep mode for a specific period of time, turn to Page 3 (DIN = 0x8003), write the amount of sleep time to SLP_CNT[7:0] and then set SLP_CNT[8] = 1 (DIN = 0x9101) to start the sleep period. Sleep mode begins when the $\overline{CS}$ line goes high, after setting SLP_CNT[8] = 1. See Table 164 for a command sequence example to place the ADIS16489 into sleep mode for 100 sec.

Table 164. Command Sequence, Timed Sleep Mode Example

DIN	Description
0x8003	Turn to Page 3
0x9064	SLP_CNT[7:0] = 0x64, 100 sec sleep time
0x9101	SLP_CNT[8] = 1, start sleep mode

To initiate an indefinite sleep mode, set SLP_CNT[7:0] = 0x00 (DIN = 0x9000), then set SLP_CNT[8] = 1 (DIN = 0x9101). To initiate a power-down period of 100 sec, use the configuration sequence in Table 164, with one exception: set SLP_CNT[9] = 1 (DIN = 0x9102) instead of setting SLP_CNT[8] = 1 (DIN = 0x9101). To initiate an indefinite power-down, set SLP_CNT[7:0] = 0x00 first, and then set SLP_CNT[9] = 1 (DIN = 0x9102).

To wake the device from sleep or power-down mode, use one of the following options to restore normal operation:

- Assert $\overline{CS}$ from high to low.
- Pulse $\overline{RST}$ low, then high again.
- Cycle the power.

If the sleep mode and power-down mode bits are both set high, the normal sleep mode bit (SLP_CNT[8]) takes precedence.

FIR FILTER CONTROL (FILTR_BNK_0, FILTR_BNK_1)

Table 165. FILTR_BNK_0 Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x03	0x16, 0x17	0x0000	R/W	Yes

Table 166. FILTR_BNK_0 Bit Definitions

Bits	Description
15	Don't care
14	Y-axis accelerometer filter enable (1 = enabled)
[13:12]	Y-axis accelerometer filter bank selection: 00 = Bank A, 01 = Bank B, 10 = Bank C, 11 = Bank D
11	X-axis accelerometer filter enable (1 = enabled)
[10:9]	X-axis accelerometer filter bank selection: 00 = Bank A, 01 = Bank B, 10 = Bank C, 11 = Bank D
8	Z-axis gyroscope filter enable (1 = enabled)
[7:6]	Z-axis gyroscope filter bank selection: 00 = Bank A, 01 = Bank B, 10 = Bank C, 11 = Bank D
5	Y-axis gyroscope filter enable (1 = enabled)
[4:3]	Y-axis gyroscope filter bank selection: 00 = Bank A, 01 = Bank B, 10 = Bank C, 11 = Bank D
2	X-axis gyroscope filter enable (1 = enabled)
[1:0]	X-axis gyroscope filter bank selection: 00 = Bank A, 01 = Bank B, 10 = Bank C, 11 = Bank D

Table 167. FILTR_BNK_1 Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x03	0x18, 0x19	0x0000	R/W	Yes

Table 168. FILTR_BNK_1 Bit Definitions

Bits	Description
[15:3]	Don't care
2	Z-axis accelerometer filter enable (1 = enabled)
[1:0]	Z-axis accelerometer filter bank selection: 00 = Bank A, 01 = Bank B, 10 = Bank C, 11 = Bank D

The FILTR_BNK_0 (see Table 165 and Table 166) and FILTR_BNK_1 (see Table 167 and Table 168) registers provide the configuration controls for the FIR filter bank in the signal chain of each sensor (see Figure 33). These registers provide on/off control for the FIR bank for each inertial sensor, along with the FIR bank (A, B, C, D) that each sensor uses.

ALARM CONFIGURATION (ALM_CNFG_0, ALM_CNFG_1, ALM_CFG_2)

The ALM_CNFG_0 (see Table 169 and Table 170), ALM_CNFG_1 (see Table 171 and Table 172) and ALM_CNFG_2 (see Table 173 and Table 174) registers provide three configuration control options for the alarm functions of each inertial sensor and the barometer: on/off, polarity, and mode of operation (static/dynamic).

Table 169. ALM_CNFG_0 Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x03	0x20, 0x21	0x0000	R/W	Yes

Solving for ΔX_ACCL_OUT, ΔZ_GYRO_OUT, ΔY_GYRO_OUT, and ΔX_GYRO_OUT

Use Equation 1 to Equation 4 to solve for ΔX_ACCL_OUT, ΔZ_GYRO_OUT, ΔY_GYRO_OUT, and ΔX_GYRO_OUT, which the following bits provide user control for in the ALM_CFG_0 register (see Table 170) in Bits[13:12], Bits[9:8], Bits[5:4], and Bits[1:0].

$$\Delta X_ACCL_OUT = \frac{1}{8}\left(\sum_{n=0}^{7} X_A(n) - \sum_{n=0}^{7} X_A(n-112)\right) \quad (1)$$

where $X_A = X_ACCL_OUT$.

$$\Delta Z_GYRO_OUT = \frac{1}{8}\left(\sum_{n=0}^{7} Z_G(n) - \sum_{n=0}^{7} Z_G(n-112)\right) \quad (2)$$

where $Z_G = Z_GYRO_OUT$.

$$\Delta Y_GYRO_OUT = \frac{1}{8}\left(\sum_{n=0}^{7} Y_G(n) - \sum_{n=0}^{7} Y_G(n-112)\right) \quad (3)$$

where $Y_G = Y_GYRO_OUT$.

$$\Delta X_GYRO_OUT = \frac{1}{8}\left(\sum_{n=0}^{7} X_G(n) - \sum_{n=0}^{7} X_G(n-112)\right) \quad (4)$$

where $X_G = X_GYRO_OUT$.

Table 170. ALM_CNFG_0 Bit Definitions

Bits	Description
15	X-axis accelerometer; 0: alarm is off, 1: alarm is on
14	Not used
[13:12]	X-axis accelerometer polarity and mode settings; select one of the four options for the condition that triggers the alarm (ALM_STS[3] = 1, see Table 20) 00: X_ACCL_OUT < XA_ALM_MAGN 01: ΔX_ACCL_OUT < XA_ALM_MAGN (see Equation 1) 10: X_ACCL_OUT > XA_ALM_MAGN 11: ΔX_ACCL_OUT > XA_ALM_MAGN (see Equation 1)
11	Z-axis gyroscope; 0: alarm is off, 1: alarm is on
10	Not used
[9:8]	Z-axis gyroscope polarity and mode settings; select one of the four options for the condition that triggers the alarm (ALM_STS[2] = 1, see Table 20) 00: Z_GYRO_OUT < ZG_ALM_MAGN 01: ΔZ_GYRO_OUT < ZG_ALM_MAGN (see Equation 2) 10: Z_GYRO_OUT > ZG_ALM_MAGN 11: ΔZ_GYRO_OUT > ZG_ALM_MAGN (see Equation 2)
7	Y-axis gyroscope; 0: alarm is off, 1: alarm is on
6	Not used
[5:4]	Y-axis gyroscope polarity and mode settings. Select one of the four options for the condition that triggers the alarm (ALM_STS[1] = 1, see Table 20) 00: Y_GYRO_OUT < YG_ALM_MAGN 01: ΔY_GYRO_OUT < YG_ALM_MAGN (see Equation 3) 10: Y_GYRO_OUT > YG_ALM_MAGN 11: ΔY_GYRO_OUT > YG_ALM_MAGN (see Equation 3)
3	X-axis gyroscope; 0: alarm is off, 1: alarm is on
2	Not used
1:0	X-axis gyroscope polarity and mode settings; select one of the four options for the condition that triggers the alarm (ALM_STS[0] = 1, see Table 20) 00: X_GYRO_OUT < XG_ALM_MAGN 01: ΔX_GYRO_OUT < XG_ALM_MAGN (see Equation 4) 10: X_GYRO_OUT > XG_ALM_MAGN 11: ΔX_GYRO_OUT > XG_ALM_MAGN (see Equation 4)

Table 171. ALM_CNFG_1 Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x03	0x22, 0x23	0x0000	R/W	Yes

Solving for ΔZ_ACCL_OUT and ΔY_ACCL_OUT

Use Equation 5 and Equation 6 to solve for ΔZ_ACCL_OUT and ΔY_ACCL_OUT in Bits[5:4] and Bits[1:0] in Table 172.

$$\Delta Z_ACCL_OUT = \frac{1}{8}\left(\sum_{n=0}^{7} Z_A(n) - \sum_{n=0}^{7} Z_A(n-112)\right) \quad (5)$$

where $Z_A = Z_ACCL_OUT$.

$$\Delta Y_ACCL_OUT = \frac{1}{8}\left(\sum_{n=0}^{7} Y_A(n) - \sum_{n=0}^{7} Y_A(n-112)\right) \quad (6)$$

where $Y_A = Y_ACCL_OUT$.

Table 172. ALM_CNFG_1 Bit Definitions

Bits	Description
[15:8]	Not used
7	Z-axis accelerometer; 0: alarm is off, 1: alarm is on
6	Not used
[5:4]	Z-axis accelerometer polarity and mode settings; select one of the four options for the condition that triggers the alarm (ALM_STS[5] = 1, see Table 20) 00: Z_ACCL_OUT < ZA_ALM_MAGN 01: ΔZ_ACCL_OUT < ZA_ALM_MAGN (see Equation 5) 10: Z_ACCL_OUT > ZA_ALM_MAGN 11: ΔZ_ACCL_OUT > ZA_ALM_MAGN (see Equation 5)
4	Z-axis accelerometer mode, 0: static, 1: dynamic
3	Y-axis accelerometer; 0: alarm is off, 1: alarm is on
2	Not used
[1:0]	Y-axis accelerometer polarity and mode settings; select one of the four options for the condition that triggers the alarm (ALM_STS[4] = 1, see Table 20) 00: Y_ACCL_OUT < YA_ALM_MAGN 01: ΔY_ACCL_OUT < YA_ALM_MAGN (see Equation 6) 10: Y_ACCL_OUT > YA_ALM_MAGN 11: ΔY_ACCL_OUT > YA_ALM_MAGN (see Equation 6)

Table 173. ALM_CNFG_2 Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x03	0x24, 0x25	0x0000	R/W	Yes

Table 174. ALM_CNFG_2

Bits	Description
[15:8]	Not used
7	Barometer alarm (1 = enabled)
6	Not used
5	Barometer alarm polarity (1 = greater than)
4	Barometer dynamic enable (1 = enabled)
[3:0]	Not used

X-AXIS GYROSCOPE ALARM (XG_ALM_MAGN)

Table 175. XG_ALM_MAGN Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x03	0x28, 0x29	0x0000	R/W	Yes

Table 176. XG_ALM_MAGN Bit Definitions

Bits	Description
[15:0]	X-axis gyroscope alarm threshold settings, twos complement, 0°/sec = 0x0000, 1 LSB = 0.02°/sec

The XG_ALM_MAGN register (see Table 175 and Table 176) contains the alarm threshold for the x-axis gyroscope, when ALM_CNFG_0[3] = 1 (see Table 170). This alarm is associated with the alarm flag in ALM_STS[0] (see Table 20).

Alarm Example

Table 177 provides a list of commands that configure the x-axis gyroscopes alarm to be active (ALM_STS[0] = 1) when the rate of rotation around the x-axis exceeds 100°/sec. The value for the XG_ALM_MAGN register is 0x1388, as follows:

100°/sec ÷ 0.02°/sec/LSB = 5000 LSB = 0x1388

Table 177. Configuration Commands, Alarm Example

DIN	Description
0x8003	Turn to page 3
0xA888	XG_ALM_MAGN[7:0] = 0x88
0xA913	XG_ALM_MAGN[15:8] = 0x13
0xA00C	ALM_CNFG_1[7:0] = 0x0C
0xA100	ALM_CNFG_1[15:8] = 0x00

Y-AXIS GYROSCOPE ALARM (YG_ALM_MAGN)

Table 178. YG_ALM_MAGN Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x03	0x2A, 0x2B	0x0000	R/W	Yes

Table 179. YG_ALM_MAGN Bit Definitions

Bits	Description
[15:0]	Y-axis gyroscope alarm threshold settings, twos complement, 0°/sec = 0x0000, 1 LSB = 0.02°/sec

The YG_ALM_MAGN register (see Table 178 and Table 179) contains the alarm threshold for the y-axis gyroscope, when ALM_CNFG_0[7] = 1 (see Table 170). This alarm is associated with the alarm flag in ALM_STS[1] (see Table 20).

Z-AXIS GYROSCOPE ALARM (ZG_ALM_MAGN)

Table 180. ZG_ALM_MAGN Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x03	0x2C, 0x2D	0x0000	R/W	Yes

Table 181. ZG_ALM_MAGN Bit Definitions

Bits	Description
[15:0]	Z-axis gyroscope alarm threshold settings, twos complement, 0°/sec = 0x0000, 1 LSB = 0.02°/sec

The ZG_ALM_MAGN register (see Table 180 and Table 181) contains the alarm threshold for the z-axis gyroscope, when ALM_CNFG_0[11] = 1 (see Table 170). This alarm is associated with the alarm flag in ALM_STS[2] (see Table 20).

X-AXIS ACCELEROMETER ALARM (XA_ALM_MAGN)

Table 182. XA_ALM_MAGN Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x03	0x2E, 0x2F	0x0000	R/W	Yes

Table 183. XA_ALM_MAGN Bit Definitions

Bits	Description
[15:0]	X-axis accelerometer alarm threshold settings, twos complement, 0 *g* = 0x0000, 1 LSB = 0.25 m*g*

The XA_ALM_MAGN register (see Table 182 and Table 183) contains the alarm threshold for the x-axis accelerometer, when ALM_CNFG_0[15] = 1 (see Table 170). This alarm is associated with the alarm flag in ALM_STS[3] (see Table 20).

Y-AXIS ACCELEROMETER ALARM (YA_ALM_MAGN)

Table 184. YA_ALM_MAGN Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x03	0x30, 0x31	0x0000	R/W	Yes

Table 185. YA_ALM_MAGN Bit Definitions

Bits	Description
[15:0]	Y-axis accelerometer alarm threshold settings, twos complement, 0 *g* = 0x0000, 1 LSB = 0.25 m*g*

The YA_ALM_MAGN register (see Table 184 and Table 185) contains the alarm threshold for the y-axis accelerometer, when ALM_CNFG_1[3] = 1 (see Table 172). This alarm is associated with the alarm flag in ALM_STS[4] (see Table 20).

Z-AXIS ACCELEROMETER ALARM (ZA_ALM_MAGN)

Table 186. ZA_ALM_MAGN Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x03	0x32, 0x33	0x0000	R/W	Yes

Table 187. ZA_ALM_MAGN Bit Definitions

Bits	Description
[15:0]	Z-axis accelerometer alarm threshold settings, twos complement, 0 *g* = 0x0000, 1 LSB = 0.25 m*g*

The ZA_ALM_MAGN register (see Table 186 and Table 187) contains the alarm threshold for the z-axis accelerometer, when ALM_ CNFG_1[7] = 1 (see Table 172). This alarm is associated with the alarm flag in ALM_STS[5] (see Table 20).

BAROMETER ALARM (BR_ALM_MAGN)

Table 188. BR_ALM_MAGN Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x03	0x3A, 0x3B	0x0000	R/W	Yes

Table 189. BR_ALM_MAGN Bit Definitions

Bits	Description
[15:0]	Barometer alarm threshold settings, twos complement, 0 *g* = 0x0000, 1 LSB = 40 µbar

The BR_ALM_MAGN register (see Table 188 and Table 189) contains the alarm threshold for barometer, when ALM_ CNFG_2[7] = 1 (see Table 174). This alarm is associated with the alarm flag in ALM_STS[11] (see Table 20).

FIRMWARE REVISION (FIRM_REV)

Table 190. FIRM_REV Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x03	0x78, 0x79	Not applicable	R	Yes

Table 191. FIRM_REV Bit Definitions

Bits	Description
[15:12]	Firmware revision binary coded decimal (BCD) code, tens digit, numerical format = 4-bit binary, range = 0 to 9
[11:8]	Firmware revision BCD code, ones digit, numerical format = 4-bit binary, range = 0 to 9
[7:4]	Firmware revision BCD code, tenths digit, numerical format = 4-bit binary, range = 0 to 9
[3:0]	Firmware revision BCD code, hundredths digit, numerical format = 4-bit binary, range = 0 to 9

The FIRM_REV register (see Table 190 and Table 191) provides the firmware revision for the internal firmware. This register uses a BCD format, where each nibble represents a digit. For example, if FIRM_REV = 0x1234, the firmware revision is 12.34.

FIRMWARE REVISION DAY AND MONTH (FIRM_DM)

Table 192. FIRM_DM Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x03	0x7A, 0x7B	Not applicable	R	Yes

Table 193. FIRM_DM Bit Definitions

Bits	Description
[15:12]	Factory configuration month BCD code, tens digit, numerical format = 4-bit binary, range = 0 to 2
[11:8]	Factory configuration month BCD code, ones digit, numerical format = 4-bit binary, range = 0 to 9
[7:4]	Factory configuration day BCD code, tens digit, numerical format = 4-bit binary, range = 0 to 3
[3:0]	Factory configuration day BCD code, ones digit, numerical format = 4-bit binary, range = 0 to 9

The FIRM_DM register (see Table 192 and Table 193) contains the month and day of the factory configuration date. FIRM_ DM[15:12] and FIRM_DM[11:8] contain digits that represent the month of the factory configuration in a BCD format. For example, November is the 11th month in a year and is represented by FIRM_DM[15:8] = 0x11. FIRM_DM[7:4] and FIRM_DM[3:0] contain digits that represent the day of factory configuration in a BCD format. For example, the 27th day of the month is represented by FIRM_DM[7:0] = 0x27.

FIRMWARE REVISION YEAR (FIRM_Y)

Table 194. FIRM_Y Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x03	0x7C, 0x7D	Not applicable	R	Yes

Table 195. FIRM_Y Bit Definitions

Bits	Description
[15:12]	Factory configuration year BCD code, thousands digit, numerical format = 4-bit binary, range = 0 to 9
[11:8]	Factory configuration year BCD code, hundreds digit, numerical format = 4-bit binary, range = 0 to 9
[7:4]	Factory configuration year BCD code, tens digit, numerical format = 4-bit binary, range = 0 to 3
[3:0]	Factory configuration year BCD code, ones digit, numerical format = 4-bit binary, range = 0 to 9

The FIRM_Y register (see Table 194 and Table 195) contains the year of the factory configuration date. For example, the year, 2013, is represented by FIRM_Y = 0x2013.

PAGE 4 (PAGE_ID)

Table 196. PAGE_ID Register Definition

Page	Addresses	Default	Access	Flash Backup
0x04	0x00, 0x01	0x0000	R/W	No

Table 197. PAGE_ID Bit Assignments

Bits	Description
[15:0]	Page number, binary numerical format

The contents in the PAGE_ID register (see Table 196 and Table 197) contain the current page setting, and provide a control for selecting another page for SPI access. For example, set DIN = 0x8002 to select Page 2 for SPI-based user access. See Table 10 for the page assignments associated with each user accessible register.

PART IDENTIFICATION NUMBERS (PART_ID1, PART_ID2, PART_ID3, PART_ID4)

Table 198. PART_ID1 Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x04	0x20, 0x21	Not applicable	R	Not applicable

Table 199. PART_ID1 Bit Definitions

Bits	Description
[15:0]	Part Identification 1

Table 200. PART_ID2 Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x04	0x22, 0x23	Not applicable	R	Not applicable

Table 201. PART_ID2 Bit Definitions

Bits	Description
[15:0]	Part Identification 2

Table 202. PART_ID3 Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x04	0x24, 0x25	Not applicable	R	Not applicable

Table 203. PART_ID3 Bit Definitions

Bits	Description
[15:0]	Part Identification 3

Table 204. PART_ID4 Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x04	0x26, 0x27	Not applicable	R	Not applicable

Table 205. PART_ID4 Bit Definitions

Bits	Description
[15:0]	Part Identification 4

FIR FILTERS

The ADIS16489 has four user configurable FIR filter banks. The sample rate of the FIR filters is identical to the inertial measurement unit (IMU) sample rate. Because decimation occurs after the FIR filters, the FIR sample rate is independent of the decimation rate and is not affected by the setting of the DEC_RATE register. If the user selects the internally generated sample clock (which is the default setting), the nominal IMU sample rate (and FIR sample rate) is 2460 SPS. If the user is supplying an external clock by setting Bit 7 of the FNCTIO_CRTL register to 1 (see Table 152 and Table 153), the FIR sample rate is the same as the ADIS16489 sample rate.

The user can individually configure and select one of the four FIR filter banks for each individual inertial sensor using the FILTR_ BNK_0 (see Table 166) and FILTR_BNK_1 (see Table 168) registers (see Figure 33). Each FIR filter bank (A, B, C, D) has 120 taps that consume two pages of memory. The coefficient associated with each tap in each filter bank has its own dedicated register that uses a 16-bit, twos complement format. The FIR filter has unity-gain when the sum of all of the coefficients is equal to 32,768. For filter designs that require fewer than 120 taps, ensure that the non-zero taps are in the lower-numbered coefficients and write 0x0000 to all unused taps to eliminate the latency associated with that particular tap.

Page 5, Page 6 (PAGE_ID)

Table 206. PAGE_ID Register Definition

Page	Addresses	Default	Access	Flash Backup
0x05. 0x06,	0x00, 0x01	0x0000	R/W	No

Table 207. PAGE_ID Bit Assignments

Bits	Description
[15:0]	Page number, binary numerical format

The contents in the PAGE_ID register (see Table 206 and Table 207) contain the current page setting, and provide a control for selecting another page for SPI access. For example, set DIN = 0x8002 to select Page 2 for SPI-based user access. See Table 10 for the page assignments associated with each user accessible register.

FIR Filter Bank A (FIR_COEF_A000 to FIR_COEF_A119)

Table 208. FIR Filter Bank A Memory Map

Page	PAGE_ID	Addresses	Register
5	0x05	0x00, 0x01	PAGE_ID
5	0x05	0x02 to 0x07	Not used
5	0x05	0x08, 0x09	FIR_COEF_A000
5	0x05	0x0A, 0x0B	FIR_COEF_A001
5	0x05	0x0C to 0x7D	FIR_COEF_A002 to FIR_COEF_A058
5	0x05	0x7E, 0x7F	FIR_COEF_A059
6	0x06	0x00, 0x01	PAGE_ID
6	0x06	0x02 to 0x07	Not used
6	0x06	0x08, 0x09	FIR_COEF_A060
6	0x06	0x0A, 0x0B	FIR_COEF_A061
6	0x06	0x0C to 0x7D	FIR_COEF_A062 to FIR_COEF_A118
6	0x06	0x7E, 0x7F	FIR_COEF_A119

Table 209 and Table 210 offer detailed register and bit definitions for one of the FIR coefficient registers in Bank A, FIR_COEF_A071. Table 211 provides a configuration example, which sets this register to a decimal value of −169 (0xFF57).

Table 209. FIR_COEF_A071 Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x06	0x1E, 0x1F	Not applicable	R/W	Yes

Table 210. FIR_COEF_A071 Bit Definitions

Bits	Description
[15:0]	FIR Bank A, Coefficient 71, twos complement

Table 211. Configuration Example, FIR Coefficient

DIN	Description
0x8006	Turn to Page 6
0x9E57	FIR_COEF_A071[7:0] = 0x57
0x9FFF	FIR_COEF_A071[15:8] = 0xFF

Page 7, Page 8 (PAGE_ID)

Table 212. PAGE_ID Register Definition

Page	Addresses	Default	Access	Flash Backup
0x07. 0x08,	0x00, 0x01	0x0000	R/W	No

Table 213. PAGE_ID Bit Assignments

Bits	Description
[15:0]	Page number, binary numerical format

The contents in the PAGE_ID register (see Table 212 and Table 213) contain the current page setting, and provide a control for selecting another page for SPI access. For example, set DIN = 0x8002 to select Page 2 for SPI-based user access. See Table 10 for the page assignments associated with each user accessible register.

FIR Filter Bank B (FIR_COEF_B000 to FIR_COEF_B119)

Table 214. Filter Bank B Memory Map

Page	PAGE_ID	Addresses	Register
7	0x07	0x00, 0x01	PAGE_ID
7	0x07	0x02 to 0x07	Not used
7	0x07	0x08, 0x09	FIR_COEF_B000
7	0x07	0x0A, 0x0B	FIR_COEF_B001
7	0x07	0x0C to 0x7D	FIR_COEF_B002 to FIR_COEF_B058
7	0x07	0x7E, 0x7F	FIR_COEF_B059
8	0x08	0x00, 0x01	PAGE_ID
8	0x08	0x02 to 0x07	Not used
8	0x08	0x08, 0x09	FIR_COEF_B060
8	0x08	0x0A, 0x0B	FIR_COEF_B061
8	0x08	0x0C to 0x7D	FIR_COEF_B062 to FIR_COEF_B118
8	0x08	0x7E, 0x7F	FIR_COEF_B119

Page 9, Page 10 (PAGE_ID)

Table 215. PAGE_ID Register Definition

Page	Addresses	Default	Access	Flash Backup
0x09. 0x0A,	0x00, 0x01	0x0000	R/W	No

Table 216. PAGE_ID Bit Assignments

Bits	Description
[15:0]	Page number, binary numerical format

The contents in the PAGE_ID register (see Table 215 and Table 216) contain the current page setting, and provide a control for selecting another page for SPI access. For example, set DIN = 0x8002 to select Page 2 for SPI-based user access. See Table 10 for the page assignments associated with each user accessible register.

FIR Filter Bank C (FIR_COEF_C000 to FIR_COEF_C119)

Table 217. Filter Bank C Memory Map

Page	PAGE_ID	Addresses	Register
9	0x09	0x00, 0x01	PAGE_ID
9	0x09	0x02 to 0x07	Not used
9	0x09	0x08, 0x09	FIR_COEF_C000
9	0x09	0x0A, 0x0B	FIR_COEF_C001
9	0x09	0x0C to 0x7D	FIR_COEF_C002 to FIR_COEF_C058
9	0x09	0x7E, 0x7F	FIR_COEF_C059
10	0x0A	0x00, 0x01	PAGE_ID
10	0x0A	0x02 to 0x07	Not used
10	0x0A	0x08, 0x09	FIR_COEF_C060
10	0x0A	0x0A, 0x0B	FIR_COEF_C061
10	0x0A	0x0C to 0x7D	FIR_COEF_C062 to FIR_COEF_C118
10	0x0A	0x7E, 0x7F	FIR_COEF_C119

Page 11, Page 12 (PAGE_ID)

Table 218. PAGE_ID Register Definition

Page	Addresses	Default	Access	Flash Backup
0x0B, 0x0C,	0x00, 0x01	0x0000	R/W	No

Table 219. PAGE_ID Bit Assignments

Bits	Description
[15:0]	Page number, binary numerical format

The contents in the PAGE_ID register (see Table 218 and Table 219) contain the current page setting, and provide a control for selecting another page for SPI access. For example, set DIN = 0x8002 to select Page 2 for SPI-based user access. See Table 10 for the page assignments associated with each user accessible register.

FIR Filter Bank D (FIR_COEF_D000 to FIR_COEF_D119)

Table 220. Filter Bank D Memory Map

Page	PAGE_ID	Addresses	Register
11	0x0B	0x00, 0x01	PAGE_ID
11	0x0B	0x02 to 0x07	Not used
11	0x0B	0x08, 0x09	FIR_COEF_D000
11	0x0B	0x0A, 0x0B	FIR_COEF_D001
11	0x0B	0x0C to 0x7D	FIR_COEF_D002 to FIR_COEF_D058
11	0x0B	0x7E, 0x7F	FIR_COEF_D059
12	0x0C	0x00, 0x01	PAGE_ID
12	0x0C	0x02 to 0x07	Not used
12	0x0C	0x08, 0x09	FIR_COEF_D060
12	0x0C	0x0A, 0x0B	FIR_COEF_D061
12	0x0C	0x0C to 0x7D	FIR_COEF_D062 to FIR_COEF_D118
12	0x0C	0x7E, 0x7F	FIR_COEF_D119

Default Filter Performance

The FIR filter banks have factory programmed filter designs. They are all low-pass filters that have unity dc gain. Table 221 provides a summary of each filter design, and Figure 34 shows the frequency response characteristics. The phase delay is equal to ½ of the total number of taps.

Table 221. FIR Filter Descriptions, Default Configuration

FIR Filter Bank	Taps	−3 dB Frequency (Hz)
A	120	310
B	120	55
C	32	275
D	32	63

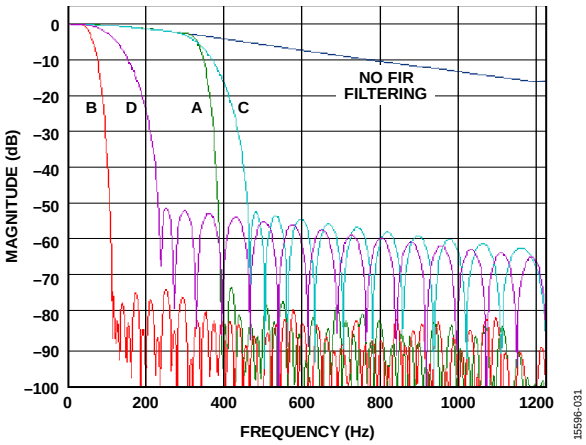


Figure 34. FIR Filter Frequency Response Curves

APPLICATIONS INFORMATION

MOUNTING BEST PRACTICES

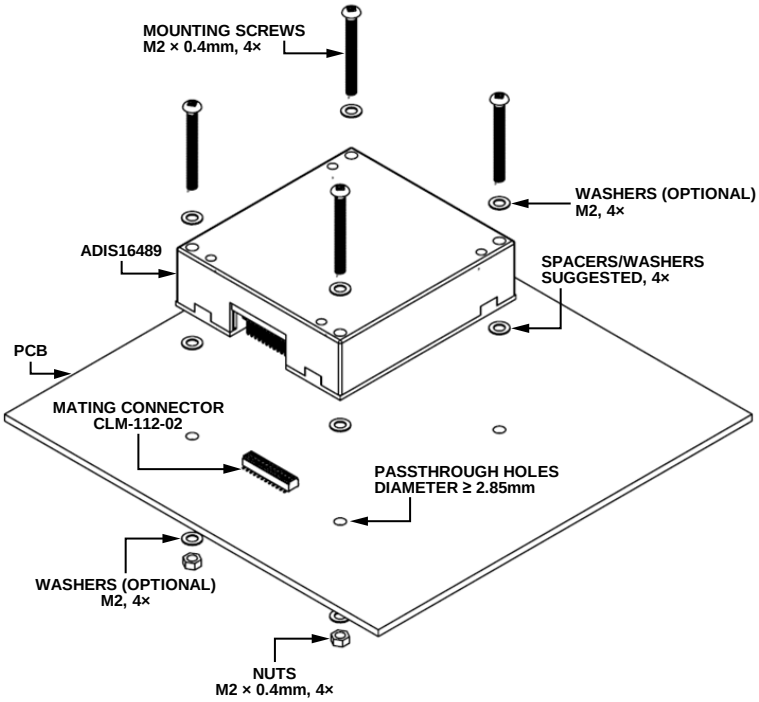


Figure 35. Mounting Example

For best performance, follow these simple rules when installing the ADIS16489 into a system:

- Eliminate opportunity for translational force (x- and y-axis direction, per Figure 20) application on the electrical connector.
- Isolate the mounting force to the four corners on the portion of the package surface that surrounds the mounting holes.
- Use uniform mounting forces on all four corners. The suggested torque setting is 40 inch ounces (0.285 Nm).

These three rules help prevent irregular force profiles, which can warp the package and introduce bias errors in the sensors. Figure 35 provides an example that leverages washers to set the package off the mounting surface and uses 2.85 mm passthrough holes and backside washers/nuts for attachment. Figure 36 and Figure 37 provide details for mounting hole and connector alignment pin drill locations.

For more information on mounting the ADIS16489, see the AN-1295 Application Note.

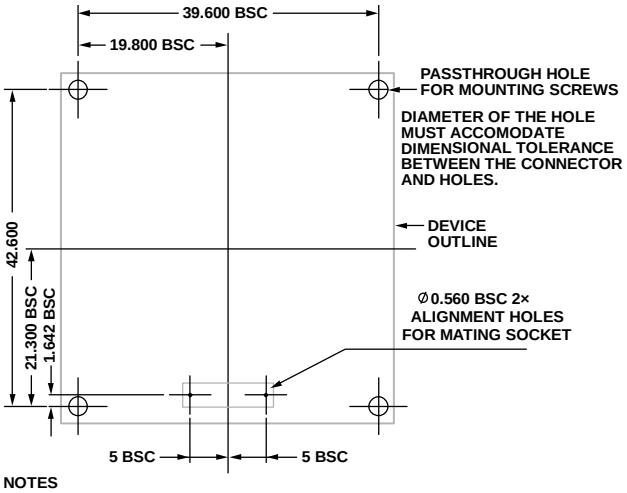


Figure 36. Suggested PCB Layout Pattern, Connector Down

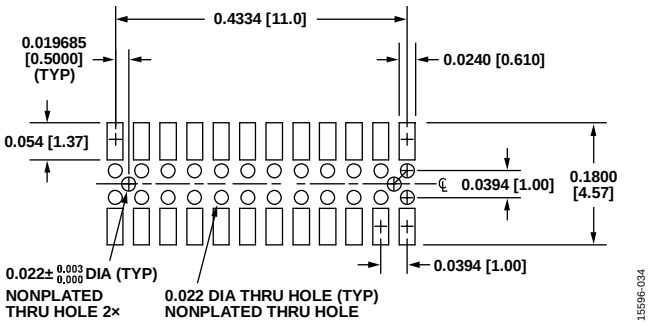


Figure 37. Suggested Layout and Mechanical Design When Using Samtec CLM-112-02-G-D-A for the Mating Connector

EVALUATION TOOLS

Breakout Board, ADIS16IMU1/PCBZ

The ADIS16IMU1/PCBZ (sold separately) provides a breakout board function for the ADIS16489, which means that it provides access to the ADIS16489 through larger connectors that support standard 1 mm ribbon cabling. It also provides four mounting holes for attachment of the ADIS16489 to the breakout board.

PC-Based Evaluation, EVAL-ADIS2

The EVAL-ADIS2 provides the system support PC-based evaluation of the ADIS16489.

POWER SUPPLY CONSIDERATIONS

The VDD power supply must charge 24 µF of capacitance (inside of the ADIS16489, across the VDD and GND pins) during its initial ramp and settling process. When VDD reaches 2.85 V, the ADIS16489 begins its internal start-up process, which generates additional transient current demand. See Figure 38 for a typical current profile during the start-up process. The first peak in Figure 38 relates to charging the 24 µF capacitor bank, whereas the second peak (~360 ms after the first peak) relates to the initialization process of the ADIS16489. See Figure 39 for a close view of the current profile associated with the second peak in Figure 38.

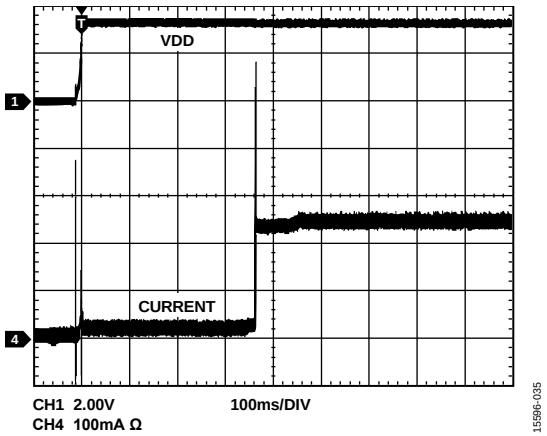


Figure 38. Transient Current Demand, Startup

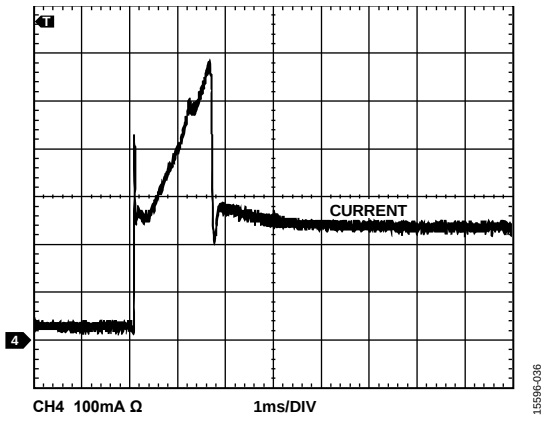


Figure 39. Transient Current Demand, Peak Demand

X-RAY SENSITIVITY

Exposure to high dose rate X-rays, such as those in production systems that inspect solder joints in electronic assemblies, can affect accelerometer bias errors. For optimal performance, avoid exposing the ADIS16489A to this type of inspection.

PACKAGING AND ORDERING INFORMATION

OUTLINE DIMENSIONS

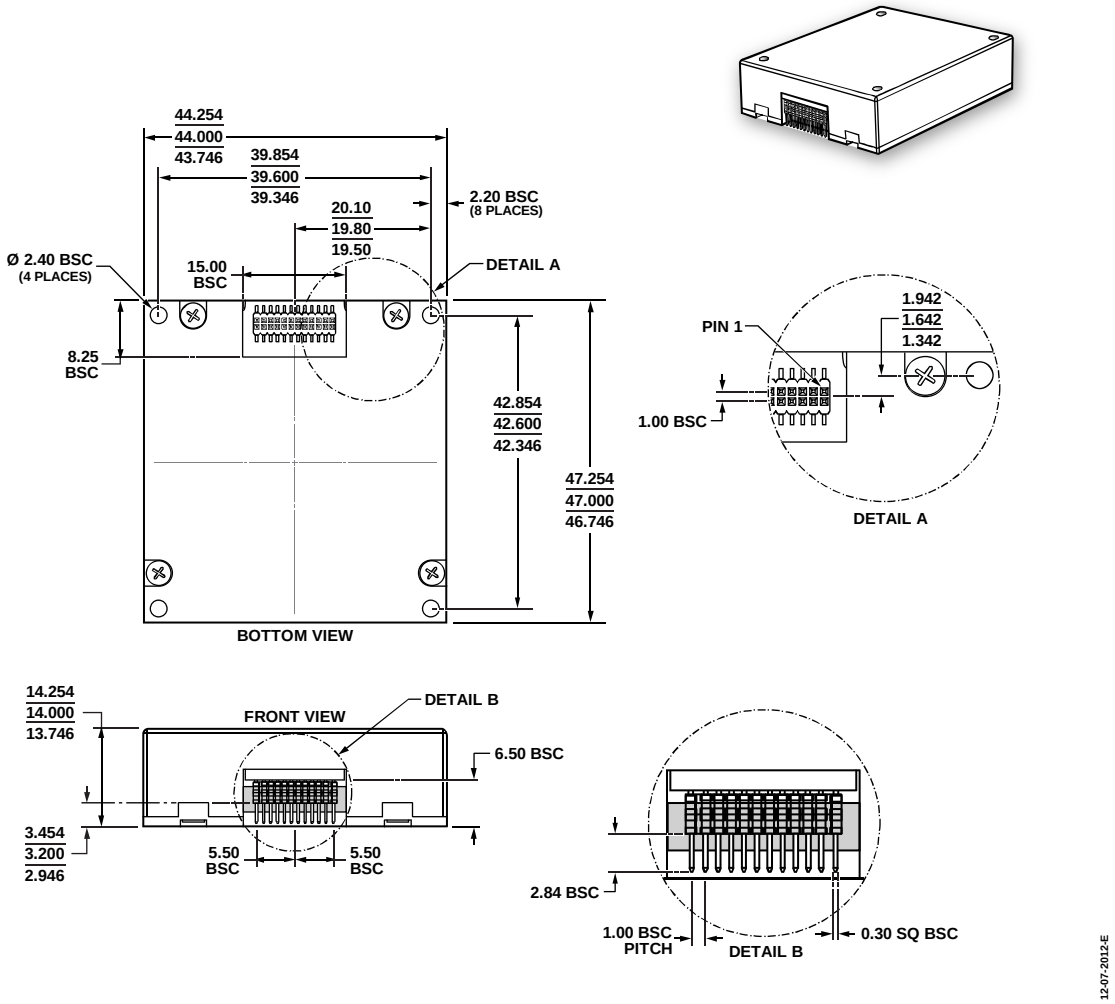


Figure 40. 24-Lead Module with Connector Interface [MODULE]
(ML-24-6)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADIS16489BMLZ-P	−40°C to +105°C	24-Lead Module with Connector Interface [MODULE]	ML-24-6

[1] Z = RoHS Compliant Part.

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D15596-8/20(B)