**NOT RECOMMENDED FOR NEW DESIGNS**
**RECOMMENDED REPLACEMENT PART**
**ISL80101-ADJ**

# ISL80101

High Performance 1A LDO

FN6931
Rev 3.00
September 6, 2016

The ISL80101 is a low voltage, high current, single output LDO specified at 1A output current. This LDO operates from input voltages of 2.2V to 6V. Fixed output voltage options are available in 1.8V, 2.5V, 3.3V and 5.0V versions. Other custom voltage options are available upon request. For the adjustable output version of the ISL80101, please refer to the ISL80101-ADJ datasheet.

A submicron BiCMOS process is utilized for this product family to deliver the best-in-class analog performance and overall value. This CMOS LDO consumes significantly lower quiescent current as a function of load compared to bipolar LDOs, which translates into higher efficiency and packages with smaller footprints. State-of-the-art internal compensation achieves a very fast load transient response. An external capacitor on the soft-start pin provides an adjustable soft-starting ramp. The ENABLE feature allows the part to be placed into a low quiescent current shutdown mode. A power-good logic output signals a fault condition.

Table 1 shows the differences between the ISL80101 and others in its family:

**TABLE 1. KEY DIFFERENCES BETWEEN FAMILY OF PARTS**

| PART NUMBER | PROGRAMMABLE $I_{LIMIT}$ | $I_{LIMIT}$ (DEFAULT) | ADJ or FIXED $V_{OUT}$ |
|---|---|---|---|
| ISL80101-ADJ | No | 1.75A | ADJ |
| ISL80101 | No | 1.75A | 1.8V, 2.5V, 3.3V, 5.0V |
| ISL80101A | Yes | 1.62A | ADJ |
| ISL80121-5 | Yes | 0.75A | 5.0V |

## Features

- ±1.8% $V_{OUT}$ accuracy guaranteed over line, load and $T_J$ = -40°C to +125°C
- Very low 130mV dropout voltage at $V_{OUT}$ = 2.5V
- Very fast transient response
- Programmable soft-starting
- Power-good output
- Excellent 65dB PSRR
- Current limit protection
- Thermal shutdown function
- Available in a 10 Ld DFN package
- Pb-free (RoHS compliant)

## Applications

- DSP, FPGA and µP core power supplies
- Noise-sensitive instrumentation systems
- Post regulation of switched mode power supplies
- Industrial systems
- Medical equipment
- Telecommunications and networking equipment
- Servers
- Hard disk drives (HD/HDD)

## Related Literature

- See AN1592, "ISL80101 High Performance 1A LDO Evaluation Board User Guide"

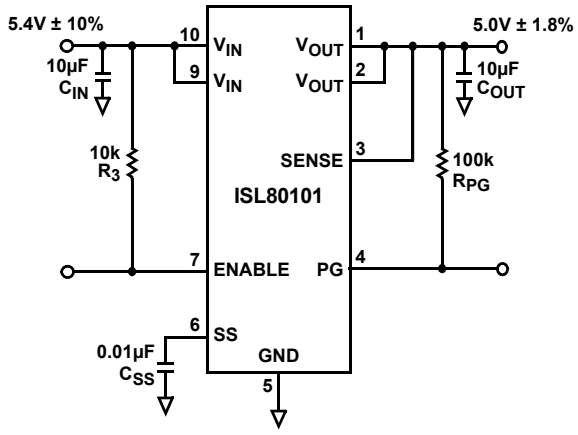



**FIGURE 1. TYPICAL APPLICATION CIRCUIT**

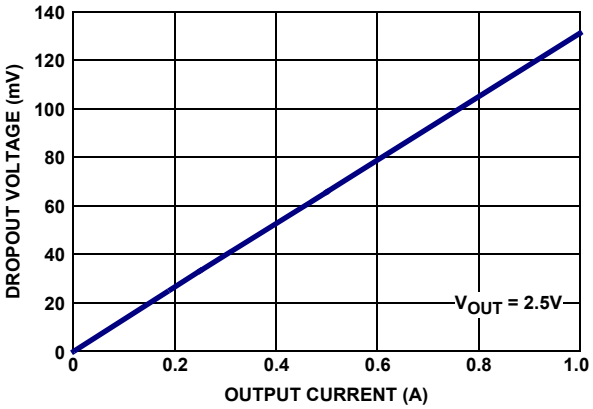



**FIGURE 2. DROPOUT vs LOAD CURRENT**

# Block Diagram

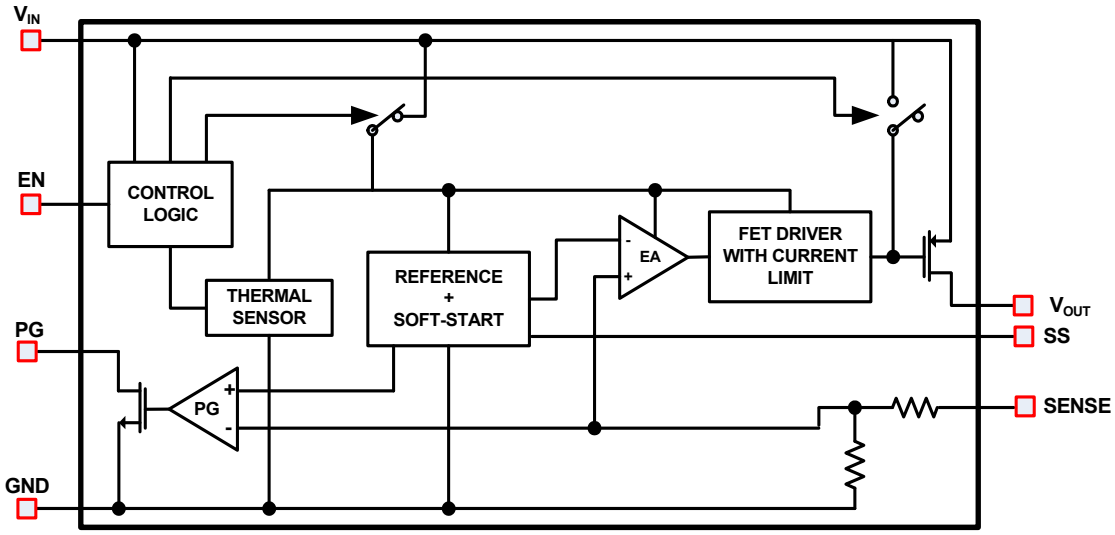



FIGURE 3. BLOCK DIAGRAM

# Ordering Information

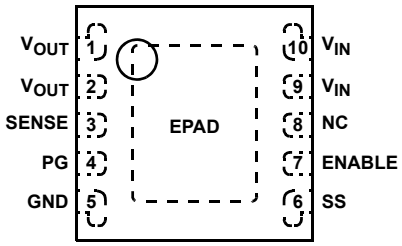
| PART NUMBER (Notes 1, 3, 4) | PART MARKING | $V_{OUT}$ VOLTAGE (Note 2) | TEMP RANGE (°C) | PACKAGE (RoHS COMPLIANT) | PKG DWG. # |
|---|---|---|---|---|---|
| ISL80101IR18Z | DZEB | 1.8V | -40 to +125 | 10 Ld 3x3 DFN | L10.3x3 |
| ISL80101IR25Z | DZFB | 2.5V | -40 to +125 | 10 Ld 3x3 DFN | L10.3x3 |
| ISL80101IR33Z | DZGB | 3.3V | -40 to +125 | 10 Ld 3x3 DFN | L10.3x3 |
| ISL80101IR50Z | DZHB | 5.0V | -40 to +125 | 10 Ld 3x3 DFN | L10.3x3 |
| ISL80101EVAL2Z | Evaluation Board | | | | |

NOTES:

1. Add "-T*" for Tape and Reel. Please refer to TB347 for details on reel specifications.
2. For other output voltages, contact Intersil Marketing.
3. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
4. For Moisture Sensitivity Level (MSL), please see device information page for ISL80101. For more information on MSL please see Technical Brief TB363.

# Pin Configuration

ISL80101
(10 LD 3x3 DFN)
TOP VIEW




# Pin Descriptions

| PIN NUMBER | PIN NAME | DESCRIPTION |
|---|---|---|
| 1, 2 | $V_{OUT}$ | Regulated output voltage. A minimum 10µF X5R/X7R output capacitor is required for stability. See "External Capacitor Requirements" on page 8 for more details. |
| 3 | SENSE | Sense is the LDO's output feedback, providing a remote voltage sensing. |
| 4 | PG | This is an open-drain logic output used to indicate the status of the output voltage. Logic low indicates $V_{OUT}$ is not in regulation. This pin must be grounded if not used. |
| 5 | GND | Ground |
| 6 | SS | External capacitor on this pin adjusts startup ramp and controls inrush current. |
| 7 | ENABLE | $V_{IN}$ independent chip enable. TTL and CMOS compatible. |
| 8 | NC | No connection; Leave floating. |
| 9, 10 | $V_{IN}$ | Input supply; A minimum of 10µF X5R/X7R input capacitor is required for proper operation. See "External Capacitor Requirements" on page 8 for more details. |
| - | EPAD | EPAD at ground potential; It is recommended to solder the EPAD to the ground plane. |

## Absolute Maximum Ratings

$V_{IN}$ Relative to GND (Note 5) . . . . . -0.3V to +6.5V
$V_{OUT}$ Relative to GND (Note 5) . . . . . -0.3V to +6.5V
PG, ENABLE, SENSE, SS
Relative to GND (Note 5) . . . . . -0.3V to +6.5V
ESD Rating
Human Body Model (Tested per JESD22 A114F) . . . . . 2.5kV
Machine Model (Tested per JESD22 A115C) . . . . . 250V
Charge Device Model (Tested per JESD22-C101C) . . . . . 2kV
Latch-Up (Tested per JESD78C, Class 2, Level A) . . . . ±100mA at +125°C

## Thermal Information

| Thermal Resistance (Typical) | $\theta_{JA}$ (°C/W) | $\theta_{JC}$ (°C/W) |
|---|---|---|
| 10 Ld DFN Package (Notes 6, 7) . . . . . | 48 | 7 |

Storage Temperature Range . . . . . -65°C to +150°C
Junction Temperature . . . . . +150°C
Pb-Free Reflow Profile . . . . . see TB493

## Recommended Operating Conditions (Notes 8)

Junction Temperature Range ($T_J$) (Note 8) . . . . . -40°C to +125°C
$V_{IN}$ Relative to GND . . . . . 2.2V to 6V
$V_{OUT}$ Range . . . . . 800mV to 5V
PG, ENABLE, SENSE, SS relative to GND . . . . . 0V to 6V
PG Sink Current . . . . . <10mA

*CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.*

NOTES:

5. Absolute maximum voltage rating is defined as the voltage applied for a lifetime average duty cycle above 6V of 1%.
6. $\theta_{JA}$ is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
7. For $\theta_{JC}$, the "case temp" location is the center of the exposed metal pad on the package underside.
8. Extended operation at these conditions may compromise reliability. Exceeding these limits will result in damage. Recommended operating conditions define limits where specifications are guaranteed.

## Electrical Specifications

Unless otherwise noted, $V_{OUT}$ + 0.4V, < $V_{IN}$ < 6V, $T_J$ = +25°C. Applications must follow thermal guidelines of the package to determine worst case junction temperature. Please refer to "Applications Information" on page 8 and Tech Brief TB379. Boldface limits apply across the operating temperature range, -40°C to +125°C.

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN (Note 9) | TYP | MAX (Note 9) | UNIT |
|---|---|---|---|---|---|---|
| **DC CHARACTERISTICS** | | | | | | |
| DC Output Voltage Accuracy | $V_{OUT}$ | 0A < $I_{LOAD}$ < 1A | **-1.8** | | **1.8** | % |
| DC Input Line Regulation | (VOUT low line- VOUT high line)/ VOUT low line | | **-1** | | **1** | % |
| DC Output Load Regulation | (VOUT no load-VOUT high load)/ VOUT no load | 0A < $I_{LOAD}$ < 1A, All voltage options | -1 | | **1** | % |
| Ground Pin Current | $I_Q$ | $I_{LOAD}$ = 0A | | 3 | **5** | mA |
| | | $I_{LOAD}$ = 1A | | 5 | **7** | mA |
| Ground Pin Current in Shutdown | $I_{SHDN}$ | ENABLE Pin = 0.2V, $V_{IN}$ = 6V | | 0.2 | **12** | µA |
| Dropout Voltage (Note 10) | $V_{DO}$ | $I_{LOAD}$ = 1A, $V_{OUT}$ = 2.5V | | 130 | **212** | mV |
| Output Short-Circuit Current | OCP | $V_{OUT}$ = 0V | | 1.75 | | A |
| Thermal Shutdown Temperature | TSD | | | 160 | | °C |
| Thermal Shutdown Hysteresis | TSDn | | | 30 | | °C |
| **AC CHARACTERISTICS** | | | | | | |
| Input Supply Ripple Rejection | PSRR | f = 1kHz, $I_{LOAD}$ = 1A; $V_{IN}$ = 2.2V | | 58 | | dB |
| | | f = 120Hz, $I_{LOAD}$ = 1A; $V_{IN}$ = 2.2V | | 65 | | dB |
| Output Noise Voltage | | $I_{LOAD}$ = 1A, BW = 100Hz < f < 100kHz, $V_{IN}$ = 2.2V, $V_{OUT}$ = 1.8V | | 53 | | $\mu V_{RMS}$ |
| **ENABLE PIN CHARACTERISTICS** | | | | | | |
| Turn-on Threshold | | | **0.5** | 0.8 | **1.0** | V |
| Hysteresis | | | **10** | 80 | **200** | mV |
| ENABLE Pin Turn-On Delay | | $C_{OUT}$ = 10µF, $I_{LOAD}$ = 1A | | 100 | | µs |

**Electrical Specifications** Unless otherwise noted, $V_{OUT}$ + 0.4V, < $V_{IN}$ < 6V, $T_J$ = +25°C. Applications must follow thermal guidelines of the package to determine worst case junction temperature. Please refer to "Applications Information" on page 8 and Tech Brief TB379. Boldface limits apply across the operating temperature range, -40°C to +125°C. **(Continued)**

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN (Note 9) | TYP | MAX (Note 9) | UNIT |
|---|---|---|---|---|---|---|
| ENABLE Pin Leakage Current | | $V_{IN}$ = 6V, ENABLE = 2.8V | | | **1** | µA |
| **SOFT-START CHARACTERISTICS** | | | | | | |
| SS Pin Currents (Note 11) | IPD | $V_{IN}$ = 3.5V, ENABLE = 0V, SS = 1V | **0.5** | 1.0 | **1.3** | mA |
| | ICHG | | **-3.3** | -2.0 | **-0.8** | µA |
| **PG PIN CHARACTERISTICS** | | | | | | |
| $V_{OUT}$ PG Flag Threshold | | | **75** | 85 | **92** | %$V_{OUT}$ |
| $V_{OUT}$ PG Flag Hysteresis | | | | 4 | | % |
| PG Flag Low Voltage | | $V_{IN}$ = 3V, $I_{SINK}$ = 500µA | | | **100** | mV |
| PG Flag Leakage Current | | $V_{IN}$ = 6V, PG = 6V | | | **1** | µA |

NOTES:

9. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
10. Dropout is defined as the difference in supply $V_{IN}$ and $V_{OUT}$ when the output is below its nominal regulation.
11. $I_{PD}$ is the internal pull-down current that discharges the external SS capacitor on disable. $I_{CHG}$ is the current from the SS pin that charges the external SS capacitor during start-up.

# Typical Operating Performance

Unless otherwise noted: $V_{IN}$ = 2.2V, $V_{OUT}$ = 1.8V, $C_{IN}$ = $C_{OUT}$ = 10µF, $T_J$ = +25°C, $I_L$ = 0A.

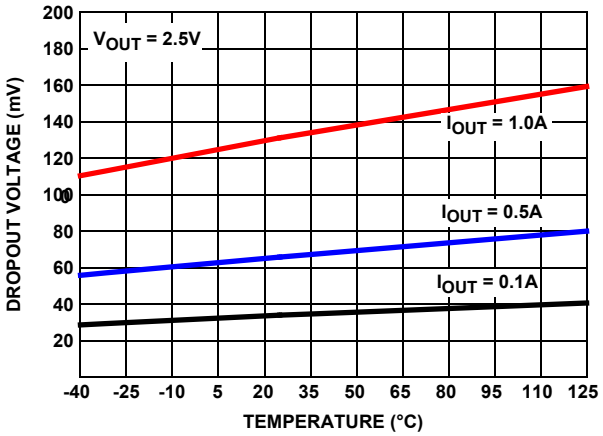



FIGURE 4. DROPOUT VOLTAGE vs TEMPERATURE

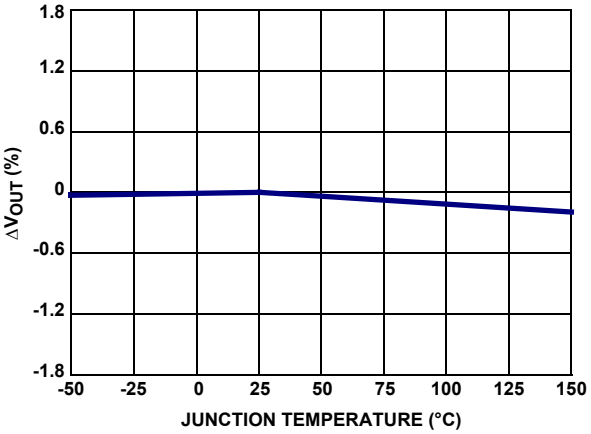



FIGURE 5. $V_{OUT}$ vs TEMPERATURE

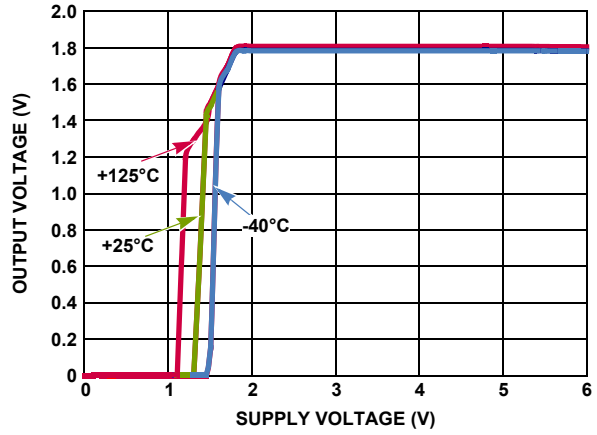



FIGURE 6. OUTPUT VOLTAGE vs SUPPLY VOLTAGE

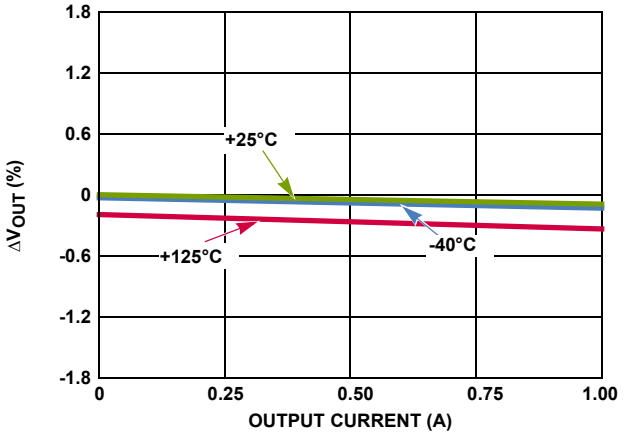



FIGURE 7. OUTPUT VOLTAGE vs OUTPUT CURRENT

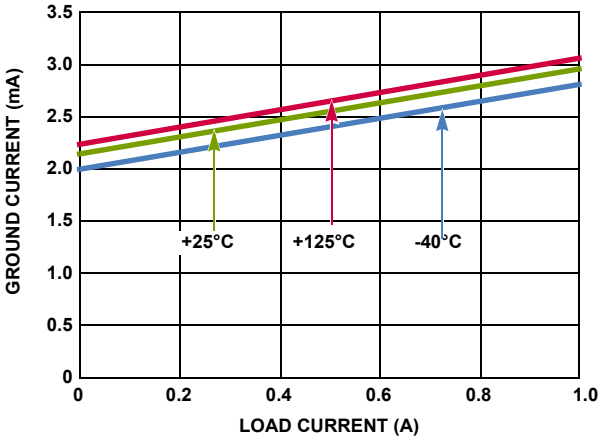



FIGURE 8. GROUND CURRENT vs LOAD CURRENT

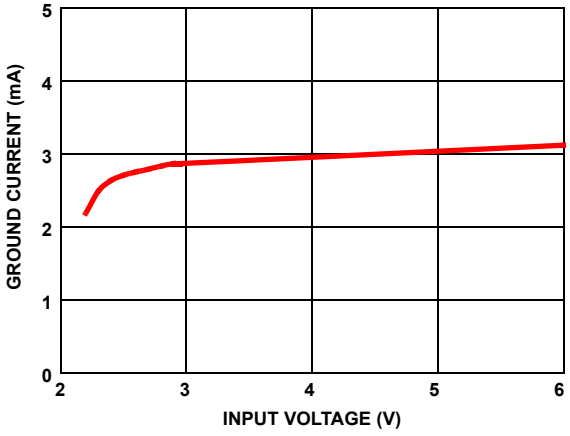



FIGURE 9. GROUND CURRENT vs SUPPLY VOLTAGE

## Typical Operating Performance

Unless otherwise noted: $V_{IN}$ = 2.2V, $V_{OUT}$ = 1.8V, $C_{IN}$ = $C_{OUT}$ = 10µF, $T_J$ = +25°C, $I_L$ = 0A. **(Continued)**

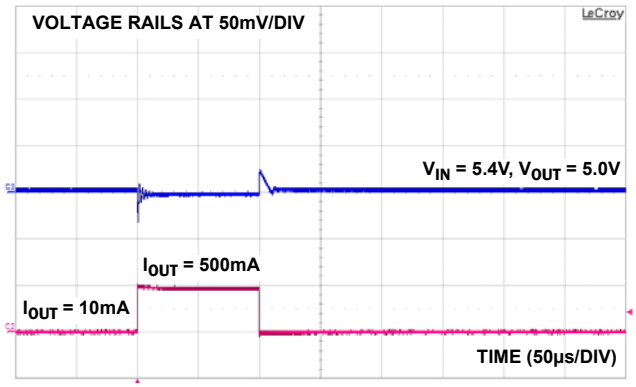



FIGURE 10A.

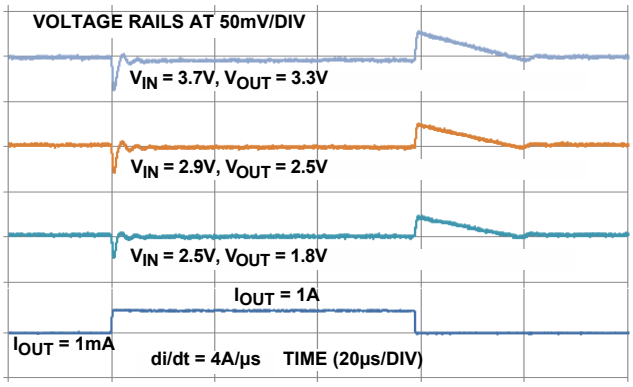



FIGURE 10B.

FIGURE 10. LOAD TRANSIENT RESPONSE

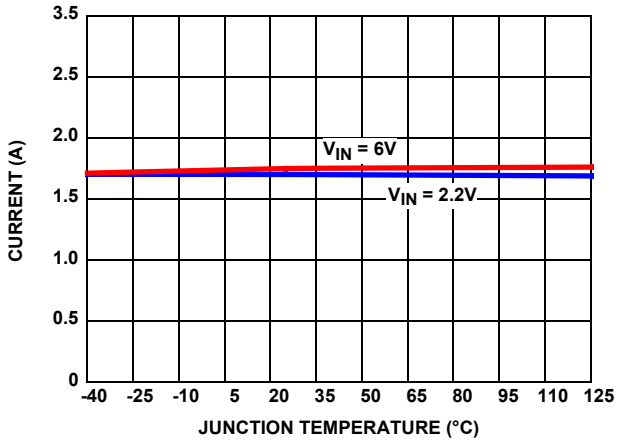



FIGURE 11. CURRENT LIMIT vs TEMPERATURE ($V_{OUT}$ = 0V)

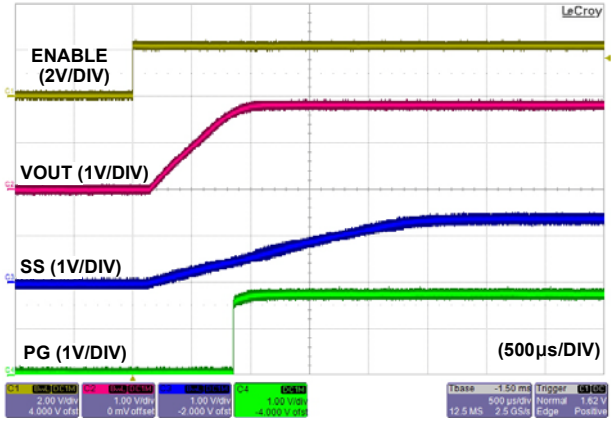



FIGURE 12. ENABLE START-UP ($C_{SS}$ = 2.2nF)

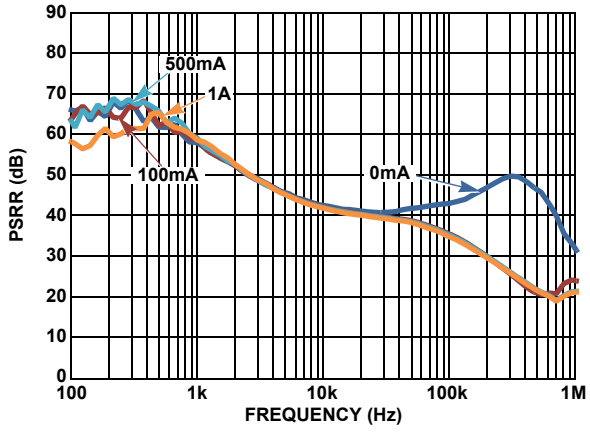



FIGURE 13. PSRR vs FREQUENCY FOR VARIOUS LOAD CURRENTS

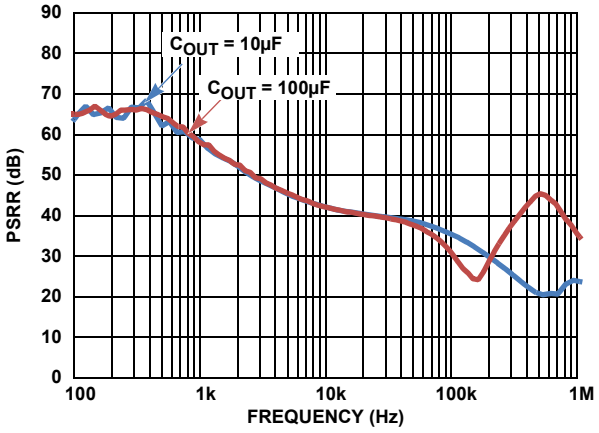



FIGURE 14. PSRR vs FREQUENCY FOR VARIOUS OUTPUT CAPACITORS ($I_{OUT}$ = 100mA)

## Typical Operating Performance

Unless otherwise noted: $V_{IN}$ = 2.2V, $V_{OUT}$ = 1.8V, $C_{IN}$ = $C_{OUT}$ = 10µF, $T_J$ = +25°C, $I_L$ = 0A. **(Continued)**

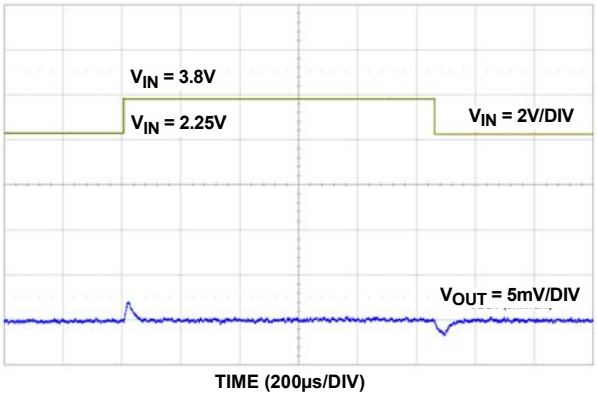



FIGURE 15. LINE TRANSIENT RESPONSE

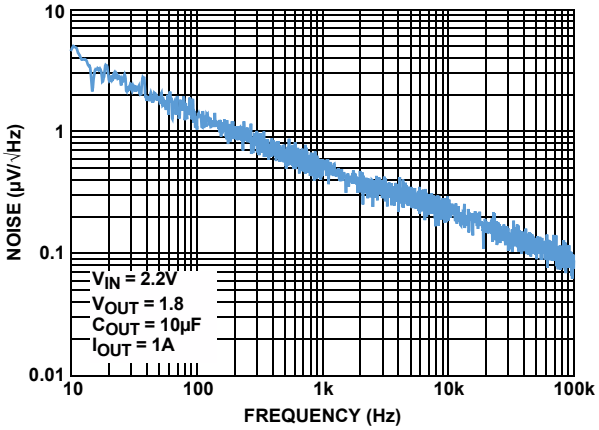



FIGURE 16. OUTPUT NOISE SPECTRAL DENSITY

# Applications Information

## Input Voltage Requirements

The ISL80101 is capable of delivering the following fixed output voltages: 1.8V, 2.5V, 3.3V, 5.0V. Due to the nature of an LDO, $V_{IN}$ must be some margin higher than $V_{OUT}$ plus dropout at the maximum rated current of the application if active filtering (PSRR) is expected from $V_{IN}$ to $V_{OUT}$. The generous dropout specification of this family of LDOs allows applications to design a level of efficiency.

## Enable Operation

The ENABLE turn-on threshold is typically 800mV with 80mV of hysteresis. An internal pull-up or pull-down resistor to change these values is available upon request. As a result, this pin must not be left floating, and should be tied to $V_{IN}$ if not used. A 1kΩ to 10kΩ pull-up resistor is required for applications that use open collector or open drain outputs to control the ENABLE pin. The ENABLE pin may be connected directly to $V_{IN}$ for applications with outputs that are always on.

## Power-Good Operation

PG is a logic output that indicates the status of $V_{OUT}$. The PG flag is an open-drain NMOS that can sink up to 10mA during a fault condition. The PG pin requires an external pull-up resistor typically connected to the $V_{OUT}$ pin. The PG pin should not be pulled up to a voltage source greater than $V_{IN}$. PG goes low when the output voltage drops below 84% of the nominal output voltage or if the part is disabled. PG functions during current limit and thermal shutdown. For applications not using this feature, connect this pin to ground.

## Soft-Start Operation

The soft-start circuit controls the rate at which the output voltage rises up to regulation at power-up or LDO enable. This start-up ramp time can be set by adding an external capacitor from the SS pin to ground. An internal 2µA current source charges up $C_{SS}$ and the feedback reference voltage is clamped to the voltage across it. The start-up time is set by Equation 1.

$$t_{start} = \frac{C_{SS} x 0.5}{2\mu A} \quad \text{(EQ. 1)}$$

Equation 2 determines the $C_{SS}$ required for a specific start-up in-rush current, where $V_{OUT}$ is the output voltage, $C_{OUT}$ is the total capacitance on the output and $I_{INRUSH}$ is the desired inrush current.

$$C_{SS} = \frac{V_{OUT} x C_{OUT} x 2\mu A}{I_{INRUSH} x 0.5V} \quad \text{(EQ. 2)}$$

The external capacitor is always discharged to ground at the beginning of start-up or enabling.

## External Capacitor Requirements

External capacitors are required for proper operation. Careful attention must be paid to the layout guidelines and selection of capacitor type and value to ensure optimal performance.

### OUTPUT CAPACITOR

The ISL80101 applies state-of-the-art internal compensation to keep the selection of the output capacitor simple for the customer. Stable operation over full temperature, $V_{IN}$ range, $V_{OUT}$ range and load extremes are guaranteed for all capacitor types and values assuming a minimum of 10µF X5R/X7R is used for local bypass on $V_{OUT}$. This output capacitor must be connected to the $V_{OUT}$ and GND pins of the LDO with PCB traces no longer than 0.5cm.

There is a growing trend to use very-low ESR multilayer ceramic capacitors (MLCC) because they can support fast load transients and also bypass very high frequency noise from other sources. However, the effective capacitance of MLCCs drops with applied voltage, age, and temperature. X7R and X5R dieletric ceramic capacitors are strongly recommended as they typically maintain a capacitance range within ±20% of nominal voltage over full operating ratings of temperature and voltage.

Additional capacitors of any value in ceramic, POSCAP, alum/tantalum electrolytic types may be placed in parallel to improve PSRR at higher frequencies and/or load transient AC output voltage tolerances.

### INPUT CAPACITOR

For proper operation, a minimum capacitance of 10µF X5R/X7R is required at the input. This ceramic input capacitor must be connected to the $V_{IN}$ and GND pins of the LDO with PCB traces no longer than 0.5cm.

## Power Dissipation and Thermals

The junction temperature must not exceed the range specified in the "Recommended Operating Conditions" on page 4. The power dissipation can be calculated by using Equation 3:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{GND} \quad \text{(EQ. 3)}$$

The maximum allowable junction temperature, $T_{J(MAX)}$ and the maximum expected ambient temperature, TA(MAX) determine the maximum allowable power dissipation, as shown in Equation 4:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A)/\theta_{JA} \quad \text{(EQ. 4)}$$

$\theta_{JA}$ is the junction-to-ambient thermal resistance.

For safe operation, enure that the power dissipation $P_D$, calculated from Equation 3, is less than the maximum allowable power dissipation $P_{D(MAX)}$.

The DFN package uses the copper area on the PCB as a heatsink. The EPAD of this package must be soldered to the copper plane (GND plane) for effective heat dissipation. Figure 17 shows a curve for the $\theta_{JA}$ of the DFN package for different copper area sizes.

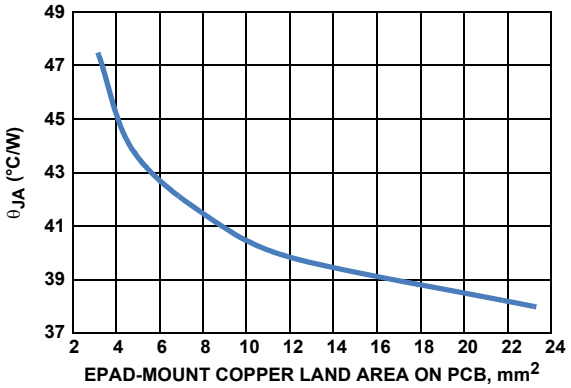



**FIGURE 17. 3mmx3mm-10 PIN DFN ON 4-LAYER PCB WITH THERMAL VIAS $\theta_{JA}$ vs EPAD-MOUNT COPPER LAND AREA ON PCB**

## Thermal Fault Protection

The power level and the thermal impedance of the package (+45°C/W for DFN) determine when the junction temperature exceeds the thermal shutdown temperature. In the event that the die temperature exceeds around +160°C, the output of the LDO will shut down until the die temperature cools down to about +130°C.

## Current Limit Protection

The ISL80101 LDO incorporates protection against overcurrent due to any short or overload condition applied to the output pin. The LDO performs as a constant current source when the output current exceeds the current limit threshold noted in the "Electrical Specifications" table on page 4. If the short or overload condition is removed from $V_{OUT}$, then the output returns to normal voltage regulation mode. In the event of an overload condition, the LDO may begin to cycle on and off due to the die temperature exceeding thermal fault condition and subsequently cooling down after the power device is turned off.

## Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

| DATE | REVISION | CHANGE |
|---|---|---|
| September 6, 2016 | FN6931.3 | Removed Note 9 “Electromigration specification defined as lifetime average junction temperature of +110°C where max rated DC current = lifetime average current” from Recommended Operating Conditions. |
| September 25, 2015 | FN6931.2 | Applied New Intersil Standards<br>Removed 1st bullet in Features on page 1 which read ±0.2% initial $V_{OUT}$ accuracy<br>Changed 7th bullet in Features on page 1 from Excellent 58dB PSRR at 1kHz to Excellent 65dB PSRR<br>“Pin Descriptions” on page 3 - description reworded for clarity.<br>Changed temperature of Latch-up in “Absolute Maximum Ratings” on page 4 from +85°C to +125°C.<br>Removed “ADJ” from Sense in “Recommended Operating Conditions” on page 4.<br>Updated the EA amp in the “Block Diagram” on page 2 by switching the + and - terminals. The positive terminal is now connected to the Sense pin.<br>Added Note 11 on page 5, “IPD is the internal pull-down current that discharges the external SS capacitor on disable. ICHG is the current from the SS pin that charges the external SS capacitor during start-up.”<br>Changed Title of Figure 4 on page 6 from Dropout vs Temperature to Dropout Voltage vs Temperature<br>Changed y-axis in Figures 6 and 8 on page 6 from: $DV_{OUT}$ (%) to: $\Delta V_{OUT}$ (%)<br>Changed Time Scale in Figure 10B on page 7 from 50µs to 20µs<br>Added $V_{IN}$ = to values in Figure 11 on page 7<br>Changed Title in Figure 13 on page 7 from PSRR vs Frequency and Load Current to PSRR vs Frequency for various load currents<br>Changed Title in Figure 14 on page 7 from PSRR vs Frequency and Output Capacitance ($I_{OUT}$ = 100mA) to PSRR vs Frequency for various output capacitors ($I_{OUT}$=100mA)<br>Updated Output Spectral Noise Density (Figure 16 on page 8)<br>Removed mention of “$V_{IN}$” in 1st sentence of “Power-Good Operation” on page 8<br><br>**Electrical Spec ifications changes**:<br>Electrical Spec Table conditions on page 4, changed from: $V_{IN} = V_{OUT} + 0.4V$, $V_{OUT}$ = 1.8V, $C_{IN} = C_{OUT}$ = 2.2µF, to: VOUT + 0.4V, < $V_{IN}$ < 6V<br>“DC Output Voltage Accuracy” on page 4, test conditions changed from: $V_{OUT} + 0.4V < V_{IN} < 6V$, $0A < I_{LOAD} < 1A$, to: $0A < I_{LOAD} < 1A$<br>“DC Input Line Regulation” on page 4 - changed symbol from $\Delta V_{OUT}/\Delta V_{IN}$ to VOUT low line - VOUT high line)/VOUT low line. Removed Test Conditions·<br>“DC Output Load Regulation” on page 4 - changed symbol from $\Delta V_{OUT}/\Delta I_{OUT}$ to $V_{OUT}$ no load-$V_{OUT}$ high load)/ $V_{OUT}$ no load and added MAX of 1<br>Ground Pin Current test conditions changed from:<br>ILOAD = 0A, 2.2V < VIN < 6V to: ILOAD = 0A<br>ILOAD = 1A, 2.2V < VIN < 6V to: ILOAD = 1A<br>Output Short-Circuit Current changed test conditions from: $V_{OUT}$ = 0V, $2.2V < V_{IN} < 6V$ to: $V_{OUT}$ = 0V<br>Thermal Shutdown Temperature - removed test conditions.<br>Removed “Rising Threshold” from “Thermal Shutdown Hysteresis”. Removed test conditions.<br>“AC CHARACTERISTICS” on page 4 changed TYP from “72” to “65” in PSRR, f = 120Hz and in Output Noise Voltage in test conditions changed “10Hz” to “100Hz” and added $V_{IN}$ = 2.2V, $V_{OUT}$ = 1.8V. TYP changed from “63” to “53”<br>“Turn-on Threshold” on page 4 changed MIN from: 0.3 to: 0.5. Removed test conditions<br>Removed “Rising Threshold” from “Hysteresis” on page 4 and removed test conditions<br>Changed in “ENABLE Pin Leakage Current” on page 5 - 3V to 2.8V in test conditions<br>Changed in “PG Flag Low Voltage” on page 5 - test conditions from: $V_{IN}$ = 2.5V, $I_{SINK}$ = 500µA; to: $V_{IN}$ = 3V, $I_{SINK}$ = 500µA<br><br>Updated POD L10.3x3 to most recent revision with change as follows:<br>Added missing dimension 0.415 in Typical Recommended land pattern.<br>Shortened the e-pad rectangle on both the recommended land pattern and the package bottom view to line up with the centers of the corner pins.<br>Tiebar Note 4 updated<br>From: Tiebar shown (if present) is a non-functional feature.<br>To: Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends). |

## Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision. **(Continued)**

| DATE | REVISION | CHANGE |
|---|---|---|
| July 27, 2011 | FN6931.1 | Added Related Literature<br>Main change - Deleted Adjustable Output Voltage Option Version from datasheet, now only refers to fixed output voltage option includes removal of all graphics referring to Adjustable voltage option.<br>Modified page 1 by adding Table of key differences, graphics and changes to text<br>page 2 - Updated Ordering Information by:<br>Removing ADJ Device ISL80101IRAJZ plus Eval boards.<br>Updated Tape and Reel Note by changing "Add "-T" or "TK"..." to "Add "T*"..."<br>Updated Abs Max Rating and Thermal Information by adding ESD ratings and Latchup<br>Changed 10 Ld DFN Tja and Tjc from “45, 4” to “48, 7”<br>Updated DC Output Voltage Accuracy by combining Vout options<br>Removed Feedback Pin (Adj Option Only), Feedback Input Current Specs<br>Removed "(1A Version)" from Output Short-circuit Current Spec<br>Removed Adjustable Inrush Current Limit Characteristics and replaced with Soft-Start Characteristics<br>page 5 - Electrical Spec Note changed from "Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design." To "Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested."<br>Complete Rewrite of Applications Information<br>POD L10.3x3 Changed Note 4 from "Dimension b applies..." to "Lead width applies..."<br>Changed Note callout in Detail X from 4 to 5<br>Changed height in side view from 0.90 MAX to 1.00 MAX<br>Added Note 4 callout next to lead width in Bottom View<br>In Land Pattern, corrected lead shape for 4 corner pins to "L" shape (was rectangular and did not match bottom view) |
| December 21, 2009 | FN6931.0 | Initial Release. |

## About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

Reliability reports are also available from our website at www.intersil.com/support.

© Copyright Intersil Americas LLC 2009-2011. All Rights Reserved.
All trademarks and registered trademarks are the property of their respective owners.

For additional products, see www.intersil.com/en/products.html

Intersil products are manufactured, assembled and tested utilizing ISO9001 quality systems as noted in the quality certifications found at www.intersil.com/en/support/qualandreliability.html

*Intersil products are sold by description only. Intersil may modify the circuit design and/or specifications of products at any time without notice, provided that such modification does not, in Intersil's sole judgment, affect the form, fit or function of the product. Accordingly, the reader is cautioned to verify that datasheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.*

For information regarding Intersil Corporation and its products, see www.intersil.com

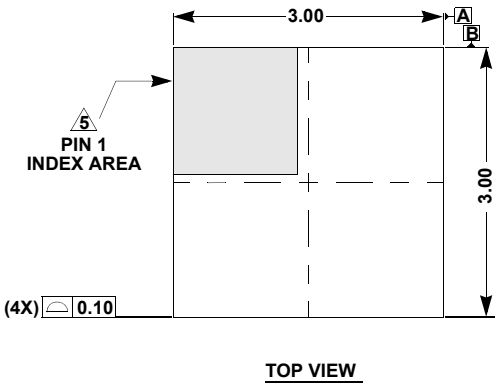
# Package Outline Drawing

For the most recent package outline drawing, see L10.3x3.

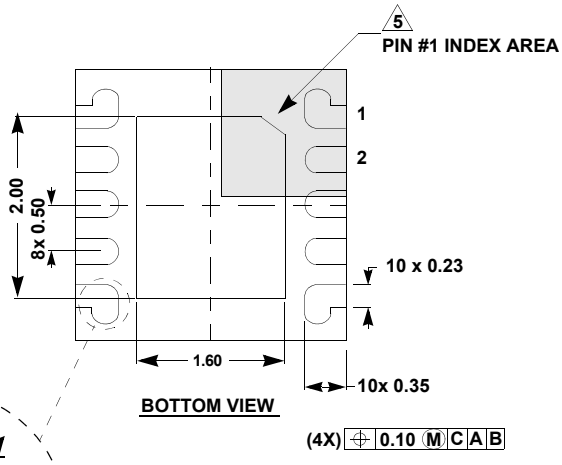
## L10.3x3

**10 LEAD DUAL FLAT PACKAGE (DFN)**

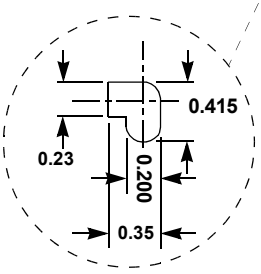
**Rev 11, 3/15**

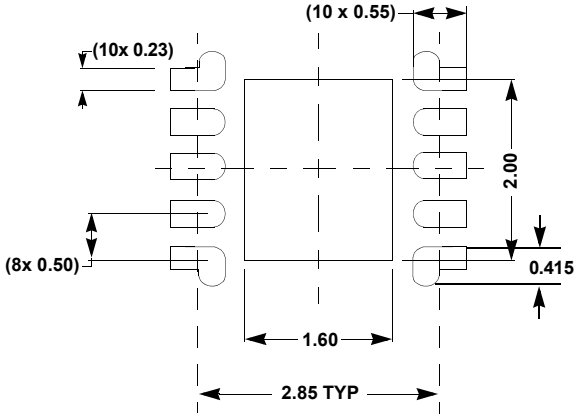



TOP VIEW

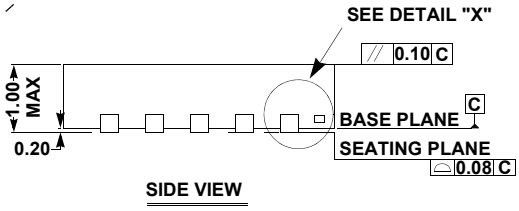



BOTTOM VIEW

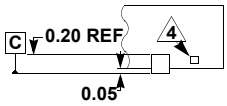



TYPICAL RECOMMENDED LAND PATTERN




SIDE VIEW




DETAIL "X"

**NOTES:**

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends).
5. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.