SIEMENS

SAB 8085AH
8-Bit Microprocessor

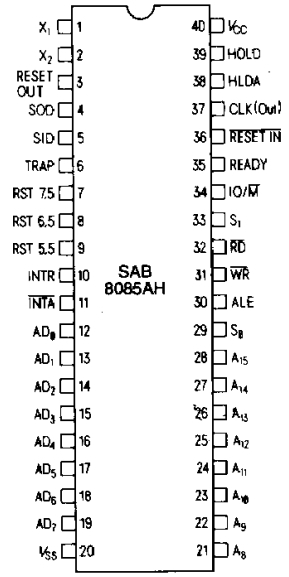
SAB 8085AH (3 MHz)

- Single +5V Power Supply with ±10% Voltage Margins
- 30% Less I_{CC} than SAB 8085A
- 100% Software Compatible with SAB 8080A
- 1.3 µs Instruction Cycle (SAB 8085AH); 0.8 µs (SAB 8085AH-2)
- On-Chip Clock Generator (with External Crystal, LC or RC Network)
- On-Chip System Controller; Advanced Cycle Status Information Available for Large System Control

SAB 8085AH-2 (5 MHz)

- Four Vectored Interrupt Inputs (one is Non-Maskable) Plus an SAB 8080A Compatible Interrupt
- Serial In/Serial Out Port
- Decimal, Binary and Double Precision Arithmetic
- Direct Addressing Capability to 64K Bytes of Memory

Pin Diagram



Pin Names

A_8-A_{15}	Address Bus	$\overline{INTA}$	Interrupt Acknowledge
AD_0-AD_7	Mux. Address/ Data Bus	RST 5.5, 6.5, 7.5	Restart Interrupts
ALE	Address Latch Enable	TRAP	Trap
S_0, S_1, IO/$\overline{M}$	Machine Cycle Status	$\overline{RESET\ IN}$	Reset in
		RESET OUT	Reset out
$\overline{RD}$	Read Control		
$\overline{WR}$	Write Control	X_1, X_2	Crystal/Clock Input
READY	Ready	CLK	Clock Output
HOLD	Hold	SID	Serial Input Data
HLDA	Hold Acknowledge	SOD	Serial Output Data
INTR	Interrupt Request	V_{CC}	+5V
		V_{SS}	Ground (OV)

SAB 8085AH is a complete 8 bit parallel Central Processing Unit (CPU). Its instruction set is 100% software compatible with the SAB 8080A microprocessor. Its high level of system integration allows a minimum of three IC's [SAB 8085AH (CPU), SAB 8156 (RAM/IO) and SAB 8355/SAB 8755A (ROM/PROM/IO)] while maintaining total system expandability. The SAB 8085AH-2 is a faster version of the SAB 8085AH.

The SAB 8085AH incorporates all of the features that the SAB 8224 (clock generator) and SAB 8228 (system controller) provided for the SAB 8080A, thereby offering a high level of system integration.

The SAB 8085AH uses a multiplexed data bus. The address is split between the 8 bit address bus and the 8 bit data bus. The on-chip address latches of SAB 8155/SAB 8156/SAB 8355/SAB 8755A memory products allow a direct interface with the SAB 8085AH.

SAB 8085AH is implemented in +5V advanced N-channel, silicon gate Siemens MYMOS technology and is a selected version of the standard SAB 8085A.

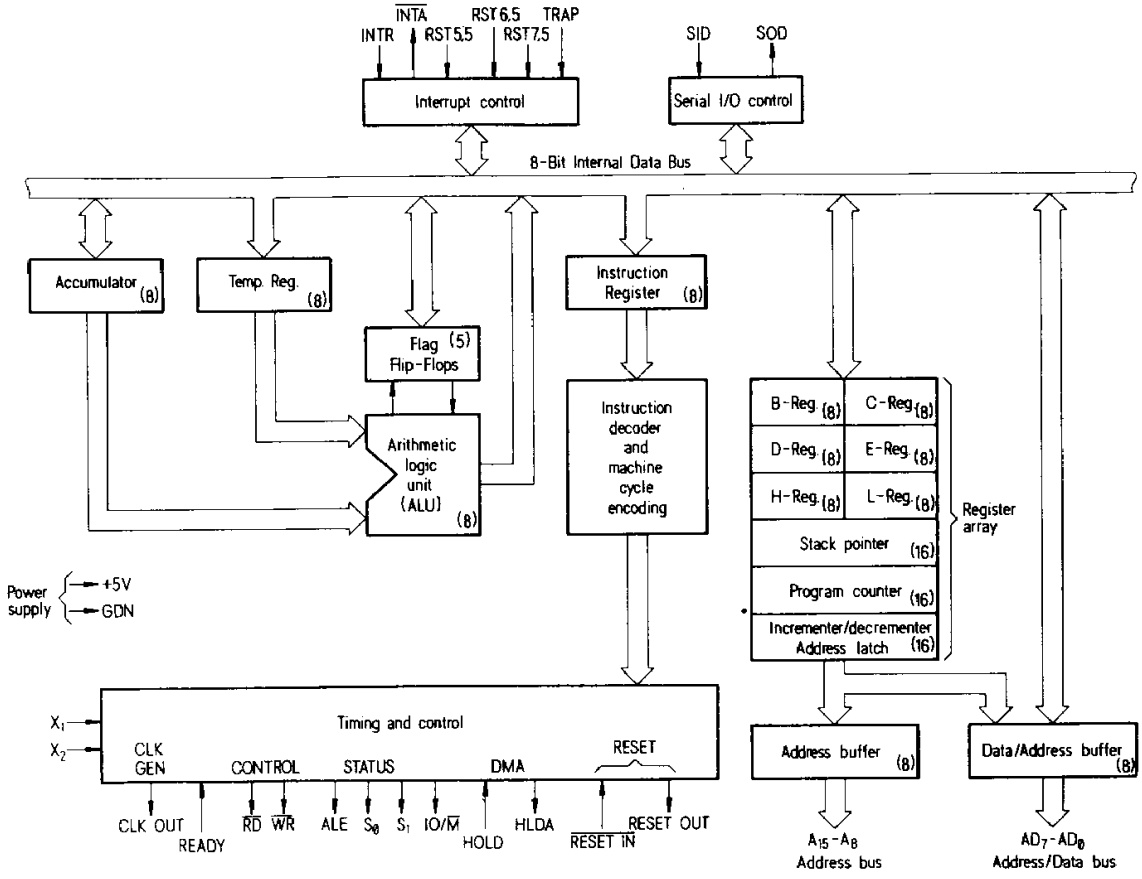
Pin Definitions and Functions

Symbol	Number	Input (I) Output (O)	Function
X_1, X_2	1, 2	I	X_1 AND X_2 – Are connected to a crystal, LC, or RC network to drive the internal clock generator. X_1 can also be an external clock input from a logic gate. The input frequency is divided by 2 to give the processor's internal operating frequency.
RESET OUT	3	O	RESET OUT – Reset Out indicates CPU is being reset. Can be used as a system reset. The signal is synchronized to the processor clock and lasts an integral number of clock periods.
SOD	4	O	SERIAL OUTPUT DATA LINE – The output SOD is set or reset as specified by the SIM instruction.
SID	5	I	SERIAL INPUT DATA LINE – The data on this line is loaded into accumulator bit 7 whenever a RIM instruction is executed.
TRAP	6	I	TRAP – Trap interrupt is a nonmaskable RESTART interrupt. It is recognized at the same time as INTR or RST 5.5-7.5. It is unaffected by any mask or Interrupt Enable. It has the highest priority of any interrupt (see following table).
RST 5.5 RST 6.5 RST 7.5	9 8 7	I	RESTART INTERRUPTS – These three inputs have the same timing as INTR except they cause an internal RESTART to be automatically inserted. The priority of these interrupts is ordered as shown in the following table. These interrupts have a higher priority than INTR. In addition, they may be individually masked out using the SIM instruction.
INTR	10	I	INTERRUPT REQUEST – Is used as a general purpose interrupt. It is sampled only during the next to the last clock cycle of an instruction and during Hold and Halt states. If it is active, the Program Counter (PC) will be inhibited from incrementing and an $\overline{\text{INTA}}$ will be issued. During this cycle a RESTART or CALL instruction can be inserted to jump to the interrupt service routine. The INTR is enabled and disabled by software. It is disabled by Reset and immediately after an interrupt is accepted.
$\overline{\text{INTA}}$	11	O	INTERRUPT ACKNOWLEDGE – Is used instead of (and has the same timing as) $\overline{\text{RD}}$ during the instruction cycle after an INTR is accepted. It can be used to activate an SAB 8259A Interrupt chip or some other interrupt port.
AD_0–AD_7	12–19	I/O	MULTIPLEXED ADDRESS/DATA BUS – Lower 8 bits of the memory address (or I/O address) appear on the bus during the first clock cycle (T state) of a machine cycle. It then becomes the data bus during the second and third clock cycles.
A_8–A_{15}	21–28	O	ADDRESS BUS – The most significant 8 bits of the memory address or the 8 bits of the I/O address, 3-stated during Hold and Halt modes and during RESET.

<table>
<tr><th>Symbol</th><th>Number</th><th>Input (I)
Output (O)</th><th>Function</th></tr>
<tr><td>$S_\emptyset$, S_1, and IO/$\overline{M}$</td><td>29, 33
34</td><td>O</td><td>MACHINE CYCLE STATUS –
<table>
<tr><th>IO/$\overline{M}$</th><th>S_1</th><th>$S_\emptyset$</th><th>Status</th></tr>
<tr><td>$\emptyset$</td><td>$\emptyset$</td><td>1</td><td>Memory write</td></tr>
<tr><td>$\emptyset$</td><td>1</td><td>$\emptyset$</td><td>Memory read</td></tr>
<tr><td>1</td><td>$\emptyset$</td><td>1</td><td>I/O write</td></tr>
<tr><td>1</td><td>1</td><td>$\emptyset$</td><td>I/O read</td></tr>
<tr><td>$\emptyset$</td><td>1</td><td>1</td><td>Opcode fetch</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Opcode fetch</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Interrupt Acknowledge</td></tr>
<tr><td>*</td><td>$\emptyset$</td><td>$\emptyset$</td><td>Halt</td></tr>
<tr><td>*</td><td>X</td><td>X</td><td>Hold</td></tr>
<tr><td>*</td><td>X</td><td>X</td><td>Reset</td></tr>
</table>
* = 3-state (high impedance)
X = unspecified
S_1 can be used as an advanced R/$\overline{W}$ status. IO/$\overline{M}$, $S_\emptyset$ and S_1 become valid at the beginning of a machine cycle and remain stable throughout the cycle. The falling edge of ALE may be used to latch the state of these lines.</td></tr>
<tr><td>ALE</td><td>30</td><td>O</td><td>ADDRESS LATCH ENABLE – It occurs during the first clock state of a machine cycle and enables the address to get latched into the on-chip latch of peripherals. The falling edge of ALE is set to guarantee setup and hold times for the address information. The falling edge of ALE can also be used to strobe the status information. ALE is never 3-stated.</td></tr>
<tr><td>$\overline{WR}$</td><td>31</td><td>O</td><td>WRITE CONTROL – A low level on $\overline{WR}$ indicates the data on the Data Bus is to be written into the selected memory or I/O location. Data is set up at the trailing edge of $\overline{WR}$. 3-stated during Hold and Halt modes and during RESET.</td></tr>
<tr><td>$\overline{RD}$</td><td>32</td><td>O</td><td>READ CONTROL – A low level on $\overline{RD}$ indicates the selected memory or I/O device is to be read and that the Data Bus is available for the data transfer, 3-stated during Hold and Halt modes and during RESET.</td></tr>
<tr><td>READY</td><td>35</td><td>I</td><td>READY – If READY is high during a read or write cycle, it indicates that the memory or peripheral is ready to send or receive data. If READY is low, the CPU will wait an integral number of clock cycles for READY to go high before completing the read or write cycle. READY must conform to specified setup and hold times.</td></tr>
<tr><td>$\overline{RESET\ IN}$</td><td>36</td><td>I</td><td>RESET IN – Sets the Program Counter to zero and resets the Interrupt Enable and HLDA flip-flops. The data and address buses and the control lines are 3-stated during RESET and because of the asynchronous nature of RESET, the processor's internal registers and flags may be altered by RESET with unpredictable results. $\overline{RESET\ IN}$ is a Schmitt-triggered input, allowing connection to an RC network for power-on RESET delay. The CPU is held in the reset condition as long as $\overline{RESET\ IN}$ is applied.</td></tr>
<tr><td>CLK</td><td>37</td><td>O</td><td>CLOCK – Clock output for use as a system clock. The period of CLK is twice the X_1, X_2 input period.</td></tr>
</table>

Symbol	Number	Input (I) Output (O)	Function
HLDA	38	O	HOLD ACKNOWLEDGE – Indicates that the CPU has received the HOLD request and that it will relinquish the bus in the next clock cycle. HLDA goes low after the Hold request is removed. The CPU takes the bus one half clock cycle after HLDA goes low.
HOLD	39	I	HOLD – Indicates that another master is requesting the use of the address and data buses. The CPU, upon receiving the hold request, will relinquish the use of the bus as soon as the completion of the current bus transfer. Internal processing can continue. The processor can regain the bus only after the HOLD is removed. When the HOLD is acknowledged, the Address, Data $\overline{RD}$, $\overline{WR}$, and IO/$\overline{M}$ lines are 3-stated.
V_{CC}	40		POWER SUPPLY (+5V)
V_{SS}	20		GROUND (OV)

Functional Block Diagram



Interrupt Priority, Restart Address, and Sensitivity

Name	Priority	Address Branched To[1] When Interrupt Occurs	Type Trigger
TRAP	1	24H	Rising edge AND high level until sampled
RST 7.5	2	3CH	Rising edge (latched)
RST 6.5	3	34H	High level until sampled
RST 5.5	4	2CH	High level until sampled
INTR	5	see Note 2	High level until sampled

NOTES
1. The processor pushes the PC on the stack before branching to the indicated address.
2. The address branched to depends on the instruction provided to the CPU when the interrupt is acknowledged.

Functional Description

The SAB 8085AH is a complete 8-bit parallel central processor. It is designed with N-channel depletion loads and requires a single +5 volt supply. Its basic clock speed is 3 MHz (SAB 8085AH) or 5 MHz (SAB 8085AH-2), thus improving on SAB 8080A's performance with higher system speed. Also it is designed to fit into a minimum system of three IC's: The CPU (SAB 8085AH), a RAM/IO (SAB 8156), and a ROM or EPROM/IO chip (SAB 8355 or SAB 8755A).

The SAB 8085AH has twelve addressable 8-bit registers. Four of them can function only as two 16-bit register pairs. Six others can be used interchangeably as 8-bit registers or as 16-bit register pairs. The SAB 8085AH register set is as follows:

Mnemonic	Register	Contents
ACC or A	Accumulator	8 bits
PC	Program Counter	16-bit address
BC, DE, HL	General-Purpose Registers; data pointer (HL)	8 bits × 6 or 16 bits × 3
SP	Stack Pointer	16-bit address
Flags or F	Flag Register	5 flags (8-bit space)

The SAB 8085AH uses a multiplexed Data Bus. The address is split between the higher 8-bit Address Bus and the lower 8-bit Address/Data Bus. During the first T state (clock cycle) of a machine cycle the low order address is sent out on the Address/Data bus. These lower 8 bits may be latched externally by the Address Latch Enable signal (ALE). During the rest of the machine cycle the data bus is used for memory or I/O data.

The SAB 8085AH provides $\overline{RD}$, $\overline{WR}$, S_0, S_1, and IO/$\overline{M}$ signals for bus control. An Interrupt Acknowledge signal ($\overline{INTA}$) is also provided. HOLD and all Interrupts are synchronized with the processor's internal clock. The SAB 8085AH also provides Serial Input Data (SID) and Serial Output Data (SOD) lines for simple serial interface.

In addition to these features, the SAB 8085AH has three maskable, vector interrupt pins and one nonmaskable TRAP interrupt.

Interrupt and Serial I/O

The SAB 8085AH has 5 interrupt inputs: INTR, RST 5.5, RST 6.5, RST 7.5, and TRAP. INTR is identical in function to the SAB 8080A INT. Each of the three RESTART inputs, 5.5, 6.5, and 7.5, has a programmable mask. TRAP is also a RESTART interrupt but it is nonmaskable.

The three maskable interrupts cause the internal execution of RESTART (saving the program counter in the stack and branching to the RESTART address) if the interrupts are enabled and if the interrupt mask is not set. The non-maskable TRAP causes the internal execution of a RESTART vector independent of the state of the interrupt enable or masks (see table above).

There are two different types of inputs in the restart interrupts. RST 5.5 and RST 6.5 are **high level-sensitive** like INTR (and INT on the SAB 8080) and are recognized with the same timing as INTR. RST 7.5 is **rising edge-sensitive.**

For RST 7.5, only a pulse is required to set an internal flip-flop which generates the internal interrupt request. The RST 7.5 request flip-flop remains set until the request is serviced. Then it is reset automatically. This flip-flop may also be reset

by using the SIM instruction or by issuing a $\overline{\text{RESET IN}}$ to the SAB 8085AH. The RST 7.5 internal flip-flop will be set by a pulse on the RST 7.5 pin even when the RST 7.5 interrupt is masked out.

The status of the three RST interrupt masks can only be affected by the SIM instruction and $\overline{\text{RESET IN}}$.

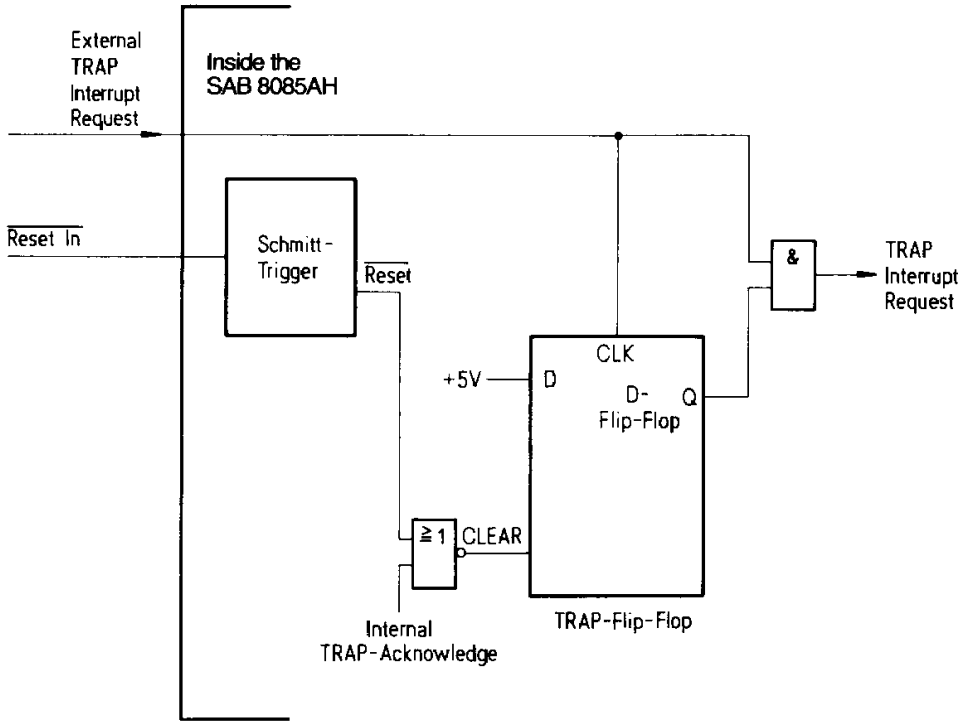
The interrupts are arranged in a fixed priority that determines which interrupt is to be recognized if more than one is pending as follows: TRAP – highest priority, RST 7.5, RST 6.5, RST 5.5, INTR – lowest priority. This priority scheme does not take into account the priority of a routine that was started by a higher priority interrupt. RST 5.5 can interrupt an RST 7.5 routine if the interrupts are re-enabled before the end of the RST 7.5 routine.

The TRAP interrupt is useful for catastrophic events such as power failure or bus error. The TRAP input is recognized just as any other interrupt but has the highest priority. It is not affected by any flag or mask. The TRAP input is both **edge and level sensitive**. The TRAP input must go high and remain high until it is acknowledged. It will not be recognized again until it goes low, then high again. This avoids any false triggering due to noise or logic glitches. The following figure illustrates the TRAP interrupt request circuitry within the SAB 8085AH. Note that the servicing of any interrupt (TRAP, RST 7.5, RST 6.5, RST 5.5, INTR) disables all future interrupts (except TRAPs) until an EI instruction is executed.

The TRAP interrupt is special in that it disables interrupts, but preserves the previous interrupt enable status. Performing the first RIM instruction following a TRAP interrupt allows you to determine whether interrupts were enabled or disabled prior to the TRAP. All subsequent RIM instructions provide current interrupt enable status. Performing a RIM instruction following INTR or RST 5.5 – 7.5 will provide current Interrupt Enable status, revealing that Interrupts are disabled.

The serial I/O system is also controlled by the RIM and SIM instructions. SID is read by RIM, and SIM sets the SOD data.

TRAP and RESET in Circuit



Driving the X_1 and X_2 Inputs

You may drive the clock inputs of the SAB 8085AH or SAB 8085AH-2 with a crystal, an LC tuned circuit, an RC network, or an external clock source. The driving frequency must be at least 1 MHz, and must be twice the desired internal clock frequency; hence, the SAB 8085AH is operated with a 6 MHz crystal (for 3 MHz clock), and the SAB 8085AH-2 can be operated with a 10 MHz crystal (for 5 MHz clock).

If a crystal is used, it must have the following characteristics:

Parallel resonance at twice the clock frequency desired

C_L (load capacitance) $\leq$ 30 pf
C_s (shunt capacitance) $\leq$ 7 pf
R_s (equivalent shunt resistance) $\leq$ 75 Ohms
Drive level: 10 mW
Frequency tolerance: $\pm$.005% (suggested)

Note the use of the 20 pF capacitor between X_2 and ground. This capacitor is required with crystal frequencies below 4 MHz to assure oscillator startup at the correct frequency. A parallel-resonant LC circuit may be used as the frequency-determining network for the SAB 8085AH, providing that its frequency tolerance of approximately $\pm$10% is acceptable. The components are from the formula:

$$f = \frac{1}{2\pi\sqrt{L\,(C_{ext} + C_{int})}}$$

To minimize variations in frequency, it is recommended that you choose a value for C_{ext} that is at least twice that of C_{int}, or 30 pF. The use of an LC circuit is not recommended for frequencies higher than approximately 5 MHz.

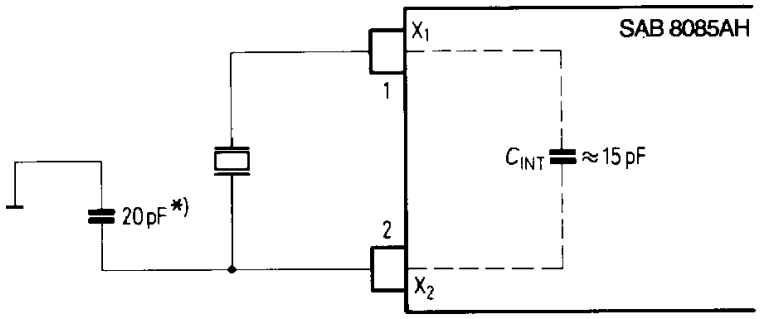
An RC circuit may be used as the frequency-determining network for the SAB 8085AH if maintaining a precise clock frequency is of no importance. Variations in the on-chip timing generation can cause a wide variation in frequency when using the RC mode. Its advantage is its low component costs. The driving frequency generated by the circuit shown is approximately 3 MHz. It is not recommended that frequencies greatly higher or lower than this be attempted.

The following figures show the recommended clock driver circuits. Note in D and E that pullup resistors are required to assure that the high level voltage of the input is at least 4V.

For driving frequencies up to and including 6 MHz you may supply the driving signal to X_1 and leave X_2 opencircuited (Figure D). If the driving frequency is from 6 MHz to 10 MHz, stability of the clock generator will be improved by driving both X_1 and X_2 with a pushpull source (Figure E). To prevent self-oscillation of the SAB 8085AH, be sure that X_2 is not coupled back to X_1 through the driving circuit.

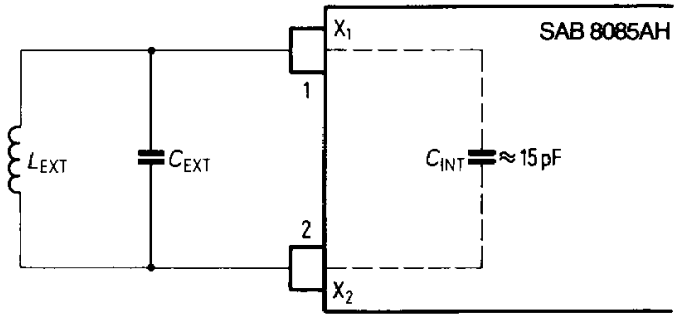
Clock Driver Circuits

A) Quartz Crystal Clock Driver

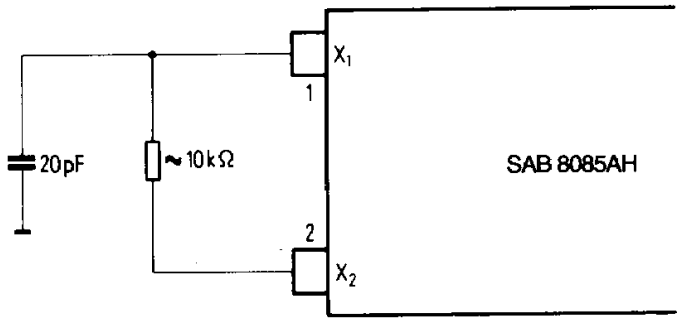


*) 20 pF Capacitors required for Crystal Frequency ≤ 4 MHz only.

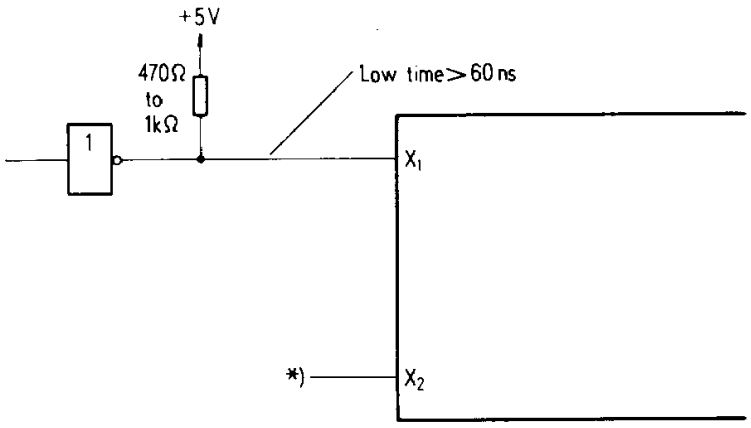
B) LC Tuned Circuit Clock Driver



C) RC Circuit Clock Driver

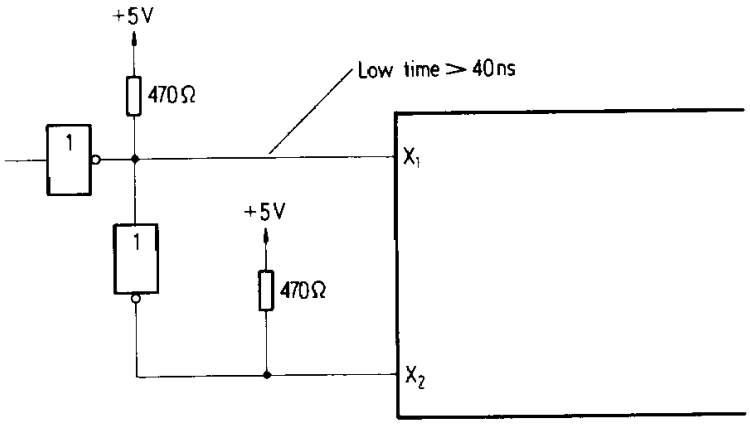


D) 1 – 6 MHz Input Frequency External Clock Driver Circuit



*) X_2 left floating

E) 1 – 10 MHz Input Frequency External Clock Driver Circuit



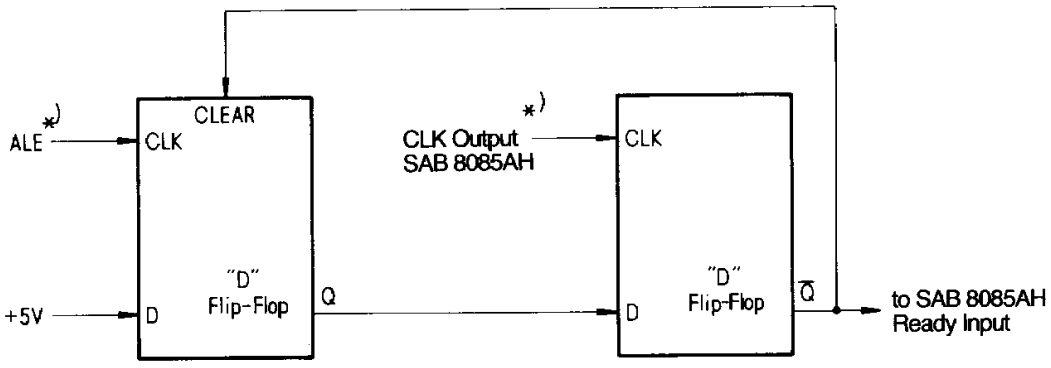
Generating Wait State

If your system requirements are such that slow memories or peripheral devices are being used, the circuit shown in the following figure may be used to insert one WAIT state in each SAB 8085AH machine cycle.

The D flip-flops should be chosen so that
- CLK is rising edge-triggered
- CLEAR is low-level active.

As in the SAB 8080, the READY line is used to extend the read and write pulse lengths so that the SAB 8085AH can be used with slow memory. HOLD causes the CPU to relinquish the bus when it is through with it by floating the Address and Data Buses.

Generation of a Wait State for SAB 8085AH CPU



*) ALE and CLK (Out) should be buffered if CLK Input of Latch Exceeds SAB 8085AH IOL or IOH.

System Interface

The SAB 8085A family includes memory components, which are directly compatible to the SAB 8085AH CPU. For example, a system consisting of the three chips, SAB 8085AH, SAB 8156, and SAB 8355 will have the following features:

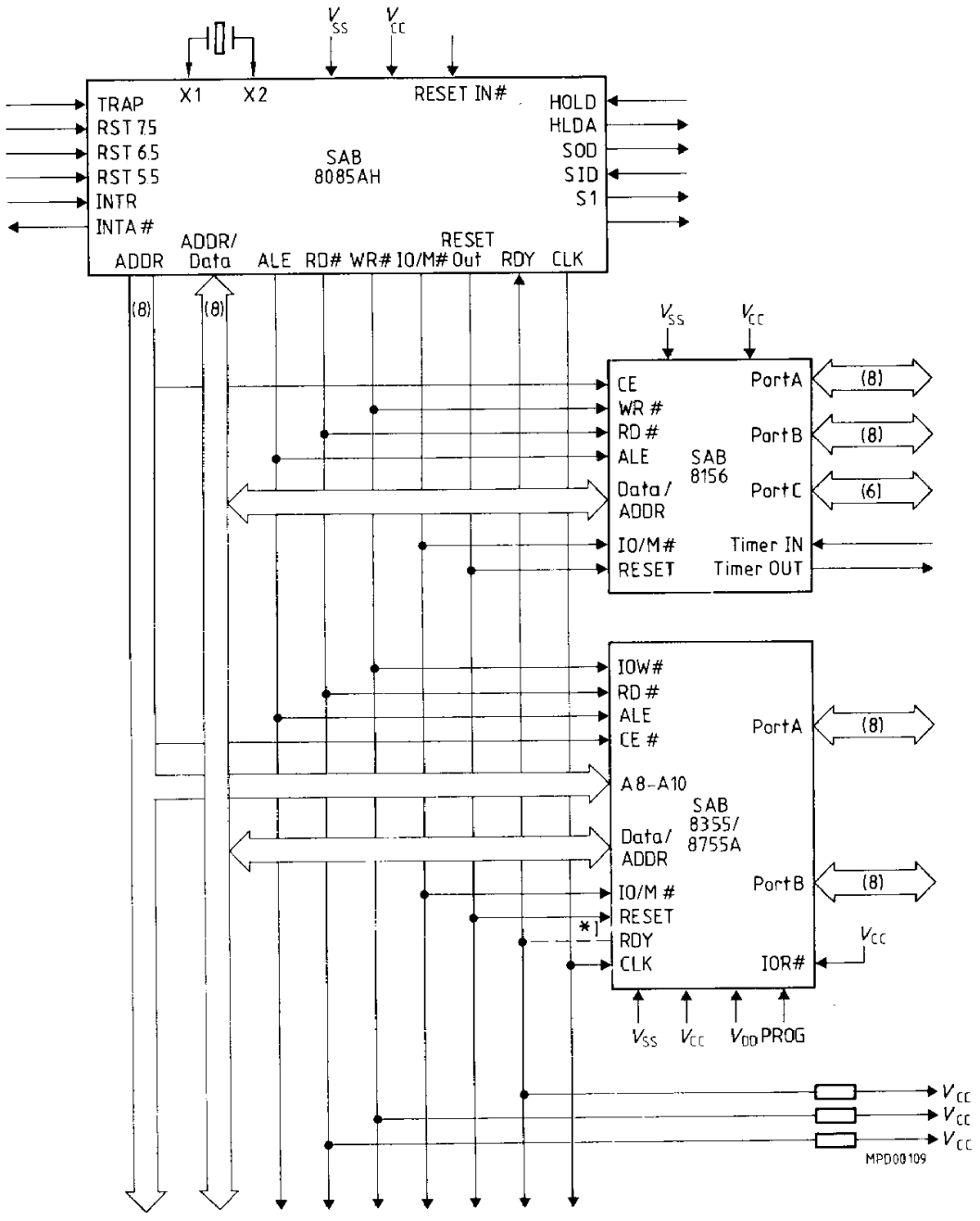
- 2K Bytes ROM
- 256 Bytes RAM
- 1 Timer/Counter
- 4 8-bit I/O Ports
- 1 6-bit I/O Port
- 4 Interrupt Levels
- Serial In/Serial Out Ports

This minimum system, using the standard I/O technique is as shown in the following figure.

In addition to standard I/O, the memory mapped I/O offers an efficient I/O addressing technique. With this technique, an area of memory address space is assigned for I/O address, thereby, using the memory address for I/O manipulation. The figure on page 11 shows the system configuration of Memory Mapped I/O using SAB 8085AH.

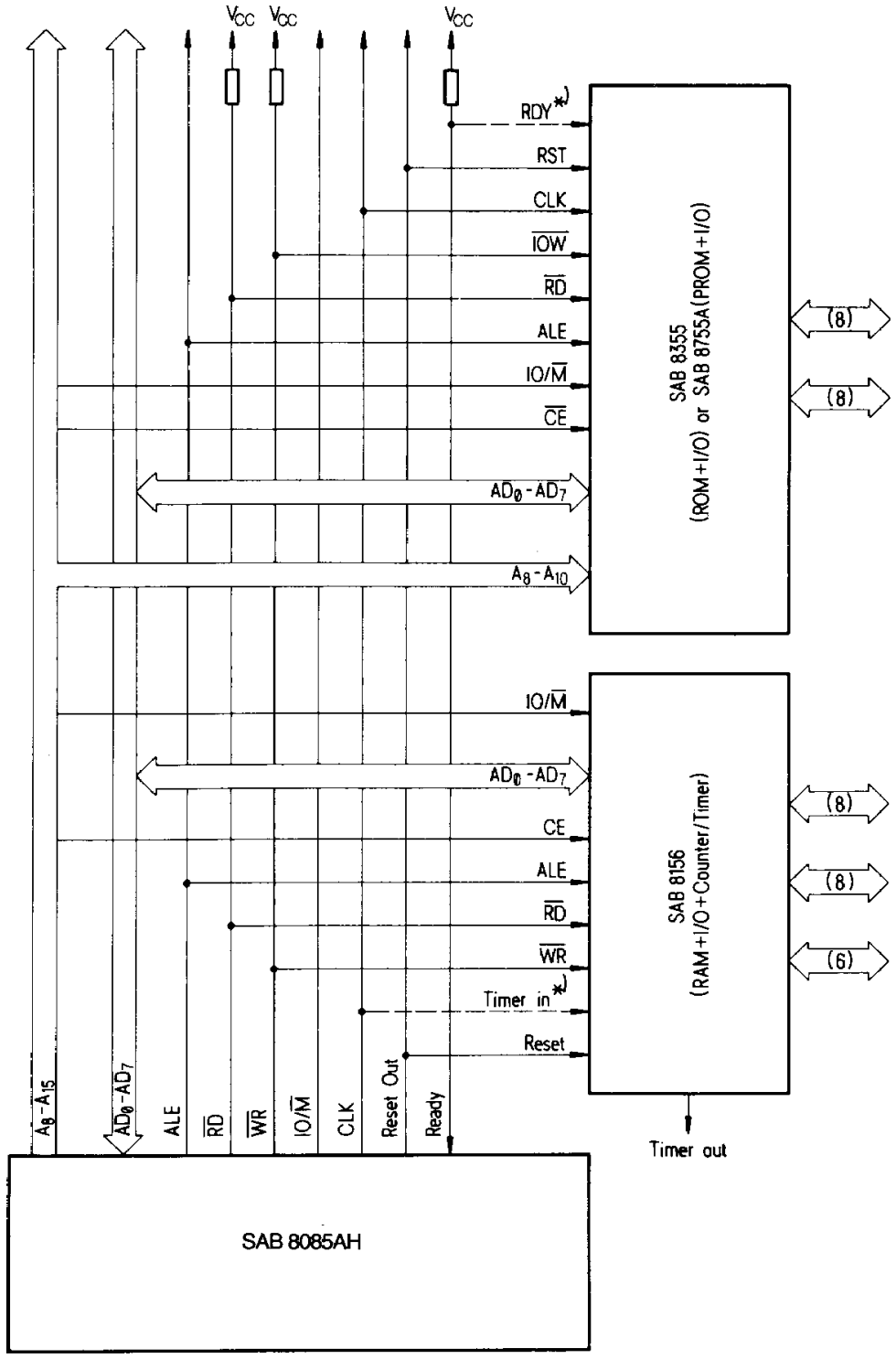
The SAB 8085AH CPU can also interface with the standard memory that does **not** have the multiplexed address/data bus. It will require a simple SAB 8282 (8-bit latch) as shown in the figure on page 12.

SAB 8085AH Minimum System (Standard I/O Technique)



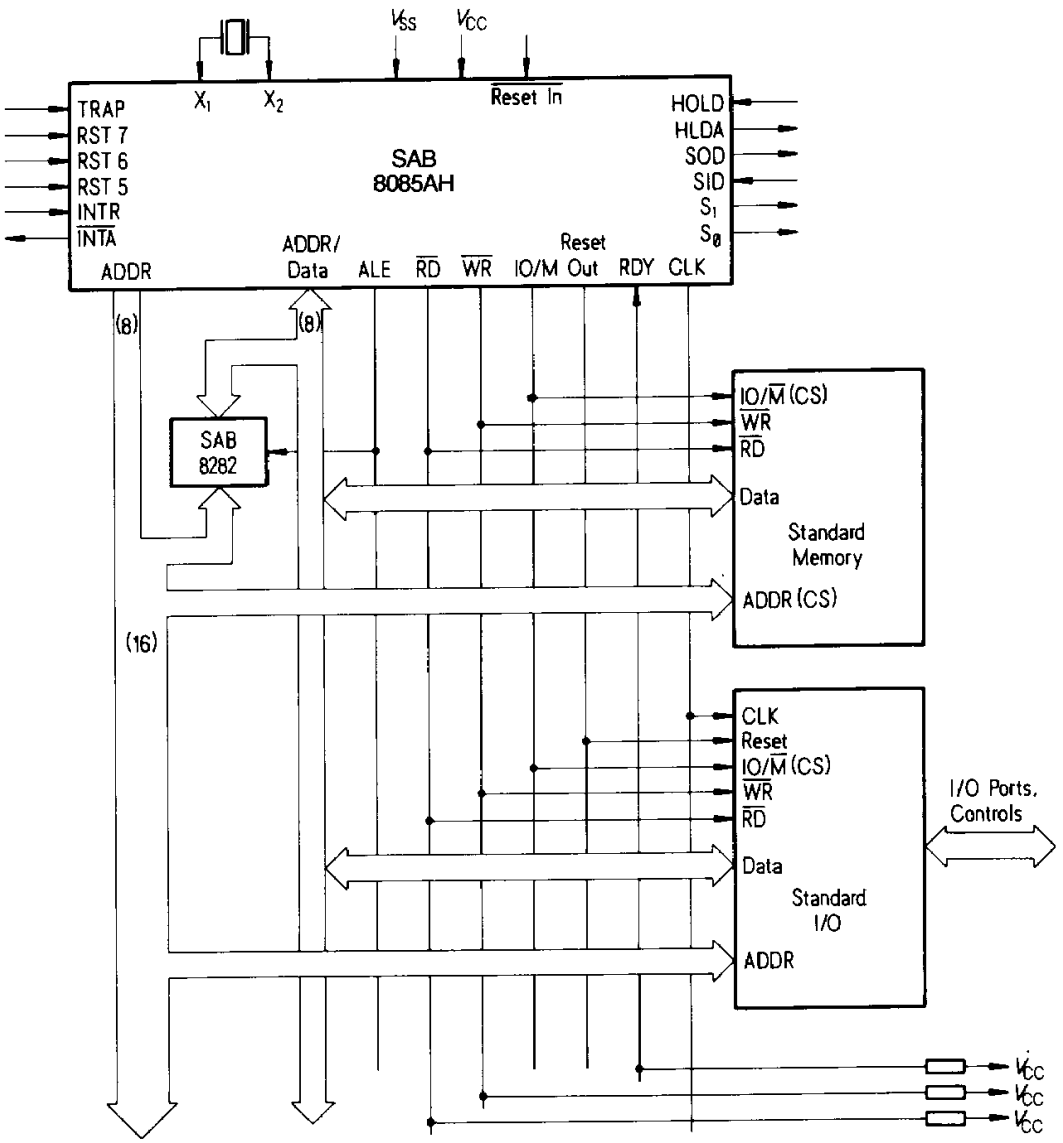
*) Optional Connection

SAB 8085AH Minimum System (Memory Mapped I/O)



*) Optional Connection

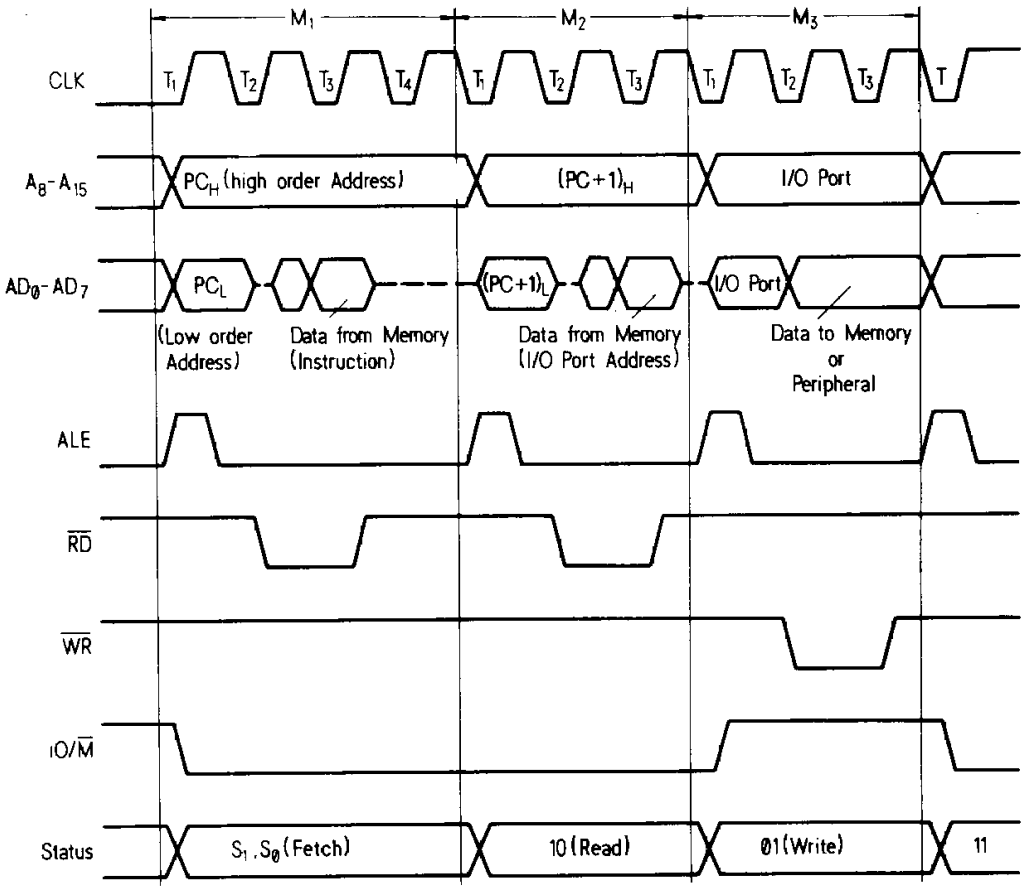
SAB 8085AH System (Using Standard Memories)



Basic System Timing

The SAB 8085AH has a multiplexed Data Bus. ALE is used as a strobe to sample the lower 8-bits of address on the Data Bus. The following figure shows an instruction fetch, memory read and I/O write cycle (as would occur during processing of the OUT instruction). Note that during the I/O write and read cycle that the I/O port address is copied on both, the upper and lower half of the address.

SAB 8085AH Basic System Timing



There are seven possible types of machine cycles. Which of these seven takes place is defined by the status of the three status lines (IO/$\overline{M}$, S_1, $S_\emptyset$) and the three control signals ($\overline{RD}$, $\overline{WR}$, and $\overline{INTA}$); (see following table). The status lines can be used as advanced controls (for device selection, for example), since they become active at the T_1 state, at the outset of each maching cycle. Control lines $\overline{RD}$ and $\overline{WR}$ become active later, at the time when the transfer of data is to take place, so are used as command lines.

SAB 8085AH Machine Cycle Chart

Machine Cycle		Status			Control		
		IO/$\overline{M}$	S1	SØ	$\overline{RD}$	$\overline{WR}$	$\overline{INTA}$
Opcode Fetch	(OF)	Ø	1	1	Ø	1	1
Memory Read		Ø	1	Ø	Ø	1	1
Memory Write		Ø	Ø	1	1	Ø	1
I/O Read	(IOR)	1	1	Ø	Ø	1	1
I/O Write	(IOW)	1	Ø	1	1	Ø	1
Acknowledge for INTR	(INA)	1	1	1	1	1	Ø
Bus Idle	(BI): DAD	Ø	1	Ø	1	1	1
	ACK of RST, TRAP	1	1	1	1	1	1
	HALT	TS	Ø	Ø	TS	TS	1

Ø = Logic "Ø"; 1 = Logic "1"; TS = High Impedance

A machine cycle normally consists of three T states, with the exception of OPCODE FETCH, which normally has either four or six T states (unless WAIT or HOLD states are forced by the receipt of $\overline{READY}$ or HOLD inputs). Any T state must be one of ten possible states, as summarized in the following table.

SAB 8085AH Machine State Chart

Machine State	Status and Buses				Control		
	S1, SØ	IO/$\overline{M}$	A_8–A_{15}	$AD_Ø$–AD_7	$\overline{RD}$, $\overline{WR}$	$\overline{INTA}$	ALE
T_1	X	X	X	X	1	1	1 [1]
T_2	X	X	X	X	X	X	Ø
T_{WAIT}	X	X	X	X	X	X	Ø
T_3	X	X	X	X	X	X	Ø
T_4	1	Ø [2]	X	TS	1	1	Ø
T_5	1	Ø [2]	X	TS	1	1	Ø
T_6	1	Ø [2]	X	TS	1	1	Ø
T_{RESET}	X	TS	TS	TS	TS	1	Ø
T_{HALT}	Ø	TS	TS	TS	TS	1	Ø
T_{HOLD}	X	TS	TS	TS	TS	1	Ø

Ø = Logic "Ø"; 1 = Logic "1"; TS = High Impedance; X = Unspecified.
[1]) ALE not generated during 2nd and 3nd machine cycles of DAD instruction.
[2]) IO/$\overline{M}$ = 1 during T_4–T_6 of INA machine cycle.

Instruction Set Summary

Mnemonic	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Operations Description
MOVE, LOAD, AND STORE									
MOVr1 r2	0	1	D	D	D	S	S	S	Move register to register
MOV M.r	0	1	1	1	0	S	S	S	Move register to memory
MOV r.M	0	1	D	D	D	1	1	0	Move memory to register
MVI r	0	0	D	D	D	1	1	0	Move immediate register
MVI M	0	0	1	1	0	1	1	0	Move immediate memory
LXI B	0	0	0	0	0	0	0	1	Load immediate register Pair B & C
LXI D	0	0	0	1	0	0	0	1	Load immediate register Pair D & E
LXI H	0	0	1	0	0	0	0	1	Load immediate register Pair H & L
STAX B	0	0	0	0	0	0	1	0	Store A indirect
STAX D	0	0	0	1	0	0	1	0	Store A indirect
LDAX B	0	0	0	0	1	0	1	0	Load A indirect
LDAX D	0	0	0	1	1	0	1	0	Load A indirect
STA	0	0	1	1	0	0	1	0	Store A direct
LDA	0	0	1	1	1	0	1	0	Load A direct
SHLD	0	0	1	0	0	0	1	0	Store H & L direct
LHLD	0	0	1	0	1	0	1	0	Load H & L direct
XCHG	1	1	1	0	1	0	1	1	Exchange D & E, H & L Registers
STACK OPS									
PUSH B	1	1	0	0	0	1	0	1	Push register Pair B & C on stack
PUSH D	1	1	0	1	0	1	0	1	Push register Pair D & E on stack
PUSH H	1	1	1	0	0	1	0	1	Push register Pair H & L on stack
PUSH PSW	1	1	1	1	0	1	0	1	Push A and Flags on stack
POP B	1	1	0	0	0	0	0	1	Pop register Pair B & C off stack
POP D	1	1	0	1	0	0	0	1	Pop register Pair D & E off stack
POP H	1	1	1	0	0	0	0	1	Pop register Pair H & L off stack
POP PSW	1	1	1	1	0	0	0	1	Pop A and Flags off stack
XTHL	1	1	1	0	0	0	1	1	Exchange top of stack, H & L
SPHL	1	1	1	1	1	0	0	1	H & L to stack pointer
LXI SP	0	0	1	1	0	0	0	1	Load immediate stack pointer
INX SP	0	0	1	1	0	0	1	1	Increment stack pointer
DCX SP	0	0	1	1	1	0	1	1	Decrement stack pointer
JUMP									
JMP	1	1	0	0	0	0	1	1	Jump unconditional
JC	1	1	0	1	1	0	1	0	Jump on carry
JNC	1	1	0	1	0	0	1	0	Jump on no carry
JZ	1	1	0	0	1	0	1	0	Jump on zero
JNZ	1	1	0	0	0	0	1	0	Jump on no zero
JP	1	1	1	1	0	0	1	0	Jump on positive
JM	1	1	1	1	1	0	1	0	Jump on minus
JPE	1	1	1	0	1	0	1	0	Jump on parity even
JPO	1	1	1	0	0	0	1	0	Jump on perity odd
PCHL	1	1	1	0	1	0	0	1	H & L to program counter

Instruction Set Summary (Cont'd)

Mnemonic	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Operations Description
CALL									
CALL	1	1	0	0	1	1	0	1	Call unconditional
CC	1	1	0	1	1	1	0	0	Call on carry
CNC	1	1	0	1	0	1	0	0	Call on no carry
CZ	1	1	0	0	1	1	0	0	Call on zerro
CNZ	1	1	0	0	0	1	0	0	Call on no zerro
CP	1	1	1	1	0	1	0	0	Call on positive
CM	1	1	1	1	1	1	0	0	Call on minus
CPE	1	1	1	0	1	1	0	0	Call on parity even
CPO	1	1	1	0	0	1	0	0	Call on parity odd
RETURN									
RET	1	1	0	0	1	0	0	1	Return
RC	1	1	0	1	1	0	0	0	Return on carry
RNC	1	1	0	1	0	0	0	0	Return on no carry
RZ	1	1	0	0	1	0	0	0	Return on zero
RNZ	1	1	0	0	0	0	0	0	Return on no zero
RP	1	1	1	1	0	0	0	0	Return on positive
RM	1	1	1	1	1	0	0	0	Return on minus
RPE	1	1	1	0	1	0	0	0	Return on parity even
RPO	1	1	1	0	0	0	0	0	Return on parity odd
RESTART									
RST	1	1	A	A	A	1	1	1	Restart
INPUT/OUTPUT									
IN	1	1	0	1	1	0	1	1	Input
OUT	1	1	0	1	0	0	1	1	Output
INCREMENT AND DECREMENT									
INR r	0	0	D	D	D	1	0	0	Increment register
DCR r	0	0	D	D	D	1	0	1	Decrement register
INR M	0	0	1	1	0	1	0	0	Increment memory
DCR M	0	0	1	1	0	1	0	1	Decrement memory
INX B	0	0	0	0	0	0	1	1	Increment B & C registers
INX D	0	0	0	1	0	0	1	1	Increment D & E registers
INX H	0	0	1	0	0	0	1	1	Increment H & L registers
DCX B	0	0	0	0	1	0	1	1	Decrement B & C
DCX D	0	0	0	1	1	0	1	1	Decrement D & E
DCX H	0	0	1	0	1	0	1	1	Decrement H & L
ADD									
ADD r	1	0	0	0	0	S	S	S	Add register to A
ADC r	1	0	0	0	1	S	S	S	Add register to A with carry
ADD M	1	0	C	0	0	1	1	0	Add memory to A
ADC M	1	0	0	0	1	1	1	0	Add memory to A with carry
ADI	1	1	0	0	0	1	1	0	Add immediate to A
ACI	1	1	0	0	1	1	1	0	Add immediate to A with carry
DAD B	0	0	0	0	1	0	0	1	Add B & C to H & L
DAD D	0	0	0	1	1	0	0	1	Add D & E to H & L
DAD H	0	0	1	0	1	0	0	1	Add H & L to H & L
DAD SP	0	0	1	1	1	0	0	1	Add stack pointer to H & L

Instruction Set Summary (Cont'd)

Mnemonic	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Operations Description
SUBTRACT									
SUB r	1	0	0	1	0	S	S	S	Subtract register from A
SBB r	1	0	0	1	1	S	S	S	Subtract register from A with borrow
SUB M	1	0	0	1	0	1	1	0	Subtract memory from A
SBB M	1	0	0	1	1	1	1	0	Subtract memory from A with borrow
SUI	1	1	0	1	0	1	1	0	Subtract immediate from A
SBI	1	1	0	1	1	1	1	0	Subtract immediate from A with borrow
LOGICAL									
ANA r	1	0	1	0	0	S	S	S	And register with A
XRA r	1	0	1	0	1	S	S	S	Exclusive OR register with A
ORA r	1	0	1	1	0	S	S	S	OR register with A
CMP r	1	0	1	1	1	S	S	S	Compare register with A
ANA M	1	0	1	0	0	1	1	0	And memory with A
XRA M	1	0	1	0	1	1	1	0	Exclusive OR memory with A
ORA M	1	0	1	1	0	1	1	0	OR memory with A
CMP M	1	0	1	1	1	1	1	0	Compare memory with A
ANI	1	1	1	0	0	1	1	0	And immediate with A
XRI	1	1	1	0	1	1	1	0	Exclusive OR immediate with A
ORI	1	1	1	1	0	1	1	0	OR immediate with A
CPI	1	1	1	1	1	1	1	0	Compare immediate with A
ROTATE									
RLC	0	0	0	0	0	1	1	1	Rotate A left
RRC	0	0	0	0	1	1	1	1	Rotate A right
RAL	0	0	0	1	0	1	1	1	Rotate A left throught carry
RAR	0	0	0	1	1	1	1	1	Rotate A right through carry
SPECIALS									
CMA	0	0	1	0	1	1	1	1	Complement A
STC	0	0	1	1	0	1	1	1	Set carry
CMC	0	0	1	1	1	1	1	1	Complement carry
DAA	0	0	1	0	0	1	1	1	Decimal adjust A
CONTROL									
EI	1	1	1	1	1	0	1	1	Enable interrupts
DI	1	1	1	1	0	0	1	1	Disable Interrupt
NOP	0	0	0	0	0	0	0	0	No-operation
HLT	0	1	1	1	0	1	1	0	Halt
NEW SAB 8085AH INSTRUCTIONS									
RIM	0	0	1	0	0	0	0	0	Read Interrupt Mask
SIM	0	0	1	1	0	0	0	0	Set Interrupt Mask

NOTES
1. DDS or SSS: B 000, C 001, D 010, E 011, H 100, L 101, Memory 110, A 111.
2. Two possible cycle times (6/12) indicate instruction cycles dependent on condition flags.

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Absolute maximum ratings *)

Ambient Temperature Under Bias	0 to 70°C
Storage Temperature	−65 to +150°C
Voltage on any Pin with Respect to Ground	−0.5 to +7 V
Power Dissipation	1.5 Watt

D.C. Characteristics

T_A = 0 to 70°C; V_{CC} = 5 V ±10%; V_{SS} = 0 V; (unless otherwise specified)

Symbol	Parameter	Limit Values		Units	Test Conditions
		Min.	Max.		
V_{IL}	Input Low Voltage	−0.5	+0.8	V	–
V_{IH}	Input High Voltage	2.0	V_{CC}+0.5		
V_{OL}	Output Low Voltage	–	0.45		I_{OL} = 2 mA
V_{OH}	Output High Voltage	2.4	–		I_{OH} = −400 µA
I_{CC}	Power Supply Current	–	120	mA	–
I_{IL}	Input Leakage		±10	µA	$0 \lesssim V_{IN} \lesssim V_{CC}$
I_{LO}	Output Leakage				0.45 V $\leq V_{OUT} \leq V_{CC}$
V_{ILR}	Input Low Level, RESET	−0.5	+0.8	V	–
V_{IHR}	Input High Level, RESET	2.4	V_{CC}+0.5		
V_{HY}	Hysteresis, RESET	0.25			

*) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

A.C. Characteristics

T_A = 0 to 70°C; V_{CC} = 5 V ± 10%; V_{SS} = 0 V

Symbol	Parameter	Limit Values				Units
		SAB 8085AH-2 [2]		SAB 8085AH [2]		
		Min.	Max.	Min.	Max.	
t_{CYC}	CLK Cycle Period	320	2000	200	2000	
t_1	CLK Low Time (Standard CLK Loading)	80	–	40	–	
t_2	CLK High Time Standard CLK Loading)	120		70		
t_r, t_f	CLK Rise and Fall Time		30	–	30	
t_{XKR}	X_1 Rising to CLK Rising	30	120	30	100	
t_{XKF}	X_1 Rising to CLK Falling		150		110	
t_{AC}	A_8–A_{15} Valid to Leading Edge of Control [1]	270	–	115	–	
t_{ACL}	A_0–A_7 Valid to Leading Edge of Control	240				
t_{AD}	A_0–A_{15} Valid to Valid Data In	–	575	–	350	
t_{AFR}	Address Float After Leading Edge of $\overline{READ}$ ($\overline{INTA}$)		0		0	
t_{AL}	A_8–A_{15} Valid Before Trailing Edge of ALE [1]	115	–	50	–	
t_{ALL}	A_0–A_7 Valid Before Trailing Edge of ALE	90				
t_{ARY}	READY Valid from Address Valid	–	220	–	100	ns
t_{CA}	Address (A_8–A_{15}) Valid After Control	120	–	60	–	
t_{CC}	Width of Control Low ($\overline{RD}$, $\overline{WR}$, $\overline{INTA}$)	400		230		
t_{CL}	Trailing Edge of Control to Leading Edge of ALE	50		25		
t_{DW}	Data Valid to Trailing Edge of $\overline{WRITE}$	420		230		
t_{HABE}	HLDA to Bus Enable	–	210	–	150	
t_{HABF}	Bus Float After HLDA					
t_{HACK}	HLDA Valid to Trailing Edge of CLK	110	–	40	–	
t_{HDH}	HOLD Hold Time	0		0		
t_{HDS}	HOLD Setup Time to Trailing Edge of CLK	170		120		
t_{INH}	INTR Hold Time	0		0		
t_{INS}	INTR, RST, and TRAP Setup Time to Falling Edge of CLK	160		150		
t_{LA}	Address Hold Time After ALE	100		50		
t_{LC}	Trailing Edge of ALE to Leading Edge of Control	130		60		
t_{LCK}	ALE Low During CLK High	100		50		

Notes see next page.

A.C. Characteristics (continued)

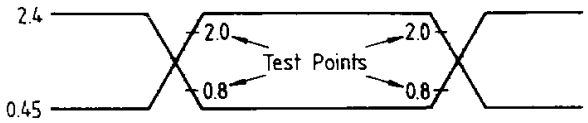
Symbol	Parameter	Limit Values				Units
		SAB 8085AH[2]		SAB 8085AH-2[2]		
		Min.	Max.	Min.	Max.	
t_{LDR}	ALE to Valid Data During Read	–	460	–	270	ns
t_{LDW}	ALE to Valid Data During Write		200		120	
t_{LL}	ALE Width	140	–	80	–	
t_{LRY}	ALE to READY Stable	–	110	–	30	
t_{RAE}	Trailing Edge of $\overline{READ}$ to Re-Enabling of Address	150	–	90	–	
t_{RD}	$\overline{READ}$ (or $\overline{INTA}$) to Valid Data	–	300	–	150	
t_{RV}	Control Trailing Edge to Leading Edge of Next Control	400	–	220	–	
t_{RDH}	Data Hold Time After $\overline{READ}$ $\overline{INTA}$[7]	0		0		ns
t_{RYH}	READY Hold Time					
t_{RYS}	READY Setup Time to Leading Edge of CLK	110		100		
t_{WD}	Data Valid After Trailing Edge of $\overline{WRITE}$	100		60		
t_{WDL}	LEADING Edge of WRITE to Data Valid	–	40	–	20	

NOTES

1. A_8–A_{15} address Specs apply to IO/$\overline{M}$, $S_\emptyset$, and S_1 except A_8–A_{15} are undefined during T_4–T_6 of OF cycle, whereas IO/$\overline{M}$, $S_\emptyset$, and S_1 are stable.
2. **Test conditions:** t_{CYC} = 320 ns (SAB 8085AH)/200 ns (SAB 8085AH-2); C_L = 150 pF.
3. For all output timing where C_L = 150 pF use the following correction factors:
   25 pF $\leq C_L <$ 150 pF: −0.10 ns/pF
   150 pF $< C_L \leq$ 300 pF: +0.30 ns/pF
4. Output timings are measured with purely capacitive load.
5. All timings are measured at output votage V_L = 0.8V, V_H = 2.0V, and 1.5V with 20 ns rise and fall time on inputs.
6. To calculate timing specifications at other values of t_{CYC} the following table should be used.
7. Data hold time is guaranteed under all loading conditions.

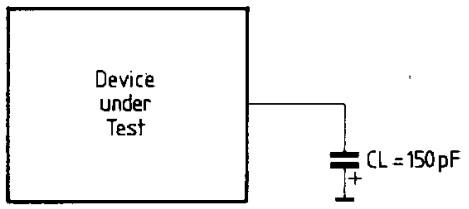
A.C. Testing

Input, Output Waveform



A.C. Testing: Input are driven at 2.4 V for a Logic "1" and 0.45 V for a Logic "0".
Timing Measurements are made at 2.0 V for a Logic "1" and 0.8 V for a Logic "0".

Load Circuit



C_L = 150 pF
C_L = includes JIG Capacitance

Bus Timing Specification as a t_{CYC} Dependent

SAB 8085AH

Symb.	Min.	Max.
t_{AL}	(1/2) T − 45	–
t_{LA}	(1/2) T − 60	
t_{LL}	(1/2) T − 20	
t_{LCK}	(1/2) T − 60	
t_{LC}	(1/2) T − 30	
t_{AD}	–	(5/2 + N) T − 225
t_{RD}		(3/2 + N) T − 180
t_{RAE}	(1/2) T − 10	–
t_{CA}	(1/2) T − 40	
t_{DW}	(3/2 + N) T − 60	
t_{WD}	(1/2) T − 60	
t_{CC}	(3/2 + N) T − 80	
t_{CL}	(1/2) T − 110	
t_{ARY}	–	(3/2) T − 260
t_{HACK}	(1/2) T − 50	–
t_{HABF}	–	(1/2) T + 50
t_{HABE}		(1/2) T + 50
t_{AC}	(2/2) T − 50	–
t_1	(1/2) T − 80	
t_2	(1/2) T − 40	
t_{RV}	(3/2) T − 80	
t_{LDR}	–	(4/2) T − 180

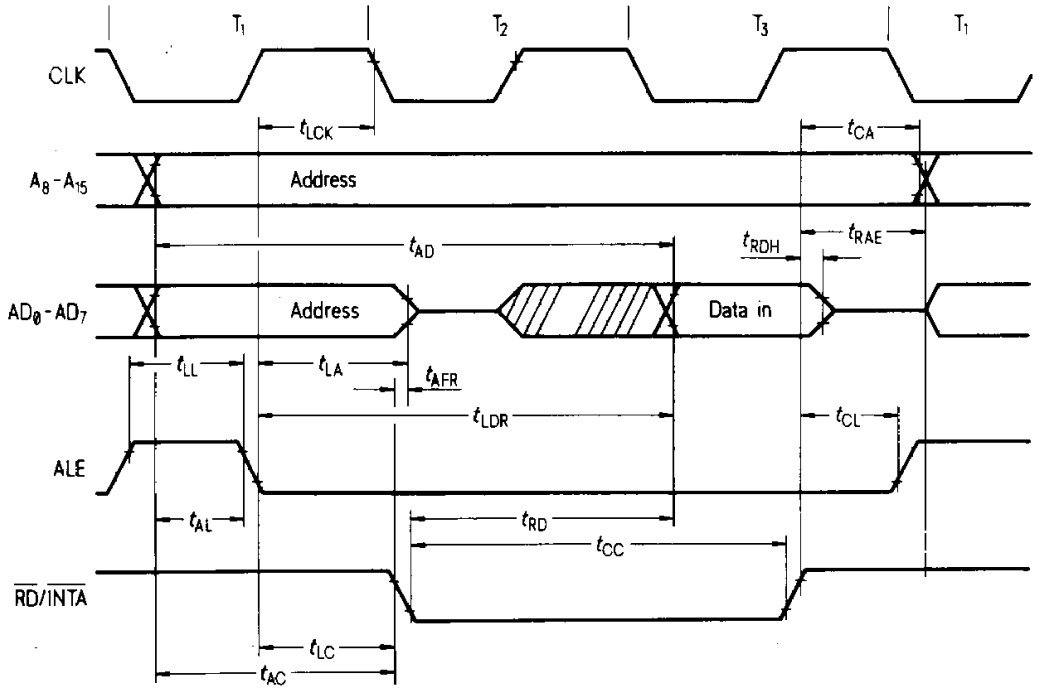
SAB 8085AH-2

Symb.	Min.	Max.
t_{AL}	(1/2) T − 50	–
t_{LA}	(1/2) T − 50	
t_{LL}	(1/2) T − 20	
t_{LCK}	(1/2) T − 50	
t_{LC}	(1/2) T − 40	
t_{AD}	–	(5/2 + N) T − 150
t_{RD}		(3/2 + N) T − 150
t_{RAE}	(1/2) T − 10	–
t_{CA}	(1/2) T − 40	
t_{DW}	(3/2 + N) T − 70	
t_{WD}	(1/2) T − 40	
t_{CC}	(3/2 + N) T − 70	
t_{CL}	(1/2) T − 75	
t_{ARY}	–	(3/2) T − 200
t_{HACK}	(1/2) T − 60	–
t_{HABF}	–	(1/2) T + 50
t_{HABE}		(1/2) T + 50
t_{AC}	(2/2) T − 85	–
t_1	(1/2) T − 60	
t_2	(1/2) T − 30	
t_{RV}	(3/2) T − 80	
t_{LDR}	–	(4/2) T − 130

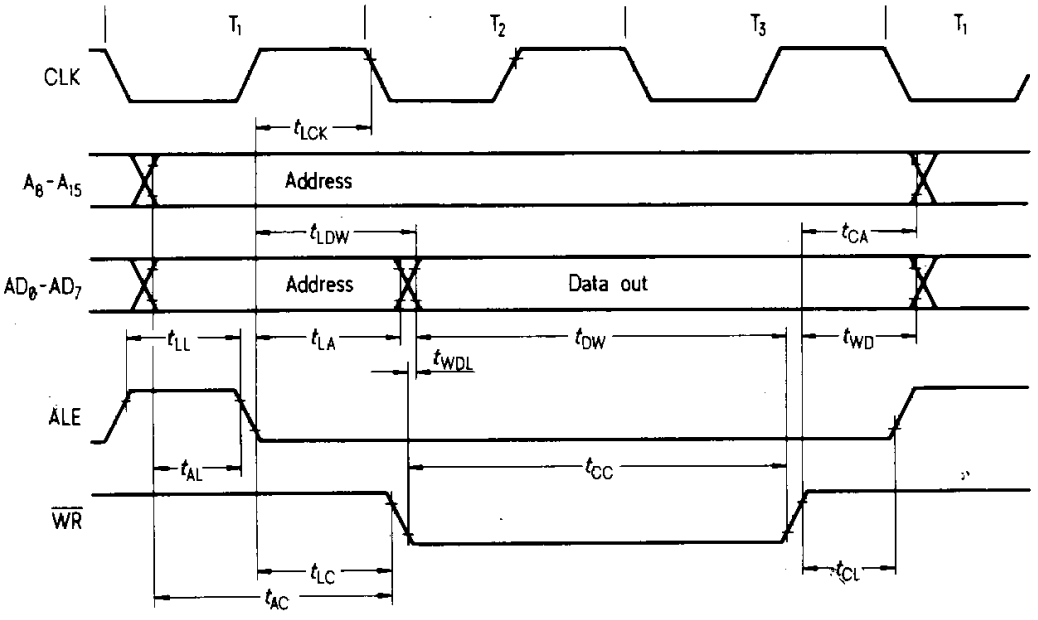
N is equal to the total WAIT states. T = t_{CYC}.

Waveforms

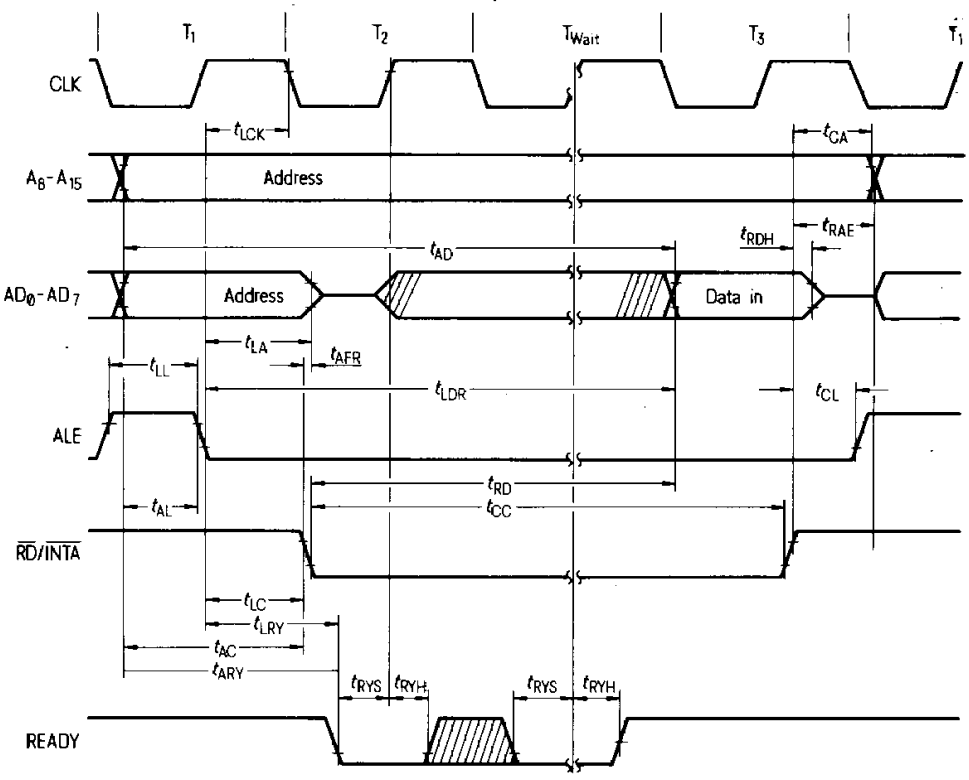
Read



Write

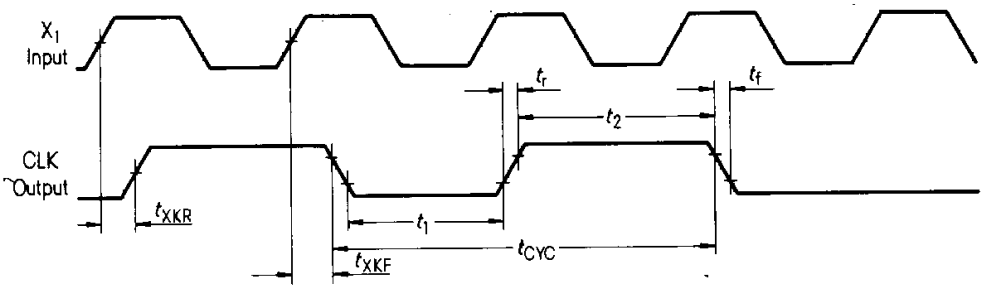


Read Operation with Cycle (Typical) – Same Ready Timing Applies to Write

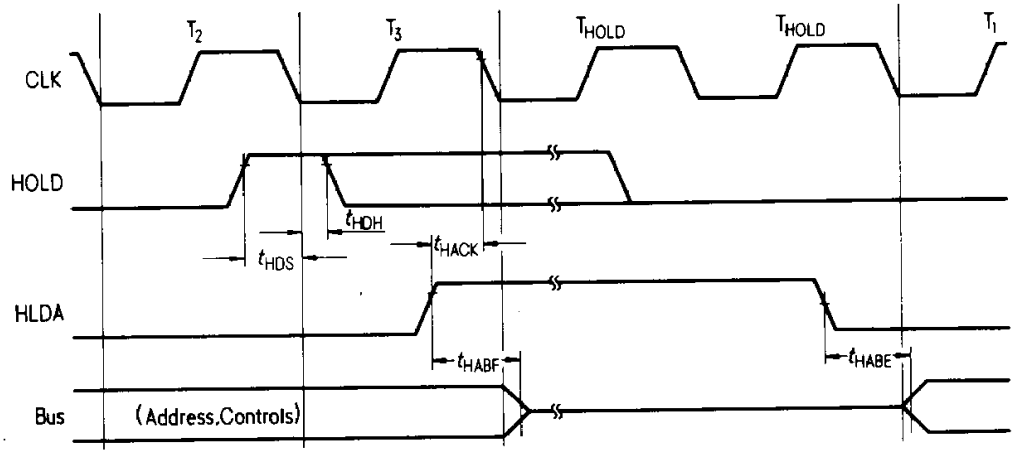


READY must remain stable during setup and hold times.

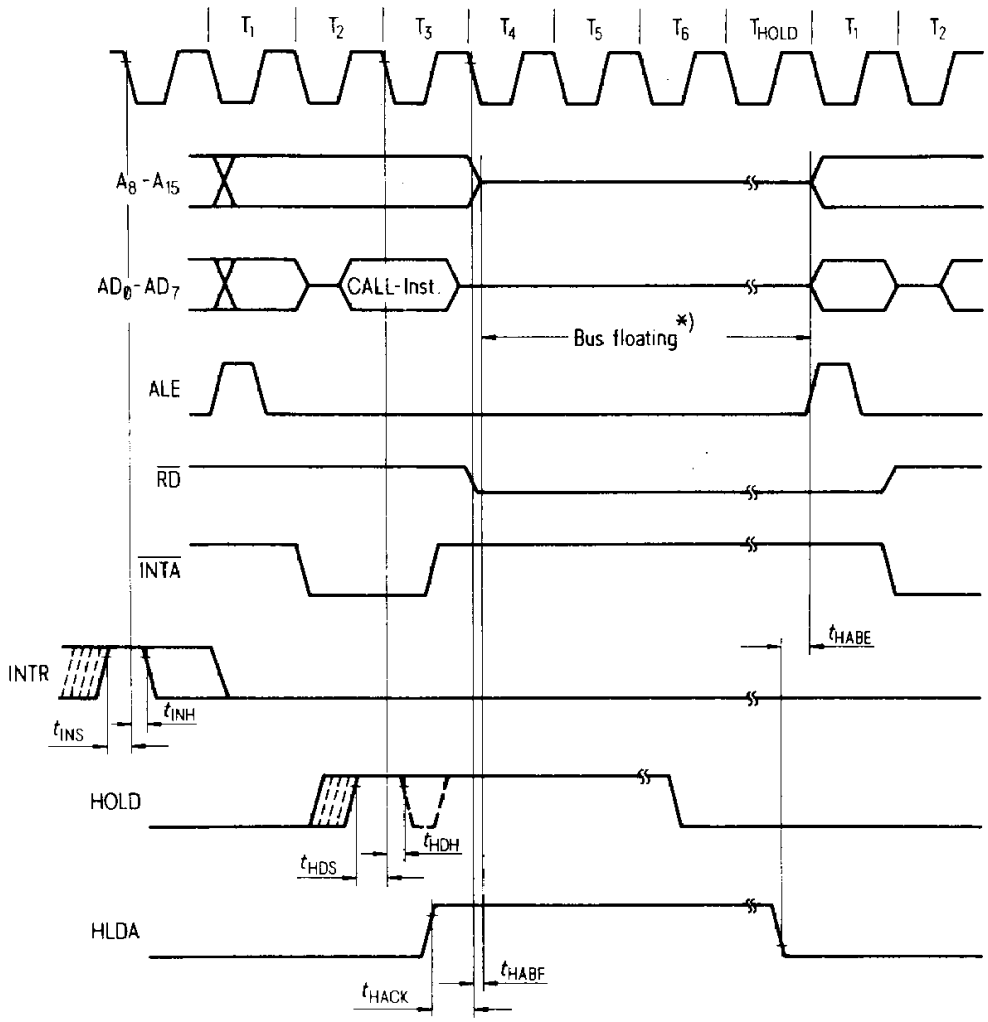
Clock


X1
Input
CLK
Output
tr
tf
t2
tXKR
t1
tXKF
tCYC

Hold


T2
T3
THOLD
THOLD
T1
CLK
HOLD
tHDH
tHDS
tHACK
HLDA
tHABF
tHABE
Bus
(Address,Controls)

Interrupt and Hold



*) IO/$\overline{M}$ is also floating during this time.

Ordering Information

Component	Description	Ordering Number
	8-Bit Microprocessor	
SAB 8085AH-P	3 MHz, 1.3 µs, (plastic)	Q 67120-C122
SAB 8085AH-2-P	5 MHz, 0.8 µs, (plastic)	Q 67120-C124

Edition 10.90

Published by Siemens AG, Bereich Halbleiter, Marketing-Kommunikation
Balanstraße 73, D-8000 München 80.

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