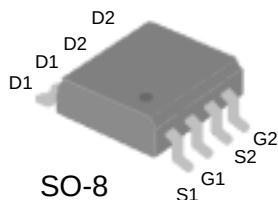


COMPLEMENTARY N AND P-CHANNEL ENHANCEMENT-MODE POWER MOSFETS

Simple drive requirement

Low on-resistance

Fast switching

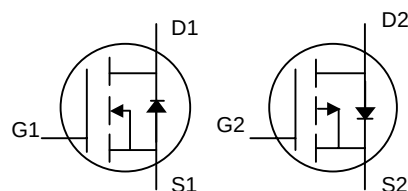


N-ch	BV_{DSS}	+30V
	$R_{DS(ON)}$	50m Ω
	I_D	+5A
P-ch	BV_{DSS}	-30V
	$R_{DS(ON)}$	70m Ω
	I_D	-4A

Description

MOSFETs from Silicon Standard Corp. provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The SO-8 package is widely preferred for commercial and industrial surface mount applications and is well suited for low-voltage applications such as DC/DC converters.



Absolute Maximum Ratings

Symbol	Parameter	Rating		Units
		N-channel	P-channel	
V_{DS}	Drain-Source Voltage	+30	-30	V
V_{GS}	Gate-Source Voltage	± 20	± 20	V
$I_D @ T_A=25^\circ\text{C}$	Continuous Drain Current ³	+5	-4	A
$I_D @ T_A=70^\circ\text{C}$	Continuous Drain Current ³	+4	-3.2	A
I_{DM}	Pulsed Drain Current ^{1,4}	+20	-20	A
$P_D @ T_A=25^\circ\text{C}$	Total Power Dissipation	2.0		W
	Linear Derating Factor	0.016		W/ $^\circ\text{C}$
T_{STG}	Storage Temperature Range	-55 to 150		$^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150		$^\circ\text{C}$

Thermal Data

Symbol	Parameter	Value	Unit
$R_{thj-amb}$	Thermal Resistance Junction-ambient	Max. 62.5	$^\circ\text{C/W}$

N-channel Electrical Characteristics @ $T_j=25^{\circ}\text{C}$ (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	30	-	-	V
$\Delta BV_{DSS}/\Delta T_j$	Breakdown Voltage Temperature Coefficient	Reference to 25°C , $I_D=1\text{mA}$	-	0.037	-	V/ $^{\circ}\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=10V, I_D=5A$	-	-	50	$\text{m}\Omega$
		$V_{GS}=4.5V, I_D=4.2A$	-	-	70	$\text{m}\Omega$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	1	-	3	V
g_{fs}	Forward Transconductance	$V_{DS}=10V, I_D=5A$	-	8	-	S
I_{DSS}	Drain-Source Leakage Current ($T_j=25^{\circ}\text{C}$)	$V_{DS}=30V, V_{GS}=0V$	-	-	1	μA
	Drain-Source Leakage Current ($T_j=55^{\circ}\text{C}$)	$V_{DS}=24V, V_{GS}=0V$	-	-	25	μA
I_{GSS}	Gate-Source Leakage	$V_{GS}=\pm 20V$	-	-	± 100	nA
Q_g	Total Gate Charge ²	$I_D=5A$	-	10.2	20	nC
Q_{gs}	Gate-Source Charge	$V_{DS}=10V$	-	1.2	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	$V_{GS}=10V$	-	3.4	-	nC
$t_{d(on)}$	Turn-on Delay Time ²	$V_{DS}=10V$	-	6	12	ns
t_r	Rise Time	$I_D=1A$	-	9	18	ns
$t_{d(off)}$	Turn-off Delay Time	$R_G=6\Omega, V_{GS}=10V$	-	15	30	ns
t_f	Fall Time	$R_D=10\Omega$	-	5.5	12	ns
C_{iss}	Input Capacitance	$V_{GS}=0V$	-	240	360	pF
C_{oss}	Output Capacitance	$V_{DS}=25V$	-	145	210	pF
C_{rss}	Reverse Transfer Capacitance	$f=1.0\text{MHz}$	-	55	80	pF

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
I_S	Continuous Source Current (Body Diode)	$V_D=V_G=0V, V_S=1.2V$	-	-	1.7	A
I_{SM}	Pulsed Source Current (Body Diode) ¹		-	-	20	A
V_{SD}	Forward On Voltage ²	$T_j=25^{\circ}\text{C}, I_S=1.7A, V_{GS}=0V$	-	0.8	1.2	V

Notes:

1. Pulse width limited by max. junction temperature.
2. Pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.
3. Surface mounted on FR4 board, $t \leq 10\text{sec}$.
4. Pulse width $\leq 10\mu s$, duty cycle $\leq 1\%$.

P-channel Electrical Characteristics @ $T_j=25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	-30	-	-	V
$\Delta BV_{DSS}/\Delta T_j$	Breakdown Voltage Temperature Coefficient	Reference to 25°C , $I_D=-1mA$	-	-0.028	-	$V/^\circ\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=-10V, I_D=-4A$	-	-	70	$m\Omega$
		$V_{GS}=-4.5V, I_D=-3A$	-	-	90	$m\Omega$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1	-	-3	V
g_{fs}	Forward Transconductance	$V_{DS}=-10V, I_D=-4A$	-	5	-	S
I_{DSS}	Drain-Source Leakage Current ($T_j=25^\circ\text{C}$)	$V_{DS}=-30V, V_{GS}=0V$	-	-	-1	μA
	Drain-Source Leakage Current ($T_j=55^\circ\text{C}$)	$V_{DS}=-24V, V_{GS}=0V$	-	-	-25	μA
I_{GSS}	Gate-Source Leakage	$V_{GS}=\pm 20V$	-	-	± 100	nA
Q_g	Total Gate Charge ²	$I_D=-4A$	-	18.3	36	nC
Q_{gs}	Gate-Source Charge	$V_{DS}=-10V$	-	3.6	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	$V_{GS}=-10V$	-	1.5	-	nC
$t_{d(on)}$	Turn-on Delay Time ²	$V_{DS}=-10V$	-	8	16	ns
t_r	Rise Time	$I_D=-1A$	-	9	18	ns
$t_{d(off)}$	Turn-off Delay Time	$R_G=6\Omega, V_{GS}=-10V$	-	21	40	ns
t_f	Fall Time	$R_D=10\Omega$	-	10	20	ns
C_{iss}	Input Capacitance	$V_{GS}=0V$	-	760	1140	pF
C_{oss}	Output Capacitance	$V_{DS}=-25V$	-	345	518	pF
C_{rss}	Reverse Transfer Capacitance	$f=1.0MHz$	-	90	135	pF

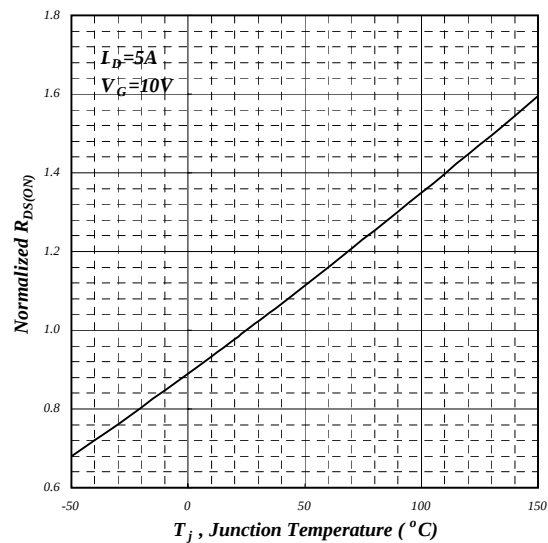
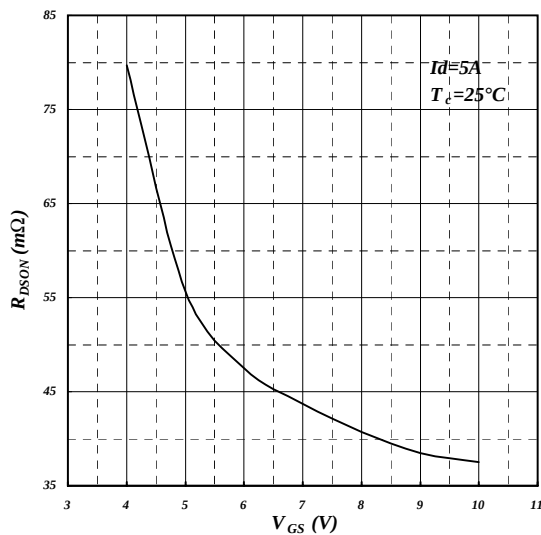
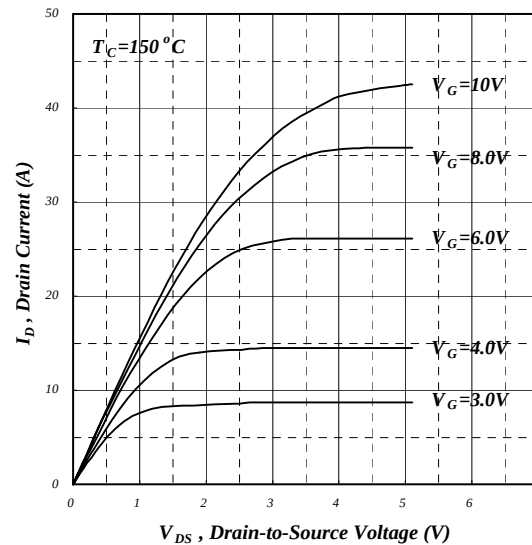
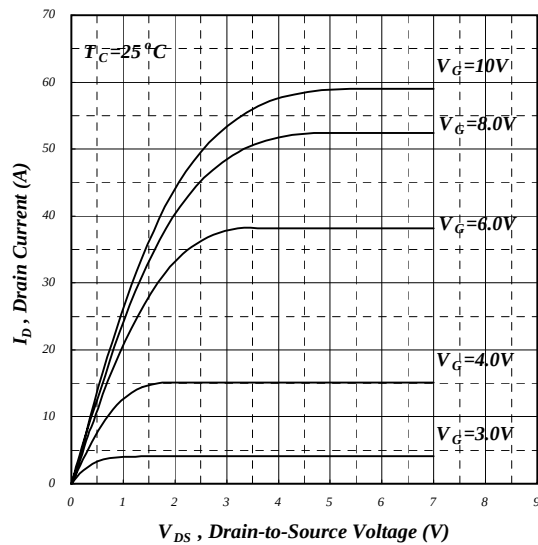
Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
I_S	Continuous Source Current (Body Diode)	$V_D=V_G=0V, V_S=-1.2V$	-	-	-1.7	A
I_{SM}	Pulsed Source Current (Body Diode) ¹		-	-	-20	A
V_{SD}	Forward On Voltage ²	$T_j=25^\circ\text{C}, I_S=-1.7A, V_{GS}=0V$	-	-	-1.2	V

Notes:

- 1.Pulse width limited by max. junction temperature.
- 2.Pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.
- 3.Surface mounted on FR4 board, $t \leq 10\text{sec}$.
- 4.Pulse width $\leq 10\mu s$, duty cycle $\leq 1\%$.

N-channel



N-channel

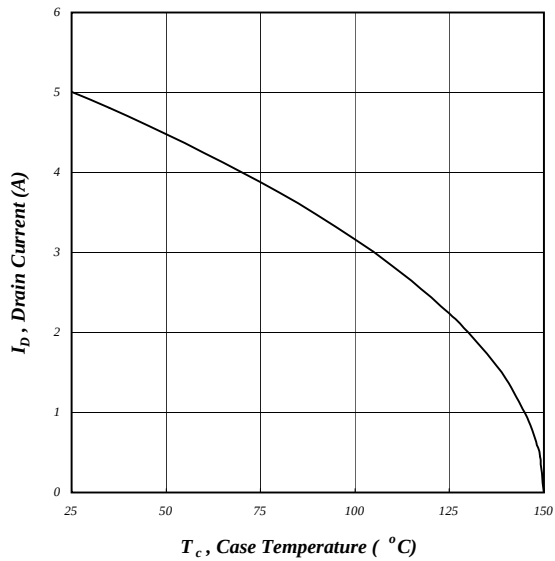


Fig 5. Maximum Drain Current vs. Case Temperature

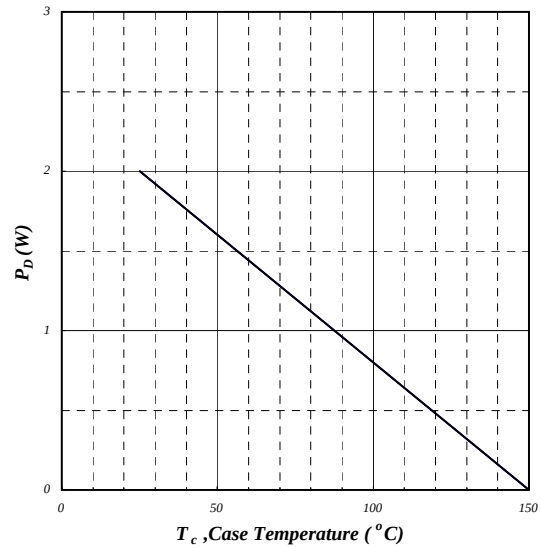


Fig 6. Typical Power Dissipation

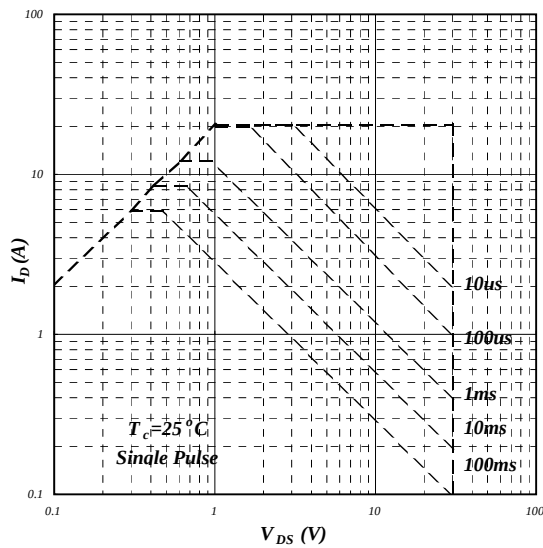


Fig 7. Maximum Safe Operating Area

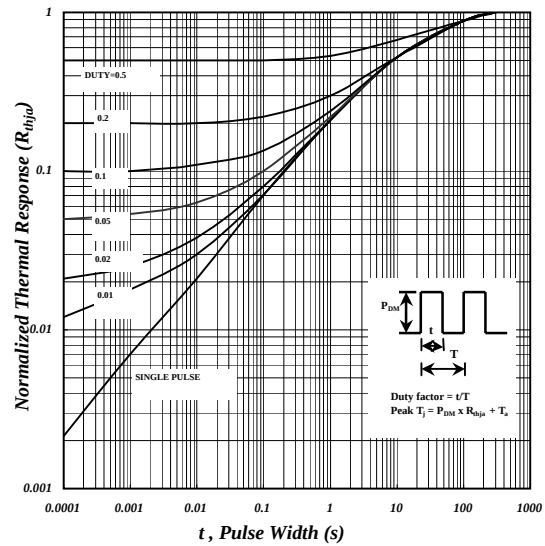


Fig 8. Effective Transient Thermal Impedance

N-channel

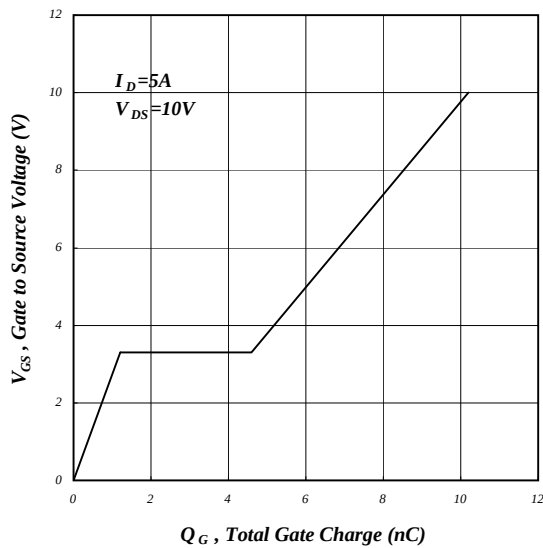


Fig 9. Gate Charge Characteristics

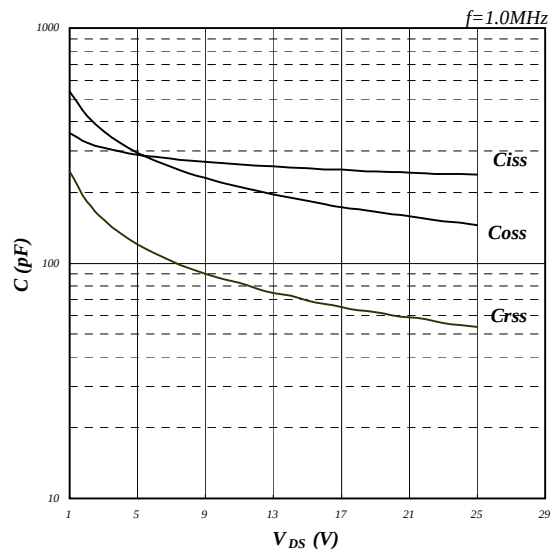


Fig 10. Typical Capacitance Characteristics

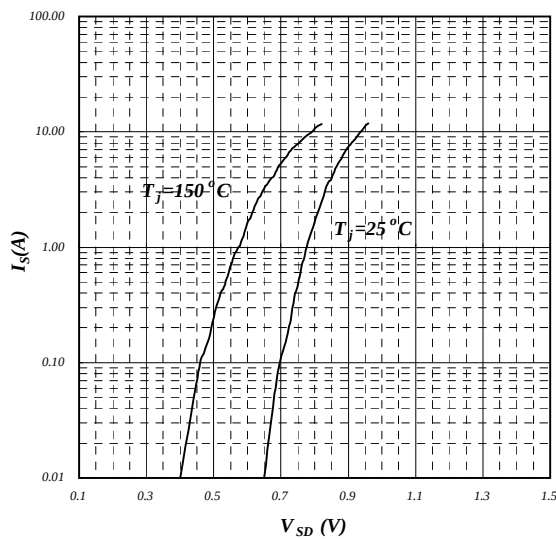


Fig 11. Forward Characteristic of Reverse Diode

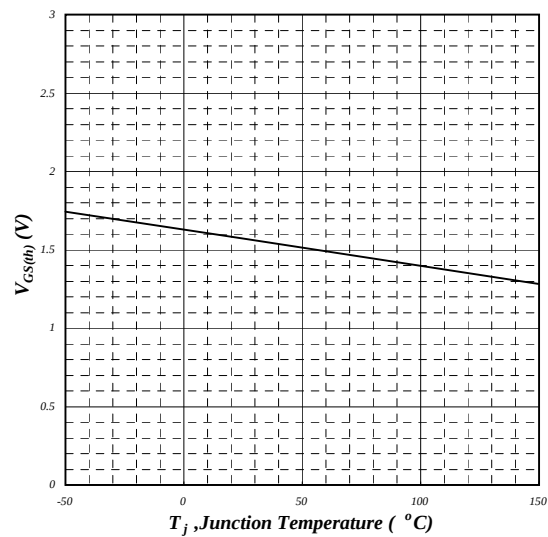


Fig 12. Gate Threshold Voltage vs. Junction Temperature

N-channel

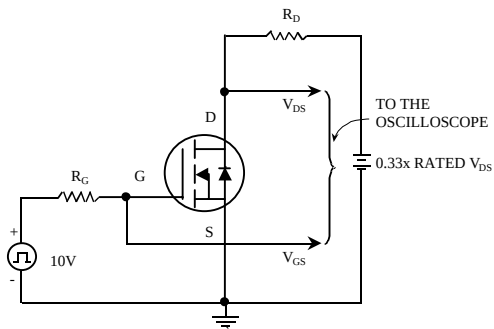


Fig 13. Switching Time Circuit

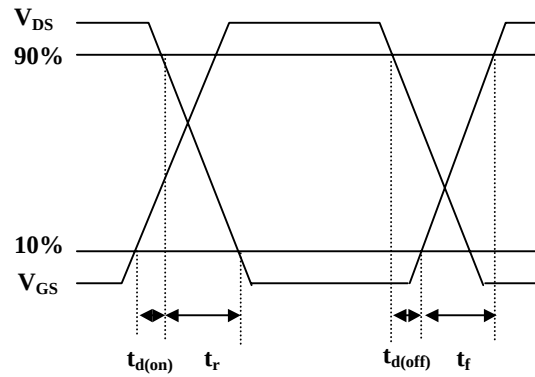


Fig 14. Switching Time Waveform

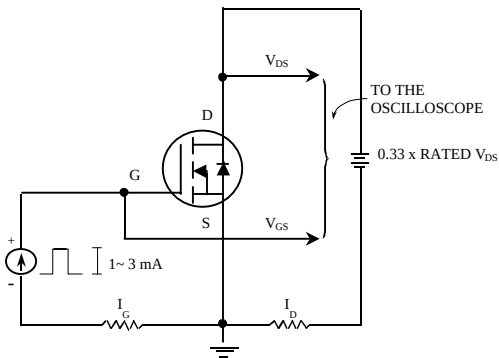


Fig 15. Gate Charge Circuit

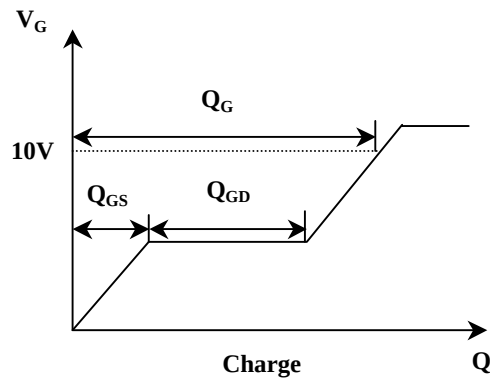


Fig 16. Gate Charge Waveform

P-channel

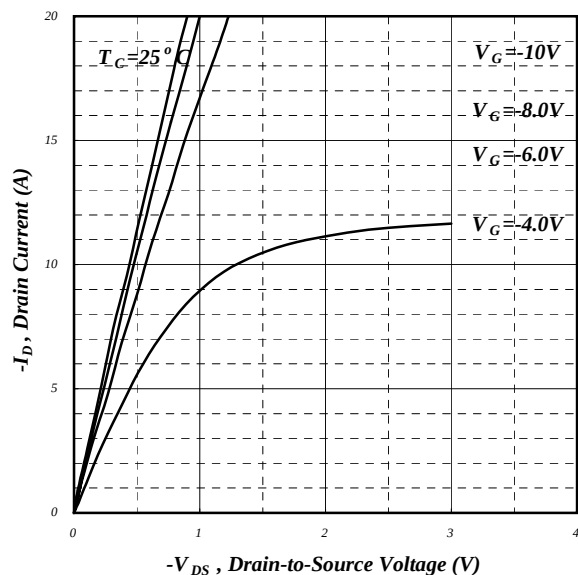


Fig 1. Typical Output Characteristics

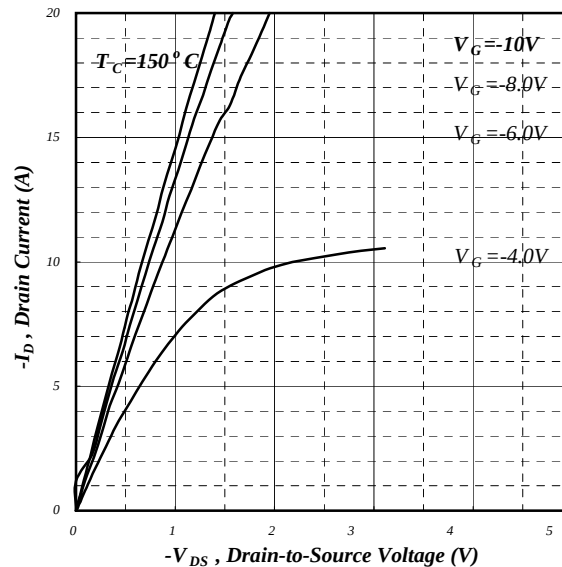


Fig 2. Typical Output Characteristics

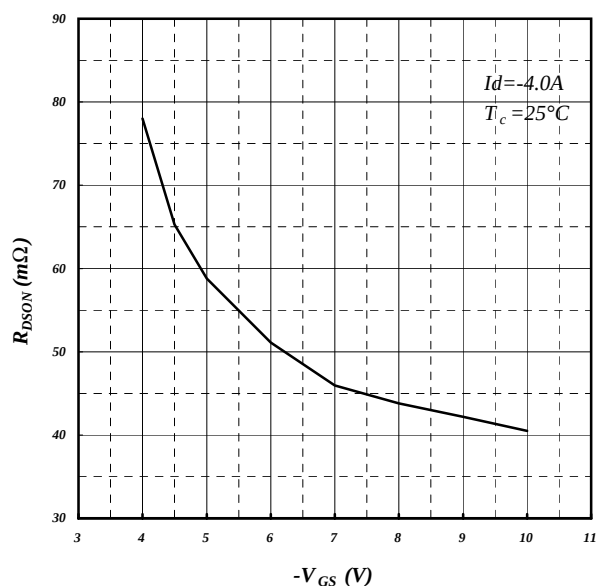


Fig 3. On-Resistance vs. Gate Voltage

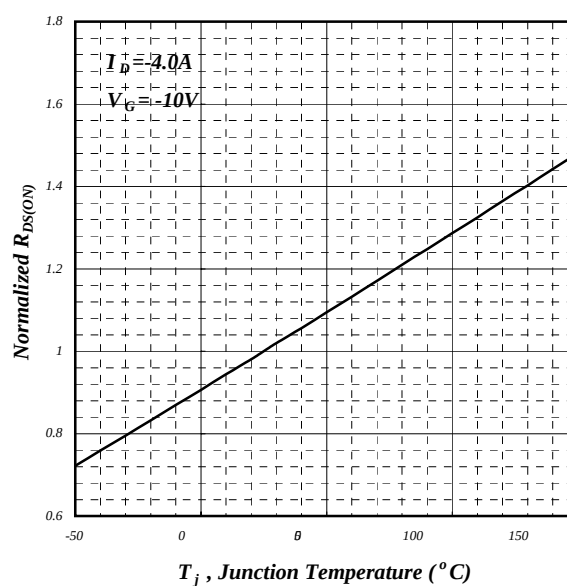


Fig 4. Normalized On-Resistance vs. Junction Temperature

P-channel

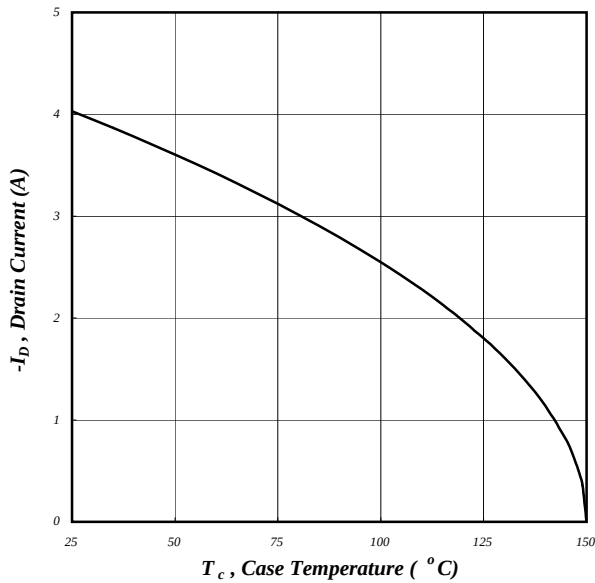


Fig 5. Maximum Drain Current vs. Case Temperature

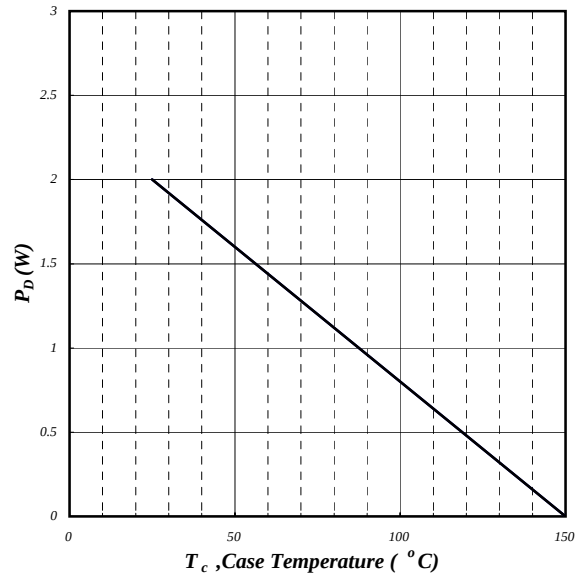


Fig 6. Typical Power Dissipation

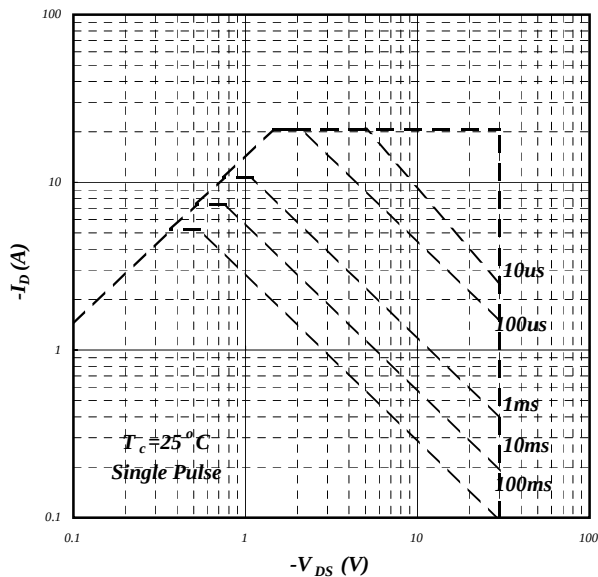


Fig 7. Maximum Safe Operating Area

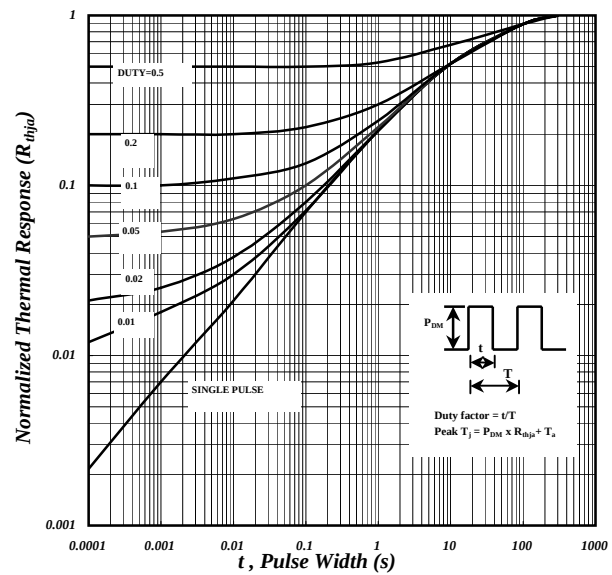


Fig 8. Effective Transient Thermal Impedance

P-channel

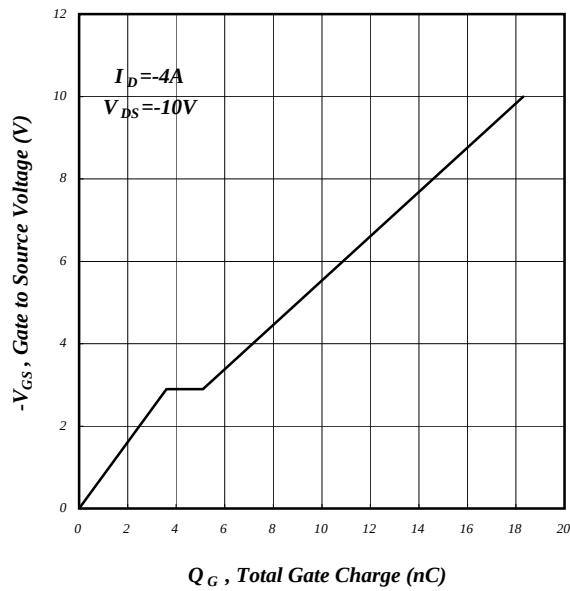


Fig 9. Gate Charge Characteristics

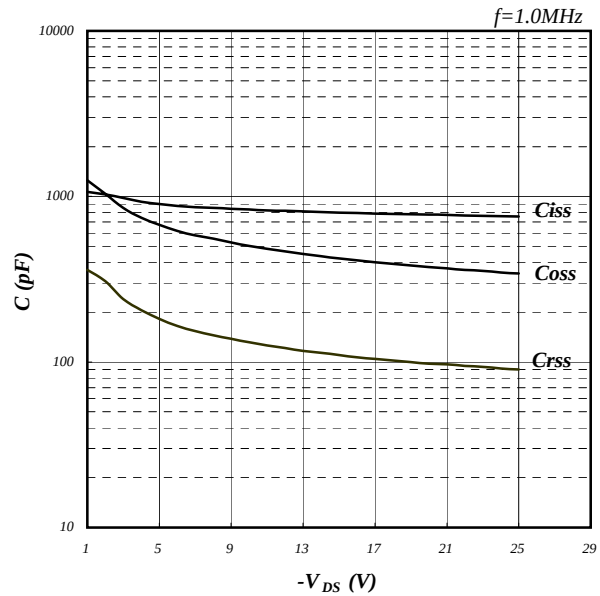


Fig 10. Typical Capacitance Characteristics

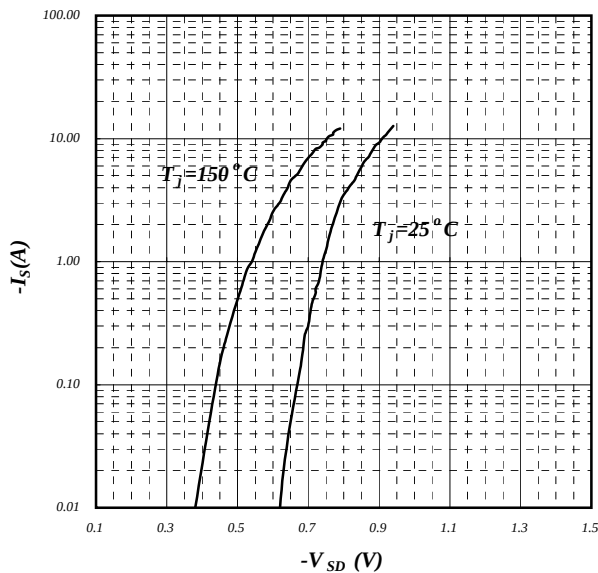


Fig 11. Forward Characteristic of Reverse Diode

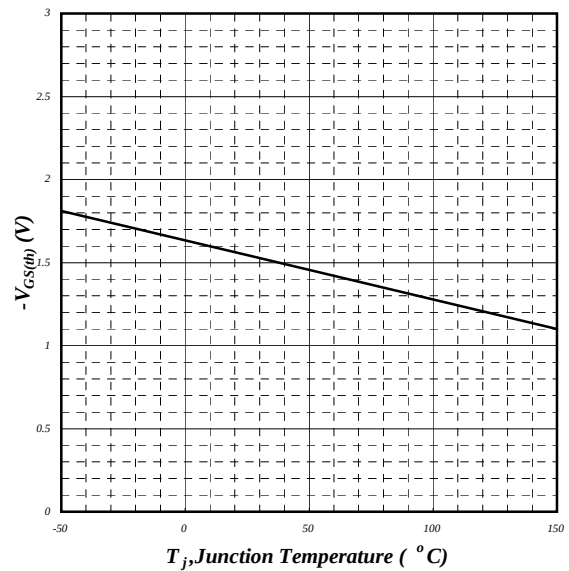


Fig 12. Gate Threshold Voltage vs. Junction Temperature

P-channel

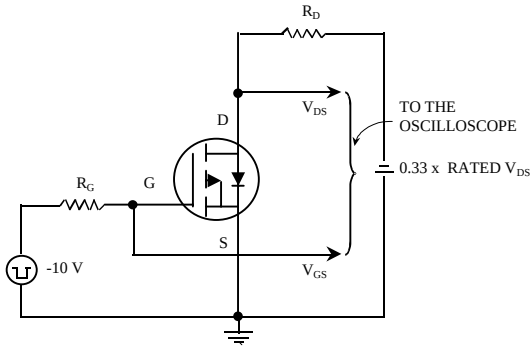


Fig 13. Switching Time Circuit

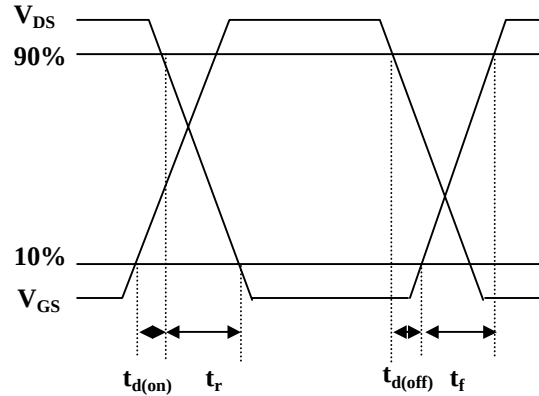


Fig 14. Switching Time Waveform

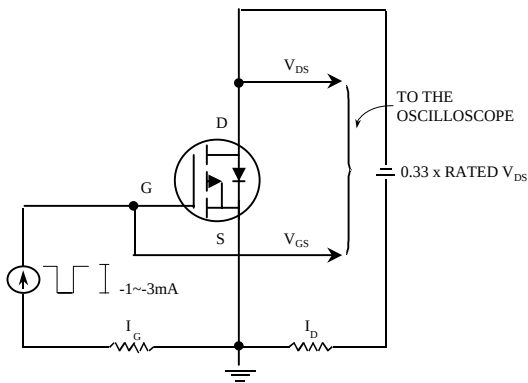


Fig 15. Gate Charge Circuit

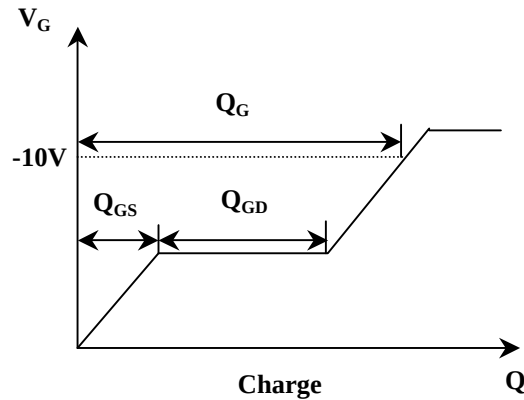


Fig 16. Gate Charge Waveform

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