ON Semiconductor®



# 2, 4, and 8-Channel Low-Capacitance ESD Protection Array

CM1230

#### **Features**

- Two, four, and eight channels of ESD protection
- Provides ESD protection to IEC61000-4-2 Level 4
  - ±8kV contact discharge
  - ±15kV air discharge
- Low loading capacitance of 0.8pF typical
- Minimal capacitance change with temperature and voltage
- Channel I/O to GND capacitance difference of 0.02pF typical is ideal for differential signals
- Channel I/O to I/O capacitance 0.15pF typical
- Zener diode protects supply rail and eliminates the need for external by-pass capacitors
- Each I/O pin can withstand over 1000 ESD strikes\*
- Available in 4, 6 and 10 bump Chip Scale Packages (CSP)
- OptiGuard™ coated for improved reliability at assembly
- RoHS-compliant, lead-free version finishing

## **Applications**

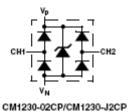
- LCD and camera data lines in wireless handsets that use high-speed serial interfaces.
- I/O port protection for mobile handsets, notebook computers, DSCs, MP3 players, PDAs, etc. including USB, 1394 and serial ATA
- Wireless handsets
- Handheld PCs/PDAs
- LCD and camera modules

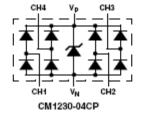
### **Product Description**

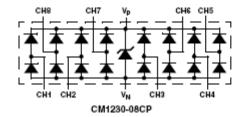
The CM1230 is a family of 2, 4 and 8 channel, very low capacitance ESD protection diode arrays in a CSP form factor. It is ideal for protecting systems with high data and clock rates or for circuits that need low capacitive loading. Each channel consists of a pair of ESD diodes that act as clamp diodes to steer ESD current pulses to either the positive or negative supply rail. A zener diode is integrated between the positive and negative supply rails. The V<sub>cc</sub> rail is protected from ESD strikes and eliminates the need for a bypass capacitor to absorb positive ESD strikes to ground. Each channel can safely dissipate ESD strikes of ±8kV, meeting the Level 4 requirement of the IEC61000-4-2 international standard as well as ±15kV air discharges per the IEC61000-4-2 specification. Using the MIL-STD-883 (Method 3015) specification for Human Body Model (HBM) ESD, the pins are protected for contact discharges at greater than ±15kV.

This device is well-suited for next generation wireless handsets that implement high-speed serial interface solutions for the LCD display and camera interfaces. In these designs, a tolerance above 1.5pF cannot be tolerated when high data rates are transferred between the baseband choppiest and the LCD driver/controller Is. Higher capacitive loading normally causes the rise and fall times to slow which hampers the functionality of circuit and operation of the wireless handset. The CM1230 incorporates *OptiGuard*<sup>IM</sup> which results in improved reliability at assembly. The CM1230 is available in a space-saving, low profile Chip Scale Package with RoHS-compliant, lead-free finishing.

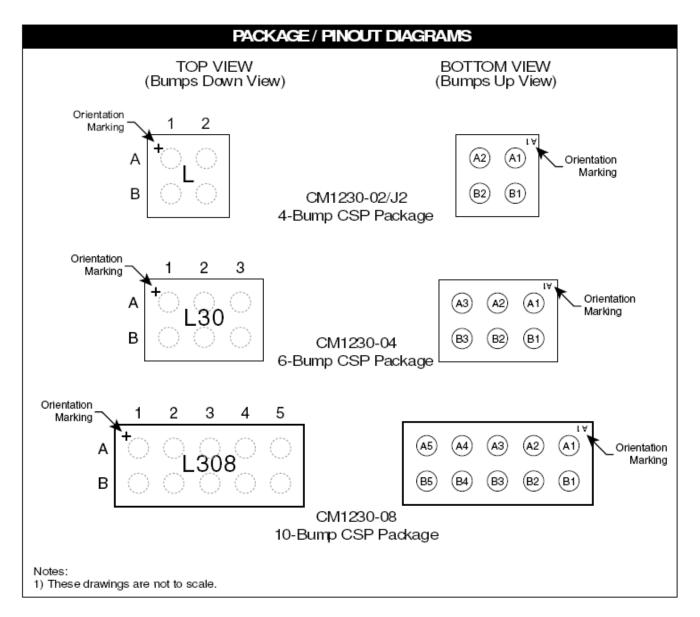
#### **Electrical Schematic**







<sup>\*</sup>Standard test condition is IEC61000-4-2 level 4 test circuit with each (A<sub>out</sub>/B<sub>out</sub>) pin subjected to ±12kV contact discharge for 1000 pulses. Discharges are timed at 1 second intervals and all 1000 strikes are completed in one continuous test run.



# **Ordering Information**

PART NUMBERING INFORMATION							
# of Channels	Channels Bumps Package Ordering Part Number <sup>1</sup>			Part Marking			
2	4	CSP-4	CM1230-02CP	L			
2	4	CSP-4	CM1230-J2CP	L			
4	6	CSP-6	CM1230-04CP	L30			
8	10	CSP-10	CM1230-08CP	L308			

Note 1: Parts are shipped in Tape and Reel form unless otherwise specified.

# **Pin Descriptions**

	2-CHANNEL, 4-BUMP CSP								
PI N	NAME	TYPE	DESCRIPTION						
A1	$V_{N}$	GND	Negative voltage supply rail						
B1	CH2	I/O	ESD Channel						
A2	CH1	I/O	ESD Channel						
B2	V <sub>P</sub>	PWR	Positive voltage supply rail						
	4-	CHANNE	EL, 6-BUMP CSP						
PI N	NAME	TYPE	DESCRIPTION						
A1	CH1	I/O	ESD Channel						
B1	CH2	I/O	ESD Channel						
A2	V <sub>P</sub>	PWR	Positive voltage supply rail						
B2	V <sub>N</sub>	GND	Negative voltage supply rail						
А3	СНЗ	I/O	ESD Channel						
В3	CH4	I/O	ESD Channel						

	8-CHANNEL, 10-BUMP CSP								
PI N	NAME	TYPE	DESCRIPTION						
A1	CH1	I/O	ESD Channel						
B1	CH2	I/O	ESD Channel						
A2	СНЗ	I/O	ESD Channel						
B2	CH4	I/O	ESD Channel						
A3	V <sub>P</sub>	PWR	Positive voltage supply rail						
В3	V <sub>N</sub>	GND	Negative voltage supply rail						
A4	CH5	I/O	ESD Channel						
B4	CH6	I/O	ESD Channel						
A5	CH7	I/O	ESD Channel						
B5	CH8	I/O	ESD Channel						

# **Specifications**

ABSOLUTE MAXIMUM RATINGS						
PARAMETER	RATING	UNITS				
Operating Supply Voltage (V <sub>P</sub> - V <sub>N</sub> )	6.0	V				
Operating Temperature Range	-40 to +85	°C				
Storage Temperature Range	-65 to +150	°C				
DC Voltage at any channel input	$(V_{N} - 0.5)$ to $(V_{P} + 0.5)$	V				

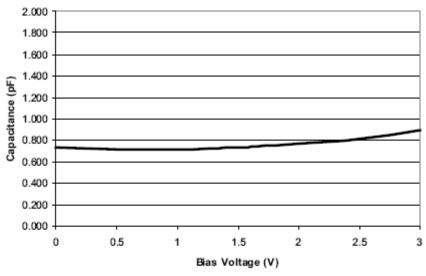
STANDARD OPERATING CONDITIONS						
PARAMETER	RATING	UNITS				
Operating Temperature Range	-40 to +85	°C				

	ELECTRICAL OPERATING CHARACTERISTICS(SEE NOTE 1)								
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS			
V <sub>P</sub>	Operating Supply Voltage (V <sub>P</sub> -V <sub>N</sub> )			3.3	5.5	V			
I <sub>P</sub>	Operating Supply Current	(V <sub>P</sub> -V <sub>N</sub> )=3.3V			8.0	μΑ			
V <sub>F</sub>	Diode Forward Voltage Top Diode Bottom Diode	I <sub>F</sub> = 8mA; T <sub>A</sub> =25°C	0.60 0.60	0.80 0.80	0.95 0.95	V V			
<b>I</b> <sub>LEAK</sub>	Channel Leakage Current	T <sub>A</sub> =25°C; V <sub>P</sub> =5V, V <sub>N</sub> =0V, V <sub>IN</sub> = 0V to 5V		±0.1	±1.0	μА			
C <sub>IN</sub>	Channel Input Capacitance	At 1 MHz, $V_p=3.3V$ , $V_N=0V$ , $V_N=1.65V$		0.8	1.20	pF			
$\Delta C_{IN}$	Channel Input Capacitance Matching	At 1 MHz, $V_p=3.3V$ , $V_N=0V$ , $V_N=1.65V$		0.02		pF			
C <sub>MUTUAL</sub>	Mutual Capacitance between signal pin and adjacent signal pin	At 1 MHz, $V_p=3.3V$ , $V_N=0V$ , $V_N=1.65V$		0.15		pF			
V <sub>ESD</sub>	In-system ESD Protection Peak Discharge Voltage at any channel input, in system a) Contact discharge per IEC 61000-4-2 standard b) Human Body Model, MIL- STD-883, Method 3015	Notes 3 and 4; $T_A$ =25°C Notes 2 and 4; $T_A$ =25°C	±8 ±15			kV kV			
V <sub>CL</sub>	Channel Clamp Voltage Positive Transients Negative Transients	$T_A = 25^{\circ}\text{C}, I_{PP} = 1\text{A}, t_P = 8/20 \mu\text{S};$ Note 4		+9.8 -1.8		V V			
R <sub>DYN</sub>	Dynamic Resistance Positive Transients Negative Transients	$I_{pp}$ = 1A, $t_p$ = 8/20 $\mu$ S Any I/O pin to Ground; Note 4		0.76 0.56		Ω			

Note 1: All parameters specified at  $T_A$  = -40°C to +85°C unless otherwise noted. Note 2: Human Body Model per MIL-STD-883, Method 3015,  $C_{Discharge}$  = 100pF,  $R_{Discharge}$  = 1.5K $\Omega$ ,  $V_P$  = 3.3V,  $V_N$  grounded. Note 3: Standard IEC 61000-4-2 with  $C_{Discharge}$  = 150pF,  $R_{Discharge}$  = 330 $\Omega$ ,  $V_P$  = 3.3V,  $V_N$  grounded. Note 4: These measurements performed with no external capacitor on  $V_P$ . Note 5: Measured under pulsed conditions, pulse width = 0.7ms, maximum current = 1.5A.

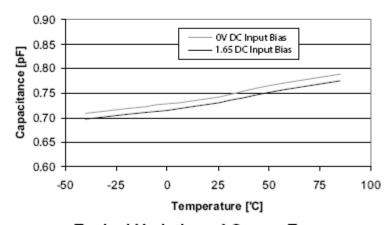
## **Performance Information**

#### **Input Channel Capacitance Performance Curves**



Typical Variation of  $C_{\rm IN}$  vs.  $V_{\rm IN}$ 

(f=1MHz,  $V_P = 3.3V$ ,  $V_N = 0V$ ,  $0.1~\mu F$  chip capacitor between  $V_P$  and  $V_{N_s}$   $T_A = 25^{\circ}C$ )

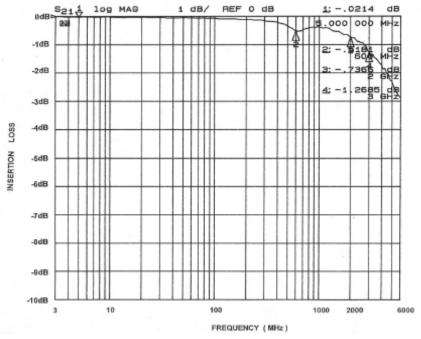


Typical Variation of CIN vs. Temp

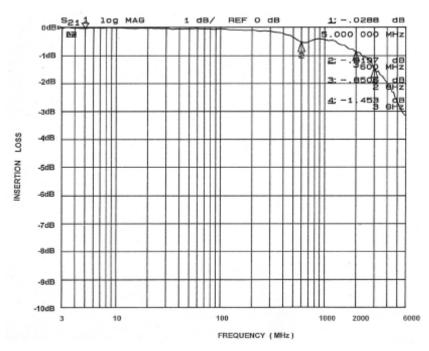
(f=1MHz,  $V_{IN}$ =30mV,  $V_P$  = 3.3V,  $V_N$  = 0V, 0.1  $\mu F$  chip capacitor between  $V_P$  and  $V_N$ )

## Performance Information (Cont'd)

Typical Filter Performance (nominal conditions unless specified otherwise, 50 Ohm Environment)



Insertion Loss VS. Frequency (0V DC Bias, V<sub>p</sub>=3.3V)



Insertion Loss VS. Frequency (2.5V DC Bias, V<sub>p</sub>=3.3V)

## **Application Information**

PARAMETER	VALUE
Pad Size on PCB	0.240mm
Pad Shape	Round
Pad Definition	Non-Solder Mask defined pads
Solder Mask Opening	0.290mm Round
Solder Stencil Thickness	0.125mm - 0.150mm
Solder Stencil Aperture Opening (laser cut, 5% tapered walls)	0.300mm Round
Solder Flux Ratio	50/50 by volume
Solder Paste Type	No Clean
Pad Protective Finish	OSP (Entek Cu Plus 106A)
Tolerance — Edge To Corner Ball	<u>+</u> 50μm
Solder Ball Side Coplanarity	<u>+</u> 20μm
Maximum Dwell Time Above Liquidous	60 seconds
Maximum Soldering Temperature for Lead-free Devices using a Lead-free Solder Paste	260°C

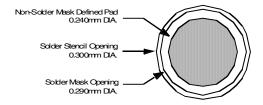


Figure 8. Recommended Non-Solder Mask Defined Pad Illustration

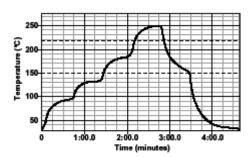


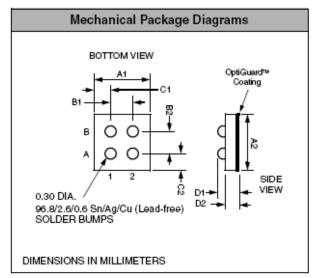
Figure 9. Lead-free (SnAgCu) Solder Ball Reflow Profile

#### **Mechanical Details**

#### **CSP-4 Mechanical Specifications (CM1230-02CP)**

The CM1230-02CP is supplied in a 4 bump Chip Scale Package (CSP). Dimensions are shown below. For complete information on the CSP, see the California Micro Devices CSP Package Information document.

PACKAGE DIMENSIONS							
Pack	age		(	Custom C	SP		
Bum	nps			4			
Dim	M	illimete	ers		Inches		
	Min	Nom	Max	Min	Nom	Max	
<b>A</b> 1	0.915	0.960	1.005	0.0360	0.0378	0.0396	
A2	0.915	0.960	1.005	0.0360	0.0378	0.0396	
B1	0.495	0.500	0.505	0.0195	0.0197	0.0199	
B2	0.495	0.500	0.505	0.0195	0.0197	0.0199	
C1	0.180	0.230	0.280	0.0071	0.0091	0.0110	
C2	0.180	0.230	0.280	0.0071	0.0091	0.0110	
D1	0.575	0.644	0.714	0.0226	0.0254	0.0281	
D2	0.368	0.419	0.470	0.0145	0.0165	0.0185	
# per tap				3500 pie	ces		
	Controlling dimension: millimeters						



Package Dimensions for CM1230-02CP Chip Scale Package

PART NUMBER	CHIP SIZE (mm)	POCKET SIZE (mm) B <sub>o</sub> X A <sub>o</sub> X K <sub>o</sub>	TAPE WIDTH W	REEL DIAMETER	QTY PER REEL	P <sub>o</sub>	P <sub>1</sub>
CM1230-02CP*	0.96 x 0.96 x 0.644	1.14 x 1.00 x 0.70	8mm	178mm (7")	3500	4mm	4mm

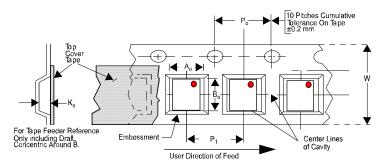


Figure 3. Tape and Reel Mechanical Data\*

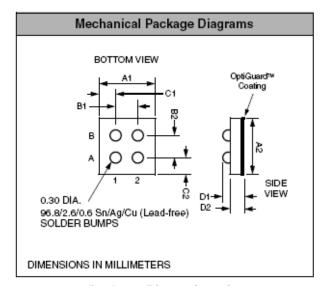
<sup>\*</sup> CM1230-02CP and CM1230-J2CP are the same mechanical package. The only difference is the Pin 1 orientation (red dot) on the tape and reel.

## Mechanical Details (cont'd)

#### **CSP-4 Mechanical Specifications (CM1230-J2CP)**

The CM1230-J2CP is supplied in a 4 bump Chip Scale Package (CSP). Dimensions are shown below. For complete information on the CSP, see the California Micro Devices CSP Package Information document.

PACKAGE DIMENSIONS							
Pack	age		(	Custom C	SP		
Burr	nps			4			
Dim	M	illimete	ers		Inches		
Dilli	Min	Nom	Max	Min	Nom	Max	
<b>A</b> 1	0.915	0.960	1.005	0.0360	0.0378	0.0396	
A2	0.915	0.960	1.005	0.0360	0.0378	0.0396	
B1	0.495	0.500	0.505	0.0195	0.0197	0.0199	
B2	0.495	0.500	0.505	0.0195	0.0197	0.0199	
C1	0.180	0.230	0.280	0.0071	0.0091	0.0110	
C2	0.180	0.230	0.280	0.0071	0.0091	0.0110	
D1	0.575	0.644	0.714	0.0226	0.0254	0.0281	
D2	0.368	0.419	0.470	0.0145	0.0165	0.0185	
# per ta	-			3500 pie	ces		
Controlling dimension: millimeters							



Package Dimensions for CM1230-J2CP Chip Scale Package

PART NUMBER	CHIP SIZE (mm)	POCKET SIZE (mm) B <sub>o</sub> X A <sub>o</sub> X K <sub>o</sub>	TAPE WIDTH W	REEL DIAMETER	QTY PER REEL	P <sub>o</sub>	P <sub>1</sub>
CM1230-J2CP*	0.96 x 0.96 x 0.644	1.14 x 1.00 x 0.70	8mm	178mm (7")	3500	4mm	4mm

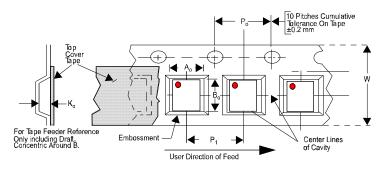


Figure 4. Tape and Reel Mechanical Data\*

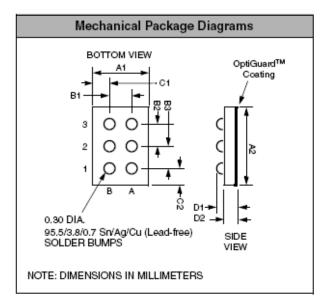
<sup>\*</sup>CM1230-02CP and CM1230-J2CP are the same mechanical package. Only difference is the Pin 1 orientation (red dot) on the tape and reel.

## Mechanical Details (cont'd)

#### **CSP-6 Mechanical Specifications**

The CM1230-04CP is supplied in a 6 bump Chip Scale Package (CSP). Dimensions are shown below. For complete information on the CSP, see the California Micro Devices CSP Package Information document.

	PACKAGE DIMENSIONS							
Pack	age		(	Custom C	SP			
Burr	nps			6				
Dim	M	lillimete	ers		Inches			
Diiii	Min	Nom	Max	Min	Nom	Max		
<b>A</b> 1	0.915	0.960	1.005	0.0360	0.0378	0.0396		
A2	1.415	1.460	1.505	0.0557	0.0575	0.0593		
B1	0.495	0.500	0.505	0.0195	0.0197	0.0199		
B2	0.495	0.500	0.505	0.0195	0.0197	0.0199		
C1	0.180	0.230	0.280	0.0071	0.0091	0.0110		
C2	0.180	0.230	0.280	0.0071	0.0091	0.0110		
D1	0.575	0.644	0.714	0.0226	0.0254	0.0281		
D2	0.368	0.419	0.470	0.0145	0.0165	0.0185		
# per ta				3500 pie	ces			
Controlling dimension: millimeters								



Package Dimensions for CM1230-04CP Chip Scale Package

PART NUMBER	CHIP SIZE (mm)	POCKET SIZE (mm) B <sub>o</sub> X A <sub>o</sub> X K <sub>o</sub>	TAPE WIDTH W	REEL DIAMETER	QTY PER REEL	P <sub>o</sub>	P <sub>1</sub>
CM1230-04CP	1.46 x 0.96 x 0.644	1.72 x 1.17 x 0.73	8mm	178mm (7")	3500	4mm	4mm

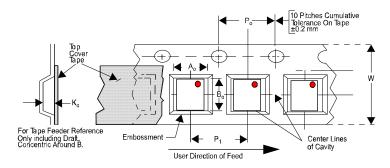


Figure 5. Tape and Reel Mechanical Data

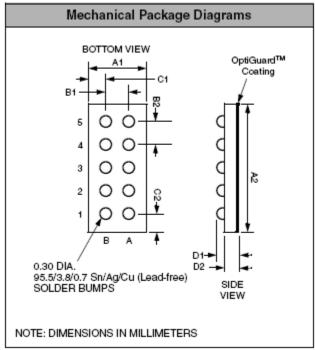
## Mechanical Details (cont'd)

#### **CSP-10 Mechanical Specifications**

The CM1230-08CP is supplied in a 10 bump Chip Scale Package (CSP). Dimensions are shown below. For complete information on the CSP, see the California Micro Devices CSP Package Information document.

	PACKAGE DIMENSIONS							
Paci	kage	Custom CSP						
Bur	nps	10						
Dim	Millimeters			Inches				
Dilli	Min	Nom	Max	Min	Nom	Max		
<b>A</b> 1	0.915	0.960	1.005	0.0360	0.0378	0.0396		
A2	2.415	2.460	2.505	0.0951	0.0969	0.0986		
B1	0.495	0.500	0.505	0.0195	0.0197	0.0199		
B2	0.495	0.500	0.505	0.0195	0.0197	0.0199		
C1	0.180	0.230	0.280	0.0071	0.0091	0.0110		
C2	0.180	0.230	0.280	0.0071	0.0091	0.0110		
D1	0.575	0.644	0.714	0.0226	0.0254	0.0281		
D2	0.368	0.419	0.470	0.0145	0.0165	0.0185		
# per tape and reel		3500 pieces						

Controlling dimension: millimeters



Package Dimensions for CM1230-08CP Chip Scale Package

PART NUMBER	CHIP SIZE (mm)	POCKET SIZE (mm) B <sub>o</sub> X A <sub>o</sub> X K <sub>o</sub>	TAPE WIDTH W	REEL DIAMETER	QTY PER REEL	P <sub>o</sub>	<b>P</b> <sub>1</sub>
CM1230-08CP	2.46 x 0.96 x 0.644	2.62 x 1.12 x 0.76	8mm	178mm (7")	3500	4mm	4mm

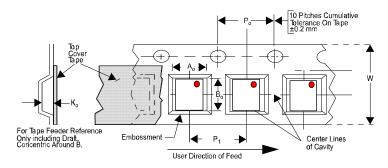


Figure 6. Tape and Reel Mechanical Data

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