



6N40

Preliminary

Power MOSFET

6 Amps, 400 Volts N-CHANNEL POWER MOSFET

DESCRIPTION

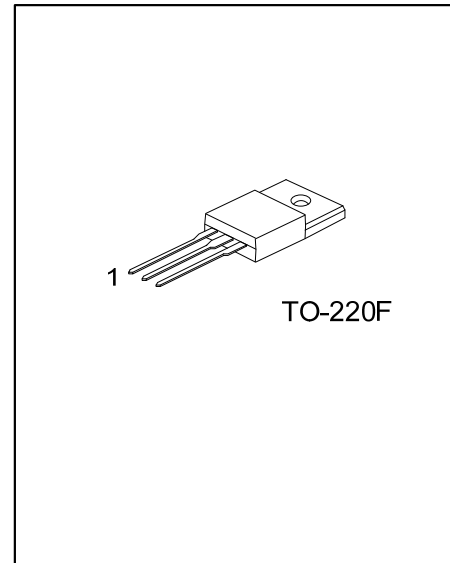
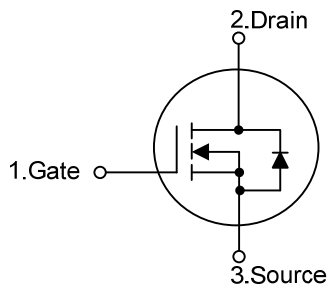
The UTC **6N40** is an N-Channel enhancement mode Power FET using UTC's perfect planar stripe, DMOS technology to provide customers with superior switching performance and minimum on-state resistance. It also can withstand high energy pulse in the avalanche and commutation mode.

The UTC **6N40** is generally used in applications , such as electronic lamp ballasts based on half bridge topology and high efficiency switched mode power supplies.

FEATURES

- * 6A, 400V, $R_{DS(ON)}=1.0\Omega @ V_{GS}=10V$
- * Fast switching speed
- * Improved dv/dt capability

SYMBOL



ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
6N40L-TF3-T	6N40G-TF3-T	TO-220F	G	D	S	Tube

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>6N40L - TF3 - T</p> <p>(1) Packing Type (2) Package Type (3) Lead Free</p>	<p>(1) T: Tube (2) TF3: TO-220F (3) G: Halogen Free, L: Lead Free</p>
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■ ABSOLUTE MAXIMUM RATINGS ($T_c = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Drain-Source Voltage	V_{DSS}	400	V
Gate-Source Voltage	V_{GSS}	± 30	V
Avalanche Current (Note 1)	I_{AR}	6	A
Drain Current	Continuous	I_D	6 (Note 6)
	Pulsed (Note 1)	I_{DM}	24 (Note 6)
Avalanche Energy	Single Pulsed (Note 2)	E_{AS}	270
	Repetitive (Note 1)	E_{AR}	7.3
Peak Diode Recovery dv/dt (Note 3)	dv/dt	4.5	V/ns
Power Dissipation	P_D	38	W
Junction Temperature	T_J	+150	$^\circ\text{C}$
Storage Temperature	T_{STG}	-55 ~ +150	$^\circ\text{C}$

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	62.5	$^\circ\text{C}/\text{W}$
Junction to Case	θ_{JC}	3.31	$^\circ\text{C}/\text{W}$

■ ELECTRICAL CHARACTERISTICS ($T_C=25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	400			V
Breakdown Voltage Temperature Coefficient	$\Delta BV_{DSS}/\Delta T_J$	$I_D=250\mu A$, Referenced to 25°C		0.54		$V/^\circ\text{C}$
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=400V, V_{GS}=0V$			1	μA
		$V_{DS}=320V, T_J=125^\circ\text{C}$			10	μA
Gate-Source Leakage Current	Forward	$V_{DS}=0V, V_{GS}=+30V$			+100	nA
	Reverse	$V_{DS}=0V, V_{GS}=-30V$			-100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2.0		4.0	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=3A$		0.83	1	Ω
Forward Transconductance	g_{FS}	$V_{DS}=40V, I_D=3A$ (Note 4)		4.7		S
DYNAMIC PARAMETERS						
Input Capacitance	C_{ISS}	$V_{DS}=25V, V_{GS}=0V, f=1.0\text{MHz}$		480	625	pF
Output Capacitance	C_{OSS}			80	105	pF
Reverse Transfer Capacitance	C_{RSS}			15	20	pF
SWITCHING PARAMETERS						
Total Gate Charge	Q_G	$V_{DS}=320V, V_{GS}=10V, I_D=6A$ (Note 4,5)		16	20	nC
Gate-Source Charge	Q_{GS}			2.3		nC
Gate-Drain Charge	Q_{GD}			8.2		nC
Turn-ON Delay Time	$t_{D(ON)}$	$V_{DD}=200V, I_D=6A, R_G=25\Omega$ (Note 4,5)		13	35	ns
Turn-ON Rise Time	t_R			65	140	ns
Turn-OFF Delay Time	$t_{D(OFF)}$			21	55	ns
Turn-OFF Fall Time	t_F			38	85	ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Body-Diode Continuous Current	I_S				6	A
Maximum Body-Diode Pulsed Current	I_{SM}				24	A
Drain-Source Diode Forward Voltage	V_{SD}	$I_S=6A, V_{GS}=0V$			1.4	V
Body Diode Reverse Recovery Time	t_{RR}	$V_{GS}=0V, I_S=6A$,		230		ns
Body Diode Reverse Recovery Charge	Q_{RR}	$di_F/dt=100A/\mu s$ (Note 4)		1.7		μC

Notes: 1. Repetitive Rating : Pulse width limited by maximum junction temperature

2. $L=13.7\text{mH}, I_{AS}=6A, V_{DD}=50V, R_G=25\Omega$, Starting $T_J=25^\circ\text{C}$

3. $I_{SD}\leq 6A, di/dt\leq 200A/\mu s, V_{DD}\leq BV_{DSS}$, Starting $T_J=25^\circ\text{C}$

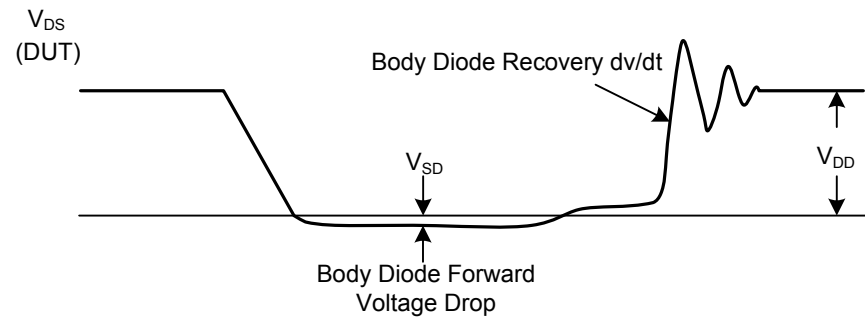
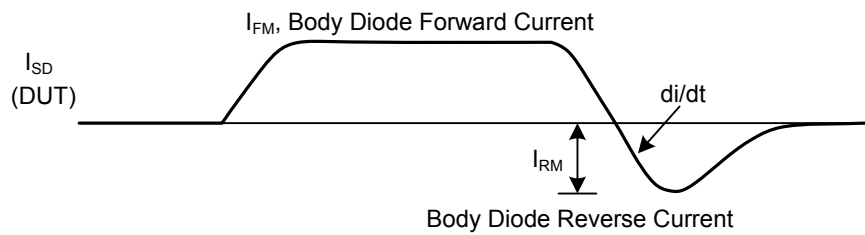
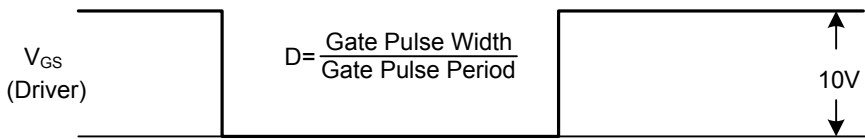
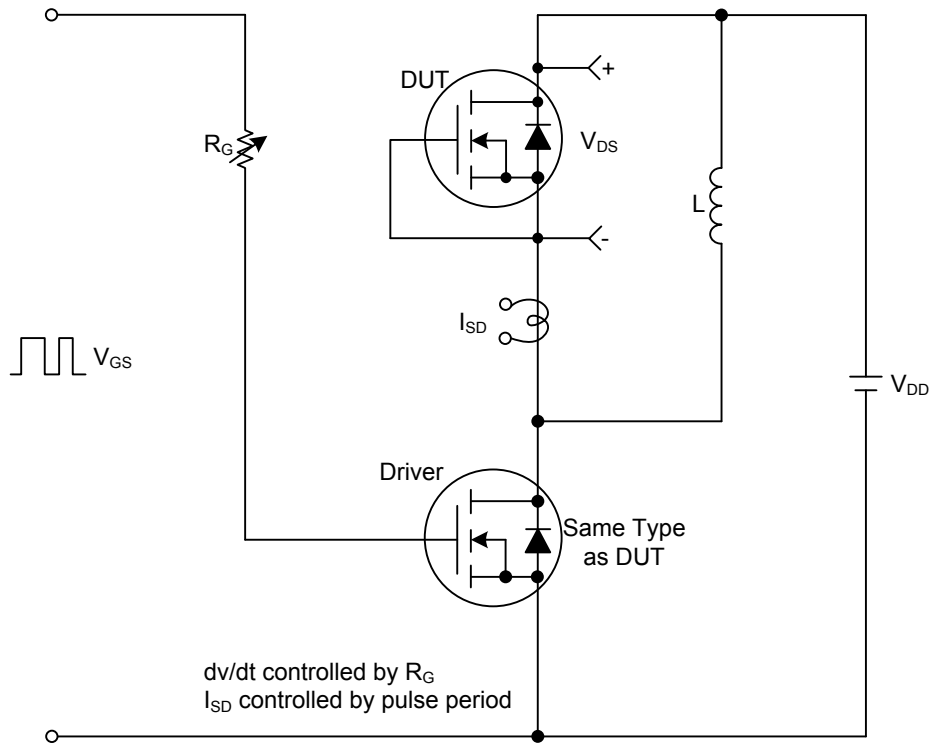
4. Pulse Test : Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$

5. Essentially independent of operating temperature

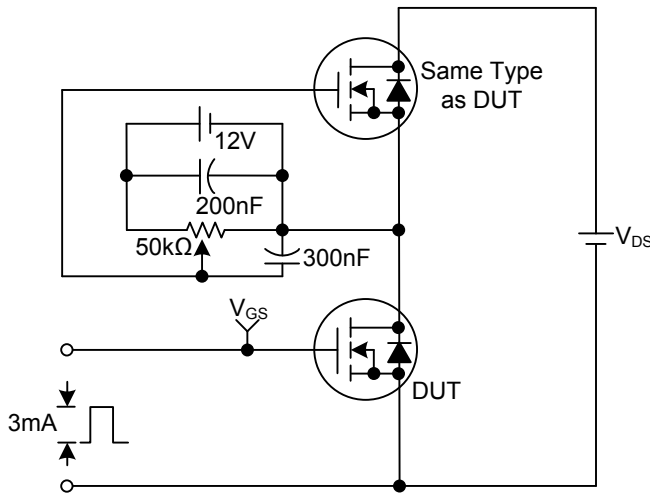
6. Drain current limited by maximum junction temperature

■ TEST CIRCUITS AND WAVEFORMS

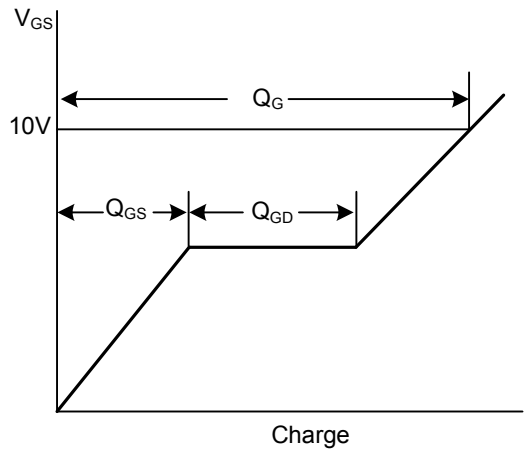
Peak Diode Recovery dv/dt Test Circuit & Waveforms



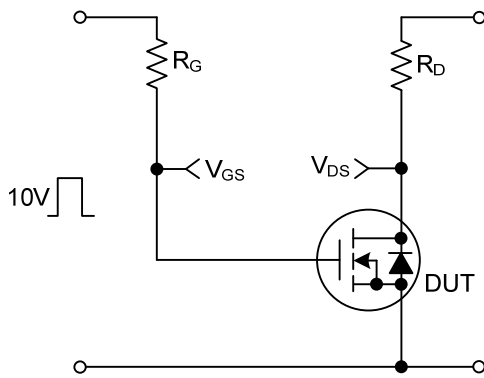
Gate Charge Test Circuit



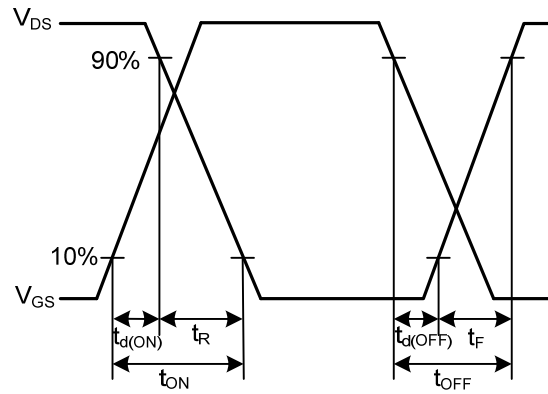
Gate Charge Waveforms



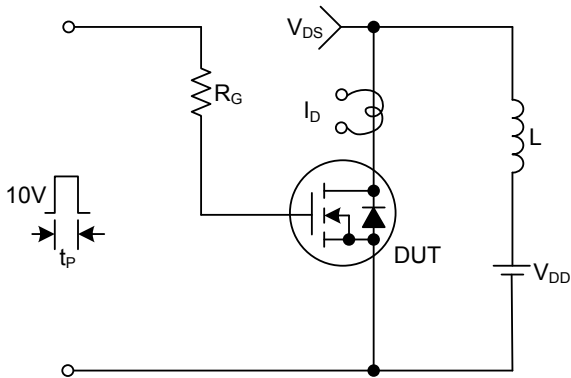
Resistive Switching Test Circuit



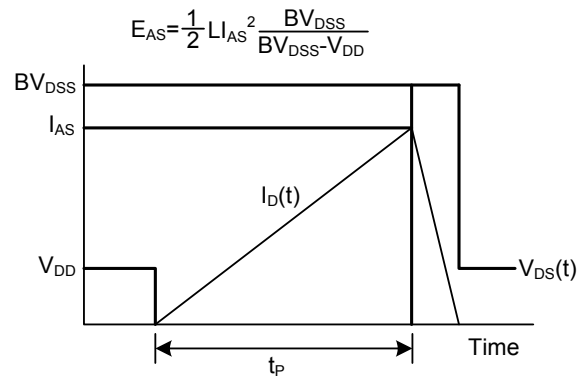
Resistive Switching Waveforms



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms



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