Structure : Silicon Monolithic Integrated Circuit

Product name : Sync. Separator With AFC

Type : **BA7071F**

Features :
1) Built-in AFC circuit
2) Horizontal free-run frequency requires no adjustment
3) Few externally attached components
4) Wide operation power supply range (2.85 V~7.5 V)
5) SOP8 Pin package

○Absolute Maximum Ratings(Ta=25℃)

Parameter	Symbol	Limits	Unit
Supply voltage	Vcc	8.0	V
Power dissipation	Pd	350 *1	mW
Operating temperature	Topr	-20～+75	℃
Storage temperature	Tstg	-55～+125	℃

※1: Derating is done at 3.5mW/℃ above Ta=25℃.
(when mounted on a 50mm x 50mm PCB board.)

○Operating Range(Ta=25℃)

Parameter	Symbol	Limits	Unit
Supply voltage	Vcc	2.85～7.5	V

※This product is not designed for protection against radioactive rays.

Application example

The product described in this specification is designed to be used with ordinary electronic equipment or devices (such as audio-visual equipment, office-automation equipment, communications devices, electrical appliances, and electronic toys). Should you intend to use this product with equipment or devices which require an extremely high level or reliability and the malfunction of which would directly endanger human life (such as medical instruments, transportation equipment, aerospace machinery, nuclear-reactor controllers, fuel controllers and other safety devices),please be sure to consult with our sales representative in advance.

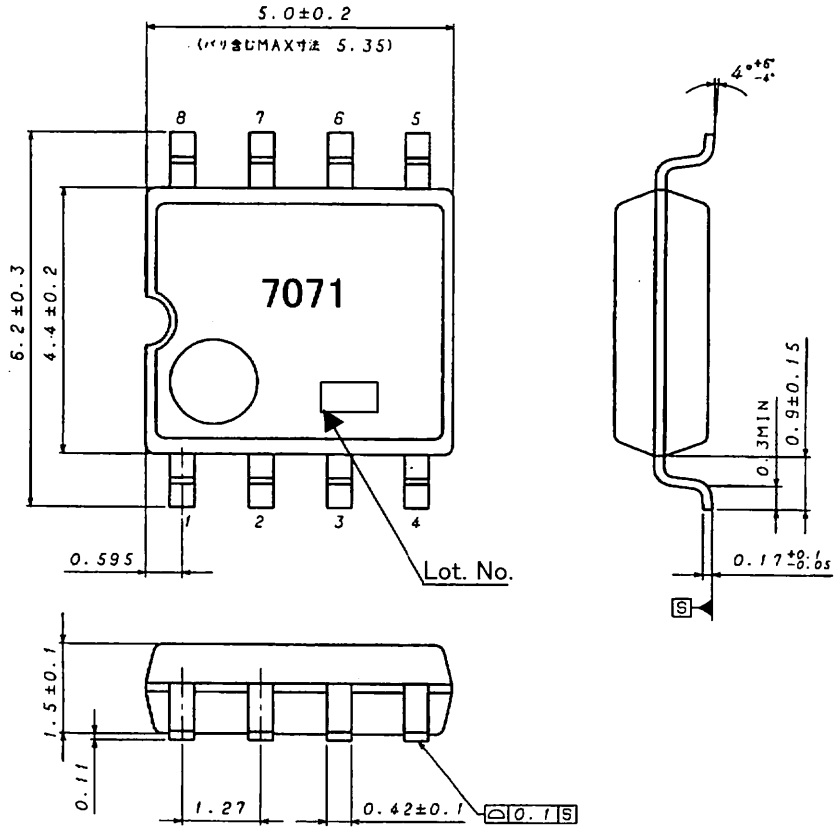
○Electrical characteristics 1/2 (Unless otherwise noted,Ta= 25℃, Vcc=3.0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Quiescent current	I_Q	1.8	3.5	5.2	mA	Pin 8 open
Minimum sync separation level	V_{synmin}	—	0.08	0.15	Vp-p	On 1pin 75Ω terminated input
Pulse voltage, Low	V_{P-L}	—	0.1	0.3	V	2pin, 7pin
Pulse voltage, High	V_{P-H}	2.7	3.0	—	V	2pin, 7pin
Horizontal free-run frequency	F_{HO}	13.3	15.7	18.1	kHz	When inputting no signal
Capture range	ΔF_{CAP}	2.5	3.2	—	kHz	—
Lock-in phase difference	T_{HPH}	0.7	1.7	2.7	μs	From pin 2 ↓ to pin 1 ↓
HD, VD phase difference1	T_{HVD1}	19.0	24.0	29.0	μs	From pin 7 ↓ to pin 2 (FLD1)
HD, VD phase difference2	T_{HVD2}	19.0	24.0	29.0	μs	From pin 7 ↑ to pin 2 (FLD1)
HD pulse width	T_{HD}	9.3	10.3	11.3	μs	2pin ↓ ↑
VD pulse width	T_{VD}	249	254	259	μs	7pin ↓ ↑
VIN,VD phase difference 2	T_{INVD}	41.0	48.0	55.0	μs	From pin 1 ↓ to pin 7 ↓

○Electrical characteristics 2/2 (Unless otherwise noted,Ta= 25℃, Vcc=5.0V)

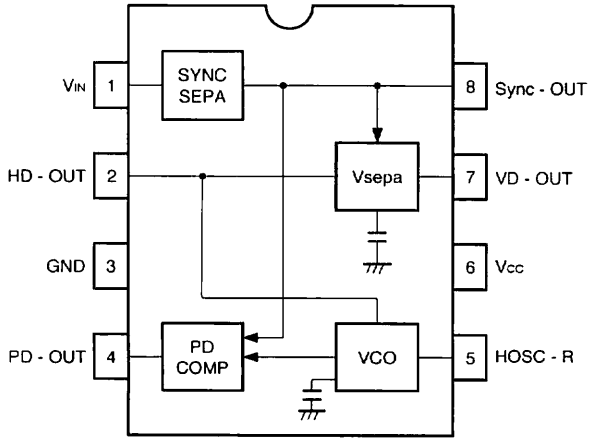
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Quiescent current	I_Q	3.0	5.8	8.6	mA	Pin 8 open
Minimum sync separation level	V_{synmin}	—	0.08	0.15	Vp-p	On 1pin 75Ω terminated input
Pulse voltage, Low	V_{P-L}	—	0.1	0.3	V	2pin, 7pin
Pulse voltage, High	V_{P-H}	4.7	5.0	—	V	2pin, 7pin
Horizontal free-run frequency	F_{HO}	13.5	15.7	17.9	kHz	When inputting no signal
Capture range	ΔF_{CAP}	2.3	2.7	—	kHz	—
Lock-in phase difference	T_{HPH}	0.6	1.6	2.6	μs	From pin 2 ↓ to pin 1 ↓
HD, VD phase difference1	T_{HVD1}	19.0	24.0	29.0	μs	From pin 7 ↓ to pin 2 (FLD1)
HD, VD phase difference2	T_{HVD2}	19.0	24.0	29.0	μs	From pin 7 ↑ to pin 2 (FLD1)
HD pulse width	T_{HD}	9.0	10.0	11.0	μs	2pin ↓ ↑
VD pulse width	T_{VD}	249	254	259	μs	7pin ↓ ↑
VIN,VD phase difference 2	T_{INVD}	41.0	48.0	55.0	μs	From pin 1 ↓ to pin 7 ↓

○Outer dimensions



SOP8 (Unit: mm)

○Block diagram



○Pin number and pin name

Pin No.	Pin name
1	VIN
2	HD-OUT
3	GND
4	PD-OUT
5	HOSC-R
6	Vcc
7	VD-OUT
8	Sync-OUT

○Cautions on use

1) Absolute maximum ratings

If applied voltage, operating temperature range, or other absolute maximum ratings are exceeded, the LSI may be damaged. Do not apply voltages or temperatures that exceed the absolute maximum ratings. If you think of a case in which absolute maximum ratings are exceeded, enforce fuses or other physical safety measures and investigate how not to apply the conditions under which absolute maximum ratings are exceeded to the LSI.

2) GND potential

Make the GND pin voltage such that it is the lowest voltage even when operating below it. Actually confirm that the voltage of each pin does not become a lower voltage than the GND pin, including transient phenomena.

3) Thermal design

Perform thermal design in which there are adequate margins by taking into account the allowable power dissipation in actual states of use.

4) Shorts between pins and miss-installation

When mounting the LSI on a board, pay adequate attention to orientation and placement discrepancies of the LSI. If it is miss-installed and the power is turned on, the LSI may be damaged. It also may be damaged if it is shorted by a foreign substance coming between pins of the LSI or between a pin and a power supply or a pin and a GND.

5) Operation in strong magnetic fields

Adequately evaluate use in a strong magnetic field, since there is a possibility of malfunction.

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