

N-Channel Lateral DMOS FETs

**SD211DE
SD213DE
SD215DE**

**SST211
SST213
SST215**

Product Summary

Part Number	$V_{(BR)DS}$ Min (V)	$V_{GS(th)}$ Max (V)	$r_{DS(on)}$ Max (Ω)	C_{rss} Max (pF)	t_{ON} Max (ns)
SD211DE	30	1.5	45 @ $V_{GS} = 10$ V	0.5	2
SD213DE	10	1.5	45 @ $V_{GS} = 10$ V	0.5	2
SD215DE	20	1.5	45 @ $V_{GS} = 10$ V	0.5	2
SST211	30	1.5	50 @ $V_{GS} = 10$ V	0.5	2
SST213	10	1.5	50 @ $V_{GS} = 10$ V	0.5	2
SST215	20	1.5	50 @ $V_{GS} = 10$ V	0.5	2

Features

- Ultra-High Speed Switching— t_{ON} : 1 ns
- Ultra-Low Reverse Capacitance: 0.2 pF
- Low Guaranteed r_{DS} @ 5 V
- Low Turn-On Threshold Voltage
- N-Channel Enhancement Mode

Benefits

- High Speed System Performance
- Low Insertion Loss at High Frequencies
- Low Transfer Signal Loss
- Simple Driver Requirement
- Single Supply Operation

Applications

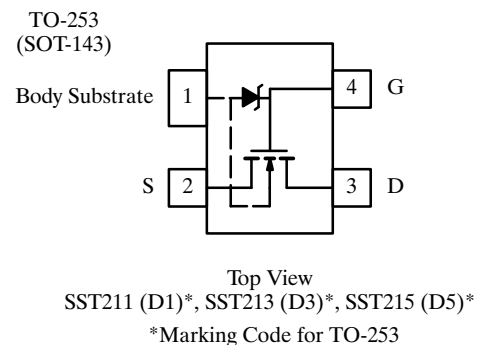
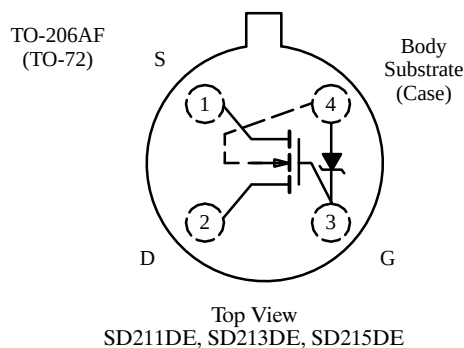
- Fast Analog Switch
- Fast Sample-and-Holds
- Pixel-Rate Switching
- DAC Deglitchers
- High-Speed Driver

Description

The SD211DE/SST211 series consists of enhancement-mode MOSFETs designed for high speed low-glitch switching in audio, video, and high-frequency applications. The SD211 may be used for ± 5 -V analog switching or as a high speed driver of the SD214. The SD214 is normally used for ± 10 -V analog switching. These MOSFETs utilize lateral construction to achieve low capacitance and ultra-fast switching speeds. An

integrated Zener diode provides ESD protection. These devices feature a poly-silicon gate for manufacturing reliability.

For similar products see: quad array—SD5000/5400 series and non-Zener protection—SD210DE/214DE.



Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70295. Applications information may also be obtained via FaxBack, request document #70607.

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

Gate-Drain, Gate-Source Voltage (SD211DE/SST211)	–30/25 V	Source-Substrate Voltage (SD211DE/SST211)	15 V
(SD213DE/SST213)	–15/25 V	(SD213DE/SST213)	15 V
(SD215DE/SST215)	–25/30 V	(SD215DE/SST215)	25 V
Gate-Substrate Voltage ^a (SD211DE/SST211)	–0.3/25 V	Drain Current	50 mA
(SD213DE/SST213)	–0.3/25 V	Lead Temperature ($1/16''$ from case for 10 seconds)	300°C
(SD215DE/SST215)	–0.3/30 V	Storage Temperature	–65 to 150°C
Drain-Source Voltage (SD211DE/SST211)	30 V	Operating Junction Temperature	–55 to 125°C
(SD213DE/SST213)	10 V	Power Dissipation ^a	300 mW
(SD215DE/SST215)	20 V		
Source-Drain Voltage (SD211DE/SST211)	10 V		
(SD213DE/SST213)	10 V		
(SD215DE/SST215)	20 V		
Drain-Substrate Voltage (SD211DE/SST211)	30 V		
(SD213DE/SST213)	15 V		
(SD215DE/SST215)	25 V		

Notes:
a. Derate 3 mW/°C above 25°C

Specifications^a

Parameter	Symbol ^b	Test Conditions ^b		Typ ^c	Limits						Unit
					211 Series		213 Series		215 Series		
					Min	Max	Min	Max	Min	Max	
Static											
Drain-Source Breakdown Voltage	V _{(BR)DS}	V _{GS} = V _{BS} = 0 V, I _D = 10 μA		35	30						V
		V _{GS} = V _{BS} = −5 V, I _D = 10 nA		30	10		10		20		
Source-Drain Breakdown Voltage	V _{(BR)SD}	V _{GD} = V _{BD} = −5 V, I _S = 10 nA		22	10		10		20		
Drain-Substrate Breakdown Voltage	V _{(BR)DBO}	V _{GB} = 0 V, I _D = 10 nA, Source Open		35	15		15		25		
Source-Substrate Breakdown Voltage	V _{(BR)SBO}	V _{GB} = 0 V, I _S = 10 μA, Drain Open		35	15		15		25		
Drain-Source Leakage	I _{DS(off)}	V _{GS} = V _{BS} = −5 V	V _{DS} = 10 V	0.4		10		10			nA
			V _{DS} = 20 V	0.9						10	
Source-Drain Leakage	I _{SD(off)}	V _{GD} = V _{BD} = −5 V	V _{SD} = 10 V	0.5		10		10			
			V _{SD} = 20 V	1						10	
Gate Leakage	I _{GBS}	V _{DB} = V _{SB} = 0 V, V _{GB} = 30V		0.01		100		100		100	
Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 1 μA V _{SB} = 0 V		0.8	0.5	1.5	0.1	1.5	0.1	1.5	V
Drain-Source On-Resistance	r _{DS(on)}	V _{SB} = 0 V I _D = 1 mA	V _{GS} = 5 V (SD Series)	58		70		70		70	Ω
			V _{GS} = 5 V (SST Series)	60		75		75		75	
			V _{GS} = 10 V (SD Series)	38		45		45		45	
			V _{GS} = 10 V (SST Series)	40		50		50		50	
			V _{GS} = 15 V	30							
			V _{GS} = 20 V	26							
			V _{GS} = 25 V	24							

Specifications^a

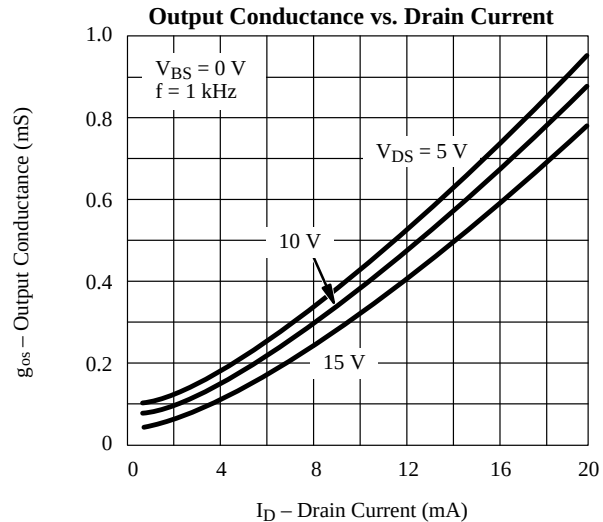
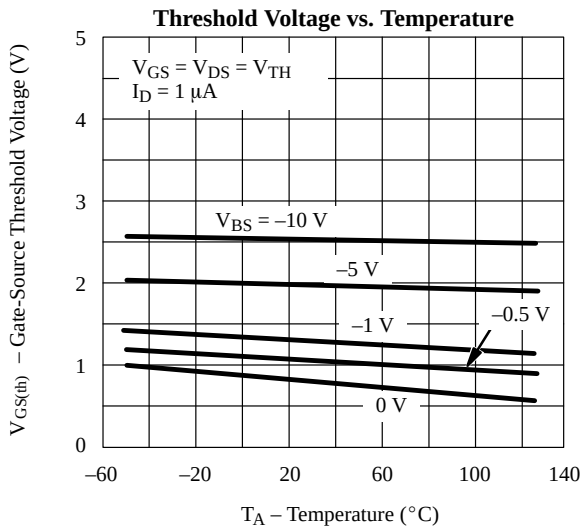
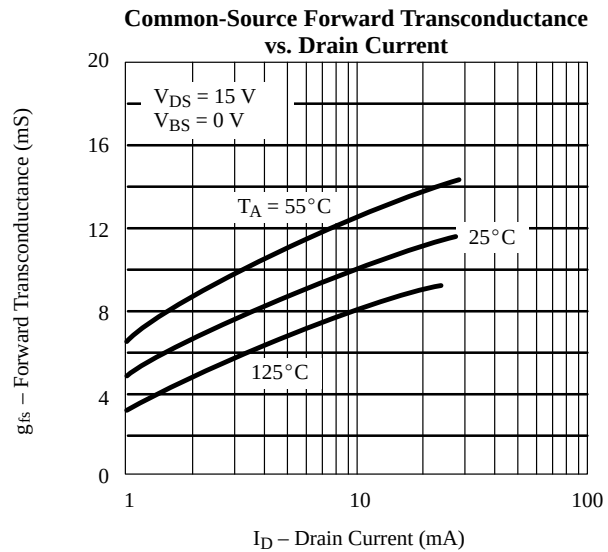
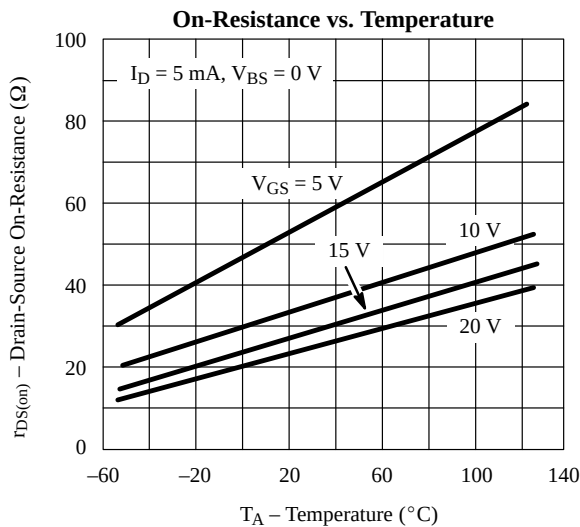
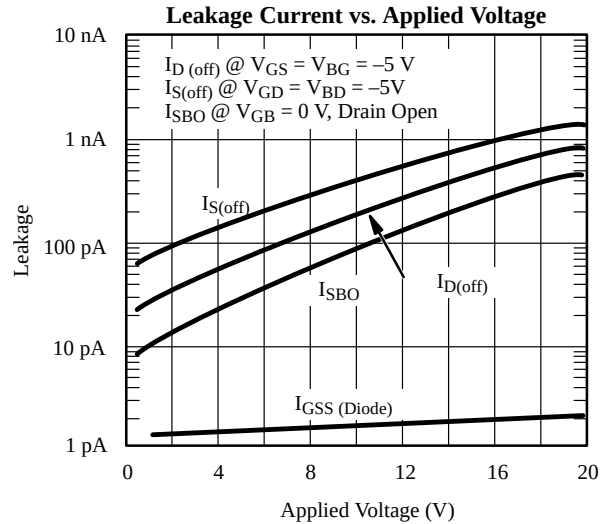
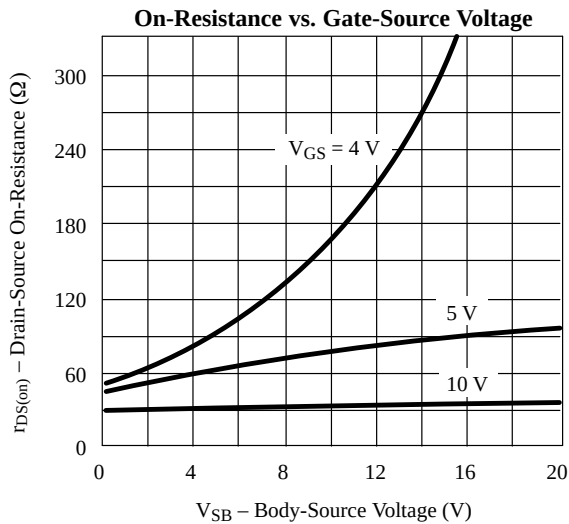
Parameter	Symbol ^b	Test Conditions ^b	Typ ^c	Limits						Unit	
				211 Series		213 Series		215 Series			
				Min	Max	Min	Max	Min	Max		
Dynamic											
Forward Transconductance	g _{fs}	V _{DS} = 10 V V _{SB} = 0 V I _D = 20 mA, f = 1 kHz	SD Series	11	10		10		10		mS
			SST Series	10.5	9		9		9		
	g _{os}		All	0.9							
Gate Node Capacitance	C _(GS+GD+GB)	V _{DS} = 10 V f = 1 MHz V _{GS} = V _{BS} = −15 V	SD Series	2.5		3.5		3.5		3.5	pF
Drain Node Capacitance	C _(GD+DB)			1.1		1.5		1.5		1.5	
Source Node Capacitance	C _(GS+SB)			3.7		5.5		5.5		5.5	
				SST Series	4.2						
Reverse Transfer Capacitance	C _{rss}		SD Series	0.2		0.5		0.5		0.5	
Switching											
Turn-On Time	t _{d(on)}	SD Series Only V _{SB} = 0 V, V _{IN} 0 to 5 V, R _G = 25 Ω V _{DD} = 5 V, R _L = 680 Ω		0.5		1		1		1	ns
	t _r			0.6		1		1		1	
Turn-Off Time	t _{d(off)}			2							
	t _f			6							

Notes:

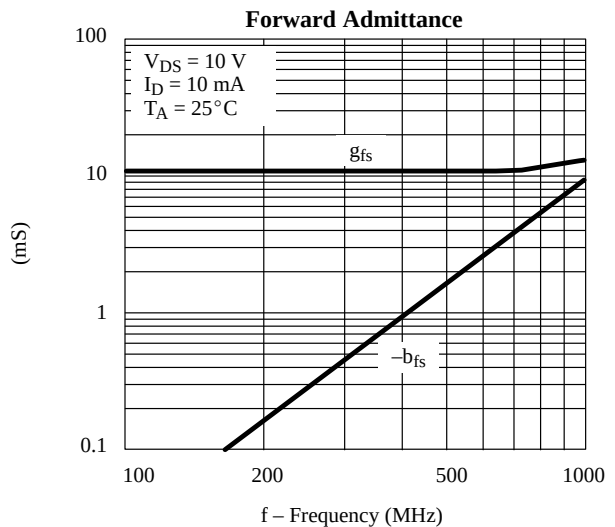
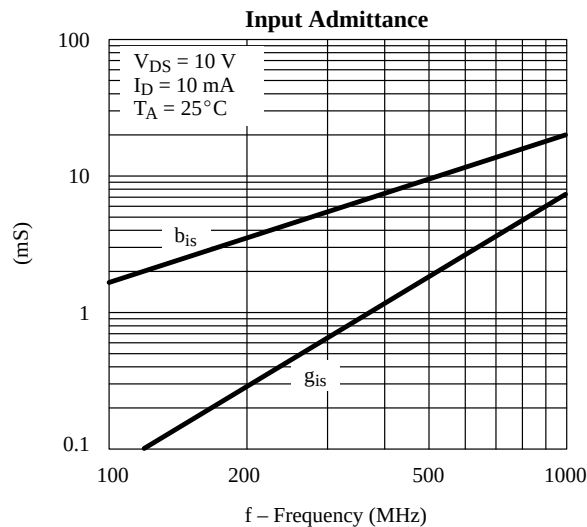
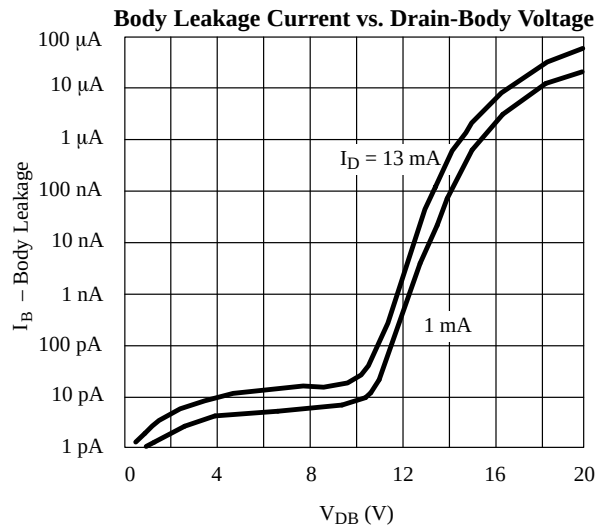
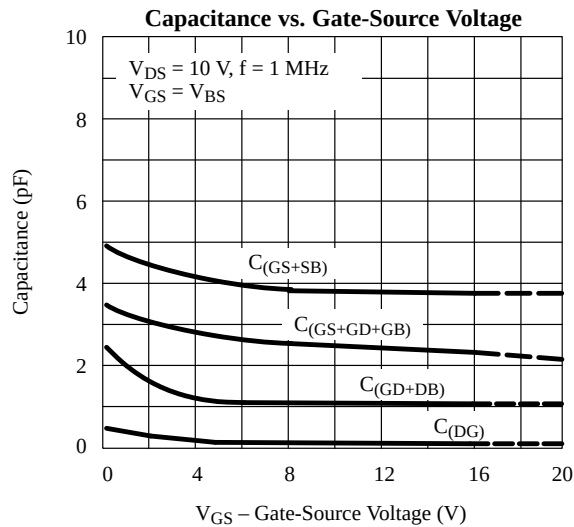
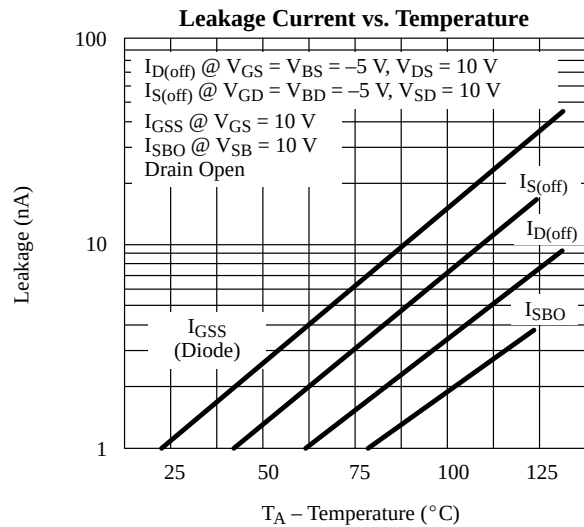
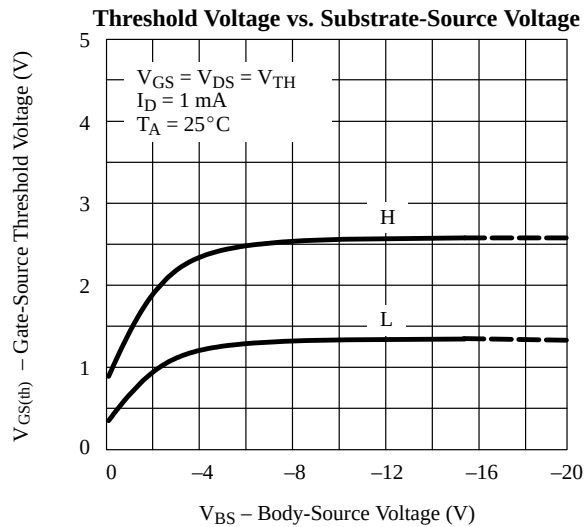
- $T_A = 25^\circ\text{C}$ unless otherwise noted.
- B is the body (substrate), and (BR) is breakdown.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

DMCBA

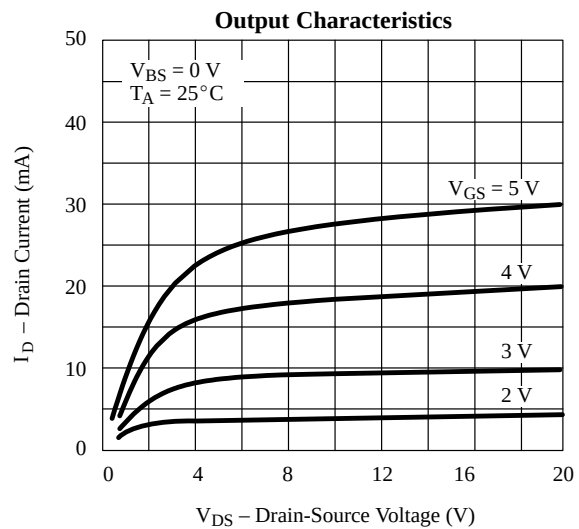
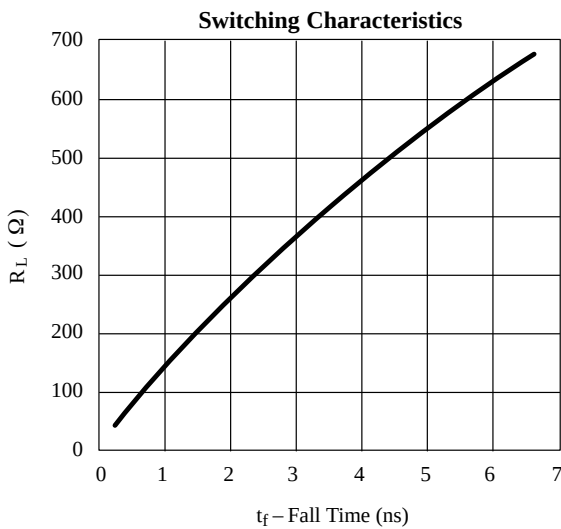
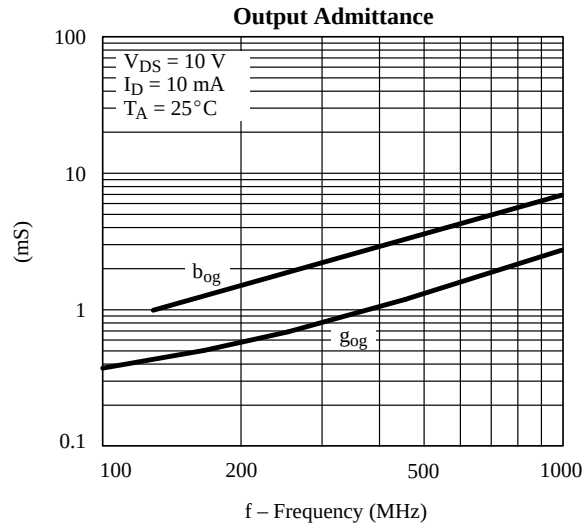
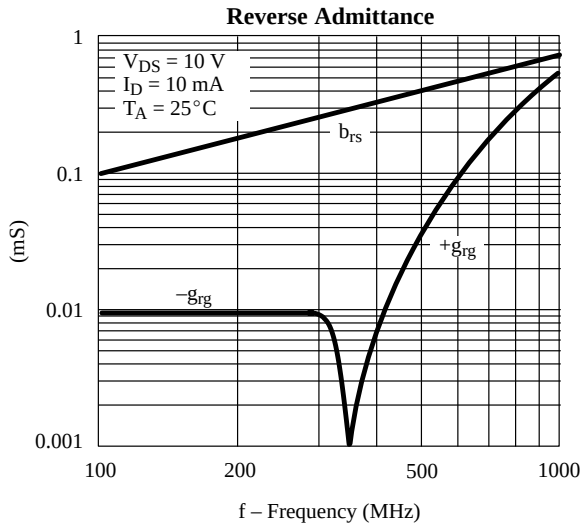
Typical Characteristics



Typical Characteristics (Cont'd)



Typical Characteristics



Switching Time Test Circuit

