



2Mx8 MONOLITHIC FLASH, SMD 5962-97609

FEATURES

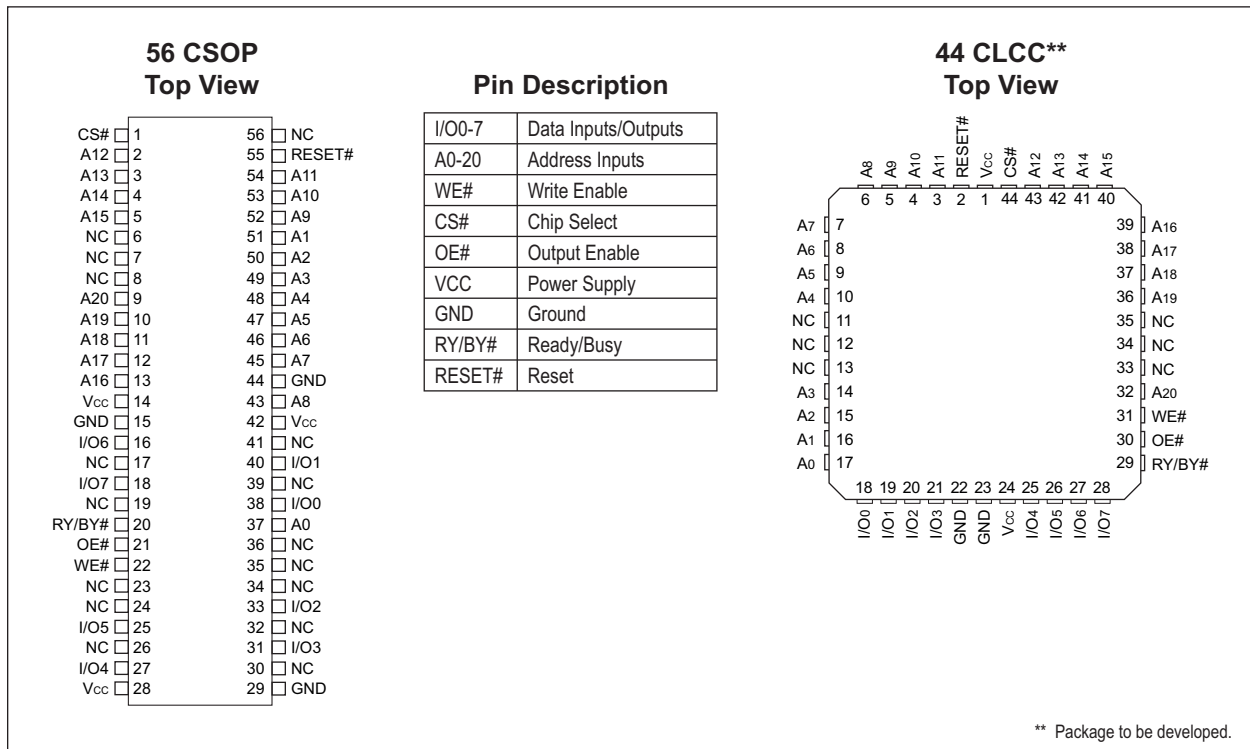
- Access Times of 90, 120, 150ns
- Packaging:
 - 56 lead, Hermetic Ceramic, 0.520" CSOP (Package 207). Fits standard 56 SSOP footprint.
 - 44 pin Ceramic LCC**
- Sector Architecture
 - 32 equal size sectors of 64KBytes each
 - Any combination of sectors can be erased. Also supports full chip erase.
- 100,000 Write/Erase Cycles Minimum
- Organized as 2Mx8
- Commercial, Industrial, and Military Temperature Ranges
- 5V Read and Write. 5V ± 10% Supply.
- Low Power CMOS
- Data# Polling and Toggle Bit feature for detection of program or erase cycle completion.
- Supports reading or programming data to a sector not being erased.
- RESET# pin resets internal state machine to the read mode.
- Multiple Ground Pins for Low Noise Operation

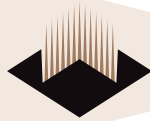
* This data sheet describes a product that is subject to change without notice.

** Package to be developed.

Note: For programming information refer to Flash Programming 16M5 Application Note.

Fig. 1 – Pin Configuration for WMF2M8-XXX5





ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Ratings	Unit
Voltage on Any Pin Relative to V _{SS}	V _T	-2.0 to +7.0	V
Power Dissipation	P _T	8	W
Storage Temperature	T _{STG}	-65 to +125	°C
Short Circuit Output Current	I _{OS}	100	mA
Endurance - Write/Erase Cycles (Mil Temp)		100,000 min	cycles
Data Retention (Mil Temp)		20	years

CAPACITANCE

T_A = +25°C

Parameter	Symbol	Conditions	Max	Unit
Address Input capacitance	CAD	V _{I/O} = 0 V, f = 1.0MHz	12	pF
Output Enable capacitance	COE	V _{IN} = 0 V, f = 1.0MHz	12	pF
Write Enable capacitance	CWE	V _{IN} = 0 V, f = 1.0MHz	12	pF
Chip Select capacitance	CCS	V _{IN} = 0 V, f = 1.0MHz	12	pF
Data I/O capacitance	CI/O	V _{I/O} = 0 V, f = 1.0MHz	12	pF

This parameter is guaranteed by design but not tested.

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	4.5	5.0	5.5	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.0	-	V _{CC} + 0.5	V
Input Low Voltage	V _{IL}	-0.5	-	+0.8	V
Operating Temperature (Mil.)	T _A	-55	-	+125	°C
Operating Temperature (Ind.)	T _A	-40	-	+85	°C

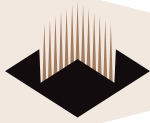
DC CHARACTERISTICS — CMOS COMPATIBLE

V_{CC} = 5.0V, V_{SS} = 0V, -55°C ≤ T_A ≤ +125°C

Parameter	Symbol	Conditions	Min	Max	Unit
Input Leakage Current	I _{LI}	V _{CC} = 5.5, V _{IN} = GND to V _{CC}		10	µA
Output Leakage Current	I _{LO}	V _{CC} = 5.5, V _{IN} = GND to V _{CC}		10	µA
V _{CC} Active Current for Read (1)	I _{CC1}	CS# = V _{IL} , OE# = V _{IH} , f = 5MHz		40	mA
V _{CC} Active Current for Program or Erase (2)	I _{CC2}	CS# = V _{IL} , OE# = V _{IH}		60	mA
V _{CC} Standby Current	I _{CC3}	V _{CC} = 5.5, CS# = V _{IH} , f = 5MHz, RESET# = V _{CC} ± 0.3V		2.0	mA
Output Low Voltage	V _{OL}	I _{OL} = 12.0 mA, V _{CC} = 4.5		0.45	V
Output High Voltage	V _{OH}	I _{OH} = -2.5 mA, V _{CC} = 4.5	0.85xV _{CC}		V
Low V _{CC} Lock-Out Voltage	V _{LKO}		3.2	4.2	V

NOTES:

1. The I_{CC} current listed includes both the DC operating current and the frequency dependent component (@ 5MHz). The frequency component typically is less than 2mA/MHz, with OE# at V_{IH}.
2. I_{CC} active while Embedded Algorithm (program or erase) is in progress.
3. DC test conditions V_{IL} = 0.3V, V_{IH} = V_{CC} - 0.3V



AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS – WE# CONTROLLED

V_{CC} = 5.0V, V_{SS} = 0V, -55°C ≤ T_A ≤ +125°C

Parameter	Symbol		-90		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	
Write Cycle Time	t _{AVAV}	t _{WC}	90		120		150		ns
Chip Select Setup Time	t _{ELWL}	t _{CS}	0		0		0		ns
Write Enable Pulse Width	t _{WLWH}	t _{WP}	45		50		50		ns
Address Setup Time	t _{AVWL}	t _{AS}	0		0		0		ns
Data Setup Time	t _{DVWH}	t _{DS}	45		50		50		ns
Data Hold Time	t _{WHDX}	t _{DH}	0		0		0		ns
Address Hold Time	t _{WLAX}	t _{AH}	45		50		50		ns
Write Enable Pulse Width High	t _{WHWL}	t _{WPH}	20		20		20		ns
Duration of Byte Programming Operation (1)	t _{WHWH1}			300		300		300	µs
Sector Erase (2)	t _{WHWH2}			15		15		15	sec
Read Recovery Time before Write	t _{GHWL}		0		0		0		µs
V _{CC} Setup Time	t _{VCS}		50		50		50		µs
Chip Programming Time				44		44		44	sec
Chip Erase Time (3)				256		256		256	sec
Output Enable Hold Time (4)		t _{OE}	10		10		10		ns
RESET# Pulse Width		t _{RP}	500		500		500		ns

NOTES:

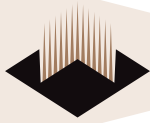
1. Typical value for t_{WHWH1} is 7µs.
2. Typical value for t_{WHWH2} is 1sec.
3. Typical value for Chip Erase Time is 32sec.
4. For Toggle and Data Polling.

AC CHARACTERISTICS – READ-ONLY OPERATIONS

V_{CC} = 5.0V, V_{SS} = 0V, -55°C ≤ T_A ≤ +125°C

Parameter	Symbol		-90		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	
Read Cycle Time	t _{AVAV}	t _{RC}	90		120		150		ns
Address Access Time	t _{AVQV}	t _{ACC}		90		120		150	ns
Chip Select Access Time	t _{ELQV}	t _{CE}		90		120		150	ns
Output Enable to Output Valid	t _{GLQV}	t _{OE}		40		50		55	ns
Output Enable Hold Time	Read Toggle & Data Polling	t _{OE}	0		0		0		ns
			10		10		10		ns
Chip Select High to Output High Z (1)	t _{EHQZ}	t _{DF}		20		30		35	ns
Output Enable High to Output High Z (1)	t _{GHQZ}	t _{DF}		20		30		35	ns
Output Hold from Addresses, CS# or OE# Change, whichever is First	t _{AXQX}	t _{OH}	0		0		0		ns
RESET# Low to Read Mode (1)		t _{Ready}		20		20		20	µs

1. Guaranteed by design, not tested.



AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS, CS# CONTROLLED

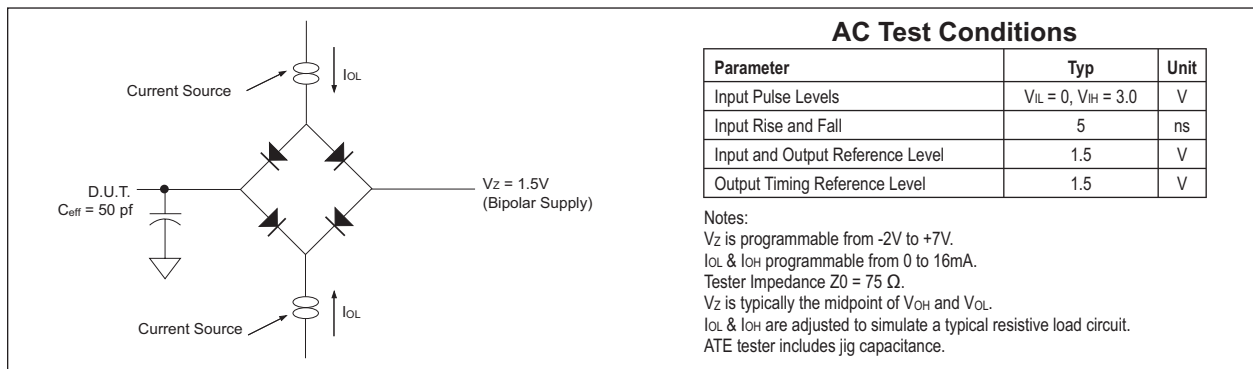
$V_{CC} = 5.0V, V_{SS} = 0V, V_{SS} = 0V, -55^{\circ}C \leq T_A \leq +125^{\circ}C$

Parameter	Symbol		-90		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{AVAV}	t_{WC}	90		120		150		ns
Write Enable Setup Time	t_{WLEL}	t_{WS}	0		0		0		ns
Chip Select Pulse Width	t_{ELEH}	t_{CP}	45		50		50		ns
Address Setup Time	t_{AVEL}	t_{AS}	0		0		0		ns
Data Setup Time	t_{DVEH}	t_{DS}	45		50		50		ns
Data Hold Time	t_{EHDX}	t_{DH}	0		0		0		ns
Address Hold Time	t_{ELAX}	t_{AH}	45		50		50		ns
Chip Select Pulse Width High	t_{EHEL}	t_{CPH}	20		20		20		ns
Duration of Byte Programming Operation (1)	t_{WHWH1}			300		300		300	μs
Sector Erase Time (2)	t_{WHWH2}			15		15		15	sec
Read Recovery Time	t_{GHEL}		0		0		0		μs
Chip Programming Time				44		44		44	sec
Chip Erase Time (3)				256		256		256	sec
Output Enable Hold Time (4)		t_{OEH}	10		10		10		ns

NOTES:

1. Typical value for t_{WHWH1} is 7 μs .
2. Typical value for t_{WHWH2} is 1sec.
3. Typical value for Chip Erase Time is 32sec.
4. For Toggle and Data Polling.

FIGURE 2 – AC TEST CIRCUIT



HARDWARE RESET (RESET#)

Parameter				
Std	Description	Test Setup	All Speed Options	Unit
t_{READY}	RESET Pin Low (During Embedded Algorithms) to Read or Write (See Note)	Max	20	μs
t_{READY}	RESET Pin Low (Not During Embedded Algorithms) to Read or Write (See Note)	Max	500	ns
t_{RP}	RESET Pulse Width	Min	500	ns
t_{RH}	RESET High Time Before Read (See Note)	Min	50	ns
t_{RB}	RY/BY Recovery Time	Min	0	ns

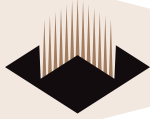
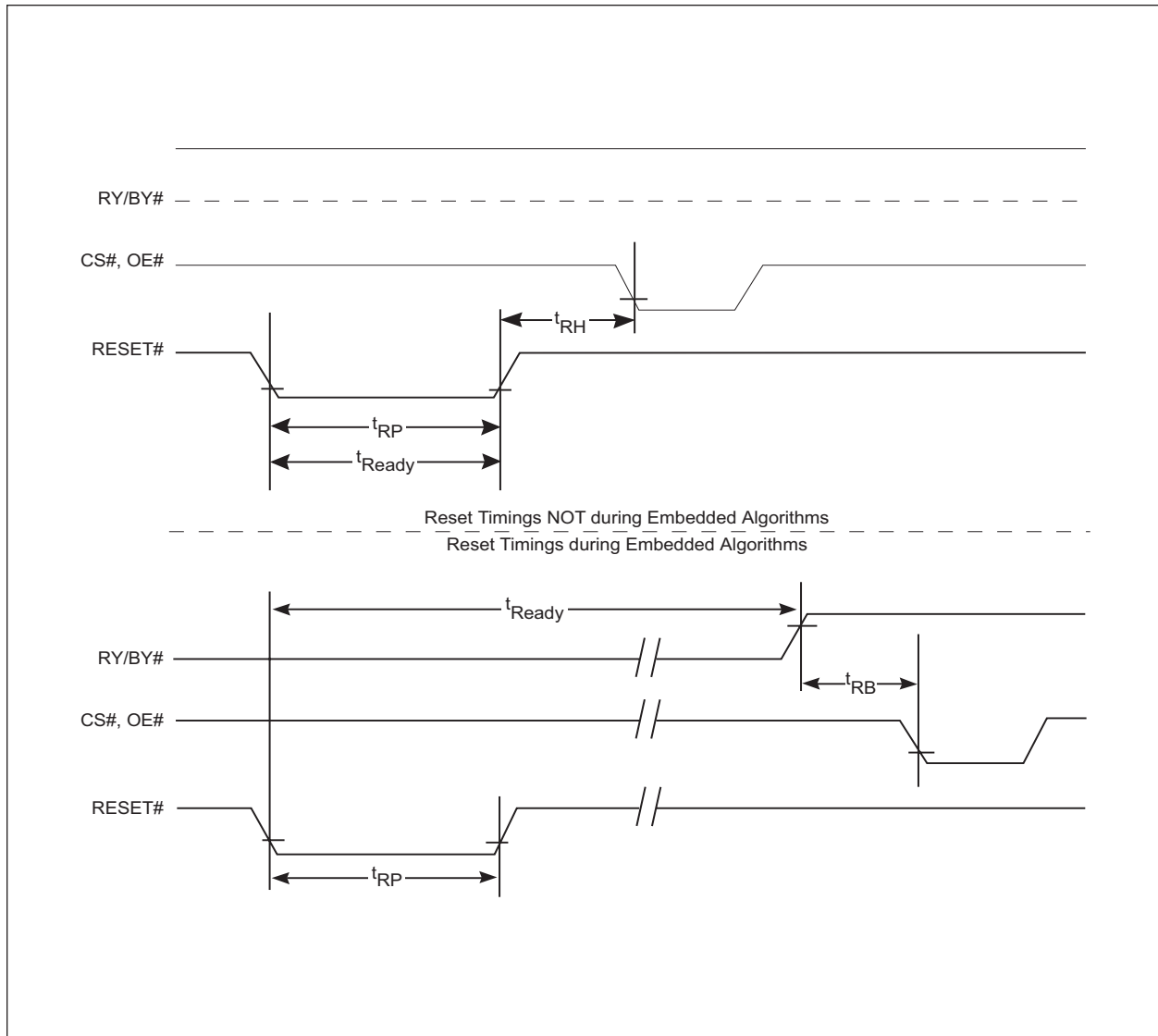


FIGURE 3 – RESET# TIMING



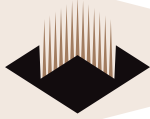
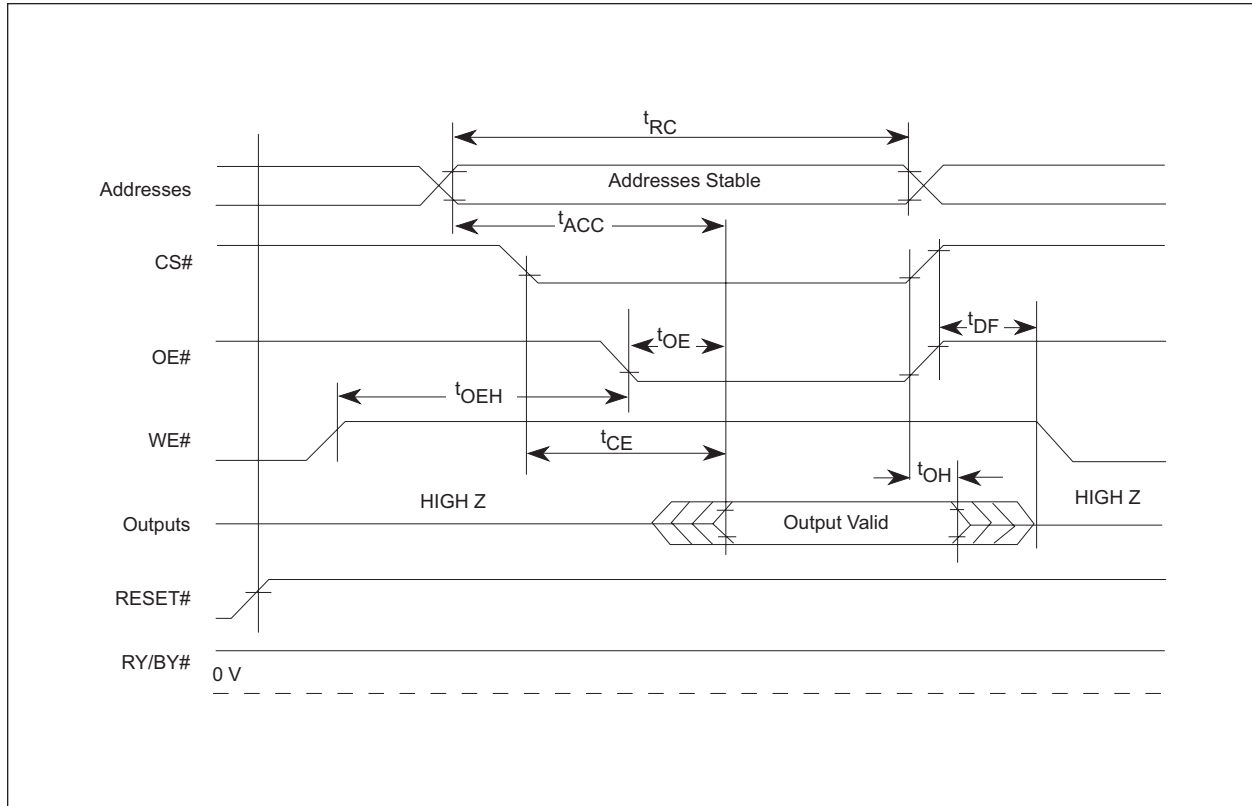


FIGURE 4 – AC WAVEFORMS FOR READ OPERATIONS



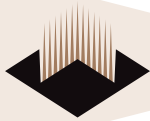
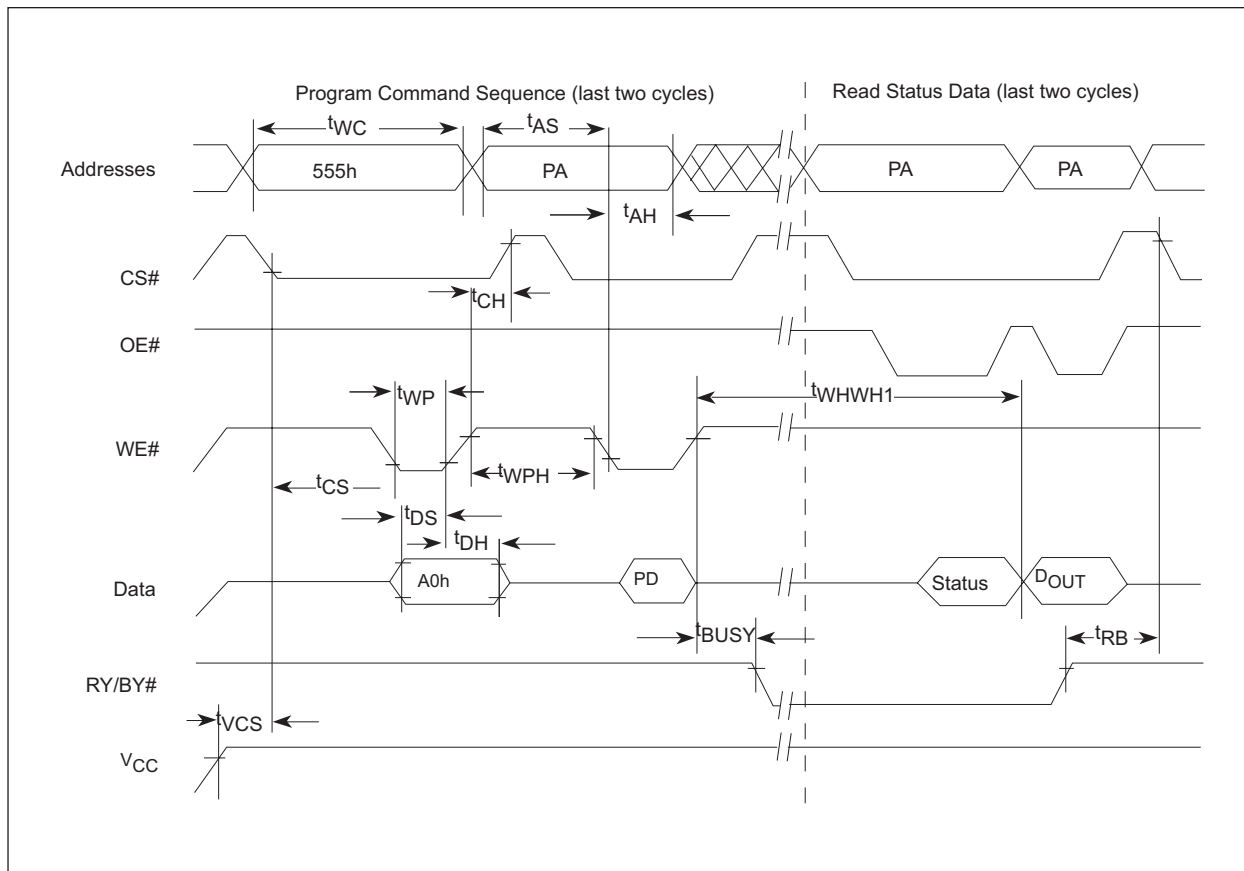


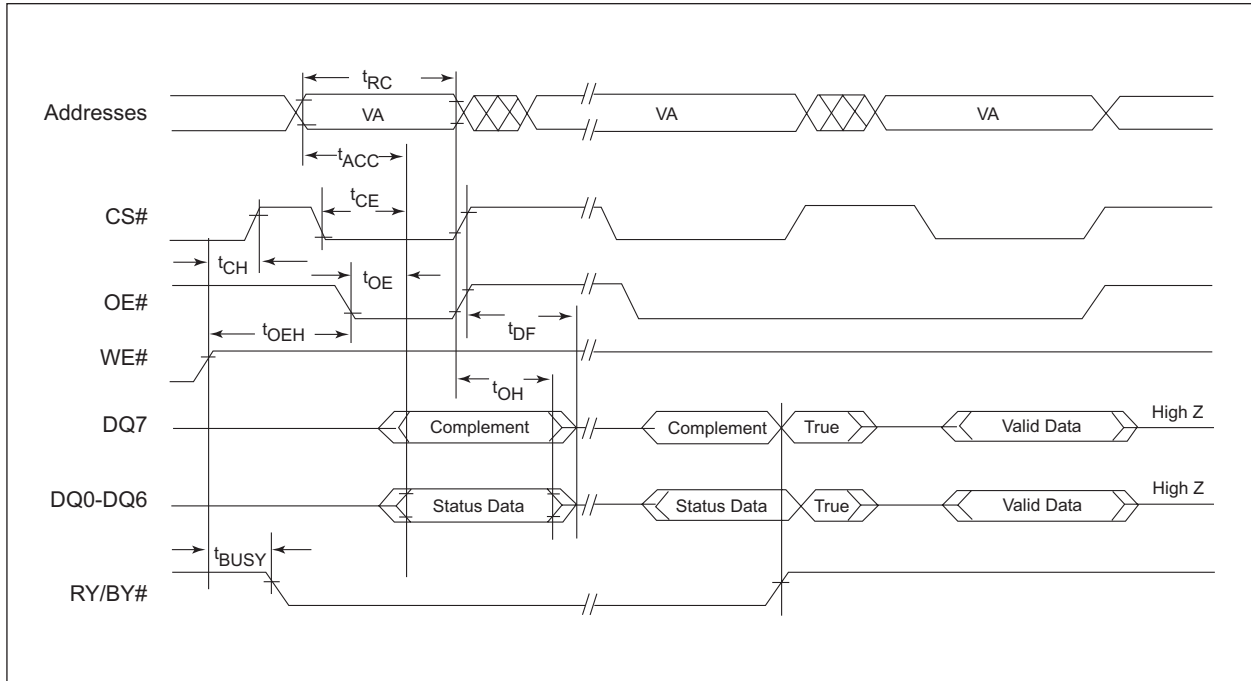
FIGURE 5 – WRITE/ERASE/PROGRAM OPERATION, WE# CONTROLLED



- Notes:
1. PA represents the address of the memory location to be programmed.
 2. PD represents the data to be programmed at byte address.
 3. D7# is the output of the complement of the data written to the device.
 4. DOUT is the output of the data written to the device.
 5. Figure indicates last two bus cycles of a four bus cycle sequence.



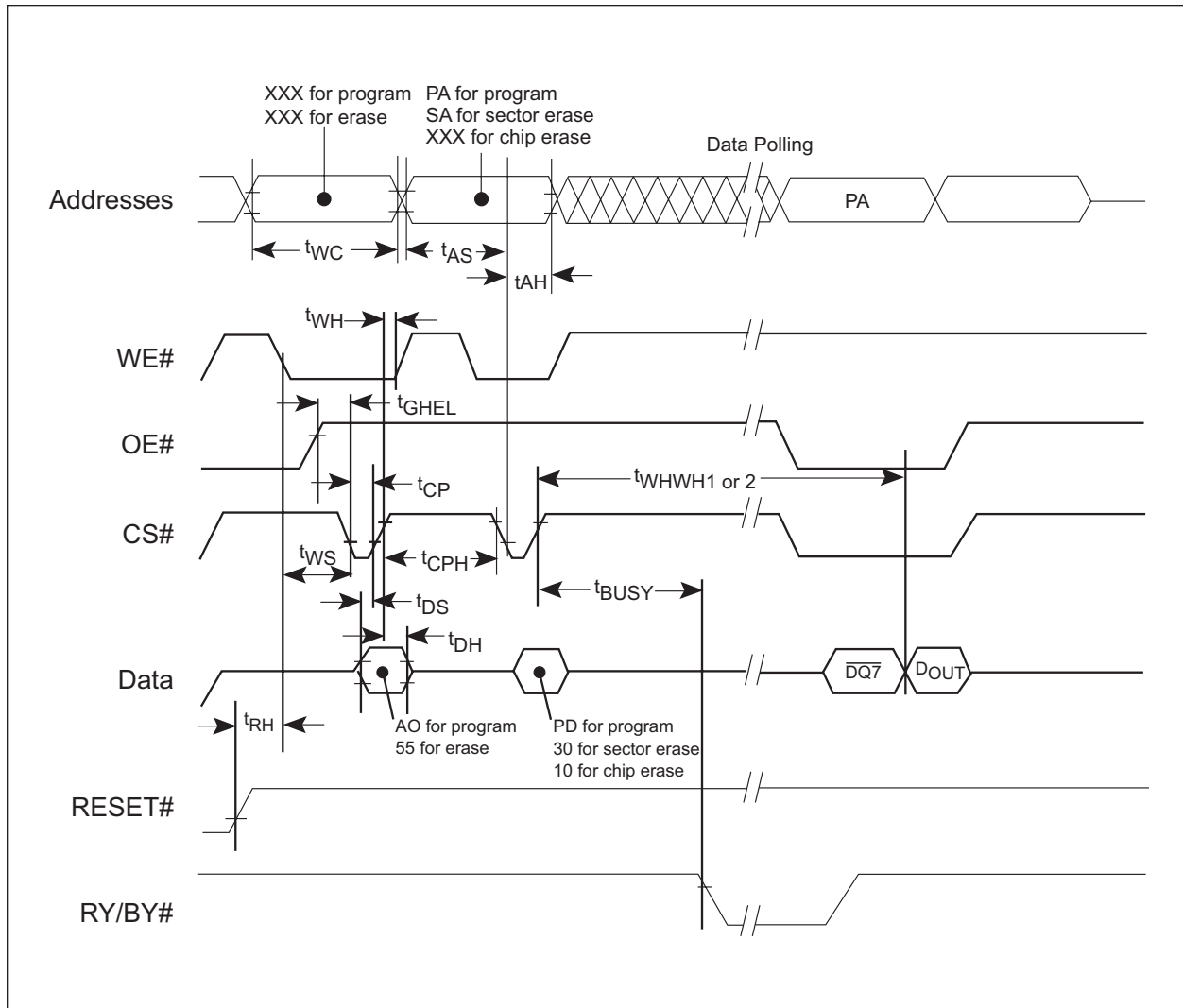
FIG. 7 – AC WAVEFORMS FOR DATA# POLLING DURING EMBEDDED ALGORITHM OPERATIONS



Notes: VA = Valid Address. Illustration shows first status cycle after command sequence, last status read cycle and array data read cycle.



FIGURE 8 – ALTERNATE CS# CONTROLLED PROGRAMMING OPERATION TIMINGS

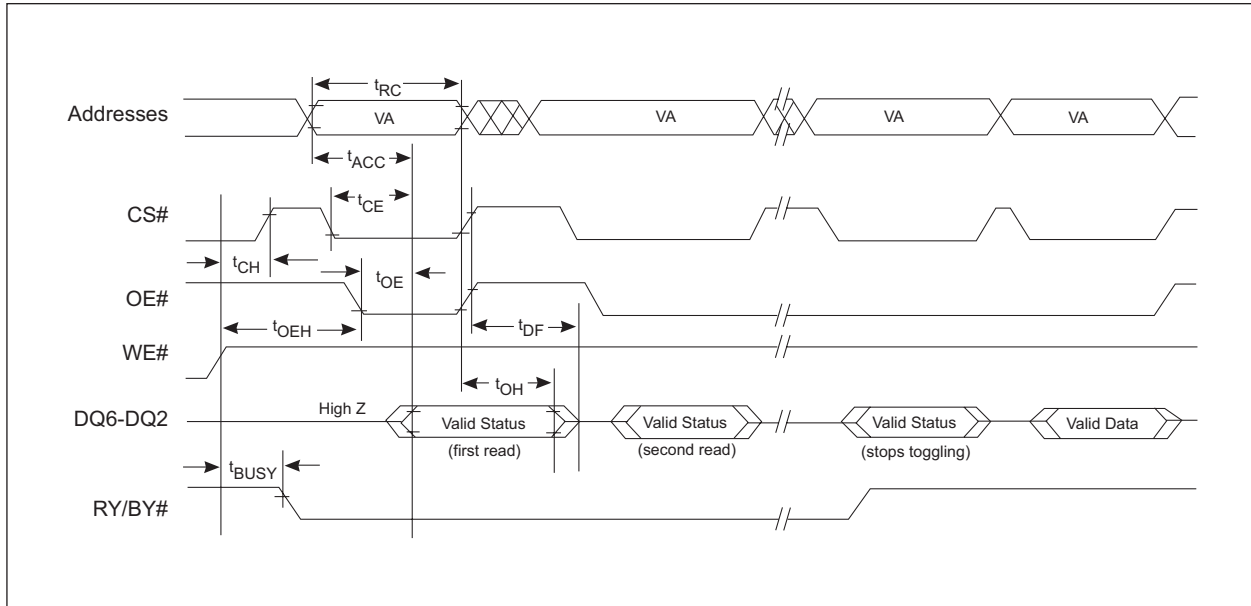


Notes:

1. PA represents the address of the memory location to be programmed.
2. PD represents the data to be programmed at byte address.
3. D7# is the output of the complement of the data written to the device.
4. DOUT is the output of the data written to the device.
5. Figure indicates last two bus cycles of a four bus cycle sequence.



FIGURE 9 – TOGGLE BIT TIMINGS (DURING EMBEDDED ALGORITHMS)

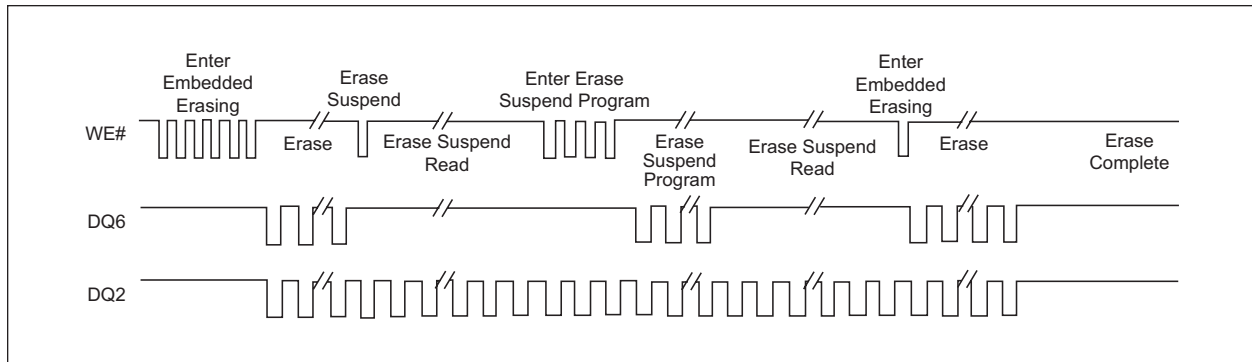


Notes:

VA = Valid address; not required for DQ6. Illustration shows first two status cycle after command sequence, last status read cycle and array data read cycle.



FIGURE 10 – DQ2 VS. DQ6



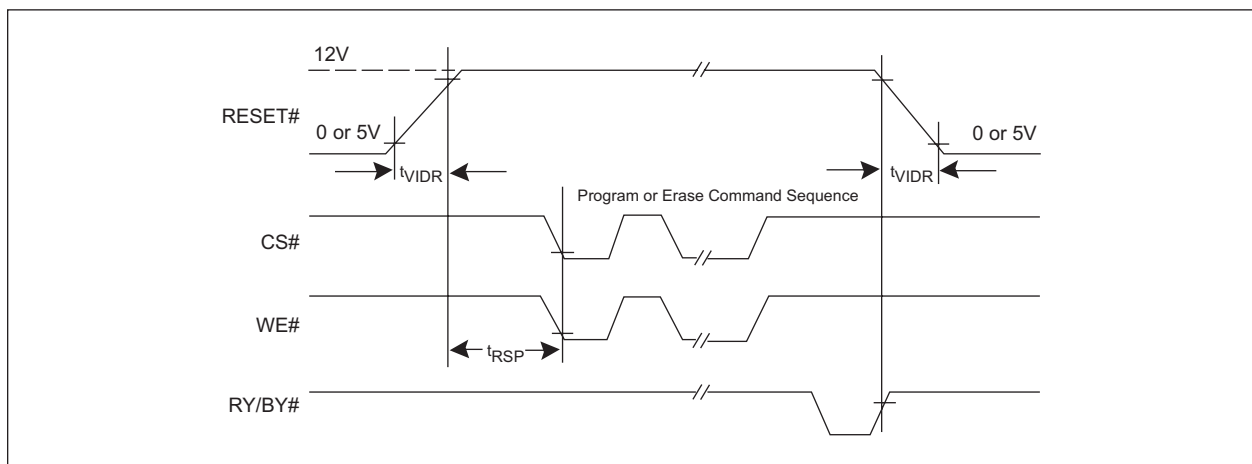
Note:
The system may use OE# or CS# to toggle DQ2 and DQ6. DQ6 toggles only when read at an address within the erase-suspended sector.

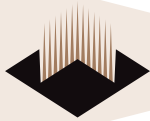
TEMPORARY SECTOR UNPROTECTED

Parameter	Description		All Speed Options	Unit
t _{VIDR}	V _{ID} Rise and Fall time (see notes)	Min	500	ns
t _{RSP}	RESET# setup time for temporary sector unprotect	Min	4	ms

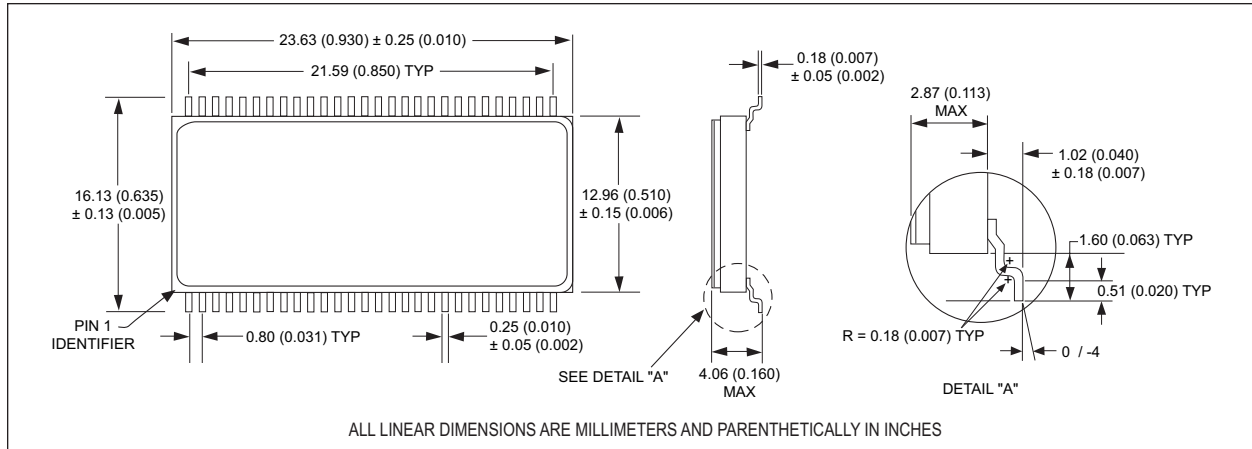
Note:
Not 100% tested.

FIGURE 11 – TEMPORARY SECTOR GROUP UNPROTECTED TIMINGS

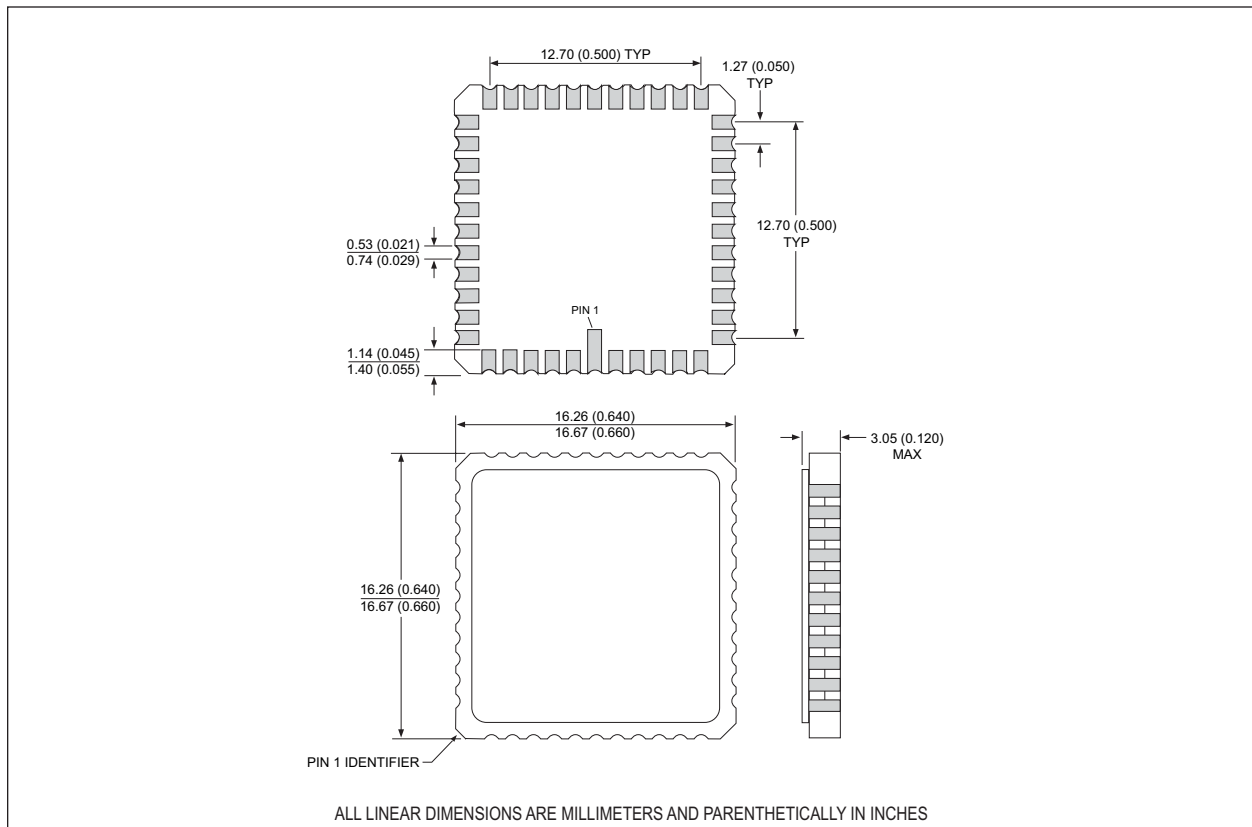




PACKAGE 207: 56 LEAD, CERAMIC SOP



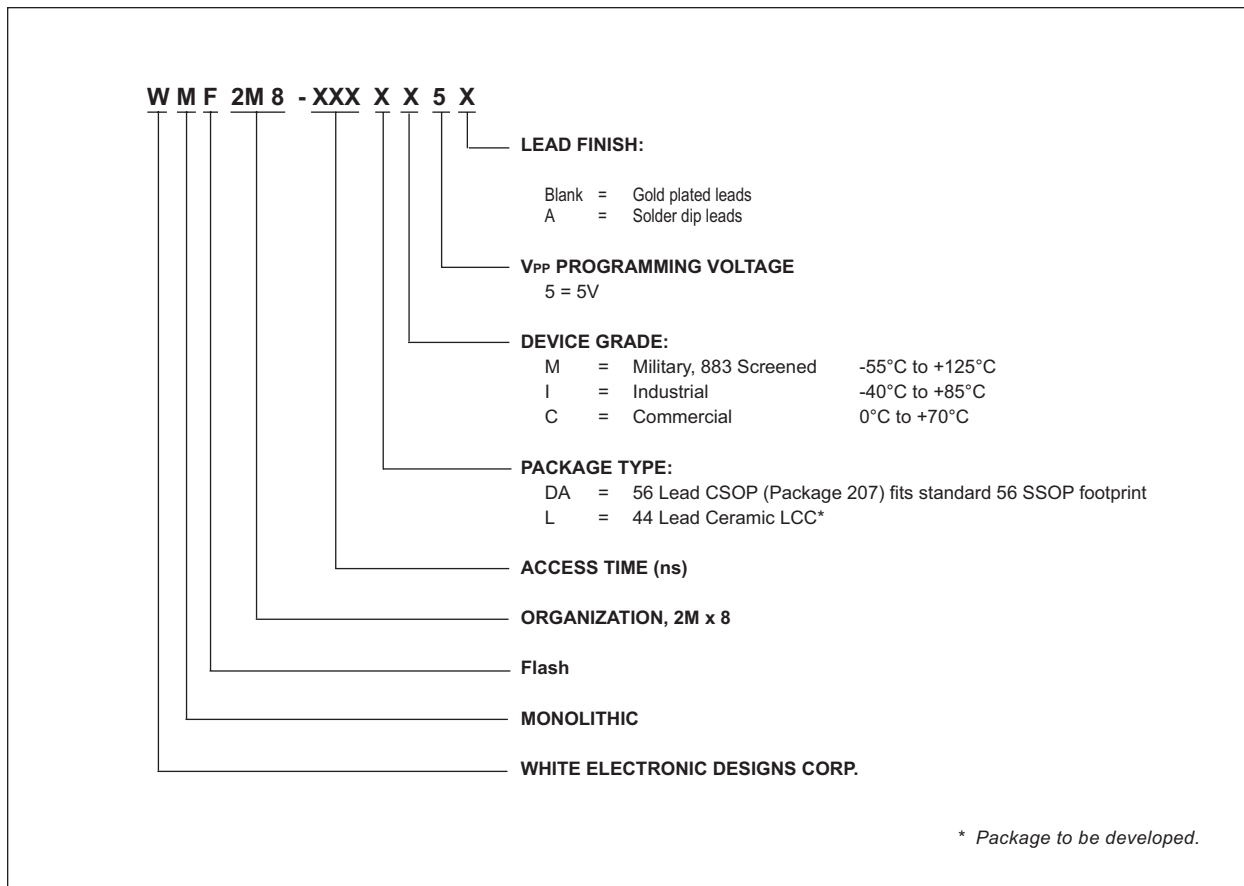
PACKAGE DIMENSION: 44 LEAD, CERAMIC LCC**



** Package to be developed.



ORDERING INFORMATION



Device Type	Sector Size	Speed	Package	SMD No.
2M x 8 Flash Monolithic	64KByte	150ns	56 lead CSOP (DA)	5962-97609 01HXX
2M x 8 Flash Monolithic	64KByte	120ns	56 lead CSOP (DA)	5962-97609 02HXX
2M x 8 Flash Monolithic	64KByte	90ns	56 lead CSOP (DA)	5962-97609 03HXX