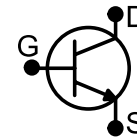


**Normally – OFF Silicon Carbide Junction Transistor**

|                                  |   |        |
|----------------------------------|---|--------|
| $V_{DS}$                         | = | 1200 V |
| $R_{DS(ON)}$                     | = | 100 mΩ |
| $I_D @ 25\text{ }^\circ\text{C}$ | = | 25 A   |
| $h_{FE}$                         | = | 80     |

**Features**

- 210 °C Maximum Operating Temperature
- Gate Oxide Free SiC Switch
- Exceptional Safe Operating Area
- Excellent Gain Linearity
- Temperature Independent Switching Performance
- Low Output Capacitance
- Positive Temperature Coefficient of  $R_{DS,ON}$
- Suitable for Connecting an Anti-parallel Diode



Die Size = 2.10 mm x 2.10 mm

**Advantages**

- Compatible with Si MOSFET/IGBT Gate Drive ICs
- > 20 μs Short-Circuit Withstand Capability
- Lowest-in-class Conduction Losses
- High Circuit Efficiency
- Minimal Input Signal Distortion
- High Amplifier Bandwidth

**Applications**

- Down Hole Oil Drilling, Geothermal Instrumentation
- Hybrid Electric Vehicles (HEV)
- Solar Inverters
- Switched-Mode Power Supply (SMPS)
- Power Factor Correction (PFC)
- Induction Heating
- Uninterruptible Power Supply (UPS)
- Motor Drives

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**Section I: Absolute Maximum Ratings**

( $T_C = 25\text{ }^\circ\text{C}$  unless otherwise specified)

| Parameter                                  | Symbol         | Conditions  | Value   | Unit | Notes   |
|--|----------------|---|---|------|---------|
| Drain – Source Voltage                     | $V_{DS}$       | $V_{GS} = 0\text{ V}$   | 1200  | V    |         |
| Continuous Drain Current                   | $I_D$          | $T_C = 25\text{ }^\circ\text{C}$  | 25  | A    |         |
| Continuous Drain Current                   | $I_D$          | $T_C > 125\text{ }^\circ\text{C}$ , assumes $R_{thJC} < 0.88\text{ }^\circ\text{C/W}$                   | 10  | A    |         |
| Continuous Gate Current                    | $I_G$          |   | 1.3   | A    |         |
| Turn-Off Safe Operating Area               | RBSOA          | $T_{VJ} = 210\text{ }^\circ\text{C}$ ,<br>Clamped Inductive Load  | $I_{D,max} = 10$<br>@ $V_{DS} \leq V_{DSmax}$ | A    | Fig. 16 |
| Short Circuit Safe Operating Area          | SCSOA          | $T_{VJ} = 210\text{ }^\circ\text{C}$ , $I_G = 1\text{ A}$ , $V_{DS} = 800\text{ V}$ ,<br>Non Repetitive | >20   | μs   |         |
| Reverse Gate – Source Voltage              | $V_{SG}$       |   | 30  | V    |         |
| Reverse Drain – Source Voltage             | $V_{SD}$       |   | 25  | V    |         |
| Operating Junction and Storage Temperature | $T_j, T_{stg}$ |   | -55 to 210                                    | °C   |         |
| Maximum Processing Temperature             | $T_{Proc}$     | 10 min. maximum   | 325   | °C   |         |

## Section II: Static Electrical Characteristics

| Parameter                        | Symbol       | Conditions   | Value |         |      | Unit | Notes  |
|----------------------------------|--------------|--|-------|---------|------|------|--------|
|                                  |              |  | Min.  | Typical | Max. |      |        |
| <b>A: On State</b>               |              |  |       |         |      |      |        |
| Drain – Source On Resistance     | $R_{DS(ON)}$ | $I_D = 10\text{ A}, T_J = 25\text{ °C}$                            |       | 100     |      | mΩ   | Fig. 4 |
|                                  |              | $I_D = 10\text{ A}, T_J = 150\text{ °C}$                           |       | 160     |      |      |        |
|                                  |              | $I_D = 10\text{ A}, T_J = 175\text{ °C}$                           |       | 180     |      |      |        |
| Gate – Source Saturation Voltage | $V_{GS,SAT}$ | $I_D = 10\text{ A}, I_D/I_G = 40, T_J = 25\text{ °C}$              |       | 3.50    |      | V    | Fig. 7 |
|                                  |              | $I_D = 10\text{ A}, I_D/I_G = 30, T_J = 175\text{ °C}$             |       | 3.27    |      |      |        |
| DC Current Gain                  | $h_{FE}$     | $V_{DS} = 8\text{ V}, I_D = 10\text{ A}, T_J = 25\text{ °C}$       |       | 80      |      | –    | Fig. 5 |
|                                  |              | $V_{DS} = 8\text{ V}, I_D = 10\text{ A}, T_J = 125\text{ °C}$      |       | 55      |      |      |        |
|                                  |              | $V_{DS} = 8\text{ V}, I_D = 10\text{ A}, T_J = 175\text{ °C}$      |       | 50      |      |      |        |
| <b>B: Off State</b>              |              |  |       |         |      |      |        |
| Drain Leakage Current            | $I_{DSS}$    | $V_{DS} = 1200\text{ V}, V_{GS} = 0\text{ V}, T_J = 25\text{ °C}$  |       | 1       |      | μA   | Fig. 8 |
|                                  |              | $V_{DS} = 1200\text{ V}, V_{GS} = 0\text{ V}, T_J = 150\text{ °C}$ |       | 1       |      |      |        |
|                                  |              | $V_{DS} = 1200\text{ V}, V_{GS} = 0\text{ V}, T_J = 175\text{ °C}$ |       | 2       |      |      |        |
| Gate Leakage Current             | $I_{SG}$     | $V_{SG} = 20\text{ V}, T_J = 25\text{ °C}$                         |       | 20      |      | nA   |        |

## Section III: Dynamic Electrical Characteristics

| Parameter                                    | Symbol            | Conditions   | Value |         |      | Unit | Notes       |
|--|-------------------|--|-------|---------|------|------|-------------|
|  |                   |  | Min.  | Typical | Max. |      |             |
| <b>A: Capacitance and Gate Charge</b>        |                   |  |       |         |      |      |             |
| Input Capacitance                            | $C_{ISS}$         | $V_{GS} = 0\text{ V}, V_{DS} = 800\text{ V}, f = 1\text{ MHz}$                 |       | 1275    |      | pF   | Fig. 9      |
| Reverse Transfer/Output Capacitance          | $C_{RSS}/C_{OSS}$ | $V_{DS} = 800\text{ V}, f = 1\text{ MHz}$                                      |       | 30      |      | pF   | Fig. 9      |
| Output Capacitance Stored Energy             | $E_{OSS}$         | $V_{GS} = 0\text{ V}, V_{DS} = 800\text{ V}, f = 1\text{ MHz}$                 |       | 12      |      | μJ   | Fig. 10     |
| Effective Output Capacitance, time related   | $C_{OSS,tr}$      | $I_D = \text{constant}, V_{GS} = 0\text{ V}, V_{DS} = 0\text{...}800\text{ V}$ |       | 55      |      | pF   |             |
| Effective Output Capacitance, energy related | $C_{OSS,er}$      | $V_{GS} = 0\text{ V}, V_{DS} = 0\text{...}800\text{ V}$                        |       | 40      |      | pF   |             |
| Gate-Source Charge                           | $Q_{GS}$          | $V_{GS} = -5\text{...}3\text{ V}$  |       | 11      |      | nC   |             |
| Gate-Drain Charge                            | $Q_{GD}$          | $V_{GS} = 0\text{ V}, V_{DS} = 0\text{...}800\text{ V}$                        |       | 55      |      | nC   |             |
| Gate Charge - Total                          | $Q_G$             |  |       | 66      |      | nC   |             |
| <b>B: Switching<sup>1</sup></b>              |                   |  |       |         |      |      |             |
| Internal Gate Resistance – ON                | $R_{G(INT-ON)}$   | $V_{GS} > 2.5\text{ V}, V_{DS} = 0\text{ V}, T_J = 175\text{ °C}$              |       | 0.19    |      | Ω    |             |
| Turn On Delay Time                           | $t_{d(on)}$       | $T_J = 25\text{ °C}, V_{DS} = 800\text{ V},$                                   |       | 10      |      | ns   |             |
| Fall Time, $V_{DS}$                          | $t_f$             | $I_D = 10\text{ A}, \text{Resistive Load}$                                     |       | 10      |      | ns   | Fig. 11, 13 |
| Turn Off Delay Time                          | $t_{d(off)}$      | Refer to Section V for additional driving information.                         |       | 22      |      | ns   |             |
| Rise Time, $V_{DS}$                          | $t_r$             |  |       | 10      |      | ns   | Fig. 12, 14 |
| Turn On Delay Time                           | $t_{d(on)}$       |  |       | 10      |      | ns   |             |
| Fall Time, $V_{DS}$                          | $t_f$             | $T_J = 175\text{ °C}, V_{DS} = 800\text{ V},$                                  |       | 10      |      | ns   | Fig. 11     |
| Turn Off Delay Time                          | $t_{d(off)}$      | $I_D = 10\text{ A}, \text{Resistive Load}$                                     |       | 35      |      | ns   |             |
| Rise Time, $V_{DS}$                          | $t_r$             |  |       | 10      |      | ns   | Fig. 12     |
| Turn-On Energy Per Pulse                     | $E_{on}$          | $T_J = 25\text{ °C}, V_{DS} = 800\text{ V},$                                   |       | 140     |      | μJ   | Fig. 11, 13 |
| Turn-Off Energy Per Pulse                    | $E_{off}$         | $I_D = 10\text{ A}, \text{Inductive Load}$                                     |       | 10      |      | μJ   | Fig. 12, 14 |
| Total Switching Energy                       | $E_{tot}$         | Refer to Section V.  |       | 150     |      | μJ   |             |
| Turn-On Energy Per Pulse                     | $E_{on}$          |  |       | 140     |      | μJ   | Fig. 11     |
| Turn-Off Energy Per Pulse                    | $E_{off}$         | $T_J = 175\text{ °C}, V_{DS} = 800\text{ V},$                                  |       | 100     |      | μJ   | Fig. 12     |
| Total Switching Energy                       | $E_{tot}$         | $I_D = 10\text{ A}, \text{Inductive Load}$                                     |       | 150     |      | μJ   |             |

<sup>1</sup> – All times are relative to the Drain-Source Voltage  $V_{DS}$

Section IV: Figures

A: Static Characteristics

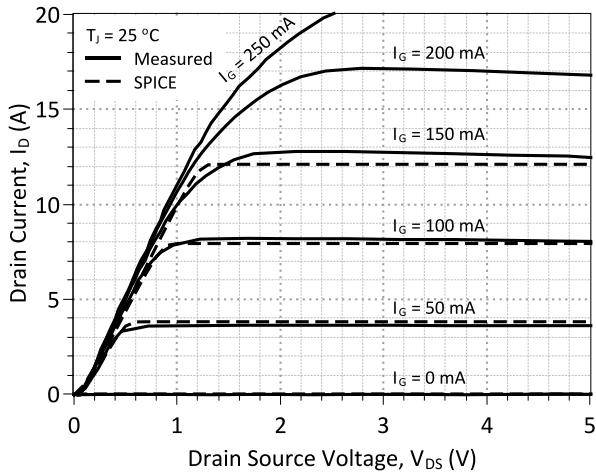


Figure 1: Typical Output Characteristics at 25 °C

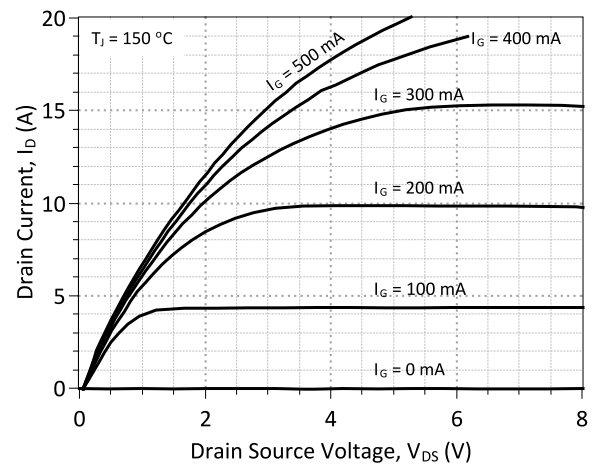


Figure 2: Typical Output Characteristics at 150 °C

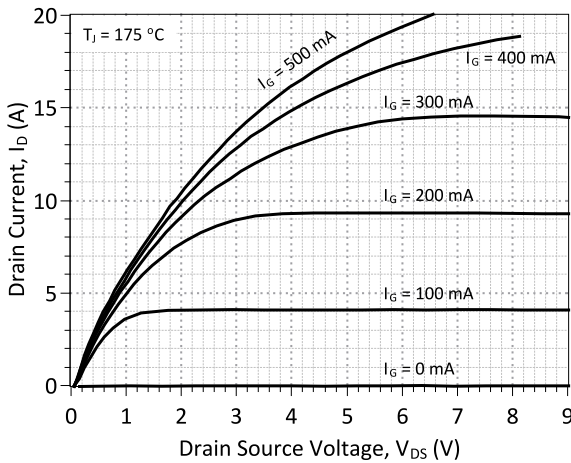


Figure 3: Typical Output Characteristics at 175 °C

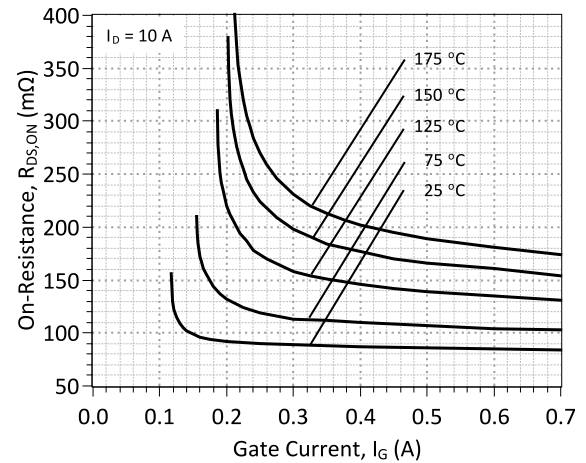


Figure 4: On-Resistance vs. Gate Current

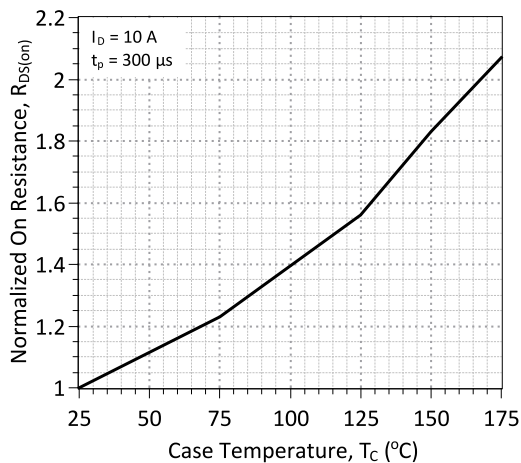


Figure 5: Normalized On-Resistance vs. Temperature

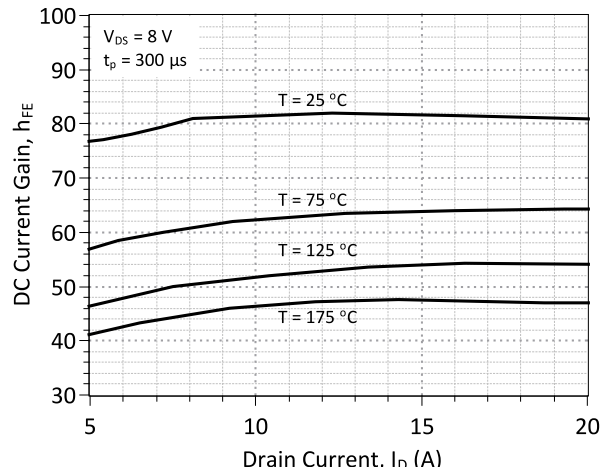


Figure 6: DC Current Gain vs. Drain Current

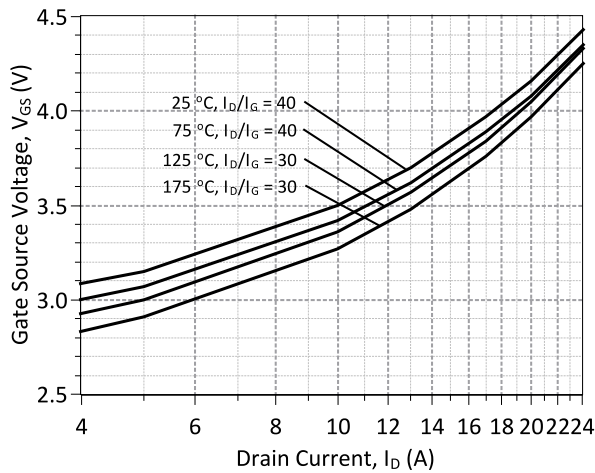


Figure 7: Typical Gate – Source Saturation Voltage

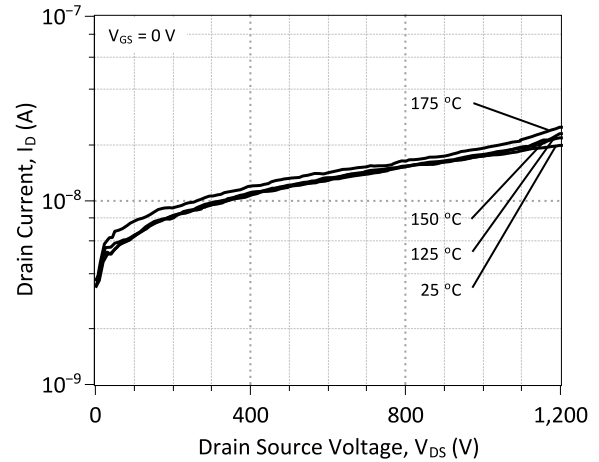


Figure 8: Typical Blocking Characteristics

**B: Dynamic Characteristics**

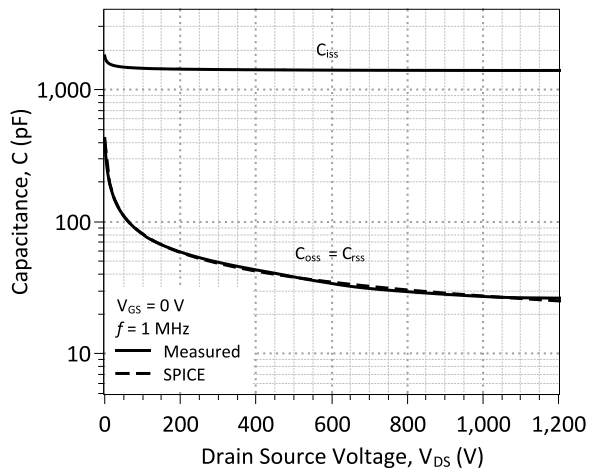


Figure 9: Input, Output, and Reverse Transfer Capacitance

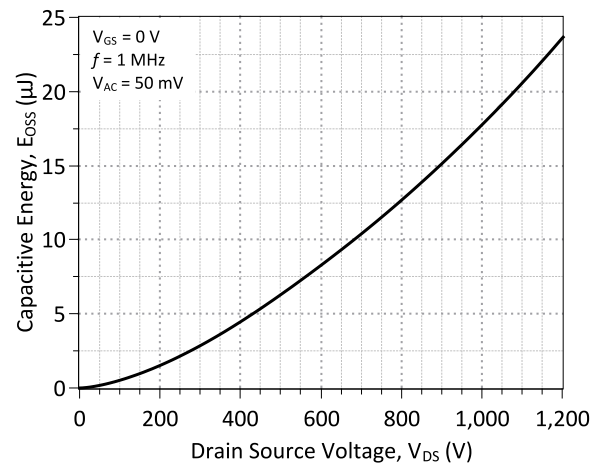


Figure 10: Energy Stored in Output Capacitance

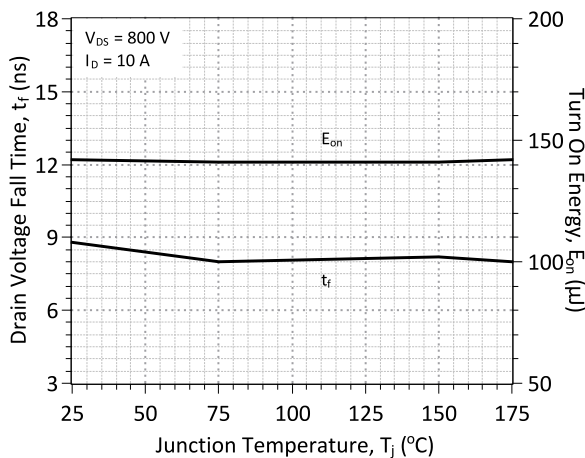


Figure 11: Typical Switching Times and Turn On Energy Losses vs. Temperature

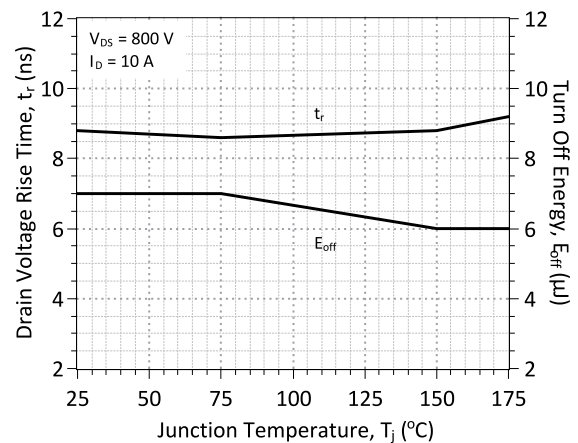


Figure 12: Typical Switching Times and Turn Off Energy Losses vs. Temperature

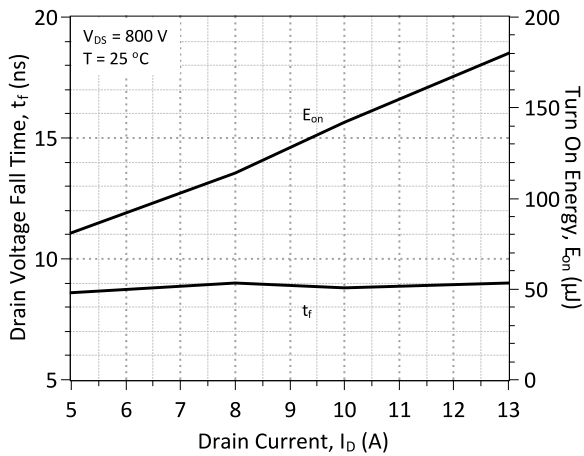


Figure 13: Typical Switching Times and Turn On Energy Losses vs. Drain Current

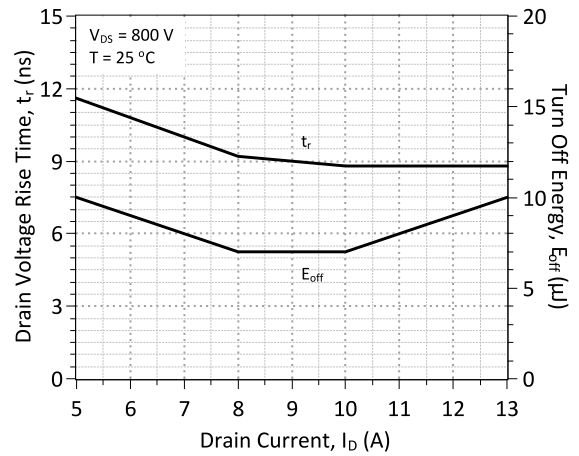


Figure 14: Typical Switching Times and Turn Off Energy Losses vs. Drain Current

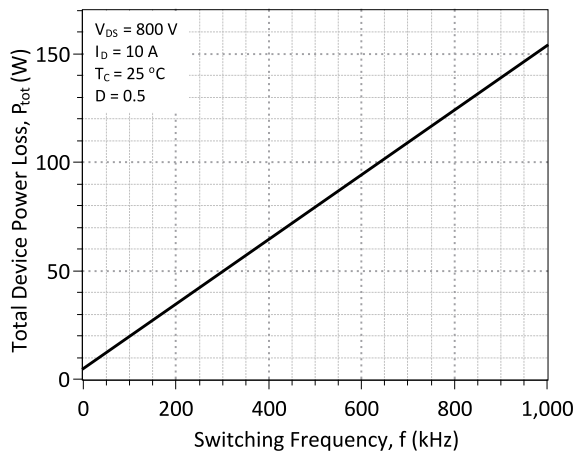


Figure 15: Typical Hard Switched Device Power Loss vs. Switching Frequency<sup>2</sup>

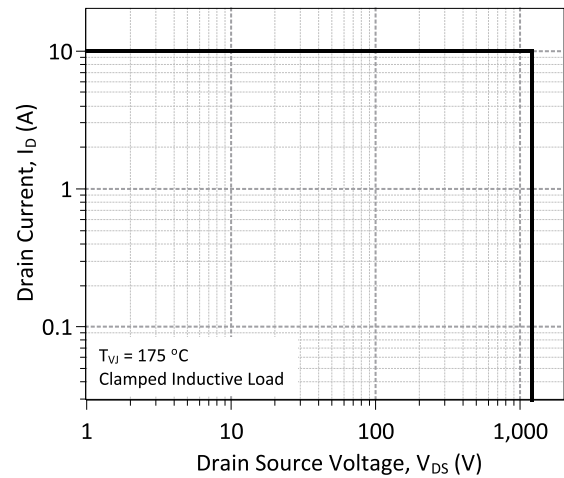


Figure 16: Turn-Off Safe Operating Area

<sup>2</sup> – Representative values based on device conduction and switching loss. Actual losses will depend on gate drive conditions, device load, and circuit topology.

## Section V: Driving the GA10JT12-CAL

| Drive Topology               | Gate Drive Power Consumption | Switching Frequency | Application Emphasis     | Availability |
|------------------------------|------------------------------|---------------------|--------------------------|--------------|
| TTL Logic                    | High                         | Low                 | Wide Temperature Range   | Coming Soon  |
| Constant Current             | Medium                       | Medium              | Wide Temperature Range   | Coming Soon  |
| High Speed – Boost Capacitor | Medium                       | High                | Fast Switching           | Production   |
| High Speed – Boost Inductor  | Low                          | High                | Ultra Fast Switching     | Coming Soon  |
| Proportional                 | Lowest                       | High                | Wide Drain Current Range | Coming Soon  |
| Pulsed Power                 | Medium                       | N/A                 | Pulse Power              | Coming Soon  |

### A: Static TTL Logic Driving

The GA10JT12-CAL may be driven using direct (5 V) TTL logic after current amplification. The (amplified) current level of the supply must meet or exceed the steady state gate current ( $I_{G,steady}$ ) required to operate the GA10JT12-CAL. The power level of the supply can be estimated from the target duty cycle of the particular application.  $I_{G,steady}$  is dependent on the anticipated drain current  $I_D$  through the SJT and the DC current gain  $h_{FE}$ , it may be calculated from the following equation. An accurate value of the  $h_{FE}$  may be read from Figure 6.

$$I_{G,steady} \approx \frac{I_D}{h_{FE}(T, I_D)} * 1.5$$

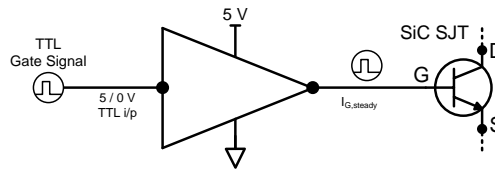


Figure 17: TTL Gate Drive Schematic

### B: High Speed Driving

The SJT is a current controlled transistor which requires a positive gate current for turn-on as well as to remain in on-state. An ideal gate current waveform for ultra-fast switching of the SJT, while maintaining low gate drive losses, is shown in Figure 18 which features a positive current peak during turn-on, a negative current peak during turn-off, and continuous gate current to remain on.

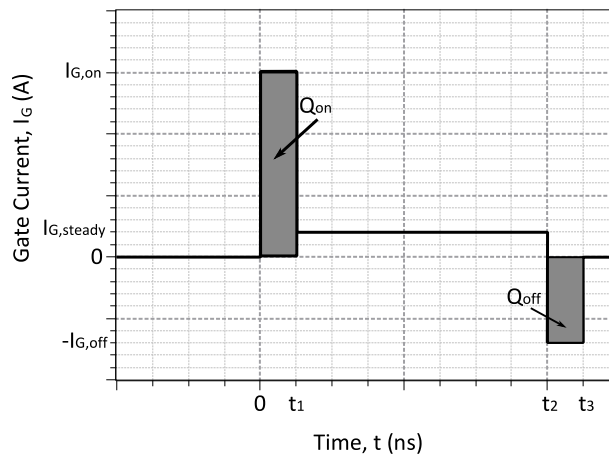


Figure 18: An idealized gate current waveform for fast switching of an SJT.

An SJT is rapidly switched from its blocking state to on-state, when the necessary gate charge,  $Q_G$ , for turn-on is supplied by a burst of high gate current,  $I_{G,on}$ , until the gate-source capacitance,  $C_{GS}$ , and gate-drain capacitance,  $C_{GD}$ , are fully charged.

$$Q_{on} = I_{G,on} * t_1$$

$$Q_{on} \geq Q_{gs} + Q_{gd}$$

Ideally,  $I_{G,pon}$  should terminate when the drain voltage falls to its on-state value in order to avoid unnecessary drive losses during the steady on-state. In practice, the rise time of the  $I_{G,on}$  pulse is affected by the parasitic inductances,  $L_{par}$  in the device package and drive circuit. A voltage developed across the parasitic inductance in the source path,  $L_s$ , can de-bias the gate-source junction, when high drain currents begin to flow through the device. The voltage applied to the gate pin should be maintained high enough, above the  $V_{GS,sat}$  (see **Error! Reference source not found.**) level to counter these effects.

A high negative peak current,  $-I_{G,off}$  is recommended at the start of the turn-off transition, in order to rapidly sweep out the injected carriers from the gate, and achieve rapid turn-off. While satisfactory turn off can be achieved with  $V_{GS} = 0$  V, a negative gate voltage  $V_{GS}$  may be used in order to speed up the turn-off transition.

Two high-speed drive topologies for the SiC SJTs are presented below.

**B:1: High Speed, Low Loss Drive with Boost Capacitor, GA03IDDJT30-FR4**

The GA10JT12- CAL may be driven using a High Speed, Low Loss Drive with Boost Capacitor topology in which multiple voltage levels, a gate resistor, and a gate capacitor are used to provide fast switching current peaks at turn-on and turn-off and a continuous gate current while in on-state. A 3 kV isolated evaluation gate drive board (GA03IDDJT30-FR4) utilizing this topology is commercially available for high and low-side driving, its datasheet provides additional details about this drive topology.

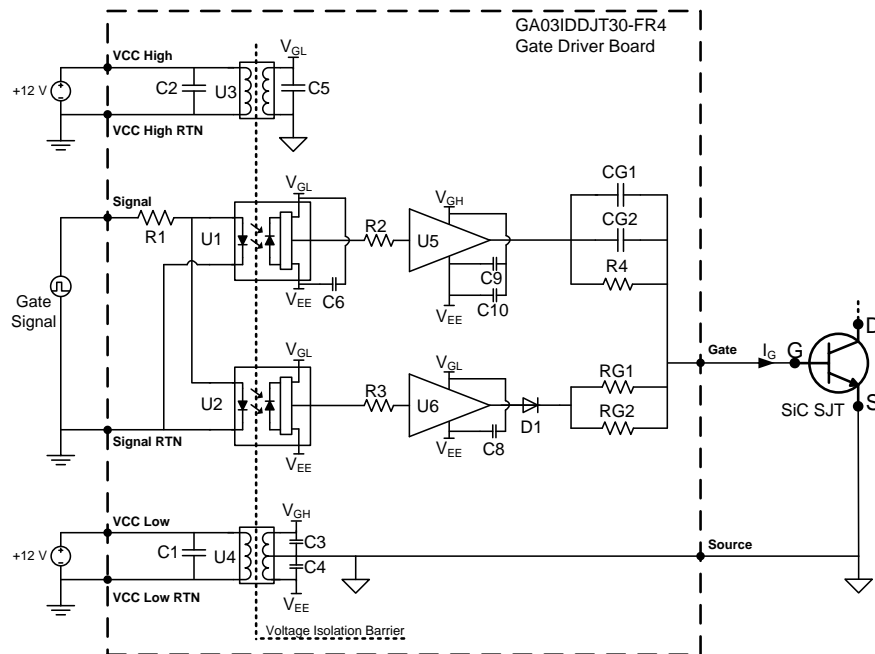


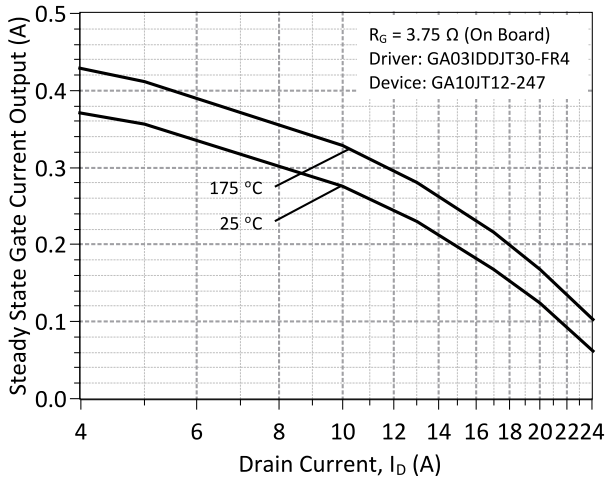
Figure 19: Topology of the GA03IDDJT30-FR4 Two Voltage Source gate driver.

The GA03IDDJT30-FR4 evaluation board comes equipped with two on board gate drive resistors (RG1, RG2) pre-installed for an effective gate resistance<sup>3</sup> of  $R_G = 3.75 \Omega$ . It may be necessary for the user to reduce RG1 and RG2 under high drain current conditions for safe operation of the GA10JT12- CAL. The steady state current supplied to the gate pin of the GA10JT12- CAL with on-board  $R_G = 3.75 \Omega$ , is shown in Figure 20. The maximum allowable safe value of  $R_G$  for the user's required drain current can be read from Figure 21.

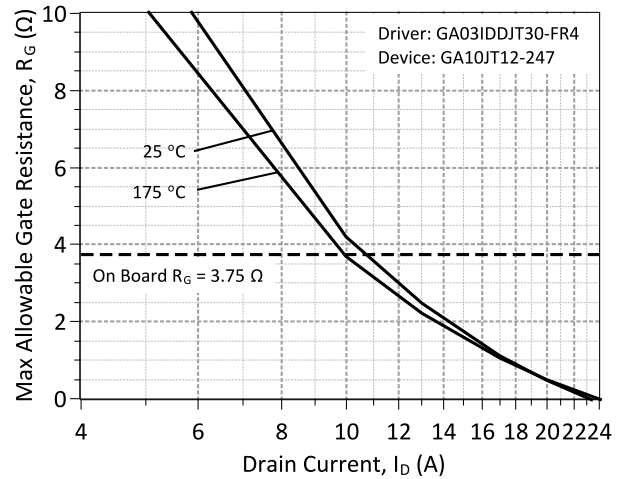
**For the GA10JT12-CAL,  $R_G$  must be reduced for  $I_D \geq \sim 10$  A for safe operation with the GA03IDDJT30-FR4.**

For operation at  $I_D \geq \sim 10$  A,  $R_G$  may be calculated from the following equation, which contains the DC current gain  $h_{FE}$  (Figure 6) and the gate-source saturation voltage  $V_{GS,sat}$  (Figure 7).

$$R_{G,max} = \frac{(4.7V - V_{GS,sat}) * h_{FE}(T, I_D)}{I_D * 1.5} - 0.6\Omega$$



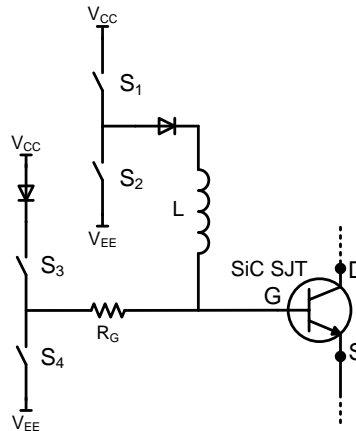
**Figure 20: Typical steady state gate current supplied by the GA03IDDJT30-FR4 board for the GA10JT12-CAL with the on board resistance of 3.75 Ω**



**Figure 21: Maximum gate resistance for safe operation of the GA10JT12-CAL at different drain currents using the GA03IDDJT30-FR4 board.**

**B:2: High Speed, Low Loss Drive with Boost Inductor**

A High Speed, Low-Loss Driver with Boost Inductor is also capable of driving the GA10JT12- CAL at high-speed. It utilizes a gate drive inductor instead of a capacitor to provide the high-current gate current pulses  $I_{G,on}$  and  $I_{G,off}$ . During operation, inductor L is charged to a specified  $I_{G,on}$  current value then made to discharge  $I_L$  into the SJT gate pin using logic control of  $S_1$ ,  $S_2$ ,  $S_3$ , and  $S_4$ , as shown in Figure 22. After turn on, while the device remains on the necessary steady state gate current  $I_{G,steady}$  is supplied from source VCC through  $R_G$ . Please refer to the article "A current-source concept for fast and efficient driving of silicon carbide transistors" by Dr. Jacek Rąbkowski for additional information on this driving topology.<sup>4</sup>



**Figure 22: Simplified Inductive Pulsed Drive Topology**

<sup>3</sup> –  $R_G = (1/RG1 + 1/RG2)^{-1}$ . Driver is pre-installed with  $RG1 = RG2 = 7.5 \Omega$

<sup>4</sup> – Archives of Electrical Engineering. Volume 62, Issue 2, Pages 333–343, ISSN (Print) 0004-0746, DOI: 10.2478/ae-2013-0026, June 2013



**C: Proportional Gate Current Driving**

For applications in which the GA10JT12- CAL will operate over a wide range of drain current conditions, it may be beneficial to drive the device using a proportional gate drive topology to optimize gate drive power consumption. A proportional gate driver relies on instantaneous drain current  $I_D$  feedback to vary the steady state gate current  $I_{G,steady}$  supplied to the GA10JT12- CAL.

**C:1: Voltage Controlled Proportional Driver**

The voltage controlled proportional driver relies on a gate drive IC to detect the GA10JT12- CAL drain-source voltage  $V_{DS}$  during on-state to sense  $I_D$ . The gate drive IC will then increase or decrease  $I_{G,steady}$  in response to  $I_D$ . This allows  $I_{G,steady}$ , and thus the gate drive power consumption, to be reduced while  $I_D$  is relatively low or for  $I_{G,steady}$  to increase when is  $I_D$  higher. A high voltage diode connected between the drain and sense protects the IC from high-voltage when the driver and GA10JT12- CAL are in off-state. A simplified version of this topology is shown in Figure 23, additional information will be available in the future at <http://www.genesicsemi.com/commercial-sic/sic-junction-transistors/>

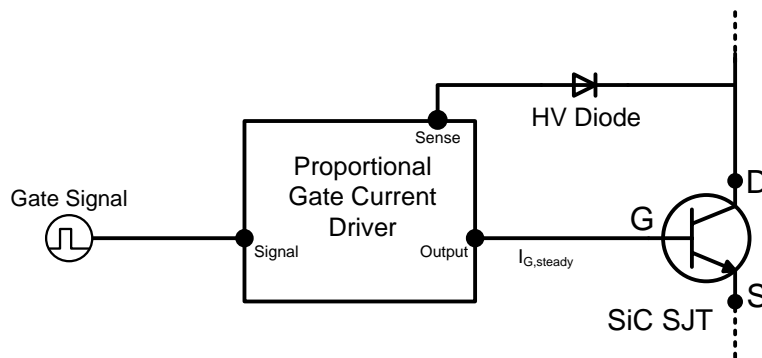


Figure 23: Simplified Voltage Controlled Proportional Driver

**C:2: Current Controlled Proportional Driver**

The current controlled proportional driver relies on a low-loss transformer in the drain or source path to provide feedback  $I_D$  of the GA10JT12- CAL during on-state to supply  $I_{G,steady}$  into the device gate.  $I_{G,steady}$  will then increase or decrease in response to  $I_D$  at a fixed forced current gain which is set by the turns ratio of the transformer,  $h_{force} = I_D / I_G = N_2 / N_1$ . GA10JT12- CAL is initially tuned-on using a gate current pulse supplied into an RC drive circuit to allow  $I_D$  current to begin flowing. This topology allows  $I_{G,steady}$ , and thus the gate drive power consumption, to be reduced while  $I_D$  is relatively low or for  $I_{G,steady}$  to increase when is  $I_D$  higher. A simplified version of this topology is shown in Figure 24, additional information will be available in the future at <http://www.genesicsemi.com/commercial-sic/sic-junction-transistors/>.

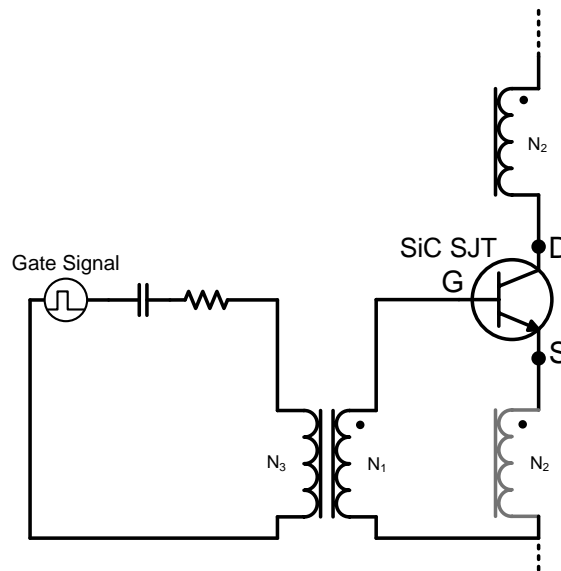
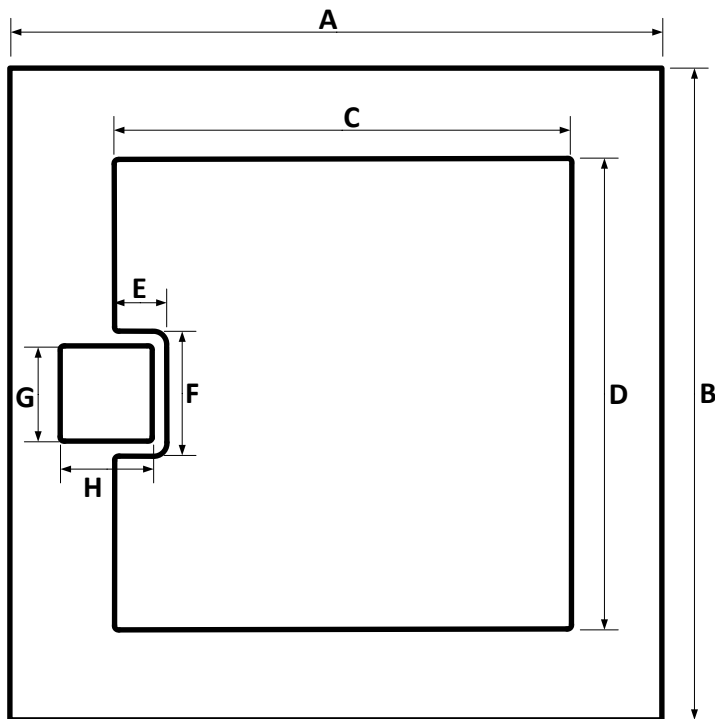


Figure 24: Simplified Current Controlled Proportional Driver

## Section VI: Mechanical Parameters

|                                 |  |                 |           |                  |
|---------------------------------|--|-----------------|-----------|------------------|
| Die Dimensions                  | 2.10 x 2.10  | mm <sup>2</sup> | 83 x 83   | mil <sup>2</sup> |
| Die Area total / active         | 4.41/3.31  | mm <sup>2</sup> | 6836/5134 | mil <sup>2</sup> |
| Die Thickness                   | 360  | μm              | 14        | mil              |
| Wafer Size                      | 100  | mm              | 3937      | mil              |
| Flat Position                   | 0  | deg             | 0         | deg              |
| Die Frontside Passivation       | Polyimide  |                 |           |                  |
| Gate/Source Pad Metallization   | 4000 nm Al   |                 |           |                  |
| Bottom Drain Pad Metallization  | 400 nm Ni + 200 nm Au  |                 |           |                  |
| Die Attach                      | Electrically conductive glue or solder   |                 |           |                  |
| Wire Bond                       | Al ≤ 10 mil (Source)<br>Al ≤ 3 mil (Gate)  |                 |           |                  |
| Reject ink dot size             | Φ ≥ 0.3 mm   |                 |           |                  |
| Recommended storage environment | Store in original container, in dry nitrogen,<br>< 6 months at an ambient temperature of 23 °C |                 |           |                  |

## Section VII: Chip Dimensions



|                     |   | mm   | mil |
|---------------------|---|------|-----|
| DIE                 | A | 2.10 | 83  |
|                     | B | 2.10 | 83  |
| SOURCE WIREBONDABLE | C | 1.47 | 58  |
|                     | D | 1.52 | 60  |
|                     | E | 0.17 | 7   |
|                     | F | 0.40 | 16  |
| GATE WIREBONDABLE   | G | 0.30 | 12  |
|                     | H | 0.30 | 12  |

**Revision History**

| Date       | Revision | Comments                           | Supersedes |
|------------|----------|------------------------------------|------------|
| 2016/02/26 | 2        | Updated Electrical Characteristics |            |
| 2015/02/05 | 1        | Updated Electrical Characteristics |            |
| 2014/07/14 | 0        | Initial release                    |            |

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**Section VIII: SPICE Model Parameters**

This is a secure document. Please copy this code from the SPICE model PDF file on our website ([http://www.genesicsemi.com/images/hit\\_sic/baredie/sjt/GA10JT12-CAL\\_SPICE.pdf](http://www.genesicsemi.com/images/hit_sic/baredie/sjt/GA10JT12-CAL_SPICE.pdf)) into LTSPICE (version 4) software for simulation of the GA10JT12-CAL.

```
*      MODEL OF GeneSiC Semiconductor Inc.
*
*      $Revision:   2.2           $
*      $Date:      26-FEB-2016   $
*
*      GeneSiC Semiconductor Inc.
*      43670 Trade Center Place Ste. 155
*      Dulles, VA 20166
*
*      COPYRIGHT (C) 2015 GeneSiC Semiconductor Inc.
*      ALL RIGHTS RESERVED
*
*      These models are provided "AS IS, WHERE IS, AND WITH NO WARRANTY
*      OF ANY KIND EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED
*      TO ANY IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A
*      PARTICULAR PURPOSE."
*      Models accurate up to 2 times rated drain current.
*
.model GA10JT12 NPN
+ IS      9.833E-48
+ ISE     1.073E-26
+ EG      3.23
+ BF      87
+ BR      0.55
+ IKF     5000
+ NF      1
+ NE      2
+ RB      4.67
+ IRB     0.001
+ RBM     0.16
+ RE      0.005
+ RC      0.08
+ CJC     229.9E-12
+ VJC     3.22
+ MJC     0.492
+ CJE     1244E-9
+ VJE     2.86
+ MJE     0.465
+ XTI     3
+ XTB     -1.35
+ TRC1    7E-3
+ VCEO    1200
+ ICRATING 10
+ MFG     GeneSiC_Semiconductor
*
*      End of GA10JT12 SPICE Model
```