EMC2101

SMBus Fan Control with 1°C Accurate Temperature Monitoring

Features

- Self-Programming with Available SMBus Compatible EEPROM
- Selectable PWM or DAC Fan Driver Output
- Temperature Monitors
  - External channel ±1°C accuracy
  - Internal channel ±2°C accuracy
  - Automatic Beta Compensation
  - Resistance Error Correction
- 3.3 Volt Operation (5 Volt Tolerant Input Buffers)
- SMBus 2.0 Compliant Interface, Supports TIMEOUT
- 8-Pin MSOP Lead-free RoHS Compliant Packages

Applications

- Graphics Processors
- Embedded Application Fan Drive
- PWM Controller + Temp Sensor

Description

The EMC2101 is an SMBus 2.0 compliant, integrated fan control solution complete with two temperature monitors, one external and one internal. Each temperature channel has programmable high limits that can assert an interrupt.

The fan drive is selectable as a Pulse Width Modulator (PWM) or Linear (DAC) output. The fan control output, whether the PWM or DAC drive circuit, uses an eight position look-up table to allow the user to program the fan speed profile based on temperature. The DAC output ranges from 0V to V_{DD} with up to 6 bit resolution while the PWM output has a range of 0% to 100% with up to 64 steps.

The EMC2101 has an option to automatically upload the contents of an attached SMBus compatible EEPROM for auto-programming upon power up.

Advanced thermal sensing enables reduced validation and characterization time as well as accurately operating with smaller-geometry processors. Resistance Error Correction (REC) automatically corrects the offset errors of board trace and device resistance, up to 100Ω. Automatic Beta Compensation allows the user the flexibility to design applications that include processor substrate transistors.

Package Types

EMC2101
8-pin MSOP

Pin			Pin
V_{DD}	1	8	SMCLK
DP	2	7	SMDATA
DN	3	6	ALERT/TACH
FAN	4	5	GND
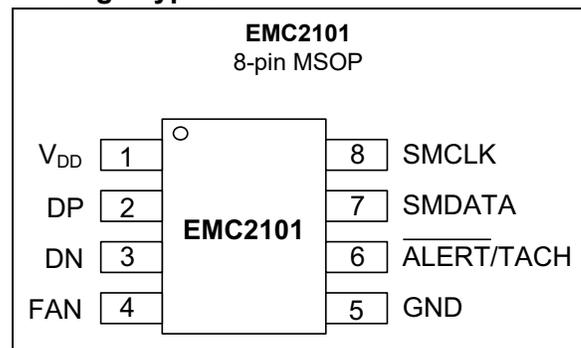
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Block Diagram
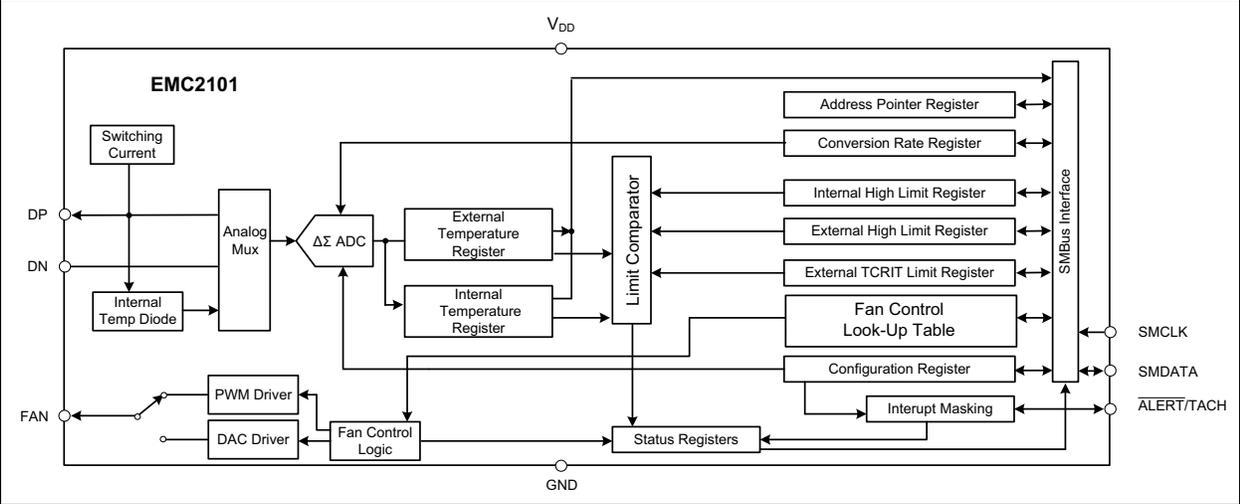
1.0 ELECTRICAL CHARACTERISTICS

1.1 Electrical Specifications

Absolute Maximum Ratings[†]

Supply Voltage (V_{DD}) .... -0.3V to +5.0V

Voltage on 5V tolerant pins (V_{5VT_pin}) .... -0.3 to 5.5V

Voltage on 5V tolerant pins ($|V_{5VT\_pin} - V_{DD}|$) (**Note**) .... -0.3 to 3.6V

Voltage on any other pin to Ground .... -0.3 to V_{DD} +0.3V

Operating Temperature Range .... -40 to +125°C

Storage Temperature Range .... -55 to +150°C

Lead Temperature Range .... Refer to JEDEC Spec. J-STD-020

Package Thermal Characteristics for 8-pin MSOP

Thermal Resistance (θ_{j-a}) .... 140.8°C/W

ESD Rating, All pins HBM 2000V

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure above maximum rating conditions for extended periods may affect device reliability.

Note: For the 5V tolerant pins that have a pull-up resistor, the pull-up voltage must not exceed 3.6V when EMC2101 is unpowered.

TABLE 1-1: ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise specified V_{DD} = 3.0V to 3.6V, T_A = 0°C to +85°C, all typical values at T_A = +27°C

Characteristic	Sym.	Min.	Typ.	Max.	Units	Conditions
DC Power						
Supply Voltage	V_{DD}	3.0	3.3	3.6	V	
Supply Current	I_{DD}	—	0.6	1	mA	16 conversion/second, PWM or DAC driver operational
		—	200	—	µA	1 conversion/16 seconds, PWM driver operational
		—	300	—	µA	1 conversion/16 seconds, DAC driver, no load
		—	300	400	µA	Temp monitoring disabled, DAC driver enabled, no load
Standby Current	$I_{STANDBY}$	—	—	270	µA	PWM disabled, monitoring disabled
Internal Temperature Monitor						
Temperature Accuracy	—	—	±1	±2	°C	
Temperature Resolution	—	—	±1	—	°C	8-bit resolution
Conversion Time Internal Channel	t_{CONV}	—	3	—	ms	

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TABLE 1-1: ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: Unless otherwise specified V_{DD} = 3.0V to 3.6V, T_A = 0°C to +85°C, all typical values at T_A = +27°C

Characteristic	Sym.	Min.	Typ.	Max.	Units	Conditions
External Temperature Monitor						
Temperature Accuracy	—	—	±0.5	±1	°C	+60°C < T_{DIODE} < +100°C 10°C < T_A < +70°C
		—	±1	±3	°C	0°C < T_{DIODE} < +125°C
Temperature Resolution	—	—	0.125	—	°C	11-bit resolution
Conversion Time External Channel	t_{CONV}	—	21	—	ms	
Diode Decoupling Capacitor	C_{FILTER}	—	—	2.2	nF	Connected across External Diode (2N3904)
Diode Decoupling Capacitor	C_{FILTER}	—	—	470	pF	Connected across Substrate Transistor (CPU diode)
Resistance Error Correction	R_{SERIES}	—	100	—	Ω	Series resistance in DP and DN lines
TACH Measurement						
TACH Accuracy	—	—	—	10	%	TACH valid
Fan Counter Clock Frequency	—	—	90	—	kHz	
Pulse Width Modulator Fan Driver						
PWM Resolution	—	—	64	—	Steps	
PWM Frequency	f_{PWM}	22	—	5k	Hz	For 64 steps, higher frequencies are possible with reduced resolution (see **Appendix B: "Advanced PWM Options"**).
PWM Duty cycle	D_{PWM}	0	—	100	%	
DAC Fan Driver						
Output Voltage Drive	V_{DAC}	0.2		V_{DD} - 0.2	V	Current Load = ±1 mA
Total Unadjusted Error	TUE	—	5	—	%	Measured at 3/4 full scale
DAC Resolution	—	—	6	—	bits	
Settling Time to within 1%	t_{SETTLE}	—	40	—	µs	Capacitive Load = 100 pF
Digital I/O pins (PWM, SMDATA, SMCLK, ALERT/TACH)						
Output High Voltage	V_{OH}	V_{DD} - 0.3	—	—	V	8 mA Current Source
Output Low Voltage	V_{OL}	—	—	0.3	V	8 mA Current Sink
Output Leakage Current	I_{LEAK}	—	—	10	µA	Device powered or unpowered T_A < +85°C Pull-up voltage ≤ 3.6V

1.2 SMBus Electrical Characteristics

TABLE 1-2: SMBUS ELECTRICAL SPECIFICATIONS

Characteristic	Sym.	Min.	Typ.	Max.	Units	Conditions
Electrical Characteristics: Unless otherwise specified V_{DD} = 3.0V to 3.6V, T_A = 0°C to +85°C, all typical values at T_A = +27°C						
SMBus Interface						
Input High Voltage	V_{IH}	2.1	—	—	V	
Input Low Voltage	V_{IL}	—	—	0.8	V	
Input High/Low Current	I_{IH}/I_{IL}	-1	—	1	µA	
Hysteresis	—	—	500	—	mV	
Input Capacitance	C_{IN}	—	5	—	pF	
Output Low Sink Current	—	—	8	—	mA	V_{OL} = 0.4V
SMBus Timing						
Clock Frequency	f_{SMB}	10	—	400	kHz	
Spike Suppression	t_{SP}	—	—	50	ns	
Bus free time Start to Stop	t_{BUF}	1.3	—	—	µs	
Hold Time: Start	$t_{HD:STA}$	0.6	—	—	µs	
Setup Time: Start	$t_{SU:STA}$	0.6	—	—	µs	
Setup Time: Stop	$t_{SU:STO}$	0.6	—	—	µs	
Data Hold Time	$t_{HD:DAT}$	0.3	—	—	µs	
Data Setup Time	$t_{SU:DAT}$	100	—	—	ns	
Clock Low Period	t_{LOW}	1.3	—	—	µs	
Clock High Period	t_{HIGH}	0.6	—	—	µs	
Clock/Data Fall Time	t_{FALL}	—	—	300	ns	Min = 20+0.1C_{LOAD} ns
Clock/Data Rise Time	t_{RISE}	—	—	300	ns	Min = 20+0.1C_{LOAD} ns (**Note 1**)
Capacitive Load	C_{LOAD}	—	—	400	pF	Per bus line

Note 1: 300 ns maximum Rise Time is required for 400 kHz bus operation. For lower clock frequencies, the maximum Rise Time is (0.1/fSMB) + 50 ns.

1.3 EEPROM Loader Electrical Specifications (EMC2101-R only)

TABLE 1-3: EEPROM LOADER ELECTRICAL SPECIFICATIONS

Characteristic	Sym.	Min.	Typ.	Max.	Units	Conditions
Electrical Characteristics: Unless otherwise specified V_{DD} = 3.0V to 3.6V, T_A = 0°C to +85°C, all typical values at T_A = +27°C						
Interface						
Input High Voltage	V_{IH}	2.1	—	—	V	
Input Low Voltage	V_{IL}	—	—	0.8	V	
Input High/Low Current	I_{IH}/I_{IL}	-1	—	1	µA	
Hysteresis	—	—	500	—	mV	
Input Capacitance	C_{IN}	—	5	—	pF	
Output Low Sink Current	—	—	8	—	mA	V_{OL} = 0.4V

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TABLE 1-3: EEPROM LOADER ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: Unless otherwise specified V_{DD} = 3.0V to 3.6V, T_A = 0°C to +85°C, all typical values at T_A = +27°C

Characteristic	Sym.	Min.	Typ.	Max.	Units	Conditions
Timing						
Loading Delay	t_{DLY}	—	10	—	ms	Delay after power-up until EEPROM loading begins. (See **Section 2.9 "Programming from EEPROM"**)
Loading Time	t_{LOAD}	—	50	—	ms	
Clock Frequency	f_{SMB}	—	50	—	kHz	
Spike Suppression	t_{SP}	—	—	50	ns	
Bus free time Start to Stop	t_{BUF}	1.3	—	—	µs	
Hold Time: Start	$t_{HD:STA}$	0.6	—	—	µs	
Setup Time: Start	$t_{SU:STA}$	0.6	—	—	µs	
Setup Time: Stop	$t_{SU:STO}$	0.6	—	—	µs	
Data Hold Time	$t_{HD:DAT}$	0.3	—	—	µs	
Data Setup Time	$t_{SU:DAT}$	100	—	—	ns	
Clock Low Period	t_{LOW}	1.3	—	—	µs	
Clock High Period	t_{HIGH}	0.6	—	—	µs	
Clock/Data Fall Time	t_{FALL}	—	—	300	ns	Min = 20+0.1 C_{LOAD} ns
Clock/Data Rise Time	t_{RISE}	—	—	300	ns	Min = 20+0.1 C_{LOAD} ns
Capacitive Load	C_{LOAD}	—	—	400	pF	Per bus line

2.0   SYSTEM MANAGEMENT BUS INTERFACE PROTOCOL

2.1   System Management Bus Interface Protocol

The EMC2101 communicates with a host controller through the SMBus. The SMBus is a two-wire serial communication protocol between a computer host and its peripheral devices. A detailed timing diagram is shown in Figure 2-1. Stretching of the SMCLK signal is supported, however the EMC2101 does not stretch the clock signal
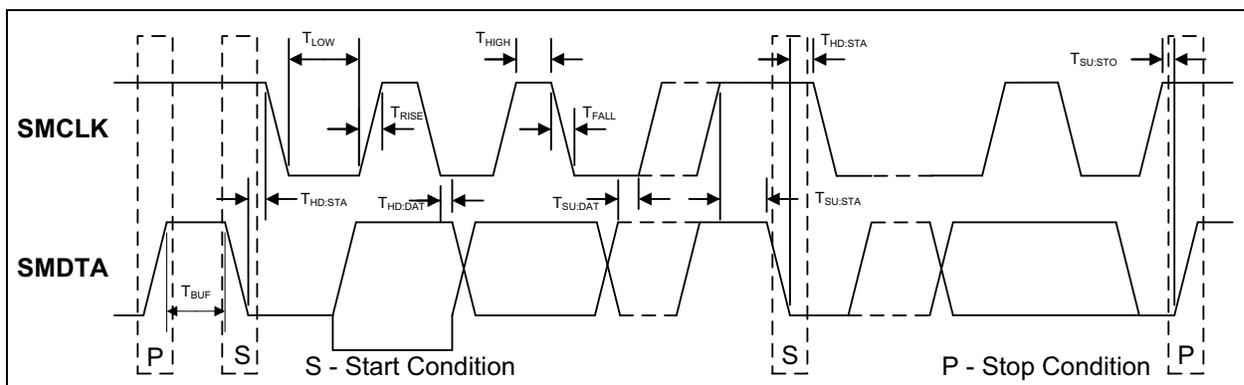
The EMC2101 powers up as an SMBus client (after loading from EEPROM as applicable).

FIGURE 2-1:   *SMBus Timing Diagram.*

The EMC2101 is SMBus 2.0 compatible and supports Send Byte, Read Byte, Write Byte, Receive Byte and the Alert Response Address as valid protocols, as shown below.

All of the protocols below use the convention in Table 2-1.

TABLE 2-1:   PROTOCOL FORMAT

Data Sent to Device	Data Sent to the Host
# of bits sent	# of bits sent

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2.2 Write Byte

The Write Byte is used to write one byte of data to the registers as shown in Table 2-2.

TABLE 2-2: WRITE BYTE PROTOCOL

START	Client Address	WR	ACK	Register Address	ACK	Register Data	ACK	STOP
1	7	1	1	8	1	8	1	1

2.3 Read Byte

The Read Byte protocol is used to read one byte of data from the registers as shown in Table 2-3.

TABLE 2-3: READ BYTE PROTOCOL

START	Client Address	WR	ACK	Register Address	ACK	
1	7	1	1	8	1	
START	Client Address	RD	ACK	Register Data	NACK	STOP
1	7	1	1	8	1	1

2.4 Send Byte

The Send Byte protocol is used to set the internal address register pointer to the correct address location. No data is transferred during the Send Byte protocol, as shown in Table 2-4.

TABLE 2-4: SEND BYTE PROTOCOL

START	Client Address	WR	ACK	Register Address	ACK	STOP
1	7	1	1	8	1	1

2.5 Receive Byte

The Receive Byte protocol is used to read data from a register when the internal register address pointer is known to be at the right location (e.g. set via Send Byte). This is used for consecutive reads of the same register as shown in Table 2-5.

TABLE 2-5: RECEIVE BYTE PROTOCOL

START	Client Address	RD	ACK	Register Data	NACK	STOP
1	7	1	1	8	1	1

2.6 Alert Response Address

The ALERT/TACH output can be used as a processor interrupt or as an SMBus Alert when configured to operate as an interrupt.

When it detects that the ALERT/TACH pin is asserted, the host sends the Alert Response Address (ARA) to the general address of 000_1100b. All devices with active interrupts will respond with their client address as shown in Table 2-6.

TABLE 2-6: ALERT RESPONSE ADDRESS PROTOCOL

START	ALERT Response Address	RD	ACK	Device Address	NACK	STOP
1	7	1	1	8	1	1

The EMC2101 responds to the ARA in the following way when the ALERT/TACH pin is configured as an Interrupt:

- Send client Address and verify that full client address was sent (i.e. the SMBus communication from the device was not prematurely stopped due to a bus contention event).
- Set the MASK bit to clear the ALERT/TACH pin only if there are no bits set in the Status Register. If there are error condition bits set in the Status Register, it must be read before the MASK bit is be set.

When the ALERT/TACH pin is configured to operate in Comparator Mode or as a TACH input (see **Section 4.4.1 "ALERT/TACH as a Temperature Comparator"**), it does not respond to the ARA command. Additionally, the EMC2101 does not respond to the ARA command if the ALERT/TACH pin is not asserted.

2.7 SMBus Address

The EMC2101 is addressed on the SMBus as `100_1100b`.

Attempting to communicate with the EMC2101 SMBus interface with an invalid client address or invalid protocol results in no response from the device and does not affect its register contents.

2.8 SMBus Timeout

The EMC2101 includes an SMBus time-out feature. Following a 25 ms period of inactivity on the SMBus, the device times-out and resets the SMBus interface.

2.9 Programming from EEPROM

The EMC2101-R acts as a simple SMBus Host to read data from a connected EEPROM using the following procedure:

1. After power-up the EMC2101-R waits for 10 ms with the SMDATA and SMCLK pins tri-stated.
2. Once the wait period has elapsed, the EMC2101-R sends a START signal followed by the 7 bit client address 101_0000b followed by a '1b' and waits for an ACK signal from the EEPROM.
3. When the EEPROM sends the ACK signal, the EMC2101-R sends a second Start signal and continues sending the Block Read Command (see Table 2-7) to the same client address. It reads 256 data bytes from the EEPROM sending an ACK between each data byte. When 256 data bytes have been received, it sends a NACK signal followed by a STOP bit.
4. Resets the device as an SMBus Client.

If the EMC2101-R does not receive an acknowledge bit from the EEPROM, then the following occurs:

1. The ALERT/TACH pin will be asserted and will remain asserted until a Host device initiates communication with the EMC2101 and reads the Status Register at offset 0x02. The ALERT/TACH pin will be deasserted after a single Status Register read (i.e. it is not sticky).
2. The EMC2101-R will reset its SMBus protocol as a client interface and start operating from the default conditions.

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TABLE 2-7: **BLOCK READ BYTE PROTOCOL**

START	Client Address	WR	ACK	Register Address	ACK	START	Client Address	RD	ACK	Register Data	. . .
1	7	1	1	8	1	1	7	1	1	8	. . .

ACK	Register Data (00h)	ACK	Register Data (01h)	ACK	Register Data (02h)	. . .	ACK	Register Data (FFh)	NACK	STOP
1	8	1	8	1	8	. . .	1	8	1	1

Note: The shaded columns represent data sent from the EMC2101 to the EEPROM device.

It is recommended that the EEPROM that is used to be an AT24C02B or equivalent device. The EEPROM client address must be `101_0000b`. The device must support a block-read command, 8-bit addressing and 8-bit data formatting using a 2-wire bus. The device must support 3.3V digital switching logic and may not pull the SMCLK and SMDATA pins above 5V. Data must be transmitted MSB first.

No other SMBus Host should exist on the SMDATA and SMCLK lines. The presence of another SMBus Host will cause errors in reading from the EEPROM.

The EEPROM should be loaded to mirror the register set of the EMC2101 with the desired configuration set. All undefined registers in the EMC2101 register set should be loaded with 00h in the EEPROM. Likewise, all registers that are read-only in the EMC2101 register set should be loaded with 00h in the EEPROM.

Because of the interaction between the Fan Control Look-up Table and the Fan Configuration Register, the EEPROM Loader stores the contents of the Fan Configuration Register and updates this register at the end of the EEPROM loading cycle. (See **Section 5.16 "Fan Configuration Register"** and **Section 5.22 "Fan Control Look-Up Table Registers"**).

3.0   PIN DESCRIPTIONS

The description of the pins is listed in Table 3-1.

TABLE 3-1:   EMC2101 PIN DESCRIPTION

8-pin MSOP	Pin Name	Pin Type	Description
1	V_{DD}	Power	3.3V Power supply
2	DP	AI	External diode positive (anode) connection
3	DN	AI	External diode negative (cathode) connection
4	FAN	OD (5V)	PWM Output (default - software programmed)
		AO	DAC Output (software programmed)
5	GND	Power	Ground
6	ALERT/TACH	OD (5V)	ALERT - Open drain I/O operates as active low interrupt or TACH input; requires pull-up resistor, which defines auto-configuration mode (see Table 4-1).
		DI (5V)	TACH - TACH input
7	SMDATA	DIOD Output (5V)	SMBus Data input/output
8	SMCLK	DIOD Output (5V)	SMBus Clock input

All pins labeled with (5V) are 5V tolerant.

For the 5V tolerant pins that have a pull-up resistor, the voltage difference between V_{DD} and the pull-up voltage must never exceed 3.6V

The pin types are described in Table 3-2.

TABLE 3-2:   PIN TYPES

Power	This pin is used to supply power or ground to the device
DI	Digital Input. This pin is used as a digital input and is 5V tolerant
AI	Analog Input. This pin is used as an input for analog signals
AO	Analog Output. This pin is used as an output for analog signals
DIOD	Digital Input/Open Drain Output. This pin is used as a digital I/O. When it is used as an output, it is open drain and requires a pull-up resistor. This pin is 5V tolerant.
OD	Open Drain Digital Output. This pin is used as a digital output. It is open drain and requires a pull-up resistor. This pin is 5V tolerant.

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4.0   GENERAL DESCRIPTION

The EMC2101 is an environmental monitoring device with a selectable PWM or DAC fan driver output, one external temperature monitoring channel and one internal temperature monitor. It contains advanced circuitry to remove errors induced by series resistance and CPU thermal diode process differences to provide accurate temperature measurements and accurate fan control.

Thermal management is performed automatically. The EMC2101 reads the temperature from both the external and internal temperature diodes and uses the external temperature data to control the fan speed.

The FAN output can be configured as a PWM (default) or DAC output. The PWM fan driver uses an eight entry look up table to create a programmable temperature response. The DAC output provides a linear drive for the system fan circuit using this same look up table.

Each temperature measurement channel is continuously compared against programmed high limits. The external diode channel is compared against a programmed low limit. ALERT/TACH interrupt pin is asserted if the measured value exceeds the high limit or drops below the low limit. In addition, the external diode contains a programmable critical temperature, TCRIT. If the measured temperature exceeds this TCRIT an interrupt is asserted on the ALERT/TACH pin and the fan is set to full on.

Finally, the EMC2101-R (only) has two configuration modes and two default fan settings based on the value of the pull-up-resistor on the ALERT/TACH pin. In the Manual Configuration Mode, the device acts as an SMBus client and waits to be configured by the system SMBus host. In the Automatic Configuration mode, the device automatically queries the SMBus for an EEPROM device and uploads configuration information from the EEPROM into its internal registers.

Figure 4-1 shows a system level block diagram of the EMC2101. Figure 4-2 shows a system level block diagram of the EMC2101-R.
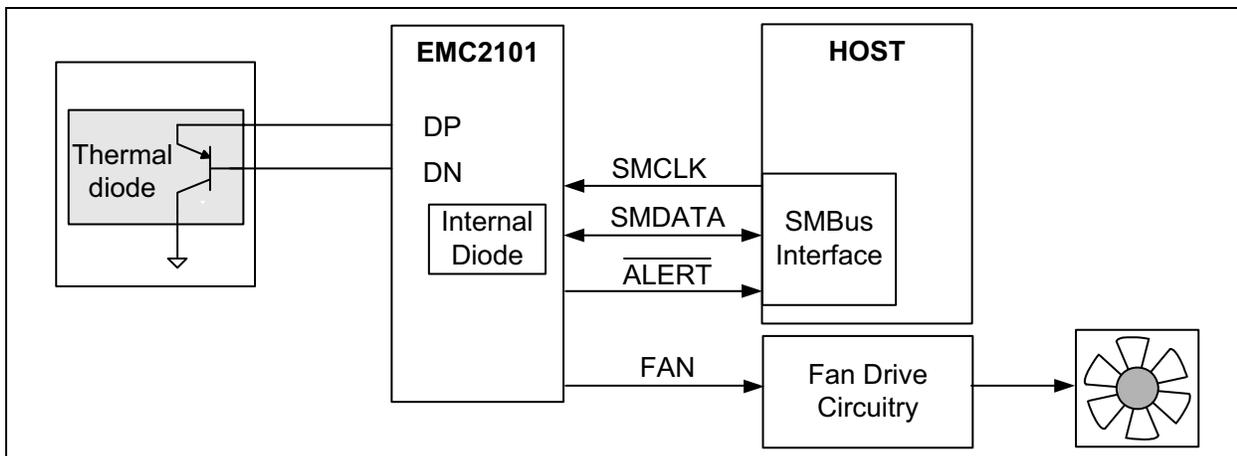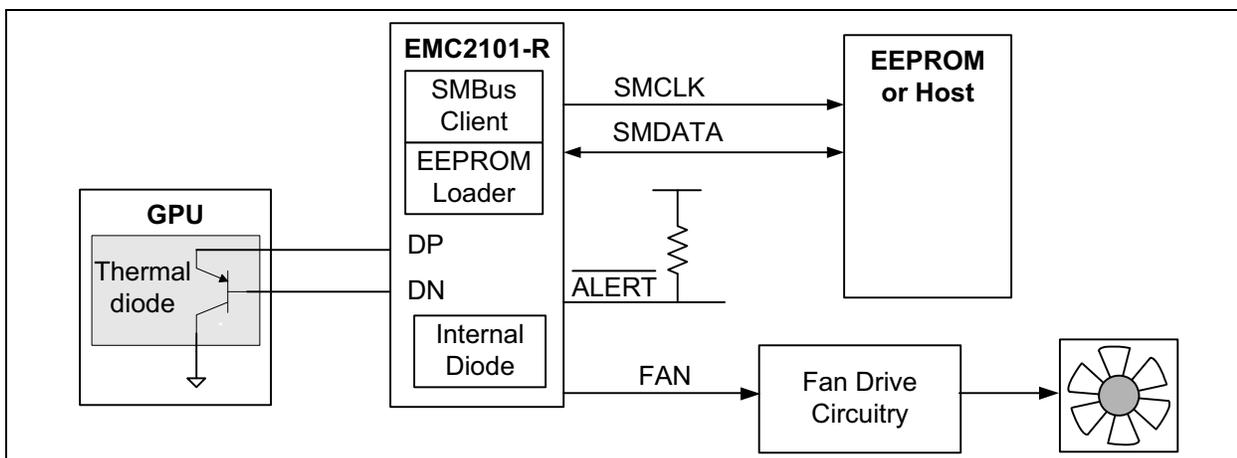

FIGURE 4-1:   *System Diagram for EMC2101.*

FIGURE 4-2:   *System Diagram for EMC2101-R.*

4.1 Modes of Operation (EMC2101-R Only)

The EMC2101-R has two modes of operation based on the pull-up resistor on the ALERT pin (see Table 4-1). The modes of operation are:

1. Host Configuration Mode: an SMBus Host configures the EMC2101-R upon startup to allow for polling for temperature or fan information or the user can use the ALERT pin interrupt to determine which action is required.

2. Automatic Configuration Mode: the EMC2101-R queries an SMBus compatible EEPROM located at a known address (see **Section 2.9 "Programming from EEPROM"**) and automatically loads its registers with the contents of the EEPROM. This mode does not require host intervention but a host can poll the device for temperature and fan information.

4.2 Power Up (EMC2101-R Only)

The EMC2101-R (only) will power up with the fan driver set to either 100% duty cycle or 0% duty cycle, depending on the value of the pull-up resistor on the ALERT/TACH pin. (See Table 4-1.) It will remain in this state until either the Fan Setting Register is written or until the following activities have occurred:

1. The Fan Control Look-Up Table is loaded and the PROG bit is set to '0'.

2. The temperature monitoring block performs its first comparison against the Look-Up Table.

If the Fan Control Look-Up Table is used, the EMC2101-R Fan Driver will be immediately set to the appropriate setting in the table based on the measured temperature.

4.3 Power Modes

The EMC2101 supports multiple power modes that are user configurable. The temperature monitoring and fan control functions of the device are independent. The power modes are:

1. Normal. The temperature monitoring and fan driver circuits are both active. The device updates all temperature channels at the user programmed conversion rate (see Register 5-4). Every time the temperature is updated, the limits are checked and the fan

driver is updated based on the values in the Fan Control Look-Up Table (if the Fan Control Look-Up Table is enabled).

2. Standby. The temperature monitoring and fan driver circuits are both disabled. The device will not update temperature data automatically and the fan output will be set to default drive. A one-shot command can be issued that will refresh the temperature data. The limits are only checked when the temperature data is updated.

3. Mixed. The temperature monitoring block is disabled, but the fan driver block is active. The device will not update temperature data automatically and the fan driver output will not be updated automatically based on temperature. A one-shot command can be issued that will refresh the temperature data and update the fan driver based on the values in the Fan Control Look-Up Table (if the Fan Control Look-Up Table is enabled).

4.4 ALERT/TACH Output

The ALERT/TACH pin (Pin 6) is an open drain output and requires a pull-up resistor to VDD when configured as an ALERT output.

When configured as a TACH input, the ALERT/TACH pin will not function as an ALERT output. Error conditions will not trigger an interrupt (though will be updated in the Status Registers as normal) and the MASK bits will do nothing. Likewise, the device will not respond to the ARA command.

For the EMC2101-R, the value of this pull-up resistor determines the initial FAN output mode of operation as well as whether the device auto loads from an EEPROM or via an SMBus host per Table 4-1.

After power-up, the EMC2101-R requires 10 ms to initialize and determine the operating mode.

When configured as an interrupt, the ALERT/TACH pin is maskable for each alert condition. If the ALERT/TACH pin is masked, then it will not respond to the corresponding condition (though the Alert Status Register will update normally). This pin has multiple functions described below and is controlled by ALERT_COMP bit (bit 0) in the Averaging Filter Register (BFh) (see **Section 5.23 "Averaging Filter Register"**).

TABLE 4-1: ALERT/TACH PULL-UP RESISTORS SMBus/FAN MODE FOR EMC2101-R

ALERT/TACH Pull-up Resistor	SMBus Mode	FAN Mode	Polarity Bit Setting (See Section 5.16, Fan Configuration Register)
5.6 kΩ ±5%	Host Load via SMBus	FAN output initialize to 100% Duty Cycle	1

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ALERT/TACH Pull-up Resistor	SMBus Mode	FAN Mode	Polarity Bit Setting (See **Section 5.16, Fan Configuration Register**)
10 kΩ ±5%	Host Load via SMBus	FAN output initialize to 0% Duty Cycle	0
18 kΩ ±5%	Auto Load via EEPROM	FAN output initialize to 100% Duty Cycle	1
33 kΩ ±5%	Auto Load via EEPROM	FAN output initialize to 0% Duty Cycle	0

4.4.1 ALERT/TACH AS A TEMPERATURE COMPARATOR

When the ALERT/TACH pin is used as a temperature comparator, the ALERT/TACH output is asserted when an out of limit measurement (> high limit, < low limit or > TCRIT limit) is detected on any diode (low limits only apply to the external diode channel) or when the external diode connections are open. When the condition is no longer true, the ALERT/TACH output will deassert. Reading from the Status Register will cause the ALERT/TACH pin to be released however it will not prevent it from being re-asserted based on the temperature comparisons.

Setting the MASK bit will not affect the ALERT/TACH pin when it is configured as a temperature comparator, however the individual channel mask bits will block the ALERT/TACH pin from being asserted.

4.4.2 ALERT/TACH AS AN INTERRUPT

When the ALERT/TACH pin is used as an interrupt signal the pin is asserted whenever an out-of-limit condition is detected. The ALERT/TACH pin will remain asserted until it is cleared even if the error condition is removed.

4.4.3 MASK BIT

The MASK bit behaves differently depending on which mode the ALERT/TACH pin is configured to operate in.

If the EMC2101 is configured with the ALERT/TACH pin operating in Interrupt Mode, the MASK bit will be set in the following cases:

1. Automatically after the Status Register has been read if any bits in the Status Register have been set, except BUSY and FAULT (see **Register 5-2**).

2. Automatically when the EMC2101 responds to an Alert Response Address (ARA) command on an SMBus and the ALERT/TACH pin is asserted. The ARA command does not clear the Status Register. If the MASK bit is cleared prior to reading and clearing the Status Register, then the ALERT/TACH pin will be asserted.

3. Directly via the SMBus.

In Interrupt Mode, the MASK bit will block the ALERT/TACH pin from being asserted in response to an error condition.

If the EMC2101 is configured with the ALERT/TACH pin operating in Comparator Mode, the MASK bit can only be set via the SMBus. In this mode, setting the MASK bit will not affect the ALERT/TACH pin.

In either mode, setting the individual channel mask bits will block the appropriate channel from asserting the ALERT/TACH pin.

4.5   Temperature Monitors

In general, thermal diode temperature measurements are based on the change in forward bias voltage of a diode when operated at two different currents. The change in forward bias voltage is proportional to absolute temperature (T), as shown in Equation 4-1.

EQUATION 4-1:

$$\Delta V_{BE} = \frac{\eta kT}{q} In \left(\frac{I_{HIGH}}{I_{LOW}} \right)$$

Where:

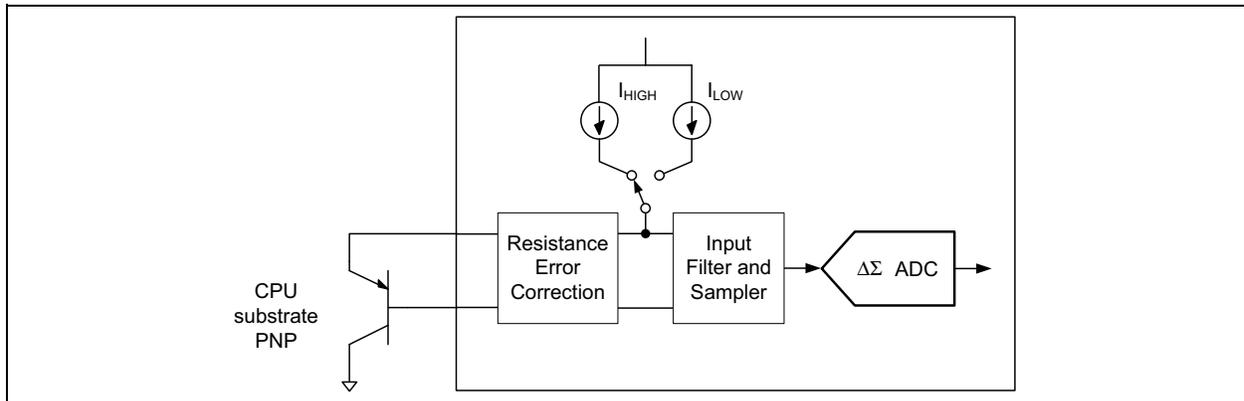|		
k	=	Boltzmann's constant
T	=	Absolute temperature in Kelvin
q	=	Electron charge
η	=	Diode ideality factor

FIGURE 4-3:   *Block Diagram of Temperature Monitoring Circuit.*

Figure 4-3 shows a block diagram of the temperature measurement circuit. As shown, the EMC2101 incorporates a delta-sigma analog to digital converter that integrates the temperature diode voltage from multiple bias currents.

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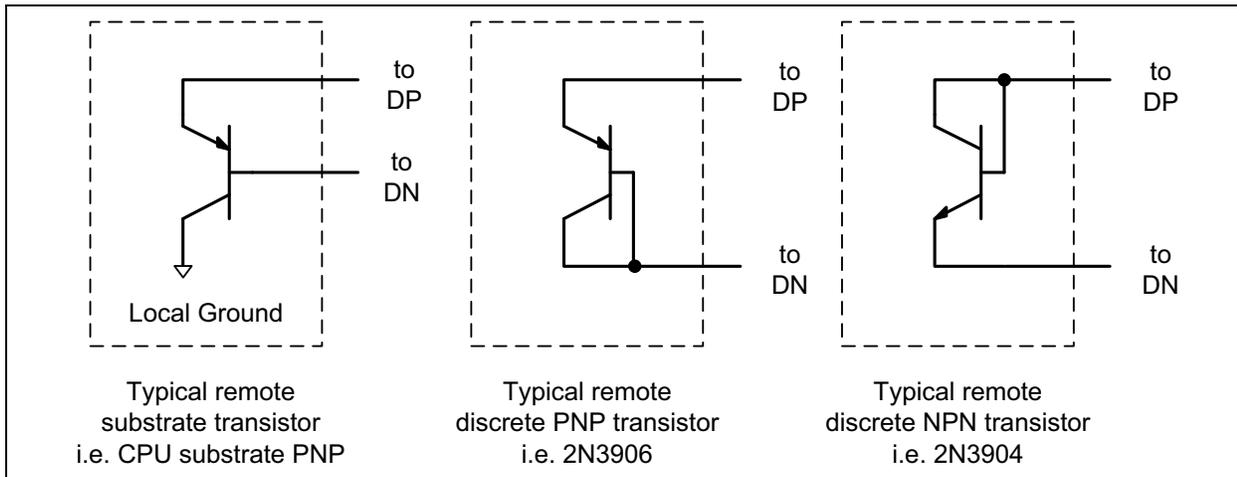The external temperature diodes can be connected as shown in Figure 4-4.

FIGURE 4-4: *External Diode Configurations.*

4.5.1 TEMPERATURE MEASUREMENT RESULTS AND DATA

The results of the internal and external temperature measurements are stored in the internal and external temperature registers respectively. These are then compared with the values stored in the High Limit Registers. The internal temperature measurements are stored in 8-bit format while the external temperature measurements are stored in 11-bit format.

The EMC2101 measures temperatures from -64°C to +127°C represented as a binary two's complement number. Internal temperatures are in +1°C steps, external temperatures are in +0.125°C steps.

Table 4-2 shows the temperature format for the external diode and Table 4-3 shows the temperature format for the internal diode.

TABLE 4-2: EMC2101 EXTERNAL TEMPERATURE DATA FORMAT

Temperature (°C)	Digital Output (Binary)
≤ -64	1100 0000 000
-55	1100 1001 000
-1	1111 1111 000
-0.125	1111 1111 111
+0	0000 0000 000
+0.125	0000 0000 001
+1	0000 0001 000
+25	0001 1001 000
+125	0111 1101 000
≥ +127.875	0111 1111 110
Diode Fault (Open condition)	0111 1111 000
Diode Fault (Short condition)	0111 1111 111

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TABLE 4-3: EMC2101 INTERNAL TEMPERATURE DATA FORMAT

Temperature (°C)	Digital Output (Binary)
≤ -64	1100 0000
-55	1100 1001
-1	1111 1111
+0	0000 0000
+1	0000 0001
+25	0001 1001
+125	0111 1101
+126	0111 1110
≥ +127	0111 1111

4.5.2 TEMPERATURE FILTER

The EMC2101 contains variable filtering options to suppress thermally or electrically noisy signals on the External Diode lines. This filter can be configured as Level 1, Level 2 or Disabled (see **Section 5.23 "Averaging Filter Register"**). The typical filter performance is shown in Figure 4-5 and Figure 4-6.
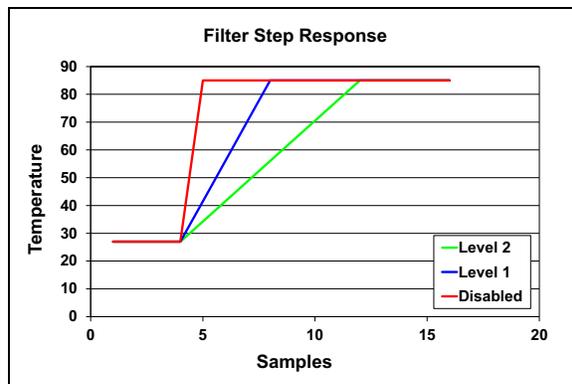

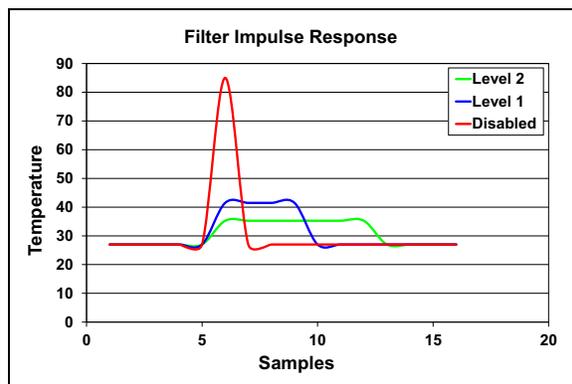**FIGURE 4-5:** *Temperature Filter Step Response.*

FIGURE 4-6: *Temperature Filter Impulse Response.*

4.5.3 BETA COMPENSATION

The EMC2101 is software configurable to monitor the temperature of basic diodes (e.g. 2N3904), or CPU thermal diodes. It automatically detects the type of external diode (CPU diode, diode connected transistor, or PN diode) and determines the optimal setting to reduce temperature errors introduced by beta variation.

4.5.4 RESISTANCE ERROR CORRECTION (REC)

Parasitic resistance in series with the external diodes will limit the accuracy obtainable from temperature measurement devices. The voltage developed across this resistance by the switching diode currents cause the temperature measurement to read higher than the true temperature. Contributors to series resistance are Printed Circuit Board (PCB) trace resistance, on die (i.e. on the processor) metal resistance, bulk resistance in the base and emitter of the temperature transistor. Typically, the error caused by series resistance is +0.7°C per ohm. Temperature errors caused by up to 100Ω of series resistance are automatically corrected.

4.5.5 PROGRAMMABLE IDEALITY FACTOR

The EMC2101 is designed for an external diode with an ideality factor of 1.008. When an external diode, processor or discrete, has a different ideality factor, an error is introduced in the temperature measurement which must be corrected. This is typically done using programmable offset registers but this correction is only accurate at one temperature since an ideality factor mismatch introduces an error that is a linear function of temperature. To provide maximum flexibility to the user, the EMC2101 provides a 6-bit register to set the ideality factor for the external diode which eliminates errors across all temperatures (see Table 5-2.).

This feature is only required in rare circumstances. The majority of errors introduced are corrected with the Beta Compensation and Resistance Error Correction circuitry.

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4.5.6 DIODE FAULTS

The EMC2101 detects the major types of diode faults; an open input DP-DN, a short across DP-DN, short to GND, and short to V_{DD}. For each temperature measurement made, the device checks for a diode fault on the external diode.

If an open fault or a short of the DP pin to V_{DD} is detected, then the temperature data is changed to +127°C and the Fault bit in the Status Register will be set. If the high and/or TCRIT limits are set below this value, and they are not masked, then the ALERT/TACH pin will be asserted. In addition, the HIGH and TCRIT status bits will be set accordingly.

If a short between the diode pins or a short to GND is detected, then the temperature data is changed to +127.875°C. If the high and/or TCRIT limits are set below this value, and they are not masked, then the ALERT/TACH pin will be asserted. In addition, the HIGH and TCRIT status bits will be set accordingly. The FAULT bit will not be set.

If the Temperature Filter is enabled and a diode fault occurs, the diode fault status bit will be set and the temperature data is updated immediately. The Filter will stop accumulating data so long as the diode fault remains in effect.

When a Diode Fault is detected, the ALERT/TACH pin behavior is still subject to the Fault Queue.

4.6 Fan Control

The EMC2101 includes either a PWM or a linear DAC based fan driver on the shared FAN pin. Both PWM and DAC use the Fan Control Look-Up Table and/or Fan Setting Register interchangeably as well as the Spin-Up Routine.

In addition, the EMC2101 can monitor the fan speed using the ALERT/TACH pin.

4.6.1 DAC DRIVER

The Linear DAC driver included in the EMC2101 has 6-bits of resolution based on the supply voltage and is used for linear drive fan circuits. Its advantages over PWM drive circuits include reduced circuit complexity at the expense of reduced effective signal range.

When using the DAC Driver, the pull-up resistor on the FAN pin should be removed.

The DAC driver output voltage is controlled by either the Fan Setting Register (see **Section 5.18 "Fan Setting Register"**) or the Fan Control Look-Up Table Registers (see **Section 5.22 "Fan Control Look-Up Table Registers"**). It is also controlled by the POLARITY bit (see **Section 5.16 "Fan Configuration Register"**). The PWM Frequency Register (see **Section 5.19 "PWM Frequency Register"**) and PWM

Divider Register (see **Section 5.20 "PWM Frequency Divide Register"**) have no effect on the DAC's output voltage range, resolution, or response.

4.6.2 PWM DRIVER

The PWM driver included in the EMC2101 has, at most, 64 steps equaling 1.5% resolution. The effective resolution, duty cycle, and frequency are all adjustable based on programmed values. The advantages over linear drive circuits include a large signal range (0% to 100% duty cycle) at the expense of added complexity on the drive circuit.

The PWM output is open drain and requires a pull-up resistor to V_{DD}.

4.6.3 TACH MONITOR

The TACH monitor counts the number of clock pulses that occur between five edges of the TACH signal. The monitor assumes that the tachometer signal is always valid (such as generated from a 4-wire fan or a direct drive fan) and that the tachometer signal generates 2 TACH pulses per fan revolution.

4.6.4 FAN CONTROL LOOK-UP TABLE

The EMC2101 uses an 8-entry look-up table to apply a user-programmable fan control profile based on measured temperature. The user programs the Fan Control Look-Up Table using incrementally higher temperatures and the desired fan output that should be set when that temperature is reached.

If the measured temperature on the External Diode channel exceeds any of these temperature thresholds, the fan output will be automatically programmed to the desired setting corresponding to the exceeded temperature. When the measured temperature drops to a point below any lower threshold minus the hysteresis value, the fan output will be set to the corresponding lower set point.

Figure 4-7 shows an example of this operation.

If the Fan Control Look-Up Table is not used, the user may program the Fan Output directly by writing to the Fan Setting Register (4Ch - see Register 5-16).
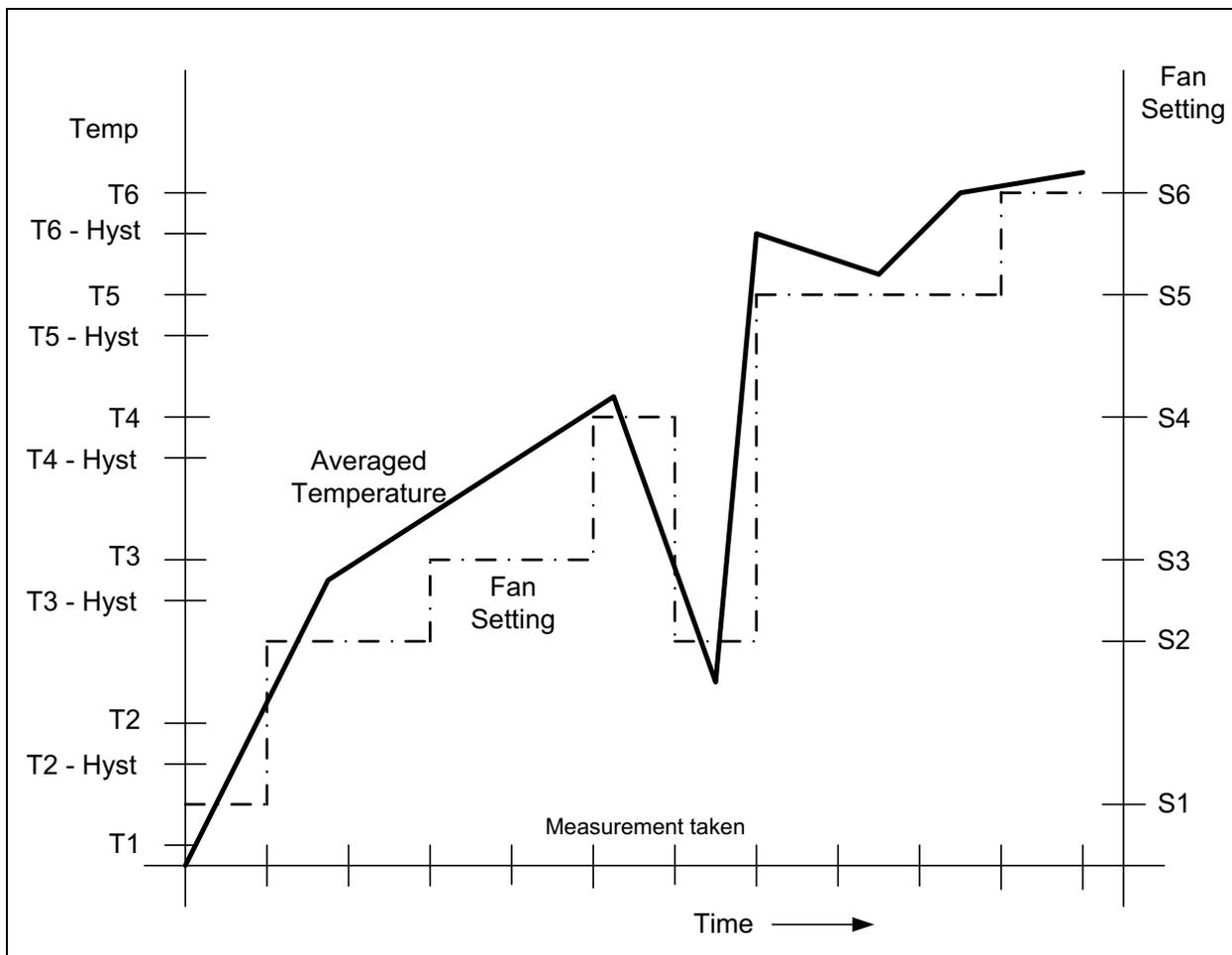
FIGURE 4-7: *Fan Control Look-Up Table Example.*

4.7 Fault Queue

The EMC2101 supports a Fault Queue feature to reduce interrupts caused by spurious temperature readings. This feature (see **Section 5.5 "Configuration Register"**) will not trigger an interrupt until the device has measured three consecutive out-of-limit HIGH, LOW, or T_CRIT temperature readings. Figure 5.8 shows an example of this behavior. The Fault Queue only applies to the External Diode channels.

FIGURE 4-8: *Example Fault Queue Response.*

5.0   REGISTER DESCRIPTION

The following registers are accessible through the SMBus Interface. The registers are described in functional order. Registers with multiple addresses are included for software compatibility. Writing or reading from either address will point to the same internal register.
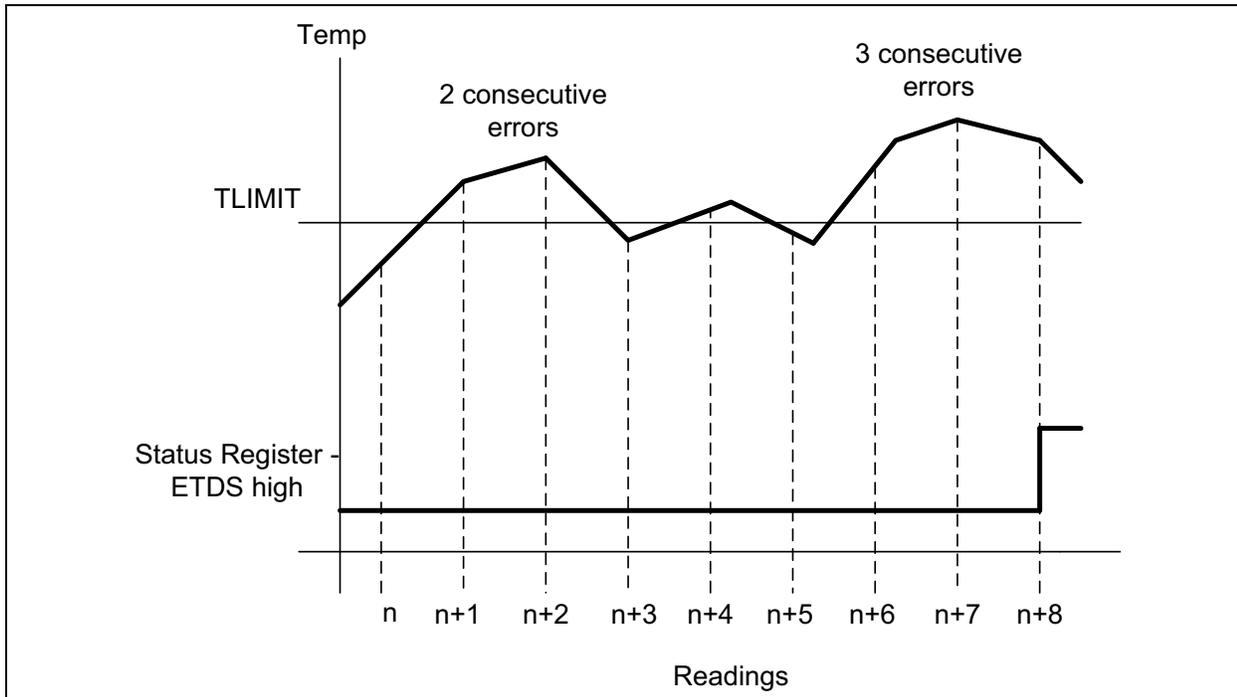
TABLE 5-1:   REGISTER SET IN HEXADECIMAL ORDER

Register Address	R/W	Register Name	Function	Default Value
00h	R	Internal Temperature	Stores the Internal Temperature	00h
01h	R	External Diode Temperature High Byte	Stores the External Temperature High Byte	00h
02h	R	Status	Reports internal, external and TCRIT alarms	00h
03h and 09h	R/W	Configuration	Alert Mask, STANDBY, TCRIT override, Alert Fault Queue	00h
04h and 0Ah	R/W	Conversion Rate	Sets conversion rate	08h (16/sec)
05h and 0Bh	R/W	Internal Temp Limit	ALERT/TACH asserted if measured temp above this value	46h (+70°C)
07h and 0Dh	R/W	External Temp High Limit High Byte	ALERT/TACH asserted if measured temp above this value	46h (+70°C)
08h and 0Eh	R/W	External Temp Low Limit High Byte	ALERT/TACH asserted if measured temp below this value	00h (+0°C)
0Ch	R/W	External Temperature Force	Force the temperature for determining the next fan speed used in the Fan Control Look-Up Table	00h
0Fh	R/W	One Shot	When written, performs a one-shot conversion.	00h
10h	R	External Diode Temperature Low Byte	Stores the External Temperature Low Byte	00h
11h	R/W	Scratchpad	Scratchpad – This register is read/write but does nothing	00h
12h	R/W	Scratchpad	Scratchpad – This register is read/write but does nothing	00h
13h	R/W	External Diode High Limit Low Byte	Fractional data of High Limit	00h
14h	R/W	External Diode Low Limit Low Byte	Fractional data of Low Limit	00h
16h	R/W	Alert Mask	Disables alarms	A4h
17h	R/W	External Diode Ideality Factor	Sets ideality factor based on diode type	12h (1.008)
18h	R/W	Beta Compensation Factor	Compensates for transistors with various beta factors	08h
19h	R/W	TCRIT Temp Limit	Fan will be set to full speed if external temp above this value	55h (+85°C)
21h	R/W	TCRIT Hysteresis	Amount of hysteresis applied to TCRIT Temp (1LSB = +1°C)	0Ah (+10°C)

Note 1:   The Look Up Table Registers are made Read Only if the PWM Program bit (bit 5) in PWM Configuration Register (4Ah) is set.

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TABLE 5-1: REGISTER SET IN HEXADECIMAL ORDER (CONTINUED)

Register Address	R/W	Register Name	Function	Default Value
46h	R	TACH Reading Low Byte	Stores the lower 6 bits of the TACH count and the TACH configuration bits	FFh
47h	R	TACH Reading High Byte	Stores the upper 8 bits of the TACH count	FFh
48h	R/W	TACH Limit Low Byte	Stores the lower 6 bits of the TACH Limit	FFh
49h	R/W	TACH Limit High Byte	Stores the upper 8 bits of the TACH Limit	FFh
4Ah	R/W	FAN Configuration	Defines polarity of PWM or DAC	20h
4Bh	R/W	Fan Spin-up	Sets Spin Up options	3Fh
4Ch	R/W	Fan Setting	Sets PWM or DAC value	00h
4Dh	R/W	PWM Frequency	Sets the final PWM Frequency	17h
4Eh	R/W	PWM Frequency Divide	Sets the base PWM frequency	01h
4Fh	R/W	Lookup Table Hysteresis	Amount of hysteresis applied to Lookup Table Temp (1LSB = +1°C)	04h (+4°C)
50h	R/W (See **Note**)	Lookup Table Temp Setting 1	Look Up Table Temperature Setting 1	7Fh
51h	R/W (See **Note**)	Lookup Table Fan Setting 1	Associated Fan Setting for Temp Setting 1	3Fh
52h	R/W (See **Note**)	Lookup Table Temp Setting 2	Look Up Table Temperature Setting 2	7Fh
53h	R/W (See **Note**)	Lookup Table Fan Setting 2	Associated Fan Setting for Temp Setting 2	3Fh
54h	R/W (See **Note**)	Lookup Table Temp Setting 3	Look Up Table Temperature Setting 3	7Fh
55h	R/W (See **Note**)	Lookup Table Fan Setting 3	Associated Fan Setting for Temp Setting 3	3Fh
56h	R/W (See **Note**)	Lookup Table Temp Setting 4	Look Up Table Temperature Setting 4	7Fh
57h	R/W (See **Note**)	Lookup Table Fan Setting 4	Associated Fan Setting for Temp Setting 4	3Fh
58h	R/W (See **Note**)	Lookup Table Temp Setting 5	Look Up Table Temperature Setting 5	7Fh
59h	R/W (See **Note**)	Lookup Table Fan Setting 5	Associated Fan Setting for Temp Setting 5	3Fh
5Ah	R/W (See **Note**)	Lookup Table Temp Setting 6	Look Up Table Temperature Setting 6	7Fh
5Bh	R/W (See **Note**)	Lookup Table Fan Setting 6	Associated Fan Setting for Temp Setting 6	3Fh
5Ch	R/W (See **Note**)	Lookup Table Temp Setting 7	Look Up Table Temperature Setting 7	7Fh
5Dh	R/W (See **Note**)	Lookup Table Fan Setting 7	Associated Fan Setting for Temp Setting 7	3Fh
5Eh	R/W (See **Note**)	Lookup Table Temp Setting 8	Look Up Table Temperature Setting 8	7Fh
5Fh	R/W (See **Note**)	Lookup Table Fan Setting 8	Associated Fan Setting for Temp Setting 8	3Fh

Note 1: The Look Up Table Registers are made Read Only if the PWM Program bit (bit 5) in PWM Configuration Register (4Ah) is set.

TABLE 5-1:   REGISTER SET IN HEXADECIMAL ORDER (CONTINUED)

Register Address	R/W	Register Name	Function	Default Value
BFh	R/W	Averaging Filter	Selects averaging function for external diode	00h
FDh	R	Product ID	ID	16h or 28h
FEh	R	Manufacturer ID	MCHP	5Dh
FFh	R	Revision Register	REV	01h

Note 1: The Look Up Table Registers are made Read Only if the PWM Program bit (bit 5) in PWM Configuration Register (4Ah) is set.

5.1   Data Read Interlock

When the External Diode High Byte Register is read, the External Diode Low byte is copied into an internal 'shadow' register. The user is free to read the low byte at any time and be guaranteed that it will correspond to the previously read high byte. Regardless if the low byte is read or not, reading from an External Diode High Byte Register will automatically refresh this stored low byte data.

When the TACH Reading Low Byte Register is read, the TACH Reading high byte is copied into an internal 'shadow' register. The user is free to read the high byte at any time and be guaranteed that it will correspond to the previously read low byte. Regardless if the high byte is read or not, reading from the TACH Reading Low Byte Register will automatically refresh this stored high byte data.

5.2   Register Descriptions

The registers are described in detail below. A bit entry of a '—' indicates that the bit is not used and will always read '0'.

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5.3   Temperature Data Registers

All temperatures are stored as an 11-bit value with the high byte representing the integer value and the low byte representing the fractional value left justified to occupy the MSBits.

REGISTER 5-1:   TEMPERATURE DATA REGISTERS (ADDRESSES 00h, 06h, 01h, 10h)

Address	R/W	Register	B7	B6	B5	B4	B3	B2	B1	B0	Default
00h	R	Internal Temperature	Sign	64	32	16	8	4	2	1	00h
01h	R	External Diode Temperature High Byte	Sign	64	32	16	8	4	2	1	00h
10h	R	External Diode Temperature Low Byte	0.5	0.25	0.125	—	—	—	—	—	00h

As shown in Register 5-1, the internal temperature monitor is stored as an 8-bit value while the external temperature is stored as an 11-bit value.

Please note that the internal temperature monitor is limited to the operating temperature limits of the part resulting in a guaranteed range of +0ºC to +85ºC.

5.4   Status Register

The Status Register is a read only register and returns the operational status of the part.

If the ALERT/TACH pin is configured as an ALERT output and any of these bits are set to '1' (except the BUSY bit and the FAULT bit), then the ALERT/TACH pin is asserted low (if interrupts are not masked (see Section 5.5, Configuration Register).

Reading from the Status Register will cause the MASK bit to be set if any bit (other than BUSY and FAULT) have been set. Each bit is automatically cleared when the error condition has been removed, however the

internal error condition flags may still be set. The ARA command must be used to clear the ALERT/TACH pin if there are no bits set in the Status Register. In addition, reading from the Status Register will clear all bits. If the error condition persists, then the bits will be reset at the end of the next conversion.

When the device is configured in Comparison Mode (see Section 5.23, Averaging Filter Register), reading the Status Register will not clear any active status bits (except EEPROM and FAULT). These bits are automatically cleared when the error condition is removed.

REGISTER 5-2:   STATUS REGISTER (ADDRESS 02h)

R	R	R	R	R	R	R	R
BUSY	INT_ HIGH	EEPROM	EXT_HIGH	EXT_LOW	FAULT	TCRIT	TACH
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	'1' = bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7   **BUSY**: Indicates that the ADC is converting; does not trigger an interrupt.

bit 6   **INT_ HIGH**: Internal temperature has met or exceeded the high limit.

bit 5   **EEPROM**: Indicates that the EEPROM could not be found when the device powers up in the Auto-Program Mode (see Section 4.1, Modes of Operation (EMC2101-R Only)). This bit only applies to the EMC2102-R. It will always read '0' for the EMC2101 device

bit 4   **EXT_HIGH**: External Diode temperature has exceeded the high limit.

bit 3   **EXT_LOW**: External Diode temperature has fallen below the low limit.

bit 2   **FAULT**: A diode fault has occurred on the External Diode.

bit 1   **TCRIT**: External Diode Temperature has met or exceeded the TCRIT limit.

bit 0   **TACH**: The TACH count has exceeded the TACH Limit.

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5.5 Configuration Register

The Configuration Register controls the basic functionality of the EMC2101. The bits are described below.

REGISTER 5-3:   CONFIGURATION REGISTER (ADDRESSES 03h AND 09h)

RW	RW	RW	RW	RW	RW	RW	RW
MASK	STANDBY	FAN_STANDBY	DAC	DIS_TO	ALT_ TCH	TCRIT OVRD	QUEUE
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0
-n = Value at POR	'1' = bit is set	'0' = Bit is cleared x = Bit is unknown

bit 7   **MSKAL**: Masks the ALERT/TACH pin functionality when the device is configured as an ALERT output in Interrupt Mode. This bit is ignored if the ALERT/TACH pin is configured as an ALERT output in Comparator Mode or if it is configured as a TACH input.
The internal error condition flags are not affected by setting the MASK bit. Therefore, if the MASK bit is set manually (instead of by reading the Status Register or sending the ARA command), and it is cleared, the ALERT/TACH pin may be reasserted without any apparent error conditions present. It is not recommended that the MASK bit be manually set to clear the ALERT/TACH pin.
1 = The ALERT/TACH pin will be masked and will not generate an interrupt. The Status Register will still be updated normally.
0 = (default) The ALERT/TACH pin will be asserted if any bit is set in the Status Register. Once the pin is asserted, it will remain asserted.

bit 6   **STANDBY**: Determines operational mode of the device.
1 = Low power standby mode. In this mode, the Temperature monitor is disabled and the Fan drivers may be disabled depending on the status of the FAN_STANDBY bit.
0 = (default) Operational mode, monitoring temperatures, updating FAN output.

bit 5   **FAN_STANDBY**: Determines the operation of the FAN driver when the device is put into low power standby mode.
1 = FAN output will be inactive when the STANBDY bit is set. The driver will be set at the default drive based on the pull-up resistors on the ALERT/TACH pin (see Table 4-1).
0 = (default) FAN output will remain active when the STANDBY bit is set.

bit 4   **DAC**: Determines FAN output mode.
1 = DAC output enabled at FAN pin.
0 = (default) PWM output enabled at FAN pin.

bit 3   **DIS_TO**: Disables the SMBus Time-out functionality.
1 = The SMBus Time-out functionality is disabled. The client block will only reset if it receives a STOP bit.
0 = (default) The SMBus Time-out functionality is enabled and will reset the client block if the clock is held in a single state for more than 25 ms and less than 35 ms.

bit 2   **ALT_TCH**: Determines the functionality of the ALERT/TACH pin.
1 = The ALERT/TACH pin will function as a high impedance TACH input. This may require an external pull-up resistor to set the proper signaling levels
0 = (default) The ALERT/TACH pin will function as an open drain, active low interrupt.

bit 1   **TCRITOVRD**: Allows the TCRIT limit to be overridden.
1 = The TCRIT limit is unlocked for modification. The TCRIT limit can only be changed once. To adjust TCRIT again, a power cycle is required.
0 = (default) TCRIT limit is set to default value and locked.

bit 0   **QUEUE**: Sets the number of external diode over-temp measurements required to assert ALERT/TACH pin.
1 = ALERT/TACH pin is asserted (and status bit set) after three consecutive external temperature measurements exceed the high limit or the TCRIT limit or drop below the low limit.
0 = (default) ALERT/TACH pin is asserted (and status bit set) after one external temperature measurement exceeds the high limit or the TCRIT limit or drops below the low limit.

5.6 Conversion Rate Register

REGISTER 5-4: CONVERSION RATE REGISTER (ADDRESS 04h AND 0Ah)

U-0	U-0	U-0	U-0	RW	RW	RW	RW
—	—	—	—	CONV3	CONV2	CONV1	CONV0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0
-n = Value at POR	'1' = bit is set	'0' = Bit is cleared x = Bit is unknown

bit 7-4   **Unimplemented**: Read as '0'

bit 3-0   **CONV[3:0]**: Determines the conversion rate as shown below:

CONV[3:0]				Conversions/Second
3	**2**	**1**	**0**	
0	0	0	0	1/16
0	0	0	1	1/8
0	0	1	0	1/4
0	0	1	1	1/2
0	1	0	0	1
0	1	0	1	2
0	1	1	0	4
0	1	1	1	8
1	0	0	0	16 (default)
1	0	0	1	32
All others				32

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5.7 Temperature Limit Registers

The EMC2101 has two 8-bit limit registers, two 11-bit limit registers, and one hysteresis register. The limits are checked after every temperature conversion.

If the measured temperature for the internal diode exceeds the Internal Temperature limit, then the INT_HIGH bit is set in the Status Register. It will remain set until the internal temperature drops below the high limit.

If the measured temperature for the External Diode exceeds the 11-bit External Diode High Limit, or drops below the 11-bit External Diode Low Limit, then the appropriate status bit will be set. The status bit will remain set until the temperature is no longer violating the respective limits.

If the External Diode exceeds the TCRIT Temp Limit (even if it does not exceed the External Diode Temperature Limit), the TCRIT bit will be set in the Status Register.

The TCRIT bit will remain set in the Status Register until the External Diode Temperature drops below a lower threshold given by Equation 5-1.

EQUATION 5-1:

$$TEMP = (T_{CRIT} - T_{CRITHYS})$$

See Section 5.3, Temperature Data Registers and Section 5.5, Configuration Register for $\overline{ALERT}$/TACH pin functionality.

REGISTER 5-5: TEMPERATURE DATA REGISTERS

Address	R/W	Register	B7	B6	B5	B4	B3	B2	B1	B0	Default
05h and 0Bh	R/W	Internal Temp Limit	—	64	32	16	8	4	2	1	46h (+70°C)
07h and 0Dh	R/W	External Diode High Limit MSB	—	64	32	16	8	4	2	1	46h (+70°C)
08h and 0Eh	R/W	External Diode Low Limit MSB	—	64	32	16	8	4	2	1	00h (+0°C)
13h	R/W	External Diode High Limit LSB	0.5	0.25	0.125	—	—	—	—	—	00h
14h	R/W	External Diode Low Limit LSB	0.5	0.25	0.125	—	—	—	—	—	00h
19h	R/W	TCRIT Temp Limit	—	64	32	16	8	4	2	1	55h (+85°C)
21h	R/W	TCRIT Hysteresis	—	64	32	16	8	4	2	1	0Ah (+10°C)

5.8 External Temperature Force Register

The External Diode Force Register is used to force the Fan Control Look-Up Table to a specific fan-speed setting. When this function is enabled (see **Section 5.16 "Fan Configuration Register"**), the contents of this register are compared against the temperature thresholds in the Fan Control Look-Up Table to determine the fan setting to use.

The contents of this register represent temperature data in the same format as the data registers and can be updated at any time.

The External Diode Temperature Registers are updated normally with the measured temperature and compared against the THIGH and TCRIT limits normally but not used to determine the fan speed.

This mode is used if the host or system requires temperature data from a source other than the EMC2101 External Diode to be used for fan control.

REGISTER 5-6: EXTERNAL DIODE FORCE REGISTER (ADDRESS 0Ch)

Address	R/W	Register	B7	B6	B5	B4	B3	B2	B1	B0	Default
0Ch	R/W	External Temperature Force	Sign	64	32	16	8	4	2	1	00h

5.9 One Shot Register

The One Shot Register initiates an update of the temperature measurements. This register can be written at any time, however will only perform a one-shot conversion when the temperature monitoring is in standby mode. When the one shot temperature conversion is complete the temperature data registers are updated and the fan setting is updated if necessary. This register is self-clearing.

REGISTER 5-7: ONE SHOT REGISTER (ADDRESS 0Fh)

Address	R/W	Register	B7	B6	B5	B4	B3	B2	B1	B0	Default
0Fh	W	One Shot	Writing to this register initiates a one shot update of the temperature data. Data is not relevant and is not stored.								00h

5.10 Scratchpad Registers

The Scratchpad Registers are R/W registers that perform no function. They are included for software compatibility.

REGISTER 5-8: SCRATCHPAD REGISTERS (ADDRESSES 11h and 12h)

Address	R/W	Register	B7	B6	B5	B4	B3	B2	B1	B0	Default
11h	R/W	Scratchpad	B7	B6	B5	B4	B3	B2	B1	B0	00h
12h	R/W	Scratchpad	B7	B6	B5	B4	B3	B2	B1	B0	00h

5.11 Alert Mask Register

The Alert Mask Register enables interrupts from the temperature monitors and limits. Regardless of the condition of the individual mask bits, the Status Register will be updated normally.

REGISTER 5-9: EXTERNAL DIODE $\overline{\text{THERM}}$ LIMIT REGISTER (ADDRESS 16h)

RW	RW	RW	RW	RW	RW	RW	RW
1	INT_MSK	1	HIGH_MSK	LOW_MSK	1	TCRIT_MSK	TCH_MSK
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0
-n = Value at POR	'1' = bit is set	'0' = Bit is cleared x = Bit is unknown

bit 6   **INT_MSK**: Disables interrupts for the Internal Diode.
            1 = The Internal Diode will not generate interrupts.
            0 = (default) The Internal Diode will generate an interrupt if its measured temperature exceeds the Internal Diode high limit.

bit 4   **HIGH_MSK**: Disables interrupts for the External Diode high limit.
            1 = The External Diode will not generate an interrupt when the high limit is exceeded.
            0 = (default) The External Diode will generate an interrupt if its measured temperature exceeds the External Diode high limit.

bit 3   **LOW_MSK**: Disables interrupts for the External Diode low limit.
            1 = The External Diode will not generate an interrupt when the temperature drops below the low limit.
            0 = (default) The External Diode will generate an interrupt if its measured temperature drops below the External Diode low limit.

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REGISTER 5-9:   EXTERNAL DIODE T̅H̅E̅R̅M̅ LIMIT REGISTER (ADDRESS 16h)

bit 1   **TCRIT_MSK**: Disables interrupts for the TCRIT Limit.
           `1` = An interrupt will not be generated if TCRIT is exceeded.
           `0` = (default) An interrupt will be generated if the External Diode Temperature exceeds TCRIT.

bit 0   **TACH_MSK**: Disables interrupts for the TACH Limit.
           `1` = An interrupt will not be generated if the TACH limit is exceeded.
           `0` = (default) An interrupt will be generated if the measured TACH value exceeds the TACH Limit
           (indicating that the fan speed is too slow).

5.12   External Ideality Factor Register

This register stores the ideality factor that is automatically applied to the external diode. The Ideality factor is a 6 bit value that allows for a bi-directional trim centered on an ideality factor of 1.008. Table 5-2 defines each setting and the corresponding Ideality factor.

REGISTER 5-10:   EXTERNAL IDEALITY FACTOR REGISTER (ADDRESS 17h)

Address	R/W	Register	B7	B6	B5	B4	B3	B2	B1	B0	Default
17h	R/W	External Ideality Factor	—	—	IDCF[5:0]						12h

TABLE 5-2:   IDEALITY FACTOR LOOK-UP TABLE

Setting	Factor	Setting	Factor	Setting	Factor
08h	0.9949	18h	1.0159	28h	1.0371
09h	0.9962	19h	1.0172	29h	1.0384
0Ah	0.9975	1Ah	1.0185	2Ah	1.0397
0Bh	0.9988	1Bh	1.0200	2Bh	1.0410
0Ch	1.0001	1Ch	1.0212	2Ch	1.0423
0Dh	1.0014	1Dh	1.0226	2Dh	1.0436
0Eh	1.0027	1Eh	1.0239	2Eh	1.0449
0Fh	1.0040	1Fh	1.0253	2Fh	1.0462
10h	1.0053	20h	1.0267	30h	1.0475
11h	1.0066	21h	1.0280	31h	1.0488
12h	1.0080	22h	1.0293	32h	1.0501
13h	1.0093	23h	1.0306	33h	1.0514
14h	1.0106	24h	1.0319	34h	1.0527
15h	1.0119	25h	1.0332	35h	1.0540
16h	1.0133	26h	1.0345	36h	1.0553
17h	1.0146	27h	1.0358	37h	1.0566

5.13 Beta Compensation Register

This register is used to set the Beta Compensation factor that is used for the External Diode channel.

When using a diode-connected transistor (such as the 2N3904) or CPUs that implement the thermal diode as a two-terminal diode, the CPU compensation circuit must be disabled by writing a value of 07h to this register.

REGISTER 5-11: BETA COMPENSATION REGISTER (ADDRESS 18h)

RW	RW	RW	RW	RW	RW	RW	RW
—	—	—	—	ENABLE	BETA[2:0]		
bit 7							bit 0

Legend:			
RC = Read-then-clear bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	'1' = bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-4 **Unimplemented**: Read as '0'

bit 3 **ENABLE**: Enables the Beta Compensation Factor Autodetection Algorithm.
1 = (default) The Beta Compensation Factor Autodetection circuitry is enabled. At the beginning of every conversion, the circuitry will determine the optimal Beta Compensation factor setting and use the detected setting. The value of the BETA[2:0] bits will be ignored.
0 = The Beta Compensation Factor Autodetection circuitry is disabled. The External Diode will always use the Beta Compensation factor set by the BETA[2:0] bits.

bit 2-0 **BETA**: Selects the Beta Compensation factor that the External Diode will use if the autodetection circuitry is disabled. Table 5-3 shows the setting that should be used based on the expected beta value of the substrate transistor connected to the External Diode channel.
Care should be taken when setting the BETA[2:0] bits. If the Beta Compensation factor is set at a beta value that is higher than the transistor beta, then the circuit may introduce measurement errors.

TABLE 5-3: CPU BETA VALUES

Enable	B2	B1	B0	Minimum Beta
0	0	0	0	0.11
0	0	0	1	0.18
0	0	1	0	0.25
0	0	1	1	0.33
0	1	0	0	0.43
0	1	0	1	1.00
0	1	1	0	2.33
0	1	1	1	Disabled
1	X	X	X	Automatic detection

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5.14   TACH Reading Registers

The TACH Registers hold the 16-bit TACH Reading. This reading represents the number of TACH counts detected. The RPM of the fan can be determined by Equation 5-2 (see also **Appendix C: "TACH Reference Table"**). The bit weighting of each TACH[15:0] bit is shown in parenthesis after the value. When determining the final fan speed, the TACH[15:0] bits need to be decoded into an equivalent decimal number.

REGISTER 5-12:   TACH READING REGISTERS (ADDRESSES 46h AND 47h)

Address	R/W	Register	B7	B6	B5	B4	B3	B2	B1	B0	Default
46h	R	TACH Reading Low Byte	TACH7 (128)	TACH6 (64)	TACH5 (32)	TACH4 (16)	TACH3 (8)	TACH2 (4)	TACH1 (2)	TACH0 (1)	FFh
47h	R	TACH Reading High Byte	TACH15 (32768)	TACH14 (16384)	TACH13 (8192)	TACH12 (4096)	TACH11 (2048)	TACH10 (1024)	TACH9 (512)	TACH8 (256)	FFh

EQUATION 5-2:

$$RPM = \frac{5,400,000}{TACH\_Count}$$

Where:

TACH_COUNT = the decimal representation of the TACH[15:0] bits.

5.15   TACH Limit Registers

The TACH Limit Registers store the maximum TACH count that the fan is expected to operate at. TACH count is inversely proportional to the actual fan speed. This limit is used to guarantee that the fan has spun up properly. If the measured TACH is higher than this limit (indicating that the fan speed is lower than the minimum RPM value), then the TACH bit is set in the Status Register.

Additionally if the measured TACH count exceeds this limit, depending on the status of the TACH_M[1:0] bits (see **Section 5.16 "Fan Configuration Register"**), the TACH reading registers may be forced to FFFFh.

REGISTER 5-13:   TACH READING LOW BYTE REGISTER (ADDRESSES 48h AND 49h)

Address	R/W	Register	B7	B6	B5	B4	B3	B2	B1	B0	Default
48h	R/W	TACH Limit Low Byte	TACH_L7	TACH_L6	TACH_L5	TACH_L4	TACH_L3	TACH_L2	TACH_L1	TACH_L0	FFh
49h	R/W	TACH Limit High Byte	TACH_L15	TACH_L14	TACH_L13	TACH_L12	TACH_L11	TACH_L10	TACH_L9	TACH_L8	FFh

5.16   Fan Configuration Register

The Fan Configuration Register enables the Fan Control Look-Up Table and polarity of the PWM signal driving the output.

REGISTER 5-14:   FAN CONFIGURATION REGISTER (ADDRESS 4Ah)

U-0	R/W	R/W	R/W	R/W	R/W	R/W	R/W
—	FORCE	PROG	POLARITY	CLK_SEL	CLK_OVR	TACH_M[1:0]	
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0
-n = Value at POR	'1' = bit is set	'0' = Bit is cleared x = Bit is unknown

bit 7   **Unimplemented**: Read as '0'

bit 6   **FORCE**: Enables the External Temperature Force Register. This bit is not used if the Fan Control Look-Up Table is not used.
1 = The External Temperature Force Register is used. When determining the position in the Fan Control Look-Up Table, the contents of the External Temperature Force Register will be used instead of the measured External Diode temperature. All limits will be checked against the measured External Diode temperature as normal.
0 = (default) The External Diode Force Register is not used. The measured External Diode temperature is used to determine the position in the Fan Control Look-Up Table.

bit 5   **PROG**: Enables the Fan Control Look-Up Table for update and sets fan driver output based on Fan Control Look-Up Table values.
1 = (default) The Fan Setting Register and Fan Control Look-Up Table Registers can be written. The value written into the Fan Setting Register will be instantly applied to the fan driver and the Fan Control Look-Up Table will not be used.
0 = The Fan Setting Register and Fan Control Look-Up Table Registers are read-only and the Fan Control Look-Up Table Registers will be used.

bit 4   **POLARITY**: Sets the polarity of the Fan output driver. For the EMC2101-R, the value of this bit is determined by the value of the pull-up resistor on the ALERT/TACH pin (see Table 4-1). When the PWM default value is set at 100% duty cycle, the default value is set to '1' and when the PWM default value is set to 0% duty cycle, the default value is set to '0'. This occurs within 10 ms after power-up.
1 = The polarity of the Fan output driver is inverted. A '00h' setting will correspond to a 100% duty cycle or maximum DAC output voltage.
0 = (default) The polarity of the Fan output driver is noninverted. A '00h' setting will correspond to a 0% duty cycle or minimum DAC output voltage.

bit 3   **CLK_SEL**: Determines the base clock that is used to determine the final PWM frequency.
1 = The base clock that is used to determine the PWM frequency is 1.4 kHz.
0 = (default) The base clock that is used to determine the PWM frequency is 360 kHz.

bit 2   **CLK_OVR**: Overrides the CLK_SEL bit and uses the Frequency Divide Register to determine the base PWM frequency. It is recommended that this bit be set for maximum PWM resolution.
1 = The base clock that is used to determine the PWM frequency is set by the Frequency Divide Register.
0 = (default) The base clock frequency for the PWM is determined by the CLK_SEL bit.

bit 1-0   **TACH_M**: Determines the basic operation of the tachometer input as shown in Table 5-4.

TABLE 5-4:   TACH MODES

TACH_M[1]	TACH_M[0]	TACH Mode
0	0	False readings when under minimum detectable RPM (TACH Limit). (Default condition, see **Note**)
0	1	FFFFh reading when under minimum detectable RPM.
1	0	
1	1	

Note: When the PWM base clock is set at 360kHz mode 00b is used regardless of the setting of the TACH_M[1:0] bits.

5.17   Fan Spin Up Configuration Register

The Fan Spin Up Configuration register controls the spin-up behavior of the device. The Fan driver enters its spin-up routine any time it transitions from a minimum fan setting (00h) to a higher fan setting (but does not invoke the spin-up routine upon power up). Once the spin-up time has been met, the fan driver is reduced to the programmed setting.

REGISTER 5-15:   FAN SPIN UP CONFIGURATION REGISTER (ADDRESS 4Bh)

U-0	U-0	R	R	R	R	R	R
—	—	FAST_TACH	SPIN_DRIVE[1:0]		SPIN_TIME[2:0]		
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0
-n = Value at POR	'1' = bit is set	'0' = Bit is cleared x = Bit is unknown

bit 7-6   **Unimplemented**: Read as '0'

bit 5   **FAST_TACH**: Determines whether the Spin-Up routine aborts when the measured TACH is less than the TACH Limit.
1 = (default) The Spin-Up routine will abort when the TACH measurement is less than the TACH Limit or the programmed Spin-Up time is met, whichever is less. In this case, the SPIN_DRIVE[1:0] bits are ignored and the drive will always be at 100%.
0 = The Spin-Up routine uses the duty cycle and spin-up time independently of the TACH reading. This bit will be ignored if the ALT_TCH bit in the Configuration Register (see Section 5.5, Configuration Register) is set to '0'.
If the SPIN_TIME[2:0] bits are set at 000b, then the Spin-Up Routine is bypassed regardless of the status of this bit.

bit 4-3   **SPIN_DRIVE**: Determines the setting of the drive circuit during the Spin-Up routine according to Table 5-5.

bit 2-0   **SPIN_TIME**: Determines the length of time that the fan drive will remain at the SPIN_DRIVE[1:0] setting as shown in Table 5-6.

TABLE 5-5:   SPIN-UP DRIVE

SPIN_DRIVE[1:0]		Spin-Up Drive
1	0	
0	0	0 - Spin-Up Cycle bypassed
0	1	50% (half drive)
1	0	75% (3/4 drive)
1	1	100% (full drive) (default)

TABLE 5-6:   SPIN-UP TIME

SPIN_TIME[2:0]			Spin-Up Time
2	1	0	
0	0	0	0 - Spin-Up Cycle bypassed
0	0	1	0.05 sec.
0	1	0	0.1 sec.
0	1	1	0.2 sec.
1	0	0	0.4 sec.
1	0	1	0.8 sec.
1	1	0	1.6 sec.
1	1	1	3.2 sec. (default)

5.18   Fan Setting Register

The Fan Setting Register drives the fan driver when the Fan Control Look-Up Table is not used (see **Section 5.16 "Fan Configuration Register"**). Any data written to the Fan Setting registers is applied immediately to the fan driver (PWM or DAC). When the Fan Control Look-Up Table is being used, any writes to this register will be ignored. If the Fan Control Look-Up Table is disabled, then the fan drive will be set at the last value that was used by the Fan Control Look-Up Table.

When the Fan Control Look-Up Table Registers are being used, the register is read-only.

REGISTER 5-16:   FAN SETTING REGISTER (ADDRESS 4Ch)

Address	R/W	Register	B7	B6	B5	B4	B3	B2	B1	B0	Default
4Ch	R/W (see text)	Fan Setting	—	—	32	16	8	4	2	1	00h

The register applies to the fan driver in both PWM and DAC operating modes. The DAC output is determined by Equation 5-3 below.

EQUATION 5-3:

$$FAN = \left(\frac{FAN\_SETTING}{64}\right) \times V_{DD}$$

These values are independent of the POLARITY bit (see **Section 5.16 "Fan Configuration Register"**s). Therefore, a value of 00h in the Fan Setting Register will always refer to minimum output drive while a setting of 3Fh in the Fan Setting Register will always refer to maximum output drive.

The output of the DAC driver is dependent upon the current load. With a low current load, the output will be from 0V to an LSB (approximately 52 mV at V_{DD} = 3.3V) below V_{DD} with a maximum of 64 linear steps.

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5.19 PWM Frequency Register

The PWM Frequency Register determines the final PWM frequency and "effective resolution" of the PWM driver. It has no affect on the DAC output resolution.

It is recommended that this register be set at 1Fh for maximum resolution. See **Appendix B: "Advanced PWM Options"** for full operation of the PWM_F register and its interactions with the PWM Resolution and Duty Cycle.

REGISTER 5-17: PWM FREQUENCY REGISTER (ADDRESS 4Dh)

Address	R/W	Register	B7	B6	B5	B4	B3	B2	B1	B0	Default
4Dh	R/W	PWM Frequency	—	—	—	PWM_F[4:0]					17h

5.20 PWM Frequency Divide Register

This register holds an alternate PWM Frequency divide value that can be used instead of the CLK_SEL bit function. This register can be written at any time, however unless the CLK_OVR bit is set to a logic '1', it is not used.

When the CLK_OVR bit is set to a logic '1', the PWM Frequency Divide Register is used in conjunction with the PWM Frequency Register to determine the final PWM frequency that the load will see. When the CLK_OVR bit is set to a logic '0', the setting of this register is not changed and is not used to determine the effective PWM frequency.

REGISTER 5-18: PWM FREQUENCY DIVIDE REGISTER (ADDRESS 4Eh)

Address	R/W	Register	B7	B6	B5	B4	B3	B2	B1	B0	Default
4Eh	R/W	PWM Frequency Divide	PWM_D[7:0]								01h

The PWM frequency when the PWM Frequency Divide Register is used is shown in Equation 5-4.

EQUATION 5-4:

$$PWM\_D = \left(\frac{360k}{2 \times PWM\_F}\right) \times \frac{1}{FREQ} = \frac{5806}{FREQ}$$

Where:

PWM_F	=	The setting of the PWM Frequency register (4Dh)
PWM_D	=	The setting of the PWM Frequency Divide Register (4Eh)
FREQ	=	The desired PWM Frequency

Maximum resolution is achieved by setting the PWM Frequency Register to 1Fh. With maximum resolution, the desired PWM frequency can be achieved by adjusting the PWM Frequency Divide Register setting (PWM_D[7:0]) as shown in Table 5-7.

For example, if the user desires a 30 Hz PWM frequency with maximum PWM resolution, then the PWM_F[4:0] bits should be set at 1Fh (31d) and the PWM_D bits should be set at C1h (193d).

TABLE 5-7:   EXAMPLES OF FAN PWM FREQUENCY WITH MAXIMUM RESOLUTION

PWM_F[4:0] = 1Fh					
PWM_D[7:0] Setting	Effective Resolution (%)	Effective Duty Cycle (at 50% FAN_SETTING)	Effective Duty Cycle (at 75% FAN_SETTING)	FAN_SETTING to get 75% Duty Cycle	Effective PWM Frequency (Hz)
01h	1.61	51.6%	77.4%	2Eh (74.2%)	5806.5
11h	1.61	51.6%	77.4%	2Eh (74.2%)	341.6
20h	1.61	51.6%	77.4%	2Eh (74.2%)	181.5
47h	1.61	51.6%	77.4%	2Eh (74.2%)	81.8
C0	1.61	51.6%	77.4%	2Eh (74.2%)	30.2
C1	1.61	51.6%	77.4%	2Eh (74.2%)	30.0
FFh	1.61	51.6%	77.4%	2Eh (74.2%)	22.7

5.21   Fan Control Look-Up Table Hysteresis Register

The Fan Control Look-Up Table Hysteresis Register determines the amount of hysteresis applied to the temperature inputs of the fan control Fan Control Look-Up Table. See **Section 4.6.4 "Fan Control Look-Up Table"**.

REGISTER 5-19:   LOOK UP TABLE HYSTERESIS REGISTER (ADDRESS 4Fh)

Address	R/W	Register	B7	B6	B5	B4	B3	B2	B1	B0	Default
4Fh	R/W	Fan Control Look-Up Table Hysteresis	—	—	—	16	8	4	2	1	04h (+4°C)

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5.22 Fan Control Look-Up Table Registers

When the PROG bit in the Fan Configuration Register (see **Section 5.16 "Fan Configuration Register"**) is set to '0', these registers become read only.

The table should be loaded with the lowest temperature in the T1 register (50h) and increasing in temperature for all settings.

See **Section 4.6.4 "Fan Control Look-Up Table"** for description of the Fan Control Look Up Table operation. The fan speed settings for each temperature threshold follow the same behavior as the Fan Setting Register (see **Section 5.18 "Fan Setting Register"**).

TABLE 5-8: FAN CONTROL LOOK UP TABLE REGISTERS

Address	R/W	Register	B7	B6	B5	B4	B3	B2	B1	B0	Default
50h	R/W	Fan Control Look-Up Table T1	0	64	32	16	8	4	2	1	7Fh
51h	R/W	Fan Control Look-Up Table S1	—	—	32	16	8	4	2	1	3Fh
52h	R/W	Fan Control Look-Up Table T2	0	64	32	16	8	4	2	1	7Fh
53h	R/W	Fan Control Look-Up Table S2	—	—	32	16	8	4	2	1	3Fh
54h	R/W	Fan Control Look-Up Table T3	0	64	32	16	8	4	2	1	7Fh
55h	R/W	Fan Control Look-Up Table S3	—	—	32	16	8	4	2	1	3Fh
56h	R/W	Fan Control Look-Up Table T4	0	64	32	16	8	4	2	1	7Fh
57h	R/W	Fan Control Look-Up Table S4	—	—	32	16	8	4	2	1	3Fh
58h	R/W	Fan Control Look-Up Table T5	0	64	32	16	8	4	2	1	7Fh
59h	R/W	Fan Control Look-Up Table S5	—	—	32	16	8	4	2	1	3Fh
5Ah	R/W	Fan Control Look-Up Table T6	0	64	32	16	8	4	2	1	7Fh
5Bh	R/W	Fan Control Look-Up Table S6	—	—	32	16	8	4	2	1	3Fh
5Ch	R/W	Fan Control Look-Up Table T7	0	64	32	16	8	4	2	1	7Fh
5Dh	R/W	Fan Control Look-Up Table S7	—	—	32	16	8	4	2	1	3Fh
5Eh	R/W	Fan Control Look-Up Table T8	0	64	32	16	8	4	2	1	7Fh
5Fh	R/W	Fan Control Look-Up Table S8	—	—	32	16	8	4	2	1	3Fh

5.23 Averaging Filter Register

The Averaging Filter Register controls the level of digital averaging that is used for the External Diode temperature measurements as well as the configuration of the ALERT/TACH pin functionality.

REGISTER 5-20: AVERAGING FILTER REGISTER (ADDRESS BFh)

U-0	U-0	U-0	U-0	U-0	RW	RW	RW
—	—	—	—	—	FILTER[1:0]		ALERT_COMP
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	'1' = bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-3   **Unimplemented**: Read as '0'

bit 2-1   **FILTER**: Controls the level of digital filtering that is applied to the External Diode temperature measurements as shown in Table 5-9. See Figure 4-5 and Figure 4-6 for examples on the filter behavior.

bit 0   **ALERT_COMP**: Determines the functionality of the ALERT/TACH pin.
1 = The ALERT/TACH pin is configured to operate as a temperature comparator (see **Section 4.4.2 "ALERT/TACH as an Interrupt"**).
0 = The ALERT/TACH pin is configured to act as an interrupt (see **Section 4.4.1 "ALERT/TACH as a Temperature Comparator"**).

TABLE 5-9: AVERAGING SETTINGS

FILTER[1:0]		Averaging
1	0	
0	0	Disabled (default)
0	1	Level 1
1	0	Level 1
1	1	Level 2

5.24 Product ID Register

The Product ID Register contains a unique 8-bit word that identifies the product.

REGISTER 5-21: PRODUCT ID REGISTER (ADDRESS FDh)

Address	R/W	Register	B7	B6	B5	B4	B3	B2	B1	B0	Default
FDh	R	Product ID Register	0	0	0	1	0	1	1	0	16h (EMC2101)
			0	0	1	0	1	0	0	0	28h (EMC2101-R)

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5.25 Manufacturer ID Register

The Manufacturer ID register contains an 8-bit word that identifies Microchip as the manufacturer of the EMC2101

REGISTER 5-22: MANUFACTURER ID REGISTER (ADDRESS FEh)

Address	R/W	Register	B7	B6	B5	B4	B3	B2	B1	B0	Default
FEh	R	Microchip ID Register	0	1	0	1	1	1	0	1	5Dh

5.26 Revision Register

The Revision register contains an 8-bit word that identifies the die revision.

TABLE 5-10: REVISION REGISTER (ADDRESS FFh)

Address	R/W	Register	B7	B6	B5	B4	B3	B2	B1	B0	Default
FFh	R	Revision Register	0	0	0	0	0	0	0	1	01h

6.0 PACKAGING INFORMATION

6.1 Package Marking Information

8-Lead MSOP

Front

Example:

```
XXXXXXX
XXXXXXX
●
```

```
2101
0MTW
●  (e3)
```

Pin 1 ⸺

Back

Pin 1 ⸺

```
YYWW
YWW
NNNA
```

```
2219
219
256A
```
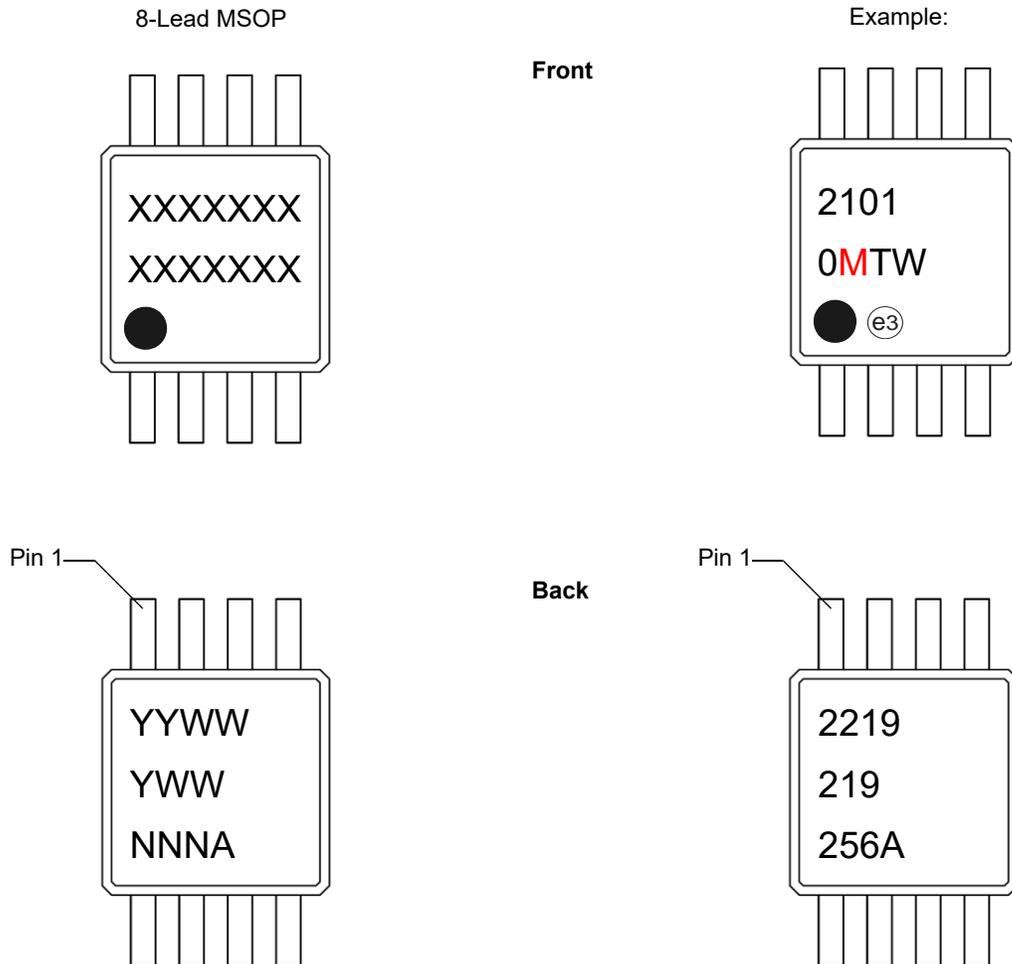
Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
Note:		In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

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8-Lead Plastic Micro Small Outline Package (UA) - 3x3 mm Body [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

TOP VIEW

SIDE VIEW

VIEW A–A

NOTE 1

SEE DETAIL B

SEATING PLANE

8-Lead Plastic Micro Small Outline Package (UA) - 3x3 mm Body [MSOP]

> **Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

DETAIL B
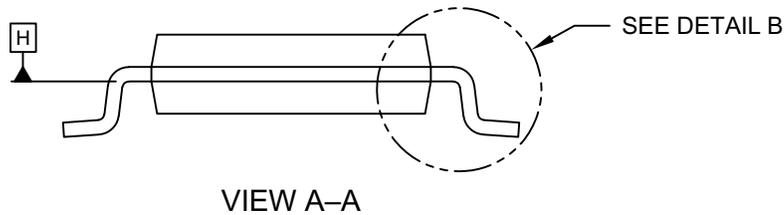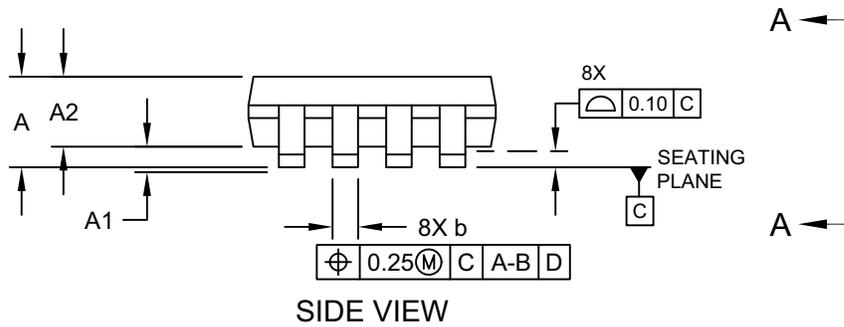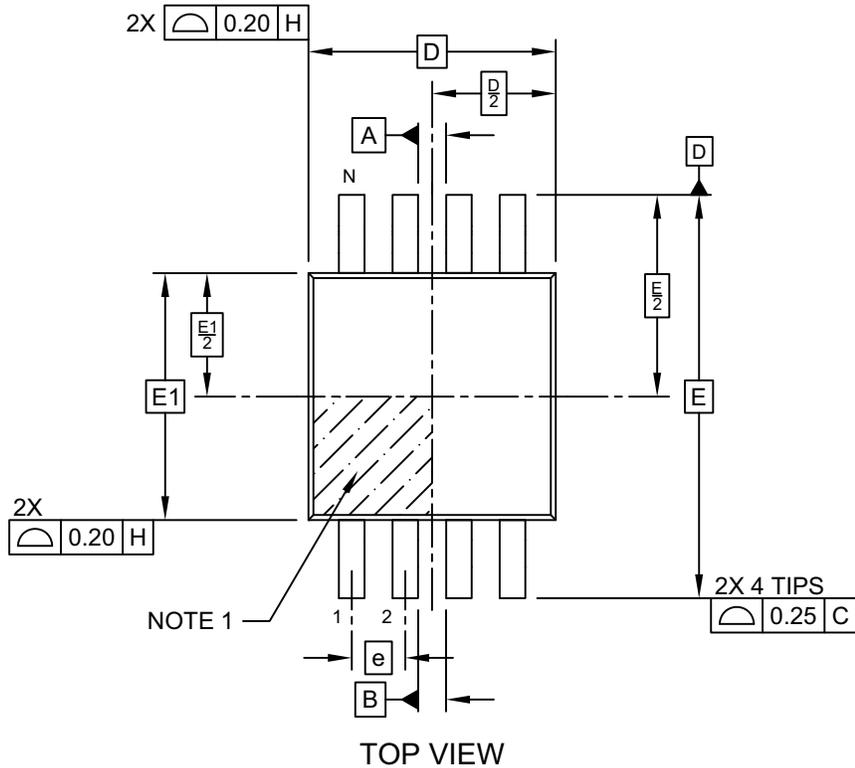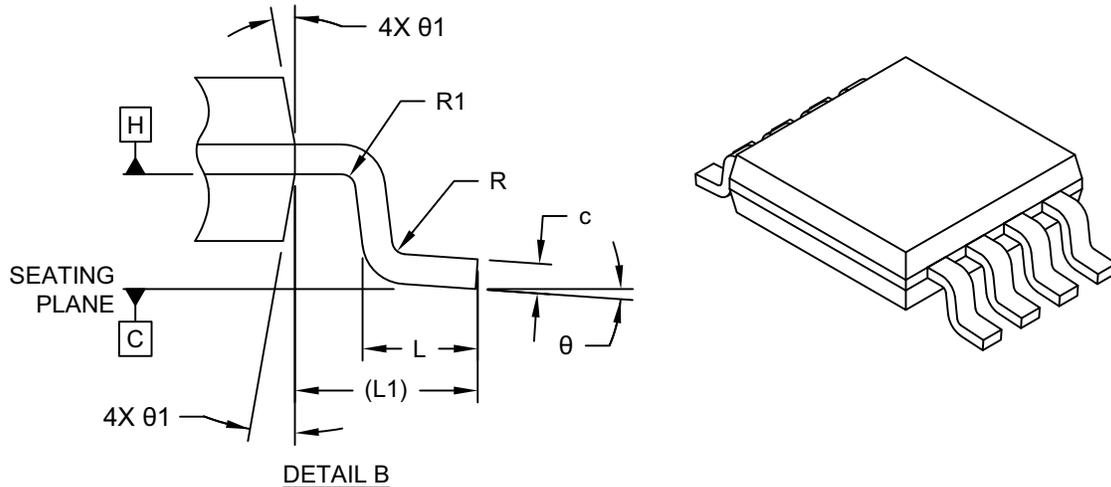
	Units	MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	1.10
Standoff	A1	0.00	–	0.15
Molded Package Thickness	A2	0.75	0.85	0.95
Overall Length	D		3.00 BSC	
Overall Width	E		4.90 BSC	
Molded Package Width	E1		3.00 BSC	
Terminal Width	b	0.22	–	0.40
Terminal Thickness	c	0.08	–	0.23
Terminal Length	L	0.40	0.60	0.80
Footprint	L1		0.95 REF	
Lead Bend Radius	R	0.07	–	–
Lead Bend Radius	R1	0.07	–	–
Foot Angle	θ	0°	–	8°
Mold Draft Angle	θ1	5°	–	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111-UA Rev D Sheet 2 of 2

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8-Lead Plastic Micro Small Outline Package (UA) - 3x3 mm Body [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

GX

SILK SCREEN

C G1

Y

X

E
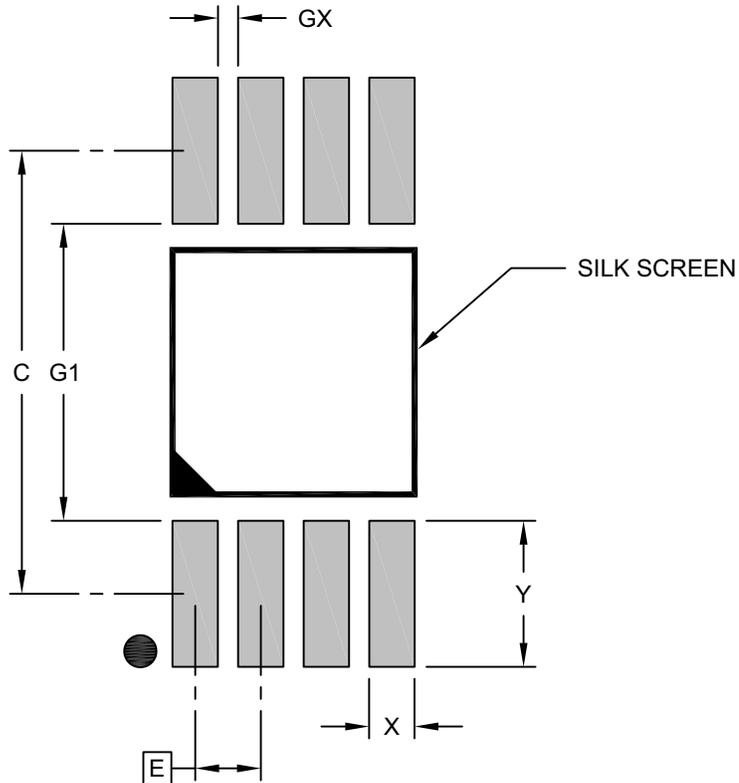
RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		4.40	
Contact Pad Width (X8)	X			0.45
Contact Pad Length (X8)	Y			1.45
Contact Pad to Contact Pad (X4)	G1	2.95		
Contact Pad to Contact Pad (X6)	GX	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

    BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2111-UA Rev D

APPENDIX A: REVISION HISTORY

Revision A (July 2022)

- Original release of this document.

NOTES:

APPENDIX B: ADVANCED PWM OPTIONS

The PWM Frequency Register determines the number of clocks (set by the CLK_SEL bit or the PWM_D register settings) represent 1/2 of the period of the final PWM output waveform. Therefore, as the PWM Frequency Register is updated, the PWM frequency is likewise updated. However, it also directly affects the PWM Resolution and PWM duty cycle.

The PWM frequency is set according to Equation 3 (**A** or **B**) or, if the PWM Divide Register is used, Equation 5-4 (see **Section 5.20 "PWM Frequency Divide Register"**).

The PWM Frequency Register does not affect the Fan Setting (either the Fan Setting Register or the Fan Setting entries in the Fan Control Look-up Table Registers).

The Fan Setting Register determines the number of clocks that the PWM output is high for is always based on 64 time steps for a PWM cycle. As the PWM Frequency Register changes (or the Fan Setting changes) the effective duty cycle will vary according to Equation 1 and the PWM resolution will vary according to Equation 2. This is a result of the "on" time determined by Fan Setting changing with respect to the overall PWM period determined by the PWM Frequency Register.

If the Fan Setting is set at a value that is higher than 2x the PWM Frequency Register settings, the PWM output will be at 100% duty cycle.

Table A.1 shows the effective resolution, duty cycle, and frequency as the PWM Frequency Register setting is changed.

EQUATION 1:

$$EFFECTIVE\_DUTY\_CYCLE = \left(\frac{FAN\_SETTING}{PWM\_F \times 2}\right) \times 100\%$$

Where:

PWM_F   =   The setting of the PWM Frequency Register (4Dh)

EQUATION 2:

$$EFFECTIVE\_RESOLUTION = \frac{100\%}{PWM\_F \times 2}$$

Where:

PWM_F   =   The setting of the PWM Frequency Register (4Dh)

EQUATION 3:

(A)

$$PWM\_FREQUENCY = \frac{360k}{2 \times PWM\_F}$$

(B)

$$PWM\_FREQUENCY = \frac{1.4k}{2 \times PWM\_F}$$

Where:

PWM_F   =   The setting of the PWM Frequency register (4Dh)

The setting of the PWM Frequency Divide Register (4Eh)

CLK_SEL = '0'

CLK_SEL = '1'

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TABLE 1: FAN EFFECTIVE DUTY CYCLE RESOLUTION AND FREQUENCY

PWM_F [4:0] Setting	Effective Resolution (%)	Effective Duty Cycle (at 75% FAN_SETTING)	EFFECTIVE Duty Cycle (at 50% FAN_SETTING)	FAN_SETTING to Get 75% Duty Cycle	PWM FREQUENCY at 360 kHz Base Frequency (kHz)	PWM FREQUENCY at 1.4 kHz Base Frequency (Hz)
00h	Setting 00h is mapped to setting 01h					
01h	50.00%	100%	100%	01h (50%)	180.0	704.2
02h	25.00%	100%	100%	03h (75%)	90.0	350.0
03h	16.67%	100%	100%	04h (66.7%)	60.0	233.3
04h	12.50%	100%	100%	06h (75%)	45.0	175.0
05h	10.00%	100%	100%	07h (70%)	36.0	140.0
06h	8.33%	100%	100%	09h (75%)	30.0	116.7
07h	7.14%	100%	100%	0Ah (71.4%)	25.7	100.0
08h	6.25%	100%	100%	0Ch (75%)	22.5	87.5
09h	5.56%	100%	100%	0Dh (72.5)	20.0	77.8
0Ah	5.00%	100%	100%	0Fh (75%)	18.0	70.0
0Bh	4.54%	100%	100%	11h (77.3%)	16.4	63.7
0Ch	4.17%	100%	100%	12h (75%)	15.0	58.3
0Dh	3.84%	100%	100%	14h (76.9%)	13.8	53.8
0Eh	3.57%	100%	100%	15h (75%)	12.8	50.0
0Fh	3.33%	100%	100%	16h (73.3%)	12.0	46.7
10h	3.13%	100%	100%	18h (75.0%)	11.25	44.0
11h	2.94%	100%	94.1%	19h (73.5%)	10.68	41.4
12h	2.78%	100%	88.9%	1Bh (75.0%)	10.00	39.1
13h	2.63%	100%	84.2%	1Ch (73.7%)	9.47	37.1
14h	2.50%	100%	80.0%	1Eh (75.0%)	9.00	35.2
15h	2.38%	100%	76.2%	1Fh (73.8%)	8.57	33.5
16h	2.27%	100%	72.7%	21h (75.0%)	8.18	32.0
17h	2.17%	100%	69.7%	22h (73.9%)	7.83	30.6
18h	2.08%	100%	66.7%	24h (75.0%)	7.50	29.3
19h	2.00%	96%	64.0%	25h (74.0%)	7.20	28.2
1Ah	1.92%	92.3%	61.5%	27h (75.0%)	6.92	27.1
1Bh	1.85%	88.9%	59.3%	28h (74.1%)	6.67	26.1
1Ch	1.79%	85.7%	57.1%	2Ah (75.0%)	6.43	25.1

TABLE 1: FAN EFFECTIVE DUTY CYCLE RESOLUTION AND FREQUENCY (CONTINUED)

PWM_F [4:0] Setting	Effective Resolution (%)	Effective Duty Cycle (at 75% FAN_SETTING)	EFFECTIVE Duty Cycle (at 50% FAN_SETTING)	FAN_SETTING to Get 75% Duty Cycle	PWM FREQUENCY at 360 kHz Base Frequency (kHz)	PWM FREQUENCY at 1.4 kHz Base Frequency (Hz)
1Dh	1.72%	82.8%	55.2%	2Bh (74.1%)	6.21	24.3
1Eh	1.67%	80.0%	53.3%	2Dh (75.0%)	6.00	23.5
1Fh	1.61%	77.4%	51.6%	2Eh (74.2%)	5.81	22.7

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APPENDIX C: TACH REFERENCE TABLE

TABLE 2: EXAMPLE TACH DECODE 10K RPM TO 1K RPM

DEC	HEX	RPM	DEC	HEX	RPM	DEC	HEX	RPM	DEC	HEX	RPM	DEC	HEX	RPM	DEC	HEX	RPM
512	200h	10547	1280	500h	4219	2048	800h	2637	2816	B00h	1918	3584	E00h	1507	4352	1100h	1241
528	210h	10227	1296	510h	4167	2064	810h	2616	2832	B10h	1907	3600	E10h	1500	4368	1110h	1236
544	220h	9926	1312	520h	4116	2080	820h	2596	2848	B20h	1896	3616	E20h	1493	4384	1120h	1232
560	230h	9643	1328	530h	4066	2096	830h	2576	2864	B30h	1885	3632	E30h	1487	4400	1130h	1227
576	240h	9375	1344	540h	4018	2112	840h	2557	2880	B40h	1875	3648	E40h	1480	4416	1140h	1223
592	250h	9122	1360	550h	3971	2128	850h	2538	2896	B50h	1865	3664	E50h	1474	4432	1150h	1218
608	260h	8882	1376	560h	3924	2144	860h	2519	2912	B60h	1854	3680	E60h	1467	4448	1160h	1214
624	270h	8654	1392	570h	3879	2160	870h	2500	2928	B70h	1844	3696	E70h	1461	4464	1170h	1210
640	280h	8438	1408	580h	3835	2176	880h	2482	2944	B80h	1834	3712	E80h	1455	4480	1180h	1205
656	290h	8232	1424	590h	3792	2192	890h	2464	2960	B90h	1824	3728	E90h	1448	4496	1190h	1201
672	2A0h	8036	1440	5A0h	3750	2208	8A0h	2446	2976	BA0h	1815	3744	EA0h	1442	4512	11A0h	1197
688	2B0h	7849	1456	5B0h	3709	2224	8B0h	2428	2992	BB0h	1805	3760	EB0h	1436	4528	11B0h	1193
704	2C0h	7670	1472	5C0h	3668	2240	8C0h	2411	3008	BC0h	1795	3776	EC0h	1430	4544	11C0h	1188
720	2D0h	7500	1488	5D0h	3629	2256	8D0h	2394	3024	BD0h	1786	3792	ED0h	1424	4560	11D0h	1184
736	2E0h	7337	1504	5E0h	3590	2272	8E0h	2377	3040	BE0h	1776	3808	EE0h	1418	4576	11E0h	1180
752	2F0h	7181	1520	5F0h	3553	2288	8F0h	2360	3056	BF0h	1767	3824	EF0h	1412	4592	11F0h	1176
768	300h	7031	1536	600h	3516	2304	900h	2344	3072	C00h	1758	3840	F00h	1406	4608	1200h	1172
784	310h	6888	1552	610h	3479	2320	910h	2328	3088	C10h	1749	3856	F10h	1400	4624	1210h	1168
800	320h	6750	1568	620h	3444	2336	920h	2312	3104	C20h	1740	3872	F20h	1395	4640	1220h	1164
816	330h	6618	1584	630h	3409	2352	930h	2296	3120	C30h	1731	3888	F30h	1389	4656	1230h	1160
832	340h	6490	1600	640h	3375	2368	940h	2280	3136	C40h	1722	3904	F40h	1383	4672	1240h	1156
848	350h	6368	1616	650h	3342	2384	950h	2265	3152	C50h	1713	3920	F50h	1378	4688	1250h	1152
864	360h	6250	1632	660h	3309	2400	960h	2250	3168	C60h	1705	3936	F60h	1372	4704	1260h	1148
880	370h	6136	1648	670h	3277	2416	970h	2235	3184	C70h	1696	3952	F70h	1366	4720	1270h	1144
896	380h	6027	1664	680h	3245	2432	980h	2220	3200	C80h	1688	3968	F80h	1361	4736	1280h	1140
912	390h	5921	1680	690h	3214	2448	990h	2206	3216	C90h	1679	3984	F90h	1355	4752	1290h	1136
928	3A0h	5819	1696	6A0h	3184	2464	9A0h	2192	3232	CA0h	1671	4000	FA0h	1350	4768	12A0h	1133
944	3B0h	5720	1712	6B0h	3154	2480	9B0h	2177	3248	CB0h	1663	4016	FB0h	1345	4784	12B0h	1129
960	3C0h	5625	1728	6C0h	3125	2496	9C0h	2163	3264	CC0h	1654	4032	FC0h	1339	4800	12C0h	1125

TABLE 2: **EXAMPLE TACH DECODE 10K RPM TO 1K RPM (CONTINUED)**

DEC	HEX	RPM	DEC	HEX	RPM	DEC	HEX	RPM	DEC	HEX	RPM	DEC	HEX	RPM	DEC	HEX	RPM
976	3D0h	5533	1744	6D0h	3096	2512	9D0h	2150	3280	CD0h	1646	4048	FD0h	1334	4816	12D0h	1121
992	3E0h	5444	1760	6E0h	3068	2528	9E0h	2136	3296	CE0h	1638	4064	FE0h	1329	4832	12E0h	1118
1008	3F0h	5357	1776	6F0h	3041	2544	9F0h	2123	3312	CF0h	1630	4080	FF0h	1324	4848	12F0h	1114
1024	400h	5273	1792	700h	3013	2560	A00h	2109	3328	D00h	1623	4096	1000h	1318	4864	1300h	1110
1040	410h	5192	1808	710h	2987	2576	A10h	2096	3344	D10h	1615	4112	1010h	1313	4880	1310h	1107
1056	420h	5114	1824	720h	2961	2592	A20h	2083	3360	D20h	1607	4128	1020h	1308	4896	1320h	1103
1072	430h	5037	1840	730h	2935	2608	A30h	2071	3376	D30h	1600	4144	1030h	1303	4912	1330h	1099
1088	440h	4963	1856	740h	2909	2624	A40h	2058	3392	D40h	1592	4160	1040h	1298	4928	1340h	1096
1104	450h	4891	1872	750h	2885	2640	A50h	2045	3408	D50h	1585	4176	1050h	1293	4944	1350h	1092
1120	460h	4821	1888	760h	2860	2656	A60h	2033	3424	D60h	1577	4192	1060h	1288	4960	1360h	1089
1136	470h	4754	1904	770h	2836	2672	A70h	2021	3440	D70h	1570	4208	1070h	1283	4976	1370h	1085
1152	480h	4688	1920	780h	2813	2688	A80h	2009	3456	D80h	1563	4224	1080h	1278	4992	1380h	1082
1168	490h	4623	1936	790h	2789	2704	A90h	1997	3472	D90h	1555	4240	1090h	1274	5008	1390h	1078
1184	4A0h	4561	1952	7A0h	2766	2720	AA0h	1985	3488	DA0h	1548	4256	10A0h	1269	5024	13A0h	1075
1200	4B0h	4500	1968	7B0h	2744	2736	AB0h	1974	3504	DB0h	1541	4272	10B0h	1264	5040	13B0h	1071
1216	4C0h	4441	1984	7C0h	2722	2752	AC0h	1962	3520	DC0h	1534	4288	10C0h	1259	5056	13C0h	1068
1232	4D0h	4383	2000	7D0h	2700	2768	AD0h	1951	3536	DD0h	1527	4304	10D0h	1255	5072	13D0h	1065
1248	4E0h	4327	2016	7E0h	2679	2784	AE0h	1940	3552	DE0h	1520	4320	10E0h	1250	5088	10E0h	1061
1264	4F0h	4272	2032	7F0h	2657	2800	AF0h	1929	3568	DF0h	1513	4336	10F0h	1245	5104	13F0h	1058

EMC2101

EMC2101

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	-XXXX-	XX
Device	Package	Tape and Reel

Device:	EMC2101:	SMBus 2.0 compliant, integrated fan control solution
	EMC2101-R:	SMBus 2.0 compliant, integrated fan control solution with EEPROM capability
Package:	ACZL=	8-Lead Plastic Micro Small Outline Package, 3x3 mm Body (MSOP)
Tape and Reel:	TR =	Tape and Reel

Examples:

a) EMC2101-ACZL-TR: SMBus 2.0 compliant, 8L-MSOP package, Tape and Reel

b) EMC2101-R-ACZL-TR: SMBus 2.0 compliant with EEPROM compatibility, 8L-MSOP package, Tape and Reel

Note 1:   Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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