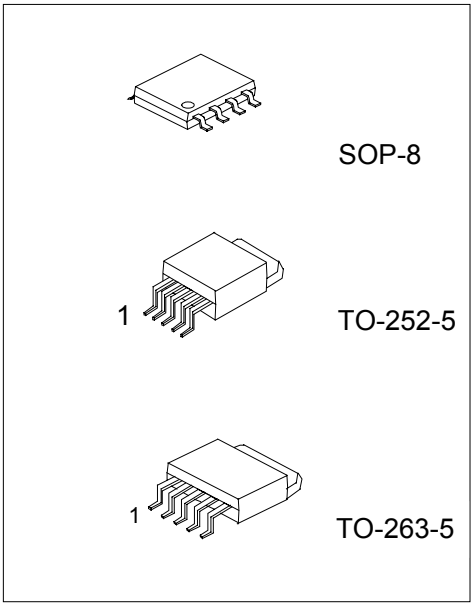
UR5515

CMOS IC

1.5A/3A BUS TERMINATION REGULATOR



*Pb-free plating product number: UR5515L

■ DESCRIPTION

The UTC **UR5515** is a linear bus termination regulator and designed to convert voltage supplies ranging from 1.6V~6.0V into a desired output voltage, which adjusted by two external voltage divider resistors. The device can both source and sink up to 1.5A/3A of current while regulating an output voltage to within 2% (DDR-I) and 3% (DDR-II) or less.

The UTC **UR5515** is capable of use in conjunction with series termination resistors to provide an excellent voltage source for active termination schemes of high speed transmission lines as those seen in high speed memory buses and distributed backplane designs.

The voltage output of the regulator can be used as a termination voltage for DDR SDRAM.

■ FEATURES

* Support Both DDR-I (1.25 V_{TT}) and DDR-II (0.9 V_{TT}) Requirements
* Capable of Sourcing and Sinking Current 1.5A/3A
* Current-limiting Protection and Thermal Shutdown Protection
* Integrated Power MOSFETs
* Generates Termination Voltages for SSTL-2
* High Accuracy Output Voltage at Full-Load
* Adjustable output voltage by External Resistors
* Minimum External Components
* Shutdown for Standby or Suspend Mode Operation with High-impedance Output.

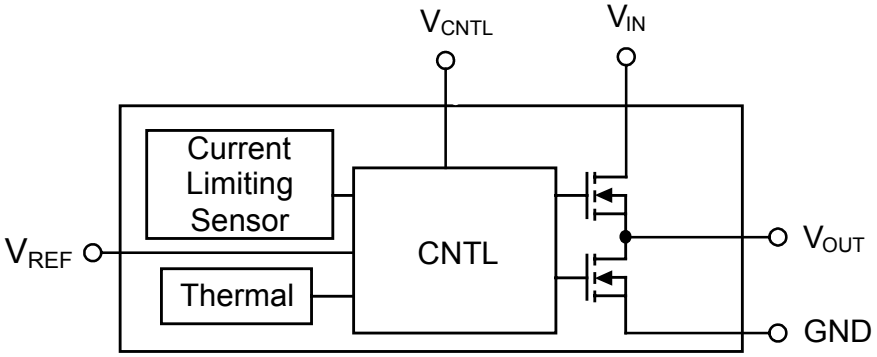
■ ORDERING INFORMATION

Order Number		Package	Packing
Normal	Lead Free Plating		
UR5515-S08-R	UR5515L-S08-R	SOP-8	Tape Reel
UR5515-S08-T	UR5515L-S08-T	SOP-8	Tube
UR5515-TN5-R	UR5515L-TN5-R	TO-252-5	Tape Reel
UR5515-TN5-T	UR5515L-TN5-T	TO-252-5	Tube
UR5515-TQ5-R	UR5515L-TQ5-R	TO-263-5	Tape Reel
UR5515-TQ5-T	UR5515L-TQ5-T	TO-263-5	Tube

■ PIN DESCRIPTION

PIN NO.		PIN NAME	DESCRIPTION
SOP-8	TO-252-5/TO-263-5		
1	1	V_{IN}	Input Voltage
2	2	GND	Ground
5,6,7,8	3	V_{CNTL}	Gate Drive Voltage
3	4	V_{REF}	Reference Voltage Input and Chip Enable
4	5	V_{OUT}	Output Voltage

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNIT
Input Voltage	V_{IN}	7	V
Power Dissipation	P_D	Internally Limited	W
Junction Temperature	T_J	125	°C
Storage Temperature Range	T_{STG}	-40 ~ 150	°C

Note:1.Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2.The device is guaranteed to meet performance specification within 0℃~70℃ operating temperature range and assured by design from –20℃~85℃.

■ ELECTRICAL CHARACTERISTICS

(Ta = 25°C, unless otherwise specified: V_{IN} = 2.5V, V_{CNTL}= 3.3V, V_{REF} = 1.25V, C_{OUT}=10μF(Ceramic).)

PARAMETER		SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Input Voltage Range(Note 1)		V_{IN}	No Load,(Note 2)	DDR-I	1.6	2.5		V
				DDR-II		1.8		
		V_{CNTL}		DDR-I		3.3	6	
				DDR-II		3.3	6	
Output Offset Voltage		V_{OS}	I_{OUT}=0A, Fig. 1 (Note 3)		-20	0	20	mV
Operating Current of V_{CNTL}		I_{CNTL}	No Load			6.5	10	mA
Load Regulation		$\lvert\triangle V_{LOAD}\rvert$	I_L: 0~1.5A, Fig. 1	DDR-I		0.8	2	%
				DDR-II		1.2	3	
			I_L: 0~-1.5A, Fig. 1	DDR-I		0.8	2	
				DDR-II		1.2	3	
Current In Shutdown Mode		I_{SHDN}	V_{REF}<0.2V, R_L=180Ω, Fig. 2			50	90	μA
Short Circuit Protection								
Current Limit	UR5515	I_{LIMIT}	Fig 3, 4		2.1			A
	UR5515A		Fig 3, 4		3.0			
Over Temperature Protection								
Thermal Shutdown Temperature		T_{SD}	3.3V≤V_{CNTL}≤5V		125	150		°C
Thermal Shutdown Hysteresis						50		°C
Shutdown Function								
Shutdown Threshold Voltage		V_{THD}	Fig 5		0.2		0.8	V

Note 1. For safely operate your system, the 3.3V rail have to be tied to V_{CNTL} rather than 5V rail
2. Keep V_{CNTL}≥V_{IN} on operation power on and power off sequences.
3. V_{OS} offset is the voltage measurement defined as V_{OUT} subtracted from V_{REF}.

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Thermal Resistance Junction-Case	SOP-8	θ_{JC}	35	°C/W
	TO-252-5		8	
	TO-263-5		4	

■ TEST CIRCUITS

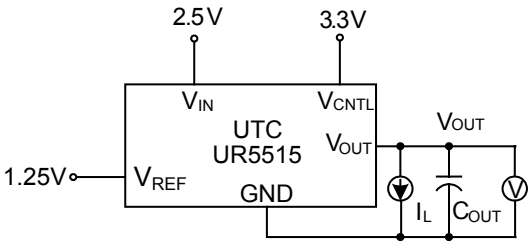


Fig1. Output Voltage Tolerance, △ V_{OUT}

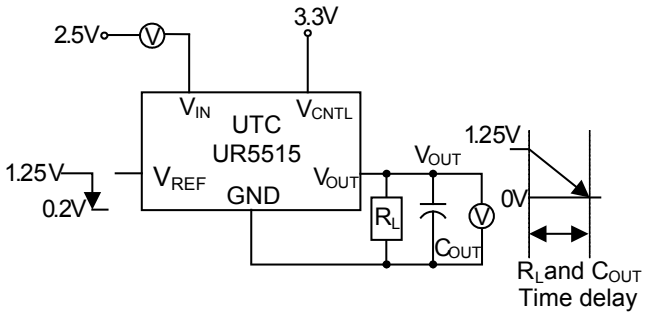


Fig2. Current in Shutdown Mode, I_{SHCLN}

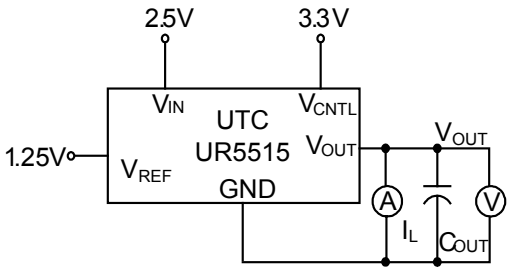


Fig3. Current Limit for HIgh Side, I_{CLHIGH}

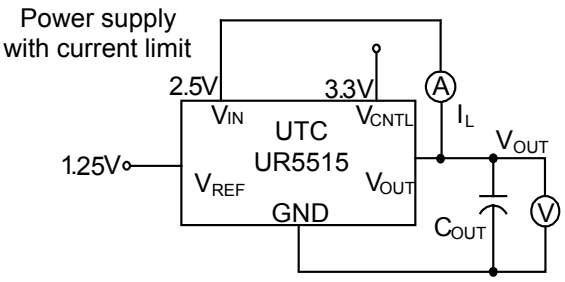


Fig4. Current Limit for Low Side, I_{CLLOW}

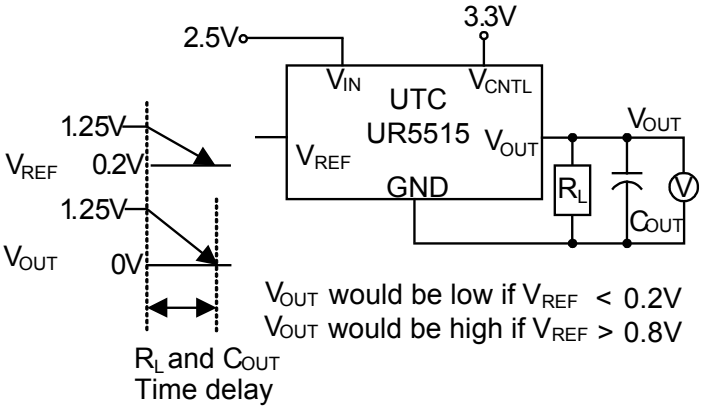
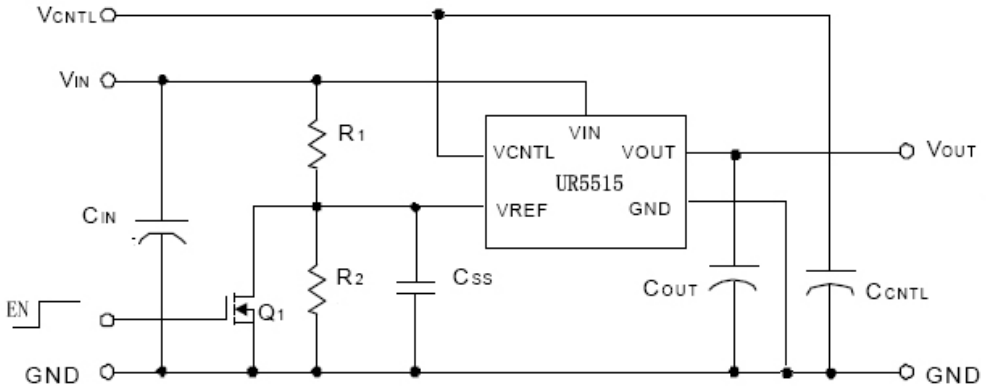


Fig5. V_{REF} Pin Shutdown Threshold Voltage

■ TYPICAL APPLICATION CIRCUIT



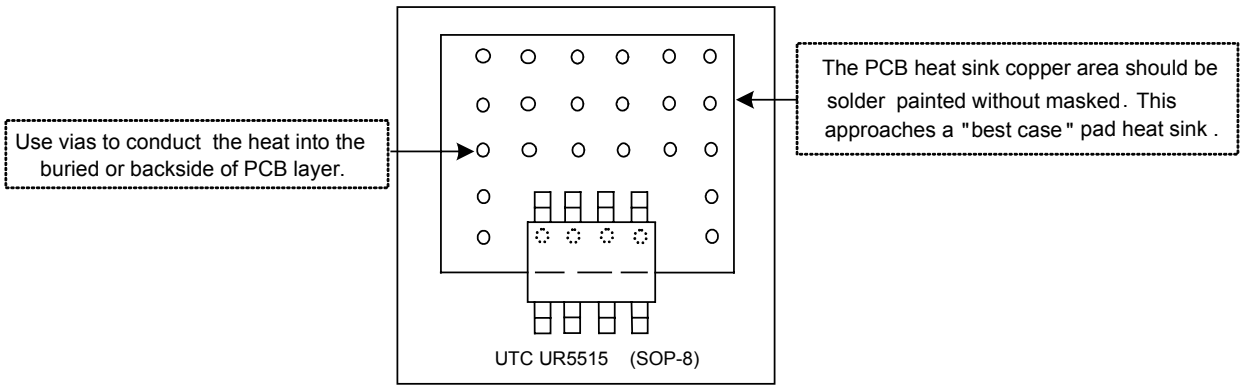
R_1= R_2= 100KΩ

$C_{OUT(min)}$=10μF(Ceramic) + 1000μF under the worst case testing condition

C_{SS}=1μF, C_{IN} = 40μF(low ESR), C_{CNTL}= 47μF

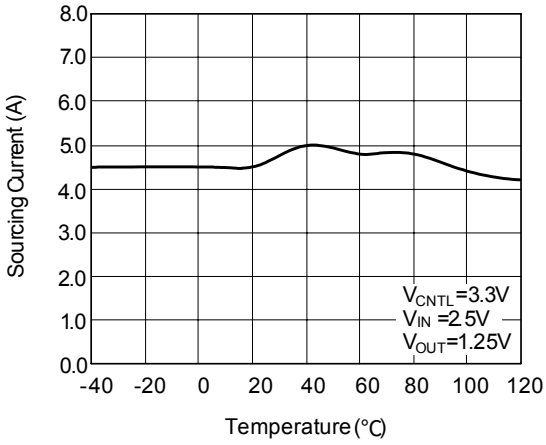
■ APPLICATIONS INFORMATION

Please note the point of thermal shutdown will be degraded by around 20°Cwhile V_{CNTL} equal to 5V compared with 3.3V. It is highly recommended that to use the 3.3V rail acted as the V_{CNTL} in SOP-8 package. Nevertheless, this small footprint of PCB for plastic SOP-8 package is not enough to dissipate effectively the heat generated when operating at high current levels. In order to control die operating temperatures, the PCB layout should allow for maximum possible copper area at the four V_{CNTL} pins. Besides, an appropriate power plane heat sink must be used to prevent overstepping maximum junction temperature. The recommended SMT is as below.

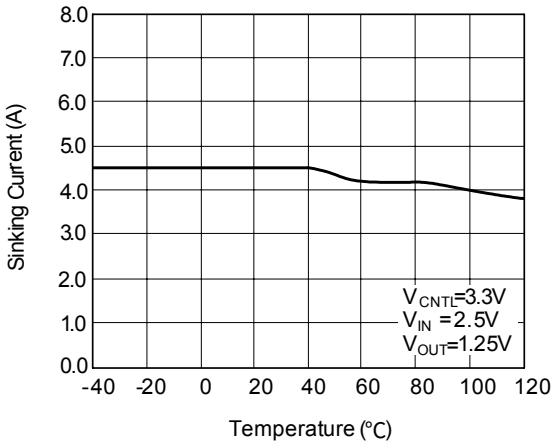


■ TYPICAL CHARACTERISTICS

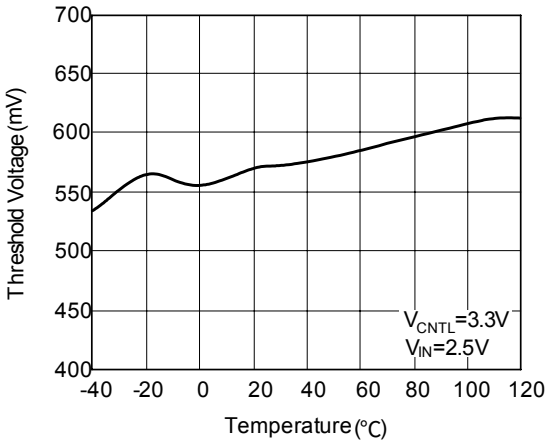
Sourcing Current(Peak) vs. Temperature



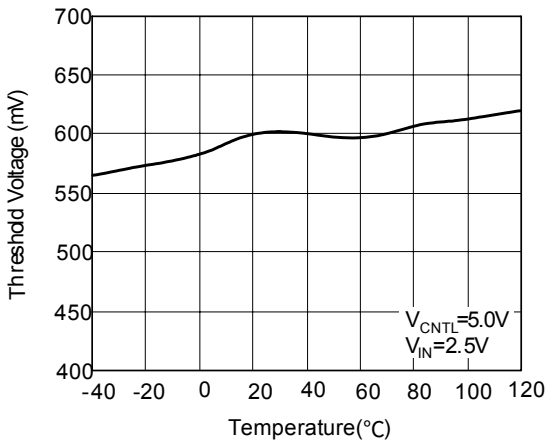
Sinking Current(Peak) vs. Temperature



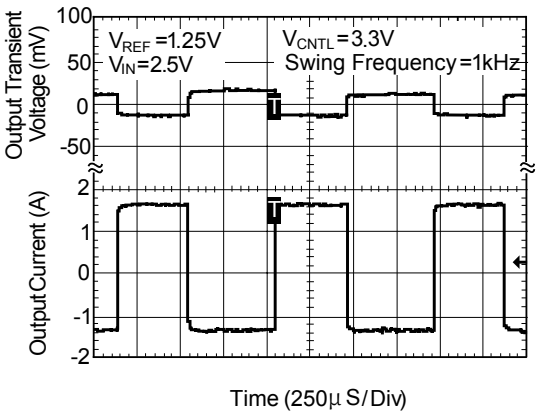
Turn-On Threshold vs. Temperature



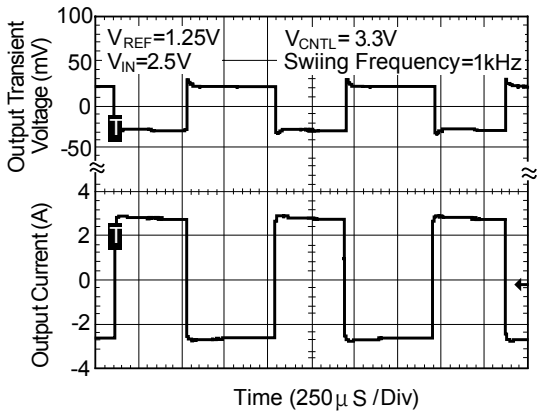
Turn-On Threshold vs. Temperature



$1.25V_{TT}$ @1.5A Transient Response

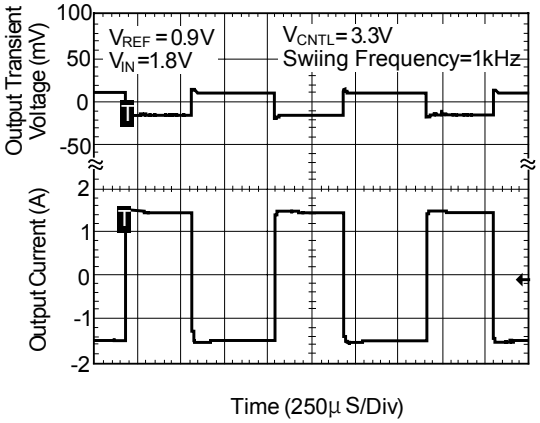


$1.25V_{TT}$ @3A Transient Response

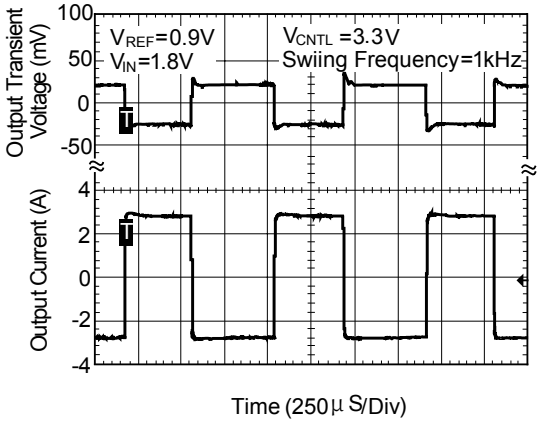


■ TYPICAL CHARACTERISTICS (cont.)

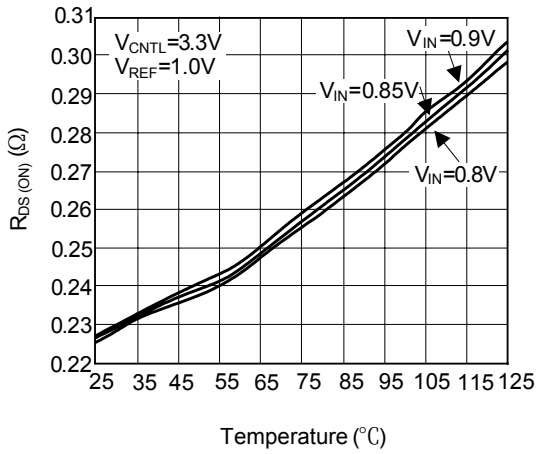
0.9V_{TT} @1.5A Transient Response



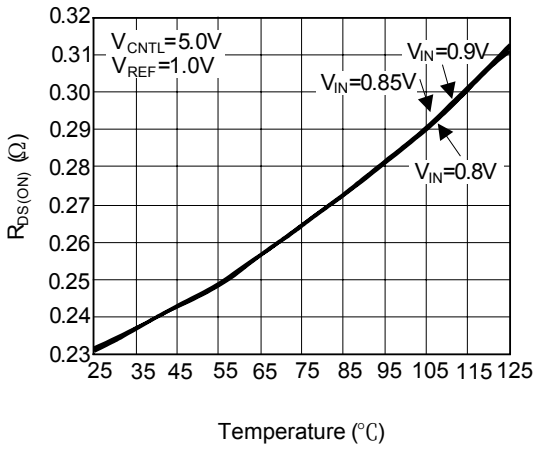
0.9V_{TT} @3A Transient Response



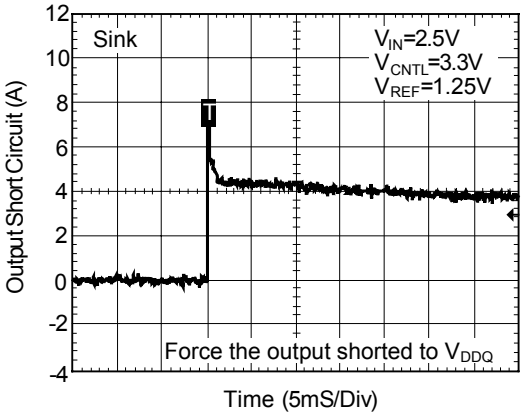
Temperature vs. $R_{DS(ON)}$



Temperature vs. $R_{DS(ON)}$



Output Short-Circuit Protection



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