SONY

CXL1517M/1518M

CMOS-CCD Signal Processor

Description

The CXL1517M/1518M are CMOS-CCD signal processors developed for CCD camera complementary color filter array processing system.

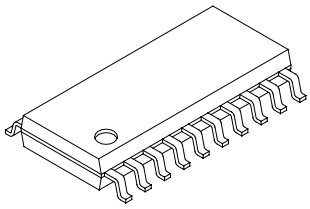
CXL1517M

452.5-bit × 2, 453.5-bit 1H CCD delay line

CXL1518M

300.5-bit × 2, 301.5-bit 1H CCD delay line

20 pin SOP (Plastic)



Structure

CMOS-CCD

Features

- Single 5V power supply
- Low power consumption (Typ.)
  - CXL1517M 120mW
  - CXL1518M 75mW
- Built-in peripheral circuits
- Built-in CDS (Correlated Double Sampling) circuit

Functions

- Clock driver
- Autobias circuit (Center and black)
- Pedestal clamp circuit
- CDS circuit
- Overflow prevention circuit

Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{DD}	6	V
• Operating temperature	Topr	–10 to +65	°C
• Storage temperature	Tstg	–55 to +150	°C
• Allowable power dissipation	P_D	500	mW

Recommended Operating Voltage Range (Ta = 25°C)

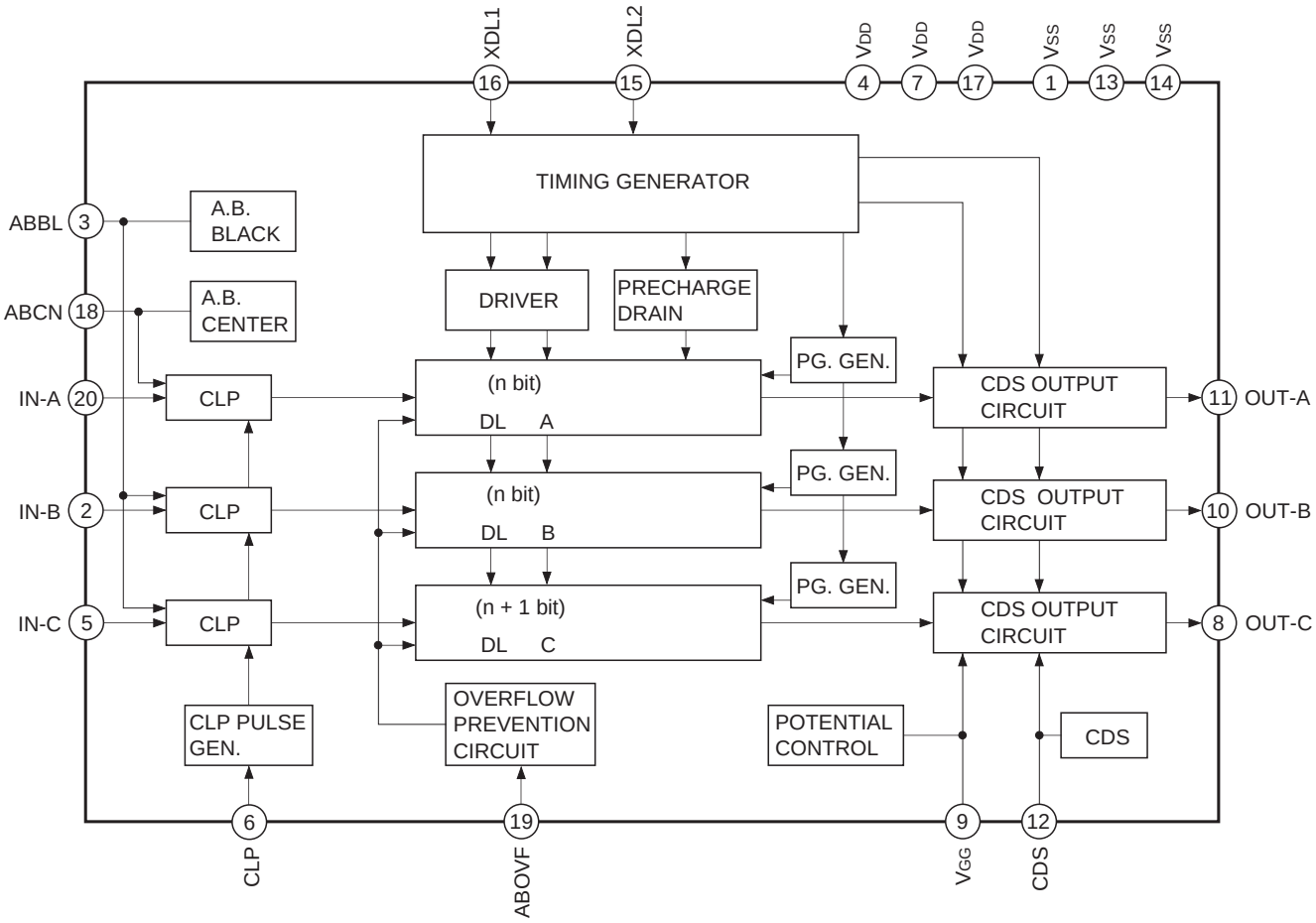
Supply voltage	V_{DD}	4.6 to 5.25	V

Item		Symbol	Min.	Typ.	Max.	Unit	Remarks
Clock voltage Low		V_L	V_{SS}		$0.3 \times V_{DD}$	V	
Clock voltage High		V_H	$0.7 \times V_{DD}$		V_{DD}	V	
Clock frequency	CXL1517M	f_{CL}		7.16		MHz	NTSC: $455f_H$ CCIR: $454f_H$
	CXL1518M	f_{CL}		4.77		MHz	NTSC: $910f_H/3$ CCIR: $908f_H/3$

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E91777A78-PS

Block Diagram and Pin Configuration (Top View)





Pin Description

Pin No.	Symbol	I/O	Description	Comment
1	V_{SS}	—	GND	Analog
2	IN-B	I	Signal input B channel (Y)	
3	ABBL	O	Autobias DC output for Y signal	Black level bias
4	V_{DD}	—	Power supply	Analog
5	IN-C	I	Signal input C channel (Y)	Black level bias at no clamp > 100k
6	CLP	I	Clamp pulse input	> 100k
7	V_{DD}	—	Power supply	Output circuit
8	OUT-C	O	Signal output C channel	
9	V_{GG}	O	Output circuit bias DC output	
10	OUT-B	O	Signal output B channel	
11	OUT-A	O	Signal output A channel	
12	CDS	O	DC output for CDS	
13	V_{SS}	—	GND	Output circuit
14	V_{SS}	—	GND	Timing
15	XDL2	I	Clock pulse input 2	> 100k
16	XDL1	I	Clock pulse input 1	> 100k
17	V_{DD}	—	Power supply	Timing
18	ABCN	O	Autobias DC output for C signal	Center level bias
19	ABOVF	O	Autobias DC output for overflow prevention circuit	
20	IN-A	I	Signal input A channel (C)	Center level bias at no clamp > 100k

Electrical Characteristics

Ta = 25°C, V_{DD} = 5.0V, V_{SS} = 0V f_{CL} = 7.16MHz (CXL1517M) f_{CL} = 4.77MHz (CXL1518M)

Item		Symbol	Test point	SW conditions				Bias conditions	Conditions	Ratings			Unit
				SW1	SW2	SW3	SW4 to 6	E1		Min.	Typ.	Max.	
Autobias center level		ABCN	V_1	a	b	a	a			4.2	4.6	4.8	V
Autobias black level		ABBL	V_2	a	b	a	a			3.9	4.3	4.5	V
Overflow prevention circuit Autobias level		ABOVF	V_3	a	b	a	a			2.6	3.0	3.3	V
CDS source level		CDS	V_4	a	a	a	a			1.2	2.3	3.5	V
Output circuit bias level		V_{GG}	V_5	a	a	a	a			0.3	0.8	3.0	V
Current * supply	CXL1517M	I_{DD}	A_1	b	a	a	a	V_1		—	24	35	mA
	CXL1518M									—	15	25	
Insertion gain		IG	V_6	b	b	a to c	a	A → V_1 B, C → V_2 + 0.25V	20 log (Output amplitude (mVp-p) / Input amplitude (SIN 100kHz, 100mVp-p))	–4.5	–3.5	—	dB
Frequency * response	CXL1517M	f_G	V_6	b ↕ c	b	a to c	a	↓	20 log (Output amplitude (SIN 1MHz, 100mVp-p) / Output amplitude (SIN 100kHz, 100mVp-p))	–1.5	–0.4	—	dB
	CXL1518M									–1.8	–0.8	—	
Linearity		Lin.	V_6	b	b	a to c	a		Note 1)	0	5	12	%
The insertion gain difference between channels		ΔG							Note 2)	0	5	12	%
Linearity difference between channels	Bch → Cch	ΔL_{BC}							Note 3)	0	1	5	%
Cross-talk between channels		CRT	V_6	b	b	a to c	a ↕ b	A → V_1 B, C → V_2 + 0.25V	Note 4)	0	1	3	%

* Standard values are different between CXL1517M and CXL1518M.

Notes)

1) Linearity testing
For A channel, set input bias to ABCN – 0.2V first, and then set it to ABCN and ABCN + 0.2V. Then input a sine wave of 100kHz and 100mVp-p, and compare the three output amplitudes. For B channel and C channel, set input bias to ABBL + 0.45V first, and then set it to ABBL + 0.25V and ABBL + 0.05V. Then input a sine wave of 100kHz and 100mVp-p, and compare the three output amplitudes. The maximum output amplitude for the respective A, B and C channels is taken as Sout max and the minimum output amplitude as Sout min. The linearity of the respective channels is defined as:

$$\text{Lin.} = \frac{\text{Sout max} - \text{Sout min}}{\text{Sout max} + \text{Sout min}} \times 200\ [\%]$$

2) Calculation of insertion gain difference
As the maximum insertion gain among A, B and C channels is taken as Gmax and the minimum as Gmin, the insertion gain difference between channels ΔG as:

$$\Delta G = \left| 1 - 10 \left(\frac{\text{Gmax} - \text{Gmin}}{20} \right) \right| \times 100\ [\%]$$

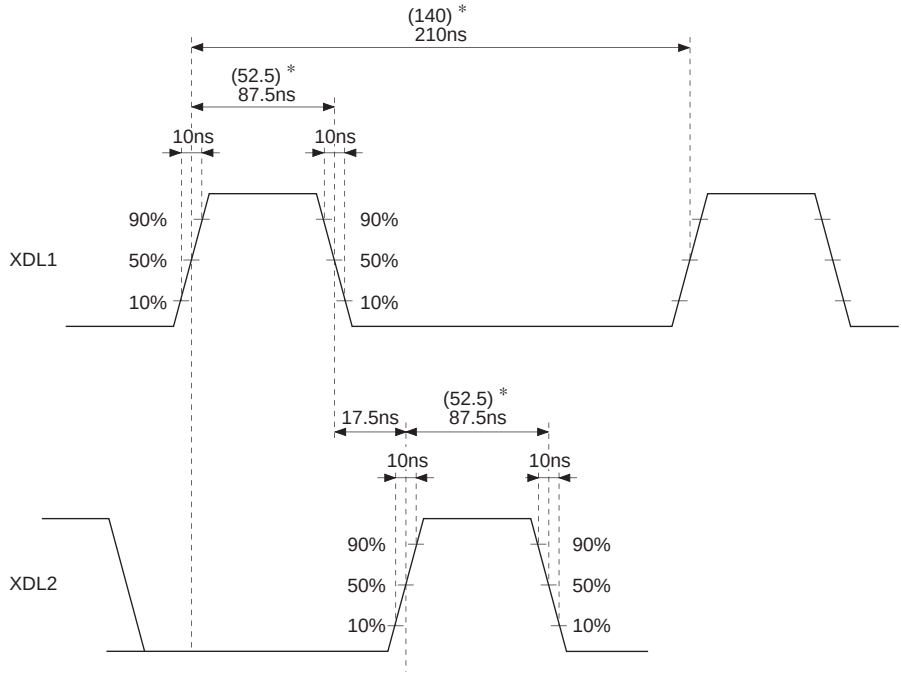
3) Calculation of linearity difference
Define B channel linearity as L_B and C channel linearily as L_C we obtain the difference ΔL_{BC} as:

$$\Delta L_{BC} = | L_B - L_C |\ [\%]$$

4) Cross-talk calculation
CRTa : The cross-talk value of A channel when B and C channels are input
$OUT_{A\text{-}a}$: The output value of A channel when A channel is input
SW3-a, SW4-a, SW5, 6-b
$OUT_{A\text{-}bc}$: The output value of A channel when B and C channels are input
(Cross-talk component)
SW3-a, SW4-b, SW5, 6-a

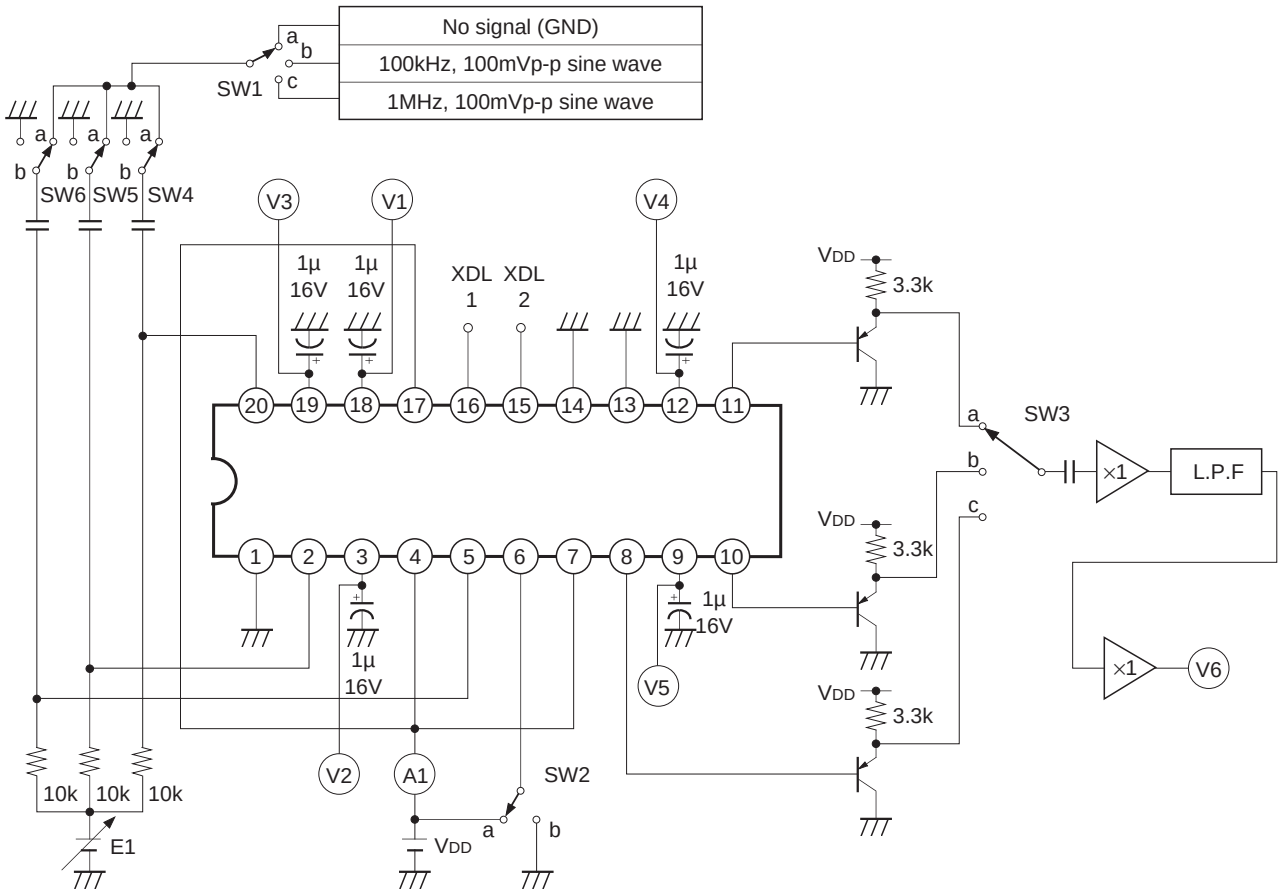
$$\text{CRTa} = \frac{OUT_{A\text{-}bc}}{OUT_{A\text{-}a}} \times 100\ [\%]$$

Clock Waveform Timing

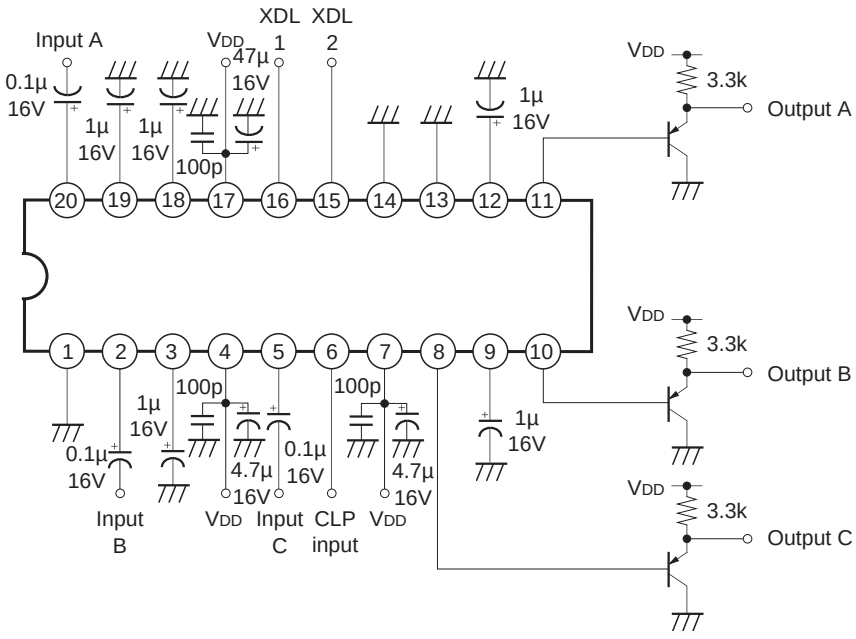


* The value in brackets is for CXL1517M.

Electrical Characteristics Test Circuit



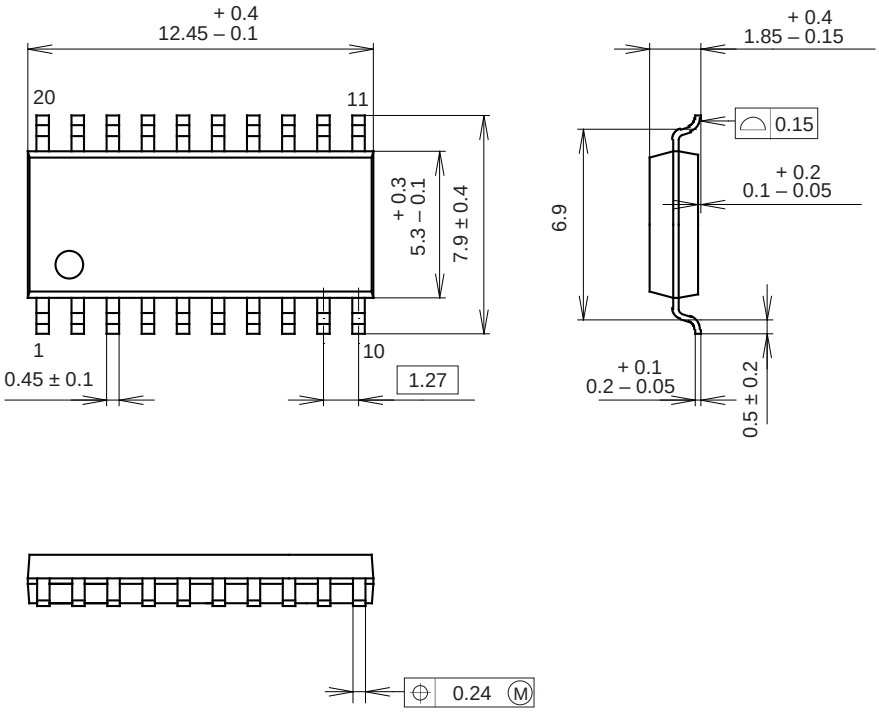
Application Circuit



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Package Outline Unit: mm

20PIN SOP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	SOP-20P-L01
EIAJ CODE	SOP020-P-0300
JEDEC CODE	

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.3g