ISL6115, ISL6116, ISL6117, ISL6120

Power Distribution Controllers

FN9100
Rev 8.00
December 3, 2015

This family of fully featured hot swap power controllers targets applications in the +2.5V to +12V range. The ISL6115 is for +12V control, the ISL6116 for +5V, the ISL6117 for +3.3V and the ISL6120 for +2.5V control applications. Each has a hard wired undervoltage (UV) monitoring and reporting threshold level approximately 80% of the aforementioned voltage.

The ISL6115 has an integrated charge pump allowing control of up to +16V rails using an external N-Channel MOSFET whereas the other devices utilize the +12V bias voltage to fully enhance the N-Channel pass FET. All ICs feature programmable overcurrent (OC) detection, current regulation (CR) with time delay to latch-off and soft-start.

The current regulation level is set by 2 external resistors; R_{ISET} sets the CR Vth and the other is a low ohmic sense element across, which the CR Vth is developed. The CR duration is set by an external capacitor on the CTIM pin, which is charged with a 20µA current once the CR Vth level is reached. If the voltage on the CTIM capacitor reaches 1.9V the IC then quickly pulls down the GATE output latching off the pass FET.

This family although designed for high side switch control the ISL6116, ISL6117, ISL6120 can also be used in a low side configuration for control of much higher voltage potentials.

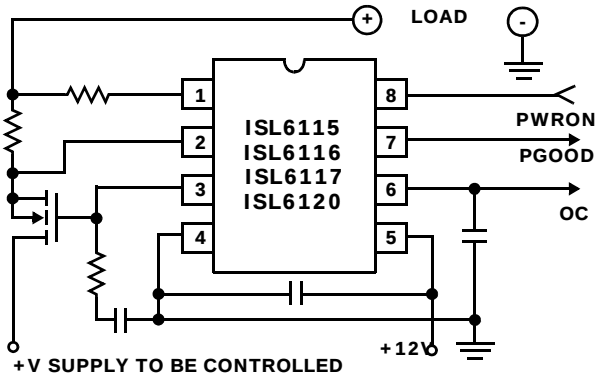
Features

- HOT SWAP Single Power Distribution Control (ISL6115 for +12V, ISL6116 for +5V, ISL6117 for +3.3V and ISL6120 for +2.5V)
- Overcurrent Fault Isolation
- Programmable Current Regulation Level
- Programmable Current Regulation Time to Latch-Off
- Rail-to-Rail Common Mode Input Voltage Range (ISL6115)
- Internal Charge Pump Allows the Use of N-Channel MOSFET for +12V Control (ISL6115)
- Undervoltage and Overcurrent Latch Indicators
- Adjustable Turn-On Ramp
- Protection During Turn-On
- Two Levels of Overcurrent Detection Provide Fast Response to Varying Fault Conditions
- 1µs Response Time to Dead Short
- Pb-Free Available (RoHS Compliant)

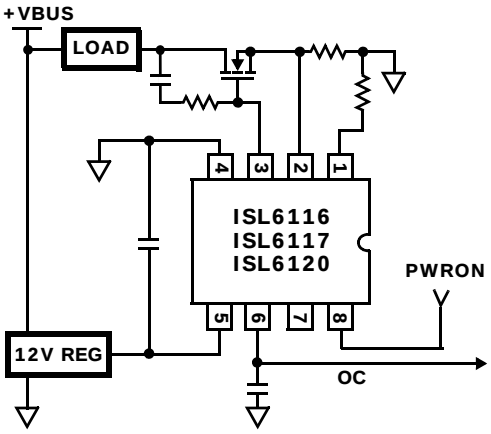
Applications

- Power Distribution Control
- Hot Plug Components and Circuit

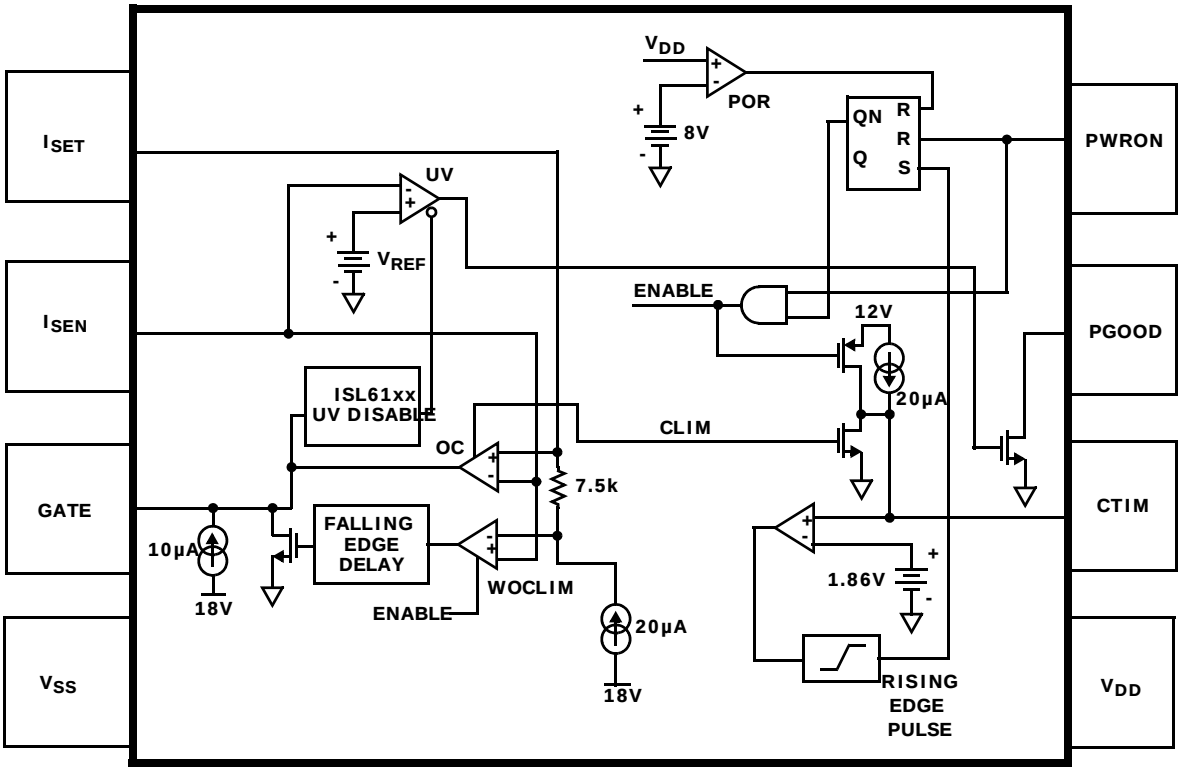
Application Circuits- High Side Controller



Application Two - Low Side Controller



Simplified Block Diagram



Ordering Information

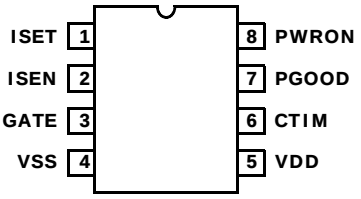
PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL6115CBZA (Notes 1, 2)	6115 CBZ	0 to +85	8 Ld SOIC (Pb-free)	M8.15
ISL6116CBZA (Notes 1, 2) **No longer available or supported**	6116 CBZ	0 to +85	8 Ld SOIC (Pb-free)	M8.15
ISL6117CBZA (Notes 1, 2)	6117 CBZ	0 to +85	8 Ld SOIC (Pb-free)	M8.15
ISL6120CBZA (Notes 1, 2) **No longer available or supported**	6120 CBZ	0 to +85	8 Ld SOIC (Pb-free)	M8.15
ISL6115EVAL1Z	Evaluation Platform			

NOTES:

1. Please refer to TB347 for details on reel specifications. Add "-T" suffix for tape and reel.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL6115. For more information on MSL please see techbrief TB363.

Pin Configuration

ISL6115, ISL6116, ISL6117, ISL6120
(8 LD SOIC)
TOP VIEW



Pin Descriptions

PIN #	SYMBOL	FUNCTION	DESCRIPTION
1	ISET	Current Set	Connect to the low side of the current sense resistor through the current limiting set resistor. This pin functions as the current limit programming pin.
2	ISEN	Current Sense	Connect to the more positive end of sense resistor to measure the voltage drop across this resistor.
3	GATE	External FET Gate Drive Pin	Connect to the gate of the external N-Channel MOSFET. A capacitor from this node to ground sets the turn-on ramp. At turn-on this capacitor will be charged to V_{DD} +5V (ISL6115) and to V_{DD} (ISL6116, ISL6117, ISL6120) by a 10µA current source.
4	VSS	Chip Return	
5	VDD	Chip Supply	12V chip supply. This can be either connected directly to the +12V rail supplying the switched load voltage or to a dedicated V_{SS} +12V supply.
6	CTIM	Current Limit Timing Capacitor	Connect a capacitor from this pin to ground. This capacitor determines the time delay between an overcurrent event and chip output shutdown (current limit time-out). The duration of current limit time-out is equal to 93kΩ x C_{TIM}.
7	PGOOD	Power Good Indicator	Indicates that the voltage on the ISEN pin is satisfactory. PGOOD is driven by an open drain N-Channel MOSFET and is pulled low when the output voltage (VISEN) is less than the UV level for the particular IC.
8	PWRON	Power-ON	PWRON is used to control and reset the chip. The chip is enabled when PWRON pin is driven high to a maximum of 5V or is left open. Do not drive this input >5V. After a current limit time-out, the chip is reset by a low level signal applied to this pin. This input has 20µA pull-up capability.

Absolute Maximum Ratings T_A = +25°C

V_{DD} . . . . . -0.3V to +16V
GATE . . . . . -0.3V to V_{DD} + 8V
ISEN, PGOOD, PWRON, CTIM, ISET . . . -0.3V to V_{DD} + 0.3V
ESD Rating
Human Body Model 5kV

Operating Conditions

V_{DD} Supply Voltage Range (ISL6115) . . . . . +12V ±15%
V_{DD} Supply Voltage Range (ISL6116, 17, 20) . . +12V ±25%
Temperature Range (T_A) . . . . . 0°C to +85°C

Thermal Information

Thermal Resistance (Typical, Note 4) θ_{JA} (°C/W)
8 Ld SOIC Package 98
Maximum Junction Temperature (Plastic Package) . . +150°C
Maximum Storage Temperature Range . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
5. All voltages are relative to GND, unless otherwise specified.

Electrical Specifications

V_{DD} = 12V, T_A = T_J = 0°C to +85°C, Unless Otherwise Specified. Temperature limits established by characterization and are not production tested. **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
CURRENT CONTROL						
ISET Current Source	I_{ISET_ft}		**18.5**	20	**21.5**	µA
ISET Current Source	I_{ISET_pt}	T_J = +15°C to +55°C	19	20	21	µA
Current Limit Amp Offset Voltage	Vio_ft	V_{ISET} - V_{ISEN}	**-6**	0	**6**	mV
Current Limit Amp Offset Voltage	Vio_pt	V_{ISET} - V_{ISEN}, T_J = +15°C to +55°C	-2	0	2	mV
GATE DRIVE						
GATE Response Time to Severe OC	pd_woc_amp	V_{GATE} to 10.8V	-	100	-	ns
GATE Response Time to Overcurrent	pd_oc_amp	V_{GATE} to 10.8V	-	600	-	ns
GATE Turn-On Current	I_{GATE}	V_{GATE} to = 6V	**8.4**	10	**11.6**	µA
GATE Pull-Down Current	OC_GATE_I_4V	Overcurrent	**45**	75	-	mA
GATE Pull-Down Current (Note 6)	WOC_GATE_I_4V	Severe Overcurrent	**0.5**	0.8	-	A
ISL6115 Undervoltage Threshold	$12V_{UV_VTH}$		**9.2**	9.6	**10**	V
ISL6115 GATE High Voltage	12VG	GATE Voltage	**V_{DD} + 4.5V**	V_{DD} + 5V	-	V
ISL6116 Undervoltage Threshold	$5V_{UV_VTH}$		**4.0**	4.35	**4.5**	V
ISL6117 Undervoltage Threshold	$3V_{UV_VTH}$		**2.4**	2.6	**2.8**	V
ISL6120 Undervoltage Threshold	$2V_{UV_VTH}$		**1.8**	1.85	**1.9**	V
ISL6116, ISL6117, ISL6120 GATE High Voltage	VG	GATE Voltage	**V_{DD} - 1.5V**	V_{DD}	-	V
BIAS						
V_{DD} Supply Current	I_{VDD}		-	3	**5**	mA
V_{DD} POR Rising Threshold	$V_{DD_POR_L2H}$	VDD Low to High	**7.8**	8.4	**9**	V
V_{DD} POR Falling Threshold	$V_{DD_POR_H2L}$	VDD High to Low	**7.5**	8.1	**8.7**	V
V_{DD} POR Threshold Hysteresis	$V_{DD_POR_HYS}$	$V_{DD_POR_L2H}$ - $V_{DD_POR_H2L}$	**0.1**	0.3	**0.6**	V
Maximum PWRON Pull-Up Voltage	PWRN_PUV	Maximum External Pull-up Voltage	-	5	-	V

Electrical Specifications V_{DD} = 12V, T_A = T_J = 0°C to +85°C, Unless Otherwise Specified. Temperature limits established by characterization and are not production tested. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
PWRON Pull-Up Voltage	PWRN_V	PWRON Pin Open	**2.7**	3.2	**-**	V
PWRON Rising Threshold	PWR_Vth		**1.4**	1.7	**2.0**	V
PWRON Hysteresis	PWR_hys		**130**	170	**250**	mV
PWRON Pull-Up Current	PWRN_I		**9**	17	**25**	µA
CURRENT REGULATION DURATION/POWER GOOD						
C_{TIM} Charging Current	C_{TIM}_ichg0	V_{CTIM} = 0V	**16**	20	**23**	µA
C_{TIM} Fault Pull-Up Current (Note 6)			**-**	20	**-**	mA
Current Limit Time-Out Threshold Voltage	C_{TIM}_Vth	CTIM Voltage	**1.3**	1.8	**2.3**	V
Power Good Pull Down Current	PG_Ipd	V_{OUT} = 0.5V	**-**	8	**-**	mA

NOTES:

6. Limits established by characterization and are not production tested.
7. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified.

Description and Operation

The members of this IC family are single power supply distribution controllers for generic hot swap applications across the +2.5V to +12V supply range. The ISL6115 is targeted for +12V switching applications whereas the ISL6116 is targeted for +5V, the ISL6117 for +3.3V and the ISL6120 for +2.5V applications. Each IC has a hardwired undervoltage (UV) threshold level approximately 17% lower than the stated voltages.

These ICs feature a highly accurate programmable current regulation (CR) level with programmable time delay to latch-off, and programmable soft-start turnHon ramp all set with a minimum of external passive components. The ICs also include severe OC protection that immediately shuts down the MOSFET switch should a rapid load current transient such as with a dead short cause the CR Vth to exceed the programmed level by 150mV. Additionally, the ICs have a UV indicator and an OC latch indicator. The functionality of the PGOOD feature is enabled once the IC is biased, monitoring and reporting any UV condition on the ISEN pin.

Upon initial power-up, the IC can either isolate the voltage supply from the load by holding the external N-Channel MOSFET switch off or apply the supply rail voltage directly to the load for true hot swap capability. The PWRON pin must be pulled low for the device to isolate the power supply from the load by holding the external N-Channel MOSFET off. With the PWRON pin held high or floating the IC will be in true hot swap mode. In both cases the IC turns on in a soft-start mode protecting the supply rail from sudden in-rush current.

At turn-on, the external gate capacitor of the N-Channel MOSFET is charged with a 10µA current source resulting in a programmable ramp (soft-start turn-on). The internal ISL6115 charge pump supplies the gate drive for the 12V supply switch driving that gate to ~V_{DD} +5V, for the other three ICs the gate drive voltage is limited to the chip bias voltage, VDD.

Load current passes through the external current sense resistor. When the voltage across the sense resistor exceeds the user programmed CR voltage threshold value, (see Table 1 for R_{ISET} programming resistor value and resulting nominal current regulation threshold voltage, V_{CR}) the controller enters its current regulation mode. At this time, the time-out capacitor, on CTIM pin is charged with a 20µA current source and the controller enters the current limit time to latch-off period. The length of the current limit time to latch-off duration is set by the value of a single external capacitor (see Table 2) for C_{TIM} capacitor value and resulting nominal current limited time-out to latch-off duration placed from the CTIM pin (pin 6) to ground. The programmed current level is held until either the OC event passes or the time-out period expires. If the former is the case then the N-Channel MOSFET is fully enhanced and the C_{TIM} capacitor is discharged. Once C_{TIM} charges to 1.87V signaling that the time-out period has expired, an internal latch is set whereby the FET gate is quickly pulled to 0V turning off the N-Channel MOSFET switch, isolating the faulty load.

TABLE 1. R_{ISET} PROGRAMMING RESISTOR VALUE

R_{ISET} RESISTOR	NOMINAL CR VTH
10kΩ	200mV
4.99kΩ	100mV
2.5kΩ	50mV
750Ω	15mV

NOTE: Nominal Vth = R_{ISET} x 20µA.

TABLE 2. C_{TIM} CAPACITOR VALUE

C_{TIM} CAPACITOR	NOMINAL CURRENT LIMITED PERIOD
0.022µF	2ms
0.047µF	4.4ms
0.1µF	9.3ms

NOTE: Nominal time-out period = C_{TIM} x 93kΩ.

This IC responds to a severe overcurrent load (defined as a voltage across the sense resistor >150mV over the OC Vth set point) by immediately driving the N-Channel MOSFET gate to 0V in about 10µs. The gate voltage is then slowly ramped up turning on the N-Channel MOSFET to the programmed current regulation level; this is the start of the time-out period.

Upon a UV condition, the PGOOD signal will pull low when tied high through a resistor to the logic or VDD supply. This pin is a UV fault indicator. For an OC latch-off indication, monitor CTIM, pin 6. This pin will rise rapidly from 1.9V to VDD once the time-out period expires.

See Figures 12 through 16 for waveforms relevant to text.

The IC is reset after an OC latch-off condition by a low level on the PWRON pin and is turned on by the PWRON pin being driven high.

Application Considerations

Design applications where the CR Vth is set extremely low (25mV or less), there is a two-fold risk to consider.

- There is the susceptibility to noise influencing the absolute CR Vth value. This can be addressed with a 100pF capacitor across the R_{SENSE} resistor.
- Due to common mode limitations of the overcurrent comparator, the voltage on the ISET pin must be 20mV above the IC ground either initially (from I_{SET}*R_{SET}) or before C_{TIM} reaches time-out (from gate charge-up). If this does not happen, the IC may incorrectly report overcurrent fault at start-up when there is no fault. Circuits with high load capacitance and initially low load current are susceptible to this type of unexpected behavior.

Do not signal nor pull-up the PWRON input to > 5V. Exceeding 6V on this pin will cause the internal charge pump to malfunction.

During the soft-start and the time-out delay duration with the IC in its current limit mode, the V_{GS} of the external N-Channel MOSFET is reduced driving the MOSFET switch into a (linear region) high $r_{DS(ON)}$ state. Strike a balance between the CR limit and the timing requirements to avoid periods when the external N-Channel MOSFETs may be damaged or destroyed due to excessive internal power dissipation. Refer to the **MOSFET SOA** information in the manufacturer's data sheet.

When driving particularly large capacitive loads a longer soft-start time to prevent current regulation upon charging and a short CR time may offer the best application solution relative to reliability and FET MTF.

Physical layout of R_{SENSE} resistor is critical to avoid the possibility of false overcurrent occurrences. Ideally, trace routing between the R_{SENSE} resistors and the IC is as direct and as short as possible with zero current in the sense lines (see Figure 1)..

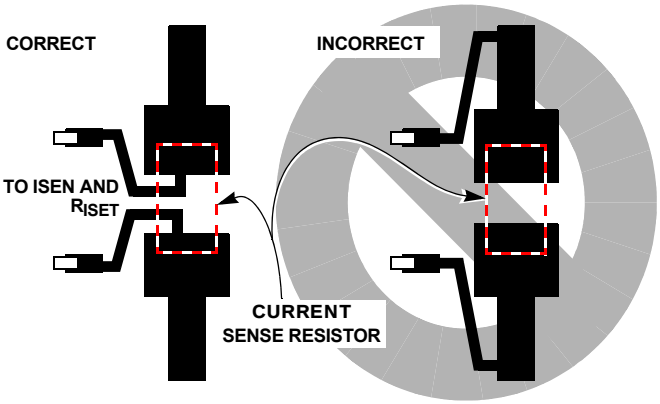


FIGURE 1. SENSE RESISTOR PCB LAYOUT

Using the ISL6116 as a -48V Low Side Hot Swap Power Controller

To supply the required V_{DD}, it is necessary to maintain the chip supply 10V to 16V above the -48V bus. This may be accomplished with a suitable regulator between the voltage rail and pin 5 (VDD). By using a regulator, the designer may ignore the bus voltage variations. However, a low-cost alternative is to use a Zener diode (see Figure 2 for typical 5A load control); this option is detailed in the following.

Note that in this configuration the PGOOD feature (pin 7) is not operational as the I_{SEN} pin voltage is always < UV threshold.

See Figures 17 through 20 for waveforms relevant to -48V and other high voltage applications.

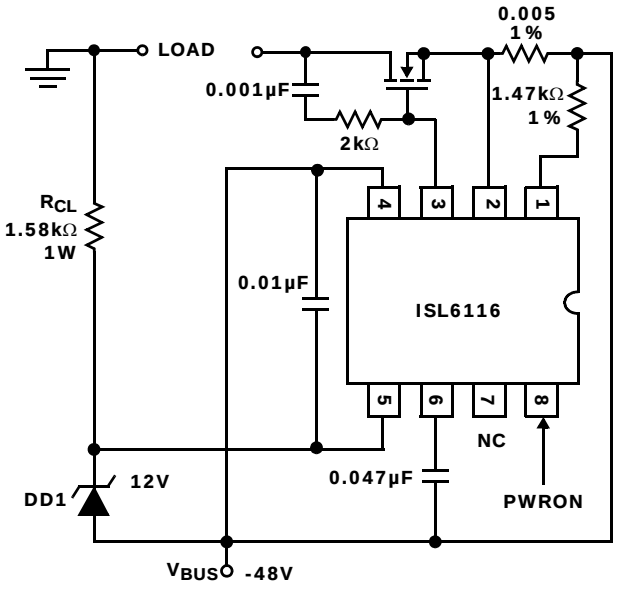


FIGURE 2. TYPICAL 5A LOAD CONTROL

Biasing the ISL6116

Table 3 gives typical component values for biasing the ISL6116 in a ±48V application. The formulas and calculations deriving these values are also shown in the following equations.

TABLE 3. TYPICAL VALUES FOR A -48V HOT SWAP APPLICATION

SYMBOL	PARAMETER
R_{CL}	1.58kΩ, 1W
DD1	12V Zener Diode, 50mA Reverse Current

When using the ISL6116 to control -48V, a Zener diode may be used to provide the +12V bias to the chip. If a Zener is used then a current limit resistor should also be used. Several items must be taken into account when choosing values for the current limit resistor (R_{CL}) and Zener Diode (DD1):

- The variation of the V_{BUS} (in this case, -48V nominal)
- The chip supply current needs for all functional conditions
- The power rating of R_{CL}.
- The current rating of DD1

Formulas

Sizing R_{CL} is expressed in Equation 1:

$$R_{CL} = \frac{V_{BUS(MIN)} - 12}{I_{CHIP}} \quad \text{(EQ. 1)}$$

Power Rating of R_{CL} is expressed in Equation 2:

$$P_{RCL} = I_C(V_{BUS(MAX)} - 12) \quad \text{(EQ. 2)}$$

DD1 current rating is expressed in Equation 3:

$$I_{DD1} = \frac{(V_{BUS(MAX)} - 12)}{R_{CL}} \quad \text{(EQ. 3)}$$

Example:

A typical -48V supply may vary from -36 to -72V. Therefore:

$V_{BUS,MAX}$ = -72V
$V_{BUS,MIN}$ = -36V

I_{CHIP} = 15mA (Max)

Sizing R_{CL} is expressed in Equation 4:

$$R_{CL} = \frac{(V_{BUS(MIN)} - 12)}{I_C}$$

$$R_{CL} = \frac{36 - 12}{0.015} \quad \text{(EQ. 4)}$$

R_{CL} = 16kΩ[TypicalValue = 1.58kΩ]

Power rating of R_{CL} is expressed in Equation 5:

$$P_{RCL} = I_C(V_{BUS(MAX)} - 12)$$

$$P_{RCL} = (0.015)(72 - 12) \quad \text{(EQ. 5)}$$

P_{RCL} = 0.9W[TypicalValue = 1W]

DD1 current rating is expressed in Equation 6:

$$I_{DD1} = \frac{(V_{BUS(MAX)} - 12)}{R_{CL}}$$

$$I_{DD1} = \frac{(72 - 12)}{1.58k\Omega} \quad \text{(EQ. 6)}$$

I_{DD1} = 38mA[TypicalValue = 12Vrating, 50mA reverse current]

Typical Performance Curves

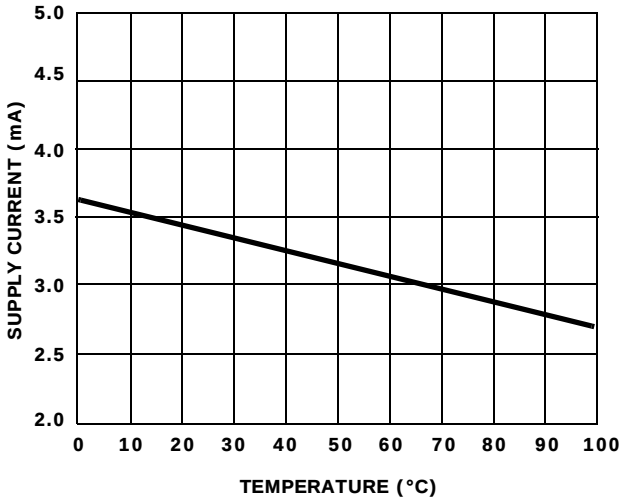


FIGURE 3. V_{DD} BIAS CURRENT

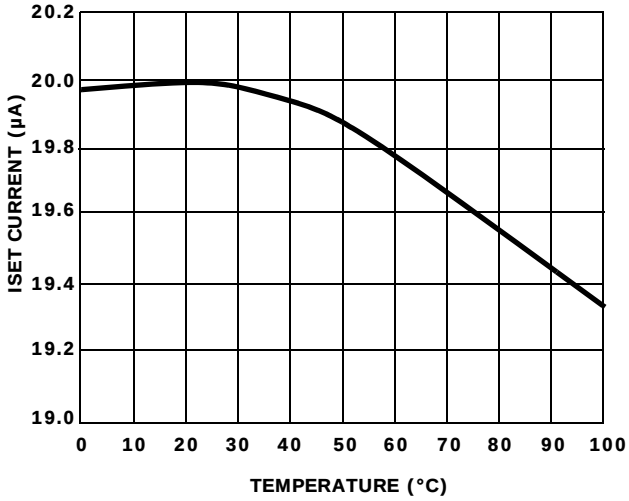


FIGURE 4. I_{SET} SOURCE CURRENT

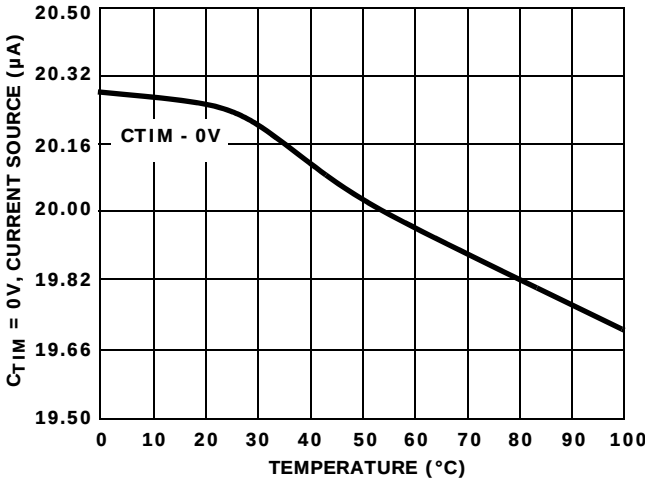


FIGURE 5. C_{TIM} CURRENT SOURCE

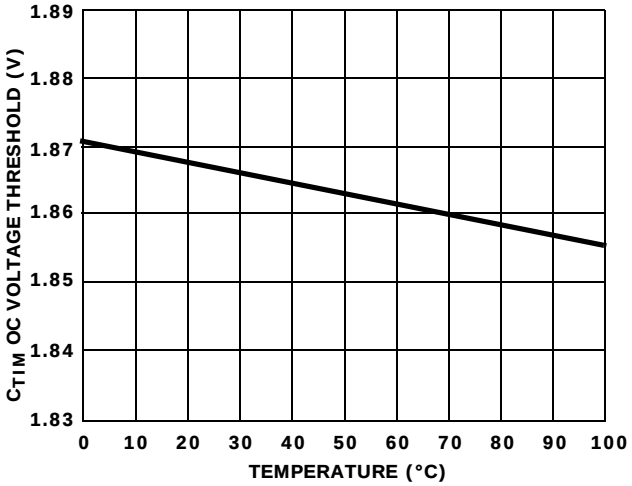


FIGURE 6. C_{TIM} OC VOLTAGE THRESHOLD

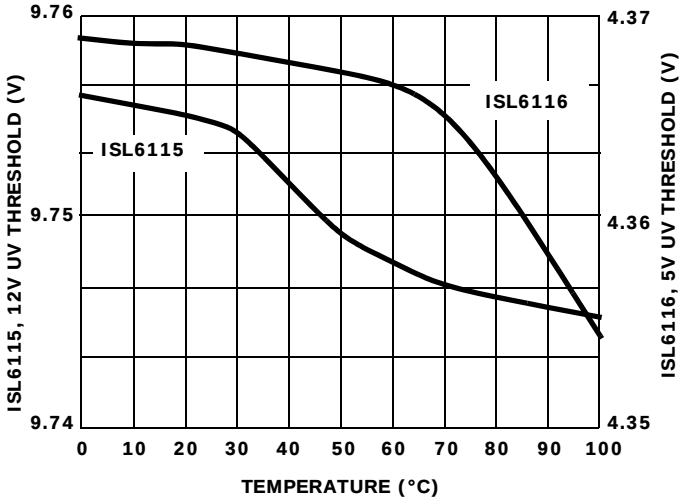


FIGURE 7. ISL6115, ISL6116 UV THRESHOLD

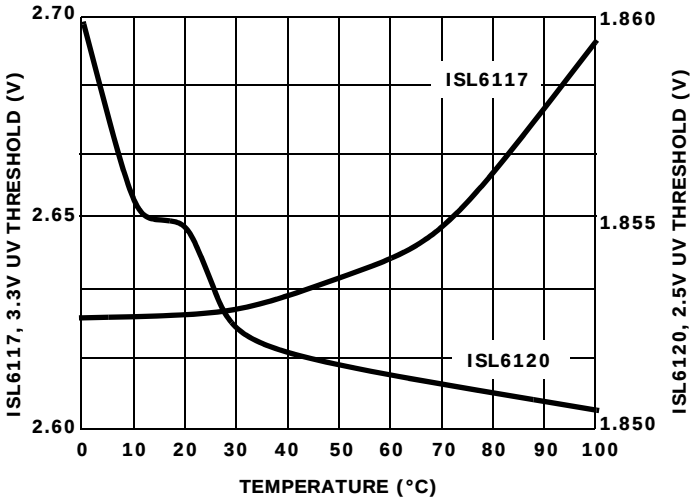


FIGURE 8. ISL6117, ISL6120 UV THRESHOLD

Typical Performance Curves (Continued)

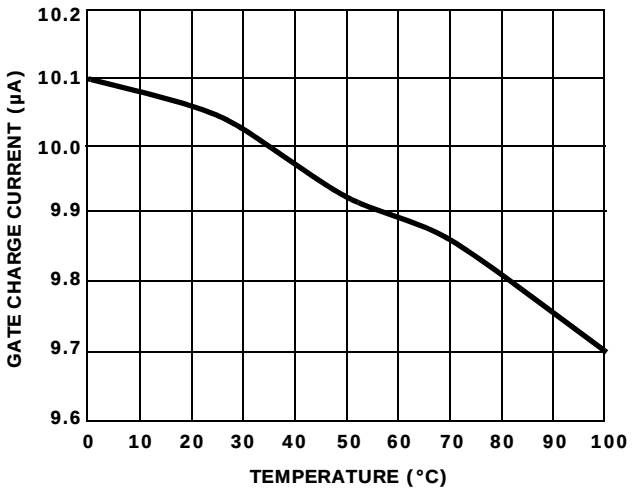


FIGURE 9. GATE CHARGE CURRENT

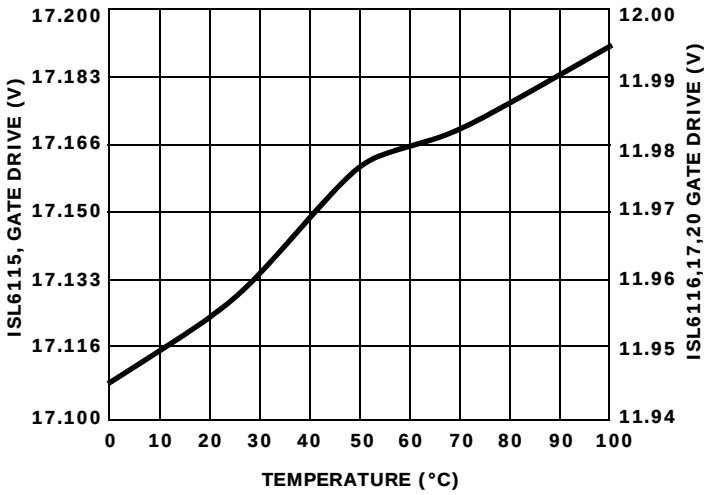


FIGURE 10. GATE DRIVE VOLTAGE, V_{DD} = 12V

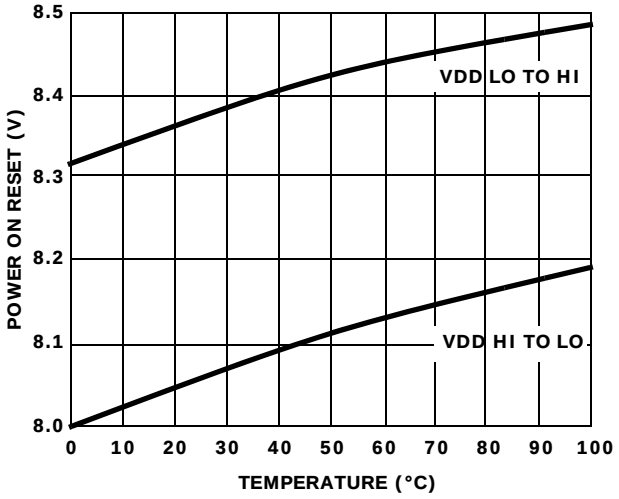


FIGURE 11. POWER-ON RESET VOLTAGE THRESHOLD

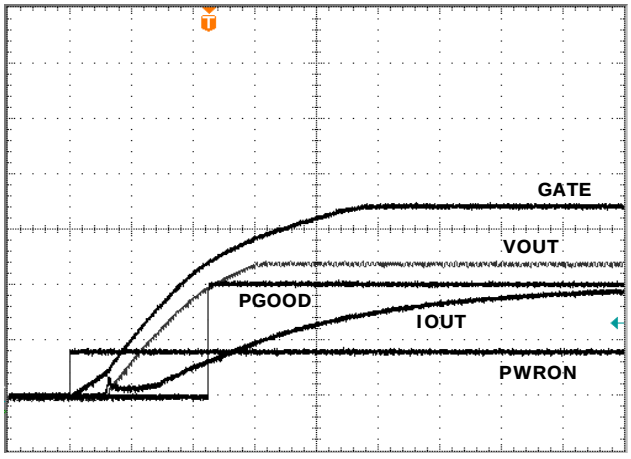


FIGURE 12. ISL6115 +12V TURN-ON

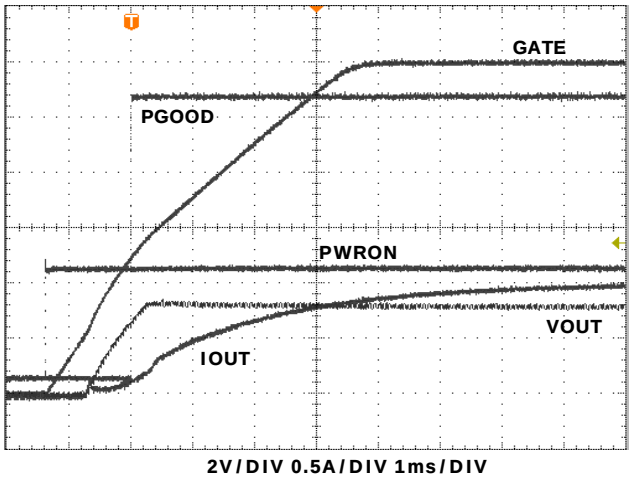


FIGURE 13. ISL6116 +5V TURN-ON

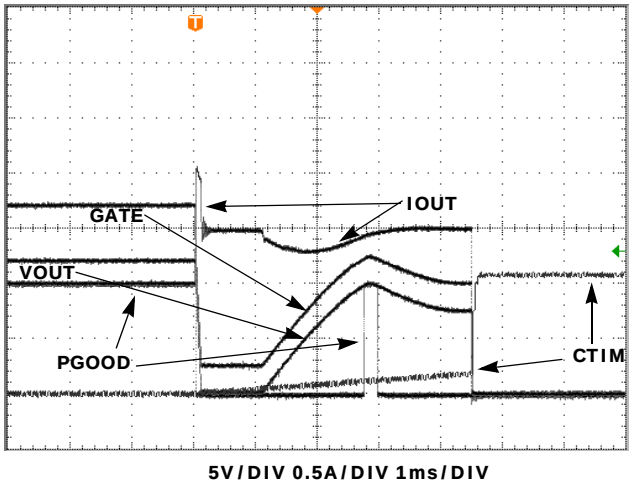


FIGURE 14. ISL6115 'LOW' OVERCURRENT RESPONSE

Typical Performance Curves (Continued)

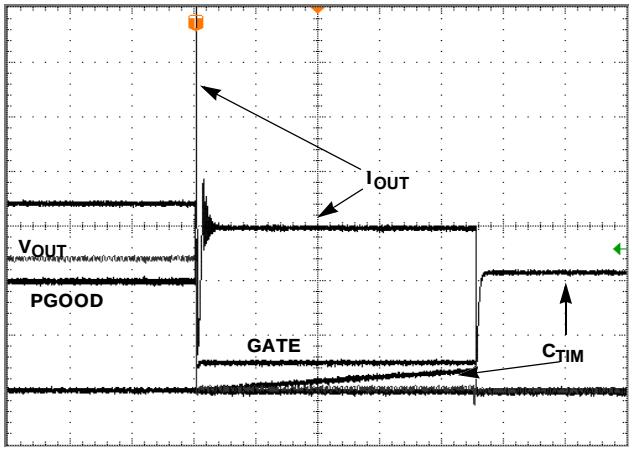


FIGURE 15. ISL6115 'HIGH' OVERCURRENT RESPONSE

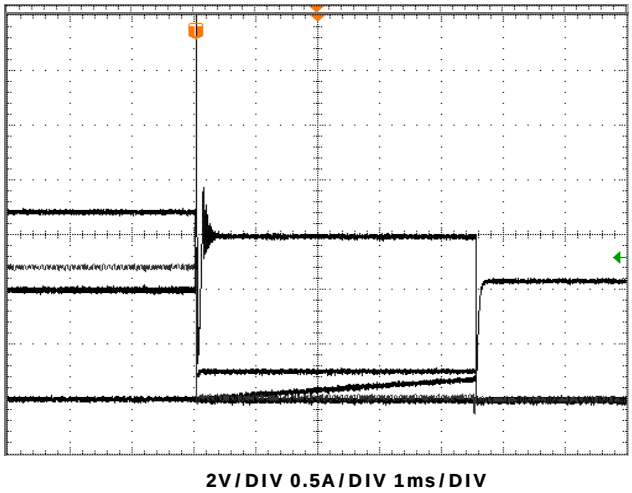


FIGURE 16. ISL6116 'HIGH' OVERCURRENT RESPONSE

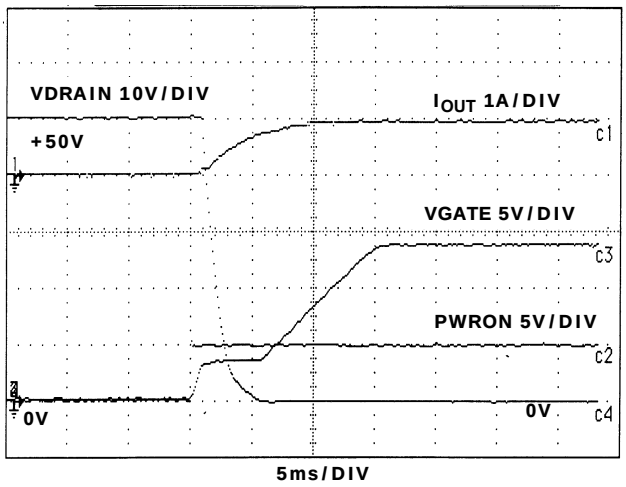


FIGURE 17. +50V LOW SIDE SWITCHING
CGATE = 100pF

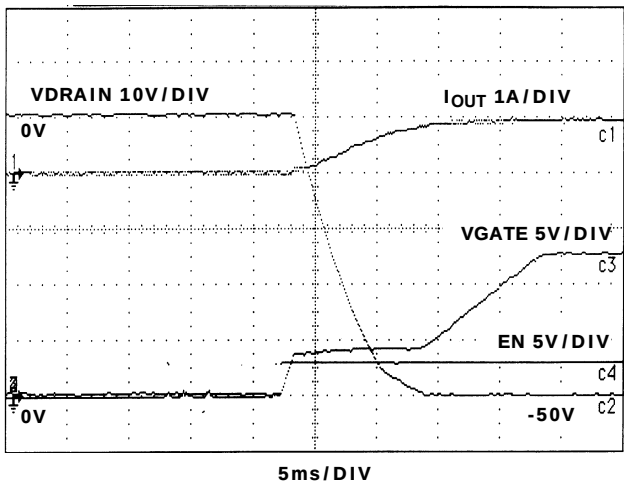


FIGURE 18. -50V LOW SIDE SWITCHING
CGATE = 1000pF

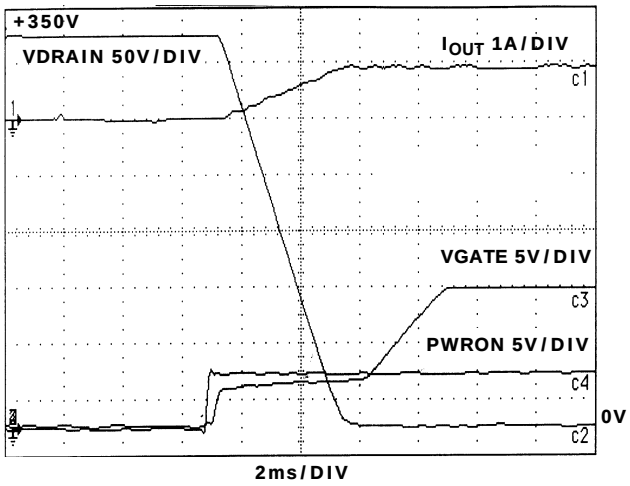


FIGURE 19. +350V LOW SIDE SWITCHING
CGATE = 100pF

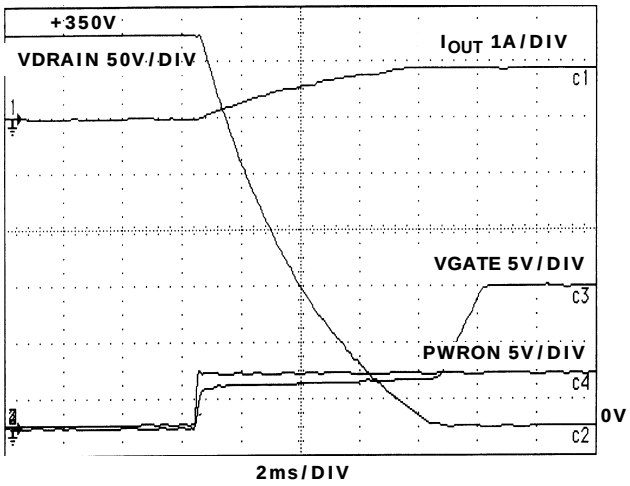


FIGURE 20. +350V LOW SIDE SWITCHING
CGATE = 1000pF

ISL6115EVAL1Z Board

The ISL6115EVAL1Z is default provided as a +12V high side switch controller with the CR level set at ~1.5A. See Figure 21 for ISL6115EVAL1Z schematic and Table 4 for BOM. Bias and load connection points are provided along with test points for each IC pin.

With J1 installed the ISL6115 will be biased from the +12V supply (V_{IN}) being switched. Connect the load to VLOAD+. PWRON pin pulls high internally enabling the ISL6115 if not driven low via PWRON test point or J2.

With R_3 = 750Ω the CR Vth is set to 15mV and with the 10mΩ sense resistor (R_1) the ISL6115EVAL1Z has a nominal CR level of 1.5A. The 0.01µF delay time to latch-off capacitor results in a nominal 1ms before latch-off of output after an OC event.

Also included with the ISL6115EVAL1Z board are one each of the ISL6116, ISL6117 and ISL6120 for evaluation of those ICs in a high side application. Remove J1 and provide a separate +12V IC bias supply via V_{BIAS} test point.

Reconfiguring the ISL6115EVAL1Z board for a higher CR level can be done by changing the R_{SENSE} and/or R_{ISET} resistor values as the provided FET is rated for a much higher current.

ISL6116EVAL1 Board

The ISL6116EVAL1 is default configured as a negative voltage low side switch controller with a ~2.4A CR level. See Figure 22 for ISL6116EVAL1 schematic and Table 4 for BOM and component description. This basic configuration is capable of controlling both larger positive or negative potential voltages with minimal changes.

Bias and load connection points are provided in addition to test points, TP1 to TP8 for each IC pin. The terminals, J1 and J4 are for the bus voltage and return, respectively, with the more negative potential being connected to J4. With the load between terminals J2 and J3 the board is now configured for evaluation. The device is enabled through LOGIN, TP9 with a TTL signal. ISL6116EVAL1 includes a level shifting circuit with an opto-coupling device for the PWRON input so that standard TTL logic can be translated to the -V reference for chip control.

When controlling a positive voltage, PWRON can be accessed at TP8.

The ISL6116EVAL1 is provided with a high voltage linear regulator for convenience to provide chip bias from ±24V to ±350V. This can be removed and replaced with the zener and resistor bias scheme as discussed earlier. High voltage regulators and power discrete devices are no longer available from Intersil but can be purchased from other semiconductor manufacturers.

Reconfiguring the ISL6116EVAL1 board for a higher CR level can be done by changing the R_{SENSE} and R_{ISET} resistor values as the provided FET is 75A rated. If evaluation at >60V, an alternate FET must be chosen with an adequate BV_{DSS}.

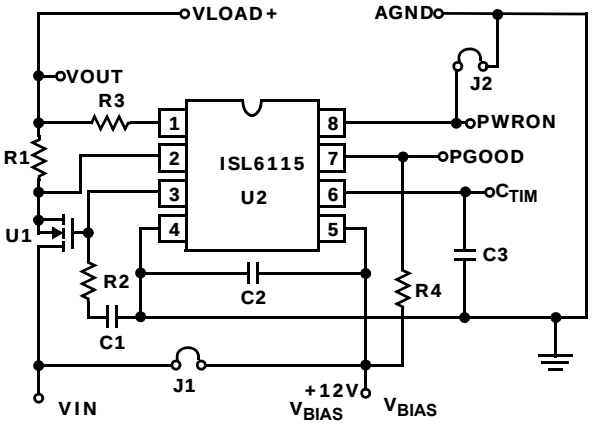


FIGURE 21. ISL6115EVAL1Z HIGH SIDE SWITCH APPLICATION

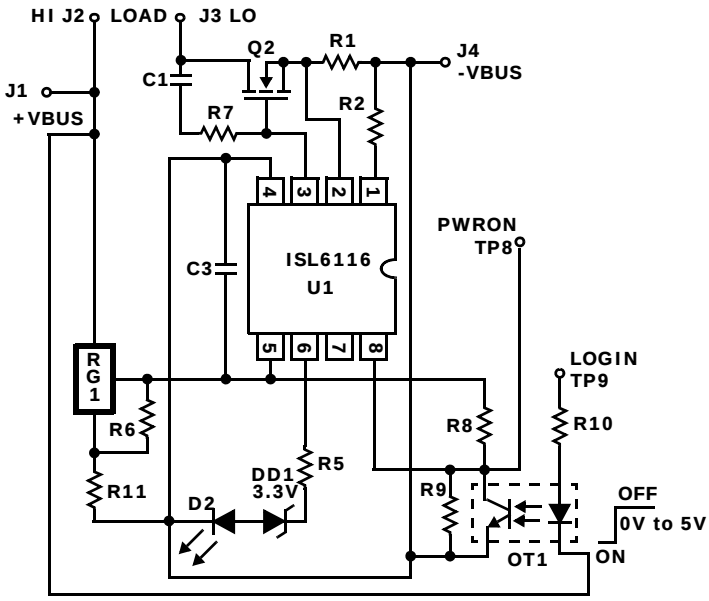


FIGURE 22. ISL6116EVAL1 NEGATIVE VOLTAGE LOW SIDE CONTROLLER

TABLE 4. BILL OF MATERIALS, ISL6115EVAL1Z, ISL6116EVAL1

COMPONENT DESIGNATOR	COMPONENT NAME	COMPONENT DESCRIPTION
ISL6115EVAL1Z		
U1	N-FET	11.5mΩ, 30V, 11.5A Logic Level N-Channel Power MOSFET or equivalent
R1	Load Current Sense Resistor	WSL-2512 10mΩ 1W Metal Strip Resistor
R2	Gate Stability Resistor	20Ω 0603 Chip Resistor
R3	Overcurrent Voltage Threshold Set Resistor	750Ω 0603 Chip Resistor (Vth = 15mV)
R4	PGOOD Pull up Resistor	10kΩ 0603 Chip Resistor
C1	Gate Timing Capacitor	0.001µF 0402 Chip Capacitor (<2ms)
C2	IC Decoupling Capacitor	0.1µF 0402 Chip Capacitor
C3	Time Delay Set Capacitor	0.01µF 0402 Chip Capacitor (1ms)
J1	Bias Voltage Selection Jumper	Install if switched rail voltage is = +12V. Remove and provide separate +12V bias voltage to U2 via V_{BIAS} if ISL6116, ISL6117 or ISL6120 is being evaluated.
J2	PWRON Disable	Install J2 to disable U2. Connects PWRON to GND.
ISL6116EVAL1		
Q2	N-FET	10mΩ, 80V, 75A N-Channel Power MOSFET or equivalent
R1	Load Current Sense Resistor	WSL-2512 10mΩ 1W Metal Strip Resistor
R2	Overcurrent Voltage Threshold Set Resistor	1.21kΩ 805 Chip Resistor (Vth = 24mV)
R7	Gate to Drain Resistor	2kΩ 805 Chip Resistor
C1	Gate Timing Capacitor	0.001µF 805 Chip Capacitor (<2ms)
C3	IC Decoupling Capacitor	0.1µF 805 Chip Capacitor
R5	LED Series Resistors	2.32kΩ 805 Chip Resistor
D2	Fault Indicating LEDs	Low Current Red SMD LED
DD1	Fault Voltage Dropping Diode	3.3V Zener Diode, SOT-23 SMD 350mW
OT1	PWRON Level Shifting Opto-Coupler	PS2801-1 NEC
R8	Level Shifting Bias Resistor	2.32kΩ 805 Chip Resistor
R9	Level Shifting Bias Resistor	1.18kΩ 805 Chip Resistor
R10	Level Shifting Bias Resistor	200Ω 805 Chip Resistor
RG1	HIP5600IS	High Voltage Linear Regulator
R6	Linear Regulator RF1	1.78kΩ 805 Chip Resistor
R11	Linear Regulator RF2	15kΩ 805 Chip Resistor

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
December 3, 2015	FN9100.8	Added Rev History and About Intersil sections. Updated Ordering Information on page 2. Updated POD M8.15 to most current version. Revision changes are as follows: Updated to new POD format by removing table and moving dimensions onto drawing and adding land pattern Changed in Typical Recommended Land Pattern the following: 2.41(0.095) to 2.20(0.087) 0.76 (0.030) to 0.60(0.023) 0.200 to 5.20(0.205) Changed Note 1 "1982" to "1994"

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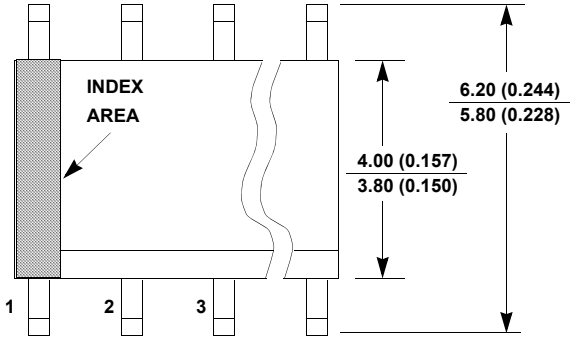
For information regarding Intersil Corporation and its products, see www.intersil.com

Package Outline Drawing

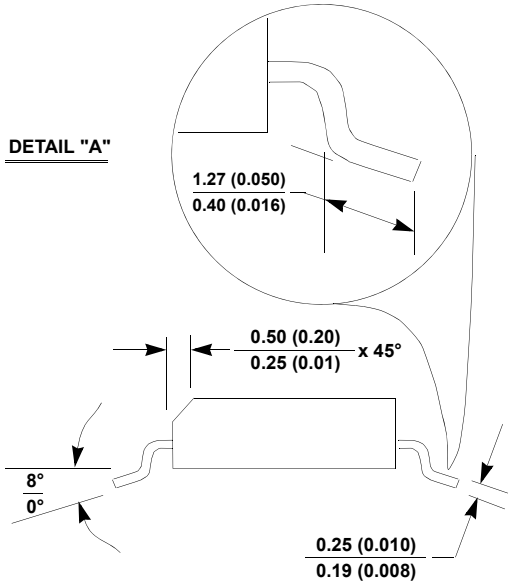
M8.15

8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

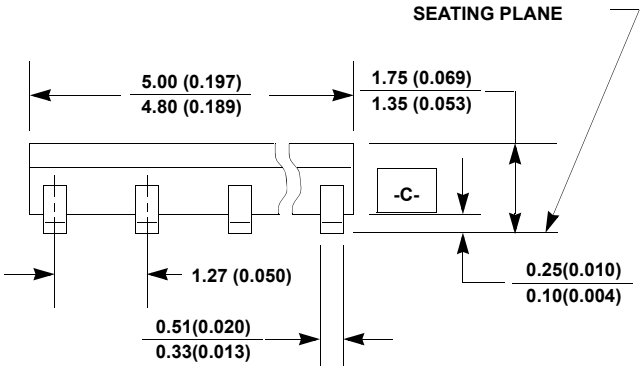
Rev 4, 1/12



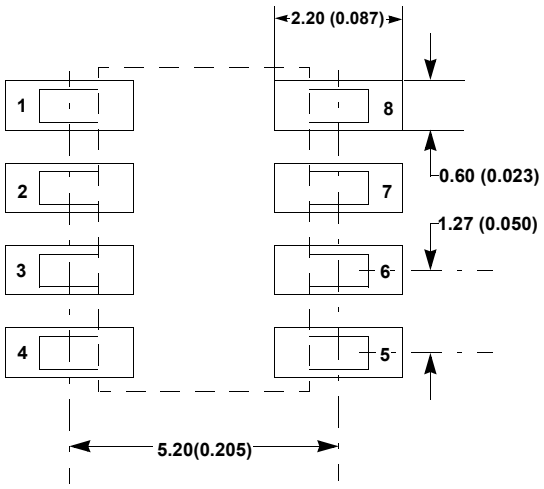
TOP VIEW



SIDE VIEW "B"



SIDE VIEW "A"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensioning and tolerancing per ANSI Y14.5M-1994.
2. Package length does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
3. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
7. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
8. This outline conforms to JEDEC publication MS-012-AA ISSUE C.