

Dual N-Channel Enhancement Mode MOSFET

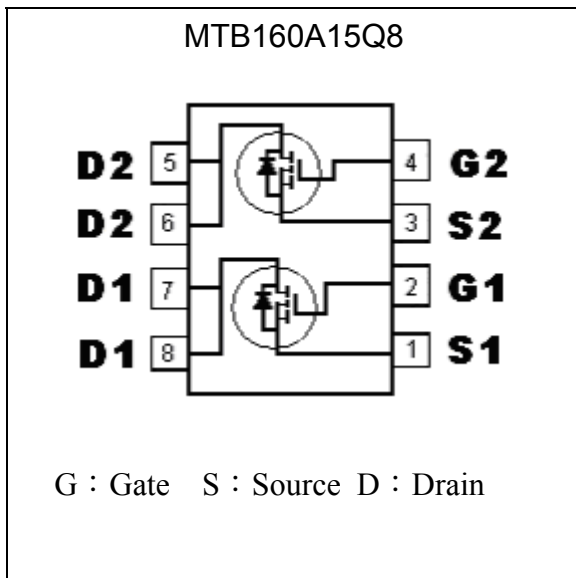
MTB160A15Q8

BV _{DSS}	150V
I _D @ T _A =25°C, V _{GS} =10V	1.8A
I _D @ T _A =70°C, V _{GS} =10V	1.5A
I _D @ T _C =25°C, V _{GS} =10V	3.2A
I _D @ T _C =100°C, V _{GS} =10V	2.3A
R _{DS(on)(typ.)} @V _{GS} =10V	169 mΩ
R _{DS(on)(typ.)} @V _{GS} =4.5V	176 mΩ

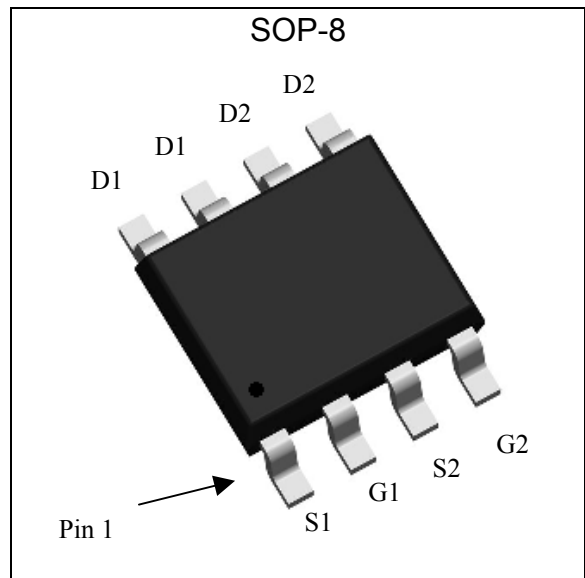
Features

- Simple drive requirement
- Low on-resistance
- Fast switching speed
- Pb-free lead plating and halogen-free package

Equivalent Circuit

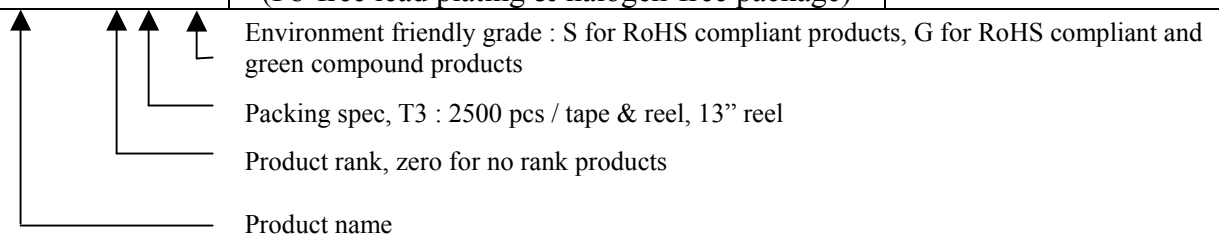


Outline



Ordering Information

Device	Package	Shipping
MTB160A15Q8-0-T3-G	SOP-8 (Pb-free lead plating & halogen-free package)	2500 pcs / Tape & Reel





The following characteristics apply to Tr 1 and Tr 2

Absolute Maximum Ratings ($T_C=25^{\circ}C$, unless otherwise noted)

Parameter		Symbol	Limits	Unit
Drain-Source Breakdown Voltage		BV_{DSS}	150	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current	$T_C=25^{\circ}C, V_{GS}=10V$	I_D	3.2	A
	$T_C=100^{\circ}C, V_{GS}=10V$		2.3	
Continuous Drain Current (Note 2)	$T_A=25^{\circ}C, V_{GS}=10V$	I_{DSM}	1.8	
	$T_A=70^{\circ}C, V_{GS}=10V$		1.5	
Pulsed Drain Current (Note 1)		I_{DM}	10	
Power Dissipation for Dual Operation @ $T_C=25^{\circ}C$		P_D	6	W
Power Dissipation for Dual Operation @ $T_A=25^{\circ}C$		P_{DSM}	3	
Power Dissipation for Single Operation @ $T_A=25^{\circ}C$			1.9 (Note 2)	
			1.1 (Note 3)	
Operating Junction and Storage Temperature Range		$T_j; T_{stg}$	-55~+175	$^{\circ}C$

Thermal Data

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-case, max	$R_{\theta JC}$	25	$^{\circ}C/W$
Thermal Resistance, Junction-to-ambient, max	$R_{\theta JA}$	50	
		78 (Note 2)	
		135 (Note 3)	

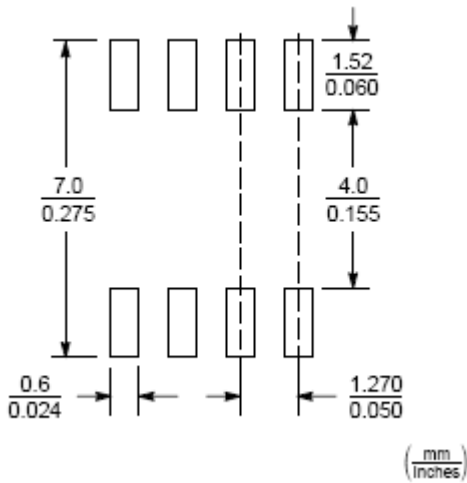
- Note : 1.Pulse width limited by maximum junction temperature.
 2.Surface mounted on 1 in² copper pad of FR-4 board, pulse width $\leq 10s$, single operation.
 3.Surface mounted on minimum copper pad, pulse width $\leq 10s$, single operation.

Electrical Characteristics ($T_C=25^{\circ}C$, unless otherwise specified)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static					
BV_{DSS}	150	-	-	V	$V_{GS}=0V, I_D=250\mu A$
$\Delta BV_{DSS}/\Delta T_j$	-	0.14	-	V/ $^{\circ}C$	Reference to $25^{\circ}C, I_D=250\mu A$
$V_{GS(th)}$	1.3	-	2.3	V	$V_{DS}=V_{GS}, I_D=250\mu A$
I_{GSS}	-	-	± 100	nA	$V_{GS}=\pm 20V, V_{DS}=0V$
I_{DSS}	-	-	1	μA	$V_{DS}=120V, V_{GS}=0V$
	-	-	10		$V_{DS}=120V, V_{GS}=0, T_j=55^{\circ}C$
$*R_{DS(ON)}$	-	169	230	m Ω	$I_D=1.8A, V_{GS}=10V$
	-	176	250		$I_D=1.5A, V_{GS}=4.5V$
$*G_{FS}$	-	7	-	S	$V_{DS}=10V, I_D=1.8A$

Dynamic					
Ciss	-	465	-	pF	V _{DS} =25V, V _{GS} =0V, f=1MHz
Coss	-	45	-		
Crss	-	26	-		
*td(ON)	-	6.4	-	ns	V _{DS} =75V, I _D =1A, V _{GS} =10V, R _G =6Ω
*tr	-	16.4	-		
*td(OFF)	-	59.6	-		
*tf	-	60	-		
*Qg	-	13.4	-	nC	V _{DS} =120V, I _D =1.8A, V _{GS} =10V
*Qgs	-	1.6	-		
*Qgd	-	3.5	-		
Body Diode					
*I _S	-	-	1.8	A	
*I _{SM}	-	-	10		
*V _{SD}	-	0.79	1.3	V	V _{GS} =0V, I _S =1.8A
trr *	-	28	-	ns	I _F =1.8A, dI _F /dt=100A/μs
Qrr *	-	37	-	nC	

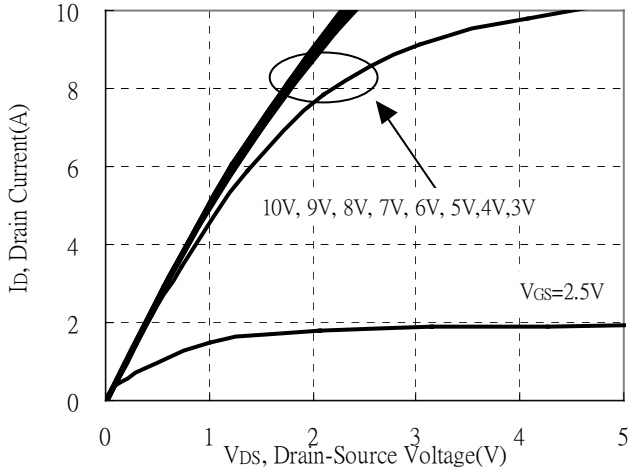
Recommended Soldering Footprint



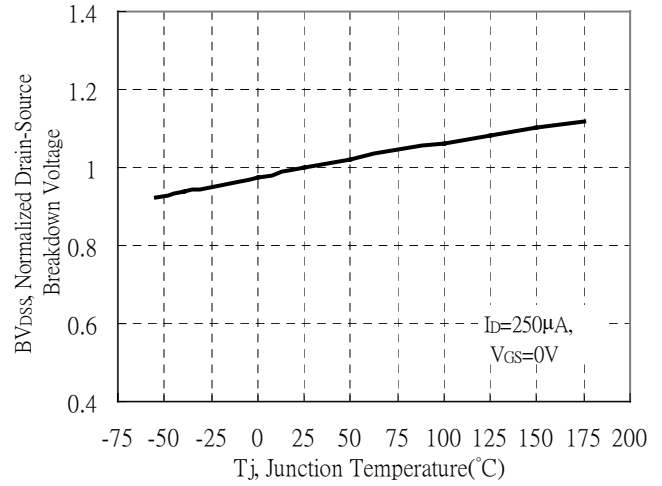


Typical Characteristics

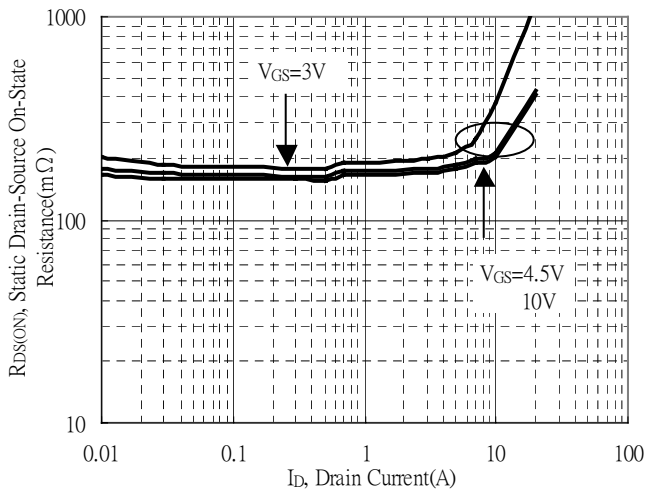
Typical Output Characteristics



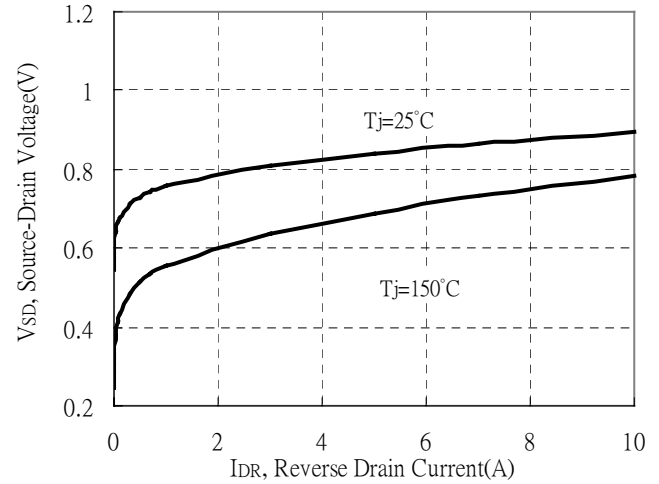
Brekdown Voltage vs Ambient Temperature



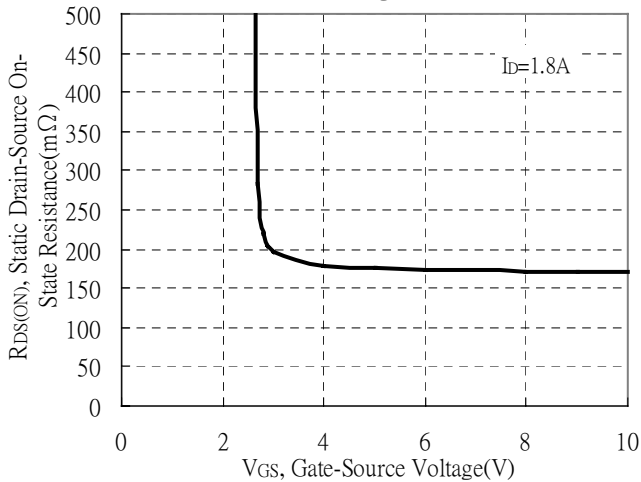
Static Drain-Source On-State resistance vs Drain Current



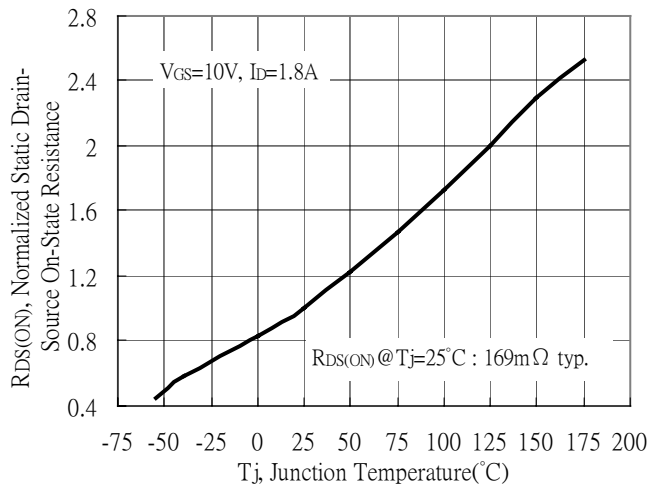
Reverse Drain Current vs Source-Drain Voltage



Static Drain-Source On-State Resistance vs Gate-Source Voltage

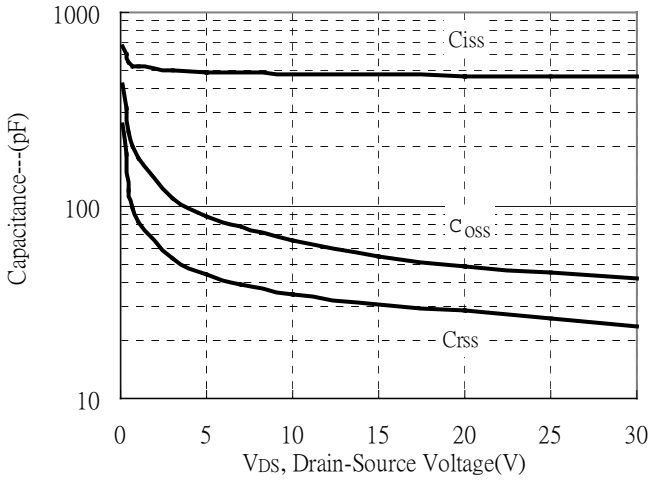


Drain-Source On-State Resistance vs Junction Temperature

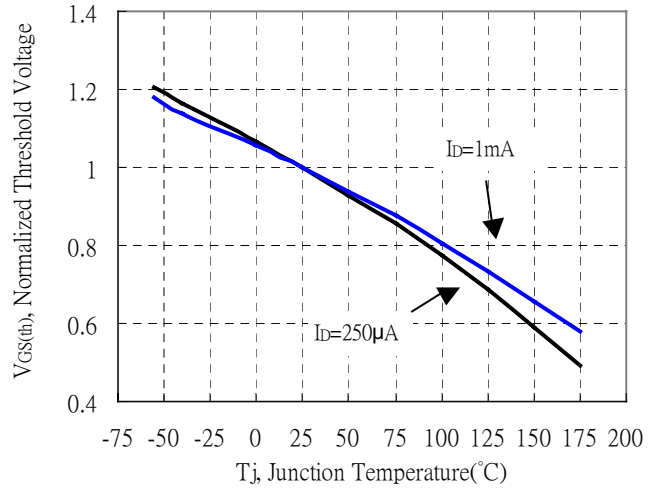


Typical Characteristics(Cont.)

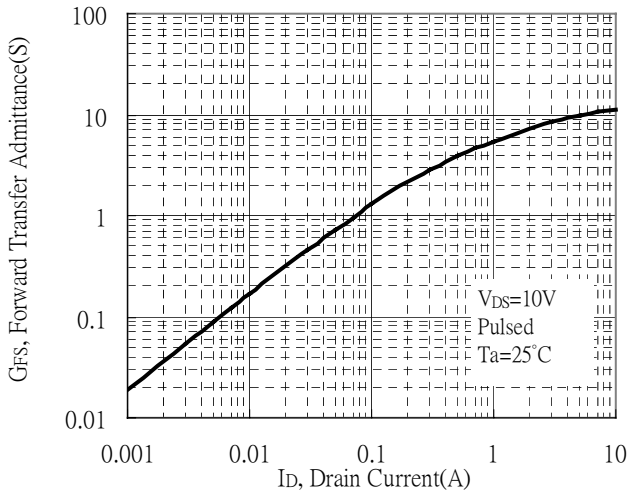
Capacitance vs Drain-to-Source Voltage



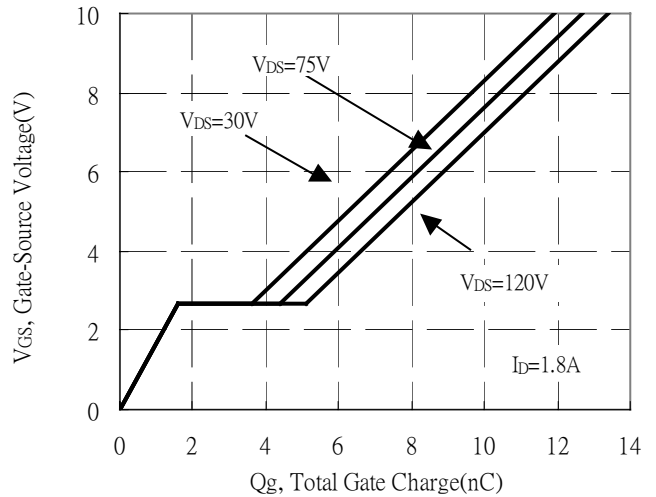
Threshold Voltage vs Junction Temperature



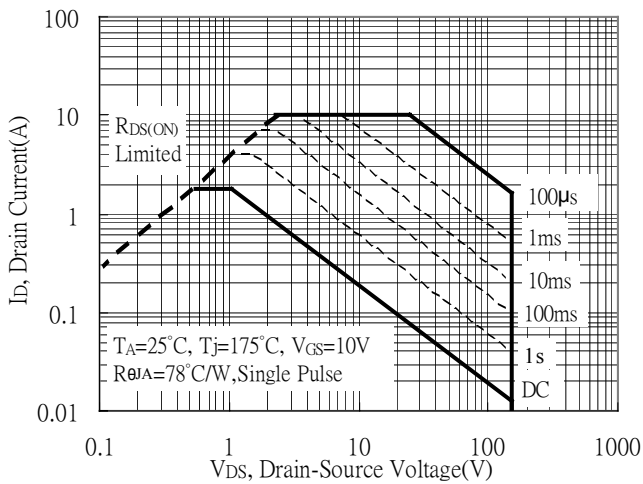
Forward Transfer Admittance vs Drain Current



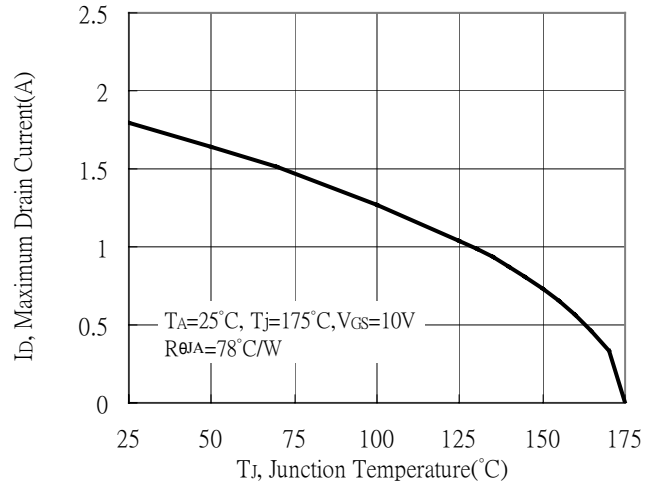
Gate Charge Characteristics



Maximum Safe Operating Area



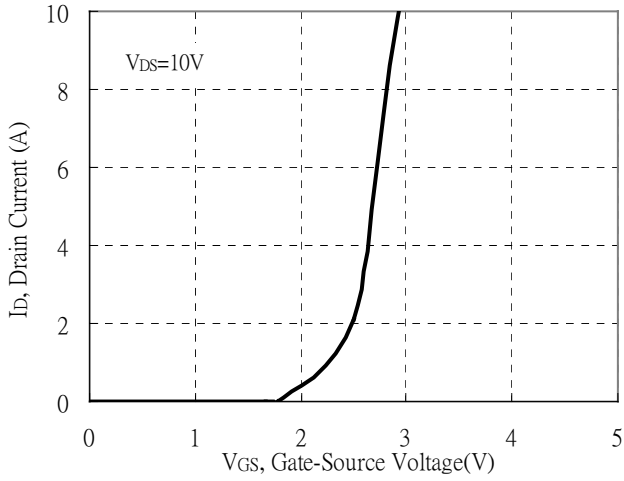
Maximum Drain Current vs Junction Temperature



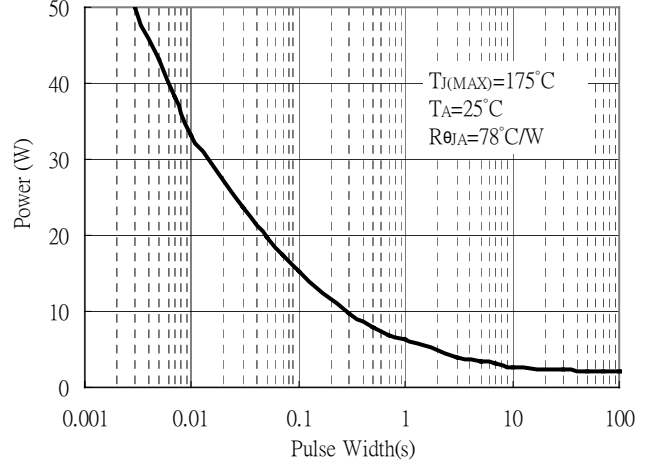


Typical Characteristics(Cont.)

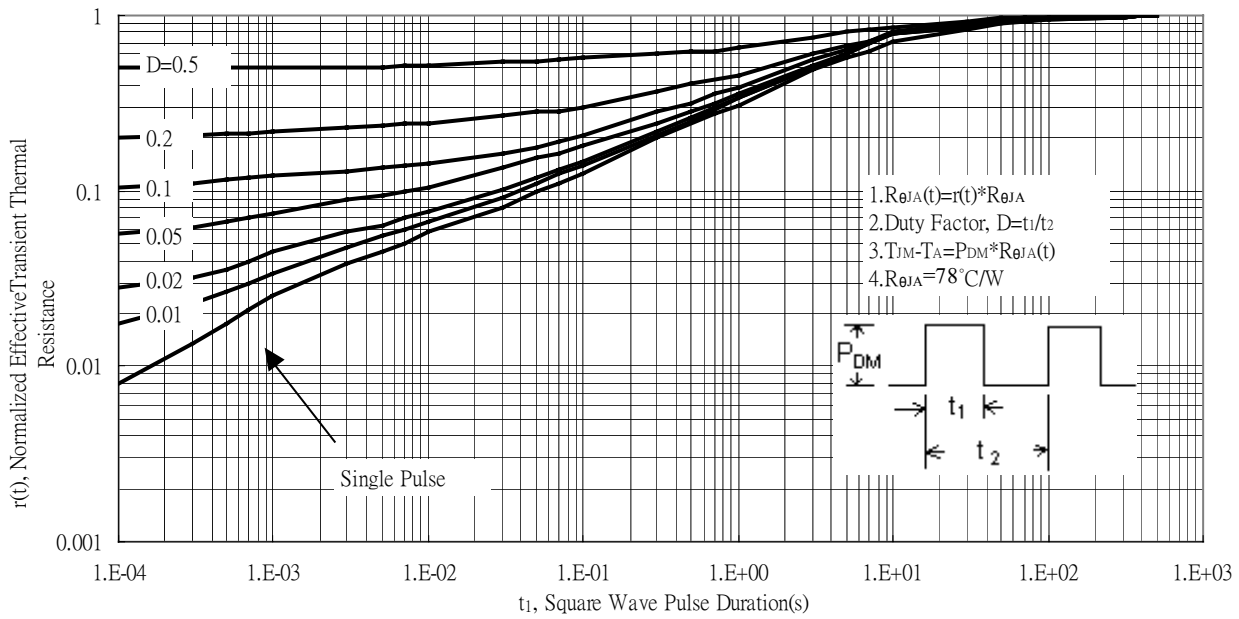
Typical Transfer Characteristics



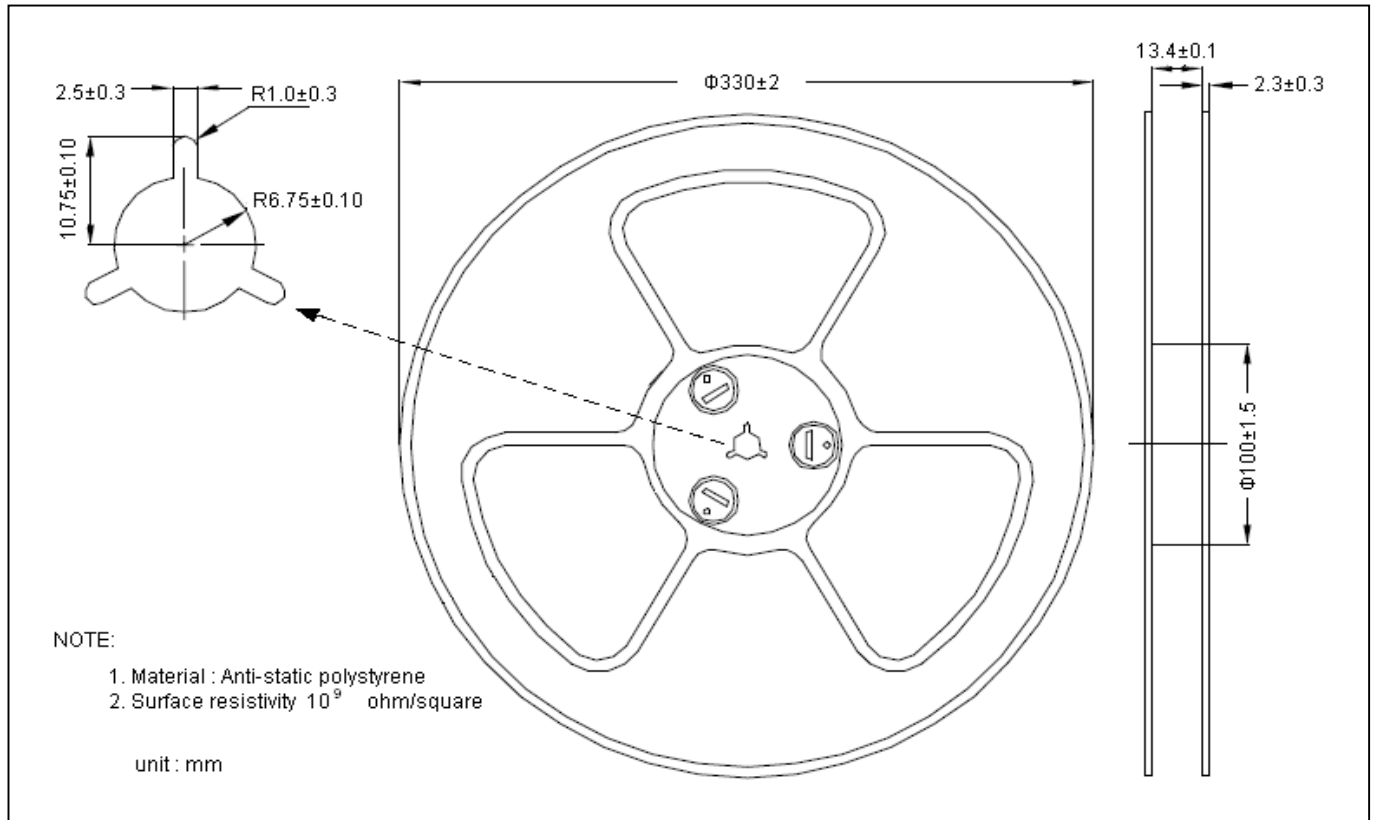
Single Pulse Power Rating, Junction to Ambient
(Note on page 2)



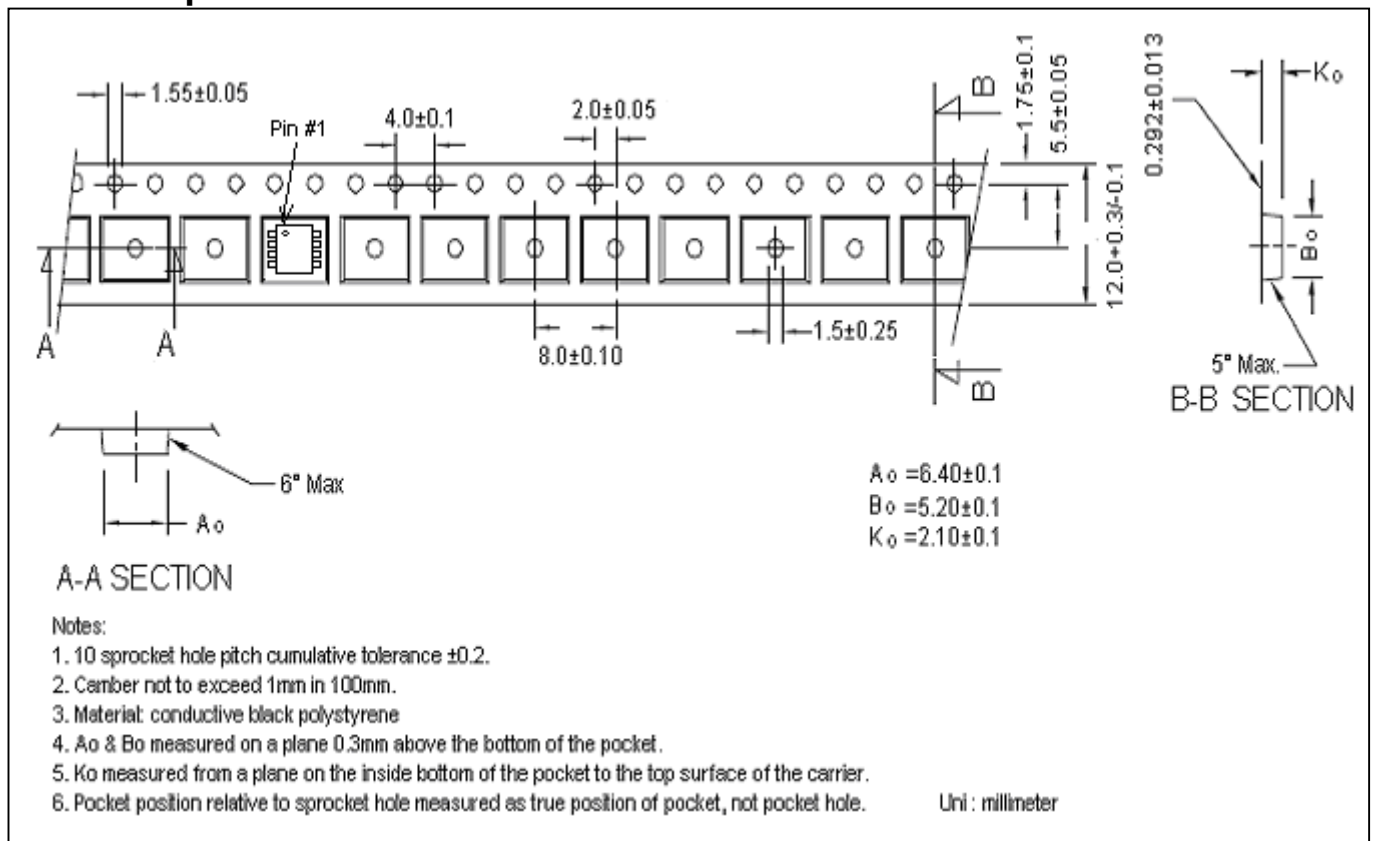
Transient Thermal Response Curves



Reel Dimension



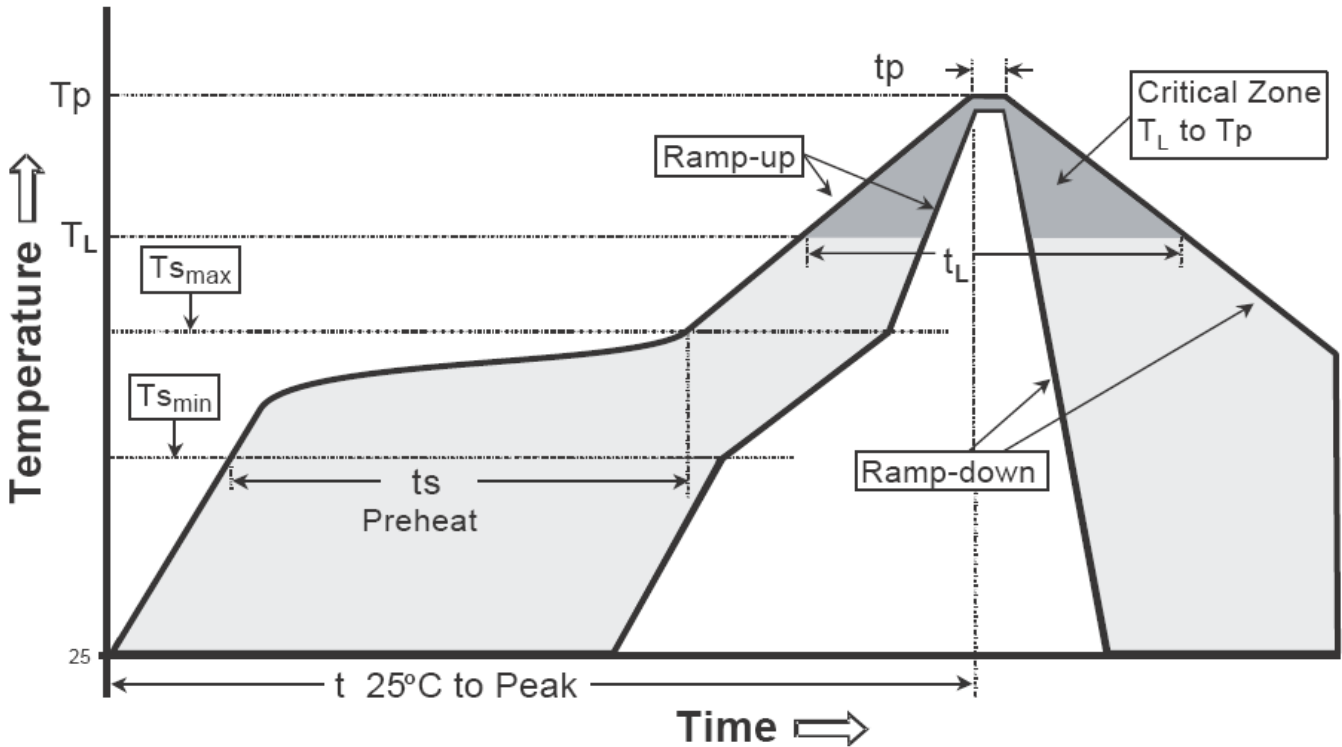
Carrier Tape Dimension



Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

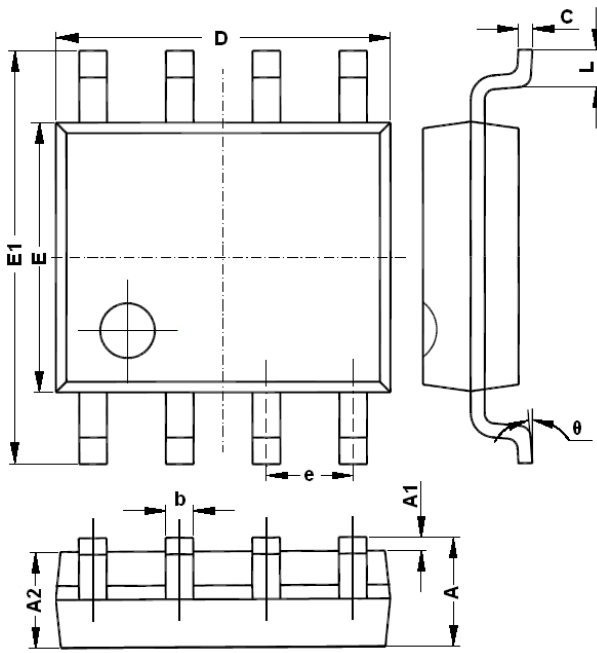
Recommended temperature profile for IR reflow



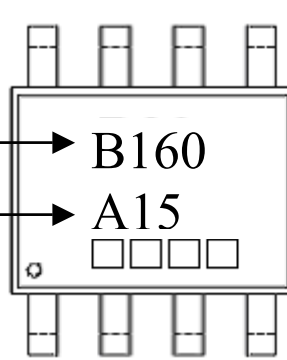
Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Tsmax to Tp)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(Ts min)	100°C	150°C
-Temperature Max(Ts max)	150°C	200°C
-Time(ts min to ts max)	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (TL)	183°C	217°C
- Time (tL)	60-150 seconds	60-150 seconds
Peak Temperature(TP)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note :1. All temperatures refer to topside of the package, measured on the package body surface.
 2.For devices mounted on FR-4 PCB of 1.6mm or equivalent grade PCB. If other grade PCB is used, care should be taken to match the coefficients of thermal expansion between components and PCB. If they are not matched well, the solder joints may crack or the bodies of the parts may crack or shatter as the assembly cools.

SOP-8 Dimension



Marking:



Device Name → **B160**

Date Code → **A15**

Date Code(counting from left to right) :

1st code: year code, the last digit of Christian year

2nd code : month code, Jan→A, Feb→B, Mar→C, Apr→D
 May→E, Jun→F, Jul→G, Aug→H, Sep→J,
 Oct→K, Nov→L, Dec→M

3rd and 4th codes : production serial number, 01~99

8-Lead SOP-8 Plastic Package
 CYStek Package Code: Q8

DIM	Millimeters		Inches		DIM	Millimeters		Inches	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069	E	3.800	4.000	0.150	0.157
A1	0.100	0.250	0.004	0.010	E1	5.800	6.200	0.228	0.244
A2	1.350	1.550	0.053	0.061	e	1.270	(BSC)	0.050	(BSC)
b	0.330	0.510	0.013	0.020	L	0.400	1.270	0.016	0.050
c	0.170	0.250	0.006	0.010	θ	0	8°	0	8°
D	4.700	5.100	0.185	0.200					

Notes: 1.Controlling dimension: millimeters.
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

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