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PHASE CONTROL THYRISTOR

AT906

Repetitive voltage up to **800 V**
Mean forward current **5597 A**
Surge current **95 kA**

FINAL SPECIFICATION

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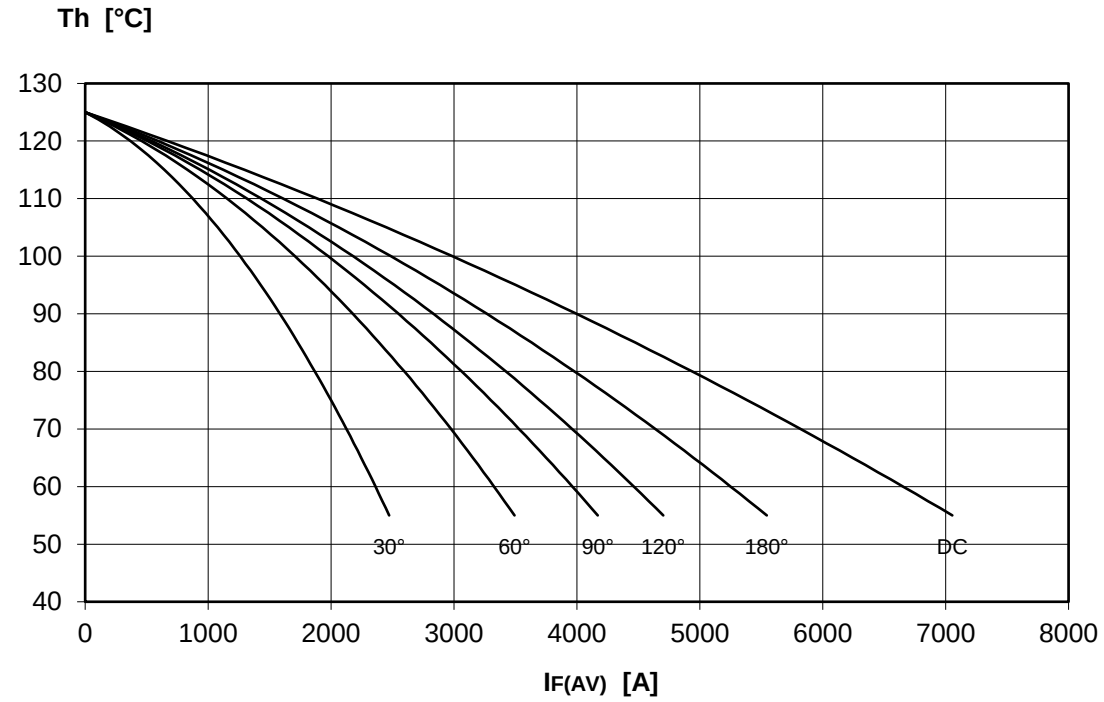
Symbol	Characteristic	Conditions	Tj [°C]	Value	Unit
BLOCKING					
V_{RRM}	Repetitive peak reverse voltage		125	800	V
V_{RSM}	Non-repetitive peak reverse voltage		125	900	V
V_{DRM}	Repetitive peak off-state voltage		125	800	V
I_{RRM}	Repetitive peak reverse current	V=VRRM	125	300	mA
I_{DRM}	Repetitive peak off-state current	V=VDRM	125	300	mA
CONDUCTING					
$I_{T(AV)}$	Mean forward current	180° sin, 50 Hz, Th=55°C, double side cooled		5597	A
$I_{T(AV)}$	Mean forward current	180° sin, 50 Hz, Tc=85°C, double side cooled		4303	A
I_{TSM}	Surge forward current	Sine wave, 10 ms	125	95	kA
I^2t	I^2t	without reverse voltage		45125 x 10^3	A^2s
V_T	On-state voltage	On-state current = 9000 A	25	1,26	V
$V_{T(TO)}$	Threshold voltage		125	0,85	V
r_T	On-state slope resistance		125	0,045	mohm
SWITCHING					
di/dt	Critical rate of rise of on-state current, min.	From 75% VDRM up to 4000A ; gate 10V, 5Ω	125	200	A/µs
dv/dt	Critical rate of rise of off-state voltage, min.	Linear ramp up to 70% of VDRM	125	1000	V/µs
t_d	Gate controlled delay time, typical	VD=100V; gate source 10V, 10Ω , tr=.5 µs	25		µs
t_q	Circuit commutated turn-off time, typical	dv/dt = 20 V/µs linear up to 75% VDRM		500	µs
Q_{rr}	Reverse recovery charge	di/dt = -20 A/µs, I= 4000 A	125		µC
I_{rr}	Peak reverse recovery current	VR= 50 V			A
I_H	Holding current, typical	VD=5V, gate open circuit	25	500	mA
I_L	Latching current, typical	VD=12V, tp=30µs	25	3000	mA
GATE					
V_{GT}	Gate trigger voltage	VD=12V	25	3,50	V
I_{GT}	Gate trigger current	VD=12V	25	400	mA
V_{GD}	Non-trigger gate voltage, min.	VD=VDRM	125	0,40	V
V_{FGM}	Peak gate voltage (forward)			30	V
I_{FGM}	Peak gate current			10	A
V_{RGM}	Peak gate voltage (reverse)			10	V
P_{GM}	Peak gate power dissipation	Pulse width 100 µs		150	W
P_G	Average gate power dissipation			3	W
MOUNTING					
$R_{th(j-h)}$	Thermal impedance, DC	Junction to heatsink, double side cooled		8,5	°C/kW
$R_{th(c-h)}$	Thermal impedance	Case to heatsink, double side cooled		1,5	°C/kW
T_j	Operating junction temperature			-30 / 125	°C
F	Mounting force			80.0 / 100.0	kN
	Mass			3000	g

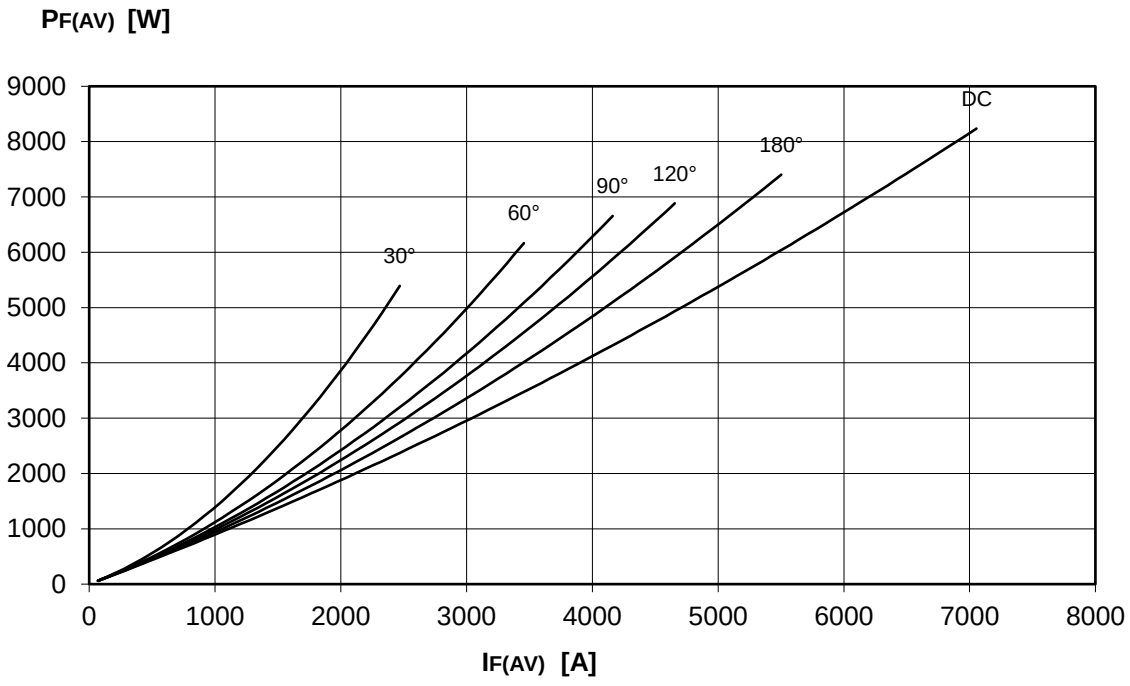
ORDERING INFORMATION : AT906 S 08

standard specification — VRRM/100

DISSIPATION CHARACTERISTICS

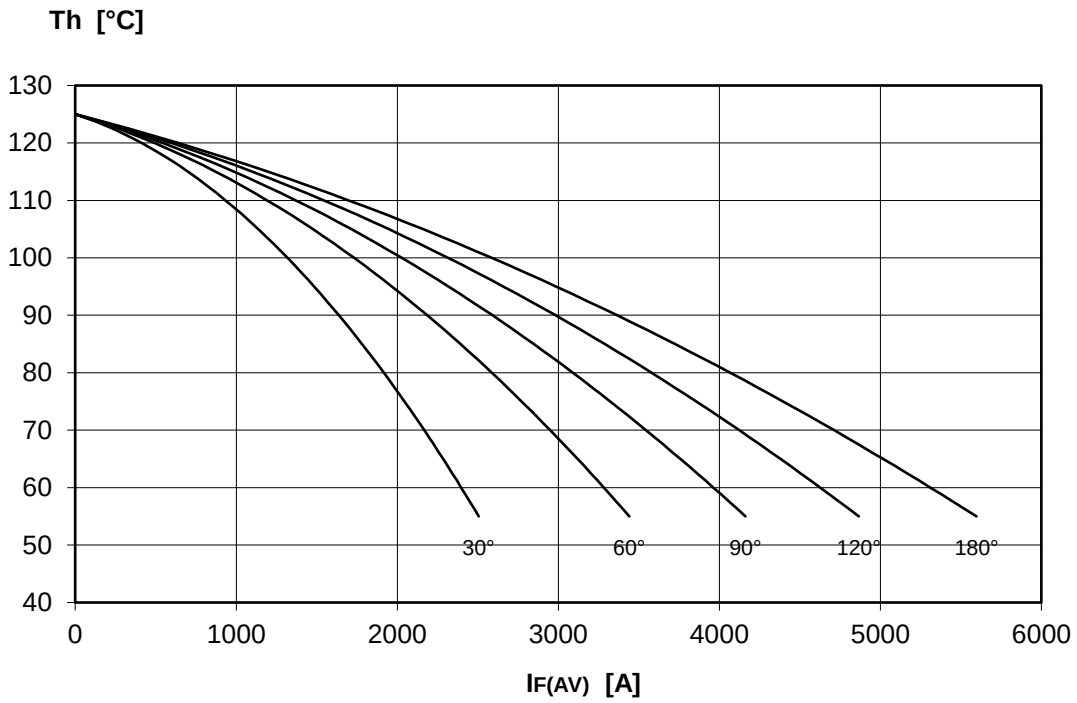
SQUARE WAVE

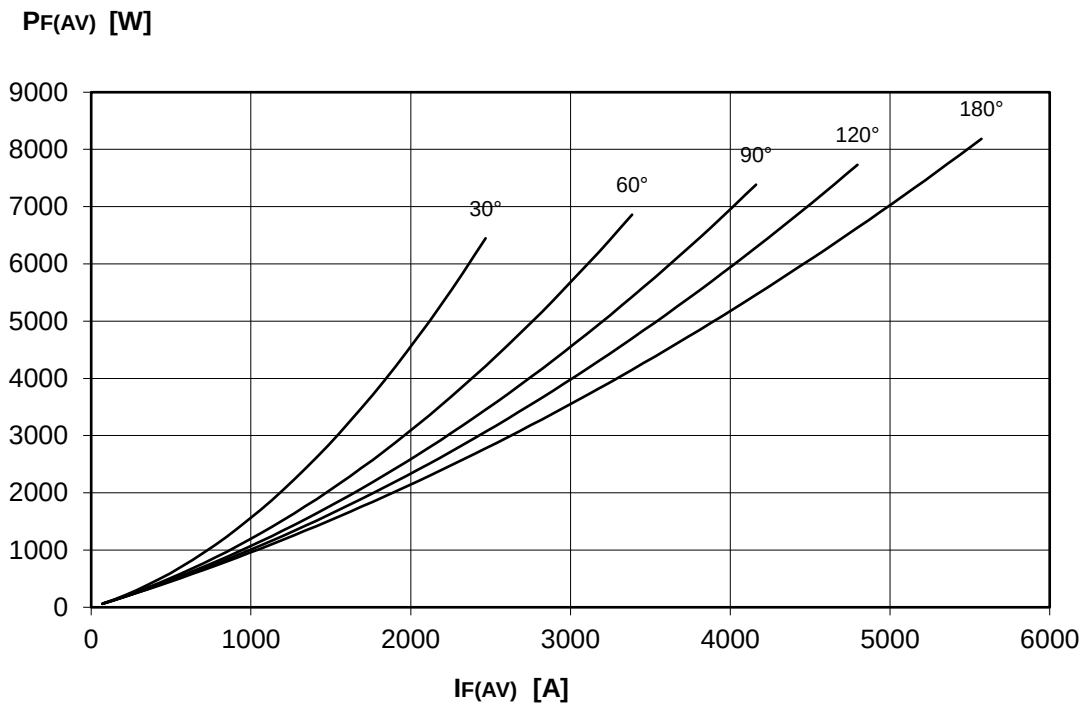




DISSIPATION CHARACTERISTICS

SINE WAVE



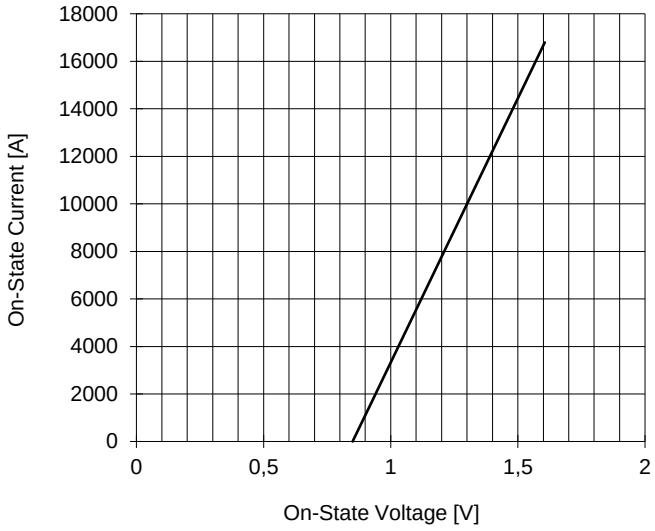


AT906 PHASE CONTROL THYRISTOR

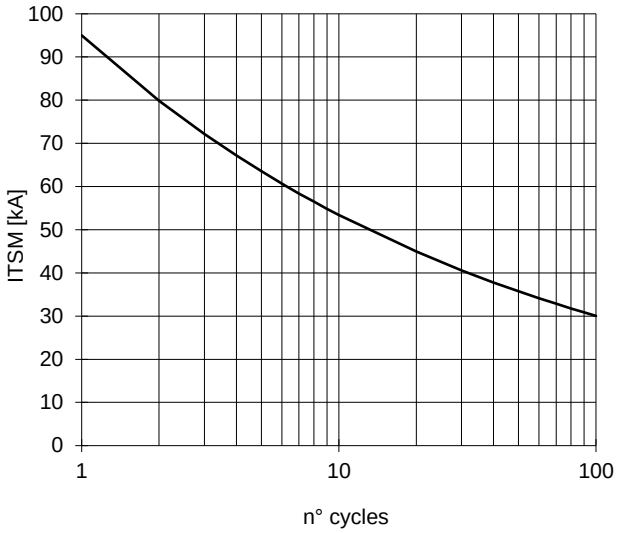
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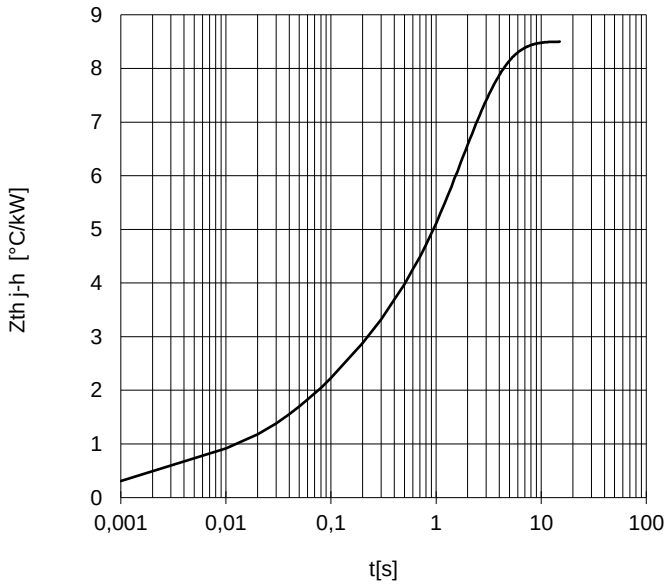
ON-STATE CHARACTERISTIC
Tj = 120 °C

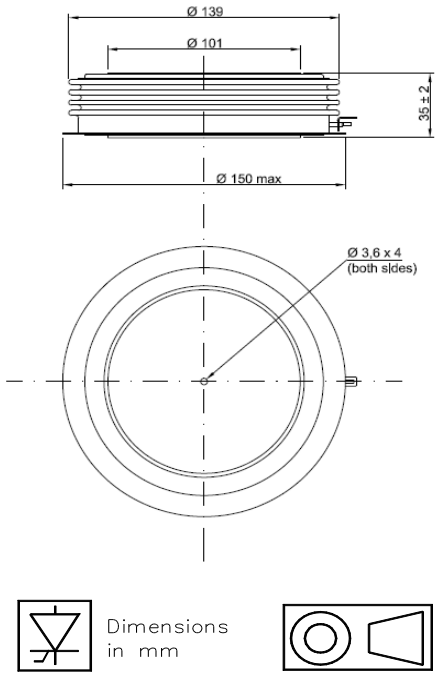


SURGE CHARACTERISTIC
Tj = 125 °C



TRANSIENT THERMAL IMPEDANCE
DOUBLE SIDE COOLED





Cathode terminal type DIN 46244 - A 4.8 - 0.8
Gate terminal type AMP 60598 - 1

All the characteristics given in this data sheet are guaranteed only with uniform clamping force, cleaned and lubricated heatsink, surfaces with flatness < .03 mm and roughness < 2 µm.
In the interest of product improvement POSEICO SpA reserves the right to change any data given in this data sheet at any time without previous notice.
If not stated otherwise the maximum value of ratings (simbols over shaded background) and characteristics is reported.

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