256-Bit Serial Nonvolatile CMOS Static RAM

FEATURES

- Single 5V Supply
- Infinite EEPROM to RAM Recall
- CMOS and TTL Compatible I/O
- Low CMOS Power Consumption:
  - –Active: 3mA Max.
  - –Standby: 30μA Max.
- Power Up/Down Protection
- 10 Year Data Retention
- JEDEC Standard Pinouts:
  - –8-lead DIP
  - –8-lead SOIC
- 100,000 Program/Erase Cycles (EEPROM)
- Auto Recall on Power-up
- Commercial, Industrial and Automotive Temperature Ranges

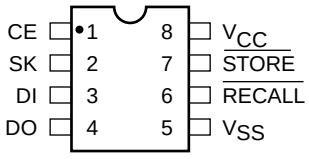
DESCRIPTION

The CAT24C44 Serial NVRAM is a 256-bit nonvolatile memory organized as 16 words x 16 bits. The high speed Static RAM array is bit for bit backed up by a nonvolatile EEPROM array which allows for easy transfer of data from RAM array to EEPROM (STORE) and from EEPROM to RAM (RECALL). STORE operations are completed in 10ms max. and RECALL operations typically within 1.5μs. The CAT24C44 features unlimited RAM write operations either through external RAM writes or internal recalls from EEPROM. Internal false store protection circuitry prohibits STORE operations when V_{CC} is less than 3.5V (typical) ensuring EEPROM data integrity.

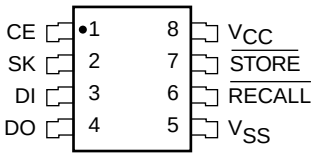
The CAT24C44 is manufactured using Catalyst's advanced CMOS floating gate technology. It is designed to endure 100,000 program/erase cycles (EEPROM) and has a data retention of 10 years. The device is available in JEDEC approved 8-lead plastic DIP and SOIC packages.

PIN CONFIGURATION

DIP Package (L)



SOIC Package (V)



PIN FUNCTIONS

Pin Name	Function
SK	Serial Clock
DI	Serial Input
DO	Serial Data Output
CE	Chip Enable
$\overline{\text{RECALL}}$	Recall
$\overline{\text{STORE}}$	Store
V_{CC}	+5V
V_{SS}	Ground

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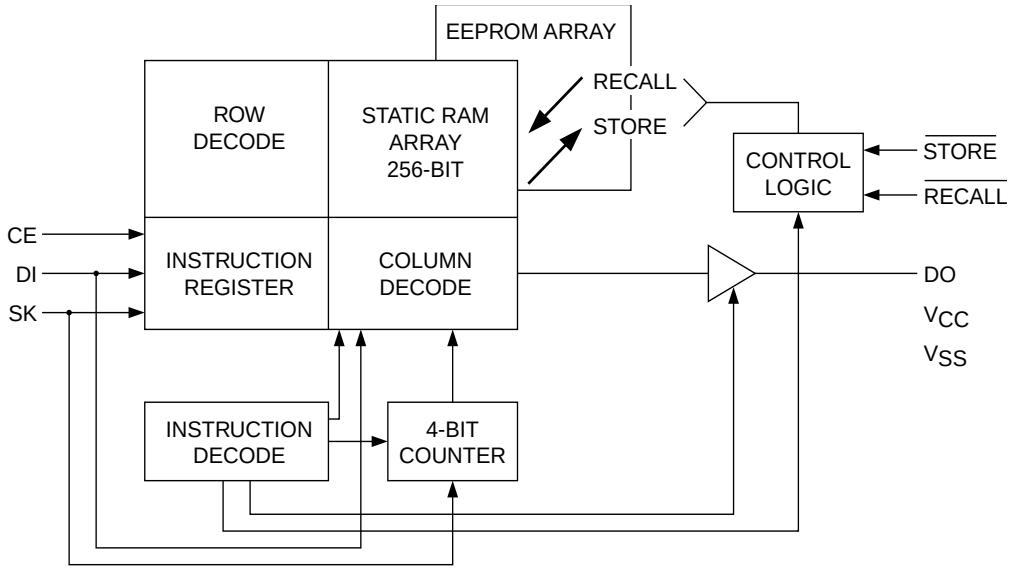
BLOCK DIAGRAM



MODE SELECTION(1)(2)

Mode	$\overline{STORE}$	$\overline{RECALL}$	Software Instruction	Write Enable Latch	Previous Recall Latch
Hardware Recall(3)	1	0	NOP	X	X
Software Recall	1	1	RCL	X	X
Hardware Store(3)	0	1	NOP	SET	TRUE
Software Store	1	1	STO	SET	TRUE

X = Don't Care

POWER-UP TIMING(4)

Symbol	Parameter	Min.	Max.	Units
VCCSR	V_{CC} Slew Rate	0.5	0.005	V/m
t_{pur}	Power-Up to Read Operations		200	µs
t_{puw}	Power-Up to Write or Store Operation		5	ms

Note:
(1) The store operation has priority over all the other operations.
(2) The store operation is inhibited when V_{CC} is below ≈ 3.5V.
(3) NOP designates that the device is not currently executing an instruction.
(4) This parameter is tested initially and after a design or process change that affects the parameter.

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ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... –55°C to +125°C

Storage Temperature ..... –65°C to +150°C

Voltage on Any Pin with Respect to Ground(2) ..... –2.0 to +VCC +2.0V

V_{CC} with Respect to Ground ..... –2.0V to +7.0V

Package Power Dissipation Capability (Ta = 25°C) 1.0W

Lead Soldering Temperature (10 secs) ..... 300°C

Output Short Circuit Current(3) ..... 100 mA

*COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Typ.	Max.	Units
N_{END}(1)	Endurance	100,000			Cycles/Byte
T_{DR}(1)	Data Retention	10			Years
V_{ZAP}(1)	ESD Susceptibility	2000			Volts
I_{LTH}(1)(4)	Latch-up	100			mA

D.C. OPERATING CHARACTERISTICS

V_{CC} = 5V ±10%, unless otherwise specified.

Symbol	Parameter	Limits			Unit	Conditions
		Min.	Typ.	Max.		
I_{CCO}	Current Consumption (Operating)			3	mA	Inputs = 5.5V, T_A = 0°C All Outputs Unloaded
I_{SB}	Current Consumption (Standby)			30	µA	CE = V_{IL}
I_{LI}	Input Current			2	µA	$0 \le V_{IN} \le 5.5V$
I_{LO}	Output Leakage Current			10	µA	$0 \le V_{OUT} \le 5.5V$
V_{IH}	High Level Input Voltage	2		V_{CC}	V	
V_{IL}	Low Level Input Voltage	0		0.8	V	
V_{OH}	High Level Output Voltage	2.4			V	I_{OH} = –2mA
V_{OL}	Low Level Output Voltage			0.4	V	I_{OL} = 4.2mA

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Parameter	Max.	Unit	Conditions
$C_{I/O}$(1)	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(1)	Input Capacitance	6	pF	V_{IN} = 0V

Note:

(1) These parameter are tested initially and after a design or process change that affects the parameter according to appropriate AEC-Q100 and JEDEC test methods.

(2) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} +2.0V for periods of less than 20 ns.

(3) Output shorted for no more than one second. No more than one output shorted at a time.

(4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1V to V_{CC} +1V.

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A.C. CHARACTERISTICS

V_{CC} = 5V ±10%, unless otherwise specified.

Symbol	Parameter	Min.	Max.	Units	Conditions
F_{SK}	SK Frequency	DC	1	MHz	
t_{SKH}	SK Positive Pulse Width	400		ns	
t_{SKL}	SK Negative Pulse Width	400		ns	C_L = 100pF + 1TTL gate
t_{DS}	Data Setup Time	400		ns	V_{OH} = 2.2V, V_{OL} = 0.65V
t_{DH}	Data Hold Time	80		ns	V_{IH} = 2.2V, V_{IL} = 0.65V
t_{PD}	SK Data Valid Time		375	ns	Input rise and fall times = 10ns
t_Z	CE Disable Time		1	µs	
t_{CES}	CE Enable Setup Time	800		ns	
t_{CEH}	CE Enable Hold Time	400		ns	
t_{CDS}	CE De-Select Time	800		ns	

A.C. CHARACTERISTICS, Store Cycle

V_{CC} = 5V ±10%, unless otherwise specified.

Symbol	Parameter	Limits		Units	Conditions
		Min.	Max.		
t_{ST}	Store Time		10	ms	C_L = 100pF + 1TTL gate
t_{STP}	Store Pulse Width	200		ns	V_{OH} = 2.2V, V_{OL} = 0.65V
t_{STZ}	Store Disable Time		100	ns	V_{IH} = 2.2V, V_{IL} = 0.65V

A.C. CHARACTERISTICS, Recall Cycle

V_{CC} = 5V ±10%, unless otherwise specified.

Symbol	Parameter	Min.	Max.	Units	Conditions
t_{RCC}	Recall Cycle Time	2.5		µs	
t_{RCP}	Recall Pulse Width	500		ns	C_L = 100pF + 1TTL gate
t_{RCZ}	Recall Disable Time		500	ns	V_{OH} = 2.2V, V_{OL} = 0.65V
t_{ORC}	Recall Enable Time	10		ns	V_{IH} = 2.2V, V_{IL} = 0.65V
t_{ARC}	Recall Data Access Time		1.5	µs	

INSTRUCTION SET

Instruction	Format			Operation
	Start Bit	Address	OP Code	
WRDS	1	XXXX	0 0 0	Reset Write Enable Latch (Disables, Writes and Stores)
STO	1	XXXX	0 0 1	Store RAM Data in EEPROM
WRITE	1	AAAA	0 1 1	Write Data into RAM Address AAAA
WREN	1	XXXX	1 0 0	Set Write Enable Latch (Enables, Writes and Stores)
RCL	1	XXXX	1 0 1	Recall EEPROM Data into RAM
READ	1	AAAA	1 1 X	Read Data From RAM Address AAAA

X = Don't care
A = Address bit

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DEVICE OPERATION

The CAT24C44 is intended for use with standard microprocessors. The CAT24C44 is organized as 16 registers by 16 bits. Seven 8-bit instructions control the device's operating modes, the RAM reading and writing, and the EEPROM storing and recalling. It is also possible to control the EEPROM store and recall functions in hardware with the $\overline{\text{STORE}}$ and $\overline{\text{RECALL}}$ pins. The CAT24C44 operates on a single 5V supply and will generate, on chip, the high voltage required during a RAM to EEPROM storing operation.

Instructions, addresses and write data are clocked into the DI pin on the rising edge of the clock (SK). The DO pin remains in a high impedance state except when outputting data from the device. The $\overline{\text{CE}}$ (Chip Enable) pin must remain high during the entire data transfer.

The format for all instructions sent to the CAT24C44 is a logical '1' start bit, 4 address bits (data read or write operations) or 4 "Don't Care" bits (device mode operations), and a 3-bit op code (see Instruction Set). For data write operations, the 8-bit instruction is followed by 16 bits of data. For data read instructions, DO will come out of the high impedance state and enable 16 bits of data to be clocked from the device. The 8th bit of the read instruction is a "Don't Care" bit. This is to eliminate any bus contention that would occur in applications where the DI and DO pins are tied together to form a common DI/DO line. A word of caution while clocking data to and from the device: If the $\overline{\text{CE}}$ pin is prematurely deselected while shifting in an instruction, that instruction will not be executed, and the shift register internal to the CAT24C44 will be cleared. If there are more than or less than 16 clocks during a memory data transfer, an improper data transfer will result. The SK clock is completely static allowing the user to stop the clock and restart it to resume shifting of data.

Read

Upon receiving a start bit, 4 address bits, and the 3-bit read command (clocked into the DI pin), the DO pin of the CAT24C44 will come out of the high impedance state and the 16 bits of data, located at the address specified in the instructions, will be clocked out of the device. When clocking data from the device, the first bit clocked out (DO) is timed from the falling edge of the 8th clock, all succeeding bits (D1–D15) are timed from the rising edge of the clock.

Write

After receiving a start bit, 4 address bits, and the 3-bit WRITE command, the 16-bit word is clocked into the device for storage into the RAM memory location specified. The $\overline{\text{CE}}$ pin must remain high during the entire write operation.

Figure 1. RAM Read Cycle Timing

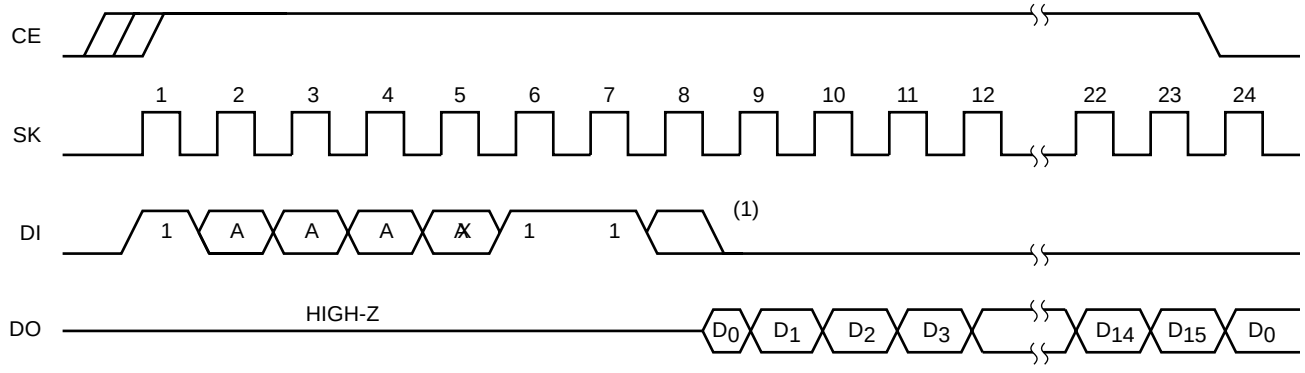
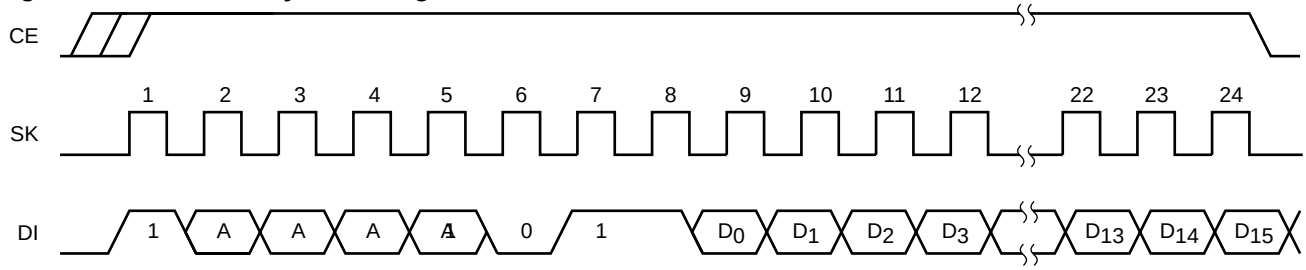


Figure 2. RAM Write Cycle Timing



Note:
(1) Bit 8 of READ instruction is "Don't Care".

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WREN/WRDS

The CAT24C44 powers up in the program disable state (the "write enable latch" is reset). Any programming after power-up or after a WRDS (RAM write/EEPROM store disable) instruction must first be preceded by the WREN (RAM write/EEPROM store enable) instruction. Once writing/storing is enabled, it will remain enabled until power to the device is removed, the WRDS instruction is sent, or an EEPROM store has been executed (STO).

The WRDS (write/store disable) can be used to disable all CAT24C44 programming functions, and will prevent any accidental writing to the RAM, or storing to the EEPROM.

Data can be read normally from the CAT24C44 regardless of the "write enable latch" status.

Figure 3. Read Cycle Timing

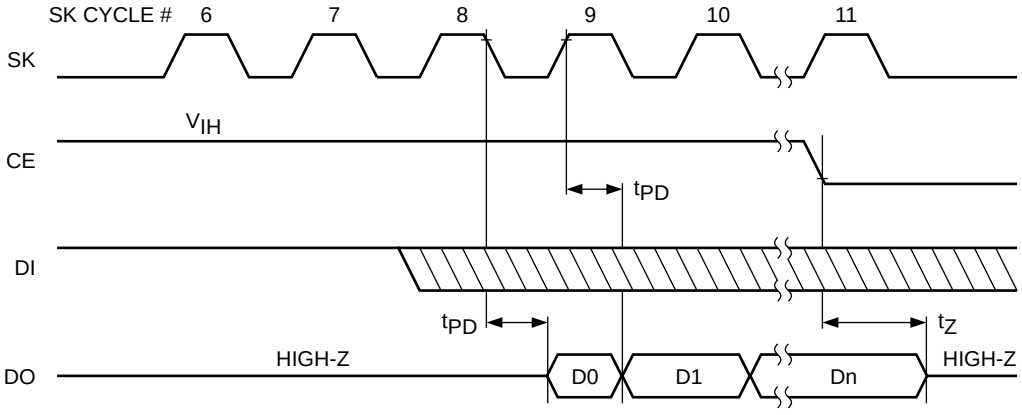
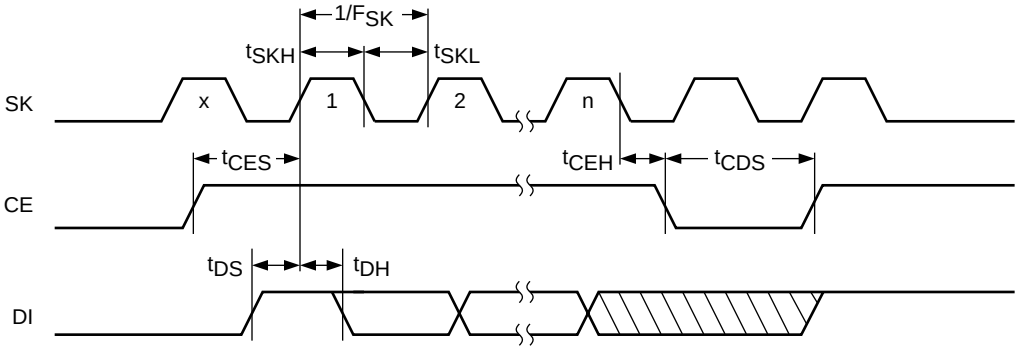


Figure 4. Write Cycle Timing



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RCL/$\overline{\text{RECALL}}$

Data is transferred from the EEPROM data memory to RAM by either sending the RCL instruction or by pulling the $\overline{\text{RECALL}}$ input pin low. A recall operation must be performed before the EEPROM store, or RAM write operations can be executed. Either a hardware or software recall operation will set the “previous recall” latch internal to the CAT24C44.

POWER-ON RECALL

The CAT24C44 has a power-on recall function that transfers the EEPROM data to the RAM. After Power-up, all functions are inhibited for at least 200ns (T_{pur}) from stable V_{cc}.

STO/$\overline{\text{STORE}}$

Data in the RAM memory area is stored in the EEPROM memory either by sending the STO instruction or by pulling the $\overline{\text{STORE}}$ input pin low. As security against any inadvertent store operations, the following conditions must each be met before data can be transferred into nonvolatile storage:

- The “previous recall” latch must be set (either a software or hardware recall operation).
- The “write enable” latch must be set (WREN instruction issued).
- STO instruction issued or $\overline{\text{STORE}}$ input low.

During the store operation, all other CAT24C44 functions are inhibited. Upon completion of the store operation, the “write enable” latch is reset. The device also provides false store protection whenever V_{CC} falls below a 3.5V level. If V_{CC} falls below this level, the store operation is disabled and the “write enable” latch is reset.

Figure 5. Recall Cycle Timing

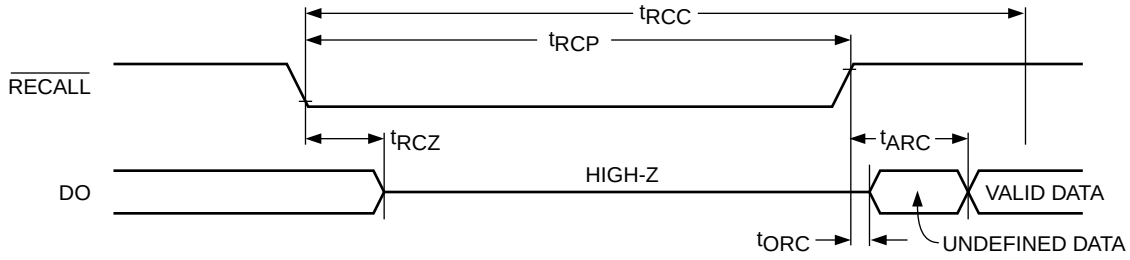

Figure 6. Hardware Store Cycle Timing

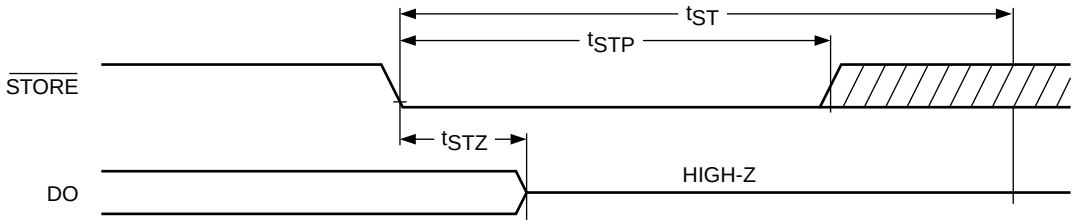

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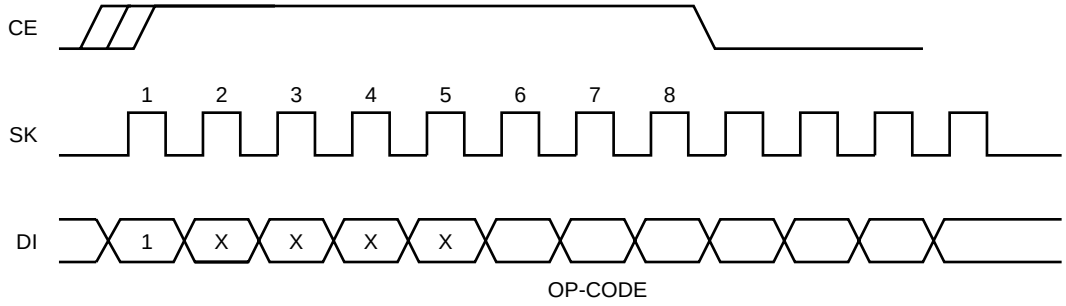
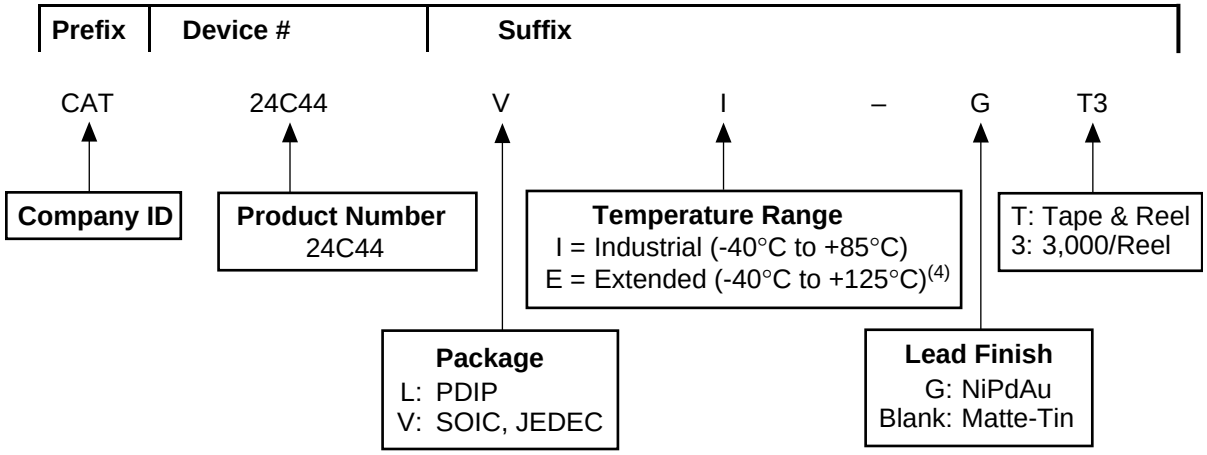
Figure 7. Non-Data Operations



ORDERING INFORMATION



Notes:
(1) All packages are RoHS-compliant (Lead-free, Halogen-free).
(2) The device used in the above example is a CAT24C44VI-GT3 (SOIC, Industrial Temperature, NiPdAu, Tape & Reel, 3,000/Reel).
(3) For additional package option please contact your nearest ON Semiconductor Sales office.
(4) Extended Temperature available upon request.

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REVISION HISTORY

Date	Revision	Description
17-Apr-04	O	Add Lead Free Logo Update Features Update Pin Configuration Update Block Diagram Update Instruction Set Update Device Operation Update Ordering Information Add Revision History Update Rev Number
16-Nov-04	P	Update Pin Configuration Update Ordering Information
17-Apr-04	Q	Update Ordering Information
03-Aug-05	R	Update Pin Configuration Update Reliability Characteristics Update Ordering Information
24-Jun-08	S	Update Pin Configuration Update Example of Ordering Information
04-Dec-08	T	Change logo and fine print to ON Semiconductor

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