

IS31FL3216

16 CHANNELS LED DRIVER

January 2012

GENERAL DESCRIPTION

The IS31FL3216 is a fun light LED controller with an audio modulation mode. It can store data of 8 frames with internal RAM to play small animations automatically.

IS31FL3216 can sample the input signal to modulate the intensity of LEDs, or control 8 frames playing by internal ADC block.

The LED current of each channel can be set in 256 steps by adjusting the PWM duty cycle through an I2C interface. 8 channels can be used as GPIO ports. IS31FL3216 is available in QFN-28 (4mm × 4mm). It operates from 2.7V to 5.5V over the temperature range of -40°C to +85°C.

APPLICATIONS

- Mobile phones and other hand-held devices for LED display
- LED in home appliances

FEATURES

- 2.7V to 5.5V supply
- I2C interface, automatic address increment function
- Internal RAM
- Modulate LED brightness with 256 steps PWM
- Each channel can be controlled independently
- Auto Frame Play Mode with 8 frames
- 8 frames memory for animations
- Audio Frame Mode with 8 frames
- 8 of 16 outputs not used as LED drivers can be used as GPIO ports
- 8 levels of maximum intensity control
- 8kV HBM ESD
- Over-temperature protection
- -40°C to +85°C temperature range
- QFN-28 (4mm × 4mm) package

TYPICAL APPLICATION CIRCUIT

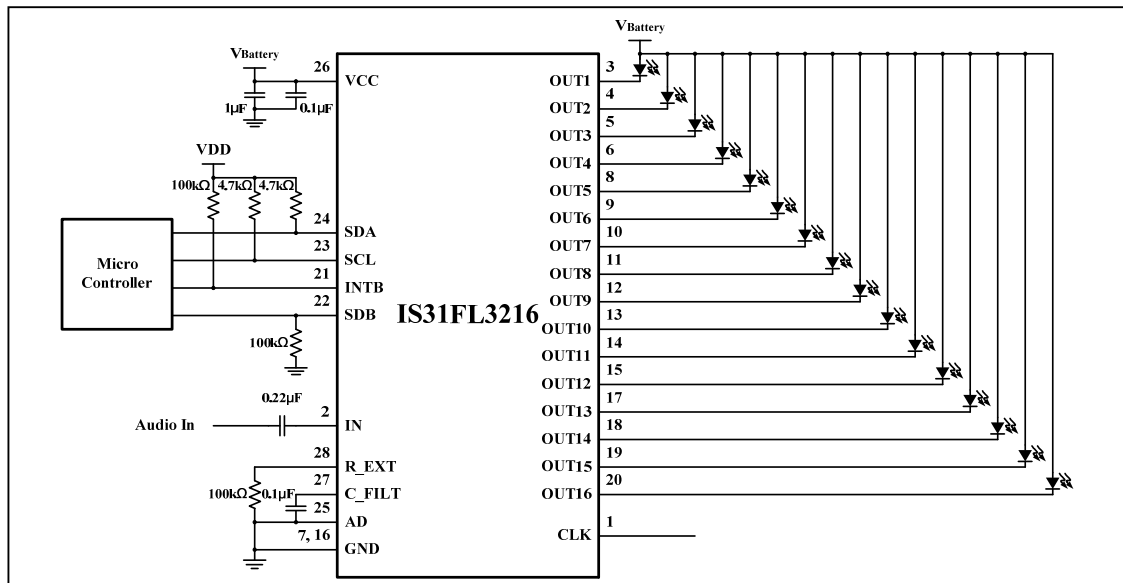


Figure 1 Typical Application Circuit

Note: The IC should be placed far away from the mobile antenna in order to prevent the EMI.

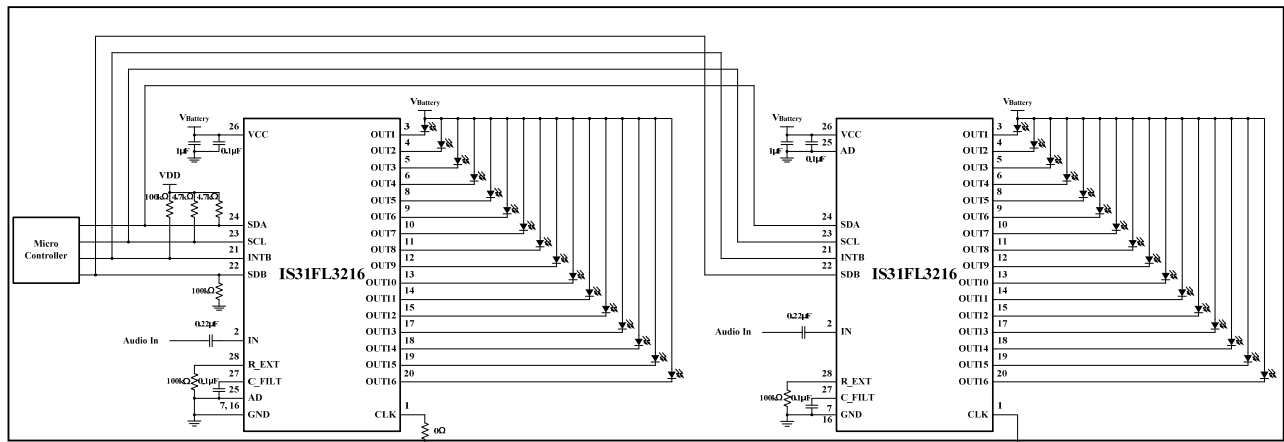
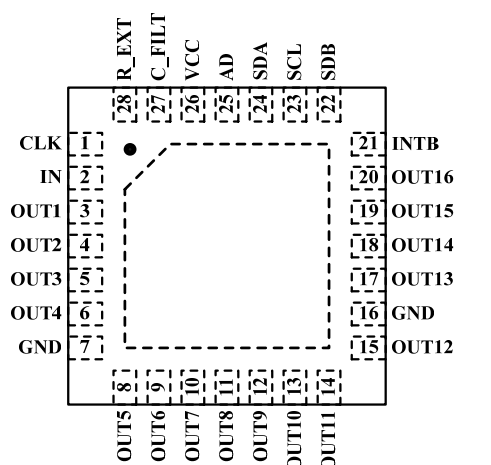


Figure 2 Typical Application Circuit (Cascade Mode)

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PIN CONFIGURATION

Package	Pin Configuration (Top View)
QFN-28	 <p>The diagram shows a top view of a QFN-28 package with 28 pins. The pins are arranged in a square pattern. Pin 1 (CLK) is at the top-left corner. Pin 2 (IN) is at the top-left edge. Pins 3-6 (OUT1-OUT4) are along the left edge. Pin 7 (GND) is at the bottom-left corner. Pins 8-15 (OUT5-OUT12) are along the bottom edge. Pins 16 (GND) and 15 (OUT12) are at the bottom-right corner. Pins 17-20 (OUT13-OUT16) are along the right edge. Pin 21 (INTB) is at the top-right corner. Pins 22 (SDB), 23 (SCL), 24 (SDA), 25 (AD), 26 (VCC), 27 (C_FILT), and 28 (R_EXT) are along the top edge. A thermal pad is located at the top-left corner, between pins 1 and 2.</p>

PIN DESCRIPTION

No.	Pin	Description
1	CLK	Clock for chip cascade.
2	IN	Audio signal input.
3 ~ 6	OUT1 ~ OUT4	Output channel for LEDs.
7,16	GND	Ground.
8 ~ 15	OUT5 ~ OUT12	Output channel.
17 ~ 20	OUT13 ~ OUT16	Output channel.
21	INTB	Interrupt output, active low.
22	SDB	Shutdown, pull to GND in the shutdown mode.
23	SCL	Serial clock input.
24	SDA	Serial data input.
25	AD	I2C address pin.
26	VCC	Power supply.
27	C_FILT	Filter capacitor for audio control.
28	R_EXT	External resistor to regulate the output current.
	Thermal Pad	Connect to GND.

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- the risk of injury or damage has been minimized;
- the user assume all such risks; and
- potential liability of Integrated Silicon Solution, Inc is adequately protected under the circumstances



IS31FL3216

ORDERING INFORMATION

Industrial Range: -40°C to +85°C

Order Part No.	Package	QTY/Reel
IS31FL3216-QFLS2-TR	QFN-28, Lead-free	2500



IS31FL3216

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	-0.3V ~ +6.0V
Voltage at any input pin	-0.3V ~ $V_{CC}+0.3V$
Current in GND terminal	1A
Maximum junction temperature, T_{JMAX}	150°C
Storage temperature range, T_{STG}	-65°C ~ +150°C
Operating temperature range, T_A	-40°C ~ +85°C
ESD (HBM)	8kV

Note:

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

$T_A = 25^\circ\text{C}$, $V_{CC} = 2.7V \sim 5.5V$, unless otherwise noted. Typical values are $T_A = 25^\circ\text{C}$, $V_{CC} = 3.6V$.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage		2.7		5.5	V
I_{CC}	Quiescent power supply current	$V_{SDB} = V_{CC}$		5.2		mA
I_{SD}	Shutdown current	$V_{SDB} = 0V$ or software shutdown		1		μA
I_{OUT}	Average output current	PWM Control Mode, $V_{DS} = 0.6V$ PWM duty cycle = 0xFF		20 (Note 1)		mA
		Audio Frame Mode, $V_{DS} = 0.6V$ $V_{IN} = 3V_{p-p}$, 1kHz square wave Audio gain = 0dB		20 (Note 1)		
V_{HR}	Current sink headroom voltage (when use as GPIO output ports)	$I_{OUT} = 20\text{mA}$		400		mV
Logic Electrical Characteristics (SDB, SDA, SCL, AD, INTB)						
V_{IL}	Logic "0" input voltage	$V_{CC} = 2.7V$			0.4	V
V_{IH}	Logic "1" input voltage	$V_{CC} = 5.5V$	1.4			V
I_{IL}	Logic "0" input current	$V_{IN} = 0V$		5 (Note 2,3)		nA
I_{IH}	Logic "1" input current	$V_{IN} = V_{CC}$		5 (Note 2,3)		nA



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DIGITAL INPUT SWITCHING CHARACTERISTICS (Note 3)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
f_{SCL}	Serial-Clock frequency				400	kHz
t_{BUF}	Bus free time between a STOP and a START condition		1.3			μ s
$t_{HD, STA}$	Hold time (repeated) START condition		0.6			μ s
$t_{SU, STA}$	Repeated START condition setup time		0.6			μ s
$t_{SU, STO}$	STOP condition setup time		0.6			μ s
$t_{HD, DAT}$	Data hold time				0.9	μ s
$t_{SU, DAT}$	Data setup time		100			ns
t_{LOW}	SCL clock low period		1.3			μ s
t_{HIGH}	SCL clock high period		0.7			μ s
t_R	Rise time of both SDA and SCL signals, receiving	(Note 4)		20+0.1Cb	300	ns
t_F	Fall time of both SDA and SCL signals, receiving	(Note 4)		20+0.1Cb	300	ns

Note 1: The average output current of each channel is IOUT.

Note 2: All LEDs are on.

Note 3: Guaranteed by design.

Note 4: Cb = total capacitance of one bus line in pF. ISINK \leq 6mA. tR and tF measured between $0.3 \times V_{CC}$ and $0.7 \times V_{CC}$.

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DETAILED DESCRIPTION

I2C INTERFACE

The IS31FL3216 uses a serial bus, which conforms to the I2C protocol, to control the chip's functions with two wires: SCL and SDA. The IS31FL3216 has a 7-bit slave address (A7:A1), followed by the R/W bit, A0. Set A0 to "0" for a write command and set A0 to "1" for a read command. The value of bits A1 and A2 are decided by the connection of the AD pin.

The complete slave address is:

Table 1 Slave Address

Bit	A7:A3	A2:A1	A0
Value	11101	AD	1/0

AD connected to GND, AD = 00;
 AD connected to VCC, AD = 11;
 AD connected to SCL, AD = 01;
 AD connected to SDA, AD = 10;

The SCL line is uni-directional. The SDA line is bi-directional (open-collector) with a pull-up resistor (typically 4.7kΩ). The maximum clock frequency specified by the I2C standard is 400kHz. In this discussion, the master is the microcontroller and the slave is the IS31FL3216.

The timing diagram for the I2C is shown in Figure 5. The SDA is latched in on the stable high level of the SCL. When there is no interface activity, the SDA line should be held high.

The "START" signal is generated by lowering the SDA signal while the SCL signal is high. The start signal will alert all devices attached to the I2C bus to check the incoming address against their own chip address.

The 8-bit chip address is sent next, most significant bit first. Each address bit must be stable while the SCL level is high.

After the last bit of the chip address is sent, the master checks for the IS31FL3216's acknowledge. The master releases the SDA line high (through a pull-up resistor).

Then the master sends an SCL pulse. If the IS31FL3216 has received the address correctly, then it holds the SDA line low during the SCL pulse. If the SDA line is not low, then the master should send a "STOP" signal (discussed later) and abort the transfer.

Following acknowledge of IS31FL3216, the register address byte is sent, most significant bit first. IS31FL3216 must generate another acknowledge indicating that the register address has been received.

Then 8-bit of data byte are sent next, most significant bit first. Each data bit should be valid while the SCL level is stable high. After the data byte is sent, the IS31FL3216 must generate another acknowledge to indicate that the data was received.

The "STOP" signal ends the transfer. To signal "STOP", the SDA signal goes high while the SCL signal is high.

ADDRESS AUTO INCREMENT

To write multiple bytes of data into IS31FL3216, load the address of the data register that the first data byte is intended for. During the IS31FL3216 acknowledge of receiving the data byte, the internal address pointer will increment by one. The next data byte sent to IS31FL3216 will be placed in the new address, and so on. The auto increment of the address will continue as long as data continues to be written to IS31FL3216 (Figure 6).

READING PORT REGISTERS

To read the device data, the bus master must first send the IS31FL3216 address with the R/W bit set to "0", followed by the command byte, which determines which register is accessed. After a restart, the bus master must then send the IS31FL3216 address with the R/W bit set to "1". Data from the register defined by the command byte is then sent from the IS31FL3216 to the master (Figure 7).

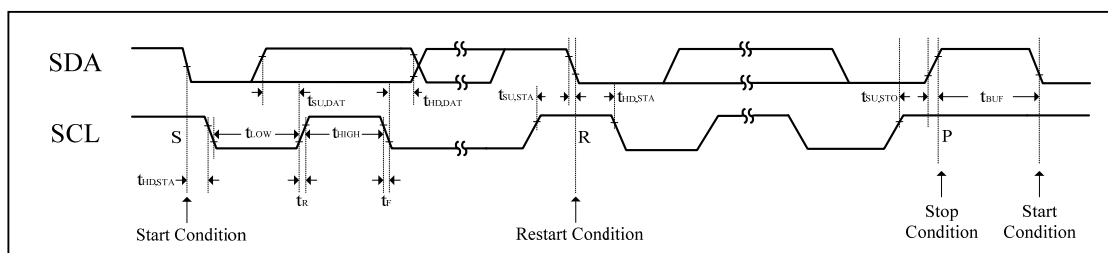


Figure 3 Interface timing

IS31FL3216

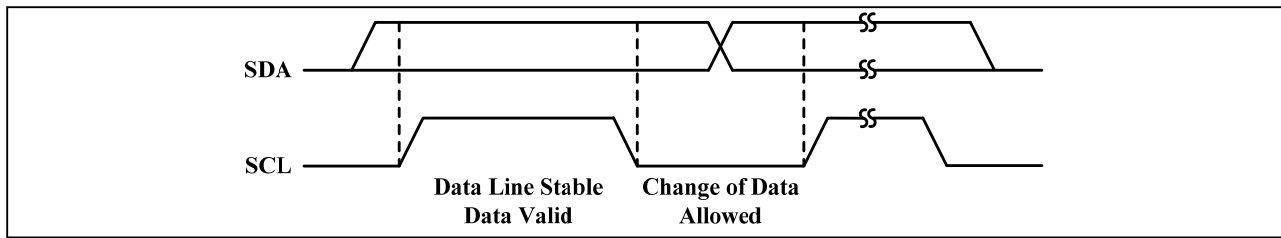


Figure 4 Bit transfer

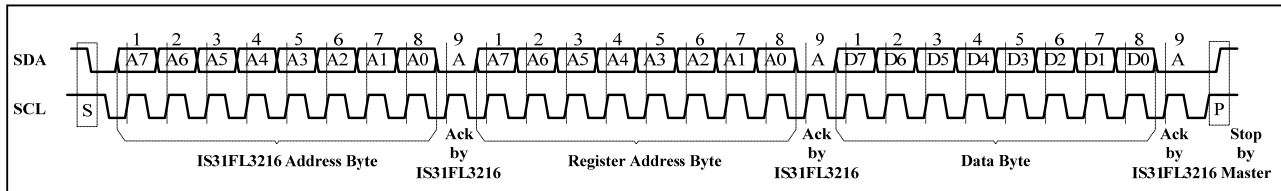


Figure 5 Writing to IS31FL3216(Typical)

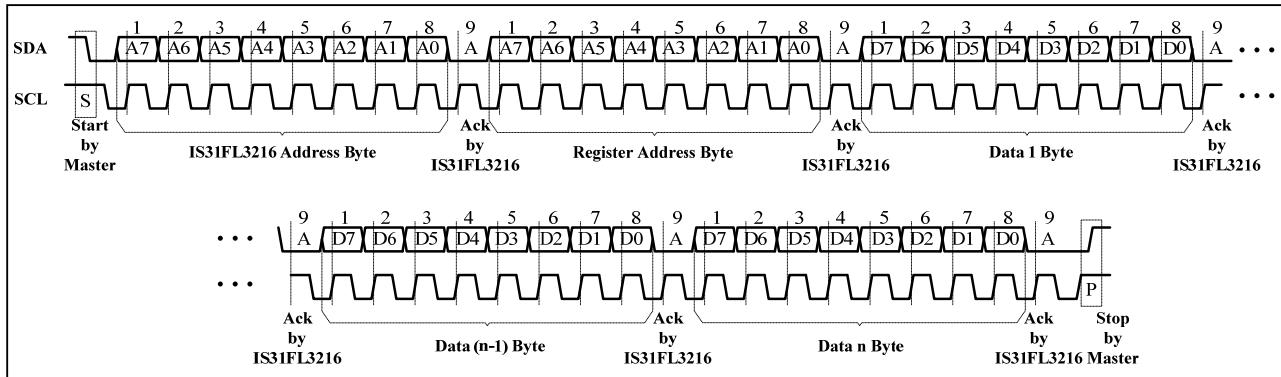


Figure 6 Writing to IS31FL3216(Automatic Address Increment)

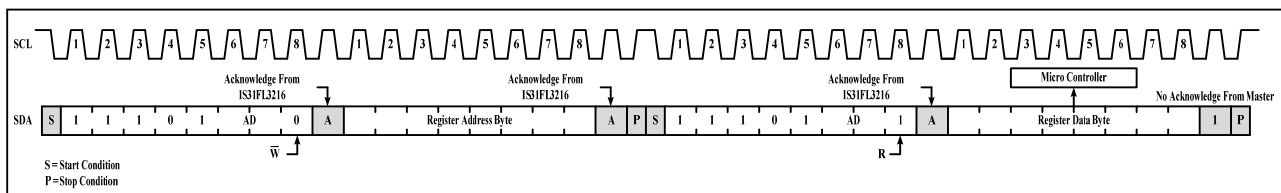


Figure 7 Reading from IS31FL3216



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REGISTER DEFINITION

Table 2 Register Function

Address	Name	Function	Table	R/W	Default
00h	Configuration Register	Set the operating mode of IS31FL3216	3	W	1000 0000
01h	LED Control Register	OUT9~OUT16 enable bit	4	W	1111 1111
02h		OUT1~OUT8 enable bit	5	W	
03h	Lighting Effect Register	Set the output current and the audio gain	6	W	0000 0000
04h	Channel Configuration Register	Set the operating mode of OUT9~OUT16	7	W	
05h	GPIO Configuration Register	Set the operating mode of OUT9~OUT16 as the GPIO port	8	W	
06h	Output Port Register	Set the logic level of OUT9~OUT16 as the output port	9	W	
07h	Interrupt Control Register	Set the interrupt function of OUT9~OUT16	10	W	
08h	State Register	Store the state of OUT9~OUT16 as the input port	11	R	
09h	ADC Sample Rate Register	Set the ADC sample rate of the input signal	12	W	0000 0000
10h~1Fh	PWM Register	Set the PWM duty cycle data	13	W	-
20h~AFh	Frame Register	Store the data of 8 frames	14	W	
B0h	Update Register	Load PWM Register data	-	W	xxxx xxxx
B6h	Frame Delay Register	Set the delay time between each frame	15	W	0000 0000
B7h	Frame Start Register	Set the start frame in Auto Frame Play Mode	16	W	

Table 3 00h Configuration Register

Bit	D7	D6:D5	D4	D3:D0
Name	SSD	MODE	AE	-
Default	1	00	0	0000

The Configuration Register sets the operating mode of IS31FL3216.

SSD Software Shutdown Enable
 0 Software shutdown mode
 1 Normal operation

MODE Operation Mode Selection
 00 PWM Control Mode
 01 Auto Frame Play Mode
 10 Audio Frame Mode

AE Audio Modulated Enable
 0 Output current is set by register
 1 Output current is modulated by audio signal

Table 4 01h LED Control Register(OUT9~OUT16)

Bit	D7:D0
Name	OUT16:OUT9
Default	1111 1111

Table 5 02h LED Control Register(OUT1~OUT8)

Bit	D7:D0
Name	OUT8:OUT1
Default	1111 1111

The LED Control Registers store the on or off state of each channel.

OUTx LED State
 0 LED off
 1 LED on

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Table 6 03h Lighting Effect Register

Bit	D7	D6:D4	D3	D2:D0
Name	CM	CS	AGCE	AGS
Default	0	000	0	000

The Lighting Effect Register sets the output current and the audio gain.

CM Chip Cascade Mode
 0 Master Mode
 1 Slave Mode

CS Output Current Selection
 000 20mA
 001 15mA
 010 10mA
 011 5mA
 100 40mA
 101 35mA
 110 30mA
 111 25mA

AGCE AGC Enable
 0 Enable
 1 Disable

AGS Audio Gain Selection
 000 0dB
 001 3dB
 010 6dB
 011 9dB
 100 12dB
 101 15dB
 110 18dB
 111 21dB

Table 7 04h Channel Configuration Register (OUT9~OUT16)

Bit	D7:D0
Name	OUT16:OUT9
Default	0000 0000

Configure the operating mode of OUT9~OUT16. If any port is set as GPIO, the Lighting Effect Register will be unavailable for the port.

OUTx Channel Configuration
 0 LED output
 1 GPIO port

Table 8 05h GPIO Configuration Register (OUT9~OUT16)

Bit	D7:D0
Name	OUT16:OUT9
Default	0000 0000

Set the state of OUT9~OUT16 as the GPIO port.

OUTx GPIO Configuration
 0 Output port
 1 Input port

Table 9 06h Output Configuration Register (OUT9~OUT16)

Bit	D7:D0
Name	OUT16:OUT9
Default	1111 1111

Set the logic level of OUT9~OUT16 as the output port.

OUTx Output State
 0 Output low
 1 Output high

Table 10 07h Interrupt Control Register (OUT9~OUT16)

Bit	D7:D0
Name	OUT16:OUT9
Default	0000 0000

Set the interrupt function of OUT9~OUT16 as the input port.

OUTx Interrupt Function Enable
 0 Enable
 1 Disable

Table 11 08h State Register (OUT9~OUT16)

Bit	D7:D0
Name	OUT16:OUT9
Default	xxxx xxxx

Store the input state of OUT9~OUT16 as the input port (Write only). The INTB pin will be pulled high until the MCU reads the data of State Register.

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Table 12 09h ADC Sample Rate Register

Bit	D7:D0
Name	SR
Default	0000 0000

The value of ADC Sample Rate Register decides the sample rate of ADC for Audio Frame Mode. The sample rate could be computed using the Formula (1):

$$SR = 15.625kHz / \sum_{n=0}^7 D[n] \cdot 2^n \quad (1)$$

Where “n” indicates the bit location in the respective ADC Sample Rate Register.

For example: D7:D0 = 10110100

$$SR = 15.625kHz / (2^2 + 2^4 + 2^5 + 2^7) = 105Hz$$

Table 13 10h~1Fh PWM Register (OUT16~OUT1)

Bit	D7:D0
Name	PWM
Default	0000 0000

The PWM Registers adjusts LED luminous intensity in 256 steps.

The value of a channel’s PWM Register decides the average output current for each output, OUT1~OUT16. The average output current may be computed using the Formula (2):

$$I_{OUT} = \frac{I_{MAX}}{256} \cdot \sum_{n=0}^7 D[n] \cdot 2^n \quad (2)$$

Where “n” indicates the bit location in the respective PWM Registers.

For example: D7:D0 = 10110101

$$I_{OUT} = I_{MAX} (2^0 + 2^2 + 2^4 + 2^5 + 2^7) / 256$$

I_{MAX} is set by the Lighting Effect Register (03h).

Table 14 20h~AFh Frame Register Address List

	LED Control Register	PWM Register
Frame 1	20h ~ 21h	22h ~ 31h
Frame 2	32h ~ 33h	34h ~ 43h
Frame 3	44h ~ 45h	46h ~ 55h
Frame 4	56h ~ 57h	58h ~ 67h
Frame 5	68h ~ 69h	6Ah ~ 79h
Frame 6	7Ah ~ 7Bh	7Ch ~ 8Bh
Frame 7	8Ch ~ 8Dh	8Eh ~ 9Dh
Frame 8	9Eh ~ 9Fh	A0h ~ AFh

Frame Registers store the data of 8 frames. Each frame is controlled by two LED Control Registers and sixteen PWM Registers.

The detail about the LED Control Register is shown in Table 4, 5 and the PWM Register is shown in Table 13.

B0h Update Register

The data sent to the PWM Register will be stored in temporary registers. A write operation of any 8-bit value to the Update Register is required to update the registers.

Table 15 B6h Frame Delay Register

Bit	D7:D5	D4:D0
Name	FDT	-
Default	000	00000

Set the delay time between each frame in Auto Frame Play Mode.

FDT	Frame Delay Time
000	32ms
001	64ms
010	128ms
011	256ms
100	512ms
101	1.024s
110	2.048s
111	4.096s

Table 16 B7h Frame Start Register

Bit	D7:D5	D4:D0
Name	FS	-
Default	000	00000

Set the start frame in Auto Frame Play Mode.

FS	Frame Start
000	Frame 1
001	Frame 2
010	Frame 3
011	Frame 4
100	Frame 5
101	Frame 6
110	Frame 7
111	Frame 8

For example, if FS bit sets to “011”, it plays from the fourth frame to the eighth frame then cycled back to the first frame.

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TYPICAL APPLICATION

PWM CONTROL

By setting the MODE bit of the Configuration Register (00h) to "00", IS31FL3216 operates in PWM Control Mode. The LED brightness of 16 channels can be modulated with 256 steps by PWM Registers. For example, if the data in PWM Register is "0000 0100", then the PWM is the fourth step.

Writing new data continuously to the registers can modulate the brightness of the LEDs to achieve a breathing effect.

GAMMA CORRECTION

In order to perform a better visual LED breathing effect we recommend using a gamma corrected PWM value to set the LED intensity. This results in a reduced number of steps for the LED intensity setting, but causes the change in intensity to appear more linear to the human eye.

Gamma correction, also known as gamma compression or encoding, is used to encode linear luminance to match the non-linear characteristics of display. Since the IS31FL3216 can modulate the brightness of the LEDs with 256 steps, a gamma correction function can be applied when computing each subsequent LED intensity setting such that the changes in brightness matches the human eye's brightness curve.

Table 17 32 gamma steps with 256 PWM steps

C(0)	C(1)	C(2)	C(3)	C(4)	C(5)	C(6)	C(7)
0	1	2	4	6	10	13	18
C(8)	C(9)	C(10)	C(11)	C(12)	C(13)	C(14)	C(15)
22	28	33	39	46	53	61	69
C(16)	C(17)	C(18)	C(19)	C(20)	C(21)	C(22)	C(23)
78	86	96	106	116	126	138	149
C(24)	C(25)	C(26)	C(27)	C(28)	C(29)	C(30)	C(31)
161	173	186	199	212	226	240	255

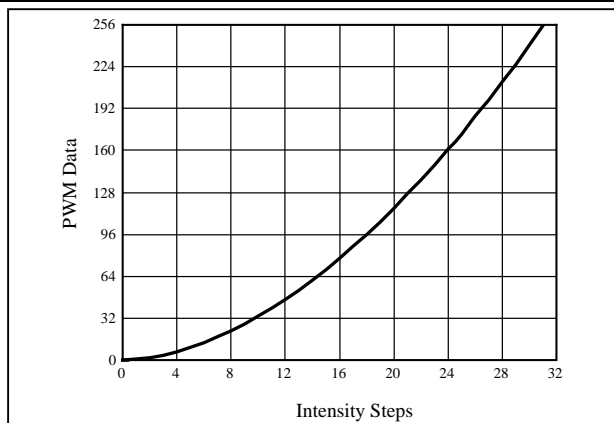


Figure 8 Gamma Correction(32 Steps)

Choosing more gamma steps provides for a more continuous looking breathing effect. This is useful for very long breathing cycles. The recommended configuration is defined by the breath cycle T. When T=1s, choose 32 gamma steps, when T=2s, choose 64 gamma steps. The user must decide the final number of gamma steps not only by the LED itself, but also based on the visual performance of the finished product.

Table 18 64 gamma steps with 256 PWM steps

C(0)	C(1)	C(2)	C(3)	C(4)	C(5)	C(6)	C(7)
0	1	2	3	4	5	6	7
C(8)	C(9)	C(10)	C(11)	C(12)	C(13)	C(14)	C(15)
8	10	12	14	16	18	20	22
C(16)	C(17)	C(18)	C(19)	C(20)	C(21)	C(22)	C(23)
24	26	29	32	35	38	41	44
C(24)	C(25)	C(26)	C(27)	C(28)	C(29)	C(30)	C(31)
47	50	53	57	61	65	69	73
C(32)	C(33)	C(34)	C(35)	C(36)	C(37)	C(38)	C(39)
77	81	85	89	94	99	104	109
C(40)	C(41)	C(42)	C(43)	C(44)	C(45)	C(46)	C(47)
114	119	124	129	134	140	146	152
C(48)	C(49)	C(50)	C(51)	C(52)	C(53)	C(54)	C(55)
158	164	170	176	182	188	195	202
C(56)	C(57)	C(58)	C(59)	C(60)	C(61)	C(62)	C(63)
209	216	223	230	237	244	251	255

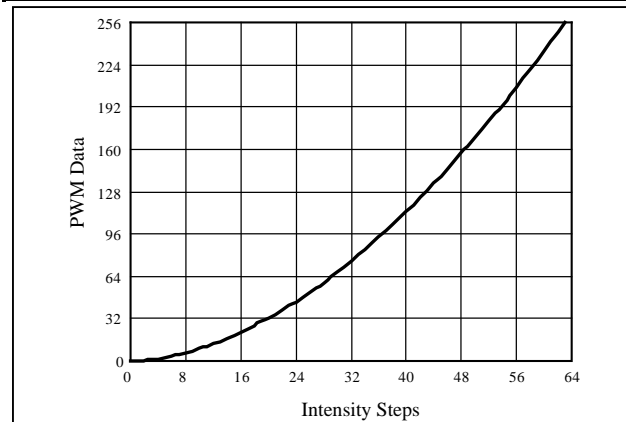


Figure 9 Gamma Correction(64 Steps)

Note, the data of 32 gamma steps is the standard value and the data of 64 gamma steps is the recommended value.

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AUTO FRAME PLAY MODE

By setting the MODE bit of the Configuration Register (00h) to “01”, the IS31FL3216 operates in Auto Frame Play Mode. It stores data of 8 frames and automatically plays in order. Customers can configure the delay time between each two frames and the first playing frame by setting the Frame Delay Register (B6h) and the Frame Start Register (B7h).

AUDIO FRAME MODE

By setting the MODE bit of the Configuration Register (00h) to “10”, the IS31FL3216 operates in Audio Frame Mode. It stores data of 8 frames and the 8 frames playing follow the input signal. 09h register is used to set the ADC sample rate for the input signal to control frames playing. It plays the first frame when the value is the smallest and plays the eighth frame when the value is the biggest (See Table 14).

AUDIO MODULATED MODE AND GAIN SETTING

By setting the AE bit of the Configuration Register to “1”, IS31FL3216 operates in Audio Modulated Mode. The intensity of LEDs is adjusted by the input signal. The audio input gain can be set by the Lighting Effect Register (03h).

CHANNEL MODE SETTING

IS31FL3216 has 16 channels for LEDs output. OUT9~OUT16 also can be set as GPIO ports. By setting the OUTx bit of the Channel Register to “1”, the corresponding channel will be used as GPIO port. When the OUTx is set to “0”, the corresponding channel will be used as LED output.

CASCADE FOR SYNCHRONIZATION OF CHIPS

Operating in the cascade mode can make two chips synchronize. By setting the CM bit of the Lighting Effect Register (03h) to “0”, IS31FL3216 operates as a master. The CLK pin offers the output clock signal. When the CM bit sets to “1”, IS31FL3216 operates as a slave. The CLK pin as a clock input pin. If there is only one chip to use, setting CM bit to “0” and the CLK pin should be floating.

INTERRUPT FUNCTION

When OUT9~OUT16 configure as input port and the interrupt function enabled, the INTB pin is available. If any input port of OUT9~OUT16 has state changing, the INTB pin will be pulled low. The MCU can get the information via reading the State Register (08h). The INTB will be back to high until the MCU reading the State Register (08h).

SHUTDOWN MODE

Shutdown mode can either be used as a means of reducing power. During shutdown mode all registers retain their data and OUT9~OUT16 still can be available as GPIO port.

SOFTWARE SHUTDOWN

By setting SSD bit of the Configuration Register (00h) to “0”, the IS31FL3216 will operate in software shutdown mode, wherein they consume only 1µA (Typ.) current. When the IS31FL3216 is in software shutdown mode, all current sources are switched off.

HARDWARE SHUTDOWN

The chip enters hardware shutdown mode when the SDB pin is pulled low.

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CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak	
Temperature min (T _{smin})	150°C
Temperature max (T _{smax})	200°C
Time (T _{smin} to T _{smax}) (t _s)	60-120 seconds
Average ramp-up rate (T _{smax} to T _p)	3°C/second max.
Liquidous temperature (T _L)	217°C
Time at liquidous (t _L)	60-150 seconds
Peak package body temperature (T _p)*	Max 260°C
Time (t _p)** within 5°C of the specified classification temperature (T _c)	Max 30 seconds
Average ramp-down rate (T _p to T _{smax})	6°C/second max.
Time 25°C to peak	8 minutes max.

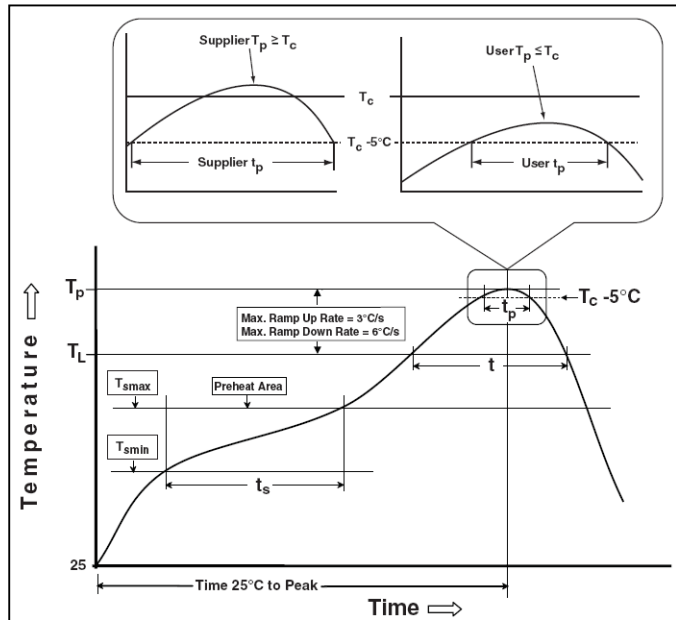
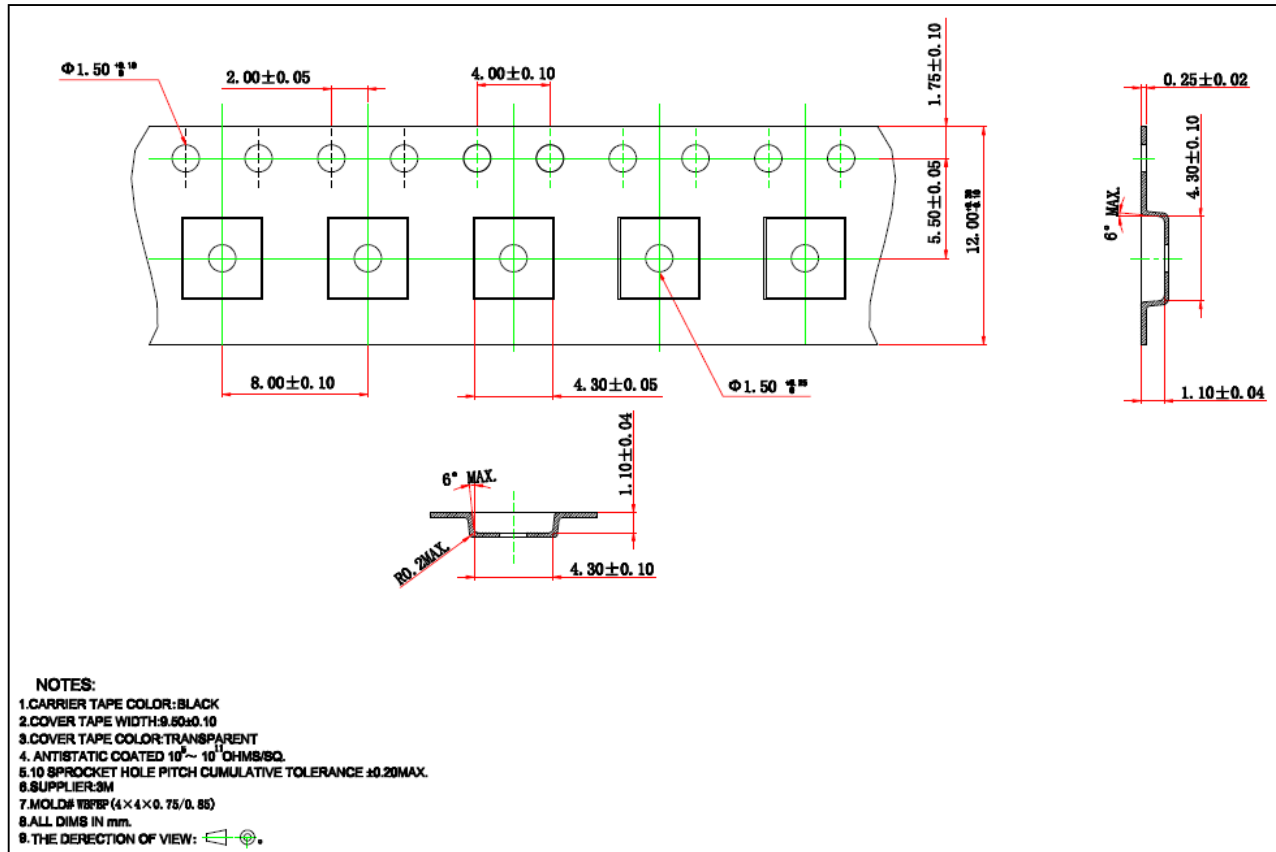


Figure 10 Classification profile

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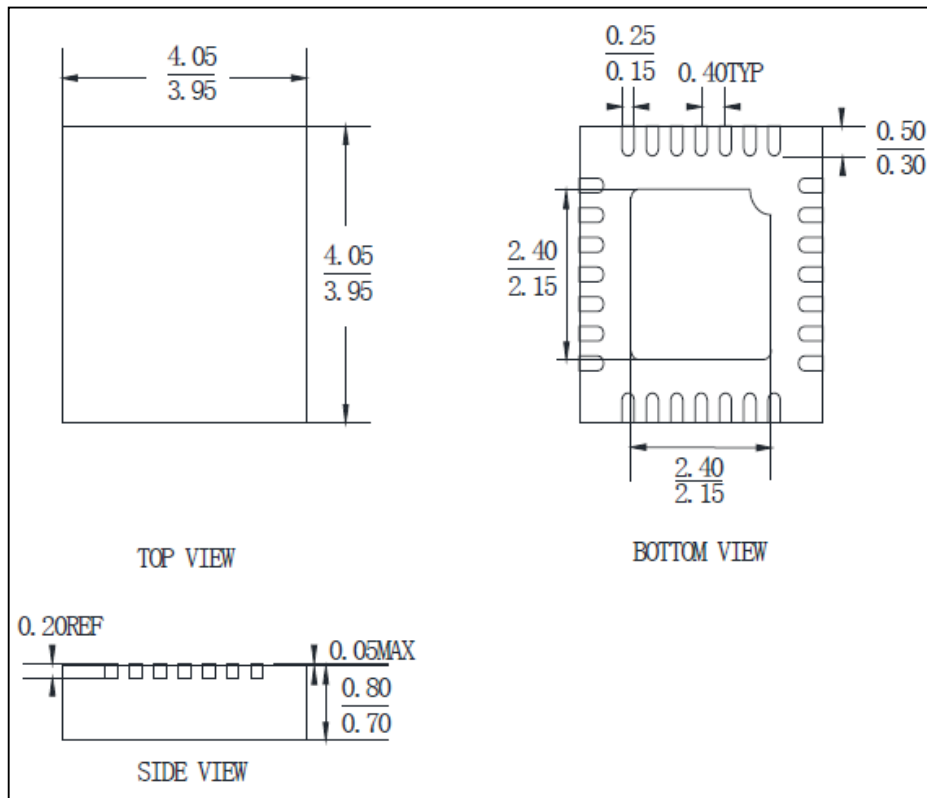
TAPE AND REEL INFORMATION



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PACKAGE INFORMATION

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Note: All dimensions in millimeters unless otherwise stated.