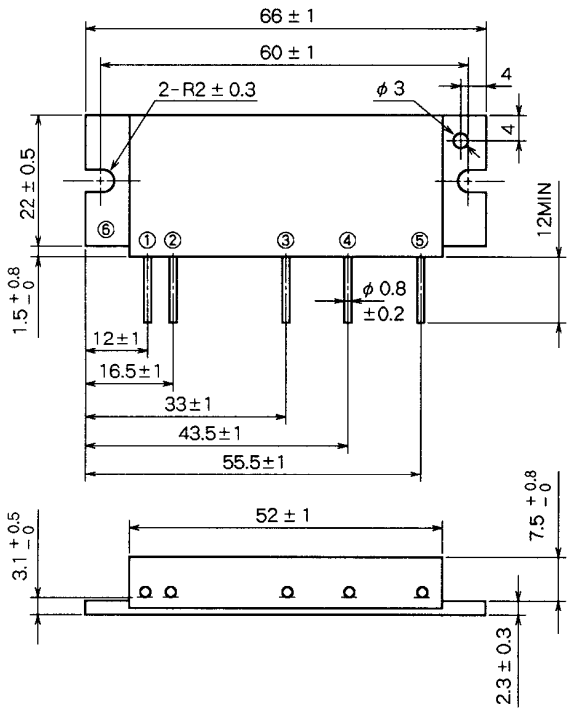
# M57745

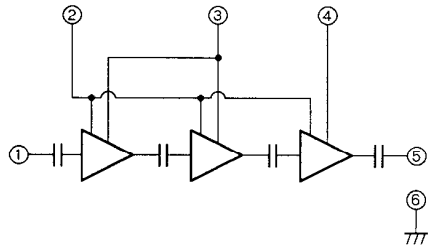
## 430-450MHz, 12.5V, 33W, SSB MOBILE RADIO

**OUTLINE DRAWING** Dimensions in mm




H3

**BLOCK DIAGRAM**



PIN :
①Pin : RF INPUT
②VBB : BASE BIAS SUPPLY
③VCC1 : 1st. DC SUPPLY
④VCC2 : 2nd. DC SUPPLY
⑤Po : RF OUTPUT
⑥GND : FIN

**ABSOLUTE MAXIMUM RATINGS** (Tc = 25℃ unless otherwise noted)

| Symbol | Parameter | Conditions | Ratings | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 17 | V |
| $V_{BB}$ | Base bias | | 10 | V |
| $I_{CC}$ | Total current | | 10 | A |
| $P_{in(max)}$ | Input power | $Z_G = Z_L = 50\ \Omega$ | 0.5 | W |
| $P_{O(max)}$ | Output power | $Z_G = Z_L = 50\ \Omega$ | 40 | W |
| $T_{C(OP)}$ | Operation case temperature | | − 30 to 110 | ℃ |
| $T_{stg}$ | Storage temperature | | − 40 to 110 | ℃ |

Note. Above parameters are guaranteed independently.

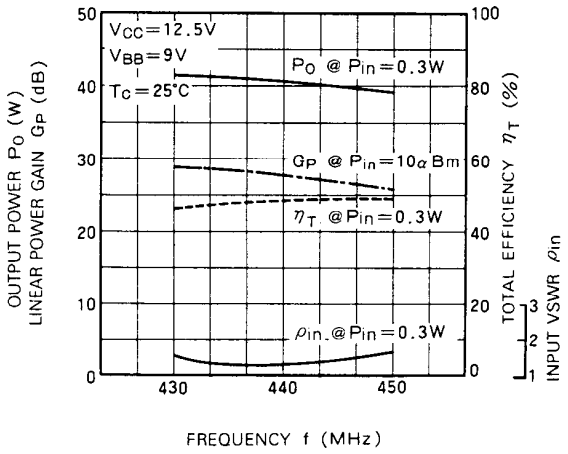
**ELECTRICAL CHARACTERISTICS** (Tc = 25℃ unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| f | Frequency range | $P_{in}$ = 0.3W<br>$V_{CC}$ = 12.5V<br>$V_{BB}$ = 9V<br>$Z_G = Z_L = 50\ \Omega$ | 430 | 450 | MHz |
| $P_O$ | Output power | | 33 | | W |
| $\eta_T$ | Total efficiency | | 40 | | % |
| 2fo | 2nd. harmonic | | | − 30 | dBc |
| 3fo | 3rd. harmonic | | | − 30 | dBc |
| $\rho$ in | Input VSWR | | | 2.5 | − |
| − | Load VSWR tolerance | $V_{CC}$ = 15.2V, $V_{BB}$ = 9V<br>$P_O$ = 30W ($P_{in}$ : controlled)<br>Load VSWR = 8.8 : 1 (All phase),<br>$Z_G = 50\ \Omega$ | No degradation or destroy | | − |

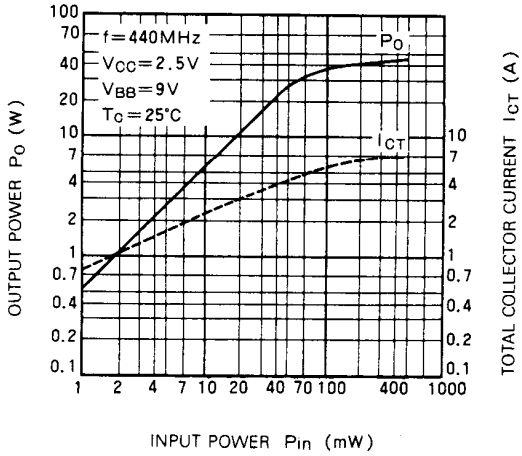
Note. Above parameters, ratings, limits and conditions are subject to change.

## TYPICAL PERFORMANCE DATA

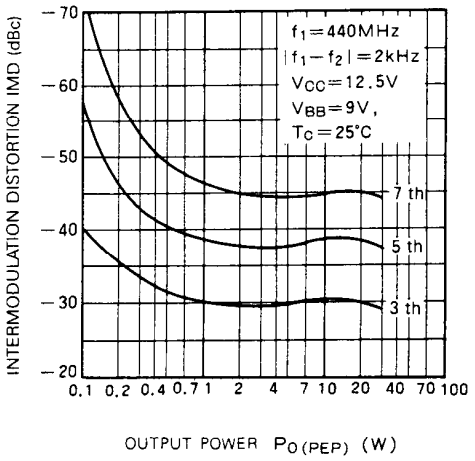
### OUTPUT POWER, LINEAR POWER GAIN, TOTAL EFFICIENCY, INPUT VSWR VS. FREQUENCY



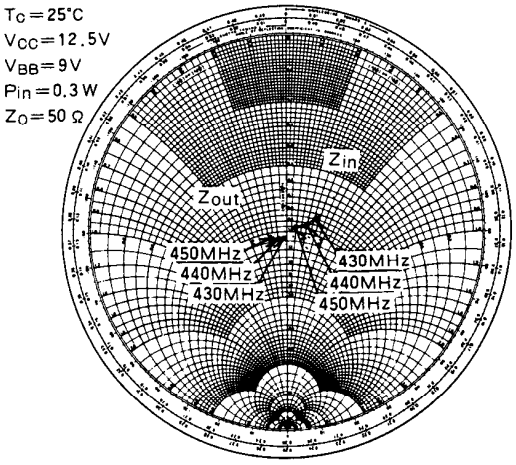

### OUTPUT POWER, TOTAL COLLECTOR CURRENT, VS. INPUT POWER




### INTERMODULATION DISTORTION VS. OUTPUT POWER




### INPUT IMPEDANCE, OUTPUT IMPEDANCE VS. FREQUENCY



## DESIGN CONSIDERATION OF HEAT RADIATION.

Please refer to following consideration when designing heat shink.

### 1. Junction temperature of incorporated transistors at standard operation.

(1) Thermal resistance between junction and package of incorporated transistors.

a) First stage transistor

$R_{th(j-c)1}$ = 12°C/W (Typ.)

b) Second stage transistor

$R_{th(j-c)2}$ = 4°C/W (Typ.)

c) Final stage transistor

$R_{th(j-c)3}$ = 1.75°C/W (Typ.)

(2) Junction temperature of incorporated transistors at standard operation.

- Conditions for standard operation.

$P_O$ = 30W, $V_{CC}$ = 12.5V, $P_{in}$ = 0.3W, $\eta_T$ = 40% (minimum rating), $P_{O1}$ (Note 1) = 2W, $P_{O2}$ (2) = 8W, $I_T$ = 6A ($I_{T1}$ (3) = 0.35A, $I_{T2}$ (4) = 1.32A, $I_{T3}$ (5) = 4.33A)

Note 1: Output power of the first stage transistor
Note 2: Output power of the second stage transistor
Note 3: Circuit current of the first stage transistor
Note 4: Circuit current of the second stage transistor
Note 5: Circuit current of the final stage transistor

- Junction temperature of the first stage transistor

$T_{j1} \fallingdotseq (V_{CC} \times I_{T1} - P_{O1} + P_{in}) \times R_{th(j-c)1} + T_C$ (6)
$= (12.5 \times 0.35 - 2 + 0.3) \times 12 + T_C$
$= 32 + T_C$ (°C)

Note 6: Package temperature of device

- Junction temperature of the second stage transistor

$T_{j2} = (V_{CC} \times I_{T2} - P_{O2} + P_{O1}) \times R_{th(j-c)2} + T_C$
$= (12.5 \times 1.32 - 8 + 2) \times 4 + T_C$
$= 42 + T_C$ (°C)

- Junction temperature of the final stage transistor

$T_{j3} = (V_{CC} \times I_{T3} - P_O + P_{O2}) \times R_{th(j-c)3} + T_C$
$= (12.5 \times 4.33 - 30 + 8) \times 1.75 + T_C$
$= 56 + T_C$ (°C)

### 2. Heat sink design

In thermal design of heat sink, try to keep the package temperature at the upper limit of the operating ambient temperature (normally $T_a$ = 60°C) and at the output power of 30W below 90°C.

The thermal resistance $R_{th(c-a)}$ (7) of the heat sink to realize this:

$$R_{th(c-a)} = \frac{T_C - T_a}{(P_O/\eta_T) - P_O + P_{in}} = \frac{90 - 60}{(30/0.4) - 30 + 0.3}$$
$$= 0.66\ (°C/W)$$

Note 7: Inclusive of the contact thermal resistance between device and heat sink.

Mounting the heat sink of the above thermal resistance on the device,

$T_{j1}$ = 122°C, $T_{j2}$ = 132°C, $T_{j3}$ = 146°C at $T_a$ = 60°C, $T_C$ = 90°C.

In the annual average of ambient temperature is 30°C,

$T_{j1}$ = 92°C, $T_{j1}$ = 102°C, $T_{j3}$ = 116°C.

As the maximum junction temperature of these incorporated transistors $T_{jmax}$ are 175°C, application under fully derated condition is ensured.