

74AC11652 OCTAL BUS TRANSCEIVER AND REGISTERS WITH 3-STATE OUTPUTS

SCAS088A - DECEMBER 1989 - REVISED APRIL 1996

- Independent Registers and Enables for A and B Buses
- Multiplexed Real-Time and Stored Data
- Inverting Data Paths
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise
- **EPIC™** (Enhanced-Performance Implanted CMOS) 1- μ m Process
- 500-mA Typical Latch-Up Immunity at 125°C

description

The 74AC11652 consists of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Output-enable (OEAB and $\overline{OEBA}$) inputs are provided to control the transceiver functions. The select-control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. A low input level selects real-time data, and a high input level selects stored data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 74AC11652.

Data on the A or B bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) inputs, regardless of the select- or enable-control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and $\overline{OEBA}$. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set remains at its last state.

The 74AC11652 is characterized for operation from -40°C to 85°C.

DW PACKAGE
(TOP VIEW)

OEAB	1	28	CLKAB
A1	2	27	SAB
A2	3	26	B1
A3	4	25	B2
A4	5	24	B3
GND	6	23	B4
GND	7	22	V_{CC}
GND	8	21	V_{CC}
GND	9	20	B5
A5	10	19	B6
A6	11	18	B7
A7	12	17	B8
A8	13	16	CLKBA
$\overline{OEBA}$	14	15	SBA



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**TEXAS
INSTRUMENTS**

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74AC11652

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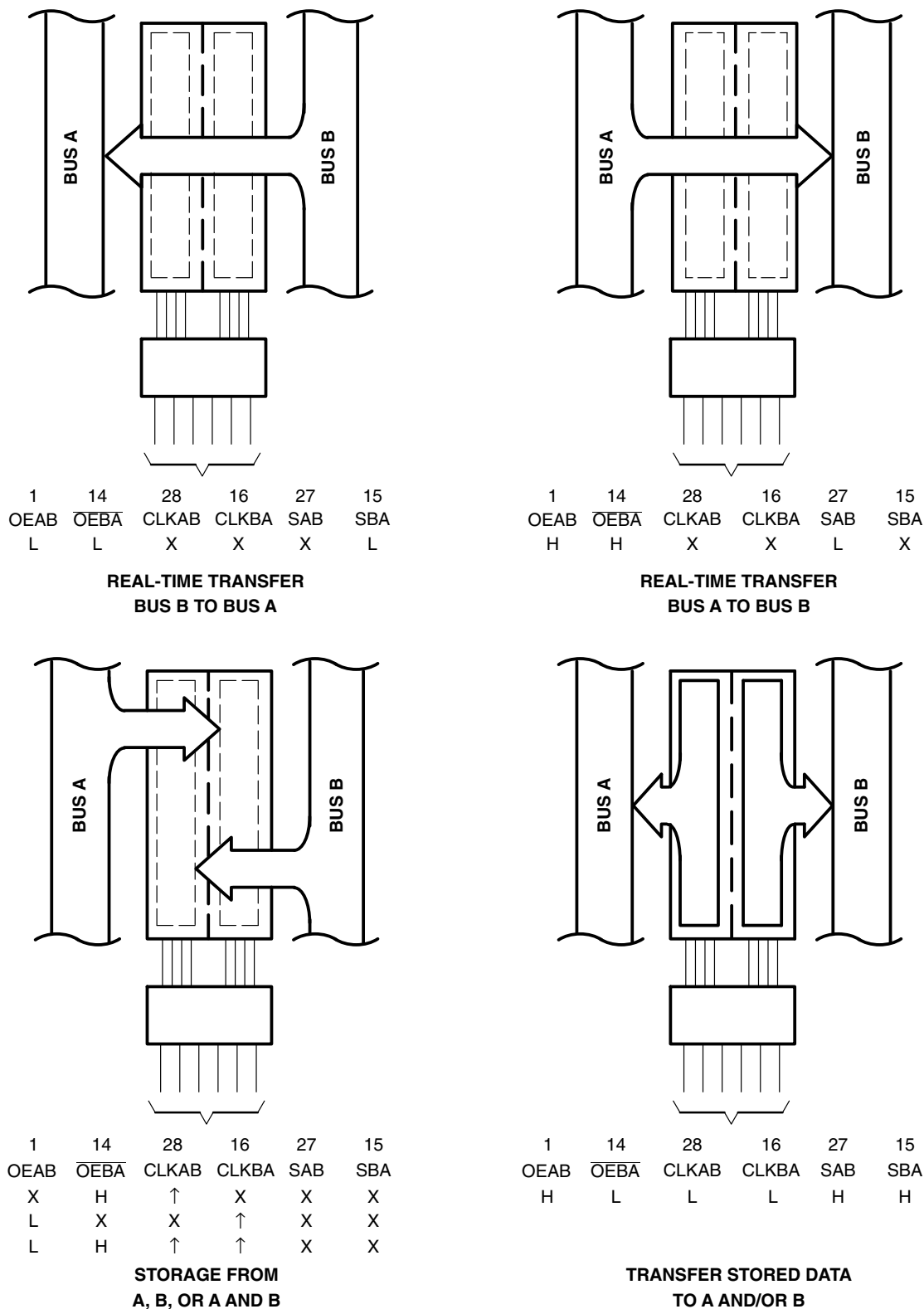


Figure 1. Bus-Management Functions

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FUNCTION TABLE

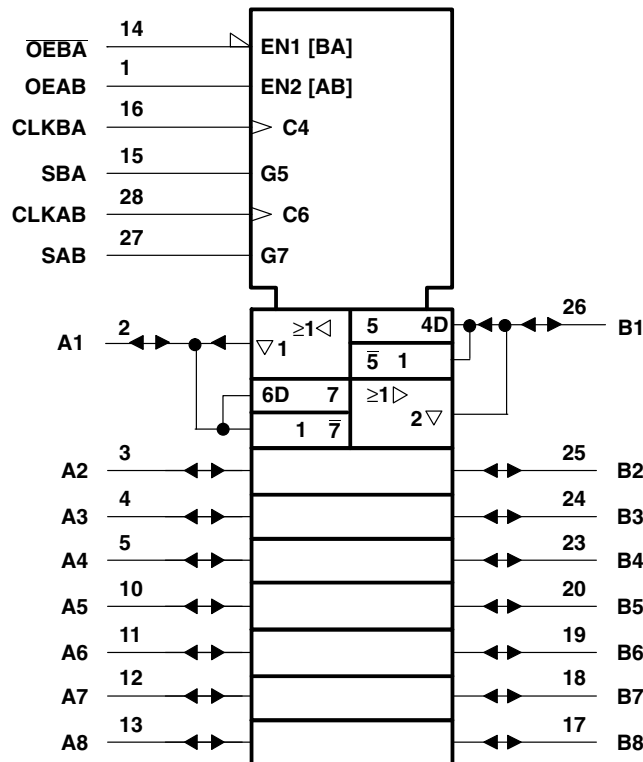
INPUTS						DATA I/O†		OPERATION OR FUNCTION
OEAB	OEBA	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
L	H	L	L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B data
X	H	↑	L	X	X	Input	Unspecified‡	Store A, hold B
H	H	↑	↑	X‡	X	Input	Output	Store A in both registers
L	X	L	↑	X	X	Unspecified‡	Input	Hold A, store B
L	L	↑	↑	X	X‡	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	L	X	H	Output	Input	Stored B data to A bus
H	H	X	X	L	X	Input	Output	Real-time A data to B bus
H	H	L	X	H	X	Input	Output	Stored A data to B bus
H	L	L	L	H	H	Output	Output	Stored A data to B bus and stored B data to A bus

† The data output functions may be enabled or disabled by a variety of level combinations at the OEAB or OEBA inputs. Data input functions are always enabled; i.e., data at the bus pins is stored on every low-to-high transition on the clock inputs.

‡ Select control = L; clocks can occur simultaneously.

Select control = H; clocks must be staggered to load both registers.

logic symbol§



§ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

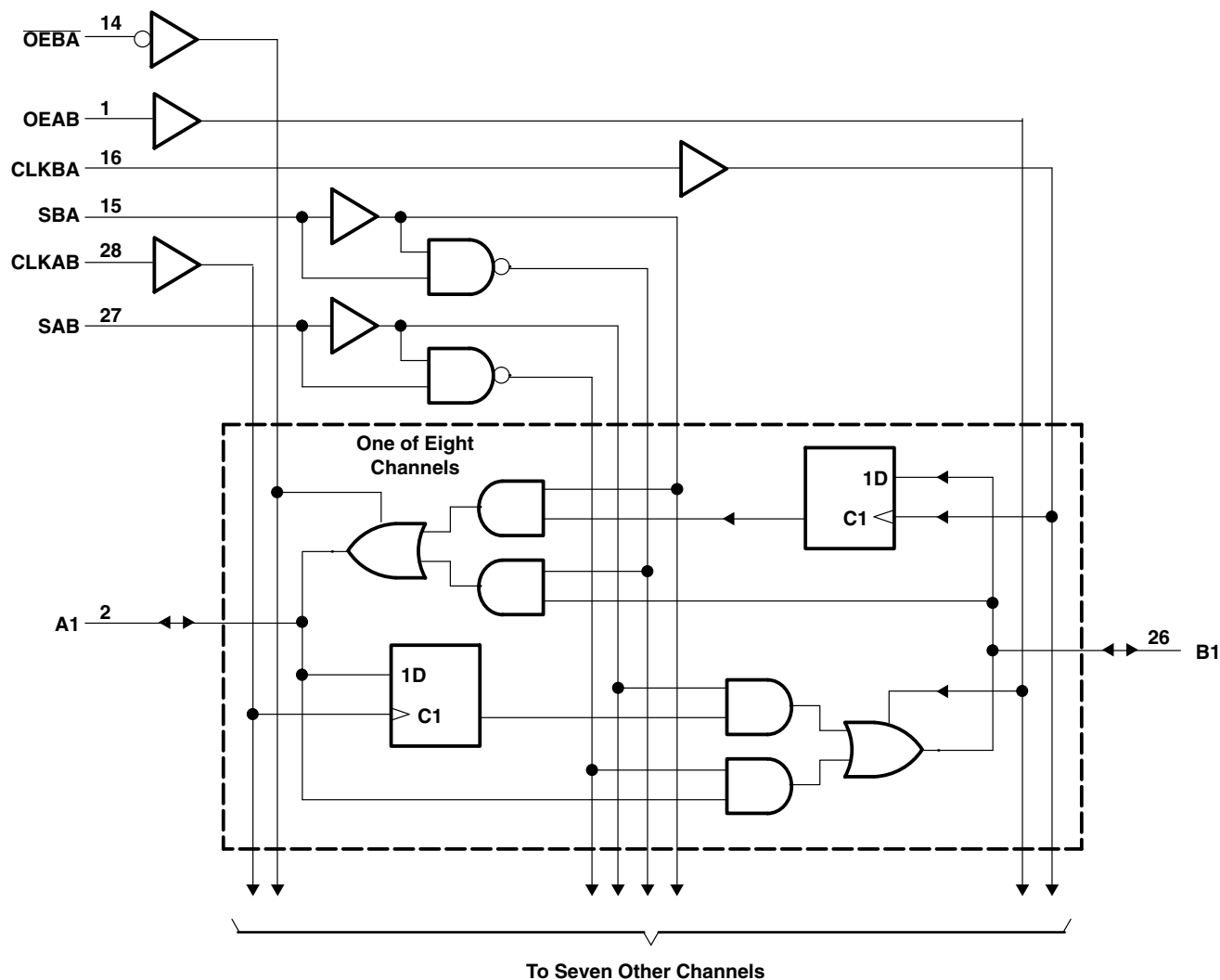
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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND	± 200 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2)	1.7 W
Storage temperature range, T_{stg}	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

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recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	5	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 3\text{ V}$	2.1		V
		$V_{CC} = 4.5\text{ V}$	3.15		
		$V_{CC} = 5.5\text{ V}$	3.85		
V_{IL}	Low-level input voltage	$V_{CC} = 3\text{ V}$		0.9	V
		$V_{CC} = 4.5\text{ V}$		1.35	
		$V_{CC} = 5.5\text{ V}$		1.65	
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 3\text{ V}$		-4	mA
		$V_{CC} = 4.5\text{ V}$		-24	
		$V_{CC} = 5.5\text{ V}$		-24	
I_{OL}	Low-level output current	$V_{CC} = 3\text{ V}$		12	mA
		$V_{CC} = 4.5\text{ V}$		24	
		$V_{CC} = 5.5\text{ V}$		24	
$\Delta t/\Delta v$	Input transition rise or fall rate	Control pins	0	5	ns/V
		Data	0	10	
T_A	Operating free-air temperature	-40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	T _A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V _{OH}		I _{OH} = − 50 μA	3 V	2.9			2.9		V
			4.5 V	4.4			4.4		
			5.5 V	5.4			5.4		
		I _{OH} = − 4 mA	3 V	2.58			2.48		
		I _{OH} = − 24 mA	4.5 V	3.94			3.8		
			5.5 V	4.94			4.8		
		I _{OH} = − 75 mA [†]	5.5 V				3.85		
V _{OL}		I _{OL} = 50 μA	3 V	0.1			0.1		V
			4.5 V	0.1			0.1		
			5.5 V	0.1			0.1		
		I _{OL} = 12 mA	3 V	0.36			0.44		
		I _{OL} = 24 mA	4.5 V	0.36			0.44		
			5.5 V	0.36			0.44		
		I _{OL} = 75 mA [†]	5.5 V				1.65		
I _I	Control inputs	V _I = V _{CC} or GND	5.5 V	±0.1			±1		μA
I _{OZ} [‡]	A or B ports	V _O = V _{CC} or GND	5.5 V	±0.5			±5		μA
I _{CC}		V _I = V _{CC} or GND, I _O = 0	5.5 V	8			80		μA
C _i	Control inputs	V _I = V _{CC} or GND	5 V	4.5					pF
C _{io}	A or B ports	V _O = V _{CC} or GND	5 V	12					pF

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

[‡] For I/O ports, the parameter I_{OZ} includes the input leakage current.



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timing requirements over recommended operating free-air temperature range, $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ (unless otherwise noted) (see Figure 2)

		$T_A = 25^\circ\text{C}$		MIN	MAX	UNIT
		MIN	MAX			
f_{clock}	Clock frequency	0	65	0	65	MHz
t_w	Pulse duration, CLK high or low	7.7		7.7		ns
t_{su}	Setup time, A or B before CLKAB $\uparrow$ or CLKBA $\uparrow$	6		6		ns
t_h	Hold time, A or B after CLKAB $\uparrow$ or CLKBA $\uparrow$	1		1		ns

timing requirements over recommended operating free-air temperature range, $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$ (unless otherwise noted) (see Figure 2)

		$T_A = 25^\circ\text{C}$		MIN	MAX	UNIT
		MIN	MAX			
f_{clock}	Clock frequency	0	105	0	105	MHz
t_w	Pulse duration, CLK high or low	4.8		4.8		ns
t_{su}	Setup time, A or B before CLKAB $\uparrow$ or CLKBA $\uparrow$	4.5		4.5		ns
t_h	Hold time, A or B after CLKAB $\uparrow$ or CLKBA $\uparrow$	1		1		ns

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			65			65		MHz
t_{PLH}	A or B	B or A	2.9	8.5	11.1	2.9	12.9	ns
t_{PHL}			3.9	10.3	12.9	3.9	14.2	
t_{PLH}	CLKBA or CLKAB	A or B	4.3	11.2	14.3	4.3	16.2	ns
t_{PHL}			5.3	13.1	16.2	5.3	17.8	
t_{PLH}	SBA or SAB $\uparrow$ (A or B high)	A or B	3.4	9.4	12	3.4	13.7	ns
t_{PHL}			4.7	11.5	14.3	4.7	15.6	
t_{PLH}	SBA or SAB $\uparrow$ (A or B low)	A or B	3.9	10.5	13.3	3.9	14.9	ns
t_{PHL}			4.8	12.1	16.3	4.8	17.7	
t_{PZH}	$\overline{\text{OEBA}}$	A	4.3	11.1	14.5	4.3	16.5	ns
t_{PZL}			5.2	14.4	19.8	5.2	22	
t_{PHZ}	$\overline{\text{OEBA}}$	A	3.7	6.4	8.1	3.7	8.5	ns
t_{PLZ}			3.5	6	7.8	3.5	8.2	
t_{PZH}	OEAB	B	4.7	11.6	15	4.7	16.9	ns
t_{PZL}			5.6	14.8	19.9	5.6	21.9	
t_{PHZ}	OEAB	B	4	6.6	8.2	4	8.6	ns
t_{PLZ}			3.5	6.1	7.7	3.5	8	

$\dagger$ These parameters are measured with the internal output state of the storage register opposite that of the bus input.

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switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			105			105		MHz
t_{PLH}	A or B	B or A	2.4	5.2	7.6	2.4	8.6	ns
t_{PHL}			3.1	6	8.7	3.1	9.6	
t_{PLH}	CLKBA or CLKAB	A or B	3.6	6.7	9.5	3.6	10.7	ns
t_{PHL}			4.4	7.8	10.8	4.4	12	
t_{PLH}	SBA or SAB (A or B high)	A or B	2.9	5.6	8.1	2.9	9.1	ns
t_{PHL}			3.8	6.9	9.6	3.8	10.7	
t_{PLH}	SBA or SAB (A or B low)	A or B	3.3	6.2	8.8	3.3	9.9	ns
t_{PHL}			4	7.1	9.9	4	10.9	
t_{PZH}	$\overline{\text{OEBA}}$	A	3.3	6.6	9.6	3.3	10.9	ns
t_{PZL}			4.2	7.4	10.9	4.2	12.2	
t_{PHZ}	$\overline{\text{OEBA}}$	A	3.6	5.5	7.2	3.6	7.6	ns
t_{PLZ}			3.3	5	6.7	3.3	7.1	
t_{PZH}	OEAB	B	4.1	7.2	10.1	4.1	11.3	ns
t_{PZL}			4.6	7.9	11.1	4.6	12.3	
t_{PHZ}	OEAB	B	3.9	5.6	7.3	3.9	7.6	ns
t_{PLZ}			3.4	5.2	6.8	3.4	7.2	

operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	60	pF
		Outputs disabled	14	

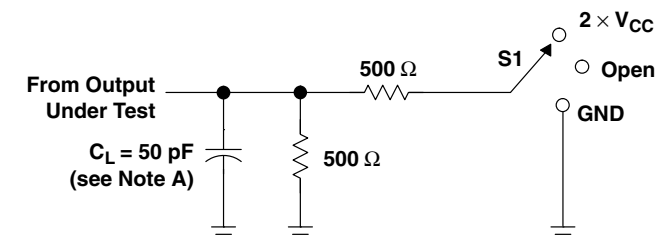
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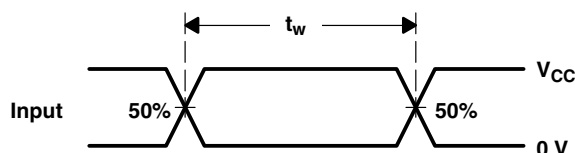
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PARAMETER MEASUREMENT INFORMATION

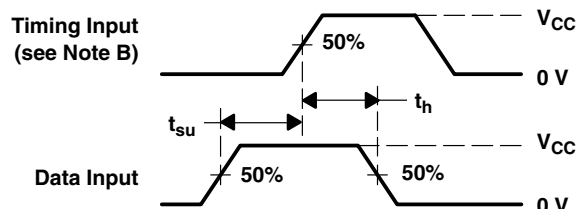


LOAD CIRCUIT

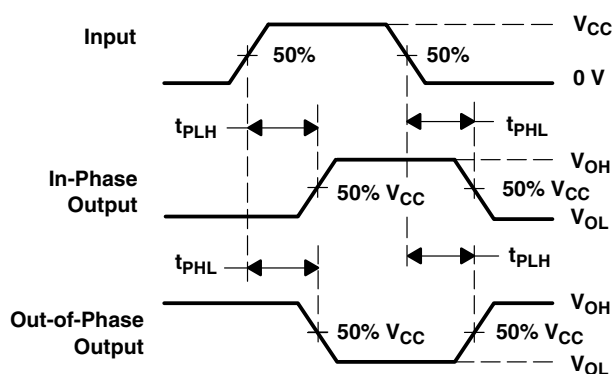
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	GND



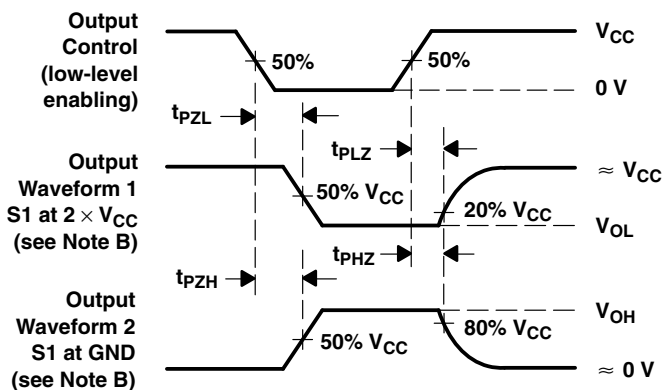
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 3 \text{ ns}$, $t_f = 3 \text{ ns}$.
 - The outputs are measured one at a time with one input transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
74AC11652DW	OBSOLETE	SOIC	DW	28		TBD	Call TI	Call TI	Replaced by CD74AC652M96
74AC11652DWR	OBSOLETE	SOIC	DW	28		TBD	Call TI	Call TI	Replaced by CD74AC652M96

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

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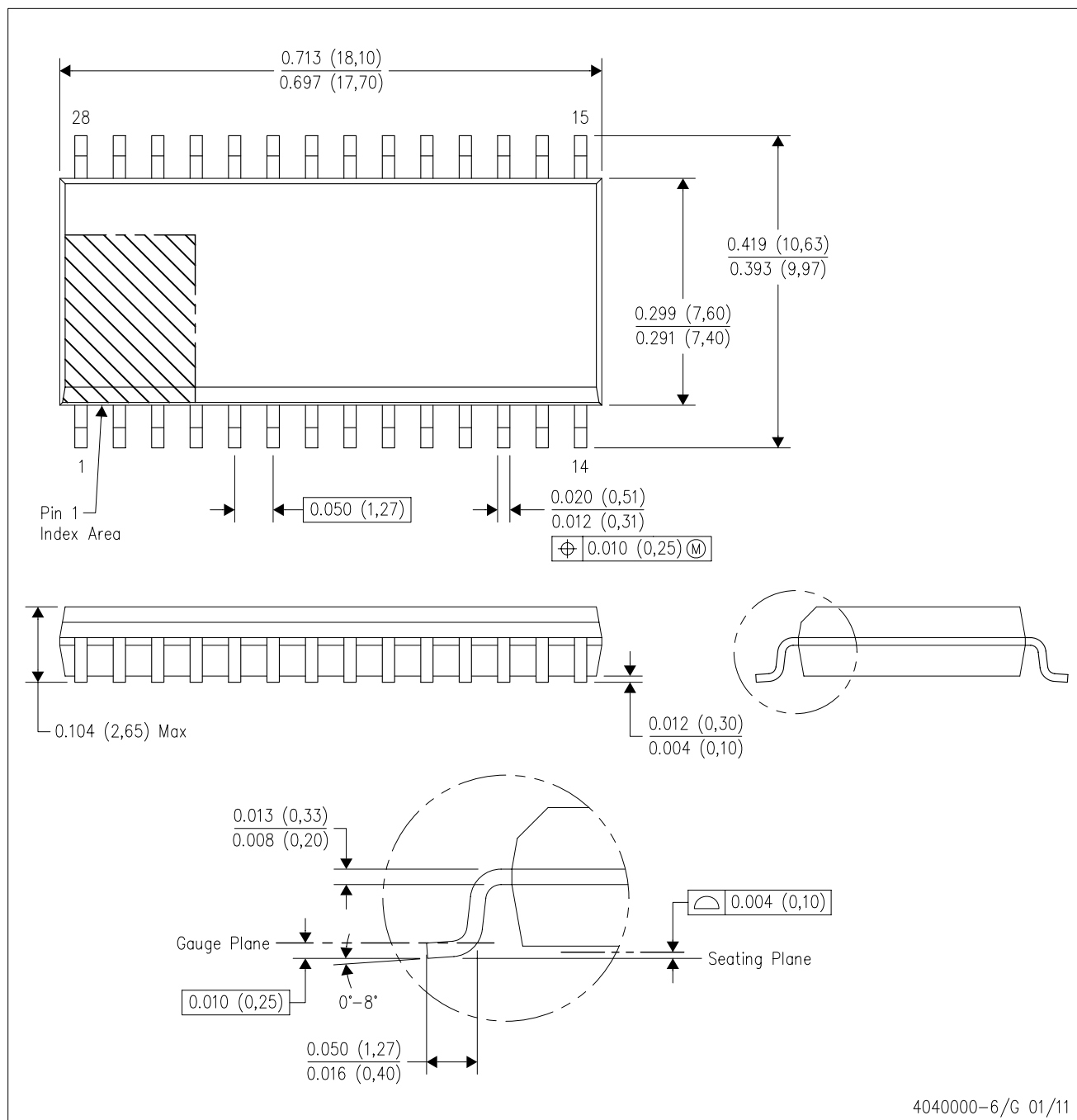
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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DW (R-PDSO-G28)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MS-013 variation AE.

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