TPSM831D31 8-V to 14-V Input, 0.25-V to 1.52-V Dual Output, 120-A + 40-A PMBus™ Power Module

1 Features

- Input Voltage Range: 8 V to 14 V
- Dual Output: 120 A (3-phase) + 40 A (1-phase)
- Output Voltage Range: 0.25 V to 1.52 V
  - Programmable in 5-mV Steps
  - Differential Remote Sense
  - ±0.5% Vref Accuracy with Remote Sense
- PMBus Interface
  - Programmable V_{OUT}, UVLO, Fault limits
  - VIN, VOUT, IOUT, Temperature Telemetry
  - Supports up to 1-MHz Bus Speed
  - On-Chip Non-Volatile Configuration Memory
- Ultra-Fast Transient Response
- Switching Frequency Range: 350 kHz to 700 kHz
- 15-mm × 48-mm Footprint and 12-mm Height
- Efficiencies up to 95%
- Dual Power Good Outputs
- Overcurrent, Overvoltage, Overtemperature Protection
- Operating IC Junction Range: –40°C to 125°C
- Operating Ambient Range: –40°C to 105°C

2 Applications

- High-Performance Processor / ASIC with Dual Power Rails
- Networking Processor Power (Broadcom®, Cavium®, Marvell®, NXP®)
- High-Current FPGA Power (Intel®, Xilinx®)
- High-Performance ARM Processor Power

3 Description

The TPSM831D31 is a PMBus™-controlled, dual-output, 4-phase power module that combines a high-performance D-CAP+™ controller with four high-efficiency Smart Power Stages, and low-loss inductors, into a rugged, thermally enhanced surface-mount package. The user supplies the input and output capacitors and a few passive components to complete the system. The first output is configured as a 3-phase power stage that can deliver up to 120 A of continuous output current. The second output is a single phase power stage that can deliver up to 40 A of output current.

The PMBus interface provides for converter configuration of each VOUT, UVLO, soft start, overcurrent, and thermal shutdown parameters. The interface provides support for telemetry that can report the actual input voltage, output voltage, output current, and device temperature. The computed input and output power can also be reported. Standard PMBus *warning* and *fault* functions are also supported. The device supports PMBus communication speeds up to 1 MHz, with 1.8-V or 3.3-V logic levels, as detailed in Section 4.3 of SMBus Specification V3.0. The module supports a subset of the commands in the PMBus 1.3 specification.

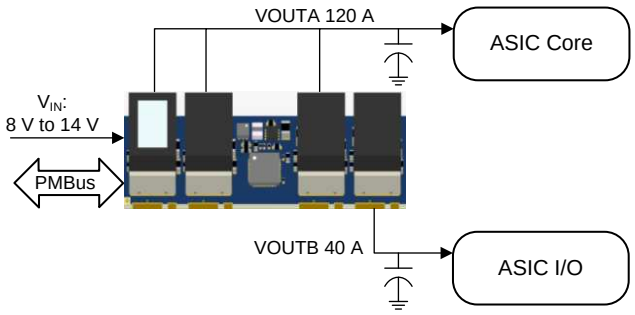
Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPSM831D31	MOA (28)	48.00 mm × 15.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

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Simplified Application



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. ADVANCE INFORMATION for pre-production products; subject to change without notice.

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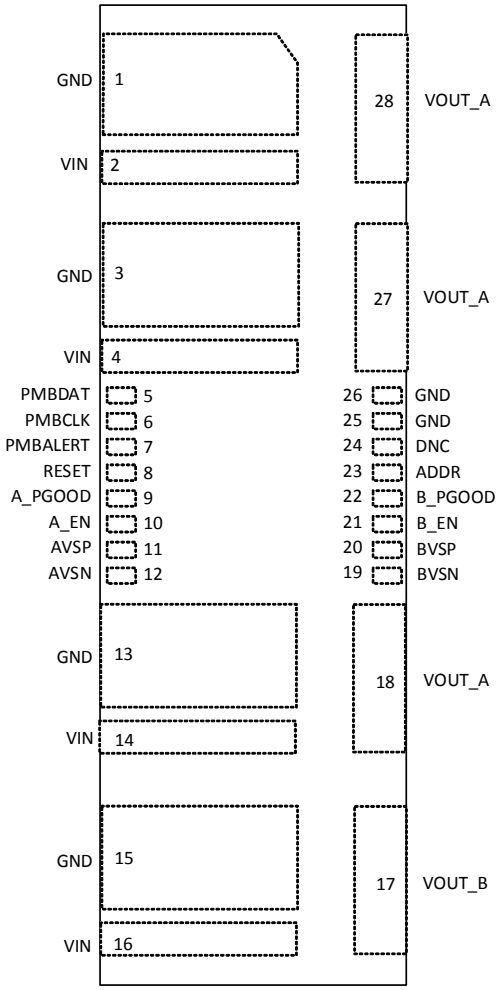
4 Revision History

DATE	REVISION	NOTES
August 2018	*	Initial release

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5 Pin Configuration and Functions

MOA Package
28-Pin QFM
Top View



Pin Functions

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
ADDR	23	I	Connect a resistor from this pin to GND to set the desired PMBus address. Do not leave this pin floating. See PMBus ADDRESS section.
A_EN	10	I	Active high enable input for VOUT_A. Asserting this pin high enables power conversion on the VOUT_A channel.
A_PGOOD	9	O	Open drain Power Good signal of the VOUT_A channel. This pin requires a pullup resistor. This pin is pulled low when a shutdown fault occurs.
AVSN	12	I	Negative input of the remote voltage sense of channel A. Connect this pin to ground at the VOUT_A load for best voltage regulation. Do not let this pin float.
AVSP	11	I	Positive input of the remote voltage sense of channel A. Connect this pin to VOUT_A at the load for best voltage regulation. Do not let this pin float.
B_EN	21	I	Active high enable input for VOUT_B. Asserting this pin high enables power conversion on the VOUT_B channel.
B_PGOOD	22	O	Open drain Power Good signal of the VOUT_B channel. This pin requires a pullup resistor. This pin is pulled low when a shutdown fault occurs.

(1) G = ground, I = input, O = output

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Pin Functions (continued)

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
BVSN	19	I	Negative input of the remote voltage sense of channel B. Connect this pin to ground at the VOUT_B load for best voltage regulation. Do not let this pin float.
BVSP	20	I	Positive input of the remote voltage sense of channel B. Connect this pin to VOUT_A at the load for best voltage regulation. Do not let this pin float.
DNC	24	—	Do not connect. This pin is connected to internal circuitry. Do not connect this pin to other signal or voltage source. Connecting the pin to GND is recommended.
GND	1	G	Power ground of the device. Connect pins 1, 3, 13, and 15 to the bypass caps associated with VIN. Connect pads 1, 3, 13, 15 to the PCB ground planes using multiple vias for optimal thermal performance.
	3		
	13		
	15		
	25		
	26		
PMBCLK	6	I	PMBus serial clock interface. (Open Drain)
PMBDAT	5	I/O	PMBus bi-directional serial data interface. (Open Drain)
PMBALERT	7	I/O	PMBus bi-directional ALERT pin interface. (Open Drain)
RESET	8	I	Active low RESET input that resets the output voltage to its programmed BOOT voltage. This pin requires a pullup resistor.
VIN	2	I	Input voltage. These pins provide voltage to the power conversion stages of the module. Connect these pins to the PCB VIN planes using multiple vias for optimal thermal performance.
	4		
	14		
	16		
VOUT_A	18	O	Output voltage of channel A. Connect these pins to the output A load. Connect external bypass capacitors between these pins and GND pins 1, 3, and 13.
	27		
	28		
VOUT_B	17	O	Output voltage of channel B. Connect this pin to the output B load. Connect external bypass capacitors between this pin and GND pin 15.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage (2)	VIN	–0.3	19	V
	ADDR, AVSP, BVSP, RESET, PMBCLK, PMBDAT	–0.3	3.6	V
	AGND, AVSN, BVSN	–0.3	0.3	V
Output voltage(1) (2)	VOUT_A, VOUT_B, A_PGOOD, B_PGOOD, PMBALERT	–0.3	3.6	V
Mechanical shock	Mil-STD-883D, Method 2002.3, 1 msec, 1/2 sine, mounted		tbd	G
Mechanical vibration	Mil-STD-883D, Method 2007.2, 20 to 2000 Hz		tbd	G
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{STG}		–55	150	°C

(1) Stresses beyond those listed under *absolutemaximum ratings* may cause permanent damage to the device. These are stress ratings onlyand functional operation of the device at these or any other conditions beyond those indicatedunder "recommended operating conditions" is not implied. Exposure to absolute-maximum-ratedconditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminalGND unless otherwise noted.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±tbd	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±tbd	

(1) JEDEC document JEP155 states that 500-V HBM allows safemanufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safemanufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VIN		8	12	14	V
VOUT_A, VOUT_B, AVSP, BVSP		0.25		1.52	V
IOUTA		0		120	A
IOUTB		0		40	A
PMBCLK, PMBDAT, RESET pullup, A_PGOOD pullup, B_PGOOD pullup, PMBALERT pullup			3.3	3.5	V
Switching frequency		350	400	700	kHz
Operating junction temperature, T_J		–40		125	°C
Operating ambient temperature, T_A		–40		105	°C
External input capacitance, C_{IN}	Ceramic		500		µF
	Non-ceramic		1000		µF
External output capacitance, C_{OUT_A}	Ceramic	600	1200		µF
	Non-ceramic	2750	5500		µF
External output capacitance, C_{OUT_B}	Ceramic	200	400		µF
	Non-ceramic	900	1800		µF

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6.4 Thermal Information

THERMAL METRIC(1)			TPSM831D31 MOA (QFN) 28 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (2)	Natural Convection	5.5	°C/W
		200 LFM	3.4	°C/W
		400 LFM	2.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter (3)		0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter (4)		1.6	°C/W
T_{SD}	Thermal shutdown temperature (default setting)		135	°C

(1) For more information about thermal metrics, see the *Semiconductor and IC Package ThermalMetrics* application report .
(2) The junction-to-ambient thermal resistance applies to devicessoldered directly to a 100 mm x 150 mm, 8-layer PCB with 2 oz. copper.
(3) The junction-to-top board characterization parameter,ψ_{JT}, estimates the junction temperature, T_J, of adevice in a real system, using a procedure described in JESD51-2A (section 6 and 7).$T_J = \psi_{JT} \times Pdis + T_T$; wherePdis is the power dissipated in the device and T_T is the temperature of thetop of the inductor.
(4) The junction-to-board characterization parameter,ψ_{JB}, estimates the junction temperature, T_J, of adevice in a real system, using a procedure described in JESD51-2A (sections 6 and 7).$T_J = \psi_{JB} \times Pdis + T_B$; wherePdis is the power dissipated in the device and T_B is the temperature of theboard 1mm from the device.

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6.5 Electrical Characteristics

T_A = –40°C to +105°C , V_{IN} = 12 V,V_{OUTA} = V_{AVSP} = 1 V, V_{OUTB} =V_{BVSP} = 1 V, V_{AVSN} = V_{BVSN} = 0V, I_{OUTA} = I_{OUTB} = 0 A, F_{SW} =400 kHz, C_{IN1} = 24 × 22-µF, 25-V, 1210 ceramic, C_{IN2}= 2 × 470 µF, electrolytic bulk, C_{OUTA1} = 12 × 100-µF, 6.3-V, 1210 ceramic,C_{OUTA2} = 12 × 470 µF, 6.3 V, C_{OUTB1} = 4 × 100-µF,6.3-V, 1210 ceramic, C_{OUTB2} = 4 × 470-µF, 6.3-V polymer bulk. Minimum andmaximum limits are specified through production test or by design. Typical values represent themost likely parametric norm and are provided for reference only.(unless otherwisenoted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT VOLTAGE						
V_{IN}	Input voltage range		8		14	V
UVLO	V_{IN} undervoltage lockout	V_{IN} increasing (default setting)		7.25		V
		V_{IN} decreasing (default setting)		6.5		V
$I_{IN(STBY)}$	Input standby current	A_EN = B_EN = GND		8	12	mA
OUTPUT VOLTAGE						
V_{OUT_A}	Boot voltage	5-mV DAC (default setting)	0.492	0.5	0.508	V
	Programmable range	5-mV DAC	0.25		1.52	V
	Programmable step size	5-mV DAC		5		mV
	Set-point voltage tolerance	5-mV DAC, 0.8 V ≤ VOUT ≤ 1 V	–5%		5%	
	Line regulation	8 V ≤ V_{IN} ≤ 14 V		0.1%		
	Load regulation	0 A ≤ I_{OUT} ≤ 120 A		0.1%		
	Output voltage ripple	20-MHz bandwidth		10		mV
V_{OUT_B}	Boot voltage	5-mV DAC (default setting)	0.492	0.5	0.508	V
	Programmable range	5-mV DAC	0.25		1.52	V
	Programmable step size	5-mV DAC		5		mV
	Set-point voltage tolerance	5-mV DAC, 0.8 V ≤ VOUT ≤ 1 V	–5%		5%	
	Line regulation	8 V ≤ V_{IN} ≤ 14 V,		0.1%		
	Load regulation	0 A ≤ I_{OUT} ≤ 120 A		0.1%		
	Output voltage ripple	20-MHz bandwidth		30		mV

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Electrical Characteristics (continued)

T_A = –40°C to +105°C , V_{IN} = 12 V,V_{OUTA} = V_{AVSP} = 1 V, V_{OUTB} =V_{BVSP} = 1 V, V_{AVSN} = V_{BVSN} = 0V, I_{OUTA} = I_{OUTB} = 0 A, F_{SW} =400 kHz, C_{IN1} = 24 × 22-µF, 25-V, 1210 ceramic, C_{IN2}= 2 × 470 µF, electrolytic bulk, C_{OUTA1} = 12 × 100-µF, 6.3-V, 1210 ceramic,C_{OUTA2} = 12 × 470 µF, 6.3 V, C_{OUTB1} = 4 × 100-µF,6.3-V, 1210 ceramic, C_{OUTB2} = 4 × 470-µF, 6.3-V polymer bulk. Minimum andmaximum limits are specified through production test or by design. Typical values represent themost likely parametric norm and are provided for reference only.(unless otherwisenoted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT CURRENT						
I_{OUT_A}	Output current	Natural convection(1)	0		120	A
	Overcurrent fault threshold	Factory default setting (150% of I_{OUT} max)		180		A
	Per phase OCL level	(default setting)		54		A
	Overcurrent warning threshold	Factory default setting (100% of I_{OUT} max)		120		A
I_{OUT_B}	Output current	Natural convection(1)	0		40	A
	Overcurrent fault threshold	Factory default setting (150% of I_{OUT} max)		60		A
	Per Phase OCL level	(default setting)		54		A
	Overcurrent warning threshold	Factory default setting (100% of I_{OUT} max)		40		A
PERFORMANCE						
	Efficiency(2)	I_{OUT_A} = 90 A, V_{OUT_B} disabled		93%		
		I_{OUT_B} = 30 A, V_{OUT_A} = disabled		92%		
TIMING						
$t_{STARTUPA}$	VOUTA start-up time	V_{VBOOT} > 0 V, no faults, TON_DELAY = 0xB1EC (PAGE 0) (default setting)	0.38	0.48	0.58	ms
$t_{STARTUPB}$	VOUTB start-up time	V_{VBOOT} > 0 V, no faults, TON_DELAY = 0xB396 (PAGE 1) (default setting)	0.8	0.9	1	ms
t_{VCCVID}	VID change to VSP change	ACK of SetVID_x command to start of voltage ramp			500	ns
t_{ON_BLANK}	Rising-edge blanking time(3)	MFR_SPEC_09<8:6> = 110b (default setting)	53	72	92	ns
SL_{SET}	Slew rate setting(3)	VOUT_TRANSITION_RATE = 0xE028 (default setting)		2.5		mV/µs
SL_{SS}	AVSP and BVSP slew rate soft-start(3)	MFR_SPEC_13<8> = 0b (default setting)		SL_{SET} /4		mV/µs
SWITCHING FREQUENCY						
f_{SW}	Switching frequency(3)	FREQUENCY_SWITCH = 0x0190 (default setting)	360	400	440	kHz
	Range(3)		350		700	kHz

(1) See SOA graph for derating over temperature.
(2) Phase shedding disabled.
(3) Applies to both VOUTA and VOUTB.

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6.6 References: DAC

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{VIDSTP}	VID step size(1)	5 mV DAC: Change VID0 HI to LO to HI		5		mV
K_{RATIO}	Voltage divider ratio(1)	VOUT_SCALE_LOOP = 0xe808, VOUT_SCALE_MONITOR = 0xe808		1.000		
V_{OUT_TRIML}	V_{OUT} offset LSB(1)	MFR_SPECIFIC_05 = 0x01	0	1.25	2.5	mV
V_{OUT_TRIMR}	V_{OUT} offset range	MFR_SPECIFIC_05 = 0x1F	37.5	38.75	40	mV
		MFR_SPECIFIC_05 = 0xA0	–43.25	–40	–37.75	
		MFR_SPECIFIC_05 = 0x5F	56.25	58.75	61.25	
		MFR_SPECIFIC_05 = 0xE0	–63	–60	–57	

(1) Applies to both VOUTA and VOUTB.

6.7 Telemetry

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{READ_VOUT}	MFR_READ_VOUT accuracy	5-mV DAC : 0.25 V ≤ V_{VSP} ≤ 1.52 V	–12		12	mV
V_{READ_VIN}	READ_VIN accuracy	8 V ≤ V_{IN} ≤ 14 V	–2.25%		2.25%	
$I_{MON_ACC_A}$	Digital current monitor accuracy, Rail A (READ_IOUT)	I_{OUT} = 120 A	–3%		3%	
$I_{MON_ACC_B}$	Digital current monitor accuracy, Rail B (READ_IOUT)	I_{OUT} = 40 A	–3%		3%	
Temp	READ_TEMP1	0.28 V (–40°C) ≤ TSEN ≤ 1.8 V (150°C)	–2	0	2	°C

6.8 Current Sense and Calibration

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{MON_CAL_OF1}$	Current monitor calibration offset LSB (per-phase)	IOUT_CAL_OFFSET resolution (per-phase)		0.125		A
$I_{MON_CAL_OF2}$	Current monitor calibration offset range (per-phase)	IOUT_CAL_OFFSET = 0xE808 (per-phase)		1		A
		IOUT_CAL_OFFSET = 0xEFF9 (per-phase)		–0.875		A
$I_{MON_CAL_OF3}$	Current monitor calibration offset LSB (total)	IOUT_CAL_OFFSET resolution (total)		0.25		A
$I_{MON_CAL_OF4}$	Current monitor calibration offset range (total)	IOUT_CAL_OFFSET = 0xE820 (total)		4		A
		IOUT_CAL_OFFSET = 0xEFE2 (total)		–3.75		A
$I_{MON_CAL_LSB}$	Current monitor calibration gain LSB	IOUT_CAL_GAIN resolution		0.3125%		
$I_{MON_CAL_GAIN}$	Current monitor calibration gain range	IOUT_CAL_GAIN = 0xD131		4.7656		mΩ
		IOUT_CAL_GAIN = 0xD150		5.25		mΩ

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6.9 Logic Interface Pins: A_EN, A_PGOOD, B_EN, B_PGOOD,RESET

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{RPGDL}	Open-drain pulldown resistance	V_{A_PGOOD} = V_{B_PGOOD} = 0.45 V		36	50	Ω
I_{VRTTLK}	Open-drain leakage current	SDIO, A_PGOOD, B_PGOOD, Hi Z Leakage, 3.3-V applied in off state	–2	0.2	2	µA
V_{AENL}	Channel A ENABLE logic low				0.7	V
V_{AENH}	Channel A ENABLE logic high		0.8			V
V_{AENHYS}	Channel A ENABLE hysteresis		0.028	0.05	0.07	V
t_{AENDIG}	Channel A ENABLE deglitch(1)		0.2			µs
I_{AENH}	Channel A I/O 1.1-V leakage	V_{A_EN} = 1.1 V			25	µA
V_{BENL}	Channel B ENABLE logic low				0.7	V
V_{BENH}	Channel B ENABLE logic high		0.8			V
V_{BENHYS}	Channel B ENABLE hysteresis		0.028	0.05	0.07	V
t_{BENDIG}	Channel B ENABLE deglitch(1)		0.2			µs
$t_{AENVRRDYF}$	Channel A ENABLE low to A_PGOOD low	From A_EN low to A_PGOOD low			1.5	µs
I_{BENH}	Channel B I/O 1.1-V leakage	V_{BENH} = 1.1 V			25	µA
V_{RSTL}	RESET logic low				0.8	V
V_{RSTH}	RESET logic high(1)		1.09			V
$t_{RSTTDLY}$	RESET delay time			1		µs

(1) Specified by design. Not production tested.

6.10 Protections: OVP and UVP

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{RDYH5}	Tracking OVP	Measured at the VSP pin wrt VID code. Device latches OFF.	330		400	mV
V_{RDYH0}		Measured at the VSP pin wrt VID code. Device latches OFF.	140		200	mV
$t_{RDYDGLTO}$	VR_RDY deglitch time	See(1)			2.5	µs
$t_{RDYDGLTU}$	VR_RDY deglitch time	f_{SW} = 500 kHz		4		µs
V_{RDYL}	Undervoltage protection(2)	(V_{VSP} + V_{DROOP}) with respect to VID	370	400	430	mV
V_{OVPA}	Fixed overvoltage protection, channel A(2)	V_{AVSP} > V_{OVP} for 1 µs, ENABLE = HI or LO, PWM to LO	2.75	2.75	2.86	V
V_{OVPB}	Fixed overvoltage protection, channel B(2)	V_{BVSP} > V_{OVP} for 1 µs, ENABLE = HI or LO, PWM to LO	1.85	1.9	1.95	V

(1) Time from VSP out of 200-mV or 400-mV VDAC boundary to VR_RDYlow.
(2) Can be programmed with different configurations.

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6.11 Typical Characteristics (V_{IN} = 12 V)

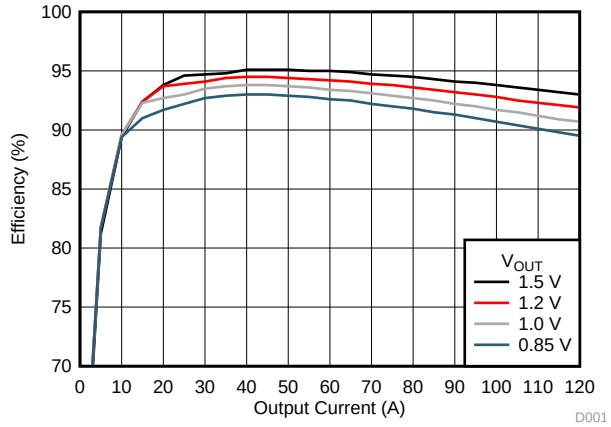


Figure 1. VOUTA Efficiency

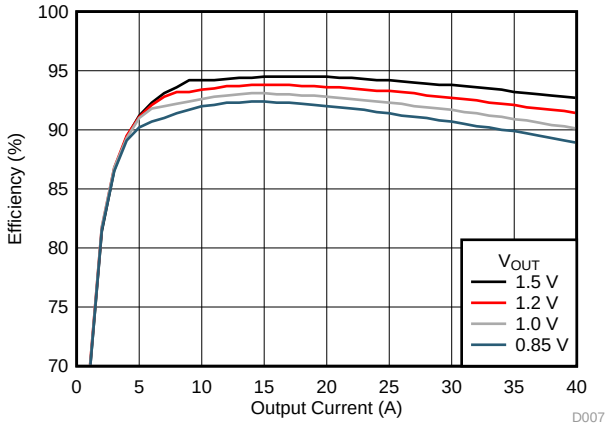


Figure 2. VOUTB Efficiency

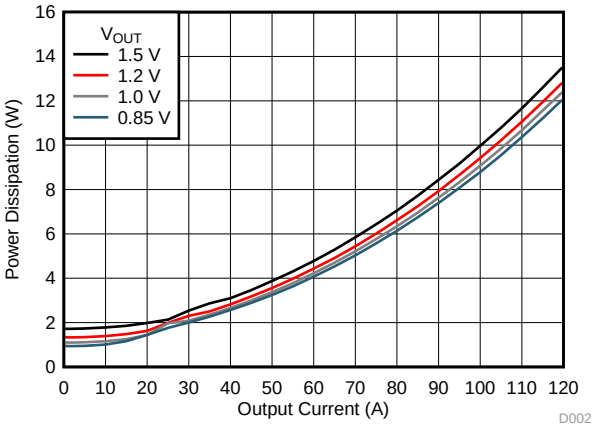


Figure 3. VOUTA Power Dissipation

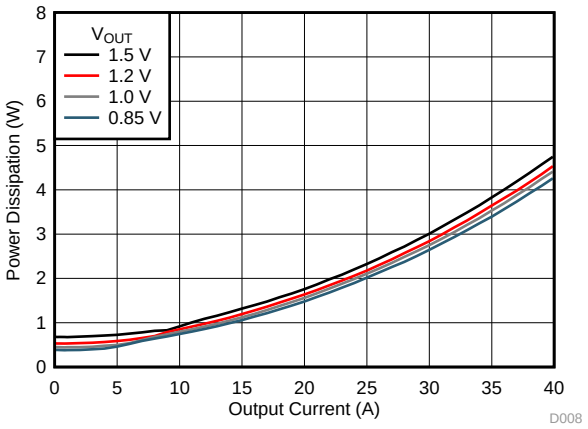


Figure 4. VOUTB Power Dissipation

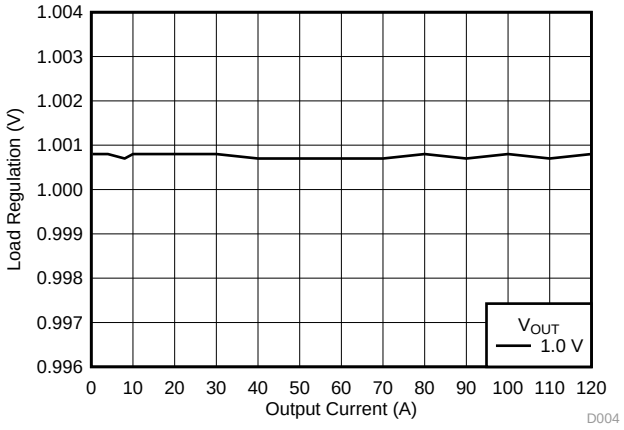


Figure 5. VOUTA Load Regulation

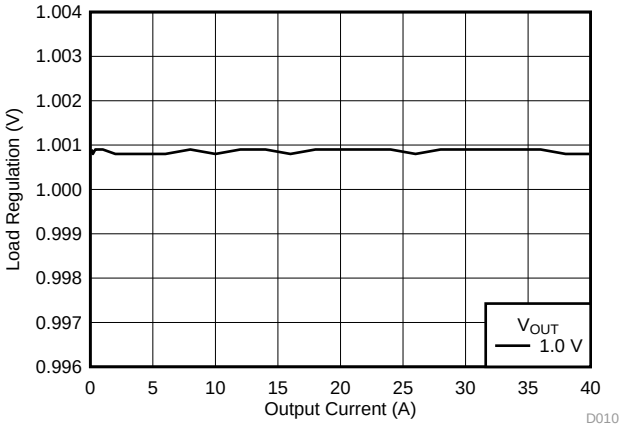
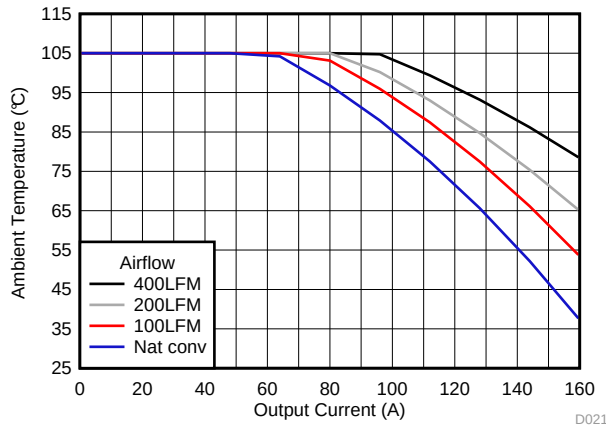


Figure 6. VOUTB Load Regulation

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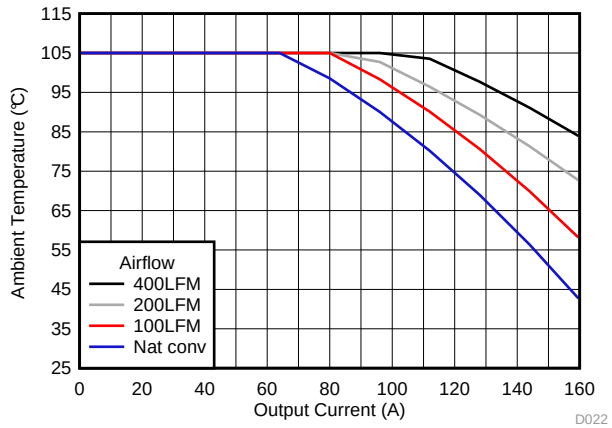
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Typical Characteristics (V_{IN} = 12 V) (continued)



V_{IN} = 12 V
F_{SW} = 400 kHz
V_{OUTA} = V_{OUTB} = 1.0 V
All phases evenly loaded

Figure 7. Thermal Safe Operating Area



V_{IN} = 12 V
F_{SW} = 400 kHz
V_{OUTA} = V_{OUTB} = 0.8 V
All phases evenly loaded

Figure 8. Thermal Safe Operating Area

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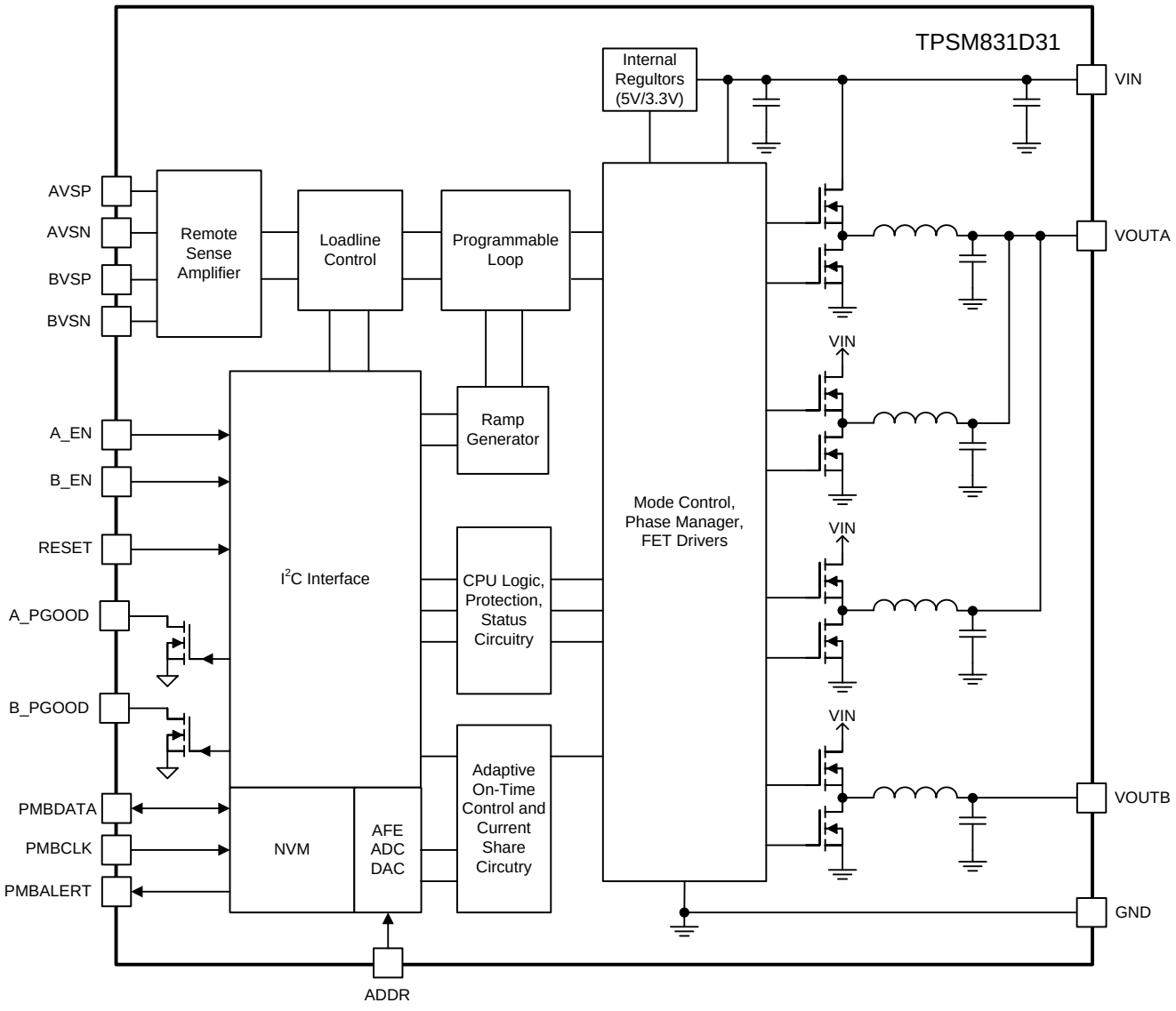
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7 Detailed Description

7.1 Overview

The TPSM831D31 is a PMBus-controlled, dual output 4-phase power module. Both outputs have a programmable output voltage range of 0.25 V to 1.52 V. The first output is configured as a 3-phase power stage that can deliver up to 120 A of output current. The second output is a single phase power stage that can deliver up to 40 A of output current

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 DCAP+ Control

For high current applications, D-CAP+ control architecture, combines the benefits of D-CAP constant on-time control with those of multiphase converters. D-CAP+ control ensures that inductor currents of individual phases are fed back so the system has accurate droop control and good current-sharing performance as well an error amplifier is utilized to improve DC accuracy over load and line.

Figure 9 illustrates the operational waveforms of D-CAP+ control architecture with 3 phases in steady state. By using the adaptive on-time control concept, a pseudo fixed switching frequency of SW_CLK is generated by comparing the summed inductor currents, ISUM, and the error amplifier output, EA, signal. By distributing the switching signal to different phases, all phases can be perfectly interleaved in steady state. During load transients, the switching frequency is varied to improve the transient performance as shown in Figure 10. Variable switching frequencies of different phases can be observed.

One important feature of a multiphase converter is the capability to dynamically add or drop the number of operational phases based on load conditions. The goal is to optimize efficiency while maintaining good load transient performance.

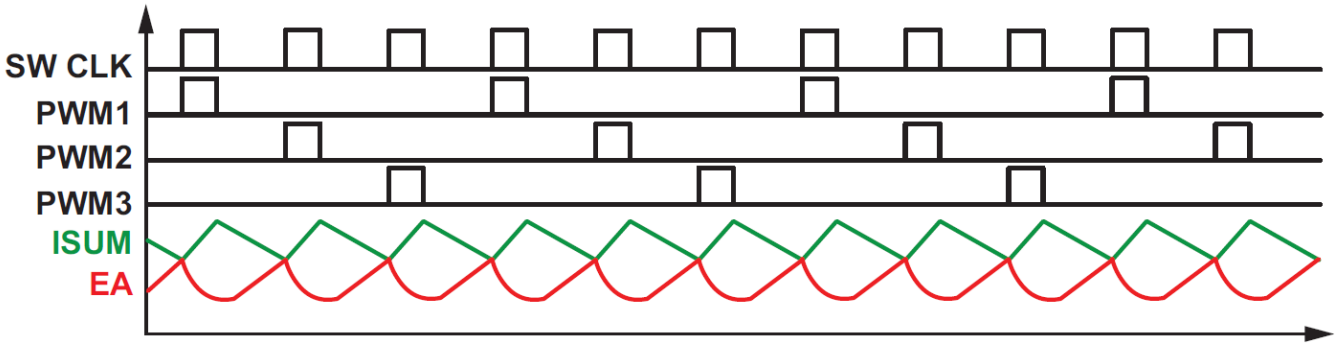


Figure 9. 3-Phase Steady State Switching

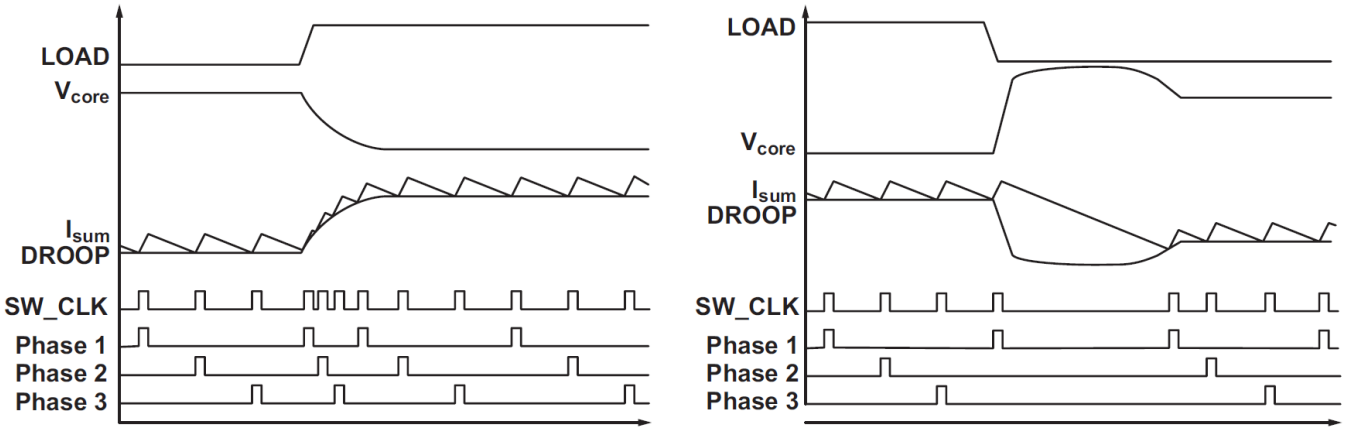


Figure 10. 3-Phase Transient Operation

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Feature Description (continued)

7.3.2 Setting the Load-Line (DROOP)

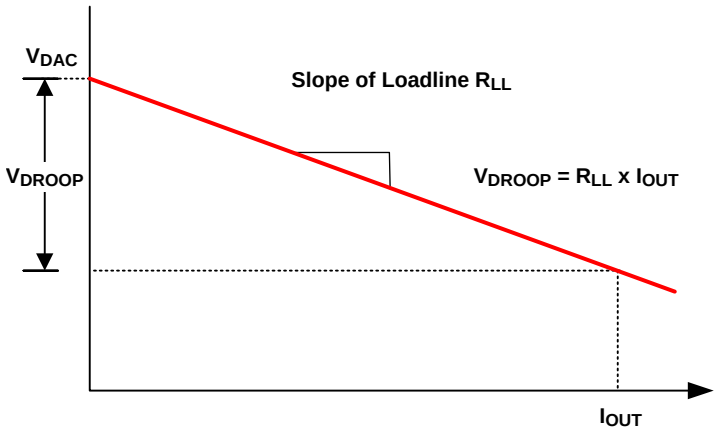


Figure 11. Load Line

The loadline can be set with VOUT_DROOP register via PMBus. The programmable range for channel A is between 0 mΩ and 3.125 mΩ with 64 options, and the range for channel B is between 0 mΩ and 0.875 mΩ with 16 options to fulfill the requirements for different applications. See Table 27 for the DC load line settings.

7.3.3 Start-Up Timing

The start-up time is the time from when a start condition is received (as programmed by the ON_OFF_CONFIG command) until the output voltage starts to rise. The start-up time for both outputs can be programmed using the TON_DELAY command as shown in Table 1.

Table 1. Start-Up Time (1)

	START-UP TIME (ms)		
	MIN	TYP	MAX
TON_DELAY = 0xB1EC	0.38	0.48	0.58
TON_DELAY = 0xB396	0.8	0.9	1
TON_DELAY = 0xBAD1	1.308	1.408	1.508
TON_DELAY = 0xC26E	2.28	2.432	2.584
TON_DELAY = others		Invalid	

(1) Channel A (PAGE 0); Channel B (PAGE 1)

7.3.4 Load Transitions

The TPSM831D31 achieves fast load transient performance using the inherent variable switching frequency characteristics. When there is a sudden load increase, the output voltage rapidly drops, which forces the PWM pulses to switch sooner and more frequently which causes the inductor current to rapidly increase. As the inductor current reaches the new load current, the device reaches a steady-state operating condition and the PWM switching resumes the steady-state frequency.

When there is a sudden load release, the output voltage rapidly rises, which forces the PWM pulses to be delayed until the inductor current reaches the new load current. At that point, the switching resumes and steady-state switching continues.

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7.3.5 Switching Frequency

The TPSM831D31 switching frequency can be selected from several values between 350 kHz to 700 kHz as shown in Table 2. The FREQUENCY_SWITCH command is used to select the desired switching frequency.

Table 2. Switching Frequency Select

FREQUENCY SELECT (kHz)	COMMAND
350	FREQUENCY_SWITCH = 0x015E
400	FREQUENCY_SWITCH = 0x0190 (factory default setting)
450	FREQUENCY_SWITCH = 0x01C2
500	FREQUENCY_SWITCH = 0x01F4
550	FREQUENCY_SWITCH = 0x0226
600	FREQUENCY_SWITCH = 0x0258
650	FREQUENCY_SWITCH = 0x028A
700	FREQUENCY_SWITCH = 0x02BC

7.3.6 RESET Function

During adaptive voltage scaling (AVS) operation, the voltage may become falsely adjusted to be out of ASIC operating range. The RESET function returns the voltage to the VBOOT voltage. When the voltage is out of ASIC operating range, the ASIC issues a RESET signal to the TPSM831D31 device. The device senses this signal and after a delay of greater than 1 µs, it sets an internal RESET_FAULT signal and sets VOUT_COMMAND to VBOOT. The device pulls the output voltage to the VBOOT level with the slew rate set by VOUT_TRANSITION_RATE command.

When the RESET pin signal goes high, the internal RESET_FAULT signal goes low.

Table 3. VBOOT

BOOT VOLTAGE SETTING (5-mV DAC)	BOOT VOLTAGE (V)
MFR_SPEC_11<7:0> = 00h	0.000
MFR_SPEC_11<7:0> = 33h	0.500
MFR_SPEC_11<7:0> = 83h	0.900
MFR_SPEC_11<7:0> = 97h	1.000
MFR_SPEC_11<7:0> = BFh	1.200

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7.3.7 VID Table

The DAC voltage VDAC can be changed via PMBus according to Table 4.

Table 4. VID Table (5 mV DAC)

VID Hex VALUE	DAC STEP	VID Hex VALUE	DAC STEP	VID Hex VALUE	DAC STEP	VID Hex VALUE	DAC STEP	VID Hex VALUE	DAC STEP	VID Hex VALUE	DAC STEP
00	0.000	2B	0.460	56	0.675	81	0.890	AC	1.105	D7	1.320
01	0.250	2C	0.465	57	0.680	82	0.895	AD	1.110	D8	1.325
02	0.255	2D	0.470	58	0.685	83	0.900	AE	1.115	D9	1.330
03	0.260	2E	0.475	59	0.690	84	0.905	AF	1.120	DA	1.335
04	0.265	2F	0.480	5A	0.695	85	0.910	B0	1.125	DB	1.340
05	0.270	30	0.485	5B	0.700	86	0.915	B1	1.130	DC	1.345
06	0.275	31	0.490	5C	0.705	87	0.920	B2	1.135	DD	1.350
07	0.280	32	0.495	5D	0.710	88	0.925	B3	1.140	DE	1.355
08	0.285	33	0.500	5E	0.715	89	0.930	B4	1.145	DF	1.360
09	0.290	34	0.505	5F	0.720	8A	0.935	B5	1.150	E0	1.365
0A	0.295	35	0.510	60	0.725	8B	0.940	B6	1.155	E1	1.370
0B	0.300	36	0.515	61	0.730	8C	0.945	B7	1.160	E2	1.375
0C	0.305	37	0.520	62	0.735	8D	0.950	B8	1.165	E3	1.380
0D	0.310	38	0.525	63	0.740	8E	0.955	B9	1.170	E4	1.385
0E	0.315	39	0.530	64	0.745	8F	0.960	BA	1.175	E5	1.390
0F	0.320	3A	0.535	65	0.750	90	0.965	BB	1.180	E6	1.395
10	0.325	3B	0.540	66	0.755	91	0.970	BC	1.185	E7	1.400
11	0.330	3C	0.545	67	0.760	92	0.975	BD	1.190	E8	1.405
12	0.335	3D	0.550	68	0.765	93	0.980	BE	1.195	E9	1.410
13	0.340	3E	0.555	69	0.770	94	0.985	BF	1.200	EA	1.415
14	0.345	3F	0.560	6A	0.775	95	0.990	C0	1.205	EB	1.420
15	0.350	40	0.565	6B	0.780	96	0.995	C1	1.210	EC	1.425
16	0.355	41	0.570	6C	0.785	97	1.000	C2	1.215	ED	1.430
17	0.360	42	0.575	6D	0.790	98	1.005	C3	1.220	EE	1.435
18	0.365	43	0.580	6E	0.795	99	1.010	C4	1.225	EF	1.440
19	0.370	44	0.585	6F	0.800	9A	1.015	C5	1.230	F0	1.445
1A	0.375	45	0.590	70	0.805	9B	1.020	C6	1.235	F1	1.450
1B	0.380	46	0.595	71	0.810	9C	1.025	C7	1.240	F2	1.455
1C	0.385	47	0.600	72	0.815	9D	1.030	C8	1.245	F3	1.460
1D	0.390	48	0.605	73	0.820	9E	1.035	C9	1.250	F4	1.465
1E	0.395	49	0.610	74	0.825	9F	1.040	CA	1.255	F5	1.470
1F	0.400	4A	0.615	75	0.830	A0	1.045	CB	1.260	F6	1.475
20	0.405	4B	0.620	76	0.835	A1	1.050	CC	1.265	F7	1.480
21	0.410	4C	0.625	77	0.840	A2	1.055	CD	1.270	F8	1.485
22	0.415	4D	0.630	78	0.845	A3	1.060	CE	1.275	F9	1.490
23	0.420	4E	0.635	79	0.850	A4	1.065	CF	1.280	FA	1.495
24	0.425	4F	0.640	7A	0.855	A5	1.070	D0	1.285	FB	1.500
25	0.430	50	0.645	7B	0.860	A6	1.075	D1	1.290	FC	1.505
26	0.435	51	0.650	7C	0.865	A7	1.080	D2	1.295	FD	1.510
27	0.440	52	0.655	7D	0.870	A8	1.085	D3	1.300	FE	1.515
28	0.445	53	0.660	7E	0.875	A9	1.090	D4	1.305	FF	1.520
29	0.450	54	0.665	7F	0.880	AA	1.095	D5	1.310		
2A	0.455	55	0.670	80	0.885	AB	1.100	D6	1.315		

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7.4 Device Functional Modes

7.4.1 Continuous Conduction Mode

The TPSM831D31 device operates in continuous conduction mode (CCM) at a fixed frequency. As programmed from the factory, phase shedding is disabled and can be enabled with a PMBus command. To begin power conversion, the EN signal and/or OPERATION command must be asserted high. Following a fault that stops power conversion, the enable contol must be pulled low and then re-asserted high to resume power conversion.

7.4.2 Operation With EN Signal Control

According to a bit value in the ON_OFF_CONFIG register, the TPSM831D31 device can be commanded to use the EN pin to enable or disable power conversion, regardless of the state of the OPERATION command. The TPSM831D31 is factory programmed to use the EN pin only. When the EN pin is pulled low, power conversion stops immediately without first waiting for a turn-off delay or actively ramping down the output voltage.

7.4.3 Operation With OPERATION Control

According to a bit value in the ON_OFF_CONFIG register, the TPSM831D31 device can be commanded to use the OPERATION command to enable or disable conversion, regardless of the state of the EN signal.

7.4.4 Operation With EN and OPERATION Control

According to a bit value in the ON_OFF_CONFIG register, the TPSM831D31 device can be commanded to require both the assertion of the EN pin, and the OPERATION command to enable or disable conversion.

7.5 Programming

7.5.1 PMBus Connections

The TPSM831D31 device can support either 100-kHz class, 400-kHz class or 1-MHz class operation, with 1.8-V or 3.3-V logic levels. Connection for the PMBus interface should follow the DC specifications given in *Section 4.3 of the System Management Bus (SMBus) Specification V3.0* . The complete SMBus specification is available from the SMBus website, smbus.org.

7.5.2 PMBus Address Selection

The PMBus slave address is set by the voltage on the ADDR pin and is selected with a resistor from the ADDR pin to GND. Refer to Table 5.

Note that TPSM831D31 uses 7 bit addressing, per the SMBus specification. Users communicating to the device using generic I^2C drivers should be aware that these 7 bits occupy the most significant bits of the first byte in each transaction, with the least significant bit being the data direction bit (0 for write operations, 1 for read operations). That is, for read transactions, the address byte is $A_6A_5A_4A_3A_2A_1A_01$ and for write operations the address byte is $A_6A_5A_4A_3A_2A_1A_00$. Refer to the SMBus specification for more information.

Table 5. PMBus Slave Address Selection

V_{ADDR} (V)	PMBus Address (7 bit binary) $A_6A_5A_4A_3A_2A_1A_0$	PMBus Address (7 bit decimal)	R_{ADDRL} (kΩ)	I^2C Address Byte (Write Operation)	I^2C Address Byte (Read Operation)
≤ 0.039 V	1011000b	88d	0	B0h	B1h
0.073 V ± 15 mV	1011001b	89d	0.453	B2h	B3h
0.122 V ± 15 mV	1011010b	90d	0.768	B4h	B5h
0.171 V ± 15 mV	1011011b	91d	1.13	B6h	B7h
0.219 V ± 15 mV	1011100b	92d	1.47	B8h	B9h
0.268 V ± 15 mV	1011101b	93d	1.87	BAh	BBh
0.317 V ± 15 mV	1011110b	94d	2.32	BCh	BDh
0.366 V ± 15 mV	1011111b	95d	2.74	BEh	BFh
0.415 V ± 15 mV	1100000b	96d	3.24	C0h	C1h
0.464 V ± 15 mV	1100001b	97d	3.74	C2h	C3h

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Table 5. PMBus Slave Address Selection (continued)

V_{ADDR} (V)	PMBus Address (7 bit binary) $A_6A_5A_4A_3A_2A_1A_0$	PMBus Address (7 bit decimal)	R_{ADDRL} (kΩ)	I^2C Address Byte (Write Operation)	I^2C Address Byte (Read Operation)
0.513 V ± 15 mV	1100010b	98d	4.32	C4h	C5h
0.562 V ± 15 mV	1100011b	99d	4.99	C6h	C7h
0.610 V ± 15 mV	1100100b	100d	5.62	C8h	C9h
0.660 V ± 15 mV	1100101b	101d	6.34	CAh	CBh
0.708 V ± 15 mV	1100110b	102d	7.15	CCh	CDh
0.757 V ± 15 mV	1100111b	103d	8.06	CEh	CFh
0.806 V ± 15 mV	1101000b	104d	9.09	D0h	D1h
0.854 V ± 15 mV	1101001b	105d	10.0	D2h	D3h
0.903 V ± 15 mV	1101010b	106d	11.3	D4h	D5h
0.952 V ± 15 mV	1101011b	107d	12.7	D6h	D7h
1.000 V ± 15 mV	1101100b	108d	14.3	D8h	D9h
1.050 V ± 15 mV	1101101b	109d	16.2	DAh	DBh
1.098 V ± 15 mV	1101110b	110d	18.2	DCh	DDh
1.147 V ± 15 mV	1101111b	111d	20.5	DEh	DFh
1.196 V ± 15 mV	1110000b	112d	23.7	E0h	E1h
1.245 V ± 15 mV	1110001b	113d	27.4	E2h	E3h
1.294 V ± 15 mV	1110010b	114d	31.6	E4h	E5h
1.343 V ± 15 mV	1110011b	115d	37.4	E6h	E7h
1.392 V ± 15 mV	1110100b	116d	45.3	E8h	E9h
1.440 V ± 15 mV	1110101b	117d	54.9	EAh	EBh
1.489 V ± 15 mV	1110110b	118d	69.8	ECh	EDh
1.540 V ± 15 mV	1110111b	119d	95.3	EEh	EFh

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7.5.3 Supported Commands

The table below summarizes the PMBus commands supported by the TPSM831D31. Only selected commands, which are most commonly used during device configuration and usage are reproduced in this document. For a full set of register maps for this device, refer to the accompanying *Technical Reference Manual*.

CMD	COMMAND NAME	DESCRIPTION	R/W, NVM	DEFAULT BEHAVIOR	DEFAULT VALUE	
					Ch. A PAGE 0	Ch. B PAGE 1
00h	PAGE	Selects which channel subsequent PMBus commands address	RW	All commands address Channel A	N/A	
01h	OPERATION	Enable or disable each channel, enter or exit margin.	RW	Conversion disabled. Margin None.	00h	00h
02h	ON_OFF_CONFIG	Configure the combination of OPERATION, and enable pin required to enable power conversion for each channel.	RW, NVM	AVR_EN/BEN pins only.	17h	17h
03h	CLEAR_FAULT	Clears all fault status registers to 00h and releases PMB_ALERT	W	Write-only	N/A	
04h	PHASE	Selects which phase of the active channel subsequent PMBus commands address	RW	Commands address all phases.	FFh	FFh
10h	WRITE_PROTECT	Used to control writing to the volatile operating memory (PMBus and restore from NVM).	RW	Writes to all commands are allowed	00h	
11h	STORE_DEFAULT_ALL	Stores all current storable register settings into NVM as new defaults.	W	Write-only	N/A	
12h	RESTORE_DEFAULT_ALL	Restores all storable register settings from NVM.	W	Write-only	N/A	
19h	CAPABILITY	Provides a way for a host system to determine key PMBus capabilities of the device.	R	1 MHz, PEC, PMB_ALERT Supported	D0h	
1Bh	SMBALERT_MASK (STATUS_VOUT)	Selects which faults/status bits may to assert PMB_ALERT	RW, NVM	All bits may assert PMB_ALERT	00h	00h
1Bh	SMBALERT_MASK (STATUS_IOUT)	Selects which faults/status bits may to assert PMB_ALERT	RW, NVM	All bits may assert PMB_ALERT	00h	00h
1Bh	SMBALERT_MASK (STATUS_INPUT)	Selects which faults/status bits may to assert PMB_ALERT	RW, NVM	LOW_VIN does not assert PMB_ALERT	08h	08h
1Bh	SMBALERT_MASK (STATUS_TEMPERATURE)	Selects which faults/status bits may to assert PMB_ALERT	RW, NVM	All bits may assert PMB_ALERT	00h	00h
1Bh	SMBALERT_MASK (STATUS_CML)	Selects which faults/status bits may to assert PMB_ALERT	RW, NVM	All bits may assert PMB_ALERT	00h	00h
1Bh	SMBALERT_MASK (STATUS_MFR_SPECIFIC)	Selects which faults/status bits may to assert PMB_ALERT	RW, NVM	All bits may assert PMB_ALERT	00h	00h
20h	VOUT_MODE	Read-only output mode indicator	R(1)	VID mode. 5 mV Step (Ch A), 5 mV Step (Ch B)	27h	27h
21h	VOUT_COMMAND	Output voltage target	RW, NVM	0.500 V (Ch A) 0.500 V (Ch B)	0033h	0033h
24h	VOUT_MAX	Sets the maximum output voltage	RW, NVM	1.520 V (Ch A) 1.520 V (Ch B)	00FFh	00FFh
25h	VOUT_MARGIN_HIGH	Load the unit with the voltage to which the output is to be changed when OPERATION command is set to “Margin High”.	RW	0.000 V (CH A) 0.000 V (Ch B)	0000h	0000h
26h	VOUT_MARGIN_LOW	Load the unit with the voltage to which the output is to be changed when OPERATION command is set to “Margin Low”.	RW	0.000 V (CH A) 0.000 V (Ch B)	0000h	0000h

(1) NVM-backed bits in the MFR_SPECIFIC or USER_DATA commands affect the reset value of these commands. Refer to the individual register maps for more detail.

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CMD	COMMAND NAME	DESCRIPTION	R/W, NVM	DEFAULT BEHAVIOR	DEFAULT VALUE	
					Ch. A PAGE 0	Ch. B PAGE 1
27h	VOUT_TRANSITION_RATE	Used to set slew rate settings for output voltage updates	RW, NVM	2.5 mV/µs (Ch A) 2.5 mV/µs (Ch B)	E028h	E028h
28h	VOUT_DROOP	The VOUT_DROOP sets the rate, in mV/A (mΩ) at which the output voltage decreases (or increases) with increasing (or decreasing) output current for use with Adaptive Voltage Positioning	RW, NVM	0.000 mΩ (Ch A) 0.000 mΩ (Ch B)	D000h	D000h
29h	VOUT_SCALE_LOOP	Used for scaling the VID code	RW, NVM	1.000 (Ch A) 1.000 (Ch B)	E808h	E808h
2Ah	VOUT_SCALE_MONITOR	Used for scaling output voltage telemetry	RW, NVM	1.000 (Ch A) 1.000 (Ch B)	E808h	E808h
2Bh	VOUT_MIN	Sets the minimum output voltage	RW, NVM	0.000 V (Ch A) 0.000 V (Ch B)	0000h	0000h
33h	FREQUENCY_SWITCH	Sets the switching frequency	RW, NVM	400 kHz (Ch A) 400 kHz (Ch B)	0190h	0190h
35h	VIN_ON	Sets value of input voltage at which the device should start power conversion.	RW, NVM	7.25 V	F01Dh	
38h	IOUT_CAL_GAIN	Sets the ratio of voltage at the current sense pins to the sensed current.	RW, NVM	5.0625 mΩ (Ch A) 5.0625 mΩ (Ch B)	D144h	D144h
39h	IOUT_CAL_OFFSET	Used to null offsets in the output current sensing circuit	RW, NVM	0.000 A (Ch A) 0.000 A (Ch B) (All Phases)	E800h	E800h
40h	VOUT_OV_FAULT_LIMIT	Sets the value of the sensed output voltage which triggers an output overvoltage fault	R	1.520 V (Ch A) 1.520 V (Ch B)	00FFh	00FFh
41h	VOUT_OV_FAULT_RESPONSE	Sets the converter response to an output overvoltage event	R	Shutdown, do not restart	80h	80h
44h	VOUT_UV_FAULT_LIMIT	Sets the value of the sensed output voltage which triggers an output undervoltage fault	R	0.000 V (Ch A) 0.000 V (Ch B)	0000h	0000h
45h	VOUT_UV_FAULT_RESPONSE	Sets the converter response to an output undervoltage event	RW, NVM	Shutdown, do not restart	80h	80h
46h	IOUT_OC_FAULT_LIMIT	Sets the output overcurrent fault limit, in amperes	RW, NVM(1)	180 A (Ch A) 60 A (Ch B)	00B4h	003Ch
47h	IOUT_OC_FAULT_RESPONSE	Defines the overcurrent fault response	RW, NVM	Shutdown, do not restart	C0h	C0h
4Ah	IOUT_OC_WARN_LIMIT	Sets the output overcurrent warning limit, in amperes	RW, NVM(1)	120 A (Ch A) 40 A (Ch B)	0078h	0028h
4Fh	OT_FAULT_LIMIT	Sets the output overtemperature fault limit, in degrees Celsius.	RW, NVM(1)	135 °C (Ch A) 135 °C (Ch B)	0087h	0087h
50h	OT_FAULT_RESPONSE	Defines the overtemperature fault response	RW, NVM	Shutdown, do not restart	80h	80h
51h	OT_WARN_LIMIT	Sets the output overtemperature warning limit, in degrees Celsius.	RW	105 °C (Ch A) 105 °C (Ch B)	0069h	0069h
55h	VIN_OV_FAULT_LIMIT	Sets the VIN overvoltage fault limit, in volts	RW, NVM	17.000 V	0011h	
56h	VIN_OV_FAULT_RESPONSE	Defines the VIN overvoltage fault response	R	Continue Uninterrupted	00h	
59h	VIN_UV_FAULT_LIMIT	Sets the VIN undervoltage fault limit, in volts	RW, NVM	6.500 V	F80Dh	
5Ah	VIN_UV_FAULT_RESPONSE	Defines the VIN undervoltage fault response	R	Shutdown, do not restart	C0h	
5Bh	IIN_OC_FAULT_LIMIT	Sets the input current overcurrent fault limit, in amperes	RW, NVM	40.0 A	F850h	
5Ch	IIN_OC_FAULT_RESPONSE	Defines the input overcurrent fault response	R	Shutdown, do not restart	C0h	
5Dh	IIN_OC_WARN_LIMIT	Sets the input current overcurrent warning limit, in amperes	RW, NVM	32.0 A	F840h	

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CMD	COMMAND NAME	DESCRIPTION	R/W, NVM	DEFAULT BEHAVIOR	DEFAULT VALUE	
					Ch. A PAGE 0	Ch. B PAGE 1
60h	TON_DELAY	Sets the time, in milliseconds, from when a start condition is received (as programmed by the ON_OFF_CONFIG command) until the output voltage starts to rise	RW, NVM	0.480 ms (Ch A) 0.896 ms (Ch B)	B1ECh	B396h
6Bh	PIN_OP_WARN_LIMIT	The PIN_OP_WARN_LIMIT command sets the value of the input power, in watts, that causes a warning that the input power is high	RW	450 W	08E1h	
78h	STATUS_BYTE	PMBus read-only status and flag bits.	RW	Current Status	N/A	N/A
79h	STATUS_WORD	PMBus read-only status and flag bits.	RW	Current Status	N/A	N/A
7Ah	STATUS_VOUT	PMBus read-only status and flag bits.	RW	Current Status	N/A	N/A
7Bh	STATUS_IOUT	PMBus read-only status and flag bits.	RW	Current Status	N/A	N/A
7Ch	STATUS_INPUT	PMBus read-only status and flag bits.	RW	Current Status	N/A	
7Dh	STATUS_TEMPERATURE	PMBus read-only status and flag bits.	RW	Current Status	N/A	N/A
7Eh	STATUS_CML	PMBus read-only status and flag bits.	RW	Current Status	N/A	
80h	STATUS_MFR_SPECIFIC	PMBus read-only status and flag bits.	RW	Current Status	N/A	N/A
88h	READ_VIN	Returns the input voltage in volts	R	Current Status	N/A	
89h	READ_IIN	Returns the input current in amperes	R	Current Status	N/A	
8Bh	READ_VOUT	Returns the output voltage in VID format	R	Current Status	N/A	N/A
8Ch	READ_IOUT	Returns the output current in amperes	R	Current Status	N/A	N/A
8Dh	READ_TEMPERATURE_1	Returns the highest power stage temperature in °C	R	Current Status	N/A	N/A
96h	READ_POUT	Returns the output power in Watts	R	Current Status	N/A	N/A
97h	READ_PIN	Returns the input power in Watts	R	Current Status	N/A	
98h	PMBUS_REVISION	Returns the version of the PMBus specification to which this device complies	R	PMBus 1.3 Part I, Part II	33h	
99h	MFR_ID	Loads the unit with bits that contain the manufacturer's ID	RW, NVM	TI	5449h	
9Ah	MFR_MODEL	Loads the unit with bits that contain the manufacturer's model number	RW, NVM	3+1 Phase Configuration	4331h	
9Bh	MFR_REVISION	Loads the unit with bits that contain the manufacturer's model revision	RW, NVM	Rev 1.0	0001h	
9Dh	MFR_DATE	Loads the unit with bits that contain the manufacture date	RW, NVM	July 2018	1207h	
9Eh	MFR_SERIAL	NVM Checksum	R	NVM checksum	679E8B7Dh	
ADh	IC_DEVICE_ID	Returns a number indicating the part number of the device	R	TPSM831D31	81h	
AEh	IC_DEVICE_REV	Returns a number indicating the device revision	R	Rev 1.0	00h	
B0h	USER_DATA_00	Used for batch NVM programming.	RW NVM	Current configuration	Factory Default Settings	
B1h	USER_DATA_01	Used for batch NVM programming.	RW NVM	Current configuration	Factory Default Settings	
B2h	USER_DATA_02	Used for batch NVM programming.	RW NVM	Current configuration	Factory Default Settings	
B3h	USER_DATA_03	Used for batch NVM programming.	RW NVM	Current configuration	Factory Default Settings	
B4h	USER_DATA_04	Used for batch NVM programming.	RW NVM	Current configuration	Factory Default Settings	
B5h	USER_DATA_05	Used for batch NVM programming.	RW NVM	Current configuration	Factory Default Settings	
B6h	USER_DATA_06	Used for batch NVM programming.	RW NVM	Current configuration	Factory Default Settings	

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CMD	COMMAND NAME	DESCRIPTION	R/W, NVM	DEFAULT BEHAVIOR	DEFAULT VALUE	
					Ch. A PAGE 0	Ch. B PAGE 1
B7h	USER_DATA_07	Used for batch NVM programming.	RW NVM	Current configuration	Factory Default Settings	
B8h	USER_DATA_08	Used for batch NVM programming.	RW NVM	Current configuration	Factory Default Settings	
B9h	USER_DATA_09	Used for batch NVM programming.	RW NVM	Current configuration	Factory Default Settings	
BAh	USER_DATA_10	Used for batch NVM programming.	RW NVM	Current configuration	Factory Default Settings	
BBh	USER_DATA_11	Used for batch NVM programming.	RW NVM	Current configuration	Factory Default Settings	
BCh	USER_DATA_12	Used for batch NVM programming.	RW NVM	Current configuration	Factory Default Settings	
D0h	MFR_SPECIFIC_00	Configures per-phase overcurrent levels, current share thresholds, and other miscellaneous settings.	RW NVM	Misc. configuration, See register maps	003Eh	203Dh
D3h	MFR_SPECIFIC_03	Returns information regarding current imbalance warnings for each phase	R	Current status	N/A	N/A
D4h	MFR_SPECIFIC_04	Returns the output voltage for the active channel, in linear format	R	Current status	N/A	N/A
D5h	MFR_SPECIFIC_05	Used to trim the output voltage of the active channel, by applying an offset to the currently selected VID code.	RW NVM	1.25 mV offset (Ch A and Ch B)	01h	01h
D6h	MFR_SPECIFIC_06	Configures dynamic load line options for both channels, and selects Auto-DCM operation.	RW NVM	Misc. configuration, See register maps	0605h	1000h
D7h	MFR_SPECIFIC_07	Configures the internal loop compensation for both channels.	RW NVM	Misc. configuration, See to register maps	0946h	01C6h
D8h	MFR_SPECIFIC_08	Used to identify catastrophic faults which occur first, and store this information to NVM	RW NVM	Current status	00h	00h
D9h	MFR_SPECIFIC_09	Used to configure non-linear transient performance enhancements such as undershoot reduction (USR)	RW NVM	Misc. configuration, See register maps	46C5h	06C7h
DAh	MFR_SPECIFIC_10	Used to configure input current sensing, and set the maximum output current	RW NVM	Misc. configuration, See register maps	C878h	0028h
DBh	MFR_SPECIFIC_11	Boot-up VID code for each channel	RW NVM	VID 051d (Ch A) VID 051d (Ch B)	33h	33h
DCh	MFR_SPECIFIC_12	Used to configure input current sensing and other miscellaneous settings	RW NVM	Misc. configuration, See register maps	C570h	07F0
DDh	MFR_SPECIFIC_13	Used to configure output voltage slew rates, DAC stepsize, and other miscellaneous settings.	RW NVM	Misc. configuration, See register maps	9CE5h	00E5h
DEh	MFR_SPECIFIC_14	Used to configure dynamic phase shedding, and compensation ramp amplitude, and dynamic ramp amplitude during USR, and different power states	RW NVM	Misc. configuration, See register maps	0007h	0007h
DFh	MFR_SPECIFIC_15	Used to configure dynamic phase shedding.	RW NVM	Misc. configuration, See register maps	1FFAh	0000h
E4h	MFR_SPECIFIC_20	Used to set the maximum operational phase number, on-the-fly.	RW NVM	Misc. configuration, See register maps	Hardware Configured	
F0h	MFR_SPECIFIC_32	Used to set the input over-power warning	RW	450 W	00E1h	
FAh	MFR_SPECIFIC_42	NVM Security	RW NVM	NVM Security Key	0000h	

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7.5.4 Commonly Used PMBus Commands

The following sections describe the most commonly used PMBus commands and their usage in the configuration, operation and testing of TPSM831D31 power solutions:

- Voltage, Current, Power, and Temperature Readings
- Output Current Sense and Calibration
- Output Voltage Margin Testing
- Loop Compensation
- Converter Protection and Response
- Dynamic Phase Shedding
- NVM Programming
- NVM Security
- Black Box Fault Recording
- Board Identification and Inventory Tracking
- Status Reporting

7.5.5 Voltage, Current, Power, and Temperature Readings

Using an internal ADC, the TPSM831D31 provides a full set of telemetry capabilities, allowing the user to read back critical information about the converter's input voltage, input current, input power, output voltage, output current, output power and temperature. The table below summarizes the available commands and their formats. Register maps for each command are included.

Table 6. Telemetry Functions

Command	Description	Format	Units	Channel/Phase
READ_VIN	Input voltage telemetry	Linear	V	Shared, Channel A and B
READ_IIN	Input current telemetry	Linear	A	Shared, Channel A and B
READ_VOUT	Output voltage telemetry (VID format)	VID	VID Code	Per Channel
READ_IOUT	Output current telemetry	Linear	A	Per Channel and Per Phase
READ_TEMPERATURE_1	Power stage temperature telemetry	Linear	°C	Per Channel, Highest phase temperature only
READ_POUT	Output power telemetry	Linear	W	Per Channel
READ_PIN	Input power telemetry	Linear	W	Shared, Channel A and B
MFR_SPECIFIC_04	Output voltage telemetry (linear format)	Linear	V	Per Channel

7.5.5.1 (88h) READ_VIN

The READ_VIN command returns the input voltage in volts. The two data bytes are formatted in the Linear Data format. The refresh rate is 1200 µs. This command should be accessed through Read Word transactions, and is shared between channel A and channel B.

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
READ_VIN_EXP					READ_VIN_MAN		
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
READ_VIN_MAN							

LEGEND: R/W = Read/Write; R = Read only

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READ_VIN

Table 7. READ_VIN Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	READ_VIN_EXP	R	Current Status	Linear two's complement format exponent.
10:0	READ_VIN_MAN	R	Current Status	Linear two's complement format mantissa.

7.5.5.2 (89h) READ_IIN

The READ_IIN command returns the input current in amperes. The refresh rate is 100 µs. The two data bytes are formatted in the Linear Data format. This command should be accessed through Read Word transactions, and is shared between channel A and channel B.

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
READ_IIN_EXP					READ_IIN_MAN		
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
READ_IIN_MAN							

LEGEND: R/W = Read/Write; R = Read only

READ_IIN

Table 8. READ_IIN Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	READ_IIN_EXP	R	Current Status	Linear two's complement format exponent.
10:0	READ_IIN_MAN	R	Current Status	Linear two's complement format mantissa.

7.5.5.3 (8Bh) READ_VOUT

The READ_VOUT command returns the actual, measured output voltage. The two data bytes are formatted in the VID Data format, and the refresh rate is 1200 us. This command should be accessed through Read Word transactions. READ_VOUT is a paged register. In order to access READ_VOUT command for channel A, PAGE must be set to 00h. In order to access READ_VOUT register for channel B, PAGE must be set to 01h.

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
READ_VOUT_VID							

LEGEND: R/W = Read/Write; R = Read only

READ_VOUT

Table 9. READ_VOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	READ_VOUT_VID	R	Current Status	Output voltage, VID format

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7.5.5.4 (8Ch) READ_IOUT

The READ_IOUT command returns the output current in amperes.

READ_IOUT is a linear format command.

READ_IOUT is a paged register. In order to access READ_IOUT for channel A, PAGE must be set to 00h. In order to access the READ_IOUT register for channel B, PAGE must be set to 01h. For simultaneous access of channels A and B, the PAGE command must be set to FFh. READ_IOUT is also a phased register. Depending on the configuration of the design, for channel A, PHASE must be set to 00h to access Phase 1, 01h to access Phase 2, etc... PHASE must be set to FFh to access all phases simultaneously. PHASE may also be set to 80h to readack the total phase current (sum of all active phase currents for the active channel) measurement, as described in Output Current Sense and Calibration. Note that READ_IOUT is only a phased command for Channel A (PAGE 0).

The READ_IOUT command must be accessed through Read Word transactions.

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
READ_IOUT_EXP					READ_IOUT_MAN		
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
READ_IOUT_MAN							

LEGEND: R/W = Read/Write; R = Read only

READ_IOUT

Table 10. READ_IOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	READ_IOUT_EXP	R	Current Status	Linear two's complement format exponent.
10:0	READ_IOUT_MAN	R	Current Status	Linear two's complement format mantissa.

Attempts to write to this command results in invalid transactions. The device ignores the invalid data, sets the appropriate flags in STATUS_CML and STATUS_WORD, and asserts the PMB_ALERT signal to notify the system host of an invalid transaction.

7.5.5.5 (8Dh) READ_TEMPERATURE_1

The READ_TEMPERATURE_1 command returns the temperature in degree Celsius. The two data bytes are formatted in the Linear Data format. The refresh rate is 1200 µs.

READ_TEMPERATURE_1 is a linear format command.

READ_TEMPERATURE_1 is a paged register. In order to access OPERATION command for channel A, READ_TEMPERATURE_1 must be set to 00h. In order to access READ_TEMPERATURE_1 register for channel B, PAGE must be set to 01h. For simultaneous access of channels A and B, the PAGE command must be set to FFh.

The READ_TEMPERATURE_1 command must be accessed through Read Word transactions.

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
READ_TEMP_EXP					READ_TEMP_MAN		
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
READ_TEMP_MAN							

LEGEND: R/W = Read/Write; R = Read only

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READ_TEMPERATURE_1

Table 11. READ_TEMPERATURE_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	READ_TEMP_EXP	R	Current Status	Linear two's complement format exponent.
10:0	READ_TEMP_MAN	R	Current Status	Linear two's complement format mantissa.

Attempts to write to this command results in invalid transactions. The device ignores the invalid data, sets the appropriate flags in STATUS_CML and STATUS_WORD, and asserts the PMB_ALERT signal to notify the system host of an invalid transaction

7.5.5.6 (96h) READ_POUT

The READ_POUT command returns the calculated output power, in watts for the active channel. The refresh rate is 1200 µs.

READ_POUT is a linear format command.

READ_POUT is a paged register. In order to access READ_POUT command for channel A, PAGE must be set to 00h. In order to access READ_POUT register for channel B, PAGE must be set to 01h. For simultaneous access of channels A and B, the PAGE command must be set to FFh.

The READ_POUT command must be accessed through Read Word transactions.

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
READ_POUT_EXP					READ_POUT_MAN		
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
READ_POUT_MAN							

LEGEND: R/W = Read/Write; R = Read only

READ_POUT

Table 12. READ_POUT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	READ_POUT_EXP	R	Current Status	Linear two's complement format exponent.
10:0	READ_POUT_MAN	R	Current Status	Linear two's complement format mantissa.

Attempts to write to this command results in invalid transactions. The device ignores the invalid data, sets the appropriate flags in STATUS_CML and STATUS_WORD, and asserts the PMB_ALERT signal to notify the system host of an invalid transaction

7.5.5.7 (97h) READ_PIN

The READ_PIN command returns the calculated input power. The refresh rate is 1200 µs.

READ_PIN is a linear format command.

The READ_PIN command must be accessed through Read Word transactions.

The READ_PIN command is shared between Channel A and Channel B. All transactions to this command will affect both channels regardless of the PAGE command.

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15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
READ_PIN_EXP					READ_PIN_MAN		
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
READ_PIN_MAN							

LEGEND: R/W = Read/Write; R = Read only

READ_PIN

Table 13. READ_PIN Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	READ_PIN_EXP	R	Current Status	Linear two's complement format exponent.
10:0	READ_PIN_MAN	R	Current Status	Linear two's complement format mantissa.

7.5.5.8 (D4h) MFR_SPECIFIC_04

The MFR_SPECIFIC_04 command is used to return the output voltage for the active channel, in the **linear** format (READ_VOUT uses VID format).

The MFR_SPECIFIC_04 command must be accessed through Read Word transactions.

MFR_SPECIFIC_04 is a Linear format command.

MFR_SPECIFIC_04 is a paged register. In order to access MFR_SPECIFIC_04 command for channel A, PAGE must be set to 00h. In order to access the MFR_SPECIFIC_04 register for channel B, PAGE must be set to 01h.

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
VOUT_LIN_EXP					VOUT_LIN_MAN		
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
VOUT_LIN_MAN							

LEGEND: R/W = Read/Write; R = Read only

MFR_SPECIFIC_04

Table 14. MFR_SPECIFIC_04 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	VOUT_LIN_EXP	R	Current Status	Linear format two's complement exponent.
10:0	VOUT_LIN_MAN	R	Current Status	Linear format two's complement mantissa.

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7.5.6 Output Current Sense and Calibration

The READ_IOUT command may be used to read the individual phase currents, and the total channel current.

7.5.6.1 Reading Individual Phase Currents

Using the PAGE and PHASE commands, the TPSM831D31 can be configured to return output current information for each individual phase. The examples below demonstrate this process:

Example #1: Read back the output current of Channel A, First Phase

1. Select Channel A. Write PAGE to 00h
2. Select first phase. Write PHASE to 00h
3. Read READ_IOUT

Example #2: Read back the output current of Channel B, Second Phase

1. Select Channel B. Write PAGE to 01h
2. Select second phase. Write PHASE to 01h
3. Read READ_IOUT

7.5.6.1.1 Reading Total Current

When the PHASE command is set to 80h, the TPSM831D31 device is configured to return the total channel current (sum of individual phase currents) in response to the READ_IOUT command.

Example: Read the Total Output Current of Channel A

1. Select Channel A. Write PAGE to 00h
2. Select total current measurement. Write PHASE to 80h
3. Read READ_IOUT

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7.5.7 Output Voltage Margin Testing

The TPSM831D31 provides several commands to enable voltage margin testing.

The upper two MARGIN bits in the OPERATION command can be used to toggle the active channel between three states:

1. **Margin None (MARGIN = 0000b).** The output voltage target is equal to VOUT_COMMAND.
2. **Margin Low (MARGIN = 01xxb).** The output voltage target is equal to VOUT_MARGIN_LOW.
3. **Margin High (MARGIN = 10xxb).** The output voltage target is equal to VOUT_MARGIN_HIGH.

In order to use OPERATION, the active channel must be configured for to respect the OPERATION command, via ON_OFF_CONFIG. Output voltage transitions will occur at the slew rate defined by VOUT_TRANSITION_RATE.

Table 15. Slew Rate Settings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SL_{SET}	Slew rate setting	VOUT_TRANSITION_RATE = 0xE050	5	6	7	mV/µs
		VOUT_TRANSITION_RATE = 0xE0A0	10	12	14	mV/µs
		VOUT_TRANSITION_RATE = 0xE0F0	15	18		mV/µs
		VOUT_TRANSITION_RATE = 0xE140	20	24		mV/µs
		VOUT_TRANSITION_RATE = 0xE190	25	30		mV/µs
		VOUT_TRANSITION_RATE = 0xE1E0	30	36		mV/µs
		VOUT_TRANSITION_RATE = 0xE230	35	42		mV/µs
		VOUT_TRANSITION_RATE = 0xE280	40	48		mV/µs
		VOUT_TRANSITION_RATE = 0xE005	0.3125			mV/µs
		VOUT_TRANSITION_RATE = 0xE00A	0.625			mV/µs
		VOUT_TRANSITION_RATE = 0xE00F	0.9375			mV/µs
		VOUT_TRANSITION_RATE = 0xE014	1.25			mV/µs
		VOUT_TRANSITION_RATE = 0xE019	1.5625			mV/µs
		VOUT_TRANSITION_RATE = 0xE01E	1.875			mV/µs
		VOUT_TRANSITION_RATE = 0xE023	2.1875			mV/µs
		VOUT_TRANSITION_RATE = 0xE028	2.5			mV/µs
		VOUT_TRANSITION_RATE = others		Invalid data		mV/µs
SL_F	AVSP and BVSP slew rate SetVID_Fast			SL_{SET}		mV/µs
SL_{S1}	AVSP and BVSP slew rate slow			SL_{SET} / 4		mV/µs
				SL_{SET} / 2		mV/µs
SL_{SS}	AVSP and BVSP slew rate slew rate soft-start	MFR_SPEC_13<8> = 0b		SL_{SET} / 4		mV/µs
		MFR_SPEC_13<8> = 1b		SL_{SET} / 16		mV/µs

The lower two MARGIN bits in the OPERATION command select overvoltage/undervoltage fault handling during margin testing:

1. **Ignore Faults (MARGIN = xx01b) .** Overvoltage/Undervoltage faults will not trigger during margin tests.
2. **Act on Faults (MARGIN = xx10b).** Overvoltage/Undervoltage faults will trigger during margin tests.

Example: Output Voltage Margin Testing (Ignore Faults)

1. Write to the PAGE command to select the desired channel (E.g. PAGE = 00h for channel A).
2. Write VOUT_COMMAND to the desired VID code during Margin None operation.
3. Write VOUT_MARGIN_LOW to the desired VID code during Margin Low operation.
4. Write VOUT_MARGIN_HIGH to the desired VID code during Margin High operation.
5. Write MFR_SPECIFIC_02 to 01h to ensure that the PMBus interface has control of the output voltage.
6. Set the CMD bit in OPERATION to 1b to ensure the device is configured to respect the OPERATION command.
7. Margin None. Write OPERATION to 80h.

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8. Margin Low. Write OPERATION to 94h.
9. Margin High. Write OPERATION to A4h.

7.5.7.1 (01h) OPERATION

The OPERATION command is used to turn the device output on or off in conjunction with the input from the AVR_EN pin for channel A, and BEN pin for channel B, acc ording to the configuration of the ON_OFF_CONFIG command. It is also used to set the output voltage to the upper or lower MARGIN levels.

OPERATION is a paged register. In order to access OPERATION command for channel A, PAGE must be set to 00h. In order to access OPERATION register for channel B, PAGE must be set to 01h. For simultaneous access of channels A and B, the PAGE command must be set to FFh.

The OPERATION command must be accessed through Read Byte/Write Byte transactions.

7	6	5	4	3	2	1	0
RW	R	RW	RW	RW	RW	RW	RW
ON	0	MARGIN				0	0

LEGEND: R/W = Read/Write; R = Read only

OPERATION

Table 16. OPERATION Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ON	RW	0b	Enable/disable power conversion for the currently selected channel(s) according to the PAGE command, when the ON_OFF_CONFIG command is configured to require input from the ON bit for output control. Note that there may be several other requirements that must be satisfied before the currently selected channel(s) can begin converting power (e.g. input voltages above UVLO thresholds, AVR_EN/BEN pins high if required by ON_OFF_CONFIG, etc...) 0b: Disable power conversion 1b: Enable power conversion
5:2	MARGIN	RW	0000b	Set the output voltage to either the value selected by the VOUT_MARGIN_HIGH or MARGIN_LOW commands, for the currently selected channel(s), according to the PAGE command. 0000b: Margin Off. Output voltage is set to the value of VOUT_COMMAND 0101b: Margin Low (Ignore Fault). Output voltage is set to the value of VOUT_MARGIN_LOW. 0110b: Margin Low (Act on Fault). Output voltage is set to the value of VOUT_MARGIN_LOW. 1001b: Margin High (Ignore Fault). Output voltage is set to the value of VOUT_MARGIN_HIGH 1010b: Margin High (Act on Fault). Output voltage is set to the value of VOUT_MARGIN_HIGH.
1:0	0	RW	00b	These bits are writeable but should always be set to 00b.

Note that the VOUT_MAX_WARN bit in STATUS_VOUT can be caused by a margin operation, if "Act on Fault" is selected, and the VOUT_MARGIN_HIGH/VOUT_MARGIN_LOW value loaded by the margin operation exceeds the value of VOUT_COMMAND.

7.5.7.2 (26h) VOUT_MARGIN_LOW

The VOUT_MARGIN_LOW command loads the unit with the voltage to which the output is to be changed when the OPERATION command is set to “Margin Low”.

VOUT_MARGIN_LOW is a VID format command. The VOUT_MARGIN_LOW command must be accessed through Read Word/Write Word transactions.

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VOUT_MARGIN_LOW is a paged register. In order to access VOUT_MARGIN_LOW for channel A, PAGE must be set to 00h. In order to access the VOUT_MARGIN_LOW register for channel B, PAGE must be set to 01h. For simultaneous access of channels A and B, the PAGE command must be set to FFh.

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
VOUT_MARGL_VID							

LEGEND: R/W = Read/Write; R = Read only

VOUT_MARGIN_LOW

Table 17. VOUT_MARGIN_LOW Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	VOUT_MARGL_VID	RW	00h	Used to set the output voltage to be loaded when the active PAGE is set to Margin Low, in VID format.

7.5.7.3 (25h) VOUT_MARGIN_HIGH

The VOUT_MARGIN_HIGH command loads the unit with the voltage to which the output is to be changed when the OPERATION command is set to “Margin High”.

VOUT_MARGIN_HIGH is a VID format command. The VOUT_MARGIN_HIGH command must be accessed through Read Word/Write Word transactions.

VOUT_MARGIN_HIGH is a paged register. In order to access VOUT_MARGIN_HIGH for channel A, PAGE must be set to 00h. In order to access the VOUT_MARGIN_HIGH register for channel B, PAGE must be set to 01h. For simultaneous access of channels A and B, the PAGE command must be set to FFh.

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
VOUT_MARGH_VID							

LEGEND: R/W = Read/Write; R = Read only

VOUT_MARGIN_HIGH

Table 18. VOUT_MARGIN_HIGH Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	VOUT_MARGH_VID	RW	00h	Used to set the output voltage to be loaded when the active PAGE is set to Margin High, in VID format.

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7.5.8 Loop Compensation

The TPSM831D31 provides several options for tuning the output voltage feedback and response to transients. These may be configured by programming the MFR_SPECIFIC_07, VOUT_DROOP, and MFR_SPECIFIC_14. Several such parameters may be configured through these commands:

- **DC Load Line** - Selects the DC shift in output voltage corresponding to increased output current. The DC load line affects both the final value the output voltage settles to, as well as the settling time. Use the VOUT_DROOP command to select the DC load line.
- **Integration Time Constant** - In order to maintain DC accuracy, the control loop includes an integration stage. Use MFR_SPECIFIC_07 to select the integration time constant.
- **Integration Path Gain** - The gain of the integration and AC paths may be selected independently. The AC and DC gains both affect the small-signal bandwidth of the converter. Use MFR_SPECIFIC_07 to select the integration path gain.
- **AC Load Line** - Selects the AC response to output voltage error. The AC load line affects the settling and response time following a load transient event. MFR_SPECIFIC_07 Use the MFR_SPECIFIC_07 command to select the AC load line.
- **AC Path Gain** - The gain of the integration and AC paths may be selected independently. The AC and DC gains both affect the small-signal bandwidth of the converter. Use MFR_SPECIFIC_07 to select the AC path gain.
- **Ramp Amplitude** - Smaller ramp settings result in faster response, but may also lead to increased frequency jitter. Likewise, large ramp settings result in lower frequency jitter, but may be slightly slower to respond to changing conditions. The ramp setting also affects the small-signal bandwidth of the converter. Use MFR_SPECIFIC_14 to select the ramp high setting.

Table 19. Dynamic Integration and Undershoot Reduction (T_A = 25°C)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DYN}	Dynamic integration voltage setting	MFR_SPEC_12<10:8> = 000b;	90	100	116	mV
		MFR_SPEC_12<10:8> = 001b;	135	150	175	mV
		MFR_SPEC_12<10:8> = 010b;	175	200	230	mV
		MFR_SPEC_12<10:8> = 011b;	225	250	285	mV
		MFR_SPEC_12<10:8> = 100b;	270	300	345	mV
		MFR_SPEC_12<10:8> = 101b;	315	350	400	mV
		MFR_SPEC_12<10:8> = 110b;	360	400	455	mV
		MFR_SPEC_12<10:8> = 111b;		OFF		mV
t_{DINT}	Dynamic integration time constant(1)	MFR_SPEC_12<7:4> = 0000b;		1		µs
		MFR_SPEC_12<7:4> = 0001b;		2		µs
		MFR_SPEC_12<7:4> = 0010b;		3		µs
		MFR_SPEC_12<7:4> = 0011b;		4		µs
		MFR_SPEC_12<7:4> = 0100b;		5		µs
		MFR_SPEC_12<7:4> = 0101b;		6		µs
		MFR_SPEC_12<7:4> = 0110b;		7		µs
		MFR_SPEC_12<7:4> = 0111b;		8		µs
		MFR_SPEC_12<7:4> = 1000b;		12		µs
		MFR_SPEC_12<7:4> = 1001b;		13		µs
		MFR_SPEC_12<7:4> = 1010b;		14		µs
		MFR_SPEC_12<7:4> = 1011b;		15		µs
		MFR_SPEC_12<7:4> = 1100b;		16		µs
		MFR_SPEC_12<7:4> = 1101b;		17		µs
		MFR_SPEC_12<7:4> = 1110b;		18		µs
		MFR_SPEC_12<7:4> = 1111b;		19		µs

(1) Specified by design. Not production tested.

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Table 19. Dynamic Integration and Undershoot Reduction (T_A = 25°C) (continued)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{USR2}	USR level 2 voltage setting	MFR_SPEC_09<14:12> = 000b;	120	140	160	mV
		MFR_SPEC_09<14:12> = 001b;	155	180	205	mV
		MFR_SPEC_09<14:12> = 010b;	190	220	245	mV
		MFR_SPEC_09<14:12> = 011b;	230	260	290	mV
		MFR_SPEC_09<14:12> = 100b;	265	300	335	mV
		MFR_SPEC_09<14:12> = 101b;	300	340	375	mV
		MFR_SPEC_09<14:12> = 110b;	335	380	420	mV
		MFR_SPEC_09<14:12> = 111b;		OFF		mV
V_{USR1}	USR level 1 voltage setting	MFR_SPEC_09<2:0> = 000b;	70	90	110	mV
		MFR_SPEC_09<2:0> = 001b;	100	120	140	mV
		MFR_SPEC_09<2:0> = 010b;	130	150	170	mV
		MFR_SPEC_09<2:0> = 011b;	160	180	205	mV
		MFR_SPEC_09<2:0> = 100b;	185	210	240	mV
		MFR_SPEC_09<2:0> = 101b;	215	240	270	mV
		MFR_SPEC_09<2:0> = 110b;	240	270	305	mV
		MFR_SPEC_09<2:0> = 111b;		OFF		mV
PH_{USR1}	Maximum phase added in USR level 1 (1)	MFR_SPEC_09<5> = 0b;		3		phases
		MFR_SPEC_09<5> = 1b;		4		phases
$V_{OUSRHYS}$	Dynamic integration/USR voltage hysteresis	MFR_SPEC_09<4:3> = 00b;	2	5	9	mV
		MFR_SPEC_09<4:3> = 01b;	5	10	15	mV
		MFR_SPEC_09<4:3> = 10b;	10	15	20	mV
		MFR_SPEC_09<4:3> = 11b;	15	20	25	mV

Table 20. Ramp Selections

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{RAMP}	RAMP Setting	MFR_SPEC_14<2:0> = 000b	30	40	55	mV
		MFR_SPEC_14<2:0> = 001b	70	80	95	mV
		MFR_SPEC_14<2:0> = 010b	110	120	135	mV
		MFR_SPEC_14<2:0> = 011b	150	160	175	mV
		MFR_SPEC_14<2:0> = 100b	190	200	215	mV
		MFR_SPEC_14<2:0> = 101b	230	240	255	mV
		MFR_SPEC_14<2:0> = 110b	270	280	300	mV
		MFR_SPEC_14<2:0> = 111b	305	320	335	mV

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7.5.8.1 (D7h) MFR_SPECIFIC_07

The MFR_SPECIFIC_07 command is used to configure the internal loop compensation for both channels. The MFR_SPECIFIC_07 command must be accessed through Write Word/Read Word transactions.

MFR_SPECIFIC_07 is a paged register. In order to access MFR_SPECIFIC_07 command for channel A, PAGE must be set to 00h. In order to access the MFR_SPECIFIC_07 register for channel B, PAGE must be set to 01h.

15	14	13	12	11	10	9	8
R	R	RW	RW	RW	RW	RW	RW
0	0	INT_GAIN		INT_TC			
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
AC_GAIN		ACLL					

LEGEND: R/W = Read/Write; R = Read only

MFR_SPECIFIC_07

Table 21. MFR_SPECIFIC_07 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	Not used	R	0	Not used and set to 0.
13:12	INT_GAIN	RW	NVM	Integration path gain. See Table 22.
11:8	INT_TC	RW	NVM	Integration time constant. See Table 23.
7:6	AC_GAIN	RW	NVM	AC path gain. See Table 24.
5:0	ACLL	RW	NVM	AC Load Line. See Table 25.

Table 22. Integration path gain settings

INT_GAIN (binary)	Integration path gain (V/V)
00b	2 × AC_GAIN
01b	1 × AC_GAIN
10b	0.66 × AC_GAIN
11b	0.5 × AC_GAIN

Table 23. Integration time constant settings

INT_TC (binary)	Time constant (µs)
0000b	5
0001b	10
0010b	15
0011b	20
0100b	25
0101b	30
0110b	35
0111b	40
1000b	1
1001b	2
1010b	3
1011b	4
1100b	5
1101b	6
1110b	7
1111b	8

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Table 24. AC path gain settings

AC_GAIN (binary)	AC path gain (V/V)
00b	1
01b	1.5
10b	2
11b	0.5

Table 25. AC load line settings

Bin	ACLL (hex)	AC Load line (mΩ)	Bin	ACLL (hex)	AC Load line (mΩ)
0	00h	0.0000	32	20h	1.6250
1	01h	0.1250	33	21h	1.7500
2	02h	0.2500	34	22h	1.8750
3	03h	0.3125	35	23h	1.9375
4	04h	0.3750	36	24h	2.000
5	05h	0.4375	37	25h	2.0625
6	06h	0.5000	38	26h	2.1250
7	07h	0.5625	39	27h	2.1875
8	08h	0.6250	40	28h	2.2500
9	09h	0.7500	41	29h	2.375
10	0Ah	0.7969	42	2Ah	2.4218
11	0Bh	0.8125	43	2Bh	2.4375
12	0Ch	0.8281	44	2Ch	2.4531
13	0Dh	0.8438	45	2Dh	2.4687
14	0Eh	0.8594	46	2Eh	2.4843
15	0Fh	0.8750	47	2Fh	2.5000
16	10h	0.8906	48	30h	2.5156
17	11h	0.9063	49	31h	2.5312
18	12h	0.9219	50	32h	2.5468
19	13h	0.9375	51	33h	2.5625
20	14h	0.9531	52	34h	2.5781
21	15h	0.9688	53	35h	2.5937
22	16h	0.9844	54	36h	2.609
23	17h	1.000	55	37h	2.625
24	18h	1.0156	56	38h	2.6406
25	19h	1.0313	57	39h	2.6562
26	1Ah	1.0469	58	3Ah	2.6718
27	1Bh	1.0625	59	3Bh	2.6875
28	1Ch	1.1250	60	3Ch	2.750
29	1Dh	1.2500	61	3Dh	2.875
30	1Eh	1.3750	62	3Eh	3.000
31	1Fh	1.5000	63	3Fh	3.125

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7.5.8.2 (28h) VOUT_DROOP

The VOUT_DROOP command sets the rate, in mV/A (mΩ) at which the output voltage decreases (or increases) with increasing (or decreasing) output current for use with adaptive voltage positioning. This is also referred to as the DC Load Line (DCLL).

VOUT_DROOP is a linear format command. The VOUT_DROOP command must be accessed through Read Word/Write Word transactions.

VOUT_DROOP is a paged register. In order to access VOUT_DROOP for channel A, PAGE must be set to 00h. In order to access the VOUT_DROOP register for channel B, PAGE must be set to 01h. For simultaneous access of channels A and B, the PAGE command must be set to FFh.

15	14	13	12	11	10	9	8
R	R	R	R	R	RW	RW	RW
VDROOP_EXP					VDROOP_MAN		
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
VDROOP_MAN							

LEGEND: R/W = Read/Write; R = Read only

VOUT_DROOP

Table 26. VOUT_DROOP Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	VDROOP_EXP	R	11010b	Linear two's complement fixed exponent, –6. LSB = 0.015625 mΩ
10:0	VDROOP_MAN	RW	NVM	Linear two's complement mantissa. See table of acceptable values below, note that Channel A and Channel B support different acceptable values of VOUT_DROOP.

The table below summarizes the acceptable values of VOUT_DROOP for channel A and channel B. Attempts to write any value other than those specified below will be treated as invalid data - invalid data will be ignored, the appropriate flags in STATUS_CML and STATUS_WORD will be set, and the PMB_ALERT will be asserted to notify the system host of an invalid transaction.

Table 27. Acceptable VOUT_DROOP Values

Bin	VOUT_DROOP (hex)	Supported by Channel A	Supported by Channel B	DC Load Line (mΩ)
0	D000h	Yes	Yes	0
1	D008h	Yes	Yes	0.125
2	D010h	Yes	Yes	0.25
3	D014h	Yes	Yes	0.3125
4	D018h	Yes	Yes	0.375
5	D01Ch	Yes	Yes	0.4375
6	D020h	Yes	Yes	0.5
7	D024h	Yes	Yes	0.5625
8	D028h	Yes	Yes	0.625
9	D030h	Yes	Yes	0.7031
10	D033h	Yes	Yes	0.7969
11	D034h	Yes	Yes	0.8125
12	D035h	Yes	Yes	0.8281
13	D036h	Yes	Yes	0.8438
14	D037h	Yes	Yes	0.8594
15	D038h	Yes	Yes	0.875
16	D039h	Yes	No	0.8906

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Table 27. Acceptable VOUT_DROOP Values (continued)

Bin	VOUT_DROOP (hex)	Supported by Channel A	Supported by Channel B	DC Load Line (mΩ)
17	D03Ah	Yes	No	0.9063
18	D03Bh	Yes	No	0.9219
19	D03Ch	Yes	No	0.9375
20	D03Dh	Yes	No	0.9531
21	D03Eh	Yes	No	0.9688
22	D03Fh	Yes	No	0.9844
23	D040h	Yes	No	1
24	D041h	Yes	No	1.0156
25	D042h	Yes	No	1.0313
26	D043h	Yes	No	1.0469
27	D044h	Yes	No	1.0625
28	D048h	Yes	No	1.125
29	D050h	Yes	No	1.25
30	D058h	Yes	No	1.375
31	D060h	Yes	No	1.5
32	D068h	Yes	No	1.625
33	D070h	Yes	No	1.75
34	D078h	Yes	No	1.875
35	D07Ch	Yes	No	1.9375
36	D080h	Yes	No	2
37	D084h	Yes	No	2.0625
38	D088h	Yes	No	2.125
39	D08Ch	Yes	No	2.1875
40	D090h	Yes	No	2.25
41	D098h	Yes	No	2.328
42	D09Bh	Yes	No	2.4218
43	D09Ch	Yes	No	2.4375
44	D09Dh	Yes	No	2.4531
45	D09Eh	Yes	No	2.4687
46	D09Fh	Yes	No	2.4843
47	D0A0h	Yes	No	2.5
48	D0A1h	Yes	No	2.5156
49	D0A2h	Yes	No	2.5312
50	D0A3h	Yes	No	2.5468
51	D0A4h	Yes	No	2.5625
52	D0A5h	Yes	No	2.5781
53	D0A6h	Yes	No	2.5937
54	D0A7h	Yes	No	2.609
55	D0A8h	Yes	No	2.625
56	D0A9h	Yes	No	2.6406
57	D0AAh	Yes	No	2.6562
58	D0ABh	Yes	No	2.6718
59	D0ACh	Yes	No	2.6875
60	D0B0h	Yes	No	2.75
61	D0B8h	Yes	No	2.875
62	D0C0h	Yes	No	3
63	D0C8h	Yes	No	3.125

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7.5.9 Converter Protection and Response

The TPSM831D31 supports a variety of power supply protection features. The table below summarizes these protection features, and their related PMBus registers. See the following sections for more details.

Table 28. TPSM831D31 Protection and Response

	Threshold		Response	
	Command Name	**Default Value**	**Command Name**	**Default Value**
Output Voltage				
Over-Voltage Protection	VOUT_OV_FAULT_LIMIT	1.520 V (Ch A) 1.520 V (Ch B)	VOUT_OV_FAULT_RESPONSE	Shutdown, do not restart
Maximum Allowed Output Voltage	VOUT_MAX	1.520 V (Ch A) 1.520 V (Ch B)	Refer to Register Description	
Under-Voltage Protection	VOUT_UV_FAULT_LIMIT	0.000 V (Ch A) 0.000 V (Ch B)	VOUT_UV_FAULT_RESPONSE	Shutdown, do not restart
Minimum Allowed Output Voltage	VOUT_MIN	0.000 V (Ch A) 0.000 V (Ch B)	Refer to Register Description	
Output Current				
Over-Current Protection	IOUT_OC_FAULT_LIMIT	180 A (Ch A) 60 A (Ch B)	IOUT_OC_FAULT_RESPONSE	Shutdown, do not restart
Over-Current Warning	IOUT_OC_WARN_LIMIT	120 A (Ch A) 40 A (Ch B)	N/A. Warning Only.	
Input Voltage				
Turn-On Threshold	VIN_ON	7.25 V	N/A	
Over-Voltage Protection	VIN_OV_FAULT_LIMIT	17.000 V	VIN_OV_FAULT_RESPONSE	Continue Uninterrupted
Under-Voltage Protection	VIN_UV_FAULT_LIMIT	6.50 V	VIN_UV_FAULT_RESPONSE	Shutdown, do not restart
Input Current				
Over-Current Protection	IIN_OC_FAULT_LIMIT	40.0 A	IIN_OC_FAULT_RESPONSE	Shutdown, do not restart
Over-Current Warning	IIN_OC_WARN_LIMIT	32.0 A	N/A. Warning Only	
Temperature				
Over-Temperature Protection	OT_FAULT_LIMIT	135 °C (Ch A) 135 °C (Ch B)	OT_FAULT_RESPONSE	Shutdown, do not restart
Over-Temperature Warning	OT_WARN_LIMIT	105 °C (Ch A) 105 °C (Ch B)	N/A. Warning Only.	

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7.5.10 Output Overvoltage Protection and Response

The output overvoltage thresholds track the configured maximum output voltage, VOUT_MAX, with a fixed offset, and may be read back in VID format via the read-only VOUT_OV_FAULT_LIMIT command. The converter response to an overvoltage fault is configured by the read-only VOUT_OV_FAULT_RESPONSE command.

7.5.10.1 (40h) VOUT_OV_FAULT_LIMIT

The VOUT_OV_FAULT_LIMIT is used to read back the value of the output voltage measured at the sense or output pins that causes an output overvoltage fault in VID format. VOUT_OV_FAULT_LIMIT is a VID format command, and must be accessed through Read Word/Write Word transactions. VOUT_OV_FAULT_LIMIT is a paged register. In order to access VOUT_OV_FAULT_LIMIT for channel A, PAGE must be set to 00h. In order to access the VOUT_OV_FAULT_LIMIT register for channel B, PAGE must be set to 01h. For simultaneous access of channels A and B, the PAGE command must be set to FFh.

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
VO_OVF_VID							

LEGEND: R/W = Read/Write; R = Read only

VOUT_OV_FAULT_LIMIT

Table 29. VOUT_OV_FAULT_LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	VO_OVF_VID	R	See below.	Read-only overvoltage fault limit, in VID format.

When the 5-mV DAC mode VID table is selected via MFR_SPECIFIC_13, the VOUT_OV_FAULT_LIMIT register will be set to FFh. When the 10-mV DAC mode VID table is enabled, the VOUT_OV_FAULT_LIMIT is determined according to the value of VOUT_MAX, with a fixed offset applied.

7.5.10.2 (41h) VOUT_OV_FAULT_RESPONSE

The VOUT_OV_FAULT_RESPONSE instructs the device on what action to take in response to an output overvoltage fault. The VOUT_OV_FAULT_RESPONSE command must be accessed through Read Byte transactions. The VOUT_OV_FAULT_RESPONSE command is shared between Channel A and Channel B. All transactions to this command will affect both channels regardless of the PAGE command.

Upon triggering the over-voltage fault, the controller is latched off, and the following actions are taken:

- Set the VOUT_OV_FAULT bit in the STATUS_BYTE
- Set the VOUT bit in the STATUS_WORD
- Set the VOUT_OV_FAULT bit in the STATUS_VOUT register
- The device notifies the host (asserts PMB_ALERT, if the corresponding mask bit in SMBALERT_MASK is not set)

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
VO_OV_RESP							

LEGEND: R/W = Read/Write; R = Read only

VOUT_OV_FAULT_RESPONSE

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Table 30. VOUT_OV_FAULT_RESPONSE Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	VO_OV_RESP	R	80h	80h: Latch-off and do not restart. To clear a shutdown event due to a fault event, the user must toggle the AVR_EN/BEN pin and/or the ON bit in OPERATION, per the settings in ON_OFF_CONFIG, or power cycle the bias power to the V3P3 pin of the controller device.

7.5.11 Maximum Allowed Output Voltage Setting

The VOUT_MAX command sets an upper limit on the output voltage that the unit may be commanded to, regardless of an other commands or combinations. The intent of this command is to provide a safeguard against a user accidentally setting the output voltage to a possibly destructive level.

7.5.11.1 (24h) VOUT_MAX

The VOUT_MAX command sets an upper limit on the output voltage that the unit may be commanded to, regardless of an other commands or combinations. The intent of this command is to provide a safeguard against a user accidentally setting the output voltage to a possibly destructive level. VOUT_MAX is a VID format command, and must be accessed through Read Word/Write Word transactions. VOUT_MAX is a paged register. In order to access VOUT_MAX for channel A, PAGE must be set to 00h. In order to access the VOUT_COMMAND register for channel B, PAGE must be set to 01h. For simultaneous access of channels A and B, the PAGE command must be set to FFh.

The device detects that an attempt has been made to program the output to a voltage greater than the value set by the VOUT_MAX command. Attempts to program the output voltage greater than VOUT_MAX can include VOUT_COMMAND attempts, and margin events while the VOUT_MARGIN_HIGH/VOUT_MARGIN_LOW values exceed the value of VOUT_MAX. These events will be treated warning conditions and not as fault conditions. If an attempt is made to program the output voltage higher than the limit set by the VOUT_MAX command, the device will respond as follows:

- The commanded output voltage will be clamped to VOUT_MAX,
- The OTHER bit will be set in the STATUS_BYTE,
- The VOUT bit will be set in the STATUS_WORD,
- The VOUT_MAX warning bit will be set in the STATUS_VOUT register, and
- The device notifies the host (asserts PMB_ALERT, if the corresponding mask bit in SMBALERT_MASK is not set).

This register should be programmed by the user depending upon the maximum output voltage the converter can support.

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
VOUT_MAX_VID							

LEGEND: R/W = Read/Write; R = Read only

VOUT_MAX

Table 31. VOUT_MAX Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	VOUT_MAX_VID	RW	NVM	Used to set the maximum VOUT of the device in VID format.

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7.5.12 Output Undervoltage Protection and Response

The output undervoltage protection threshold is configured based on commanded output voltage, VOUT_COMMAND, including the shift due to the DC load line, and a fixed offset. The undervoltage threshold may be read back in VID format via the read-only VOUT_UV_FAULT_LIMIT command. The converter response to an overvoltage fault is configured by the read-only VOUT_UV_FAULT_RESPONSE command.

7.5.12.1 (44h) VOUT_UV_FAULT_LIMIT

The VOUT_UV_FAULT_LIMIT is used to read back the value of the output voltage measured at the sense or output pins that causes an output undervoltage fault in VID format. VOUT_UV_FAULT_LIMIT is a VID format command, and must be accessed through Read Word transactions. VOUT_UV_FAULT_LIMIT is a paged register. In order to access VOUT_UV_FAULT_LIMIT for channel A, PAGE must be set to 00h. In order to access the VOUT_UV_FAULT_LIMIT register for channel B, PAGE must be set to 01h. For simultaneous access of channels A and B, the PAGE command must be set to FFh.

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
VO_UVF_VID							

LEGEND: R/W = Read/Write; R = Read only

VOUT_UV_FAULT_LIMIT

Table 32. VOUT_UV_FAULT_LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	VO_UVF_VID	R	See below.	Read-only undervoltage fault limit, in VID format.

7.5.12.2 (45h) VOUT_UV_FAULT_RESPONSE

The VOUT_UV_FAULT_RESPONSE instructs the device on what action to take in response to an output undervoltage fault.

Upon triggering the undervoltage fault, the following actions are taken:

- Set the OTHER bit in the STATUS_BYTE
- Set the VOUT bit in the STATUS_WORD
- Set the VOUT_UV_FAULT bit in the STATUS_VOUT register
- The device notifies the host (asserts PMB_ALERT, if the corresponding mask bit in SMBALERT_MASK is not set)

The VOUT_UV_FAULT_RESPONSE command must be accessed through Read Byte/Write Byte transactions.

The VOUT_UV_FAULT_RESPONSE command is shared between Channel A and Channel B. All transactions to this command will affect both channels regardless of the PAGE command.

7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
VO_UV_RESP							

LEGEND: R/W = Read/Write; R = Read only

VOUT_UV_FAULT_RESPONSE

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Table 33. VOUT_UV_FAULT_RESPONSE Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	VO_UV_RESP	RW	NVM	00h: Ignore. The controller will set the appropriate status bits, and alert the host, but continue converting power. BAh: Shutdown and restart. The controller will shutdown the channel on which the fault occurred, and attempt to restart 20ms later. This will occur continuously until the condition causing the fault has disappeared, or the controller has been disabled. 80h: Latch-off and do not restart. To clear a shutdown event due to a fault event, the user must toggle the AVR_EN/BEN pin and/or the ON bit in OPERATION, per the settings in ON_OFF_CONFIG, or power cycle the bias power to the V3P3 pin of the controller device.

7.5.13 Minimum Allowed Output Voltage Setting

The VOUT_MIN command sets a lower bound on the output voltage to which the unit can be commanded, regardless of any other commands or combinations. The intent of this command is to provide a safeguard against a user accidentally setting the output voltage to a possibly destructive level rather than to be the primary output under voltage protection.

7.5.13.1 (2Bh) VOUT_MIN

The VOUT_ MIN command sets a lower bound on the output voltage to which the unit can be commanded, regardless of any other commands or combinations. The intent of this command is to provide a safeguard against a user accidentally setting the output voltage to a possibly destructive level rather than to be the primary output under voltage protection. VOUT_MIN is a VID format command, and must be accessed through Read Word/Write Word transactions. VOUT_MIN is a paged register. In order to access VOUT_MIN for channel A, PAGE must be set to 00h. In order to access the VOUT_MIN register for channel B, PAGE must be set to 01h. For simultaneous access of channels A and B, the PAGE command must be set to FFh.

If an attempt is made to program the output voltage lower than the limit set by this command, the device will respond as follows:

- The commanded output voltage will be clamped to VOUT_MIN
- The OTHER bit will be set in the STATUS_BYTE
- The VOUT bit will be set in the STATUS_WORD
- The VOUT_MAX_MIN Warning bit will be set in the STATUS_VOUT register
- The device notifies the host (asserts PMB_ALERT, if the corresponding mask bit in SMBALERT_MASK is not set).

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
VOUT_MIN_VID							

LEGEND: R/W = Read/Write; R = Read only

VOUT_MIN

Table 34. VOUT_MIN Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	VOUT_MIN_VID	RW	NVM	Used to set a lower bound for output voltage programming for the active PAGE, is set to in VID format.

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7.5.14 Output Overcurrent Protection and Response

Overcurrent thresholds are configured using the IOUT_OC_FAULT_LIMIT. When the overcurrent fault threshold is reached, the converter will respond according to the settings in IOUT_OC_FAULT_RESPONSE. The IOUT_OC_WARN_LIMIT may also be used to configure an information-only overcurrent warning, which triggers prior to an overcurrent fault. Note, that the MFR_SPECIFIC_00 command, not listed below, also contains settings for per-phase overcurrent limits. Refer to the device *Technical Reference Manual* for more information.

7.5.14.1 (46h) IOUT_OC_FAULT_LIMIT

The IOUT_OC_FAULT_LIMIT command sets the value of the total output current, in amperes, that causes the over-current detector to indicate an over-current fault condition. The command has two data bytes and the data format is Linear as shown in the table below. The units are amperes. IOUT_OC_FAULT_LIMIT is a linear format command, and must be accessed through Read Word/Write Word transactions. IOUT_OC_FAULT_LIMIT is a paged register. In order to access IOUT_OC_FAULT_LIMIT command for channel A, PAGE must be set to 00h. In order to access IOUT_OC_FAULT_LIMIT register for channel B, PAGE must be set to 01h. For simultaneous access of channels A and B, the PAGE command must be set to FFh.

15	14	13	12	11	10	9	8
R	R	R	R	R	RW	RW	RW
IOOCF_EXP					IOOCF_MAN		
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
IOOCF_MAN							

LEGEND: R/W = Read/Write; R = Read only

IOUT_OC_FAULT_LIMIT

Table 35. IOUT_OC_FAULT_LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	IOOCF_EXP	R	00000b	Linear two's complement exponent, 0. LSB = 1.0 A
10:0	IOOCF_MAN	RW	See below.	Linear two's complement mantissa

At power-on, or after a RESTORE_DEFAULT_ALL operation, the IOUT_OC_FAULT_LIMIT command will be loaded with the value of IOUT_MAX × 1.50. The IOUT_MAX bits for each channel are stored in MFR_SPECIFIC_10 (PAGE 0 for channel A, PAGE 1 for channel B). IOUT_OC_FAULT_LIMIT may be changed during operation, but returns to this value on reset.

7.5.14.2 (4Ah) IOUT_OC_WARN_LIMIT

The IOUT_OC_WARN_LIMIT command sets the value of the output current, in amperes, that causes the over-current detector to indicate an over-current warning condition. IOUT_OC_WARN_LIMIT is a linear format command, and must be accessed through Read Word/Write Word transactions. IOUT_OC_WARN_LIMIT is a paged register. In order to access IOUT_OC_WARN_LIMIT command for channel A, PAGE must be set to 00h. In order to access IOUT_OC_WARN_LIMIT register for channel B, PAGE must be set to 01h. For simultaneous access of channels A and B, the PAGE command must be set to FFh.

Upon triggering the overcurrent warning, the following actions are taken:

- Set the OTHER bit in the STATUS_BYTE
- Set the IOUT bit in the STATUS_WORD
- Set the IOUT Over current Warning bit in the STATUS_IOUT register
- The device notifies the host (asserts PMB_ALERT, if the corresponding mask bit in SMBALERT_MASK is not set)

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15	14	13	12	11	10	9	8
R	R	R	R	R	RW	RW	RW
IOOCW_EXP					IOOCW_MAN		
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
IOOCW_MAN							

LEGEND: R/W = Read/Write; R = Read only

IOUT_OC_WARN_LIMIT

Table 36. IOUT_OC_WARN_LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	IOOCW_EXP	R	00000b	Linear two's complement exponent, 0. LSB = 1.0 A
10:0	IOOCW_MAN	RW	See below.	Linear two's complement mantissa.

At power-on, or after a RESTORE_DEFAULT_ALL operation, the IOUT_OC_WARN_LIMIT command will be loaded with the value of IOUT_MAX. The IOUT_MAX bits for each channel are stored in MFR_SPECIFIC_10 (PAGE 0 for channel A, PAGE 1 for channel B). IOUT_OC_WARN_LIMIT may be changed during operation, but will return to this value on reset.

7.5.14.3 (47h) IOUT_OC_FAULT_RESPONSE

The IOUT_OC_FAULT_RESPONSE instructs the device on what action to take in response to an output over-current fault. The IOUT_OC_FAULT_RESPONSE command must be accessed through Read Byte/Write Byte transactions. The IOUT_OC_FAULT_RESPONSE command is shared between Channel A and Channel B. All transactions to this command will affect both channels regardless of the PAGE command.

NOTE

IOUT_OC_WARN_LIMIT maximum default value is 180A for VOUTA and 60A for VOUTB. If an application maximum load current is less than 180A, IOUT_OC_WARN_LIMIT needs to change as the default max load current value is restored each time after power-on or RESTORE_DEFAULT_ALL operation.

Upon triggering the over-current fault, the controller is latched off, and the following actions are taken:

- Set the IOUT_OC_FAULT bit in the STATUS_BYTE
- Set the IOUT bit in the STATUS_WORD
- Set the IOUT_OC_FAULT bit in the STATUS_IOUT register
- The device notifies the host (asserts PMB_ALERT, if the corresponding mask bit in SMBALERT_MASK is not set)

7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
IO_OC_RESP							

LEGEND: R/W = Read/Write; R = Read only

IOUT_OC_FAULT_RESPONSE

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Table 37. IOUT_OC_FAULT_RESPONSE Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	IO_OC_RESP	RW	NVM	C0h: Latch-off and do not restart. To clear a shutdown event due to a fault event, the user must toggle the AVR_EN/BEN pin and/or the ON bit in OPERATION, per the settings in ON_OFF_CONFIG, or power cycle the bias power to the V3P3 pin of the controller device. FAh: Shutdown and restart. The controller will shutdown the channel on which the fault occurred, and attempt to restart 20ms later. This will occur continuously until the condition causing the fault has disappeared, or the controller has been disabled.

7.5.14.4 Per Phase Overcurrent Limit Thresholds

Table 38. OCL

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{OCLAx}	Phase OCL levels for Channel A (ACSPx-VREF), valley current limit	MFR_SPEC_00<3:0>, (PAGE0) = 0000b	12.5	14.5	16.5	A
		MFR_SPEC_00<3:0>, (PAGE0) = 0001b	16.5	18.5	20.5	A
		MFR_SPEC_00<3:0>, (PAGE0) = 0010b	20.5	22.5	24.5	A
		MFR_SPEC_00<3:0>, (PAGE0) = 0011b	24.5	26.5	28.5	A
		MFR_SPEC_00<3:0>, (PAGE0) = 0100b	28.5	30.5	32.5	A
		MFR_SPEC_00<3:0>, (PAGE0) = 0101b	32.5	34.5	36.5	A
		MFR_SPEC_00<3:0>, (PAGE0) = 0110b	36.5	38.5	40.5	A
		MFR_SPEC_00<3:0>, (PAGE0) = 0111b	40.5	42.5	44.5	A
		MFR_SPEC_00<3:0>, (PAGE0) = 1000b	44.5	46.5	48.5	A
		MFR_SPEC_00<3:0>, (PAGE0) = 1001b	48.5	50.5	52.5	A
		MFR_SPEC_00<3:0>, (PAGE0) = 1010b	52.5	54.5	56.5	A
		MFR_SPEC_00<3:0>, (PAGE0) = 1011b	56.5	58.5	60.5	A
		MFR_SPEC_00<3:0>, (PAGE0) = 1100b	60.5	62.5	64.5	A
		MFR_SPEC_00<3:0>, (PAGE0) = 1101b	64.5	66.5	68.5	A
		MFR_SPEC_00<3:0>, (PAGE0) = 1110b	68.5	70.5	72.5	A
		MFR_SPEC_00<3:0>, (PAGE0) = 1111b	72.5	74.5	76.5	A
I_{OCLBx}	Phase OCL levels for Channel B (BCSPx-VREF), valley current limit	MFR_SPEC_00<3:0>, (PAGE1) = 0000b	12	14	16	A
		MFR_SPEC_00<3:0>, (PAGE1) = 0001b	16	18	20	A
		MFR_SPEC_00<3:0>, (PAGE1) = 0010b	20	22	24	A
		MFR_SPEC_00<3:0>, (PAGE1) = 0011b	24	26	28	A
		MFR_SPEC_00<3:0>, (PAGE1) = 0100b	28	30	32	A
		MFR_SPEC_00<3:0>, (PAGE1) = 0101b	32	34	36	A
		MFR_SPEC_00<3:0>, (PAGE1) = 0110b	36	38	40	A
		MFR_SPEC_00<3:0>, (PAGE1) = 0111b	40	42	44	A
		MFR_SPEC_00<3:0>, (PAGE1) = 1000b	44	46	48	A
		MFR_SPEC_00<3:0>, (PAGE1) = 1001b	48	50	52	A
		MFR_SPEC_00<3:0>, (PAGE1) = 1010b	52	54	56	A
		MFR_SPEC_00<3:0>, (PAGE1) = 1011b	56	58	60	A
		MFR_SPEC_00<3:0>, (PAGE1) = 1100b	60	62	64	A
		MFR_SPEC_00<3:0>, (PAGE1) = 1101b	64	66	68	A
		MFR_SPEC_00<3:0>, (PAGE1) = 1110b	68	70	72	A
		MFR_SPEC_00<3:0>, (PAGE1) = 1111b	72	74	76	A

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7.5.15 Input Under-Voltage Lockout (UVLO)

The TPSM831D31 may not start converting power until the power stage input voltage reaches the level specified by VIN_ON.

7.5.15.1 (35h) VIN_ON

The VIN_ON command sets the value of the input voltage, in Volts, at which the unit should start power conversion. This command has two data bytes encoded in linear data format, and must be accessed through Read Word/Write Word transactions. The VIN_ON command is shared between Channel A and Channel B. All transactions to this command will affect both channels regardless of the PAGE command. The supported range for VIN_ON is from 4.0 V volts to 11.25 Volts.

15	14	13	12	11	10	9	8
R	R	R	R	R	RW	RW	RW
VINON_EXP					VINON_MAN		
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
VINON_MAN							

LEGEND: R/W = Read/Write; R = Read only

VIN_ON

Table 39. VIN_ON Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	VINON_EXP	R	11110b	Linear two's complement exponent, –2. LSB = 0.25 V
10:0	VINON_MAN	RW	NVM	Linear two's complement mantissa. See the table of acceptable values below.

Table 40. Acceptable Values of VIN_ON

VIN_ON (hex)	Turn-On Voltage (V)
F01Dh	7.25
F021h	8.25
F025h	9.25
F029h	10.25
F02Dh	11.25

Table 41. VIN Undervoltage Fault Limits

VIN_UV_FAULT_LIMIT (hex)	Fault Threshold (V)
F80Fh	7.5
F811h	8.5
F813h	9.5
F815h	10.5
F817h	11.5

7.5.16 Input Over-Voltage Protection and Response

The TPSM831D31 provides protection from input transients via the VIN_OV_FAULT_LIMIT and VIN_OV_FAULT_RESPONSE commands.

7.5.16.1 (55h) VIN_OV_FAULT_LIMIT

The VIN_OV_FAULT_LIMIT command sets the value of the input voltage that causes an input overvoltage fault. VIN_OV_FAULT_LIMIT is a linear format command, and must be accessed through Read Word/Write Word transactions. The VIN_OV_FAULT_LIMIT command is shared between Channel A and Channel B. All transactions to this command will affect both channels regardless of the PAGE command.

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15	14	13	12	11	10	9	8
R	R	R	R	R	RW	RW	RW
VIN_OVF_EXP					VIN_OVF_MAN		
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
VIN_OVF_MAN							

LEGEND: R/W = Read/Write; R = Read only

VIN_OV_FAULT_LIMIT

Table 42. VIN_OV_FAULT_LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	VIN_OVF_EXP	R	00000b	Linear two's complement exponent, 0. LSB = 1 V
10:0	VIN_OVF_MAN	RW	NVM	Linear two's complement mantissa. Valid values of the mantissa range from 0d to 31d.

7.5.16.2 (56h) VIN_OV_FAULT_RESPONSE

The VIN_OV_FAULT_RESPONSE command instructs the device on what action to take in response to an input overvoltage fault. The VIN_OV_FAULT_RESPONSE command must be accessed through Read Byte transactions. The VIN_OV_FAULT_RESPONSE command is shared between Channel A and Channel B. All transactions to this command will affect both channels regardless of the PAGE command.

In response to the VIN_OV_LIMIT being exceeded, the device will:

- Set the OTHER bit in the STATUS_BYTE
- Set the INPUT bit in the upper byte of the STATUS_WORD
- Sets the VIN_OV_FAULT bit in the STATUS_INPUT register
- Notify the host (assert the PMB_ALERT signal, if the corresponding mask bit in SMBALERT_MASK is not set)

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
VI_OVF_RESP							

LEGEND: R/W = Read/Write; R = Read only

VIN_OV_FAULT_RESPONSE

Table 43. VIN_OV_FAULT_RESPONSE Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	VI_OVF_RESP	R	00h	00h: Ignore. The controller will set the appropriate status bits, and alert the host, but continue converting power.

7.5.17 Input Undervoltage Protection and Response

The TPSM831D31 provides protection from input transients via the VIN_UV_FAULT_LIMIT and VIN_UV_FAULT_RESPONSE commands.

7.5.17.1 (59h) VIN_UV_FAULT_LIMIT

The VIN_UV_FAULT_LIMIT command sets the value of the input voltage that causes an Input Under voltage Fault. This fault is masked until the input exceeds the value set by the VIN_ON command for the first time, and the unit has been enabled. VIN_UV_FAULT_LIMIT is a linear format command, and must be accessed through Read Word/Write Word transactions. The VIN_UV_FAULT_LIMIT command is shared between Channel A and Channel B. All transactions to this command will affect both channels regardless of the PAGE command.

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15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
VIN_UVF_EXP					VIN_UVF_MAN		
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
VIN_UVF_MAN							

LEGEND: R/W = Read/Write; R = Read only

VIN_UV_FAULT_LIMIT

Table 44. VIN_UV_FAULT_LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	VIN_UVF_EXP	RW	NVM	Linear two's complement exponent. See the table of acceptable values below.
10:0	VIN_UVF_MAN	RW	NVM	Linear two's complement mantissa. See the table of acceptable values below.

Table 45. Acceptable Values of VIN_UV_FAULT_LIMIT

VIN_UV_FAULT_LIMIT (hex)	VIN UVF Limit (V)
F80Dh	6.5
F80Fh	7.5
F811h	8.5
F813h	9.5
F815h	10.5
F817h	11.5

7.5.17.2 (5Ah) VIN_UV_FAULT_RESPONSE

The VIN_UV_FAULT_RESPONSE command instructs the device on what action to take in response to an input overvoltage fault. The VIN_UV_FAULT_RESPONSE command must be accessed through Read Byte transactions. The VIN_UV_FAULT_RESPONSE command is shared between Channel A and Channel B. All transactions to this command will affect both channels regardless of the PAGE command.

In response to the VIN_UV_LIMIT being exceeded, the device will:

- Set the OTHER bit in the STATUS_BYTE
- Set the INPUT bit in the upper byte of the STATUS_WORD
- Set the VIN_UV_FAULT bit in the STATUS_INPUT register
- The device notifies the host (asserts PMB_ALERT, if the corresponding mask bit in SMBALERT_MASK is not set)

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
VI_UVF_RESP							

LEGEND: R/W = Read/Write; R = Read only

VIN_UV_FAULT_RESPONSE

Table 46. VIN_UV_FAULT_RESPONSE Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	VI_UVF_RESP	R	C0h	C0h: Shutdown and restart when the fault condition is no longer present.

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7.5.18 Input Overcurrent Protection and Response

Input overcurrent protection is configured via the IIN_OC_FAULT_LIMIT, IIN_OC_WARN_LIMIT and IIN_OC_FAULT_RESPONSE commands.

7.5.18.1 (5Bh) IIN_OC_FAULT_LIMIT

The IIN_OC_FAULT_LIMIT command sets the value of the input current, in amperes, that causes the input over current fault condition. IIN_OC_FAULT_LIMIT is a linear format command, and must be accessed through Read Word/Write Word transactions. The IIN_OC_FAULT_LIMIT command is shared between Channel A and Channel B. All transactions to this command will affect both channels regardless of the PAGE command.

15	14	13	12	11	10	9	8
R	R	R	R	R	RW	RW	RW
IIN_OCF_EXP					IIN_OCF_MAN		
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
IIN_OCF_MAN							

LEGEND: R/W = Read/Write; R = Read only

IIN_OC_FAULT_LIMIT

Table 47. IIN_OC_FAULT_LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	IIN_OCF_EXP	R	11111b	Linear two's complement format exponent, –1. LSB = 0.5 A.
10:0	IIN_OCF_MAN	RW	See below.	Linear two's complement format mantissa. Acceptable values range from 0d (0 A) to 127d (63.5 A).

During operation, the IIN_OC_FAULT_LIMIT may be changed to any valid value, as specified above. The IIN_OC_FAULT_LIMIT command has only limited NVM backup. The table below summarizes the values that IIN_OC_FAULT_LIMIT may be restored to following a reset, or RESTORE_DEFAULT_ALL operation.

Table 48. IIN_OC_FAULT_LIMIT reset values

Hex Value	IIN_OC_FAULT_LIMIT during NVM store operation	IIN_OC_FAULT_LIMIT following Reset/Restore Operation
F810h	8 A	8 A
F820h	16 A	16 A
F830h	24 A	24 A
F840h	32 A	32 A
F850h	40 A	40 A
F860h	48 A	48 A
F870h	56 A	56 A
F87Fh	63.5 A	63.5 A
Any other valid data	Any other valid data	63.5 A

7.5.18.2 (5Dh) IIN_OC_WARN_LIMIT

The IIN_OC_WARN_LIMIT command sets the value of the input current, in amperes, that causes the input overcurrent warning condition. The IIN_OC_WARN_LIMIT command must be accessed through Read Word/Write Word transactions. The IIN_OC_WARN_LIMIT command is shared between Channel A and Channel B. All transactions to this command will affect both channels regardless of the PAGE command.

Upon triggering the over-current warning, the following actions are taken:

- Set the OTHER bit in the STATUS_BYTE
- Set the INPUT bit in the STATUS_WORD
- Set the IIN Over-current Warning bit in the STATUS_INPUT register
- The device notifies the host (asserts PMB_ALERT, if the corresponding mask bit in SMBALERT_MASK is not

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set)

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
IIN_OCW_EXP					IIN_OCW_MAN		
7	6	5	4	3	2	1	0
R	RW	RW	RW	RW	RW	RW	RW
IIN_OCW_MAN							

LEGEND: R/W = Read/Write; R = Read only

IIN_OC_WARN_LIMIT

Table 49. IIN_OC_FAULT_LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	IIN_OCW_EXP	R	11111b	Linear two's complement format exponent, –1. LSB = 0.5 A.
10:0	IIN_OCW_MAN	RW	See below.	Linear two's complement format mantissa. Acceptable values range from 0d (0 A) to 127d (63.5 A).

During operation, the IIN_OC_FAULT_LIMIT may be changed to any valid value, as specified above. The IIN_OC_FAULT_LIMIT command has only limited NVM backup. The table below summarizes the values that IIN_OC_FAULT_LIMIT may be restored to following a reset, or RESTORE_DEFAULT_ALL operation.

Table 50. IIN_OC_WARN_LIMIT reset values

Hex Value	IIN_OC_WARN_LIMIT during NVM store operation	IIN_OC_WARN_LIMIT following Reset/Restore Operation
F810h	8 A	8 A
F820h	16 A	16 A
F830h	24 A	24 A
F840h	32 A	32 A
F850h	40 A	40 A
F860h	48 A	48 A
F870h	56 A	56 A
F87Fh	63.5 A	63.5 A
Any other valid data	Any other valid data	63.5 A

7.5.18.3 (5Ch) IIN_OC_FAULT_RESPONSE

The IIN_OC_FAULT_RESPONSE command instructs the device on what action to take in response to an input over-current fault. IIN_OC_FAULT_RESPONSE command must be accessed through Read Byte transactions. The IIN_OC_FAULT_RESPONSE command is shared between Channel A and Channel B. All transactions to this command will affect both channels regardless of the PAGE command.

Upon triggering the input over-current fault, the controller is latched off, and the following actions are taken:

- Set the OTHER bit in the STATUS_BYTE
- Set the INPUT bit in the STATUS_WORD
- Set the IIN_OC_FAULT bit in the STATUS_INPUT register
- The device notifies the host (asserts PMB_ALERT and VR_FAULT, if the corresponding mask bit in SMBALERT_MASK is not set)

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
IIN_OC_RESP							

LEGEND: R/W = Read/Write; R = Read only

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IIN_OC_FAULT_RESPONSE

Table 51. IIN_OC_FAULT_LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	IIN_OC_RESP	R	C0h	C0h: Latch-off and do not restart. To clear a shutdown event due to a fault event, the user must toggle the AVR_EN/BEN pin and/or the ON bit in OPERATION, per the settings in ON_OFF_CONFIG, or power cycle the bias power to the V3P3 pin of the controller device.

7.5.19 Overtemperature Protection and Response

Overtemperature protection is configured via the OT_FAULT_LIMIT, OT_WARN_LIMIT and OT_FAULT_RESPONSE commands.

7.5.19.1 (4Fh) OT_FAULT_LIMIT

The OT_FAULT_LIMIT command sets the value of the temperature limit, in degrees Celsius, that causes an overtemperature fault condition when the sensed temperature from the external sensor exceeds this limit. The default value is selected inMFR_SPECIFIC_13, using the OTF_DFLT bit. Refer to the device *Technical Reference Manual* for more information. OT_FAULT_LIMIT is a linear format command, and must be accessed through Read Word/Write Word transactions. OT_FAULT_LIMIT is a paged register. In order to access OT_FAULT_LIMIT command for channel A, PAGE must be set to 00h. In order to access OT_FAULT_LIMIT register for channel B, PAGE must be set to 01h. For simultaneous access of channels A and B, the PAGE command must be set to FFh.

15	14	13	12	11	10	9	8
R	R	R	R	R	RW	RW	RW
OTF_EXP					OTF_MAN		
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
OTF_MAN							

LEGEND: R/W = Read/Write; R = Read only

OT_FAULT_LIMIT

Table 52. OT_FAULT_LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	OTF_EXP	R	00000b	Linear two's complement exponent, 0. LSB = 1 ºC
10:0	OTF_MAN	RW	NVM	Linear two's complement mantissa. The default OT_FAULT_LIMIT is set by the OTF_DFLT bit in MFR_SPECIFIC_13.

7.5.19.2 (51h) OT_WARN_LIMIT

The OT_WARN_LIMIT command sets the temperature, in degrees Celsius, of the unit at which it should indicate an Over-temperature Warning event. OT_WARN_LIMIT is a linear format command, and must be accessed through Read Word/Write Word transactions. OT_WARN_LIMIT is a paged register. In order to access OT_WARN_LIMIT command for channel A, PAGE must be set to 00h. In order to access OT_WARN_LIMIT register for channel B, PAGE must be set to 01h. For simultaneous access of channels A and B, the PAGE command must be set to FFh.

In response to the OT_WARN_LIMIT being exceeded, the device will:

- Set the TEMPERATURE bit in the STATUS_BYTE
- Set the Over-temperature Warning bit in the STATUS_TEMPERATURE register
- Notify the host (asserts PMB_ALERT, if the corresponding mask bit in SMBALERT_MASK is not set)

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15	14	13	12	11	10	9	8
R	R	R	R	R	RW	RW	RW
OTW_EXP					OTW_MAN		
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
OTW_MAN							

LEGEND: R/W = Read/Write; R = Read only

OT_WARN_LIMIT

Table 53. OT_WARN_LIMIT Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	OTF_EXP	R	00000b	Linear two's complement exponent, 0. LSB = 1 ºC
10:0	OTF_MAN	RW	105d	Linear two's complement mantissa. Default = 105 ºC

7.5.19.3 (50h) OT_FAULT_RESPONSE

The OT_FAULT_RESPONSE instructs the device on what action to take in response to an output over-temperature fault. The OT_FAULT_RESPONSE command must be accessed through Read Byte/Write Byte transactions. The OT_FAULT_RESPONSE command is shared between Channel A and Channel B. All transactions to this command will affect both channels regardless of the PAGE command.

Upon triggering the over-temperature fault, the controller is latched off, and the following actions are taken:

- Set the TEMPERATURE bit in the STATUS_BYTE
- Set the OT_FAULT bit in the STATUS_TEMPERATURE register
- The device notifies the host (asserts PMB_ALERT, if the corresponding mask bit in SMBALERT_MASK is not set).

7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
OTF_RESP							

LEGEND: R/W = Read/Write; R = Read only

OT_FAULT_RESPONSE

Table 54. OT_FAULT_RESPONSE Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OTF_RESP	RW	NVM	80h: Latch-off and do not restart. To clear a shutdown event due to a fault event, the user must toggle the AVR_EN/BEN pin and/or the ON bit in OPERATION, per the settings in ON_OFF_CONFIG, or power cycle the bias power to the V3P3 pin of the controller device. C0h: Shutdown and restart when the fault condition is no longer present.

7.5.20 Dynamic Phase Shedding (DPS)

The dynamic phase shedding (DPS) feature allows the TPSM831D31 to dynamically select the number of operational phases for each channel, based on the total output current. This increases the total converter efficiency by reducing unnecessary switching losses when the output current is low enough to be supported by a fewer number of phases, than are available in hardware. The MFR_SPECIFIC_14 and MFR_SPECIFIC_15 commands may be used to configure dynamic phase shedding behavior and thresholds.

The DPS_EN bit in MFR_SPECIFIC_14 may be used to enable or disable dynamic phase shedding. Un-setting (writing to 0b) this bit forces each channel to use the maximum number of available phases, regardless of the output current. DPS is disabled as the factory default.

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The phase add/drop thresholds, at which phases are added or dropped are configured based on the peak efficiency point per phase. For a given switching frequency/duty cycle, the efficiency of an individual power stage has a "peak" point, at which switching losses become less significant and conduction losses begin to dominate. For a multiphase converter, the optimum efficiency is achieved when all of the power stages operate as close as possible to their peak efficiency point. For example, consider a 4-phase design, with power stages that have a peak efficiency point of 12 A per phase. When the total output current is 25 A, if all four phases were active, each phase would be supplying 6.25 A, and hence would be operating far away from their peak efficiency point. With only two phases active, however, each phase supplies 12.5A, meaning that each power stage is operating close to its peak efficiency point, therefore the total converter efficiency is higher overall.

In order to maintain regulation during severe load transient events, phases may be added immediately whenever the total peak current reaches phase addition thresholds. To prevent chattering, phases are dropped when the total average current falls below phase drop thresholds, after a delay of 85 µs typically. Phases are always added/dropped, in numerical order. For example, phase 3 is added after phase 2, and dropped after phase 4.

The DPS_COURSE_TH bits in MFR_SPECIFIC_15 select the peak efficiency point per phase. Refer to the power stage datasheet to determine the peak efficiency point per phase.

Phase adding thresholds are configured based on the peak efficiency point per phase. Each phase transition has a configurable threshold of 6 A to 12 A above the peak efficiency point. For example, the threshold at which the converter transitions from 2 phases to 3 phases is determined by the DPS_2TO3_FINE_ADD bits in MFR_SPECIFIC_15. When 8 A is selected, the total peak current which causes the third phase to be added is $2 \times I_{EFF(PEAK)} + 8$ A. See the register descriptions below for more detailed information.

Likewise, phase drop thresholds are configured based on the peak efficiency point per phase. Each phase transition has a configurable threshold of 2A below A to 4 A above the peak efficiency point. For example, the threshold at which the converter transitions from 3 phases to 2 phases is determined by the DPS_3TO2_FINE_DROP bits in MFR_SPECIFIC_14. When 0 A is selected, the total average current which causes the third phase to be dropped is $2 \times I_{EFF(PEAK)}$. See the register descriptions below for more detailed information.

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Table 55. Dynamic Phase Add and Drop

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{DPSTHA1}$	Dynamic phase adding threshold, 1 to 2 Phases (peak current)	Peak Efficiency = 12 A; (MFR_SPECIFIC_15<1:0> = 00b); Offset = 2 A; (MFR_SPECIFIC_15<4:3> = 00b); V_{RIPPLE} ≈ 18 A (estimation)	21	23	25	A
		Peak Efficiency = 12 A; (MFR_SPECIFIC_15<1:0> = 00b); Offset = 4 A; (MFR_SPECIFIC_15<4:3> = 01b); V_{RIPPLE} ≈ 18 A (estimation)	23	25	27	A
		Peak Efficiency = 12 A; (MFR_SPECIFIC_15<1:0> = 00b); Offset = 6 A; (MFR_SPECIFIC_15<4:3> = 10b); V_{RIPPLE} ≈ 18 A (estimation)	25	27	29	A
		Peak Efficiency = 12 A; (MFR_SPECIFIC_15<1:0> = 00b); Offset = 8 A; (MFR_SPECIFIC_15<4:3> = 11b); V_{RIPPLE} ≈ 18 A (estimation)	27	29	31	A
		Peak Efficiency = 14 A; (MFR_SPECIFIC_15<1:0> = 01b); Offset = 2 A; (MFR_SPECIFIC_15<4:3> = 00b); V_{RIPPLE} ≈ 18 A (estimation)	23	25	27	A
		Peak Efficiency = 14 A; (MFR_SPECIFIC_15<1:0> = 01b); Offset = 4 A; (MFR_SPECIFIC_15<4:3> = 01b); V_{RIPPLE} ≈ 18 A (estimation)	25	27	29	A
		Peak Efficiency = 14 A; (MFR_SPECIFIC_15<1:0> = 01b); Offset = 6 A; (MFR_SPECIFIC_15<4:3> = 10b); V_{RIPPLE} ≈ 18 A (estimation)	27	29	31	A
		Peak Efficiency = 14 A; (MFR_SPECIFIC_15<1:0> = 01b); Offset = 8 A; (MFR_SPECIFIC_15<4:3> = 11b); V_{RIPPLE} ≈ 18 A (estimation)	29	31	33	A
		Peak Efficiency = 16 A; (MFR_SPECIFIC_15<1:0> = 10b); Offset = 2 A; (MFR_SPECIFIC_15<4:3> = 00b); V_{RIPPLE} ≈ 18 A (estimation)	25	27	29	A
		Peak Efficiency = 16 A; (MFR_SPECIFIC_15<1:0> = 10b); Offset = 4 A; (MFR_SPECIFIC_15<4:3> = 01b); V_{RIPPLE} ≈ 18 A (estimation)	27	29	31	A
		Peak Efficiency = 16 A; (MFR_SPECIFIC_15<1:0> = 10b); Offset = 6 A; (MFR_SPECIFIC_15<4:3> = 10b); V_{RIPPLE} ≈ 18 A (estimation)	29	31	33	A
		Peak Efficiency = 16 A; (MFR_SPECIFIC_15<1:0> = 10b); Offset = 8 A; (MFR_SPECIFIC_15<4:3> = 11b); V_{RIPPLE} ≈ 18 A (estimation)	31	33	35	A
		Peak Efficiency = 18 A; (MFR_SPECIFIC_15<1:0> = 11b); Offset = 2 A; (MFR_SPECIFIC_15<4:3> = 00b); V_{RIPPLE} ≈ 18 A (estimation)	27	29	31	A
		Peak Efficiency = 18 A; (MFR_SPECIFIC_15<1:0> = 11b); Offset = 4 A; (MFR_SPECIFIC_15<4:3> = 01b); V_{RIPPLE} ≈ 18 A (estimation)	29	31	33	A
		Peak Efficiency = 18 A; (MFR_SPECIFIC_15<1:0> = 11b); Offset = 6 A; (MFR_SPECIFIC_15<4:3> = 10b); V_{RIPPLE} ≈ 18 A (estimation)	31	33	35	A
		Peak Efficiency = 18 A; (MFR_SPECIFIC_15<1:0> = 11b); Offset = 8 A; (MFR_SPECIFIC_15<4:3> = 11b); V_{RIPPLE} ≈ 18 A (estimation)	33	35	37	A

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Table 55. Dynamic Phase Add and Drop (continued)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{DPSTHS1}$	Dynamic phase shedding threshold, 2 to 1 phase (average current)	Peak Efficiency = 12 A; (MFR_SPECIFIC_15<1:0> = 00b); Offset = -6 A; (MFR_SPECIFIC_15<14:13> = 00b)	4	6	8	A
		Peak Efficiency = 12 A; (MFR_SPECIFIC_15<1:0> = 00b); Offset = -4 A; (MFR_SPECIFIC_15<14:13> = 01b)	6	8	10	A
		Peak Efficiency = 12 A; (MFR_SPECIFIC_15<1:0> = 00b); Offset = -2 A; (MFR_SPECIFIC_15<14:13> = 10b)	8	10	12	A
		Peak Efficiency = 12 A; (MFR_SPECIFIC_15<1:0> = 00b); Offset = 0 A; (MFR_SPECIFIC_15<14:13> = 11b)	10	12	14	A
		Peak Efficiency = 14 A; (MFR_SPECIFIC_15<1:0> = 01b); Offset = -6 A; (MFR_SPECIFIC_15<14:13> = 00b)	6	8	10	A
		Peak Efficiency = 14 A; (MFR_SPECIFIC_15<1:0> = 01b); Offset = -4 A; (MFR_SPECIFIC_15<14:13> = 01b)	8	10	12	A
		Peak Efficiency = 14 A; (MFR_SPECIFIC_15<1:0> = 01b); Offset = -2 A; (MFR_SPECIFIC_15<14:13> = 10b)	10	12	14	A
		Peak Efficiency = 14 A; (MFR_SPECIFIC_15<1:0> = 01b); Offset = 0 A; (MFR_SPECIFIC_15<14:13> = 11b)	12	14	16	A
		Peak Efficiency = 16 A; (MFR_SPECIFIC_15<1:0> = 10b); Offset = -6 A; (MFR_SPECIFIC_15<14:13> = 00b)	8	10	12	A
		Peak Efficiency = 16 A; (MFR_SPECIFIC_15<1:0> = 10b); Offset = -4 A; (MFR_SPECIFIC_15<14:13> = 01b)	10	12	14	A
		Peak Efficiency = 16 A; (MFR_SPECIFIC_15<1:0> = 10b); Offset = -2 A; (MFR_SPECIFIC_15<14:13> = 10b)	12	14	16	A
		Peak Efficiency = 16 A; (MFR_SPECIFIC_15<1:0> = 10b); Offset = 0 A; (MFR_SPECIFIC_15<14:13> = 11b)	14	16	18	A
		Peak Efficiency = 18 A; (MFR_SPECIFIC_15<1:0> = 11b); Offset = -6 A; (MFR_SPECIFIC_15<14:13> = 00b)	10	12	14	A
		Peak Efficiency = 18 A; (MFR_SPECIFIC_15<1:0> = 11b); Offset = -4 A; (MFR_SPECIFIC_15<14:13> = 01b)	12	14	16	A
		Peak Efficiency = 18 A; (MFR_SPECIFIC_15<1:0> = 11b); Offset = -2 A; (MFR_SPECIFIC_15<14:13> = 10b)	14	16	18	A
		Peak Efficiency = 18 A; (MFR_SPECIFIC_15<1:0> = 11b); Offset = 0 A; (MFR_SPECIFIC_15<14:13> = 11b)	16	18	20	A

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Table 55. Dynamic Phase Add and Drop (continued)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{DPSTHA2}$	Dynamic phase adding threshold, 2 to 3 phases (peak current)	Peak Efficiency = 12 A; (MFR_SPECIFIC_15<1:0> = 00b); Offset = 4 A; (MFR_SPECIFIC_15<6:5> = 00b); V_{RIPPLE} = 14 A (estimation)	32.5	35	37.5	A
		Peak Efficiency = 12 A; (MFR_SPECIFIC_15<1:0> = 00b); Offset = 6 A; (MFR_SPECIFIC_15<6:5> = 01b); V_{RIPPLE} = 14 A (estimation)	34.5	37	39.5	A
		Peak Efficiency = 12 A; (MFR_SPECIFIC_15<1:0> = 00b); Offset = 8 A; (MFR_SPECIFIC_15<6:5> = 10b); V_{RIPPLE} = 14 A (estimation)	36.5	39	41.5	A
		Peak Efficiency = 12 A; (MFR_SPECIFIC_15<1:0> = 00b); Offset = 10 A; (MFR_SPECIFIC_15<6:5> = 11b); V_{RIPPLE} = 14 A (estimation)	38.5	41	43.5	A
		Peak Efficiency = 14 A; (MFR_SPECIFIC_15<1:0> = 01b); Offset = 4 A; (MFR_SPECIFIC_15<6:5> = 00b); V_{RIPPLE} = 14 A (estimation)	36.5	39	41.5	A
		Peak Efficiency = 14 A; (MFR_SPECIFIC_15<1:0> = 01b); Offset = 6 A; (MFR_SPECIFIC_15<6:5> = 01b); V_{RIPPLE} = 14 A (estimation)	38.5	41	43.5	A
		Peak Efficiency = 14 A; (MFR_SPECIFIC_15<1:0> = 01b); Offset = 8 A; (MFR_SPECIFIC_15<6:5> = 10b); V_{RIPPLE} = 14 A (estimation)	40.5	43	45.5	A
		Peak Efficiency = 14 A; (MFR_SPECIFIC_15<1:0> = 01b); Offset = 10 A; (MFR_SPECIFIC_15<6:5> = 11b); V_{RIPPLE} = 14 A (estimation)	42.5	45	47.5	A
		Peak Efficiency = 16 A; (MFR_SPECIFIC_15<1:0> = 10b); Offset = 4 A; (MFR_SPECIFIC_15<6:5> = 00b); V_{RIPPLE} = 14 A (estimation)	40.5	43	45.5	A
		Peak Efficiency = 16 A; (MFR_SPECIFIC_15<1:0> = 10b); Offset = 6 A; (MFR_SPECIFIC_15<6:5> = 01b); V_{RIPPLE} = 14 A (estimation)	42.5	45	47.5	A
		Peak Efficiency = 16 A; (MFR_SPECIFIC_15<1:0> = 10b); Offset = 8 A; (MFR_SPECIFIC_15<6:5> = 10b); V_{RIPPLE} = 14 A (estimation)	44.5	47	49.5	A
		Peak Efficiency = 16 A; (MFR_SPECIFIC_15<1:0> = 10b); Offset = 10 A; (MFR_SPECIFIC_15<6:5> = 11b); V_{RIPPLE} = 14 A (estimation)	46.5	49	51.5	A
		Peak Efficiency = 18 A; (MFR_SPECIFIC_15<1:0> = 11b); Offset = 4 A; (MFR_SPECIFIC_15<6:5> = 00b); V_{RIPPLE} = 14 A (estimation)	44.5	47	49.5	A
		Peak Efficiency = 18 A; (MFR_SPECIFIC_15<1:0> = 11b); Offset = 6 A; (MFR_SPECIFIC_15<6:5> = 01b); V_{RIPPLE} = 14 A (estimation)	46.5	49	51.5	A
		Peak Efficiency = 18 A; (MFR_SPECIFIC_15<1:0> = 11b); Offset = 8 A; (MFR_SPECIFIC_15<6:5> = 10b); V_{RIPPLE} = 14 A (estimation)	48.5	51	53.5	A
		Peak Efficiency = 18 A; (MFR_SPECIFIC_15<1:0> = 11b); Offset = 10 A; (MFR_SPECIFIC_15<6:5> = 11b); V_{RIPPLE} = 14 A (estimation)	50.5	53	55.5	A

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Table 55. Dynamic Phase Add and Drop (continued)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{DPSTHS2}$	Dynamic phase shedding threshold, 3 to 2 phases (average current)	Peak Efficiency = 12 A; (MFR_SPECIFIC_15<1:0> = 00b); Offset = -4 A; (MFR_SPECIFIC_14<9:8> = 00b)	17.5	20	22.5	A
		Peak Efficiency = 12 A; (MFR_SPECIFIC_15<1:0> = 00b); Offset = -2 A; (MFR_SPECIFIC_14<9:8> = 01b)	19.5	22	24.5	A
		Peak Efficiency = 12 A; (MFR_SPECIFIC_15<1:0> = 00b); Offset = 0 A; (MFR_SPECIFIC_14<9:8> = 10b)	21.5	24	26.5	A
		Peak Efficiency = 12 A; (MFR_SPECIFIC_15<1:0> = 00b); Offset = 2 A; (MFR_SPECIFIC_14<9:8> = 11b)	23.5	26	28.5	A
		Peak Efficiency = 14 A; (MFR_SPECIFIC_15<1:0> = 01b); Offset = -4 A; (MFR_SPECIFIC_14<9:8> = 00b)	21.5	24	26.5	A
		Peak Efficiency = 14 A; (MFR_SPECIFIC_15<1:0> = 01b); Offset = -2 A; (MFR_SPECIFIC_14<9:8> = 01b)	23.5	26	28.5	A
		Peak Efficiency = 14 A; (MFR_SPECIFIC_15<1:0> = 01b); Offset = 0 A; (MFR_SPECIFIC_14<9:8> = 10b)	25.5	28	30.5	A
		Peak Efficiency = 14 A; (MFR_SPECIFIC_15<1:0> = 01b); Offset = 2 A; (MFR_SPECIFIC_14<9:8> = 11b)	27.5	30	32.5	A
		Peak Efficiency = 16 A; (MFR_SPECIFIC_15<1:0> = 10b); Offset = -4 A; (MFR_SPECIFIC_14<9:8> = 00b)	25.5	28	30.5	A
		Peak Efficiency = 16 A; (MFR_SPECIFIC_15<1:0> = 10b); Offset = -2 A; (MFR_SPECIFIC_14<9:8> = 01b)	27.5	30	32.5	A
		Peak Efficiency = 16 A; (MFR_SPECIFIC_15<1:0> = 10b); Offset = 0 A; (MFR_SPECIFIC_14<9:8> = 10b)	29.5	32	34.5	A
		Peak Efficiency = 16 A; (MFR_SPECIFIC_15<1:0> = 10b); Offset = 2 A; (MFR_SPECIFIC_14<9:8> = 11b)	31.5	34	36.5	A
		Peak Efficiency = 18 A; (MFR_SPECIFIC_15<1:0> = 11b); Offset = -4 A; (MFR_SPECIFIC_14<9:8> = 00b)	29.5	32	34.5	A
		Peak Efficiency = 18 A; (MFR_SPECIFIC_15<1:0> = 11b); Offset = -2 A; (MFR_SPECIFIC_14<9:8> = 01b)	31.5	34	36.5	A
		Peak Efficiency = 18 A; (MFR_SPECIFIC_15<1:0> = 11b); Offset = 0 A; (MFR_SPECIFIC_14<9:8> = 10b)	33.5	36	38.5	A
		Peak Efficiency = 18 A; (MFR_SPECIFIC_15<1:0> = 11b); Offset = 2 A; (MFR_SPECIFIC_14<9:8> = 11b)	35.5	38	40.5	A

7.5.20.1 (DEh) MFR_SPECIFIC_14

The MFR_SPECIFIC_14 command is used to configure dynamic phase shedding, and compensation ramp amplitude, and dynamic ramp amplitude during USR, and different power states. The MFR_SPECIFIC_14 command must be accessed through Write Word/Read Word transactions.

MFR_SPECIFIC_14 is a paged register. In order to access MFR_SPECIFIC_14 command for channel A, PAGE must be set to 00h. In order to access the MFR_SPECIFIC_14 register for channel B, PAGE must be set to 01h.

15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
n/a	n/a	n/a	n/a	n/a	n/a	DPS_3TO2_FINE_DROP	
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
DPS_EN	DYN_RAMP_USR		DYN_RAMP_2 PH	DYN_RAMP_1 PH	RAMP		

LEGEND: R/W = Read/Write; R = Read only

MFR_SPECIFIC_14

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Table 56. MFR_SPECIFIC_14 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	n/a	RW	NVM	n/a
9:8	DPS_3TO2_FINE_DROP	RW	NVM	Dynamic phase drop threshold, fine adjustment, 3 phases to 2 phases. Set as an offset from peak efficiency point per phase in Amperes. Phases drop when average phase current reaches the stated threshold. $I_{EFF(PEAK)}$ refers to the value selected by DPS_COURSE_TH in MFR_SPECIFIC_15. 00b: Threshold = 2 × $I_{EFF(PEAK)}$ – 2 A 01b: Threshold = 2 × $I_{EFF(PEAK)}$ 10b: Threshold = 2 × $I_{EFF(PEAK)}$ + 2 A 11b: Threshold = 2 × $I_{EFF(PEAK)}$ + 4 A
7	DPS_EN	RW	NVM	Enable or Disable Dynamic Phase Shedding 0b: Disable dynamic phase shedding 1b: Enable dynamic phase shedding
6:5	DYN_RAMP_USR	RW	NVM	Dynamic ramp amplitude setting during USR operation. Only applies to USR Level 1. 00b: Equal to the settings in the RAMP bits 01b: 40 mV 10b: 80 mV 11b: 120 mV
4	DYN_RAMP_2PH	RW	NVM	Dynamic ramp amplitude setting during 2 phase operation. 0b: Equal to the settings in the RAMP bits 1b: 120 mV
3	DYN_RAMP_1PH	RW	NVM	Dynamic ramp amplitude setting during 1 phase operation. 0b: Equal to the settings in the RAMP bits 1b: 80 mV
2:0	RAMP	RW	NVM	Ramp amplitude settings. See Table 57.

Table 57. Ramp Amplitude Settings

RAMP (binary)	Ramp Amplitude Setting (mV)
000b	40
001b	80
010b	120
011b	160
100b	200
101b	240
110b	280
111b	320

7.5.20.2 (DFh) MFR_SPECIFIC_15

The MFR_SPECIFIC_15 command is used to configure dynamic phase shedding. The MFR_SPECIFIC_15 command must be accessed through Write Word/Read Word transactions.

MFR_SPECIFIC_15 is a paged register. In order to access MFR_SPECIFIC_15 command for channel A, PAGE must be set to 00h. In order to access the MFR_SPECIFIC_15 register for channel B, PAGE must be set to 01h.

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15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
DPS_DCM	DPS_2TO1_FINE_DROP		n/a	n/a	n/a	n/a	n/a
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
n/a	DPS_2TO3_FINE_ADD		DPS_1TO2_FINE_ADD		2TO1_PH_EN	DPS_COURSE_TH	

LEGEND: R/W = Read/Write; R = Read only

MFR_SPECIFIC_15

Table 58. MFR_SPECIFIC_15 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	DPS_DCM	RW	NVM	Enable DCM mode during 1 phase operation, when higher order phases are dropped due to dynamic phase shedding. 0b: Disable DCM operation during 1 phase operation 1b: Enable DCM operation during 1 phase operation
14:13	DPS_2TO1_FINE_DROP	RW	NVM	Dynamic phase drop threshold, fine adjustment, 2 phases to 1phase. Set as an offset from peak efficiency point per phase in Amperes. Phases drop when average phase current reaches the stated threshold. $I_{EFF(PEAK)}$ refers to the value selected by DPS_COURSE_TH below. 00b: Threshold = 1× $I_{EFF(PEAK)}$ – 2 A 01b: Threshold = 1 × $I_{EFF(PEAK)}$ 10b: Threshold = 1 × $I_{EFF(PEAK)}$ + 2 A 11b: Threshold = 1 × $I_{EFF(PEAK)}$ + 4 A
12:7	n/a	RW	NVM	n/a
6:5	DPS_2TO3_FINE_ADD	RW	NVM	Dynamic phase add threshold, fine adjustment, 2 phases to 3 phases. Set as an offset from peak efficiency point per phase in Amperes. Phases add when peak phase current reaches the stated threshold. $I_{EFF(PEAK)}$ refers to the value selected by DPS_COURSE_TH below 00b: Threshold = 2 × $I_{EFF(PEAK)}$ + 6A 01b: Threshold = 2 × $I_{EFF(PEAK)}$ + 8 A 10b: Threshold = 2 × $I_{EFF(PEAK)}$ + 10 A 11b: Threshold = 2 × $I_{EFF(PEAK)}$ + 12 A
5:4	DPS_1TO2_FINE_ADD	RW	NVM	Dynamic phase add threshold, fine adjustment, 1 phase to 2 phases. Set as an offset from peak efficiency point per phase in Amperes. Phases add when peak phase current reaches the stated threshold. $I_{EFF(PEAK)}$ refers to the value selected by DPS_COURSE_TH below 00b: Threshold = 1 × $I_{EFF(PEAK)}$ + 6A 01b: Threshold = 1 × $I_{EFF(PEAK)}$ + 8 A 10b: Threshold = 1 × $I_{EFF(PEAK)}$ + 10 A 11b: Threshold = 1 × $I_{EFF(PEAK)}$ + 12 A
3	2TO1_PH_EN	RW	NVM	Enable phase dropping from 2 phases to 1 phase operation. 0b: Disable phase shedding to 1 phase 1b: Enable phase shedding to 1 phase
2:0	DPS_COURSE_TH	RW	NVM	Sets the peak efficiency point per phase. This is used to determine phase add/drop thresholds. 00b: $I_{EFF(PEAK)}$ = 12 A 01b: $I_{EFF(PEAK)}$ = 14 A 10b: $I_{EFF(PEAK)}$ = 16 A 11b: $I_{EFF(PEAK)}$ = 18 A

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7.5.21 NVM Programming

The USER_DATA_00 - USER_DATA_12 commands are provided to streamline NVM programming. These 6-byte block commands are mapped internally to all of the user-configurable parameters the TPSM831D31 supports. The MFR_SERIAL command also provides a checksum, to streamline verification of desired programming values.

The generalized procedure for programming the TPSM831D31 is summarized below.

Configure User-Programmable Parameters

1. First, configure all of the user-accessible parameters via the standard PMBus, and Manufacturer Specific commands. TI provides the Fusion Digital Power Designer graphical interface software to streamline this step. The user can also refer to the *Technical Reference Manual* for a full set of register maps for these commands.
2. Once the device is configured as desired, issue the STORE_DEFAULT_ALL command to commit these values to NVM, and update the checksum value. Wait approximately 100 ms after issuing STORE_DEFAULT_ALL before communicating with the device again.
3. Write PAGE to 00h
4. Read-back and Record the value of IC_DEVICE_ID and IC_DEVICE_REV commands
5. Read-back and Record the value of the USER_DATA_00 through USER_DATA_12 commands
6. Read-back and Record the value of the MFR_SERIAL command
7. Read-back and Record the value of VOUT_MAX
8. Write PAGE to 01h
9. Read-back and Record the value of VOUT_MAX

Program and Verify NVM (repeat for each device)

1. Power the device by supplying +3.3V to the V3P3 pin. Power conversion should be disabled for NVM programming.
2. Read-back and verify that IC_DEVICE_ID and IC_DEVICE_REV values match those recorded previously. This ensures that user-parameters being programmed correspond to the same device/revision as previously configured.
3. Write PAGE to 00h.
4. Write the USER_DATA_00 through USER_DATA_12 commands, with the values recorded previously.
5. Write VOUT_MAX (Page 0) with the value recorded previously.
6. Write PAGE to 01h
7. Write VOUT_MAX (Page 1) with the value recorded previously.
8. Issue STORE_DEFAULT_ALL. Wait appx 100 ms after issuing STORE_DEFAULT_ALL before communicating with the device again.
9. Read-back the MFR_SERIAL command, and compare the value to that recorded previously. If the new MFR_SERIAL matches the value recorded previously, NVM programming was successful.

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7.5.22 NVM Security

The MFR_SPECIFIC_42 command can be optionally used to set a password for NVM programming. To prevent a hacker from simply sending the password command with all possible passwords, the TPSM831D31 goes into a special extra-secure state when an incorrect password is received. In this state, all passwords are rejected, even the valid one. The device must be power cycled to clear this state so that another password attempt may be made. When NVM security is enabled, the TPSM831D31 will not accept writes to any command other than PAGE and PHASE, which are necessary for reading certain parameters.

Enabling NVM Security

1. Set the NVM password. Write MFR_SPECIFIC_42 to a value other than FFFFh.
2. Issue STORE_DEFAULT_ALL
3. Wait 100ms for the NVM store to complete
4. Power cycle V3P3. NVM Security will be enabled at the next power-up.

Disabling NVM Security

To disable NVM security, use the following procedure:

1. Write the password to MFR_SPECIFIC_42 to disable NVM security. Once the correct password has been given, NVM security will be disabled, and the device will once again accept write transactions to configuration registers.

NVM security will be re-enabled at the next power-on, unless MFR_SPECIFIC_42 is set to FFFFh (NVM Security Disabled), and an NVM store operation (issue STORE_DEFAULT_ALL and wait 100 ms) is performed.

Determining Whether NVM Security is Active

Reads to the MFR_SPECIFIC_42 command returns one of three values:

- 0000h = NVM Security is Disabled
- 0001h = NVM Security is Enabled
- 0002h = MFR_SPECIFIC_42 is locked due to incorrect password entry

7.5.22.1 (FAh) MFR_SPECIFIC_42

MFR_SPECIFIC_42 is used for NVM Security. The MFR_SPECIFIC_42 command must be accessed through Read Word/Write Word transactions.

MFR_SPECIFIC_42 is a shared register. Write transactions to this register will apply to both channels, and read transactions to this register returns the same data regardless of the current PAGE.

15	14	13	12	11	10	9	8
RW	RW	RW	RW	RW	RW	RW	RW
NVM_SECURITY_KEY							
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
NVM_SECURITY_KEY							

LEGEND: R/W = Read/Write; R = Read only

MFR_SPECIFIC_42

Table 59. MFR_SPECIFIC_42 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	NVM_SECURITY_KEY	RW	NVM	16 bit code for NVM security key.

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7.5.23 Black Box Recording

The TPSM831D31 provides a "black box" feature to aid in system-level debugging. According to the PMBus specification, status bits are latched whenever the condition causing them occurs, regardless of whether or not other status bits are already set. This, however, makes it difficult for the system designer to understand which fault condition occurred first, in the case that one fault condition causes others to trigger. The MFR_SPECIFIC_08 command provides a "snapshot" of the first faults to occur chronologically, for each channel, which may be stored to NVM, for future debugging. Only the most catastrophic fault conditions are logged, such as the over-voltage fault, over-current fault, and power stage failure. The black box command may also be reset, or cleared by writing 00h to the register, and storing to NVM if the NVM value must also be cleared.

Resetting the Black Box Record

Resetting the record allows the user to determine which faults occur first, *after* the register is cleared. To clear the record, write 00h to MFR_SPECIFIC_08, and issue STORE_DEFAULT_ALL.

Triggering Black Box Recording

Black box recording is always active, whether or not the TPSM831D31 is converting power. Note however many of the critical faults summarized in MFR_SPECIFIC_08 are only possible to trigger during power conversion. Whenever any of the following catastrophic faults occur, the MFR_SPECIFIC_08 register will be updated according to the register description below, but only if the black box record has been cleared since the last catastrophic faults occurred. Faults logged include:

- Overvoltage Fault (Device was Converting Power)
- Overvoltage Fault (Device was not Converting Power)
- Input Overcurrent Fault
- Output Overcurrent Fault
- Power Stage Fault
- Input Over-Power Fault

Retrieving the Black Box Record

Reading the MFR_SPECIFIC_08 returns the current value of the Black Box record. If the register reads 00h, no catastrophic faults have occurred since the record was last cleared. If any value other than 00h is stored in the register, then de-code the value according to the register description below. In order to read-back the black box record following a power-down, the STORE_DEFAULT_ALL command must be issued, to store the contents of the black box record to NVM.

7.5.23.1 (D8h) MFR_SPECIFIC_08

The MFR_SPECIFIC_08 command is used to identify catastrophic faults which occur first, and store this information to NVM. See the product datasheet for more information. The MFR_SPECIFIC_08 command must be accessed through Write Byte/Read Byte transactions. MFR_SPECIFIC_08 is a shared register. Transactions to this register do not require specific PAGE settings. However, note that channels A and B have independent bit fields within the command.

7	6	5	4	3	2	1	0
R	R	RW	RW	RW	RW	RW	RW
0	0	CF_CHA			CF_CHB		

LEGEND: R/W = Read/Write; R = Read only

MFR_SPECIFIC_08

Table 60. MFR_SPECIFIC_08 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	Not used	R	0	Not used and set to 0.
5:3	CF_CHA	RW	NVM	Catastrophic fault record for channel A.
2:0	CF_CHB	RW	NVM	Catastrophic fault record for channel B.

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Whenever a catastrophic fault occurs, the first event detected will trigger the MFR_SPECIFIC_08 command to update according to the tables below. This recording happens independently for channel A and channel B. If the PMBus host issues a STORE_DEFAULT_ALL, this information will be committed to NVM, and may be retrieved at a later time. In order to clear the record for either channel, the PMBus host must write the corresponding bits (CF_CHA for channel A, CF_CHB for channel B) to 000b, and issue STORE_DEFAULT_ALL.

Attempts to write any non-zero value to this command will be treated as invalid data - data will be ignored, the appropriate flags in STATUS_CML, and STATUS_WORD, will be set, and the PMB_ALERT pin will be asserted to notify the host of the invalid transaction.

Table 61. Catastrophic Fault Recording Interpretation

CF_CHA / CF_CHB (binary)	Interpretation
000b	No fault occurred
001b	OVF occurred, power conversion was disabled
010b	OVF occurred, power conversion was enabled
011b	IIN Overcurrent fault occurred
100b	IOUT Overcurrent fault occurred
101b	Overtemperature fault occurred
110b	Power stage fault occurred
111b	Input overpower warning occurred

7.5.24 Board Identification and Inventory Tracking

The TPSM831D31 provides several bytes of arbitrarily programmable NVM-backed memory to allow for inventory management and board identification. By default, these values reflect information about the date/revision of the TPSM831D31 device being used itself. This provides a convenient and easy to use method of tracking boards, revisions and manufacturing dates. The following commands are provided for this purpose:

- MFR_ID - 16 bits of NVM for end-users to track the power module supplier name
- MFR_MODEL - 16 bits of NVM for tracking the manufacturer model number
- MFR_REVISION - 16 bits of NVM for tracking power module revision code
- MFR_DATE - 16 bits of NVM for tracking power module manufacturing date code

7.5.25 Status Reporting

The TPSM831D31 provides several registers containing status information. The flags in these registers are latched whenever their corresponding condition occurs, and are not cleared until either the CLEAR_FAULTS command is issued, or the host writes a value of 1b to that bit location. Register maps for the all of the supported status registers are shown in the following sections.

7.5.25.1 (78h) STATUS_BYTE

The STATUS_BYTE command returns one byte of information with a summary of the most critical faults, such as over-voltage, overcurrent, over-temperature, etc.

The STATUS_BYTE command must be accessed through Read Byte transactions. STATUS_BYTE is a paged register. In order to access STATUS_WORD command for channel A, PAGE must be set to 00h. In order to access STATUS_WORD register for channel B, PAGE must be set to 01h. If PAGE is set FFh, the device return value will reflect the status of Channel A.

7	6	5	4	3	2	1	0
0	R	R	R	R	R	R	R
BUSY	OFF	VOUT_OV	IOUT_OC	VIN_UV	TEMP	CML	OTHER

Figure 12. STATUS_BYTE

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Table 62. STATUS_BYTE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BUSY	R	0	Not supported and always set to 0.
6	OFF	R	Current Status	This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled. 0: Raw status indicating the IC is providing power to VOUT. 1: Raw status indicating the IC is not providing power to VOUT.
5	VOUT_OV	R	Current Status	Output Over-Voltage Fault Condition 0: Latched flag indicating no VOUT OV fault has occurred. 1: Latched flag indicating a VOUT OV fault occurred
4	IOUT_OC	R	Current Status	Output Over-Current Fault Condition 0: Latched flag indicating no IOUT OC fault has occurred. 1: Latched flag indicating an IOUT OC fault has occurred.
3	VIN_UV	R	Current Status	Input Under-Voltage Fault Condition 0: Latched flag indicating VIN is above the UVLO threshold. 1: Latched flag indicating VIN is below the UVLO threshold.
2	TEMP	R	Current Status	Over-Temperature Fault/Warning 0: Latched flag indicating no OT fault or warning has occurred. 1: Latched flag indicating an OT fault or warning has occurred.
1	CML	R	Current Status	Communications, Memory or Logic Fault 0: Latched flag indicating no communication, memory, or logic fault has occurred. 1: Latched flag indicating a communication, memory, or logic fault has occurred.
0	OTHER	R	Current Status	Other Fault (None of the Above) This bit is used to flag faults not covered with the other bit faults. In this case, UVF or OCW faults are examples of other faults not covered by the bits [7:1] in this register. 0: No fault has occurred 1: A fault or warning not listed in bits [7:1] has occurred.

Per the description in the PMBus 1.3 specification, part II, TPSM831D31 does support clearing of status bits by writing to STATUS registers. However, the bits in the STATUS_BYTE are summary bits only and reflect the status of corresponding bits in STATUS_VOUT, STATUS_IOUT, etc... To clear these bits individually, the user must clear them by writing to the corresponding STATUS_X register. For example: the output overcurrent fault sets the IOUT_OC bit in STATUS_BYTE, and the IOUT_OC_FLT bit in STATUS_IOUT. Writing a 1 to the IOUT_OC_FLT bit in STATUS_IOUT clears the fault in both STATUS_BYTE and STATUS_IOUT. Writes to STATUS_BYTE itself will be treated as invalid transactions.

7.5.25.2 (79h) STATUS_WORD

The STATUS_WORD command returns two bytes of information with a summary of critical faults, such as over-voltage, overcurrent, over-temperature, etc..

The STATUS_WORD command must be accessed through Read Word transactions. STATUS_WORD is a paged register. In order to access STATUS_WORD command for channel A, PAGE must be set to 00h. In order to access STATUS_WORD register for channel B, PAGE must be set to 01h. If PAGE is set FFh, the device return value will reflect the status of Channel A.

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
VOUT	IOUT	INPUT	MFR	PGOOD	FANS	OTHER	UNKNOWN
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
BUSY	OFF	VOUT_OV	IOUT_OC	VIN_UV	TEMP	CML	OTHER

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Figure 13. STATUS_WORD

Table 63. STATUS_WORD Register Field Descriptions

Bit	Field	Type	Reset	Description
15	VOUT	R	Current Status	Output Voltage Fault/Warning. Refer to STATUS_VOUT for more information. 0: Latched flag indicating no VOUT fault or warning has occurred. 1: Latched flag indicating a VOUT fault or warning has occurred.
14	IOUT	R	Current Status	Output Current Fault/Warning. Refer to STATUS_IOUT for more information. 0: Latched flag indicating no IOUT fault or warning has occurred. 1: Latched flag indicating an IOUT fault or warning has occurred.
13	INPUT	R	Current Status	Input Voltage/Current Fault/Warning. Refer to STATUS_INPUT for more information. 0: Latched flag indicating no VIN or IIN fault or warning has occurred. 1: Latched flag indicating a VIN or IIN fault or warning has occurred.
12	MFR	R	Current Status	MFR_SPECIFIC Fault. Refer to STATUS_MFR for more information. 0: Latched flag indicating no MFR_SPECIFIC fault has occurred. 1: Latched flag indicating a MFR_SPECIFIC fault has occurred.
11	PGOOD	R	Current Status	Power Good Status. Note: Per the PMBus specification, the PGOOD bit is not latched, always reflecting the current status of the AVR_RDY/BVR_RDY pin. 0: Raw status indicating AVR_RDY/BVR_RDY pin is at logic high. 1: Raw status indicating AVR_RDY/BVR_RDY pin is at logic low.
10	FANS	R	0	Not supported and always set to 0.
9	OTHER	R	0	Not supported and always set to 0.
8	UNKNOWN	R	0	Not supported and always set to 0.
7	BUSY	R	0	Not supported and always set to 0.
6	OFF	R	Current Status	This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled. 0: Raw status indicating the IC is providing power to VOUT. 1: Raw status indicating the IC is not providing power to VOUT.
5	VOUT_OV	R	Current Status	Output Over-Voltage Fault Condition 0: Latched flag indicating no VOUT OV fault has occurred. 1: Latched flag indicating a VOUT OV fault occurred
4	IOUT_OC	R	Current Status	Output Over-Current Fault Condition 0: Latched flag indicating no IOUT OC fault has occurred. 1: Latched flag indicating an IOUT OC fault has occurred.
3	VIN_UV	R	Current Status	Input Under-Voltage Fault Condition 0: Latched flag indicating VIN is above the UVLO threshold. 1: Latched flag indicating VIN is below the UVLO threshold.
2	TEMP	R	Current Status	Over-Temperature Fault/Warning 0: Latched flag indicating no OT fault or warning has occurred. 1: Latched flag indicating an OT fault or warning has occurred.
1	CML	R	Current Status	Communications, Memory or Logic Fault 0: Latched flag indicating no communication, memory, or logic fault has occurred. 1: Latched flag indicating a communication, memory, or logic fault has occurred.
0	OTHER	R	Current Status	Other Fault (None of the Above) This bit is used to flag faults not covered with the other bit faults. In this case, UVF or OCW faults are examples of other faults not covered by the bits [7:1] in this register. 0: No fault has occurred 1: A fault or warning not listed in bits [7:1] has occurred.

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Per the description in the PMBus 1.3 specification, part II, TPSM831D31 does support clearing of status bits by writing to STATUS registers. However, the bits in the STATUS_WORD are summary bits only and reflect the status of corresponding bits in STATUS_VOUT, STATUS_IOUT, etc... To clear these bits individually, the user must clear them by writing to the corresponding STATUS_X register. For example: the output overcurrent fault sets the IOUT_OC bit in STATUS_WORD, and the IOUT_OC_FLT bit in STATUS_IOUT. Writing a 1 to the IOUT_OC_FLT bit in STATUS_IOUT clears the fault in both STATUS_WORD and STATUS_IOUT. Writes to STATUS_WORD will be treated as invalid transactions.

7.5.25.3 (7Ah) STATUS_VOUT

The STATUS_VOUT command returns one byte of information relating to the status of the converter's output voltage related faults.

The STATUS_VOUT command must be accessed through Read Byte/Write Byte transactions. STATUS_VOUT is a paged register. In order to access STATUS_VOUT command for channel A, PAGE must be set to 00h. In order to access STATUS_VOUT register for channel B, PAGE must be set to 01h. If PAGE is set FFh, the device return value will reflect the status of Channel A.

7	6	5	4	3	2	1	0
RW	0	0	RW	RW	0	0	0
VOUT_OVF	VOUT_OVW	VOUT_UVW	VOUT_UVF	VOUT_MIN_MAX	TON_MAX	TOFF_MAX	VOUT_TRACK

Figure 14. STATUS_VOUT

Table 64. STATUS_VOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	VOUT_OVF	RW	Current Status	Output Over-Voltage Fault 0: Latched flag indicating no VOUT OV fault has occurred. 1: Latched flag indicating a VOUT OV fault has occurred.
6	VOUT_OVW	R	0	Not supported and always set to 0.
5	VOUT_UVW	R	0	Not supported and always set to 0.
4	VOUT_UVF	RW	Current Status	Output Under-Voltage Fault 0: Latched flag indicating no VOUT UV fault has occurred. 1: Latched flag indicating a VOUT UV fault has occurred.
3	VOUT_MIN_MAX	RW	Current Status	Output Voltage Max/Min Exceeded Warning 0: Latched flag indicating no VOUT_MAX/VOUT_MIN warning has occurred. 1: Latched flag indicating that an attempt has been made to set the output voltage to a value higher than allowed by the VOUT_MAX/VOUT_MIN command.
2	TON_MAX	R	0	Not supported and always set to 0.
1	TOFF_MAX	R	0	Not supported and always set to 0.
0	VOUT_TRACK	R	0	Not supported and always set to 0.

Per the description in the PMBus 1.3 specification, part II, TPSM831D31 does support clearing of status bits by writing to STATUS registers. Writing a 1 to any supported bit in this register will attempt to clear it as a fault condition.

7.5.25.4 (7Bh) STATUS_IOUT

The STATUS_IOUT command returns one byte of information relating to the status of the converter's output current related faults.

The STATUS_IOUT command must be accessed through Read Byte/Write Byte transactions. STATUS_IOUT is a paged register. In order to access STATUS_IOUT command for channel A, PAGE must be set to 00h. In order to access STATUS_IOUT register for channel B, PAGE must be set to 01h. If PAGE is set FFh, the device return value will reflect the status of Channel A.

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7	6	5	4	3	2	1	0
RW	0	RW	0	RW	0	0	0
IOUT_OCF	IOUT_OCUVF	IOUT_OCW	IOUT_UCF	CUR_SHAREF	POW_LIMIT	POUT_OPF	POUT_OPW

Figure 15. STATUS_IOUT

Table 65. STATUS_IOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	IOUT_OCF	RW	Current Status	Output Over-Current Fault 0: Latched flag indicating no IOUT OC fault has occurred. 1: Latched flag indicating a IOUT OC fault has occurred .
6	IOUT_OCUVF	R	0	Not supported and always set to 0.
5	IOUT_OCW	RW	Current Status	0: Latched flag indicating no IOUT OC warning has occurred 1: Latched flag indicating a IOUT OC warning has occurred
4	IOUT_UCF	R	0	Not supported and always set to 0.
3	CUR_SHAREF	RW	Current Status	0: Latched flag indicating no current sharing fault has occurred 1: Latched flag indicating a current sharing fault has occurred
2	POW_LIMIT	R	0	Not supported and always set to 0.
1	POUT_OPF	R	0	Not supported and always set to 0.
0	POUT_OPW	R	0	Not supported and always set to 0.

Per the description in the PMBus 1.3 specification, part II, TPSM831D31 does support clearing of status bits by writing to STATUS registers. Writing a 1 to any supported bit in this register will attempt to clear it as a fault condition.

7.5.25.5 (7Ch) STATUS_INPUT

The STATUS_INPUT command returns one byte of information relating to the status of the converter's input voltage and current related faults.

The STATUS_INPUT command must be accessed through Read Byte/Write Byte transactions. The STATUS_INPUT command is shared between Channel A and Channel B. All transactions to this command will affect both channels regardless of the PAGE command.

7	6	5	4	3	2	1	0
RW	0	0	RW	RW	RW	RW	RW
VIN_OVF	VIN_OVW	VIN_UVW	VIN_UVF	LOW_VIN	IIN_OCF	IIN_OCW	PIN_OPW

Figure 16. STATUS_INPUT Register

Table 66. STATUS_INPUT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	VIN_OVF	R	Current Status	Input Over-Voltage Fault 0: Latched flag indicating no VIN OV fault has occurred. 1: Latched flag indicating a VIN OV fault has occurred.
6	VIN_OVW	R	0	Not supported and always set to 0.
5	VIN_UVW	R	0	Not supported and always set to 0.
4	VIN_UVF	R	Current Status	Input Under-Voltage Fault 0: Latched flag indicating no VIN UV fault has occurred. 1: Latched flag indicating a VIN UV fault has occurred.
3	LOW_VIN	R	Current Status	Unit Off for insufficient input voltage 0: Latched flag indicating no LOW_VIN fault has occurred. 1: Latched flag indicating a LOW_VIN fault has occurred
2	IIN_OCF	R	Current Status	Input Over-Current Fault 0: Latched flag indicating no IIN OC fault has occurred. 1: Latched flag indicating a IIN OC fault has occurred.

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Table 66. STATUS_INPUT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	IIN_OCW	R	Current Status	Input Over-Current Warning 0: Latched flag indicating no IIN OC warning has occurred. 1: Latched flag indicating a IIN OC warning has occurred.
0	PIN_OPW	R	Current Status	Input Over-Power Warning 0: Latched flag indicating no input over-power warning has occurred. 1: Latched flag indicating a input over-power warning has occurred.

Per the description in the PMBus 1.3 specification, part II, TPSM831D31 does support clearing of status bits by writing to STATUS registers. Writing a 1 to any supported bit in this register will attempt to clear it as a fault condition.

7.5.25.6 (7Dh) STATUS_TEMPERATURE

The STATUS_TEMPERATURE command returns one byte of information relating to the status of the converter's temperature related faults.

The STATUS_TEMPERATURE command must be accessed through Read Byte/Write Byte transactions. STATUS_TEMPERATURE is a paged register. In order to access STATUS_TEMPERATURE command for channel A, PAGE must be set to 00h. In order to access STATUS_TEMPERATURE register for channel B, PAGE must be set to 01h. If PAGE is set FFh, the device return value will reflect the status of Channel A.

7	6	5	4	3	2	1	0
RW	RW	0	0	0	0	0	0
OTF	OTW	UTW	UTF	Reserved			

Figure 17. STATUS_TEMPERATURE Register

Table 67. STATUS_TEMPERATURE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OTF	RW	Current Status	Over-Temperature Fault 0: (Default) A temperature fault has not occurred. 1: A temperature fault has occurred.
6	OTW	RW	Current Status	Over-Temperature Warning 0: (Default) A temperature warning has not occurred. 1: A temperature warning has occurred.
5	UTW	R	0	Not supported and always set to 0.
4	UTF	R	0	Not supported and always set to 0.
3-0	Reserved	R	0000	Always set to 0.

Per the description in the PMBus 1.3 specification, part II, TPSM831D31 does support clearing of status bits by writing to STATUS registers. Writing a 1 to any supported bit in this register will attempt to clear it as a fault condition.

7.5.25.7 (7Eh) STATUS_CML

The STATUS_CML command returns one byte with contents regarding communication, logic, or memory conditions.

The STATUS_CML command must be accessed through Read Byte/Write Byte transactions. The STATUS_CML command is shared between Channel A and Channel B. All transactions to this command will affect both channels regardless of the PAGE command.

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7	6	5	4	3	2	1	0
RW	RW	RW	RW	0	0	RW	0
IV_CMD	IV_DATA	PEC_FAIL	MEM	PRO_FAULT	Reserved	COM_FAIL	CML_OTHER

Figure 18. STATUS_CML Register

Table 68. STATUS_CML Register Field Descriptions

Bit	Field	Type	Reset	Description
7	IV_CMD	RW	Current Status	Invalid or Unsupported Command Received 0: Latched flag indicating no invalid or unsupported command has been received. 1: Latched flag indicating an invalid or unsupported command has been received.
6	IV_DATA	RW	Current Status	Invalid or Unsupported Data Received 0: Latched flag indicating no invalid or unsupported data has been received. 1: Latched flag indicating an invalid or unsupported data has been received.
5	PEC_FAIL	RW	Current Status	Packet Error Check Failed 0: Latched flag indicating no packet error check has failed 1: Latched flag indicating a packet error check has failed
4	Reserved	R	0	Always set to 0.
3	MEM	RW	Current Status	Memory/NVM Error 0: Latched flag indicating no memory error has occurred 1: Latched flag indicating a memory error has occurred
2	Reserved	R	0	Always set to 0.
1	COM_FAIL	RW	Current Status	Other Communication Faults 0: Latched flag indicating no communication fault other than the ones listed in this table has occurred. 1: Latched flag indicating a communication fault other than the ones listed in this table has occurred.
0	CML_OTHER	R	0	Not supported and always set to 0.

Per the description in the PMBus 1.3 specification, part II, TPSM831D31 does support clearing of status bits by writing to STATUS registers. Writing a 1 to any bit in this register will attempt to clear it as a fault condition.

7.5.25.8 (80h) STATUS_MFR_SPECIFIC

The STATUS_MFR_SPECIFIC command returns one byte containing manufacturer-defined faults or warnings.

The STATUS_MFR_SPECIFIC command must be accessed through Read Byte/Write Byte transactions. STATUS_MFR_SPECIFIC is a paged register. In order to access STATUS_MFR_SPECIFIC command for channel A, PAGE must be set to 00h. In order to access STATUS_MFR_SPECIFIC register for channel B, PAGE must be set to 01h. If PAGE is set FFh, the device return value will reflect the status of Channel A.

Figure 19. STATUS_MFR_SPECIFIC Register

7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	0	0	RW
FLT_PS	VSNS_OPEN	MAX_PH_WARN	TSNS_LOW	RST_VID (Page 0)	Reserved		PHFLT

Table 69. STATUS_MFR_SPECIFIC Register Field Descriptions

Bit	Field	Type	Reset	Description
7	MFR_FAULT_PS	RW	Current Status	Power Stage Fault 0b: Latched flag indicating no fault from TI power stage has occurred. 1b: Latched flag indicating a fault from TI power stage has occurred.
6	VSNS_OPEN	RW	Current Status	VSNS pin open 0b: Latched flag indicating VSNS pin was not open at power-up. 1b: Latched flag indicating VSNS pin was open at power-up.

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Table 69. STATUS_MFR_SPECIFIC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	MAX_PH_WARN	RW	Current Status	Maximum Phase Warning If the selected operational phase number is larger than the maximum available phase number specified by the hardware, then MAX_PH_WARN is set, and the operational phase number is changed to the maximum available phase number. 0b: Latched flag indicating no maximum phase warning has occurred. 1b: Latched flag indicating a maximum phase warning has occurred.
4	TSNS_LOW	RW	Current Status	0b: Latched flag indicating that TSEN < 150 mV before soft-start. 1b: Latched flag indicating that TSEN ≥ 150 mV before soft-start.
3	RST_VID (Page 0)	RW	Current Status	RST_VID (Page 0 only) 0b: A VID reset operation has NOT occurred 1b: A VID reset operation has occurred
2:1	Reserved	R	00b	Always set to 0.
0	PHFLT	RW	Current Status	Phase current share fault. The PHFLT bit is set if any phase has current imbalance warnings occurring repetitively for 7 detection cycles (~500 µs continuously). Phases with current imbalance warnings may be read back via MFR_SPECIFIC_03. 0b: No repetitive current share fault has occurred 1b: Repetitive current share fault has occurred

Per the description in the PMBus 1.3 specification, part II, TPSM831D31 does support clearing of status bits by writing to STATUS registers. Writing a 1 to any supported bit in this register will attempt to clear it as a fault condition.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPSM831D31 device has a very simple design procedure. All programmable parameters can be configured by PMBus and stored in NVM as the new default values to minimize external component count. This design describes a typical 3-phase, 0.85-V, 120-A application and 1-phase 1.2-V, 40-A application.

8.2 Typical Application

The TPSM831D31 is a highly integrated, dual-output power module that supports PMBus commands. Use the following design procedure to select key component values and set the appropriate behavioral options through the PMBus.

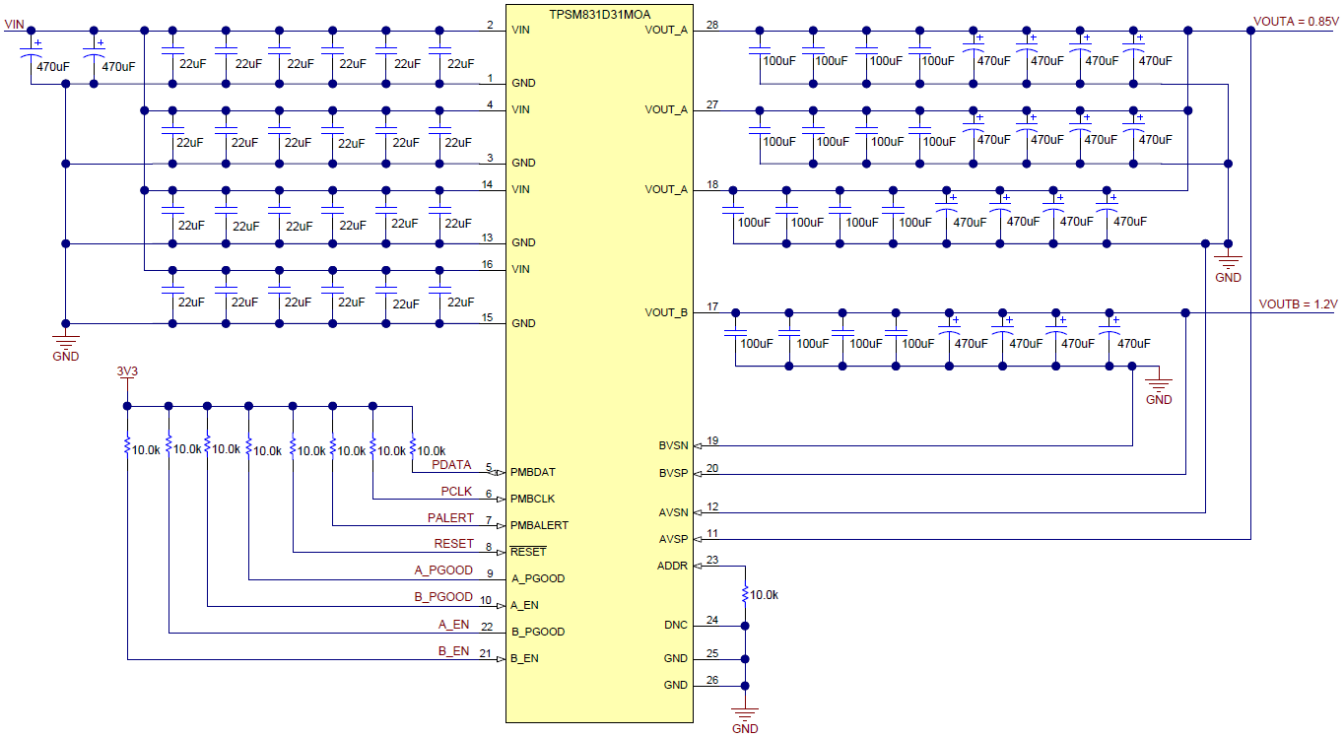


Figure 20. Typical Dual Output Schematic
(Dual Outputs: VOUTA = 0.85 V, 120 A and VOUTB =1.2 V, 40 A)

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8.2.1 Design Requirements

Table 70. Typical Application Specifications

	VOUTA	VOUTB
Input voltage range	10.8 V – 13.2 V	
Output voltage	0.85 V	1.2 V
I_{OUT}	120 A	40 A
$I_{DYN(max)}$	60 A	20 A
Switching frequeny (f_{SW})	400 kHz	

8.2.2 Detailed Design Procedure

For this design, the default settings inside the module are optimal for the application. The amount of input and output capacitors have been selected for operation up to full load for each output and for exceptional transient performance.

8.2.3 Application Performance Plot

The transient response waveform, Figure 21, is typical when using the specified input and output capacitors as shown Figure 20. The conditions shown in the waveform are: V_{IN} = 12 V, V_{OUT} = 1 V, 60-A load step at 100A/µs.

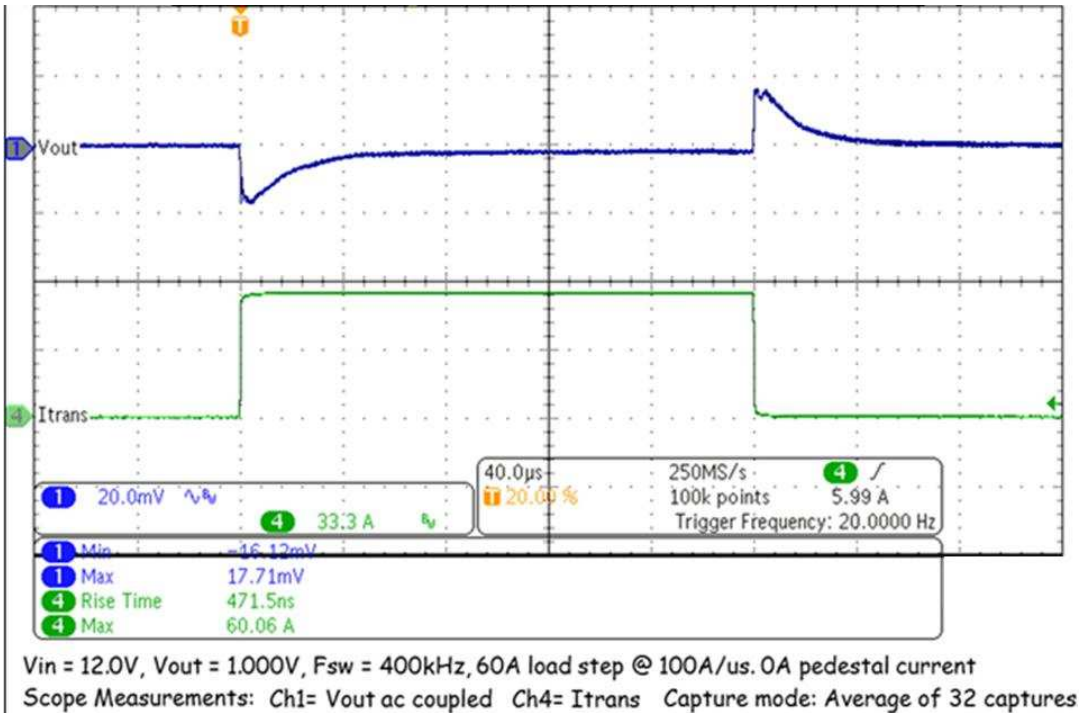


Figure 21. Typical Transient Response

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9 Power Supply Recommendations

The TPSM831D31 device is designed to operate from an input voltage supply between 8 V and 14 V. This supply must be well regulated. These devices are not designed for split-rail operation. Proper bypassing of input supplies and internal regulators is also critical for noise performance, as is PCB layout and grounding scheme.

10 Layout

10.1 Layout Guidelines

- Use the recommended land pattern including the via pattern for the module footprint.

10.2 Layout Examples

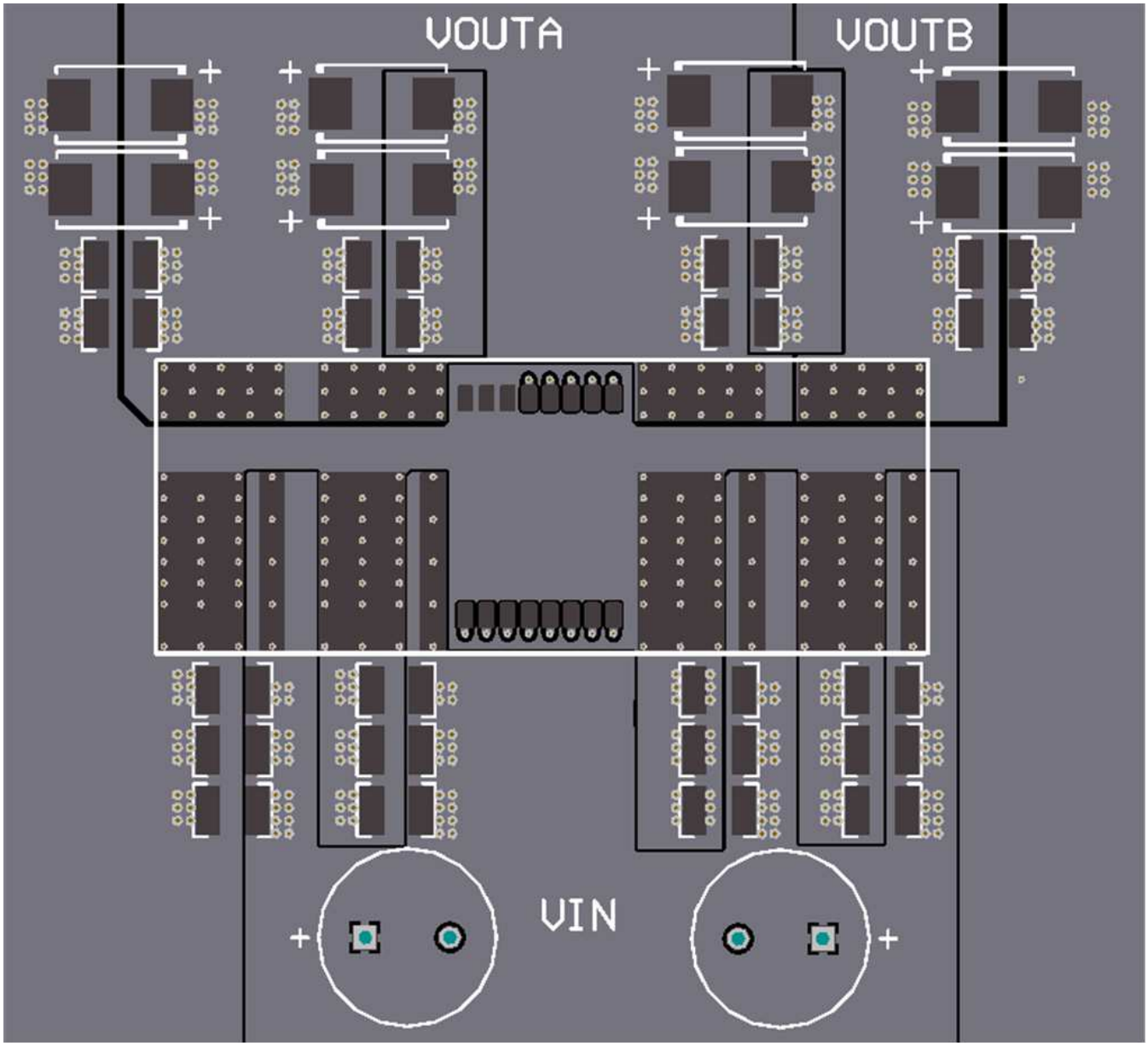


Figure 22. Top Layer (Top View)

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Layout Examples (continued)

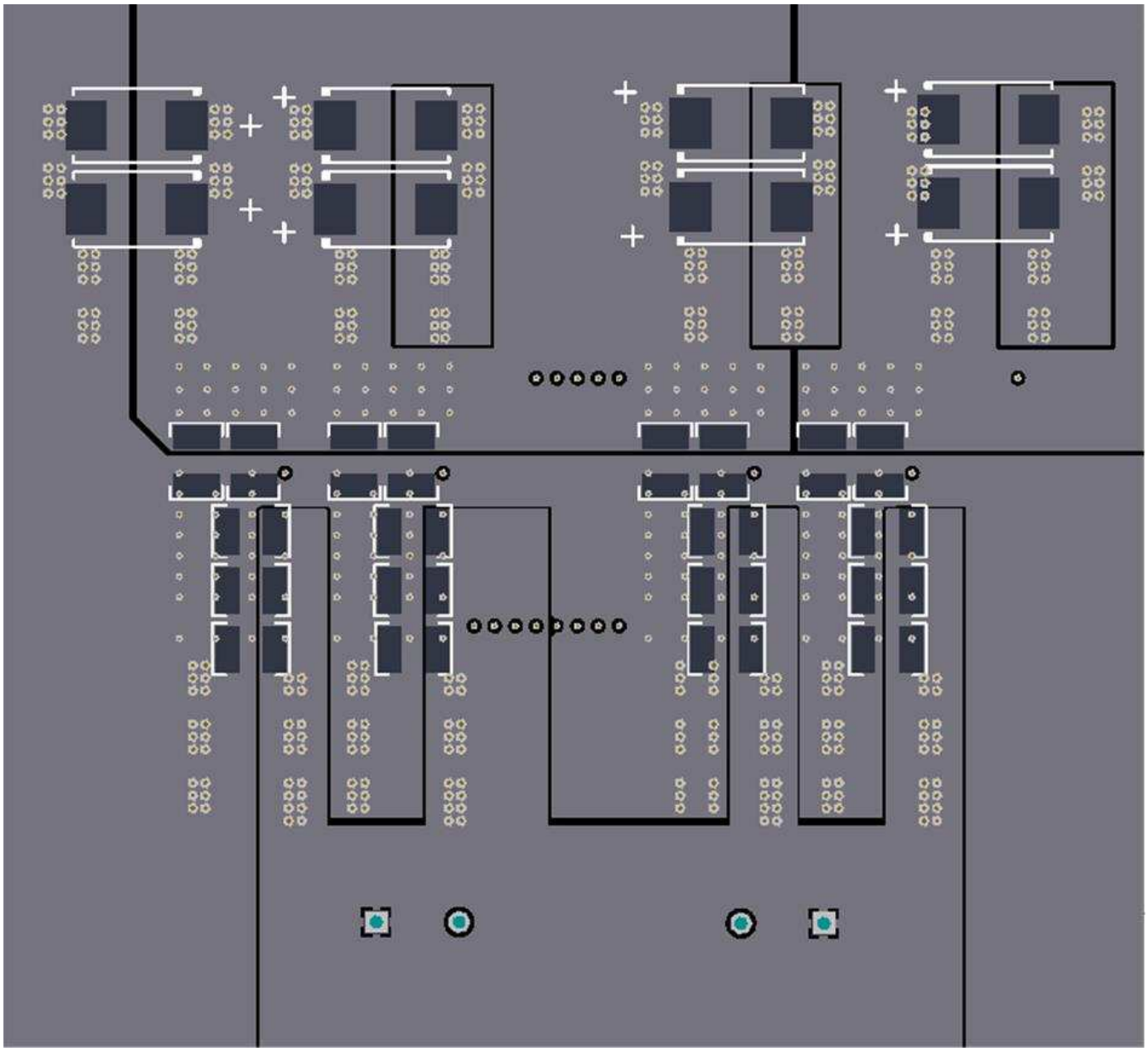


Figure 23. Bottom Layer (Top View)

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11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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11.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTPSM831D31MOA	ACTIVE	QFM	MOA	32	1	TBD	Call TI	Call TI	-40 to 105		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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