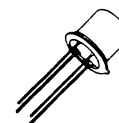


Silicon Controlled Switch



The General Electric Type 3N86 is a PLANAR PNPN silicon controlled switch (SCS) offering outstanding circuit design flexibility by providing leads to all four semiconductor regions. Unique fabrication processes based on planar oxide passivation have resulted in high reliability and uniformity at low cost. The SCS is thoroughly characterized at temperature extremes to permit worst case circuit design. The 3N86 can be considered an integrated PNP-NPN transistor pair in a positive feedback configuration. As such it offers fewer connections, fewer parts, lower cost and better characterization than is available from two separate transistors. Its characterization permits it to be used as an extremely sensitive SCR, as a complementary SCR, or as a "transistor" with "latching" capabilities. Type 3N86 is intended for applications requiring extremely low holding current, high triggering sensitivity at either gate and high turn-off gain.

FEATURES:

- Completely eliminates rate effect problems
- Dynamic and static breakover voltages are identical
- Extremely high triggering sensitivity at both gates
- Low holding current
- High turn-off gain
- Design parameters specified at worst-case temperatures
- Characterized for SCR and complementary SCR type applications
- Characterized as PNPN and also as transistor integrated pair
- All planar, completely oxide passivated
- Leads to all four semiconductor regions

absolute maximum ratings⁽¹⁾ (25°C) (unless otherwise specified)

Voltage

Anode to cathode forward and reverse
Anode gate to anode reverse
Cathode gate to cathode reverse

65 volts
65 volts
5 volts

Total Current

Continuous DC forward⁽²⁾
Peak recurrent forward ($T_A = 100^\circ\text{C}$, 100 μsec .
pulse width, 1% duty cycle)
Peak non-recurrent forward (10 μsec . pulse width)

200 ma
1.0 amps
5.0 amps

Gate Current (Forward Bias)

Continuous DC anode gate⁽²⁾
Peak anode gate ($T_A = 100^\circ\text{C}$, 100 μsec .
pulse width, 1% duty cycle)
Peak cathode gate ($T_A = 100^\circ\text{C}$, 100 μsec .
pulse width, 1% duty cycle)
Continuous DC cathode gate

100 ma
200 ma
500 ma
20 ma

Dissipation

Total power⁽²⁾
Cathode gate power⁽²⁾

400 mw
100 mw

Temperature

Operating junction
Storage

-65 to +150 °C
-65 to +200 °C

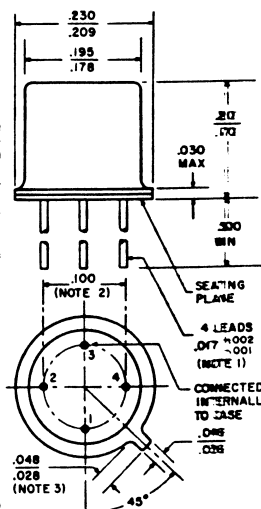
DIMENSIONS WITHIN
JEDEC OUTLINE TO-18
EXCEPT FOR
LEAD CONFIGURATION

NOTE 1: Lead diameter is controlled in the zone between .050 and .250 from the seating plane. Between .250 and end of lead a max. of .021 is held.

NOTE 2: Leads having maximum diameter (.019) measured in gaging plane .054 ± .001 — .000 below the seating plane of the device shall be within .007 of true position relative to a maximum width tab.

NOTE 3: Measured from max. diameter of the actual device.

PNP EMITTER 4
PNP BASE 3
PNP COLLECTOR 2
NPN BASE 1
NPN EMITTER 4
(A) ANODE
(C) CATHODE
CATHODE GATE 2
ANODE GATE 3
ALL DIMEN IN INCHES AND ARE REFERENCE UNLESS TOLERANCED



NOTE 1: Symbols and nomenclature are defined below.

NOTE 2: Derate currents and power linearly to 150°C, the maximum rated temperature. The absolute maximum rating at any given temperature shall be in terms of the more conservative of the two parameters, i.e., current or power.

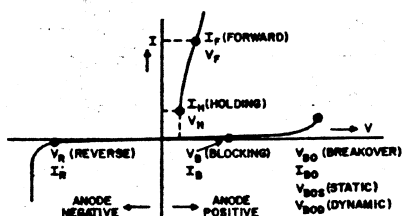


FIG. 1
ANODE TO CATHODE CHARACTERISTICS
NOTE - ABSENCE OF S IDENTIFIES ANODE TO CATHODE SYMBOLS. DOT IDENTIFIES OPERATING POINT. BRACKETS INDICATE MEANING OF SUBSCRIPT LETTER.

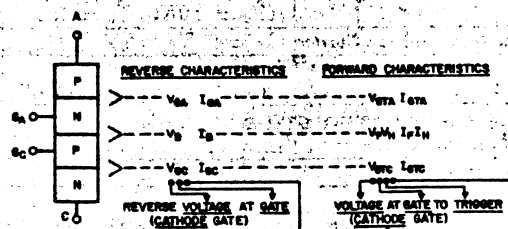


FIG. 2
REVERSE CHARACTERISTICS
FORWARD CHARACTERISTICS
NOTE: S IDENTIFIES GATE SYMBOLS. LAST LETTER (A OR C) MAY BE DROPPED IF NO AMBIGUITY RESULTS IN SPECIFIC CHARACTERIZATION. F MEANS "FORWARD" AND T MEANS "TRIGGER"

DEFINITION OF TERMS USED IN SCS SPECIFICATIONS

PNPN devices available at present do not have a common nomenclature. In part, this is due to their different construction and varied applications. SCS nomenclature permits the reverse characteristics of all three junctions to be specified. The anode forward characteristic and gate triggering characteristics can also be specified fully. The principles used in assigning symbols are illustrated below and with outline drawing above.

CUTOFF CHARACTERISTICS

Forward Blocking Current

 $(R_{GC} = 10K, V_{AC} = 65V)$

Reverse Blocking Current

 $(R_{GC} = 10K, V_{CA} = 65V)$ Cathode Gate Reverse Cutoff Current $(V_{GC} = -5V)$ Anode Gate Reverse Cutoff Current $(V_{GA} = -65V)$

CONDUCTING CHARACTERISTICS

Forward Voltage $(I_A = 200ma, R_{GC} = 10K)$ Forward Voltage $(I_A = 100ma, I_{GA} = 50ma, R_{GC} = 10K)$ Holding Current
 $(R_{GC} = 10K)$ Holding Current
 $(R_{GC} = 10K, I_{GA} = 50ma)$ Saturation Voltage $(G_A \text{ to } C) (I_{GC} = 5ma, I_{GA} = 50ma, I_A = 0)$ Saturation Voltage $(G_A \text{ to } C) (I_{GC} = 0, I_{GA} = 50ma, I_A = 5ma)$

TRIGGERING CHARACTERISTICS

Cathode Gate Current to Trigger

 $(I_{GTC} \text{ from current source, } V_{AC} = 40V, R_A = 800\Omega)$

Cathode Gate Current to Trigger

 $(I_{GTC} \text{ from current source, } V_{AC} = 40V, R_A = 800\Omega, I_{GA} = 50ma)$

Cathode Gate Voltage to Trigger

 $(V_{AC} = 40V, R_A = 800\Omega, R_{GC} = 10K, R_{GA} = \infty, I_{GTC} \text{ from current source})$

Cathode Gate Voltage to Trigger

 $(V_{AC} = 40V, R_A = 800\Omega, R_{GC} = 10K, I_{GA} = 50ma, I_{GTC} \text{ from current source})$

Anode Gate Current to Trigger

 $(I_{GTA} \text{ from current source, } V_{AC} = 40V, R_C = 800\Omega, R_{GC} = 10K)$

Anode Gate Voltage to Trigger

 $(I_{GTA} \text{ from current source, } V_{AC} = 40V, R_C = 800\Omega, R_{GC} = 10K, R_{GA} = 1K)$

TRANSIENT CHARACTERISTICS

Turn-On Time

 $(V_{AC} = 20V, I_A = 100ma, I_{GC} = 100\mu A) \text{ (See circuit, Figure 3)}$ Turn-On Time $(V_{AC} = 20V, I_A = 100ma, I_{GC} = 100\mu A, I_{GA} = 50ma)$

Recovery Time

 $(V_{AC} = 20V, I_A = 100ma, R_{GC} = 10K) \text{ (See circuit, Figure 4)}$ Recovery Time $(V_{AC} = 20V, I_A = 100ma, R_{GC} = 10K, I_{GA} = 50ma)$

Collector Capacitance Voltage Gate to Gate = 20V

Rate of Rise of Forward Blocking Voltage

Electrical Characteristics (25°C) (unless otherwise specified)

DC CHARACTERISTICS

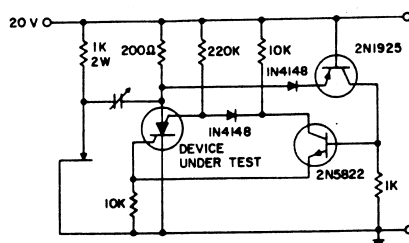
Collector to Base Breakdown Voltage $(I_C = [\pm] 1.0\mu A, I_B = 0)$ Emitter to Base Breakdown Voltage $(I_C = 0, I_B \text{ [NPN]} = 20\mu A, I_B \text{ [PNP]} = -1\mu A)$ Collector Saturation Voltage $(I_C = 50ma, I_B = 5ma)$ Base Saturation Voltage $(I_C = 1ma, I_B = 5ma)$ Forward Current Transfer Ratio $(V_{CE} = 0.5V, I_C = 3ma)$ Forward Current Transfer Ratio $(V_{CE} = -2.0V, I_C = -1ma)$ CUTOFF CHARACTERISTICS $(V_{AQ} = 65 \text{ volts})$ Collector to Emitter Leakage Current $(T_A = 150^\circ C)$ $(R_B = 10K\Omega, T_A = 150^\circ C)$ Collector to Base Leakage Current $(I_B = 0, T_A = 150^\circ C)$ Emitter to Base Leakage Current $(I_C = 0, T_A = 150^\circ C)$ $(V_{EB} = 5Vdc, I_C = 0)$

TRANSIENT CHARACTERISTICS

Collector Capacitance $(I_B = 0, V_{EB} = [\pm] 20V)$

Gain Bandwidth Product

NOTE 3: The transistor characterization is essentially a restatement of the SCS characterization and is meant to facilitate using the SCS as a complementary PNP-NPN integrated transistor pair.

NOTE 4: The $[\pm]$ sign indicates that the PNP and NPN transistors require opposite polarities as identified by the test conditions.
NOTE 5: The dv/dt rating is unlimited when the anode gate lead is returned to the anode voltage through a current limiting resistor.

RECOVERY TEST SET

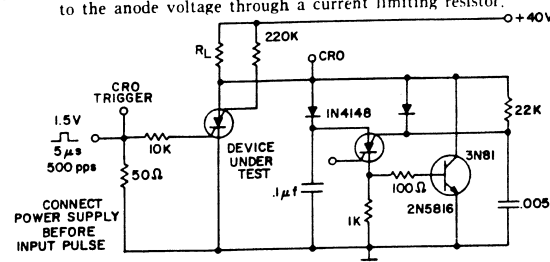
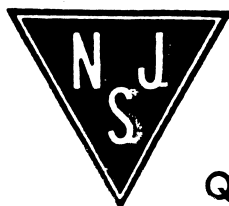


FIG. 4

TURN ON TIME TEST SET

SCS CHARACTERIZATION

TRANSISTOR CHARACTERIZATION



Quality Semi-Conductors