700MHz to 6GHz Low Power Direct Quadrature Modulator

FEATURES

- **Frequency Range: 700MHz to 6GHz**
- **Low Power: 2.7V to 3.6V Supply; 29.5mA**
- **Low LO Carrier Leakage: –43dBm at 1.8GHz**
- **Side-Band Suppression: –50dBc at 1.8GHz**
- **Output IP3: 19dBm at 1.8GHz**
- **Low RF Output Noise Floor: –157dBm/Hz at 30MHz Offset, P_{RF} = 1.8dBm, f_{RF} = 2.17GHz**
- **Sine Wave or Square Wave LO Drive**
- **SPI Control:**
  Adjustable Gain: 19dB in 1dB Steps
  Effecting Supply Current from 9mA to 39mA
  I/Q Offset Adjust: –64dBm LO Carrier Leakage
  I/Q Gain/Phase Adjust: –61dBc Side-Band Suppressed
- **24-Lead 4mm × 4mm Plastic QFN Package**

APPLICATIONS

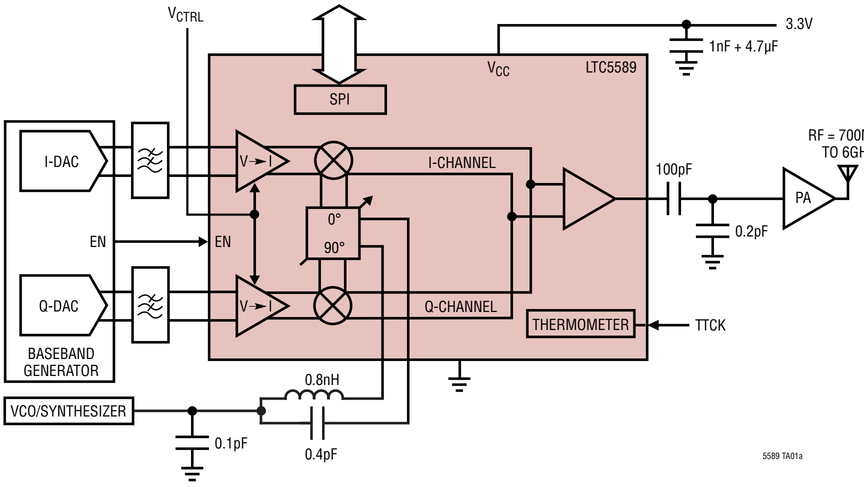
- Wireless Microphones
- Battery Powered Radios
- Vector Modulator
- 2.45GHz and 5.8GHz Transmitters
- Software Defined Radios (SDR)
- Military Radios

DESCRIPTION

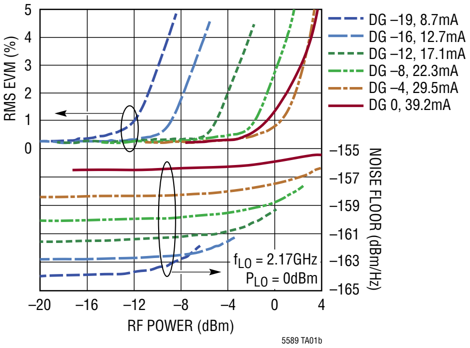
The LTC®5589 is a direct conversion I/Q modulator designed for low power wireless applications that enables direct modulation of differential baseband I and Q signals on an RF carrier. Single side-band modulation or side-band suppressed upconversion can be achieved by applying 90° phase-shifted signals to the I and Q inputs. The I/Q baseband input ports can be either AC or DC coupled to a source with a common mode voltage level of about 1.4V. The SPI interface controls the supply current, modulator gain, and allows adjustments of I and Q gain and phase imbalance to optimize the LO carrier feedthrough and side-band suppression. The LO port can be driven with sine wave or square wave LO drive. A fixed LC network on the LO and RF ports covers 700MHz to 6GHz operating range. An on-chip thermometer can be activated to compensate for gain-temperature variations. More accurate temperature measurements can be made using an on-chip diode. In addition, a continuous analog gain control (V_{CTRL}) pin can be used for fast power control.

TYPICAL APPLICATION

700MHz to 6GHz Direct Conversion Transmitter Application



EVM and Noise Floor vs RF Output Power and Digital Gain Setting with 1Ms/s 16-QAM Signal

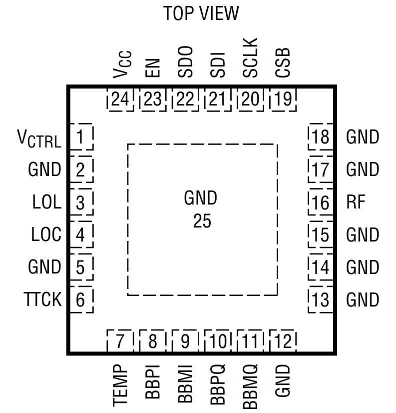


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage	3.8V
Common Mode Voltage of BBPI, BBMI, and BBPQ, BBMQ	2V
LOL, LOC DC Voltage	±50mV
LOL, LOC Input Power (Note 15)	20dBm
Output Current TEMP, SDO	10mA
Voltage on Any Pin (Note 16)	–0.3V to V_{CC} + 0.3V
T_{JMAX}	150°C
Case Operating Temperature Range	–40°C to 105°C
Storage Temperature Range	–65°C to 150°C

PIN CONFIGURATION



UF PACKAGE
24-LEAD (4mm × 4mm) PLASTIC QFN
T_{JMAX} = 150°C, θ_{JC} = 7°C/W
EXPOSED PAD (PIN 25) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

(**http://www.linear.com/product/LTC5589#orderinfo**)

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	CASE TEMPERATURE RANGE
LTC5589IUF#PBF	LTC5589IUF#TRPBF	5589	24-Lead (4mm × 4mm) Plastic QFN	–40°C to 105°C

Consult LTC Marketing for parts specified with wider operating temperature ranges..

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

Please refer to: http://www.linear.com/designtools/packaging/ for the most recent package drawings.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_C = 25°C. V_{CC} = 3.3V, EN = 3.3V, V_{CTRL} = 3.3V, P_{LO} = 0dBm, BBPI, BBMI, BBPQ, BBMQ common mode DC voltage V_{CMBB} = 1.4V_{DC}, I and Q baseband input signal = 2MHz, 2.1MHz, 1$V_{P-P(DIFF,\ I\ or\ Q)}$, I and Q 90° shifted, lower sideband selection, all registers set to default values, unless otherwise noted. Test circuit is shown in Figure 12.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{LO} = 800MHz, f_{RF1} = 797.9MHz, f_{RF2} = 798MHz, Register 0x00 = 0x70 (Decimal 112), L1 = 4.7nH, C5 = 2pF, C18 = 0.2pF							
$S_{22(ON)}$	RF Port Return Loss				–24		dB
$f_{LO(MATCH)}$	LO Match Frequency Range	S_{11} < –10dB			0.74 to 1.97		GHz
Gain	Conversion Voltage Gain	20 • Log ($V_{RF(OUT)(50\Omega)}/V_{IN(DIFF)(I\ or\ Q)}$)			–10.5		dB
P_{OUT}	Absolute Output Power	1$V_{P-P(DIFF)}$ CW Signal, I and Q			–6.5		dBm
OP1dB	Output 1dB Compression				4.1		dBm
OIP2	Output 2nd Order Intercept	(Note 5)			70.6		dBm
OIP3	Output 3rd Order Intercept	(Note 6)			19.9		dBm
NFloor	RF Output Noise Floor	No Baseband AC Input Signal (Note 3)			–159.6		dBm/Hz
SB	Side-Band Suppression	(Note 7)			–48		dBc

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_C = 25°C. V_{CC} = 3.3V, EN = 3.3V, V_{CTRL} = 3.3V, P_{LO} = 0dBm, BBPI, BBMI, BBPQ, BBMQ common mode DC voltage V_{CMBB} = 1.4V_{DC}, I and Q baseband input signal = 2MHz, 2.1MHz, 1$V_{P\text{-}P(DIFF,\ I\ or\ Q)}$, I and Q 90° shifted, lower sideband selection, all registers set to default values, unless otherwise noted. Test circuit is shown in Figure 12.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
LOFT	Carrier Leakage (LO Feedthrough)	(Note 7) EN = Low (Note 7)			–46 –71		dBm dBm
2LOFT	LO Feedthrough at 2xLO				–62.5		dBm
2LO	Signal Powers at 2xLO	Maximum of $2f_{LO} - 2f_{BB}$; $2f_{LO} - f_{BB}$; $2f_{LO} + f_{BB}$, $2f_{LO} + 2f_{BB}$			–49.1		dBc
3LOFT	LO Feedthrough at 3xLO				–57.9		dBm
3LO	Signal Powers at 3xLO	Maximum of $3f_{LO} - f_{BB}$; $3f_{LO} + f_{BB}$			–10.6		dBc
$BW1dB_{BB}$	–1dB Baseband Bandwidth	R_{SOURCE} = 50Ω, Differential			43		MHz
$BW3dB_{BB}$	–3dB Baseband Bandwidth	R_{SOURCE} = 50Ω, Differential			91		MHz
f_{LO} = 1800MHz, f_{RF1} = 1797.9MHz, f_{RF2} = 1798MHz, Register 0x00 = 0x4B (Decimal 75), L1 = 4.7nH, C5 = 2pF, C18 = 0.2pF							
$S_{22(ON)}$	RF Port Return Loss				–21		dB
$f_{LO(MATCH)}$	LO Match Frequency Range	S_{11} < –10dB			0.84 to 5.8		GHz
Gain	Conversion Voltage Gain	20 • Log ($V_{RF(OUT)(50\Omega)}/V_{IN(DIFF)(I\ or\ Q)}$)			–9.7		dB
P_{OUT}	Absolute Output Power	1$V_{P\text{-}P(DIFF)}$ CW Signal, I and Q			–5.7		dBm
OP1dB	Output 1dB Compression				4.6		dBm
OIP2	Output 2nd Order Intercept	(Note 5)			60.4		dBm
OIP3	Output 3rd Order Intercept	(Note 6)			19		dBm
NFloor	RF Output Noise Floor	No Baseband AC Input Signal (Note 3)			–158.8		dBm/Hz
SB	Side-Band Suppression	(Note 7)			–50		dBc
LOFT	Carrier Leakage (LO Feedthrough)	(Note 7) EN = Low (Note 7)			–43 –52		dBm dBm
2LOFT	LO Feedthrough at 2xLO				–61.3		dBm
2LO	Signal Powers at 2xLO	Maximum of $2f_{LO} - 2f_{BB}$; $2f_{LO} - f_{BB}$; $2f_{LO} + f_{BB}$, $2f_{LO} + 2f_{BB}$			–47		dBc
3LOFT	LO Feedthrough at 3xLO				–73.8		dBm
3LO	Signal Powers at 3xLO	Maximum of $3f_{LO} - f_{BB}$; $3f_{LO} + f_{BB}$			–18.6		dBc
	Gain from LO to RF	BBPI = BBPQ = 1.9V			10		dB
	LO Input Noise Figure	BBMI = BBMQ = 0.9V			12.5		dB
	LO Input 3rd Order Intercept	(Vector Modulator)			–2		dBm
$BW1dB_{BB}$	–1dB Baseband Bandwidth	R_{SOURCE} = 50Ω, Differential			92		MHz
$BW3dB_{BB}$	–3dB Baseband Bandwidth	R_{SOURCE} = 50Ω, Differential			168		MHz
f_{LO} = 2500MHz, f_{RF1} = 2497.9MHz, f_{RF2} = 2498MHz, Register 0x00 = 0x3F (Decimal 63), L1 = 4.7nH, C5 = 2pF, C18 = 0.2pF							
$S_{22(ON)}$	RF Port Return Loss				–21		dB
$f_{LO(MATCH)}$	LO Match Frequency Range	S_{11} < –10dB			0.86 to 6		GHz
Gain	Conversion Voltage Gain	20 • Log ($V_{RF(OUT)(50\Omega)}/V_{IN(DIFF)(I\ or\ Q)}$)			–10.2		dB
P_{OUT}	Absolute Output Power	1$V_{P\text{-}P(DIFF)}$ CW Signal, I and Q			–6.2		dBm
OP1dB	Output 1dB Compression				3.9		dBm
OIP2	Output 2nd Order Intercept	(Note 5)			62		dBm
OIP3	Output 3rd Order Intercept	(Note 6)			17.5		dBm

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_C = 25°C. V_{CC} = 3.3V, EN = 3.3V, V_{CTRL} = 3.3V, P_{LO} = 0dBm, BBPI, BBMI, BBPQ, BBMQ common mode DC voltage V_{CMBB} = 1.4V_{DC}, I and Q baseband input signal = 2MHz, 2.1MHz, 1$V_{P-P(DIFF,\ I\ or\ Q)}$, I and Q 90° shifted, lower sideband selection, all registers set to default values, unless otherwise noted. Test circuit is shown in Figure 12.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
NFloor	RF Output Noise Floor	No Baseband AC Input Signal (Note 3) P_{OUT} = 1.8dBm (Note 17)			–158.1 –157		dBm/Hz dBm/Hz
SB	Side-Band Suppression	(Note 7)			–41.5		dBc
LOFT	Carrier Leakage (LO Feedthrough)	(Note 7) EN = Low (Note 7)			–40.2 –50		dBm dBm
2LOFT	LO Feedthrough at 2xLO				–65.4		dBm
2LO	Signal Powers at 2xLO	Maximum of $2f_{LO} – 2f_{BB}$; $2f_{LO} – f_{BB}$; $2f_{LO} + f_{BB}$, $2f_{LO} + 2f_{BB}$			–48.8		dBc
3LOFT	LO Feedthrough at 3xLO				–77.2		dBm
3LO	Signal Powers at 3xLO	Maximum of $3f_{LO} – f_{BB}$; $3f_{LO} + f_{BB}$			–25.9		dBc
$BW1dB_{BB}$	–1dB Baseband Bandwidth	R_{SOURCE} = 50Ω, Differential			65		MHz
$BW3dB_{BB}$	–3dB Baseband Bandwidth	R_{SOURCE} = 50Ω, Differential			167		MHz
f_{LO} = 3500MHz, f_{RF1} = 3497.9MHz, f_{RF2} = 3498MHz, Register 0x00 = 0x2F (Decimal 47), L1 = 0.8nH, C5 = 0.4pF, C18 = 0.1pF (5.8GHz LO Match)							
$S_{22(ON)}$	RF Port Return Loss				–25		dB
$f_{LO(MATCH)}$	LO Match Frequency Range	S_{11} < –10dB			1.2 to 6		GHz
Gain	Conversion Voltage Gain	20 • Log ($V_{RF(OUT)(50Ω)}$/$V_{IN(DIFF)(I\ or\ Q)}$)			–12.7		dB
P_{OUT}	Absolute Output Power	1$V_{P-P(DIFF)}$ CW Signal, I and Q			–8.7		dBm
OP1dB	Output 1dB Compression	(Note 18)			1.1		dBm
OIP2	Output 2nd Order Intercept	(Note 5)			41.8		dBm
OIP3	Output 3rd Order Intercept	(Note 6)			14.6		dBm
NFloor	RF Output Noise Floor	No Baseband AC Input Signal (Note 3)			–159.6		dBm/Hz
SB	Side-Band Suppression	(Note 7)			–43		dBc
LOFT	Carrier Leakage (LO Feedthrough)	(Note 7) EN = Low (Note 7)			–34.5 –39.8		dBm dBm
2LOFT	LO Feedthrough at 2xLO				–66.5		dBm
2LO	Signal Powers at 2xLO	Maximum of $2f_{LO} – 2f_{BB}$; $2f_{LO} – f_{BB}$; $2f_{LO} + f_{BB}$, $2f_{LO} + 2f_{BB}$			–46.3		dBc
3LOFT	LO Feedthrough at 3xLO				–71.4		dBm
3LO	Signal Powers at 3xLO	Maximum of $3f_{LO} – f_{BB}$; $3f_{LO} + f_{BB}$			–31.7		dBc
$BW1dB_{BB}$	–1dB Baseband Bandwidth	R_{SOURCE} = 50Ω, Differential			76		MHz
$BW3dB_{BB}$	–3dB Baseband Bandwidth	R_{SOURCE} = 50Ω, Differential			173		MHz
f_{LO} = 4500MHz, f_{RF1} = 4497.9MHz, f_{RF2} = 4498MHz, Register 0x00 = 0x24 (Decimal 36), L1 = 0.8nH, C5 = 0.4pF, C18 = 0.1pF (5.8GHz LO Match)							
$S_{22(ON)}$	RF Port Return Loss				–20		dB
$f_{LO(MATCH)}$	LO Match Frequency Range	S_{11} < –10dB			1.3 to 6		GHz
Gain	Conversion Voltage Gain	20 • Log ($V_{RF(OUT)(50Ω)}$/$V_{IN(DIFF)(I\ or\ Q)}$)			–16.3		dB
P_{OUT}	Absolute Output Power	1$V_{P-P(DIFF)}$ CW Signal, I and Q			–12.3		dBm
OP1dB	Output 1dB Compression	(Note 18)			–2.2		dBm
OIP2	Output 2nd Order Intercept	(Note 5)			35.2		dBm
OIP3	Output 3rd Order Intercept	(Note 6)			11.2		dBm
NFloor	RF Output Noise Floor	No Baseband AC Input Signal (Note 3)			–161.3		dBm/Hz

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_C = 25°C. V_{CC} = 3.3V, EN = 3.3V, V_{CTRL} = 3.3V, P_{LO} = 0dBm, BBPI, BBMI, BBPQ, BBMQ common mode DC voltage V_{CMBB} = $1.4V_{DC}$, I and Q baseband input signal = 2MHz, 2.1MHz, $1V_{P-P(DIFF,\ I\ or\ Q)}$, I and Q 90° shifted, lower sideband selection, all registers set to default values, unless otherwise noted. Test circuit is shown in Figure 12.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SB	Side-Band Suppression	(Note 7)			–44		dBc
LOFT	Carrier Leakage (LO Feedthrough)	(Note 7) EN = Low (Note 7)			–33 –34		dBm dBm
2LOFT	LO Feedthrough at 2xLO				–67		dBm
2LO	Signal Powers at 2xLO	Maximum of $2f_{LO} – 2f_{BB}$; $2f_{LO} – f_{BB}$; $2f_{LO} + f_{BB}$, $2f_{LO} + 2f_{BB}$			–45		dBc
3LOFT	LO Feedthrough at 3xLO				–73		dBm
3LO	Signal Powers at 3xLO	Maximum of $3f_{LO} – f_{BB}$; $3f_{LO} + f_{BB}$			–42		dBc
$BW1dB_{BB}$	–1dB Baseband Bandwidth	R_{SOURCE} = 50Ω, Differential			98		MHz
$BW3dB_{BB}$	–3dB Baseband Bandwidth	R_{SOURCE} = 50Ω, Differential			176		MHz
f_{LO} = 5800MHz, f_{RF1} = 5797.9MHz, f_{RF2} = 5798MHz, Register 0x00 = 0x1A (Decimal 26), L1 = 0.8nH, C5 = 0.4pF, C18 = 0.1pF (5.8GHz LO Match)							
$S_{22(ON)}$	RF Port Return Loss				–14.8		dB
$f_{LO(MATCH)}$	LO Match Frequency Range	S_{11} < –10dB			1.3 to 6		GHz
Gain	Conversion Voltage Gain	20 • Log ($V_{RF(OUT)(50Ω)}/V_{IN(DIFF)(I\ or\ Q)}$)			–21		dB
P_{OUT}	Absolute Output Power	$1V_{P-P(DIFF)}$ CW Signal, I and Q			–17		dBm
OP1dB	Output 1dB Compression	(Note 18)			–7.1		dBm
OIP2	Output 2nd Order Intercept	(Note 5)			28.3		dBm
OIP3	Output 3rd Order Intercept	(Note 6)			7		dBm
NFloor	RF Output Noise Floor	No Baseband AC Input Signal (Note 3)			–162.7		dBm/Hz
SB	Side-Band Suppression	(Note 7)			–31		dBc
LOFT	Carrier Leakage (LO Feedthrough)	(Note 7) EN = Low (Note 7)			–37.6 –29.9		dBm dBm
2LOFT	LO Feedthrough at 2xLO				–72.5		dBm
2LO	Signal Powers at 2xLO	Maximum of $2f_{LO} – 2f_{BB}$; $2f_{LO} – f_{BB}$; $2f_{LO} + f_{BB}$, $2f_{LO} + 2f_{BB}$			–46.9		dBc
3LOFT	LO Feedthrough at 3xLO				–78.6		dBm
3LO	Signal Powers at 3xLO	Maximum of $3f_{LO} – f_{BB}$; $3f_{LO} + f_{BB}$			–53.3		dBc
$BW1dB_{BB}$	–1dB Baseband Bandwidth	R_{SOURCE} = 50Ω, Differential			100		MHz
$BW3dB_{BB}$	–3dB Baseband Bandwidth	R_{SOURCE} = 50Ω, Differential			181		MHz
Analog Variable Gain Control (V_{CTRL})							
$V_{CTRL}R$	Gain Control Voltage Range	Set Bit 6 in Register 0x01			0.9 to 3.3		V
G_{CTRL}	Gain Control Gain Range	Set Bit 6 in Register 0x01			–73 to –10		dB
τ_{CTRL}	Gain Control Response Time	Set Bit 6 in Register 0x01 (Note 8)			20		ns
Z_{CTRL}	Gain Control Input Impedance	Set Bit 6 in Register 0x01			10		pF
I_{CTRL}	DC Input Current	Set Bit 6 in Register 0x01 Clear Bit 6 in Register 0x01			2.55 0		mA mA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_C = 25°C. V_{CC} = 3.3V, EN = 3.3V, V_{CTRL} = 3.3V, P_{LO} = 0dBm, BBPI, BBMI, BBPQ, BBMQ common mode DC voltage V_{CMBB} = 1.4V_{DC}, I and Q baseband input signal = 2MHz, 2.1MHz, 1$V_{P-P(DIFF,\ I\ or\ Q)}$, I and Q 90° shifted, lower sideband selection, all registers set to default values, unless otherwise noted. Test circuit is shown in Figure 12.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Baseband Inputs (BBPI, BBMI, BBPQ, BBMQ)							
V_{CMBB}	DC Common Mode Voltage	Internally Generated			1.41		V
$R_{IN(DIFF)}$	Input Resistance	Differential			1.8		kΩ
$R_{IN(CM)}$	Common Mode Input Resistance	Four Baseband Pins Shorted			350		Ω
$I_{BB(OFF)}$	Baseband Leakage Current	Four Baseband Pins Shorted, EN = Low			1.3		nA
V_{SWING}	Amplitude Swing	No Hard Clipping, Single-Ended, Digital Gain (DG) = –10			1.2		V_{P-P}
Power Supply (V_{CC})							
V_{CC}	Supply Voltage Range		●	2.7		3.6	V
$V_{RET(MIN)}$	Minimum Data Retention Voltage	(Note 14)	●	1.8	1.5		V
$I_{CC(ON)}$	Supply Current	EN = High		20	29.5	37	mA
$I_{CC(RANGE)}$	Supply Current Range	EN = High, Register 0x01 = 0x00			39		mA
		EN = High, Register 0x01 = 0x13			9		mA
$I_{CC(OFF)}$	Supply Current, Sleep Mode	EN = 0V			0.6	9	µA
t_{ON}	Turn-On Time	EN = Low to High (Notes 8, 12)			30		ns
t_{OFF}	Turn-Off Time	EN = High to Low (Notes 9, 12)			33		ns
t_{SB}	Side-Band Suppression Settling	Register 0x00 Change, <–50dBc (Notes 12, 18)			350		ns
t_{LO}	LO Suppression Settling	Register 0x02 Change, <–60dBm (Note 12)			125		ns
Serial Port (CSB, SCLK, SDI, SDO), Enable (EN) and TTCK, SCLK = 20MHz							
V_{IH}	Input High Voltage		●	1.1			V
V_{IL}	Input Low Voltage		●			0.2	V
I_{IH}	Input High Current				0.02		nA
I_{IL}	Input Low Current				–0.4		nA
V_{OH}	Output High Voltage	(Note 13)	●	V_{CC_L} – 0.2			V
V_{OL}	Output Low Voltage	I_{SINK} = 8mA (Note 10)	●			0.7	V
I_{OH}	SDO Leakage Current	for SDO = High			0.5		nA
V_{HYS}	Input Trip Point Hysteresis				110		mV
t_{CKH}	SCLK High Time		●	22.5			ns
t_{CSS}	CSB Setup Time		●	20			ns
t_{CSH}	CSB High Time		●	30			ns
t_{CS}	SDI to SCLK Setup Time		●	20			ns
t_{CH}	SDI to SCLK Hold Time		●	10			ns
t_{DO}	SCLK to SDO Time		●	45			ns
$t_{C\%}$	SCLK Duty Cycle		●	45	50	55	%
f_{CLK}	Maximum SCLK Frequency		●	20			MHz
V_{TEMP}	Temperature Diode Voltage	I_{TEMP} = 100µA			772		mV
	Temperature Slope	I_{TEMP} = 100µA			–1.5		mV/°C

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC5589 is guaranteed functional over the operating case temperature range from –40°C to 105°C.

Note 3: At 6MHz offset from the LO signal frequency. 100nF between BBPI and BBMI, 100nF between BBPQ and BBMQ.

Note 4: The Default Register Settings are listed in Table 1.

Note 5: IM2 is measured at f_{LO} – 4.1MHz.

Note 6: IM3 is measured at f_{LO} – 2.2MHz and f_{LO} – 1.9MHz. OIP3 = lowest of (1.5 • P{f_{LO} – 2.1MHz} – 0.5 • P{f_{LO} – 2.2MHz}) and (1.5 • P{f_{LO} – 2MHz} – 0.5 • P{f_{LO} – 1.9MHz}).

Note 7: Without side-band or LO feedthrough nulling (unadjusted).

Note 8: RF power is within 10% of final value.

Note 9: RF power is at least 30dB down from its ON state.

Note 10: V_{OL} voltage scales linear with current sink. For example for $R_{PULL\text{-}UP}$ = 1kΩ, V_{CC_L} = 3.3V the SDO sink current is about (3.3 – 0.2) /1kΩ = 3.1mA. Max V_{OL} = 0.7 • 3.1/8 = 0.271V, with $R_{PULL\text{-}UP}$ the SDO pull-up resistor and V_{CC_L} the digital supply voltage to which $R_{PULL\text{-}UP}$ is connected to.

Note 11: I and Q baseband Input signal = 2MHz CW, 0.8$V_{P\text{-}P,\ DIFF}$ each, I and Q 0° shifted.

Note 12: f_{LO} = 1800MHz, P_{LO} = 0dBm, C4 = 10pF

Note 13: Maximum V_{OH} is derated for capacitive load using the following formula: V_{CC_L} • exp (–0.5 • T_{CLK}/($R_{PULL\text{-}UP}$ • C_{LOAD}), with T_{CLK} the time of one SCLK cycle, $R_{PULL\text{-}UP}$ the SDO pull-up resistor, V_{CC_L} the digital supply voltage to which $R_{PULL\text{-}UP}$ is connected to, and C_{LOAD} the capacitive load at the SDO pin. For example for T_{CLK} = 100ns (10MHz SCLK), $R_{PULL\text{-}UP}$ = 1kΩ, C_{LOAD} = 10pF and V_{CC_L} = 3.3V the derating is 3.3 • exp(–5) = 22.2mV, thus maximum V_{OH} = 3.3V – 0.1 – 0.0222 = 3.177V.

Note 14: Minimum V_{CC} in order to retain register data content.

Note 15: Guaranteed by design and characterization. This parameter is not tested.

Note 16: RF pin guaranteed by design while using a 100pF coupling capacitor. The RF pin is not tested.

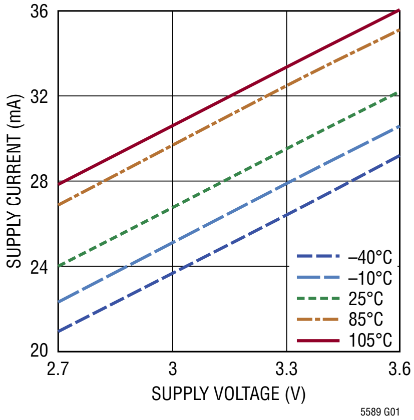
Note 17: f_{LO} = 2.17GHz, f_{NOISE} = 2.14GHz, f_{BB} = 2kHz. 100nF between BBPI and BBMI, 100nF between BBPQ and BBMQ.

Note 18: Using 2.14GHz bandpass filter with BW = 5MHz, f_{BB} = 25MHz, f_{LO} = 2.115GHz, measured from parallel load (see Figure 7).

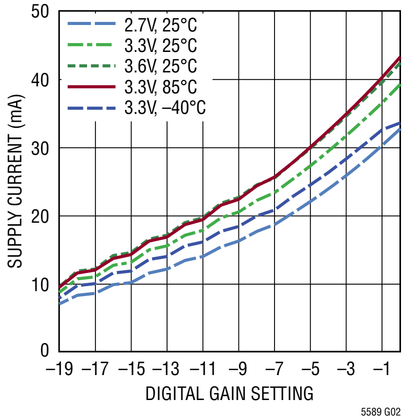
TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 3.3V, EN = 3.3V, V_{CTRL} = 3.3V, T_C = 25°C, P_{LO} = 0dBm, f_{LO} = 1.8GHz, BBPI, BBMI, BBPQ, BBMQ common mode DC voltage V_{CMBB} = 1.4V_{DC}, I and Q baseband input signal = 2MHz, 2.1MHz, 1$V_{P\text{-}P(DIFF,\ I\ or\ Q)}$, I and Q 90° shifted, lower sideband selection, TEMPUPDT = 0, register 0x00 value according to Table 6, all other registers set to default values, unless otherwise noted. Test circuit is shown in Figure 12.

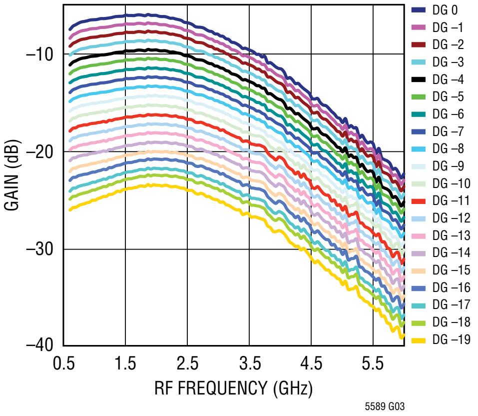
Supply Current vs Supply Voltage



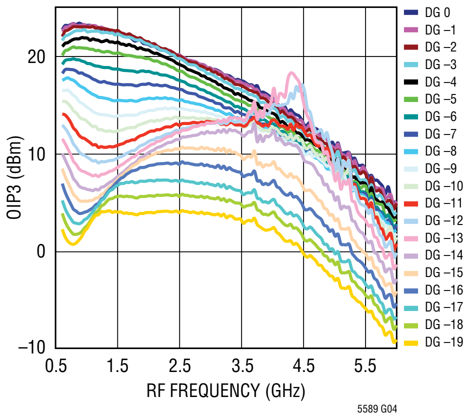
Supply Current vs Digital Gain Setting



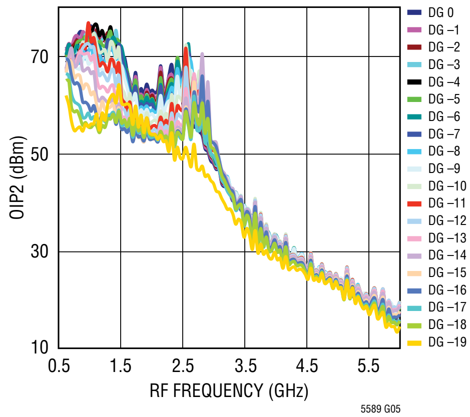
Gain vs RF Frequency and Digital Gain Setting



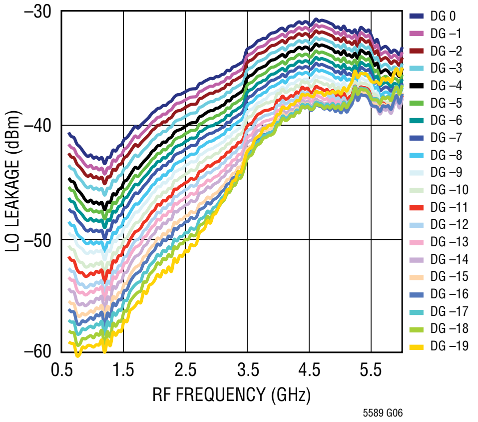
Output IP3 vs RF Frequency and Digital Gain Setting



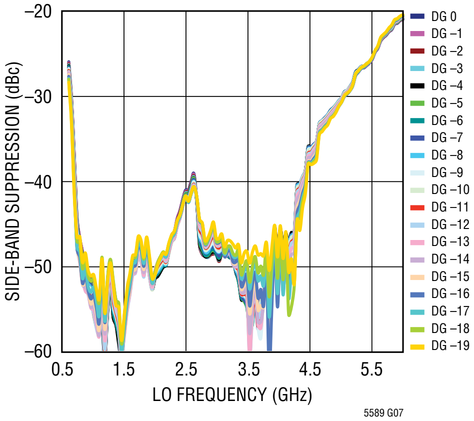
Output IP2 vs RF Frequency and Digital Gain Setting



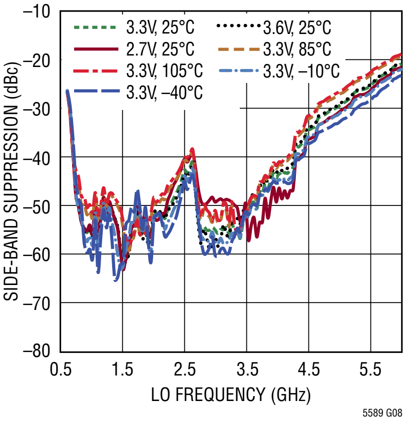
LO Leakage vs RF Frequency and Digital Gain Setting



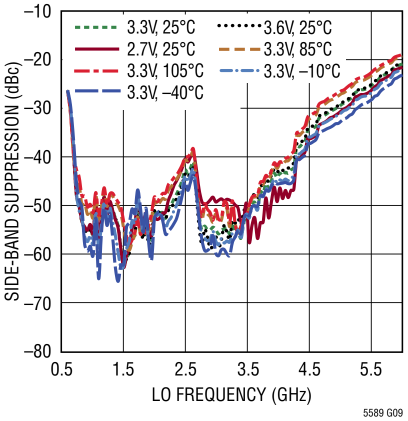
Side-Band Suppression vs LO Frequency and Digital Gain Setting



Side-Band Suppression vs LO Frequency for Gain TempComp Off



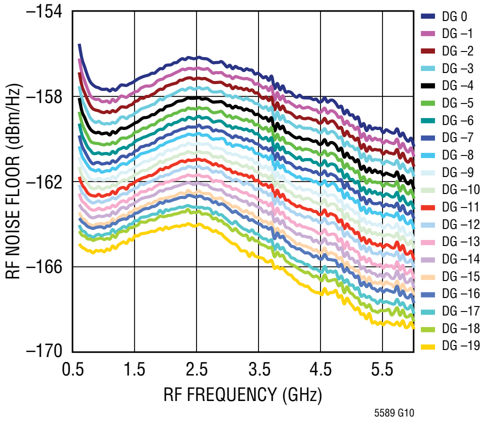
Side-Band Suppression vs LO Frequency for Gain TempComp On



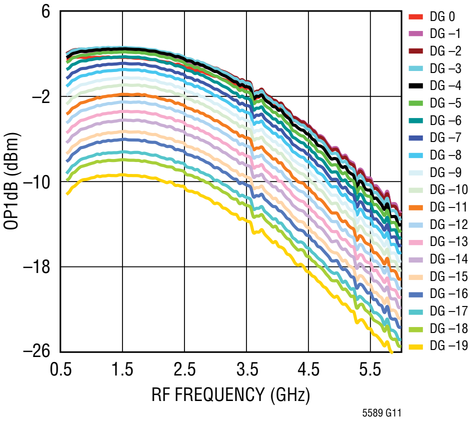
TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 3.3V, EN = 3.3V, V_{CTRL} = 3.3V, T_C = 25°C, P_{LO} = 0dBm, f_{LO} = 1.8GHz, BBPI, BBMI, BBPQ, BBMQ common mode DC voltage V_{CMBB} = 1.4V_{DC}, I and Q baseband input signal = 2MHz, 2.1MHz, 1$V_{P\text{-}P(DIFF,\ I\ or\ Q)}$, I and Q 90° shifted, lower sideband selection, TEMPUPDT = 0, register 0x00 value according to Table 6, all other registers set to default values, unless otherwise noted. Test circuit is shown in Figure 12.

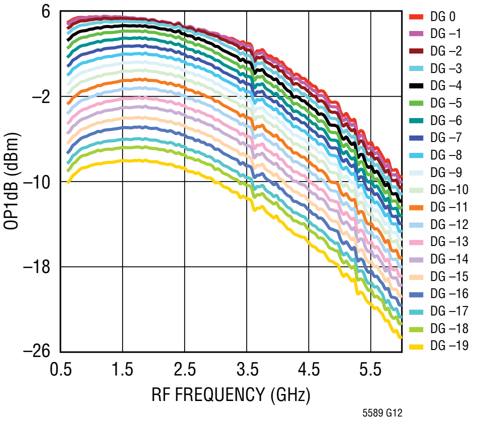
Noise Floor vs RF Frequency and Digital Gain Setting



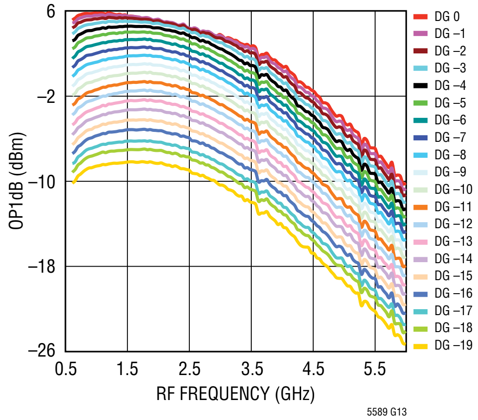
Output 1dB Compression Point vs RF Frequency and Digital Gain Setting and 2.7V Supply



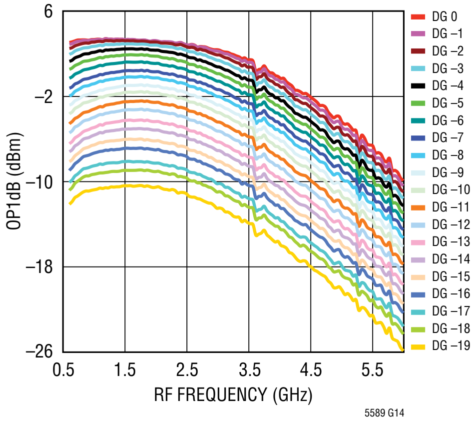
Output 1dB Compression Point vs RF Frequency and Digital Gain Setting and 3.3V Supply



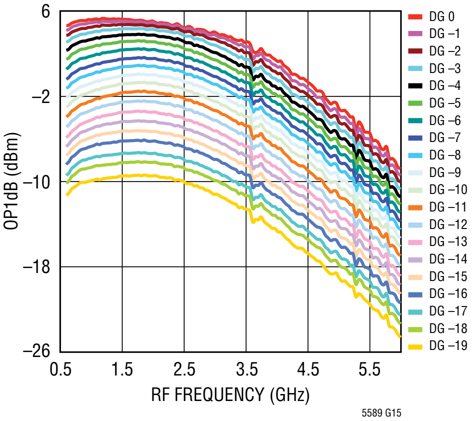
Output 1dB Compression Point vs RF Frequency and Digital Gain Setting and 3.6V Supply



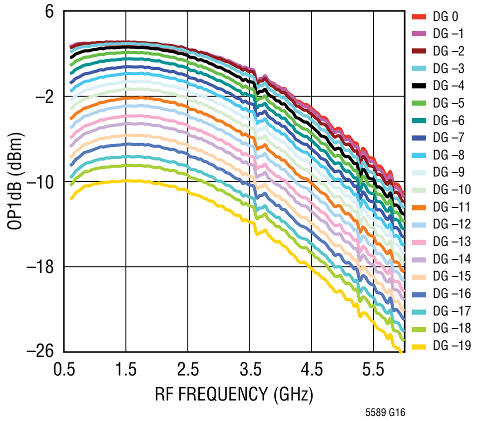
Output 1dB Compression Point vs RF Frequency and Digital Gain Setting at 2.7V Supply, –40°C



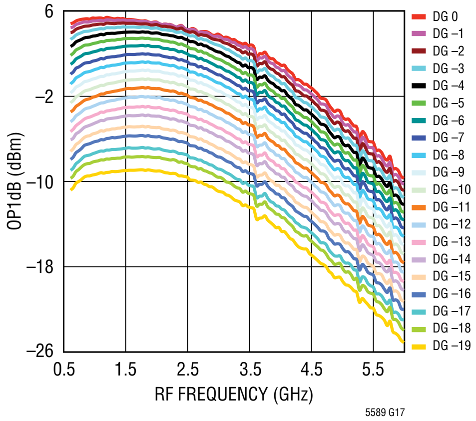
Output 1dB Compression Point vs RF Frequency and Digital Gain Setting at 3.3V Supply, –40°C



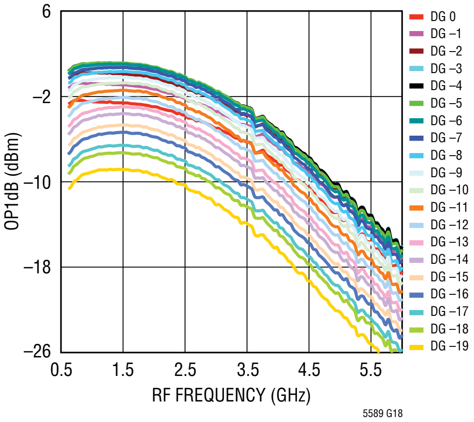
Output 1dB Compression Point vs RF Frequency and Digital Gain Setting at 2.7V Supply, –10°C



Output 1dB Compression Point vs RF Frequency and Digital Gain Setting at 3.3V Supply, –10°C



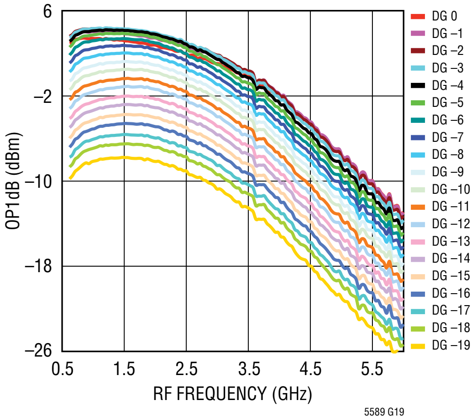
Output 1dB Compression Point vs RF Frequency and Digital Gain Setting at 2.7V Supply, 85°C



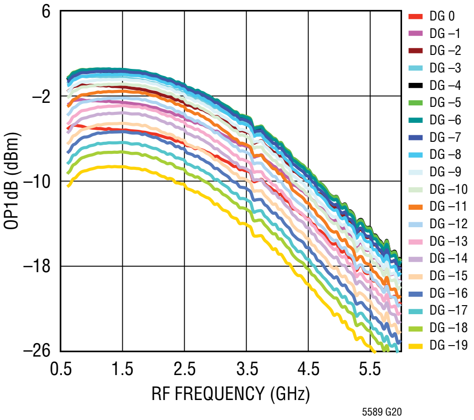
TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 3.3V, EN = 3.3V, V_{CTRL} = 3.3V, T_C = 25°C, P_{LO} = 0dBm, f_{LO} = 1.8GHz, BBPI, BBMI, BBPQ, BBMQ common mode DC voltage V_{CMBB} = 1.4V_{DC}, I and Q baseband input signal = 2MHz, 2.1MHz, 1$V_{P-P(DIFF,\ I\ or\ Q)}$, I and Q 90° shifted, lower sideband selection, TEMPUPDT = 0, register 0x00 value according to Table 6, all other registers set to default values, unless otherwise noted. Test circuit is shown in Figure 12.

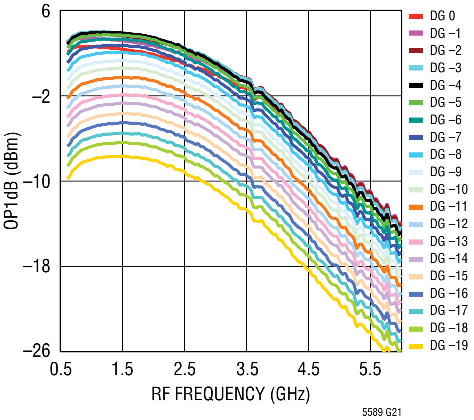
Output 1dB Compression Point vs RF Frequency and Digital Gain Setting at 3.3V Supply, 85°C



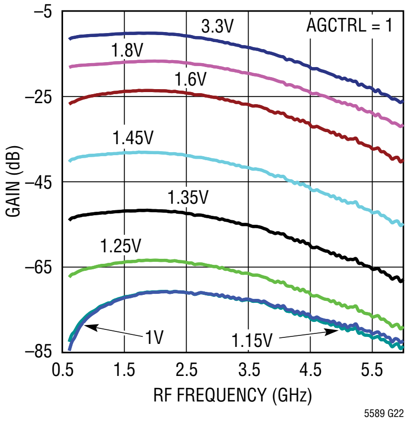
Output 1dB Compression Point vs RF Frequency and Digital Gain Setting at 2.7V Supply, 105°C



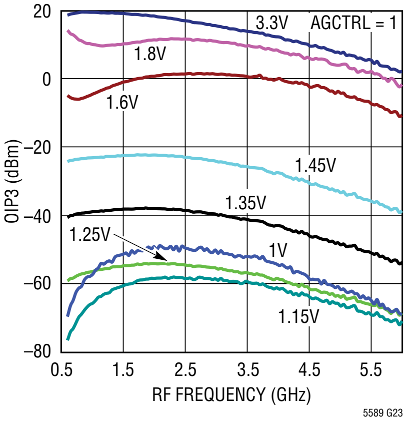
Output 1dB Compression Point vs RF Frequency and Digital Gain Setting at 3.3V Supply, 105°C



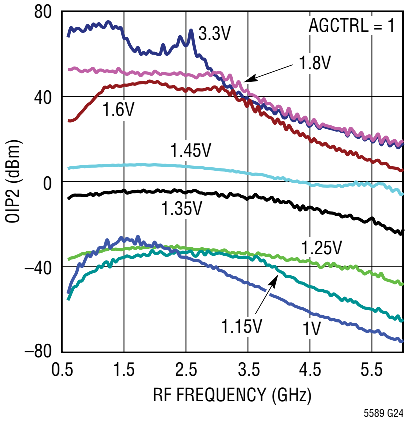
Gain vs RF Frequency and V_{CTRL}



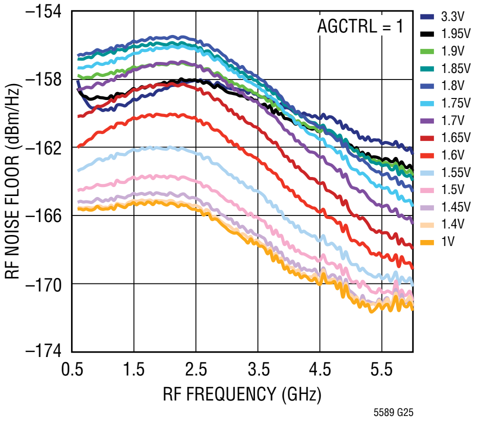
Output IP3 vs RF Frequency and V_{CTRL}



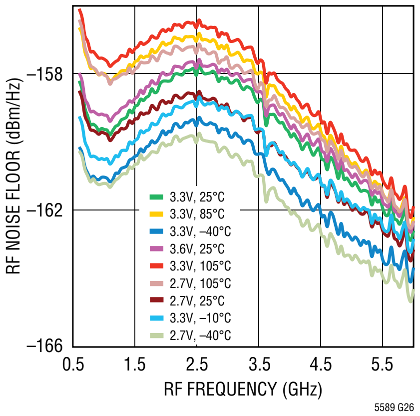
Output IP2 vs RF Frequency and V_{CTRL}



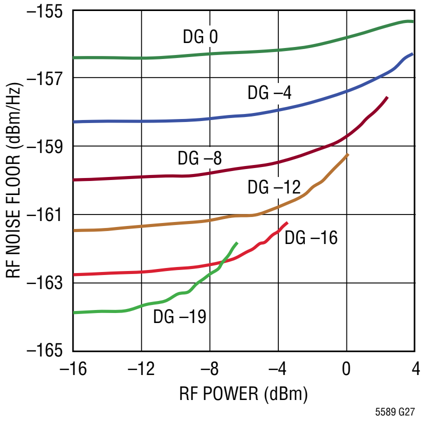
Noise Floor vs RF Frequency and V_{CTRL}



Noise Floor vs RF Frequency



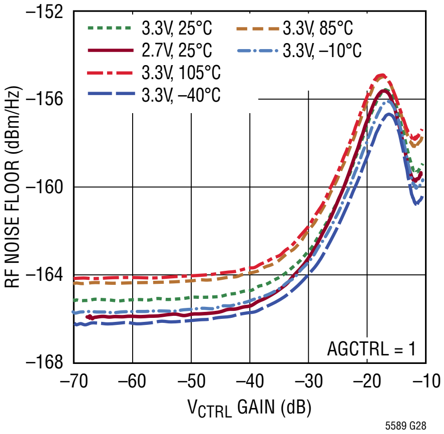
Noise Floor vs RF Power



TYPICAL PERFORMANCE CHARACTERISTICS

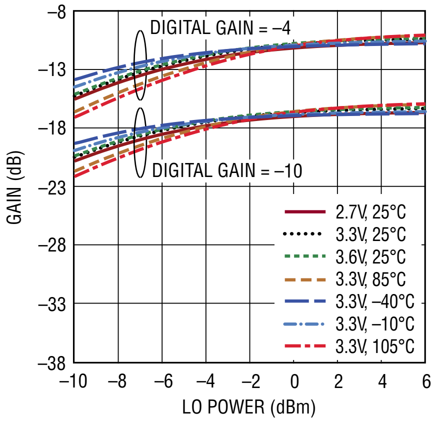
V_{CC} = 3.3V, EN = 3.3V, V_{CTRL} = 3.3V, T_C = 25°C, P_{LO} = 0dBm, f_{LO} = 1.8GHz, BBPI, BBMI, BBPQ, BBMQ common mode DC voltage V_{CMBB} = 1.4V_{DC}, I and Q baseband input signal = 2MHz, 2.1MHz, 1$V_{P-P(DIFF, I or Q)}$, I and Q 90° shifted, lower sideband selection, TEMPUPDT = 0, register 0x00 value according to Table 6, all other registers set to default values, unless otherwise noted. Test circuit is shown in Figure 12.

Noise Floor vs V_{CTRL} Gain



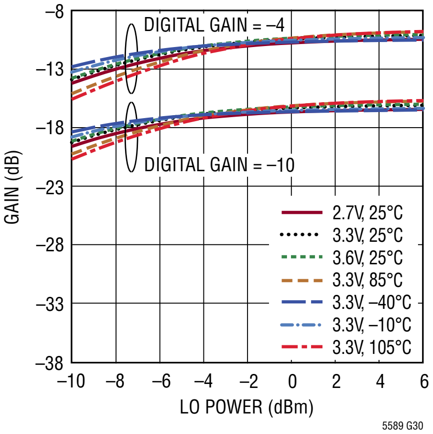
5589 G28

Gain vs LO Power at f_{LO} = 700MHz



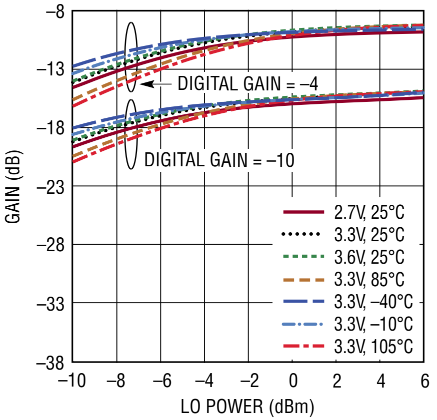
5589 G29

Gain vs LO Power at f_{LO} = 900MHz



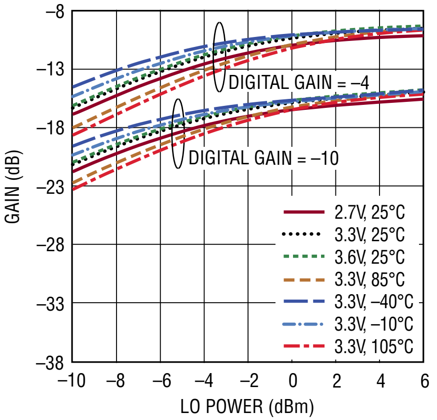
5589 G30

Gain vs LO Power at f_{LO} = 1800MHz



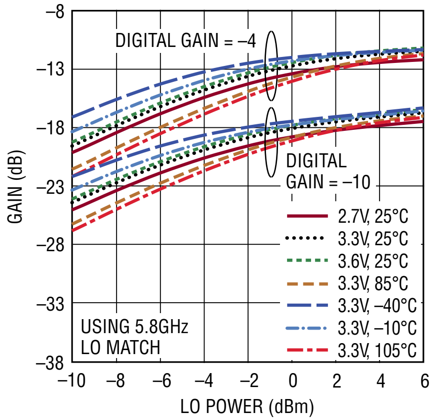
5589 G31

Gain vs LO Power at f_{LO} = 2500MHz



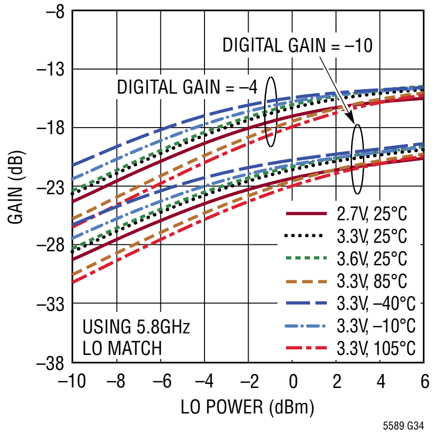
5589 G32

Gain vs LO Power at f_{LO} = 3500MHz



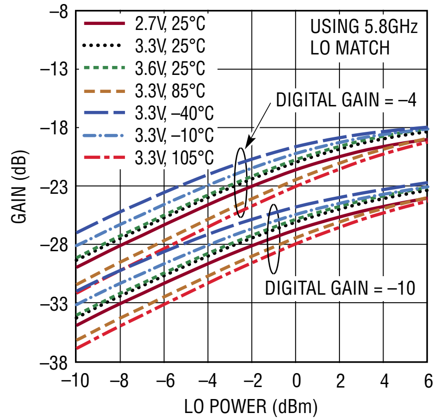
5589 G33

Gain vs LO Power at f_{LO} = 4500MHz



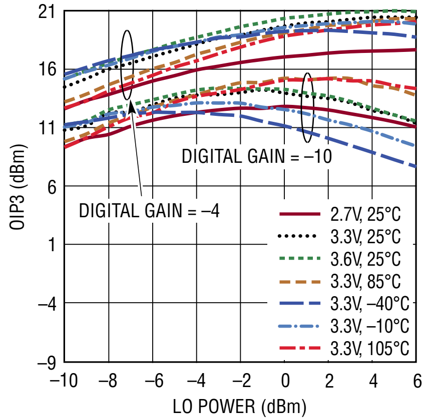
5589 G34

Gain vs LO Power at f_{LO} = 5800MHz



5589 G35

Output IP3 vs LO Power at f_{LO} = 700MHz

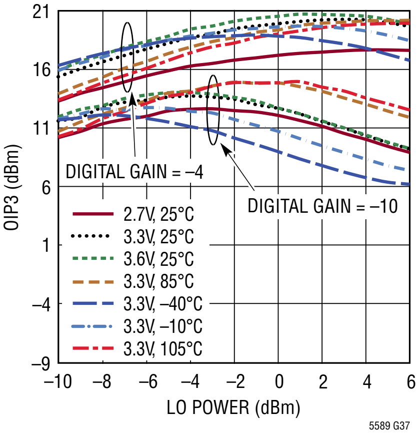


5589 G36

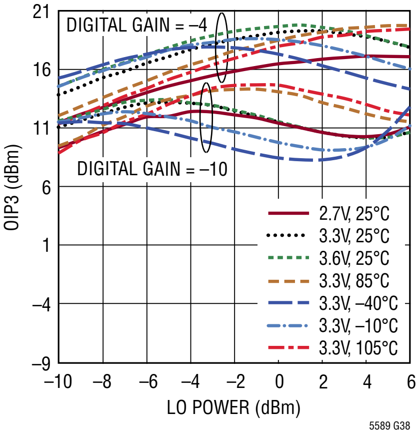
TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 3.3V, EN = 3.3V, V_{CTRL} = 3.3V, T_C = 25°C, P_{LO} = 0dBm, f_{LO} = 1.8GHz, BBPI, BBMI, BBPQ, BBMQ common mode DC voltage V_{CMBB} = 1.4V_{DC}, I and Q baseband input signal = 2MHz, 2.1MHz, 1$V_{P-P(DIFF,\ I\ or\ Q)}$, I and Q 90° shifted, lower sideband selection, TEMPUPDT = 0, register 0x00 value according to Table 6, all other registers set to default values, unless otherwise noted. Test circuit is shown in Figure 12.

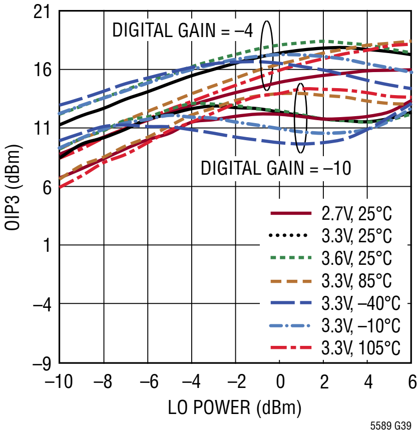
Output IP3 vs LO Power at f_{LO} = 900MHz



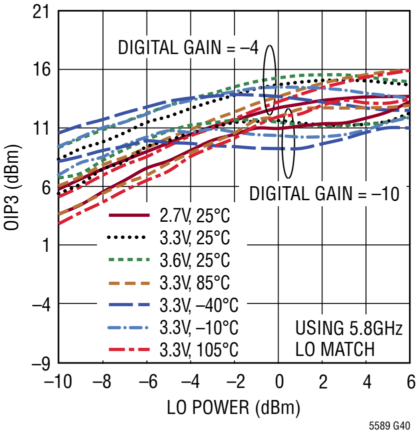
Output IP3 vs LO Power at f_{LO} = 1800MHz



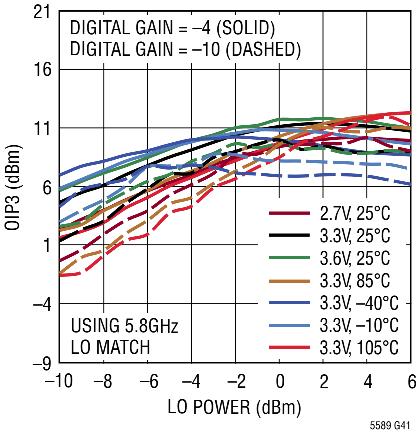
Output IP3 vs LO Power at f_{LO} = 2500MHz



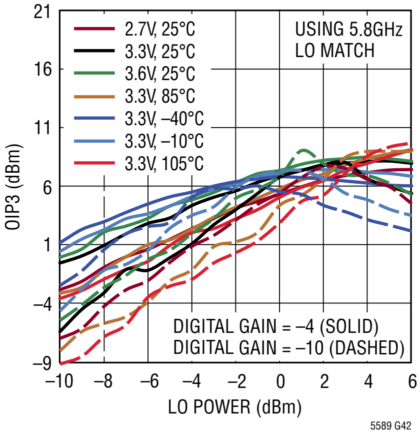
Output IP3 vs LO Power at f_{LO} = 3500MHz



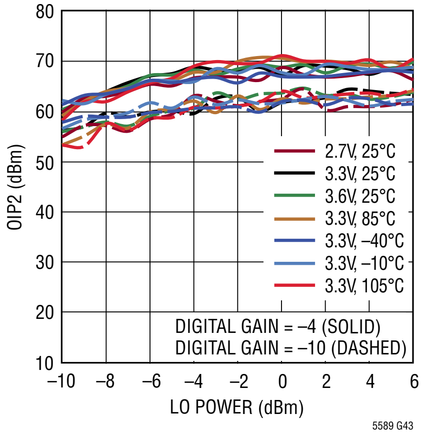
Output IP3 vs LO Power at f_{LO} = 4500MHz



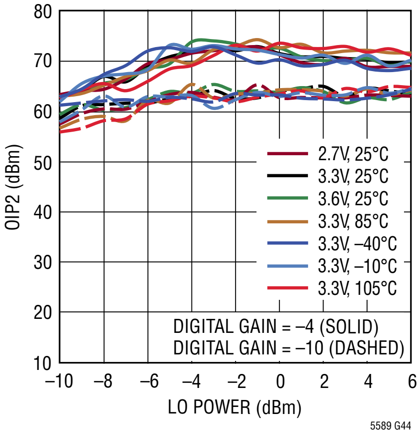
Output IP3 vs LO Power at f_{LO} = 5800MHz



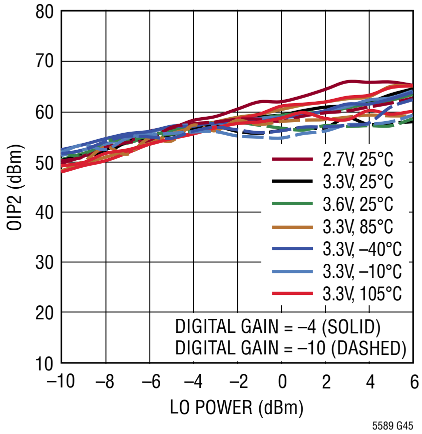
Output IP2 vs LO Power at f_{LO} = 700MHz



Output IP2 vs LO Power at f_{LO} = 900MHz



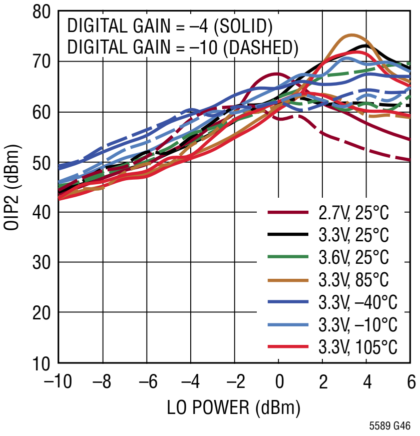
Output IP2 vs LO Power at f_{LO} = 1800MHz



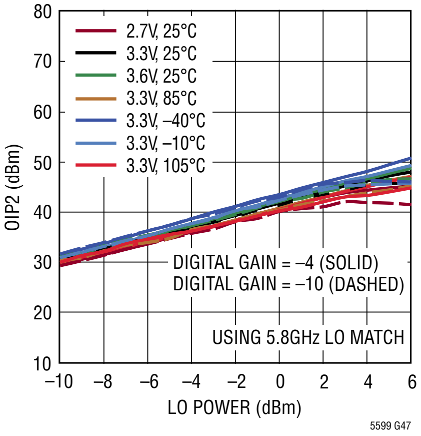
TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 3.3V, EN = 3.3V, V_{CTRL} = 3.3V, T_C = 25°C, P_{LO} = 0dBm, f_{LO} = 1.8GHz, BBPI, BBMI, BBPQ, BBMQ common mode DC voltage V_{CMBB} = 1.4V_{DC}, I and Q baseband input signal = 2MHz, 2.1MHz, 1$V_{P-P(DIFF,\ I\ or\ Q)}$, I and Q 90° shifted, lower sideband selection, TEMPUPDT = 0, register 0x00 value according to Table 6, all other registers set to default values, unless otherwise noted. Test circuit is shown in Figure 12.

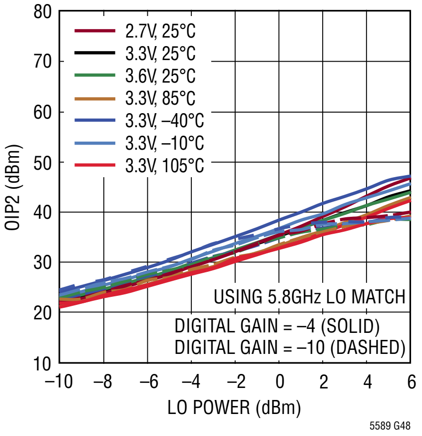
Output IP2 vs LO Power at f_{LO} = 2500MHz



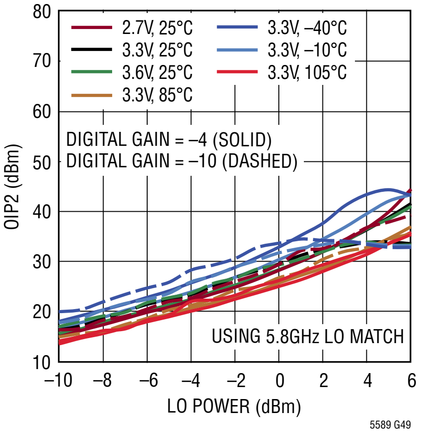
Output IP2 vs LO Power at f_{LO} = 3500MHz



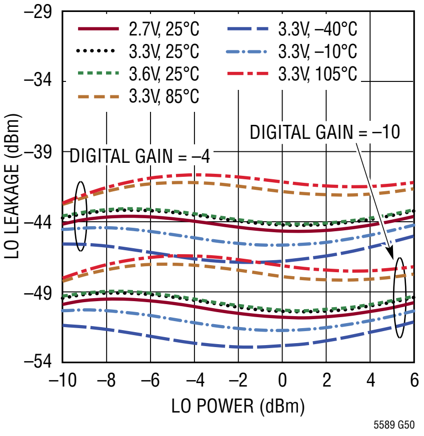
Output IP2 vs LO Power at f_{LO} = 4500MHz



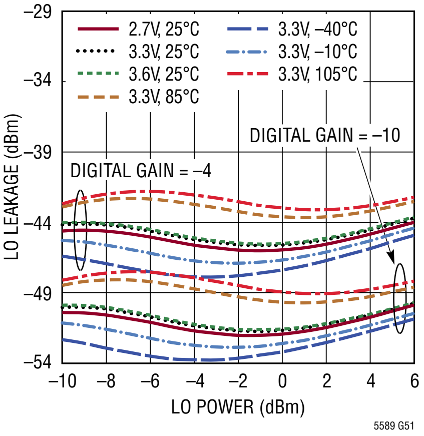
Output IP2 vs LO Power at f_{LO} = 5800MHz



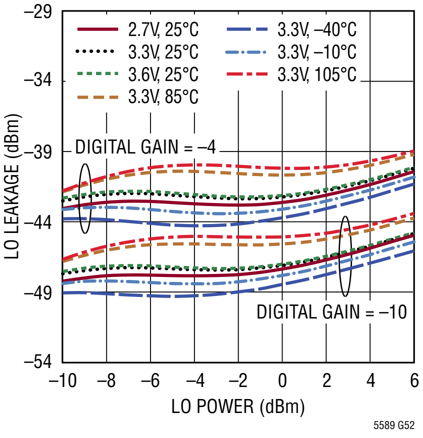
LO Leakage vs LO Power at f_{LO} = 700MHz



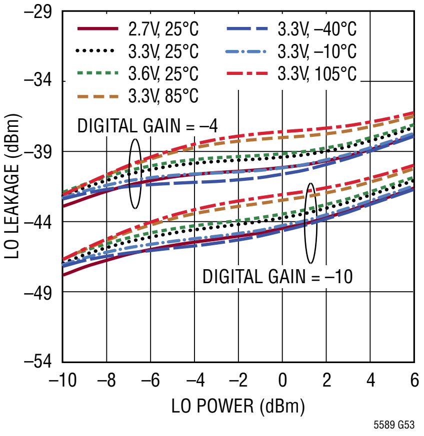
LO Leakage vs LO Power at f_{LO} = 900MHz



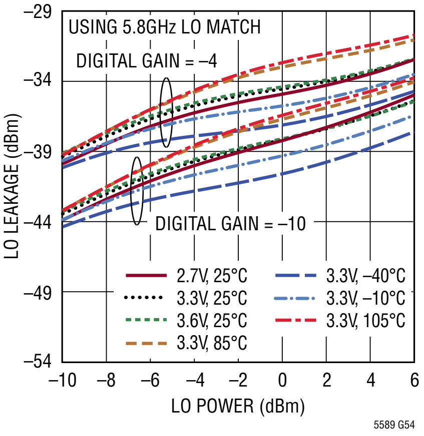
LO Leakage vs LO Power at f_{LO} = 1800MHz



LO Leakage vs LO Power at f_{LO} = 2500MHz



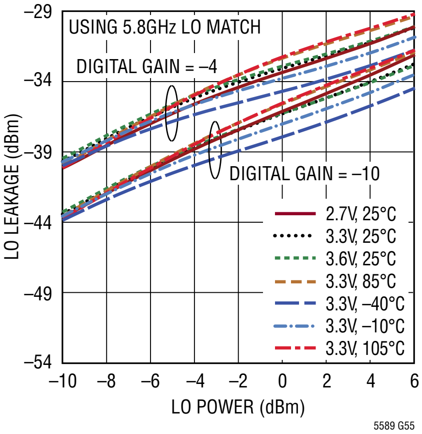
LO Leakage vs LO Power at f_{LO} = 3500MHz



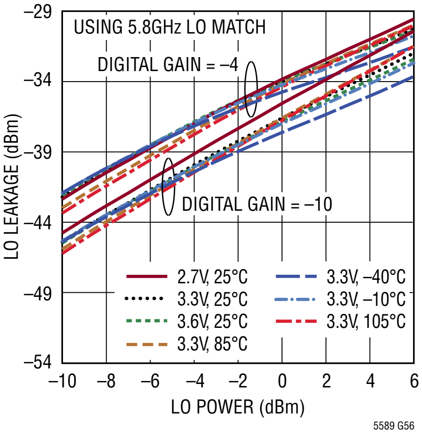
TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 3.3V, EN = 3.3V, V_{CTRL} = 3.3V, T_C = 25°C, P_{LO} = 0dBm, f_{LO} = 1.8GHz, BBPI, BBMI, BBPQ, BBMQ common mode DC voltage V_{CMBB} = 1.4V_{DC}, I and Q baseband input signal = 2MHz, 2.1MHz, 1$V_{P\text{-}P(DIFF,\ I\ or\ Q)}$, I and Q 90° shifted, lower sideband selection, TEMPUPDT = 0, register 0x00 value according to Table 6, all other registers set to default values, unless otherwise noted. Test circuit is shown in Figure 12.

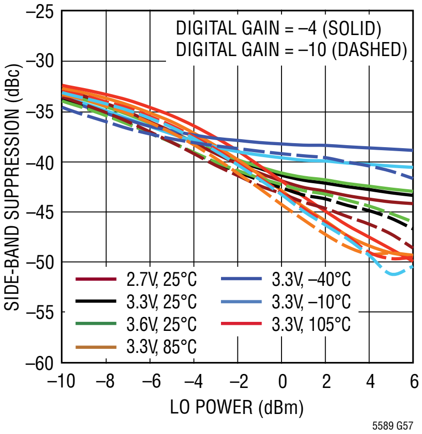
LO Leakage vs LO Power at f_{LO} = 4500MHz



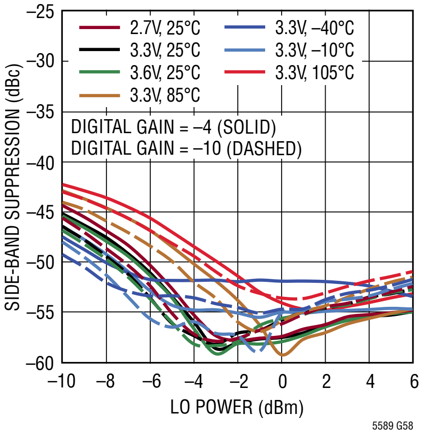
LO Leakage vs LO Power at f_{LO} = 5800MHz



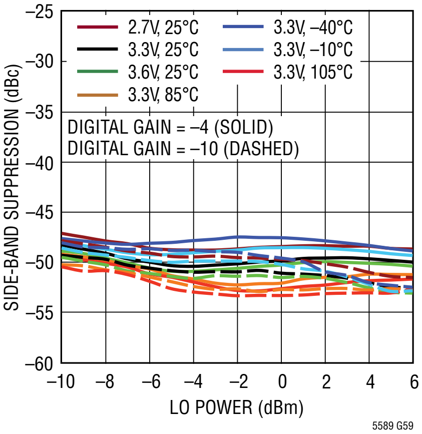
Side-Band Suppression vs LO Power at f_{LO} = 700MHz



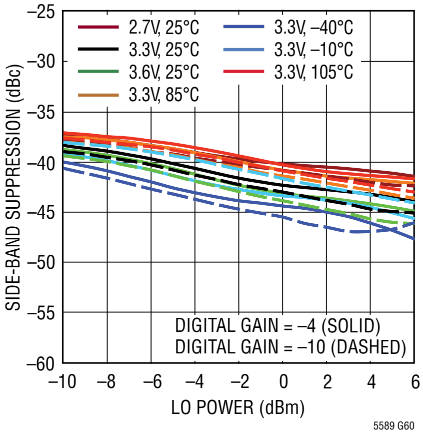
Side-Band Suppression vs LO Power at f_{LO} = 900MHz



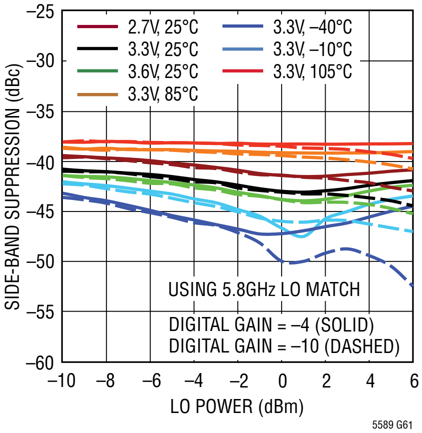
Side-Band Suppression vs LO Power at f_{LO} = 1800MHz



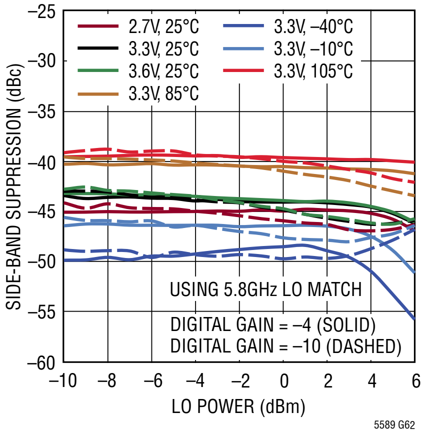
Side-Band Suppression vs LO Power at f_{LO} = 2500MHz



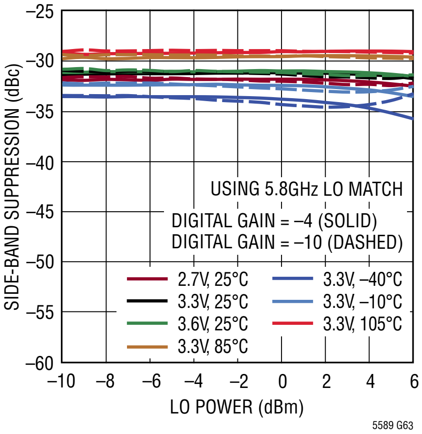
Side-Band Suppression vs LO Power at f_{LO} = 3500MHz



Side-Band Suppression vs LO Power at f_{LO} = 4500MHz

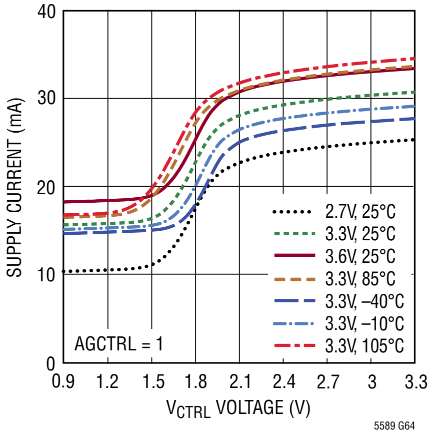


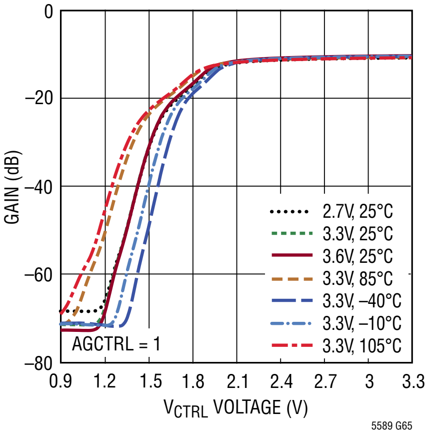
Side-Band Suppression vs LO Power at f_{LO} = 5800MHz

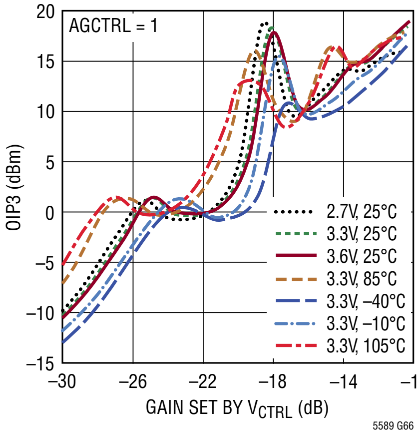


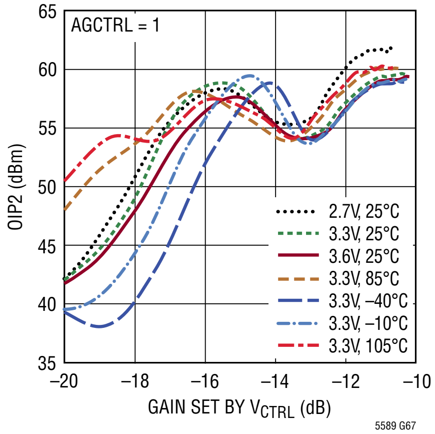
TYPICAL PERFORMANCE CHARACTERISTICS

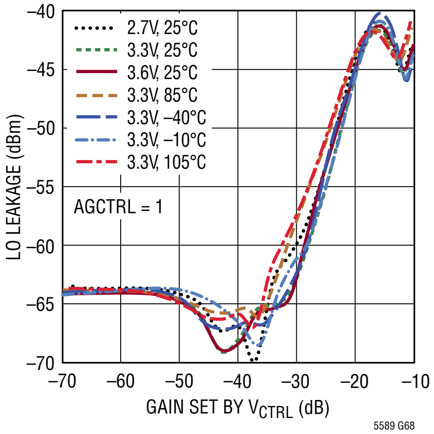
V_{CC} = 3.3V, EN = 3.3V, V_{CTRL} = 3.3V, T_C = 25°C, P_{LO} = 0dBm, f_{LO} = 1.8GHz, BBPI, BBMI, BBPQ, BBMQ common mode DC voltage V_{CMBB} = 1.4V_{DC}, I and Q baseband input signal = 2MHz, 2.1MHz, 1$V_{P-P(DIFF,\ I\ or\ Q)}$, I and Q 90° shifted, lower sideband selection, TEMPUPDT = 0, register 0x00 value according to Table 6, all other registers set to default values, unless otherwise noted. Test circuit is shown in Figure 12.

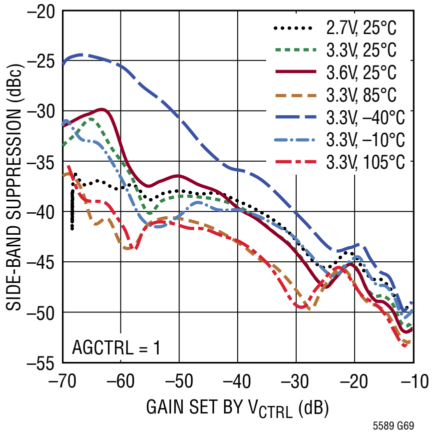

Supply Current vs V_{CTRL} Voltage

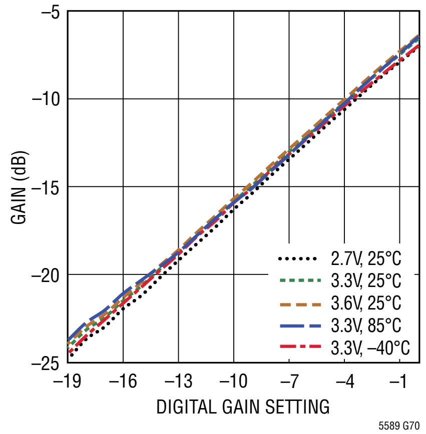

Gain vs V_{CTRL} Voltage

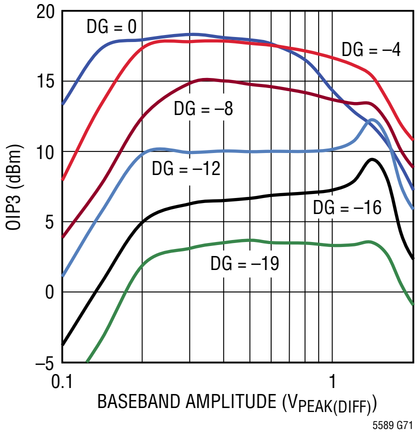

Output IP3 vs V_{CTRL} Gain

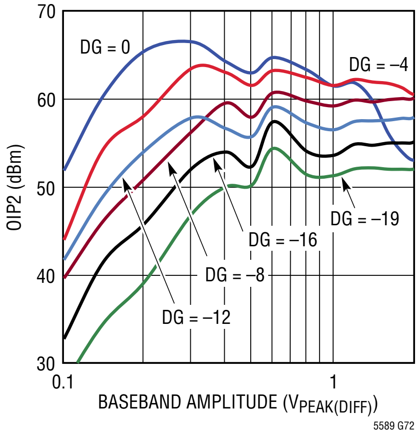

Output IP2 vs V_{CTRL} Gain


LO Leakage vs V_{CTRL} Gain


Side-Band Suppression vs V_{CTRL} Gain


Gain vs Digital Gain Setting

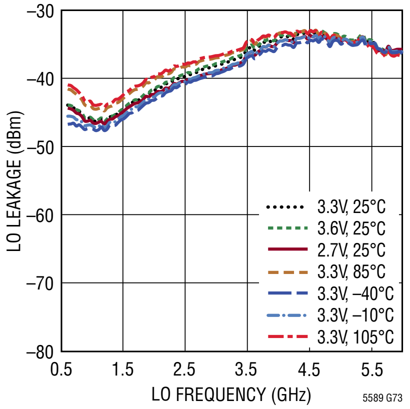

Output IP3 vs Baseband Amplitude


Output IP2 vs Baseband Amplitude

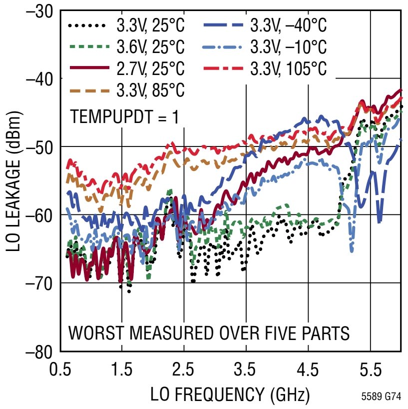
TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 3.3V, EN = 3.3V, V_{CTRL} = 3.3V, T_C = 25°C, P_{LO} = 0dBm, f_{LO} = 1.8GHz, BBPI, BBMI, BBPQ, BBMQ common mode DC voltage V_{CMBB} = 1.4V_{DC}, I and Q baseband input signal = 2MHz, 2.1MHz, 1$V_{P\text{-}P(DIFF,\ I\ or\ Q)}$, I and Q 90° shifted, lower sideband selection, TEMPUPDT = 0, register 0x00 value according to Table 6, all other registers set to default values, unless otherwise noted. Test circuit is shown in Figure 12.

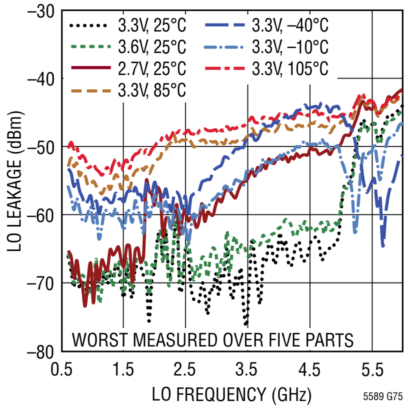
LO Leakage vs LO Frequency for Gain TempComp On



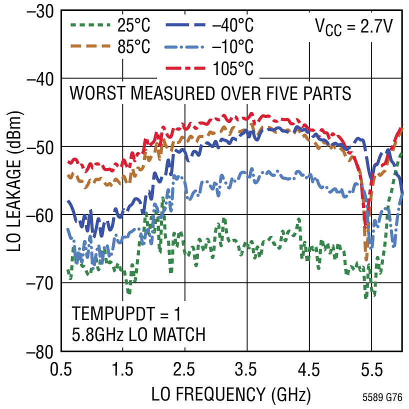
LO Leakage vs LO Frequency After 25°C, 3.3V Calibration Using Reg. 0x02 and 0x03, Gain TempComp Off



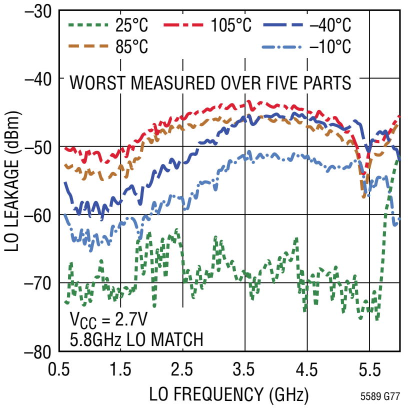
LO Leakage vs LO Frequency After 25°C, 3.3V Calibration Using Reg. 0x02 and 0x03, Gain TempComp On



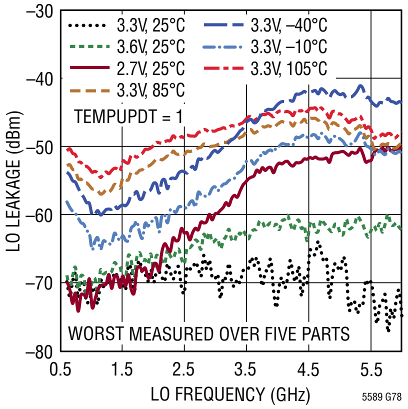
LO Leakage vs LO Frequency After 25°C, 2.7V Calibration Using Reg. 0x02 and 0x03, Gain TempComp Off



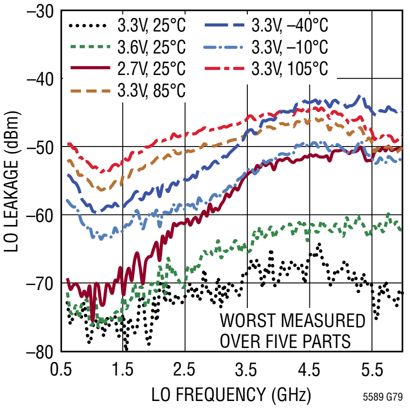
LO Leakage vs LO Frequency After 25°C, 2.7V Calibration Using Reg. 0x02 and 0x03, Gain TempComp On



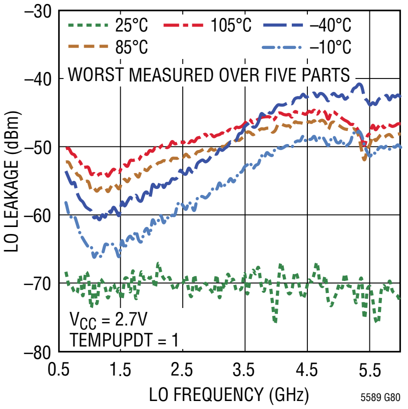
LO Leakage vs LO Frequency After 25°C, 3.3V Calibration Using I and Q Offset, Gain TempComp Off



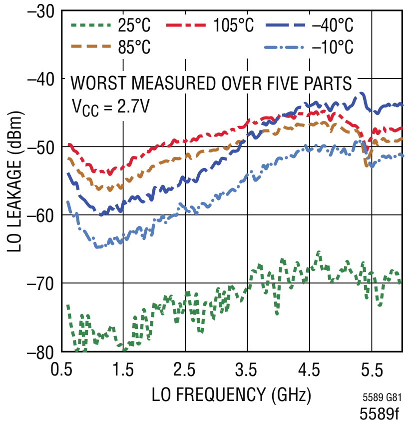
LO Leakage vs LO Frequency After 25°C, 3.3V Calibration Using I and Q Offset, Gain TempComp On



LO Leakage vs LO Frequency After 25°C, 2.7V Calibration Using I and Q Offset, Gain TempComp Off



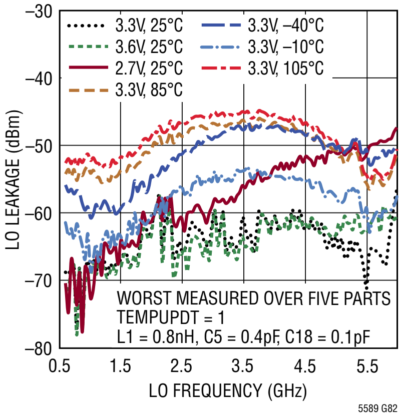
LO Leakage vs LO Frequency After 25°C, 2.7V Calibration Using I and Q Offset, Gain TempComp On



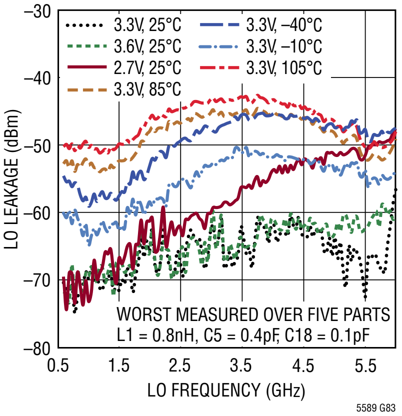
TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 3.3V, EN = 3.3V, V_{CTRL} = 3.3V, T_C = 25°C, P_{LO} = 0dBm, f_{LO} = 1.8GHz, BBPI, BBMI, BBPQ, BBMQ common mode DC voltage V_{CMBB} = 1.4V_{DC}, I and Q baseband input signal = 2MHz, 2.1MHz, 1$V_{P\text{-}P(DIFF,\ I\ or\ Q)}$, I and Q 90° shifted, lower sideband selection, TEMPUPDT = 0, register 0x00 value according to Table 6, all other registers set to default values, unless otherwise noted. Test circuit is shown in Figure 12.

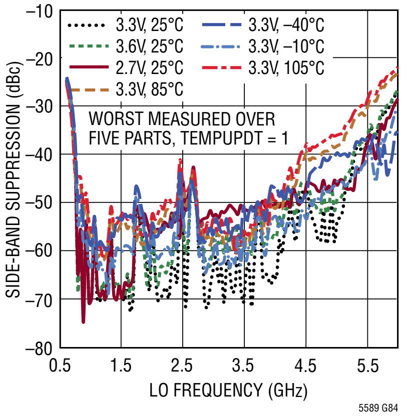
LO Leakage vs LO Frequency After 25°C, 3.3V Calibration with 5.8GHz Match Using Reg. 0x02 and 0x03, Gain TempComp Off



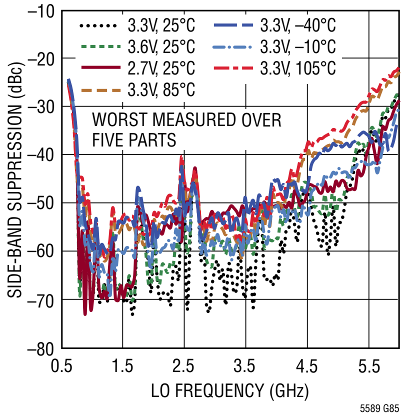
LO Leakage vs LO Frequency After 25°C, 3.3V Calibration with 5.8GHz Match Using Reg. 0x02 and 0x03, Gain TempComp On



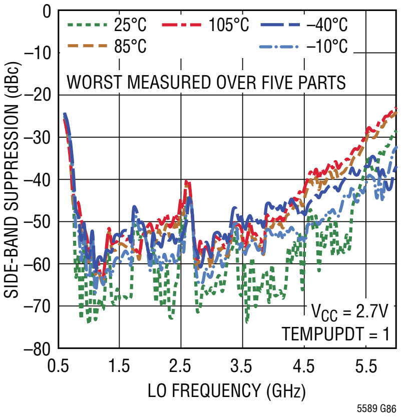
Side-Band Suppression vs LO Frequency After 25°C, 3.3V Calibration, Gain TempComp Off



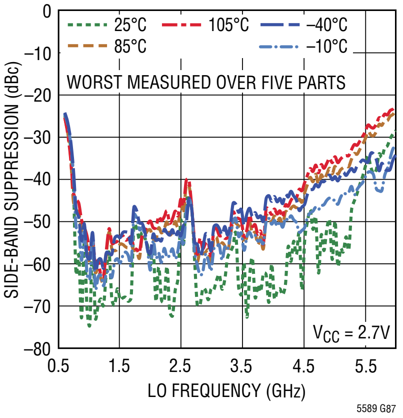
Side-Band Suppression vs LO Frequency After 25°C, 3.3V Calibration, Gain TempComp On



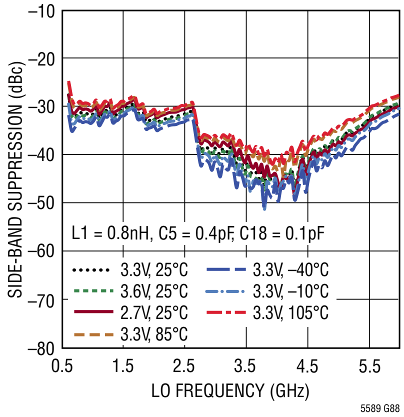
Side-Band Suppression vs LO Frequency After 25°C, 2.7V Calibration, Gain TempComp Off



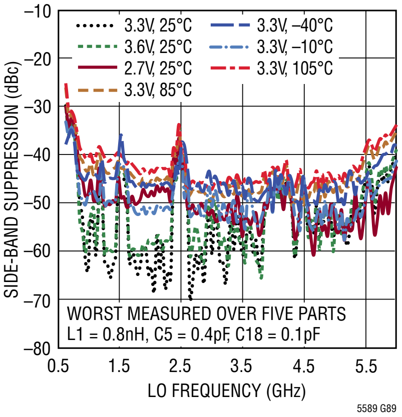
Side-Band Suppression vs LO Frequency After 25°C, 2.7V Calibration, Gain TempComp On



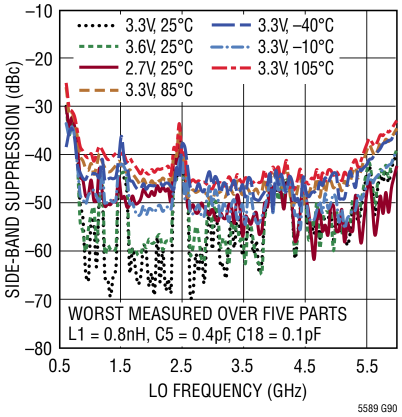
Side-Band Suppression vs LO Frequency Using 5.8GHz Match



Side-Band Suppression vs LO Frequency After 25°C, 3.3V Calibration with 5.8GHz Match Using Reg. 0x02 and 0x03, Gain TempComp Off



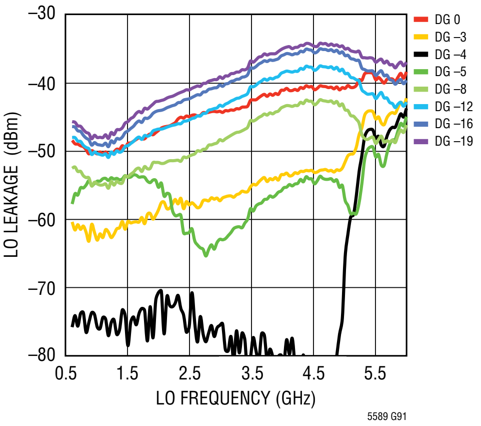
Side-Band Suppression vs LO Frequency After 25°C, 3.3V Calibration with 5.8GHz Match Using Reg. 0x02 and 0x03, Gain TempComp On



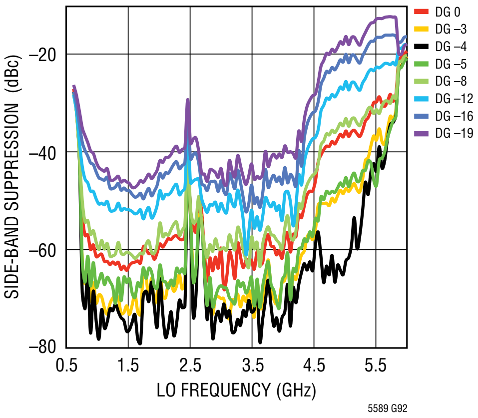
TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 3.3V, EN = 3.3V, V_{CTRL} = 3.3V, T_C = 25°C, P_{LO} = 0dBm, f_{LO} = 1.8GHz, BBPI, BBMI, BBPQ, BBMQ common mode DC voltage V_{CMBB} = 1.4V_{DC}, I and Q baseband input signal = 2MHz, 2.1MHz, 1$V_{P-P(DIFF,\ I\ or\ Q)}$, I and Q 90° shifted, lower sideband selection, TEMPUPDT = 0, register 0x00 value according to Table 6, all other registers set to default values, unless otherwise noted. Test circuit is shown in Figure 12.

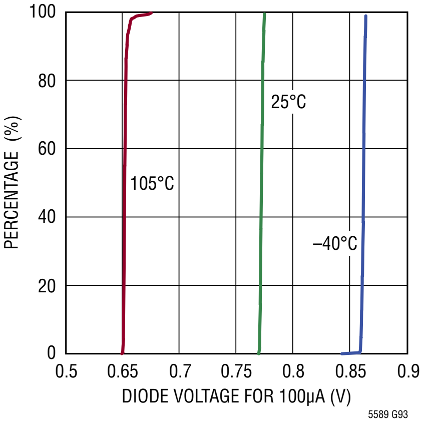
LO Leakage vs LO Frequency and Digital Gain Setting After Calibration Using Reg. 0x02 and 0x03 at Digital Gain = –4



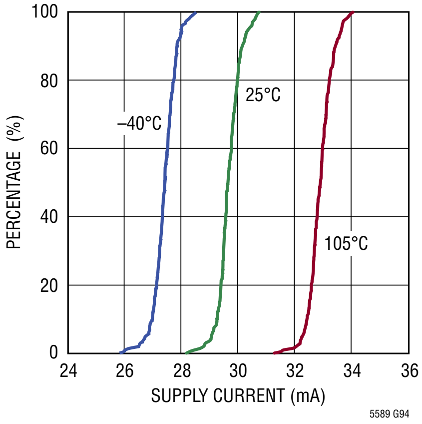
Side-Band Suppression vs LO Frequency and Digital Gain Setting After Calibration at Digital Gain = –4



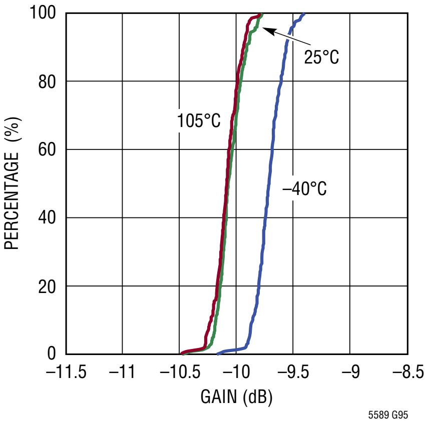
Temperature Sensing Diode Voltage Cumulative Distribution



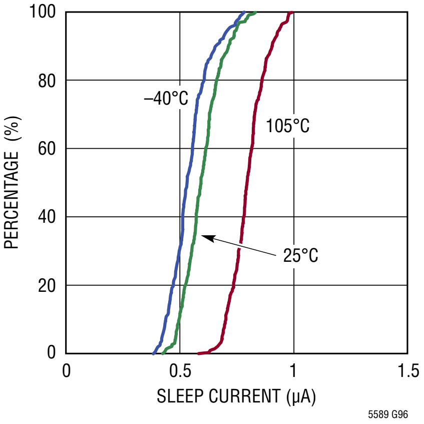
Supply Current Cumulative Distribution



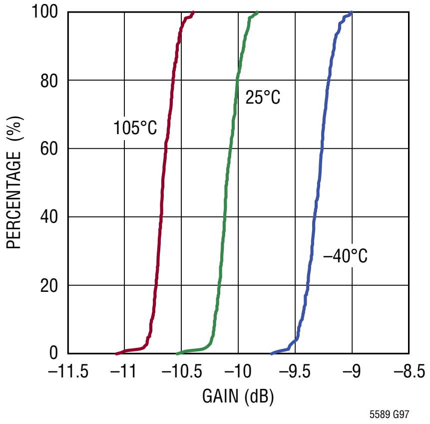
Gain Cumulative Distribution for Gain TempComp On



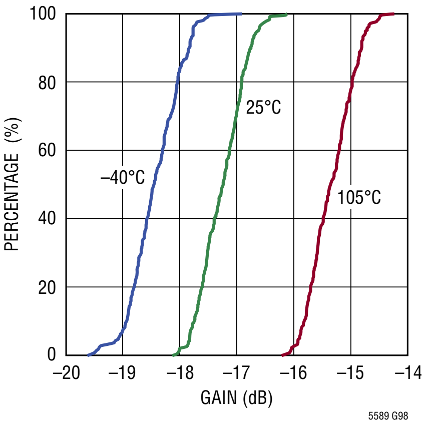
Sleep Current Cumulative Distribution



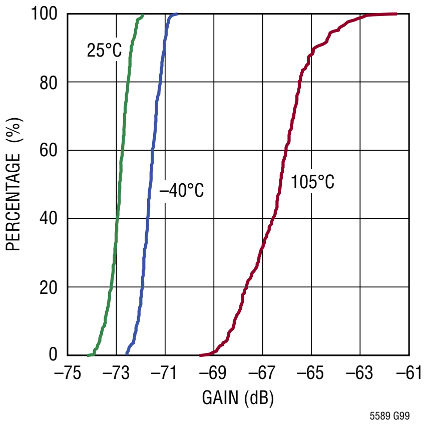
Gain Cumulative Distribution for Gain TempComp Off



Gain Cumulative Distribution for V_{CTRL} = 1.75V



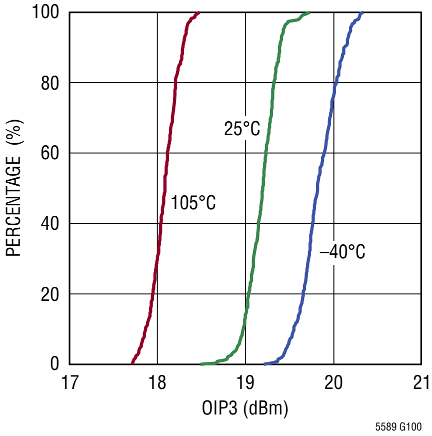
Gain Cumulative Distribution for V_{CTRL} = 1V



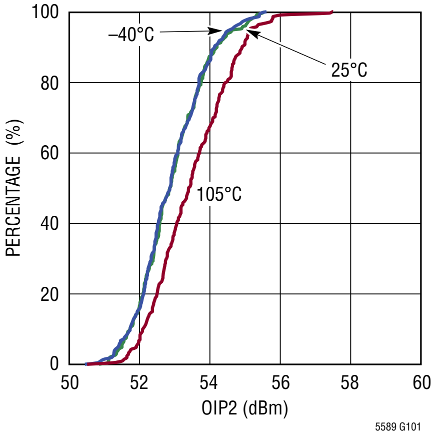
TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 3.3V, EN = 3.3V, V_{CTRL} = 3.3V, T_C = 25°C, P_{LO} = 0dBm, f_{LO} = 1.8GHz, BBPI, BBMI, BBPQ, BBMQ common mode DC voltage V_{CMBB} = 1.4V_{DC}, I and Q baseband input signal = 2MHz, 2.1MHz, 1$V_{P-P(DIFF, I or Q)}$, I and Q 90° shifted, lower sideband selection, TEMPUPDT = 0, register 0x00 value according to Table 6, all other registers set to default values, unless otherwise noted. Test circuit is shown in Figure 12.

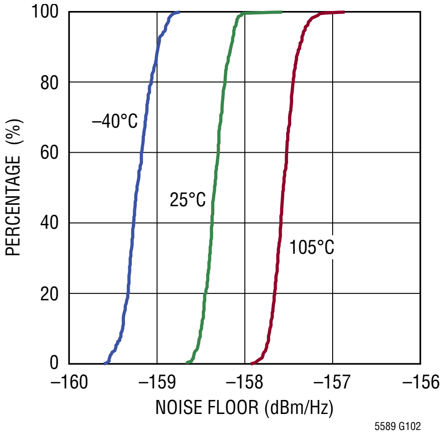
Output IP3 Cumulative Distribution



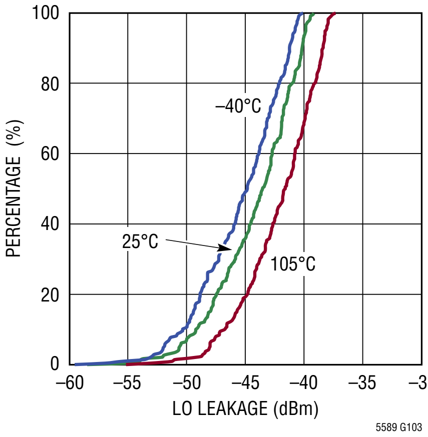
Output IP2 Cumulative Distribution



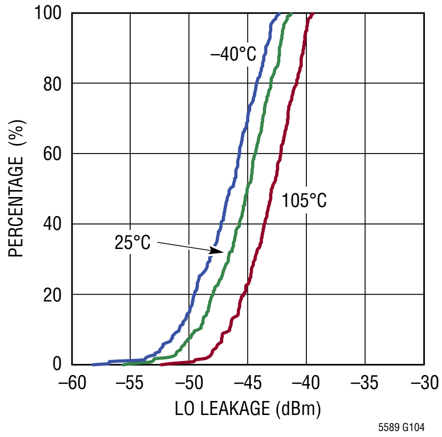
Output Noise Floor Cumulative Distribution



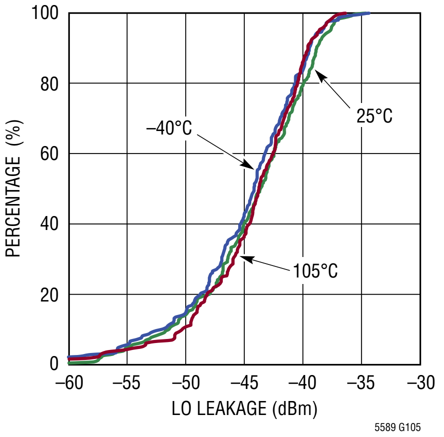
LO Leakage Cumulative Distribution for Floating Baseband Pins



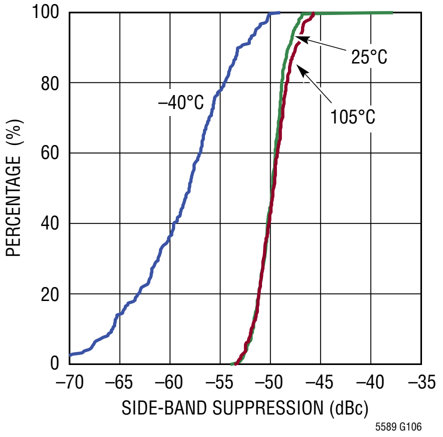
LO Leakage Cumulative Distribution



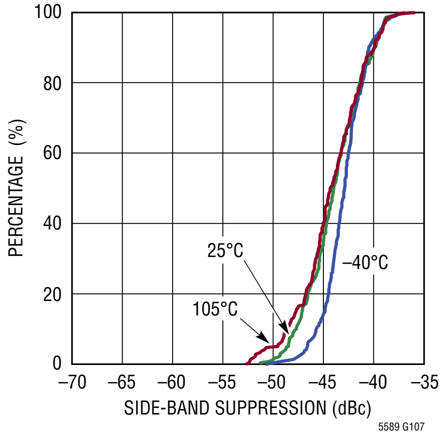
LO Leakage Cumulative Distribution for V_{CTRL} = 1.75V



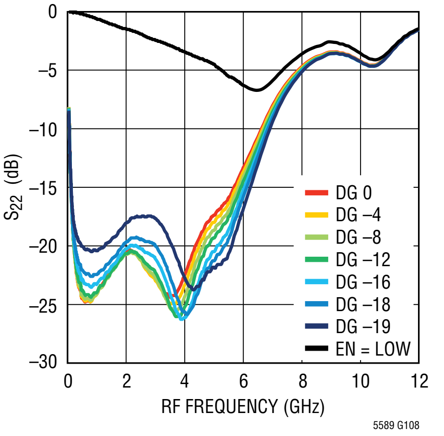
Side-Band Suppression Cumulative Distribution



Side-Band Suppression Cumulative Distribution for V_{CTRL} = 1.75V



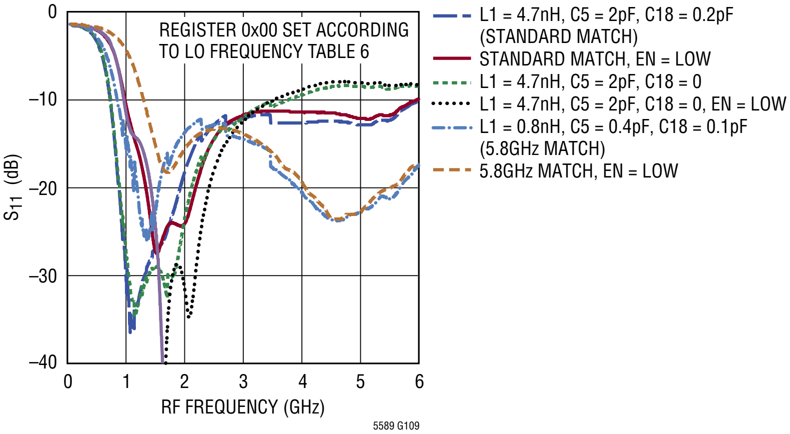
RF Return Loss



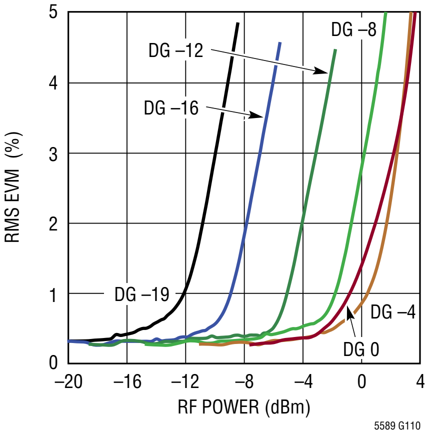
TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 3.3V, EN = 3.3V, V_{CTRL} = 3.3V, T_C = 25°C, P_{LO} = 0dBm, f_{LO} = 1.8GHz, BBPI, BBMI, BBPQ, BBMQ common mode DC voltage V_{CMBB} = 1.4V_{DC}, I and Q baseband input signal = 2MHz, 2.1MHz, 1$V_{P\text{-}P(DIFF,\ I\ or\ Q)}$, I and Q 90° shifted, lower sideband selection, TEMPUPDT = 0, register 0x00 value according to Table 6, all other registers set to default values, unless otherwise noted. Test circuit is shown in Figure 12.

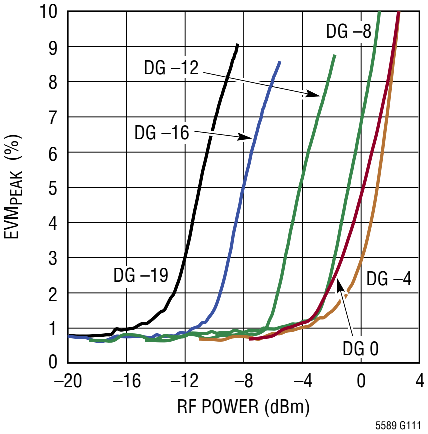
LO Return Loss



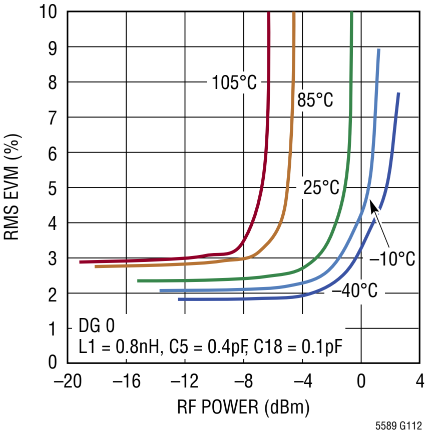
RMS EVM vs RF Output Power at f_{LO} = 2.17GHz with 1Ms/s 16-QAM Signal



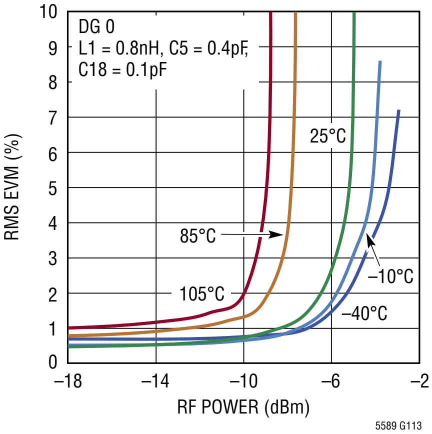
Peak EVM vs RF Output Power at f_{LO} = 2.17GHz with 1Ms/s 16-QAM Signal



RMS EVM vs RF Output Power at f_{LO} = 5.8GHz with 1Ms/s 16-QAM Signal



RMS EVM vs RF Output Power at f_{LO} = 5.8GHz with 1Ms/s 16-QAM Signal After 25°C, 3.3V Calibration



PIN FUNCTIONS

V_{CTRL} (Pin 1): Variable Gain Control Input. This analog control pin sets the gain. Write a "1" to bit 6 in register 0x01 (AGCTRL = 1) to activate this pin, resulting in about 2.5mA current draw from a positive supply. Typical V_{CTRL} voltage range is 0.9V to 3.3V. Gain transfer function is not linear-in-dB. Tie to V_{CC} when not used.

GND (Pins 2, 5, 12, 13, 14, 15, 17, 18, Exposed Pad 25): Ground. All these pins are connected together internally. For best RF performance all ground pins should be connected to RF ground.

LOL, LOC (Pins 3, 4): LO Inputs. This is not a differential input. Both pins are 50Ω inputs. An LC diplexer is recommended to be used at these pins (see Figure 12). AC-coupling capacitors are required at these pins if the applied DC level is higher than ±50mV.

TTCK (Pin 6): Temperature Update. When the TTCK temperature update mode is selected in register 0x01 (bit 7 = High, TEMPUPDT = 1), the temperature readout and digital gain compensation vs temperature can be updated through a logic low to logic high transition at this pin. Do not float.

TEMP (Pin 7): Temperature Sensing Diode. This pin is connected to the anode of a diode that may be used to measure the die temperature, by forcing a current and measuring the voltage. This diode is not part of the on-chip thermometer.

BBPI, BBMI (Pins 8, 9): Baseband Inputs of the I-Channel. The input impedance of each input is about 1kΩ. It should be externally biased to a 1.4V common mode level, or AC-coupled. Do not apply common mode voltage beyond $2V_{DC}$.

BBPQ, BBMQ (Pins 10, 11): Baseband Inputs of the Q-Channel. The input impedance of each input is about 1kΩ. It should be externally biased to a 1.4V common mode level, or AC-coupled. Do not apply common mode voltage beyond $2V_{DC}$. Float if Q-channel is disabled.

RF (Pin 16): RF Output. The output impedance at RF frequencies is 50Ω. Its DC output voltage is about 1.7V if enabled. An AC-coupling capacitor should be used at this pin with a recommended value of 100pF.

CSB (Pin 19): Serial Port Chip Select. This CMOS input initiates a serial port transaction when driven low, ending the transaction when driven back high. Do not float.

SCLK (Pin 20): Serial Port Clock. This CMOS input clocks serial port input data on its rising edge. Do not float.

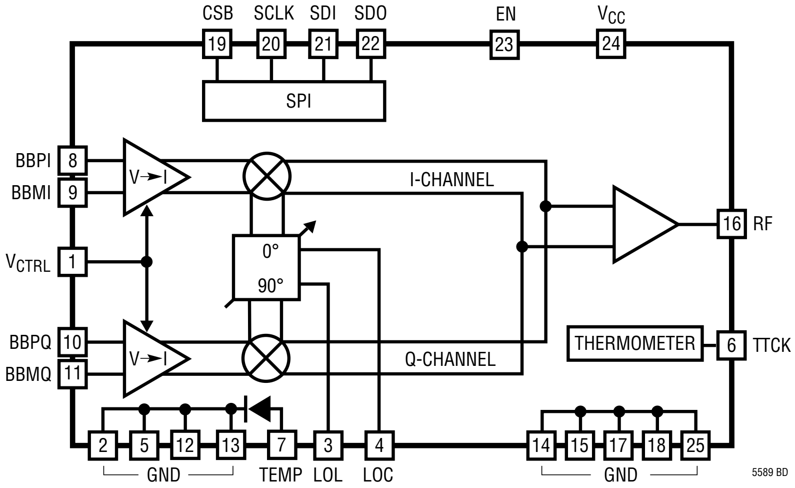
SDI (Pin 21): Serial Port Data Input. The serial port uses this CMOS input for data. Do not float.

SDO (Pin 22): Serial Port Data Output. This NMOS output presents data from the serial port during a read transaction. Connect this pin to the digital supply voltage through a pull-up resistor of sufficiently large value, to ensure that the current does not exceed 10mA when pulled low.

EN (Pin 23): Enable Pin. The chip is completely turned on when a logic high voltage is applied to this pin, and completely turned off for a logic low voltage. Do not float.

V_{CC} (Pin 24): Power Supply. It is recommended to use 1nF and 4.7µF capacitors for decoupling to ground on this pin.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

The LTC5589 consists of I and Q input differential voltage-to-current converters, I and Q upconverting mixers, an RF output buffer and an LO quadrature phase generator. An SPI bus addresses nine control registers, enabling optimization of side-band suppression, LO leakage, and adjustment of the modulator gain. See Table 1 for a summary of the writable registers and their default values. A full map of all the registers in the LTC5589 is listed in Table 8 and Table 9 in the Appendix.

Table 1. SPI Writable Registers and Default Register Values.

ADDRESS	DEFAULT VALUE	SETTING	REGISTER FUNCTION
0x00	0x3E	2.56GHz	LO Frequency Tuning
0x01	0x84	DG = –4	Gain
0x02	0x80	0mV	Offset I-Channel
0x03	0x80	0mV	Offset Q-Channel
0x04	0x80	0dB	I/Q Gain Ratio
0x05	0x10	0°	I/Q Phase Balance
0x06	0x50	OFF	LO Port Matching Override
0x07	0x06	OFF	Temperature Correction Override
0x08	0x00	NORMAL	Operating Mode

Without using the SPI the registers will use the default values which may not result in the optimum side-band suppression (SB). For example: for LO frequency from about 2.44GHz to about 2.72GHz, the SB is about –40dBc; from 1.7GHz to 2.44GHz and 2.72GHz to 2.93GHz it falls to about –35dBc.

Aside of powering up the LTC5589, the register values can be reset to the default values by setting SRESET = 1 (bit 3, register 0x08). After about 50ns SRESET is automatically set back to 0.

External I and Q baseband signals are applied to the differential baseband input pins: BBPI, BBMI and BBPQ, BBMQ. These voltage signals are converted to currents and translated to RF frequency by means of double-balanced upconverting mixers. The mixer outputs are combined at the inputs of the RF output buffer, which also transforms the output impedance to 50Ω. The center frequency of the resulting RF signal is equal to the LO signal frequency. The LO inputs drive a phase shifter which splits the LO signal into in-phase and quadrature signals which drive the upconverting mixers. In most applications, the LOL input is driven by the LO source via a 4.7nH inductor, while the LOC input is driven by the LO source via a 2pF capacitor. This inductor and capacitor form a diplexer circuit tuned to 1.4GHz. The RF output is single-ended and internally 50Ω matched across a wide RF frequency range from 55MHz to 6.6GHz with better than 10dB return loss using C4 = 100pF and C17 = 0.2pF. See Figure 12.

Baseband Interface

The baseband inputs (BBPI, BBMI, BBPQ, BBMQ) present a differential input impedance of about 1.8kΩ, as depicted in Figure 1. The baseband bandwidth depends on the source impedance and the frequency setting (register 0x00). It is recommended to compensate the baseband input impedance in the baseband lowpass filter design in order to achieve best gain flatness vs baseband frequency. The S-parameters for (each of) the baseband inputs are given in Table 2 for various LO frequency and gain settings.

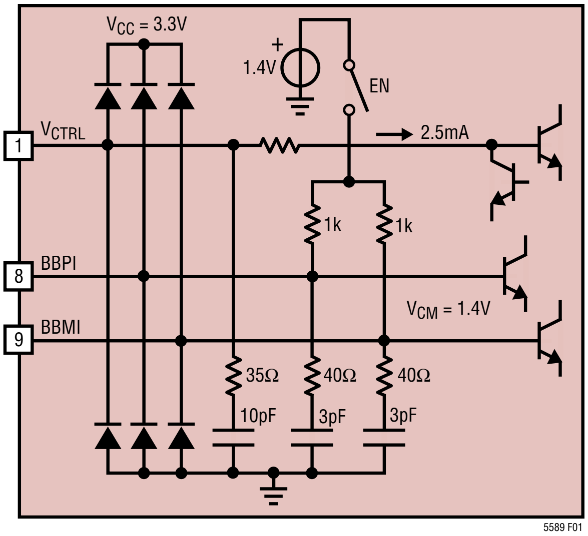


Figure 1. Simplified Circuit Schematic of the Base Band Input Interface (Only One Channel Is Shown).

Table 2. Differential Baseband (BB) Input Impedance vs Frequency for EN = High and V_{CMBB} = 1.4V

BB FREQUENCY (MHz)	INPUT IMPEDANCE (Ω)		REFL COEFFICIENT	
	REAL*	IMAG* (CAP)	MAG	ANGLE(°)
LO FREQUENCY = 0.8GHz (REG. 0x00 = 0x70), DIGITAL GAIN = –4dB				
1	1.84k	–12.8k (12pF)	0.897	–0.9
10	1.76k	–1.4k (11.3pF)	0.893	–8.2
20	1.55k	–705 (11.2pF)	0.881	–16
40	1.08k	–360(11pF)	0.841	–31
100	368	–157 (9.8pF)	0.680	–68
LO FREQUENCY = 1.8GHz (REG. 0x00 = 0x4B), DIGITAL GAIN = –4dB				
1	1.84k	–16.8k (9.2pF)	0.897	–0.7
10	1.79k	–1.74k (9.1pF)	0.895	–6.6
20	1.65k	–876 (9pF)	0.887	–13
40	1.27	–444 (8.9pF)	0.860	–26
100	501	–186 (8.3pF)	0.733	–58
200	204	–113 (6.9pF)	0.591	–91
LO FREQUENCY = 2.5GHz (REG. 0x00 = 0x3F), DIGITAL GAIN = –4dB				
1	1.84k	–17.7k (8.7pF)	0.897	–0.6
10	1.8k	–1.84k (8.6pF)	0.895	–6.2
20	1.67k	–924 (8.5pF)	0.888	–12
40	1.31k	–468 (8.5pF)	0.864	–24
100	539	–194 (7.9pF)	0.745	–56
200	219	–116 (6.7pF)	0.602	–89
400	100	–81 (4.8pF)	0.524	–122
LO FREQUENCY = 3.8GHz (REG. 0x00 = 0x2B), DIGITAL GAIN = –4dB				
1	1.84k	–18.8k (8.2pF)	0.897	–0.6
10	1.8k	–1.96k (8.1pF)	0.895	–5.9
20	1.69k	–985 (8pF)	0.889	–12
40	1.36k	–499 (7.9pF)	0.868	–23
100	585	–206 (7.5pF)	0.758	–53
200	238	–120 (6.4pF)	0.616	–85
400	106	–83 (4.7pF)	0.528	–119
LO FREQUENCY = 5.8GHz (REG. 0x00 = 0x1A), DIGITAL GAIN = –4dB				
1	1.84k	–19.6k (7.8pF)	0.897	–0.6
10	1.81k	–2k (7.8pF)	0.895	–5.7
20	1.69k	–1.02 (7.7pF)	0.890	–11
40	1.38k	–516 (7.7pF)	0.869	–22
100	611	–212 (7.2pF)	0.765	–51
200	250	–123 (6.3pF)	0.623	–84
400	110	–84 (4.6pF)	0.530	–118
LO FREQUENCY = 1.8GHz (REG. 0x00 = 0x4B), DIGITAL GAIN = 0dB				
1	1.78k	–16.9k (9.1pF)	0.902	–0.7
10	1.73k	–1.75k (9pF)	0.891	–6.6
20	1.6k	–878 (9pF)	0.884	–13
40	1.24k	–445 (8.9pF)	0.857	–25
100	497	–186 (8.3pF)	0.732	–58
200	203	–113 (6.8pF)	0.590	–91
LO FREQUENCY = 1.8GHz (REG. 0x00 = 0x4B), DIGITAL GAIN = –19dB				
1	1.94k	–16.7k (9.2pF)	0.893	–0.7
10	1.88k	–1.74k (9.1pF)	0.899	–6.6
20	1.72k	–874 (9pF)	0.892	–13
40	1.31k	–443 (8.9pF)	0.865	–26
100	507	–185 (8.3pF)	0.736	–58
200	205	–112 (6.9pF)	0.592	–91
EN = Low (Chip Disabled)				
1	1.96k	–20.1k (7.6pF)	0.903	–0.6
10	1.92k	–2.08k (7.6pF)	0.901	–5.5
20	1.8k	–1.05k (7.5pF)	0.895	–11
40	1.46k	–530 (8.9pF)	0.876	–21
100	639	–218 (8.3pF)	0.772	–50
200	260	–126 (6.1pF)	0.629	–82

*Parallel Equivalent

In Table 3 the common-mode S-parameters of the differential baseband inputs are given. The circuit is optimized for a common mode voltage of 1.4V which can be internally or externally applied. In case of AC-coupling to the baseband pins (1.4V internally generated bias) make sure that the high pass filter corner is not affecting the low frequency components of the baseband signal. Even a small error for low baseband frequencies can result in degraded EVM.

The baseband input offset voltage depends on the source resistance. In case of AC-coupling the 1 sigma offset is about 1.7mV, resulting in about –43.7dBm LO leakage. For shorted baseband pins (0Ω source resistance), the LO leakage improves to about –45.6dBm. In case of AC-coupling the LO leakage can be reduced by connecting a resistor in parallel with the baseband inputs, thus

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Table 3. Common-Mode Baseband (BB) Input Impedance vs Frequency for EN = High and V_{CMBB} = 1.4V

BB FREQUENCY (MHz)	INPUT IMPEDANCE (Ω)		REFL COEFFICIENT	
	REAL*	IMAG* (CAP)	MAG	ANGLE(°)
LO FREQUENCY = 0.8GHz (REG. 0x00 = 0x70), DIGITAL GAIN = –4dB				
1	536	–5.82k (25pF)	0.911	–0.5
10	534	–605 (24.9pF)	0.911	–4.7
20	541	–301 (25pF)	0.912	–9.5
40	447	–145 (26pF)	0.897	–20
100	165	–61 (24.2pF)	0.771	–46
LO FREQUENCY = 1.8GHz (REG. 0x00 = 0x4B), DIGITAL GAIN = –4dB				
1	536	–8.71k (16.8pF)	0.911	–0.3
10	547	–907 (16.6pF)	0.913	–3.2
20	599	–445 (16.9pF)	0.920	–6.4
40	620	–203 (18.7pF)	0.924	–14
100	322	–78 (18.9pF)	0.869	–36
200	135	–41 (18.1pF)	0.764	–64
LO FREQUENCY = 2.5GHz (REG. 0x00 = 0x3F), DIGITAL GAIN = –4dB				
1	537	–9.76k (15pF)	0.911	–0.3
10	550	–1.02k (14.8pF)	0.913	–2.8
20	609	–496 (15.2pF)	0.921	–5.8
40	654	–223 (17pF)	0.927	–13
100	380	–84 (17.4pF)	0.886	–33
200	167	–43 (17pF)	0.799	–61
400	55	–22 (16.6pF)	0.697	–102
LO FREQUENCY = 3.8GHz (REG. 0x00 = 0x2B), DIGITAL GAIN = -4dB				
1	537	–11.2k (13pF)	0.911	–0.3
10	551	–1.17k (12.8pF)	0.913	–2.4
20	617	–571 (13.1pF)	0.922	–5
40	685	–252 (15pF)	0.930	–11.3
100	449	–94 (15.6pF)	0.901	–30
200	217	–48 (15.5pF)	0.835	–56
400	71	–24 (15.7pF)	0.722	–97
LO FREQUENCY = 5.8GHz (REG. 0x00 = 0x1A), DIGITAL GAIN = –4dB				
1	537	–12.3k (11.9pF)	0.911	–0.2
10	552	–1.28k (11.8pF)	0.913	–2.2
20	620	–620 (12.2pF)	0.923	–4.6
40	698	–271 (14pF)	0.931	–11
100	486	–101 (14.6pF)	0.908	–28
200	249	–51 (14.6pF)	0.851	–53
400	83	–25 (14.9pF)	0.745	–93
LO FREQUENCY = 1.8GHz (REG. 0x00 = 0x4B), DIGITAL GAIN = 0dB				
1	515	–8.6k (17pF)	0.907	–0.3
10	523	–895 (16.8pF)	0.909	–3.2
20	564	–443 (17pF)	0.915	–6.5
40	587	–203 (18.7pF)	0.919	–14
100	313	–78 (18.9pF)	0.865	–36
200	133	–41 (18.1pF)	0.762	–64
LO FREQUENCY = 1.8GHz (REG. 0x00 = 0x4B), DIGITAL GAIN = –19dB				
1	569	–8.94k (16.4pF)	0.916	–0.3
10	587	–929 (16.2pF)	0.918	–3.1
20	663	–447 (16.8pF)	0.928	–6.4
40	675	–203 (18.7pF)	0.930	–14
100	337	–78 (18.9pF)	0.874	–36
200	138	–41 (18pF)	0.768	–64
EN = Low (Chip Disabled)				
1	1.01k	–10.6k (14.2pF)	0.952	–0.3
10	1.07k	–1.08k (13.9pF)	0.952	–2.6
20	975	–546 (13.8pF)	0.950	–5.2
40	898	–275 (13.8pF)	0.946	–10
100	612	–108 (13.6pF)	0.925	–26
200	314	–54 (13.6pF)	0.877	–50

*Parallel Equivalent

lowering baseband input impedance and offset. Further, the low combined baseband input leakage current of 1.3nA in shutdown mode retains the voltage over the coupling capacitors, which helps to settle faster when the part is enabled again. It is recommended to drive the baseband inputs differentially to maintain the linearity. When a DAC is used as the signal source, a reconstruction filter should be placed between the DAC output and the LTC5589 baseband inputs to avoid aliasing.

Internal Gain Trim DACs

Four internal gain trim DACs (one for each baseband pin) are configured as 11-bit each. The usable DAC input value range is integer continuous from 64 to 2047 and 0 for shutdown. The DACs are not intended for baseband signal generation but for gain and offset setting only, because there are no reconstruction filters between the DACs and the mixer core, and there is only indirect access between

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the DAC values and the register settings. The following functions are implemented in this way:

- Coarse digital gain control with 1dB steps
- Fine digital gain control with 0.1dB steps
- Gain-temperature correction
- DC offset adjustment in the I-channel
- DC offset adjustment in the Q-channel
- I/Q gain balance control
- Disable Q-channel
- Continuous variable gain control

Coarse Digital Gain Control (DG) with 1dB Steps (Register 0x01)

Twenty digital gain positions 1dB apart are implemented by hardwiring a corresponding DAC code for all four DACs. The coarse digital gain is set by writing to the five least-significant bits in register 0x01, see Table 8 and 9. The gain is the highest for code 00000 (code 0 = 0dB, DG = 0) and the lowest for code 10011 (code 19 = –19dB, DG = –19). Note that the gain 0dB set by the digital gain control is not the same as the voltage gain of the part. The remaining 12 codes (decimal 20 to 31) are reserved.

The digital gain in dB equals minus the decimal value written into the 5 least-significant bits of the gain register. The formula relating the modulator gain G(in V/V) relative to the maximum conversion gain therefore equals:

$$G(V/V) = 10^{(DG/20)}$$

Fine Digital Gain Control(FDG) with 0.1dB Steps and Gain-Temperature Correction (Register 0x07)

Sixteen digital gain positions about 0.1dB apart can be set directly using the four least-significant bits in register 0x07 combined with bit 2 = 1 in register 0x08 (TEMPCORR = 1). For coarse digital gain settings code 9 and higher, some or more subsequent codes of the fine digital gain positions may be the same due to the limited resolution of the 11-bit DACs. The main purpose of these 0.1dB gain steps is to implement an automatic gain/temperature correction which can be activated by setting TEMPCORR = 0. In that case, the input of the fine digital gain control will be the on-chip thermometer. The on-chip thermometer generates a 4-bit digital code with code 0 corresponding to –30°C and code 15 corresponding to 120°C and 10°C spacing between the codes. The on-chip thermometer output code can be updated continuous (by clearing TEMPUPDT, bit 7 in register 0x01, see Table 8) or can be updated by bringing the external pin TTCK from low to high (and setting TEMPUPDT = 1). In case of continuous update the code will be an asynchronous update whenever the temperature crosses a certain threshold (TempComp On). In some cases it is desired to prevent a gain update to happen in the middle of a data frame. In that case, the gain/temperature update can be synchronized using the TTCK pin for example at the beginning or end of a data frame. For TempComp OFF, TEMPUPDT is set to 1 while TTCK is not toggling, deactivating the temperature gain compensation. The on-chip temperature can be read back by reading register 0x1F (TEMP[3:0]).The decimal value of TEMP[3:0] is given by:

$$TEMP[3:0] = round(T/10) + 3$$

with T the actual on-chip temperature in °C. It's accuracy is about ±10°C. TEMP[3:0] defaults to 7 after an EN low to high transition with TEMPUPDT = 1. Switching from TEMPUPDT = 0 to TEMPUPDT = 1, TEMP[3:0] indicates the temperature during the last time TTCK went from low to high. Note that the actual on-chip temperature cannot be read if TEMPCORR = 1 or when TEMPUPDT = 1 without toggling TTCK.

Analog Gain Control

The LTC5589 supports analog control of the conversion gain through a voltage applied to V_{CTRL} (pin 1). The gain can be controlled downward from the digital gain setting (DG) programmed in register 0x01. In order to minimize distortion in the RF output signal the AGCTRL bit (bit 6 in register 0x01) should be set to 1. If analog gain control is not used, V_{CTRL} should be connected to V_{CC} and AGCTRL set to 0; this saves about 2.5mA of supply current. The typical usable gain control range is from 0.9V to 3.3V. Setting V_{CTRL} to a voltage lower than V_{CC} with AGCTRL = 0 significantly impairs the linearity of the RF output signal and lowers the V_{CTRL} response time. A simplified schematic is shown in Figure 1.

I/Q DC Offset Adjustment (Registers 0x02 and 0x03) and LO Leakage

Offsets in the I- and Q-channel translates into LO leakage at the RF port. This offset can either be caused by the I/Q modulator or, in case the baseband connections are DC-coupled, applied externally. Registers 0x02 and 0x03 (I-offset and Q-offset) can be set to cancel this offset and hence lower the LO leakage. To adjust the offset in the I-channel, the BBPI DAC is set to a (slightly) different value than the BBMI DAC, introducing an offset. These 8-bit registers defaults are 128 and represents 0 offset. The register value can be set from 1 to 255. The value 0 represents an unsupported code and should not be used. Since the input referred offset depends on the gain the input offset value (V_{OS}) can be calculated as:

$$V_{OS} = 1260/((3632 \bullet G)/(N_{OS} - 128) - (N_{OS} - 128)/(3632 \bullet G))$$

and $V_{OS} = 0$ for $N_{OS} = 128$. G represents the gain from Table 4.

Table 4. Coarse Digital Gain (DG) Register Settings.

DG (dB)	G(V/V)	DEC	BINARY	HEX
0	1.000	0	00000	0x00
–1	0.891	1	00001	0x01
–2	0.794	2	00010	0x02
–3	0.708	3	00011	0x03
–4	0.631	4	00100	0x04
–5	0.562	5	00101	0x05
–6	0.501	6	00110	0x06
–7	0.447	7	00111	0x07
–8	0.398	8	01000	0x08
–9	0.355	9	01001	0x09
–10	0.316	10	01010	0x0A
–11	0.282	11	01011	0x0B
–12	0.251	12	01100	0x0C
–13	0.224	13	01101	0x0D
–14	0.200	14	01110	0x0E
–15	0.178	15	01111	0x0F
–16	0.158	16	10000	0x10
–17	0.141	17	10001	0x11
–18	0.126	18	10010	0x12
–19	0.112	19	10011	0x13

A positive offset means that the voltage of the positive input terminal (BBPI or BBPQ) is increased relative to the negative input terminal (BBMI or BBMQ).

I/Q Gain Ratio (Register 0x04) and Side-Band Suppression

The 8-bit I/Q gain ratio register 0x04 controls the ratio of the I-channel mixer conversion gain G_I and the Q-channel mixer conversion gain G_Q. Together with the quadrature phase imbalance register 0x05, register 0x04 allows further optimization of the modulator side-band suppression.

The expression relating the gain ratio G_I/G_Q to the contents of the 8-bit register 0x04, represented by decimal N_{IQ} and the nominal conversion gain G equals:

$$20 \log (G_I/G_Q) = 20 \log ((3632 \bullet G - (N_{IQ} - 128))/(3632 \bullet G + (N_{IQ} - 128))) \text{ (dB)}$$

The step size of the gain ratio trim in dB vs N_{IQ} is approximately constant for the same digital gain setting. For digital gain setting = –4, for example, the step size is about 7.6mdB. Table 5 lists the gain step size for each digital gain setting that follows from the formula above.

Table 5. I/Q Gain Ratio Step Size vs Digital Gain Setting

DG (dB)	G (V/V)	$\Delta G_I/G_Q$ (mdB)
0	1.000	4.8
–1	0.891	5.4
–2	0.794	6.0
–3	0.708	6.8
–4	0.631	7.6
–5	0.562	8.5
–6	0.501	9.6
–7	0.447	10.7
–8	0.398	12.0
–9	0.355	13.5
–10	0.316	15.1
–11	0.282	17.1
–12	0.251	19.2
–13	0.224	21.5
–14	0.200	24.2
–15	0.178	27.3
–16	0.158	30.7
–17	0.141	34.6
–18	0.126	39.0
–19	0.112	44.1

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The conversion gain of the I-channel and Q-channel are equal for N_{IQ} = 128. The I-channel gain is larger than the Q-channel gain for $N_{IQ} > 128$.

Disable Q-Channel

If bit 5 in register 0x01 (QDISABLE) is set, the Q-channel is switched off, turning the I/Q modulator into an upconversion mixer. It is recommended to float the BBPQ and BBMQ pins in this mode. The default mode is Q-channel on (QDISABLE = 0).

LO Section (Register 0x00)

The internal LO chain consists of a polyphase filter which generates the I and Q signals for the image-reject double-balanced mixer. The center frequency of the polyphase filter is set by the lower seven bits of register 0x00. The recommended settings vs LO frequency are given in Table 6 (see the QuikEval™ GUI).

Table 6. Register 0x00 Setting vs LO Frequency

REGISTER VALUE			LO FREQUENCY RANGE (MHz)	
DECIMAL	BINARY	HEX	LOWER BOUND	UPPER BOUND
0	0000000	00	N/A	N/A
1	0000001	01	N/A	N/A
2	0000010	02	N/A	N/A
3	0000011	03	N/A	N/A
4	0000100	04	9204	N/A
5	0000101	05	9015	9204
6	0000110	06	8829	9015
7	0000111	07	8648	8829
8	0001000	08	8470	8648
9	0001001	09	8295	8470
10	0001010	0A	8125	8295
11	0001011	0B	7958	8125
12	0001100	0C	7794	7958
13	0001101	0D	7634	7794
14	0001110	0E	7477	7634
15	0001111	0F	7323	7477
16	0010000	10	7172	7323
17	0010001	11	7025	7172
18	0010010	12	6880	7025
19	0010011	13	6739	6880
20	0010100	14	6600	6739
21	0010101	15	6464	6600
22	0010110	16	6332	6464
23	0010111	17	6201	6332
24	0011000	18	6074	6201
25	0011001	19	5862	6074
26	0011010	1A	5768	5862
27	0011011	1B	5622	5768
28	0011100	1C	5556	5622
29	0011101	1D	5223	5556
30	0011110	1E	5167	5223
31	0011111	1F	5031	5167
32	0100000	20	4951	5031
33	0100001	21	4789	4951
34	0100010	22	4725	4789
35	0100011	23	4618	4725
36	0100100	24	4439	4618
37	0100101	25	4260	4439
38	0100110	26	4178	4260
39	0100111	27	4092	4178
40	0101000	28	4008	4092
41	0101001	29	3926	4008
42	0101010	2A	3845	3926
43	0101011	2B	3766	3845
44	0101100	2C	3688	3766
45	0101101	2D	3613	3688
46	0101110	2E	3538	3613
47	0101111	2F	3465	3538
48	0110000	30	3394	3465
49	0110001	31	3324	3394
50	0110010	32	3256	3324
51	0110011	33	3189	3256
52	0110100	34	3123	3189
53	0110101	35	3059	3123
54	0110110	36	2996	3059
55	0110111	37	2935	2996
56	0111000	38	2874	2935
57	0111001	39	2815	2874
58	0111010	3A	2757	2815
59	0111011	3B	2701	2757
60	0111100	3C	2645	2701
61	0111101	3D	2591	2645

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Table 6. Register 0x00 Setting vs LO Frequency (continued)

REGISTER VALUE			LO FREQUENCY RANGE (MHz)	
DECIMAL	BINARY	HEX	LOWER BOUND	UPPER BOUND
62	0111110	3E	2537	2591
63	0111111	3F	2485	2537
64	1000000	40	2434	2485
65	1000001	41	2384	2434
66	1000010	42	2335	2384
67	1000011	43	2287	2335
68	1000100	44	2240	2287
69	1000101	45	2194	2240
70	1000110	46	2149	2194
71	1000111	47	2104	2149
72	1001000	48	2061	2104
73	1001001	49	2019	2061
74	1001010	4A	1818	2019
75	1001011	4B	1710	1818
76	1001100	4C	1590	1710
77	1001101	4D	1506	1590
78	1001110	4E	1479	1506
79	1001111	4F	1453	1479
80	1010000	50	1427	1453
81	1010001	51	1402	1427
82	1010010	52	1377	1402
83	1010011	53	1353	1377
84	1010100	54	1329	1353
85	1010101	55	1305	1329
86	1010110	56	1282	1305
87	1010111	57	1278	1282
88	1011000	58	1221	1278
89	1011001	59	1160	1221
90	1011010	5A	1143	1160
91	1011011	5B	1140	1143
92	1011100	5C	1116	1140
93	1011101	5D	1088	1116
94	1011110	5E	1085	1088
95	1011111	5F	1079	1085
96	1100000	60	1062	1079
97	1100001	61	1037	1062
98	1100010	62	1030	1037
99	1100011	63	1017	1030
100	1100100	64	999	1017
101	1100101	65	981	999
102	1100110	66	964	981
103	1100111	67	947	964
104	1101000	68	930	947
105	1101001	69	914	930
106	1101010	6A	897	914
107	1101011	6B	880	897
108	1101100	6C	860	880
109	1101101	6D	849	860
110	1101110	6E	829	849
111	1101111	6F	810	829
112	1110000	70	792	810
113	1110001	71	774	792
114	1110010	72	757	774
115	1110011	73	741	757
116	1110100	74	726	741
117	1110101	75	712	726
118	1110110	76	699	712
119	1110111	77	687	699
120	1111000	78	675	687
121	1111001	79	663	675
122	1111010	7A	651	663
123	1111011	7B	639	651
124	1111100	7C	628	639
125	1111101	7D	618	628
126	1111110	7E	609	618
127	1111111	7F	N/A	609

A simplified circuit schematic of the LOL and LOC interfaces is depicted in Figure 2. The LOL and LOC inputs are not differential LO inputs. They are 50Ω inputs and are intended to be driven with an inductor going to the LOL input and a capacitor to the LOC input. Do not interchange the capacitor and inductor, as this will result in very poor performance.

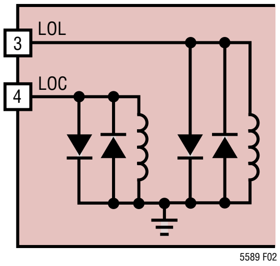

Figure 2. Simplified Circuit Schematic for the LOL and LOC Inputs

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For a wideband LO range an inductor value of 4.7nH and a capacitor value of 2pF (standard LO match, L1 and C5, see Fig. 12) is recommended at these pins, forming a diplexer circuit with center frequency of 1.4GHz. This diplexer helps to improve the uncalibrated side-band suppression significantly around 1.4GHz. Even for LO frequencies far from 1.4GHz the diplexer performs better than a single-ended LO drive or a differential drive. A 0.2pF capacitor is added in front of the diplexer in order to improve the high-frequency LO return loss (C18). Above 3.5GHz it is recommended to use the 5.8GHz LO Match (L1 = 0.8nH, C5 = 0.4pF, C18 = 0.1pF) This will improve return loss, side-band suppression, gain, OIP2 and OIP3 at higher LO frequencies. Due to factory calibration of the polyphase filter the typical side-band suppression is about 45dBc for frequencies from 700MHz to 4.2GHz using standard match and 30dBc from 4.2GHz to 6GHz using 5.8GHz LO Match. An adjustment of table 6 is recommended below 3.5GHz in case wide-band performance up to 6GHz is required. Using the 5.8GHz LO match changes the optimum register 0x00 settings below 3.5GHz compared using the standard LO match. Optimization shows good side-band suppression performance from 850MHz up to 6GHz using 5.8GHz LO match.

Vector Modulator

The LTC5589 can be used as a vector modulator by applying an RF signal to the LO port and obtaining a phase/gain modified signal at the RF output. The phase and gain can be set by DC values at the baseband inputs in combination with the settings of registers 0x00 to 0x08. For best performance it is recommended to design the LO input diplexer components L1, C5 and C18 to match the RF input signal frequency. The values for L1 and C5 are approximately:

$$L1 = 50/(2\pi f_{RF})$$

$$C5 = 1/(100\pi f_{RF})$$

I/Q Phase Balance Adjustment Register 0x05 and Side-Band Suppression

Ideally the I-channel LO phase is exactly 90° ahead of the Q-channel LO phase, so called quadrature. In practice however, the I/Q phase difference differs from exact quadrature by a small error due to component parameter variations and harmonic content in the LO signal (see below).

The I/Q phase imbalance register (0x05) allows adjustment of the I/Q phase shift to compensate for such errors. Together with gain ratio register 0x04, it can thus be used to optimize the side-band suppression of the modulator.

Register 0x05 contains two parts (see Table 8); the five least significant bits IQPHF realize a fine phase adjustment, while the three most significant bits IQPHE are used for coarse adjustments. The fine phase adjustment realized by IQPHF can be approximated as:

$$\varphi_{IQ} = -((N_{ph} - 16)/15)$$

where N_{ph} is the decimal value of IQPHF. A positive value for φ_{IQ} means that the I-channel LO phase is more than 90° ahead of the Q-channel LO phase. The extension bits IQPHE provide a larger phase adjustment range.

The extension bits IQPHE introduce a large phase offset in addition to the fine adjustment realized by the IQPHF bits. The sign of this large offset can be positive or negative, controlled by IQPHSIGN (bit 7 in register 0x00). Including these bits, the total phase shift from quadrature can be expressed as:

$$\varphi_{IQ} = -(M_{PH}/15) \text{ (degrees) with}$$

$$M_{PH} = N_{COARSE} + N_{PH} - 16 \text{ and}$$

$$N_{COARSE} = 32 \cdot (-1)^{IQPHSIGN + 1} \cdot N_{EXT}$$

where N_{ext} equals the decimal value of the IQPHE bits. The valid range of values for $(N_{ph} - 16)$ is thus expanded from {–16, –15, ... , +15} to {–240, –239, ... , +239}. Table 7 in the Appendix lists all the possible combinations. The coding ranges for IQPHSIGN = 0 and IQPHSIGN = 1 overlap between $M_{ph} = -16$ and $M_{ph} = +15$, such that IQPHSIGN only needs to be changed for larger phase shifts.

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As a side effect, the extension bits slightly detune the center frequency of the polyphase filter, after crossing the boundary to a new N_{COARSE} value. This can be observed as a large step in the actual phase shift. A solution for this is to decrease the value in the frequency register 0x00 (increase the polyphase filter center frequency) at the N_{COARSE} value boundaries. The result is a smooth phase adjustment.

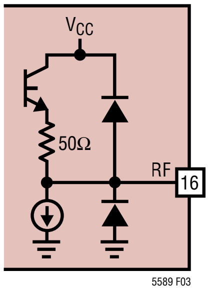

Figure 3. Simplified Circuit Schematic for the RF Output Port

Whenever the polyphase filter center frequency is adjusted to improve the smoothness of the phase adjustment, it is recommended to manually program the LO port impedance match using the CLOO bits in register 0x06. By default, changing the filter center frequency also automatically adjusts the matching of the LO port (when CLOEN, bit 4 in register 0x06 is set). However, since the LO carrier frequency does not change, automatic adjustment of the LO match is undesirable in this case; it may add another large step to the phase adjustment. Instead, the LO match should remain unchanged while the filter center frequency is adjusted. This can be achieved as follows. First, the current LO matching configuration is read from the CLO bits in register 0x1D, and written to the CLOO override bits in register 0x06. Subsequently, the CLOEN bit (bit 4, register 0x06) is cleared to disable automatic LO match adjustment. As a result the center frequency can be adjusted in register 0x00 without changing the LO match.

At 700MHz the maximum phase shift is about ±0.15°, while at 800MHz it improves to about ±5.8°. At 6GHz the maximum phase shift is about ±6.7° and a phase adjustment causes considerable gain imbalance as a side effect. Iterative adjustment of I/Q gain and phase is required for optimum side-band suppression.

Square Wave LO Drive

Harmonic content of the LO signal adversely affects quadrature phase error and gain accuracy, whenever a polyphase filter is used for quadrature generation. The LTC5589 can correct for phase and gain errors due to harmonics in the LO carrier (e.g. in a square wave) by setting appropriate values in the I/Q gain and I/Q phase registers. Such adjustments are typically needed when the 3rd-order harmonic of the LO signal exceeds the desirable side-band suppression minus 17dB. Although the polyphase filter is less sensitive to the second harmonic content of the LO carrier, its influence can still be significant. For –35dBc second harmonic content, the side-band suppression can degrade to –60dBc; for –28dBc it is –40dBc, assuming no I/Q gain and phase adjustments are made.

RF Output

After upconversion, the RF outputs of the I and Q mixers are combined. An on-chip buffer performs internal differential to single-ended conversion, while transforming the output signal to 50Ω as shown in Figure 3.

The RF port return loss vs frequency and digital gain setting for EN = High and EN = Low is given in the typical performance characteristics section.

For V_{CC} = 3.3V and EN = High the RF pin DC voltage is about 1.77V. For V_{CC} = 3.3V and EN = Low the RF pin DC voltage is about 3.1V.

Enable Interface

Figure 4 shows a simplified schematic of the EN pin interface. The voltage necessary to turn on the LTC5589 is 1.1V. To disable (shut down) the chip, the enable voltage must be below 0.2V.

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SERIAL PORT

The SPI-compatible serial port provides control and monitoring functionality.

Communication Sequence

The serial bus is comprised of CSB, SCLK, SDI and SDO. Data transfers to the part are accomplished by the serial bus master device first taking CSB low to enable the LTC5589's port. Input data applied on SDI is clocked on the rising edge of SCLK, with all transfers MSB first. The communication burst is terminated by the serial bus master returning CSB high. See Figure 5 for details.

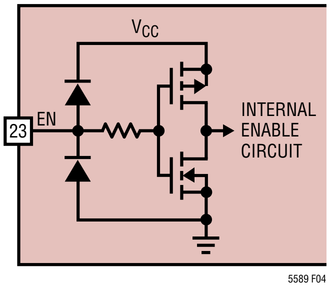

Figure 4. Simplified Circuit Schematic of the EN interface

Data is read from the part during a communication burst using SDO. Readback may be multidrop (more than one LTC5589 connected in parallel on the serial bus), as SDO is high impedance (Hi-Z) when CSB = 1, or when data is not being read from the part. *If the LTC5589 is not used in a multidrop configuration, or if the serial port master is not capable of setting the SDO line level between read sequences, it is recommended to attach a resistor between SDO and* V_{CC_L} *to ensure the line returns to* V_{CC_L} *during Hi-Z states. The resistor value should be large enough to ensure that the SDO output current does not exceed 10mA. See Figure 6 for details.*

Single Byte Transfers

The serial port is arranged as a simple memory map, with status and control available in 9 read/write and 23 read-only byte-wide registers. All data bursts are comprised of at least two bytes. The 7 most significant bits of the first byte are the register address, with an LSB of 1 indicating a read from the part, and LSB of 0 indicating a write to the part. The subsequent byte, or bytes, is data from/to the specified register address. See Figure 7 for an example of a detailed write sequence, and Figure 8 for a read sequence.

Figure 9 shows an example of two write communication bursts. The first byte of the first burst sent from the serial bus master on SDI contains the destination register ad-

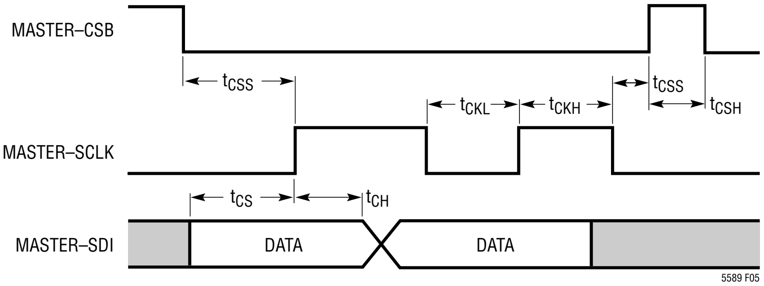

Figure 5. Serial Port Write Timing Diagram

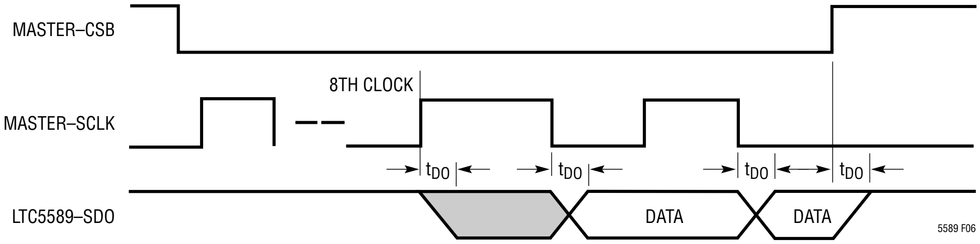

Figure 6. Serial Port Read Timing Diagram

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dress (Addr0) and an LSB of 0 indicating a write. The next byte is the data intended for the register at address Addr0. CSB is then taken high to terminate the transfer. The first byte of the second burst contains the destination register address (Addr1) and an LSB indicating a write. The next byte on SDI is the data intended for the register at address Addr1. CSB is then taken high to terminate the transfer.

Note that the written data is transferred to the internal register at the falling edge of the 16th clock cycle (parallel load).

Multiple Byte Transfers

More efficient data transfer of multiple bytes is accomplished by using the LTC5589's register address auto-increment feature as shown in Figure 10. The serial port master sends the destination register address in the first byte and its data in the second byte as before, but continues sending bytes destined for subsequent registers. Byte 1's address is Addr0+1, Byte 2's address is Addr0+2, and so on. If the register address pointer attempts to increment past 31 (0x1F), it is automatically reset to 0.

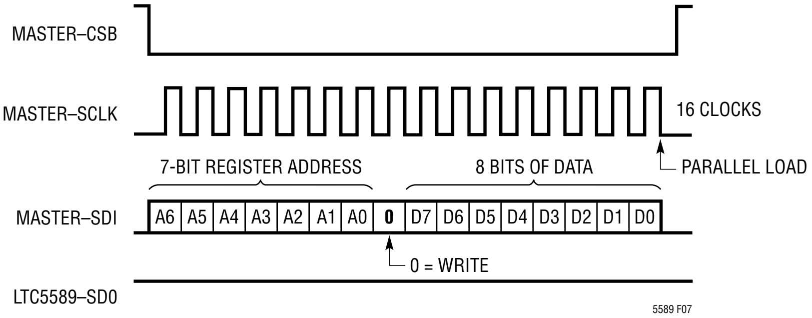

Figure 7. Serial Port Write Sequence

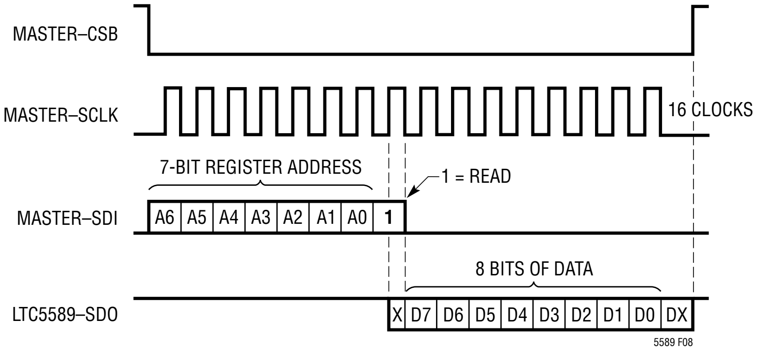

Figure 8. Serial Port Read Sequence

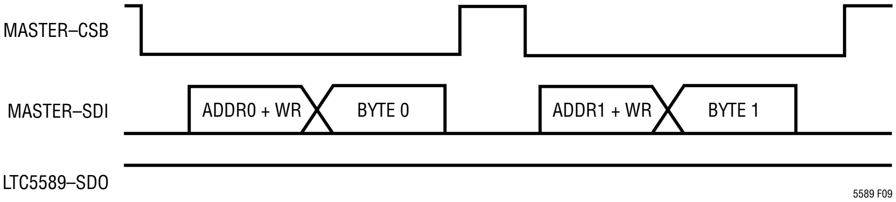

Figure 9. Serial Port Single Byte Writes

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An example of an auto-increment read from the part is shown in Figure 11. The first byte of the burst sent from the serial bus master on SDI contains the destination register address (Addr0) and an LSB of 1 indicating a read. Once the LTC5589 detects a read burst, it takes SDO out of the Hi-Z condition and sends data bytes sequentially, beginning with data from register Addr0. The part ignores all other data on SDI until the end of the burst.

Multidrop Configuration

Several LTC5589s may share the serial bus. In this multidrop configuration, SCLK, SDI, and SDO are common between all parts. The serial bus master must use a separate CSB for each LTC5589 and ensure that only one device has CSB asserted at any time. It is recommended to attach a high value resistor to SDO to ensure the line returns to a known level (V_{CC_L}) during Hi-Z states.

Serial Port Registers

The memory map of the LTC5589 may be found in the Appendix in Table 8, with detailed bit descriptions found in Table 9. The register address shown in hexadecimal format under the ADDR column is used to specify each register. Each register is denoted as either read-only (R) or read-write (R/W). The register's default value on device power-up or after a reset (bit 3, register 0x08, SRESET) is shown at the right.

SPI Signal Levels

The SPI bus supports signal levels from a digital V_{CC_L} from 1.2V to 3.6V. The CSB = 1.2V condition creates an additional static input sleep current of 0.2μA. For CSB = 1.8V or higher the extra sleep current can be neglected.

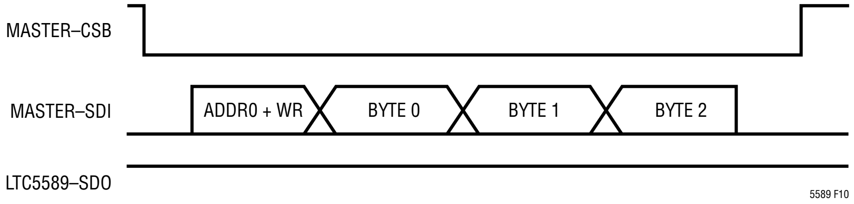

Figure 10. Serial Port Auto-Increment Write

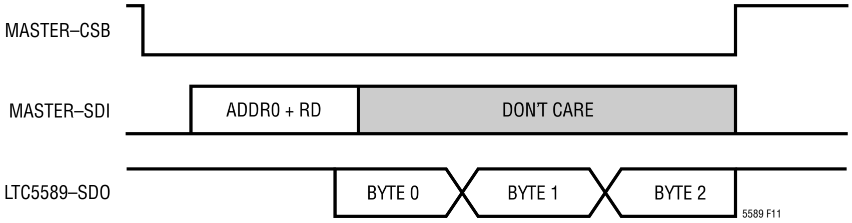

Figure 11. Serial Port Auto-Increment Read

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Evaluation Board

Figure 12 shows the evaluation board schematic. A good ground connection is required for the exposed pad. If this is not done properly, the RF performance will degrade. Figures 13 and 14 show the component side and bottom side of the evaluation board.

Ferrite bead FB1 limits the supply voltage ramping speed in case V_{CC} is abruptly connected to a voltage source.

In the application, limit the V_{CC} ramp speed to a maximum of 1V/µs.

Baseband termination components C6 to C9 and R8 to R11 are not installed in the customer demo board to avoid a low frequency corner point in order to maintain EVM performance.

For better performance at frequencies above 3.5GHz, it is recommended to use L1 = 0.8nH, C5 = 0.4pF and C18 = 0.1pF.

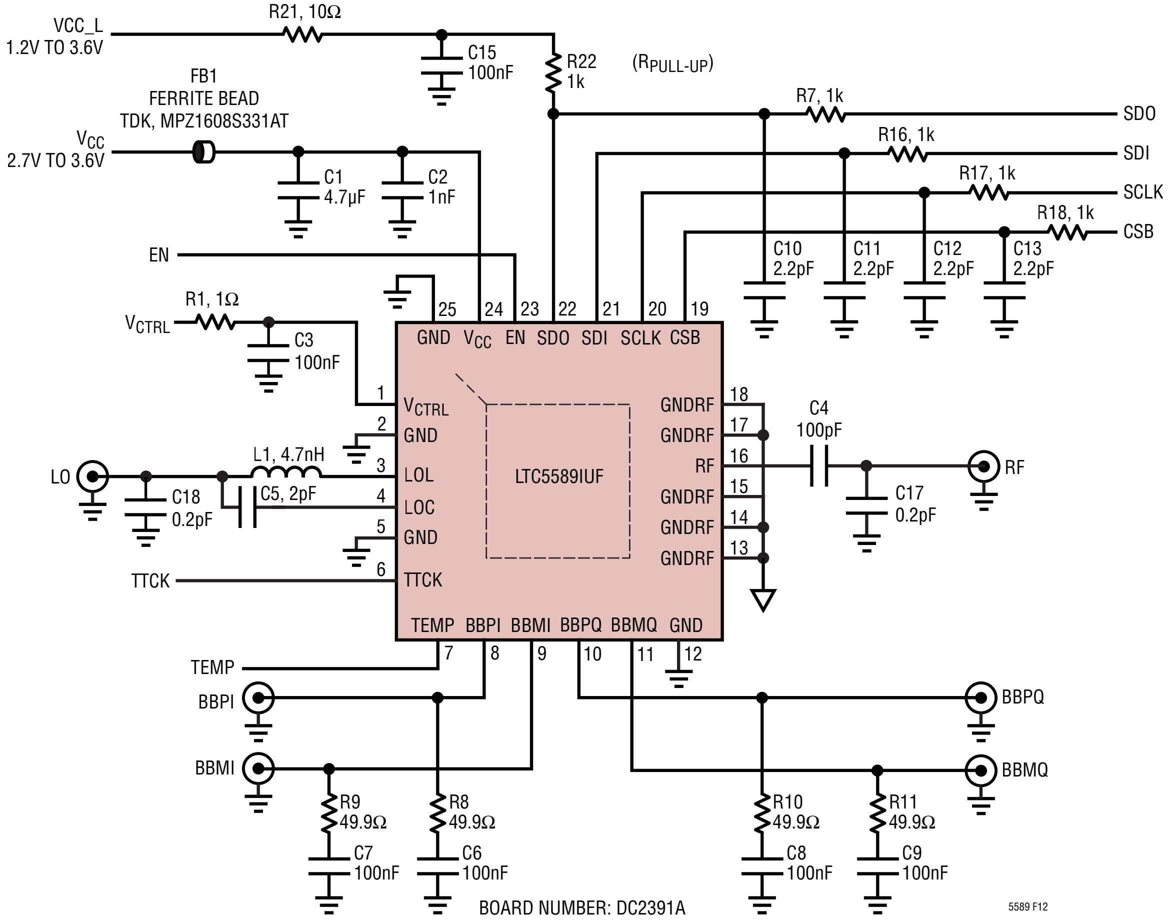

Figure 12. Test Circuit Schematic

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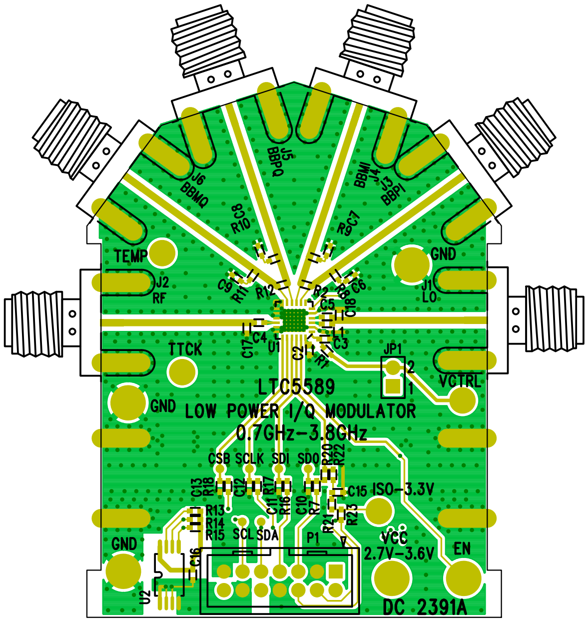

Figure 13. Evaluation Board Component Side

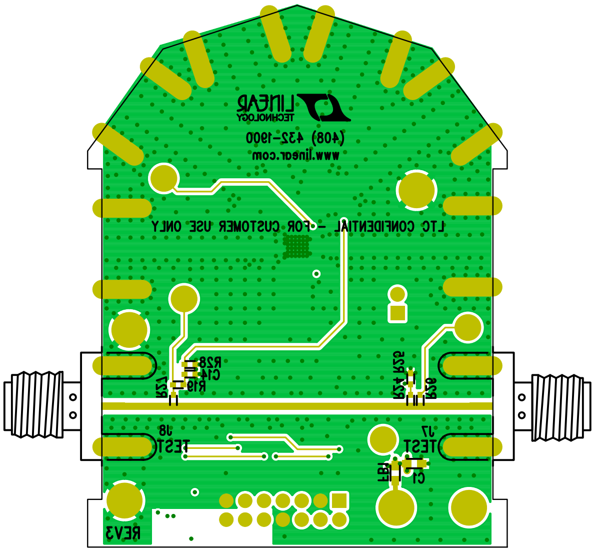

Figure 14. Evaluation Board Bottom Side

APPENDIX

Phase Shift Register (0x05) Map

This appendix summarizes the detailed value assignments for the phase shift register, including the extension bits and sign bit (bit 7 in register 0x00).

Table 7. Register 0x05 Phase Shift Register Settings, Including the Extension Bits and Sign Bit (Bit 7 in Register 0x00)

M_{PH}	N_{COARSE}	N_{PH}	B_{PH}
–240	–224	0	011100000
–239	–224	1	011100001
–238	–224	2	011100010
–237	–224	3	011100011
–236	–224	4	011100100
–235	–224	5	011100101
–234	–224	6	011100110
–233	–224	7	011100111
–232	–224	8	011101000
–231	–224	9	011101001
–230	–224	10	011101010
–229	–224	11	011101011
–228	–224	12	011101100
–227	–224	13	011101101
–226	–224	14	011101110
–225	–224	15	011101111
–224	–224	16	011110000
–223	–224	17	011110001
–222	–224	18	011110010
–221	–224	19	011110011
–220	–224	20	011110100
–219	–224	21	011110101
–218	–224	22	011110110
–217	–224	23	011110111
–216	–224	24	011111000
–215	–224	25	011111001
–214	–224	26	011111010
–213	–224	27	011111011
–212	–224	28	011111100
–211	–224	29	011111101
–210	–224	30	011111110
–209	–224	31	011111111
–208	–192	0	011000000
–207	–192	1	011000001
–206	–192	2	011000010
–205	–192	3	011000011

Table 7. Register 0x05 Phase Shift Register Settings, Including the Extension Bits and Sign Bit (Bit 7 in Register 0x00) (continued)

M_{PH}	N_{COARSE}	N_{PH}	B_{PH}
–204	–192	4	011000100
–203	–192	5	011000101
–202	–192	6	011000110
–201	–192	7	011000111
–200	–192	8	011001000
–199	–192	9	011001001
–198	–192	10	011001010
–197	–192	11	011001011
–196	–192	12	011001100
–195	–192	13	011001101
–194	–192	14	011001110
–193	–192	15	011001111
–192	–192	16	011010000
–191	–192	17	011010001
–190	–192	18	011010010
–189	–192	19	011010011
–188	–192	20	011010100
–187	–192	21	011010101
–186	–192	22	011010110
–185	–192	23	011010111
–184	–192	24	011011000
–183	–192	25	011011001
–182	–192	26	011011010
–181	–192	27	011011011
–180	–192	28	011011100
–179	–192	29	011011101
–178	–192	30	011011110
–177	–192	31	011011111
–176	–160	0	010100000
–175	–160	1	010100001
–174	–160	2	010100010
–173	–160	3	010100011
–172	–160	4	010100100
–171	–160	5	010100101
–170	–160	6	010100110
–169	–160	7	010100111
–168	–160	8	010101000
–167	–160	9	010101001
–166	–160	10	010101010
–165	–160	11	010101011
–164	–160	12	010101100

APPENDIX

Table 7. Register 0x05 Phase Shift Register Settings, Including the Extension Bits and Sign Bit (Bit 7 in Register 0x00) (continued)

M_{PH}	N_{COARSE}	N_{PH}	B_{PH}
–163	–160	13	010101101
–162	–160	14	010101110
–161	–160	15	010101111
–160	–160	16	010110000
–159	–160	17	010110001
–158	–160	18	010110010
–157	–160	19	010110011
–156	–160	20	010110100
–155	–160	21	010110101
–154	–160	22	010110110
–153	–160	23	010110111
–152	–160	24	010111000
–151	–160	25	010111001
–150	–160	26	010111010
–149	–160	27	010111011
–148	–160	28	010111100
–147	–160	29	010111101
–146	–160	30	010111110
–145	–160	31	010111111
–144	–128	0	010000000
–143	–128	1	010000001
–142	–128	2	010000010
–141	–128	3	010000011
–140	–128	4	010000100
–139	–128	5	010000101
–138	–128	6	010000110
–137	–128	7	010000111
–136	–128	8	010001000
–135	–128	9	010001001
–134	–128	10	010001010
–133	–128	11	010001011
–132	–128	12	010001100
–131	–128	13	010001101
–130	–128	14	010001110
–129	–128	15	010001111
–128	–128	16	010010000
–127	–128	17	010010001
–126	–128	18	010010010
–125	–128	19	010010011
–124	–128	20	010010100
–123	–128	21	010010101

Table 7. Register 0x05 Phase Shift Register Settings, Including the Extension Bits and Sign Bit (Bit 7 in Register 0x00) (continued)

M_{PH}	N_{COARSE}	N_{PH}	B_{PH}
–122	–128	22	010010110
–121	–128	23	010010111
–120	–128	24	010011000
–119	–128	25	010011001
–118	–128	26	010011010
–117	–128	27	010011011
–116	–128	28	010011100
–115	–128	29	010011101
–114	–128	30	010011110
–113	–128	31	010011111
–112	–96	0	001100000
–111	–96	1	001100001
–110	–96	2	001100010
–109	–96	3	001100011
–108	–96	4	001100100
–107	–96	5	001100101
–106	–96	6	001100110
–105	–96	7	001100111
–104	–96	8	001101000
–103	–96	9	001101001
–102	–96	10	001101010
–101	–96	11	001101011
–100	–96	12	001101100
–99	–96	13	001101101
–98	–96	14	001101110
–97	–96	15	001101111
–96	–96	16	001110000
–95	–96	17	001110001
–94	–96	18	001110010
–93	–96	19	001110011
–92	–96	20	001110100
–91	–96	21	001110101
–90	–96	22	001110110
–89	–96	23	001110111
–88	–96	24	001111000
–87	–96	25	001111001
–86	–96	26	001111010
–85	–96	27	001111011
–84	–96	28	001111100
–83	–96	29	001111101
–82	–96	30	001111110

APPENDIX

Table 7. Register 0x05 Phase Shift Register Settings, Including the Extension Bits and Sign Bit (Bit 7 in Register 0x00) (continued)

M_{PH}	N_{COARSE}	N_{PH}	B_{PH}
–81	–96	31	001111111
–80	–64	0	001000000
–79	–64	1	001000001
–78	–64	2	001000010
–77	–64	3	001000011
–76	–64	4	001000100
–75	–64	5	001000101
–74	–64	6	001000110
–73	–64	7	001000111
–72	–64	8	001001000
–71	–64	9	001001001
–70	–64	10	001001010
–69	–64	11	001001011
–68	–64	12	001001100
–67	–64	13	001001101
–66	–64	14	001001110
–65	–64	15	001001111
–64	–64	16	001010000
–63	–64	17	001010001
–62	–64	18	001010010
–61	–64	19	001010011
–60	–64	20	001010100
–59	–64	21	001010101
–58	–64	22	001010110
–57	–64	23	001010111
–56	–64	24	001011000
–55	–64	25	001011001
–54	–64	26	001011010
–53	–64	27	001011011
–52	–64	28	001011100
–51	–64	29	001011101
–50	–64	30	001011110
–49	–64	31	001011111
–48	–32	0	000100000
–47	–32	1	000100001
–46	–32	2	000100010
–45	–32	3	000100011
–44	–32	4	000100100
–43	–32	5	000100101
–42	–32	6	000100110
–41	–32	7	000100111
–40	–32	8	000101000
–39	–32	9	000101001
–38	–32	10	000101010
–37	–32	11	000101011
–36	–32	12	000101100
–35	–32	13	000101101
–34	–32	14	000101110
–33	–32	15	000101111
–32	–32	16	000110000
–31	–32	17	000110001
–30	–32	18	000110010
–29	–32	19	000110011
–28	–32	20	000110100
–27	–32	21	000110101
–26	–32	22	000110110
–25	–32	23	000110111
–24	–32	24	000111000
–23	–32	25	000111001
–22	–32	26	000111010
–21	–32	27	000111011
–20	–32	28	000111100
–19	–32	29	000111101
–18	–32	30	000111110
–17	–32	31	000111111
–16	0	0	x00000000
–15	0	1	x00000001
–14	0	2	x00000010
–13	0	3	x00000011
–12	0	4	x00000100
–11	0	5	x00000101
–10	0	6	x00000110
–9	0	7	x00000111
–8	0	8	x00001000
–7	0	9	x00001001
–6	0	10	x00001010
–5	0	11	x00001011
–4	0	12	x00001100
–3	0	13	x00001101
–2	0	14	x00001110
–1	0	15	x00001111
0	0	16	x00010000

APPENDIX

Table 7. Register 0x05 Phase Shift Register Settings, Including the Extension Bits and Sign Bit (Bit 7 in Register 0x00) (continued)

M_{PH}	N_{COARSE}	N_{PH}	B_{PH}
1	0	17	x00010001
2	0	18	x00010010
3	0	19	x00010011
4	0	20	x00010100
5	0	21	x00010101
6	0	22	x00010110
7	0	23	x00010111
8	0	24	x00011000
9	0	25	x00011001
10	0	26	x00011010
11	0	27	x00011011
12	0	28	x00011100
13	0	29	x00011101
14	0	30	x00011110
15	0	31	x00011111
16	32	0	100100000
17	32	1	100100001
18	32	2	100100010
19	32	3	100100011
20	32	4	100100100
21	32	5	100100101
22	32	6	100100110
23	32	7	100100111
24	32	8	100101000
25	32	9	100101001
26	32	10	100101010
27	32	11	100101011
28	32	12	100101100
29	32	13	100101101
30	32	14	100101110
31	32	15	100101111
32	32	16	100110000
33	32	17	100110001
34	32	18	100110010
35	32	19	100110011
36	32	20	100110100
37	32	21	100110101
38	32	22	100110110
39	32	23	100110111
40	32	24	100111000
41	32	25	100111001

Table 7. Register 0x05 Phase Shift Register Settings, Including the Extension Bits and Sign Bit (Bit 7 in Register 0x00) (continued)

M_{PH}	N_{COARSE}	N_{PH}	B_{PH}
42	32	26	100111010
43	32	27	100111011
44	32	28	100111100
45	32	29	100111101
46	32	30	100111110
47	32	31	100111111
48	64	0	101000000
49	64	1	101000001
50	64	2	101000010
51	64	3	101000011
52	64	4	101000100
53	64	5	101000101
54	64	6	101000110
55	64	7	101000111
56	64	8	101001000
57	64	9	101001001
58	64	10	101001010
59	64	11	101001011
60	64	12	101001100
61	64	13	101001101
62	64	14	101001110
63	64	15	101001111
64	64	16	101010000
65	64	17	101010001
66	64	18	101010010
67	64	19	101010011
68	64	20	101010100
69	64	21	101010101
70	64	22	101010110
71	64	23	101010111
72	64	24	101011000
73	64	25	101011001
74	64	26	101011010
75	64	27	101011011
76	64	28	101011100
77	64	29	101011101
78	64	30	101011110
79	64	31	101011111
80	96	0	101100000
81	96	1	101100001
82	96	2	101100010

APPENDIX

Table 7. Register 0x05 Phase Shift Register Settings, Including the Extension Bits and Sign Bit (Bit 7 in Register 0x00) (continued)

M_{PH}	N_{COARSE}	N_{PH}	B_{PH}
83	96	3	101100011
84	96	4	101100100
85	96	5	101100101
86	96	6	101100110
87	96	7	101100111
88	96	8	101101000
89	96	9	101101001
90	96	10	101101010
91	96	11	101101011
92	96	12	101101100
93	96	13	101101101
94	96	14	101101110
95	96	15	101101111
96	96	16	101110000
97	96	17	101110001
98	96	18	101110010
99	96	19	101110011
100	96	20	101110100
101	96	21	101110101
102	96	22	101110110
103	96	23	101110111
104	96	24	101111000
105	96	25	101111001
106	96	26	101111010
107	96	27	101111011
108	96	28	101111100
109	96	29	101111101
110	96	30	101111110
111	96	31	101111111
112	128	0	110000000
113	128	1	110000001
114	128	2	110000010
115	128	3	110000011
116	128	4	110000100
117	128	5	110000101
118	128	6	110000110
119	128	7	110000111
120	128	8	110001000
121	128	9	110001001
122	128	10	110001010
123	128	11	110001011

Table 7. Register 0x05 Phase Shift Register Settings, Including the Extension Bits and Sign Bit (Bit 7 in Register 0x00) (continued)

M_{PH}	N_{COARSE}	N_{PH}	B_{PH}
124	128	12	110001100
125	128	13	110001101
126	128	14	110001110
127	128	15	110001111
128	128	16	110010000
129	128	17	110010001
130	128	18	110010010
131	128	19	110010011
132	128	20	110010100
133	128	21	110010101
134	128	22	110010110
135	128	23	110010111
136	128	24	110011000
137	128	25	110011001
138	128	26	110011010
139	128	27	110011011
140	128	28	110011100
141	128	29	110011101
142	128	30	110011110
143	128	31	110011111
144	160	0	110100000
145	160	1	110100001
146	160	2	110100010
147	160	3	110100011
148	160	4	110100100
149	160	5	110100101
150	160	6	110100110
151	160	7	110100111
152	160	8	110101000
153	160	9	110101001
154	160	10	110101010
155	160	11	110101011
156	160	12	110101100
157	160	13	110101101
158	160	14	110101110
159	160	15	110101111
160	160	16	110110000
161	160	17	110110001
162	160	18	110110010
163	160	19	110110011
164	160	20	110110100

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Table 7. Register 0x05 Phase Shift Register Settings, Including the Extension Bits and Sign Bit (Bit 7 in Register 0x00) (continued)

M_{PH}	N_{COARSE}	N_{PH}	B_{PH}
165	160	21	110110101
166	160	22	110110110
167	160	23	110110111
168	160	24	110111000
169	160	25	110111001
170	160	26	110111010
171	160	27	110111011
172	160	28	110111100
173	160	29	110111101
174	160	30	110111110
175	160	31	110111111
176	192	0	111000000
177	192	1	111000001
178	192	2	111000010
179	192	3	111000011
180	192	4	111000100
181	192	5	111000101
182	192	6	111000110
183	192	7	111000111
184	192	8	111001000
185	192	9	111001001
186	192	10	111001010
187	192	11	111001011
188	192	12	111001100
189	192	13	111001101
190	192	14	111001110
191	192	15	111001111
192	192	16	111010000
193	192	17	111010001
194	192	18	111010010
195	192	19	111010011
196	192	20	111000100
197	192	21	111010101
198	192	22	111010110
199	192	23	111010111
200	192	24	111011000
201	192	25	111011001
202	192	26	111011010
203	192	27	111011011

Table 7. Register 0x05 Phase Shift Register Settings, Including the Extension Bits and Sign Bit (Bit 7 in Register 0x00) (continued)

M_{PH}	N_{COARSE}	N_{PH}	B_{PH}
204	192	28	111011100
205	192	29	111011101
206	192	30	111011110
207	192	31	111011111
208	224	0	111100000
209	224	1	111100001
210	224	2	111100010
211	224	3	111100011
212	224	4	111100100
213	224	5	111100101
214	224	6	111100110
215	224	7	111100111
216	224	8	111101000
217	224	9	111101001
218	224	10	111101010
219	224	11	111101011
220	224	12	111101100
221	224	13	111101101
222	224	14	111101110
223	224	15	111101111
224	224	16	111110000
225	224	17	111110001
226	224	18	111110010
227	224	19	111110011
228	224	20	111110100
229	224	21	111110101
230	224	22	111110110
231	224	23	111110111
232	224	24	111111000
233	224	25	111111001
234	224	26	111111010
235	224	27	111111011
236	224	28	111111100
237	224	29	111111101
238	224	30	111111110
239	224	31	111111111

APPENDIX

Table 8. Serial Port Register Contents

ADDR	MSB	[6]	[5]	[4]	[3]	[2]	[1]	LSB	R/W	DEFAULT
0x00	IQPHSIGN	FREQ[6]	FREQ[5]	FREQ[4]	FREQ[3]	FREQ[2]	FREQ[1]	FREQ[0]	R/W	0x3E
0x01	TEMPUPDT	AGCTRL	QDISABLE	GAIN[4]	GAIN[3]	GAIN[2]	GAIN[1]	GAIN[0]	R/W	0x84
0x02	OFFSETI[7]	OFFSETI[6]	OFFSETI[5]	OFFSETI[4]	OFFSETI[3]	OFFSETI[2]	OFFSETI[1]	OFFSETI[0]	R/W	0x80
0x03	OFFSETQ[7]	OFFSETQ[6]	OFFSETQ[5]	OFFSETQ[4]	OFFSETQ[3]	OFFSETQ[2]	OFFSETQ[1]	OFFSETQ[0]	R/W	0x80
0x04	IQGR[7]	IQGR[6]	IQGR[5]	IQGR[4]	IQGR[3]	IQGR[2]	IQGR[1]	IQGR[0]	R/W	0x80
0x05	IQPHE[2]	IQPHE[1]	IQPHE[0]	IQPHF[4]	IQPHF[3]	IQPHF[2]	IQPHF[1]	IQPHF[0]	R/W	0x10
0x06	*	*	*	CLOEN	CLOO[3]	CLOO[2]	CLOO[1]	CLOO[0]	R/W	0x50
0x07	0†	0†	0†	0†	GAINF[3]	GAINF[2]	GAINF[1]	GAINF[0]	R/W	0x06
0x08	0†	0†	0†	0†	SRESET	TEMPCORR	THERMINP	*	R/W	0x00
0x09	0†	0†	0†	0†	0†	0†	0†	0†	R	0x00
0x0A	*†	*†	*†	*†	*†	*†	*†	*†	R	
0x0B	0†	0†	0†	0†	FUSE[3]	FUSE[2]	FUSE[1]	FUSE[0]	R	0x0X
0x0C	0†	0†	CPPP0[5]	CPPP0[4]	CPPP0[3]	CPPP0[2]	CPPP0[1]	CPPP0[0]	R	0xXX
0x0D	0†	CPPP1[6]	CPPP1[5]	CPPP1[4]	CPPP1[3]	CPPP1[2]	CPPP1[1]	CPPP1[0]	R	0x0X
0x0E	0†	0†	CPPM0[5]	CPPM0[4]	CPPM0[3]	CPPM0[2]	CPPM0[1]	CPPM0[0]	R	0xXX
0x0F	0†	CPPM1[6]	CPPM1[5]	CPPM1[4]	CPPM1[3]	CPPM1[2]	CPPM1[1]	CPPM1[0]	R	0x0X
0x10	0†	GPI0[6]	GPI0[5]	GPI0[4]	GPI0[3]	GPI0[2]	GPI0[1]	GPI0[0]	R	0x08
0x11	GPI1[7]	GPI1[6]	GPI1[5]	GPI1[4]	GPI1[3]	GPI1[2]	GPI1[1]	GPI1[0]	R	0xFF
0x12	0†	GPI2[6]	GPI2[5]	GPI2[4]	GPI2[3]	GPI2[2]	GPI2[1]	GPI2[0]	R	0x01
0x13	0†	GMI0[6]	GMI0[5]	GMI0[4]	GMI0[3]	GMI0[2]	GMI0[1]	GMI0[0]	R	0x08
0x14	GMI1[7]	GMI1[6]	GMI1[5]	GMI1[4]	GMI1[3]	GMI1[2]	GMI1[1]	GMI1[0]	R	0xFF
0x15	0†	GMI2[6]	GMI2[5]	GMI2[4]	GMI2[3]	GMI2[2]	GMI2[1]	GMI2[0]	R	0x01
0x16	0†	GPQ0[6]	GPQ0[5]	GPQ0[4]	GPQ0[3]	GPQ0[2]	GPQ0[1]	GPQ0[0]	R	0x08
0x17	GPQ1[7]	GPQ1[6]	GPQ1[5]	GPQ1[4]	GPQ1[3]	GPQ1[2]	GPQ1[1]	GPQ1[0]	R	0xFF
0x18	0†	GPQ2[6]	GPQ2[5]	GPQ2[4]	GPQ2[3]	GPQ2[2]	GPQ2[1]	GPQ2[0]	R	0x01
0x19	0†	GMQ0[6]	GMQ0[5]	GMQ0[4]	GMQ0[3]	GMQ0[2]	GMQ0[1]	GMQ0[0]	R	0x08
0x1A	GMQ1[7]	GMQ1[6]	GMQ1[5]	GMQ1[4]	GMQ1[3]	GMQ1[2]	GMQ1[1]	GMQ1[0]	R	0xFF
0x1B	0†	GMQ2[6]	GMQ2[5]	GMQ2[4]	GMQ2[3]	GMQ2[2]	GMQ2[1]	GMQ2[0]	R	0x01
0x1C	0†	0†	0†	0†	0†	0†	0†	0†	R	0x00
0x1D	0†	0†	0†	0†	CLO[3]	CLO[2]	CLO[1]	CLO[0]	R	0x00
0x1E	0†	0†	0†	GOR	IDT[3]	IDT[2]	IDT[1]	IDT[0]	R	0x04
0x1F	0†	0†	0†	0†	TEMP[3]	TEMP[2]	TEMP[1]	TEMP[0]	R	0x0Y

*unused †read-only; values written are disregarded, X = production dependent, Y = resets to 7 after EN from Low to High with TEMPUPDT = 1, for EN = Low all read-only (R) registers default to 0x00.

APPENDIX

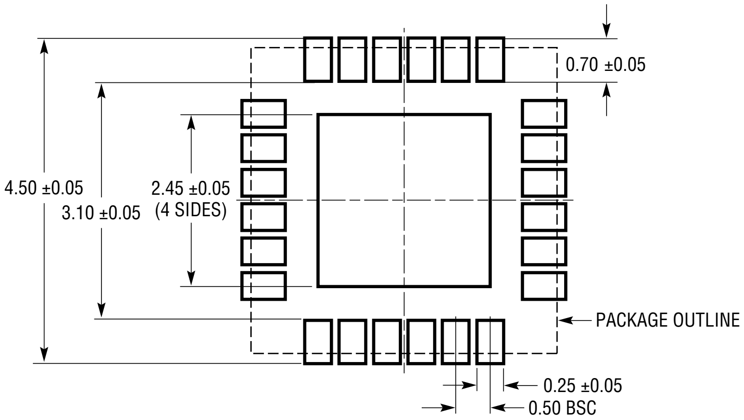
Table 9. Serial Port Register Bit Field Summary

BITS	FUNCTION	DESCRIPTION	VALID VALUES	DEFAULT
AGCTRL	Analog Gain Control Enable	Enables analog control through V_{CTRL} (Pin 1) when AGCTRL = 1.	0, 1	0
CLO[3:0]	LO Port Match Cap Array	LO port match, automatically adjusted through programming FREQ[6:0]	0x00 to 0x0F	0x00
CLOO[3:0]	LO Port Cap Array Override	Programs LO port match capacitor array when CLOEN = 0	0x00 to 0x0F	0x00
CLOEN	Automatic LO Match Enable	Automatic LO port impedance matching enabled when CLOEN = 1. Override bits CLOO[3:0] control LO port match when CLOEN = 0.	0, 1	1
CPPM0[5:0]	C_{ppQ} Fine Control	C_{ppQ} = CPPM0[5:0] + number of 1's in CPPM1[6:0] × 64	0x00 to 0x5F	0xXX
CPPM1[6:0]	C_{ppQ} Coarse Control		0x00 to 0x7F	0x0X
CPPP0[5:0]	C_{ppI} Fine Control	C_{ppI} = CPPP0[5:0] + number of 1's in CPPP1[6:0] × 64	0x00 to 0x5F	0xXX
CPPP1[6:0]	C_{ppI} Coarse Control		0x00 to 0x7F	0x0X
FREQ[6:0]	PolyPhase Filter Frequency	Programs the center frequency of the PolyPhase filter, according to Table 6.	0x00 to 0x79	0x3E
FUSE[3:0]	Fuse Read Out		0x00 to 0x0F	0x0X
GAIN[4:0]	Coarse Digital Gain Control	Programs the conversion gain in 1dB steps, according to Table 4.	0x00 to 0x13	0x04
GAINF[3:0]	Fine Digital Gain Control	Conversion gain control in approximately 0.1dB steps, when TEMPCORR = 1.	0x00 to 0x0F	0x06
GMI0[6:0]	Fine GMI DAC Read-Out	BBMI input stage gain GmI.	0x00 to 0x7F	0x08
GMI1[7:0]	Coarse GMI DAC Read-Out1	GmI = GMI0[6:0] + (number of 1's in GMI1[7:0] and GMI2[6:0]) × 128	0x00 to 0x07	0xFF
GMI2[6:0]	Coarse GMI DAC Read-Out2		0x00 to 0x07	0x01
GMQ0[6:0]	Fine GMQ DAC Read-Out	BBMQ input stage gain GmQ.	0x00 to 0x7F	0x08
GMQ1[7:0]	Coarse GMQ DAC Read-Out1	GmQ = GMQ0[6:0] + (number of 1's in GMQ1[7:0] and GMQ2[6:0]) × 128	0x00 to 0x07	0xFF
GMQ2[6:0]	Coarse GMQ DAC Read-Out2		0x00 to 0x07	0x01
GOR	Gain Out of Range	For DG < –19 GOR = 1; Else GOR = 0	0, 1	0
GPI0[6:0]	Fine GPI DAC Read-Out	BBPI input stage gain GpI.	0x00 to 0x7F	0x08
GPI1[7:0]	Coarse GPI DAC Read-Out1	GpI = GPI0[6:0] + (number of 1's in GPI1[7:0] and GPI2[6:0]) × 128	0x00 to 0x07	0xFF
GPI2[6:0]	Coarse GPI DAC Read-Out2		0x00 to 0x07	0x01
GPQ0[6:0]	Fine GPQ DAC Read-Out	BBPQ input stage gain GpQ.	0x00 to 0x7F	0x08
GPQ1[7:0]	Coarse GPQ DAC Read-Out1	GpQ = GPQ0[6:0] + (number of 1's in GPQ1[7:0] and GPQ2[6:0]) × 128	0x00 to 0x07	0xFF
GPQ2[6:0]	Coarse GPQ DAC Read-Out2		0x00 to 0x07	0x01
IDT[3:0]	RF Buffer Bias		0x00 to 0x0D	0x04
IQGR[7:0]	I/Q Gain Ratio Control	Adjust the gain difference in approximate constant steps in dB. See Table 5.	0x00 to 0xFF	0x80
IQPHE[2:0]	I/Q Phase Extension Bits	Extend the IQ phase adjustment range. See Table 7.	0x00 to 0x07	0x00
IQPHF[4:0]	Fine I/Q Phase Balance Control	Fine adjustment of IQ LO phase difference. See Table 7. Zero phase shift for 0x10.	0x00 to 0x1F	0x10
IQPHSIGN	Sign IQ Phase Extension Bits	Encodes the sign of the IQ phase extension bits IQPHE[2:0]. Positive for IQPHSIGN = 1.	0, 1	0
OFFSETI[7:0]	I-Channel Offset Control	Adjusts DC offset in the I-channel. Zero offset for 0x80.	0x01 to 0xFF	0x80
OFFSETQ[7:0]	Q-Channel Offset Control	Adjusts DC offset in the Q-channel. Zero offset for 0x80.	0x01 to 0xFF	0x80
QDISABLE	Disable Q-Channel	QDISABLE = 1 shuts down the Q-channel, turning the LTC5589 into an upconversion mixer.	0, 1	0
SRESET	Soft Reset	Writing 1 to this bit resets all registers to their default values.	0, 1	0
TEMP[3:0]	Thermometer Output	Digital representation of die temperature. Step size about 10°C.	0x00 to 0x07	0x07
TEMPCORR	Temperature Correction Disable	TEMPCORR = 1 disables temperature correction of the gain, and enables manual fine-adjustment using bits GAINF[3:0].	0, 1	0
TEMPUPDT	Temperature Correction Update	TEMPUPDT = 1 synchronizes temperature correction of the gain to a LOW - HIGH transition on the TTCK pin. Asynchronous correction for TEMPUPDT = 0.	0, 1	1
THERMINP	Thermometer Input Select	For test purposes only. Should be set to 0.	0	0

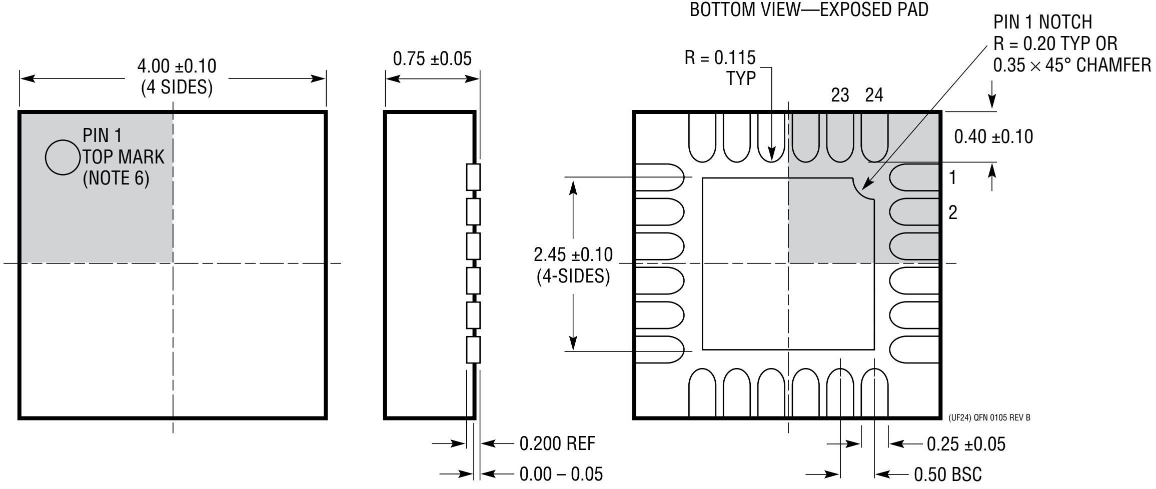
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC5589#packaging for the most recent package drawings.

UF Package
24-Lead Plastic QFN (4mm × 4mm)
(Reference LTC DWG # 05-08-1697 Rev B)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGGD-X)—TO BE APPROVED
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE, IF PRESENT
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

TYPICAL APPLICATION

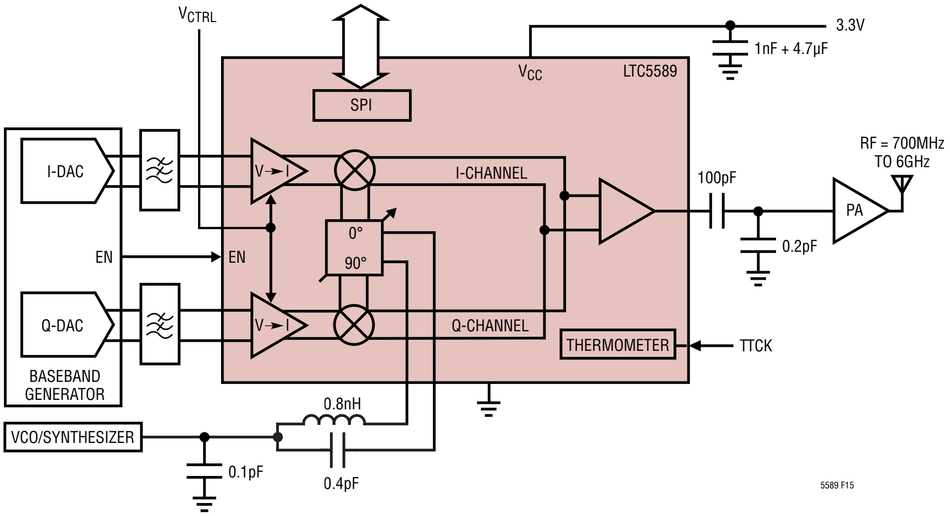


Figure 15. 700MHz to 6GHz Direct Conversion Transmitter Application

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
Infrastructure		
LT5518	1.5GHz to 2.4GHz High Linearity Direct Quadrature Modulator	22.8dBm OIP3 at 2GHz, –158.2dBm/Hz Noise Floor, 3kΩ $2.1V_{DC}$ Baseband Interface, 5V/128mA Supply
LT5528	1.5GHz to 2.4GHz High Linearity Direct Quadrature Modulator	21.8dBm OIP3 at 2GHz, –159.3dBm/Hz Noise Floor, 50Ω $0.5V_{DC}$ Baseband Interface, 5V/128mA Supply
LT5558	600MHz to 1100MHz High Linearity Direct Quadrature Modulator	22.4dBm OIP3 at 900MHz, –158dBm/Hz Noise Floor, 3kΩ $2.1V_{DC}$ Baseband Interface, 5V/108mA Supply
LT5568	700MHz to 1050MHz High Linearity Direct Quadrature Modulator	22.9dBm OIP3 at 850MHz, –160.3dBm/Hz Noise Floor, 50Ω $0.5V_{DC}$ Baseband Interface, 5V/117mA Supply
LT5571	620MHz to 1100MHz High Linearity Direct Quadrature Modulator	21.7dBm OIP3 at 900MHz, –159dBm/Hz Noise Floor, Hi-Z $0.5V_{DC}$ Baseband Interface, 5V/97mA Supply
LT5572	1.5GHz to 2.5GHz High Linearity Direct Quadrature Modulator	21.6dBm OIP3 at 2GHz, –158.6dBm/Hz Noise Floor, Hi-Z $0.5V_{DC}$ Baseband Interface, 5V/120mA Supply
LTC5598	5MHz to 1600MHz High Linearity Direct Quadrature Modulator	27.7dBm OIP3 at 140MHz, –160dBm/Hz Noise Floor with P_{OUT} = 5dBm
LT5560	0.01MHz to 4GHz Low Power Active Mixer	IIP3 = 9dBm, 2.6dB Conversion Gain, 9.3dB NF, 3.0V/10mA Supply Current
LT5506/LT5546	40MHz to 500MHz Quadrature Demodulator with VGA	56dB Gain, –49 to 0dBm IIP3, 6.8dB NF, 1.8V to 5.25V/26.5mA Supply Current
LTC5510	1MHz to 6GHz, 3.3V Wideband High Linearity Active Mixer	1.5dB Gain, 27dBm IIP3, 11.6dB NF, 3.3V/105mA Supply Current
LTC5599	30MHz to 1300MHz Low Power Direct Quadrature Modulator	OIP3 = 20.8dBm, -156.7dBm/Hz Noise Floor, 3.3V/28mA Supply
RF Power Detector		
LT5581	6GHz Low Power RMS Detector	40dB Dynamic Range, ±1dB Accuracy Over Temperature, 1.5mA Supply Current
LTC5582	40MHz to 10GHz RMS Power Detector	57dB Dynamic Range, ±1dB Accuracy Over Temperature, Single-Ended RF Input (No Transformer)
LT5534	50MHz to 3GHz RF Power Detector with 60dB Dynamic Range	60dB Dynamic Range, Linear-in-dB Response, 2.7V to 5.25V/7mA
LTC5532	300MHz to 7GHz RF Detector with Gain and Offset Adjustment	Temperature Compensated Schottky Detector, –32dBm to 10dBm Input Power Range, 500µA Supply Current

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