深圳市拓普微科技开发有限公司
SHENZHEN TOPWAY TECHNOLOGY CO., LTD.

LMT043DFFFWD-NAA

LCD Module User Manual

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Date: 2016-11-23	Date:	Date:

Rev.	Descriptions	Release Date
0.1	Preliminary new release	2016-11-23

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1. General Specification

Screen Size(Diagonal) :	4.3 inch
Resolution :	480(RGB) x 272
Signal Interface :	8bit data, 1bit address, 8080mode
Color Depth :	16.7M color (24bit) （*1）
Dot Pitch :	0.198 x 0.198 (mm)
Pixel Configuration :	RGB Stripe
Display Mode :	Transmissive / Positive (normal white)
Surface Treatment :	Anti-Glare Treatment
Viewing Direction :	12 o'clock (Gray Scale Inversion Direction)（*2）
	6 o'clock（*3）
Outline Dimension :	121.0 x 70.0 x 10.7（MAX） (mm)
	(see attached drawing for details)
Active Area :	95.0x 53.86 (mm)
Backlight :	White LED
Operating Temperature :	-20 ~ +70°C
Storage Temperature :	-30 ~ +80°C

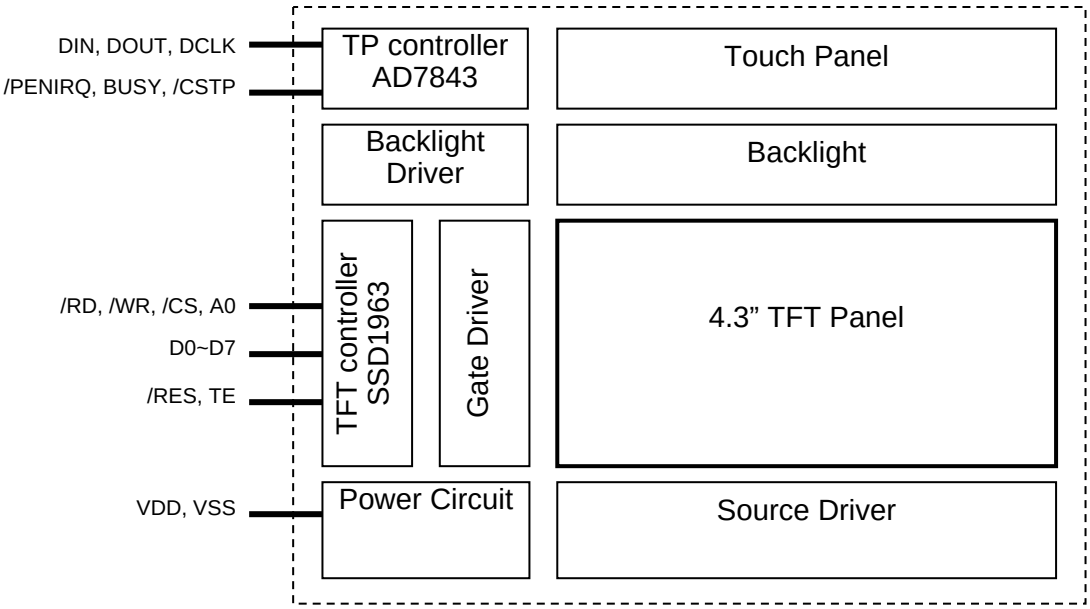
Note:

*1 Color tune may slightly changed by temperature and driving voltage.

*2 For saturated color display content (eg. pure-red, pure-green, pure-blue or pure-colors-combinations).

*3 For "color scales" display content.

2. Block Diagram



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3. K1 Terminal Function (Input Terminal)

No.	Pin Name	I/O	Descriptions
1	VSS	P	Power Supply GND (0V)
2			
3	VDD	I	Positive Power Supply (3.3 V)
4			
5	A0	I	Register Select A0=0, command A0=1, data or parameter
6	/CS	I	Chip Select signal
7	/RES	I	Reset signal, /RES=1, normal /RES=0, reset execute
8	D0	I/O	8bit Data bus
:	:		
15	D7		
16	TE	O	Tear Signal (*1)
17	/RD	I	Read signal
18	/WR	I	Write signal
19	NC	-	No Connection
20	NC		
21	/PENIRQ	O	Pen Interrupt (*2)(*3)
22	DOUT	O	Data Output(*3)
23	BUSY	O	Busy Output(*3)
24	DIN	I	Data Input(*3)
25	/CSTP	I	Chip Select, also for initiating the conversions(*3)
26	DCLK	I	Clock Input for Serial Data & conversions(*3)

Note.
*1. Tear signal may leave open when not use
*2. Pulled-up by internal resistor
*3. It is Touch Panel Controller's communication interface

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4. Absolute Maximum Ratings

Items	Symbol	Min.	Max.	Unit	Condition
Power Supply voltage	V_{DD}	-0.3	4.0	V	
Operating Temperature	T_{OP}	-20	70	°C	No Condensation
Storage Temperature	T_{ST}	-30	80	°C	No Condensation

Note:
*1. This rating applies to all parts of the module. And should not be exceeded.
*2. The operating temperature only guarantees operation of the circuit. The contrast, response speed, and the other specification related to electro-optical display quality is determined at the room temperature, T_{OP}=25℃
*3. Ambient temperature when the backlight is lit (reference value)
*4. Any Stresses exceeding the Absolute Maximum Ratings may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

5. Electrical Characteristics

5.1 DC Characteristics

VDD =3.3V,Top=25℃, VSS=0V

Items	Symbol	Min.	Typ.	Max.	Unit	Remark
Power Supply Voltage	V_{DD}	3.1	3.3	3.6	V	*2
Input logic high voltage	V_{IH}	0.85VDD	-	VDD	V	*2, *3
Input logic low voltage	V_{IL}	0	-	0.4	V	*2, *3
Output logic high voltage	V_{OH}	0.7VDD	-	VDD	V	*2, *3
Output logic low voltage	V_{OL}	0	-	0.8	V	*2, *3
Logic Supply Current (VDD)	I_{VDD}	-	260.0	-	mA	Backlight (100%PWM)

Note:
*1. Never Apply logic signal before the VDD supply.
*2. VDD setting should match the signals voltage
*3. For all the inputs signals
*4. PLL Clock Freq=200MHz

5.2 Touch panel Characteristics

Items	MIN.	TYP.	MAX.	Unit	Note
Surface hardness	3	-	-	H	-
Operating Force	30	-	160	g	-
Life Time	-	1,000,000	-	times	-
linearity	-1.5	-	+1.5	%	-
Transparency	78	-	-	%	-
Operation temperature	-20	-	70	℃	-
Storage temperature	-30	-	80	℃	-

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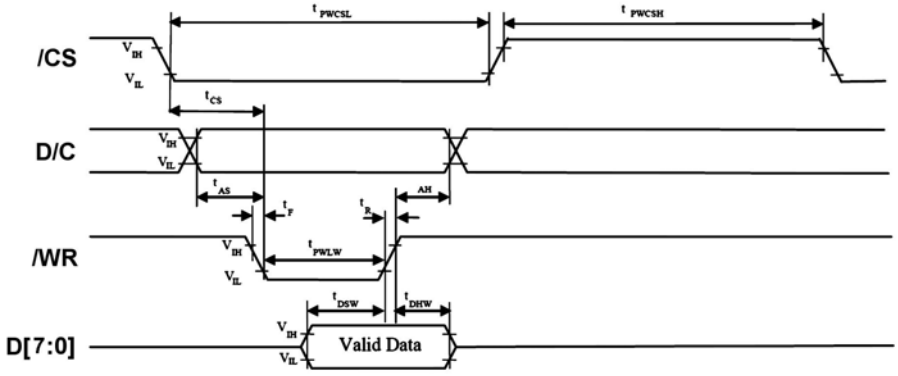
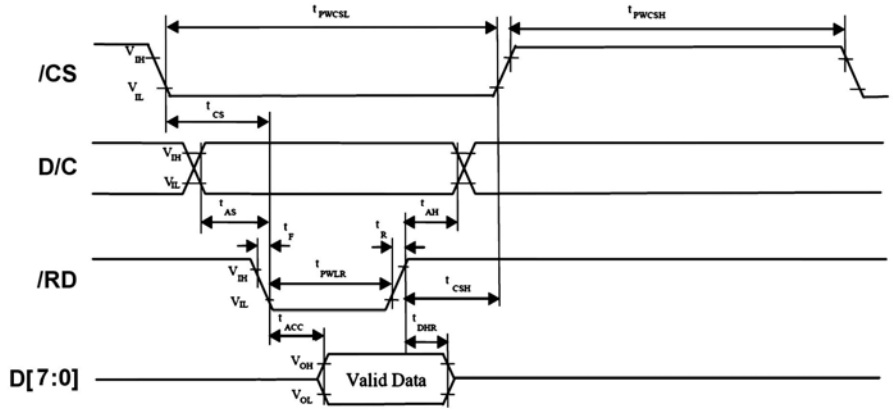
6. AC Characteristics

6.1 TFT Controller Timing Characteristics



8080 Mode Write Timing



8080 Mode Read Timing

V_{SS}=0V, V_{DD}=3.3V, T_{OP}=25°C

Item	Symbol	MIN.	TYP.	MAX.	Unit
System Clock Period(*1)	t_{MCLK}	$1/f_{MCLK}$	-	-	ns
Control Pulse High Width Write	t_{PWCSL}	16	$1.5*t_{MCLK}$	-	ns
Read		38	$1.3*t_{MCLK}$	-	ns
Control Pulse Low Width Write (next write cycle)	t_{PWCSH}	16	$1.5*t_{MCLK}$	-	ns
Write (next read cycle)		100	$9*t_{MCLK}$	-	ns
Read		100	$9*t_{MCLK}$	-	ns
Address Setup Time	t_{AS}	1.3	-	-	ns
Address Hold Time	t_{AH}	2.5	-	-	ns
Write Data Setup Time	t_{DSW}	5	-	-	ns
Write Data Hold Time	t_{DHW}	1.3	-	-	ns
Write Low Time	t_{PWLW}	15	-	-	ns
Read Data Hold Time	t_{DHR}	1.3	-	-	ns
Access Time	t_{ACC}	40	-	-	ns
Read Low Time	t_{PWLR}	45	-	-	ns
Rise Time	t_R	-	-	0.4	ns
Fall Time	t_F	-	-	0.4	ns
Chip select setup time	t_{CS}	2.5	-	-	ns
Chip select hold time to read signal	t_{CSH}	4	-	-	ns

Note:
*1. t_{MCLK} is the System Clock Period, which may config by internal PLL setting
*2. LMT043DFFFWD-NNA is driving by external 10MHz, and clock up by enabling the SSD1963 internal PLL
*3. Suggested PLL clock setting is 200MHz

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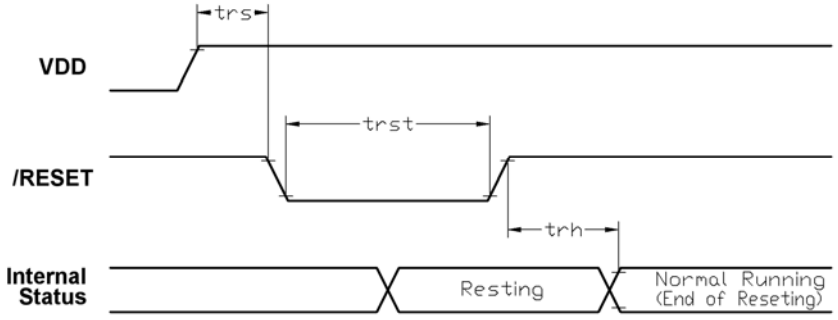
6.1.1 TFT Controller Reset Timing



V_{SS}=0V, V_{DD}=3.3V, T_{OP}=25°C

Item	Symbol	MIN.	TYP.	MAX.	Unit
Reset setup time	trs	2	-	-	ms
Reset pulse	trst	0.2	-	-	ms
Reset hold time	trh	2	-	-	ms

6.2 Touch Panel Controller Timing Characteristics

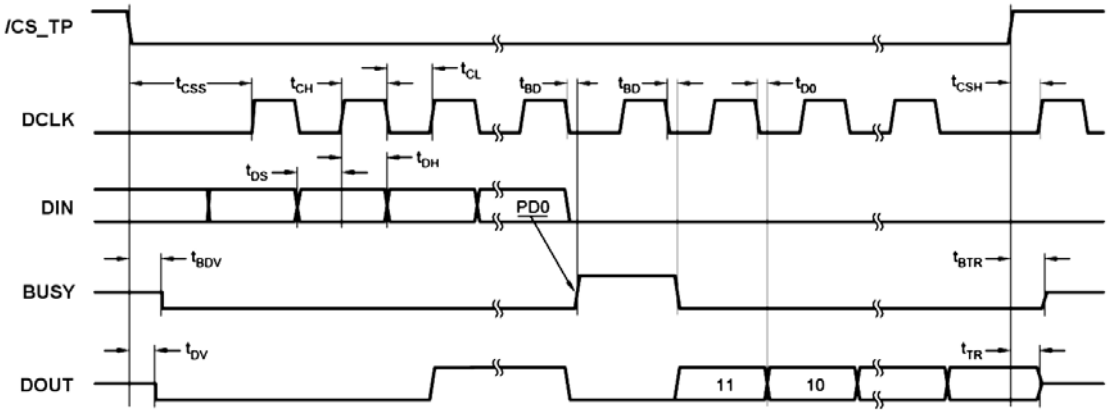
6.2.1 ADS7843 Digital Timing

VSS=0V, VDD=3.3V, T_{OP}=25°C

Item	Symbol	MIN.	TYP.	MAX.	Unit
Acquisition Time	t_{ACQ}	1.9	-	-	us
DIN Valid Prior to DCLK Rising	t_{DS}	125	-	-	ns
DIN Hold After DCLK HIGH	t_{DH}	13	-	-	ns
DCLK Falling to DOUT Valid	t_{DO}	-	-	250	ns
/CS_TP Falling to DOUT Enabled	t_{DV}	-	-	160	ns
/CS_TP Rising to DOUT Disabled	t_{TR}	-	-	250	ns
/CS_TP Falling to First DCLK Rising	t_{CSS}	125	-	-	ns
/CS_TP Rising to DCLK Ignored	t_{CSH}	10	-	-	ns
DCLK HIGH	t_{CH}	250	-	-	ns
DCLK LOW	t_{CL}	250	-	-	ns
DCLK Falling to BUSY Rising	t_{BD}	-	-	250	ns
/CS_TP Falling to BUSY Enabled	t_{BDV}	-	-	160	ns
/CS_TP Rising to BUSY Disabled	t_{BTR}	-	-	250	ns

Note. Please Refer to ADS7843E datasheet for details.

6.2.2 Timing diagram



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7. Optical Characteristics

Item		Symbol	Condition	Min	Typ	Max	Unit	Remark
View Angles		θT	CR≧10	60	70	--	Degree	Note 2
		θB		40	50	--		
		θL		60	70	--		
		θR		60	70	--		
Contrast Ratio		CR	θ=0°	400	500	--		Note1、Note3
Response Time		T_{ON}	25℃	--	20	30	ms	Note1 Note4
		T_{OFF}						
Chromaticity	White	x	Backlight is on	0.265	0.315	0.365		Note5 Note1
		y		0.285	0.335	0.385		
	Red	x		0.531	0.581	0.631		
		y		0.295	0.345	0.395		
	Green	x		0.298	0.348	0.395		
		y		0.531	0.581	0.631		
	Blue	x		0.103	0.153	0.203		
		y		0.045	0.095	0.145		
Uniformity		U		75	80	--	%	Note1、Note6
NTSC				--	50	--	%	Note 5
Luminance		L		250	300	--	cd/m^2	Note1、Note7

Note：
The parameter is slightly changed by temperature, driving voltage and materiel
Please see the Notes for testing conditions

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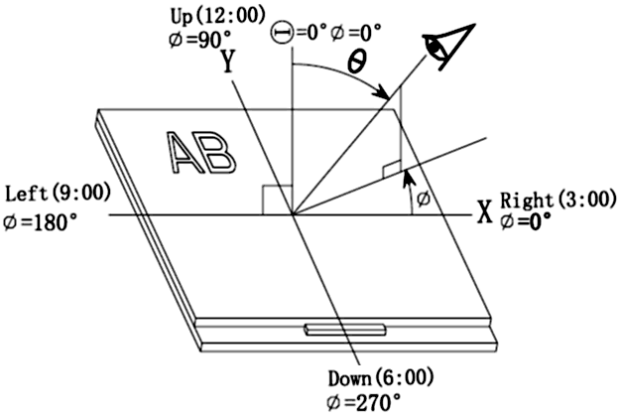
Note 1:
The data are measured after LEDs are turned on for 5 minutes. LCM displays full white. The brightness is the average value of 9 measured spots. Measurement equipment SR-3A (1°)
Measuring condition:
- Measuring surroundings: Dark room
- Measuring temperature: Ta=25℃.
- Adjust operating voltage to get optimum contrast at the center of the display.

Note 2:
The definition of viewing angle:
Refer to the graph below marked by θ and Φ

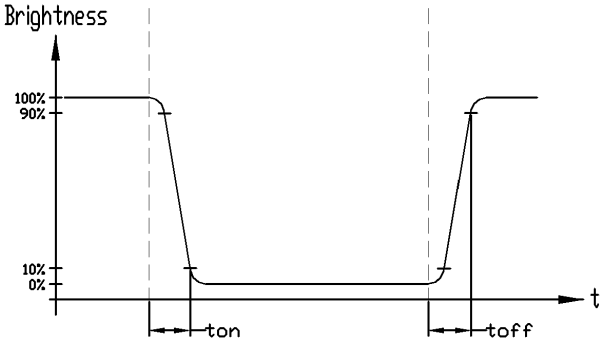


Note 3:
The definition of contrast ratio (Test LCM using SR-3A (1°)):

$$\text{Contrast Ratio(CR)} = \frac{\text{Luminance When LCD is at "White" state}}{\text{Luminance When LCD is at "Black" state}}$$

(Contrast Ratio is measured in optimum common electrode voltage)

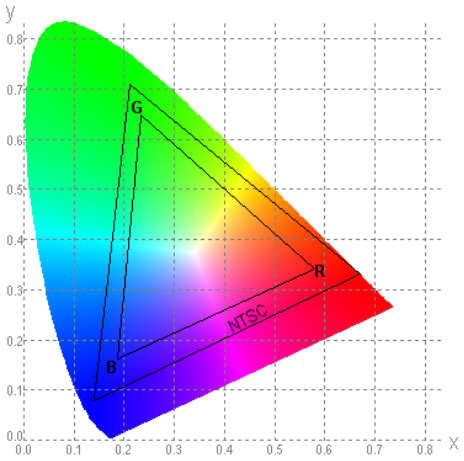
Note 4:
Definition of Response time. (Test LCD using BM-7A(2°)):
The output signals of photo detector are measured when the input signals are changed from "black" to "white"(falling time) and from "white" to "black"(rising time), respectively. The response time is defined as the time interval between the 10% and 90% of amplitudes.Refer to figure as below.



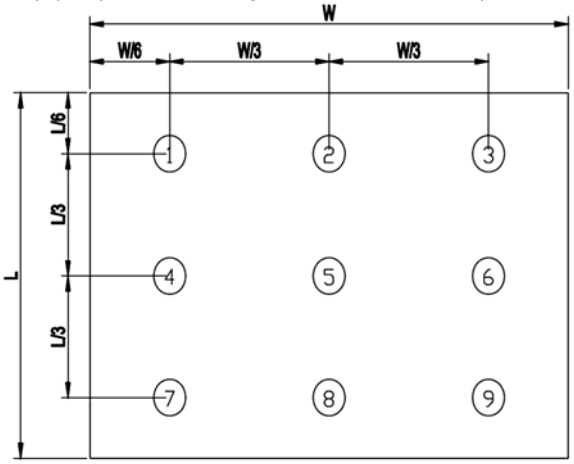
Note 5:
Definition of Color of CIE1931 Coordinate and NTSC Ratio.

Color gamut:

$$S = \frac{\text{Area of RGB triangle}}{\text{Area of NTSC triangle}} \times 100\%$$



Note 6:
The luminance uniformity is calculated by using following formula.
△Bp = Bp (Min.) / Bp (Max.)×100 (%)
Bp (Max.) = Maximum brightness in 9 measured spots
Bp (Min.) = Minimum brightness in 9 measured spots.



Note 7:
Measured the luminance of white state at center point

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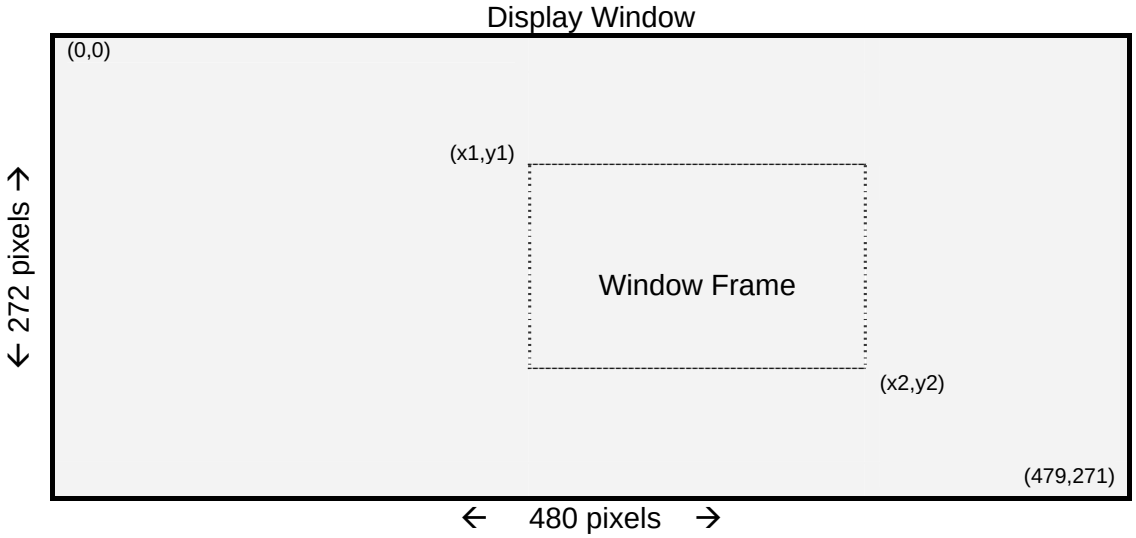
8. Function Specifications

8.1 TFT Controller Functions

8.1.1 Display Memory Addressing

TFT module with 480x272 pixels, using SSD1963, address the display memory with a co-ordinate system as follow.



8.1.2 Command Packet

- Command Packet organizes with “Command Code” followed by “Parameter”
- Command Code and Parameters are 8bit only
- Number of Parameters is depends on Command type
  some of the command followed with no parameter.

Seq.	D/C	/RD	/WR	Lo byte (D7:D0)
1	0	1	↑	Command code
2	1	1	↑	Parameter 1
3	1	1	↑	Parameter 2
4	1	1	↑	Parameter 3
:	:	:	:	:

8.1.3 Data Format

- Display Data is in 24bit format (R:G:B=8:8:8)
- 24bit data built one pixels
- Display Data could be continue write (depends on command and configuration)

D/C	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
1	1	↑	R7	R6	R5	R4	R3	R2	R1	R0
1	1	↑	G7	G6	G5	G4	G3	G2	G1	G0
1	1	↑	B7	B6	B5	B4	B3	B2	B1	B0
1	1	↑	R7	R6	R5	R4	R3	R2	R1	R0
1	1	↑	G7	G6	G5	G4	G3	G2	G1	G0
1	1	↑	B7	B6	B5	B4	B3	B2	B1	B0
:	:	:	:	:	:	:	:	:	:	:

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8.1.4 Command Table

Code (hex)	Command	Description
0x00	nop	No operation
0x01	soft_reset	Software Reset
0x0A	get_power_mode	Get the current power mode
0x0B	get_address_mode	Get the frame buffer to the display panel read order
0x0C	Reserved	Reserved
0x0D	get_display_mode	The SSD1963 returns the Display Image Mode.
0x0E	get_tear_effect_status	Get the Tear Effect status
0x0F	Reserved	Reserved
0x10	enter_sleep_mode	Turn off the panel. This command will pull low the GPIO0. If GPIO0 is configured as normal GPIO or LCD miscellaneous signal with command set_gpio_conf, this command will be ignored.
0x11	exit_sleep_mode	Turn on the panel. This command will pull high the GPIO0. If GPIO0 is configured as normal GPIO or LCD miscellaneous signal with command set_gpio_conf, this command will be ignored.
0x12	enter_partial_mode	Part of the display area is used for image display.
0x13	enter_normal_mode	The whole display area is used for image display.
0x20	exit_invert_mode	Displayed image colors are not inverted.
0x21	enter_invert_mode	Displayed image colors are inverted.
0x26	set_gamma_curve	Selects the gamma curve used by the display panel.
0x28	set_display_off	Blanks the display panel
0x29	set_display_on	Show the image on the display panel
0x2A	set_column_address	Set the column address
0x2B	set_page_address	Set the page address
0x2C	write_memory_start	Transfer image information from the host processor interface to the SSD1963 starting at the location provided by set_column_address and set_page_address
0x2E	read_memory_start	Transfer image data from the SSD1963 to the host processor interface starting at the location provided by set_column_address and set_page_address
0x30	set_partial_area	Defines the partial display area on the display panel
0x33	set_scroll_area	Defines the vertical scrolling and fixed area on display area
0x34	set_tear_off	Synchronization information is not sent from the SSD1963 to the host processor
0x35	set_tear_on	Synchronization information is sent from the SSD1963 to the host processor at the start of VFP
0x36	set_address_mode	Set the read order from frame buffer to the display panel
0x37	set_scroll_start	Defines the vertical scrolling starting point
0x38	exit_idle_mode	Full color depth is used for the display panel
0x39	enter_idle_mode	Reduce color depth is used on the display panel.
0x3A	Reserved	Reserved
0x3C	write_memory_continue	Transfer image information from the host processor interface to the SSD1963 from the last written location
0x3E	read_memory_continue	Read image data from the SSD1963 continuing after the last read_memory_continue or read_memory_start
0x44	set_tear_scanline	Synchronization information is sent from the SSD1963 to the host processor when the display panel refresh reaches the provided scanline
0x45	get_scanline	Get the current scan line
0xA1	read_ddb	Read the DDB from the provided location
0xA8	Reserved	Reserved

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8.1.5 Command Table(continue)

Code (hex)	Command	Description
0xB0	set_lcd_mode_	Set the LCD panel mode and resolution
0xB1	get_lcd_mode	Get the current LCD panel mode, pad strength and resolution
0xB4	set_hori_period	Set front porch
0xB5	get_hori_period	Get current front porch settings
0xB6	set_vert_period	Set the vertical blanking interval between last scan line and next LFRAME pulse
0xB7	get_vert_period	Set the vertical blanking interval between last scan line and next LFRAME pulse
0xB8	set_gpio_conf	Set the GPIO configuration. If the GPIO is not used for LCD, set the direction. Otherwise, they are toggled with LCD signals.
0xB9	get_gpio_conf	Get the current GPIO configuration
0xBA	set_gpio_value	Set GPIO value for GPIO configured as output
0xBB	get_gpio_status	Read current GPIO status. If the individual GPIO was configured as input, the value is the status of the corresponding pin. Otherwise, it is the programmed value.
0xBC	set_post_proc	Set the image post processor
0xBD	get_post_proc	Set the image post processor
0xBE	set_pwm_conf	Set the image post processor
0xBF	get_pwm_conf	Set the image post processor
0xC0	set_lcd_gen0	Set the rise, fall, period and toggling properties of LCD signal generator 0
0xC1	get_lcd_gen0	Get the current settings of LCD signal generator 0
0xC2	set_lcd_gen1	Set the rise, fall, period and toggling properties of LCD signal generator 1
0xC3	get_lcd_gen1	Get the current settings of LCD signal generator 1
0xC4	set_lcd_gen2	Set the rise, fall, period and toggling properties of LCD signal generator 2
0xC5	get_lcd_gen2	Get the current settings of LCD signal generator 2
0xC6	set_lcd_gen3	Set the rise, fall, period and toggling properties of LCD signal generator 3
0xC7	get_lcd_gen3	Get the current settings of LCD signal generator 3
0xC8	set_gpio0_rop	Set the GPIO0 with respect to the LCD signal generators using ROP operation. No effect if the GPIO0 is configured as general GPIO.
0xC9	get_gpio0_rop	Get the GPIO0 properties with respect to the LCD signal generators.
0xCA	set_gpio1_rop	Set the GPIO1 with respect to the LCD signal generators using ROP operation. No effect if the GPIO1 is configured as general GPIO.
0xCB	get_gpio1_rop	Get the GPIO1 properties with respect to the LCD signal generators.
0xCC	set_gpio2_rop	Set the GPIO2 with respect to the LCD signal generators using ROP operation. No effect if the GPIO2 is configured as general GPIO.
Hex Code	Command	Description
0xCD	get_gpio2_rop	Get the GPIO2 properties with respect to the LCD signal generators.
0xCE	set_gpio3_rop	Set the GPIO3 with respect to the LCD signal generators using ROP operation. No effect if the GPIO3 is configured as general GPIO.
0xCF	get_gpio3_rop	Get the GPIO3 properties with respect to the LCD signal generators.
0xD0	set_dbc_conf	Set the dynamic back light configuration
0xD1	get_dbc_conf	Get the current dynamic back light configuration
0xD4	set_dbc_th	Set the threshold for each level of power saving
0xD5	get_dbc_th	Get the threshold for each level of power saving
0xE0	set_pll	Start the PLL. Before the start, the system was operated with the crystal oscillator or clock input
0xE2	set_pll_mn	Set the PLL
0xE3	get_pll_mn	Get the PLL settings
0xE4	get_pll_status	Get the current PLL status
0xE5	set_deep_sleep	Set deep sleep mode
0xE6	set_lshift_freq	Set the LSHIFT (pixel clock) frequency
0xE7	get_lshift_freq	Get current LSHIFT (pixel clock) frequency setting
0xE8	Reserved	Reserved
0xE9	Reserved	Reserved
0xF0	set_pixel_data_interface	Set the pixel data format of the parallel host processor interface
0xF1	get_pixel_data_interface	Get the current pixel data format settings
0xFF	Reserved	Reserved

Note. Please Refer to SSD1963 datasheet for details.

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8.1.6 Hardware Related Parameter

Booster and Power circuit

Internal TFT standBY and Backlight driver are controlled by SSD1963 GPIO0 and GPIO1 respectively. It is necessary to enable them for normal operation via command

Backlight Brightness PWM control

It is suggested to config the backlight brightness control signal as 3kHz PWM signal for best performance.

8.1.7 Startup Program (Example)

```
   RST=1; delayms(10);                                  // wait for all power stable
   RST=0; delayms(1);                                   // reset pulse
   RST=1; delayms(10);                                  // wait till internal reset routine finish

   SdCmd(0xe2); SdData(0x3B); SdData(0x02); SdData(0x04); delayms(10);       // config PLL to 200MHz
   SdCmd(0xe0); SdData(0x01); delayms(10);                                   // enable PLL
   SdCmd(0xe0); SdData(0x03); delayms(10);                                   // switch to use PLL clock

   SdCmd(0x11);                                          // exit_sleep_mode
   SdCmd(0x13);                                          // enter_normal_mode (exit_partial_mode)
   SdCmd(0x20);                                          // exit_invert_mode
   SdCmd(0x38);                                          // exit_idle_mode (using full color)

   SdCmd(0xB8);                                          // set_gpio_conf
      SdData(0x0f);                                      // GPIO[0~3] controlled by host
      SdData(0x01);                                      // GPIO0 as normal GPIO
   SdCmd(0xba); SdData(0x01); delayms(10);               // GPIO[0~3]=0001, enable DC-CD booster
   SdCmd(0xba); SdData(0x03); delayms(10);               // GPIO[0~3]=0011, enable backlight booster

   SdCmd(0xf0); SdData(0x00);                            // set_pixel_data_interface (MCU) 8bit
   SdCmd(0xb0);                                          // set_lcd_mode
      SdData(0x24);                                      // 24bit, disable FRC or dithering, DCLK=rising edge
      SdData(0x20);                                      // HSYNC=active lo, VSYNC=active low, default TFT m
      SdData(0x01); SdData(0xdf);                        // panel size 480-1
      SdData(0x01); SdData(0x0f);                        // panel size 272-1

   SdCmd(0xb4);                                          // set_hori_period
      SdData(0x02); SdData(0x0c);                        // total pulse per line, HT=525-1
      SdData(0x00); SdData(0x2a);                        // horizontal front porch, HPS=41+2-1
      SdData(0x07);                                      // (default), not use
      SdData(0x00); SdData(0x00);                        // (default), not use
      SdData(0x00);                                      // (default), not use

   SdCmd(0xb6);                                          // set_vert_period
      SdData(0x01); SdData(0x1d);                        // total line per frame, VT=286-1
      SdData(0x00); SdData(0x0b);                        // vertical front porch, VPS=10+2-1
      SdData(0x09);                                      // (default), not use
      SdData(0x00); SdData(0x00);                        // (default), not use

   SdCmd(0xe6); SdData(0x00); SdData(0xb8); SdData(0x50);// config PCLK=9.0MHz(PLL@200MHz)

   SdCmd(0x36);                                          // set_address_mode
      SdData(0x00);                                      // top to bottom, left to right, RGB, normal

   SdCmd(0xbe);                                          // set_pwm_conf
      SdData(0x00);                                      // PWM clock set to 3kHz (PLL@200MHz)
      SdData(150);                                       // PWM width at about 60% (150/255)
      SdData(0x01);                                      // C[3]=0, non_DBC control; C[0]=1, enable PWM
      SdData(0xf0);                                      // DBC manual level at middle
      SdData(0x00);                                      // DBC minimum lever at middle
      SdData(0x00);                                      // disable the DBC response delay setting

   SdCmd(0x29);                                          // display on

   SdCmd(0x2c);                                          // write_memory_start
      SdData(0xff); SdData(0xff); SdData(0xff);          // write a white pixel
      SdData(0xff); SdData(0x00); SdData(0x00);          // write a red pixel
      ..........                                         // continue write display data
```

Note. Above example program may need modification to fit correspondent application.

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8.2 Touch Panel Controller Functions

8.2.1 ADS7843 Control Byte

Order of the control bits in the control byte

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
S	A2	A1	A0	MODE	SER/DFR	PD1	PD0

8.2.2 Descriptions of the Control Bits within the Control Byte.

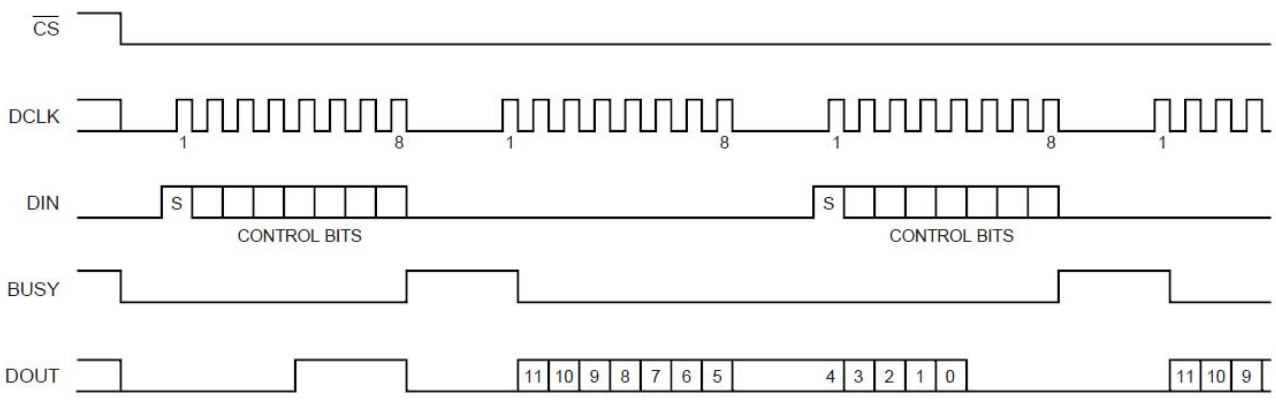
BIT	NAME	DESCRIPTION
7	S	Start Bit. Control byte starts with first HIGH bit on DIN. A new control byte can start every 16th clock cycle in 12-bit conversion mode or every 12th clock cycle in 8-bit conversion mode.
6-4	A2-A0	Channel Select Bits. Along with the SER/DFR bit, these bits control the setting of the multiplexer input, switches, and reference inputs.
3	MODE	12-Bit/8-Bit Conversion Select Bit. This bit controls the number of bits for the following conversion: 12bits (LOW) or 8 bits (HIGH).
2	SER/DFR	Single-Ended/Differential Reference Select Bit. Along with bits A2-A0, this bit controls the setting of the multiplexer input, switches, and reference inputs.
1-0	PD1-PD0	Power-Down Mode Select Bits.

8.2.3 Power-Down Selection.

PD1	PD0	PENIRQ	DESCRIPTION
0	0	Enable	Power-down between conversions. When each conversion is finished, the converter enters a low power mode. At the start of the next conversion,the device instantly powers up to full power.There is no need for additional delays to assure full operation and the very first conversion is valid. The Y– switch is on while in power-down.
0	1	Disable	Same as mode 00, except PENIRQ is disabled.The Y– switch is off while in power-down mode.
1	0	Disable	Reserved for future use.
1	1	Disable	No power-down between conversions, device is always powered.

8.2.4 Conversion Timing

16 Clocks per Conversion, 8-bit Bus Interface. No DCLK Delay Required with Dedicated Serial Port.



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9. Precautions of using LCD Modules

Mounting

- Mounting must use holes arranged in four corners or four sides.
- The mounting structure so provide even force on to LCD module. Uneven force (ex. Twisted stress) should not applied to the module. And the case on which a module is mounted should have sufficient strength so that external force is not transmitted directly to the module.
- It is suggested to attach a transparent protective plate to the surface in order to protect the polarizer. It should have sufficient strength in order to the resist external force.
- The housing should adopt radiation structure to satisfy the temperature specification.
- Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the polarizer at high temperature and the latter causes circuit break by electro-chemical reaction.
- Do not touch, push or rub the exposed polarizers with glass, tweezers or anything harder than HB pencil lead. Never rub with dust clothes with chemical treatment. Do not touch the surface of polarizer for bare hand or greasy cloth.(Some cosmetics deteriorate the polarizer.)
- When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzine. Normal-hexane is recommended for cleaning the adhesives used to attach front / rear polarizers. Do not use acetone, toluene and alcohol because they cause chemical damage to the polarizer.
- Wipe off saliva or water drops as soon as possible. Their long time contact with polarizer

Operating

- The spike noise causes the mis-operation of circuits. It should be within the ±200mV level (Over and under shoot voltage)
- Response time depends on the temperature.(In lower temperature, it becomes longer.)
- Brightness depends on the temperature. (In lower temperature, it becomes lower.) And in lower temperature, response time(required time that brightness is stable after turned on) becomes longer.
- Be careful for condensation at sudden temperature change. Condensation makes damage to polarizer or electrical contacted parts. And after fading condensation, smear or spot will occur.
- When fixed patterns are displayed for a long time, remnant image is likely to occur.
- Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimized the interference

Electrostatic Discharge Control

Since a module is composed of electronic circuits, it is not strong to electrostatic discharge. Make certain that treatment persons are connected to ground through wrist band etc. And don't touch interface pin directly.

Strong Light Exposure

Strong light exposure causes degradation of polarizer and color filter.

Storage

When storing modules as spares for a long time, the following precautions are necessary.

- Store them in a dark place. Do not expose the module to sunlight or fluorescent light. Keep the temperature between 5°C and 35°C at normal humidity.
- The polarizer surface should not come in contact with any other object. It is recommended that they be stored in the container in which they were shipped.

Protection Film

- When the protection film is peeled off, static electricity is generated between the film and polarizer. This should be peeled off slowly and carefully by people who are electrically grounded and with well ion-blown equipment or in such a condition, etc.
- The protection film is attached to the polarizer with a small amount of glue. If some stress is applied to rub the protection film against the polarizer during the time you peel off the film, the glue is apt tore main on the polarizer. Please carefully peel off the protection film without rubbing it against the polarizer.
- When the module with protection film attached is stored for a long time, sometimes there remains a very small amount of glue still on the polarizer after the protection film is peeled off.
- You can remove the glue easily. When the glue remains on the polarizer surface or its vestige is recognized, please wipe them off with absorbent cotton waste or other soft material like chamois soaked with normal-hexane.

Transportation

The LCD modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.

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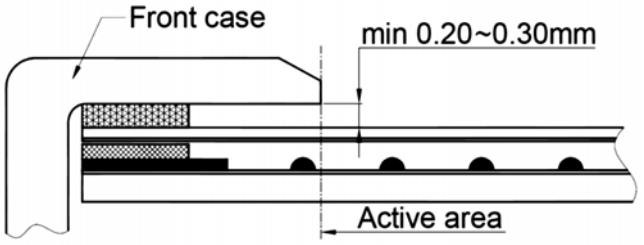
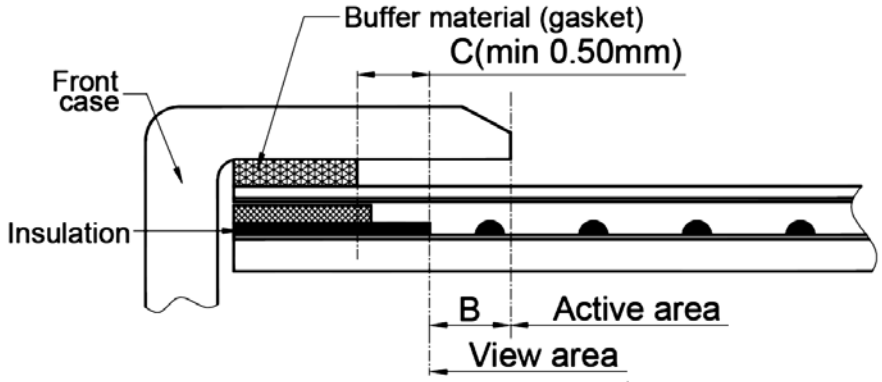
附录：Touch panel Design Precautions

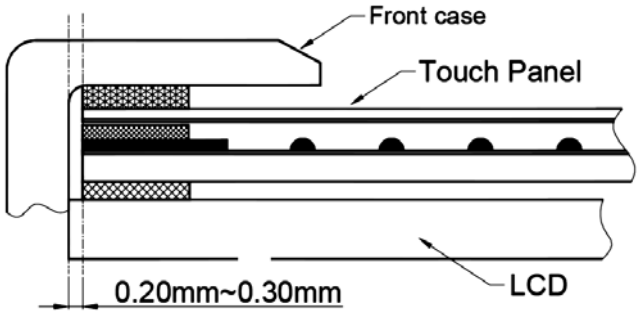
1. It should prevent front case touching the touch panel Active Area (A.A.) to prevent abnormal touch.
   It should left gab (e.g. 0.2~0.3mm) in between.



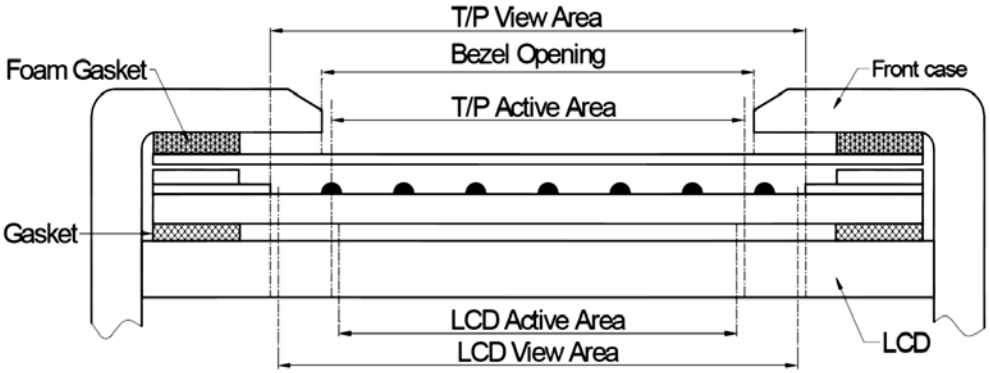
2. Outer case design should take care about the area outside the A.A.
   Those areas contain circuit wires which is having different thickness. Touching those areas could deform the ITO film. As a result case the ITO cold be damaged and shorten its lifetime.
   It is suggested to protect those areas with gasket (between the front case and the touch panel).
   The suggested figures are B≥0.50mm; C≥0.50mm。



3. The front case side wall should keep space (e.g. 0.2 ~ 0.3mm) from the touch panel.



4. In general design,
   touch panel V.A. should be bigger than the LCD V.A.
   and touch panel A.A. should be bigger than the LCD A.A.



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