SONY

CXA2022S

I²C Bus Sound Processor for TV

Description

The CXA2022S is a bipolar IC designed as an I²C bus control sound processor for TV. This IC has simulate stereo, surround, tone control, balance, volume, muting, AGC and other functions.

Features

- Allows control by I²C bus
- Employs a special surround system to prevent "vocal missing" in the surround mode
- Adopts an AGC circuit to absorb the difference in sound level between input sources and improves S/N ratio of hearing characteristics

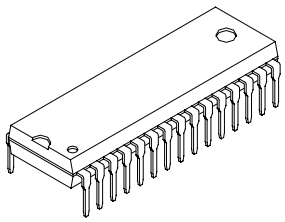
Absolute Maximum Ratings

• Supply voltage	V_{CC}	14	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation	P_D	1.25	W

Recommended Operating Condition

Supply voltage	8 to 13	V

30 pin SDIP (Plastic)



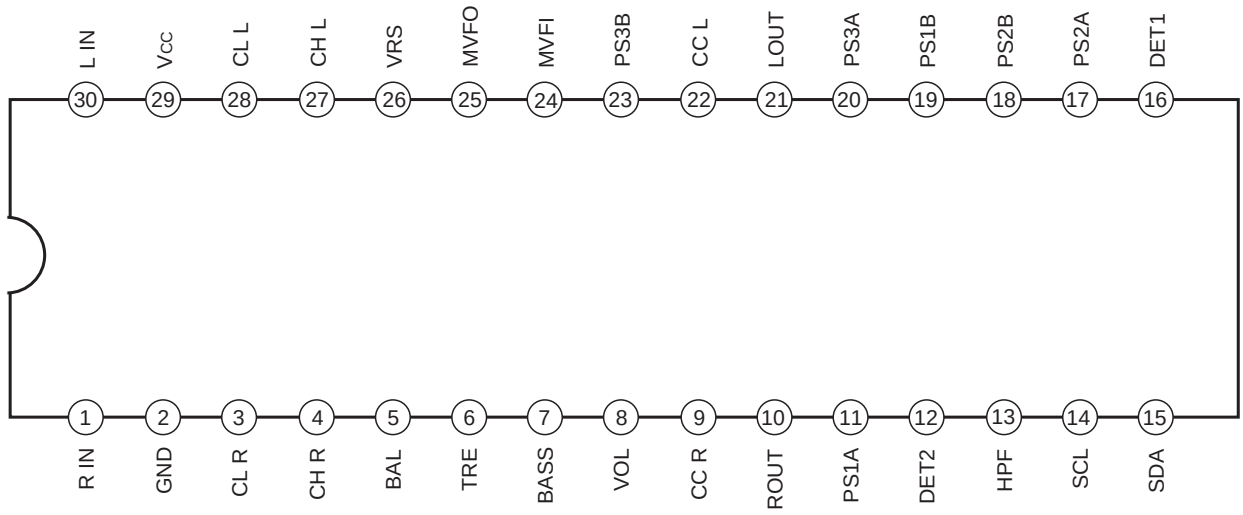
Structure

Bipolar silicon monolithic IC

Applications

TVs

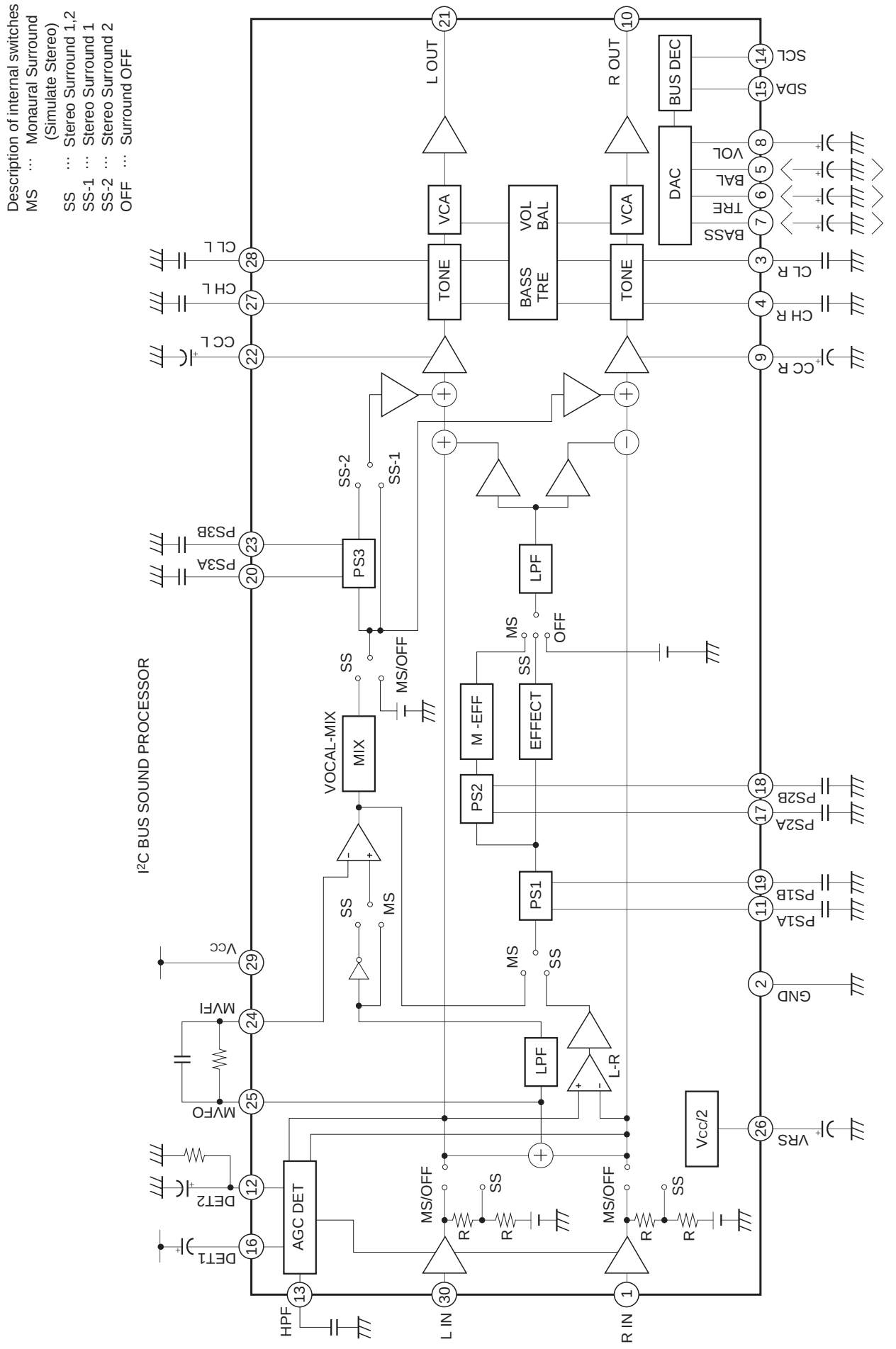
Pin Configuration



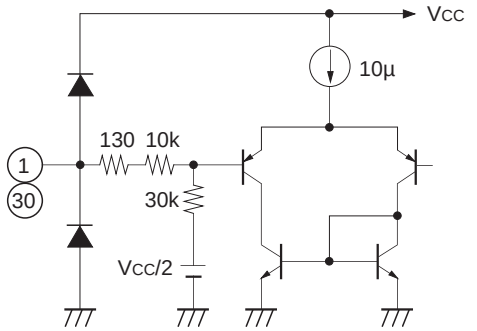
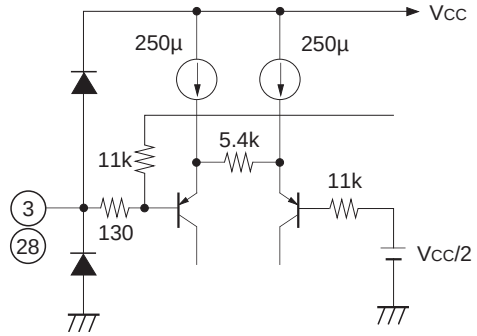
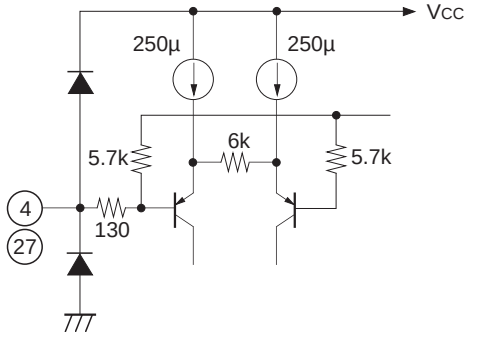
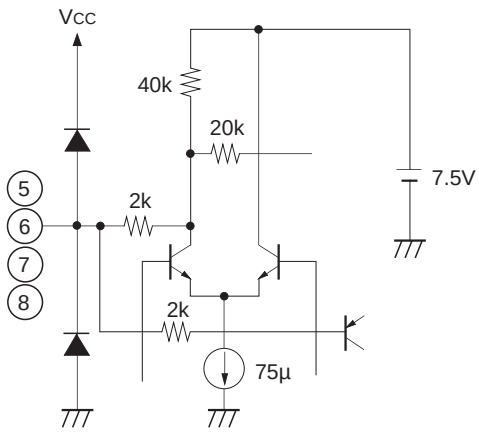
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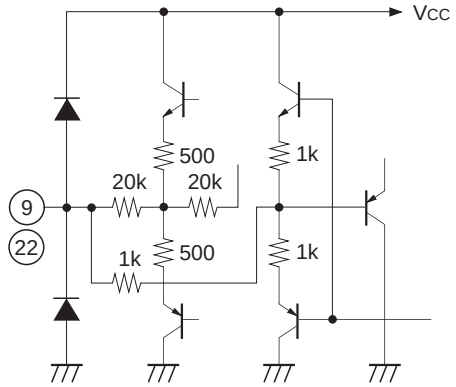
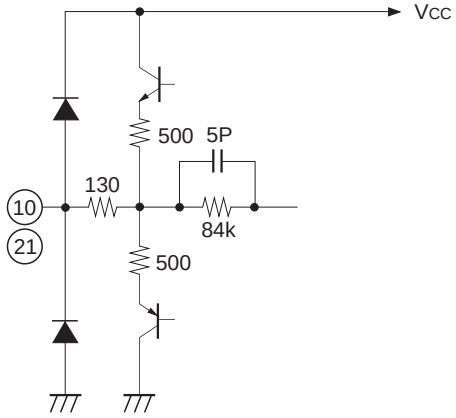
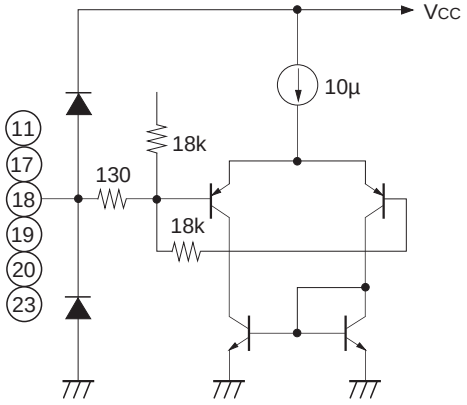
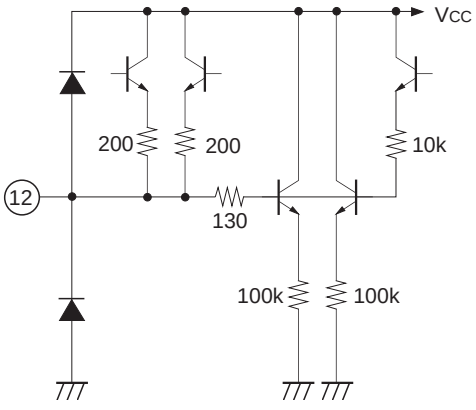
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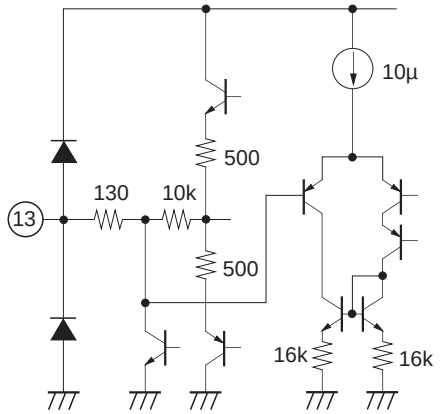
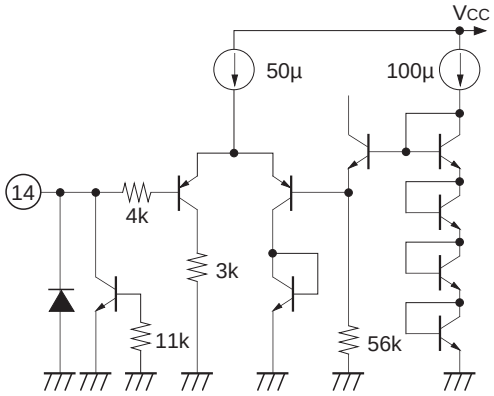
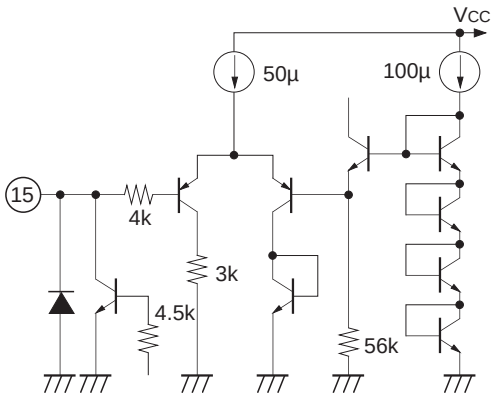
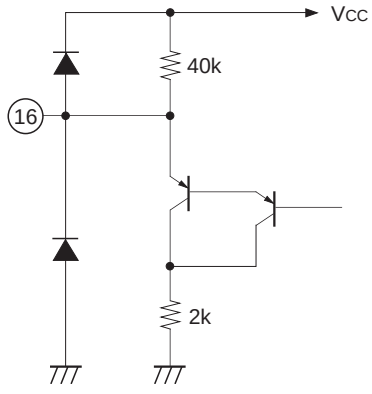
Block Diagram

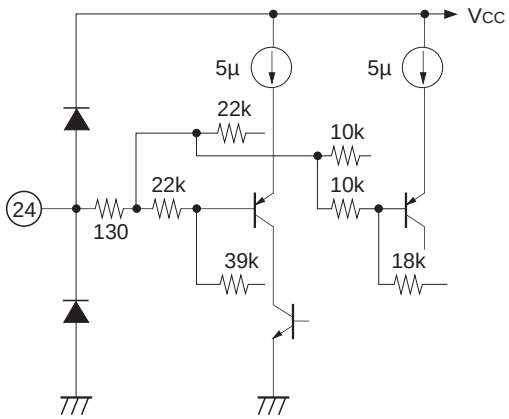
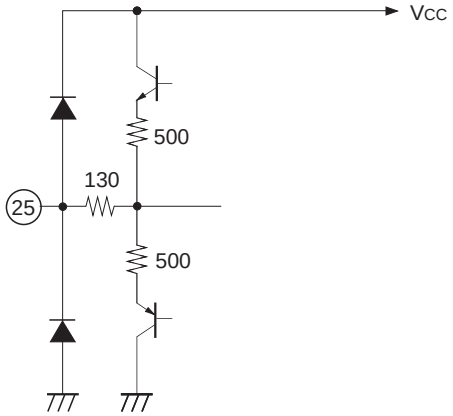
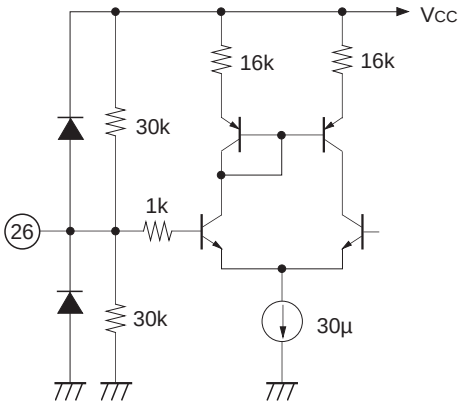


Pin Description (Ta = 25°C, Vcc = 12V)

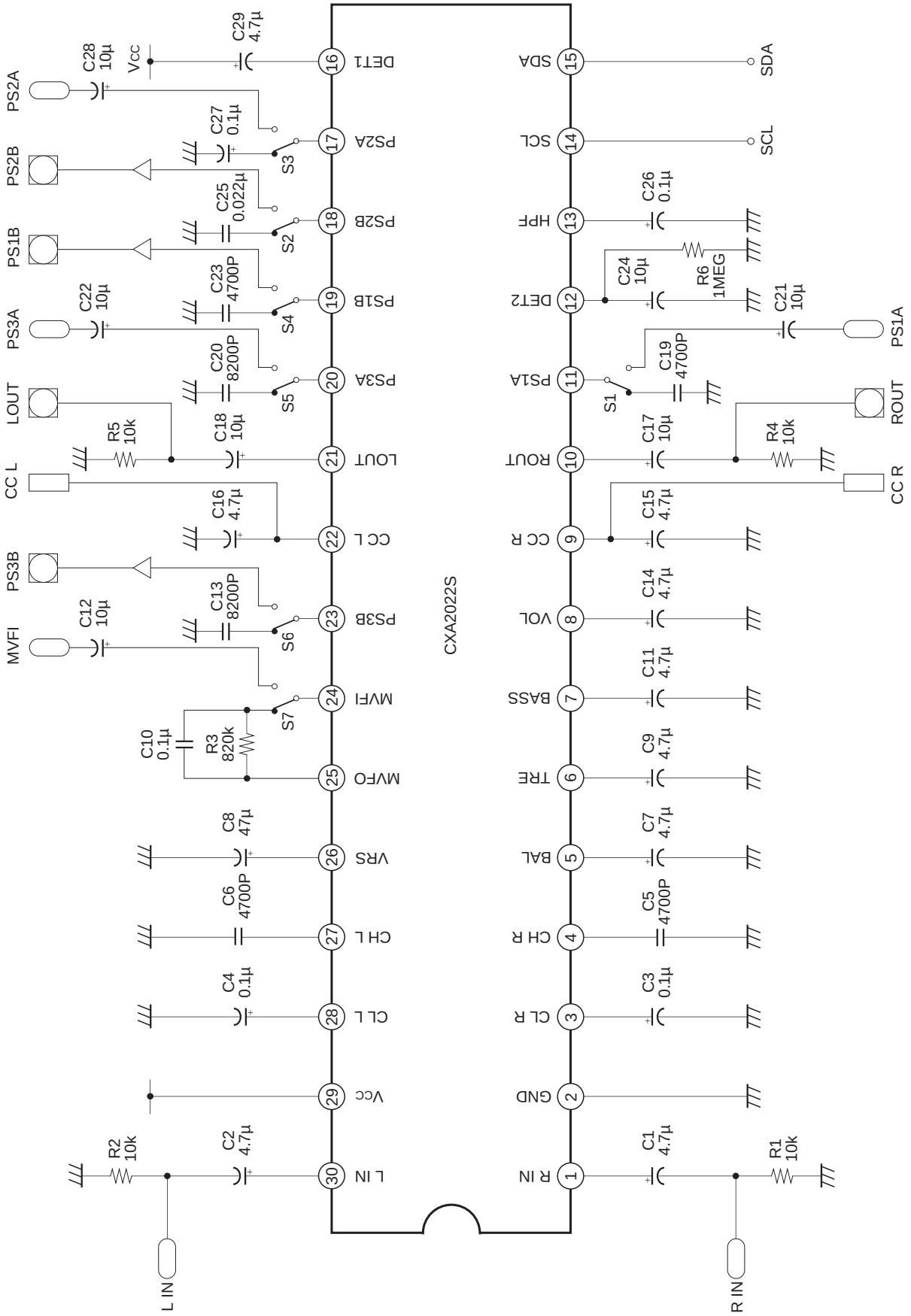
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
1 30	R IN L IN	6V		Input pins.
2	GND	0V		GND
3 28	CL R CL L	6V		External pins for LPF capacitance (BASS).
4 27	CH R CH L	6V		External pins for HPF capacitance (TREBLE).
5 6 7 8	BAL TRE BASS VOL	4.5V		DAC output pins. Connect LPF capacitance of DAC. Internal impedance is approximetely 20kΩ.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
9 22	CC R CC L	6V		DC-cut pins for L and R. Internal impedance is approximately 20kΩ.
10 21	ROUT LOUT	6V		Output pins.
11 17 18 19 20 23	PS1A PS2A PS2B PS1B PS3A PS3B	6V		External capacitance pins for surround phase-shifter. Internal impedance is approximately 18kΩ.
12	DET2			AGC detector output and control pin.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
13	HPF	6V		HPF external capacitance pin of AGC.
14	SCL			I²C bus clock line pin.
15	SDA			I²C bus data line pin.
16	DET1	7.8V		AGC detector output pin. Connect capacitance for setting time constant.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
24	MVFI	6V		External pin for surround filter.
25	MVFO	6V		External pin for surround filter.
26	VRS	6V		Vcc/2 reference voltage pin.
29	Vcc	12V		Power supply.

Electrical Characteristics Measurement Circuit



Control Register Table (SLAVE ADDRESS = 82H)

DATA							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
VOLUME (00)						MUTE (0)	AGC (0)
BASS (00)					*	MODE (00)	
TREBLE (00)					*		
BALANCE (00)						*	
SURR-EFFECT (00)				MONO-EFFECT (00)			
VOCAL-MIX (00)				*			

(Power ON setting value)

AGC : 0 = OFF/1 = ON
MUTE : 0 = OFF/1 = ON

MODE : 00 = Surround OFF
: 01 = Simulate Stereo
: 10 = Stereo Surround 1
: 11 = Stereo Surround 2

* Undefined

Description of Register

- VOLUME: Common to both L and R channels
  0 = Minimum
  3F = Maximum

- MUTE: MUTE switch
  0 = Mute OFF
  1 = Mute ON (muting state)

- AGC: AGC switch
  0 = AGC OFF
  1 = AGC ON

- BASS: Low frequency control
  0 = Minimum
  10 = Typical
  1F = Maximum

- MODE: Surround mode setting
  00 = Surround OFF
  01 = Simulate Stereo (Monaural Surround)
  10 = Stereo Surround 1
  11 = Stereo Surround 2

- TREBLE: High frequency control
  00 = Minimum
  10 = Typical
  1F = Maximum

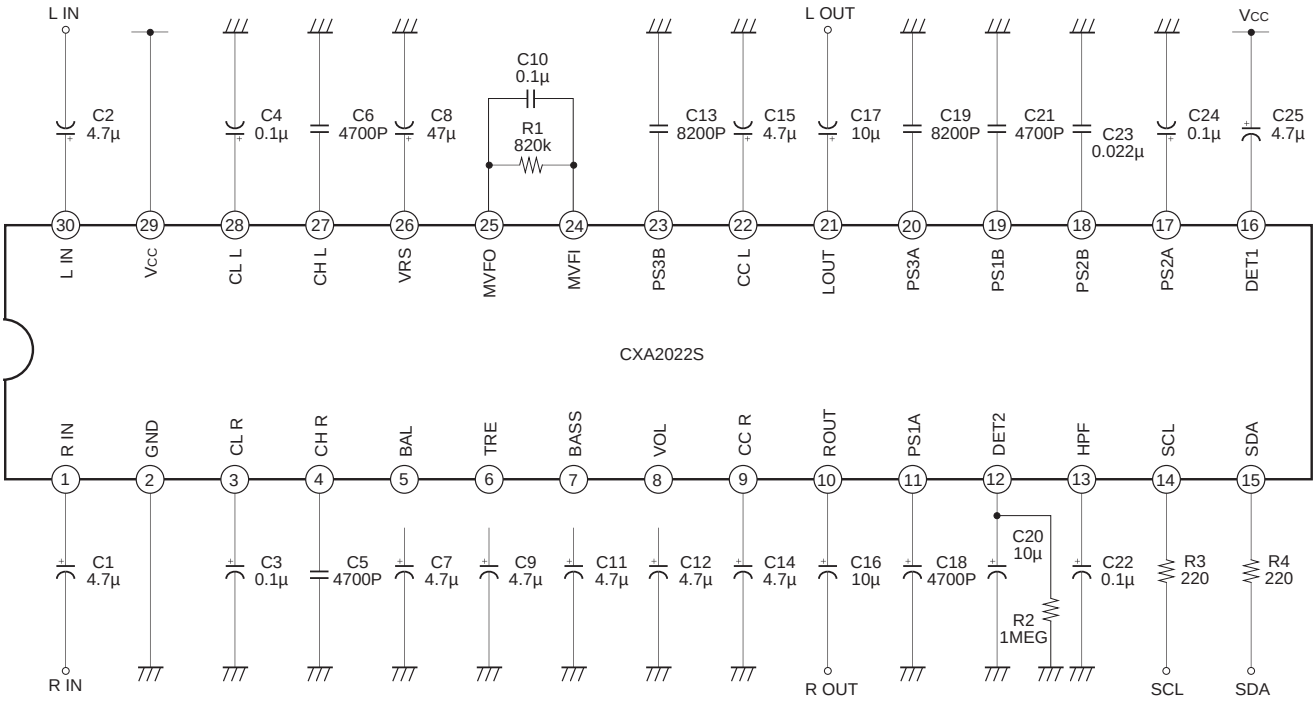
- BALANCE: Balance control for L and R channels
  00 = L channel (Minimum), R channel (Maximum)
  20 = Typical
  3F = L channel (Maximum), R channel (Minimum)

- SURR-EFFECT: Effect setting for Stereo Surround 1 and 2
  0 = Minimum
  8 = Typical
  F = Maximum

- MONO-EFFECT: Effect setting for Simulate Stereo (Monaural Surround)
  0 = Minimum
  F = Maximum

- VOCAL-MIX: Addition amount setting of middle frequency for Stereo Surround 1 and 2
  0 = Minimum
  8 = Typical
  F = Maximum

Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Electrical Characteristics

(Ta = 25°C, V_{CC} = 12V)

No.	Measurement item	Signal	Input conditions										Input point	Input signal	SW set to ON	Measure-ment point	Remarks	Min.	Typ.	Max.	Unit
			VOL	MUTE	AGC	BASS	MODE	TRE	BAL	S-EFF	M-EFF	V-MIX									
1	Current consumption	I_{CC}	3F	0	0	10	0	10	20	8	8	8						20	35	55	mA
2	FLAT L, R	$V_{F\,L,\,R}$	↓										L-IN R-IN	1kHz 2.4Vrms		LOUT ROUT	REF: INPUT	–2.0	0	2.0	dB
3	REF, Level L, R	$V_{R\,L,\,R}$	20											↓			↓	–17	–14	–11	dB
4	VOL MIN L, R	$V_{MIN\,L,\,R}$	0															—	—	–70	dB
5	FLAT f characteristics 100Hz	$V_{LF\,L,\,R}$	20											100Hz 2.4Vrms			REF: $V_{R\,L,\,R}$	–1.5	0	1.5	dB
6	FLAT f characteristics 10kHz	$V_{HF\,L,\,R}$				↓		↓						10kHz 2.4Vrms				–1.5	0	1.5	dB
7	BASS BOOST 100Hz	$V_{BST\,LF}$				1F		1F						100Hz 2.4Vrms				8.5	11	13.5	dB
8	TREBLE BOOST 10kHz	$V_{BST\,HF}$				↓		↓						10kHz 2.4Vrms				8.5	11	13.5	dB
9	BASS CUT 100Hz	$V_{CUT\,LF}$				0		0						100Hz 2.4Vrms				–13.5	–11	–8.5	dB
10	TREBLE CUT 10kHz	$V_{CUT\,HF}$				↓		↓	↓					10kHz 2.4Vrms		↓		–13.5	–11	–8.5	dB
11	BALANCE BOOST L	$V_{BAL\,BST\,L}$				10		10	3F					1kHz 2.4Vrms		LOUT		0	1.2	2.0	dB
12	BALANCE CUT L	$V_{BAL\,CUT\,L}$				↓		↓	0					↓		↓		—	—	–30	dB
13	BALANCE BOOST R	$V_{BAL\,BST\,R}$				↓		↓	↓					↓		ROUT		0	1.2	2.0	dB
14	BALANCE CUT R	$V_{BAL\,CUT\,R}$	↓			↓		↓	3F					↓		↓	↓	—	—	–30	dB
15	Distortion L, R	Vdist	3F	↓	↓	↓	↓	↓	20	↓	↓	↓	↓	↓		LOUT ROUT		—	—	2.0	%

No.	Measurement item	Signal	Input conditions										Input point	Input signal	SW set to ON	Measure-ment point	Remarks	Min.	Typ.	Max.	Unit
			VOL	MUTE	AGC	BASS	MODE	TRE	BAL	S-EFF	M-EFF	V-MIX									
16	Mute L, R	$V_{MT\ L,\ R}$	3F	1	0	10	0	10	20	8	8	8	L-IN R-IN	1kHz 2.4Vrms		LOUT ROUT	REF: INPUT	—	—	–70	dB
17	Crass-Talk L → R	$V_{CT\ L,\ R}$		0									L-IN			ROUT	REF: V_{FR}	—	—	–70	dB
18	Crass-Talk R → L	$V_{CT\ R,\ L}$											R-IN			LOUT	REF: V_{FL}	—	—	–70	dB
19	NOISE LEVEL L, R	$V_{NOI\ L,\ R}$														LOUT ROUT		—	—	–60	dBm
20	AGC BOOST L, R	$V_{GCB\ L,\ R}$			0 ↓ 1								L-IN R-IN	1kHz 10mVrms			REF: AGC-OFF (0)	0.5	3	5.5	dB
21	AGC BOOST L, R	$V_{GCB2\ L,\ R}$			0 ↓ 1									1kHz 50mVrms			REF: AGC-OFF (0)	5	7	10	dB
22	AGC NULL L, R	$V_{GCN\ L,\ R}$			0 ↓ 1									1kHz 160mVrms			REF: AGC-OFF (0)	–2.5	–0.5	2	dB
23	AGC CUT L, R	$V_{GCC\ L,\ R}$			0 ↓ 1									1kHz 2Vrms			REF: AGC-OFF (0)	–24	–20	–16	dB
24	MONO FIL 100HZ	$M_{FL\ L}$			0		1							100Hz 1.25Vrms	SW2	PS2B	REF: INPUT	–11	–8.5	–6	dB
25	MONO FIL 500HZ	$M_{FL\ M}$												500Hz 1.25Vrms				–18	–15.5	–13	dB
26	MONO FIL 10kHz	$M_{FL\ H}$												10kHz 1.25Vrms				–1.5	1.0	3.5	dB
27	MS MIX LEVEL L, R	$M_{MX\ L,\ R}$									F		PS1A	1kHz 350mVrms	SW1	LOUT ROUT		13	16	19	dB
28	SS DIF GAIN L	$S_{DG\ L}$					2				8		L-IN	1kHz 2.5Vrms	SW4	PS1B		–4	–2	0	dB
29	SS DIF GAIN R	$S_{DG\ R}$					3						R-IN					–4	–2	0	dB
30	SS MIX LEVEL L	$S_{MX\ L}$					2			F			PS1A	1kHz 350mVrms	SW1	LOUT		13	16	19	dB

No.	Measurement item	Signal	Input conditions										Input point	Input signal	SW set to ON	Measure-ment point	Remarks	Min.	Typ.	Max.	Unit
			VOL	MUTE	AGC	BASS	MODE	TRE	BAL	S-EFF	M-EFF	V-MIX									
31	SS MIX LEVEL R	$S_{MX\ R}$	3F	0	0	10	3	10	20	F	8	8	PS1A	1kHz 350mVrms	SW1	ROUT	REF: INPUT	13	16	19	dB
32	V-FIL 100HZ	$V_{FIL\ L}$					2			8		F	L-IN R-IN	100Hz 2.5Vrms	SW6	PS3B		–7.5	–5	–2.5	dB
33	V-FIL 1kHz	$V_{FIL\ M}$					3							1kHz 2.5Vrms				–3	–0.5	2	dB
34	V-FIL 10kHz	$V_{FIL\ H}$					2							10kHz 2.5Vrms				–10.5	–8	–5.5	dB
35	V-MIX L, R	$V_{MX\ L,\ R}$											MVFI	1kHz 500mVrms	SW7	LOUT ROUT		10.5	13.5	16.5	dB
36	SS2-MIX	$SS2_{MX}$					3					8	PS3A		SW5	LOUT		11	14	17	dB
37	DC OFF-Set OFF → MS-L, R	DO_{OM}					0 → 1				F					LOUT ROUT	REF: MODE0	–150	0	150	mV
38	DC OFF-Set OFF → SS1-L, R	$DO_{OSS1L,\ R}$					0 → 2											–150	0	150	mV
39	DC OFF-Set OFF → SS2-L	DO_{OSS2}					0 → 3									LOUT		–150	0	150	mV
40	DC OFF-Set SS2 → MS-L, R	$DO_{SS2M\ L,\ R}$					3 → 1									LOUT ROUT	REF: MODE3	–150	0	150	mV
41	DC OFF-Set SS1 → MS-L	DO_{SS1M}					2 → 1									LOUT	REF: MODE2	–150	0	150	mV
42	VOL MIN NOISE L, R	$V_{MINNO\ L,\ R}$	0				0									LOUT ROUT	30kHz LPF	—	–92	–85	dBm

Description of Operation

- AGC circuit
  The AGC circuit is provided at the input. When AGC is set to ON, this circuit is 0dB for small signal input, boosts for medium signal input, and achieves gain reduction for large signal input. The sound level defference between input sources can be absorbed at this circuit.

- Surround circuit
  The surround circuit provides three modes; MONO (Simulate Stereo), STEREO-1 and STEREO-2.

  MONO mode
  L + R signals, passed through the mono filter and then through four stages of phase shifters (PS1A, PS1B, PS2A, PS2B) and 9kHz LPF, are added to L and R channels at opposite phase to each other.
  The surround effect can be changed by the MONO-EFFECT.

  STEREO-1 mode
  L-R signals, passed through two stages of phase shifters (PS1A, PS1B) and 9kHz LPF, are added to L and R channels at opposite phase to each other. The surround effect can be changed by the SURR-EFFECT. In addition, L + R signals passed through the middle frequency BPF (1kHz BPF) are added to L and R channels at in-phase to each other to prevent "vocal missing" in the surround mode. The addition amount of middle frequency can be changed by the VOCAL-MIX.

  STEREO-2 mode
  L-R signals, passed through two stages of phase shifters (PS1A, PS1B) and 9kHz LPF, are added to L and R channels at opposite phase to each other. The surround effect can be changed by the SURR-EFFECT. In addition, L + R signals passed through the middle frequency BPF (1kHz BPF) are added to R channel, and the middle frequency signals passed further through two stages of phase shifters (PS3A, PS3B) are added to the L channel. The addition amount of middle frequency (L and R) can be changed by the VOCAL-MIX.

Phase Shifter

Each of the phase shifters PS1, PS2 and PS3 consists of two stages of phase shifters (A, B). The transfer function for a stage of phase shifter is expressed by the following equation.

$$V_O = \frac{1 - SCR}{1 + SCR} \text{ Vin}$$

R: Internal resistance ≈ 18kΩ, C: External capacitance

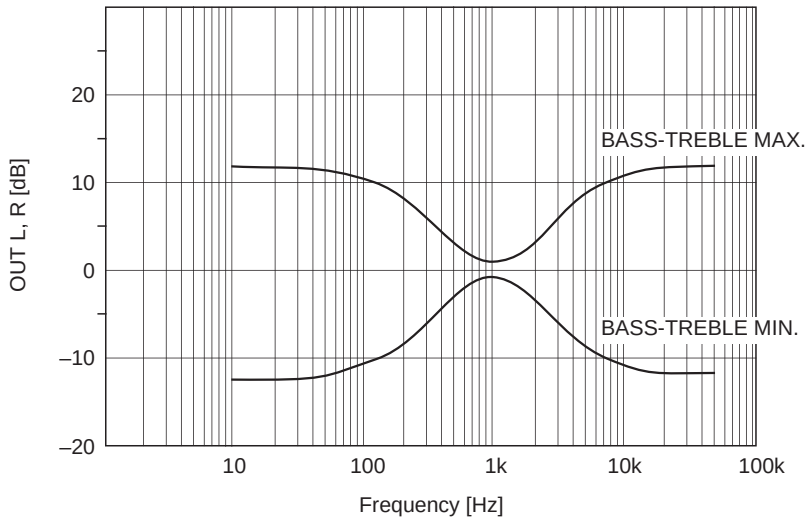
- TONE circuit
  Provides tone controls for BASS and TREBLE. The external capacitance of C_L for BASS and C_H for TREBLE can determine the characteristics. The number of steps is 32.

- BALANCE and VOLUME circuit
  Provides controls for BALANCE and VOLUME. the number of steps is 64 each.

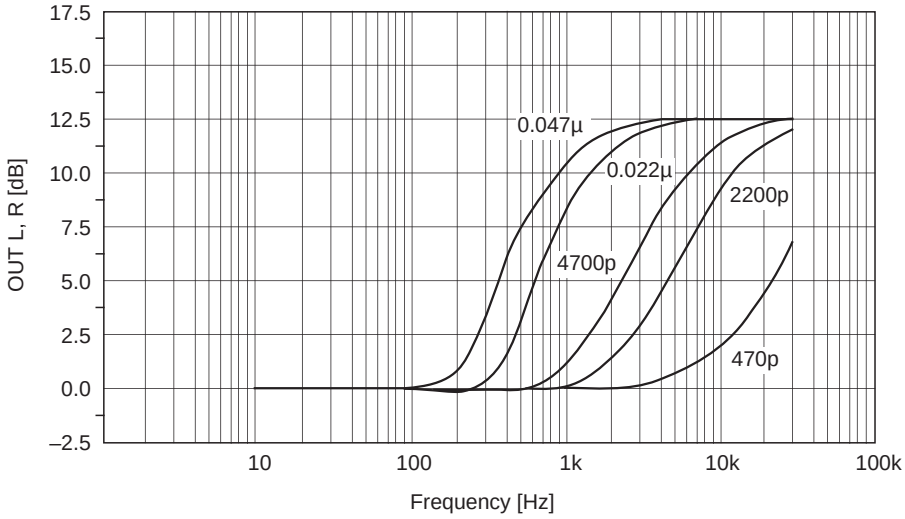
- DAC circuit
  Provides controls for BASS, TREBLE, VOLUME and BALANCE. The internal impedance is approximately 20kΩ and the LPF capacitance is used externally.

Example of Representative Characteristics

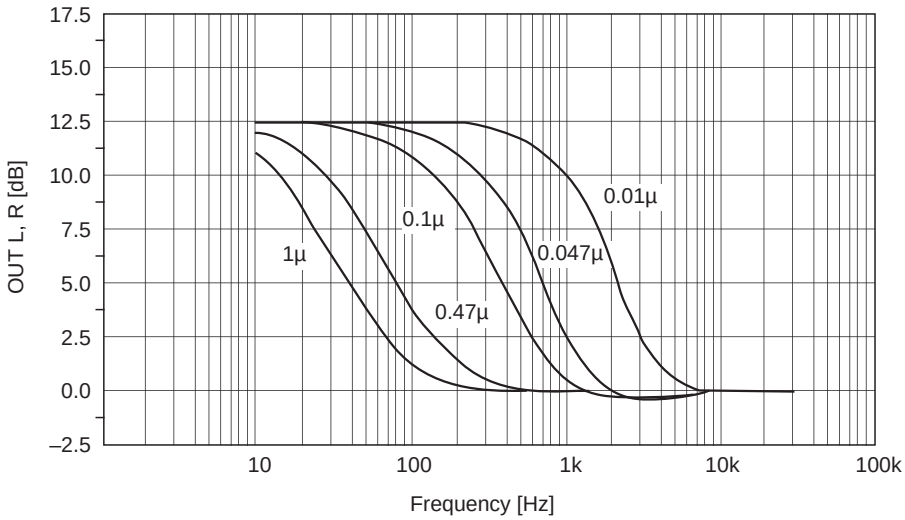
TONE characteristics



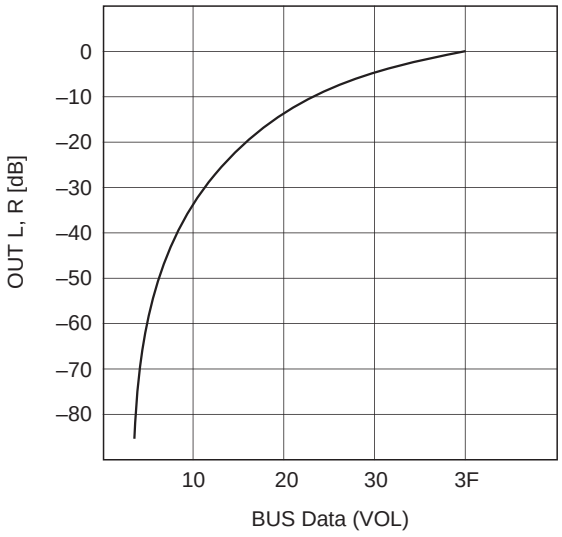
CH. vs. TREBLE-CONTROL (MAX)



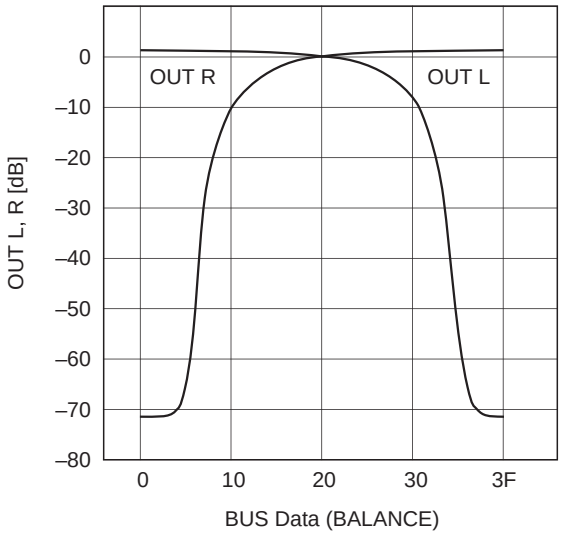
CH. vs. BASS-CONTROL (MAX)



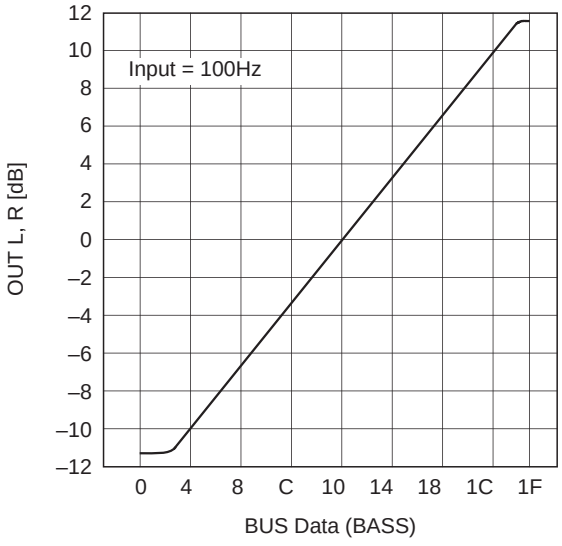
VOL CONTROL characteristics



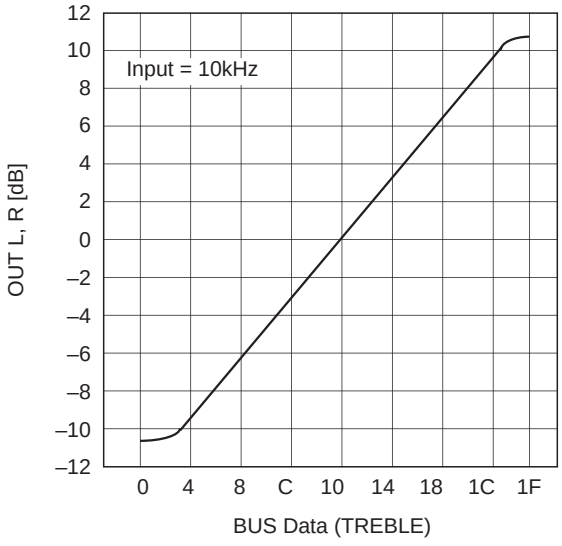
BALANCE CONTROL characteristics



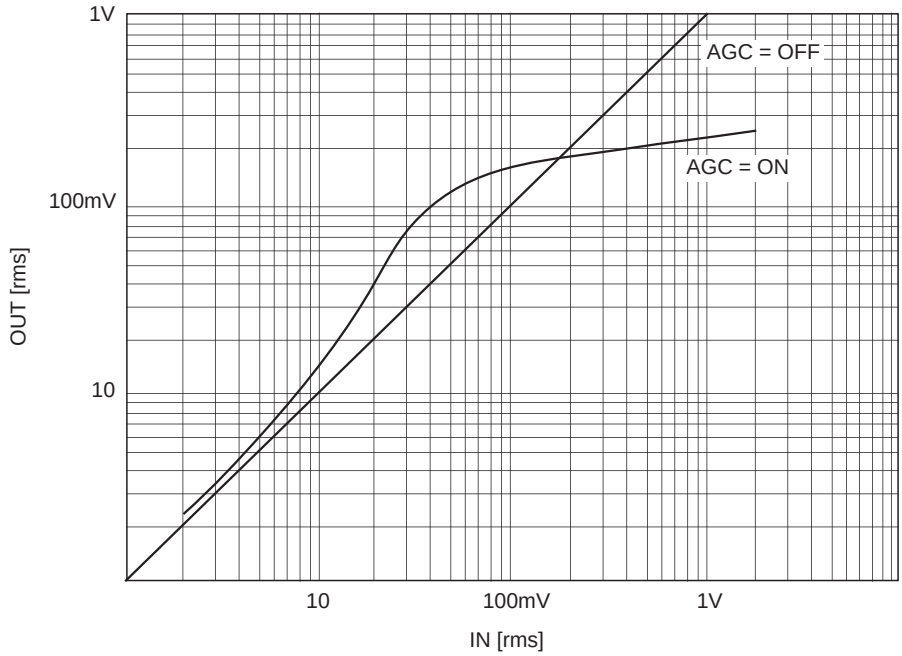
BASS CONTROL characteristics



TREBLE CONTROL characteristics

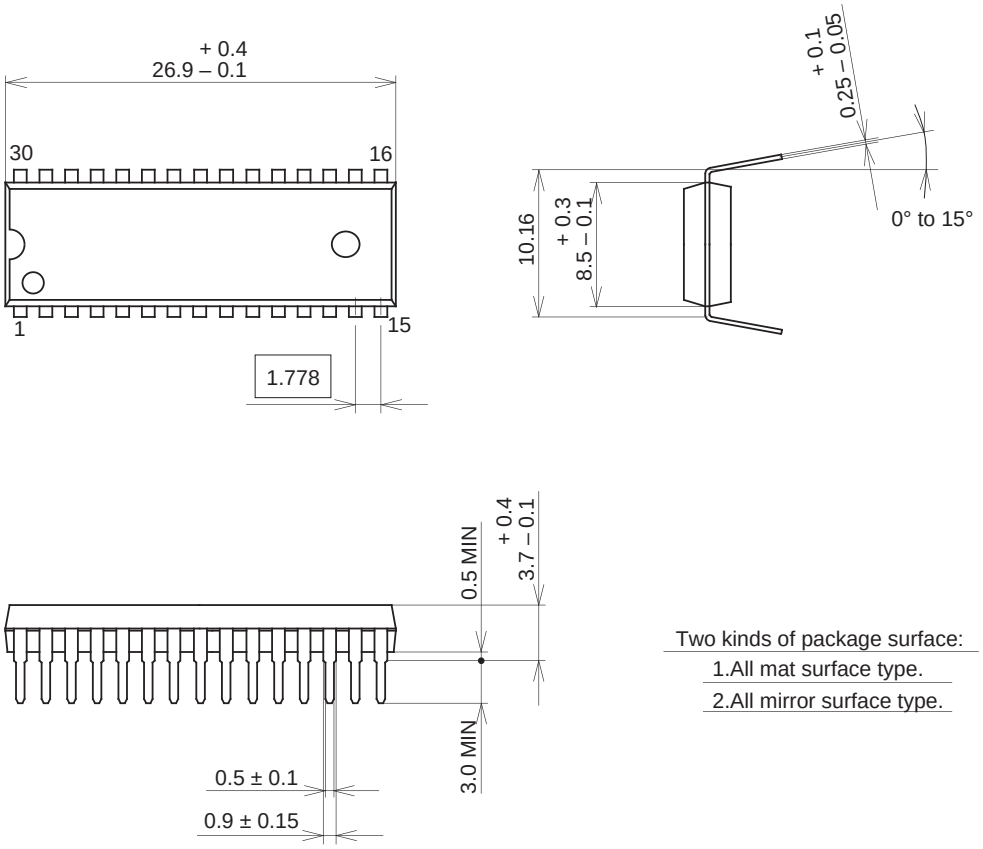


AGC characteristics



Package Outline Unit : mm

30PIN SDIP (PLASTIC)



Two kinds of package surface:
1.All mat surface type.
2.All mirror surface type.

SONY CODE	SDIP-30P-01
EIAJ CODE	SDIP030-P-0400
JEDEC CODE	————

PACKAGE STRUCTURE

MOLDING COMPOUND	EPOXY RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	1.8g

NOTE : PALLADIUM PLATING
This product uses S-PdPPF (Sony Spec.-Palladium Pre-Plated Lead Frame).