TUSB8020B Two-Port USB 3.0 Hub

1 Features

- Two-Port USB 3.0 Compliant Hub, USBIF TID#330000057
- USB 2.0 Hub Features
  - Multi-Transaction Translator (MTT) Hub: Two Transaction Translators
  - Four Asynchronous Endpoint Buffers Per Transaction Translator
- Supports Battery Charging
  - CDP Mode (Upstream Port Connected)
  - DCP Mode (Upstream Port Unconnected)
  - DCP Mode Complies With Chinese Telecommunications Industry Standard YD/T 1591-2009
- Support D+/D– Divider Mode
- Supports Operation as a USB 3.0 or USB 2.0 Compound Device
- Per Port or Ganged Power Switching and Overcurrent Notification Inputs
- OTP ROM, Serial EEPRO,M or I^2C/SMBus Slave Interface for Custom Configurations:
  - VID and PID
  - Port Customizations
  - Manufacturer and Product Strings (not by OTP ROM)
  - Serial Number (not by OTP ROM)
- Application Feature Selection Using Terminal Selection or EEPROM/ or I^2C/SMBus Slave Interface
- Provides 128-Bit Universally Unique Identifier (UUID)
- Supports On-Board and In-System OTP/EEPROM Programming Through the USB 2.0 Upstream Port
- Single Clock Input, 24-MHz Crystal or Oscillator
- No Special Driver Requirements; Works Seamlessly on any Operating System With USB Stack Support
- 48-Pin HTQFP Package (PHP)

2 Applications

- Computer Systems
- Docking Stations
- Monitors
- Set-Top Boxes

3 Description

The TUSB8020B is a two-port USB 3.0 compliant hub. It provides simultaneous SuperSpeed USB and high-speed/full-speed connections on the upstream port and provides SuperSpeed USB, high-speed, full-speed, or low-speed connections on the downstream ports. When the upstream port is connected to an electrical environment that only supports high-speed or full-speed/low-speed connections, SuperSpeed USB connectivity is disabled on the downstream ports. When the upstream port is connected to an electrical environment that only supports full-speed/low-speed connections, SuperSpeed USB and high-speed connectivity are disabled on the downstream ports.

The TUSB8020B supports per port or ganged power switching and overcurrent protection.

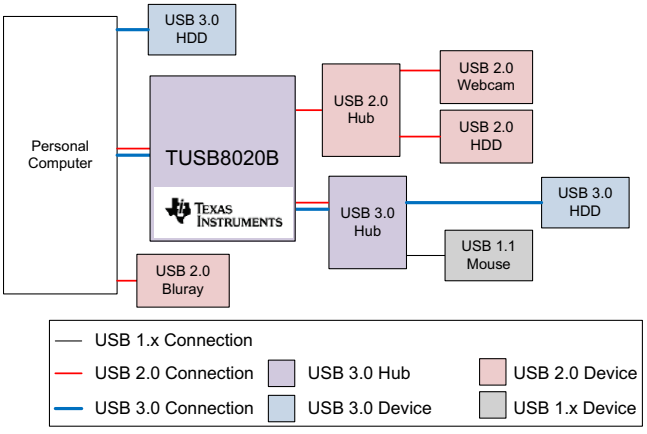
An individually port power controlled hub switches power on or off to each downstream port as requested by the USB host. Also when an individually port power controlled hub senses an overcurrent event, only power to the affected downstream port will be switched off.

A ganged hub switches on power to all its downstream ports when power is required to be on for any port. The power to the downstream ports is not switched off unless all ports are in a state that allows power to be removed. Also when a ganged hub senses an overcurrent event, power to all downstream ports will be switched off.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TUSB8020B	HTQFP (48)	7.00 mm × 7.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



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4 Revision History

Changes from Original (July 2014) to Revision A **Page**

- Changed device status to production data ... 1

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5 Description (continued)

The TUSB8020B downstream ports provide support for battery charging applications by providing battery charging connected downstream port (CDP) handshaking support. It also supports a dedicated charging port (DCP) mode when the upstream port is not connected. The DCP mode supports USB devices which support the USB Battery Charging and the Chinese Telecommunications Industry Standard YD/T 1591-2009. In addition, an automatic mode provides transparent support for BC devices and devices supporting Divider Mode charging solutions when the upstream port is unconnected.

The TUSB8020B provides terminal strap configuration for some features including battery charging support, and also provides customization though OTP ROM, I^2C EEPROM or through an I^2C/SMBus slave interface for PID, VID, and custom port and phy configurations. Custom string support is also available when using an I^2C EEPROM or the I^2C/SMBus slave interface.

The device is available in a 48-pin HTQFP package and is offered in a commercial version (TUSB8020B) for operation over the temperature range of 0°C to 70°C and in an industrial version (TUSB8020BI) for operation over the temperature range of –40°C to 85°C.

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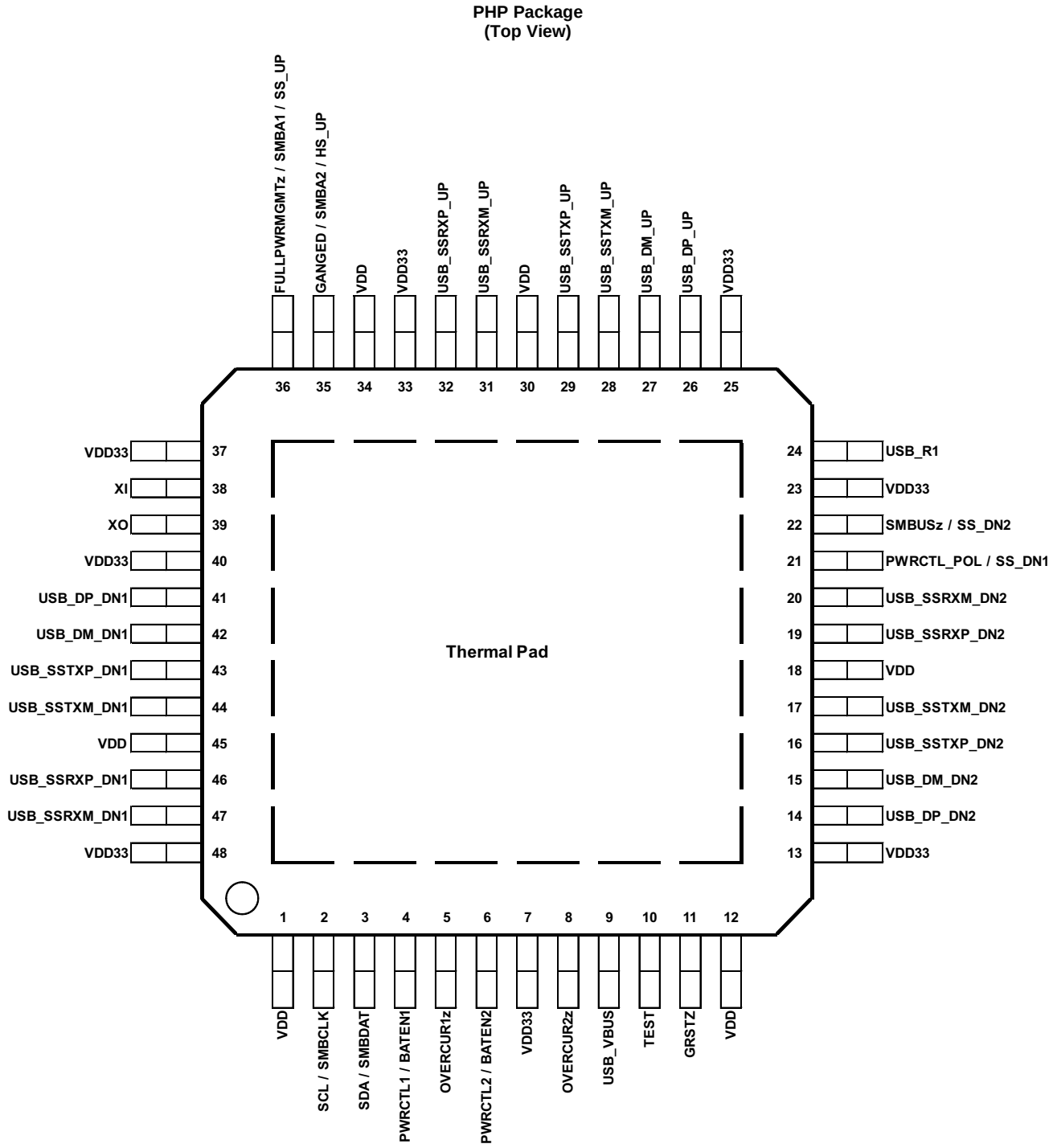
6 Pin Configuration and Functions



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Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
CLOCK AND RESET SIGNALS			
GRSTz	11	I PU	Global power reset. This reset brings all of the TUSB8020B internal registers to their default states. When GRSTz is asserted, the device is completely nonfunctional.
XI	38	I	Crystal input. This terminal is the crystal input for the internal oscillator. The input may alternately be driven by the output of an external oscillator. When using a crystal a 1-MΩ feedback resistor is required between XI and XO.
XO	39	O	Crystal output. This terminal is the crystal output for the internal oscillator. If XI is driven by an external oscillator this pin may be left unconnected. When using a crystal a 1-MΩ feedback resistor is required between XI and XO.
USB UPSTREAM SIGNALS			
USB_SSTXP_UP	29	O	USB SuperSpeed transmitter differential pair (positive)
USB_SSTXM_UP	28	O	USB SuperSpeed transmitter differential pair (negative)
USB_SSRXP_UP	32	I	USB SuperSpeed receiver differential pair (positive)
USB_SSRXM_UP	31	I	USB SuperSpeed receiver differential pair (negative)
USB_DP_UP	26	I/O	USB high-speed differential transceiver (positive)
USB_DM_UP	27	I/O	USB high-speed differential transceiver (negative)
USB_R1	24	I	Precision resistor reference. A 9.53-kΩ ±1% resistor should be connected between USB_R1 and GND.
USB_VBUS	9	I	USB upstream port power monitor. The VBUS detection requires a voltage divider. The signal USB_VBUS must be connected to VBUS through a 90.9-kΩ ±1% resistor, and to ground through a 10-kΩ ±1% resistor from the signal to ground.
USB DOWNSTREAM SIGNALS			
USB_SSTXP_DN1	43	O	USB SuperSpeed transmitter differential pair (positive) downstream port 1.
USB_SSTXM_DN1	44	O	USB SuperSpeed transmitter differential pair (negative) downstream port 1.
USB_SSRXP_DN1	46	I	USB SuperSpeed receiver differential pair (positive) downstream port 1.
USB_SSRXM_DN1	47	I	USB SuperSpeed receiver differential pair (negative) downstream port 1.
USB_DP_DN1	41	I/O	USB high-speed differential transceiver (positive) downstream port 1.
USB_DM_DN1	42	I/O	USB high-speed differential transceiver (negative) downstream port 1.
PWRCTL1/BATEN1	4	I/O PD	USB port 1 power-on control for downstream power or battery charging enable. The terminal is used for control of the downstream power switch for Port 1. In addition, the value of the terminal is sampled at the deassertion of reset to determine the value of the battery charging support for Port 1 as indicated in the Battery Charging Support register. 0 = Battery charging not supported 1 = Battery charging supported
OVERCUR1z	5	I PU	USB DS port 1 overcurrent detection input. This terminal is used to connect the over current output of the downstream port power switch for port 1. 0 = An overcurrent event has occurred 1 = An overcurrent event has not occurred If power management is enabled, the external circuitry needed should be determined by the power switch. In ganged mode, either OVERCUR1z or OVERCUR2z can be used. In ganged mode, the overcurrent will be reported as a hub event instead of a port event.
USB_SSTXP_DN2	16	O	USB SuperSpeed transmitter differential pair (positive) downstream port 2.
USB_SSTXM_DN2	17	O	USB SuperSpeed transmitter differential pair (negative) downstream port 2.
USB_SSRXP_DN2	19	I	USB SuperSpeed receiver differential pair (positive) downstream port 2.
USB_SSRXM_DN2	20	I	USB SuperSpeed receiver differential pair (negative) downstream port 2.
USB_DP_DN2	14	I/O	USB high-speed differential transceiver (positive) downstream port 2.
USB_DM_DN2	15	I/O	USB high-speed differential transceiver (negative) downstream port 2.
PWRCTL2/BATEN2	6	I/O PD	Power-on control /battery charging enable for downstream port 2. This terminal is used for control of the downstream power switch for port 2. The value of the terminal is sampled at the deassertion of reset to determine the value of the battery charging support for port 2 as indicated in the Battery Charging Support register. 0 = Battery charging not supported 1 = Battery charging supported
OVERCUR2z	8	I PU	Overcurrent detection for downstream port 2. This terminal is used to connect the over current output of the downstream port power switch for port 2. 0 = An overcurrent event has occurred 1 = An overcurrent event has not occurred If power management is enabled, the external circuitry needed should be determined by the power switch. In ganged mode either OVERCUR1z or OVERCUR2z can be used. In ganged mode the overcurrent will be reported as a hub event instead of a port event.

(1) I = input, O = output, I/O = input/output, PU = internal pullup resistor, PD = internal pulldown resistor, and PWR = power signal

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Pin Functions (continued)

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
I²C/SMBUS SIGNALS			
SCL/SMBCLK	2	I/O PD	I²C clock/SMBus clock. Function of terminal depends on the setting of the SMBUSz input. When SMBUSz = 1, this terminal acts as the serial clock interface for an I²C EEPROM. When SMBUSz = 0, this terminal acts as the serial clock interface for an SMBus host. This pin must be pulled up to use the OTP ROM. Can be left unconnected if external interface not implemented.
SDA/SMBDAT	3	I/O PD	I²C data/SMBus data. Function of terminal depends on the setting of the SMBUSz input. When SMBUSz = 1, this terminal acts as the serial data interface for an I²C EEPROM. When SMBUSz = 0, this terminal acts as the serial data interface for an SMBus host. This pin must be pulled up to use the OTP ROM. Can be left unconnected if external interface not implemented.
TEST AND MISCELLANEOUS SIGNALS			
SMBUSz/SS_DN2	22	I PU	SMBUS mode / SuperSpeed USB Status for downstream port 2 The value of the terminal is sampled at the deassertion of reset to enable I²C or SMBus mode. 0 = SMBus mode selected 1 = I²C mode selected After reset, this signal indicates the SuperSpeed USB connection status of downstream port 2. A value of 1 indicates the connection is SuperSpeed USB.
PWRCTL_POL/SS_DN1	21	I/O PD	Power control polarity / SuperSpeed USB status for downstream port 1. The value of the terminal is sampled at the deassertion of reset to set the polarity of PWRCTL[2:1]. 0 = PWRCTL polarity is active high. 1 = PWRCTL polarity is active low. After reset, this signal indicates the SuperSpeed USB connection status of downstream port 1. A value of 1 indicates the connection is SuperSpeed USB.
GANGED/SMBA2/ HS_UP	35	I PU	Ganged operation enable/SMBus address bit 2/ high-speed status for upstream port The value of the terminal is sampled at the deassertion of reset to set the power switch and over current detection mode as follows: 0 = Individual power control supported when power switching is enabled. 1 = Power control gangs supported when power switching is enabled. When SMBus mode is enabled using SMBUSz, this terminal sets the value of the SMBus slave address bit 2. SMBus slave address bits 2 and 3 are always 1 for the TUSB8020B. After reset, this signal indicates the high-speed USB connection status of the upstream port. A value of 1 indicates the upstream port is connected to a high-speed USB capable port.
FULLPWRMGMTz/ SMBA1/SS_UP	36	I, PU	Full power management enable/ SMBus Address bit 1/ Super-Speed USB status for upstream port The value of the terminal is sampled at the deassertion of reset to set the power switch control follows: 0 = Power switching supported 1 = Power switching not supported Full power management is the ability to control power to the downstream ports of the TUSB8020B using PWRCTL[2:1]/BATEN[2:1]. When SMBus mode is enabled using SMBUSz, this terminal sets the value of the SMBus slave address bit 1. SMBus slave address bit 3 is always 1 for the TUSB8020B. Can be left unconnected if full power management and SMBus are not implemented. After reset, this signal indicates the SuperSpeed USB connection status of the upstream port. A value of 1 indicates the upstream port is connected to a SuperSpeed USB capable port.
TEST	10	I PD	TEST mode enable. When this terminal is asserted high at reset enables test mode. This terminal is reserved for factory use. It is recommended to pull-down this terminal to ground.
POWER AND GROUND SIGNALS			
VDD	1, 12, 18, 30, 34, 45	PWR	1.1-V power rail
VDD33	7, 13, 23, 25, 33, 37, 40, 48	PWR	3.3-V power rail
GND	PAD	—	Ground

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7 Specifications

7.1 Absolute Maximum Ratings(1)

over operating free-air temperature (unless otherwise noted)

		MIN	MAX	UNIT
VDD	Steady-state supply voltage	–0.3	1.4	V
VDD33	Steady-state supply voltage	–0.3	3.8	V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	–2000	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	–500	500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
VDD(1)	1.1-V supply voltage		0.99	1.1	1.26	V
VDD33	3.3-V supply voltage		3	3.3	3.6	V
USB_VBUS	Voltage at USB_VBUS PAD		0		1.155	V
T_A	Operating free-air temperature range	TUSB8020B	0	25	70	°C
		TUSB8020BI	–40	25	85	
T_J	Operating junction temperature range		–40	25	105	°C

(1) A 1.05-V, 1.1-V, or 1.2-V supply may be used as long as minimum and maximum supply conditions are met.

7.4 Thermal Information

THERMAL METRIC(1)		TUSB8020B PHP 48 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(2)	31.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance(3)	16.1	
$R_{\theta JB}$	Junction-to-board thermal resistance(4)	13	
ψ_{JT}	Junction-to-top characterization parameter(5)	0.5	
ψ_{JB}	Junction-to-board characterization parameter(6)	12.9	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance(7)	0.9	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

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7.5 3.3-V I/O Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		OPERATION	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage (1)	VDD33		2		VDD33	V
V_{IL}	Low-level input voltage (1)	VDD33		0		0.8	V
V_I	Input voltage			0		VDD33	V
V_O	Output voltage (2)			0		VDD33	V
t_t	Input transition time (t_{rise} and t_{fall})			0		25	ns
V_{hys}	Input hysteresis (3)					0.13 × VDD33	V
V_{OH}	High-level output voltage	VDD33	I_{OH} = –4 mA	2.4			V
V_{OL}	Low-level output voltage	VDD33	I_{OL} = 4 mA			0.4	V
I_{OZ}	High-impedance, output current (2)	VDD33	V_I = 0 to VDD33			±20	µA
I_{OZP}	High-impedance, output current with internal pullup or pulldown resistor (4)	VDD33	V_I = 0 to VDD33			±225	µA
I_I	Input current (5)	VDD33	V_I = 0 to VDD33			±15	µA

(1) Applies to external inputs and bidirectional buffers
(2) Applies to external outputs and bidirectional buffers
(3) Applies to GRSTz
(4) Applies to pins with internal pullups/pulldowns
(5) Applies to external input buffers

7.6 Power-Up Timing Requirements

		MIN	TYP	MAX	UNIT
t_{d1}	V_{DD33} stable before V_{DD} stable. No timing relationship between V_{DD33} and V_{DD}	0			ms
t_{d2}	V_{DD} and V_{DD33} stable before deassertion of GRSTZ.	3			ms
t_{su_io}	Setup for MISC inputs sampled at the deassertion of GRSTZ (1)	0.1			µs
t_{hd_io}	Hold for MISC inputs sampled at the deassertion of GRSTZ. (1)	0.1			µs
t_{VDD33_RAMP}	V_{DD33} supply ramp requirements	0.2		100	ms
t_{VDD_RAMP}	V_{DD} supply ramp requirements	0.2		100	ms

(1) Miscellaneous pins sampled at deassertion of GRSTZ: FULLPWRMGMTz, GANGED, PWRCTL_POL, SMBUSz, BATEN1, and BATEN2

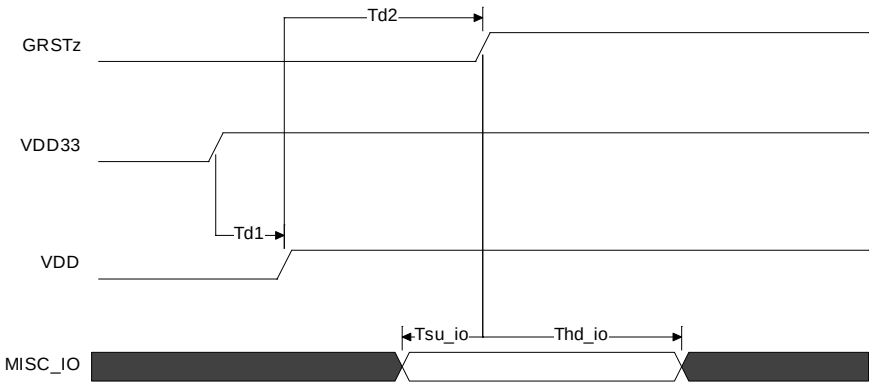

Figure 1. Power-Up Timing Requirements

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7.7 Hub Input Supply Current

Typical values measured at T_A = 25°C

PARAMETER	VDD33	VDD11	UNIT
	3.3 V	1.1 V	
LOW-POWER MODES			
Power-on (after reset)	5	39	mA
Disconnect from host	5	39	mA
Suspend (USB2 host)	5	39	mA
Suspend (USB3 host)	6	40	mA
ACTIVE MODES (US STATE / DS STATE)			
3.0 host / 1 SS device and hub in U1	50	218	mA
3.0 host / 1 SS device and hub in U0	50	342	mA
3.0 host / 2 SS devices and hub in U1	50	284	mA
3.0 host / 2 SS devices and hub in U0	50	456	mA
3.0 host / 1 SS and 1 HS device in U1	92	242	mA
3.0 host / 1 SS and 1 HS device in U0	93	364	mA
2.0 host / 1 HS device active	48	71	mA
2.0 host / 2 HS devices active	60	80	mA

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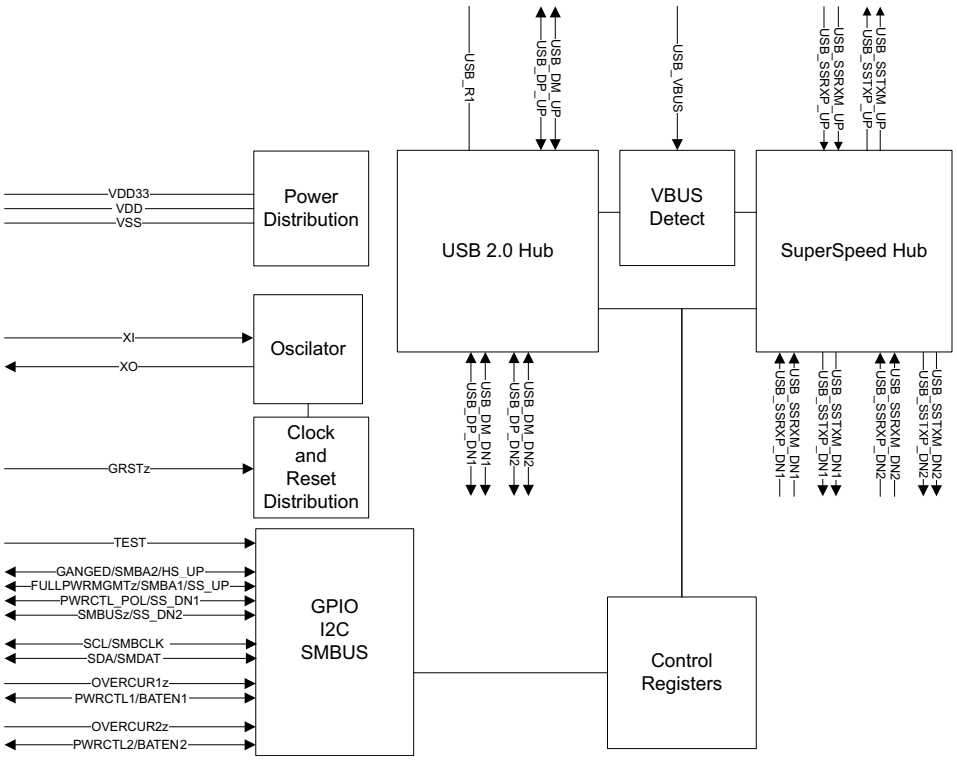
8 Detailed Description

8.1 Overview

The TUSB8020B is a two-port USB 3.0 compliant hub. It provides simultaneous SuperSpeed USB and high-speed/full-speed connections on the upstream port and provides SuperSpeed USB, high-speed, full-speed, or low-speed connections on the downstream ports. When the upstream port is connected to an electrical environment that only supports high-speed or full-speed/low-speed connections, SuperSpeed USB connectivity is disabled on the downstream ports. When the upstream port is connected to an electrical environment that only supports full-speed/low-speed connections, SuperSpeed USB and high-speed connectivity are disabled on the downstream ports.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Battery Charging Features

The TUSB8020B provides support for battery charging. Battery charging support may be enabled on a per port basis through the REG_6h(batEn[1:0]).

Battery charging support includes both charging downstream port (CDP) and dedicated charging port (DCP) modes. The DCP mode is compliant with the Chinese Telecommunications Industry Standard YD/T 1591-2009.

In addition to standard DCP mode, the TUSB8020B provides a mode (AUTOMODE) which automatically provides support for DCP devices and devices that support custom charging indication. AUTOMODE is enabled by default. When in AUTOMODE, the port automatically switches between a divider mode and the DCP mode depending on the portable device connected. The divider mode places a fixed DC voltage on the ports DP and DM signals which allows some devices to identify the capabilities of the charger. The default divider mode indicates support for up to 5 W. The divider mode can be configured to report a high-current setting (up to 10 W) through REG_Ah(HiCurAcpModeEn). When AUTOMODE is enabled, the CDP mode is not functional. CDP mode can not be used when AUTOMODE is enabled.

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Feature Description (continued)

The battery charging mode for each port depends on the state of Reg_6h(batEn[n]), the status of the VBUS input, and the state of REG_Ah(autoModeEnz) upstream port, as identified in Table 1. Battery charging can also be enabled through the PWRCTL1/BATEN1 and PWRCTL2/BATEN2 pins.

Table 1. TUSB8020B Battery Charging Modes

batEn[n]	VBUS	autoModeEnz	BC Mode Port x (x = n + 1)
0	Don't care	Don't care	Don't care
1	<4 V	0	Automode(1) (2)
		1	DCP(3) (4)
	>4 V	1	CDP(3)

(1) Auto-mode automatically selects divider-mode or DCP mode.
(2) Divider mode can be configured for high-current mode through register or OTP settings.
(3) USB device is USB Battery Charging Specification Revision 1.2 Compliant
(4) USB device is Chinese Telecommunications Industry Standard YD/T 1591-2009

8.3.2 USB Power Management

The TUSB8020B can be configured for power switched applications using either per-port or ganged power-enable controls and over-current status inputs.

Power switch support is enabled by REG_5h(fullPwrMgmtz) and the per-port or ganged mode is configured by REG_5h(ganged). It can also be enabled through the FULLPWRMGMTz pin. Also ganged or individual control can be controlled by the GANGED pin.

The TUSB8020B supports both active-high and active-low power-enable controls. The PWRCTL[2:1] polarity is configured by REG_Ah(pwrctlPol). The polarity can also be configured by the PWRCTL_POL pin.

8.3.3 One-Time Programmable (OTP) Configuration

The TUSB8020B allows device configuration through OTP non-volatile memory (OTP). The programming of the OTP is supported using vendor-defined USB device requests. For details using the OTP features, contact your TI representative.

Table 2 provides a list features which may be configured using the OTP. The bit field section in Table 2 shows which features can be controlled by OTP ROM. The bits not listed in the table are not accessible by the OTP ROM.

Table 2. OTP Configurable Features

CONFIGURATION REGISTER OFFSET	BIT FIELD	DESCRIPTION
REG_01h	[7:0]	Vendor ID LSB
REG_02h	[7:0]	Vendor ID MSB
REG_03h	[7:0]	Product ID LSB
REG_04h	[7:0]	Product ID MSB
REG_07h	[0]	Port removable configuration for downstream ports 1. OTP configuration is inverse of rmbl[1:0], that is: 1 = Not removable 0 = Removable
REG_07h	[1]	Port removable configuration for downstream ports 2. OTP configuration is inverse of rmbl[1:0], that is: 1 = Not removable 0 = Removable
REG_0Ah	[1]	Automode enable
REG_0Ah	[4]	High-current divider mode enable.
REG_F2h	[3:1]	USB power switch power-on delay.

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8.3.4 Clock Generation

The TUSB8020B accepts a crystal input to drive an internal oscillator or an external clock source. If a crystal is used, a 1-MΩ shunt resistor is required. Keep the XI and XO traces as short as possible and away from any switching leads to minimize noise coupling.

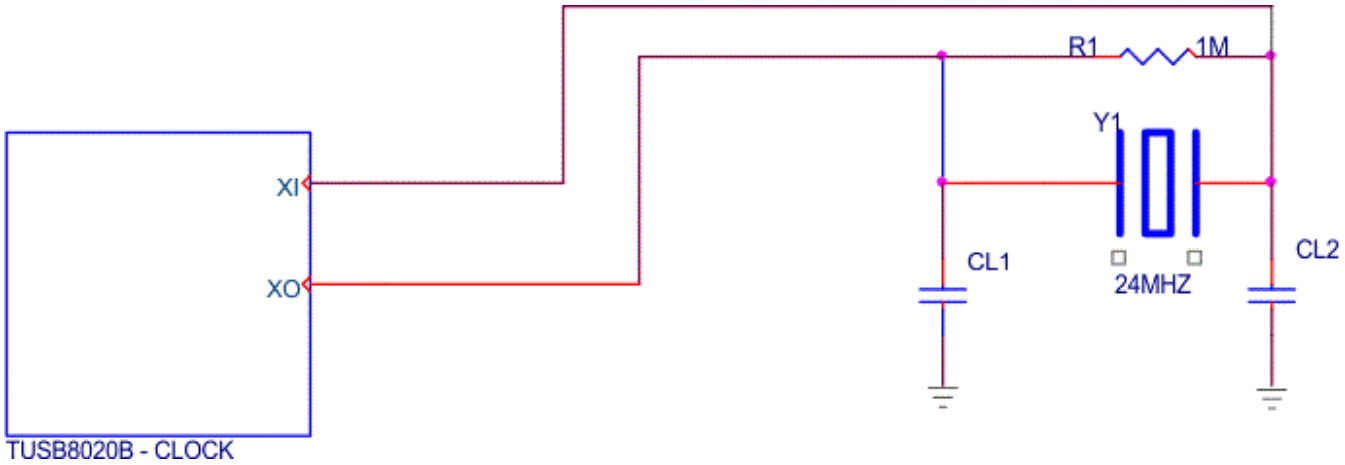

Figure 2. TUSB8020B Clock

8.3.4.1 Crystal Requirements

The crystal must be fundamental mode with load capacitance of 12 to 24 pF and frequency stability rating of ±100 PPM or better. To ensure proper startup oscillation condition, TI recommends a maximum crystal equivalent series resistance (ESR) of 50 Ω. A parallel load capacitor should be used if a crystal source is used. The exact load capacitance value used depends on the crystal vendor. Refer to application note *Selection and Specification of Crystals for Texas Instruments USB 2.0 Devices* (SLLA122) for details on how to determine the load capacitance value.

8.3.4.2 Input Clock Requirements

When using an external clock source such as an oscillator, the reference clock should have a ±100 PPM or better frequency stability and have less than 50-ps absolute peak-to-peak jitter or less than 25-ps peak-to-peak jitter after applying the USB 3.0 jitter transfer function. XI should be tied to the 1.8-V clock source and XO should be left floating.

8.3.5 Power-Up and Reset

The TUSB8020B does not have specific power sequencing requirements with respect to the VDD or VDD33 power rails. The VDD or VDD33 power rails may be powered up for an indefinite period of time while the other is not powered up if all of these constraints are met:

- All maximum ratings and recommended operating conditions are observed.
- All warnings about exposure to maximum rated and recommended conditions are observed, particularly junction temperature. These apply to power transitions as well as normal operation.
- Bus contention while VDD33 is powered-up must be limited to 100 hours over the projected lifetime of the device.
- Bus contention while VDD33 is powered-down may violate the absolute maximum ratings.

A supply bus is powered up when the voltage is within the recommended operating range. A supply bus is powered down when it is below that range, either stable or in transition.

A minimum reset duration of 3 ms is required, which is defined as the time when the power supplies are in the recommended operating range to the deassertion of GRSTz. This can be generated using programmable-delay supervisory device or using an RC circuit.

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8.4 Device Functional Modes

8.4.1 External Configuration Interface

The TUSB8020B supports a serial interface for configuration register access. The device may be configured by an attached I^2C EEPROM or accessed as a slave by a SMBus-capable host controller. The external interface is enabled when both the SCL/SMBCLK and SDA/SMBDAT terminals are pulled up to 3.3 V at the deassertion of reset. The mode, I^2C master, or SMBus slave is determined by the state of SMBUSz/SS_DN2 terminal at reset.

8.4.2 I^2C EEPROM Operation

The TUSB8020B supports a single-master, standard mode (100 kbit/s) connection to a dedicated I^2C EEPROM when the I^2C interface mode is enabled. In I^2C mode, the TUSB8020B reads the contents of the EEPROM at bus address 1010000b using 7-bit addressing starting at address 0.

If the value of the EEPROM contents at byte 00h equals 55h, the TUSB8020B loads the configuration registers according to the EEPROM map. If the first byte is not 55h, the TUSB8020B exits the I^2C mode and continues execution with the default values in the configuration registers. The hub will not connect on the upstream port until the configuration is completed. If the TUSB8020B detects an unprogrammed EEPROM (value other than 55h), it enters programming mode and a programming endpoint within the hub is enabled.

Note, the bytes located above offset Ah are optional. The requirement for data in those addresses depends on the options configured in the Device Configuration, Phy Custom Configuration, and Device Configuration 2 registers.

For details on I^2C operation, refer to the UM10204 I^2C-bus Specification and User Manual.

8.4.3 SMBus Slave Operation

When the SMBus interface mode is enabled, the TUSB8020B supports read block and write block protocols as a slave-only SMBus device.

The TUSB8020B slave address is 1000 1xyz, where:

- x is the state of GANGED/SMBA2/HS_UP terminal at reset
- y is the state of FULLPWRMGMTz/SMBA1/SS_UP terminal at reset
- z is the read/write bit; 1 = read access, 0 = write access.

If the TUSB8020B is addressed by a host using an unsupported protocol, it does not respond. The TUSB8020B waits indefinitely for configuration by the SMBus host and does not connect on the upstream port until the SMBus host indicates configuration is complete by clearing the CFG_ACTIVE bit.

For details on SMBus requirements, refer to the System Management Bus Specification.

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8.5 Register Maps

8.5.1 Configuration Registers

The internal configuration registers are accessed on byte boundaries. The configuration register values are loaded with defaults but can be overwritten when the TUSB8020B is in I^2C or SMBus mode.

Table 3. TUSB8020B Register Map

BYTE ADDRESS	CONTENTS	EEPROM CONFIGURABLE
00h	ROM Signature Register	No
01h	Vendor ID LSB	Yes
02h	Vendor ID MSB	Yes
03h	Product ID LSB	Yes
04h	Product ID MSB	Yes
05h	Device Configuration Register	Yes
06h	Battery Charging Support Register	Yes
07h	Device Removable Configuration Register	Yes
08h	Port Used Configuration Register	Yes
09h	Reserved	Yes, program to 00h
0Ah	Device Configuration Register 2	Yes
0Bh to 0Fh	Reserved	
10h to 1Fh	UUID Byte [15:0]	No
20h to 21h	LangID Byte [1:0]	Yes, if customStrings is set
22h	Serial Number String Length	Yes, if customSerNum is set
23h	Manufacturer String Length	Yes, if customStrings is set
24h	Product String Length	Yes, if customStrings is set
25h to 2Fh	Reserved	Yes
30h to 4Fh	Serial Number String Byte [31:0]	Yes, if customSerNum is set
50h to 8Fh	Manufacturer String Byte [63:0]	Yes, if customStrings is set
90h to CFh	Product String Byte [63:0]	Yes, if customStrings is set
D0 to DFh	Reserved	No
F0h	Additional Feature Configuration Register	Yes
F1h	Reserved	Yes
F2h	Charging Port Control Register	Yes
F3 to F7h	Reserved	No
F8h	Device Status and Command Register	No
F9 to FFh	Reserved	No

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8.5.1.1 ROM Signature Register (offset = 0h) [reset = 0h]

Figure 3. Register Offset 0h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; –n = value after reset

Table 4. ROM Signature Register

Bit	Field	Type	Reset	Description
7:0	romSignature	R/W	0h	ROM Signature Register. This register is used by the TUSB8020B in I^2C mode to validate the attached EEPROM has been programmed. The first byte of the EEPROM is compared to the mask 55h and if not a match, the TUSB8020B aborts the EEPROM load and executes with the register defaults.

8.5.1.2 Vendor ID LSB Register (offset = 1h) [reset = 51h]

Figure 4. Register Offset 51h

7	6	5	4	3	2	1	0
0	1	0	1	0	0	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; –n = value after reset

Table 5. Vendor ID LSB Register

Bit	Field	Type	Reset	Description
7:0	vendorIdLsb	R/W	51h	Vendor ID LSB. Least significant byte of the unique vendor ID assigned by the USB-IF; the default value of this register is 51h representing the LSB of the TI Vendor ID 0451h. The value may be overwritten to indicate a customer vendor ID. This field is read/write unless the OTP ROM VID and OTP ROM PID values are non-zero. If both values are non-zero, the value when reading this register shall reflect the OTP ROM value.

8.5.1.3 Vendor ID MSB Register (offset = 2h) [reset = 4h]

Figure 5. Register Offset 2h

7	6	5	4	3	2	1	0
0	0	0	0	0	1	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; –n = value after reset

Table 6. Vendor ID MSB Register

Bit	Field	Type	Reset	Description
7:0	vendorIdMsb	R/W	4h	Vendor ID MSB. Most significant byte of the unique vendor ID assigned by the USB-IF; the default value of this register is 04h representing the MSB of the TI Vendor ID 0451h. The value may be overwritten to indicate a customer vendor ID. This field is read/write unless the OTP ROM VID and OTP ROM PID values are non-zero. If both values are non-zero, the value when reading this register shall reflect the OTP ROM value.

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8.5.1.4 Product ID LSB Register (offset = 3h) [reset = 25h]

Figure 6. Register Offset 3h

7	6	5	4	3	2	1	0
0	0	1	0	0	1	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; –n = value after reset

Table 7. Product ID LSB Register

Bit	Field	Type	Reset	Description
7:0	productIdLsb	R/W	25h	Product ID LSB. Least significant byte of the product ID assigned by TI and reported in the SuperSpeed device descriptor. The default value of this register is 25h representing the LSB of the SuperSpeed product ID assigned by TI. The value reported in the USB 2.0 device descriptor is the value of this register bit wise XORed with 00000010b. The value may be overwritten to indicate a customer product ID. This field is read/write unless the OTP ROM VID and OTP ROM PID values are non-zero. If both values are non-zero, the value when reading this register shall reflect the OTP ROM value.

8.5.1.5 Product ID MSB Register (offset = 4h) [reset = 80h]

Figure 7. Register Offset 4h

7	6	5	4	3	2	1	0
1	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; –n = value after reset

Table 8. Bit Descriptions – Product ID MSB Register

Bit	Field	Type	Reset	Description
7:0	productIdLsb	R/W	80h	Product ID MSB. Most significant byte of the product ID assigned by TI; the default value of this register is 80h representing the MSB of the product ID assigned by TI. The value may be overwritten to indicate a customer product ID. This field is read/write unless the OTP ROM VID and OTP ROM PID values are non-zero. If both values are non-zero, the value when reading this register will reflect the OTP ROM value.

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8.5.1.6 Device Configuration Register (offset = 5h) [reset = 1Xh]

Figure 8. Register Offset 5h

7	6	5	4	3	2	1	0
0	0	0	1	X	X	0	0
R/W	R/W	R/W	R	R/W	R/W	R/W	R

LEGEND: R/W = Read/Write; R = Read only; –n = value after reset

Table 9. Device Configuration Register

Bit	Field	Type	Reset	Description
7	customStrings	R/W	1Xh	Custom strings enable. This bit controls the ability to write to the Manufacturer String Length, Manufacturer String, Product String Length, Product String, and Language ID registers. 0 = The Manufacturer String Length, Manufacturer String, Product String Length, Product String, and Language ID registers are read only. 1 = The Manufacturer String Length, Manufacturer String, Product String Length, Product String, and Language ID registers may be loaded by EEPROM or written by SMBus. The default value of this bit is 0.
6	customSernum	R/W	1Xh	Custom serial number enable. This bit controls the ability to write to the serial number registers. 0 = The Serial Number String Length and Serial Number String registers are read only. 1 = The Serial Number String Length and Serial Number String registers may be loaded by EEPROM or written by SMBus. The default value of this bit is 0.
5	u1u2Disable	R/W	1Xh	U1 U2 Disable. This bit controls the U1/U2 support. 0 = U1/U2 support is enabled. 1 = U1/U2 support is disabled, the TUSB8020B does not initiate or accept any U1 or U2 requests on any port, upstream or downstream, unless it receives or sends a Force_LinkPM_Accept LMP. After receiving or sending an FLPMA LMP, it continues to enable U1 and U2 according to USB 3.0 protocol until it gets a power-on reset or is disconnected on its upstream port. When the TUSB8020B is in I^2C mode, the TUSB8020B loads this bit from the contents of the EEPROM. When the TUSB8020B is in SMBUS mode, the value may be overwritten by an SMBus host.
4	RSVD	R	1Xh	Reserved. This bit is reserved and returns 1 when read.
3	ganged	R/W	1Xh	Ganged. This bit is loaded at the deassertion of reset with the value of the GANGED/SMBA2/HS_UP terminal. 0 = When fullPwrMgmtz = 0, each port is individually power switched and enabled by the PWRCTL[2:1]/BATEN[2:1] terminals 1 = When fullPwrMgmtz = 0, the power switch control for all ports is ganged and enabled by the PWRCTL1/BATEN1 terminal When the TUSB8020B is in I^2C mode, the TUSB8020B loads this bit from the contents of the EEPROM. When the TUSB8020B is in SMBUS mode, the value may be overwritten by an SMBus host.
2	fullPwrMgmtz	R/W	1Xh	Full Power Management. This bit is loaded at the deassertion of reset with the value of the FULLPWRMGMTz/SMBA1/SS_UP terminal. 0 = Port power switching and over-current status reporting is enabled 1 = Port power switching and over-current status reporting is disabled When the TUSB8020B is in I^2C mode, the TUSB8020B loads this bit from the contents of the EEPROM. When the TUSB8020B is in SMBUS mode, the value may be overwritten by an SMBus host.
1	RSVD	R/W	1Xh	Reserved. This bit is reserved and should not be altered from the default.
0	RSVD	R	1Xh	Reserved. This field is reserved and returns 0 when read.

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8.5.1.7 Battery Charging Support Register (offset = 6h) [reset = 0Xh]

Figure 9. Register Offset 6h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	X	X
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; –n = value after reset

Table 10. Battery Charging Support Register

Bit	Field	Type	Reset	Description
7:2	RSVD	R	0Xh	Reserved. Read only, returns 0 when read.
1:0	batEn[1:0]	R/W	0Xh	Battery Charger Support. The bits in this field indicate whether the downstream port implements the charging port features. 0 = The port is not enabled for battery charging support features 1 = The port is enabled for battery charging support features Each bit corresponds directly to a downstream port, that is batEn0 corresponds to downstream port 1, and batEN1 corresponds to downstream port 2. The default value for these bits are loaded at the deassertion of reset with the value of PWRCTL/BATEN[1:0]. When in I2C/SMBus mode the bits in this field may be overwritten by EEPROM contents or by an SMBus host.

8.5.1.8 Device Removable Configuration Register (offset = 7h) [reset = 0Xh]

Figure 10. Register Offset 7h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	X	X
R/W	R	R	R	R	R	R	R/W

LEGEND: R/W = Read/Write; R = Read only; –n = value after reset

Table 11. Device Removable Configuration Register

Bit	Field	Type	Reset	Description
7	customRmbl	R/W	0Xh	Custom removable status. When this field is a 1, the TUSB8020B uses rmbl bits in this register to identify removable status for the ports.
6:2	RSVD	R	0Xh	Reserved. Read only, returns 0 when read. Bits 3:2 are RW. They are reserved and return 0 when read.
1:0	rmbl[1:0]	R/W	0Xh	Removable. The bits in this field indicate whether a device attached to downstream ports 2 through 1 are removable or permanently attached. 0 = The device attached to the port is not removable 1 = The device attached to the port is removable Each bit corresponds directly to a downstream port n + 1, that is rmbl0 corresponds to downstream port 1, rmbl1 corresponds to downstream port 2, and so forth. This field is read only unless the customRmbl bit is set to 1. Otherwise the value of this filed reflects the inverted values of the OTP ROM non_rmb[1:0] field.

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8.5.1.9 Port Used Configuration Register (offset = 8h) [reset = 0h]

Figure 11. Register Offset 8h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	1
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; –n = value after reset

Table 12. Port Used Configuration Register

Bit	Field	Type	Reset	Description
7:0	RSVD	R	0h	Reserved. Read only.

8.5.1.10 PHY Custom Configuration Register (offset = 9h) [reset = 0h]

Figure 12. Register Offset 9h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	1
R	R	R/W	R	R	R	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; –n = value after reset

Table 13. PHY Custom Configuration Register

Bit	Field	Type	Reset	Description
7:6	RSVD	R	0h	Reserved. Read only, returns 0 when read.
5	RSVD	R/W	0h	Reserved. This bit is reserved and should not be altered from the default.
4:2	RSVD	R	0h	Reserved. Read only, returns 0 when read.
1:0	RSVD	R/W	0h	Reserved. This field is reserved and should not be altered from the default.

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8.5.1.11 Device Configuration Register 2 (offset = Ah)

Figure 13. Register Offset Ah

7	6	5	4	3	2	1	0
0	0	X	0	0	0	0	0
R	RW	RW	RW	RW	RW	RW	R

LEGEND: R/W = Read/Write; R = Read only; –n = value after reset

Table 14. Bit Descriptions – Device Configuration Register 2

Bit	Field Name	Access	Reset	Description
7	RSVD	RO		Reserved. Read only, returns 0 when read.
6	customBCfeatures	RW		Custom Battery Charging Feature Enable. This bit controls the ability to write to the battery charging feature configuration controls. 0 = The HiCurAcpModeEn and AutoModeEnz bits are read only and the values are loaded from the OTP ROM. 1 = The HiCurAcpModeEn and AutoModeEnz bits are read/write and can be loaded by EEPROM or written by SMBus. from this register. This bit may be written simultaneously with HiCurAcpModeEn and AutoModeEnz.
5	pwrctlPol	RW		Power enable polarity. This bit is loaded at the deassertion of reset with the inverse value of the PWRCTL_POL terminal. 0 = PWRCTL polarity is active low 1 = PWRCTL polarity is active high When the TUSB8020B is in I^2C mode, the TUSB8020B loads this bit from the contents of the EEPROM. When the TUSB8020B is in SMBUS mode, the value may be overwritten by an SMBus host.
4	HiCurAcpModeEn	RO/RW		High-current ACP mode enable. This bit enables the high-current tablet charging mode when the automatic battery charging mode is enabled for downstream ports. 0 = High current divider mode disabled 1 = High current divider mode enabled This bit is read only unless the customBCfeatures bit is set to 1. Otherwise the value of this bit reflects the value of the OTP ROM HiCurAcpModeEn bit.
3	RSVD	RW		Reserved
2	dsportEcrEn	RW		DSPort ECR enable. This bit enables full implementation of the DSPORT ECR (April 2013). 0 = DSPort ECR (April 2013) is enabled with the exception of changes related to the CCS bit is set upon entering U0, and changes related to avoiding or reporting compliance mode entry. 1 = The full DSport ECR (April 2013) is enabled.
1	autoModeEnz	RO/RW		Automatic Mode Enable. This bit is loaded from the OTP ROM. The automatic mode only applies to downstream ports with battery charging enabled when the upstream port is not connected. Under these conditions: 0 = Automatic mode battery charging features are enabled. Only battery charging DCP and custom BC (divider mode) is enabled. 1 = Automatic mode is disabled; only battery charging DCP and CDP mode is supported. Note: When the upstream port is connected, battery charging CDP mode is supported on all ports when this field is one. This bit is read only unless the customBCfeatures bit is set to 1. Otherwise the value of this bit reflects the value of the OTP ROM AutoModeEnz bit.
0	RSVD	RO		Reserved. Read only, returns 0 when read.

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8.5.1.12 UUID Registers (offset = 10h to 1Fh)

Figure 14. Register Offset 10h to 1Fh

7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; –n = value after reset

Table 15. Bit Descriptions – UUID Byte N Register

Bit	Field Name	Access	Reset	Description
7:0	uuidByte[n]	RO		UUID byte N. The UUID returned in the Container ID descriptor. The value of this register is provided by the device and is meets the UUID requirements of Internet Engineering Task Force (IETF) RFC 4122 A UUID URN Namespace.

8.5.1.13 Language ID LSB Register (offset = 20h)

Figure 15. Register Offset 20h

7	6	5	4	3	2	1	0
0	0	0	0	1	0	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; –n = value after reset

Table 16. Bit Descriptions – Language ID LSB Register

Bit	Field Name	Access	Reset	Description
7:0	langIdLsb	RW		Language ID least significant byte. This register contains the value returned in the LSB of the LANGID code in string index 0. The TUSB8020B only supports one language ID. The default value of this register is 09h representing the LSB of the LangID 0409h indicating English United States. When customStrings is 1, this field may be overwritten by the contents of an attached EEPROM or by an SMBus host.

8.5.1.14 Language ID MSB Register (offset = 21h)

Figure 16. Register Offset 21h

7	6	5	4	3	2	1	0
0	0	0	0	0	1	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; –n = value after reset

Table 17. Bit Descriptions – Language ID MSB Register

Bit	Field Name	Access	Reset	Description
7:0	langIdMsb	RO/RW		Language ID most significant byte. This register contains the value returned in the MSB of the LANGID code in string index 0. The TUSB8020B only supports one language ID. The default value of this register is 04h representing the MSB of the LangID 0409h indicating English United States. When customStrings is 1, this field may be overwritten by the contents of an attached EEPROM or by an SMBus host.

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8.5.1.15 Serial Number String Length Register (offset = 22h)

Figure 17. Register Offset 22h

7	6	5	4	3	2	1	0
0	0	0	1	1	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; –n = value after reset

Table 18. Bit Descriptions – Serial Number String Length Register

Bit	Field Name	Access	Reset	Description
7:6	RSVD	RO		Reserved. Read only, returns 0 when read.
5:0	serNumStringLen	RO/RW		Serial number string length. The string length in bytes for the serial number string. The default value is 18h indicating that a 24-byte serial number string is supported. The maximum string length is 32 bytes. When customSernum is 1, this field may be overwritten by the contents of an attached EEPROM or by an SMBus host. When the field is non-zero, a serial number string of serNumbStringLen bytes is returned at string index 1 from the data contained in the Serial Number String registers.

8.5.1.16 Manufacturer String Length Register (offset = 23h)

Figure 18. Register Offset 23h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; –n = value after reset

Bit Descriptions – Manufacturer String Length Register

Bit	Field Name	Access	Reset	Description
7	RSVD	RO		Reserved. Read only, returns 0 when read.
6:0	mfgStringLen	RO/RW		Manufacturer string length. The string length in bytes for the manufacturer string. The default value is 0, indicating that a manufacturer string is not provided. The maximum string length is 64 bytes. When customStrings is 1, this field may be overwritten by the contents of an attached EEPROM or by an SMBus host. When the field is non-zero, a manufacturer string of mfgStringLen bytes is returned at string index 3 from the data contained in the Manufacturer String registers.

8.5.1.17 Product String Length Register (offset = 24h)

Figure 19. Register Offset 24h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; –n = value after reset

Bit Descriptions – Product String Length Register

Bit	Field Name	Access	Reset	Description
7	RSVD	RO		Reserved. Read only, returns 0 when read.
6:0	prodStringLen	RO/RW		Product string length. The string length in bytes for the product string. The default value is 0, indicating that a product string is not provided. The maximum string length is 64 bytes. When customStrings is 1, this field may be overwritten by the contents of an attached EEPROM or by an SMBus host. When the field is non-zero, a product string of prodStringLen bytes is returned at string index 2 from the data contained in the Product String registers.

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8.5.1.18 Serial Number Registers (offset = 30h to 4Fh)

Figure 20. Register Offset 30h to 4Fh

7	6	5	4	3	2	1	0
X	X	x	x	x	x	x	x
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; –n = value after reset

Table 19. Bit Descriptions – Serial Number Registers

Bit	Field Name	Access	Reset	Description
7:0	serialNumber[n]	RO/RW		Serial Number byte N. The serial number returned in the Serial Number string descriptor at string index 1. The default value of these registers is set by TI. When customSernum is 1, these registers may be overwritten by EEPROM contents or by an SMBus host.

8.5.1.19 Manufacturer String Registers (offset = 50h to 8Fh)

Figure 21. Register Offset 50h to 8Fh

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; –n = value after reset

Table 20. Bit Descriptions – Manufacturer String Registers

Bit	Field Name	Access	Reset	Description
7:0	mfgStringByte[n]	RO/RW		Manufacturer string byte N. These registers provide the string values returned for string index 3 when mfgStringLen is greater than 0. The number of bytes returned in the string is equal to mfgStringLen. The programmed data should be in UNICODE UTF-16LE encodings as defined by The Unicode Standard, Worldwide Character Encoding, Version 5.0.

8.5.1.20 Product String Registers (offset = 90h to CFh)

Figure 22. Register Offset 90h to CFh

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; –n = value after reset

Table 21. Bit Descriptions – Product String Byte N Register

Bit	Field Name	Access	Reset	Description
7:0	prodStringByte[n]	RW		Product string byte N. These registers provide the string values returned for string index 2 when prodStringLen is greater than 0. The number of bytes returned in the string is equal to prodStringLen. The programmed data should be in UNICODE UTF-16LE encodings as defined by The Unicode Standard, Worldwide Character Encoding, Version 5.0.

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8.5.1.21 Additional Feature Configuration Register (offset = F0h)

Figure 23. Register Offset F0h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; –n = value after reset

Table 22. Bit Descriptions – Additional Feature Configuration Register

Bit	Field Name	Access	Reset	Description
7:1	RSVD	RO		Reserved. Read only, returns 0 when read.
0	usb3spreadDis	RW		USB3 Spread Spectrum Disable. This bit allows firmware to disable the spread spectrum function of the USB3 phy PLL. 0 = Spread spectrum function is enabled 1= Spread spectrum function is disabled This bit is loaded at the deassertion of reset with the value of the SCL/SMBCLK terminal.

8.5.1.22 Charging Port Control Register (offset = F2h)

Figure 24. Register Offset F2h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R	R	R	R	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; –n = value after reset

Table 23. Bit Descriptions – Charging Port Control Register

Bit	Field Name	Access	Reset	Description
7:4	RSVD	RO		Reserved. Read only, returns 0 when read.
3:1	pwronTime	RW		Power-On Delay Time. When dsportEcrEn is set, this field sets the delay time from the removal disable of PWRCTL to the enable of PWRCTL when transitioning battery charging modes. For example, when disabling the power on a transition from custom charging mode to Dedicated Charging Port Mode. The nominal timing is defined as follows: TPWRON_EN = (pwronTime + 1) × 200 ms (1) These registers may be overwritten by EEPROM contents or by an SMBus host.
0	RSVD	RW		Reserved. This bit is reserved and should not be altered from the default.

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8.5.1.23 Device Status and Command Register (offset = F8h)

Figure 25. Register Offset F8h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R	R	R	R	R	R	RSU	RCU

LEGEND: R/W = Read/Write; R = Read only; –n = value after reset

Table 24. Bit Descriptions – Device Status and Command Register

Bit	Field Name	Access	Reset	Description
7:2	RSVD	R		Reserved. Read only, returns 0 when read.
1	smbusRst	RSU		SMBus interface reset. This bit loads the registers back to their GRSTz values. This bit is set by writing a 1 and is cleared by hardware on completion of the reset. A write of 0 has no effect.
0	cfgActive	RCU		Configuration active. This bit indicates that configuration of the TUSB8020B is currently active. The bit is set by hardware when the device enters the I^2C or SMBus mode. The TUSB8020B will not connect on the upstream port while this bit is 1. When in the SMBus mode, this bit must be cleared by the SMBus host to exit the configuration mode and allow the upstream port to connect. The bit is cleared by a writing 1. A write of 0 has no effect.

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9 Application and Implementation

9.1 Application Information

The TUSB8020B is a two-port USB 3.0 compliant hub. It provides simultaneous SuperSpeed USB and high-speed/full-speed connections on the upstream port and provides SuperSpeed USB, high-speed, full-speed, or low-speed connections on the downstream port. The TUSB8020B can be used in any application that needs additional USB compliant ports. For example, a specific notebook may only have two downstream USB ports. By using the TUSB8020B, the notebook can increase the downstream port count to three.

9.2 Typical Application

A common application for the TUSB8020B is as a self-powered standalone USB hub product. The product is powered by an external 5-V DC power adapter. In this application using a USB cable, TUSB8020B device's upstream port is plugged into a USB host controller. The downstream ports of the TUSB8020B are exposed to users for connecting USB hard drives, camera, flash drive, and so forth.

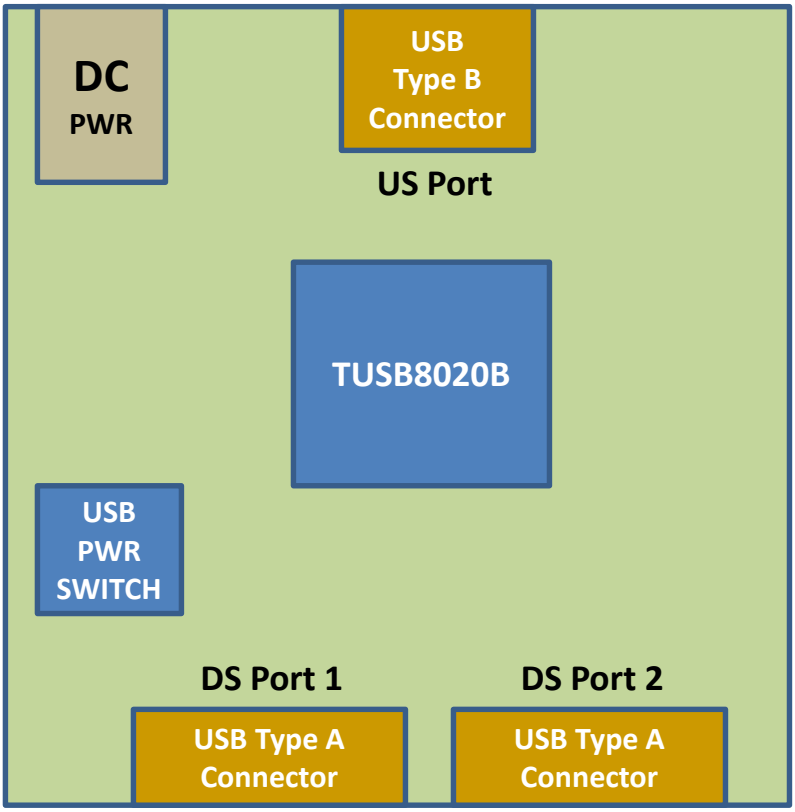

Figure 26. Discrete USB Hub Product

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Typical Application (continued)

9.2.1 Design Requirements

Table 25. Input Parameters

DESIGN PARAMETER	EXAMPLE VALUE
VDD supply	1.1 V
VDD33 supply	3.3 V
Upstream port USB support (SS, HS, FS)	SS, HS, FS
Downstream port 1 USB support (SS, HS, FS, LS)	SS, HS, FS, LS
Downstream port 2 USB support (SS, HS, FS, LS)	SS, HS, FS, LS
Number of removable downstream ports	2
Number of non-removable downstream ports	0
Full power management of downstream ports	Yes (FULLPWRMGMTZ = 0)
Individual control of downstream port power switch	Yes (GANGED = 0)
Power switch enable polarity	Active high (PWRCTL_POL = 0)
Battery charge support for downstream port 1	Yes
Battery charge support for downstream port 2	Yes
I^2C EEPROM support	No
24-MHz clock source	Crystal

9.2.2 Detailed Design Procedure

9.2.2.1 Upstream Port Implementation

The upstream of the TUSB8020B is connected to a USB3 type B connector. This particular example has GANGED terminal and FULLPWRMGMTZ terminal pulled low, which results in individual power support each downstream port. The VBUS signal from the USB3 type B connector is fed through a voltage divider. The purpose of the voltage divider is to make sure the level meets USB_VBUS input requirements.

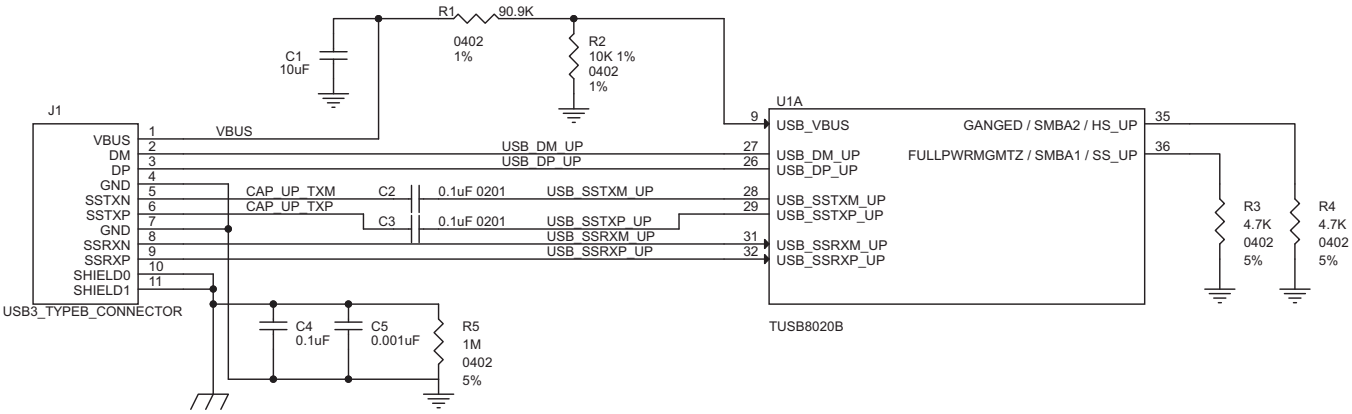

Figure 27. Upstream Port Implementation

9.2.2.2 Downstream Port 1 Implementation

The downstream port 1 of the TUSB8020B is connected to a USB3 type A connector. With BATEN1 terminal pulled up, battery charge support is enabled for port 1. If battery charge support is not needed, then the pullup resistor on BATEN1 should be uninstalled. The PWRCTL_POL is pulled-down, which results in active-high power enable (PWRCTL1 and PWRCTL2) for a USB VBUS power switch.

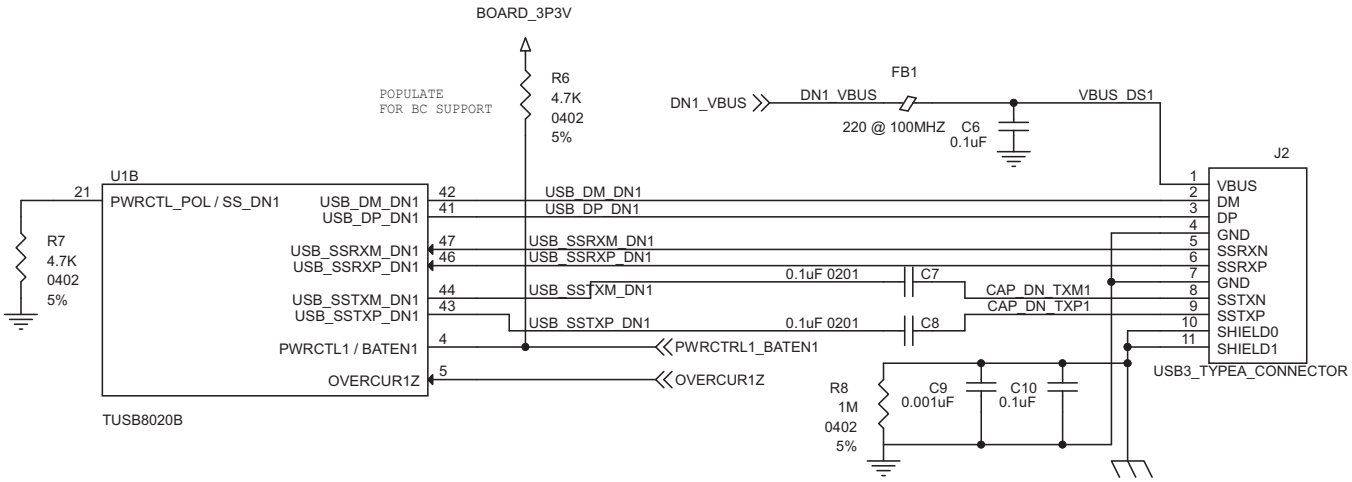

Figure 28. Downstream Port 1 Implementation

9.2.2.3 Downstream Port 2 Implementation

The downstream port 2 of the TUSB8020B is connected to a USB3 type A connector. With BATEN2 terminal pulled up, battery charge support is enabled for port 2. If battery charge support is not needed, then the pullup resistor on BATEN2 should be uninstalled.

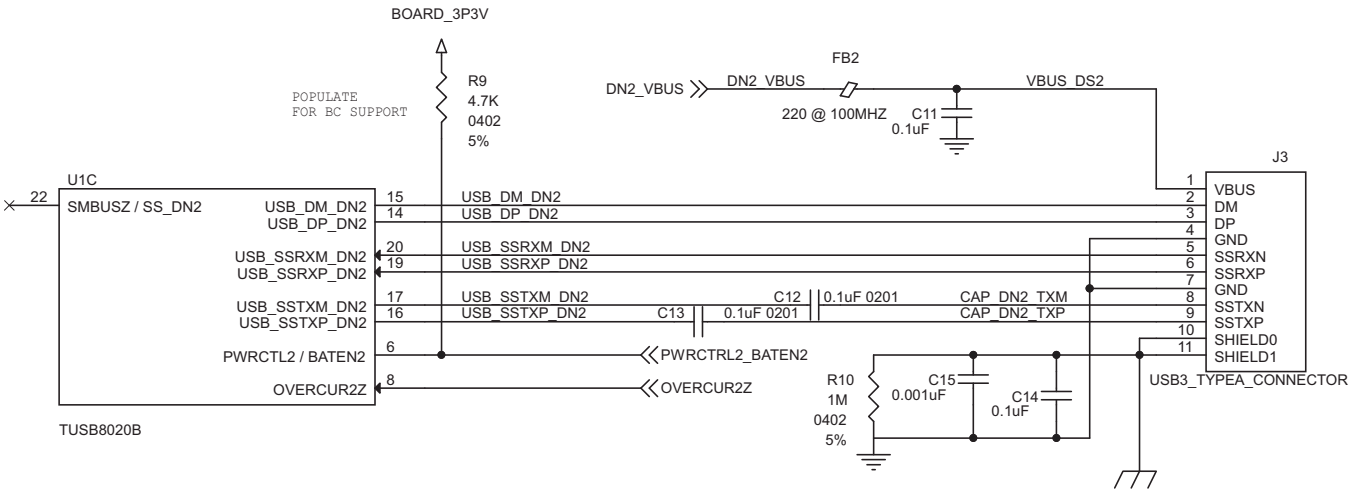

Figure 29. Downstream Port 2 Implementation

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9.2.2.4 VBUS Power Switch Implementation

This particular example uses the TI TPS2561 dual-channel precision adjustable current-limited power switch. For details on this power switch or other power switches available from TI, refer to www.ti.com.

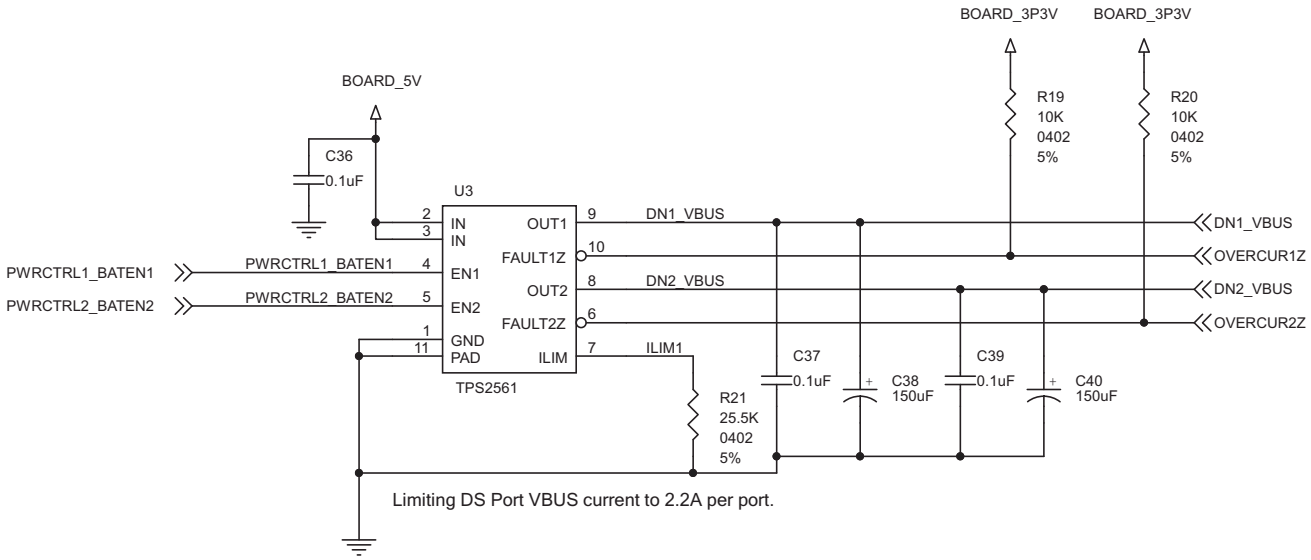

Figure 30. Power Switch Implementation

9.2.2.5 Clock, Reset, and Miscellaneous

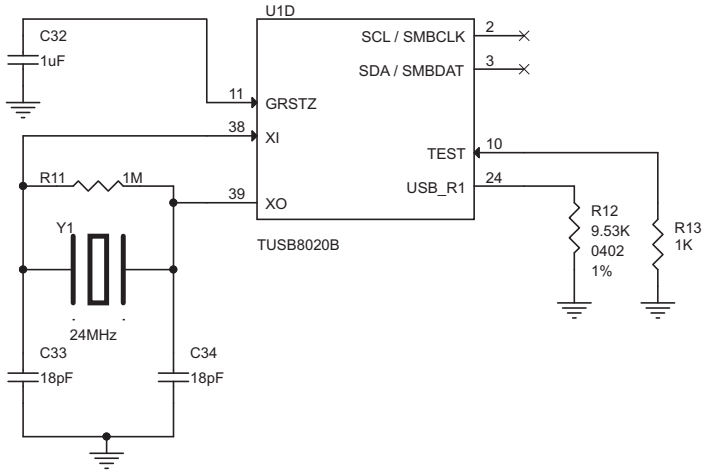

Figure 31. Clock, Reset, and Miscellaneous

9.2.2.6 Power Implementation

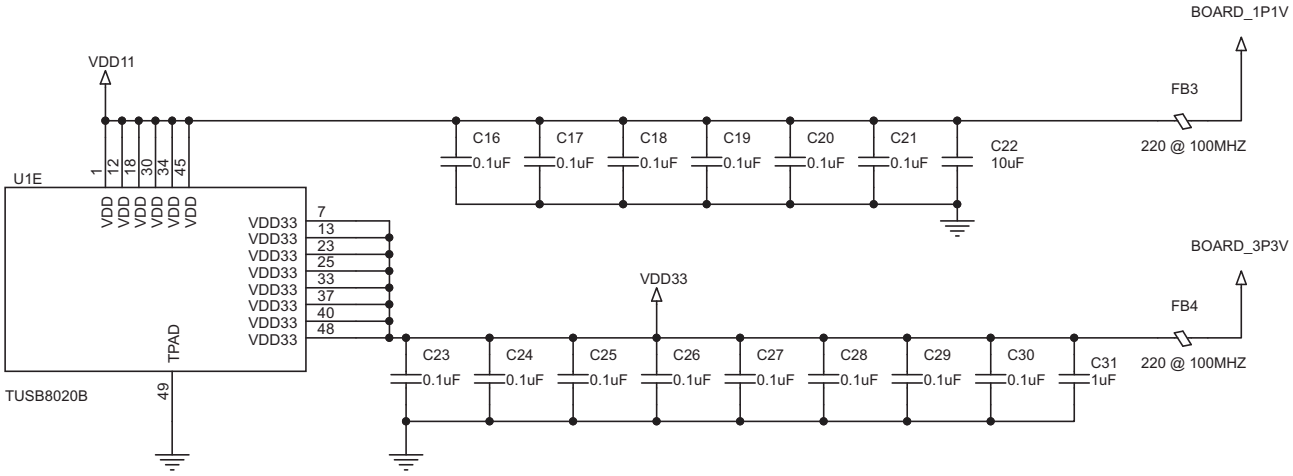

Figure 32. Power Implementation

9.2.3 Application Curves

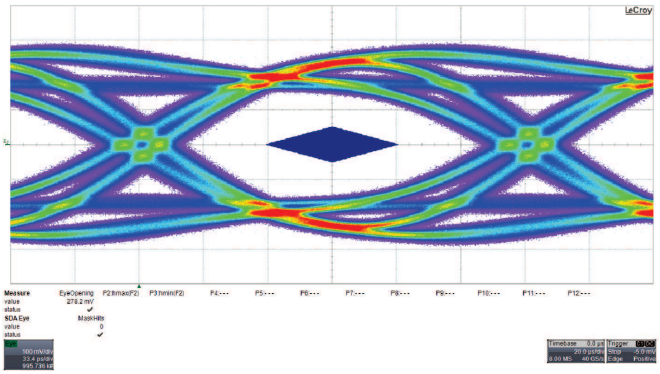

Figure 33. SuperSpeed TX Eye for Downstream Port 1

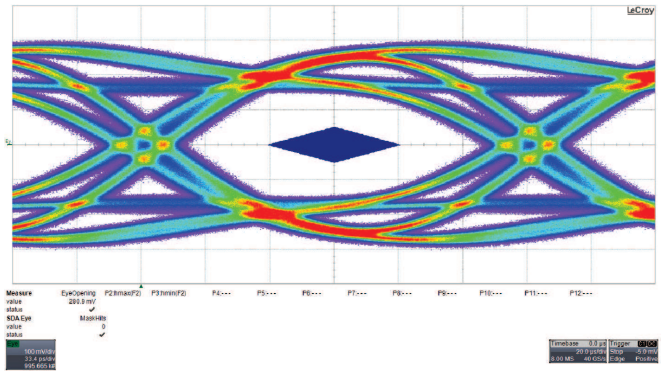

Figure 34. SuperSpeed TX Eye for Downstream Port 2

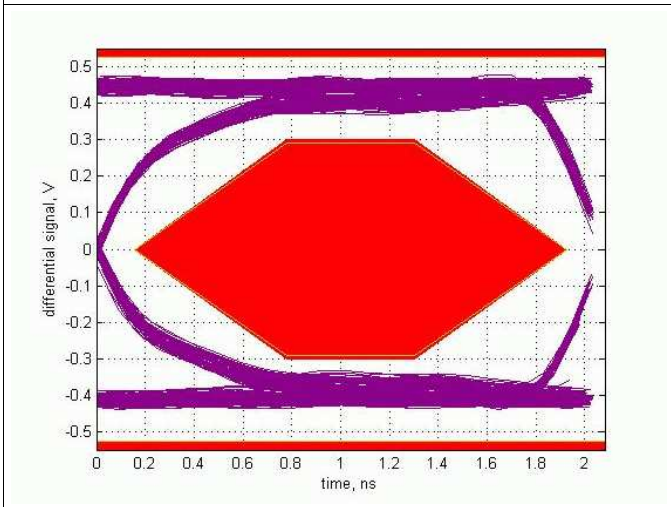

Figure 35. HighSpeed TX Eye for Downstream Port 1

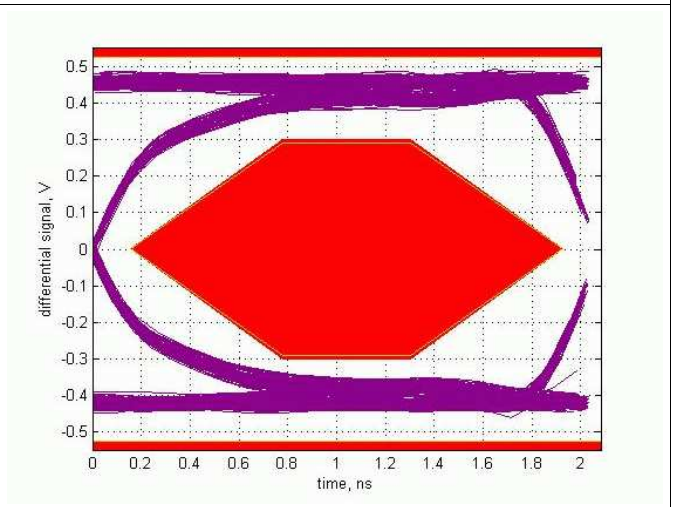

Figure 36. HighSpeed TX Eye for Downstream Port 2

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10 Power Supply Recommendations

10.1 Power Supply

V_{DD} should be implemented as a single power plane, as should V_{DD33}.

- The V_{DD} terminals of the TUSB8020B supply 1.1-V (nominal) power to the core of the TUSB8020B. This power rail can be isolated from all other power rails by a ferrite bead to reduce noise.
- The DC resistance of the ferrite bead on the core power rail can affect the voltage provided to the device due to the high current draw on the power rail. The output of the core voltage regulator may need to be adjusted to account for this or a ferrite bead with low DC resistance (less than 0.05 Ω) can be selected.
- The V_{DD33} terminals of the TUSB8020B supply 3.3-V power rail to the I/O of the TUSB8020B. This power rail can be isolated from all other power rails by a ferrite bead to reduce noise.
- All power rails require a 10-µF capacitor or 1-µF capacitors for stability and noise immunity. These bulk capacitors can be placed anywhere on the power rail. The smaller decoupling capacitors should be placed as close to the TUSB8020B power pins as possible with an optimal grouping of two of differing values per pin.

10.2 Downstream Port Power

- The downstream port power, VBUS, must be supplied by a source capable of supplying 5 V and at least 900 mA per port. Downstream port power switches can be controlled by the TUSB8020BPHP signals. It is possible to leave the downstream port power always enabled.
- Each downstream port's VBUS requires a large bulk low-ESR capacitor of 22 µF or larger to limit in-rush current.
- TI recommends ferrite beads on the VBUS pins of the downstream USB port connections for both ESD and EMI reasons. A 0.1-µF capacitor on the USB connector side of the ferrite provides a low-impedance path to ground for fast rise time ESD current that might have coupled onto the VBUS trace from the cable.

10.3 Ground

TI recommends to use only one board ground plane in the design. This provides the best image plane for signal traces running above the plane. The thermal pad of the TUSB8020B and any of the voltage regulators should be connected to this plane with vias. An earth or chassis ground is only implemented near the USB port connectors on a different plane for EMI and ESD purposes.

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11 Layout

11.1 Layout Guidelines

11.1.1 Placement

1. A 9.53-kΩ ±1% resistor connected to terminal USB_R1 should be placed as close as possible to the TUSB8020B.
2. A 0.1-µF capacitor should be placed as close as possible on each V_{DD} and V_{DD33} power pin.
3. The 100-nF capacitors on the SSTXP and SSTXM nets should be placed close to the USB connector (type A, type B, and so forth).
4. The ESD and EMI protection devices (if used) should also be placed as possible to the USB connector.
5. If a crystal is used, it must be placed as close as possible to the TUSB8020B device's XI and XO terminals.
6. Place voltage regulators as far away as possible from the TUSB8020B, crystal, and differential pairs.
7. In general, the large bulk capacitors associated with each power rail should be placed as close as possible to the voltage regulators.

11.1.2 Package Specific

1. The TUSB8020B package has a 0.5-mm pin pitch.
2. The TUSB8020B package has a 3.6-mm × 3.6-mm thermal pad. This thermal pad must be connected to ground through a system of vias.
3. All vias under device, except for those connected to thermal pad, should be solder masked to avoid potential issues with thermal pad layouts.

11.1.3 Differential Pairs

This section describes the layout recommendations for all of the TUSB8020B differential pairs: USB_DP_XX, USB_DM_XX, USB_SSTXP_XX, USB_SSTXM_XX, USB_SSRXP_XX, and USB_SSRXM_XX.

- Must be designed with a differential impedance of 90 Ω ±10%.
- To minimize crosstalk, TI recommends to keep high-speed signals away from each other. Each pair should be separated by at least 5× the signal trace width. Separating with ground as depicted in the layout example also helps minimize crosstalk.
- Route all differential pairs on the same layer adjacent to a solid ground plane.
- Do not route differential pairs over any plane split.
- Adding test points causes impedance discontinuity, and therefore, negatively impacts signal performance. If test points are used, they should be placed in series and symmetrically. They must not be placed in a manner that causes stub on the differential pair.
- Avoid 90° turns in trace. The use of bends in differential traces should be kept to a minimum. When bends are used, the number of left and right bends should be as equal as possible and the angle of the bend should be ≥135°. Taking this action minimizes any length mismatch caused by the bends, and therefore, minimizes the impact bends have on EMI.
- Minimize the trace lengths of the differential pair traces. Eight inches is the maximum recommended trace length for SS differential-pair signals and USB 2.0 differential-pair signals. Longer trace lengths require very careful routing to assure proper signal integrity.
- Match the etch lengths of the differential pair traces (that is DP and DM or SSRXP and SSRXM or SSTXP and SSTXM). There should be less than 5-mils difference between a SS differential-pair signal and its complement. The USB 2.0 differential pairs should not exceed 50-mils relative trace length difference.
- The etch lengths of the differential pair groups do not need to match (that is the length of the SSRX pair to that of the SSTX pair), but all trace lengths should be minimized.
- Minimize the use of vias in the differential-pair paths as much as possible. If this is not practical, ensure that the same via type and placement are used for both signals in a pair. Any vias used should be placed as close as possible to the TUSB8020B device.
- To ease routing, the polarity of the SS differential pairs can be swapped. This means that SSTXP can be routed to SSTXM or SSRXM can be routed to SSRXP.
- Do not place power fuses across the differential-pair traces.

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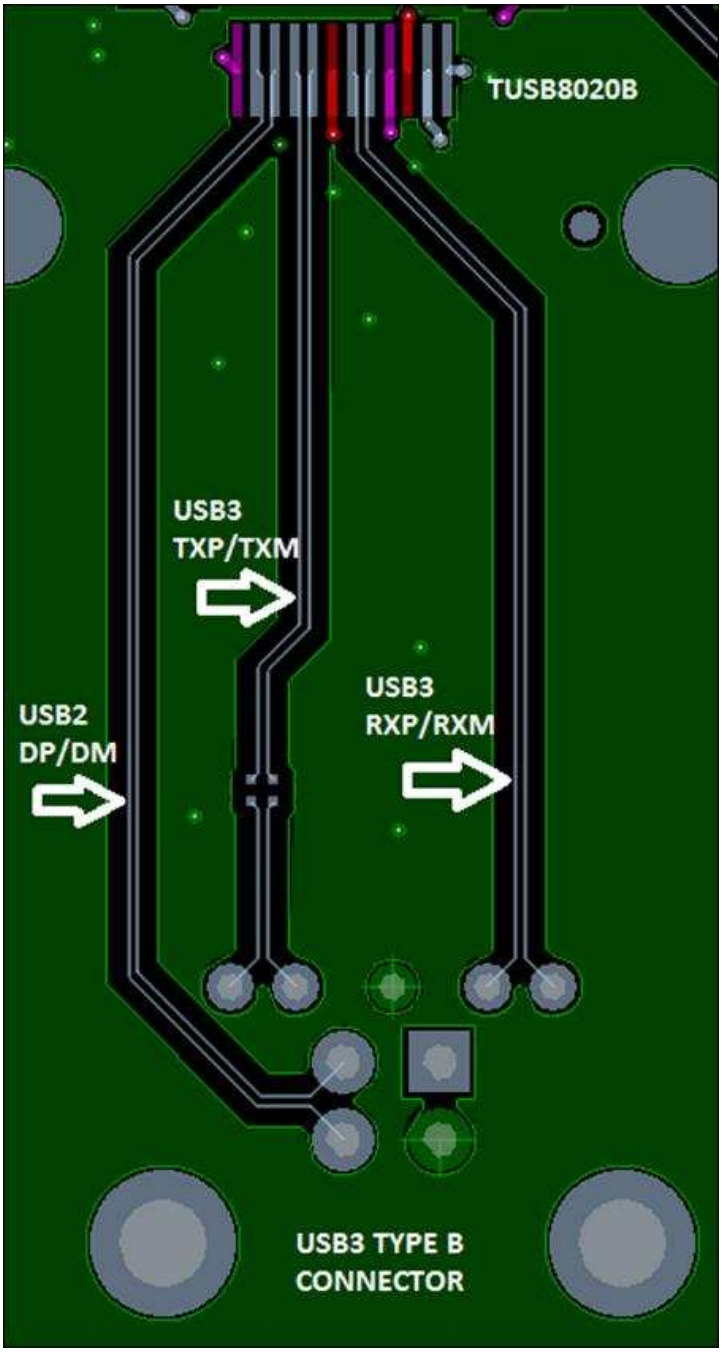
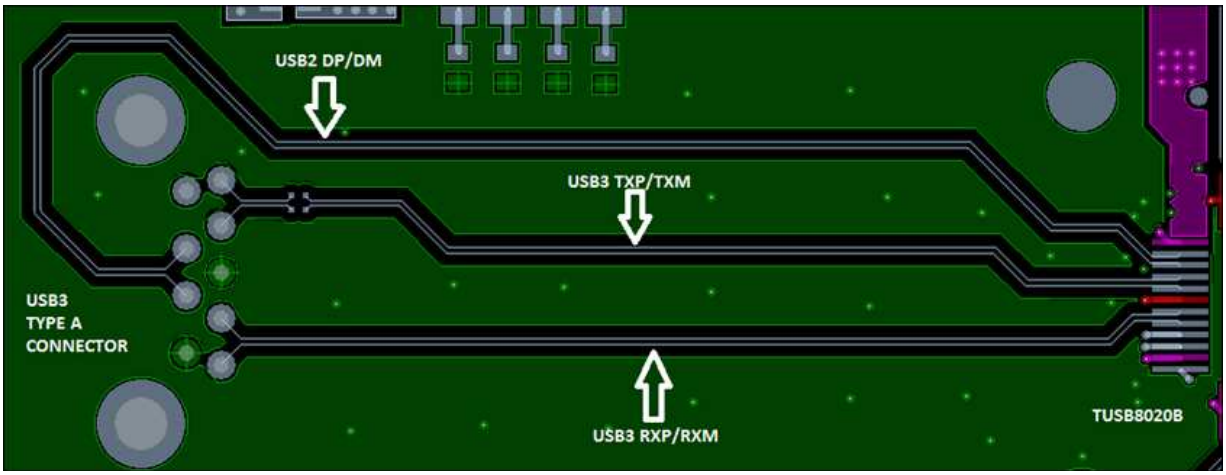
11.2 Layout Example

11.2.1 Upstream Port

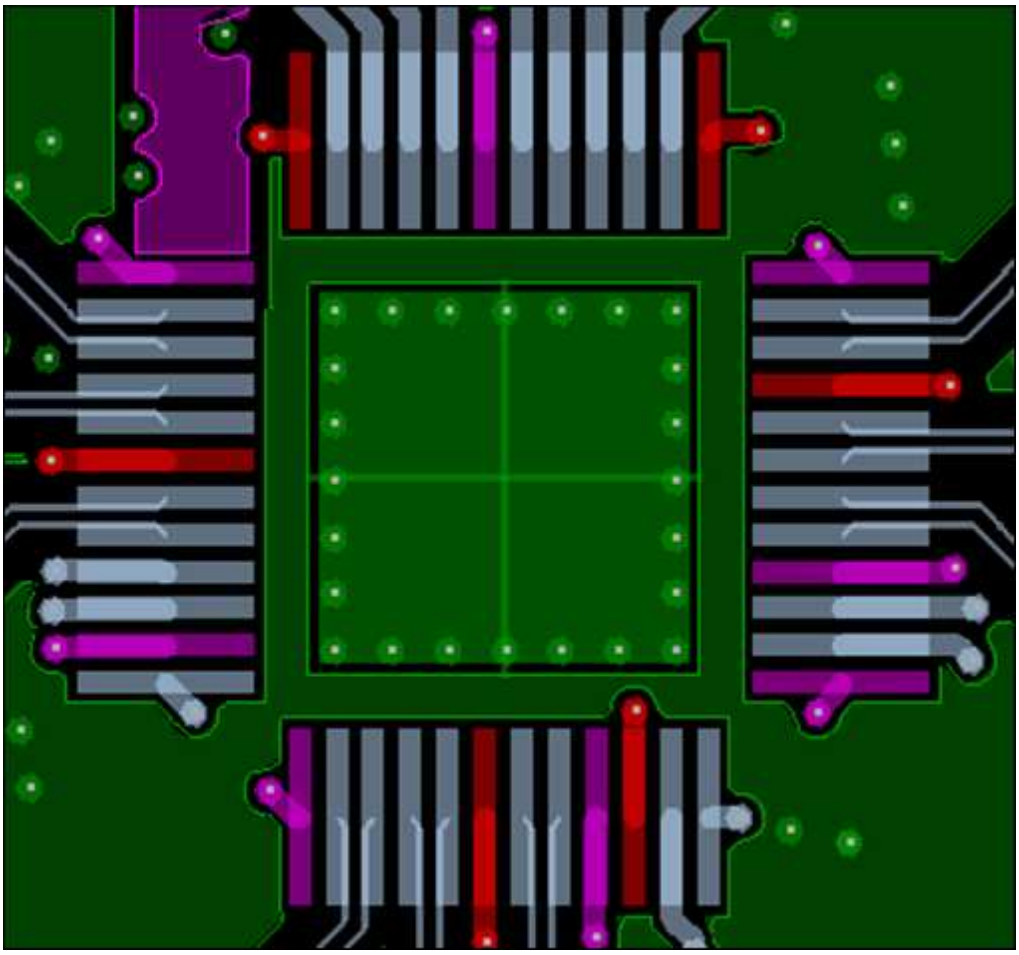


Layout Example (continued)

11.2.2 Downstream Port



11.2.3 Thermal Pad



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12 Device and Documentation Support

12.1 Trademarks

All trademarks are the property of their respective owners.

12.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TUSB8020BIPHP	ACTIVE	HTQFP	PHP	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	T8020BI	Samples
TUSB8020BIPHPR	ACTIVE	HTQFP	PHP	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	T8020BI	Samples
TUSB8020BPHP	ACTIVE	HTQFP	PHP	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	0 to 70	TUSB8020B	Samples
TUSB8020BPHPR	ACTIVE	HTQFP	PHP	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	0 to 70	TUSB8020B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TUSB8020B :

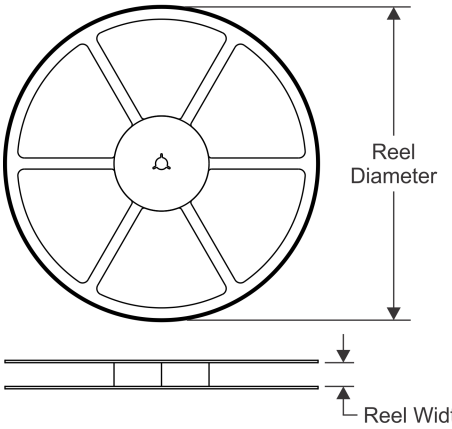
- Automotive: TUSB8020B-Q1

NOTE: Qualified Version Definitions:

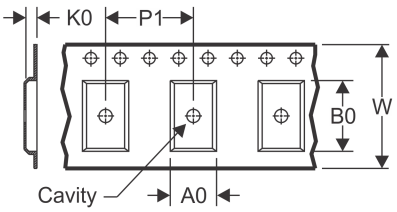
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

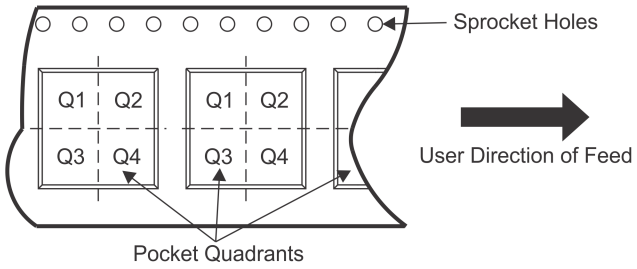


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

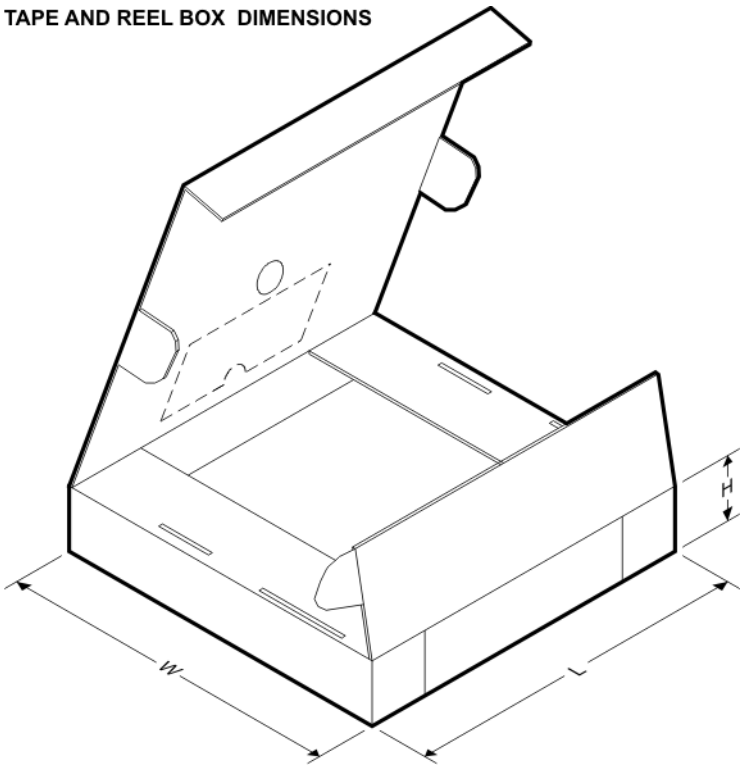
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TUSB8020BIPHPR	HTQFP	PHP	48	1000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2
TUSB8020BPHPR	HTQFP	PHP	48	1000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2

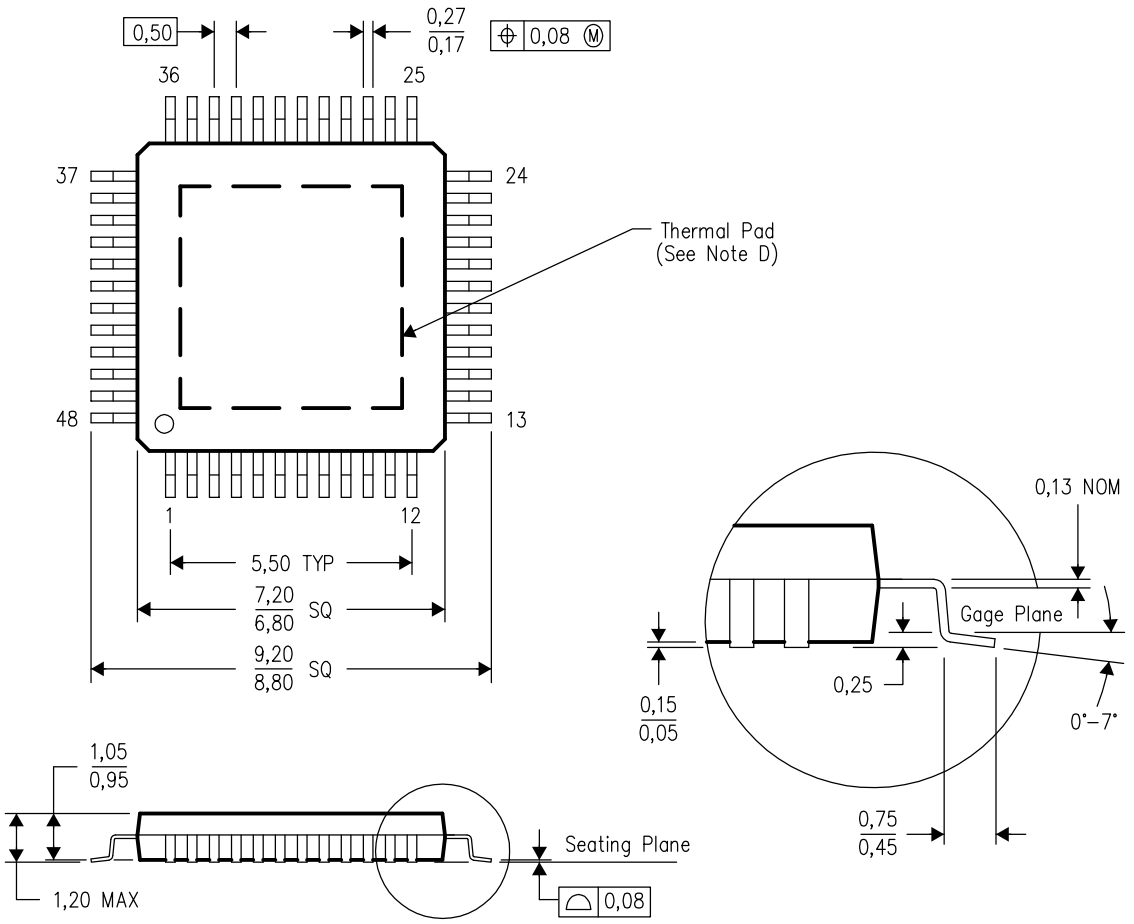
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TUSB8020BIPHPR	HTQFP	PHP	48	1000	336.6	336.6	31.8
TUSB8020BPHPR	HTQFP	PHP	48	1000	336.6	336.6	31.8

PHP (S–PQFP–G48) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. Falls within JEDEC MS–026

PowerPAD is a trademark of Texas Instruments.

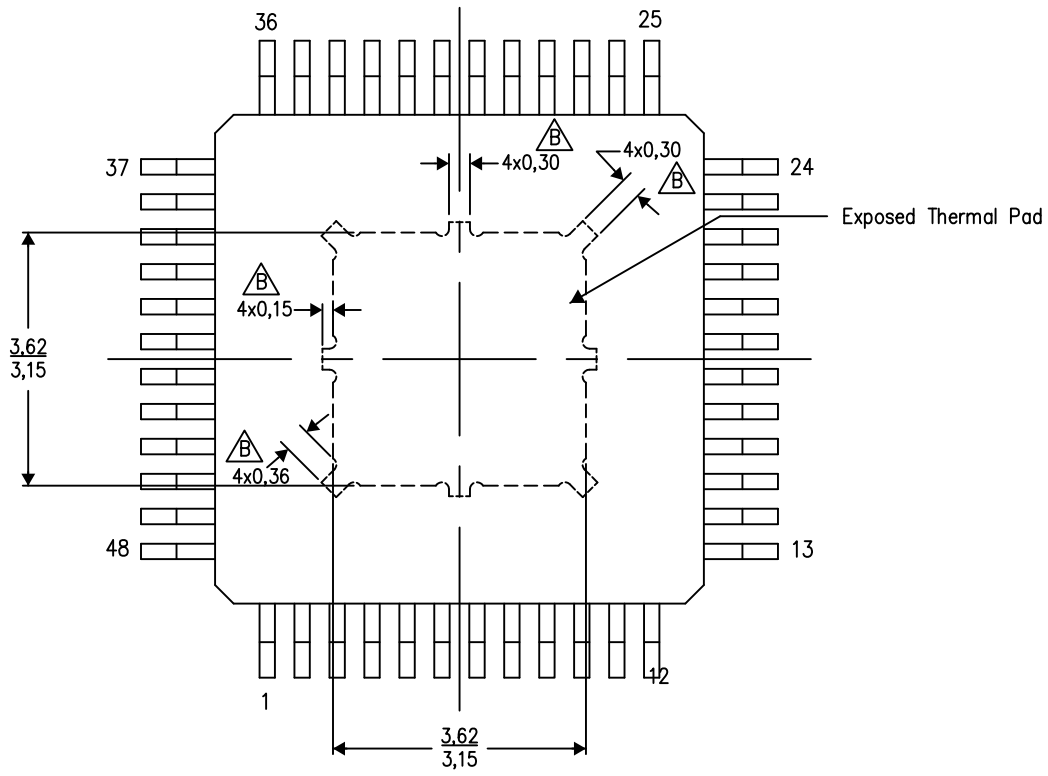
PHP (S–PQFP–G48) PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206329–13/P 03/15

NOTE: A. All linear dimensions are in millimeters

B Tie strap features may not be present.

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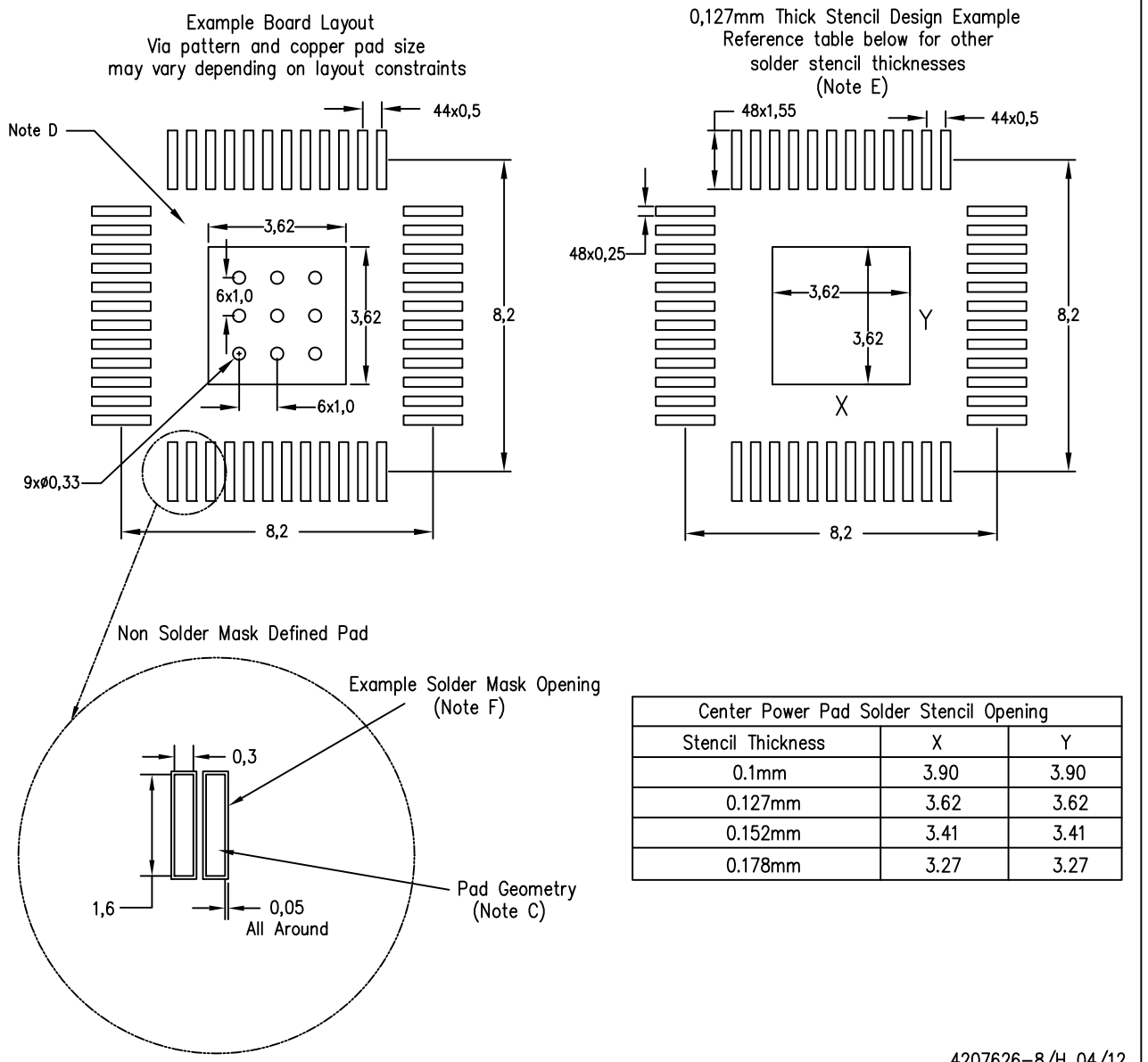
PHP (S–PQFP–G48) PowerPAD™ PLASTIC QUAD FLATPACK



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.90	3.90
0.127mm	3.62	3.62
0.152mm	3.41	3.41
0.178mm	3.27	3.27

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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting options for vias placed in the thermal pad.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
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