Precision CMOS Analog Switches

DESCRIPTION

The DG417, DG418, DG419 monolithic CMOS analog switches were designed to provide high performance switching of analog signals. Combining low power, low leakages, high speed, low on-resistance and small physical size, the DG417 series is ideally suited for portable and battery powered industrial and military applications requiring high performance and efficient use of board space.

To achieve high-voltage ratings and superior switching performance, the DG417 series is built on Vishay Siliconix's high voltage silicon gate (HVSG) process. Break-before-make is guaranteed for the DG419, which is an SPDT configuration. An epitaxial layer prevents latchup.

Each switch conducts equally well in both directions when on, and blocks up to the power supply level when off.

The DG417 and DG418 respond to opposite control logic levels as shown in the Truth Table.

FEATURES

- ± 15 V analog signal range
- On-resistance - $R_{DS(on)}$: 20 Ω
- Fast switching action - t_{ON}: 100 ns
- Ultra low power requirements - P_D: 35 nW
- TTL and CMOS compatible
- MiniDIP and SOIC packaging
- 44 V supply max. rating
- 44 V supply max. rating
- Compliant to RoHS directive 2002/95/EC

Pb-free Available
RoHS* COMPLIANT

BENEFITS

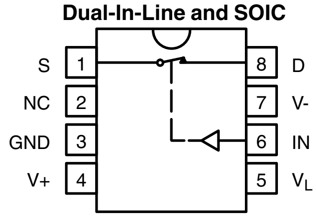
- Wide dynamic range
- Low signal errors and distortion
- Break-before-make switching action
- Simple interfacing
- Reduced board space
- Improved reliability

APPLICATIONS

- Precision test equipment
- Precision instrumentation
- Battery powered systems
- Sample-and-hold circuits
- Military radios
- Guidance and control systems
- Hard disk drives

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

DG417
Dual-In-Line and SOIC

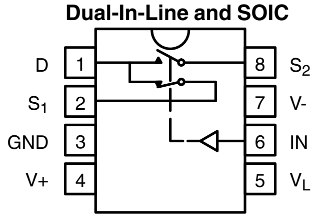


Top View

TRUTH TABLE		
Logic	**DG417**	**DG418**
0	ON	OFF
1	OFF	ON

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

DG419
Dual-In-Line and SOIC



Top View

TRUTH TABLE DG419		
Logic	**SW_1**	**SW_2**
0	ON	OFF
1	OFF	ON

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

* Pb containing terminations are not RoHS compliant, exemptions may apply

ORDERING INFORMATION

Temp. Range	Package	Part Number
DG417, DG418		
- 40 °C to 85 °C	8-Pin Plastic MiniDIP	DG417DJ DG417DJ-E3
		DG418DJ DG418DJ-E3
	8-Pin Narrow SOIC	DG417DY DG417DY-E3 DG417DY-T1 DG417DY-T1-E3
		DG418DY DG418DY-E3 DG418DY-T1 DG418DY-T1-E3
DG419		
- 40 °C to 85 °C	8-Pin Plastic MiniDIP	DG419DJ DG419DJ-E3
	8-Pin Narrow SOIC	DG419DY DG419DY-E3 DG419DY-T1 DG419DY-T1-E3

ABSOLUTE MAXIMUM RATINGS

Parameter (Voltages referenced to V-)		Limit	Unit
V+		44	V
GND		25	
V_L		(GND - 0.3) to (V+) + 0.3	
Digital Inputs[a], V_S, V_D		(V-) - 2 to (V+) + 2 or 30 mA, whichever occurs first	
Current , (Any Terminal) Continuous		30	mA
Current, S or D (Pulsed at 1 ms, 10 % Duty Cycle)		100	
Storage Temperature	(AK Suffix)	- 65 to 150	°C
	(DJ, DY Suffix)	- 65 to 125	
Power Dissipation (Package)[b]	8-Pin Plastic MiniDIP[c]	400	mW
	8-Pin Narrow SOIC[d]	400	
	8-Pin CerDIP[e]	600	

Notes:
a. Signals on S_X, D_X, or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC board.
c. Derate 6 mW/°C above 75 °C.
d. Derate 6.5 mW/°C above 75 °C.
e. Derate 12 mW/°C above 75 °C.

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S10-1528-Rev. G, 19-Jul-10

SCHEMATIC DIAGRAM Typical Channel

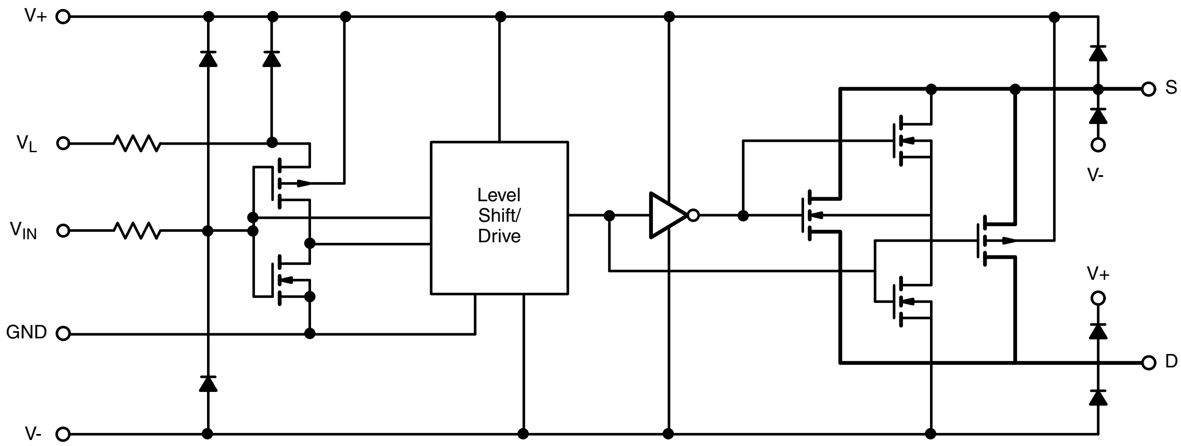


Figure 1.

SPECIFICATIONS[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V- = - 15 V V_L = 5 V, V_{IN} = 2.4 V, 0.8 V[f]		Temp.[b]	Typ.[c]	A Suffix - 55 °C to 125 °C Min.[d]	A Suffix - 55 °C to 125 °C Max.[d]	D Suffix - 40 °C to 85 °C Min.[d]	D Suffix - 40 °C to 85 °C Max.[d]	Unit
Analog Switch										
Analog Signal Range[e]	V_{ANALOG}			Full		- 15	15	- 15	15	V
Drain-Source On-Resistance	$R_{DS(on)}$	I_S = - 10 mA, V_D = ± 12.5 V V+ = 13.5 V, V- = - 13.5 V		Room Full	20		35 45		35 45	Ω
Switch Off Leakage Current	$I_{S(off)}$	V+ = 16.5, V- = - 16.5 V V_D = ± 15.5 V V_S = ± 15.5 V		Room Full	- 0.1	- 0.25 - 20	0.25 20	- 0.25 - 5	0.25 5	nA
	$I_{D(off)}$		DG417 DG418	Room Full	- 0.1	- 0.25 - 20	0.25 20	- 0.25 - 5	0.25 5	
			DG419	Room Full	- 0.1	- 0.75 - 60	0.75 60	- 0.75 - 12	0.75 12	
Channel Off Leakage Current	$I_{D(on)}$	V+ = 16.5 V, V- = - 16.5 V V_S = V_D = ± 15.5 V	DG417 DG418	Room Full	- 0.4	- 0.4 - 40	0.4 40	- 0.4 - 10	0.4 10	
			DG419	Room Full	- 0.4	- 0.75 - 60	0.75 60	- 0.75 - 12	0.75 12	
Digital Control										
Input Current V_{IN} Low	I_{IL}			Full	0.005	- 0.5	0.5	- 0.5	0.5	µA
Input Current V_{IN} High	I_{IH}			Full	0.005	- 0.5	0.5	- 0.5	0.5	
Dynamic Characteristics										
Turn-On Time	t_{ON}	R_L = 300 Ω, C_L = 35 pF V_S = ± 10 V See Switching Time Test Circuit	DG417 DG418	Room Full	100		175 250		175 250	ns
Turn-Off Time	t_{OFF}		DG417 DG418	Room Full	60		145 210		145 210	
Transition Time	t_{TRANS}	R_L = 300 Ω, C_L = 35 pF V_{S1} = ± 10 V, V_{S2} = ± 10 V	DG419	Room Full			175 250		175 250	
Break-Before-Make Time Delay (DG403)	t_D	R_L = 300 Ω, C_L = 35 pF V_{S1} = V_{S2} = ± 10 V	DG419	Room	13	5		5		
Charge Injection	Q	C_L = 10 nF, V_{gen} = 0 V, R_{gen} = 0 Ω		Room	60					pC

SPECIFICATIONS[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V- = - 15 V V_L = 5 V, V_{IN} = 2.4 V, 0.8 V[f]	Temp.[b]	Typ.[c]	A Suffix - 55 °C to 125 °C Min.[d]	A Suffix - 55 °C to 125 °C Max.[d]	D Suffix - 40 °C to 85 °C Min.[d]	D Suffix - 40 °C to 85 °C Max.[d]	Unit
Dynamic Characteristics									
Source Off Capacitance	$C_{S(off)}$	f = 1 MHz, V_S = 0 V	Room	8					pF
Drain Off Capacitance	$C_{D(off)}$	f = 1 MHz, V_S = 0 V; DG417 DG418	Room	8					pF
Channel On Capacitance	$C_{D(on)}$	f = 1 MHz, V_S = 0 V; DG417 DG418	Room	30					pF
		DG419	Room	35					pF
Power Supplies									
Positive Supply Current	I+	V+ = 16.5 V, V- = - 16.5 V V_{IN} = 0 or 5 V	Room Full	0.001		1 5		1 5	µA
Negative Supply Current	I-		Room Full	- 0.001	- 1 - 5		- 1 - 5		µA
Logic Supply Current	I_L		Room Full	0.001		1 5		1 5	µA
Ground Current	I_{GND}		Room Full	- 0.0001	- 1 - 5		- 1 - 5		µA

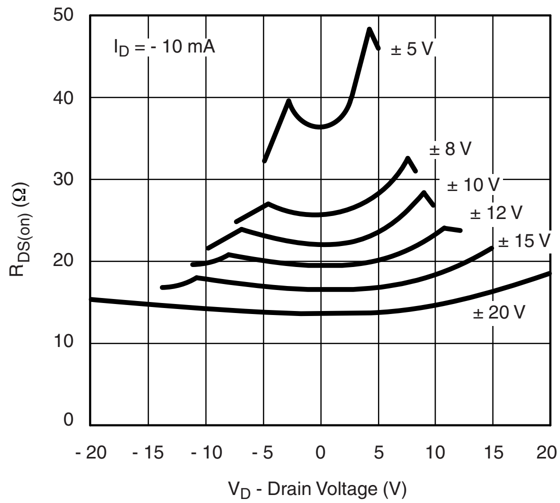
SPECIFICATIONS[a] for Unipolar Supplies

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 12 V, V- = 0 V V_L = 5 V, V_{IN} = 2.4 V, 0.8 V[f]	Temp.[b]	Typ.[c]	A Suffix - 55 °C to 125 °C Min.[d]	A Suffix - 55 °C to 125 °C Max.[d]	D Suffix - 40 °C to 85 °C Min.[d]	D Suffix - 40 °C to 85 °C Max.[d]	Unit
Analog Switch									
Analog Signal Range[e]	V_{ANALOG}		Full		0	12	0	12	V
Drain-Source On-Resistance	$R_{DS(on)}$	I_S = - 10 mA, V_D = 3.8 V V+ = 10.8 V	Room	40					Ω
Dynamic Characteristics									
Turn-On Time	t_{ON}	R_L = 300 Ω, C_L = 35 pF, V_S = 8 V See Switching Time Test Circuit	Room	110					ns
Turn-Off Time	t_{OFF}		Room	40					ns
Break-Before-Make Time Delay	t_D	DG419 Only R_L = 300 Ω, C_L = 35 pF	Room	60					ns
Charge Injection	Q	C_L = 10 nF, V_{gen} = 0 V, R_{gen} = 0 Ω	Room	5					pC
Power Supplies									
Positive Supply Current	I+	V+ = 13.2 V, V_L = 5.25 V V_{IN} = 0 or 5 V	Room	0.001					µA
Negative Supply Current	I-		Room	- 0.001					µA
Logic Supply Current	I_L		Room	0.001					µA
Ground Current	I_{GND}		Room	- 0.001					µA

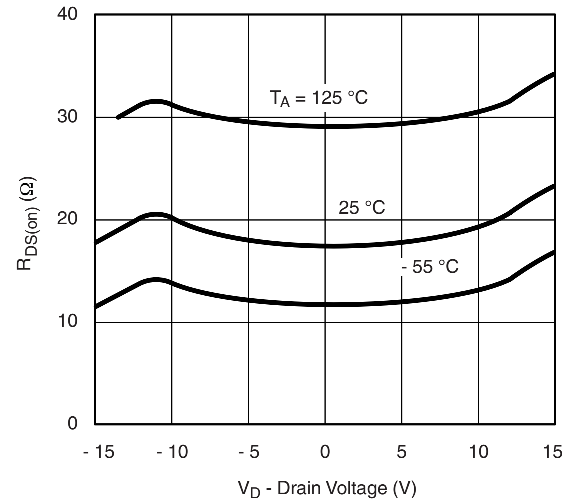
Notes:
a. Refer to Process Option Flowchart.
b. Room = 25 °C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

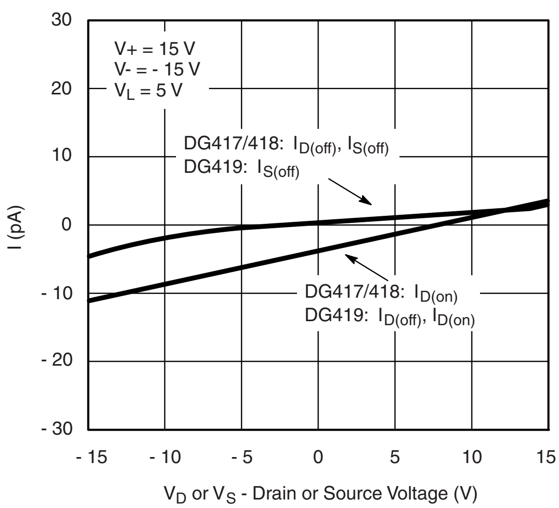
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



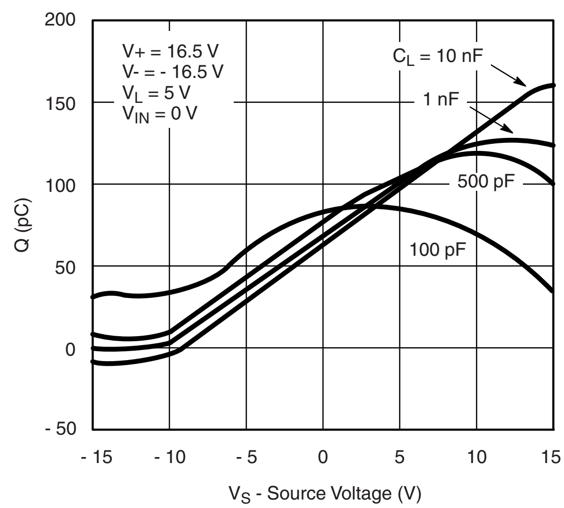
$R_{DS(on)}$ vs. V_D and Supply Voltage



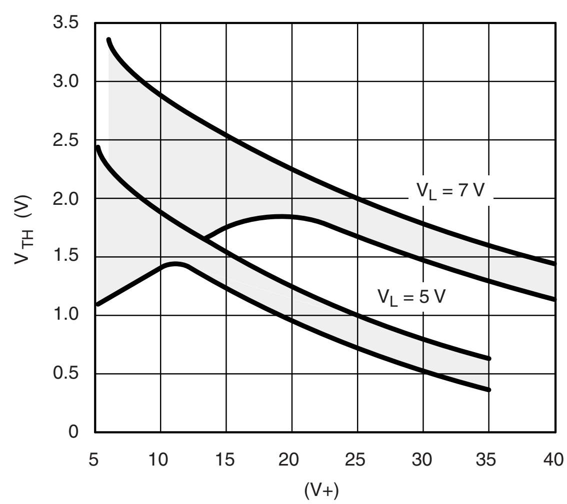
$R_{DS(on)}$ vs. Temperature



Leakage Currents vs. Analog Voltage

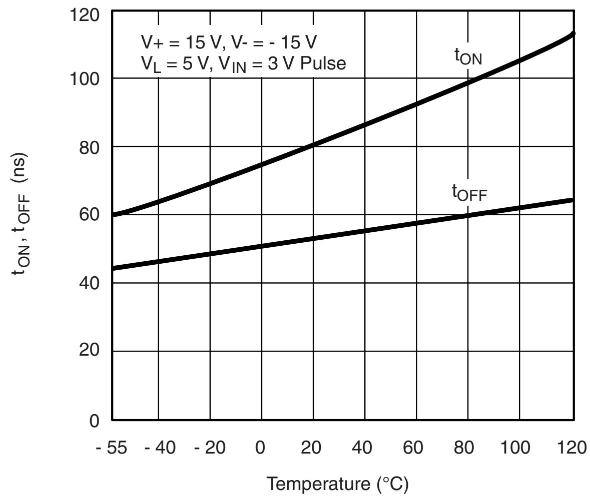


Drain Charge Injection

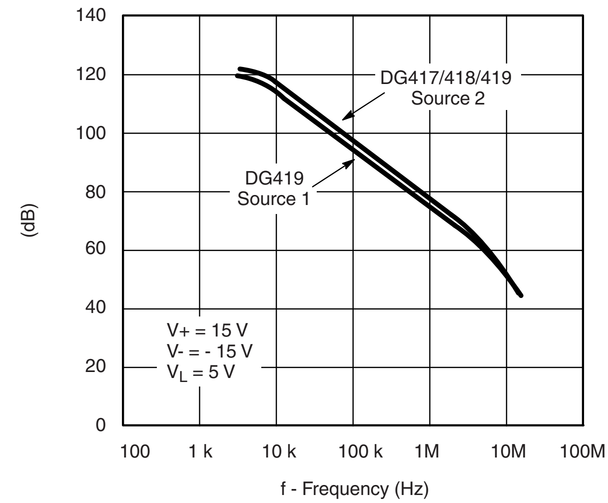


Input Switching Threshold vs. Supply Voltages

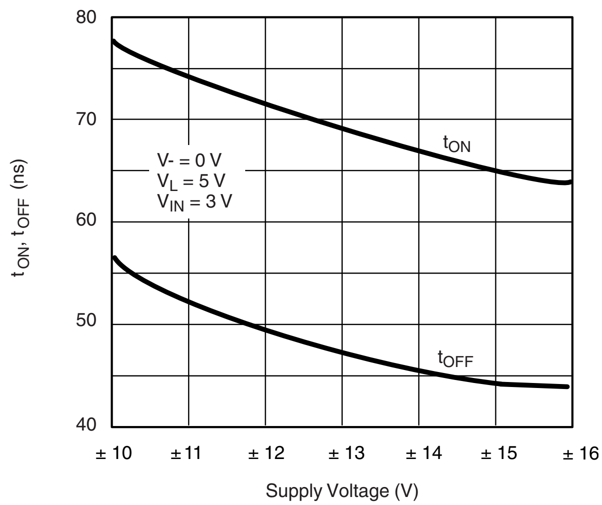
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



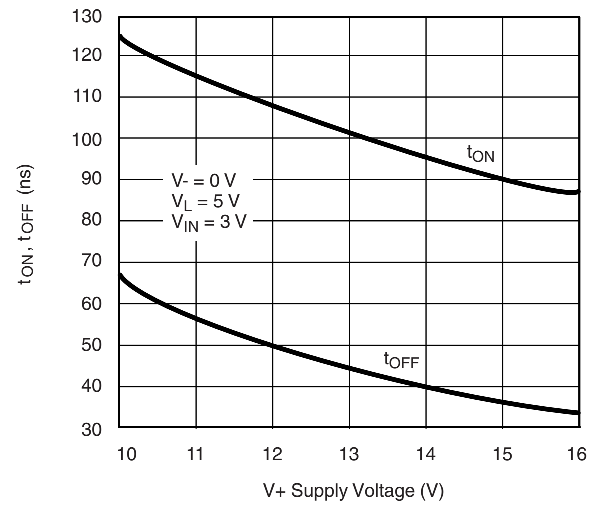
Switching Time vs. Temperature



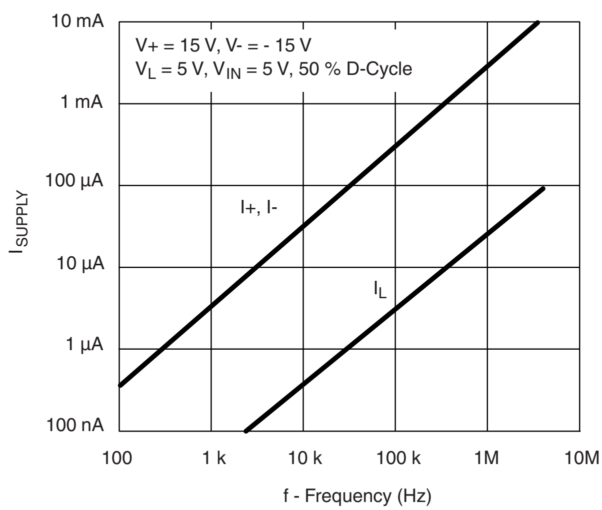
Crosstalk and Off Isolation vs. Frequency



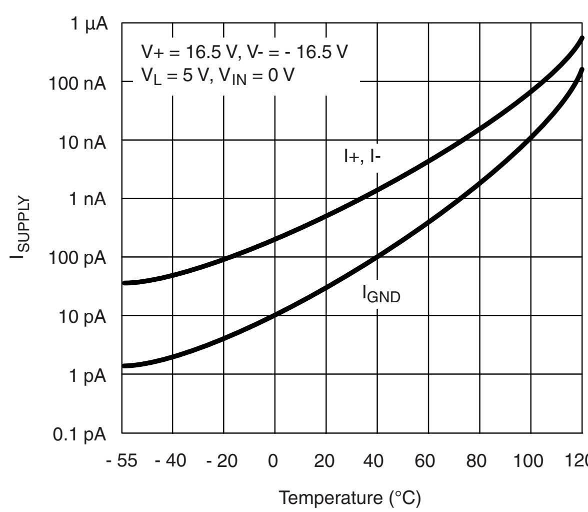
Switching Time vs. Supply Voltages



Switching Time vs. V+



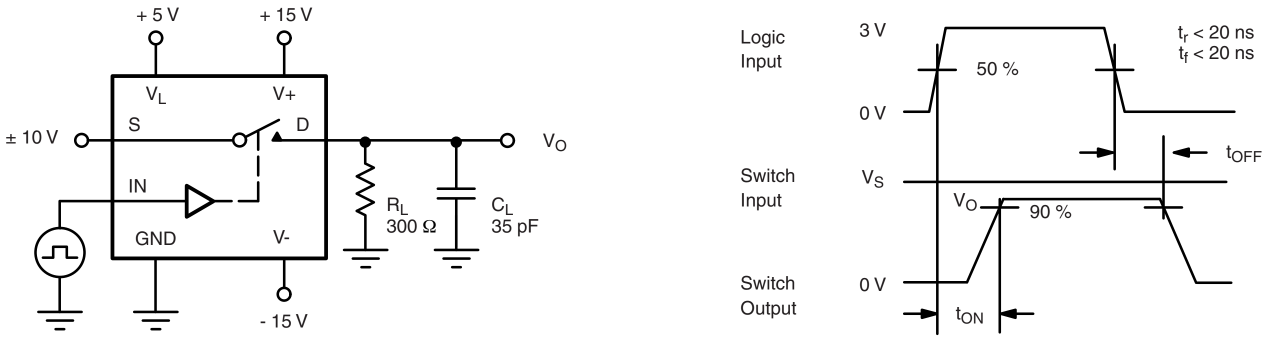
Power Supply Currents vs. Switching Frequency



Supply Current vs. Temperature

TEST CIRCUITS

V_O is the steady state output with the switch on.



C_L (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$

Note: Logic input waveform is inverted for switches that have the opposite logic sense.

Figure 2. Switching Time (DG417, DG418)

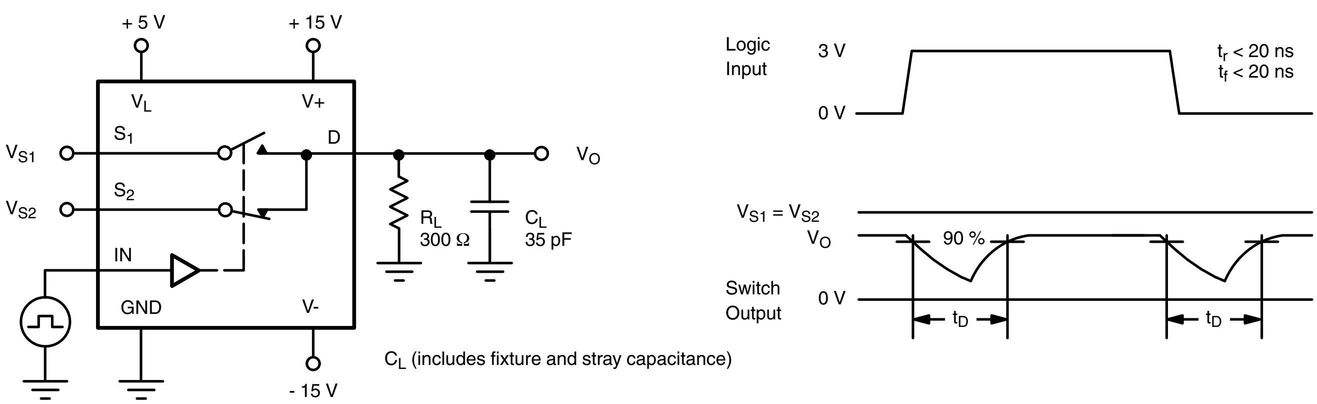
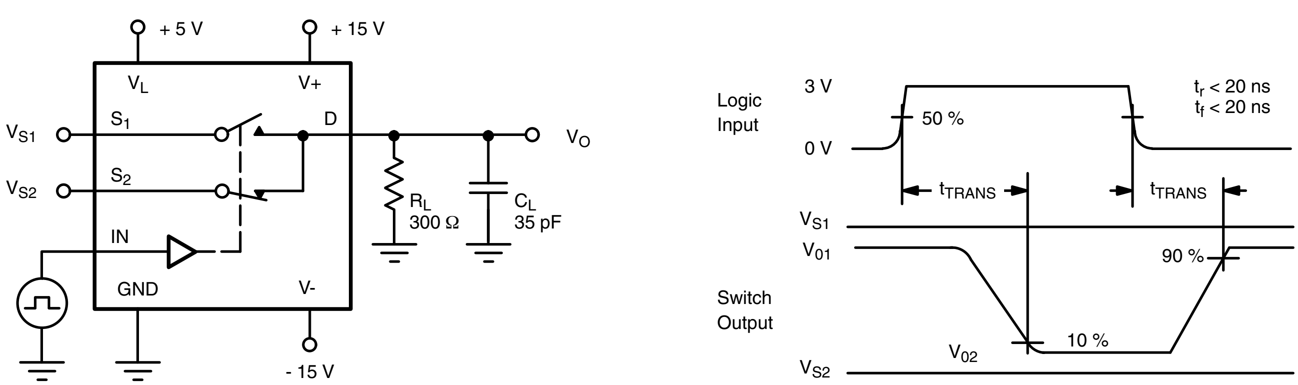


Figure 3. Break-Before-Make (DG419)



C_L (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$

Figure 4. Transition Time (DG419)

TEST CIRCUITS

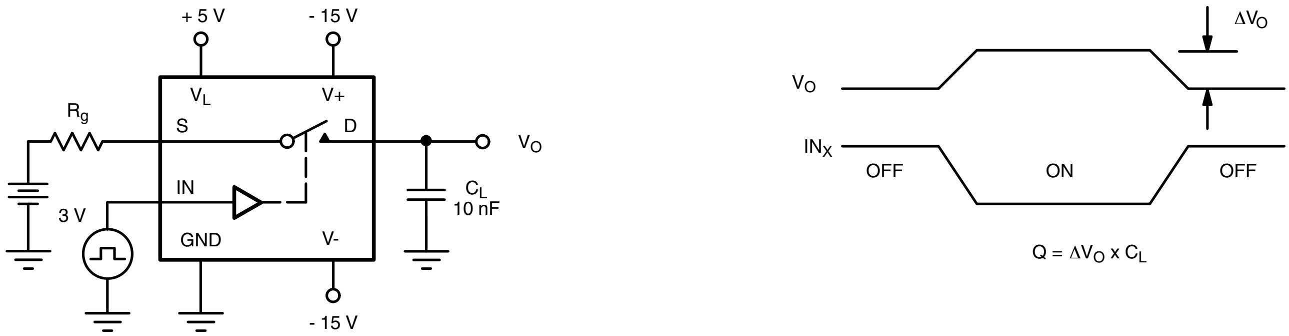
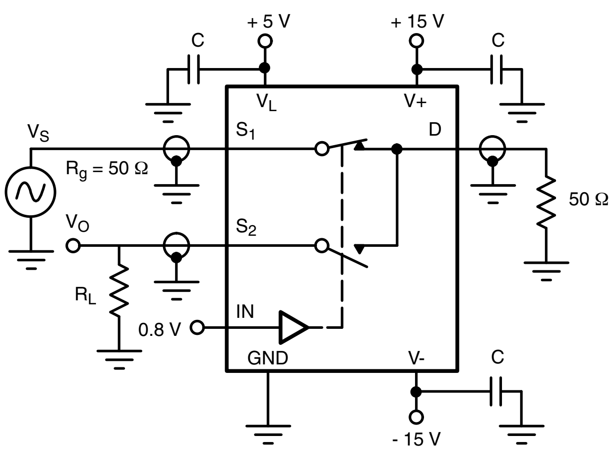


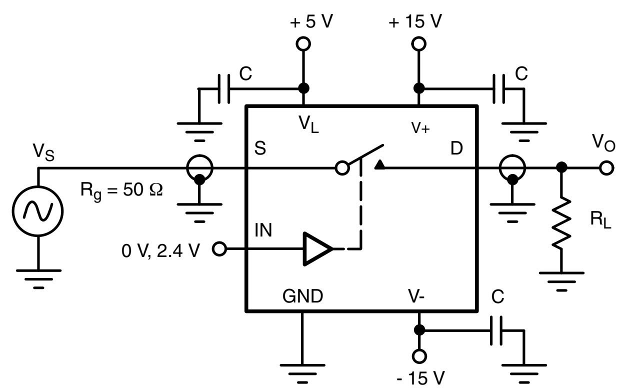
Figure 5. Charge Injection



$$X_{TALK}\ \text{Isolation} = 20 \log \left| \frac{V_S}{V_O} \right|$$

C = RF bypass

Figure 6. Crosstalk (DG419)



$$\text{Off Isolation} = 20 \log \left| \frac{V_S}{V_O} \right|$$

Figure 7. Off Isolation

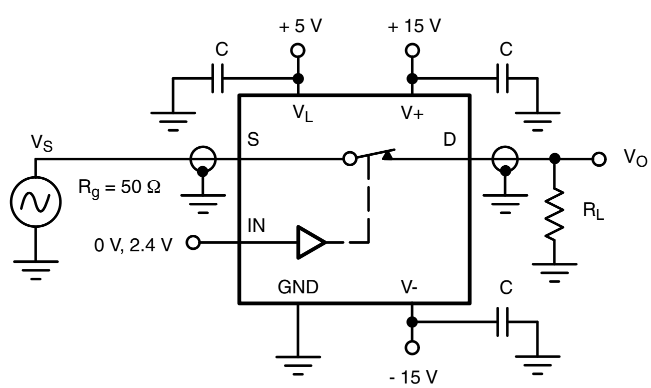


Figure 8. Insertion Loss

TEST CIRCUITS

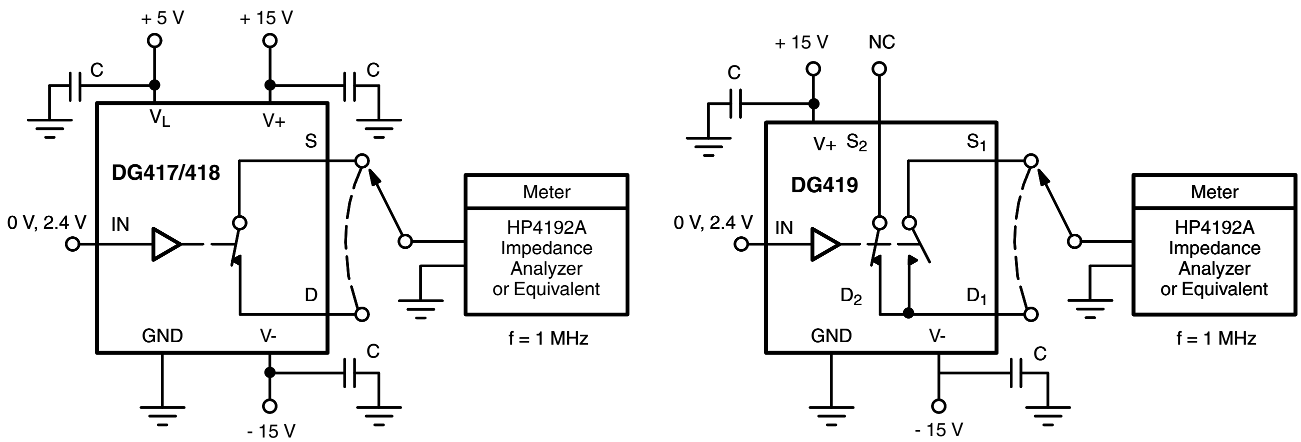


Figure 9. Source/Drain Capacitances

APPLICATIONS

Switched Signal Powers Analog Switch

The analog switch in Figure 10 derives power from its input signal, provided the input signal amplitude exceeds 4 V and its frequency exceeds 1 kHz.

This circuit is useful when signals have to be routed to either of two remote loads. Only three conductors are required: one for the signal to be switched, one for the control signal and a common return.

A positive input pulse turns on the clamping diode D_1 and charges C_1. The charge stored on C_1 is used to power the chip; operation is satisfactory because the switch requires less than 1 µA of stand-by supply current. Loading of the signal source is imperceptible. The DG419's on-resistance is a low 100 Ω for a 5 V input signal.

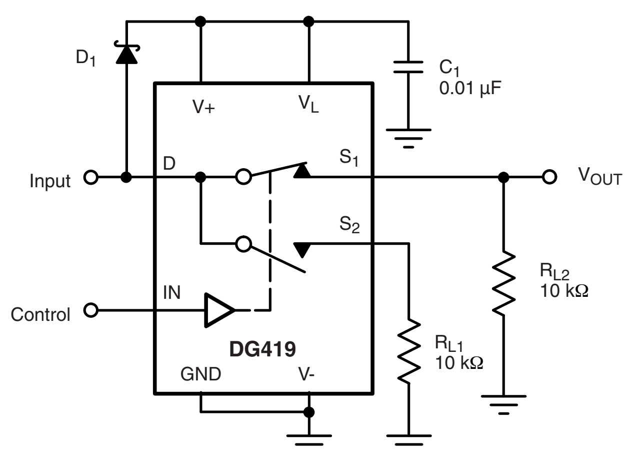


Figure 10. Switched Signal Powers Remote SPDT Analog Switch

APPLICATIONS

Micropower UPS Transfer Switch

When V_{CC} drops to 3.3 V, the DG417 changes states, closing SW_1 and connecting the backup cell, as shown in Figure 10. D_1 prevents current from leaking back towards the rest of the circuit. Current consumption by the CMOS analog switch is around 100 pA; this ensures that most of the power available is applied to the memory, where it is really needed. In the stand-by mode, hundreds of A are sufficient to retain memory data.

When the 5 V supply comes back up, the resistor divider senses the presence of at least 3.5 V, and causes a new change of state in the analog switch, restoring normal operation.

Programmable Gain Amplifier

The DG419, as shown in figure 11, allows accurate gain selection in a small package. Switching into virtual ground reduces distortion caused by $R_{DS(on)}$ variation as a function of analog signal amplitude.

GaAs FET Driver

The DG419, as shown in figure 12 may be used as a GaAs FET driver. It translates a TTL control signal into - 8 V, 0 V level outputs to drive the gate.

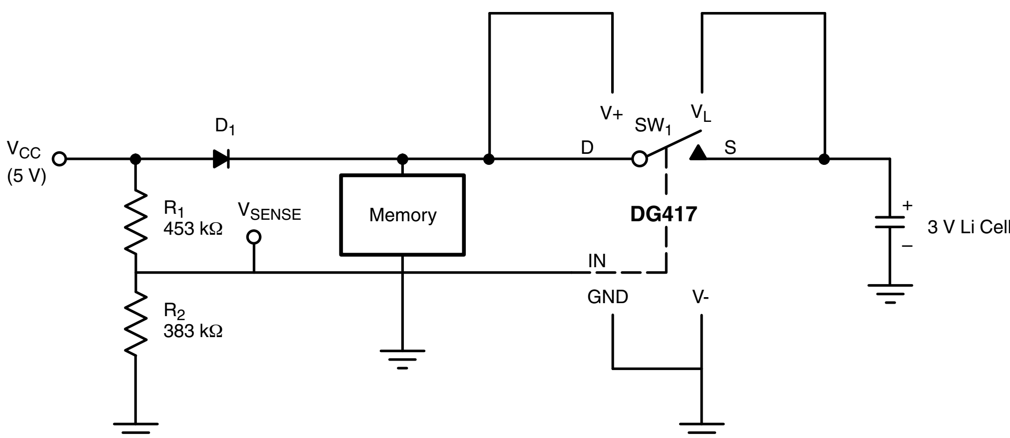


Figure 11. Micropower UPS Circuit

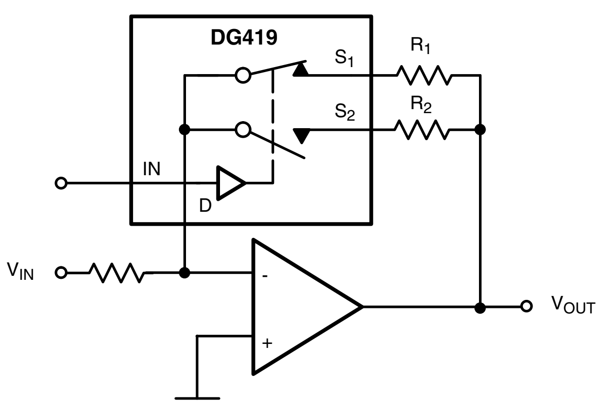


Figure 12. Programmable Gain Amplifier

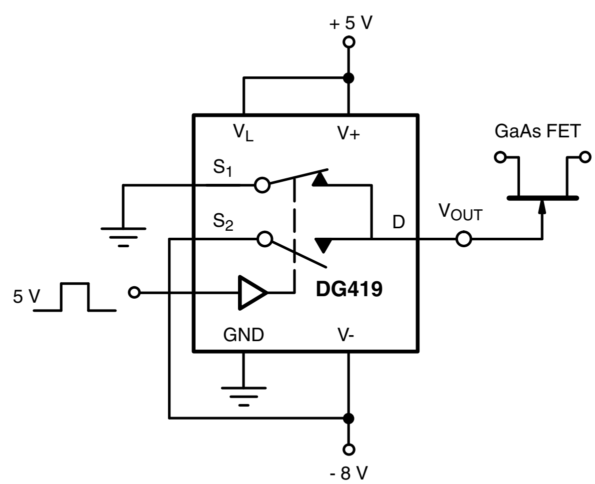
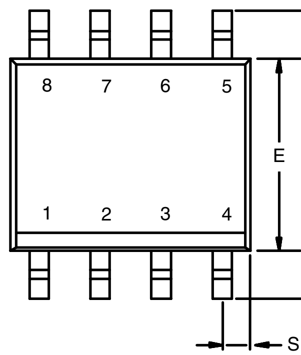
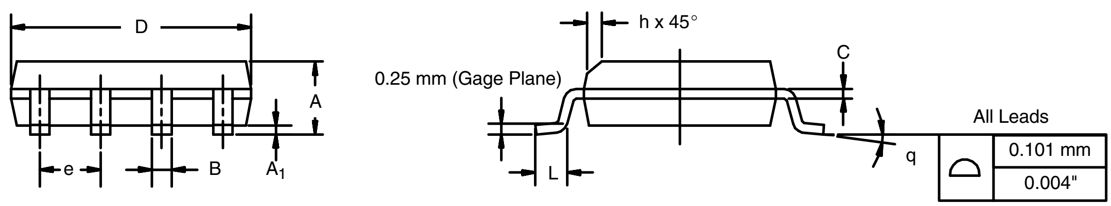


Figure 13. GaAs FET Driver

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?70051.

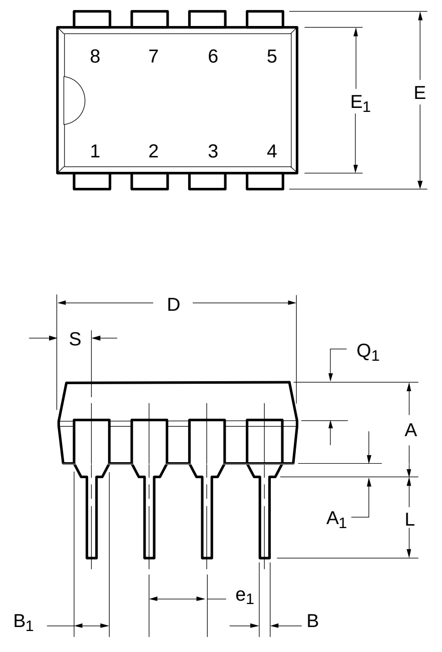
SOIC (NARROW): 8-LEAD
JEDEC Part Number: MS-012

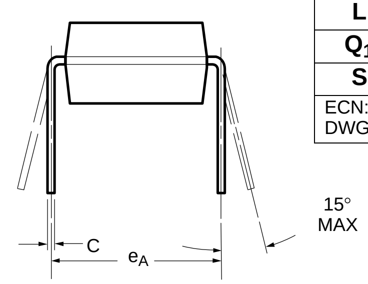




DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A_1	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06 DWG: 5498				

PDIP: 8-LEAD

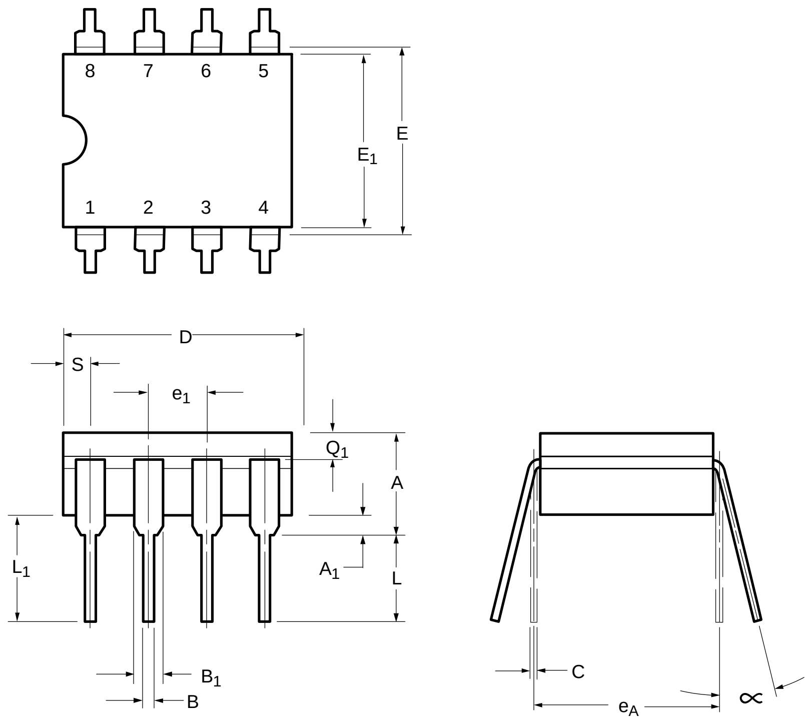




Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	3.81	5.08	0.150	0.200
A_1	0.38	1.27	0.015	0.050
B	0.38	0.51	0.015	0.020
B_1	0.89	1.65	0.035	0.065
C	0.20	0.30	0.008	0.012
D	9.02	10.92	0.355	0.430
E	7.62	8.26	0.300	0.325
E_1	5.59	7.11	0.220	0.280
e_1	2.29	2.79	0.090	0.110
e_A	7.37	7.87	0.290	0.310
L	2.79	3.81	0.110	0.150
Q_1	1.27	2.03	0.050	0.080
S	0.76	1.65	0.030	0.065
ECN: S-03946—Rev. E, 09-Jul-01 DWG: 5478				

NOTE: End leads may be half leads.

CERDIP: 8-LEAD



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	4.06	5.08	0.160	0.200
A_1	0.51	1.14	0.020	0.045
B	0.38	0.51	0.015	0.020
B_1	1.14	1.65	0.045	0.065
C	0.20	0.30	0.008	0.012
D	9.40	10.16	0.370	0.400
E	7.62	8.26	0.300	0.325
E_1	6.60	7.62	0.260	0.300
e_1	2.54 BSC		0.100 BSC	
e_A	7.62 BSC		0.300 BSC	
L	3.18	3.81	0.125	0.150
L_1	3.18	5.08	0.150	0.200
Q_1	1.27	2.16	0.050	0.085
S	0.64	1.52	0.025	0.060
∝	0°	15°	0°	15°
ECN: S-03946—Rev. C, 09-Jul-01 DWG: 5348				

Mounting LITTLE FOOT®, SO-8 Power MOSFETs

Wharton McDaniel

Surface-mounted LITTLE FOOT power MOSFETs use integrated circuit and small-signal packages which have been been modified to provide the heat transfer capabilities required by power devices. Leadframe materials and design, molding compounds, and die attach materials have been changed, while the footprint of the packages remains the same.

See Application Note 826, *Recommended Minimum Pad Patterns With Outline Drawing Access for Vishay Siliconix MOSFETs*, (http://www.vishay.com/ppg?72286), for the basis of the pad design for a LITTLE FOOT SO-8 power MOSFET. In converting this recommended minimum pad to the pad set for a power MOSFET, designers must make two connections: an electrical connection and a thermal connection, to draw heat away from the package.

In the case of the SO-8 package, the thermal connections are very simple. Pins 5, 6, 7, and 8 are the drain of the MOSFET for a single MOSFET package and are connected together. In a dual package, pins 5 and 6 are one drain, and pins 7 and 8 are the other drain. For a small-signal device or integrated circuit, typical connections would be made with traces that are 0.020 inches wide. Since the drain pins serve the additional function of providing the thermal connection to the package, this level of connection is inadequate. The total cross section of the copper may be adequate to carry the current required for the application, but it presents a large thermal impedance. Also, heat spreads in a circular fashion from the heat source. In this case the drain pins are the heat sources when looking at heat spread on the PC board.

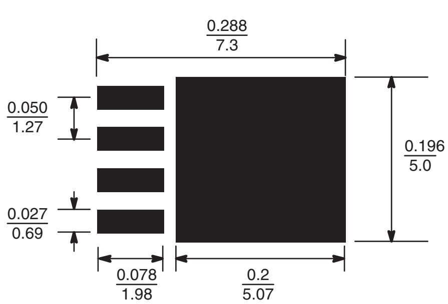


Figure 1. Single MOSFET SO-8 Pad Pattern With Copper Spreading

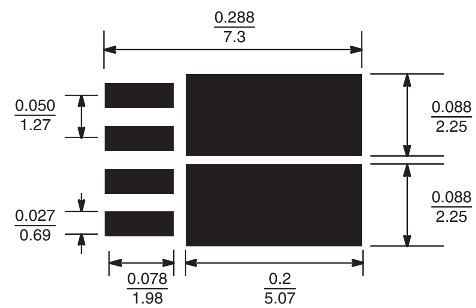


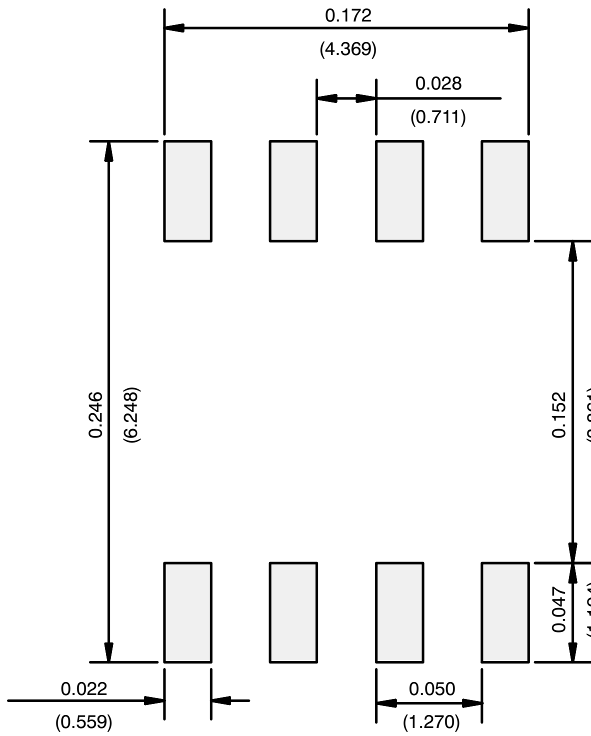
Figure 2. Dual MOSFET SO-8 Pad Pattern With Copper Spreading

The minimum recommended pad patterns for the single-MOSFET SO-8 with copper spreading (Figure 1) and dual-MOSFET SO-8 with copper spreading (Figure 2) show the starting point for utilizing the board area available for the heat-spreading copper. To create this pattern, a plane of copper overlies the drain pins. The copper plane connects the drain pins electrically, but more importantly provides planar copper to draw heat from the drain leads and start the process of spreading the heat so it can be dissipated into the ambient air. These patterns use all the available area underneath the body for this purpose.

Since surface-mounted packages are small, and reflow soldering is the most common way in which these are affixed to the PC board, “thermal” connections from the planar copper to the pads have not been used. Even if additional planar copper area is used, there should be no problems in the soldering process. The actual solder connections are defined by the solder mask openings. By combining the basic footprint with the copper plane on the drain pins, the solder mask generation occurs automatically.

A final item to keep in mind is the width of the power traces. The absolute minimum power trace width must be determined by the amount of current it has to carry. For thermal reasons, this minimum width should be at least 0.020 inches. The use of wide traces connected to the drain plane provides a low impedance path for heat to move away from the device.

RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads
Dimensions in Inches/(mm)

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