TOSHIBA BIPOLAR LINEAR INTEGRATED CIRCUIT SILICON MONOLITHIC

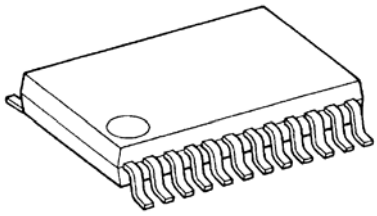
TA1395FNG

Mixer/Oscillator and PLL IC for TV/VCR Tuner

The TA1395FNG is a tuner IC for TV and VCR applications that integrates a PLL block and mixer, oscillator and IF amplifier on a single chip.

The control data of the PLL block conforms to I²C-bus formats.

Small flat package: SSOP24 (0.65 mm pitch)



SSOP24-P-300-0.65A

Weight: 0.09 g (typ.)

Features

- Vcc: 5V (typ.)
- Two-band mixer
- Two-band oscillator
- IF output driver
- Asymmetrical IF output
- I²C bus format control
- 33-V high voltage tuning amplifier built-in
- Three-bit bandswitch drive transistor
- Frequency steps: 31.25 kHz, 50 kHz, 62.5 kHz (when a 4 MHz crystal is used)
- Four-programmable chip address
- Power on reset circuit
- Automatic changeover between 1/4 and 1/2 prescaler through data input
- Standby mode
- Package: Pb-free

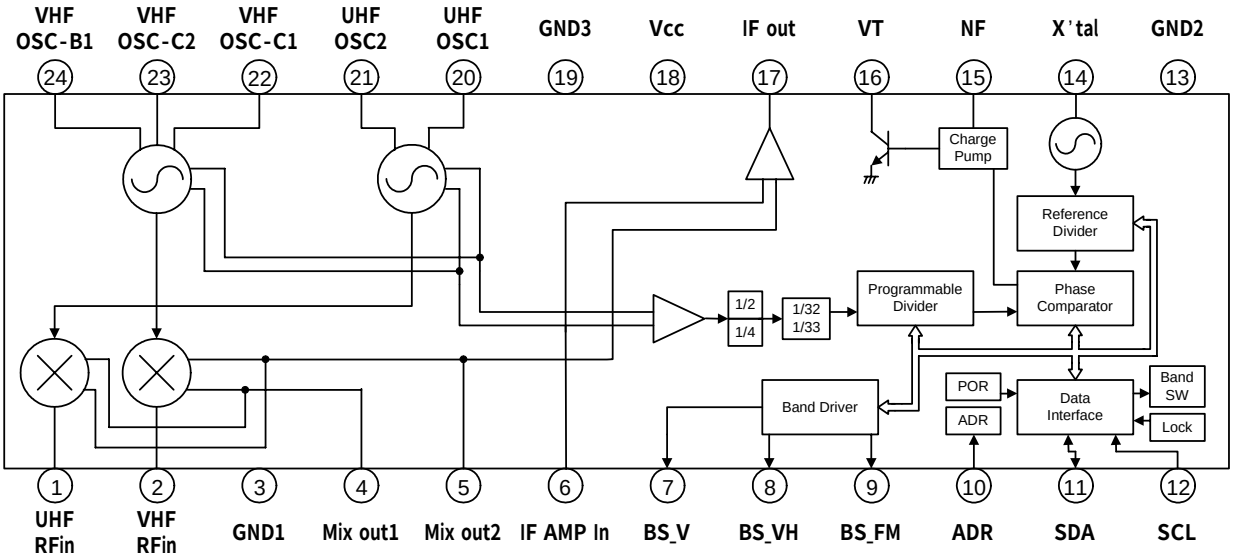
Power on reset status

- Frequency step: 62.5 kHz
- Charge pump current: Low
- Counter data: ALL [0]
- Band driver: OFF
- Tuning amplifier: OFF (charge pump is sink mode)
- Local oscillator and mixer: UHF mode

note1: This device is easy to be damaged by high voltage or electric fields. In regards to this, please handle with care.

note2: Install the product correctly. Otherwise, it may result in break down, damage and/or degration to the product or equipment.

Block Diagram



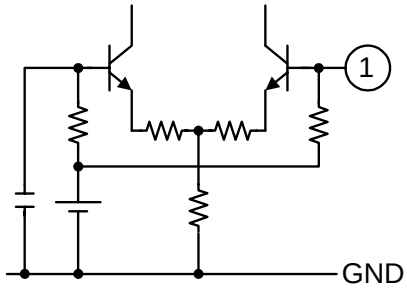
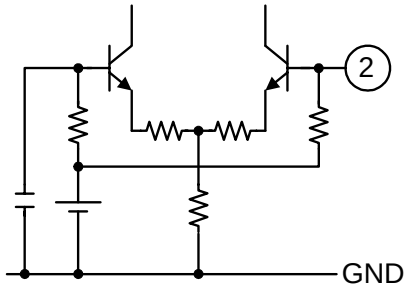
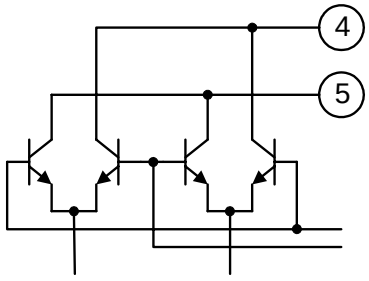
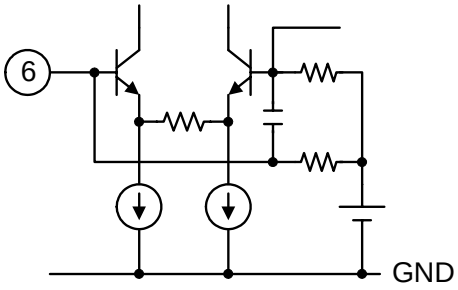
Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

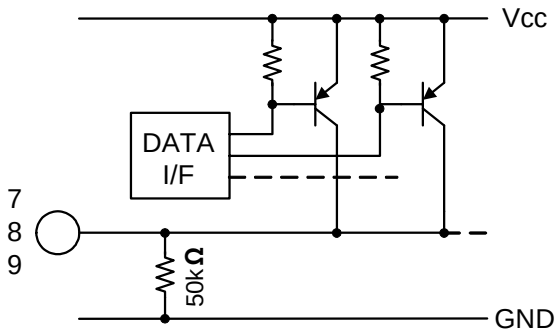
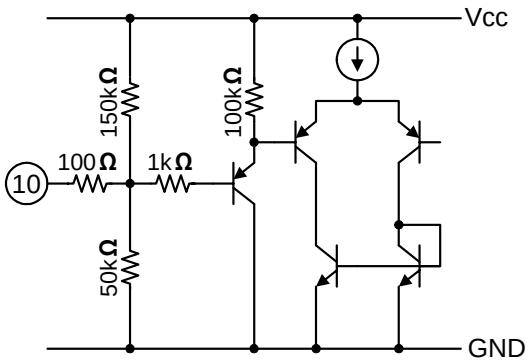
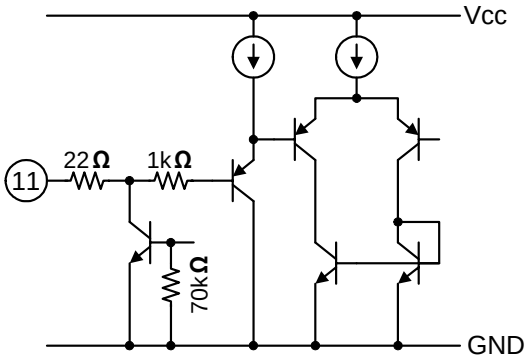
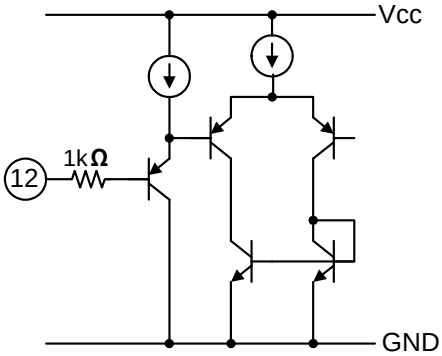
Terminal Name

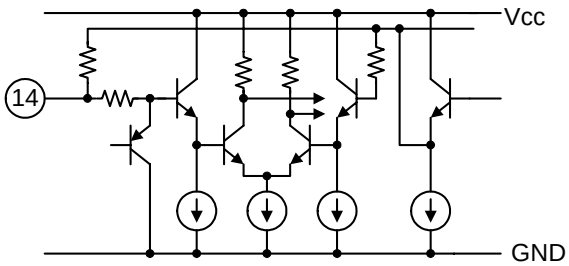
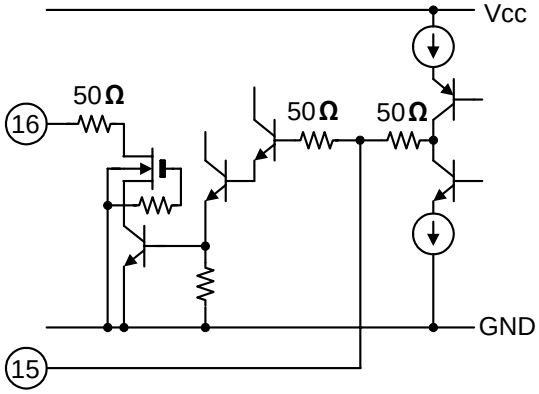
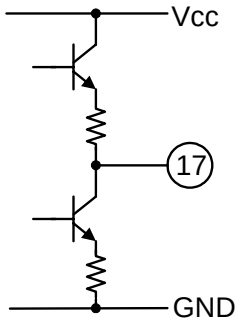
Pin No.	Pin Name
1	UHF RF input
2	VHF RF input
3	GND 1
4	Mixer output 1
5	Mixer output 2
6	IF AMP input
7	Band output port : BS_V
8	Band output port : BS_VH
9	Band output port : BS_FM
10	ADR (address setting)
11	SDA in/output
12	SCL input
13	GND 2
14	Crystal input
15	NF
16	Vt output
17	IF output
18	Vcc
19	GND 3
20	UHF oscillator 1
21	UHF oscillator 2
22	VHF oscillator –C1
23	VHF oscillator –C2
24	VHF oscillator –B1

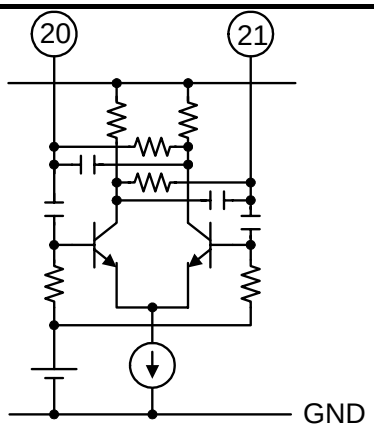
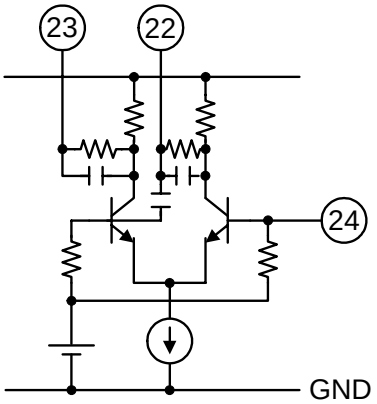
Terminal Function

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

Pin No.	Pin Name.	Function	Interface
1	UHF RF Input	RF signal input pin for the UHF band. Asymmetrical input type	
2	VHF RF Input	RF signal input pin for the VHF band. Asymmetrical input type	
3	GND 1	Ground pin	–
4 5	Mixer Output	Mixer output pins A tank circuit is connected between the pins for tuning. Since these are open collector outputs, be sure to connect with a power supply through a load (resistance, coil).	
6	IF Amp Input	IF AMP input pin This pin and a pin4 are connected through a capacity.	

Pin No.	Pin Name.	Function	Interface
7 8 9	BS_V BS_VH BS_FM	The output port of the band block can be set up using the bandswitch data. Bear in mind that drive current differs according to each band drive port.	
10	ADR	Address setting pin The address of the PLL block is set up using the voltage applied to this pin.	
11	SDA	Serial data input and output pin	
12	SCL	Serial clock input pin	
13	GND 2	Ground pin	–

Pin No.	Pin Name.	Function	Interface
14	Crystal Input	Crystal oscillator input pin. A 4-MHz crystal is used.	
15	NF	Be sure to connect a resistance (of about 33 kΩ) between pin 16 and the 33-V external power supply for tuning. To prevent abnormal oscillation, connect between pin 16 and GND a capacity element that does not affect a PLL.	
16	Vt Output		
17	IF Output	IF signal output pin Asymmetrical output type. Output impedance is about 75Ω.	
18	Vcc	Power supply pin	–
19	GND 3	Ground pin	–

Pin No.	Pin Name.	Function	Interface
20 21	UHF Oscillator	Local oscillator for the UHF band The oscillator type is symmetrical amplifier.	
22 23 24	VHF Oscillator	Local oscillator for the VHF band The oscillator type is symmetrical amplifier.	

Maximum Ratings

CHARACTERISTIC	PIN No	SYMBOL	RATING	UNIT
Vcc	18	Vcc	6	V
Tuning Amplifier Voltage Applied	16	VBT	38	V
Input terminal voltage	—	VIN	GND-0.3~Vcc+0.3	V
Power Dissipation	—	PD	890 (note4)	mW
Operating Temperature	—	Topr	-20~85	℃
Junction Temperature	—	Tj	150	℃
Storage Temperature	-	Tstg	-55~150	℃

note3: The absolute maximum ratings of a semiconductor device are a set of specified parameter values that must not beexceeded during operation, even for an instant. If any of these rating are exceeded during operation, the electrical characteristics of the device may be irreparably altered, in which case the reliability and lifetime of the device can no longer be guaranteed. Moreover, any exceeding of the ratings during operation may cause breakdown, damage and/or degradation in other equipment. Applications using the device should be designed so that no maximum rating will ever be exceeded under any operating conditions. Before using, creating and/or producing designs, refer to and comply with the precautions and conditions set forth in this documents.

note4: 50 × 50 × 1.6 mm, Cu 40% board used. When using the device at above Ta = 25℃, decrease the power dissipation by 7.2 mW for each increase of 1℃.

Operating Supply Voltage

Pin No.	SYMBOL	MIN.	TYP.	MAX.	UNIT
18	Vcc	4.5	5.0	5.5	V

Electric Characteristics

(Unless otherwise specified, Vcc = 5 V, Ta = 25℃)

CHARACTERISTICS	SYMBOL	TEST CIRCUIT	BAND	TEST CONDITION (note5, 6)	MIN.	TYP.	MAX.	UNIT
Power Supply and Current	Icc-1	1	VHF	B1 = ON (BS_VH=open)	52	65	78	mA
	Icc-2		UHF	B3 = ON (BS_FM=open)	53	66	79	
	Icc-3		-	Power Save setting	6	9	12	
Conversion Gain (see 1)	CG	2	VHF	RF = 55.25 MHz -40 dBmWin	21	24	27	dB
			VHF	RF = 367.25 MHz -40 dBmWin	22	25	28	
			UHF	RF = 373.25 MHz -40 dBmWin	26	29	32	
			UHF	RF = 801.25 MHz -40 dBmWin	27	30	33	
IF Output Power Level (see 2)	Ifp	2	VHF	RF = 55.25 MHz	8.5	11.0	—	dBmW
			VHF	RF = 367.25 MHz	8.5	11.0	—	
			UHF	RF = 373.25 MHz	8.5	11.0	—	
			UHF	RF = 801.25 MHz	8.5	11.0	—	
Conversion Gain Shift (see 3)	CGs	2	VHF	RF = 55.25 MHz -35 dBmWin	—	—	± 0.5	dB
			VHF	RF = 367.25 MHz -35 dBmWin	—	—	± 0.5	
			UHF	RF = 373.25 MHz -35 dBmWin	—	—	± 0.5	
			UHF	RF = 801.25 MHz -35 dBmWin	—	—	± 0.5	
Band Port Drive Current BS_V	IBD-V	1	—	Pin 7, maximum drive current	—	—	5	mA
Band Port Drive Current BS_VH	IBD-VH	1	—	Pin 8, maximum drive current	—	—	10	mA
Band Port Drive Current BS_FM	IBD-FM	1	—	Pin 9, maximum drive current	—	—	5	mA
Band Port Drive Maximum Current	IBD-MAX	1	—	Maximum drive current / 2 port ON	—	—	15	mA
Band Port Drive Voltage Drop	VBDsat	1	—	With each port at maximum current drive. 1 port ON	—	0.15	0.2	V
Tuning Amplifier Output Voltage (Close Loop)	Vt out	1	—	Isink = 1.5 mA	0.3	—	33	V
Tuning Amplifier Maximum Current	Ivt	1	—	VBT = 33 V	—	—	1.5	mA
Crystal Negative Resistance	XtR	1	—	4-MHz crystal used	1	2	—	kΩ
Ratio Setting Range	N	-	—	15-bit counter	1024	—	32767	Ratio
Logic Input Low Voltage	VBsL	1	—	SDA, SCL pin	- 0.3	—	1.5	V
Logic Input High Voltage	VBsH	1	—	SDA, SCL pin	2.7	—	Vcc +0.3	V
Logic Input Current (Low)	I BsL	1	—	SDA, SCL pin	- 20	—	10	μA
Logic Input Current (High)	I BsH	1	—	SDA, SCL pin	- 10	—	20	μA
Charge Pump Output Current	Ichg	1	—	CP = 0	±40	±55	±70	μA
			—	CP = 1	±190	±250	±310	
ACK Output Voltage	VACK	1	—	Isink = 3 mA	—	—	0.4	V

note5: IF output frequency: 45.75 MHz note6: IF output load: 75 Ω

Reference Data

(Unless otherwise specified, Vcc = 5 V, Ta = 25℃)

This data is a reference value and is not guaranteed.

CHARACTERISTICS	SYMBOL	TEST CIRCUIT	BAND	TEST CONDITION (note5,6)	MIN.	TYP.	MAX.	UNIT
Noise Figure (see 4)	NF	2, 3	VHF	RF = 55.25 MHz, DSB	—	12.0	14.0	dB
			VHF	RF = 367.25 MHz, DSB	—	11.0	13.0	
			UHF	RF = 373.25 MHz, DSB	—	8.5	10.5	
			UHF	RF = 801.25 MHz, DSB	—	9.0	11.0	
Frequency Shift (The PLL is not operating.) (see 5)	fB	2	VHF	OSC = 101 MHz	—	—	±50	kHz
			VHF	OSC = 413 MHz	—	—	±200	
			UHF	OSC = 419 MHz	—	—	±150	
			UHF	OSC = 847 MHz	—	—	±700	
Switch On Drift (The PLL is not operating.) (see 6)	Δfs	2	VHF	OSC = 101 MHz	—	—	±250	kHz
			VHF	OSC = 413 MHz	—	—	±1350	
			UHF	OSC = 419 MHz	—	—	±450	
			UHF	OSC = 847 MHz	—	—	±1550	
1% Cross Modulation (see 7)	CM	2, 4	VHF	fd = 55.25 MHz, -40dBmWin	- 25	- 21	—	dBmW
			VHF	fd = 367.25 MHz, -40dBmWin	- 28	- 24	—	
			UHF	fd = 373.25 MHz, -40dBmWin	- 30	- 26	—	
			UHF	fd = 801.25 MHz, -40dBmWin	- 31	- 27	—	
C / S Beat (see 8)	IM3	2, 4	VHF	fd = 55.25 MHz, -10dBmWout	65	70	—	dBc
			VHF	fd = 367.25 MHz, -10dBmWout	65	70	—	
			UHF	fd = 373.25 MHz, -10dBmWout	65	70	—	
			UHF	fd = 801.25 MHz, -10dBmWout	65	70	—	
Ch Beat (see 9)	Ch5	2, 4	VHF	fp = 77.25MHz, fud = 83.25MHz Lo = 123MHz	62	67	—	dBc
	Ch6			fp = 83.25MHz, fud = 87.75MHz Lo = 129MHz	66	71	—	
	chA-5			fp = 91.25MHz Lo = 137MHz	65	70	—	
RF Input Maximum Level Without Lock-out	RF-in	2	VHF	Pin 2	—	—	10	dBmW
			UHF	Pin 1				
Crystal External Input Minimum Level	Xo extl-l	1	—	4-MHz signal input	300	—	—	mVp-p
Crystal External Input Maximum Level	Xo extl-h	1	—	4-MHz signal input	—	—	650	mVp-p
Crystal External Input Frequency	Xo extf	1	—	D / U is above 10dB	—	4	—	MHz

note5: IF output frequency: 45.75 MHz note6: IF output load: 75 Ω

I²C Bus Line Characteristic

CHARACTERISTICS	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
SCL Clock Frequency	fscl	–	0	-	400	kHz
Bus Free Time between a STOP and a START Condition	tBUF		1.3	-	-	μs
Hold Time (Repeated) START Condition	tHD;STA		0.6	-	-	μs
Low Period of the SCL Clock	tLOW		1.3	-	-	μs
High Period of the SCL Clock	tHIGH		0.6	-	-	μs
Set-up Time for a Repeated START Condition	tSU;STA		0.6	-	-	μs
Data Hold Time	tHD;DAT		0	-	0.9	μs
Data Set-up Time	tSU;DAT		100	-	-	μs
Rise Time of both SDA and SCL Signal	tR		-	-	300	μs
Fall Time of both SDA and SCL Signals	tF		-	-	300	μs
Set up Time for STOP Condition	tsU;STO		0.6	-	-	μs

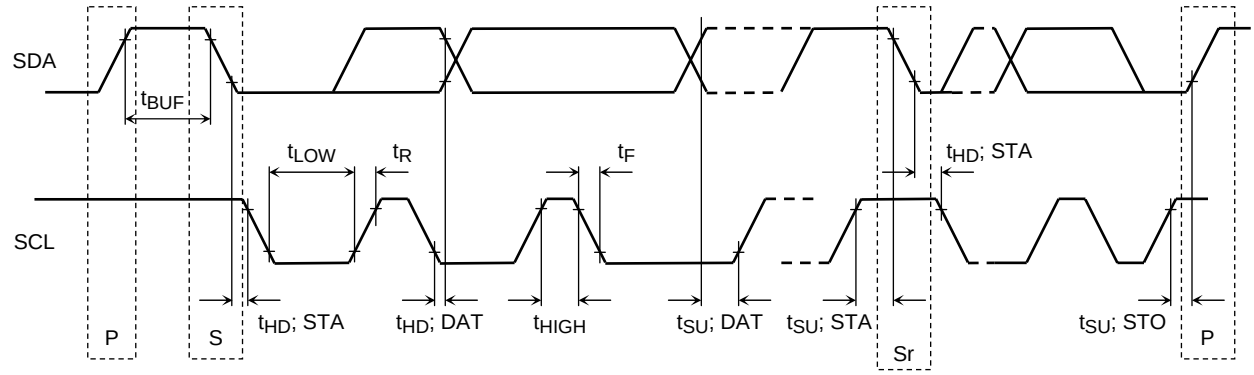


Figure 1: I²C-bus data timing chart (falling edge timing)

Timing charts may be simplified for explanatory purposes.

Test Conditions

Conversion Gain (see 1)
RF Input level = -40dBmW (untuned)

IF Output Power Level (see 2)
Measure IF output level when it is maximum level.

Conversion Gain Shift (see 3)
The conversion gain shift is defined as a change in conversion gain when supply voltage varies from Vcc = 5 V to 4.5 V or from Vcc = 5 V to 5.5 V.

Noise Figure (see 4)
Noise figure meter used. Direct reading. (DSB)

Frequency Shift (the PLL is not operating) (see 5)
The frequency shift is defined as a change in oscillator frequency when supply voltage varies from Vcc = 5 V to 4.5 V or from Vcc = 5 V to 5.5 V.

Switch On Drift (the PLL is not operating) (see 6)
It is frequency change of oscillator by three minutes on the basis of the three seconds back of an after a power supply.

1% Cross Modulation (see 7)
- fd = fp : (fd input level = -40dBmW)
- fud = fp ±12MHz, 100 kHz AM30%

Input two signals, and increase the fud input level.
Measure the fud input level when the suppression level reaches 56.5dB.

C/S Beat (see 8)
- fp
- fs = fp + 4.5MHz
- fc = fp + 3.58MHz

fp = fs = fc : 3 signal are same level input
Measure the suppression level when the PIF(45.75MHz) level is -10dBmW output.

Ch Beat (see 9)
*Ch5 beat
- fp = 77.25MHz
- fud = 83.25MHz

Lo = 123MHz tuning
Beat frequency = fud × 2 – Lo = 43.5MHz
fp = fud : 2 signal are same level input
Measure the suppression level when the PIF(45.75MHz) level is -10dBmW output.

*Ch6 beat
- fp = 83.25MHz
- fs = 87.75MHz

Lo = 129MHz tuning
Beat frequency = fp + fs – Lo = 42MHz
fp = fs : 2 signal are same level input
Measure the suppression level when the PIF(45.75MHz) level is -10dBmW output.

*ChA-5 beat
- fp = 91.25MHz

Lo = 137MHz tuning
Beat frequency = Lo – fp × 2 = 45.5MHz
Measure the suppression level when the PIF(45.75MHz) level is -10dBmW output.

Description of PLL Block Operation

- I²C bus control -

The TA1395FNG conforms to the I²C-bus format.

I²C-bus mode enables two-way bus communications with Write Mode, which receives data, and Read Mode, which sends data.

Write Mode and Read Mode are set using the last bit (R/W bit) of the address byte. If the last address bit is set to [0], Write Mode is selected; if it is set to [1], Read Mode is selected.

Addresses can be set using the hardware bits, and four programmable addresses are available. With this setting, multiple frequency synthesizers can be used in the same I²C-bus. The address for the hardware bit setting can be selected by applying voltage to the address setting pin (ADR: pin 10).An address is selected according to the set bits.

If the correct address bytes are received, the serial data (SDA) line is "Low" during acknowledgment; when Write Mode is set, the serial data (SDA) line is "Low" during the next acknowledgment if the data byte is programmed. The IC is equipped with 1/2 and 1/4 built-in prescalers, and it is possible to change from one prescaler to the other using input data.

When a frequency step of 62.5 kHz is selected, the 1/2 prescaler operates with a divider ratio of 1024 to 4095, and the 1/4 prescaler operates with a divider ratio of 4096 to 32767.

When the frequency step selected is 31.25 kHz and 50 kHz, the 1/2 prescaler operates with a divider ratio of 1024 to 8191, and the 1/4 prescaler operates with a divider ratio of 8192 to 32767.

In addition, even if the prescaler is changed, the data is calculated in the internal circuit and is processed so that the comparison frequency in each the frequency step does not change.

For a frequency step of 62.5 kHz: 15.625 kHz comparison frequency

For a frequency step of 50 kHz: 12.5 kHz comparison frequency

For a frequency step of 31.25 kHz: 7.8125 kHz comparison frequency

This IC incorporates a built-in power-on reset circuit for which a detection voltage of approximately 1.4 V has been set. When the Vcc is supplied, a delay or stoppage in a power supply voltage close to this detection voltage may cause the power-on reset circuit to malfunction, in which case there is a risk that some data may not be received even after the recommended voltage has been restored.

A) Write Mode (Setting Command)

When WRITE mode is set so that the different types of information may be received, byte 1 is used to specify the address data; byte 2 and byte 3, the frequency data; byte 4, function setting data such as the divider ratio setting; and byte 5, the output port data (bandswitch data).

Data are latched and transferred one after the other in the case of byte 3, byte 4 and byte 5, while byte 2 and byte 3 are latched and transferred as a two-byte set (byte 2 + byte 3).

Once a correct address is received and acknowledged, the data type is determined by whether the first bit of the next byte is set to [0] or [1]. [0] indicates frequency data, while [1] indicates function setting or output data.

Until the I²C-bus STOP CONDITION is detected, the additional data can be input without transmitting the address data again. (For example: Frequency sweep is possible with additional frequency data.)

If data transmission is aborted, data programmed before the abort are valid.

BYTE 1

Hardware bit setting of byte 1 is possible using the address data.
The hardware bit is set with the voltage applied to the address-setting pin (ADR: pin 10).

BYTE 2, BYTE 3

Byte 2 , byte 3 are stored in the 15-bit shift register with counter data for the frequency setting, and control the 15-bit programmable counter ratio.

The program frequency can be calculated in the following formula:

$$fosc = 4 \times fr \times N.$$

fosc	: Program frequency
4	: Prescaler
fr	: Phase comparator reference frequency
N	: Counter total divider ratio

fr is calculated using the crystal oscillator and the reference frequency divider ratio set in byte 4 (control byte): fr = crystal oscillator frequency / reference divider ratio.

The reference frequency divider ratio can be set to 1/512, 1/320, and 1/256.

When using a 4-MHz crystal oscillator, fr = 7.8125 kHz, 12.5 kHz, and 15.625 kHz.

The step frequency is 31.25 kHz, 50.0 kHz, and 62.5 kHz.

BYTE 4

Byte 4 is a control byte used to set the different functions. Bit 2 (CP) and controls the output current of the charge-pump circuit. When bit 2 is set to [0], the output current is set to ±55 μA; when it is set to [1] , it is ±250 μA.

Bit 3 (T2), bit 4 (T1), and bit 5 (T0) are used to set charge pump, the phase comparator reference signal output and counter divider output in test mode. (For details of test mode, see the test mode setting table.)

Bit 6 (Rsa) and bit 7 (Rsb) are used to set the crystal reference frequency divider ratio. (For details of the crystal reference frequency divider ratio, see the table for crystal reference frequency divider ratios.)

Bit 8 (OS) is used to set the charge-pump driver amplifier output setting. When bit 8 is set to [0], the output is ON (the normal setting used); when it is set to [1], the output is OFF (charge pump is sink mode).

BYTE 5

Byte 5 is used to set the test mode and control the output ports (BS_V, BS_VH, BS_FM).
When a bandswitch data is set to [0], the output port is OFF; when it is set to [1], it is ON.
Bandswitch setting is also used to switch between the VHF and UHF bands and it is control standby mode.

- When the bandswitch data for either B1 or B2 is [1], VHF mode is effective.
- When the bandswitch data for both B1 and B2 is [0], UHF mode is effective.
- When the bandswitch data for both B1 and B2 is [1], Standby mode is effective.

Set the following maximum values for currents to the bandswitch driver. Ensure also that the total band current is within 15 mA when two bands are operating at the same time.

- BS_V (pin 7) output current: 5 mA (maximum)
- BS_VH (pin 8) output current: 10 mA (maximum)
- BS_FM (pin 9) output current: 5 mA (maximum)

B) READ MODE (Status Request)

When Read Mode is set, power-on reset operation status and phase comparator lock detector output status are output to the master device.

Bit 1 (POR) indicates the power-on reset operation status. When the power supply of Vcc stops, this bit is set to [1]. The conditions for reset to [0] are that voltage supplied to Vcc is 3V or higher, that transmission is requested in READ MODE, and that the status is output. (When Vcc is turned on, bit 1 is also set to [1].)

Bit 2 (FL) indicates the phase comparator lock status. When this is locked, [1] is output; when it is unlocked, [0] is output.

DATA FORMAT

A) WRITE MODE

		MSB							LSB	
1	Address Byte	1	1	0	0	0	MA1	MA0	R/W = 0	ACK
2	Divider Byte 1	0	N14	N13	N12	N11	N10	N9	N8	ACK
3	Divider Byte 2	N7	N6	N5	N4	N3	N2	N1	N0	ACK (L)
4	Control Byte	1	CP	T2	T1	T0	Rsa	Rsb	OS	ACK (L)
5	Band SW Byte	X	X	X	X	X	B3	B2	B1	ACK (L)

X :DON'T CARE
ACK :Acknowledged
(L) :Latch and transfer timing

B) READ MODE

		MSB							LSB	
1	Address Byte	1	1	0	0	0	MA1	MA0	R/W=1	ACK
2	Status Byte	POR	FL	1	1	1	1	1	1	-

ACK :Acknowledged

DATA SPECIFICATIONS

●MA1, MA0 : programmable hardware address bits

MA1	MA0	ADDRESS PIN APPLIED VOLTAGE
0	0	0 to 0.1Vcc
0	1	OPEN or 0.2Vcc to 0.3Vcc
1	0	0.4Vcc to 0.6Vcc
1	1	0.9Vcc to Vcc

●N14 – N0 : programmable counter data

● CP : charge pump output current setting
[0] : ± 55 μA (typ.)
[1] : ± 250 μA (typ.)

●T2, T1, T0 : test mode setting bits

CHARACTERISTIC		T2	T1	T0	NOTE
Normal operation		0	0	X	-
Charge-pump	OFF	0	1	0	Charge pump is OFF (check output: NF)
	SINK	1	1	0	Only charge pump sink current is ON (check output: NF)
	SOURCE	0	1	1	Only charge pump source current is ON (check output: NF)
Reference signal output		1	0	0	Reference signal output (check output: BS_FM)
1/2 counter divider output		1	0	1	1/2 counter output (check output: BS_V)

X :DON'T CARE

note7: Testing of the counter divider output requires the input of programmable counter data.

●Rsa, Rsb: Reference frequency divider ratio select bit.

Rsa	Rsb	DIVIDER RATIO	COMPARE FREQUENCY	STEP FREQUENCY
1	1	1/256	15.265kHz	62.5kHz
0	1	1/512	7.8125kHz	31.25kHz
X	1	1/320	12.5kHz	50kHz

●OS: tuning amplifier control bit
[0] : tuning amplifier ON (normal operation)
[1] : tuning amplifier OFF (charge pump is sink mode)

●B3, B2, B1: Band output port control and band change control bit
The Bandswitch data controls band port, mixer and oscillator, standby mode.
When the standby mode set, it is operating only bus-inter-face and crystal oscillator.

B2, B1 data

Bandswitch Data		Band Output Port		Operation Mixer, Oscillator
B2	B1	BS_V (pin7)	BS_VH (pin8)	–
0	0	OFF	OFF	UHF
0	1	ON	OFF	VHF
1	0	ON	ON	VHF
1	1	OFF	OFF	OFF (Standby Mode)

B3 data

Bandswitch Data	Band Output Port	Operation Mixer, Oscillator
B3	BS_FM (pin9)	–
0	OFF	Not relation
1	ON	Not relation

●POR: power-on reset flag
[0] : normal operation
[1] : reset operation

●FL: lock detect flag
[0] : unlocked
[1] : locked

●X : don't care

-EXAMPLE OF BUS DATA TRANSMITTER-

S: Start
ADR: Address Byte
DIV1: Divider Byte 1 (frequency data)
DIV2: Divider Byte 2 (frequency data)
CONT: Control Byte
BAND: Bandswitch Byte
A: Acknowledge
P: Stop

[1] Transmitter - 1

S	ADR	A	DIV1	A	DIV2	A	CONT	A	BAND	A	P

[2] Transmitter - 2

S	ADR	A	CONT	A	BAND	A	DIV1	A	DIV2	A	P

[3] Transmitter – 3 (This can be applied if control data and bandswitch data have already been programmed.)

S	ADR	A	DIV1	A	DIV2	A	P

[4] Transmitter – 4 (This can be applied if frequency data have already been programmed.)

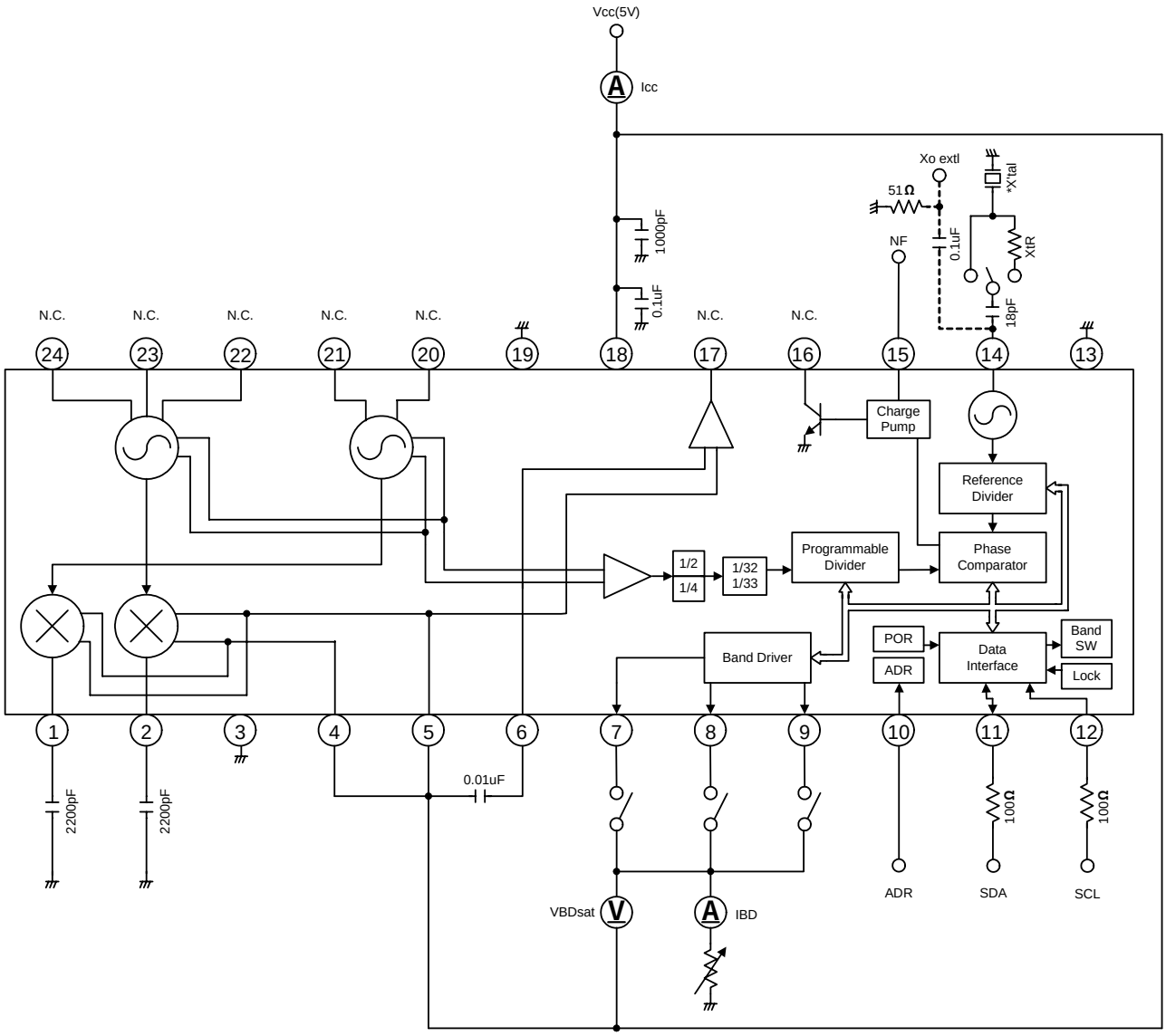
S	ADR	A	CONT	A	BAND	A	P

[5] Transmitter – 5 (This can be applied if frequency counter data and bandswitch data have already been programmed.)

S	ADR	A	CONT	A	P

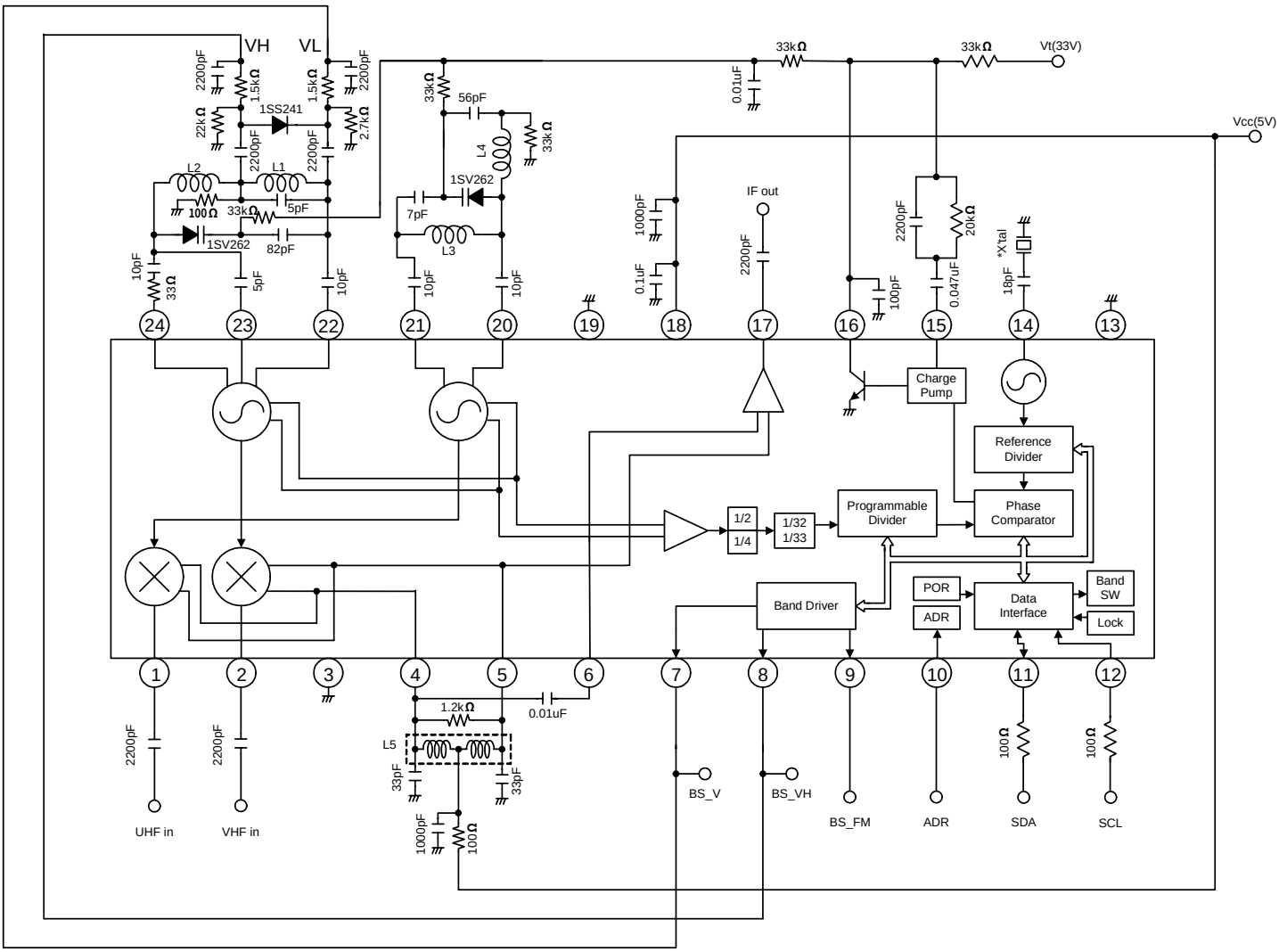
Until the I²C-bus STOP condition is detected, it is possible to input the additional data without transmitting the address data again. (For example: Frequency sweep is possible with additional frequency data.)
If data transmission is aborted, data programmed before the abort are valid.

TEST CIRCUIT 1



note8: Components in the test circuits are only used to obtain and confirm the device characteristics. These components and circuits do not warrant to prevent the application equipment from malfunction or failure.

TEST CIRCUIT 2



note8: Components in the test circuits are only used to obtain and confirm the device characteristics. These components and circuits do not warrant to prevent the application equipment from malfunction or failure.

L1 : 0.4mmd, 2.5mmφ, 6.5t
L2 : 0.4mmd, 2.5mmφ, 2.5t
L3 : 0.4mmd, 2.5mmφ, 2.5t
L4 : 0.4mmd, 1.5mmφ, 1.5t
L5 : Toko (886BNF-0357)

X'tal : 4MHz (NDK; AT-51)

*IF output pin is 75Ω load.

Measurement bus data setting
- Charge pump: High [250 μA (typ.)]
- Frequency step: 62.5 kHz

TEST CIRCUIT 3

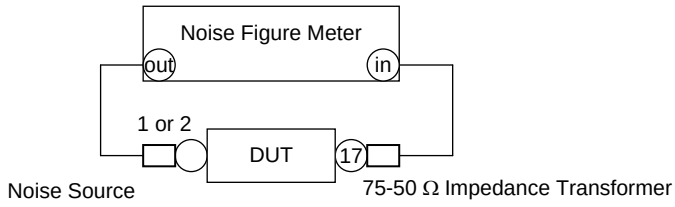


Figure 2: Noise Figure measurement

TEST CIRCUIT 4

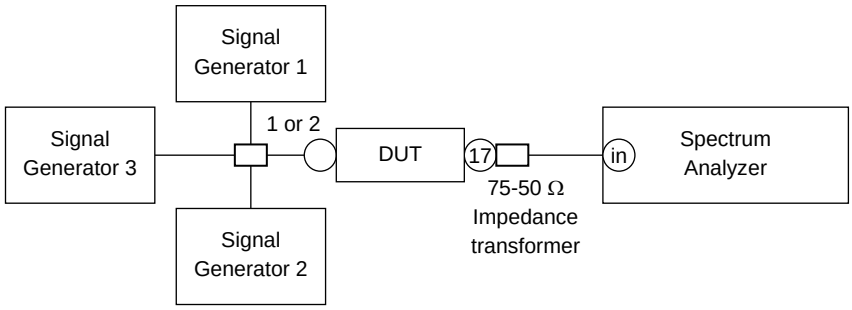
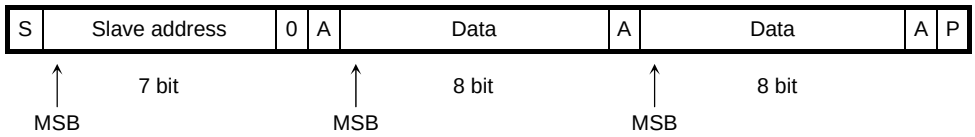


Figure 3: 1%Cross Modulation _ C/S beat _ Ch beat measurement

I^2C BUS CONTROL SUMMARY

Data transmission format

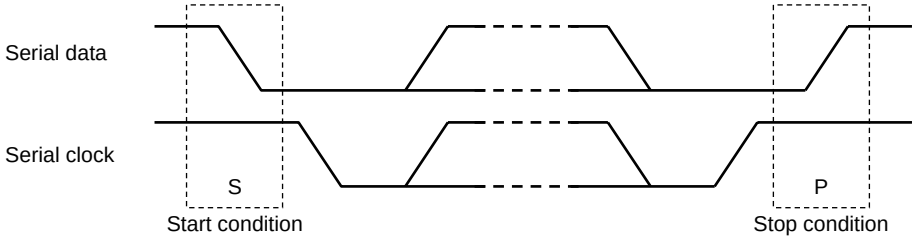


S: Start condition

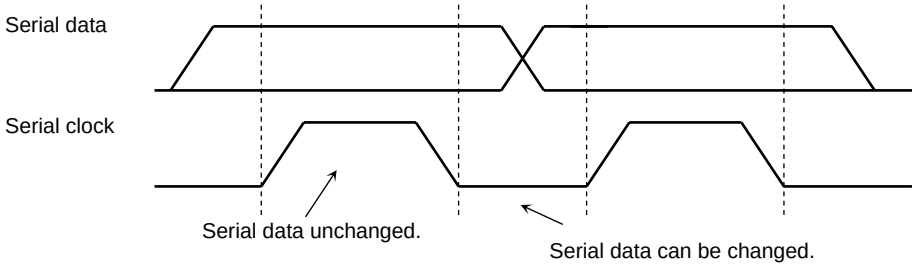
P: Stop condition

A: Acknowledge

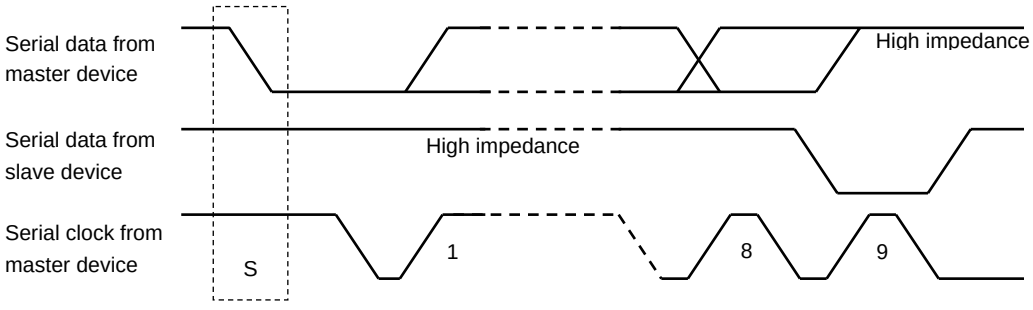
(1) Start / stop conditions



(2) Bit transfer



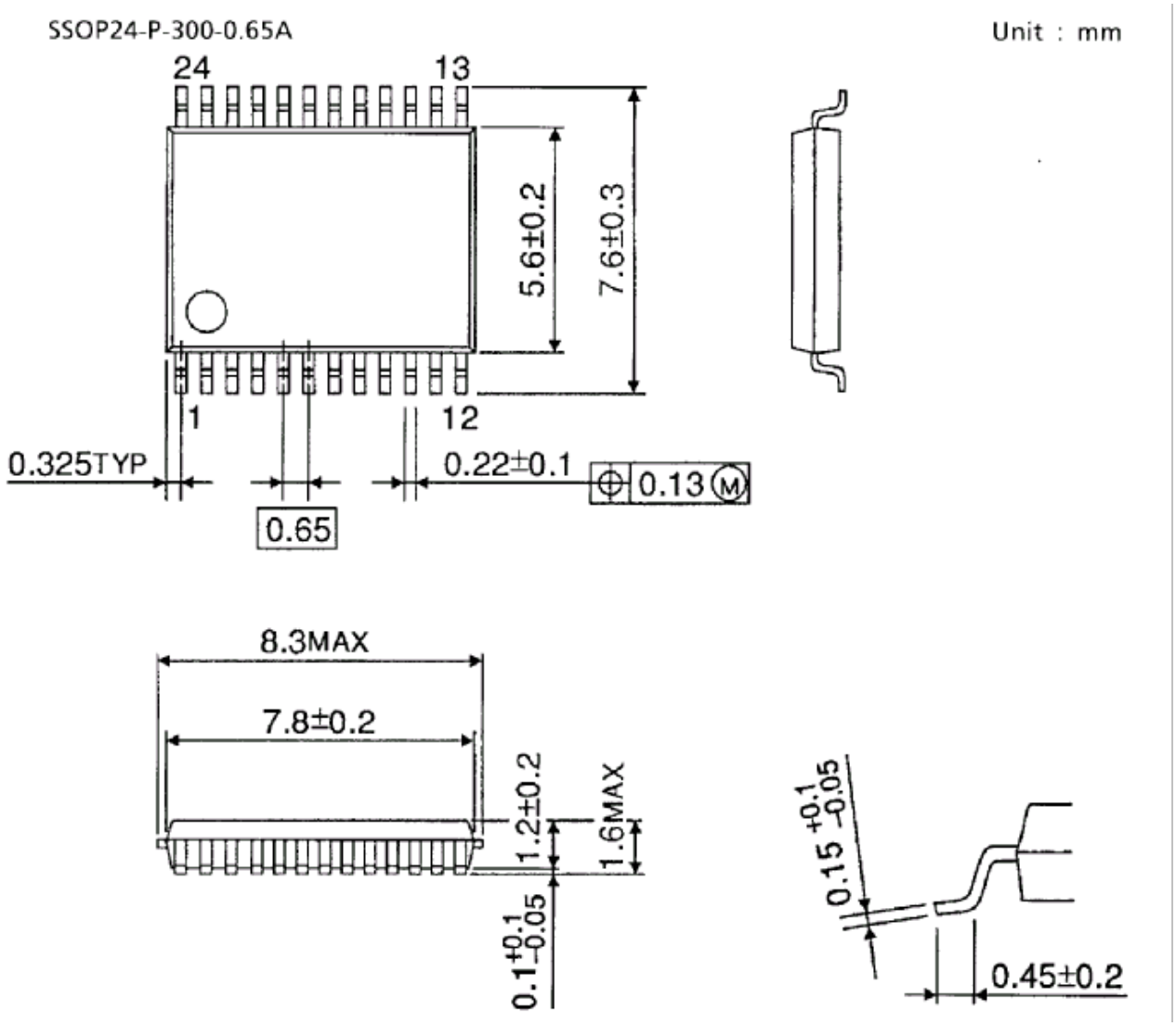
(3) Acknowledge



(4) Slave address

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	0	0	0	*	*	0

OUTLINE DRAWING



Weight: 0.09 g (typ.)

HANDLING PRECAUTIONS

1. Using a human charge model (C=100pF, R=1.5kΩ, test repeated three times), the product's electrostatic resistance was determined to be low in the following cases.
   (1) When a positive voltage is applied across pin1(UHF RF input) and Vcc and any GND.
   (2) When a positive voltage is applied across pin2(VHF RF input) and any GND.
   (3) When a positive voltage is applied across pin16(Vt output) and Vcc and any GND.
   Accordingly, please handle the product with care.

2. The device should not be inserted into or removed from the test apparatus while the voltage is being applied; otherwise breakdown or deterioration in performance of the device may result.
   Also, avoid any abrupt increasing or decreasing of the voltage.
   Overshoot or chattering of the power supply may cause the IC to be degraded.
   To avoid this problem, equip the power supply line with filters.

3. The peripheral circuits described in this datasheet are given only as system examples for evaluating the performance of the device. Toshiba neither recommend the configuration or related values of the peripheral circuits nor intend to manufacture such application systems in large quantities.
   Please note that the high-frequency characteristics of the device may vary depending on the external components, mounting method and other factors relating to the application design. Therefore it is the responsibility of users incorporating the device into their designs to evaluate the characteristics of application circuits.
   Toshiba only guarantee the quality and characteristics of the device as described in this datasheet and do not assume any responsibility for the customer's application design.

4. In order better to understand the quality and reliability of Toshiba semiconductor products and to incorporate them into designs in an appropriate manner, please refer to the latest Semiconductor Reliability Handbook (Integrated Circuits) published by Toshiba Semiconductor Company.

   The handbook can also be viewed online at " http://www.semicon.toshiba.co.jp/ "

Solderability

Regarding solderability, the following conditions have been confirmed.

(1) Use of Sn-63Pb solder bath
- Solder bath temperature = 230°C
- Dipping time = 5 seconds
- The number Number of times = once
- Use of R-type flux

(2) Use of Sn-3.0Ag-0.5Cu solder bath
- Solder bath temperature = 245°C
- Dipping time = 5 seconds
- Number of times = once
- Use of R-type flux

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030619EBA

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