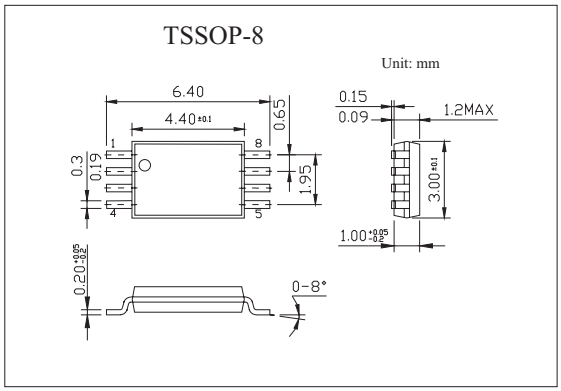
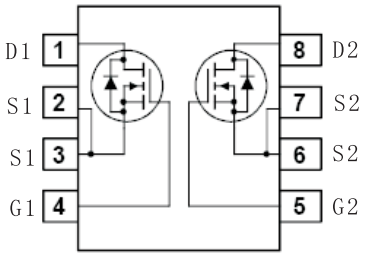
Dual N-Channel 2.5V Specified PowerTrench MOSFET

KDW2503N



Features

- 5.5 A, 20 V. $R_{DS(ON)}$ = 0.021Ω @ V_{GS} = 4.5 V
  $R_{DS(ON)}$ = 0.035Ω @ V_{GS} =2.5V
- Fast switching speed
- High performance trench technology for extremely low $R_{DS(ON)}$
- Extended VGSS range (±12V) for battery applications



Absolute Maximum Ratings Ta = 25℃

Parameter	Symbol	Rating	Unit
Drain to Source Voltage	V_{DSS}	20	V
Gate to Source Voltage	V_{GS}	±12	V
Drain Current Continuous (Note 1a)	I_D	5.5	A
Drain Current Pulsed		30	A
Power Dissipation for Single Operation (Note 1a)	P_D	1	W
Power Dissipation for Single Operation (Note 1b)		0.6	
Operating and Storage Temperature	T_J, T_{STG}	-55 to 175	℃
Thermal Resistance Junction to Ambient (Note 1a)	$R_{\theta JA}$	125	℃/W
Thermal Resistance Junction to Ambient (Note 1b)	$R_{\theta JA}$	208	℃/W

KDW2503N

■ Electrical Characteristics Ta = 25℃

Parameter	Symbol	Testconditons	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	B_{VDSS}	V_{GS} = 0 V, I_D = 250 μA	20			V
Breakdown Voltage Temperature Coefficient	$\frac{\Delta BV_{DSS}}{\Delta T_J}$	I_D = 250 μA, Referenced to 25℃		14		mV/℃
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 16 V, V_{GS} = 0 V			1	μA
Gate-Body Leakage, Forward	I_{GSSF}	V_{GS} = 12 V, V_{DS} = 0 V			100	nA
Gate-Body Leakage, Reverse	I_{GSSR}	V_{GS} = -12 V, V_{DS} = 0 V			-100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	0.6	0.8	1.5	V
Gate Threshold Voltage Temperature Coefficient	$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	I_D = 250 μA, Referenced to 25℃		-3.2		mV/℃
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} =4.5 V, I_D =5.5 A		17	21	mΩ
		V_{GS} = 2.5 V, I_D = 4.2 A		24	35	
		V_{GS} = 4.5 V, I_D =5.5 A,TJ = 125℃		23	34	
On-State Drain Current	$I_{D(on)}$	V_{GS} = 4.5 V, V_{DS} = 5V	30			A
Forward Transconductance	g_{FS}	V_{DS} = 5 V, I_D = 5.5A		26		S
Input Capacitance	C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V,f = 1.0 MHz		1082		pF
Output Capacitance	C_{oss}			277		pF
Reverse Transfer Capacitance	C_{rss}			130		pF
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 10 V, I_D = 1 A,V_{GS} = 4.5 V, R_{GEN} = 6 Ω		8	20	ns
Turn-On Rise Time	tr			8	27	ns
Turn-Off Delay Time	$t_{d(off)}$			24	38	ns
Turn-Off Fall Time	tf			8	16	ns
Total Gate Charge V_{gs}=5V	Q_g	V_{DS} = 10 V, I_D = 5.5 A,V_{GS}=4.5V(Note 2)		12	17	nC
Gate-Source Charge	Q_{gs}			2		nC
Gate-Drain Charge	Q_{gd}			3		nC
Maximum Continuous Drain-Source Diode Forward Current	I_S				0.83	A
Drain-Source Diode Forward Voltage	V_{SD}	V_{GS} = 0 V, I_S = 0.83 A (Not 2)		0.7	1.2	V

Notes:

1 $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

a) $R_{\theta JA}$ is 125℃/W (steady state) when mounted on a 1 $inch^2$ copper pad on FR-4.

b) $R_{\theta JA}$ is 208 ℃/W (steady state) when mounted on a minimum copper pad on FR-4.

2. Pulse Test: Pulse Width ＜ 300 μs, Duty Cycle ＜ 2.0%