Ordering number : EN5792

Monolithic Digital IC

# LB1991V

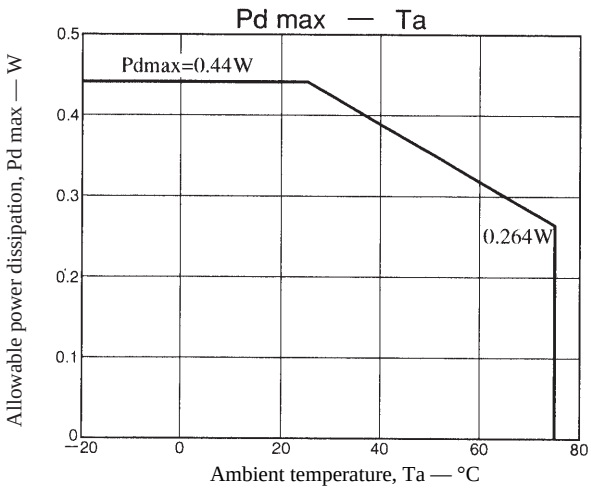
## Three-Phase Brushless Motor Driver for Portable VCR Capstan Motors

## Overview

The LB1991V is a 3-phase brushless motor driver IC that is optimal for driving the capstan motor in portable VCR products.

## Functions

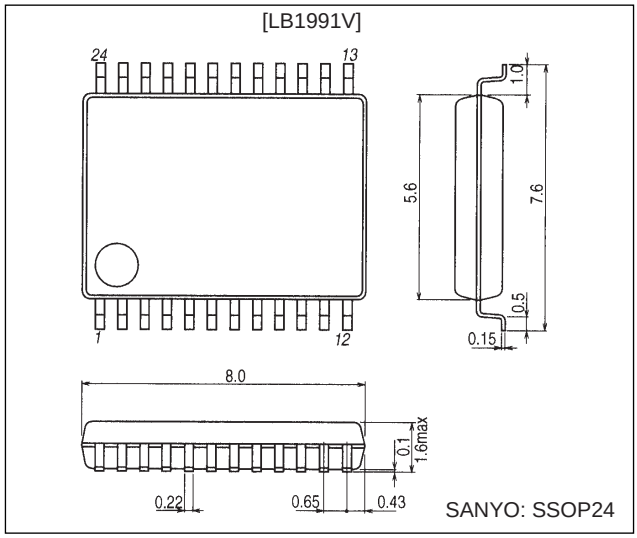
- 3-phase full-wave voltage drive technique (120° voltage-linear technique)
- Torque ripple correction circuit (overlap correction)
- Speed control technique based on motor voltage and current control.
- Built-in FG comparators
- Built-in thermal shutdown circuit




## Package Dimensions

unit: mm

**3175A-SSOP24**




## Specifications

### Absolute Maximum Ratings at Ta = 25°C

| Parameter | Symbol | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Maximum supply voltage | $V_{CC}1$ max | | 10 | V |
| | $V_{CC}2$ max | | 11 | V |
| | $V_S$ max | | 11 | V |
| Applied output voltage | $V_O$ max | | $V_S$ + 2 | V |
| Maximum output current | $I_O$ max | | 1.0 | A |
| Allowable power dissipation | Pd max | Independent IC | 440 | mW |
| Operating temperature | Topr | | –20 to +75 | °C |
| Storage temperature | Tstg | | –55 to +150 | °C |

### Allowable Operating Ranges at Ta = 25°C

| Parameter | Symbol | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Supply voltage | $V_{CC}1$ | $V_{CC}1 \le V_{CC}2$ | 2.7 to 6.0 | V |
| | $V_{CC}2$ | | 3.5 to 9.0 | V |
| | $V_S$ | | Up to $V_{CC}2$ | V |
| Hall input amplitude | $V_{HALL}$ | Between Hall effect element inputs | ±20 to ±80 | mVp-p |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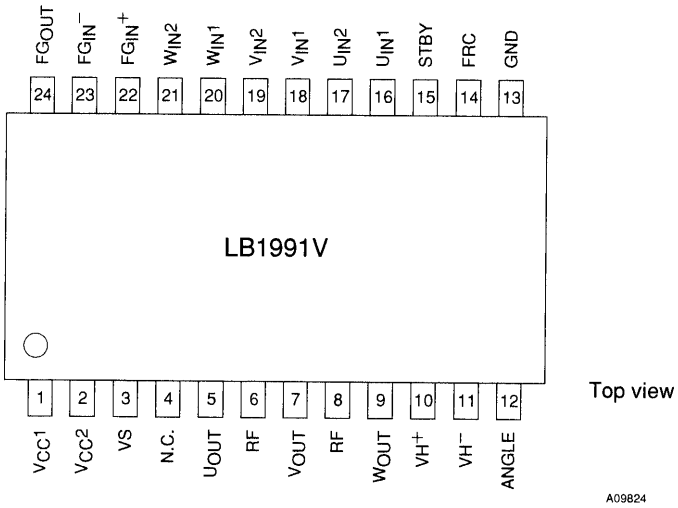
## Electrical Characteristics at Ta = 25°C, $V_{CC}1$ = 3 V, $V_{CC}2$ = 4.75 V, $V_S$ = 1.5 V

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|---|---|---|---|---|---|---|
| | | | min | typ | max | |
| [Supply Current] | | | | | | |
| $V_{CC}1$ current drain | $I_{CC}1$ | $I_{OUT}$ = 100 mA | | 3 | 5 | mA |
| $V_{CC}2$ current drain | $I_{CC}2$ | $I_{OUT}$ = 100 mA | | 7.0 | 10.0 | mA |
| $V_{CC}1$ quiescent current | $I_{CC}1Q$ | $V_{STBY}$ = 0 V | | 1.5 | 3.0 | mA |
| $V_{CC}2$ quiescent current | $I_{CC}2Q$ | $V_{STBY}$ = 0 V | | | 100 | µA |
| VS quiescent current | $I_SQ$ | $V_{STBY}$ = 0 V | | 75 | 100 | µA |
| [VX1] | | | | | | |
| High side residual voltage | $V_{XH}1$ | $I_{OUT}$ = 0.2 A | 0.15 | 0.22 | 0.29 | V |
| Low side residual voltage | $V_{XL}1$ | $I_{OUT}$ = 0.2 A | 0.15 | 0.20 | 0.25 | V |
| [VX2] | | | | | | |
| High side residual voltage | $V_{XH}2$ | $I_{OUT}$ = 0.5 A | | 0.25 | 0.40 | V |
| Low side residual voltage | $V_{XL}2$ | $I_{OUT}$ = 0.5 A | | 0.25 | 0.40 | V |
| Output saturation voltage | $V_O$(sat) | $I_{OUT}$ = 0.8 A, Sink + Source | | | 1.4 | V |
| Overlap | O.L | $R_L$ = 39 Ω × 3, Rangle = 20 kΩ *2 | 73 | 80 | 87 | % |
| High/low overlap difference | ΔO.L | (Average high side overlap) – (Average low side overlap) *2 | –8 | | +8 | % |
| [Hall Amplifiers] | | | | | | |
| Input offset voltage | $V_{HOFF}$ | *1 | –5 | | +5 | mV |
| Common-mode input voltage range | $V_{HCM}$ | Rangle = 20 kΩ | 0.95 | | 2.1 | V |
| I/O voltage gain | $V_{GVH}$ | Rangle = 20 kΩ | 25.5 | 28.5 | 31.5 | dB |
| [Standby Pin] | | | | | | |
| High-level voltage | $V_{STH}$ | | 2.5 | | | V |
| Low-level voltage | $V_{STL}$ | | | | 0.4 | V |
| Input current | $I_{STIN}$ | $V_{STBY}$ = 3 V | | 25 | 40 | µA |
| Leakage current | $I_{STLK}$ | $V_{STBY}$ = 0 V | | | –30 | µA |
| [FRC Pin] | | | | | | |
| High-level voltage | $V_{FRCH}$ | | 2.5 | | | V |
| Low-level voltage | $V_{FRCL}$ | | | | 0.4 | V |
| Input current | $I_{FRCIN}$ | $V_{FRC}$ = 3 V | | 20 | 30 | µA |
| Leakage current | $I_{FRCLK}$ | $V_{FRC}$ = 0 V | | | –30 | µA |
| [VH] | | | | | | |
| Hall supply voltage | $V_{HALL}$ | $I_H$ = 5 mA, $V_H$(+) – $V_H$(–) | 0.85 | 0.95 | 1.05 | V |
| (–) pin voltage | $V_H$(–) | $I_H$ = 5 mA | 0.81 | 0.88 | 0.95 | V |
| [FG Comparator] | | | | | | |
| Input offset voltage | $V_{FGOFF}$ | | –3 | | +3 | mV |
| Input bias voltage | $I_{bFG}$ | $V_{FGIN}$+ = $V_{FGIN}$– = 1.5 V | | | 500 | nA |
| Input bias current offset | $\Delta I_{bFG}$ | $V_{FGIN}$+ = $V_{FGIN}$– = 1.5 V | –100 | | +100 | nA |
| Common-mode input voltage range | $V_{FGCM}$ | | 1.2 | | 2.5 | V |
| Output high-level voltage | $V_{FGOH}$ | At the internal pull-up resistors | 2.8 | | | V |
| Output low-level voltage | $V_{FGOL}$ | At the internal pull-up resistors | | | 0.2 | V |
| Voltage gain | $V_{GFG}$ | *1 | | 100 | | dB |
| Output current (sink) | $I_{FGOS}$ | For the output pin low level | | | 5 | mA |
| [TSD] | | | | | | |
| TSD operating temperature | T-TSD | Design target value *1 | | 180 | | °C |
| TSD temperature hysteresis | ΔTSD | Design target value *1 | | 20 | | °C |

Notes: 1. Items specified as design target values in the conditions column are not tested.
2. The standard for overlap is the value as measured.

## Pin Assignment

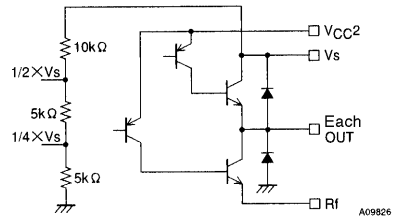
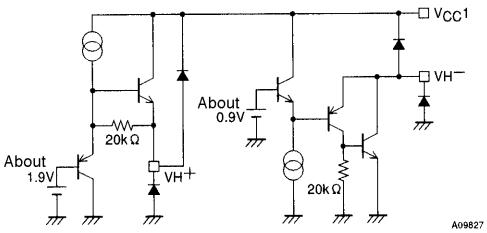
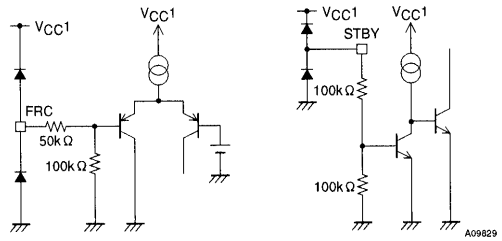
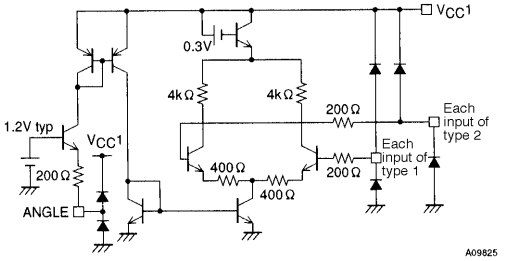
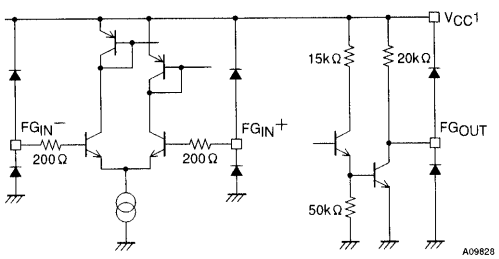



## Truth Table

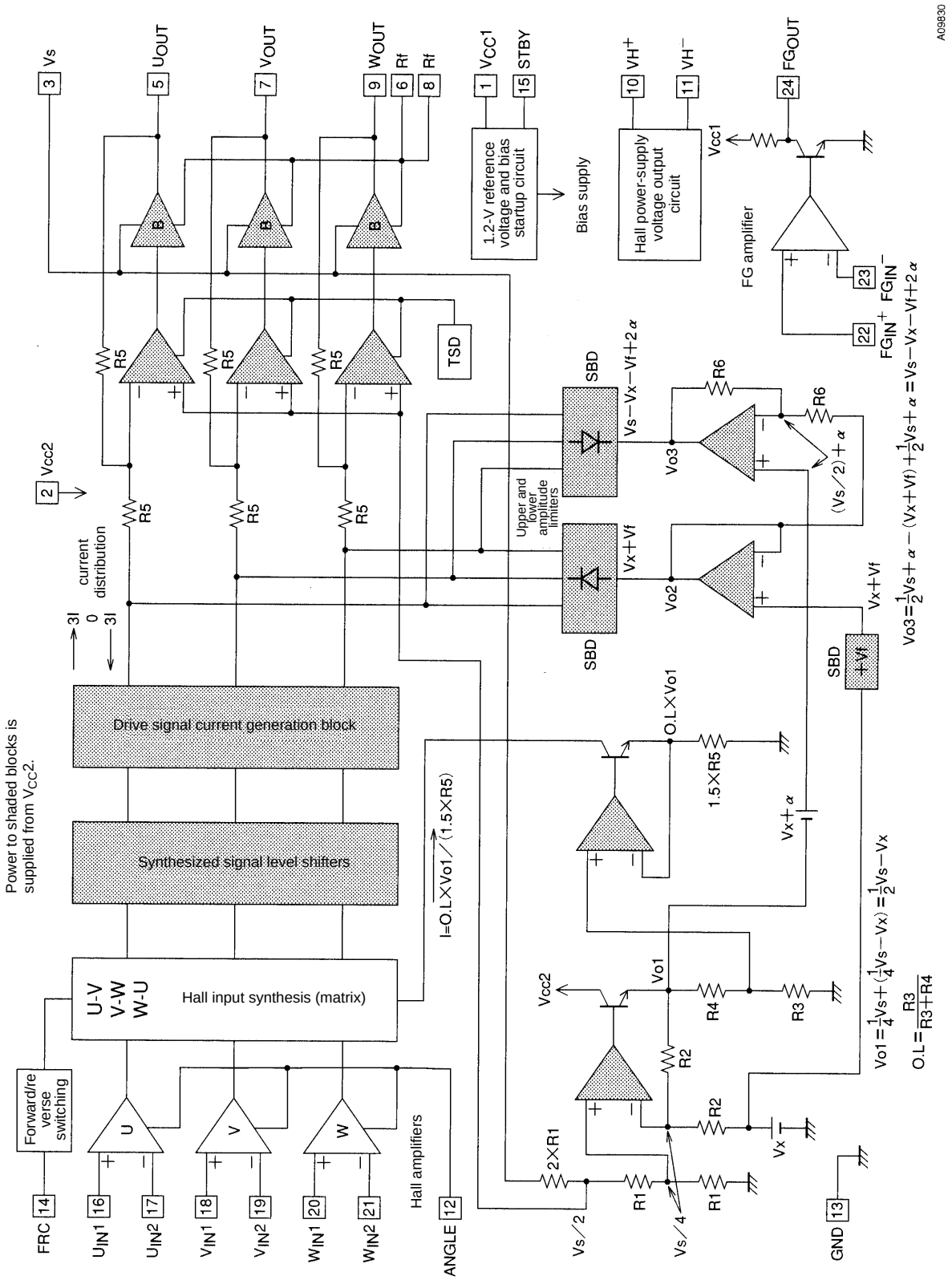
| | Source phase → Sink phase | Hall input | | | FRC |
|---|---|---|---|---|---|
| 1 | V → W | H | H | L | H |
| | W → V | | | | L |
| 2 | U → W | H | L | L | H |
| | W → U | | | | L |
| 3 | U → V | H | L | H | H |
| | V → U | | | | L |
| 4 | W → V | L | L | H | H |
| | V → W | | | | L |
| 5 | W → U | L | H | H | H |
| | U → W | | | | L |
| 6 | V → U | L | H | L | H |
| | U → V | | | | L |

Note: The “H” entries in the FRC column indicate a voltage of 2.50 V or higher, and the “L” entries indicate a voltage of 0.4 V or lower. (When $V_{CC}1$ is 3 V.) At the Hall inputs, for each phase a high-level input is the state where the (+) input is 0.02 V or higher than the (–) input. Similarly, a low-level input is the state where the (+) input is 0.02 V or lower than the (–) input.

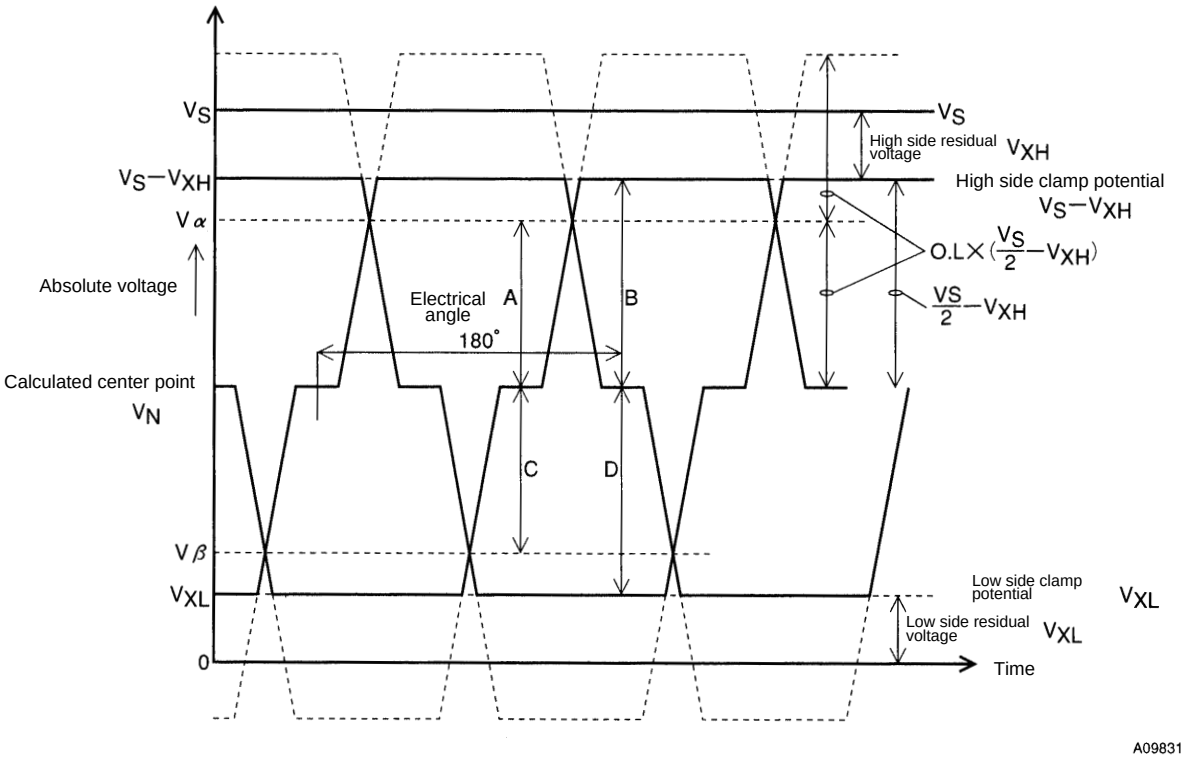
## Pin Functions

| Pin No. | Pin | Equivalent circuit | Pin function |
|---|---|---|---|
| 1 | $V_{CC}1$ | Supply voltage for all circuits other than the IC internal output block and the amplitude control block. | |
| 2 | $V_{CC}2$ | Supply voltage for the IC internal output control block and the amplitude control block. | |
| 3 | $V_S$ | Motor drive power supply. The voltage applied to this pin must not exceed $V_{CC}2$. | |
| 5 | $U_{OUT}$ | U phase output |  |
| 7 | $V_{OUT}$ | V phase output (These outputs include built-in spark killer diodes.) | |
| 9 | $W_{OUT}$ | W phase output | |
| 6, 8 | $R_f$ | Ground for the output power transistors | |
| 10 | $VH^+$ | Hall element bias voltage supply<br>A voltage that is typically 0.95 V is generated between the $VH^+$ and $VH^-$ pins. (When IH is 5 mA.) |  |
| 11 | $VH^-$ | | |
| 13 | GND | Ground for circuits other than the output transistor<br>The Rf pin potential is the lowest output transistor potential. | |
| 14 | FRC | Forward/reverse selection. Applications can select motor forward or reverse direction rotation using this pin. (This pin has hysteresis characteristics.) |  |
| 15 | STBY | Selects the bias supply for all circuits other than the FG comparators. The bias supply is cut when this pin is set to the low level. | |
| 16<br>17 | $U_{IN}1$<br>$U_{IN}2$ | U phase Hall element input<br>The logic high level is the state where the IN+ voltage is greater than the IN- voltage. |  |
| 18<br>19 | $V_{IN}1$<br>$V_{IN}2$ | V phase Hall element input<br>The logic high level is the state where the IN+ voltage is greater than the IN- voltage. | |
| 20<br>21 | $W_{IN}1$<br>$W_{IN}2$ | W phase Hall element input<br>The logic high level is the state where the IN+ voltage is greater than the IN- voltage. | |
| 12 | ANGLE | Hall input/output gain control. The gain is controlled by the resistor connected between this pin and ground. | |
| 22 | $FG_{IN}+$ | FG comparator noninverting inputs. There is no internally applied bias. |  |
| 23 | $FG_{IN}-$ | FG comparator inverting inputs. There is no internally applied bias. | |
| 24 | $FG_{OUT}$ | FG comparator outputs. There is an internal 20-kΩ resistor load. | |

## Block Diagram



## Overlap Generation and Calculation Method




[Overlap Generation]
Since the voltage generated in the amplitude control block is, taking the center point as the reference, 2 × <overlap> × (1/2 $V_S - V_X$) on one side, the intersection point of the waveform will be <overlap> × (1/2 $V_S - V_X$) from the center point.
To clamp that waveform at (1/2 $V_S - V_X$) referenced to the center point the overlap must be:
A/B × 100 = <overlap> × 100 (%).

[Overlap Calculation]
• High side overlap

Calculated center point: $V_N = \dfrac{(V_S - V_{XH} - V_{XL})}{2} + V_{XL} = \dfrac{(V_S - V_{XH} + V_{XL})}{2}$

Since $A = V\alpha - V_N$, $B = V_S - V_{XH} - V_N$, the high side overlap will be:

$$\text{<overlap>} = \frac{A}{B} = \frac{V\alpha - ((V_S - V_{XH} + V_{XL})/2)}{V_S - V_{XH} - ((V_S - V_{XH} + V_{XL})/2)} \times 100\ (\%)$$

Which can be calculated as:

$$= \frac{2V\alpha - (V_S - V_{XH}) - V_{XL}}{(V_S - V_{XH}) - V_{XL}} \times 100\ (\%).$$

• Low side overlap

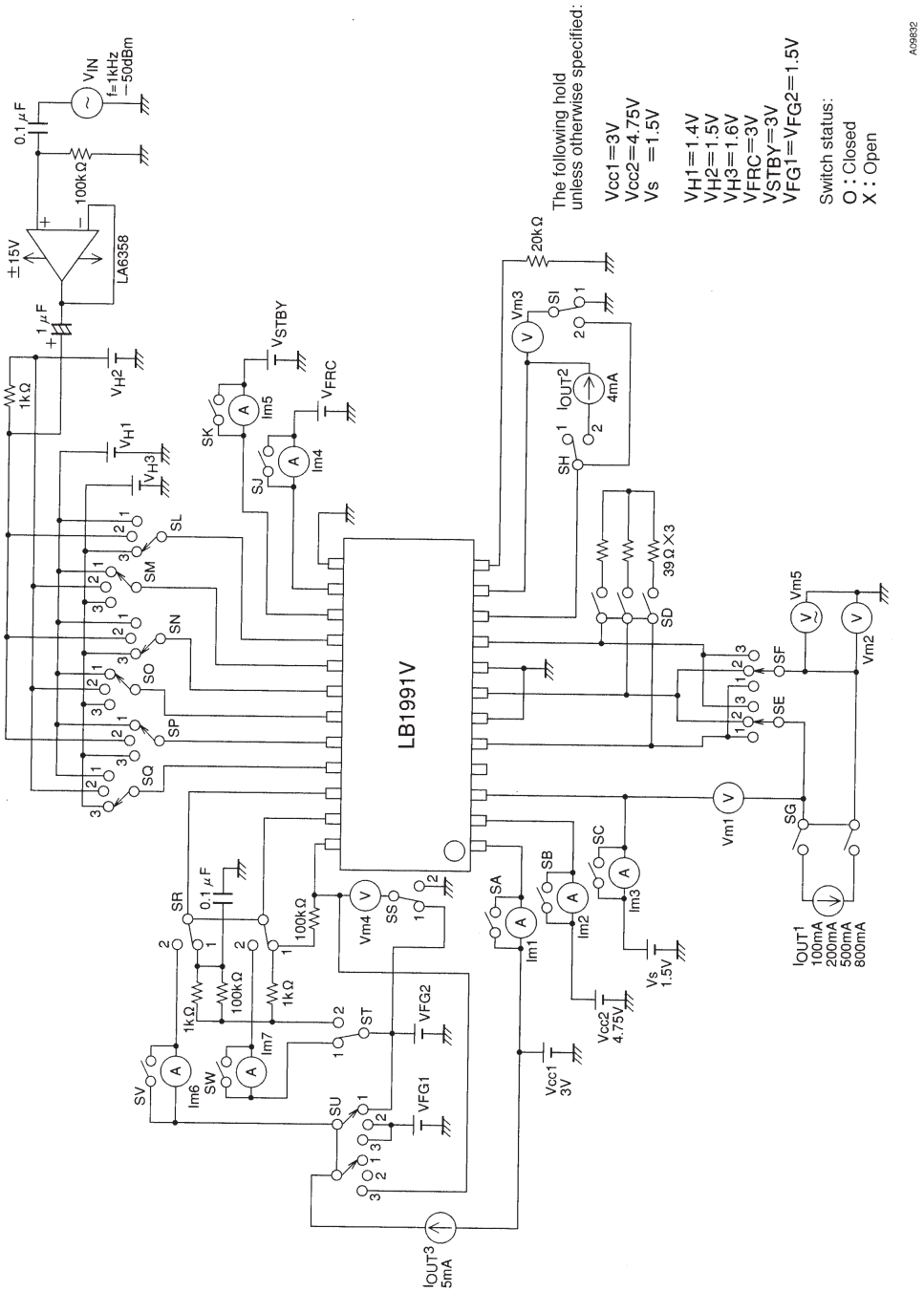
Since $C = V_N - V\beta$, and $D = V_N - V_{XL}$, the low side overlap will be:

$$\text{<overlap>} = \frac{C}{D} = \frac{((V_S - V_{XH} + V_{XL})/2)}{((V_S - V_{XH} + V_{XL})/2) - V_{XL}} \times 100$$

Which can be calculated as:

$$= \frac{(V_S - V_{XH}) - V_{XL} - 2V\beta}{(V_S - V_{XH}) - V_{XL}} \times 100\ (\%).$$

## Test Circuit

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