MSPM0L130x Mixed-Signal Microcontrollers

1 Features

- **Core**
  - Arm® 32-bit Cortex®-M0+ CPU, frequency up to 32 MHz
- **Operating characteristics**
  - Extended temperature: –40°C to 125°C
  - Wide supply voltage range: 1.62 V to 3.6 V
- **Memories**
  - Up to 64KB of flash
  - Up to 4KB of SRAM
- **High-performance analog peripherals**
  - One 12-bit 1.45-Msps analog-to-digital converter (ADC) with up to 10 total external channels
  - Configurable 1.4-V or 2.5-V internal ADC voltage reference (VREF)
  - Two zero-drift, zero-crossover chopper operational amplifiers (OPA)
    - 0.5-μV/°C drift with chopping
    - 10-pA input bias current [1]
    - Integrated programmable gain stage up to 32x
  - One general-purpose amplifier (GPAMP)
  - One high-speed comparator (COMP) with 8-bit reference DAC
    - 40-ns propagation delay in high-speed mode
    - Support low-power mode operation (1 μA)
  - Integrated temperature sensor
- **Optimized low-power modes**
  - RUN: 96 μA/MHz (CoreMark)
  - STOP: 200 μA at 4 MHz and 45 μA at 32 kHz
  - STANDBY: 1.1 μA with SRAM retention
  - SHUTDOWN: 83 nA with IO wakeup capability
- **Intelligent digital peripherals**
  - 3-channel DMA controller
  - Four 16-bit general-purpose timers, each with two capture/compare registers supporting low-power operation in STANDBY mode, supporting a total of 8 PWM channels
  - Windowed watchdog timer
- **Enhanced communication interfaces**
  - Two UART interfaces; one supports LIN, IrDA, DALI, Smart Card, Manchester and both support low-power operation in STANDBY mode
  - Two I^2C interfaces; one supports FM+ (1 Mbit/s) and both support SMBus, PMBus, and wakeup from STOP mode
  - One SPI supports up to 16 Mbit/s
- **Clock system**
  - Internal 4- to 32-MHz oscillator with up to ±1% accuracy (SYSOSC)
  - Internal 32-kHz low-frequency oscillator (LFOSC)
- **Data integrity**
  - Cyclic redundancy checker (CRC-16 or CRC-32)
- **Flexible I/O features**
  - Up to 28 GPIOs
  - Two 5-V-tolerant open-drain IOs with fail-safe protection
- **Development support**
  - 2-pin serial wire debug (SWD)
- **Package options**
  - 32-pin VQFN (RHB)
  - 28-pin VSSOP (DGS)
  - 24-pin VQFN (RGE)
  - 20-pin VSSOP (DGS)
  - 16-pin SOT (DYY), WQFN (RTR)[2]
- **Family members**)
  - MSPM0L13x3: 8KB of flash, 2KB of RAM
  - MSPM0L13x4: 16KB of flash, 2KB of RAM
  - MSPM0L13x5: 32KB of flash, 4KB of RAM
  - MSPM0L13x6: 64KB of flash, 4KB of RAM
- **Development kits and software** (also see *Tools and Software*)
  - LP-MSPM0L1306 LaunchPad™ development kit
  - MSP Software Development Kit (SDK)

2 Applications

- Battery charging and management
- Power supplies and power delivery
- Personal electronics
- Building security and fire safety
- Connected peripherals and printers
- Grid infrastructure
- Smart metering
- Communication modules
- Medical and healthcare
- Lighting

ADVANCE INFORMATION

[1] MSPM0L134x only
[2] The 16-pin WQFN package is product preview.

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. ADVANCE INFORMATION for preproduction products; subject to change without notice.

ADVANCE INFORMATION

3 Description

MSPM0L134x and MSPM0L130x microcontrollers (MCUs) are part of MSP's highly-integrated, ultra-low-power 32-bit MCU family based on the enhanced Arm® Cortex®-M0+ core platform operating at up to 32-MHz frequency. These cost-optimized MCUs offer high-performance analog peripheral integration, support extended temperature ranges from -40°C to 125°C, and operate with supply voltages ranging from 1.62 V to 3.6 V.

The MSPM0L134x and MSPM0L130x devices provide up to 64KB embedded flash program memory with up to 4KB SRAM. These MCUs incorporate a high-speed on-chip oscillator with an accuracy up to ±1%, eliminating the need for an external crystal. Additional features include a 3-channel DMA, 16- and 32-bit CRC accelerator, and a variety of high-performance analog peripherals such as one 12-bit 1.45-MSPS ADC with configurable internal voltage reference, one high-speed comparator with built-in reference DAC, two zero-drift zero-crossover operational amplifiers with programmable gain, one general-purpose amplifier, and an on-chip temperature sensor. These devices also offer intelligent digital peripherals such as four 16-bit general purpose timers, one windowed watchdog timer, and a variety of communication peripherals including two UARTs, one SPI, and two I^2Cs. These communication peripherals offer protocol support for LIN, IrDA, DALI, Manchester, Smart Card, SMBus, and PMBus.

The TI MSPM0 family of low-power MCUs consists of devices with varying degrees of analog and digital integration allowing for customers find the MCU that meets their project's needs. The architecture combined with extensive low-power modes are optimized to achieve extended battery life in portable measurement applications.

MSPM0L134x and MSPM0L130x MCUs are supported by an extensive hardware and software ecosystem with reference designs and code examples to get the design started quickly. Development kits include a LaunchPad available for purchase and design files for a Target-Socket Board. TI also provides a free MSP Software Development Kit (SDK), which is available as a component of Code Composer Studio™ IDE desktop and cloud version within the TI Resource Explorer. MSPM0 MCUs are also supported by extensive online collateral, training with MSP Academy, and online support through the TI E2E™ support forums.

For complete module descriptions, see the *MSPM0 L-Series 32-MHz Microcontrollers Technical Reference Manual*.

CAUTION

System-level ESD protection must be applied in compliance with the device-level ESD specification to prevent electrical overstress or disturbing of data or code memory. See MSP430™ System-Level ESD Considerations for more information; the principles in this application note are applicable to MSPM0 MCUs.

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4 Functional Block Diagram

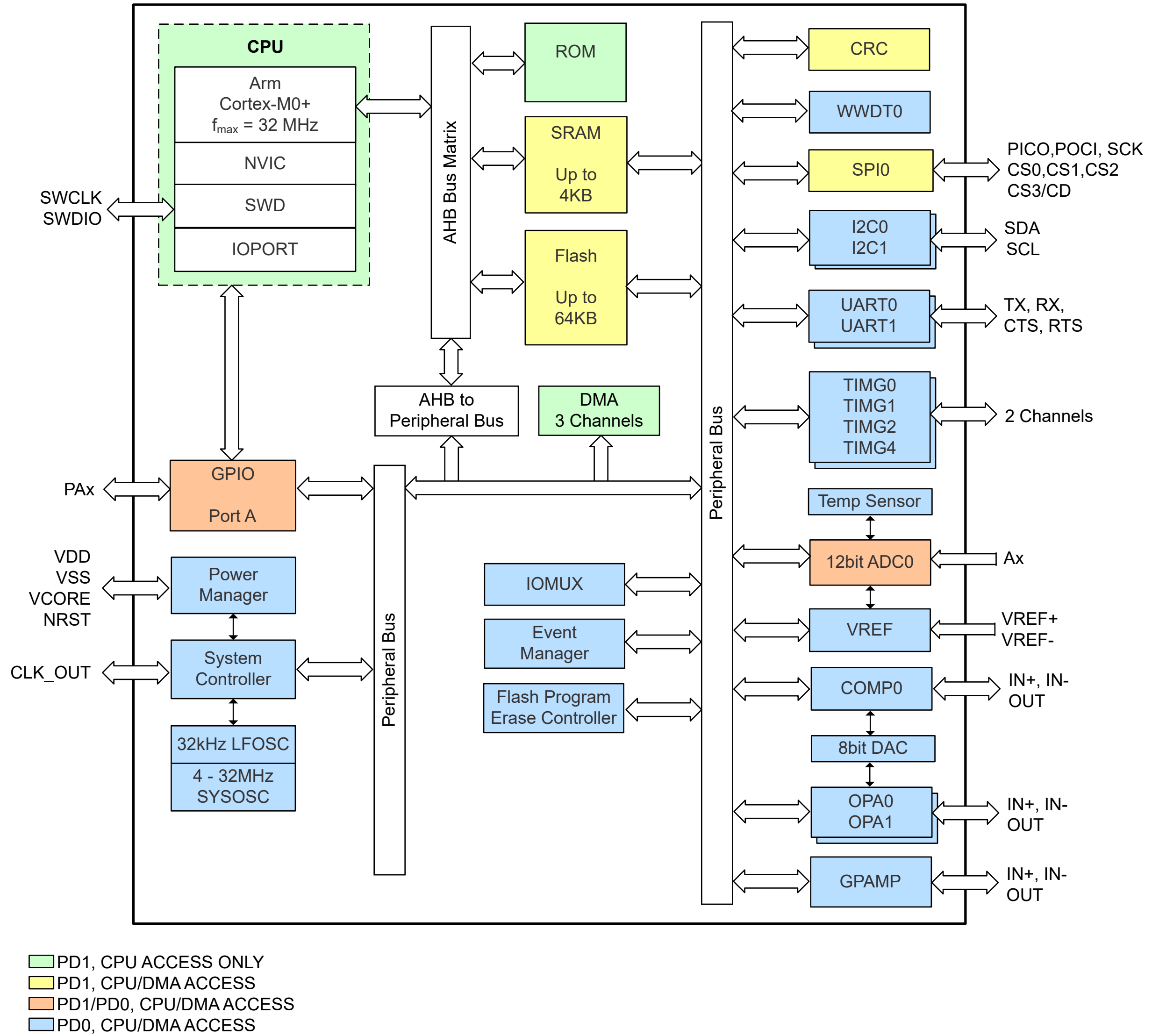

Figure 4-1. MSPM0L130x Functional Block Diagram

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ADVANCE INFORMATION

5 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

5.1 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all MSP MCU devices and support tools. . Each MSP MCU commercial family member has one of two prefixes: MSP or X. These prefixes represent evolutionary stages of product development from engineering prototypes (X) through fully qualified production devices (MSP).

X – Experimental device that is not necessarily representative of the final device's electrical specifications

MSP – Fully qualified production device

X devices are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes." MSP devices have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies. Predictions show that prototype devices (X) have a greater failure rate than the standard production devices. TI recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the temperature range, package type, and distribution format. Figure 5-1 provides a legend for reading the complete device name.

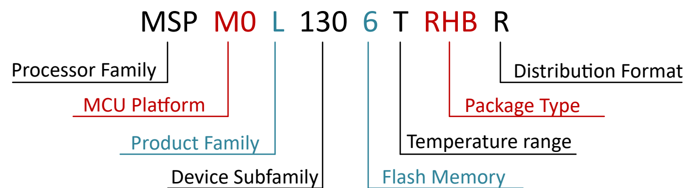

Figure 5-1. Device Nomenclature

Table 5-1. Device Nomenclature

Processor Family	MSP = Mixed-signal processor X= Experimental silicon
MCU Platform	M0 = Arm-based 32-bit M0+
Product Family	L = 32-MHz frequency
Device Subfamily	130 = ADC, 2x OPA, COMP 134 = ADC, 2x OPA (10-pA input bias current), COMP
Flash Memory	4 = 16KB 5 = 32KB 6 = 64KB
Temperature Range	T = –40°C to 105°C S = –40°C to 125°C
Package Type	See www.ti.com/packaging
Distribution Format	T = Small reel R = Large reel No marking = Tube or tray

For orderable part numbers of MSP devices in different package types, see the Package Option Addendum of this document, ti.com, or contact your TI sales representative.

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5.2 Tools and Software

Design Kits and Evaluation Modules

MSPM0 LaunchPad (LP) Boards: LP-MSPM0L1306	Empowers you to immediately start developing on the industry's best integrated analog and most cost-optimized general purpose MSPM0 MCU family. Exposes all device pins and functionality; includes some built-in circuitry, out-of-box software demos, and on-board XDS110 debug probe for programming/debugging/EnergyTrace. The LP ecosystem includes dozens of BoosterPack stackable plug-in modules to extend functionality.

Embedded Software

MSPM0 Software Development Kit (SDK)	Contains software drivers, middleware libraries, documentation, tools, and code examples that create a familiar and easy user experience for all MSPM0 devices.

Software Development Tools

TI Cloud Tools	Start your evaluation and development on a web browser without any installation. Cloud tools also have a downloadable, offline version.
TI Resource Explorer	Online portal to TI SDKs. Accessible in CCS IDE or in TI Cloud Tools.
SysConfig	Intuitive GUI to configure device and peripherals, resolve system conflicts, generate configuration code, and automate pin mux settings. Accessible in CCS IDE or in TI Cloud Tools. (offline version)
MSP Academy	Great starting point for all developers to learn about the MSPM0 MCU Platform with training modules that span a wide range of topics. Part of TIRex.
GUI Composer	GUIs that simplify evaluation of certain MSPM0 features, such as configuring and monitoring a fully integrated analog signal chain without any code needed.

IDE & compiler tool chains

Code Composer Studio™ (CCS)	Includes TI Arm-Clang compiler. Supports all TI Arm Cortex MCUs and boasts competitive code size performance advantages, fast compile time, code coverage support, safety certification support, and completely free to use.
IAR Embedded Workbench® IDE	
Keil® MDK IDE	
GNU Arm Embedded Tool Chain	

5.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

5.4 Trademarks

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5.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

5.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

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6 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

ADVANCE INFORMATION

PACKAGE OUTLINE

DGS0020A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. No JEDEC registration as of September 2020.
5. Features may differ or may not be present.

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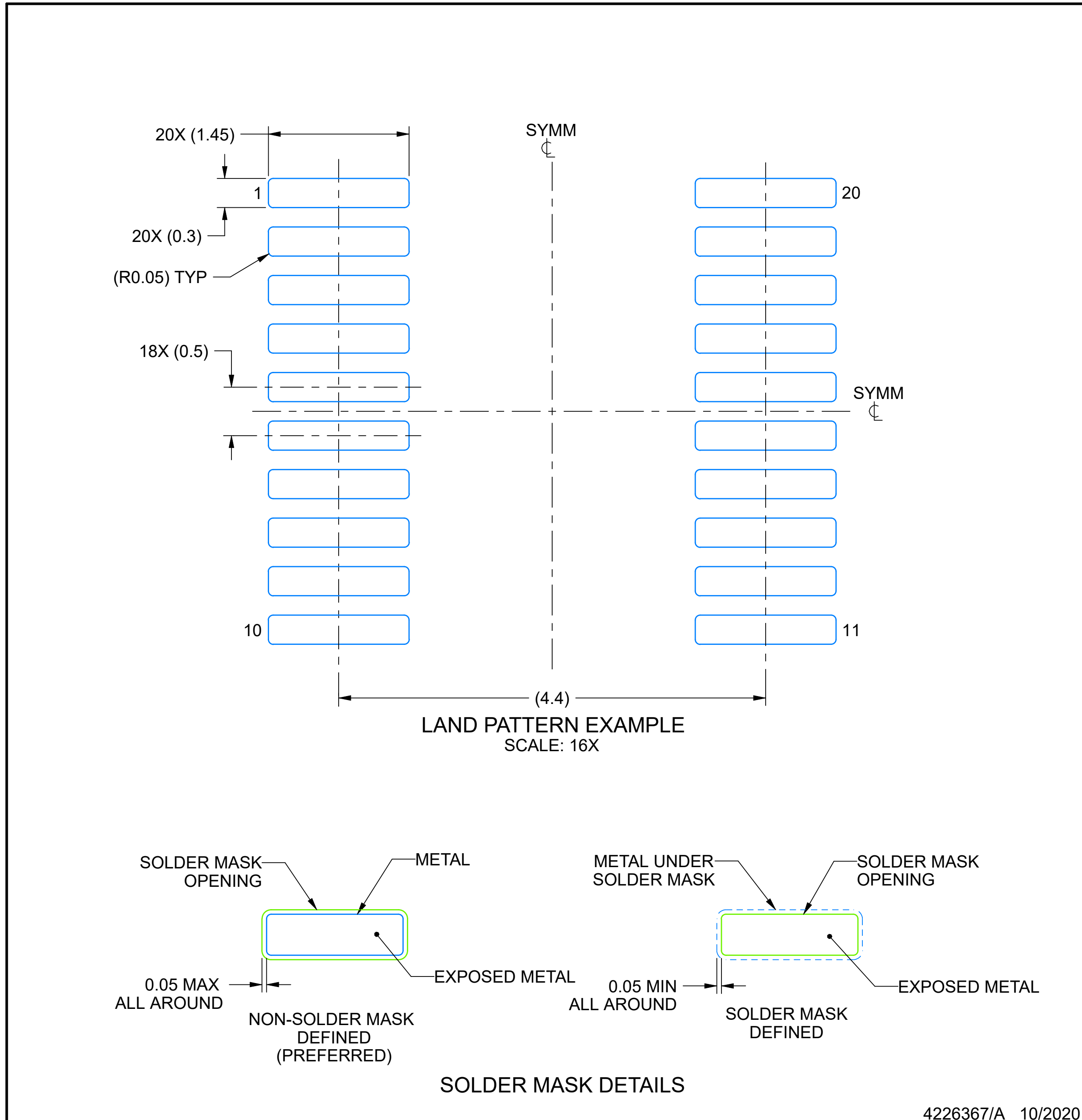
EXAMPLE BOARD LAYOUT

DGS0020A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

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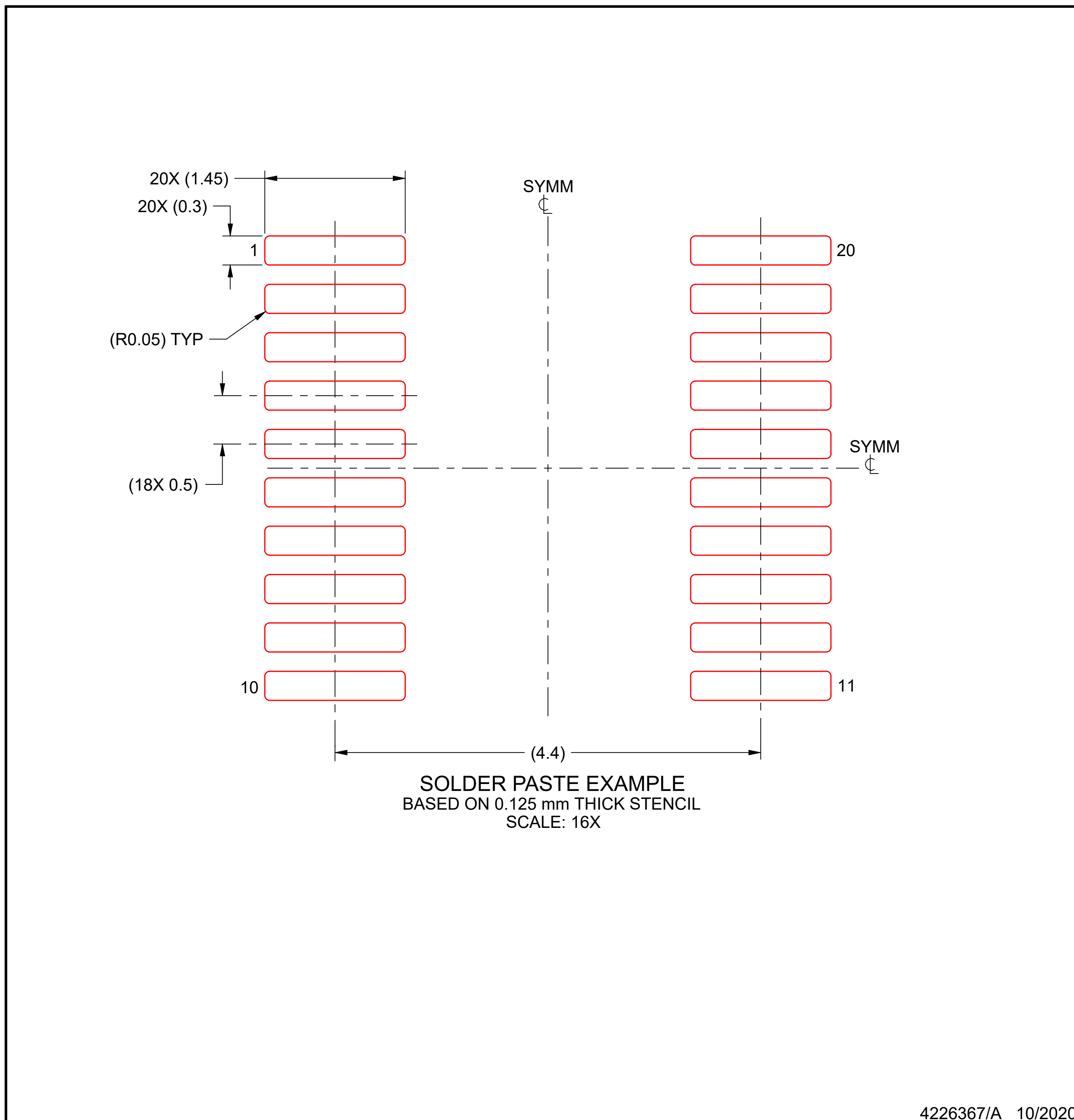
EXAMPLE STENCIL DESIGN

DGS0020A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

ADVANCE INFORMATION



NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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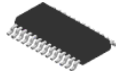
PACKAGE OUTLINE



DGS0028A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

PIN 1 INDEX AREA
A
5.1
4.7 TYP
26X 0.5
28
1
7.2
7.0
NOTE 3
2X 6.5
14
15
B
3.1
2.9
28X 0.275
0.165
⌖ 0.1Ⓜ C A B
C
⌓ 0.1 C
SEATING PLANE
4X (0° -15°)
SEE DETAIL A
4X (7° -15°)
(0.15) TYP
0.25
GAGE PLANE
1.1 MAX
0° -8°
0.7
0.4
0.15
0.05
DETAIL A
TYPICAL

4226365/A 10/2020

PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. No JEDEC registration as of September 2020.
5. Features may differ or may not be present.

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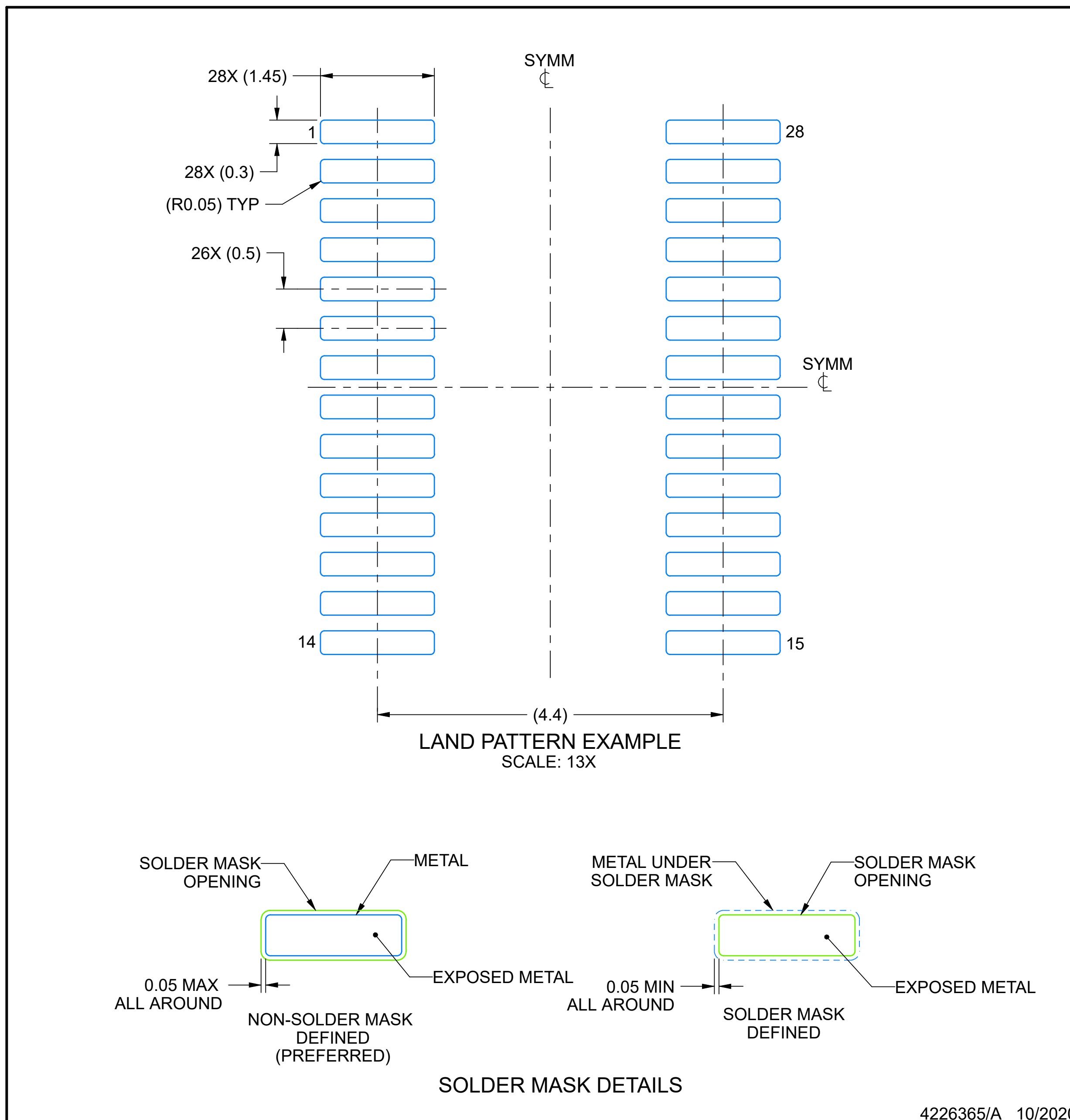
ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

DGS0028A VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

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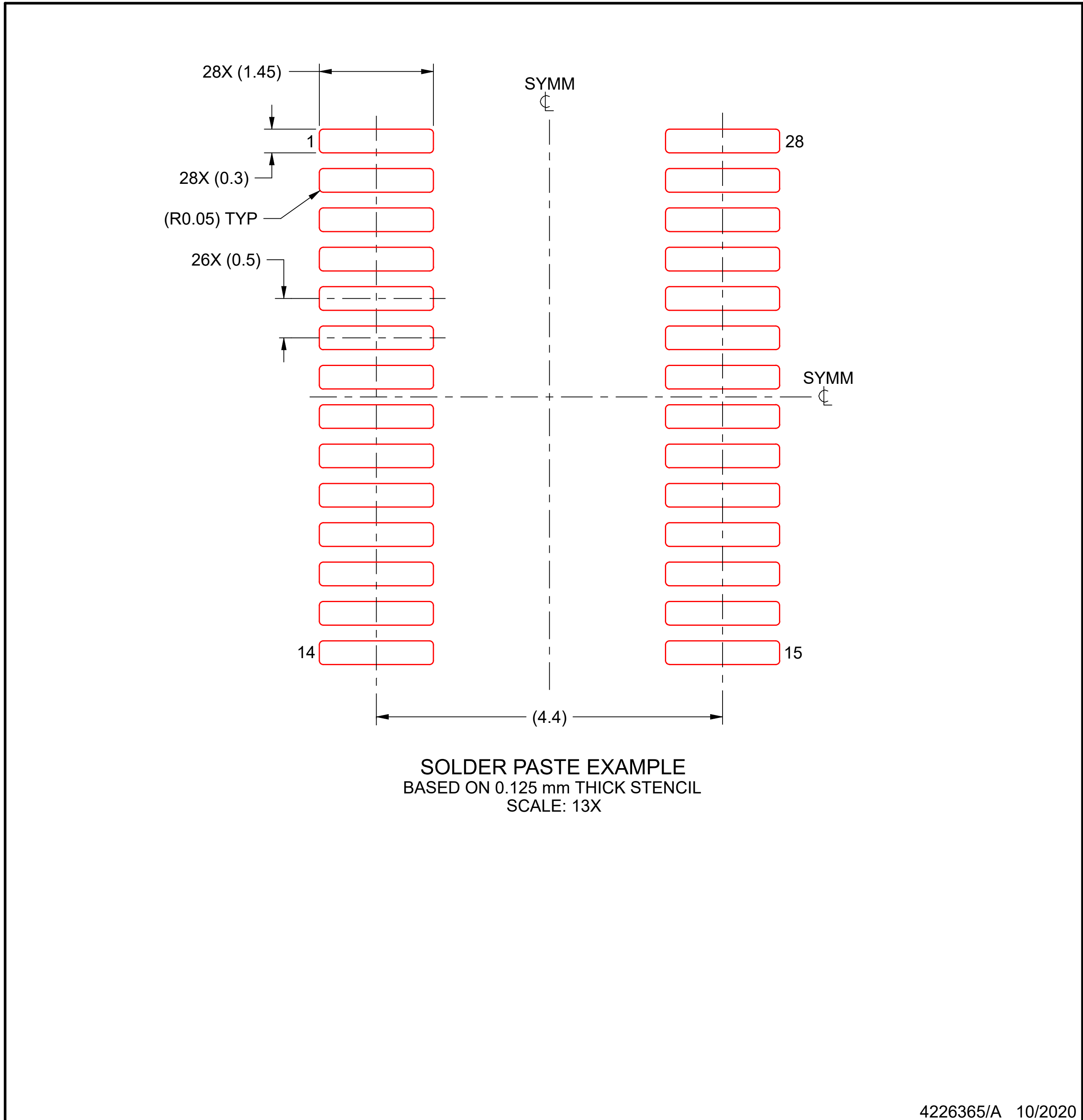
EXAMPLE STENCIL DESIGN

DGS0028A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

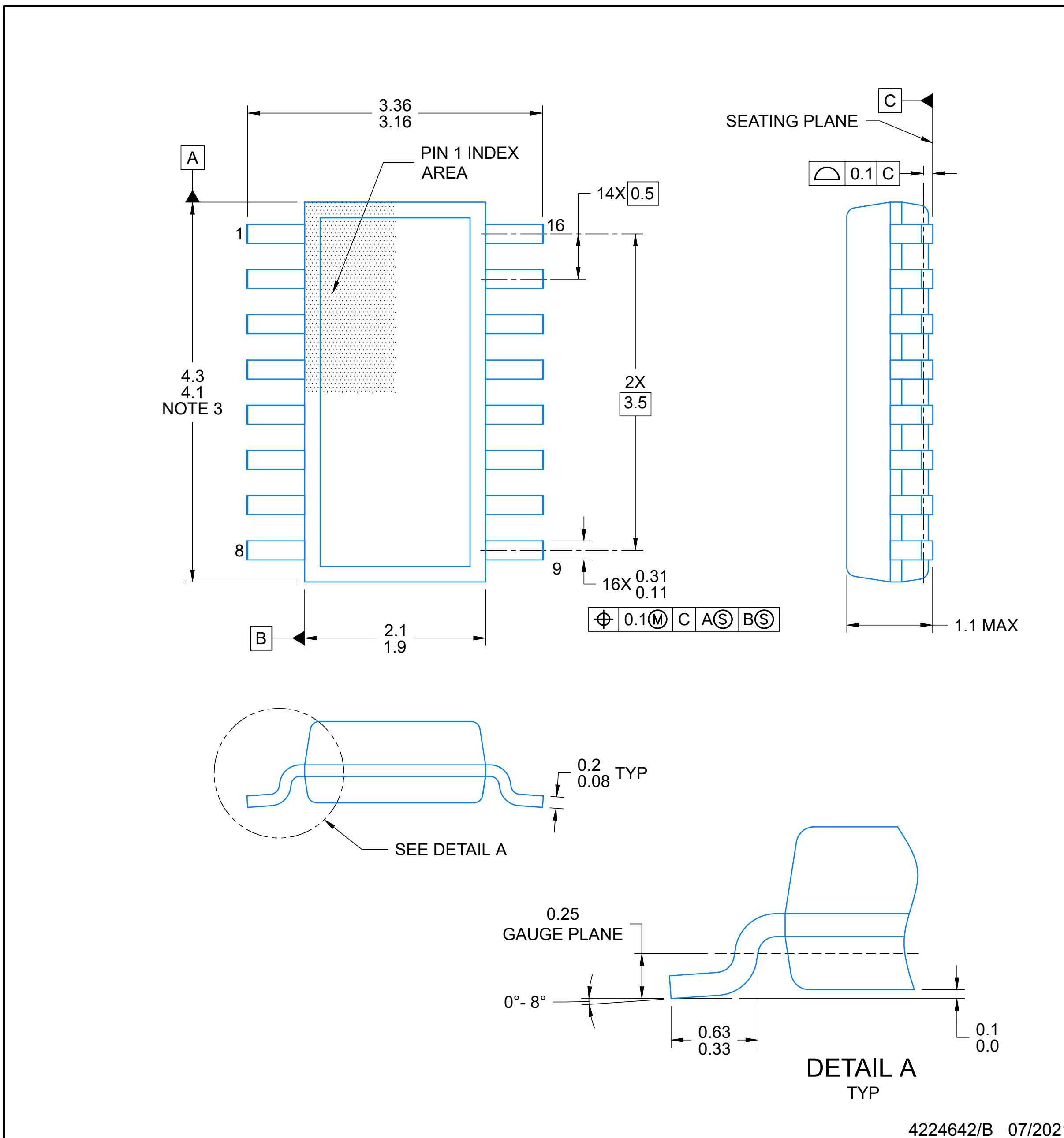
ADVANCE INFORMATION

ADVANCE INFORMATION

PACKAGE OUTLINE

DYY0016A SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AA

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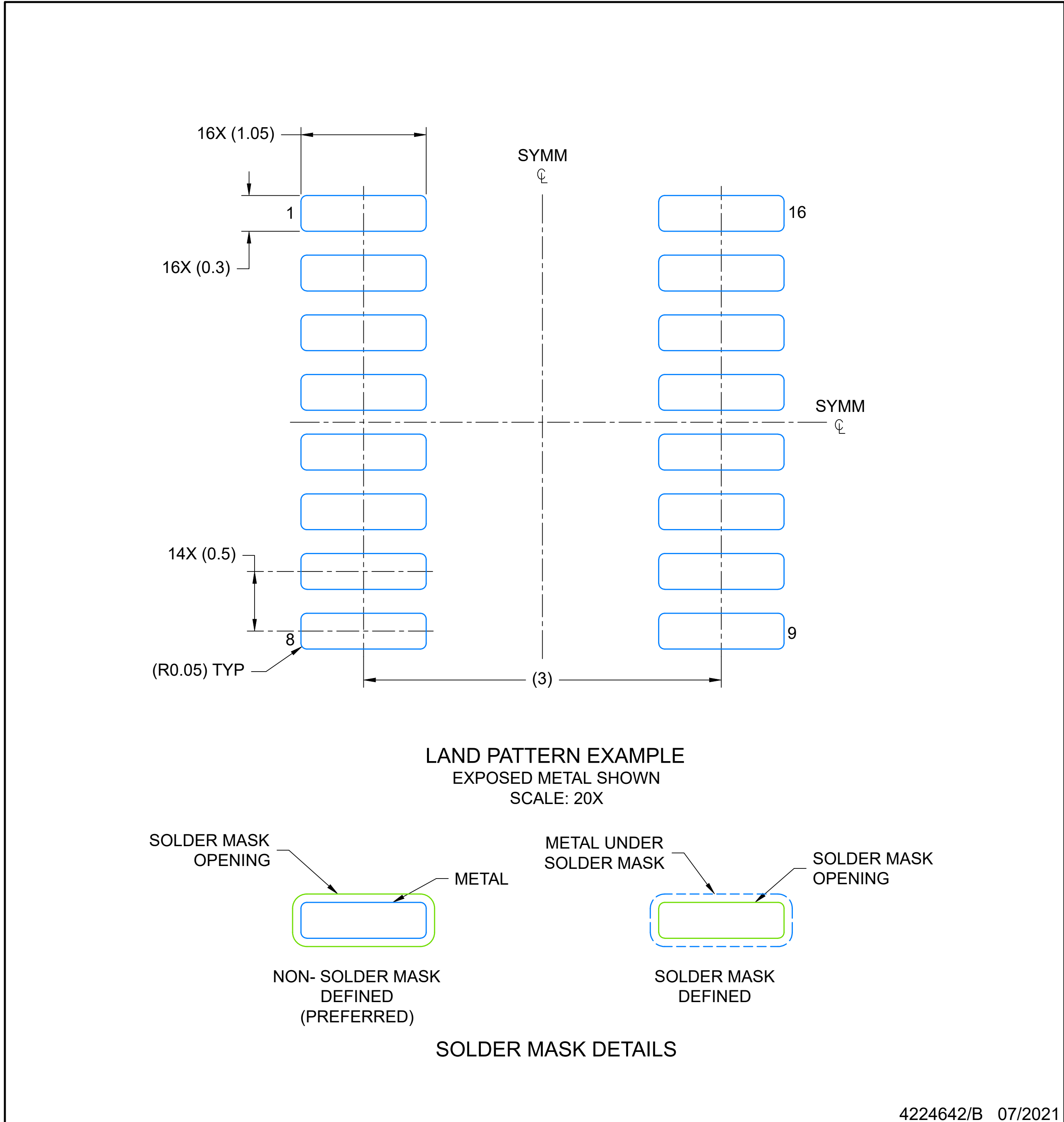
EXAMPLE BOARD LAYOUT

DYY0016A SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

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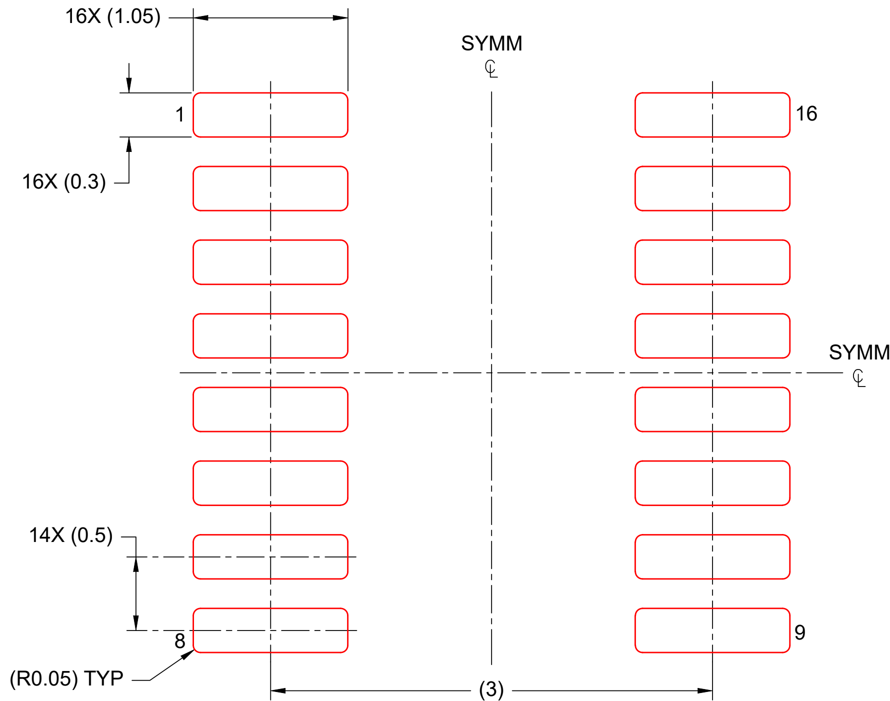
ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

DYY0016A SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

4224642/B 07/2021

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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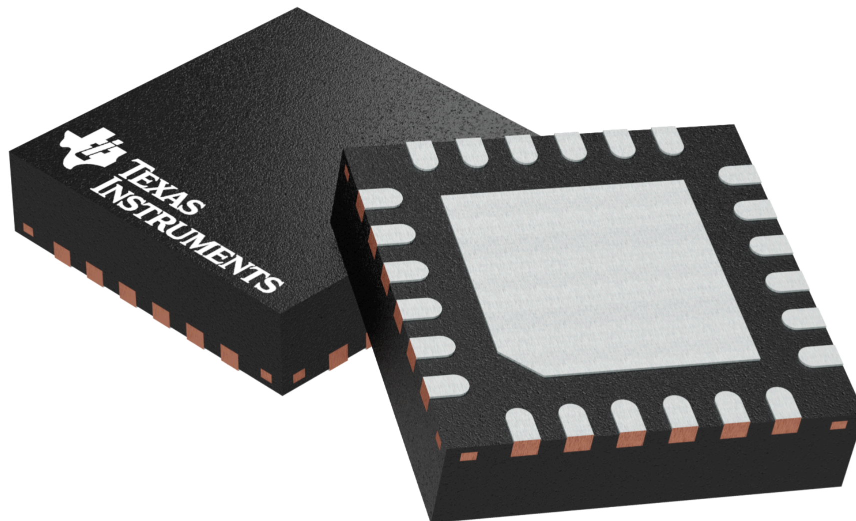
GENERIC PACKAGE VIEW

RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



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Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4204104/H

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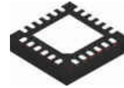
ADVANCE INFORMATION



PACKAGE OUTLINE

RGE0024B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

A B 4.1 3.9 PIN 1 INDEX AREA 4.1 3.9 0.5 0.3 0.3 0.2 DETAIL OPTIONAL TERMINAL TYPICAL

1 MAX C SEATING PLANE 0.05 0.00 0.08 C

2X 2.5 2.45±0.1 7 12 SEE TERMINAL DETAIL 6 EXPOSED THERMAL PAD 13 (0.2) TYP 2X 2.5 25 SYMM 20X 0.5 1 18 24X 0.3 0.2 PIN 1 ID (OPTIONAL) 24 SYMM 19 0.1 C A B 0.05 24X 0.5 0.3

4219013/A 05/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

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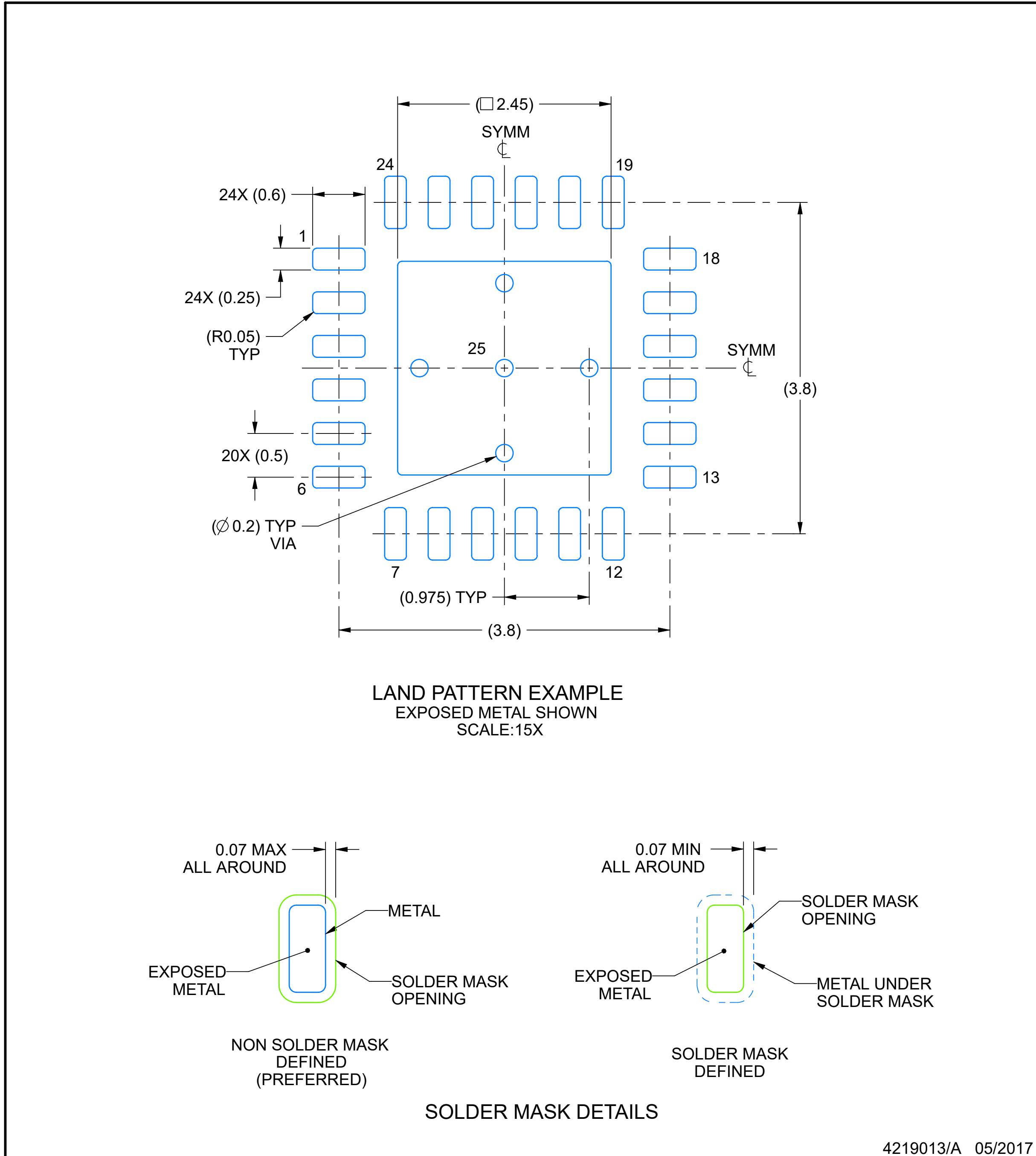
EXAMPLE BOARD LAYOUT

RGE0024B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

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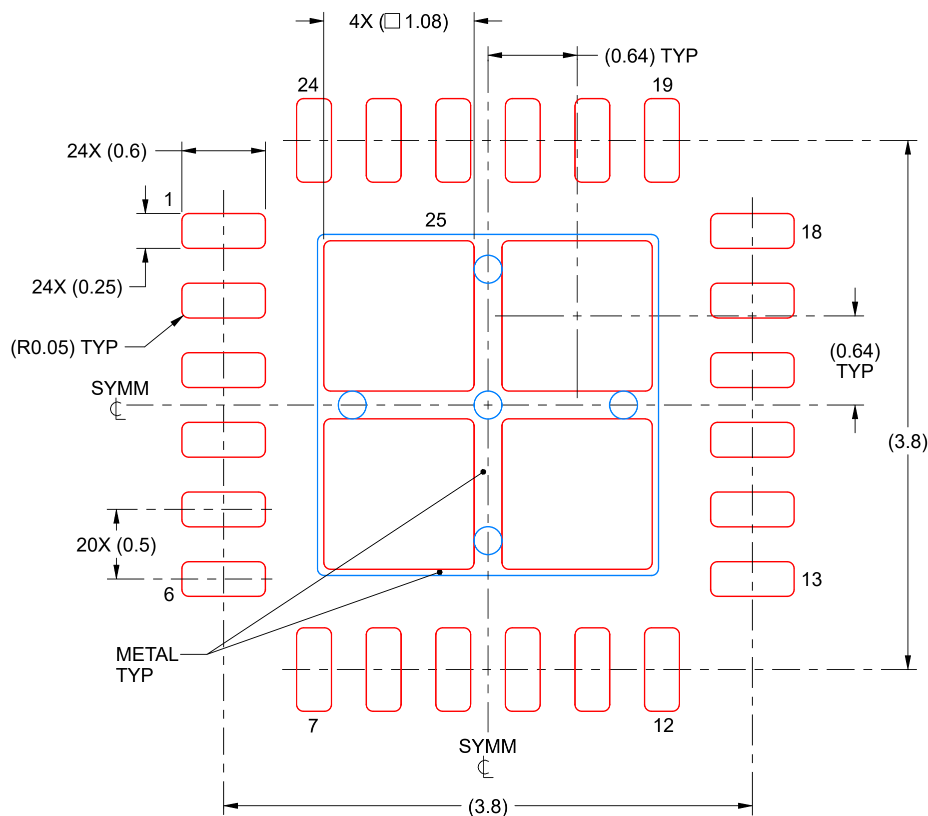
EXAMPLE STENCIL DESIGN

RGE0024B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4219013/A 05/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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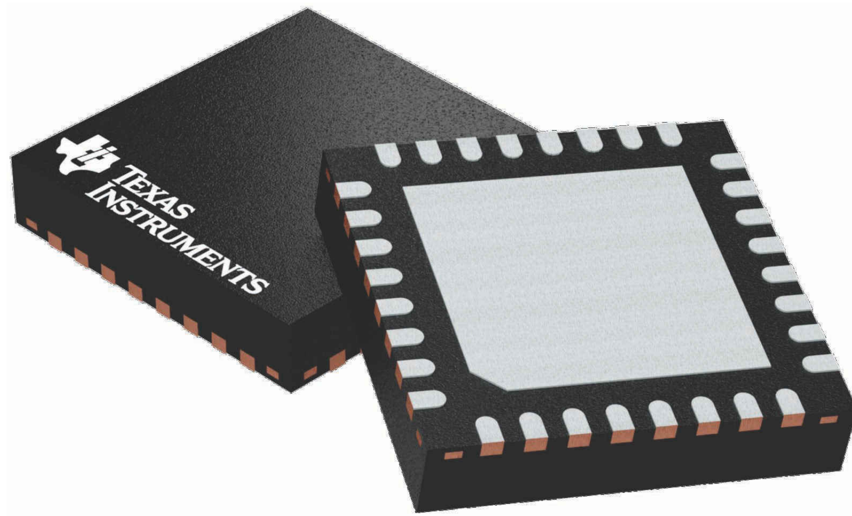
GENERIC PACKAGE VIEW

RHB 32 **VQFN - 1 mm max height**

5 x 5, 0.5 mm pitch PLASTIC QUAD FLATPACK - NO LEAD



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Refer to the product data sheet for package details.

4224745/A

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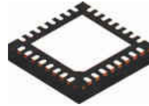
ADVANCE INFORMATION

PACKAGE OUTLINE

RHB0032E



VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

A
5.1
4.9
B
PIN 1 INDEX AREA
5.1
4.9
(0.1)
SIDE WALL DETAIL
OPTIONAL METAL THICKNESS
1 MAX
C
SEATING PLANE
0.05
0.00
0.08 C
2X 3.5
□3.45±0.1
9
16
EXPOSED
THERMAL PAD
(0.2) TYP
28X 0.5
8
17
SEE SIDE WALL
DETAIL
2X
3.5
33
SYMM
℄
32X 0.3
0.2
1
24
0.1Ⓜ C A B
0.05Ⓜ C
PIN 1 ID
(OPTIONAL)
32
25
SYMM
℄
32X 0.5
0.3

4223442/B 08/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

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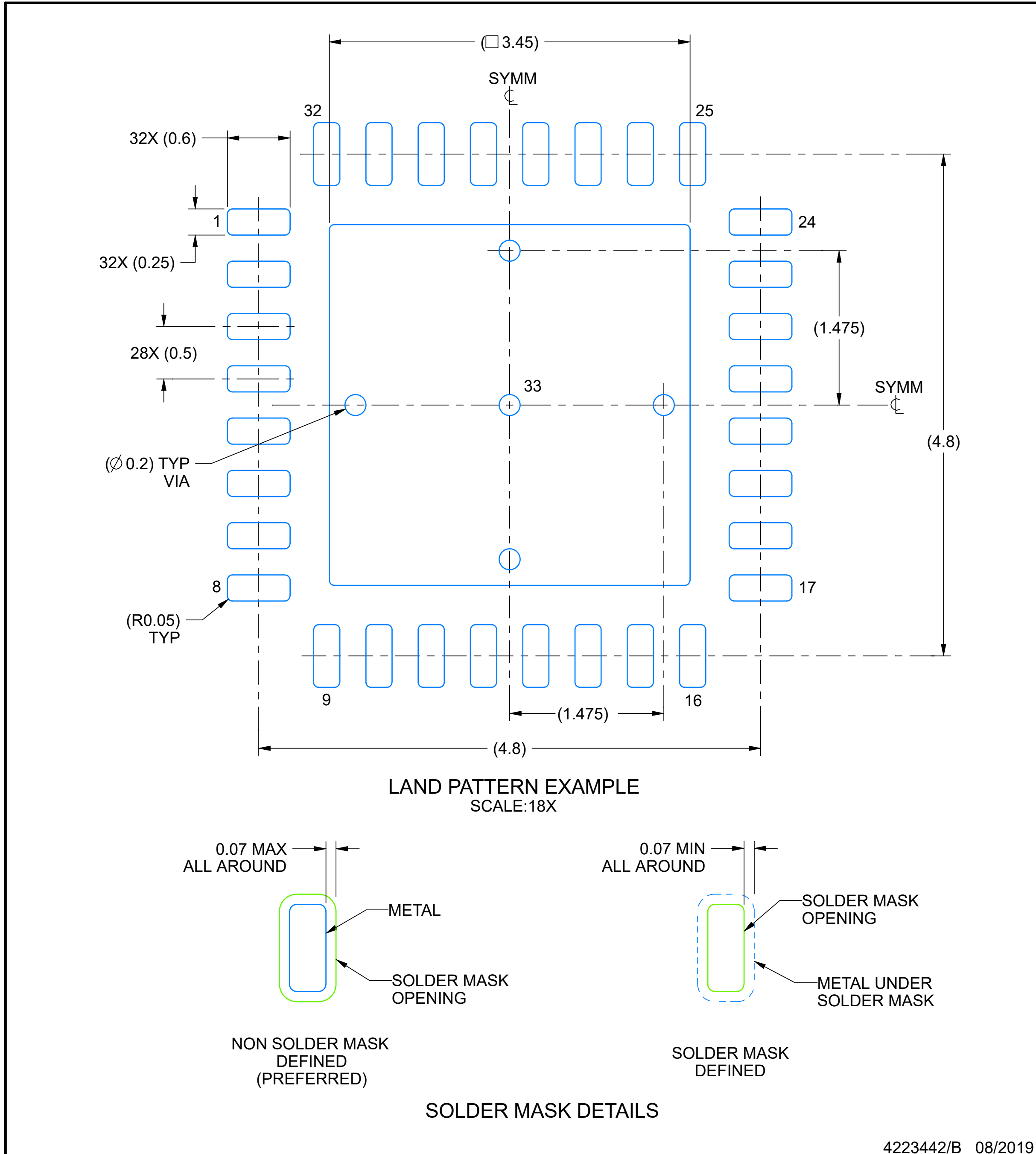
ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

RHB0032E VQFN - 1 mm max height

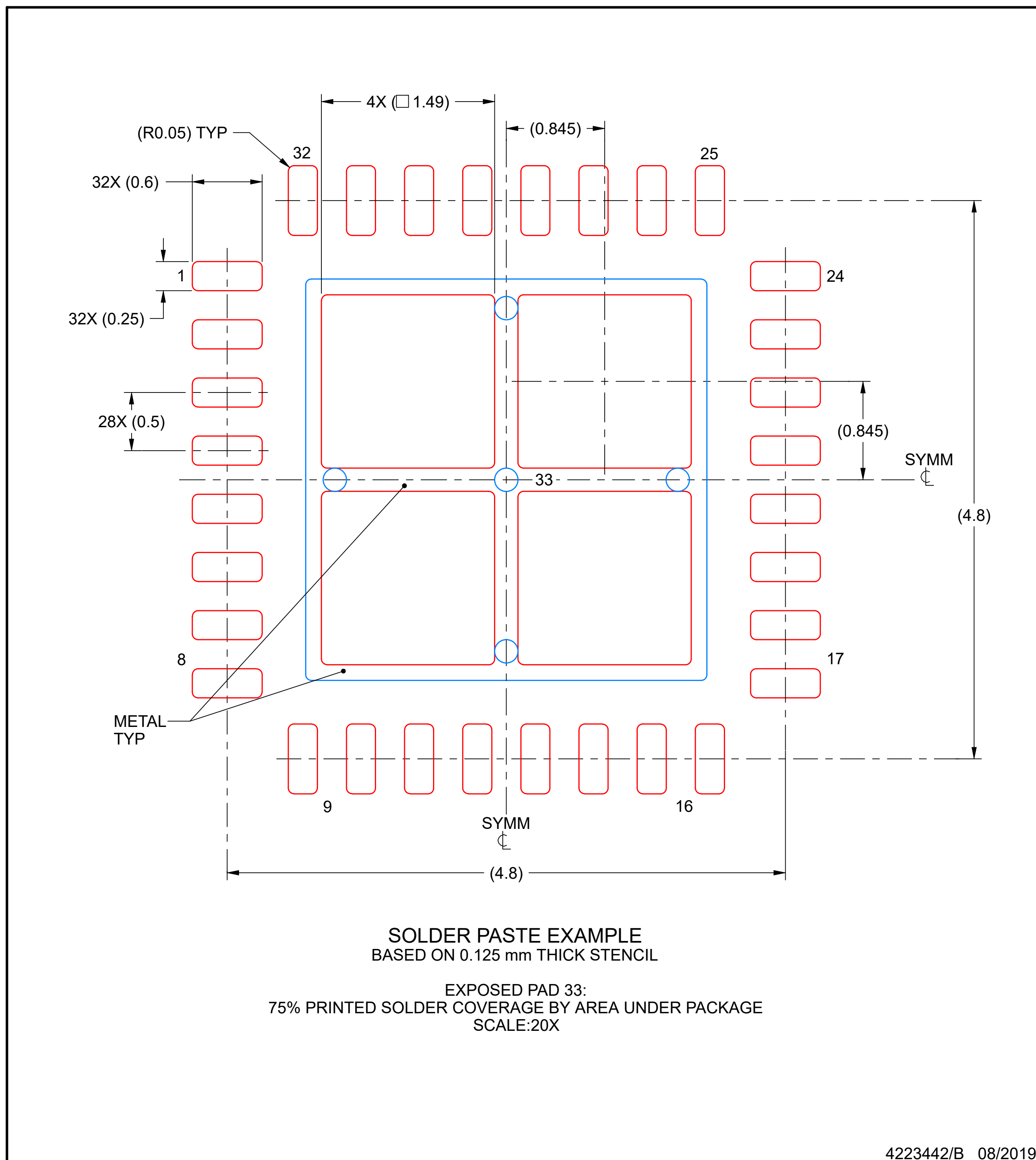
PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

ADVANCE INFORMATION



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
October 2022	*	Initial Release

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
XMSM0L1303SRGER	ACTIVE	VQFN	RGE	24	3000	TBD	Call TI	Call TI	-40 to 125		Samples
XMSM0L1304SDGS20R	ACTIVE	VSSOP	DGS	20	5000	TBD	Call TI	Call TI	-40 to 125		Samples
XMSM0L1304SDGS28R	ACTIVE	VSSOP	DGS	28	5000	TBD	Call TI	Call TI	-40 to 125		Samples
XMSM0L1304SDYYR	ACTIVE	SOT-23-THIN	DYY	16	3000	TBD	Call TI	Call TI	-40 to 125		Samples
XMSM0L1304SRGER	ACTIVE	VQFN	RGE	24	3000	TBD	Call TI	Call TI	-40 to 125		Samples
XMSM0L1304SRHBR	ACTIVE	VQFN	RHB	32	3000	TBD	Call TI	Call TI	-40 to 125		Samples
XMSM0L1305SDGS20R	ACTIVE	VSSOP	DGS	20	5000	TBD	Call TI	Call TI	-40 to 125		Samples
XMSM0L1305SDGS28R	ACTIVE	VSSOP	DGS	28	5000	TBD	Call TI	Call TI	-40 to 125		Samples
XMSM0L1305SDYYR	ACTIVE	SOT-23-THIN	DYY	16	3000	TBD	Call TI	Call TI	-40 to 125		Samples
XMSM0L1305SRGER	ACTIVE	VQFN	RGE	24	3000	TBD	Call TI	Call TI	-40 to 125		Samples
XMSM0L1305SRHBR	ACTIVE	VQFN	RHB	32	3000	TBD	Call TI	Call TI	-40 to 125		Samples
XMSM0L1306SDGS20R	ACTIVE	VSSOP	DGS	20	5000	TBD	Call TI	Call TI	-40 to 125		Samples
XMSM0L1306SDGS28R	ACTIVE	VSSOP	DGS	28	5000	TBD	Call TI	Call TI	-40 to 125		Samples
XMSM0L1306SDYYR	ACTIVE	SOT-23-THIN	DYY	16	3000	TBD	Call TI	Call TI	-40 to 125		Samples
XMSM0L1306SRGER	ACTIVE	VQFN	RGE	24	5000	TBD	Call TI	Call TI	-40 to 125		Samples
XMSM0L1306SRHBR	ACTIVE	VQFN	RHB	32	5000	TBD	Call TI	Call TI	-40 to 125		Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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