NIPPON PRECISION CIRCUITS INC.

# SM8706A

## Clock Generator for DVD Players

## OVERVIEW

The SM8706A is a clock generator IC that generates 3 clocks with 6 outputs from a 36.8640MHz master clock for application in DVD players. The SM8706A has 2 built-in PLL circuits that together with a crystal oscillator can generate the 384fs and 768fs audio system clocks, 27MHz and 54MHz video system clocks, and 16.9344MHz and 33.8688MHz signal processor system clocks required for a DVD player. The SM8706A also supports the 44.1kHz and 48kHz sampling frequencies, and the sampling frequency can be switched while the device is operating.

## FEATURES

- 36.8640MHz master clock (internal PLL reference clock)
- Generated clocks
  - Video system output: 27MHz, 54MHz
  - Audio system output: 384fs, 768fs
  - Signal processor system output: 16.9344MHz, 33.8688MHz
- Supported sampling frequency fs: 44.1/48kHz
- Low jitter output: 40ps (typ, 1-sigma, 25pF load)
- Supply voltage: 3.3V ± 0.3V
- 16-pin VSOP package

## APPLICATIONS

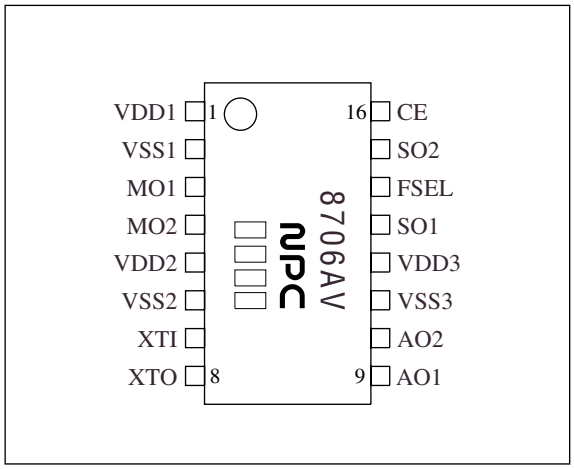
- DVD players
- DVD car navigation system

## ORDERING INFORMATION

| Device | Package |
|---|---|
| SM8706AV | 16-pin VSOP |

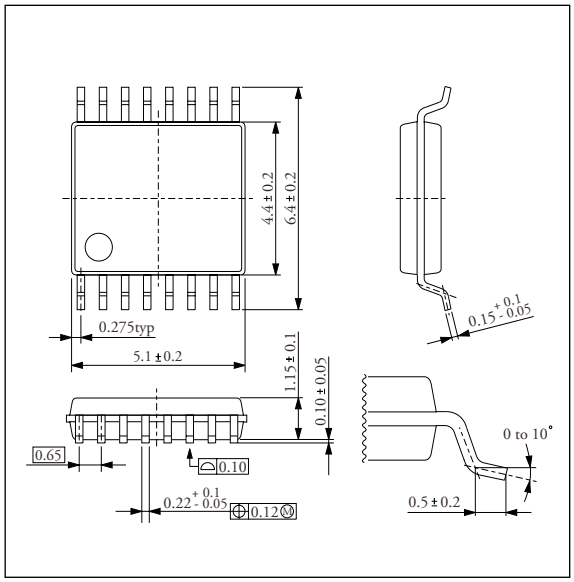
## PINOUT

(Top view)

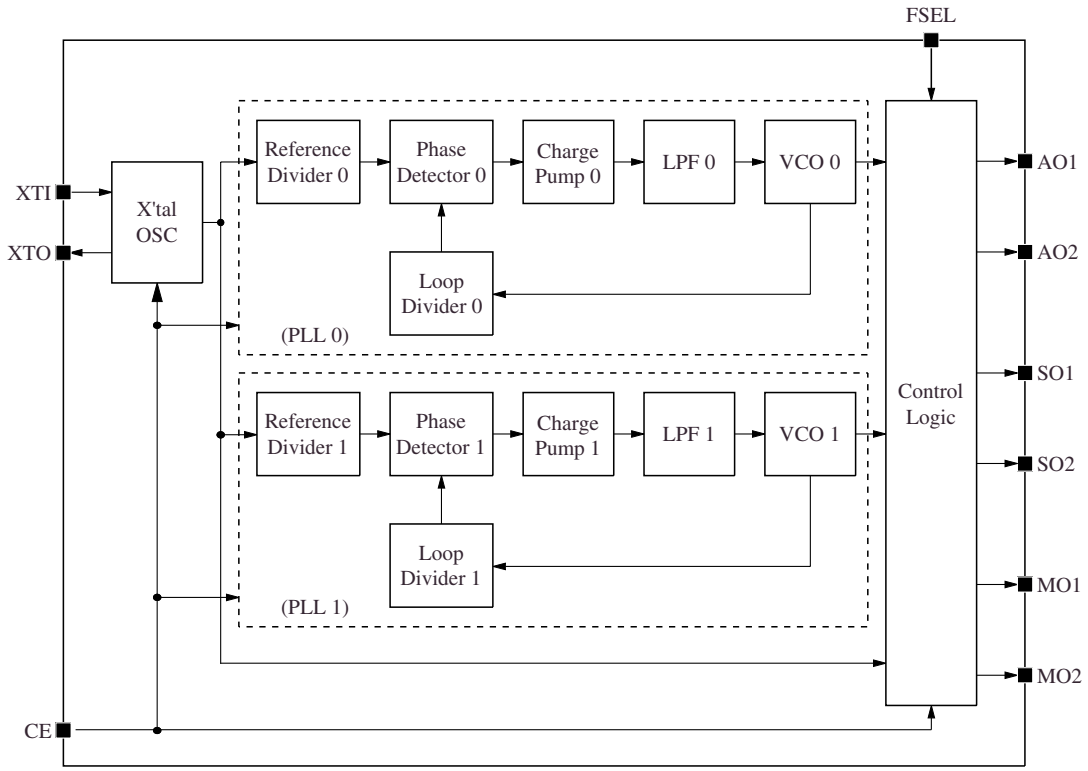



## PACKAGE DIMENSIONS

(Unit: mm)
Weight: 0.07g



## BLOCK DIAGRAM




## PIN DESCRIPTION

| Number | Name | I/O | Description |
|---|---|---|---|
| 1 | VDD1 | – | Supply 1 for digital block |
| 2 | VSS1 | – | Ground 1 for digital block |
| 3 | MO1 | O | Video system output 1 (27MHz fixed) |
| 4 | MO2 | O | Video system output 2 (54MHz fixed) |
| 5 | VDD2 | – | Supply 2 for analog block |
| 6 | VSS2 | – | Ground 2 for analog block |
| 7 | XTI | I | Crystal oscillator connection or external clock input |
| 8 | XTO | O | Crystal oscillator connection |
| 9 | AO1 | O | Audio system output 1 (384fs output) |
| 10 | AO2 | O | Audio system output 2 (768fs output) |
| 11 | VSS3 | – | Ground 3 for digital block |
| 12 | VDD3 | – | Supply 3 for digital block |
| 13 | SO1 | O | Signal processor system output 1 (16.9344MHz fixed) |
| 14 | FSEL | I | Sampling frequency select<br>FSEL = HIGH: fs = 48kHz<br>FSEL = LOW: fs = 44.1kHz<br>(with internal pull-up resistor, Schmitt-trigger input) |
| 15 | SO2 | O | Signal processor system output 2 (33.8688MHz fixed) |
| 16 | CE | I | Chip enable (HIGH = Enable, LOW = Disable) |

Note: Unless otherwise noted, VDD applies to VDD1, VDD2, and VDD3. Similarly, VSS applies to VSS1, VSS2, and VSS3.

# SPECIFICATIONS

## Absolute Maximum Ratings

| Parameter | Symbol | Condition | Rating | Unit |
|---|---|---|---|---|
| Supply voltage range | $V_{DD1}$ , $V_{DD2}$ , $V_{DD3}$ | | – 0.3 to 6.5 | V |
| Supply voltage deviation | $V_{DD1} - V_{DD2}$ , $V_{DD1} - V_{DD3}$ , $V_{DD2} - V_{DD3}$ | | ± 0.1 | V |
| Input voltage range | $V_{IN}$ | | – 0.3 to $V_{DD}$ + 0.3 | V |
| Output voltage range | $V_{OUT}$ | | – 0.3 to $V_{DD}$ + 0.3 | V |
| Power dissipation | $P_D$ | | 165 | mW |
| Storage temperature range | $T_{stg}$ | | – 55 to 125 | °C |

## Recommended Operating Conditions

$V_{SS} = V_{SS1} = V_{SS2} = V_{SS3} = 0V$ unless otherwise noted.

| Parameter | Symbol | Condition | Rating | | | Unit |
|---|---|---|---|---|---|---|
| | | | min | typ | max | |
| Supply voltage ranges[1, 2, 3] | $V_{DD1}$ , $V_{DD2}$ , $V_{DD3}$ | | + 3.0 | – | + 3.6 | V |
| Output load capacitance 1 | $C_{L1}$ | MO1, SO1, SO2 outputs | – | – | 25 | pF |
| Output load capacitance 2 | $C_{L2}$ | All outputs excluding MO1, SO1, SO2, XTO | – | – | 15 | pF |
| Master clock frequency | $f_{XTAL}$ | When using crystal oscillator | – | 36.8640 | – | MHz |
| Operating temperature range | $T_{opr}$ | | – 40 | – | + 85 | °C |

1. The supply voltage is defined relative to $V_{SS}$ = 0V
2. The supply voltages applied on VDD1, VDD2, and VDD3 should be derived from a common supply source.
3. If the supply voltages on VDD1, VDD2, and VDD3 are from different sources, they should be applied simultaneously. The SM8706A may be damaged if the supply voltage timing is different.

## DC Electrical Characteristics

$f_{XTAL}$ = 36.8640MHz, $V_{DD}$ = 3.0V ± 0.3V, $V_{SS}$ = 0V, Ta = – 40 to 85 °C unless otherwise noted.

| Parameter | Symbol | Condition | Rating | | | Unit |
|---|---|---|---|---|---|---|
| | | | min | typ | max | |
| Current consumption | $I_{DD}$ | $V_{DD}$ = 3.3V, Ta = 25°C, fs = 48kHz, Crystal oscillator, no load on all outputs | – | 35 | 45 | mA |
| HIGH-level input voltage | $V_{IH}$ | FSEL, CE, XTI, $V_{DD}$ = 3.3V | 0.8 $V_{DD}$ | – | – | V |
| LOW-level input voltage | $V_{IL}$ | | – | – | 0.2 $V_{DD}$ | V |
| HIGH-level input current[1] | $I_{IH1}$ | FSEL, CE, $V_{IN} = V_{DD}$ | – | – | 1 | µA |
| LOW-level input current[1] | $I_{IL1}$ | FSEL, CE, $V_{IN}$ = 0V | – 100 | – | – | µA |
| HIGH-level input current | $I_{IH2}$ | XTI, $V_{IN} = V_{DD}$ | – | – | 40 | µA |
| LOW-level input current | $I_{IL2}$ | XTI, $V_{IN}$ = 0V | – 40 | – | – | µA |
| HIGH-level output voltage | $V_{OH}$ | All outputs excluding XTO, $I_{OH}$ = – 2mA | $V_{DD}$ – 0.4 | – | – | V |
| LOW-level output voltage | $V_{OL}$ | All outputs excluding XTO, $I_{OL}$ = 2mA | – | – | 0.4 | V |

1. FSEL and CE pins have Schmitt-trigger input and built-in pull-up resistor.

## AC Electrical Characteristics

$f_{XTAL}$ = 36.8640MHz, $V_{DD}$ = 3.0V ± 0.3V, $V_{SS}$ = 0V, Ta = – 40 to 85 °C unless otherwise noted.

| Parameter | Symbol | Condition | Rating | | | Unit |
|---|---|---|---|---|---|---|
| | | | min | typ | max | |
| External input clock frequency[1] | $f_{XTI}$ | XTI, applies to external clock input use only | – | 36.8640 | – | MHz |
| Output clock rise time[2] | $t_r$ | MO1, SO1, SO2, $C_L$ = 25 pF, transition between $V_{OL}$ = 0.2$V_{DD}$ and $V_{OH}$ = 0.8$V_{DD}$ | – | 2.0 | – | ns |
| | | Outputs excluding MO1, SO1, SO2, and XTO, $C_L$ = 15pF, transition between $V_{OL}$ = 0.2$V_{DD}$ and $V_{OH}$ = 0.8$V_{DD}$ | – | 2.0 | – | |
| Output clock fall time[2] | $t_f$ | MO1, SO1, SO2, $C_L$ = 25pF, transition between $V_{OH}$ = 0.8$V_{DD}$ and $V_{OL}$ = 0.2$V_{DD}$ | – | 2.0 | – | ns |
| | | Outputs excluding MO1, SO1, SO2, and XTO, $C_L$ = 15pF, transition between $V_{OH}$ = 0.8$V_{DD}$ and $V_{OL}$ = 0.2$V_{DD}$ | – | 2.0 | – | |
| Output clock jitter[3] | $t_{jitter}$ (1-sigma) | MO1, SO1, SO2, Ta = 25°C, $C_L$ = 25pF, $V_O$ = 0.5$V_{DD}$ | – | 40 | – | ps |
| | | Outputs excluding MO1, SO1, SO2, and XTO, Ta = 25°C, $C_L$ = 15pF, $V_O$ = 0.5$V_{DD}$ | – | 40 | – | |
| Output clock duty cycle[2] | Dt | MO1, SO1, SO2, Ta = 25°C, $C_L$ = 25pF, $V_O$ = 0.5$V_{DD}$ | 45 | 50 | 55 | % |
| | | Outputs excluding MO1, SO1, SO2, and XTO, Ta = 25°C, $C_L$ =15 pF, $V_O$ = 0.5$V_{DD}$ | 45 | 50 | 55 | |
| Settling time[2] | $t_S$ | All outputs excluding XTO | – | – | 1 | µs |
| Power-up time[2,4] | $t_P$ | All outputs excluding XTO | – | 1 | 5 | ms |

1. When using an external clock input, the XTI duty should be 50% with 3.3V clock signal amplitude level. The input signal voltage should not exceed the absolute maximum rating, otherwise damage may occur.
2. The numeric values are measured values obtained using the circuit in Figure 1 and the NPC standard evaluation board.
3. The numeric values are measured values obtained using the circuit in Figure 2 and the NPC standard evaluation board.
4. This is the time, after the supply is turned ON from the OFF state, until the output clock reaches ± 0.1% of the specified frequency.

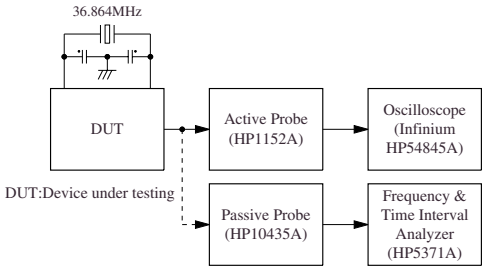



Figure 1. Measurement circuit 1

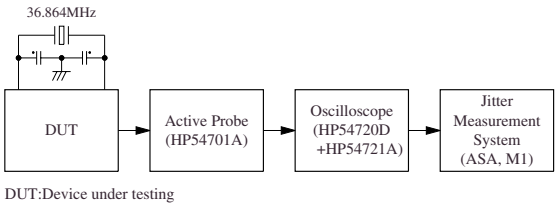



Figure 2. Measurement circuit 2

# FUNCTIONAL DESCRIPTION

## 36.8640MHz Master Clock

The SM8706A 36.8640MHz master clock circuit is configured, as shown in Figure 3, with the crystal oscillator element connected between XTI (pin 7) and XTO (pin 8).

Alternatively, the 36.8640MHz master clock can be supplied from an external master clock input on XTI, as shown in Figure 4.

If an external input clock on XTI is used, it is recommended that the frequency be 36.8640MHz, with 50% duty, and 3.3V voltage amplitude level.

Furthermore, when using an external clock input, the input signal voltage should not exceed the absolute maximum rating, otherwise damage may occur.

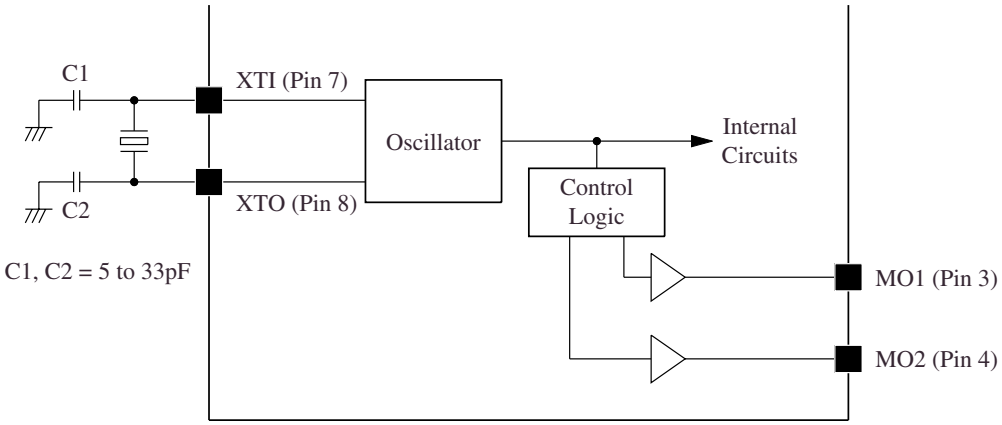



Figure 3. Crystal oscillator connection

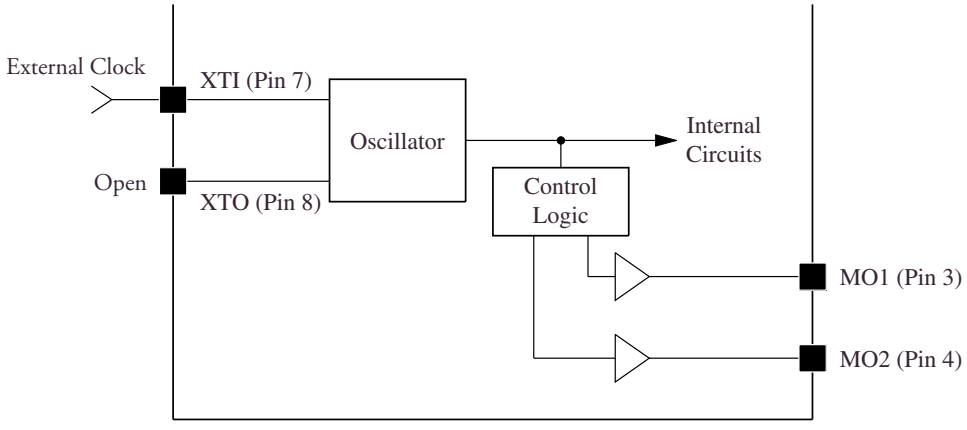



Figure 4. External clock input

## Sampling Frequency and Output Clock Frequency

The SM8706A sampling frequency fs can be switched between 44.1kHz when FSEL (pin 14) is LOW, and 48kHz when FSEL is HIGH. The audio outputs (AO1 and AO2) are a 384fs and 768fs frequency clock, respectively, where fs is determined by the setting on FSEL. In addition, the signal processor outputs (SO1 and SO2) are a 16.9344MHz and 33.8688MHz frequency clock, respectively, derived from the master clock. The video outputs (MO1 and MO2) are a 27MHz and 54MHz frequency clock, respectively, derived from the master clock.

When CE (Pin16) is HIGH, the chip is enabled. When LOW, the chip is disabled. When disabled, all output go LOW and all internal circuits stop operating. When CE goes LOW to HIGH, the chip moves from disabled to enabled, the time taken until the output frequency clocks stabilize is a maximum of 5ms.

The SM8706A output clock frequencies that can be selected is shown in Table 1. The output clock response timing relative to the CE setting is shown in Figure 5.

Table 1. Sampling frequency and output clock frequency (36.8640MHz master clock frequency)

| FSEL (Pin 14) | Sampling frequency fs [kHz] | CE (Pin 16) | Output clock frequency [MHz] | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | AO1 (Pin 9) | AO2 (Pin 10) | SO1 (Pin 13) | SO2 (Pin 15) | MO1 (Pin 3) | MO2 (Pin 4) |
| LOW | 44.1 | H | 16.9344 | 33.8688 | 16.9344 | 33.8688 | 27.0000 | 54.0000 |
| HIGH | 48 | | 18.4320 | 36.8640 | 16.9344 | 33.8688 | 27.0000 | 54.0000 |
| LOW | 44.1 | L | L | L | L | L | L | L |
| HIGH | 48 | | | | | | | |

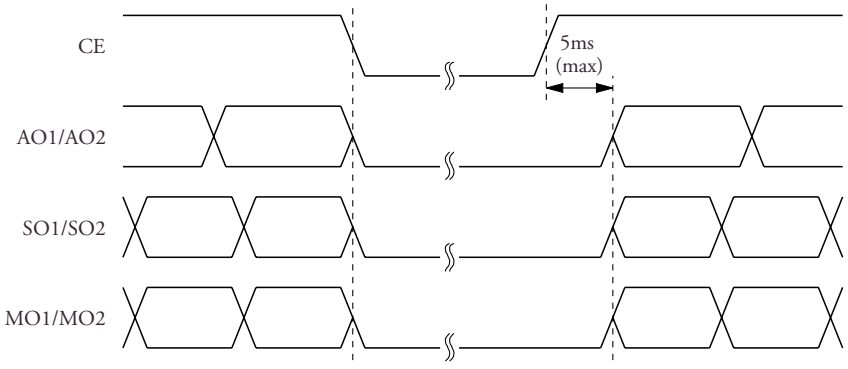



Figure 5. CE switching response

## Sampling Frequency Switching Settling Time

The clock output response timing when the sampling frequency fs is switched using FSEL is shown in Figure 6. The settling time $t_s$ for the audio output clock when switching the sampling frequency is 1µs maximum.

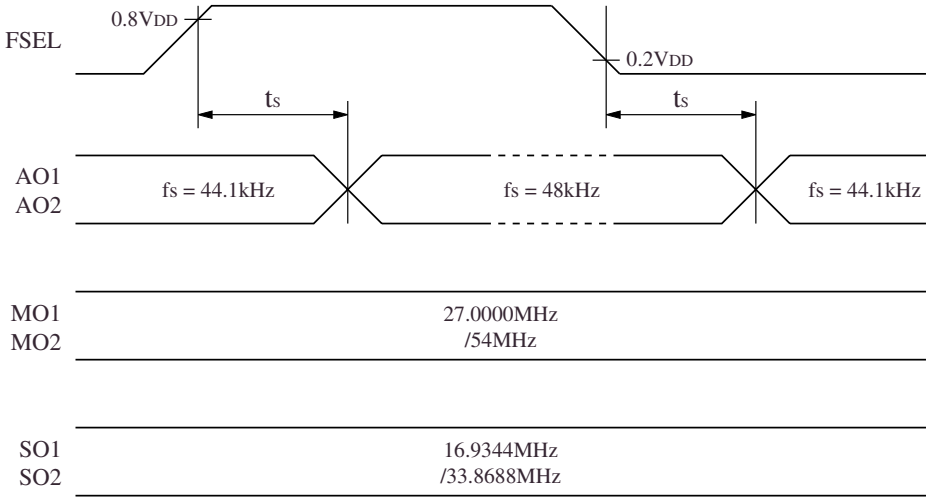



Figure 6. Output signal switching timing

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