M466F0804DT1-L EDO Mode

8M x 64 DRAM SODIMM Using 4Mx16, 4K Refresh 3.3V, Low power/Self-Refresh

GENERAL DESCRIPTION

The Samsung M466F0804DT1-L is a 8Mx64bits Dynamic RAM high density memory module. The Samsung M466F0804DT1-L consists of eight CMOS 4Mx16bits DRAMs in TSOP 400mil packages and a 2K EEPROM in 8-pin TSSOP package mounted on a 144-pin glass-epoxy sub-strate. A 0.1uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The M466F0804DT1-L is a Small Out-line Dual in-line Memory Module and is intended for mounting into 144 pin edge connector sockets.

FEATURES

- Part Identification
  - M466F0804DT1-L(4096 cycles/128ms, TSOP, L-ver)
- Extended Data Out Mode Operation
- New JEDEC standard proposal with EEPROM
- Serial Presense Detect with EEPROM
- $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- Self -refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- LVTTL compatible inputs and outputs
- Single +3.3V±0.3V power supply
- PCB : Height(1000mil), double sided component

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
-L50	50ns	13ns	84ns	20ns
-L60	60ns	15ns	104ns	25ns

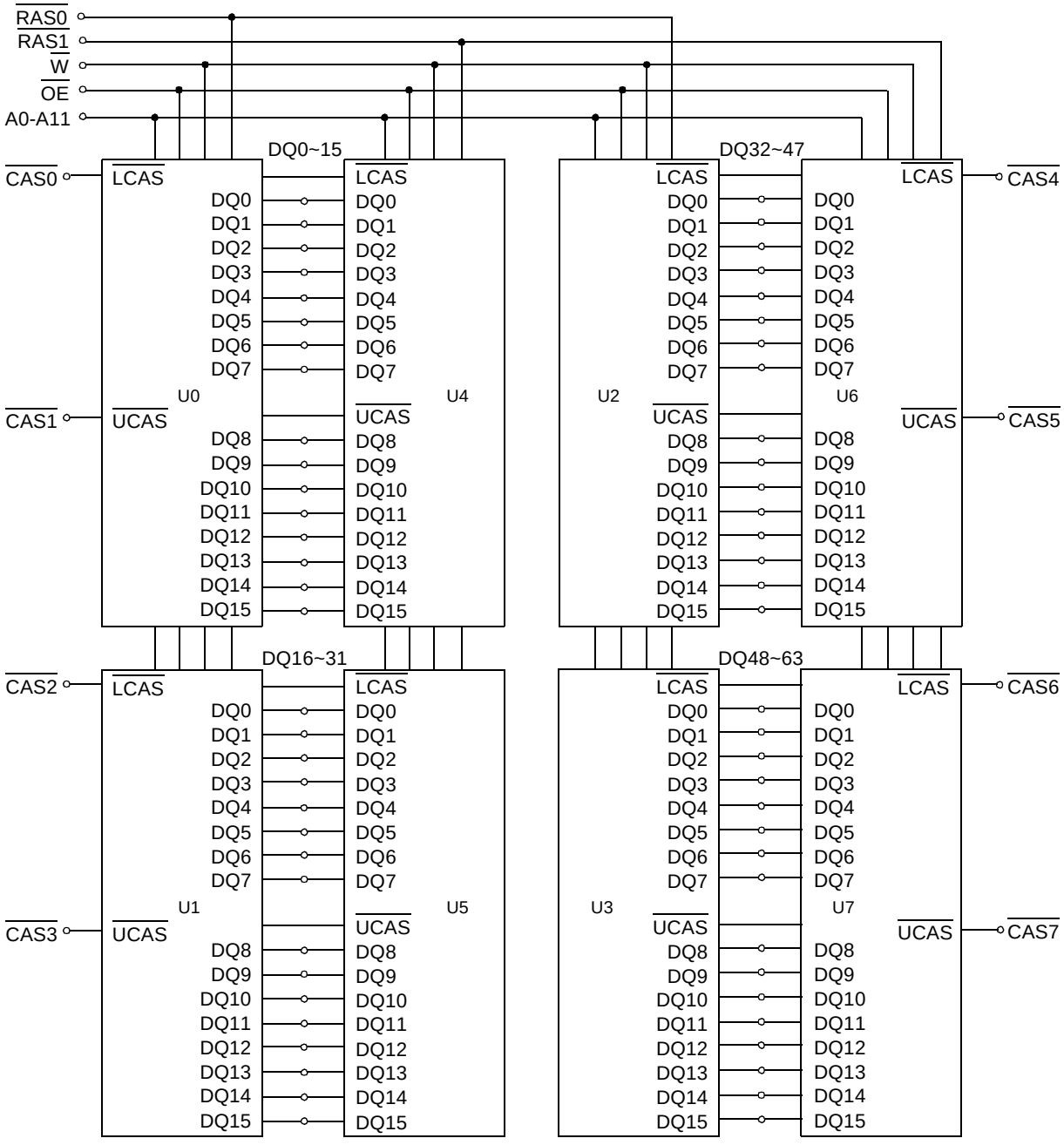
PIN CONFIGURATIONS

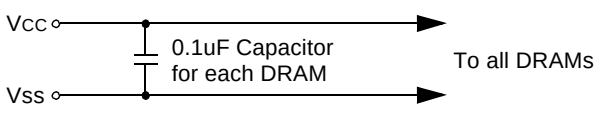
Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	Vss	2	Vss	49	DQ13	50	DQ45	97	DQ22	98	DQ54
3	DQ0	4	DQ32	51	DQ14	52	DQ46	99	DQ23	100	DQ55
5	DQ1	6	DQ33	53	DQ15	54	DQ47	101	Vcc	102	Vcc
7	DQ2	8	DQ34	55	Vss	56	Vss	103	A6	104	A7
9	DQ3	10	DQ35	57	RSVD	58	RSVD	105	A8	106	A11
11	Vcc	12	Vcc	59	RSVD	60	RSVD	107	Vss	108	Vss
13	DQ4	14	DQ36	61	RFU	62	RFU	109	A9	110	NC
15	DQ5	16	DQ37	63	Vcc	64	Vcc	111	A10	112	NC
17	DQ6	18	DQ38	65	RFU	66	RFU	113	Vcc	114	Vcc
19	DQ7	20	DQ39	67	$\overline{W}$	68	RFU	115	$\overline{CAS2}$	116	$\overline{CAS6}$
21	Vss	22	Vss	69	$\overline{RAS0}$	70	RFU	117	$\overline{CAS3}$	118	$\overline{CAS7}$
23	$\overline{CAS0}$	24	$\overline{CAS4}$	71	$\overline{RAS1}$	72	RFU	119	Vss	120	Vss
25	$\overline{CAS1}$	26	$\overline{CAS5}$	73	$\overline{OE}$	74	RFU	121	DQ24	122	DQ56
27	Vcc	28	Vcc	75	Vss	76	Vss	123	DQ25	124	DQ57
29	A0	30	A3	77	RSVD	78	RSVD	125	DQ26	126	DQ58
31	A1	32	A4	79	RSVD	80	RSVD	127	DQ27	128	DQ59
33	A2	34	A5	81	Vcc	82	Vcc	129	Vcc	130	Vcc
35	Vss	36	Vss	83	DQ16	84	DQ48	131	DQ28	132	DQ60
37	DQ8	38	DQ40	85	DQ17	86	DQ49	133	DQ29	134	DQ61
39	DQ9	40	DQ41	87	DQ18	88	DQ50	135	DQ30	136	DQ62
41	DQ10	42	DQ42	89	DQ19	90	DQ51	137	DQ31	138	DQ63
43	DQ11	44	DQ43	91	Vss	92	Vss	139	Vss	140	Vss
45	Vcc	46	Vcc	93	DQ20	94	DQ52	141	SDA	142	SCL
47	DQ12	48	DQ44	95	DQ21	96	DQ53	143	Vcc	144	Vcc

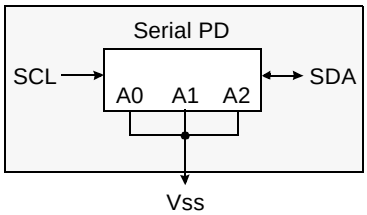
PIN NAMES

Pin Name	Function
A0 to	Address Inputs
DQ0 - DQ63	Data In/Out
$\overline{W}$	Read/Write Enable
$\overline{OE}$	Output Enable
$\overline{RAS0}$, $\overline{RAS1}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS7}$	Column Address Strobe
Vcc	Power(+3.3V)
Vss	Ground
NC	No Connection
SDA	Serial Address / Data I/O
SCL	Serial Clock
RSVD	Reserved Use
RFU	Reserved for Future Use

FUNCTIONAL BLOCK DIAGRAM







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ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative V_{SS}	V_{IN}, V_{OUT}	-0.5 to +4.6	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-0.5 to +4.6	V
Storage Temperature	T_{stg}	-55 to +125	°C
Power Dissipation	P_D	8	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	V_{CC}+0.3[*1]	V
Input Low Voltage	V_{IL}	-0.3[*2]	-	0.8	V

*1 : V_{CC}+1.3V at pulse width≤15ns, which is measured at V_{CC}.
*2 : -1.3V at pulse width≤15ns, which is measured at V_{SS}.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	M466F0804DT1-L		Unit
		Min	Max	
I_{CC1}	-50 -60	- -	484 444	mA mA
I_{CC2}	Don't care	-	8	mA
I_{CC3}	-50 -60	- -	484 444	mA mA
I_{CC4}	-50 -60	- -	364 324	mA mA
I_{CC5}	Don't care	-	1.6	mA
I_{CC6}	-50 -60	- -	484 444	mA mA
I_{CC7} I_{CCS}	Don't care	- -	2.8 2.8	mA mA
$I_{I(L)}$ $I_{O(L)}$	Don't care	-10 -10	10 10	uA uA
V_{OH} V_{OL}	Don't care	2.4 -	- 0.4	V V

I_{CC1} : Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)
I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=W=V_{IH})
I_{CC3} : $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)
I_{CC4} : Extended Data Out Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{HPC}=min)
I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=W=V_{CC}-0.2V)
I_{CC6} : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)
I_{CC7} : Battery back-up current. Average power supply, Battery back-up mode.
Input high voltage(V_{IH})=V_{CC}-0.2V, Input low voltage(V_{IL})=0.2V, UCAS,LCAS=0.2V,
DQ=Don't care, t_{RC}=31.25us, t_{RAS}=t_{RAS}min~300ns
I_{CCS} : Self Refresh Current, $\overline{RAS}$=UCAS=LCAS=V_{IL}, W=OE=A0~A11=V_{CC}-0.2V or 0.2V, DQ~DQ63=V_{CC}-0.2V or Open
$I_{(IL)}$: Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.3V, all other pins not under test=0 V)
$I_{(OL)}$: Output Leakage Current(Data Out is disabled, 0V≤V_{OUT}≤V_{CC})
V_{OH} : Output High Voltage Level (I_{OH} = -2mA)
V_{OL} : Output Low Voltage Level (I_{OL} = 2mA)

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one EDO mode cycle time, t_{HPC}.

CAPACITANCE (T_A = 25°C, V_{CC}=3.3V, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0-A11]	C_{IN1}	-	50	pF
Input capacitance[W, OE]	C_{IN2}	-	66	pF
Input capacitance[RAS0, RAS1]	C_{IN3}	-	38	pF
Input capacitance[CAS0 - CAS7]	C_{IN4}	-	24	pF
Input/Output capacitance[DQ0 - 63]	C_{DQ}	-	24	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC}=3.3V±0.3V. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.2/0.7V, V_{oh}/V_{ol}=2.0/0.8V, output loading CL=100pF

Parameter	Symbol	-50		-60		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	84		104		ns	
Read-modify-write cycle time	t_{RWC}	128		153		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	3,4,9
Access time from $\overline{CAS}$	t_{CAC}		13		15	ns	3,4,5
Access time from column address	t_{AA}		25		30	ns	3,9
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	3		3		ns	3
$\overline{OE}$ to output in Low-Z	t_{OLZ}	3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	t_{CEZ}	3	13	3	13	ns	3,11
Transition time(rise and fall)	t_T	1	50	1	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	8		10		ns	
$\overline{CAS}$ hold time	t_{CSH}	38		40		ns	
$\overline{CAS}$ pulse width	t_{CAS}	8	10K	10	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	17	37	20	45	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	12	25	15	30	ns	9
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		ns	
Row address set-up time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	7		10		ns	
Column address set-up time	t_{ASC}	0		0		ns	12
Column address hold time	t_{CAH}	7		10		ns	12
Column address to $\overline{RAS}$ lead time	t_{RAL}	25		30		ns	
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	7
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		ns	7
Write command set-up time	t_{WCS}	0		0		ns	6
Write command hold time	t_{WCH}	7		10		ns	6
Write command pulse width	t_{WP}	7		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	8		10		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	7		10		ns	15
Data set-up time	t_{DS}	0		0		ns	8,18
Data hold time	t_{DH}	7		10		ns	8,18
Refresh period	t_{REF}		128		128	ms	
$\overline{CAS}$ to $\overline{W}$ dealy time	t_{CWD}	33		38		ns	6,14
$\overline{RAS}$ to $\overline{W}$ dealy time	t_{RWD}	70		84		ns	6

AC CHARACTERISTICS (0°C≤TA≤70°C, VCC=3.3V±0.3V. See notes 1,2.)

Test condition : Vih/Vil=2.2/0.7V, Voh/Vol=2.0/0.8V, output loading CL=100pF

Parameter	Symbol	-50		-60		Unit	Note
		Min	Max	Min	Max		
Column address to $\overline{W}$ delay time	t_{AWD}	45		53		ns	6
$\overline{CAS}$ precharge to $\overline{W}$ delay time	t_{CPWD}	47		58		ns	6
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	5		5		ns	16
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		ns	17
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		28		35	ns	3
Hyper page mode cycle time	t_{HPC}	20		25		ns	10
Hyper page mode read-modify write cycle time	t_{HPRWC}	67		73		ns	10
$\overline{CAS}$ precharge time (Hyper page cycle)	t_{CP}	7		10		ns	13
$\overline{RAS}$ pulse width (Hyper page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	30		35		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time (C-B-R refresh)	t_{WRP}	10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time (C-B-R refresh)	t_{WRH}	10		10		ns	
$\overline{OE}$ access time	t_{OEA}		13		15	ns	3
$\overline{OE}$ to data delay	t_{OED}	10		13		ns	
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	3	13	3	13	ns	
$\overline{OE}$ command hold time	t_{OEH}	5		5		ns	
Output data hold time	t_{DOH}	5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	t_{REZ}	3	13	3	15	ns	11
Output buffer turn off delay from $\overline{W}$	t_{WEZ}	3	13	3	15	ns	
$\overline{W}$ to data delay	t_{WED}	15		15		ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	t_{OCH}	5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	t_{CHO}	5		5		ns	
$\overline{OE}$ precharge time	t_{OEP}	5		5		ns	
$\overline{W}$ pulse width(Hyper page cycle)	t_{WPE}	5		5		ns	
$\overline{RAS}$ pulse width (C-B-R self refresh)	t_{RASS}	100		100		us	19,20,21
$\overline{RAS}$ precharge time (C-B-R self refresh)	t_{RPS}	90		110		ns	19,20,21
$\overline{CAS}$ hold time (C-B-R self refresh)	t_{CHS}	-50		-50		ns	19,20,21

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. Input voltage levels are V_{ih}/V_{il}. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 1 TTL loads and 100pF.

4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

5. Assumes that $t_{RCD} \geq t_{RCD}$(max).

6. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are non-restrictive operating parameter. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{RWD} \geq t_{RWD}$(min), $t_{CWD} \geq t_{CWD}$(min), $t_{AWD} \geq t_{AWD}$(min) and $t_{CPWD} \geq t_{CPWD}$(min). The cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of data out(at access time) is indeterminate.

7. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

8. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles.

9. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit access time is controlled by t_{AA}.

10. $t_{ASC} \geq 6$ns, Assume tT=2.0ns

11. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high before $\overline{RAS}$ high going , the open circuit condition of the output is achieved by $\overline{RAS}$ going.

12. t_{ASC} is referenced to the earlier $\overline{CAS}$ falling edge and t_{CAH} is referenced to the later $\overline{CAS}$ falling edge.

13. t_{CP} is specified from the last $\overline{CAS}$ rising edge in the previous cycle to the first $\overline{CAS}$ falling edge in the next cycle.

14. t_{CWD} is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.

15. t_{CWL} is specified from $\overline{W}$ falling edge to the earlier $\overline{CAS}$ rising edge.

16. t_{CSR} is referenced to earlier $\overline{CAS}$ falling edge to the $\overline{RAS}$ falling edge.

17. t_{CHR} is referenced to the later $\overline{CAS}$ rising from $\overline{RAS}$ falling edge.

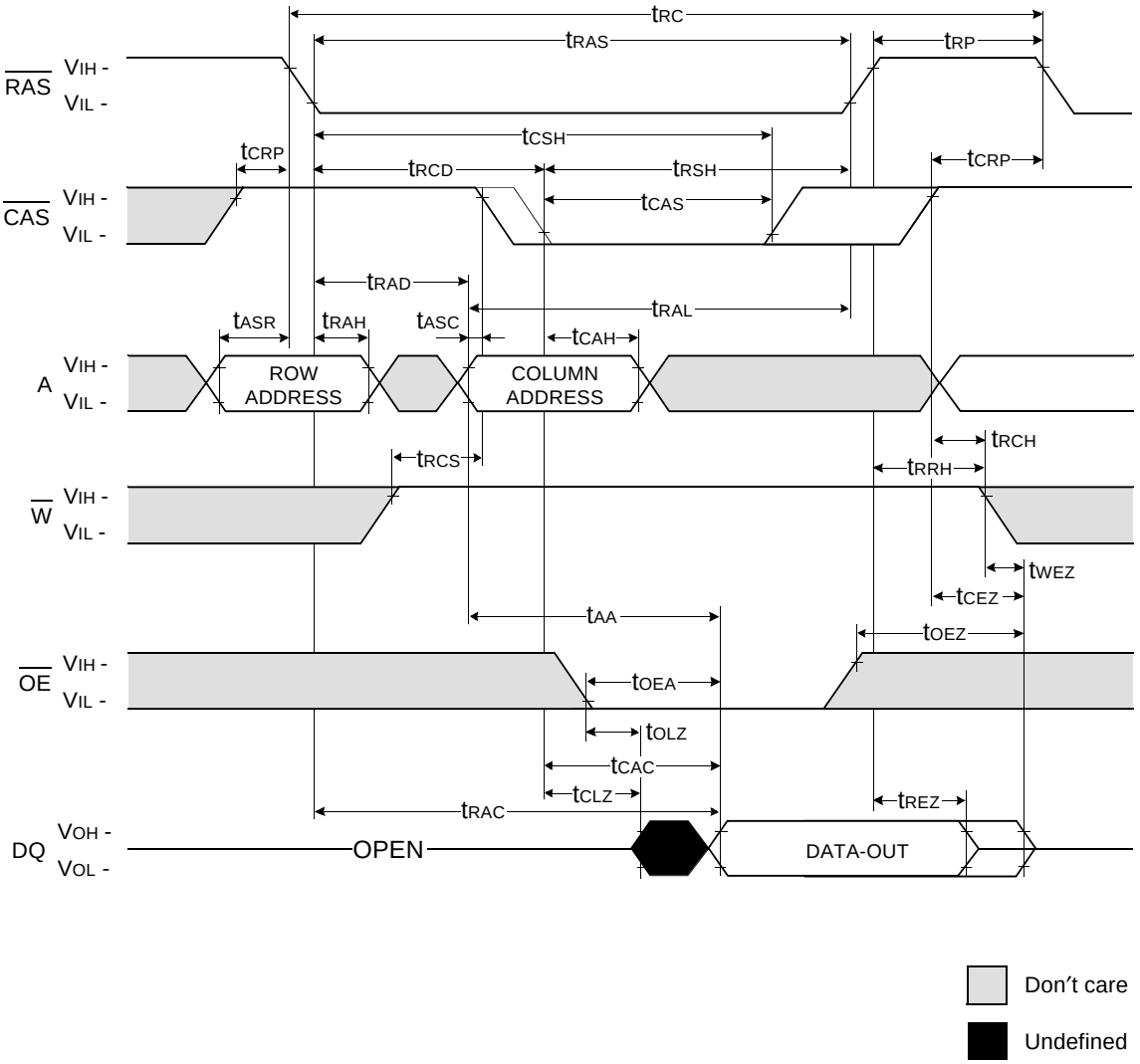
18. t_{DS}, t_{DH} is specified by the earlier $\overline{CAS}$ falling edge.

19. If $t_{RASS} \geq 100$us, then $\overline{RAS}$ precharge time must use t_{RPS} instead of t_{RP}.

20. For $\overline{RAS}$-only refresh and burst $\overline{CAS}$-before-$\overline{RAS}$ refresh mode, 4096 cycles of burst refresh must be executed within 64ms before and after self refresh, in order to meet refresh specification.

21. For distributed $\overline{CAS}$-before-$\overline{RAS}$ with 15.6us interval $\overline{CAS}$-before-$\overline{RAS}$ should be executed with in 15.6us immediately before and after self refresh in order to meet refresh specification.

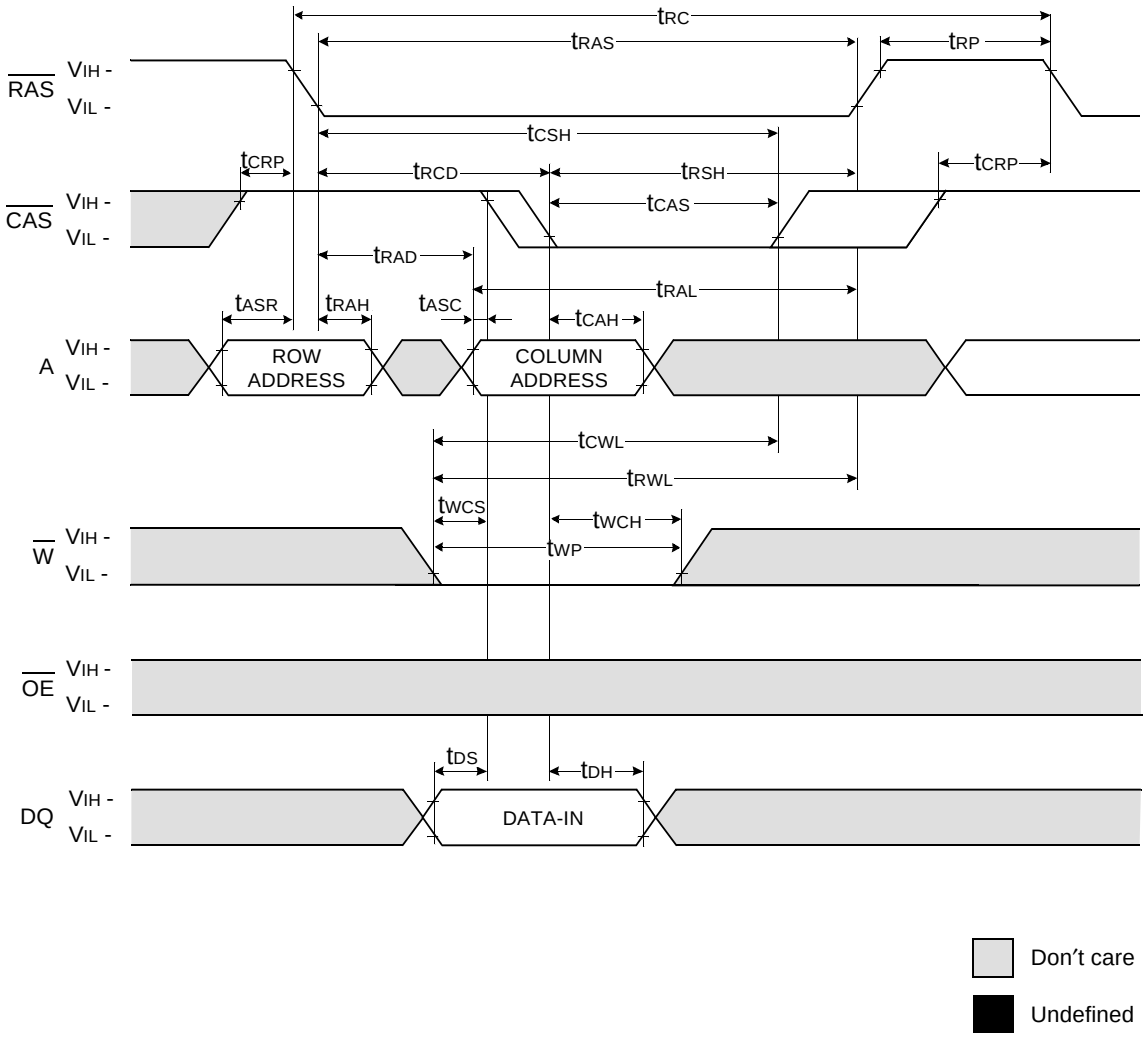
READ CYCLE



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WRITE CYCLE (EARLY WRITE)

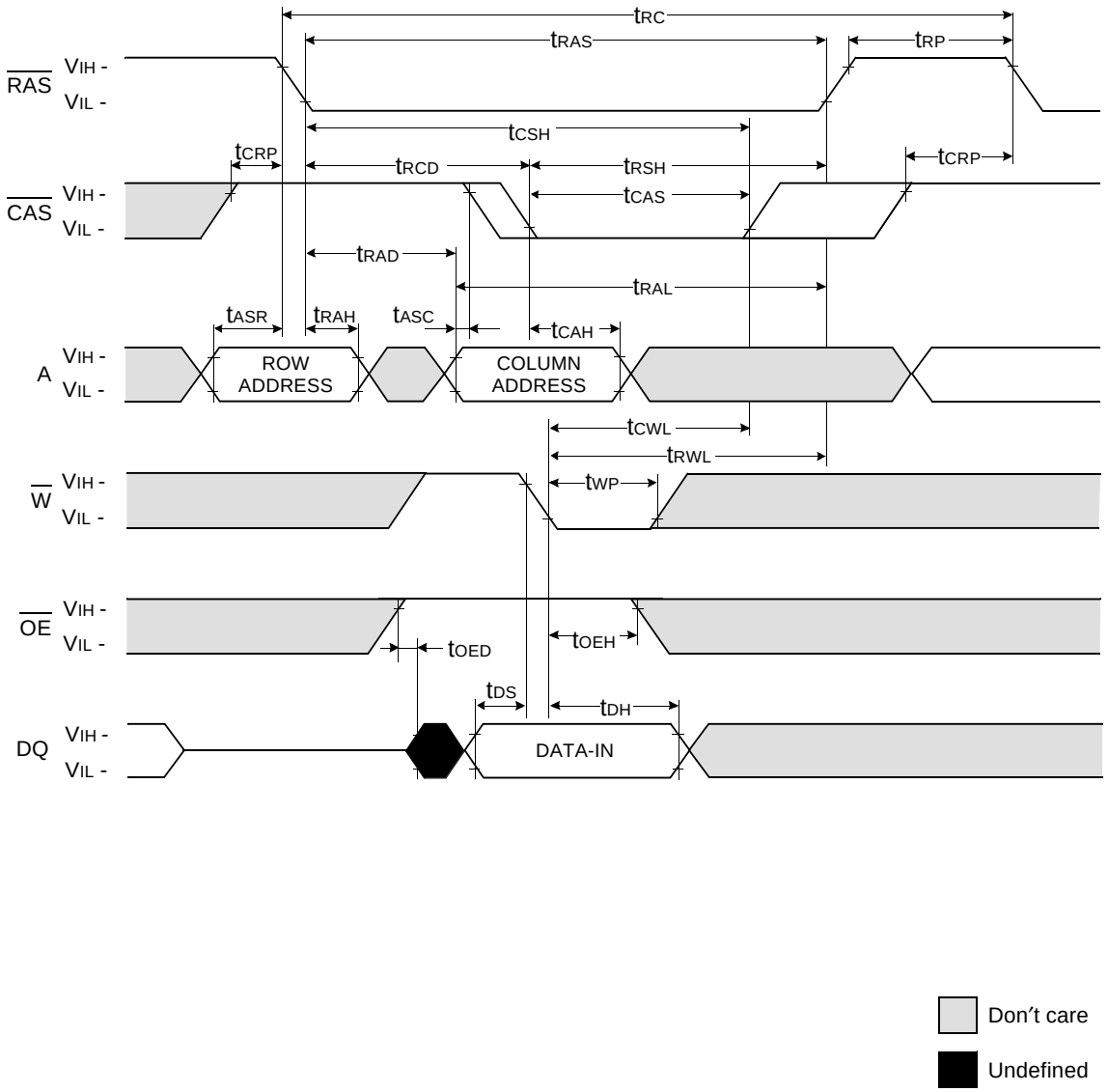
NOTE : DOUT = OPEN



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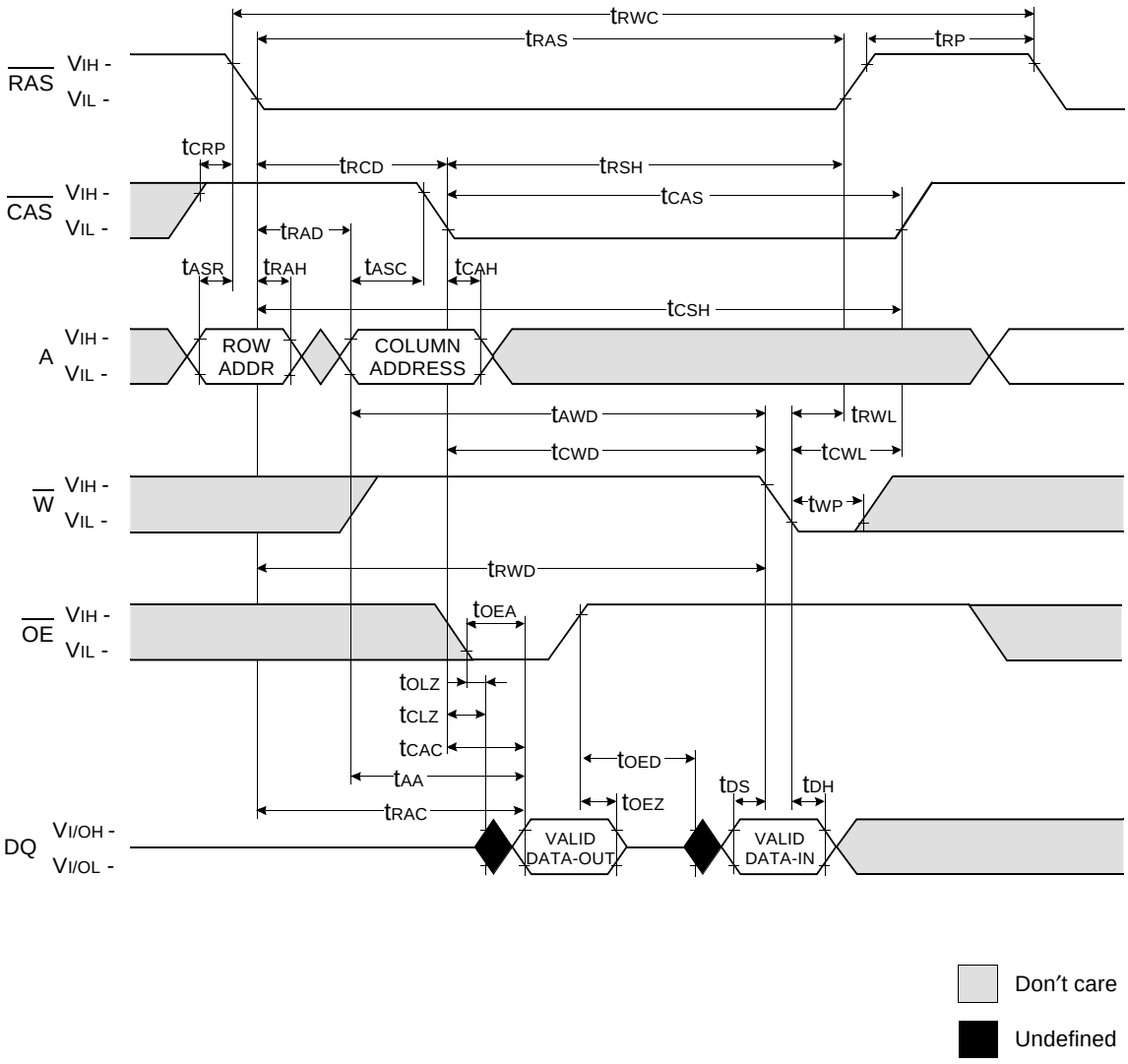
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

NOTE : DOUT = OPEN



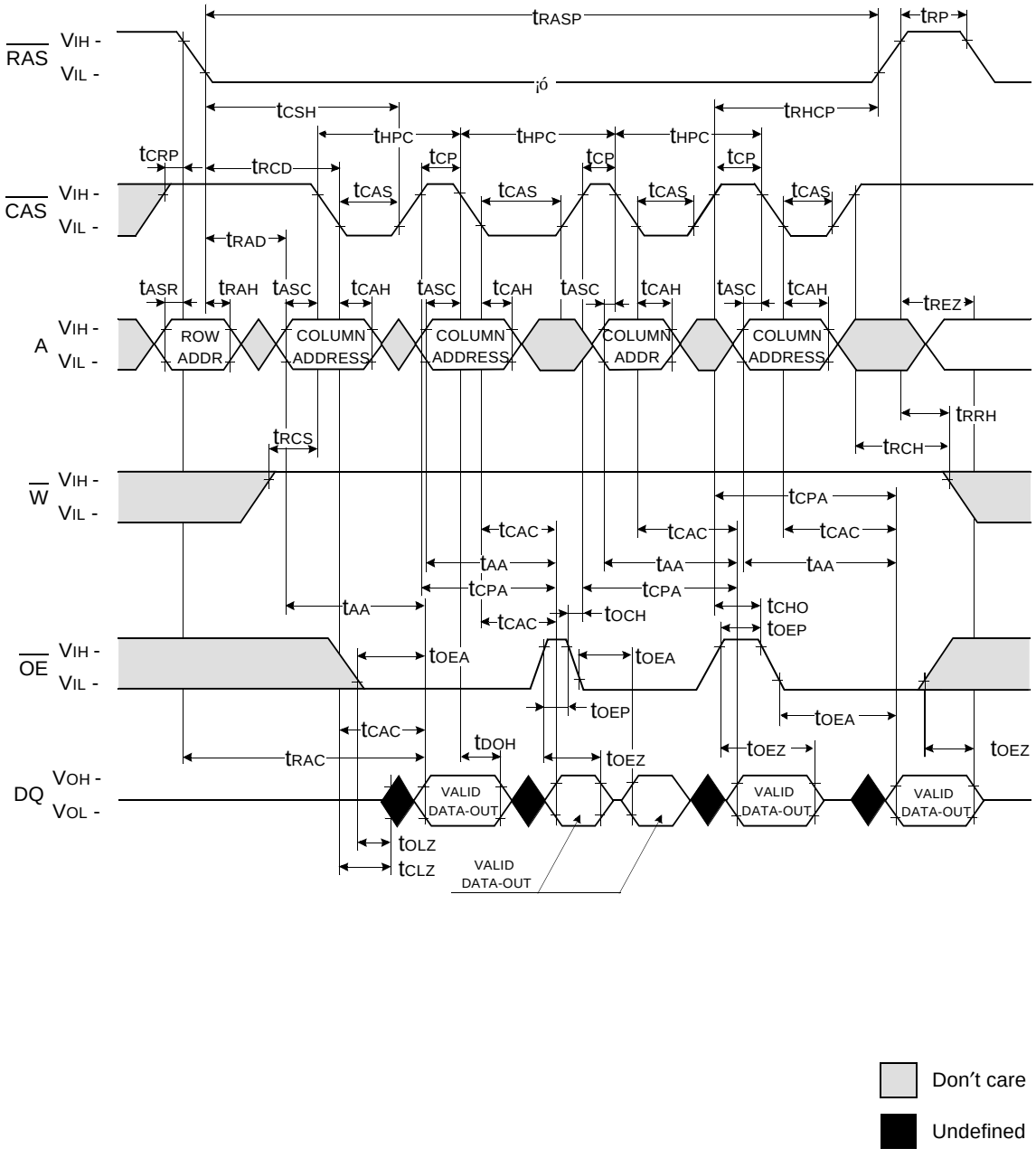
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READ - MODIFY - WRITE CYCLE



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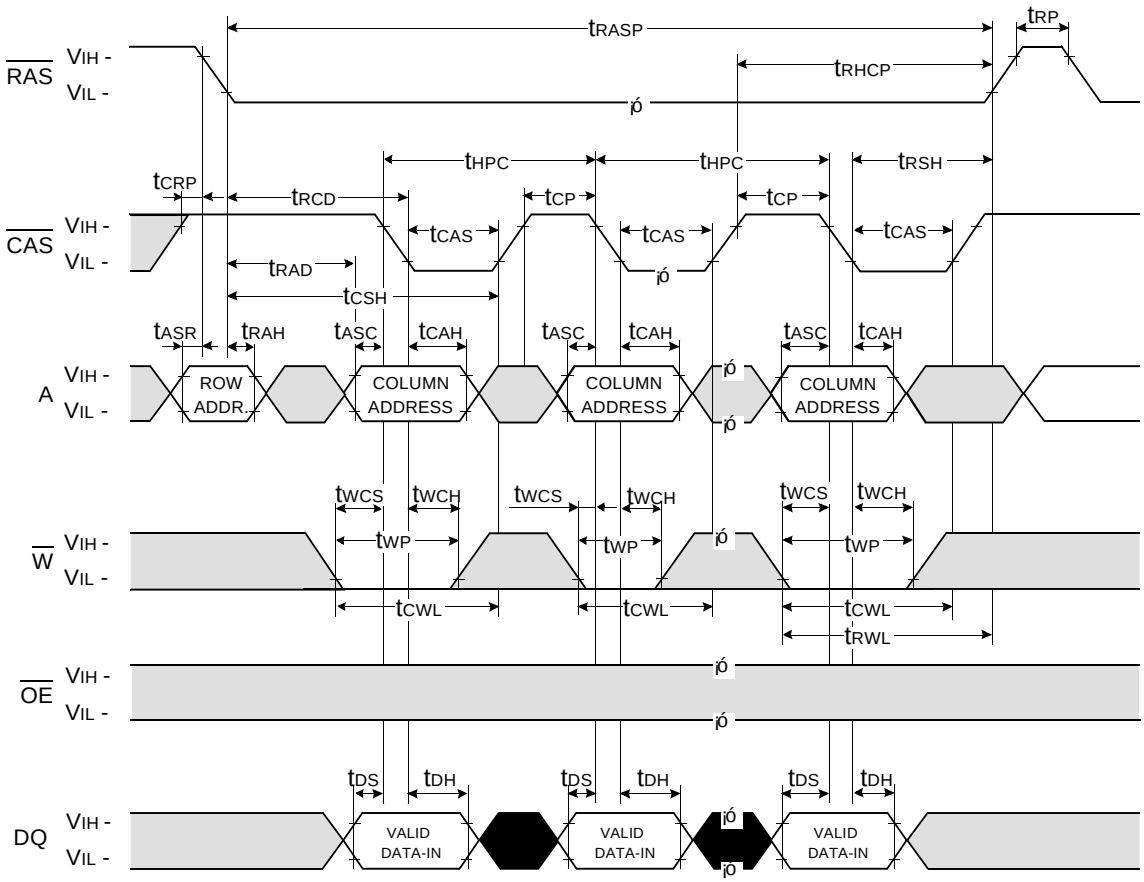
HYPER PAGE READ CYCLE



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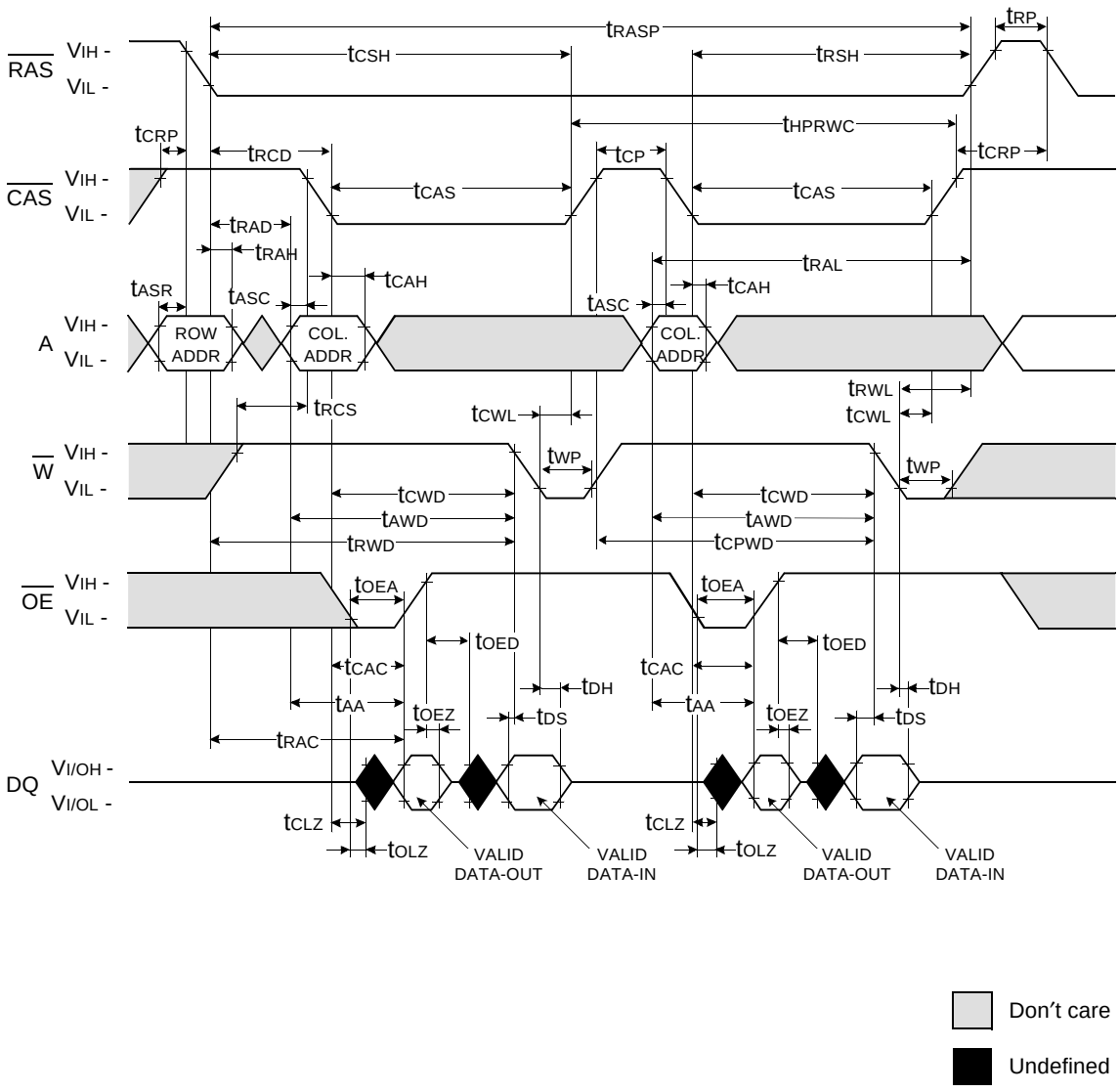
HYPER PAGE WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN



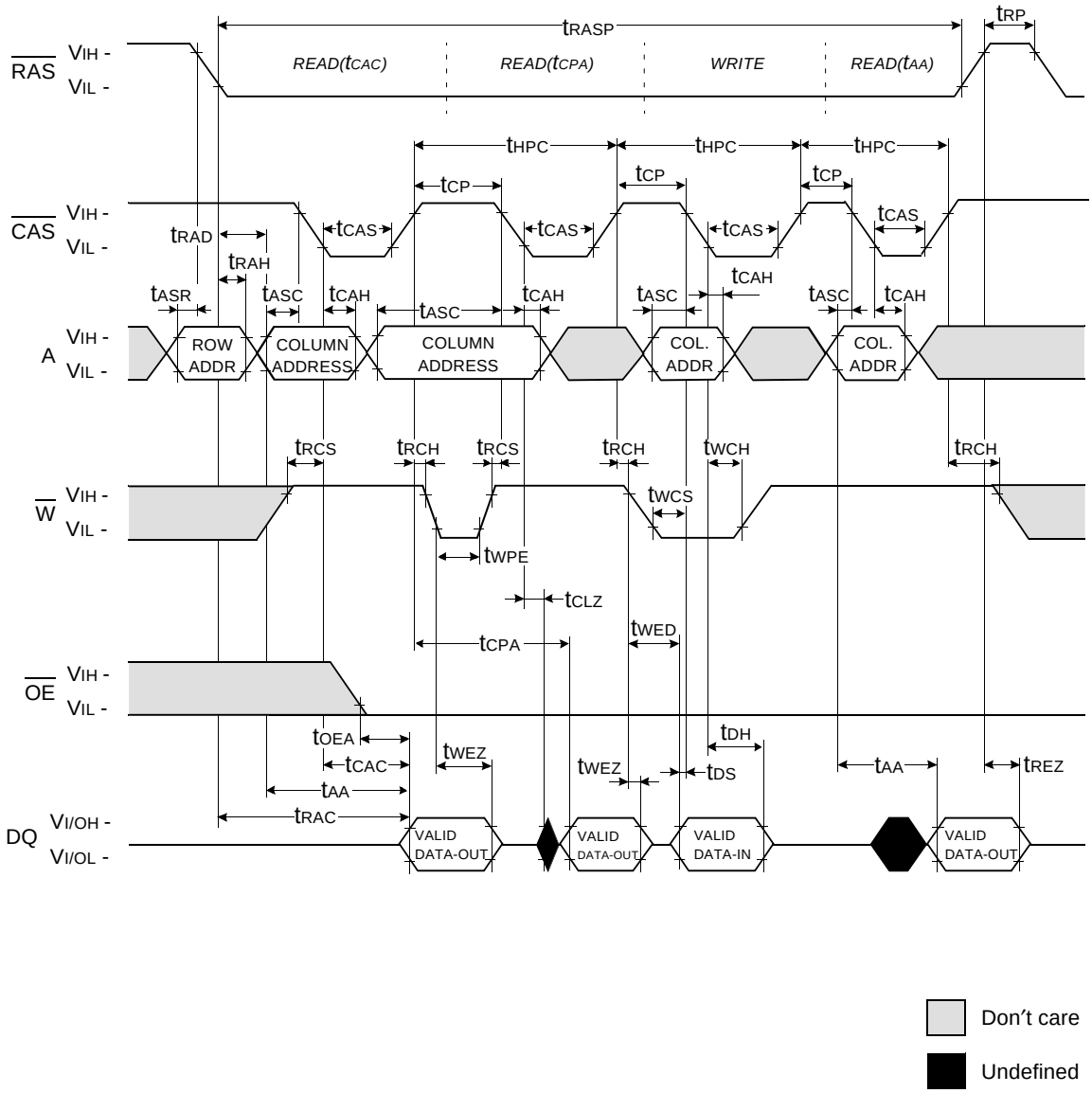
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HYPER PAGE READ-MODIFY-WRITE CYCLE



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HYPER PAGE READ AND WRITE MIXED CYCLE

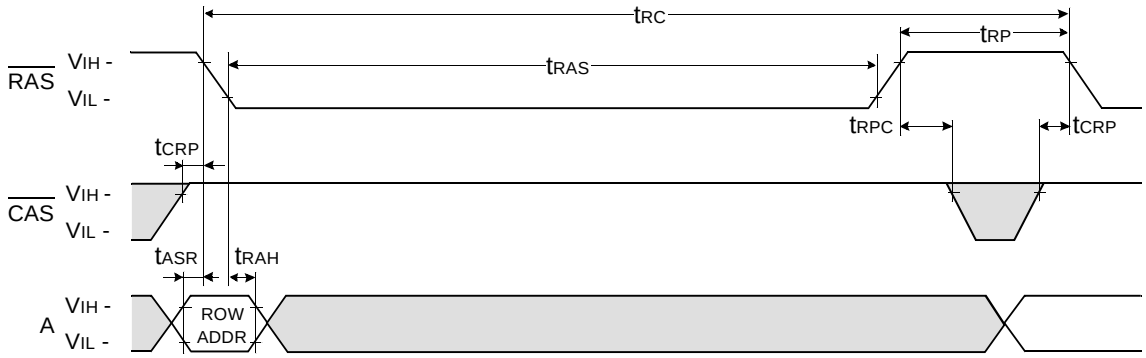


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$\overline{RAS}$ - ONLY REFRESH CYCLE*

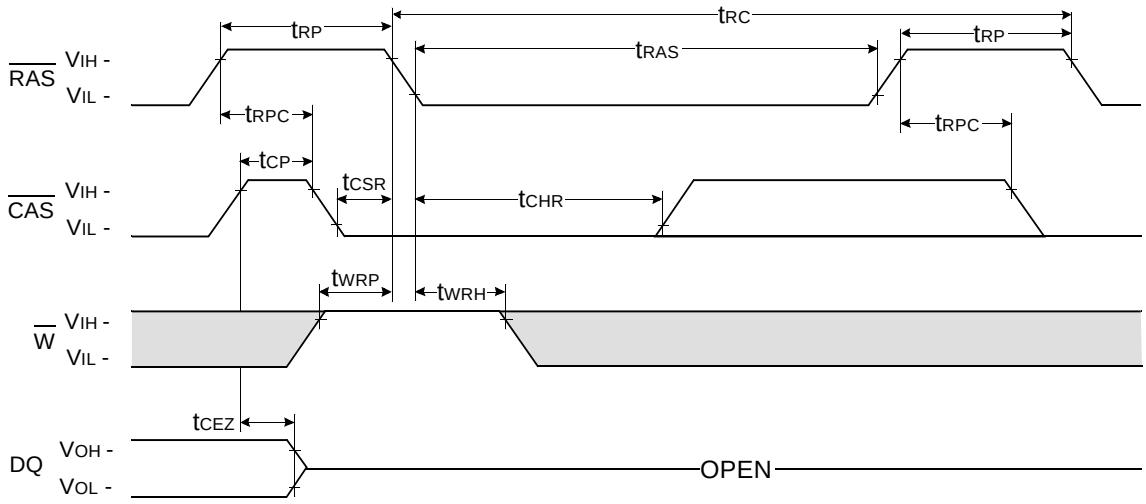
NOTE : $\overline{W}$, $\overline{OE}$, D_{IN} = Don't care

D_{OUT} = OPEN



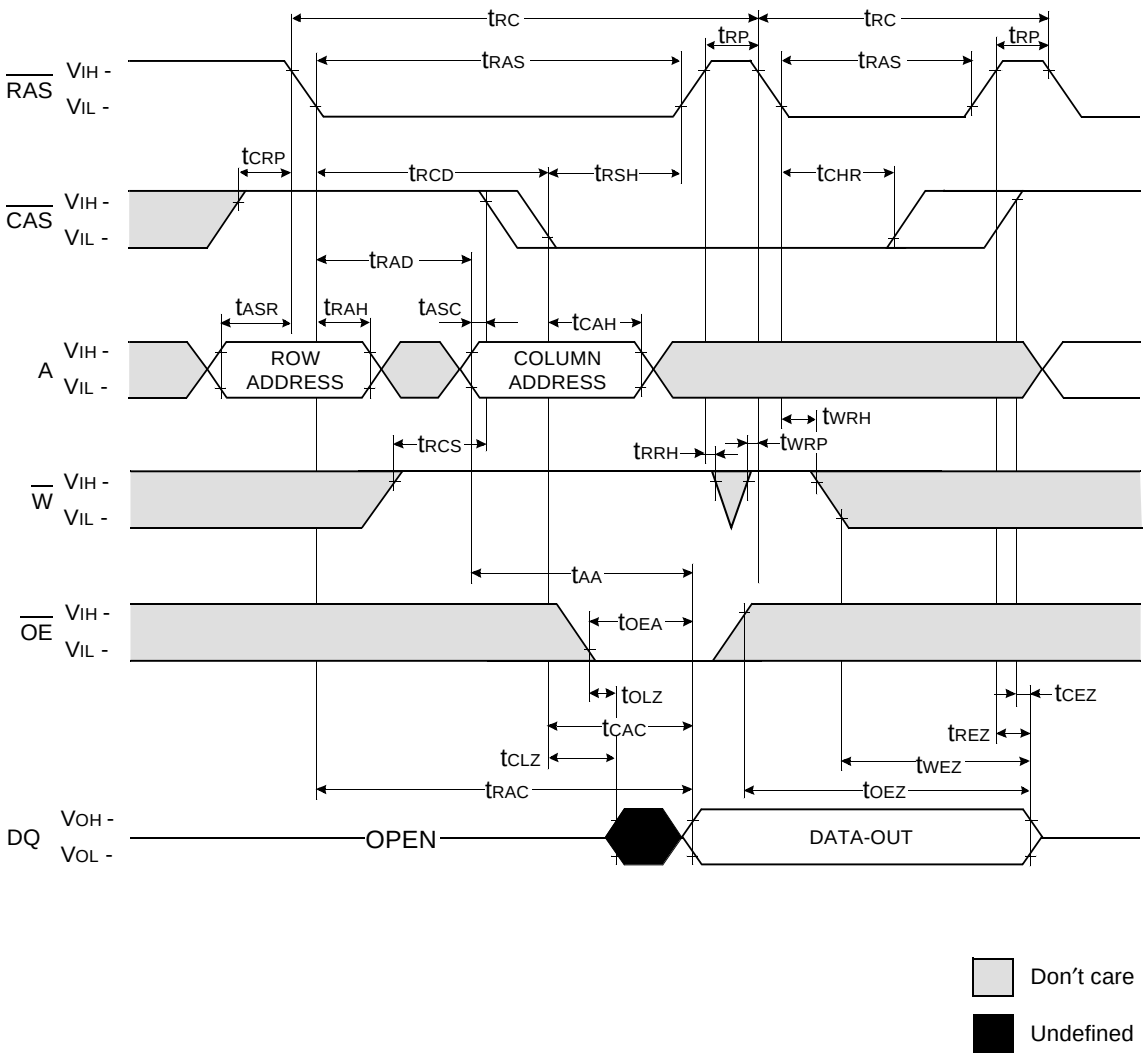
$\overline{CAS}$ - BEFORE - $\overline{RAS}$ REFRESH CYCLE

NOTE : $\overline{OE}$, A = Don't care



* In $\overline{RAS}$-only refresh cycle of 64Mb A-dile & B-die, when $\overline{CAS}$ signal transits from Low to High, the valid data may be cut off.

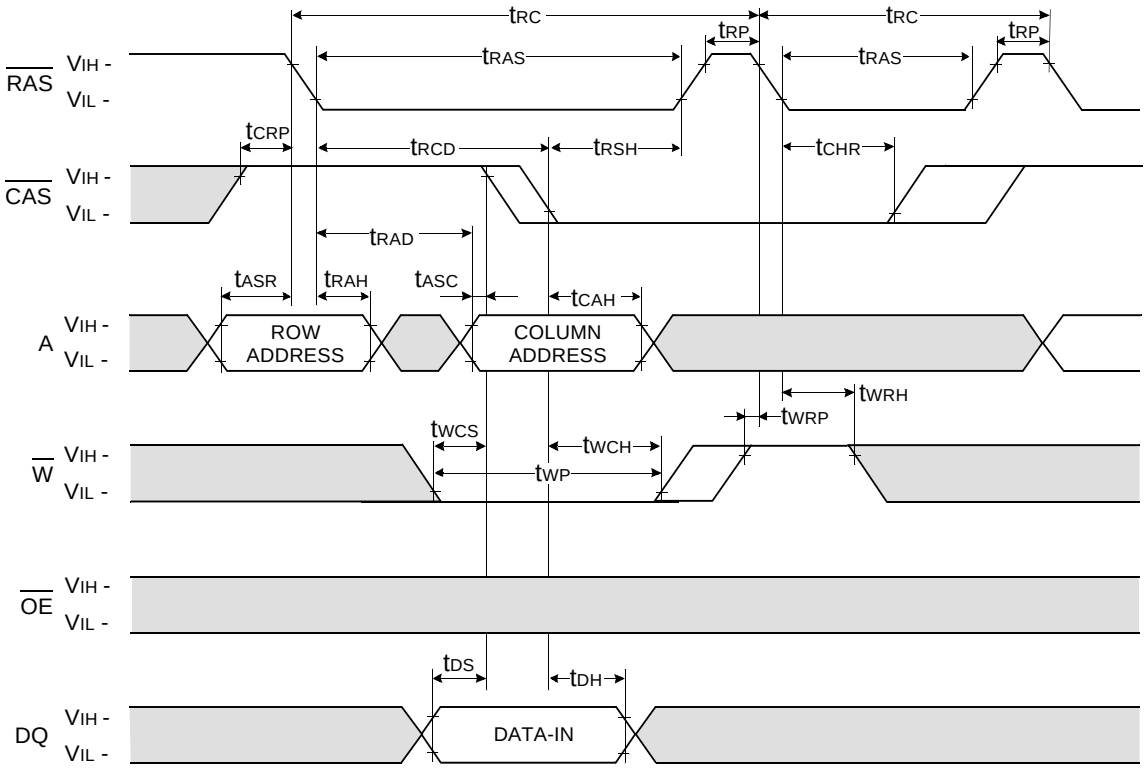
HIDDEN REFRESH CYCLE (READ)



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HIDDEN REFRESH CYCLE (WRITE)

NOTE : DOUT = OPEN

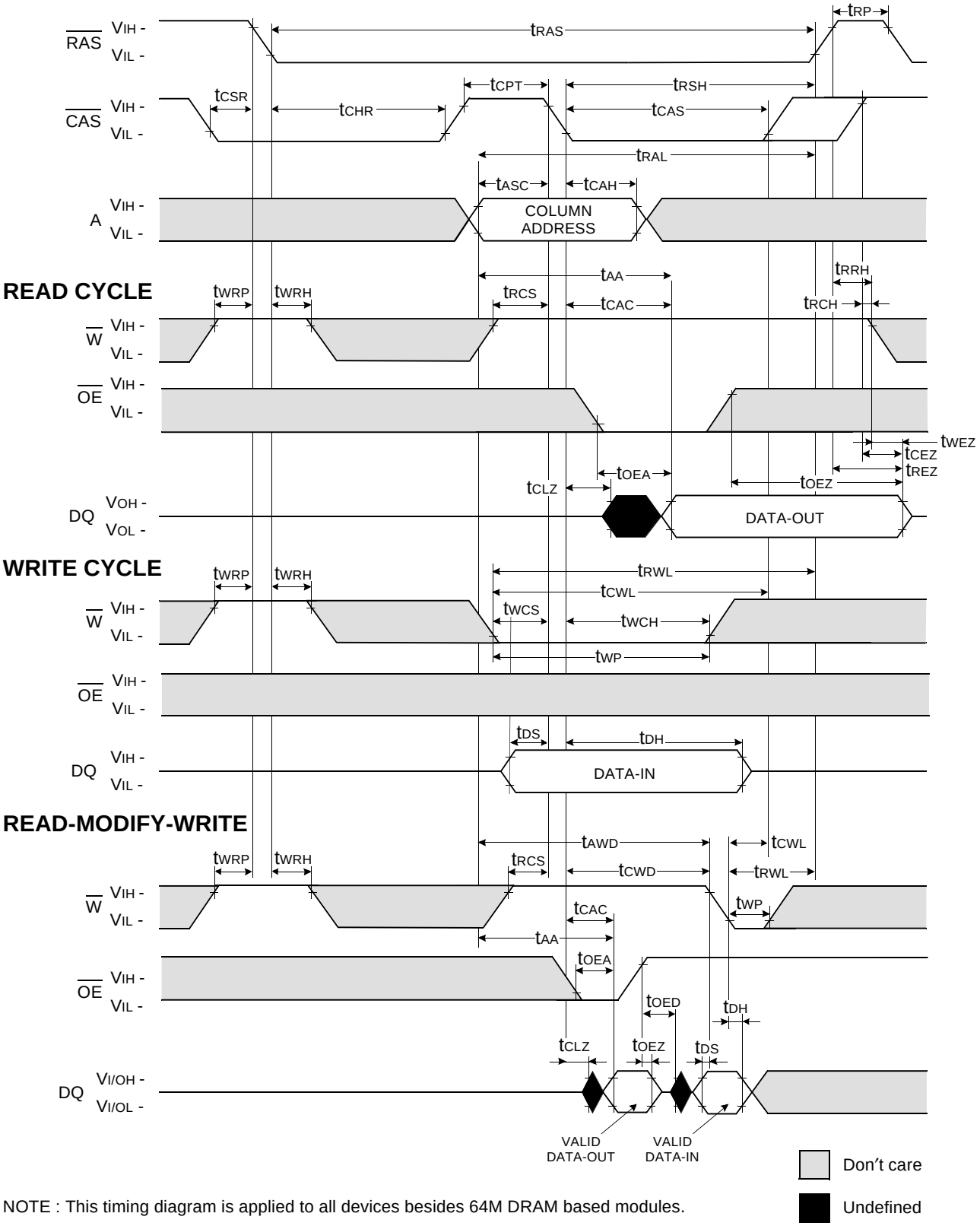


Don't care

Undefined

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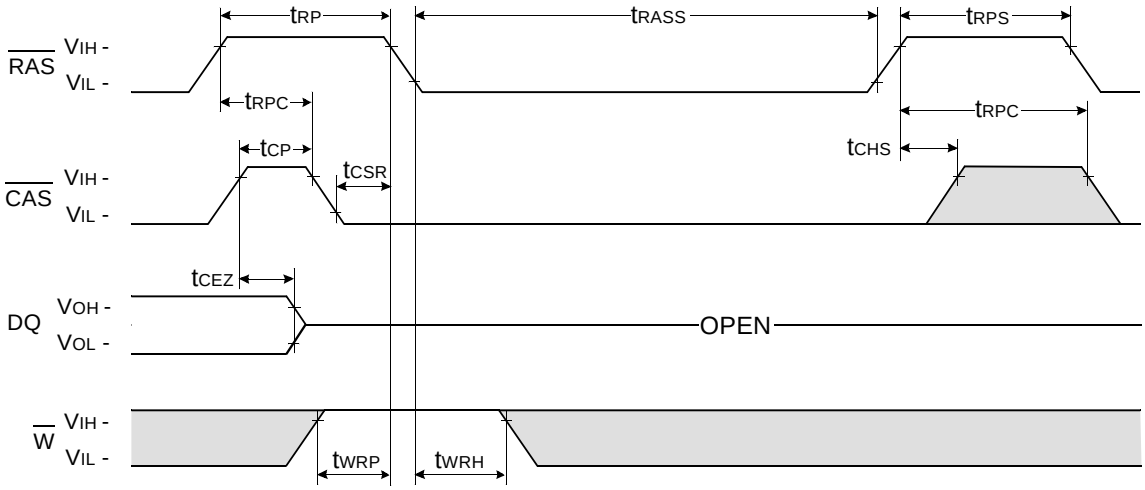
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



NOTE : This timing diagram is applied to all devices besides 64M DRAM based modules.

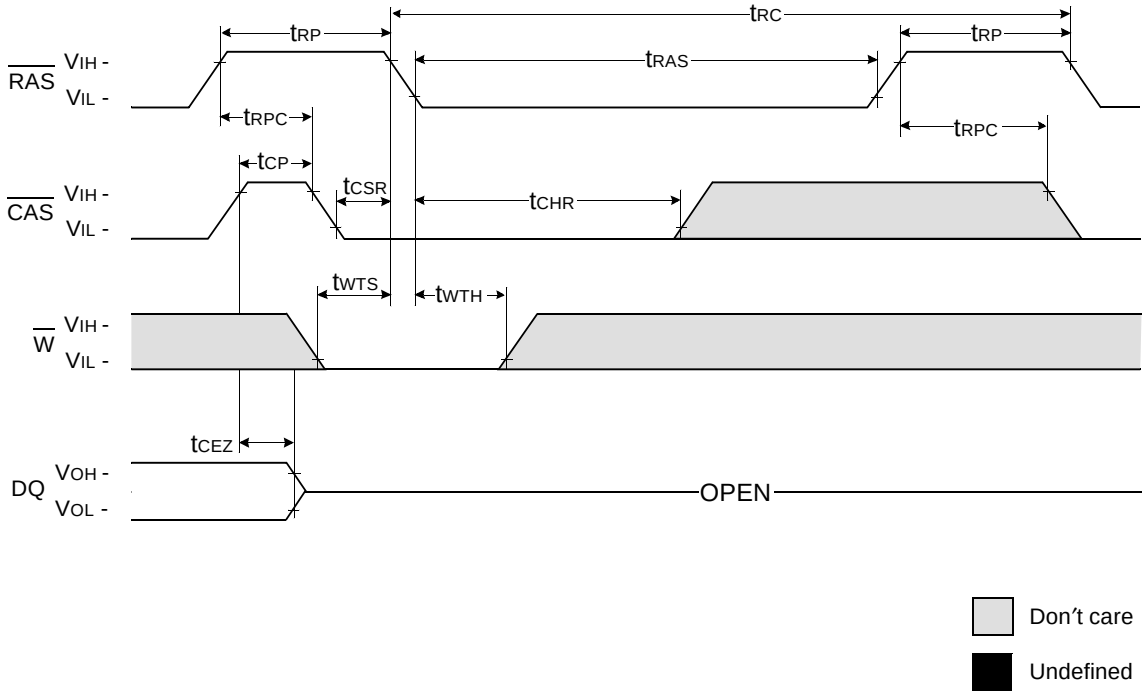
$\overline{CAS}$ - BEFORE - $\overline{RAS}$ SELF REFRESH CYCLE

NOTE : $\overline{OE}$, A = Don't care



TEST MODE IN CYCLE

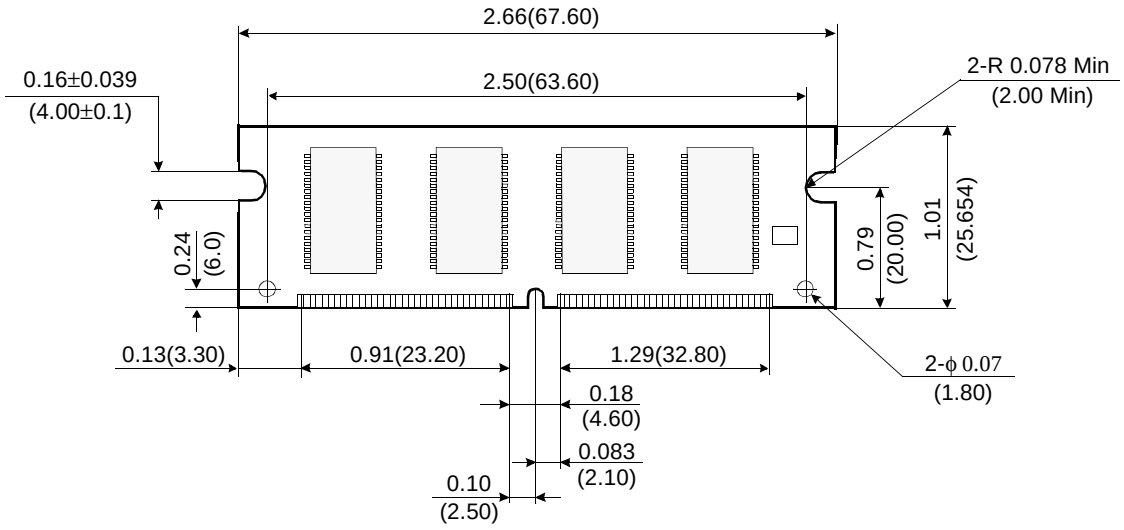
NOTE : $\overline{OE}$, A = Don't care



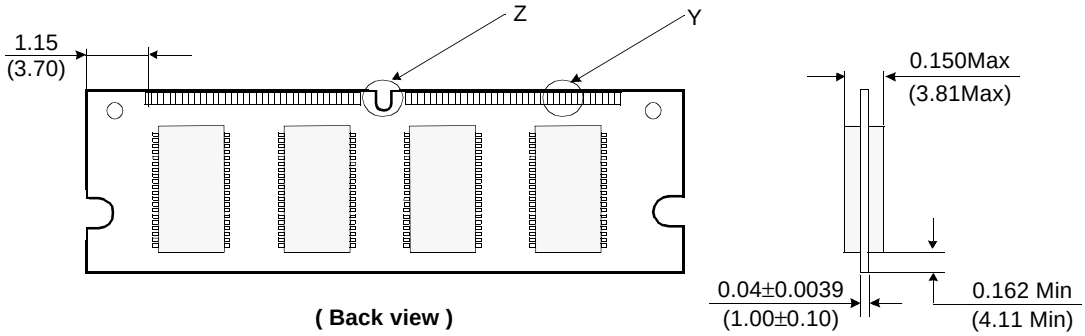
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PACKAGE DIMENSIONS

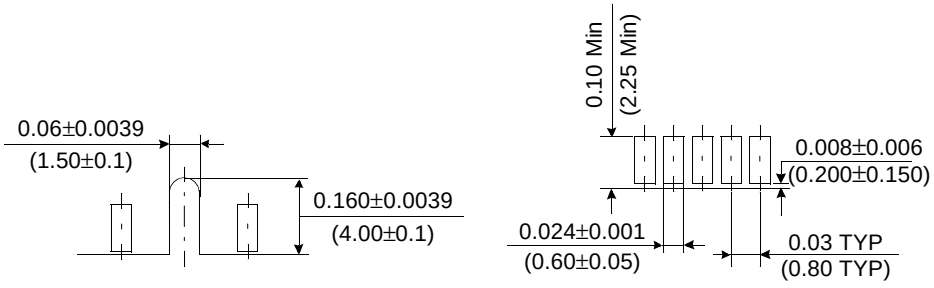
Units : Inches (millimeters)



(Front view)



(Back view)



Detail Z **Detail Y**

Tolerances : ±.005(.13) unless otherwise specified

The used device is 4Mx16 DRAM with EDO mode, TSOP II
DRAM Part No. : K4E641612D-T