19-1196; Rev 0; 2/97

MAXIM

Low-Power, 12-Bit Voltage-Output DACs with Serial Interface

General Description

The MAX5352/MAX5353 combine a low-power, voltage-output, 12-bit digital-to-analog converter (DAC) and a precision output amplifier in an 8-pin µMAX or DIP package. The MAX5352 operates from a single +5V supply, and the MAX5353 operates from a single +3.3V supply. Both devices draw less than 280µA of supply current.

The output amplifier's inverting input is available to the user, allowing specific gain configurations, remote sensing, and high output current capability. This makes the MAX5352/MAX5353 ideal for a wide range of applications, including industrial process control. Other features include a software shutdown and power-on reset.

The serial interface is compatible with SPI™/QSPI™ and Microwire™. The DAC has a double-buffered input, organized as an input register followed by a DAC register. A 16-bit serial word loads data into the input register. The DAC register can be updated independently or simultaneously with the input register. All logic inputs are TTL/CMOS-logic compatible and buffered with Schmitt triggers to allow direct interfacing to optocouplers.

Applications

Industrial Process Controls

Automatic Test Equipment

Digital Offset and Gain Adjustment

Motion Control

Remote Industrial Controls

Microprocessor-Controlled Systems

Features

- **12-Bit DAC with Configurable Output Amplifier**
- **+5V Single-Supply Operation (MAX5352)**
  +3.3V Single-Supply Operation (MAX5353)
- **Low Supply Current: 0.28mA Normal Operation**
  2µA Shutdown Mode
- **Available in 8-Pin µMAX**
- **Power-On Reset Clears DAC Output to Zero**
- **SPI/QSPI and Microwire Compatible**
- **Schmitt-Trigger Digital Inputs for Direct Optocoupler Interface**
- **+3.3V MAX5353 Directly Interfaces with +5V Logic**

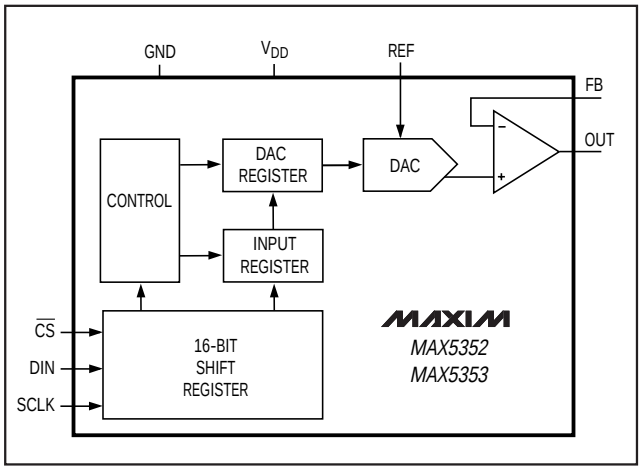
Ordering Information

PART*	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX5352ACPA	0°C to +70°C	8 Plastic DIP	±1/2
MAX5352BCPA	0°C to +70°C	8 Plastic DIP	±1
MAX5352ACUA	0°C to +70°C	8 µMAX	±1/2
MAX5352BCUA	0°C to +70°C	8 µMAX	±1

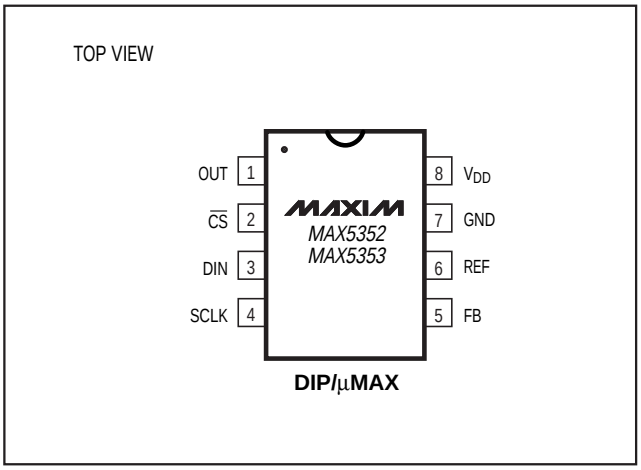
Ordering Information continued at end of data sheet.

**Contact factory for availability of 8-pin SO package.*

Functional Diagram



Pin Configuration



DIP/µMAX

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For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .....-0.3V, +6V
REF, OUT, FB to GND .....-0.3V to (V_{DD} + 0.3V)
Digital Inputs to GND .....-0.3V to +6V
Continuous Current into Any Pin.....±20mA
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
µMAX (derate 4.10mW/°C above +70°C) 330mW
CERDIP (derate 8.00mW/°C above +70°C).....640mW

Operating Temperature Ranges
MAX5352_C_A/MAX5353_C_A.....0°C to +70°C
MAX5352_E_A/MAX5353_E_A .....-40°C to +85°C
MAX5352BMJA/MAX5353BMJA .....-55°C to +125°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: MAX5352

(V_{DD} = +5V ±10%, REF = 2.5V, GND = 0V, R_L = 5kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C. Output buffer connected in unity-gain configuration (Figure 8).)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE—ANALOG SECTION						
Resolution	N		12			Bits
Integral Nonlinearity (Note 1)	INL	MAX5352A			±0.5	LSB
		MAX5352B			±1.0	
		MAX5352BMJA			±2.0	
Differential Nonlinearity	DNL	Guaranteed monotonic			±1.0	LSB
Offset Error	V_{OS}			±0.3	±8	mV
Offset-Error Tempco	TCV_{OS}			6		ppm/°C
Gain Error (Note 1)	GE			-0.3	±3	LSB
Gain-Error Tempco				1		ppm/°C
Power-Supply Rejection Ratio	PSRR	4.5V ≤ V_{DD} ≤ 5.5V			600	µV/V
REFERENCE INPUT						
Reference Input Range	V_{REF}		0		V_{DD} - 1.4	V
Reference Input Resistance	R_{REF}	Code dependent, minimum at code 1554 hex	14	20		kΩ
MULTIPLYING-MODE PERFORMANCE						
Reference -3dB Bandwidth		V_{REF} = 0.67Vp-p		650		kHz
Reference Feedthrough		Input code = all 0s, V_{REF} = 3.6Vp-p at 1kHz		-84		dB
Signal-to-Noise Plus Distortion Ratio	SINAD	V_{REF} = 1Vp-p at 25kHz, code = full scale		77		dB
DIGITAL INPUTS						
Input High Voltage	V_{IH}		2.4			V
Input Low Voltage	V_{IL}				0.8	V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{DD}		0.001	±0.5	µA
Input Capacitance	C_{IN}			8		pF

ELECTRICAL CHARACTERISTICS: MAX5352 (continued)

(V_{DD} = +5V ±10%, REF = 2.5V, GND = 0V, R_L = 5kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C. Output buffer connected in unity-gain configuration (Figure 8).)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE						
Voltage Output Slew Rate	SR			0.6		V/µs
Output Settling Time		To ±1/2LSB, V_{STEP} = 2.5V		14		µs
Output Voltage Swing		Rail-to-rail (Note 2)		0 to V_{DD}		V
Current into FB				0.001	±0.1	µA
Start-Up Time				20		µs
Digital Feedthrough		$\overline{CS}$ = V_{DD}, DIN = 100kHz		5		nV-s
POWER SUPPLIES						
Supply Voltage	V_{DD}		4.5		5.5	V
Supply Current	I_{DD}	(Note 3)		0.28	0.4	mA
Supply Current in Shutdown		(Note 3)		4	20	µA
Reference Current in Shutdown				0.001	±0.5	µA
TIMING CHARACTERISTICS (Figure 6)						
SCLK Clock Period	t_{CP}		100			ns
SCLK Pulse Width High	t_{CH}		40			ns
SCLK Pulse Width Low	t_{CL}		40			ns
$\overline{CS}$ Fall to SCLK Rise Setup Time	t_{CSS}		40			ns
SCLK Rise to $\overline{CS}$ Rise Hold Time	t_{CSH}		0			ns
DIN Setup Time	t_{DS}		40			ns
DIN Hold Time	t_{DH}		0			ns
SCLK Rise to $\overline{CS}$ Fall Delay	t_{CS0}		40			ns
$\overline{CS}$ Rise to SCLK Rise Hold Time	t_{CS1}		40			ns
$\overline{CS}$ Pulse Width High	t_{CSW}		100			ns

Note 1: Guaranteed from code 11 to code 4095 in unity-gain configuration.

Note 2: Accuracy is better than 1LSB for V_{OUT} = 8mV to V_{DD} - 100mV, guaranteed by a power-supply rejection test at the end points.

Note 3: R_L = ∞, digital inputs at GND or V_{DD}.

ELECTRICAL CHARACTERISTICS: MAX5353

(V_{DD} = +3.15V to +3.6V, REF = 1.25V, GND = 0V, R_L = 5kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C. Output buffer connected in unity-gain configuration (Figure 8).)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE—ANALOG SECTION						
Resolution	N		12			Bits
Integral Nonlinearity (Note 4)	INL	MAX5353A			±1	LSB
		MAX5353B			±2	
		MAX5353BMJA			±4	
Differential Nonlinearity	DNL	Guaranteed monotonic			±1.0	LSB
Offset Error	V_{OS}			±0.3	±8	mV
Offset-Error Tempco	TCV_{OS}			6		ppm/°C
Gain Error (Note 4)	GE			-0.3	±3	LSB
Gain-Error Tempco				1		ppm/°C
Power-Supply Rejection Ratio	PSRR				600	µV/V
REFERENCE INPUT						
Reference Input Range	V_{REF}		0		V_{DD} - 1.4	V
Reference Input Resistance	R_{REF}	Code dependent, minimum at code 1554 hex	14	20		kΩ
MULTIPLYING-MODE PERFORMANCE (V_{DD} = +3.3V)						
Reference -3dB Bandwidth		V_{REF} = 0.67Vp-p		650		kHz
Reference Feedthrough		Input code = all 0s, V_{REF} = 1.9Vp-p at 1kHz		-84		dB
Signal-to-Noise Plus Distortion Ratio	SINAD	V_{REF} = 1Vp-p at 25kHz, code = full scale		72		dB
DIGITAL INPUTS						
Input High Voltage	V_{IH}		2.4			V
Input Low Voltage	V_{IL}				0.6	V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{DD}		0.001	±0.5	µA
Input Capacitance	C_{IN}			8		pF
DYNAMIC PERFORMANCE						
Voltage Output Slew Rate	SR			0.6		V/µs
Output Settling Time		To ±1/2LSB, V_{STEP} = 1.25V		14		µs
Output Voltage Swing		Rail-to-rail (Note 5)		0 to V_{DD}		V
Current into FB				0.001	±0.1	µA
Start-Up Time				20		µs
Digital Feedthrough		$\overline{CS}$ = V_{DD}, DIN = 100kHz		5		nV-s
POWER SUPPLIES						
Supply Voltage	V_{DD}		3.15		3.6	V
Supply Current	I_{DD}	(Note 6)		0.24	0.4	mA
Supply Current in Shutdown		(Note 6)		1.6	10	µA
Reference Current in Shutdown				0.001	±0.5	µA

ELECTRICAL CHARACTERISTICS: MAX5353 (continued)

(V_{DD} = +3.15V to +3.6V, REF = 1.25V, GND = 0V, R_L = 5kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C. Output buffer connected in unity-gain configuration (Figure 8).)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TIMING CHARACTERISTICS (Figure 6)						
SCLK Clock Period	t_{CP}		100			ns
SCLK Pulse Width High	t_{CH}		40			ns
SCLK Pulse Width Low	t_{CL}		40			ns
$\overline{CS}$ Fall to SCLK Rise Setup Time	t_{CSS}		40			ns
SCLK Rise to $\overline{CS}$ Rise Hold Time	t_{CSH}		0			ns
DIN Setup Time	t_{DS}		40			ns
DIN Hold Time	t_{DH}		0			ns
SCLK Rise to $\overline{CS}$ Fall Delay	t_{CS0}		40			ns
$\overline{CS}$ Rise to SCLK Rise Hold Time	t_{CS1}		40			ns
$\overline{CS}$ Pulse Width High	t_{CSW}		100			ns

Note 4: Guaranteed from code 22 to code 4095 in unity-gain configuration.

Note 5: Accuracy is better than 1LSB for V_{OUT} = 8mV to V_{DD} - 150mV, guaranteed by a power-supply rejection test at the end points.

Note 6: R_L = ∞, digital inputs at GND or V_{DD}.

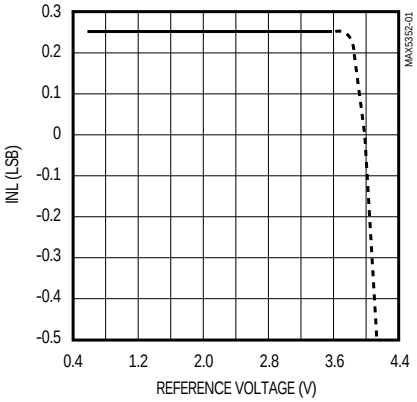
Low-Power, 12-Bit Voltage-Output DACs with Serial Interface

Typical Operating Characteristics

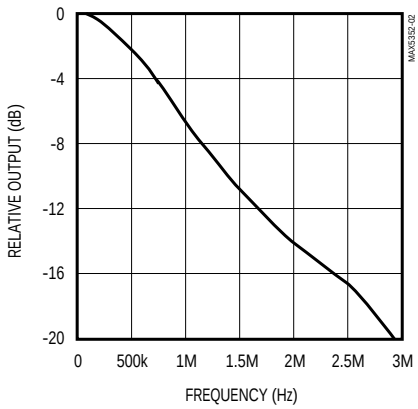
(MAX5352 only, V_{DD} = +5V, R_L = 5kΩ, C_L = 100pF, T_A = +25°C, unless otherwise noted.)

MAX5352

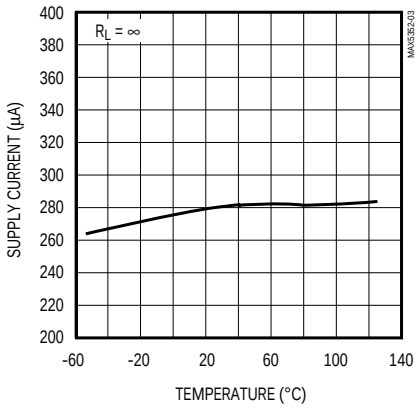
INTEGRAL NONLINEARITY vs. REFERENCE VOLTAGE



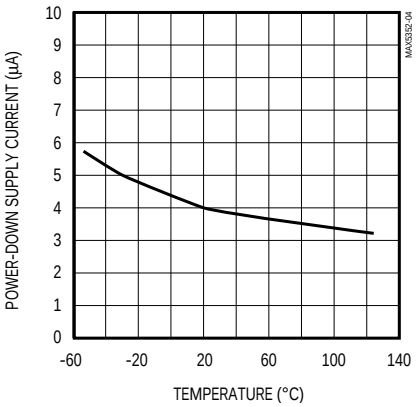
REFERENCE VOLTAGE INPUT FREQUENCY RESPONSE



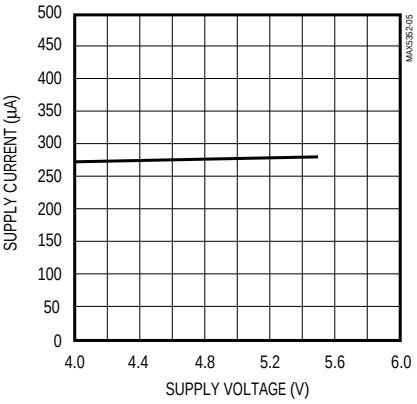
SUPPLY CURRENT vs. TEMPERATURE



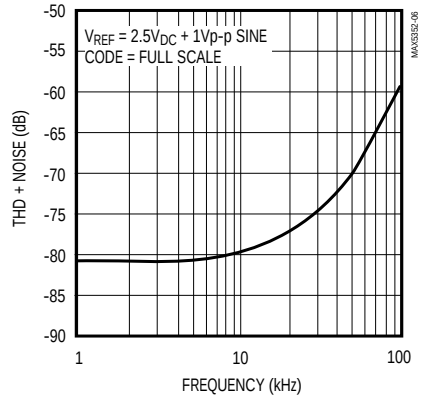
POWER-DOWN SUPPLY CURRENT vs. TEMPERATURE



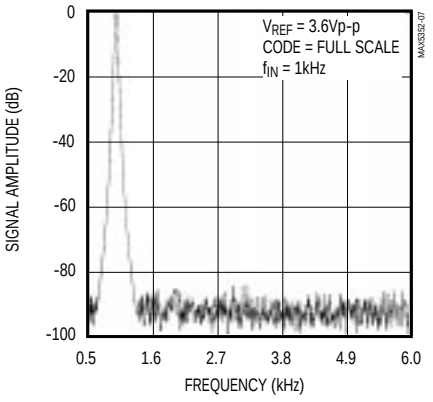
SUPPLY CURRENT vs. SUPPLY VOLTAGE



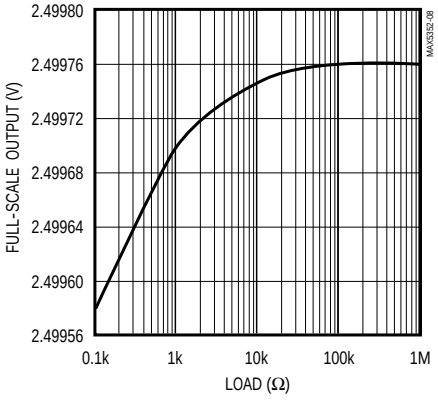
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



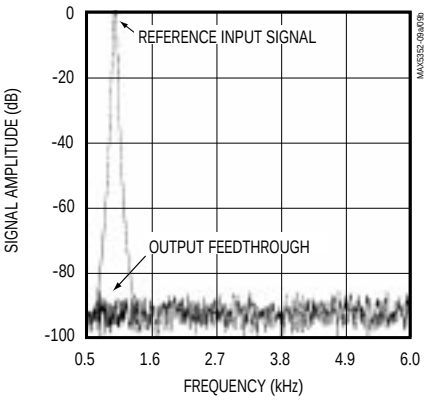
OUTPUT FFT PLOT



FULL-SCALE OUTPUT vs. LOAD



REFERENCE FEEDTHROUGH AT 1kHz

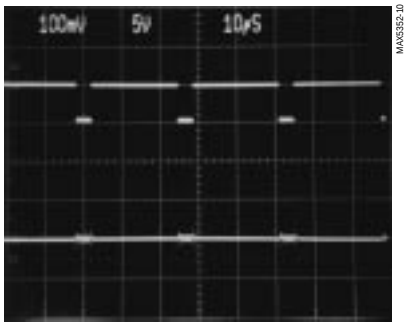


Typical Operating Characteristics (continued)

(MAX5352 only, V_{DD} = +5V, R_L = 5kΩ, C_L = 100pF, T_A = +25°C, unless otherwise noted.)

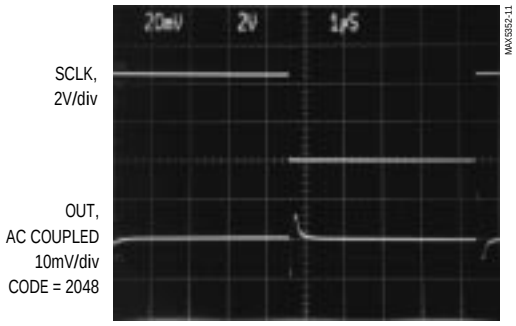
MAX5352 (continued)

MAJOR-CARRY TRANSITION



10µs/div

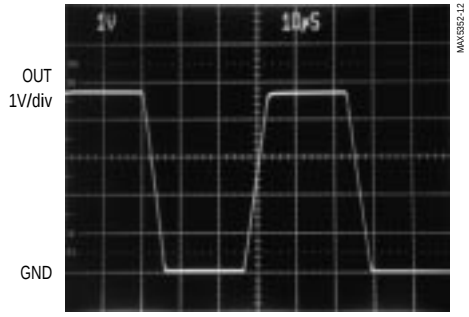
DIGITAL FEEDTHROUGH (f_{SCLK} = 100kHz)



2µs/div

$\overline{CS}$ = 5V

DYNAMIC RESPONSE



10µs/div

GAIN = 2, SWITCHING FROM CODE 0 TO 4020

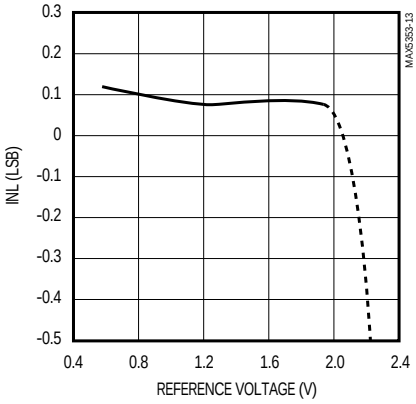
Low-Power, 12-Bit Voltage-Output DACs with Serial Interface

Typical Operating Characteristics (continued)

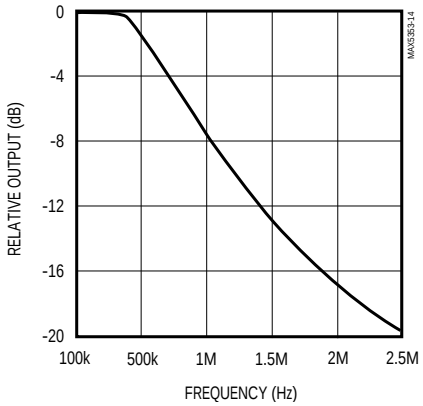
(MAX5353 only, V_{DD} = +3.3V, R_L = 5kΩ, C_L = 100pF, T_A = +25°C, unless otherwise noted.)

MAX5353

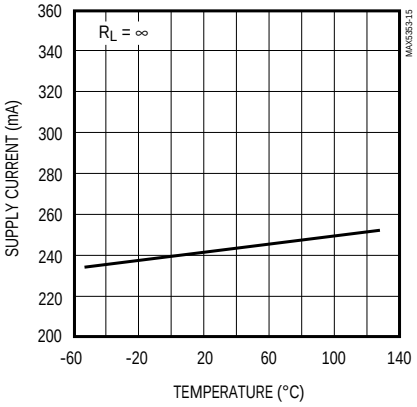
INTEGRAL NONLINEARITY vs. REFERENCE VOLTAGE



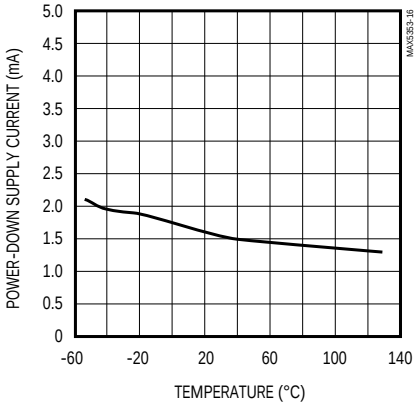
REFERENCE VOLTAGE INPUT FREQUENCY RESPONSE



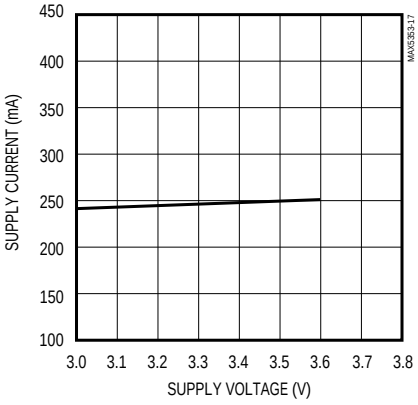
SUPPLY CURRENT vs. TEMPERATURE



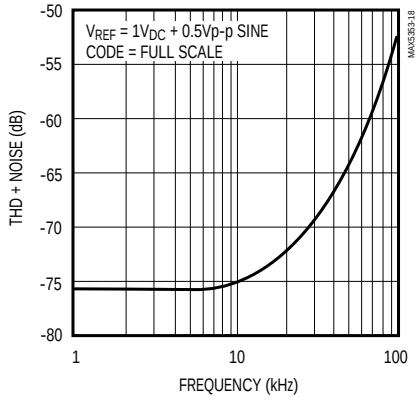
POWER-DOWN SUPPLY CURRENT vs. TEMPERATURE



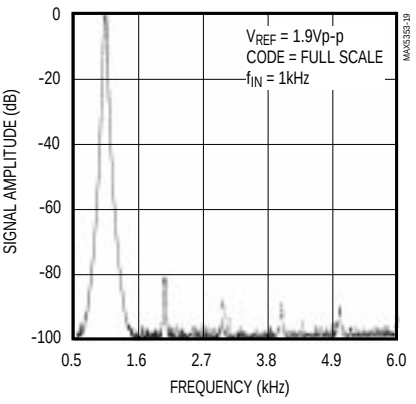
SUPPLY CURRENT vs. SUPPLY VOLTAGE



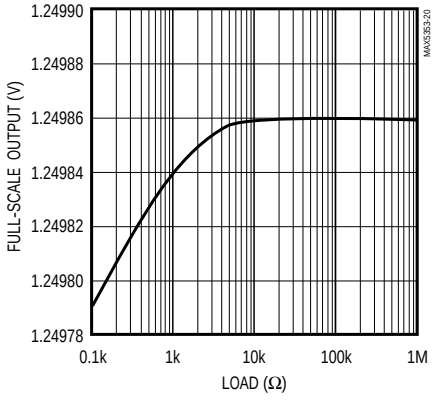
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



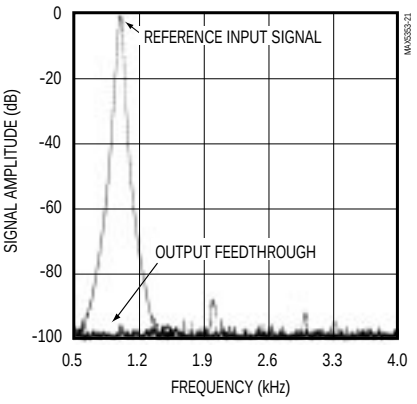
OUTPUT FFT PLOT



FULL-SCALE OUTPUT vs. LOAD



REFERENCE FEEDTHROUGH AT 1kHz



Pin Description

PIN	NAME	FUNCTION
1	OUT	DAC Output Voltage
2	$\overline{CS}$	Chip-Select Input. Active low.
3	DIN	Serial-Data Input
4	SCLK	Serial-Clock Input
5	FB	DAC Output Amplifier Feedback
6	REF	Reference Voltage Input
7	GND	Ground
8	V_{DD}	Positive Power Supply

Detailed Description

The MAX5352/MAX5353 contain a voltage-output digital-to-analog converter (DAC) that is easily addressed using a simple 3-wire serial interface. Each IC includes a 16-bit shift register, and has a double-buffered input composed of an input register and a DAC register (see *Functional Diagram*). In addition to the voltage output, the amplifier's negative input is available to the user.

The DAC is an inverted R-2R ladder network that converts a digital input (12 data bits plus one sub-bit) into an equivalent analog output voltage in proportion to the applied reference voltage. Figure 1 shows a simplified circuit diagram of the DAC.

Reference Inputs

The reference input accepts positive DC and AC signals. The voltage at the reference input sets the full-scale output voltage for the DAC. The reference input voltage range is 0V to (V_{DD} - 1.4V). The output voltage (V_{OUT}) is represented by a digitally programmable voltage source, as expressed in the following equation:

$$V_{OUT} = (V_{REF} \times NB / 4096) \times Gain$$

where NB is the numeric value of the DAC's binary input code (0 to 4095), V_{REF} is the reference voltage, and Gain is the externally set voltage gain.

The impedance at the reference input is code dependent, ranging from a low value of 14kΩ when the DAC has an input code of 1554 hex, to a high value exceeding several giga ohms (leakage currents) with an input code of 0000 hex. Because the input impedance at the reference pin is code dependent, load regulation of the reference source is important.

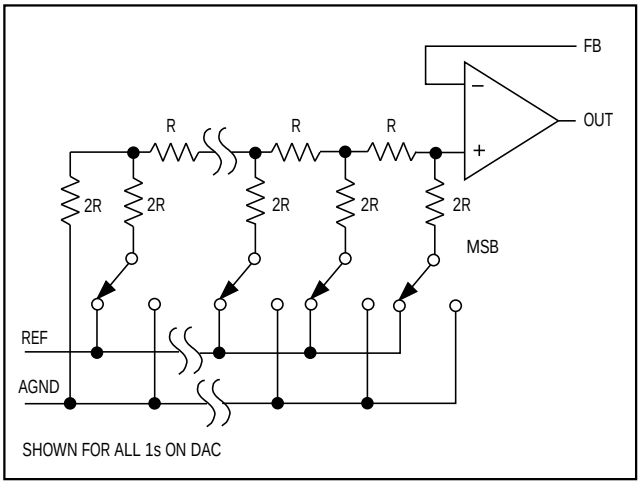


Figure 1. Simplified DAC Circuit Diagram

In shutdown mode, the MAX5352/MAX5353's REF input enters a high-impedance state with a typical input leakage current of 0.001µA.

The reference input capacitance is also code dependent and typically ranges from 15pF (with an input code of all 0s) to 50pF (at full scale).

The MAX873 +2.5V reference is recommended for the MAX5352.

Output Amplifier

The MAX5352/MAX5353's DAC output is internally buffered by a precision amplifier with a typical slew rate of 0.6V/µs. Access to the output amplifier's inverting input provides the user greater flexibility in output gain setting/signal conditioning (see the *Applications Information* section).

With a full-scale transition at the MAX5352/MAX5353 output, the typical settling time to ±1/2LSB is 14µs when loaded with 5kΩ in parallel with 100pF (loads less than 2kΩ degrade performance).

The amplifier's output dynamic responses and settling performances are shown in the *Typical Operating Characteristics*.

Shutdown Mode

The MAX5352/MAX5353 feature a software-programmable shutdown that reduces supply current to a typical value of 4µA. Writing 111X XXXX XXXX XXXX as the input-control word puts the device in shutdown mode (Table 1).

In shutdown mode, the amplifier's output and the reference input enter a high-impedance state. The serial interface remains active. Data in the input registers is retained in shutdown, allowing the MAX5352/MAX5353

to recall the output state prior to entering shutdown. Exit shutdown mode by either recalling the previous configuration or by updating the DAC with new data. When powering up the device or bringing it out of shutdown, allow 20µs for the output to stabilize.

Serial-Interface Configurations

The MAX5352/MAX5353's 3-wire serial interface is compatible with both Microwire™ (Figure 2) and SPI™/QSPI™ (Figure 3). The serial input word consists of three control bits followed by 12+1 data bits (MSB first), as shown in Figure 4. The 3-bit control code determines the MAX5352/MAX5353's response outlined in Table 1.

The MAX5352/MAX5353's digital inputs are double buffered. Depending on the command issued through the serial interface, the input register can be loaded without affecting the DAC register, the DAC register can be loaded directly, or the DAC register can be updated from the input register (Table 1).

The +3.3V MAX5353 can also directly interface with +5V logic.

Serial-Interface Description

The MAX5352/MAX5353 require 16 bits of serial data. Table 1 lists the serial-interface programming commands. For certain commands, the 12+1 data bits are "don't cares." Data is sent MSB first and can be sent in two 8-bit packets or one 16-bit word ($\overline{CS}$ must remain low until 16 bits are transferred). The serial data is composed of three control bits (C2, C1, C0), followed by the 12+1 data bits D11...D0, S0 (Figure 4). Set the sub-bit (S0) to zero. The 3-bit control code determines:

- the register to be updated,
- the configuration when exiting shutdown.

Figure 5 shows the serial-interface timing requirements. The chip-select pin ($\overline{CS}$) must be low to enable the DAC's serial interface. When $\overline{CS}$ is high, the interface control circuitry is disabled. $\overline{CS}$ must go low at least t_{CSS} before the rising serial clock (SCLK) edge to properly clock in the first bit. When $\overline{CS}$ is low, data is clocked into the internal shift register via the serial-data input pin (DIN) on SCLK's rising edge. The maximum guaranteed clock frequency is 10MHz. Data is latched into the MAX5352/MAX5353 input/DAC register on $\overline{CS}$'s rising edge.

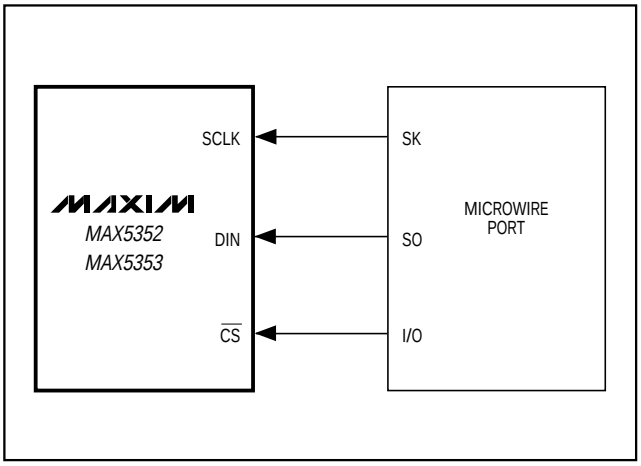


Figure 2. Connections for Microwire

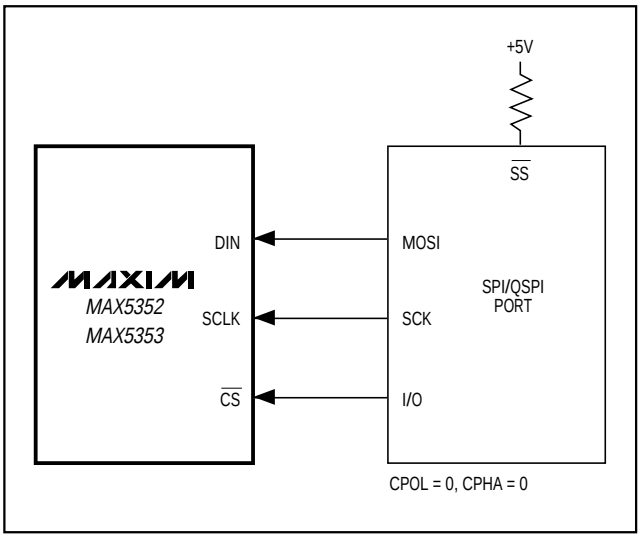


Figure 3. Connections for SPI/QSPI

MSB .....LSB			
← 16 Bits of Serial Data →			
Control Bits			Data Bits MSB .....LSB Sub-Bit
C2	C1	C0	D11 .....D0, S0
← 3 Control Bits →			← 12+1 Data Bits →

Figure 4. Serial-Data Format

Table 1. Serial-Interface Programming Commands

16-BIT SERIAL WORD					FUNCTION
C2	C1	C0	D11.....D0 MSB LSB	S0	
X	0	0	12 bits of data	0	Load input register; DAC register immediately updated (also exit shutdown).
X	0	1	12 bits of data	0	Load input register; DAC register unchanged.
X	1	0	XXXXXXXXXXXX	X	Update DAC register from input register (also exit shutdown; recall previous state).
1	1	1	XXXXXXXXXXXX	X	Shutdown
0	1	1	XXXXXXXXXXXX	X	No operation (NOP)

"X" = Don't care

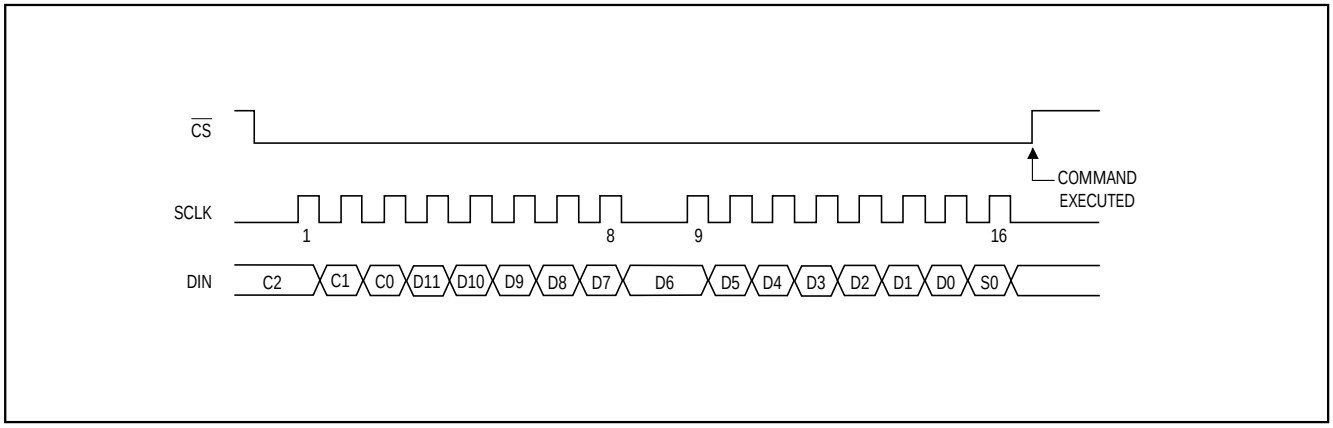


Figure 5. Serial-Interface Timing Diagram

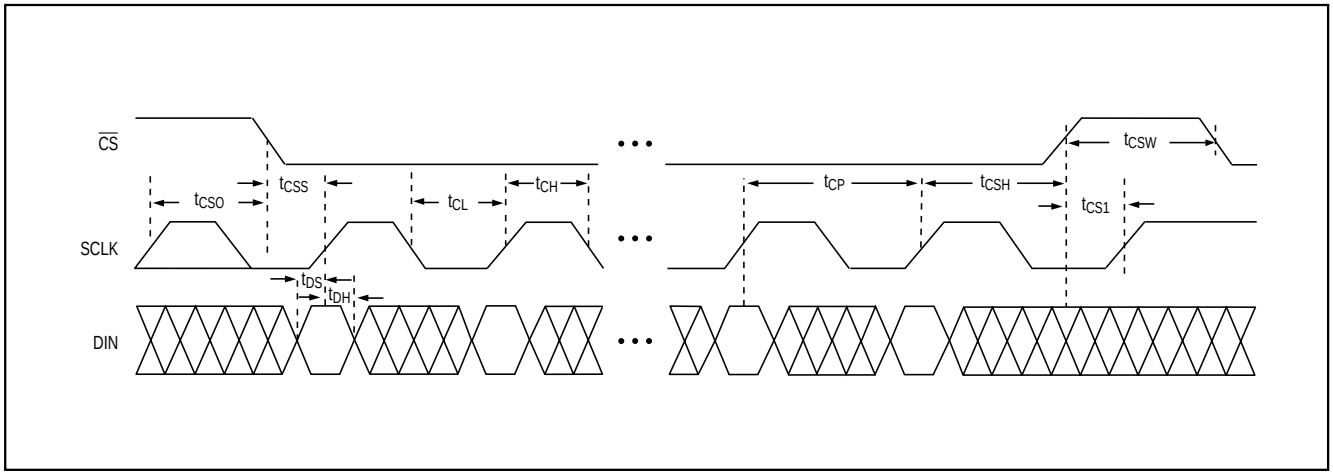


Figure 6. Detailed Serial-Interface Timing Diagram

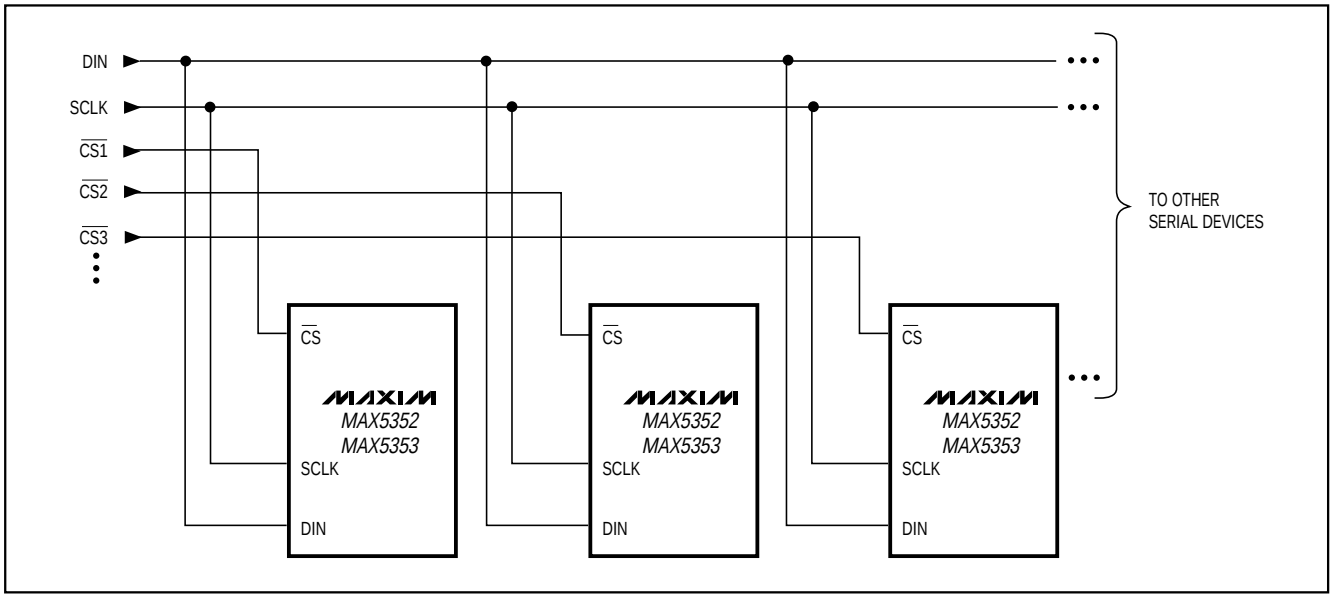


Figure 7. Multiple MAX5352/MAX5353s Sharing Common DIN and SCLK Lines

Figure 7 shows a method of connecting several MAX5352/MAX5353s. In this configuration, the clock and the data bus are common to all devices, and separate chip-select lines are used for each IC.

Applications Information

Unipolar Output

For a unipolar output, the output voltage and the reference input have the same polarity. Figure 8 shows the MAX5352/MAX5353 unipolar output circuit, which is also the typical operating circuit. Table 2 lists the unipolar output codes.

Figure 9 illustrates a rail-to-rail output. This circuit shows the MAX5352 with the output amplifier configured with a closed-loop gain of +2 to provide a 0V to 5V full-scale range when a 2.5V reference is used. When the MAX5353 is used with a 1.25V reference, this circuit provides a 0V to 2.5V full-scale range.

Bipolar Output

The MAX5352/MAX5353 output can be configured for bipolar operation using Figure 10's circuit according to the following equation:

$$V_{OUT} = V_{REF} [(2NB / 4096) - 1]$$

where NB is the numeric value of the DAC's binary input code. Table 3 shows digital codes (offset binary) and the corresponding output voltage for Figure 10's circuit.

Table 2. Unipolar Code Table

DAC CONTENTS MSB LSB	ANALOG OUTPUT
1111 1111 1111 (0)	$+V_{REF}\left(\frac{4095}{4096}\right)$
1000 0000 0001 (0)	$+V_{REF}\left(\frac{2049}{4096}\right)$
1000 0000 0000 (0)	$+V_{REF}\left(\frac{2048}{4096}\right) = \frac{+V_{REF}}{2}$
0111 1111 1111 (0)	$+V_{REF}\left(\frac{2047}{4096}\right)$
0000 0000 0001 (0)	$+V_{REF}\left(\frac{1}{4096}\right)$
0000 0000 0000 (0)	0V

NOTE: ( ) are for sub-bit.

Using an AC Reference

In applications where the reference has AC-signal components, the MAX5352/MAX5353 have multiplying capability within the reference input range specifications. Figure 11 shows a technique for applying a sine-wave signal to the reference input where the AC signal is offset before being applied to REF. The reference voltage must never be more negative than GND.

Table 3. Bipolar Code Table

DAC CONTENTS MSB LSB	ANALOG OUTPUT
1111 1111 1111 (0)	$+V_{REF}\left(\frac{2047}{2048}\right)$
1000 0000 0001 (0)	$+V_{REF}\left(\frac{1}{2048}\right)$
1000 0000 0000 (0)	0V
0111 1111 1111 (0)	$-V_{REF}\left(\frac{1}{2048}\right)$
0000 0000 0001 (0)	$-V_{REF}\left(\frac{2047}{2048}\right)$
0000 0000 0000 (0)	$-V_{REF}\left(\frac{2048}{2048}\right) = -V_{REF}$

NOTE: ( ) are for sub-bit.

The MAX5352's total harmonic distortion plus noise (THD+N) is typically less than -77dB (full-scale code), and the MAX5353's THD+N is typically less than -72dB (full-scale code), given a 1Vp-p signal swing and input frequencies up to 25kHz. The typical -3dB frequency is 650kHz for both devices, as shown in the *Typical Operating Characteristics* graphs.

Digitally Programmable Current Source

The circuit of Figure 12 places an NPN transistor (2N3904 or similar) within the op-amp feedback loop to implement a digitally programmable, unidirectional current source. The output current is calculated with the following equation:

$$I_{OUT} = (V_{REF}/R) \times (NB/4096)$$

where NB is the numeric value of the DAC's binary input code and R is the sense resistor shown in Figure 12.

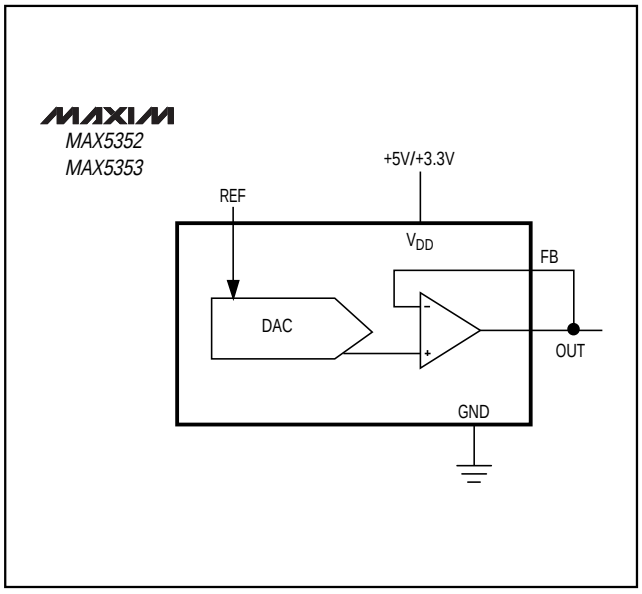


Figure 8. Unipolar Output Circuit

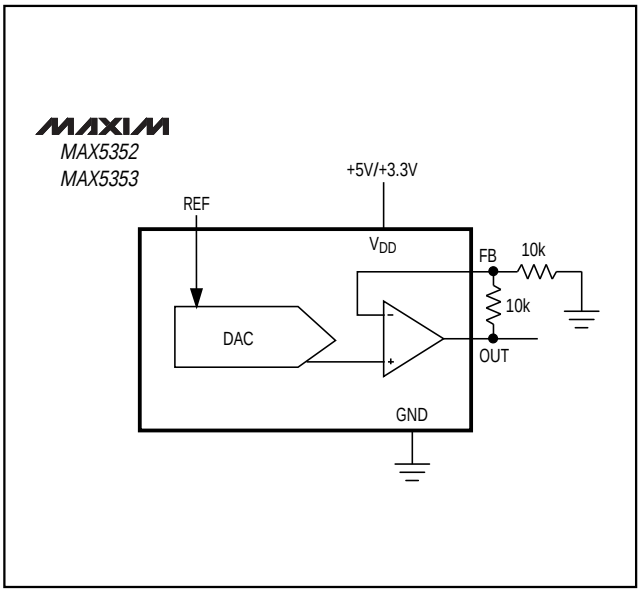


Figure 9. Unipolar Rail-to-Rail Output Circuit

Low-Power, 12-Bit Voltage-Output DACs with Serial Interface

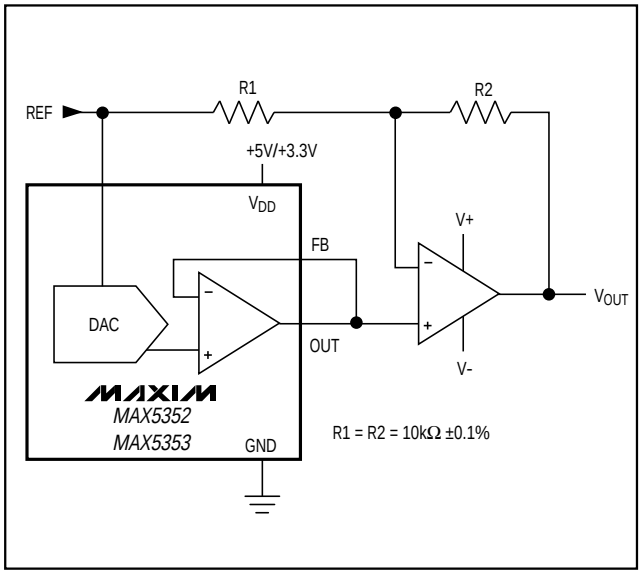


Figure 10. Bipolar Output Circuit

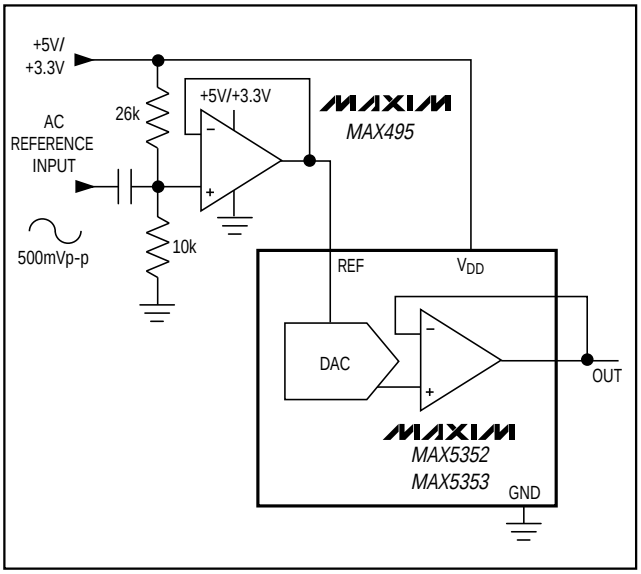


Figure 11. AC Reference Input Circuit

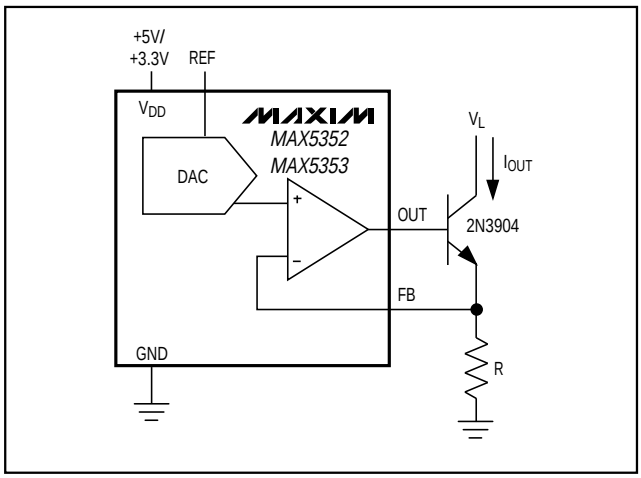


Figure 12. Digitally Programmable Current Source

Power-Supply Considerations

On power-up, the input and DAC registers are cleared (set to zero code).

For rated MAX5352/MAX5353 performance, REF must be at least 1.4V below V_{DD}. Bypass V_{DD} with a 4.7µF capacitor in parallel with a 0.1µF capacitor to GND. Use short lead lengths and place the bypass capacitors as close to the supply pins as possible.

Grounding and Layout Considerations

Digital or AC transient signals on GND can create noise at the analog output. Tie GND to the highest-quality ground available.

Good printed circuit board ground layout minimizes crosstalk between the DAC output, reference input, and digital input. Reduce crosstalk by keeping analog lines away from digital lines. Wire-wrapped boards are not recommended.

_Ordering Information (continued)

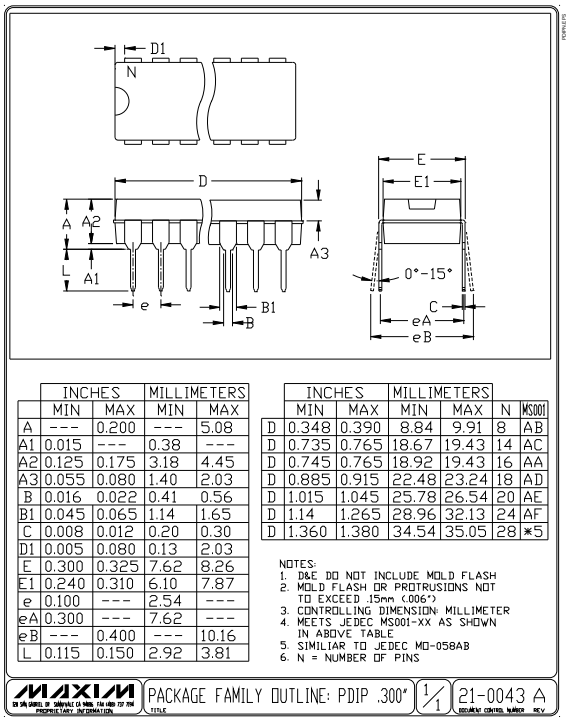
PART*	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX5352AEPA	-40°C to +85°C	8 Plastic DIP	±1/2
MAX5352BEPA	-40°C to +85°C	8 Plastic DIP	±1
MAX5352AEUA	-40°C to +85°C	8 µMAX	±1/2
MAX5352BEUA	-40°C to +85°C	8 µMAX	±1
MAX5352BMJA	-55°C to +125°C	8 CERDIP**	±2
MAX5353ACPA	0°C to +70°C	8 Plastic DIP	±1
MAX5353BCPA	0°C to +70°C	8 Plastic DIP	±2
MAX5353ACUA	0°C to +70°C	8 µMAX	±1
MAX5353BCUA	0°C to +70°C	8 µMAX	±2
MAX5353AEPA	-40°C to +85°C	8 Plastic DIP	±1
MAX5353BEPA	-40°C to +85°C	8 Plastic DIP	±2
MAX5353AEUA	-40°C to +85°C	8 µMAX	±1
MAX5353BEUA	-40°C to +85°C	8 µMAX	±2
MAX5353BMJA	-55°C to +125°C	8 CERDIP**	±4

**Contact factory for availability of 8-pin SO package.*
***Contact factory for availability and processing to MIL-STD-883.*

_____Chip Information

TRANSISTOR COUNT: 1677

_____Package Information



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	---	0.200	---	5.08
A1	0.015	---	0.38	---
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.016	0.022	0.41	0.56
B1	0.045	0.065	1.14	1.65
C	0.008	0.012	0.20	0.30
D1	0.005	0.080	0.13	2.03
E	0.300	0.325	7.62	8.26
E1	0.240	0.310	6.10	7.87
e	0.100	---	2.54	---
eA	0.300	---	7.62	---
eB	---	0.400	---	10.16
L	0.115	0.150	2.92	3.81

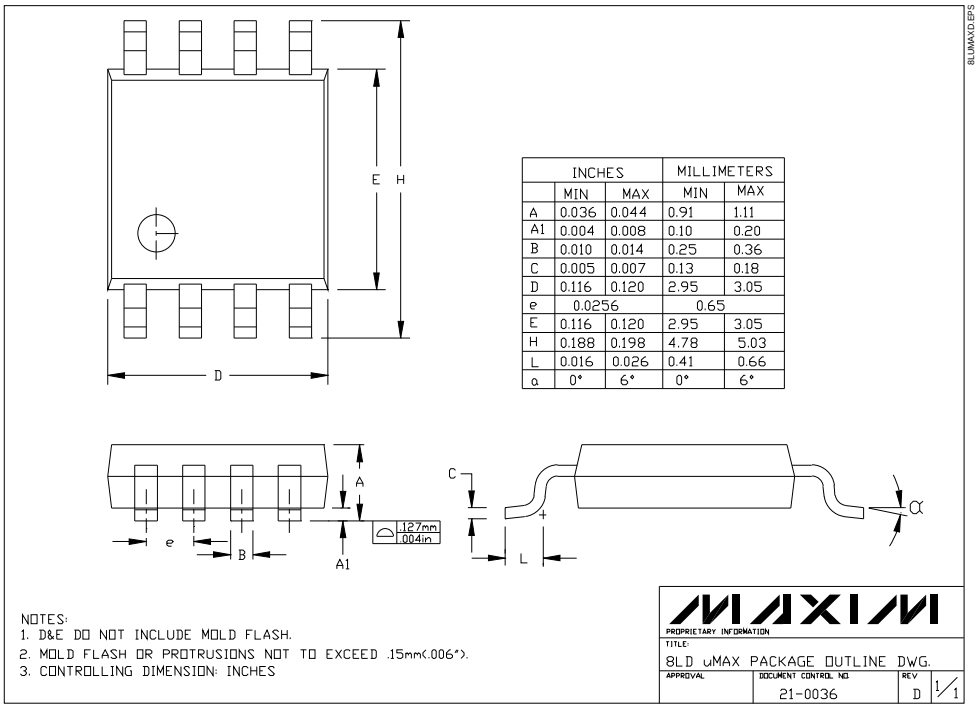
	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS001
D	0.348	0.390	8.84	9.91	8	AB
D	0.735	0.765	18.67	19.43	14	AC
D	0.745	0.765	18.92	19.43	16	AA
D	0.885	0.915	22.48	23.24	18	AD
D	1.015	1.045	25.78	26.54	20	AE
D	1.14	1.265	28.96	32.13	24	AF
D	1.360	1.380	34.54	35.05	28	*5

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC MS001-XX AS SHOWN IN ABOVE TABLE
5. SIMILIAR TO JEDEC MO-058AB
6. N = NUMBER OF PINS

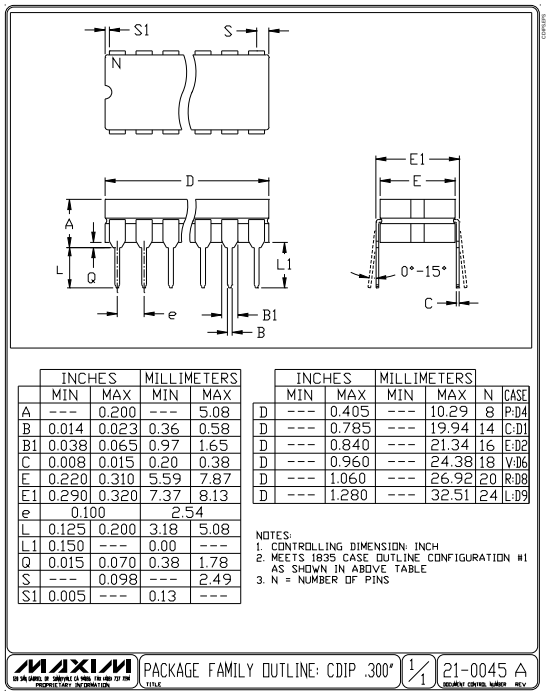
MAXIM | PACKAGE FAMILY OUTLINE: PDIP .300" | 1/1 | 21-0043 A

Low-Power, 12-Bit Voltage-Output DACs with Serial Interface

Package Information (continued)



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.036	0.044	0.91	1.11
A1	0.004	0.008	0.10	0.20
B	0.010	0.014	0.25	0.36
C	0.005	0.007	0.13	0.18
D	0.116	0.120	2.95	3.05
e	0.0256		0.65	
E	0.116	0.120	2.95	3.05
H	0.188	0.198	4.78	5.03
L	0.016	0.026	0.41	0.66
α	0°	6°	0°	6°



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	---	0.200	---	5.08
B	0.014	0.023	0.36	0.58
B1	0.038	0.065	0.97	1.65
C	0.008	0.015	0.20	0.38
E	0.220	0.310	5.59	7.87
E1	0.290	0.320	7.37	8.13
e	0.100		2.54	
L	0.125	0.200	3.18	5.08
L1	0.150	---	0.00	---
Q	0.015	0.070	0.38	1.78
S	---	0.098	---	2.49
S1	0.005	---	0.13	---

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	CASE
D	---	0.405	---	10.29	8	P-D4
D	---	0.785	---	19.94	14	C-D1
D	---	0.840	---	21.34	16	E-D2
D	---	0.960	---	24.38	18	V-D6
D	---	1.060	---	26.92	20	R-D8
D	---	1.280	---	32.51	24	L-D9

NOTES:
1. CONTROLLING DIMENSION: INCH
2. MEETS 1835 CASE OUTLINE CONFIGURATION #1 AS SHOWN IN ABOVE TABLE
3. N = NUMBER OF PINS

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