OKI Semiconductor

This version: Jul. 1999
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# ML63187/63189B

**4-Bit Microcontroller with Built-in 1024-Dot Matrix LCD Drivers and Melody Circuit, Operating at 0.9 V (Min.)**

## GENERAL DESCRIPTION

The ML63187/63189B is a CMOS 4-bit microcontroller with built-in 1024-dot matrix LCD drivers and operates at 0.9 V (min.). The ML63187/63189B is suitable for applications such as games, toys, watches, etc. which are provided with an LCD display.
The ML63187/63189B is an M6318x series mask ROM-version product of OLMS-63K family, which employs Oki's original CPU core nX-4/250.

## FEATURES

- Rich instruction set
  408 instructions
  Transfer, rotate, increment/decrement, arithmetic operations, comparison, logic operations, mask operations, bit operations, ROM table reference, stack operations, flag operations, branch, conditional branch, call/return, control.

- Rich selection of addressing modes
  Indirect addressing of four data memory types, with current bank register, extra bank register, HL register and XY register.
  Data memory bank internal direct addressing mode.

- Processing speed
  Two clocks per machine cycle, with most instructions executed in one machine cycle.
  Minimum instruction execution time : 61 µs (@ 32.768 kHz system clock)
  1 µs (@ 2 MHz system clock)

- Clock generation circuit
  Low-speed clock : Crystal oscillation or RC oscillation selected with mask option (30 to 80 kHz)
  High-speed clock : Ceramic oscillation or RC oscillation selected with software (2 MHz max.)

- Program memory space
  - ML63187 : 16K words
  - ML63189B : 32K words

  Basic instruction length is 16 bits/1 word

- Data memory space
  - ML63187 : 1024 nibbles
  - ML63189B : 1536 nibbles

• Stack level
Call stack level : 16 levels
Register stack level : 16 levels

• I/O ports
Input ports: Selectable as input with pull-up resistor/input with pull-down resistor/high-impedance input
Input-output ports: Selectable as input with pull-up resistor/input with pull-down resistor/high-impedance input
Selectable as P-channel open drain output/N-channel open drain output/CMOS output/high-impedance output
Can be interfaced with external peripherals that use a different power supply than this device uses.
Number of ports:
ML63187
Input-output port : 2 ports × 4 bits
ML63189B
Input port : 1 port × 4 bits
Input-output port : 4 ports × 4 bits

• Melody output
Melody frequency : 529 to 2979 Hz
Tone length : 63 types
Tempo : 15 types
Melody data : Resides in the program memory
Buzzer driver signal output : 4 kHz

• LCD driver
Number of segments : 1024 Max. (64 SEG × 16 COM)
1/1 to 1/16 duty
1/4 or 1/5 bias (regulator built-in)
Selectable as all-ON mode/all-OFF mode/power down mode/normal display mode
Adjustable contrast

• Reset function
Reset through RESET pin
Power-on reset
Reset by low-speed oscillation halt

• Battery check
Low-voltage supply check
The value of the judgment voltage is selected by the software by setting the LD1 and LD0 bits of BLDCON.

| LD1 | LD0 | Judgment Voltage (V) | Remarks |
|---|---|---|---|
| 0 | 0 | 1.05 ±0.10 | Ta = 25°C |
| 0 | 1 | 1.20 ±0.10 | Ta = 25°C |
| 1 | 0 | 1.80 ±0.10 | Ta = 25°C |
| 1 | 1 | 2.40 ±0.10 | Ta = 25°C |

- Power supply backup
  Backup circuit (voltage multiplier) enables operation at 0.9 V minimum

- Timers and counter
  8-bit timer × 4
    Selectable as auto-reload mode/capture mode/clock frequency measurement mode
  Watchdog timer × 1
  100 Hz timer × 1
    Measurable in steps of 1/100 sec.
  15-bit time base counter × 1
    1, 2, 4, 8, 16, 32, 64, and 128 Hz signals can be read

- Shift register

| | | |
|---|---|---|
| Shift clock | : | 1 × or 1/2 × system clock, timer 1 overflow, external clock |
| Data length | : | 8 bits |

- Interrupt sources

ML63187

| | | |
|---|---|---|
| External interrupt | : | 2 |
| Internal interrupt | : | 12 (watchdog timer interrupt is a nonmaskable interrupt) |

ML63189B

| | | |
|---|---|---|
| External interrupt | : | 3 |
| Internal interrupt | : | 12 (watchdog timer interrupt is a nonmaskable interrupt) |

- Operating temperature
  –20 to +70°C

- Operating voltage

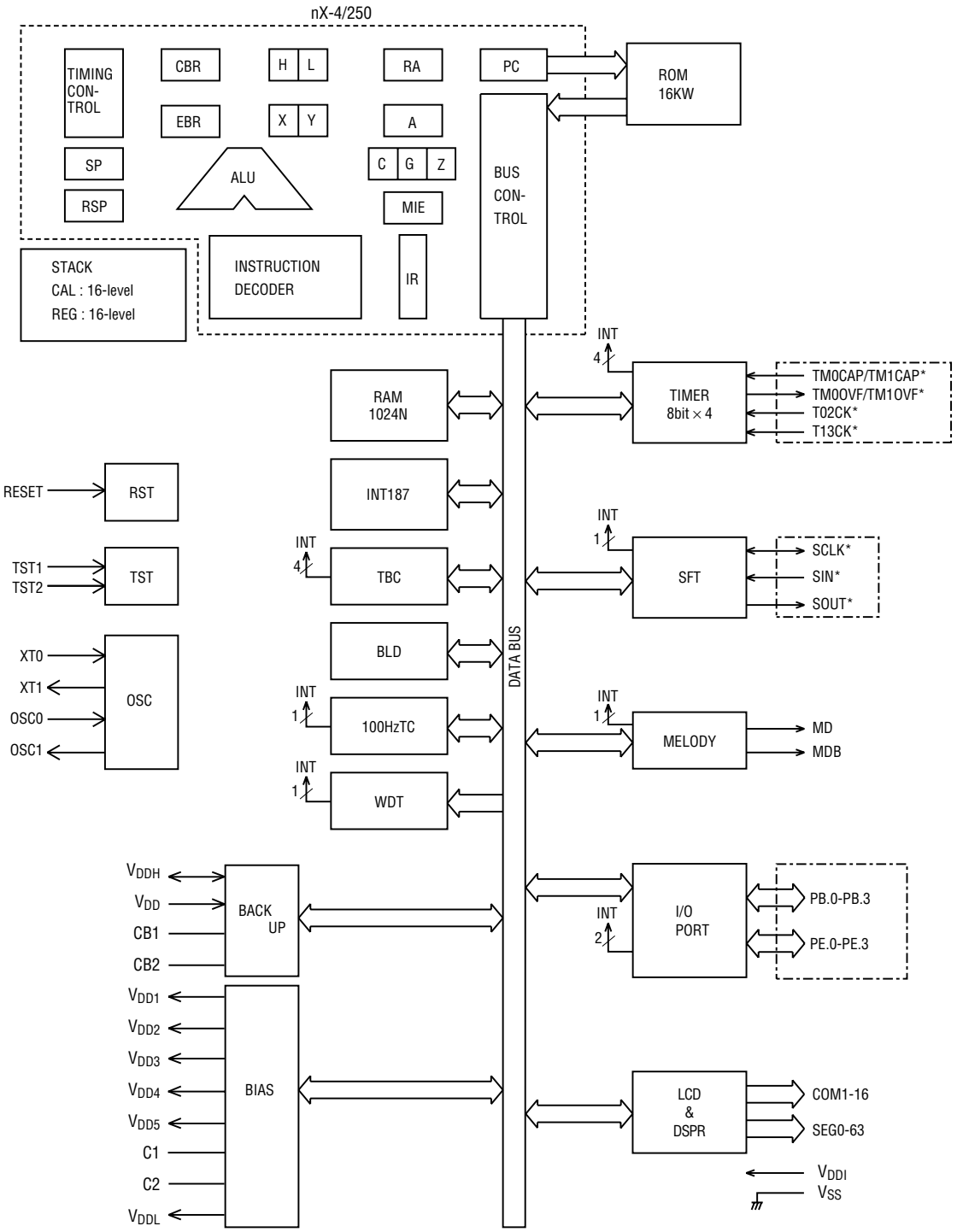
| | | |
|---|---|---|
| When backup used | : | 0.9 to 2.7 V<br>(Operating frequency: 30 to 80 kHz)<br>1.2 to 2.7 V<br>(Operating frequency: 300 to 500 kHz)<br>1.5 to 2.7 V<br>(Operating frequency: 200 kHz to 1 MHz) |
| When backup not used | : | 1.8 to 5.5 V<br>(Operating frequency: 200 kHz to 2 MHz) |

- Package:

| | | |
|---|---|---|
| 128-pin plastic QFP (QFP128-P-1420-0.50-K) | : | (Product name: ML63187-xxxGA, ML63189B-xxxGA) |
| Chip | : | ML63187-xxx, ML63189B-xxx<br>xxx indicates a code number. |

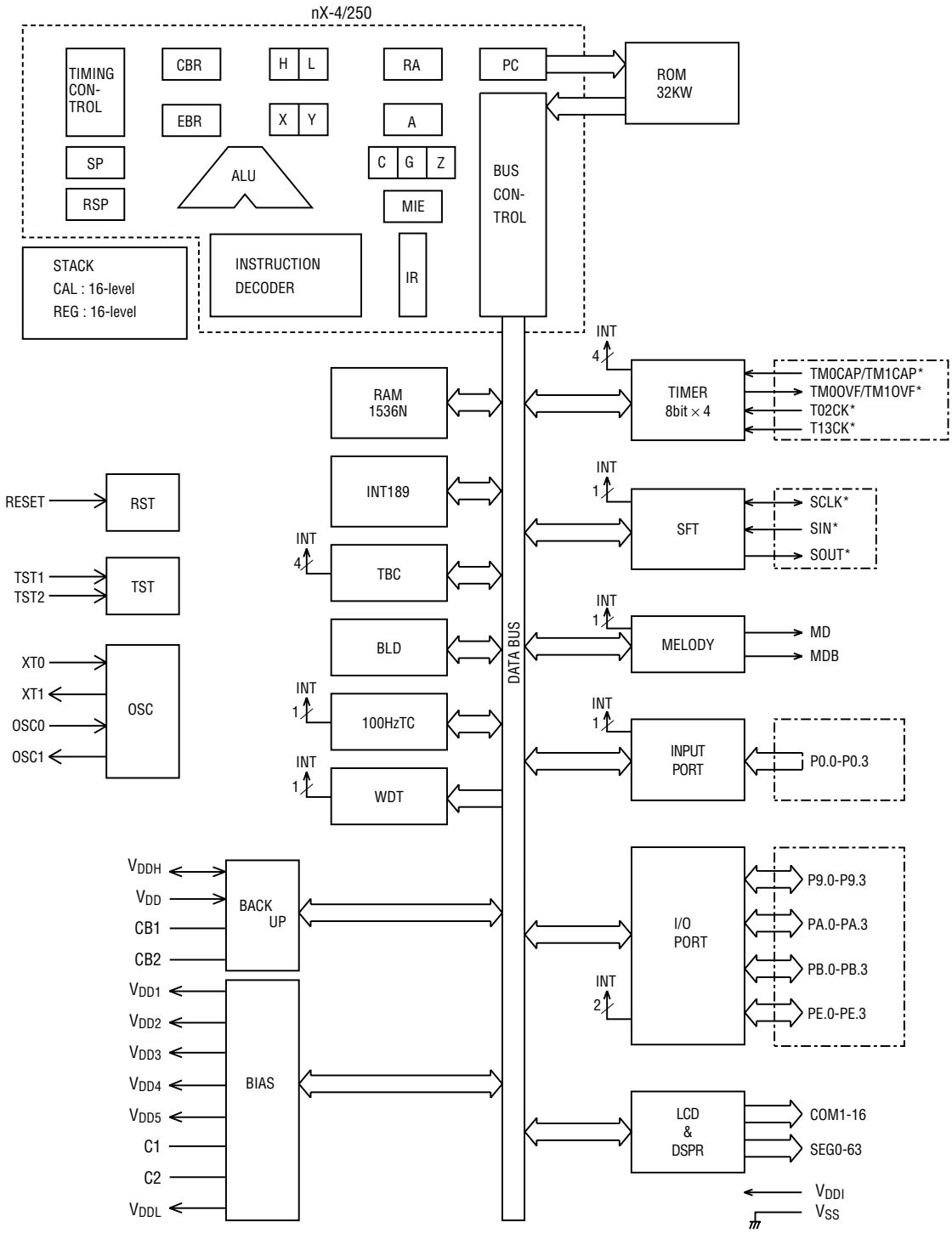
## BLOCK DIAGRAM (ML63187)

An asterisk (*) indicates the port secondary function. ⬚ indicates that the power is supplied to the circuits corresponding to the signal names inside ⬚ from $V_{DDI}$ (power supply for interface).

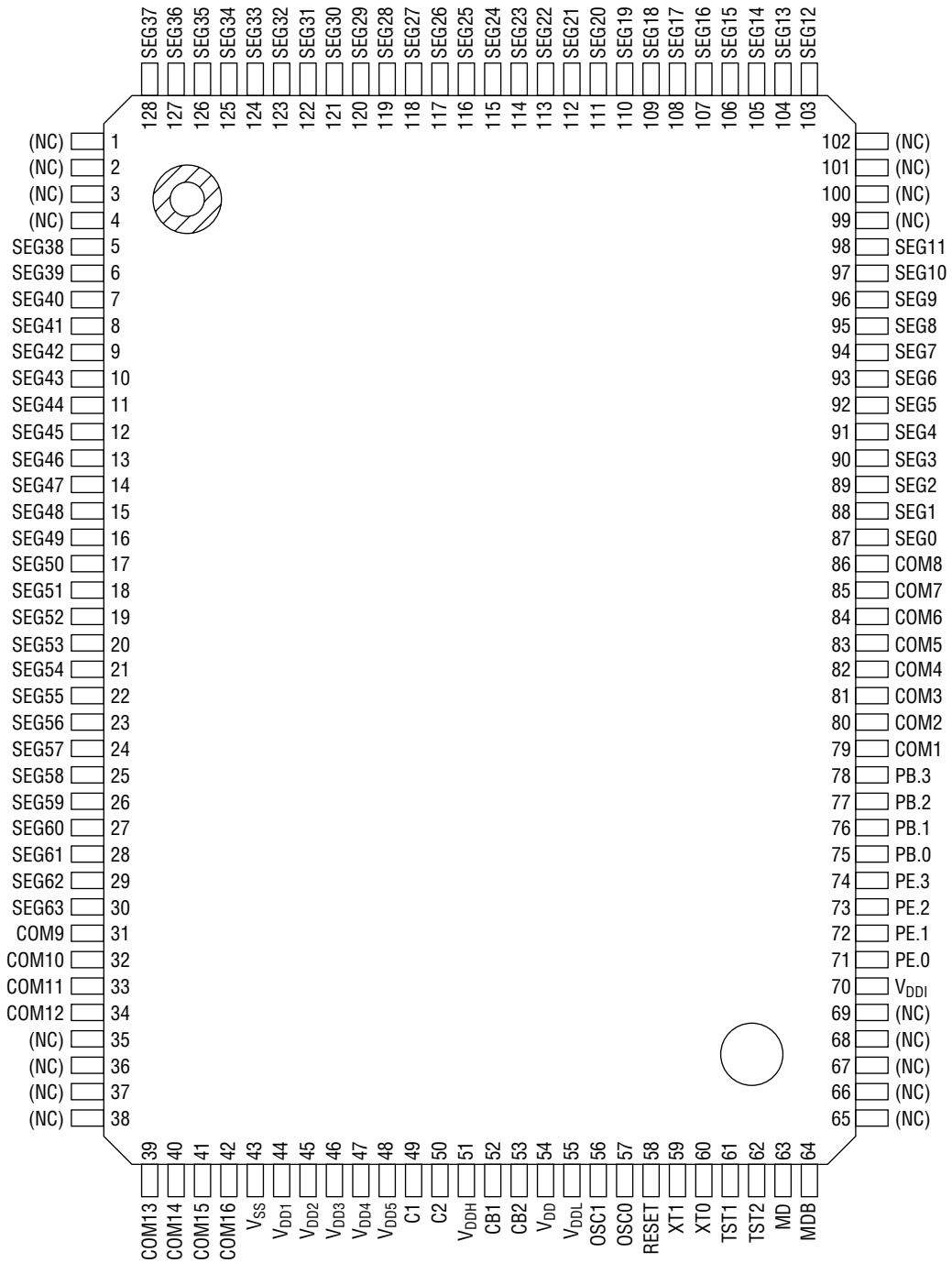


## BLOCK DIAGRAM (ML63189B)

An asterisk (*) indicates the port secondary function. ⬚ indicates that the power is supplied to the circuits corresponding to the signal names inside ⬚ from $V_{DDI}$ (power supply for interface).



## PIN CONFIGURATION (TOP VIEW) (ML63187)

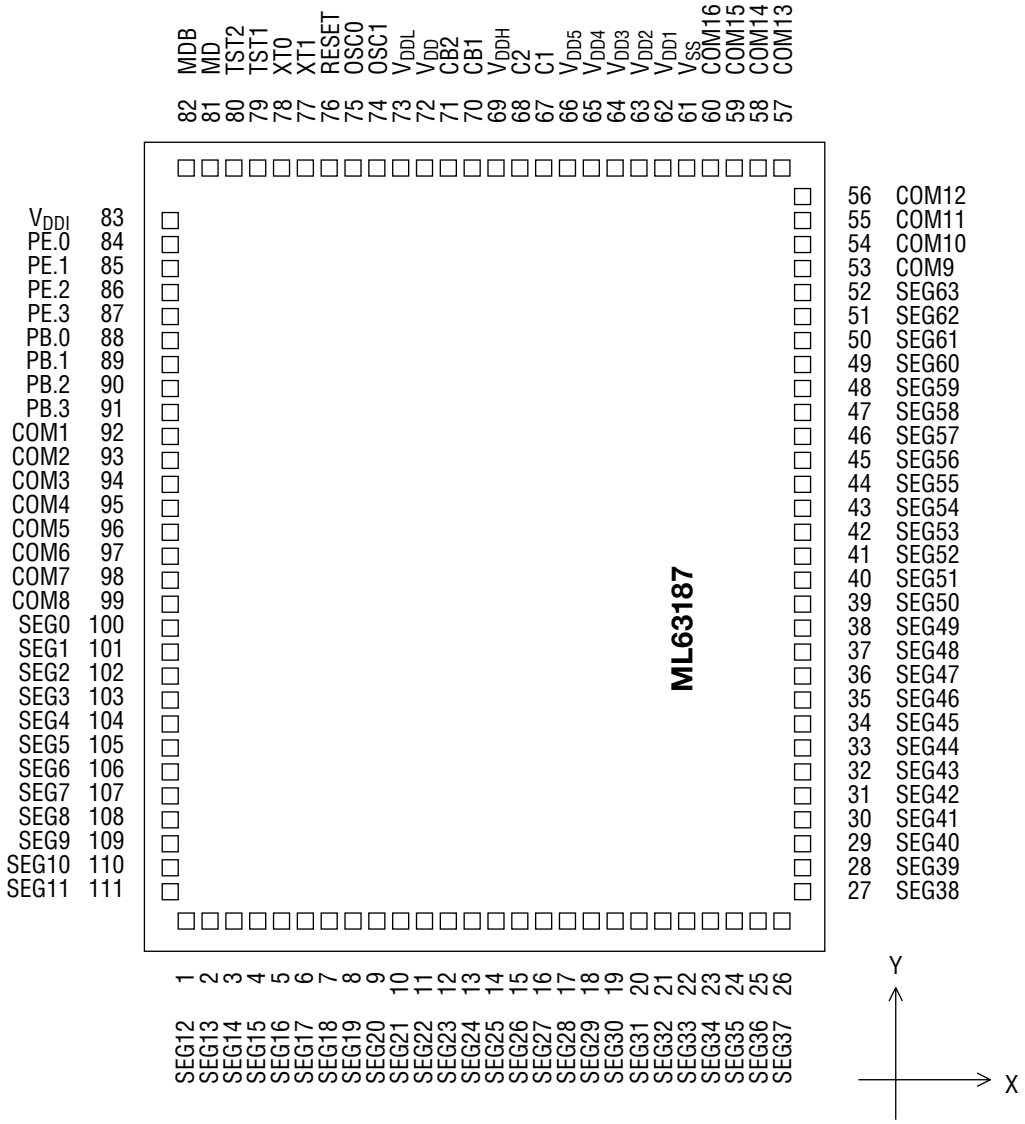



**128-Pin Plastic QFP**

Note: Pins marked as (NC) are no-connection pins which are left open.

## PAD CONFIGURATION (ML63187)

### Pad Layout



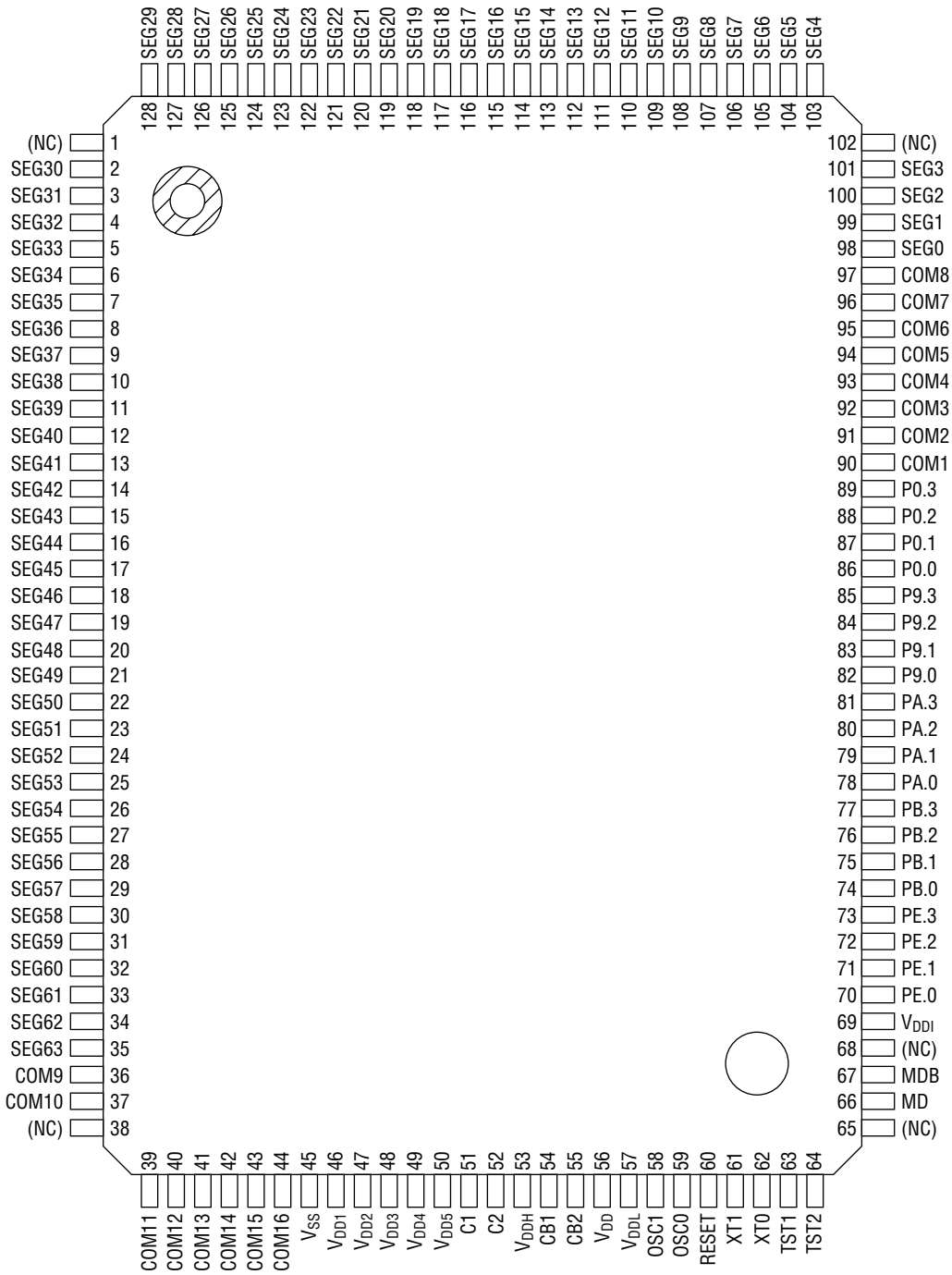

| | |
|---|---|
| Chip size | : 4.238 mm × 4.914 mm |
| Chip thickness | : 350 µm (280 µm: available as required) |
| Coordinate origin | : center of chip |
| Pad hole size | : 100 µm × 100 µm |
| Pad size | : 110 µm × 110 µm |
| Minimum pad pitch | : 140 µm |

Note: The chip substrate voltage is $V_{SS}$.

## Pad Coordinates (ML63187)

| Pad No. | Pad Name | X (µm) | Y (µm) | Pad No. | Pad Name | X (µm) | Y (µm) | Pad No. | Pad Name | X (µm) | Y (µm) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | SEG12 | –1755 | –2311 | 42 | SEG53 | 1969 | 70 | 83 | $V_{DDI}$ | –1969 | 1895 |
| 2 | SEG13 | –1615 | –2311 | 43 | SEG54 | 1969 | 211 | 84 | PE.0 | –1969 | 1755 |
| 3 | SEG14 | –1474 | –2311 | 44 | SEG55 | 1969 | 351 | 85 | PE.1 | –1969 | 1615 |
| 4 | SEG15 | –1334 | –2311 | 45 | SEG56 | 1969 | 491 | 86 | PE.2 | –1969 | 1474 |
| 5 | SEG16 | –1193 | –2311 | 46 | SEG57 | 1969 | 632 | 87 | PE.3 | –1969 | 1334 |
| 6 | SEG17 | –1053 | –2311 | 47 | SEG58 | 1969 | 772 | 88 | PB.0 | –1969 | 1193 |
| 7 | SEG18 | –913 | –2311 | 48 | SEG59 | 1969 | 913 | 89 | PB.1 | –1969 | 1053 |
| 8 | SEG19 | –772 | –2311 | 49 | SEG60 | 1969 | 1053 | 90 | PB.2 | –1969 | 913 |
| 9 | SEG20 | –632 | –2311 | 50 | SEG61 | 1969 | 1193 | 91 | PB.3 | –1969 | 772 |
| 10 | SEG21 | –491 | –2311 | 51 | SEG62 | 1969 | 1334 | 92 | COM1 | –1969 | 632 |
| 11 | SEG22 | –351 | –2311 | 52 | SEG63 | 1969 | 1474 | 93 | COM2 | –1969 | 491 |
| 12 | SEG23 | –211 | –2311 | 53 | COM9 | 1969 | 1615 | 94 | COM3 | –1969 | 351 |
| 13 | SEG24 | –70 | –2311 | 54 | COM10 | 1969 | 1755 | 95 | COM4 | –1969 | 211 |
| 14 | SEG25 | 70 | –2311 | 55 | COM11 | 1969 | 1895 | 96 | COM5 | –1969 | 70 |
| 15 | SEG26 | 211 | –2311 | 56 | COM12 | 1969 | 2036 | 97 | COM6 | –1969 | –70 |
| 16 | SEG27 | 351 | –2311 | 57 | COM13 | 1755 | 2311 | 98 | COM7 | –1969 | –211 |
| 17 | SEG28 | 491 | –2311 | 58 | COM14 | 1615 | 2311 | 99 | COM8 | –1969 | –351 |
| 18 | SEG29 | 632 | –2311 | 59 | COM15 | 1474 | 2311 | 100 | SEG0 | –1969 | –491 |
| 19 | SEG30 | 772 | –2311 | 60 | COM16 | 1334 | 2311 | 101 | SEG1 | –1969 | –632 |
| 20 | SEG31 | 913 | –2311 | 61 | $V_{SS}$ | 1193 | 2311 | 102 | SEG2 | –1969 | –772 |
| 21 | SEG32 | 1053 | –2311 | 62 | $V_{DD1}$ | 1053 | 2311 | 103 | SEG3 | –1969 | –913 |
| 22 | SEG33 | 1193 | –2311 | 63 | $V_{DD2}$ | 913 | 2311 | 104 | SEG4 | –1969 | –1053 |
| 23 | SEG34 | 1334 | –2311 | 64 | $V_{DD3}$ | 772 | 2311 | 105 | SEG5 | –1969 | –1193 |
| 24 | SEG35 | 1474 | –2311 | 65 | $V_{DD4}$ | 632 | 2311 | 106 | SEG6 | –1969 | –1334 |
| 25 | SEG36 | 1615 | –2311 | 66 | $V_{DD5}$ | 491 | 2311 | 107 | SEG7 | –1969 | –1474 |
| 26 | SEG37 | 1755 | –2311 | 67 | C1 | 351 | 2311 | 108 | SEG8 | –1969 | –1615 |
| 27 | SEG38 | 1969 | –2036 | 68 | C2 | 211 | 2311 | 109 | SEG9 | –1969 | –1755 |
| 28 | SEG39 | 1969 | –1895 | 69 | $V_{DDH}$ | 70 | 2311 | 110 | SEG10 | –1969 | –1895 |
| 29 | SEG40 | 1969 | –1755 | 70 | CB1 | –70 | 2311 | 111 | SEG11 | –1969 | –2036 |
| 30 | SEG41 | 1969 | –1615 | 71 | CB2 | –211 | 2311 | | | | |
| 31 | SEG42 | 1969 | –1474 | 72 | $V_{DD}$ | –351 | 2311 | | | | |
| 32 | SEG43 | 1969 | –1334 | 73 | $V_{DDL}$ | –491 | 2311 | | | | |
| 33 | SEG44 | 1969 | –1193 | 74 | OSC1 | –632 | 2311 | | | | |
| 34 | SEG45 | 1969 | –1053 | 75 | OSC0 | –772 | 2311 | | | | |
| 35 | SEG46 | 1969 | –913 | 76 | RESET | –913 | 2311 | | | | |
| 36 | SEG47 | 1969 | –772 | 77 | XT1 | –1053 | 2311 | | | | |
| 37 | SEG48 | 1969 | –632 | 78 | XT0 | –1193 | 2311 | | | | |
| 38 | SEG49 | 1969 | –491 | 79 | TST1 | –1334 | 2311 | | | | |
| 39 | SEG50 | 1969 | –351 | 80 | TST2 | –1474 | 2311 | | | | |
| 40 | SEG51 | 1969 | –211 | 81 | MD | –1615 | 2311 | | | | |
| 41 | SEG52 | 1969 | –70 | 82 | MDB | –1755 | 2311 | | | | |

## PIN CONFIGURATION (TOP VIEW) (ML63189B)

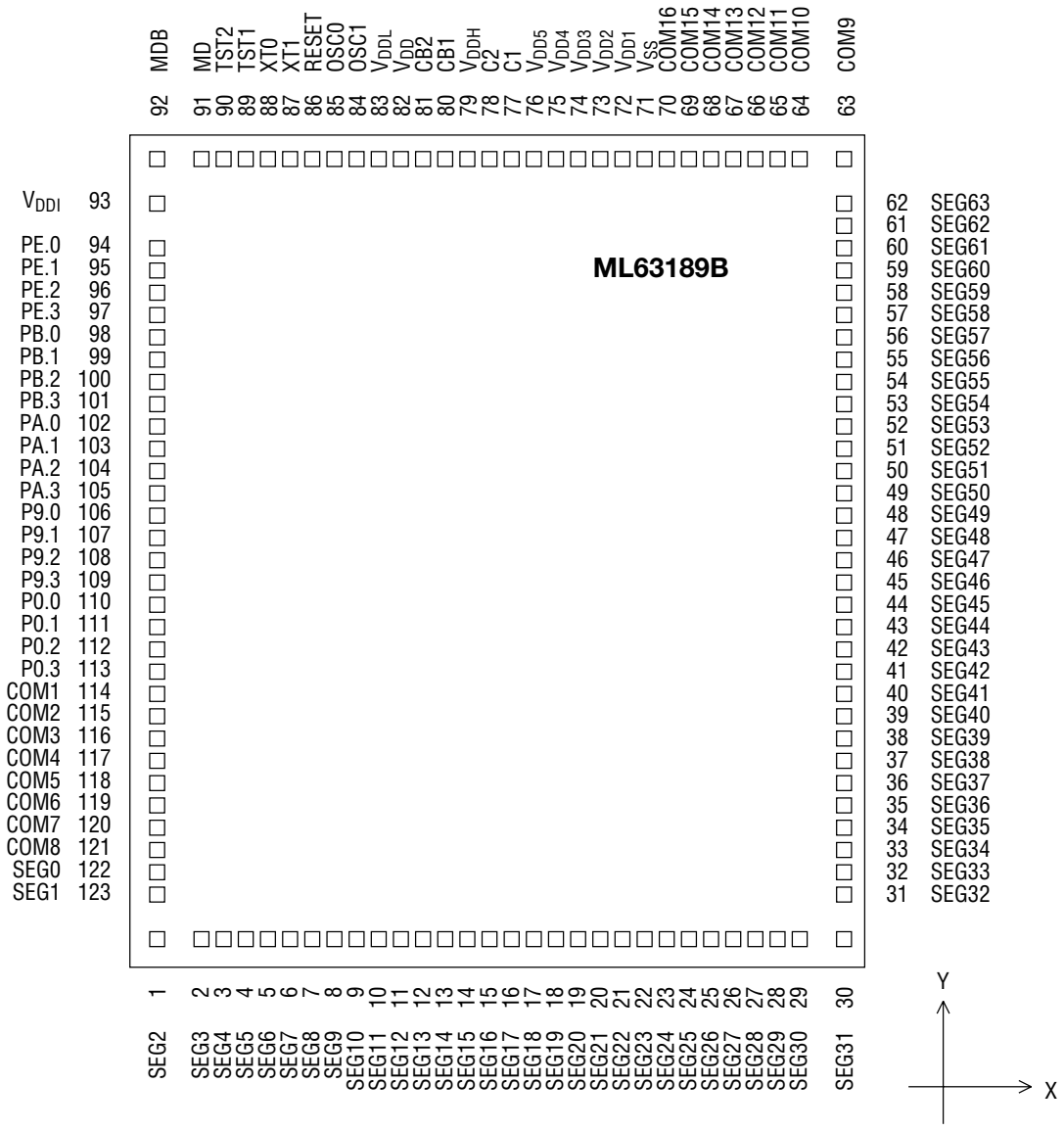



**128-Pin Plastic QFP**

Note: Pins marked as (NC) are no-connection pins which are left open.

## PAD CONFIGURATION (ML63189B)

### Pad Layout




| | |
|---|---|
| Chip size | : 4.81 mm × 5.20 mm |
| Chip thickness | : 350 µm (280 µm: available as required) |
| Coordinate origin | : center of chip |
| Pad hole size | : 100 µm × 100 µm |
| Pad size | : 110 µm × 110 µm |
| Minimum pad pitch | : 140 µm |

Note: The chip substrate voltage is $V_{SS}$.

## Pad Coordinates (ML63189B)

| Pad No. | Pad Name | X (µm) | Y (µm) | Pad No. | Pad Name | X (µm) | Y (µm) | Pad No. | Pad Name | X (µm) | Y (µm) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | SEG2 | –2259 | –2438 | 42 | SEG43 | 2259 | –632 | 83 | $V_{DDL}$ | –772 | 2438 |
| 2 | SEG3 | –1895 | –2438 | 43 | SEG44 | 2259 | –491 | 84 | OSC1 | –913 | 2438 |
| 3 | SEG4 | –1755 | –2438 | 44 | SEG45 | 2259 | –351 | 85 | OSC0 | –1053 | 2438 |
| 4 | SEG5 | –1615 | –2438 | 45 | SEG46 | 2259 | –211 | 86 | RESET | –1193 | 2438 |
| 5 | SEG6 | –1474 | –2438 | 46 | SEG47 | 2259 | –70 | 87 | XT1 | –1334 | 2438 |
| 6 | SEG7 | –1334 | –2438 | 47 | SEG48 | 2259 | 70 | 88 | XT0 | –1474 | 2438 |
| 7 | SEG8 | –1193 | –2438 | 48 | SEG49 | 2259 | 211 | 89 | TST1 | –1615 | 2438 |
| 8 | SEG9 | –1053 | –2438 | 49 | SEG50 | 2259 | 351 | 90 | TST2 | –1775 | 2438 |
| 9 | SEG10 | –913 | –2438 | 50 | SEG51 | 2259 | 491 | 91 | MD | –1895 | 2438 |
| 10 | SEG11 | –772 | –2438 | 51 | SEG52 | 2259 | 632 | 92 | MDB | –2259 | 2438 |
| 11 | SEG12 | –632 | –2438 | 52 | SEG53 | 2259 | 772 | 93 | $V_{DDI}$ | –2259 | 2132 |
| 12 | SEG13 | –491 | –2438 | 53 | SEG54 | 2259 | 913 | 94 | PE.0 | –2259 | 1895 |
| 13 | SEG14 | –351 | –2438 | 54 | SEG55 | 2259 | 1053 | 95 | PE.1 | –2259 | 1755 |
| 14 | SEG15 | –211 | –2438 | 55 | SEG56 | 2259 | 1193 | 96 | PE.2 | –2259 | 1615 |
| 15 | SEG16 | –70 | –2438 | 56 | SEG57 | 2259 | 1334 | 97 | PE.3 | –2259 | 1474 |
| 16 | SEG17 | 70 | –2438 | 57 | SEG58 | 2259 | 1474 | 98 | PB.0 | –2259 | 1334 |
| 17 | SEG18 | 211 | –2438 | 58 | SEG59 | 2259 | 1615 | 99 | PB.1 | –2259 | 1193 |
| 18 | SEG19 | 351 | –2438 | 59 | SEG60 | 2259 | 1755 | 100 | PB.2 | –2259 | 1053 |
| 19 | SEG20 | 491 | –2438 | 60 | SEG61 | 2259 | 1895 | 101 | PB.3 | –2259 | 913 |
| 20 | SEG21 | 632 | –2438 | 61 | SEG62 | 2259 | 2036 | 102 | PA.0 | –2259 | 772 |
| 21 | SEG22 | 772 | –2438 | 62 | SEG63 | 2259 | 2176 | 103 | PA.1 | –2259 | 632 |
| 22 | SEG23 | 913 | –2438 | 63 | COM9 | 2259 | 2438 | 104 | PA.2 | –2259 | 491 |
| 23 | SEG24 | 1053 | –2438 | 64 | COM10 | 1895 | 2438 | 105 | PA.3 | –2259 | 351 |
| 24 | SEG25 | 1193 | –2438 | 65 | COM11 | 1755 | 2438 | 106 | P9.0 | –2259 | 211 |
| 25 | SEG26 | 1334 | –2438 | 66 | COM12 | 1615 | 2438 | 107 | P9.1 | –2259 | 70 |
| 26 | SEG27 | 1474 | –2438 | 67 | COM13 | 1474 | 2438 | 108 | P9.2 | –2259 | –70 |
| 27 | SEG28 | 1615 | –2438 | 68 | COM14 | 1334 | 2438 | 109 | P9.3 | –2259 | –211 |
| 28 | SEG29 | 1755 | –2438 | 69 | COM15 | 1193 | 2438 | 110 | P0.0 | –2259 | –351 |
| 29 | SEG30 | 1895 | –2438 | 70 | COM16 | 1053 | 2438 | 111 | P0.1 | –2259 | –491 |
| 30 | SEG31 | 2259 | –2438 | 71 | $V_{SS}$ | 913 | 2438 | 112 | P0.2 | –2259 | –632 |
| 31 | SEG32 | 2259 | –2176 | 72 | $V_{DD1}$ | 772 | 2438 | 113 | P0.3 | –2259 | –772 |
| 32 | SEG33 | 2259 | –2036 | 73 | $V_{DD2}$ | 632 | 2438 | 114 | COM1 | –2259 | –913 |
| 33 | SEG34 | 2259 | –1895 | 74 | $V_{DD3}$ | 491 | 2438 | 115 | COM2 | –2259 | –1053 |
| 34 | SEG35 | 2259 | –1755 | 75 | $V_{DD4}$ | 351 | 2438 | 116 | COM3 | –2259 | –1193 |
| 35 | SEG36 | 2259 | –1615 | 76 | $V_{DD5}$ | 211 | 2438 | 117 | COM4 | –2259 | –1334 |
| 36 | SEG37 | 2259 | –1474 | 77 | C1 | 70 | 2438 | 118 | COM5 | –2259 | –1474 |
| 37 | SEG38 | 2259 | –1334 | 78 | C2 | –70 | 2438 | 119 | COM6 | –2259 | –1615 |
| 38 | SEG39 | 2259 | –1193 | 79 | $V_{DDH}$ | –211 | 2438 | 120 | COM7 | –2259 | –1755 |
| 39 | SEG40 | 2259 | –1053 | 80 | CB1 | –351 | 2438 | 121 | COM8 | –2259 | –1895 |
| 40 | SEG41 | 2259 | –913 | 81 | CB2 | –491 | 2438 | 122 | SEG0 | –2259 | –2036 |
| 41 | SEG42 | 2259 | –772 | 82 | $V_{DD}$ | –632 | 2438 | 123 | SEG1 | –2259 | –2176 |

## PIN DESCRIPTIONS

The basic functions of each pin of the ML63187/ML63189B are described in Table 1.
A symbol with a slash (/) denotes a pin that has a secondary function.
Refer to Table 2 for secondary functions.
For type, "—" denotes a power supply pin, "I" an input pin, "O" an output pin, and "I/O" an input-output pin.

**Table 1 Pin Descriptions (Basic Functions)**

| Function | Symbol | Pin No. | | Pad No. | | Type | Description |
|---|---|---|---|---|---|---|---|
| | | ML63187 | ML63189B | ML63187 | ML63189B | | |
| Power Supply | $V_{DD}$ | 54 | 56 | 72 | 82 | — | Positive power supply |
| | $V_{SS}$ | 43 | 45 | 61 | 71 | — | Negative power supply |
| | $V_{DD1}$ | 44 | 46 | 62 | 72 | — | Power supply pins for LCD bias (internally generated). Capacitors (0.1 µF) should be connected between these pins and $V_{SS}$. |
| | $V_{DD2}$ | 45 | 47 | 63 | 73 | | |
| | $V_{DD3}$ | 46 | 48 | 64 | 74 | | |
| | $V_{DD4}$ | 47 | 49 | 65 | 75 | | |
| | $V_{DD5}$ | 48 | 50 | 66 | 76 | | |
| | C1 | 49 | 51 | 67 | 77 | — | Capacitor connection pins for LCD bias generation. |
| | C2 | 50 | 52 | 68 | 78 | — | A capacitor (0.1 µF) should be connected between C1 and C2. |
| | $V_{DDI}$ | 70 | 69 | 83 | 93 | — | Positive power supply pin for external interface (power supply for input, and input-output ports) |
| | $V_{DDL}$ | 55 | 57 | 73 | 83 | — | Positive power supply pin for internal logic (internally generated). A capacitor (0.1 µF) should be connected between this pin and $V_{SS}$. |
| | $V_{DDH}$ | 51 | 53 | 69 | 79 | — | Voltage multiplier pin for power supply backup (internally generated). A capacitor (1.0 µF) should be connected between this pin and $V_{SS}$. |
| | CB1 | 52 | 54 | 70 | 80 | — | Pins to connect a capacitor for voltage multiplier. A capacitor (1.0 µF) should be connected between CB1 and CB2. |
| | CB2 | 53 | 55 | 71 | 81 | — | |
| Oscillation | XT0 | 60 | 62 | 78 | 88 | I | Low-speed clock oscillation pins. An option for using crystal oscillation or RC oscillation is chosen by the mask option. If the crystal oscillation is chosen, a crystal should be connected between XT0 and XT1, and capacitor ($C_G$) should be connected between XT0 and $V_{SS}$. If the RC oscillation is chosen, external oscillation resistor ($R_{OSL}$) should be connected between XT0 and XT1. |
| | XT1 | 59 | 61 | 77 | 87 | O | |
| | OSC0 | 57 | 59 | 75 | 85 | I | High-speed clock oscillation pins. A ceramic resonator and capacitors ($C_{L0}$, $C_{L1}$) or external oscillation resistor ($R_{OSH}$) should be connected to these pins. |
| | OSC1 | 56 | 58 | 74 | 84 | O | |

**Table 1 Pin Descriptions (Basic Functions) (continued)**

| Function | Symbol | Pin No. | | Pad No. | | Type | Description |
|---|---|---|---|---|---|---|---|
| | | ML63187 | ML63189B | ML63187 | ML63189B | | |
| Test | TST1 | 61 | 63 | 79 | 89 | I | Input pins for testing.<br>A pull-down resistor is internally connected to these pins.<br>The user cannot use these pins. |
| | TST2 | 62 | 64 | 80 | 90 | I | |
| Reset | RESET | 58 | 60 | 76 | 86 | I | Reset input pin.<br>Setting this pin to "H" level puts this device into a reset state.<br>Then, setting this pin to "L" level starts executing an instruction from address 0000H.<br>A pull-down resistor is internally connected to this pin. |
| Melody | MD | 63 | 66 | 81 | 91 | O | Melody output pin (non-inverted output) |
| | MDB | 64 | 67 | 82 | 92 | O | Melody output pin (inverted output) |
| Port | P0.0/INT5 | — | 86 | — | 110 | I | 4-bit input ports.<br>Pull-up resistor input, pull-down resistor input, or high-impedance input is selectable for each bit.<br>Applied to the ML63189B only. |
| | P0.1/INT5 | | 87 | | 111 | | |
| | P0.2/INT5 | | 88 | | 112 | | |
| | P0.3/INT5 | | 89 | | 113 | | |
| | P9.0 | — | 82 | — | 106 | I/O | 4-bit input-output ports.<br>In input mode, pull-up resistor input, pull-down resistor input, or high-impedance input is selectable for each bit.<br>In output mode, P-channel open drain output, N-channel open drain output, CMOS output, or high-impedance output is selectable for each bit.<br>P9.0 to P9.3 and PA.0 to PA.3 are applied to the ML63189B only. |
| | P9.1 | | 83 | | 107 | | |
| | P9.2 | | 84 | | 108 | | |
| | P9.3 | | 85 | | 109 | | |
| | PA.0 | — | 78 | — | 102 | I/O | |
| | PA.1 | | 79 | | 103 | | |
| | PA.2 | | 80 | | 104 | | |
| | PA.3 | | 81 | | 105 | | |
| | PB.0/INT0/ TM0CAP/ TM0OVF | 75 | 74 | 88 | 98 | I/O | |
| | PB.1/INT0/ TM1CAP/ TM1OVF | 76 | 75 | 89 | 99 | | |
| | PB.2/INT0/T02CK | 77 | 76 | 90 | 100 | | |
| | PB.3/INT0/T13CK | 78 | 77 | 91 | 101 | | |
| | PE.0/SIN | 71 | 70 | 84 | 94 | I/O | |
| | PE.1/SOUT | 72 | 71 | 85 | 95 | | |
| | PE.2/SCLK | 73 | 72 | 86 | 96 | | |
| | PE.3/INT2 | 74 | 73 | 87 | 97 | | |

**Table 1 Pin Descriptions (Basic Functions) (continued)**

| Function | Symbol | Pin No. | | Pad No. | | Type | Description |
|---|---|---|---|---|---|---|---|
| | | ML63187 | ML63189B | ML63187 | ML63189B | | |
| LCD | COM1 | 79 | 90 | 92 | 114 | O | LCD common signal output pins |
| | COM2 | 80 | 91 | 93 | 115 | | |
| | COM3 | 81 | 92 | 94 | 116 | | |
| | COM4 | 82 | 93 | 95 | 117 | | |
| | COM5 | 83 | 94 | 96 | 118 | | |
| | COM6 | 84 | 95 | 97 | 119 | | |
| | COM7 | 85 | 96 | 98 | 120 | | |
| | COM8 | 86 | 97 | 99 | 121 | | |
| | COM9 | 31 | 36 | 53 | 63 | | |
| | COM10 | 32 | 37 | 54 | 64 | | |
| | COM11 | 33 | 39 | 55 | 65 | | |
| | COM12 | 34 | 40 | 56 | 66 | | |
| | COM13 | 39 | 41 | 57 | 67 | | |
| | COM14 | 40 | 42 | 58 | 68 | | |
| | COM15 | 41 | 43 | 59 | 69 | | |
| | COM16 | 42 | 44 | 60 | 70 | | |
| | SEG0 | 87 | 98 | 100 | 122 | O | LCD segment signal output pins |
| | SEG1 | 88 | 99 | 101 | 123 | | |
| | SEG2 | 89 | 100 | 102 | 1 | | |
| | SEG3 | 90 | 101 | 103 | 2 | | |
| | SEG4 | 91 | 103 | 104 | 3 | | |
| | SEG5 | 92 | 104 | 105 | 4 | | |
| | SEG6 | 93 | 105 | 106 | 5 | | |
| | SEG7 | 94 | 106 | 107 | 6 | | |
| | SEG8 | 95 | 107 | 108 | 7 | | |
| | SEG9 | 96 | 108 | 109 | 8 | | |
| | SEG10 | 97 | 109 | 110 | 9 | | |
| | SEG11 | 98 | 110 | 111 | 10 | | |
| | SEG12 | 103 | 111 | 1 | 11 | | |
| | SEG13 | 104 | 112 | 2 | 12 | | |
| | SEG14 | 105 | 113 | 3 | 13 | | |
| | SEG15 | 106 | 114 | 4 | 14 | | |
| | SEG16 | 107 | 115 | 5 | 15 | | |
| | SEG17 | 108 | 116 | 6 | 16 | | |
| | SEG18 | 109 | 117 | 7 | 17 | | |
| | SEG19 | 110 | 118 | 8 | 18 | | |
| | SEG20 | 111 | 119 | 9 | 19 | | |
| | SEG21 | 112 | 120 | 10 | 20 | | |
| | SEG22 | 113 | 121 | 11 | 21 | | |
| | SEG23 | 114 | 122 | 12 | 22 | | |
| | SEG24 | 115 | 123 | 13 | 23 | | |

**Table 1 Pin Descriptions (Basic Functions) (continued)**

| Function | Symbol | Pin No. | | Pad No. | | Type | Description |
|---|---|---|---|---|---|---|---|
| | | ML63187 | ML63189B | ML63187 | ML63189B | | |
| LCD | SEG25 | 116 | 124 | 14 | 24 | O | LCD segment signal output pins |
| | SEG26 | 117 | 125 | 15 | 25 | | |
| | SEG27 | 118 | 126 | 16 | 26 | | |
| | SEG28 | 119 | 127 | 17 | 27 | | |
| | SEG29 | 120 | 128 | 18 | 28 | | |
| | SEG30 | 121 | 2 | 19 | 29 | | |
| | SEG31 | 122 | 3 | 20 | 30 | | |
| | SEG32 | 123 | 4 | 21 | 31 | | |
| | SEG33 | 124 | 5 | 22 | 32 | | |
| | SEG34 | 125 | 6 | 23 | 33 | | |
| | SEG35 | 126 | 7 | 24 | 34 | | |
| | SEG36 | 127 | 8 | 25 | 35 | | |
| | SEG37 | 128 | 9 | 26 | 36 | | |
| | SEG38 | 5 | 10 | 27 | 37 | | |
| | SEG39 | 6 | 11 | 28 | 38 | | |
| | SEG40 | 7 | 12 | 29 | 39 | | |
| | SEG41 | 8 | 13 | 30 | 40 | | |
| | SEG42 | 9 | 14 | 31 | 41 | | |
| | SEG43 | 10 | 15 | 32 | 42 | | |
| | SEG44 | 11 | 16 | 33 | 43 | | |
| | SEG45 | 12 | 17 | 34 | 44 | | |
| | SEG46 | 13 | 18 | 35 | 45 | | |
| | SEG47 | 14 | 19 | 36 | 46 | | |
| | SEG48 | 15 | 20 | 37 | 47 | | |
| | SEG49 | 16 | 21 | 38 | 48 | | |
| | SEG50 | 17 | 22 | 39 | 49 | | |
| | SEG51 | 18 | 23 | 40 | 50 | | |
| | SEG52 | 19 | 24 | 41 | 51 | | |
| | SEG53 | 20 | 25 | 42 | 52 | | |
| | SEG54 | 21 | 26 | 43 | 53 | | |
| | SEG55 | 22 | 27 | 44 | 54 | | |
| | SEG56 | 23 | 28 | 45 | 55 | | |
| | SEG57 | 24 | 29 | 46 | 56 | | |
| | SEG58 | 25 | 30 | 47 | 57 | | |
| | SEG59 | 26 | 31 | 48 | 58 | | |
| | SEG60 | 27 | 32 | 49 | 59 | | |
| | SEG61 | 28 | 33 | 50 | 60 | | |
| | SEG62 | 29 | 34 | 51 | 61 | | |
| | SEG63 | 30 | 35 | 52 | 62 | | |

Table 2 shows the secondary functions of each pin of the ML63187/ML63189B.

**Table 2 Pin Descriptions (Secondary Functions)**

| Function | Symbol | Pin No. | | Pad No. | | Type | Description |
|---|---|---|---|---|---|---|---|
| | | ML63187 | ML63189B | ML63187 | ML63189B | | |
| External Interrupt | PB.0/INT0 | 75 | 74 | 88 | 98 | I | External 0 interrupt input pins.<br>The change of input signal level causes an interrupt to occur.<br>The Port B Interrupt Enable register (PBIE) enables or disables an interrupt for each bit. |
| | PB.1/INT0 | 76 | 75 | 89 | 99 | | |
| | PB.2/INT0 | 77 | 76 | 90 | 100 | | |
| | PB.3/INT0 | 78 | 77 | 91 | 101 | | |
| | PE.3/INT2 | 74 | 73 | 87 | 97 | I | External 2 interrupt input pin.<br>The change of input signal level causes an interrupt to occur. |
| | P0.0/INT5 | — | 86 | — | 110 | I | External 5 interrupt input pins.<br>The change of input signal level causes an interrupt to occur.<br>The Port 0 Interrupt Enable register (P0IE) enable or disable an interrupt for each bit.<br>Applied to the ML63189B only. |
| | P0.1/INT5 | | 87 | | 111 | | |
| | P0.2/INT5 | | 88 | | 112 | | |
| | P0.3/INT5 | | 89 | | 113 | | |

**Table 2 Pin Descriptions (Secondary Functions) (continued)**

| Function | Symbol | Pin No. | | Pad No. | | Type | Description |
|---|---|---|---|---|---|---|---|
| | | ML63187 | ML63189B | ML63187 | ML63189B | | |
| Capture | PB.0/TM0CAP | 75 | 74 | 88 | 98 | I | Timer 0 capture input pin. |
| | PB.1/TM1CAP | 76 | 75 | 89 | 99 | I | Timer 1 capture input pin. |
| Timer | PB.0/TM0OVF | 75 | 74 | 88 | 98 | O | Timer 0 overflow flag output pin. |
| | PB.1/TM1OVF | 76 | 75 | 89 | 99 | O | Timer 1 overflow flag output pin. |
| | PB.2/T02CK | 77 | 76 | 90 | 100 | I | External clock input pin for timer 0 and timer 2. |
| | PB.3/T13CK | 78 | 77 | 91 | 101 | I | External clock input pin for timer 1 and timer 3. |
| Shift Register | PE.0/SIN | 71 | 70 | 84 | 94 | I | Shift register receive data input pin. |
| | PE.1/SOUT | 72 | 71 | 85 | 95 | O | Shift register transmit data output pin. |
| | PE.2/SCLK | 73 | 72 | 86 | 96 | I/O | Shift register clock input-output pin.<br>Clock output when this device is used as a master processor.<br>Clock input when this device is used as a slave processor. |

## ABSOLUTE MAXIMUM RATINGS

($V_{SS}$ = 0 V)

| Parameter | Symbol | Condition | Rating | Unit |
|---|---|---|---|---|
| Power Supply Voltage 1 | $V_{DD1}$ | Ta = 25°C | –0.3 to +1.6 | V |
| Power Supply Voltage 2 | $V_{DD2}$ | Ta = 25°C | –0.3 to +2.9 | V |
| Power Supply Voltage 3 | $V_{DD3}$ | Ta = 25°C | –0.3 to +4.2 | V |
| Power Supply Voltage 4 | $V_{DD4}$ | Ta = 25°C | –0.3 to +5.5 | V |
| Power Supply Voltage 5 | $V_{DD5}$ | Ta = 25°C | –0.3 to +6.8 | V |
| Power Supply Voltage 6 | $V_{DD}$ | Ta = 25°C | –0.3 to +6.0 | V |
| Power Supply Voltage 7 | $V_{DDI}$ | Ta = 25°C | –0.3 to +6.0 | V |
| Power Supply Voltage 8 | $V_{DDH}$ | Ta = 25°C | –0.3 to +6.0 | V |
| Power Supply Voltage 9 | $V_{DDL}$ | Ta = 25°C | –0.3 to +6.0 | V |
| Input Voltage 1 | $V_{IN1}$ | $V_{DD}$ Input, Ta = 25°C | –0.3 to $V_{DD}$ + 0.3 | V |
| Input Voltage 2 | $V_{IN2}$ | $V_{DDI}$ Input, Ta = 25°C | –0.3 to $V_{DDI}$ + 0.3 | V |
| Output Voltage 1 | $V_{OUT1}$ | $V_{DD1}$ Output, Ta = 25°C | –0.3 to $V_{DD1}$ + 0.3 | V |
| Output Voltage 2 | $V_{OUT2}$ | $V_{DD2}$ Output, Ta = 25°C | –0.3 to $V_{DD2}$ + 0.3 | V |
| Output Voltage 3 | $V_{OUT3}$ | $V_{DD3}$ Output, Ta = 25°C | –0.3 to $V_{DD3}$ + 0.3 | V |
| Output Voltage 4 | $V_{OUT4}$ | $V_{DD4}$ Output, Ta = 25°C | –0.3 to $V_{DD4}$ + 0.3 | V |
| Output Voltage 5 | $V_{OUT5}$ | $V_{DD5}$ Output, Ta = 25°C | –0.3 to $V_{DD5}$ + 0.3 | V |
| Output Voltage 6 | $V_{OUT6}$ | $V_{DD}$ Output, Ta = 25°C | –0.3 to $V_{DD}$ + 0.3 | V |
| Output Voltage 7 | $V_{OUT7}$ | $V_{DDI}$ Output, Ta = 25°C | –0.3 to $V_{DDI}$ + 0.3 | V |
| Output Voltage 8 | $V_{OUT8}$ | $V_{DDH}$ Output, Ta = 25°C | –0.3 to $V_{DDH}$ + 0.3 | V |
| Storage Temperature | $T_{STG}$ | — | –55 to +150 | °C |

## RECOMMENDED OPERATING CONDITIONS

• When backup is used

($V_{SS}$ = 0 V)

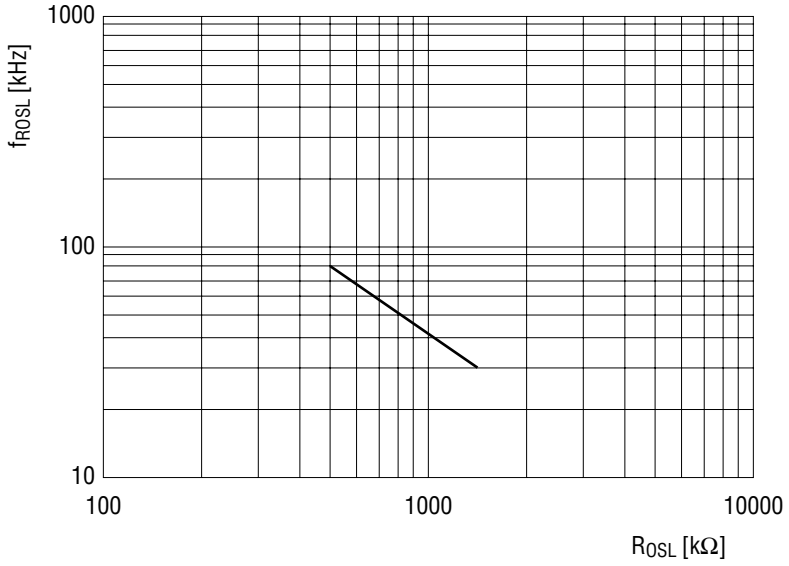
| Parameter | Symbol | Condition | | Range | Unit |
|---|---|---|---|---|---|
| Operating Temperature | $T_{op}$ | — | | –20 to +70 | °C |
| Operating Voltage | $V_{DD}$ | — | | 0.9 to 2.7 | V |
| | $V_{DDI}$ | — | | 0.9 to 5.5 | V |
| Crystal Oscillation Frequency | $f_{XT}$ | $C_G$ = 5 to 25 pF | | 32.768 to 76.8 | kHz |
| Low-speed RC Oscillation Frequency | $f_{ROSL}$ | $R_{OSL}$ = 1.5 MΩ | | 32 ±30% | kHz |
| | | $R_{OSL}$ = 700 kΩ | | 60 ±30% | |
| | | $R_{OSL}$ = 500 kΩ | | 80 ±30% | |
| Ceramic Oscillation Frequency | $f_{CM}$ | $V_{DD}$ = 0.9 to 1.2 V | | Not applied | Hz |
| | | $V_{DD}$ = 1.2 to 2.7 V | | 300k to 500k | |
| | | $V_{DD}$ = 1.5 to 2.7 V | | 200k to 1M | |
| High-speed RC Oscillation Frequency | $f_{ROSH}$ | $V_{DD}$ = 0.9 to 1.2 V | | Not applied | Hz |
| | | $V_{DD}$ = 1.2 to 2.7 V | $R_{OSH}$ = 400 kΩ | 200k ±30% | |
| | | | $R_{OSH}$ = 100 kΩ | 700k ±30% | |
| | | | $R_{OSH}$ = 75 kΩ | 1M ±30% | |

• When backup is not used

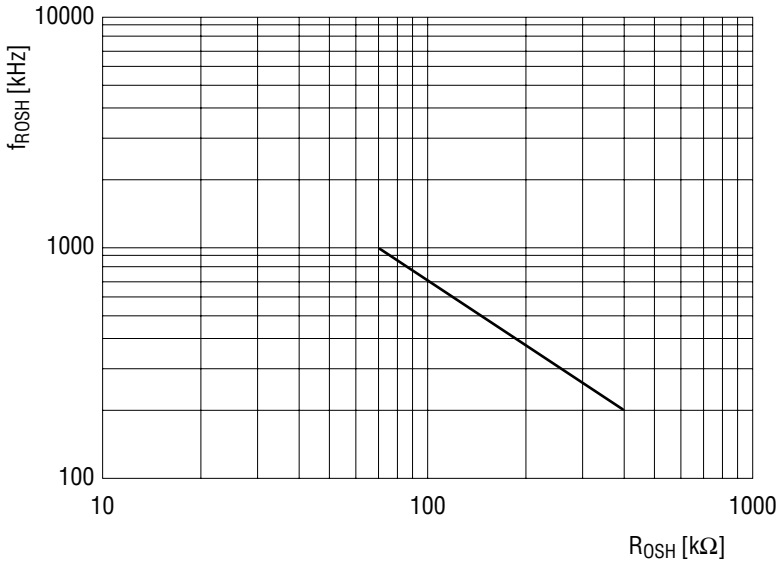
($V_{SS}$ = 0 V)

| Parameter | Symbol | Condition | | Range | Unit |
|---|---|---|---|---|---|
| Operating Temperature | $T_{op}$ | — | | –20 to +70 | °C |
| Operating Voltage | $V_{DD}$ | — | | 1.8 to 5.5 | V |
| | $V_{DDI}$ | — | | 1.8 to 5.5 | V |
| Crystal Oscillation Frequency | $f_{XT}$ | $C_G$ = 5 to 25 pF | | 32.768 to 76.8 | kHz |
| Low-speed RC Oscillation Frequency | $f_{ROSL}$ | $R_{OSL}$ = 1.5 MΩ | | 32 ±30% | kHz |
| | | $R_{OSL}$ = 700 kΩ | | 60 ±30% | |
| | | $R_{OSL}$ = 500 kΩ | | 80 ±30% | |
| Ceramic Oscillation Frequency | $f_{CM}$ | $V_{DD}$ = 1.8 to 5.5 V | | 200k to 2M | Hz |
| High-speed RC Oscillation Frequency | $f_{ROSH}$ | $V_{DD}$ = 1.8 to 5.5 V | $R_{OSH}$ = 100 kΩ | 700k ±30% | Hz |
| | | | $R_{OSH}$ = 75 kΩ | 1M ±30% | |
| | | | $R_{OSH}$ = 51 kΩ | 1.35M ±30% | |
| | | $V_{DD}$ = 1.8 to 3.5 V, $R_{OSH}$ = 30 kΩ | | 2M ±30% | |

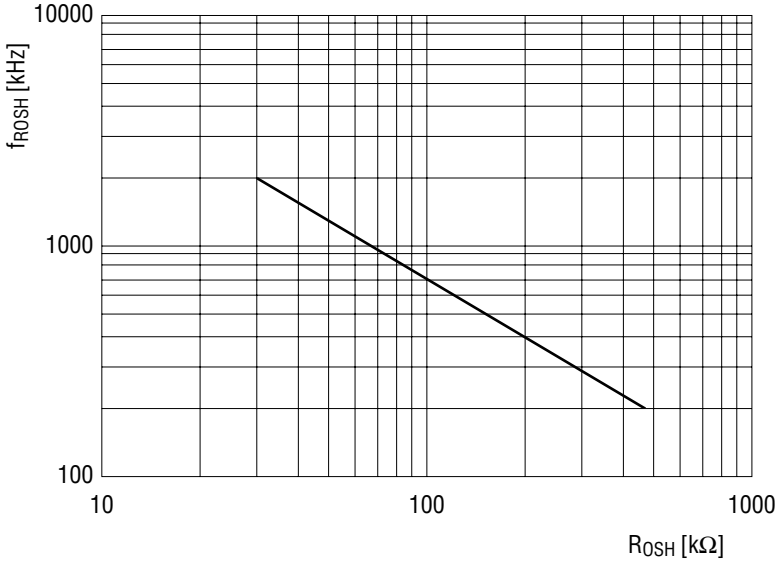
• Typical characteristics of low-speed RC oscillation
When backup is used/backup is not used ($V_{DD}$ = $V_{DDI}$ = 1.5 V/$V_{DD}$ = $V_{DDI}$ = 3.0 V)




• Typical characteristics of high-speed RC oscillation
When backup is used ($V_{DD}$ = $V_{DDI}$ = 1.5 V)



• Typical characteristics of high-speed RC oscillation
When backup is not used ($V_{DD}$ = $V_{DDI}$ = 3.0 V)



# ELECTRICAL CHARACTERISTICS

## DC Characteristics

($V_{DD}$ = $V_{DDI}$ = 0.9 to 5.5 V, $V_{SS}$ = 0 V, Ta = –20 to +70°C unless otherwise specified)

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit | Measuring Circuit |
|---|---|---|---|---|---|---|---|
| $V_{DD2}$ Voltage | $V_{DD2}$ | 1/5 bias, 1/4 bias (Ta = 25°C) | 1.7 | 1.8 | 1.9 | V | 1 |
| $V_{DD2}$ Voltage Temperature Deviation | $\Delta V_{DD2}$ | — | — | –4 | — | mV/°C | |
| $V_{DD1}$ Voltage | $V_{DD1}$ | 1/5 bias, 1/4 bias | Typ.– 0.1 | 1/2 × $V_{DD2}$ | Typ.+ 0.1 | V | |
| $V_{DD3}$ Voltage | $V_{DD3}$ | 1/5 bias | Typ.– 0.3 | 3/2 × $V_{DD2}$ | Typ.+ 0.3 | V | |
| | | 1/4 bias (connect $V_{DD3}$ and $V_{DD2}$) | Typ.– 0.2 | $V_{DD2}$ | Typ.+ 0.2 | | |
| $V_{DD4}$ Voltage | $V_{DD4}$ | 1/5 bias | Typ.– 0.4 | 2 × $V_{DD2}$ | Typ.+ 0.4 | V | |
| | | 1/4 bias | Typ.– 0.3 | 3/2 × $V_{DD2}$ | Typ.+ 0.3 | | |
| $V_{DD5}$ Voltage | $V_{DD5}$ | 1/5 bias | Typ.– 0.5 | 5/2 × $V_{DD2}$ | Typ.+ 0.5 | V | |
| | | 1/4 bias | Typ.– 0.4 | 2 × $V_{DD2}$ | Typ.+ 0.4 | | |
| $V_{DDH}$ Voltage (Backup used) | $V_{DDH}$ | High-speed clock oscillation stopped $V_{DD}$ = 1.5 V | 2.8 | — | 3.0 | V | |
| | | High-speed clock oscillation (Ceramic oscillation, 1 MHz) $V_{DD}$ = 1.5 V | 2.0 | — | 2.7 | V | |
| $V_{DDL}$ Voltage | $V_{DDL}$ | High-speed clock oscillation stopped | 1.0 | 1.5 | 2.0 | V | |
| | | High-speed clock oscillation ($V_{DD}$ = 1.2 to 5.5 V) | 1.2 | — | 5.5 | V | |
| Crystal Oscillation Start Voltage | $V_{STA}$ | Oscillation start time: within 5 seconds | 1.2 | — | — | V | |
| Crystal Oscillation Hold Voltage | $V_{HOLD}$ | Backup | 0.9 | — | — | V | |
| | | Backup not used | 1.7 | — | — | V | |
| Crystal Oscillation Stop Detect Time | $T_{STOP}$ | — | 0.1 | — | 5.0 | ms | |
| External Crystal Oscillator Capacitance | $C_G$ | — | 5 | — | 25 | pF | |
| Internal Crystal Oscillator Capacitance | $C_D$ | — | 20 | 25 | 30 | pF | |
| External Ceramic Oscillator Capacitance | $C_{L0, 1}$ | CSA2.00MG (Murata MFG.-make) used $V_{DD}$ = 3.0 V | — | 30 | — | pF | |
| Internal RC Oscillator Capacitance | $C_{OS}$ | — | 8 | 12 | 16 | pF | |
| POR Voltage | $V_{POR1}$ | $V_{DD}$ = 1.5 V | 0.0 | — | 0.4 | V | |
| | | $V_{DD}$ = 3.0 V | 0.0 | — | 0.7 | V | |
| Non-POR Voltage | $V_{POR2}$ | $V_{DD}$ = 1.5 V | 1.2 | — | 1.5 | V | |
| | | $V_{DD}$ = 3.0 V | 2.0 | — | 3.0 | V | |
| BLD Judgment Voltage | $V_{BLDC}$ | LD1 = 1, LD0 = 1, Ta = 25°C | 2.30 | 2.40 | 2.50 | V | — |
| | | LD1 = 1, LD0 = 0, Ta = 25°C | 1.70 | 1.80 | 1.90 | | |
| | | LD1 = 0, LD0 = 1, Ta = 25°C | 1.10 | 1.20 | 1.30 | | |
| | | LD1 = 0, LD0 = 0, Ta = 25°C | 0.95 | 1.05 | 1.15 | | |
| BLD Judgment Voltage Temperature Deviation | $\Delta V_{BLDC}$ | $V_{BLDC}$ = 2.40 V (LD1 = 1, LD0 = 1) | — | –3.5 | — | mV/°C | |
| | | $V_{BLDC}$ = 1.80 V (LD1 = 1, LD0 = 0) | — | –2.3 | — | | |
| | | $V_{BLDC}$ = 1.20 V (LD1 = 0, LD0 = 1) | — | –1.6 | — | | |
| | | $V_{BLDC}$ = 1.05 V (LD1 = 0, LD0 = 0) | — | –1.2 | — | | |

Notes: 1. "$T_{STOP}$" indicates that if the crystal oscillator stops over the value of $T_{STOP}$, the system reset occurs.
2. "POR" denotes Power On Reset.
3. "$V_{POR1}$" indicates that POR occurs when $V_{DD}$ falls from $V_{DD}$ to $V_{POR1}$ and again rises up to $V_{DD}$.
4. "$V_{POR2}$" indicates that POR does not occur when $V_{DD}$ falls from $V_{DD}$ to $V_{POR2}$ and again rises up to $V_{DD}$.

## DC Characteristics (continued)

• When backup is used

($V_{DD}$ = $V_{DDI}$ = 1.5 V, $V_{SS}$ = 0 V, 1/5 bias, Ta = –20 to +70°C unless otherwise specified)

| Parameter | Symbol | Condition | | Min. | Typ. | Max. | Unit | Measuring Circuit |
|---|---|---|---|---|---|---|---|---|
| Supply Current 1 | $I_{DD1}$ | CPU is in HALT state. (High-speed clock oscillation stopped) | Ta = –20 to +50°C | — | 5 | 6.5 | µA | 1 |
| | | | Ta = –20 to +70°C | — | 5 | 10 | | |
| Supply Current 2 | $I_{DD2}$ | CPU is in HALT state. LCD is in Power Down mode. (High-speed clock oscillation stopped) | Ta = –20 to +50°C | — | 4 | 5 | µA | |
| | | | Ta = –20 to +70°C | — | 4 | 8 | | |
| Supply Current 3 | $I_{DD3}$ | CPU is in operation at low-speed oscillation. (High-speed clock oscillation stopped) | Ta = –20 to +50°C | — | 16 | 18 | µA | |
| | | | Ta = –20 to +70°C | — | 16 | 20 | µA | |
| Supply Current 4 | $I_{DD4}$ | CPU is in operation at high-speed oscillation (RC oscillation, $R_{OSH}$ = 100 kΩ) | | — | 800 | 1000 | µA | |
| Supply Current 5 | $I_{DD5}$ | CPU is in operation at high-speed oscillation (Ceramic oscillation, 1 MHz) | | — | 700 | 850 | µA | |

• When backup is not used

($V_{DD}$ = $V_{DDI}$ = 3.0 V, $V_{SS}$ = 0 V, 1/5 bias, Ta = –20 to +70°C unless otherwise specified)

| Parameter | Symbol | Condition | | Min. | Typ. | Max. | Unit | Measuring Circuit |
|---|---|---|---|---|---|---|---|---|
| Supply Current 1 | $I_{DD1}$ | CPU is in HALT state. (High-speed clock oscillation stopped) | Ta = –20 to +50°C | — | 2.2 | 3 | µA | 1 |
| | | | Ta = –20 to +70°C | — | 2.2 | 5 | | |
| Supply Current 2 | $I_{DD2}$ | CPU is in HALT state. LCD is in Power Down mode. (High-speed clock oscillation stopped) | Ta = –20 to +50°C | — | 1.8 | 2.5 | µA | |
| | | | Ta = –20 to +70°C | — | 1.8 | 4 | | |
| Supply Current 3 | $I_{DD3}$ | CPU is in operation at low-speed oscillation. (High-speed clock oscillation stopped) | Ta = –20 to +50°C | — | 7.5 | 9 | µA | |
| | | | Ta = –20 to +70°C | — | 7.5 | 12 | | |
| Supply Current 4 | $I_{DD4}$ | CPU is in operation at high-speed oscillation (RC oscillation, $R_{OSH}$ = 100 kΩ) | | — | 550 | 700 | µA | |
| Supply Current 5 | $I_{DD5}$ | CPU is in operation at high-speed oscillation (Ceramic oscillation, 2 MHz) | | — | 850 | 1000 | µA | |

## DC Characteristics (continued)

($V_{DD}$ = $V_{DDI}$ = $V_{DDH}$ = 3.0 V, $V_{DD1}$ = 1.1 V, $V_{DD2}$ = 2.2 V, $V_{DD3}$ = 3.3 V, $V_{DD4}$ = 4.4 V, $V_{DD5}$ = 5.5 V, Ta = –20 to +70°C unless otherwise specified)

| Parameter | Symbol | Condition | | Min. | Typ. | Max. | Unit | Measuring Circuit |
|---|---|---|---|---|---|---|---|---|
| Output Current 1 (P9.0 to P9.3)* (PA.0 to PA.3)* (PB.0 to PB.3) (PE.0 to PE.3) | $I_{OH1}$ | $V_{OH1}$ = $V_{DDI}$ – 0.5 V | $V_{DDI}$ = 1.5 V | –2.5 | –1.4 | –0.4 | mA | |
| | | | $V_{DDI}$ = 3.0 V | –6.0 | –3.5 | –1.0 | mA | |
| | | | $V_{DDI}$ = 5.0 V | –8.5 | –5.0 | –1.5 | mA | |
| | $I_{OL1}$ | $V_{OL1}$ = 0.5 V | $V_{DDI}$ = 1.5 V | 0.4 | 1.4 | 2.5 | mA | |
| | | | $V_{DDI}$ = 3.0 V | 1.0 | 3.0 | 6.0 | mA | |
| | | | $V_{DDI}$ = 5.0 V | 1.5 | 3.7 | 8.5 | mA | |
| Output Current 2 (MD, MDB) | $I_{OH2}$ | $V_{OH2}$ = $V_{DD}$ – 0.7 V | $V_{DD}$ = 1.5 V | –4.0 | –2.0 | –0.5 | mA | |
| | | | $V_{DD}$ = 3.0 V | –11.0 | –6.0 | –2.0 | mA | |
| | | | $V_{DD}$ = $V_{DDH}$ = 5.0 V | –14.0 | –9.0 | –4.0 | mA | |
| | $I_{OL2}$ | $V_{OL2}$ = 0.7 V | $V_{DD}$ = 1.5 V | 0.5 | 2.0 | 4.0 | mA | |
| | | | $V_{DD}$ = 3.0 V | 2.0 | 5.5 | 11.0 | mA | |
| | | | $V_{DD}$ = $V_{DDH}$ = 5.0 V | 4.0 | 7.0 | 14.0 | mA | |
| Output Current 3 (SEG0 to SEG63) (COM1 to COM16) | $I_{OH3}$ | $V_{OH3}$ = $V_{DD5}$ – 0.2 V ($V_{DD5}$ level) | | — | — | –4 | µA | 2 |
| | $I_{OHM3}$ | $V_{OHM3}$ = $V_{DD4}$ + 0.2 V ($V_{DD4}$ level) | | 4 | — | — | µA | |
| | $I_{OHM3S}$ | $V_{OHM3S}$ = $V_{DD4}$ – 0.2 V ($V_{DD4}$ level) | | — | — | –4 | µA | |
| | $I_{OMH3}$ | $V_{OMH3}$ = $V_{DD3}$ + 0.2 V ($V_{DD3}$ level) | | 4 | — | — | µA | |
| | $I_{OMH3S}$ | $V_{OMH3S}$ = $V_{DD3}$ – 0.2 V ($V_{DD3}$ level) | | — | — | –4 | µA | |
| | $I_{OML3}$ | $V_{OML3}$ = $V_{DD2}$ + 0.2 V ($V_{DD2}$ level) | | 4 | — | — | µA | |
| | $I_{OML3S}$ | $V_{OML3S}$ = $V_{DD2}$ – 0.2 V ($V_{DD2}$ level) | | — | — | –4 | µA | |
| | $I_{OLM3}$ | $V_{OLM3}$ = $V_{DD1}$ + 0.2 V ($V_{DD1}$ level) | | 4 | — | — | µA | |
| | $I_{OLM3S}$ | $V_{OLM3S}$ = $V_{DD1}$ – 0.2 V ($V_{DD1}$ level) | | — | — | –4 | µA | |
| | $I_{OL3}$ | $V_{OL3}$ = $V_{SS}$ + 0.2 V ($V_{SS}$ level) | | 4 | — | — | µA | |
| Output Current 4 (OSC1) | $I_{OH4R}$ | $V_{OH4R}$ = $V_{DDH}$ – 0.5 V (RC oscillation) | $V_{DD}$ = $V_{DDH}$ = 3.0 V | –2.5 | –1.3 | –0.25 | mA | |
| | | | $V_{DD}$ = $V_{DDH}$ = 5.0 V | –3.5 | –1.7 | –0.5 | mA | |
| | $I_{OL4R}$ | $V_{OL4R}$ = 0.5 V (RC oscillation) | $V_{DD}$ = $V_{DDH}$ = 3.0 V | 0.25 | 1.5 | 2.5 | mA | |
| | | | $V_{DD}$ = $V_{DDH}$ = 5.0 V | 0.5 | 1.8 | 3.5 | mA | |
| | $I_{OH4C}$ | $V_{OH4C}$ = $V_{DDH}$ – 0.5 V (ceramic oscillation) | $V_{DD}$ = $V_{DDH}$ = 3.0 V | –500 | –250 | –100 | µA | |
| | | | $V_{DD}$ = $V_{DDH}$ = 5.0 V | –800 | –350 | –200 | µA | |
| | $I_{OL4C}$ | $V_{OL4C}$ = 0.5 V (ceramic oscillation) | $V_{DD}$ = $V_{DDH}$ = 3.0 V | 200 | 500 | 800 | µA | |
| | | | $V_{DD}$ = $V_{DDH}$ = 5.0 V | 400 | 700 | 1000 | µA | |
| Output Leakage Current (P9.0 to P9.3)* (PA.0 to PA.3)* (PB.0 to PB.3) (PE.0 to PE.3) | $I_{OOH}$ | $V_{OH}$ = $V_{DDI}$ | | — | — | 0.3 | µA | |
| | $I_{OOL}$ | $V_{OL}$ = $V_{SS}$ | | –0.3 | — | — | µA | |

*: Applied to the ML63189B only.

## DC Characteristics (continued)

($V_{DD}$ = $V_{DDI}$ = $V_{DDH}$ = 3.0 V, $V_{DD1}$ = 1.1 V, $V_{DD2}$ = 2.2 V, $V_{DD3}$ = 3.3 V, $V_{DD4}$ = 4.4 V, $V_{DD5}$ = 5.5 V, Ta = –20 to +70°C unless otherwise specified)

| Parameter | Symbol | Condition | | Min. | Typ. | Max. | Unit | Measuring Circuit |
|---|---|---|---|---|---|---|---|---|
| Input Current 1 (P0.0 to P0.3)* (P9.0 to P9.3)* (PA.0 to PA.3)* (PB.0 to PB.3) (PE.0 to PE.3) | $I_{IH1}$ | $V_{IH1}$ = $V_{DDI}$ (when pulled down) | $V_{DDI}$ = 1.5 V | 2 | 20 | 45 | µA | 3 |
| | | | $V_{DDI}$ = 3.0 V | 30 | 120 | 260 | µA | |
| | | | $V_{DDI}$ = 5.0 V | 70 | 350 | 650 | µA | |
| | $I_{IL1}$ | $V_{IL1}$ = $V_{SS}$ (when pulled up) | $V_{DDI}$ = 1.5 V | –45 | –20 | –2 | µA | |
| | | | $V_{DDI}$ = 3.0 V | –260 | –120 | –30 | µA | |
| | | | $V_{DDI}$ = 5.0 V | –650 | –350 | –70 | µA | |
| | $I_{IH1Z}$ | $V_{IH1}$ = $V_{DDI}$ (in a high impedance state) | | 0.0 | — | 1.0 | µA | |
| | $I_{IL1Z}$ | $V_{IL1}$ = $V_{SS}$ (in a high impedance state) | | –1.0 | — | 0.0 | µA | |
| Input Current 2 (OSC0) | $I_{IL2}$ | $V_{IL2}$ = $V_{SS}$ (when pulled up) | $V_{DD}$ = $V_{DDH}$ = 3.0 V | –350 | –170 | –30 | µA | |
| | | | $V_{DD}$ = $V_{DDH}$ = 5.0 V | –750 | –450 | –200 | µA | |
| | $I_{IH2R}$ | $V_{IH2R}$ = $V_{DDH}$ (RC oscillation) | | 0.0 | — | 1.0 | µA | |
| | $I_{IL2R}$ | $V_{IL2R}$ = $V_{SS}$ (RC oscillation) | | –1.0 | — | 0.0 | µA | |
| | $I_{IH2C}$ | $V_{IH2C}$ = $V_{DDH}$ (ceramic oscillation) | $V_{DD}$ = $V_{DDH}$ = 3.0 V | 0.5 | 1.8 | 4.0 | µA | |
| | | | $V_{DD}$ = $V_{DDH}$ = 5.0 V | 3 | 6 | 10 | µA | |
| | $I_{IL2C}$ | $V_{IL2C}$ = $V_{SS}$ (ceramic oscillation) | $V_{DD}$ = $V_{DDH}$ = 3.0 V | –4.0 | –1.8 | –0.5 | µA | |
| | | | $V_{DD}$ = $V_{DDH}$ = 5.0 V | –10 | –6 | –3 | µA | |
| Input Current 3 (RESET) | $I_{IH3}$ | $V_{IH3}$ = $V_{DD}$ | $V_{DD}$ = 1.5 V | 10 | 180 | 350 | µA | |
| | | | $V_{DD}$ = 3.0 V | 150 | 1100 | 2400 | µA | |
| | | | $V_{DD}$ = $V_{DDH}$ = 5.0 V | 0.5 | 2.7 | 5.0 | mA | |
| | $I_{IL3}$ | $V_{IL3}$ = $V_{SS}$ | | –1.0 | — | 0.0 | µA | |
| Input Current 4 (TST1, TST2) | $I_{IH4}$ | $V_{IH4}$ = $V_{DD}$ | $V_{DD}$ = 1.5 V | 50 | 750 | 1500 | µA | |
| | | | $V_{DD}$ = 3.0 V | 0.5 | 3.0 | 5.5 | mA | |
| | | | $V_{DD}$ = $V_{DDH}$ = 5.0 V | 2.0 | 6.5 | 11.0 | mA | |
| | $I_{IL4}$ | $V_{IL4}$ = $V_{SS}$ | | –1.0 | — | 0.0 | µA | |

*: Applied to the ML63189B only.

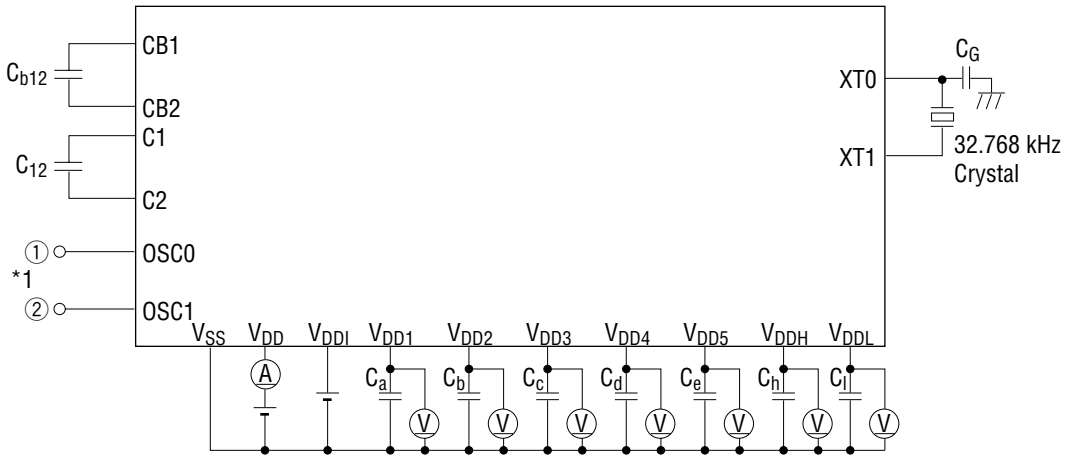
## DC Characteristics (continued)

($V_{DD}$ = $V_{DDI}$ = $V_{DDH}$ = 3.0 V, $V_{DD1}$ = 1.1 V, $V_{DD2}$ = 2.2 V, $V_{DD3}$ = 3.3 V, $V_{DD4}$ = 4.4 V, $V_{DD5}$ = 5.5 V, Ta = –20 to +70°C unless otherwise specified)

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit | Measuring Circuit |
|---|---|---|---|---|---|---|---|
| Input Voltage 1 (P0.0 to P0.3)* (P9.0 to P9.3)* (PA.0 to PA.3)* (PB.0 to PB.3) (PE.0 to PE.3) | $V_{IH1}$ | $V_{DDI}$ = 1.5 V | 1.2 | — | 1.5 | V | 4 |
| | | $V_{DDI}$ = 3.0 V | 2.4 | — | 3.0 | V | |
| | | $V_{DDI}$ = 5.0 V | 4.0 | — | 5.0 | V | |
| | $V_{IL1}$ | $V_{DDI}$ = 1.5 V | 0.0 | — | 0.3 | V | |
| | | $V_{DDI}$ = 3.0 V | 0.0 | — | 0.6 | V | |
| | | $V_{DDI}$ = 5.0 V | 0.0 | — | 1.0 | V | |
| Input Voltage 2 (OSC0) | $V_{IH2}$ | $V_{DD}$ = $V_{DDH}$ = 3.0 V | 2.4 | — | 3.0 | V | |
| | | $V_{DD}$ = $V_{DDH}$ = 5.0 V | 4.0 | — | 5.0 | V | |
| | $V_{IL2}$ | $V_{DD}$ = $V_{DDH}$ = 3.0 V | 0.0 | — | 0.6 | V | |
| | | $V_{DD}$ = $V_{DDH}$ = 5.0 V | 0.0 | — | 1.0 | V | |
| Input Voltage 3 (RESET, TST1, TST2) | $V_{IH3}$ | $V_{DD}$ = 1.5 V | 1.35 | — | 1.5 | V | |
| | | $V_{DD}$ = 3.0 V | 2.4 | — | 3.0 | V | |
| | | $V_{DD}$ = 5.0 V | 4.0 | — | 5.0 | V | |
| | $V_{IL3}$ | $V_{DD}$ = 1.5 V | 0.0 | — | 0.15 | V | |
| | | $V_{DD}$ = 3.0 V | 0.0 | — | 0.6 | V | |
| | | $V_{DD}$ = 5.0 V | 0.0 | — | 1.0 | V | |
| Hysteresis Width 1 (P0.0 to P0.3)* (P9.0 to P9.3)* (PA.0 to PA.3)* (PB.0 to PB.3) (PE.0 to PE.3) | $\Delta V_{T1}$ | $V_{DDI}$ = 1.5 V | 0.05 | 0.1 | 0.3 | V | |
| | | $V_{DDI}$ = 3.0 V | 0.2 | 0.5 | 1.0 | V | |
| | | $V_{DDI}$ = 5.0 V | 0.25 | 1.0 | 1.5 | V | |
| Hysteresis Width 2 (RESET, TST1, TST2) | $\Delta V_{T2}$ | $V_{DD}$ = 1.5 V | 0.05 | 0.1 | 0.3 | V | |
| | | $V_{DD}$ = 3.0 V | 0.2 | 0.5 | 1.0 | V | |
| | | $V_{DD}$ = 5.0 V | 0.25 | 1.0 | 1.5 | V | |
| Input Pin Capacitance (P0.0 to P0.3)* (P9.0 to P9.3)* (PA.0 to PA.3)* (PB.0 to PB.3) (PE.0 to PE.3) | $C_{IN}$ | — | — | — | 5 | pF | 1 |

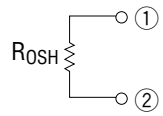
*: Applied to the ML63189B only.

## Measuring circuit 1

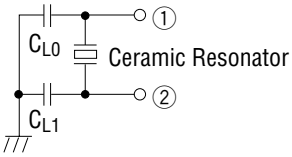



$C_a$, $C_b$, $C_c$, $C_d$, $C_e$, $C_l$, $C_{12}$ : 0.1 µF
$C_{b12}$, $C_h$ : 1 µF
$C_G$ : 15 pF
$C_{L0}$ : 30 pF
$C_{L1}$ : 30 pF
Ceramic Resonator : CSA2.00MG (2 MHz)
CSB1000J (1 MHz)
(Murata MFG.-make)

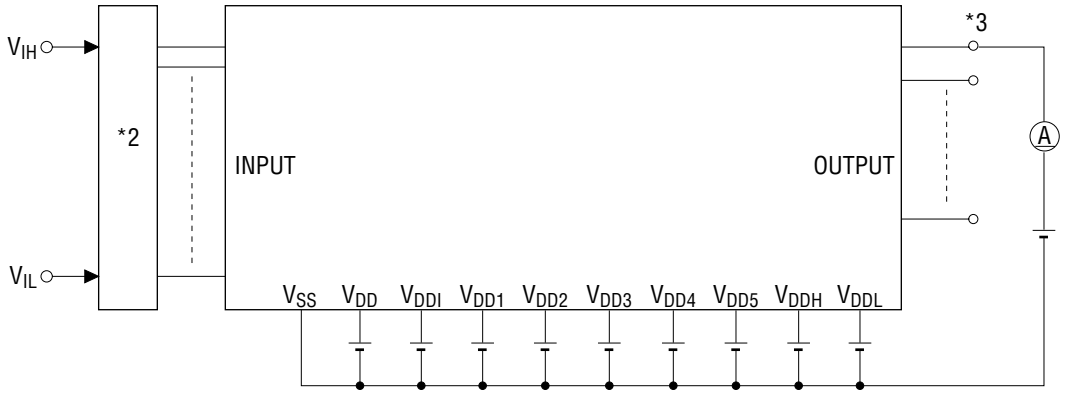
*1 RC Oscillator




Ceramic Oscillator

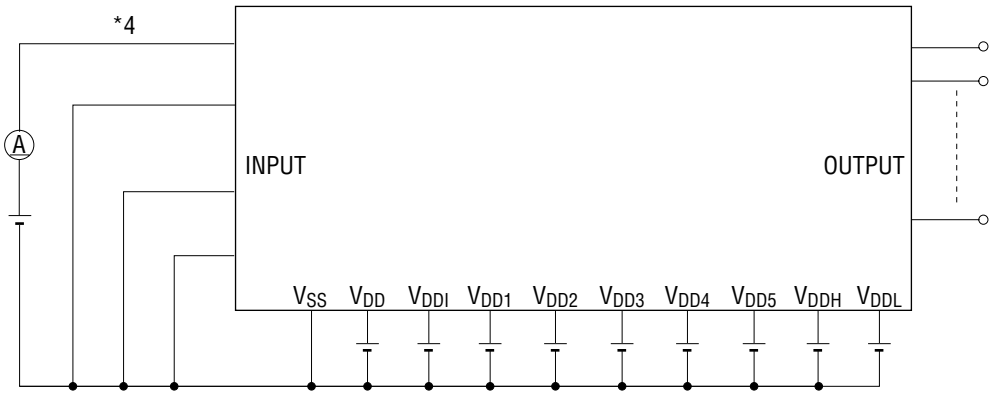



## Measuring circuit 2

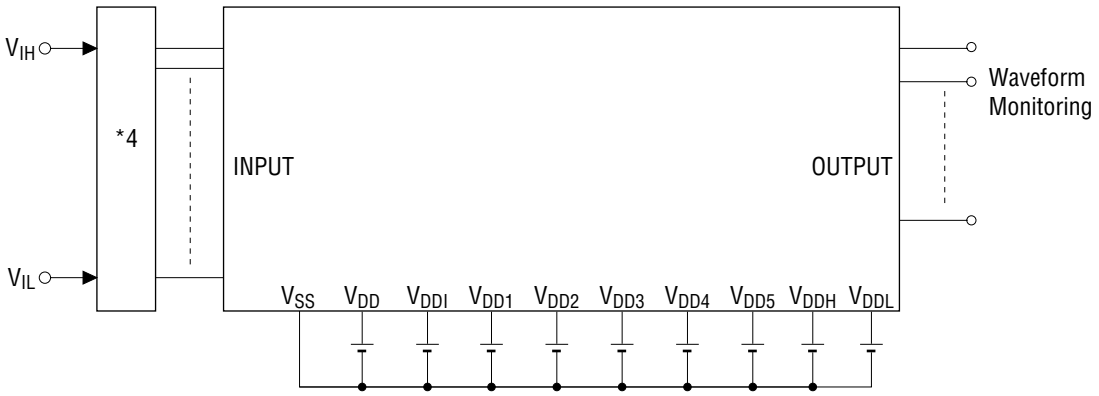



*2 Input logic circuit to determine the specified measuring conditions.
*3 Measured at the specified output pins.

### Measuring circuit 3




### Measuring circuit 4



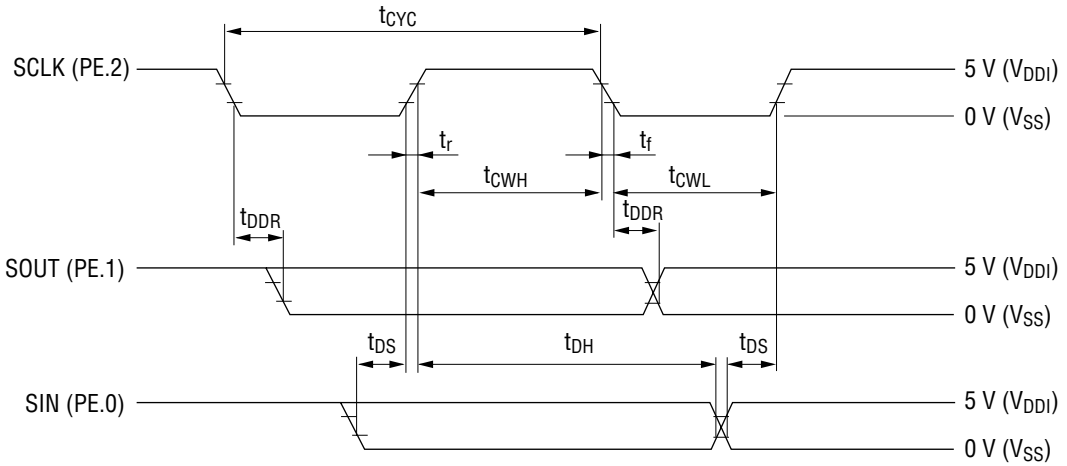

*4 Measured at the specified input pins.

## AC Characteristics (Serial Interface, Shift Register)

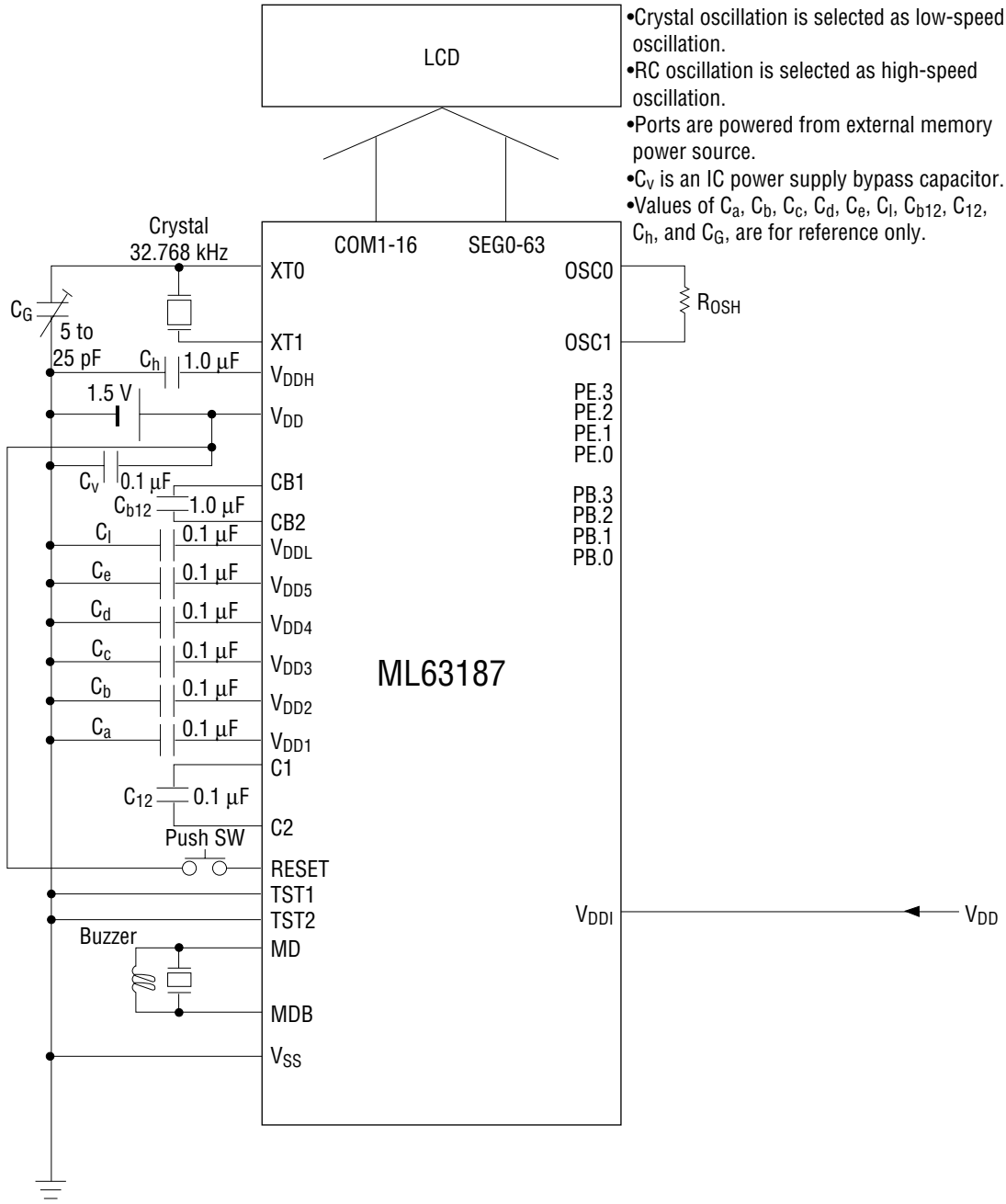
($V_{DD}$ = 0.9 to 5.5 V, $V_{DDH}$ = 1.8 to 5.5 V, $V_{SS}$ = 0 V, $V_{DDI}$ = 5.0 V, Ta = –20 to +70°C unless otherwise specified)

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| SCLK Input Fall Time | $t_f$ | — | — | — | 1.0 | µs |
| SCLK Input Rise Time | $t_r$ | — | — | — | 1.0 | µs |
| SCLK Input "L" Level Pulse Width | $t_{CWL}$ | — | 0.8 | — | — | µs |
| SCLK Input "H" Level Pulse Width | $t_{CWH}$ | — | 0.8 | — | — | µs |
| SCLK Input Cycle Time | $t_{CYC}$ | $V_{DDI}$ = 5 V to $V_{DD}$ | 1.8 | — | — | µs |
| SCLK Output Cycle Time | $t_{CYC1(O)}$ | CPU in operation state at 32.768 kHz | — | 30.5 | — | µs |
| | $t_{CYC2(O)}$ | CPU in operation at 2 MHz<br>$V_{DD}$ = $V_{DDH}$ = 1.8 V to 3.5 V | — | 0.5 | — | µs |
| SOUT Output Delay Time | $t_{DDR}$ | $C_l$ = 10 pF | — | — | 0.4 | µs |
| SIN Input Setup Time | $t_{DS}$ | — | 0.5 | — | — | µs |
| SIN Input Hold Time | $t_{DH}$ | — | 0.8 | — | — | µs |

AC characteristics timing
("H" level = 4.0 V, "L" level = 1.0 V)



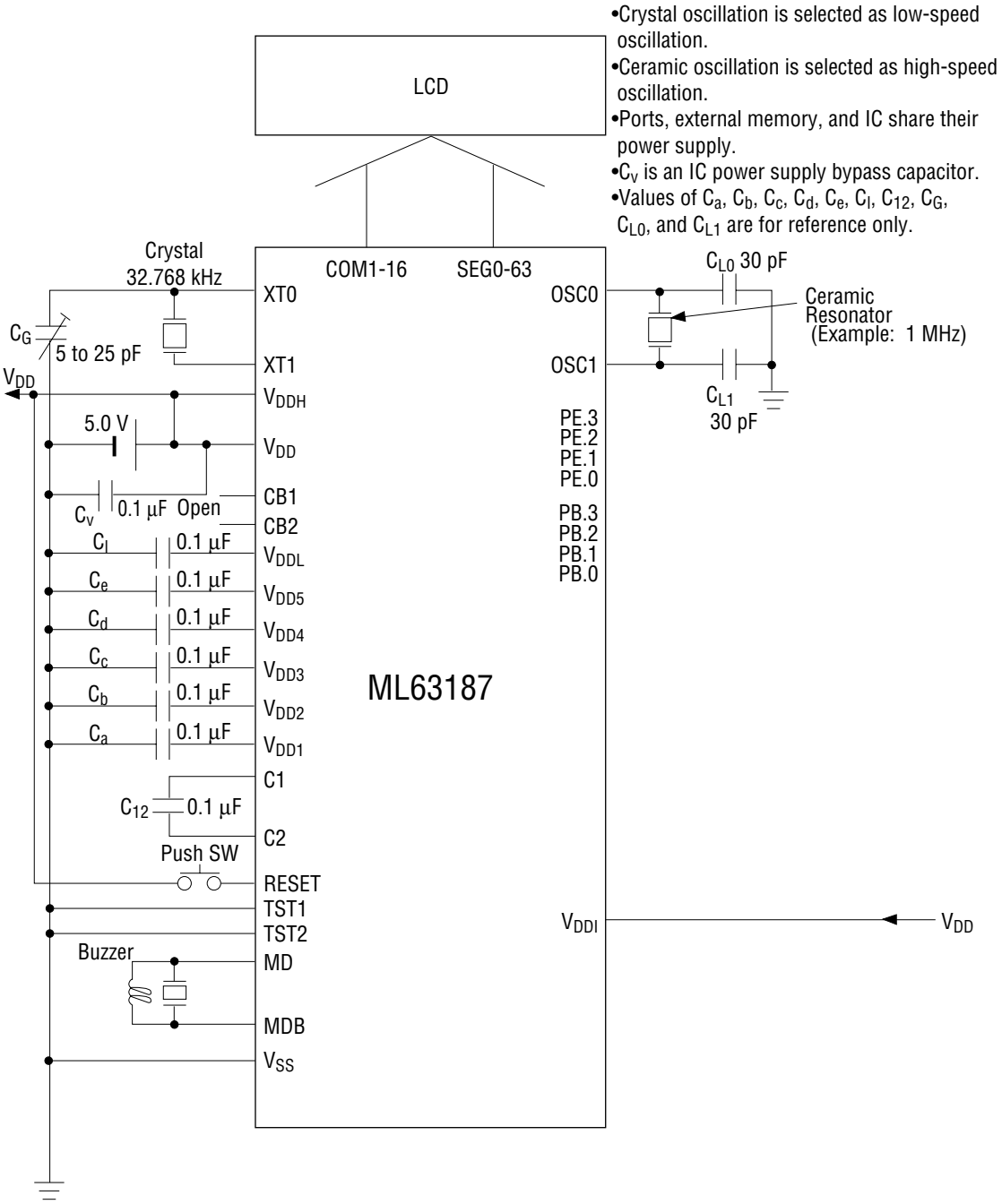
## APPLICATION CIRCUITS (ML63187)




Note: $V_{DDI}$ is the power supply pin for the input-output ports.
Be sure to connect the $V_{DDI}$ pin either to the positive power supply pin ($V_{DD}$) of this device or to the positive power supply pin of the external memory.

**Application Circuit Example with Power Supply Backup**

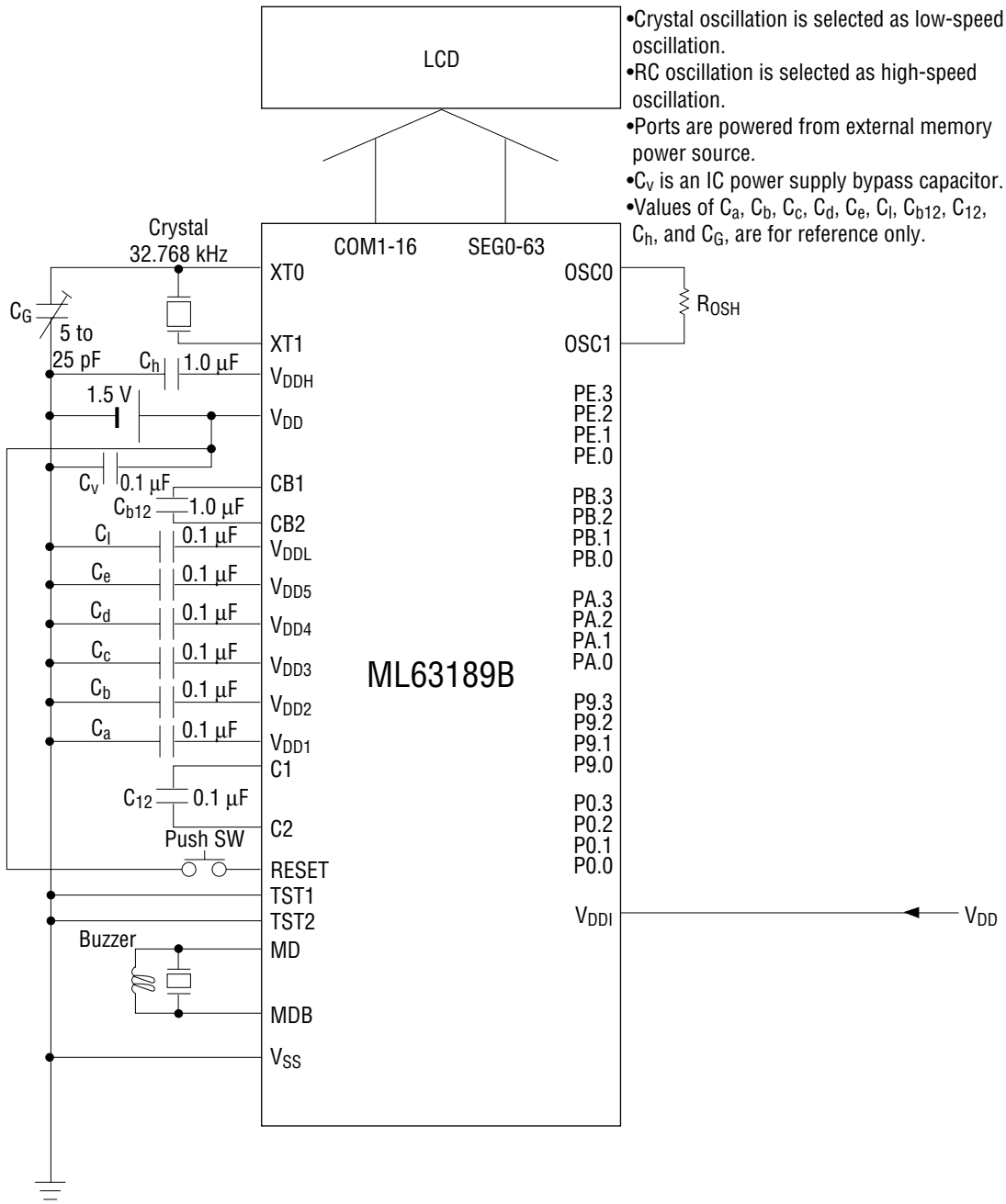
## APPLICATION CIRCUITS (ML63187)




Note: $V_{DDI}$ is the power supply pin for the input-output ports.
Be sure to connect the $V_{DDI}$ pin either to the positive power supply pin ($V_{DD}$) of this device or to the positive power supply pin of the external memory.

**Application Circuit Example with No Power Supply Backup**

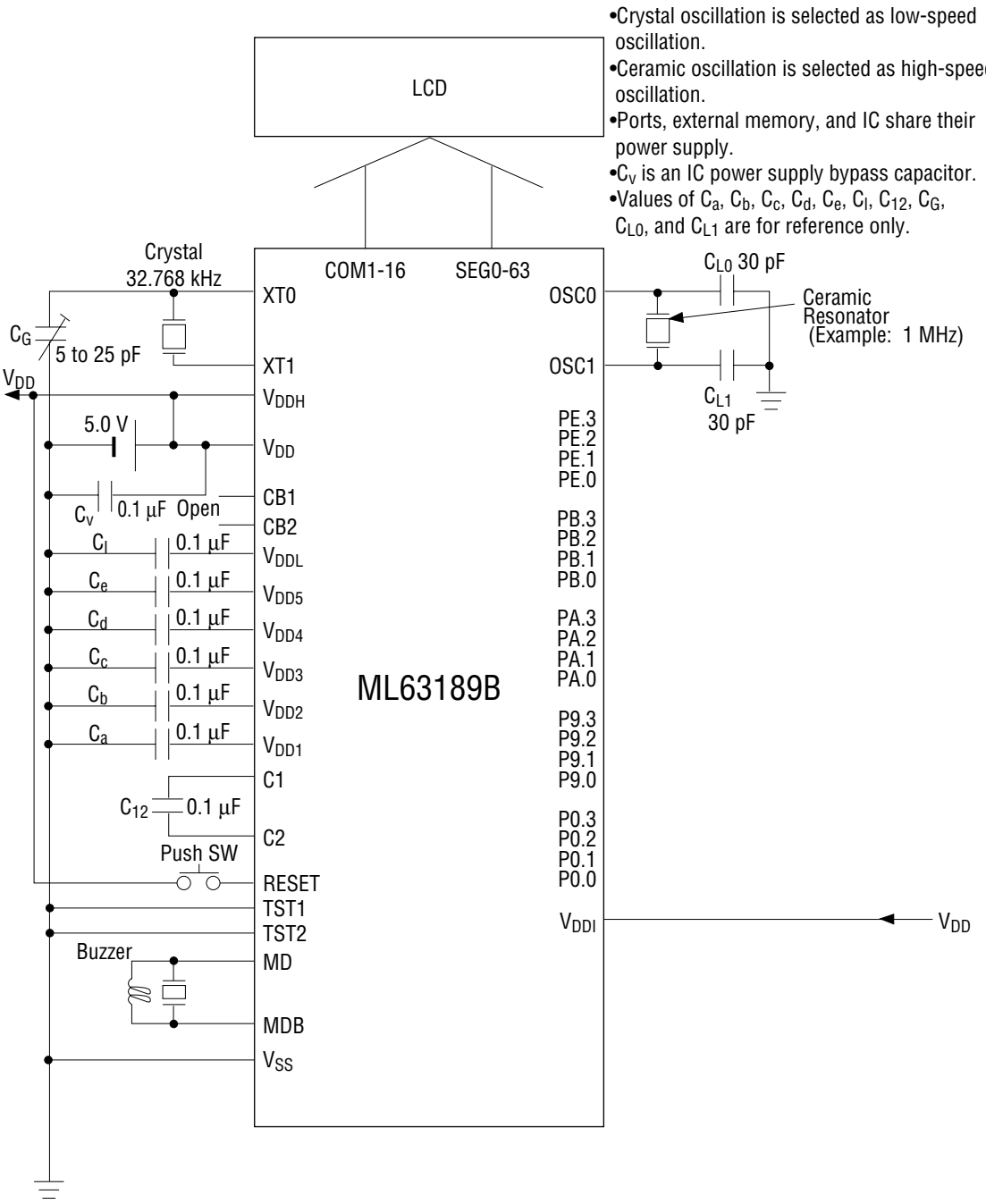
## APPLICATION CIRCUITS (ML63189B)




Note: $V_{DDI}$ is the power supply pin for the input and input-output ports.
Be sure to connect the $V_{DDI}$ pin either to the positive power supply pin ($V_{DD}$) of this device or to the positive power supply pin of the external memory.

**Application Circuit Example with Power Supply Backup**

## APPLICATION CIRCUITS (ML63189B)



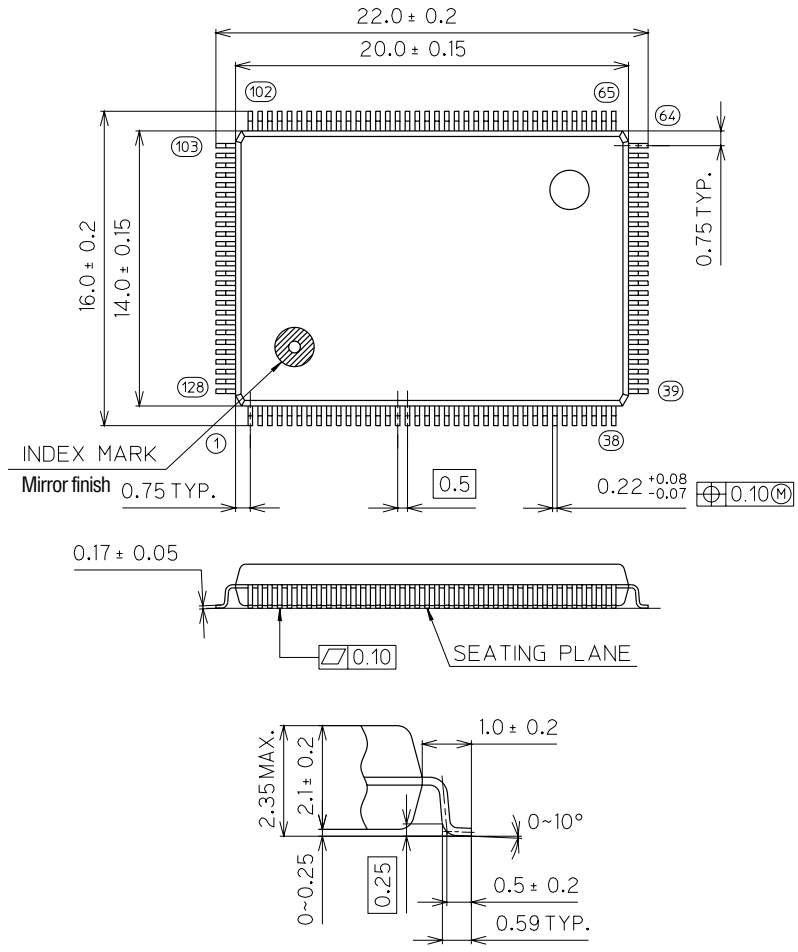

Note: $V_{DDI}$ is the power supply pin for the input and input-output ports.
Be sure to connect the $V_{DDI}$ pin either to the positive power supply pin ($V_{DD}$) of this device or to the positive power supply pin of the external memory.

**Application Circuit Example with No Power Supply Backup**

## PACKAGE DIMENSIONS

(Unit : mm)

QFP128-P-1420-0.50-K




| | |
|---|---|
| Package material | Epoxy resin |
| Lead frame material | 42 alloy |
| Pin treatment | Solder plating |
| Solder plate thickness | 5 μm or more |
| Package weight (g) | 1.19 TYP. |

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, TQFP, LQFP, SOJ, QFJ (PLCC), SHP, and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person on the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

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