National Semiconductor

December 10, 2007

LMH6739
Very Wideband, Low Distortion Triple Video Buffer

General Description

The LMH6739 is a very wideband, DC coupled monolithic selectable gain buffer designed specifically for ultra high resolution video systems as well as wide dynamic range systems requiring exceptional signal fidelity. Benefiting from National's current feedback architecture, the LMH6739 offers gains of −1, 1 and 2. At a gain of +2 the LMH6739 supports ultra high resolution video systems with a 400 MHz 2 V_{PP} 3 dB Bandwidth. With 12-bit distortion level through 30 MHz (R_L = 100Ω), 2.3nV/√Hz input referred noise, the LMH6739 is the ideal driver or buffer for high speed flash A/D and D/A converters. Wide dynamic range systems such as radar and communication receivers requiring a wideband amplifier offering exceptional signal purity will find the LMH6739's low input referred noise and low harmonic distortion make it an attractive solution. The LMH6739 is offered in a space saving SSOP package.

Features

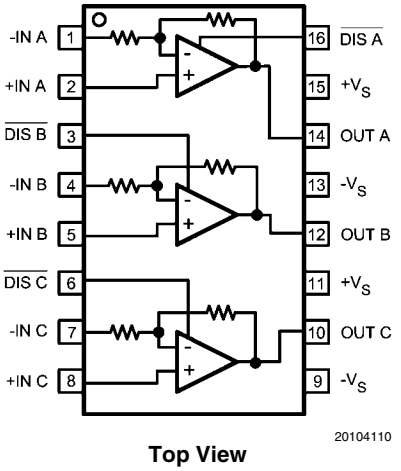
- 750 MHz −3 dB small signal bandwidth (A_V = +1)
- −85 dBc 3rd harmonic distortion (20 MHz)
- 2.3 nV/√Hz input noise voltage
- 3300 V/µs slew rate
- 32 mA supply current (10.6 mA per op amp)
- 90 mA linear output current
- 0.02/0.01 Diff. Gain/ Diff. Phase (R_L = 150Ω)
- 2mA shutdown current

Applications

- RGB video driver
- High resolution projectors
- Flash A/D driver
- D/A transimpedance buffer
- Wide dynamic range IF amp
- Radar/communication receivers
- DDS post-amps
- Wideband inverting summer
- Line driver

Connection Diagram

16-Pin SSOP



20104110

Top View

Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
16-Pin SSOP	LMH6739MQ	LH6739MQ	95 Units/Rail	MQA16
	LMH6739MQX		2.5k Units Tape and Reel	

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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 3)	
Human Body Model	2000V
Machine Model	200V
Supply Voltage ($V^+ - V^-$)	13.2V
I_{OUT}	(Note 4)
Common Mode Input Voltage	$\pm V_{CC}$
Maximum Junction Temperature	+150°C
Storage Temperature Range	−65°C to +150°C
Soldering Information	
Infrared or Convection (20 sec.)	235°C
Wave Soldering (10 sec.)	260°C
Storage Temperature Range	−65°C to +150°C

Operating Ratings (Note 1)

Temperature Range (Note 5)	−40°C to +85°C
Supply Voltage ($V^+ - V^-$)	8V to 12V
Thermal Resistance	

Package	**(θ_{JC})**	**(θ_{JA})**
16-Pin SSOP	36°C/W	120°C/W

Electrical Characteristics (Note 2)

T_A = 25°C, A_V = +2, V_{CC} = ±5V, R_L = 100Ω; unless otherwise specified.

Symbol	Parameter	Conditions	Min (Note 7)	Typ (Note 6)	Max (Note 7)	Units
Frequency Domain Performance						
UGBW	−3 dB Bandwidth	Unity Gain, V_{OUT} = 200 mV_{PP}		750		MHz
SSBW	−3 dB Bandwidth	V_{OUT} = 200 mV_{PP}		480		MHz
LSBW		V_{OUT} = 2 V_{PP}		400		
	0.1 dB Bandwidth	V_{OUT} = 2 V_{PP}		150		MHz
GFR2	Rolloff	@ 300 MHz, V_{OUT} = 2 V_{PP}		1.0		dB
Time Domain Response						
TRS	Rise and Fall Time	2V Step		0.9		ns
TRL	(10% to 90%)	5V Step		1.7		
SR	Slew Rate	5V Step		3300		V/µs
t_s	Settling Time to 0.1%	2V Step		10		ns
t_e	Enable Time	From $\overline{\text{Disable}}$ = rising edge.		7.3		ns
t_d	Disable Time	From $\overline{\text{Disable}}$ = falling edge.		4.5		ns
Distortion						
HD2L	2nd Harmonic Distortion	2 V_{PP}, 5 MHz		−80		dBc
HD2		2 V_{PP}, 20 MHz		−71		
HD2H		2 V_{PP}, 50 MHz		−55		
HD3L	3rd Harmonic Distortion	2 V_{PP}, 5 MHz		−90		dBc
HD3		2 V_{PP}, 20 MHz		−85		
HD3H		2 V_{PP}, 50 MHz		−65		
Equivalent Input Noise						
V_N	Non-Inverting Voltage	>1 MHz		2.3		$nV/\sqrt{Hz}$
I_{CN}	Inverting Current	>1 MHz		12		$pA/\sqrt{Hz}$
N_{CN}	Non-Inverting Current	>1 MHz		3		$pA/\sqrt{Hz}$
Video Performance						
DG	Differential Gain	4.43 MHz, R_L = 150Ω		.02		%
DP	Differential Phase	4.43 MHz, R_L = 150Ω		.01		degree
Static, DC Performance						
V_{OS}	Input Offset Voltage (Note 8)			0.5	±2.5 **±4.5**	mV
I_{BN}	Input Bias Current (Note 8)	Non-Inverting	−16 **−21**	−8	0 **+5**	µV
I_{BI}	Input Bias Current (Note 8)	Inverting		−2	±30 **±40**	µA

Symbol	Parameter	Conditions	Min (Note 7)	Typ (Note 6)	Max (Note 7)	Units
PSRR	Power Supply Rejection Ratio (Note 8)		50 **48.5**	53		dB
CMRR	Common Mode Rejection Ratio (Note 8)		46 **44**	50		dB
I_{CC}	Supply Current (Note 8)	All three amps Enabled, No Load		32	35 **40**	mA
	Supply Current Disabled V^+	$R_L = \infty$		1.9	2.2	mA
	Supply Current Disabled V^-	$R_L = \infty$		1.1	1.3	mA
	Internal Feedback & Gain Set Resistor Value		375	450	525	Ω
	Gain Error	$R_L = \infty$		0.2	±1.1	%
Miscellaneous Performance						
$R_{IN}+$	Non-Inverting Input Resistance			1000		kΩ
$C_{IN}+$	Non-Inverting Input Capacitance			.8		pF
$R_{IN}-$	Inverting Input Impedance	Output impedance of input buffer.		30		Ω
R_O	Output Impedance	DC		0.05		Ω
V_O	Output Voltage Range (Note 8)	$R_L = 100\Omega$	±3.25 **±3.1**	±3.5		V
		$R_L = \infty$	±3.65 **±3.5**	±3.8		
CMIR	Common Mode Input Range (Note 8)	CMRR > 40 dB	±1.9 **±1.7**	±2.0		V
I_O	Linear Output Current (Notes 4, 8)	V_{IN} = 0V, V_{OUT} < ±30 mV	80 **60**	90		mA
I_{SC}	Short Circuit Current (Note 9)	V_{IN} = 2V Output Shorted to Ground		160		mA
I_{IH}	Disable Pin Bias Current High	$\overline{\text{Disable}}$ Pin = V^+		10		µA
I_{IL}	Disable Pin Bias Current Low	$\overline{\text{Disable}}$ Pin = 0V		–350		µA
V_{DMAX}	Voltage for Disable	$\overline{\text{Disable}}$ Pin ≤ V_{DMAX}			0.8	V
V_{DMIM}	Voltage for Enable	$\overline{\text{Disable}}$ Pin ≥ V_{DMIN}	2.0			V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications, see the Electrical Characteristics tables.

Note 2: Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self heating where $T_J > T_A$. See Applications Information for information on temperature de-rating of this device. Min/Max ratings are based on product characterization and simulation. Individual parameters are tested as noted.

Note 3: Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC)

Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).

Note 4: The maximum output current (I_{OUT}) is determined by device power dissipation limitations. See the Power Dissipation section of the Application Information for more details.

Note 5: The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

Note 6: Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.

Note 7: Limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlations using the Statistical Quality Control (SQC) method.

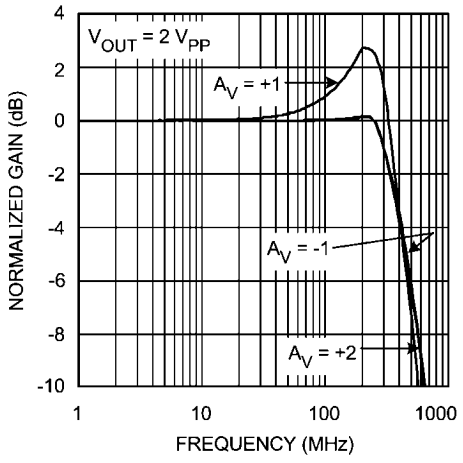
Note 8: Parameter 100% production tested at 25° C.

Note 9: Short circuit current should be limited in duration to no more than 10 seconds. See the Power Dissipation section of the Application Information for more details.

Typical Performance Characteristics

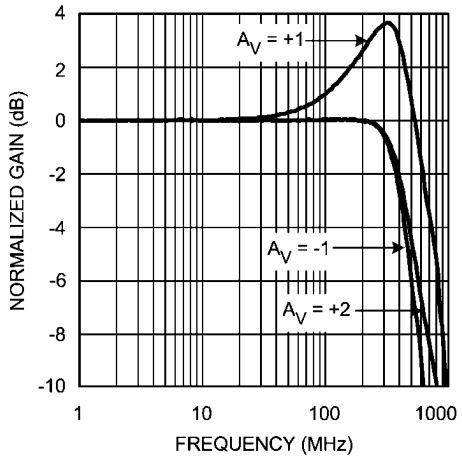
A_V = +2, V_{CC} = ±5V, R_L = 100Ω; unless otherwise specified).

Large Signal Frequency Response



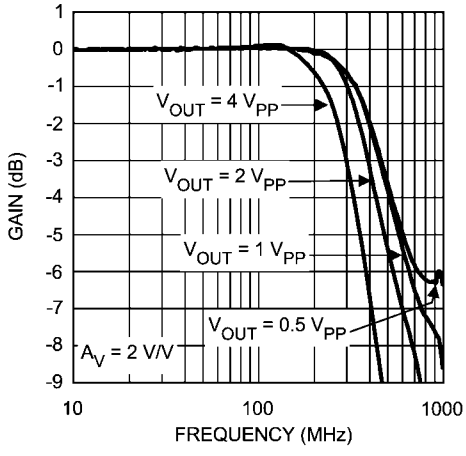
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Small Signal Frequency Response



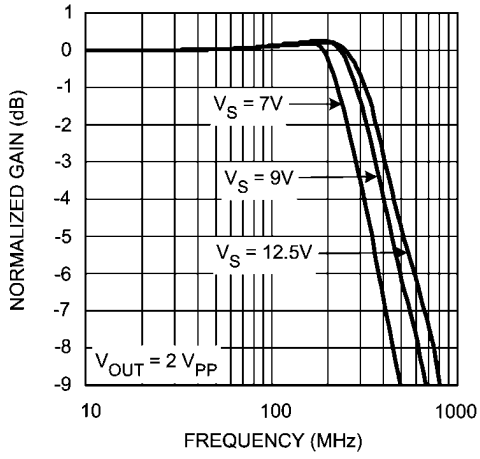
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Frequency Response vs. V_{OUT}



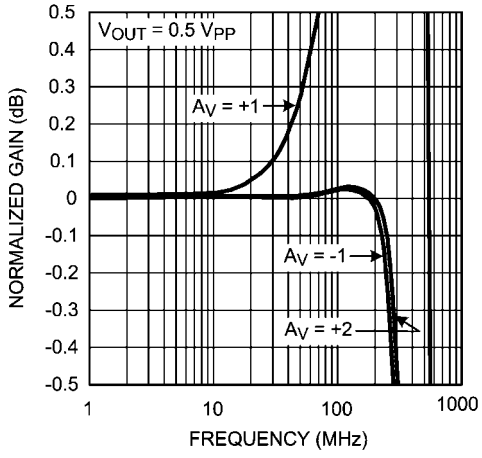
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Frequency Response vs. Supply Voltage



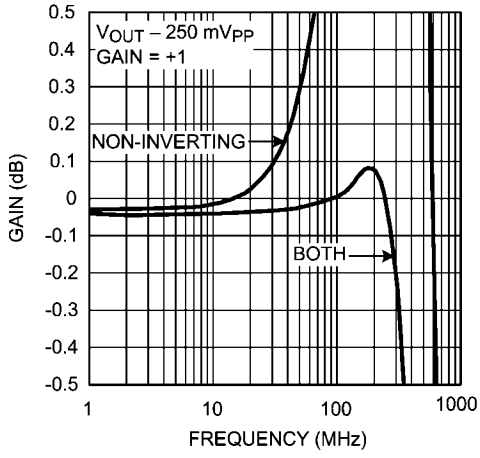
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Gain Flatness



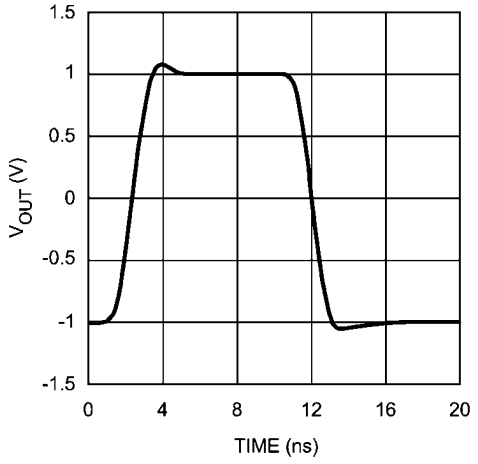
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Gain Flatness, Dual Input Buffer



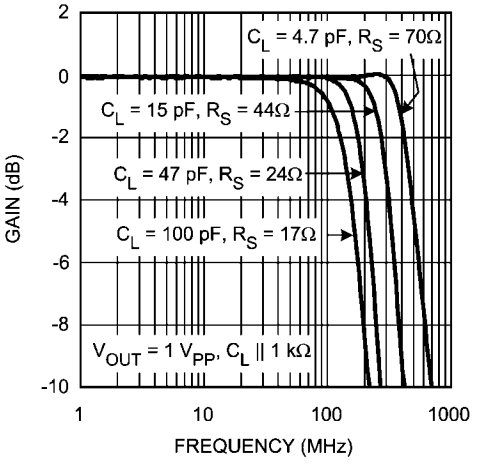
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Pulse Response



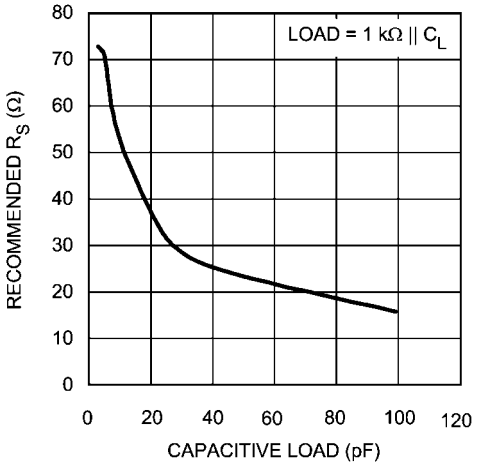
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Frequency Response vs. Capacitive Load



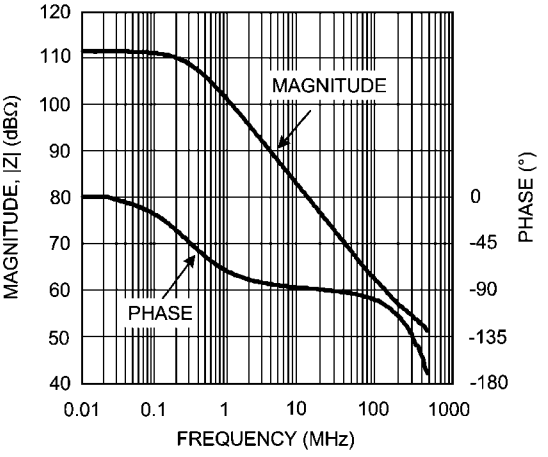
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Series Output Resistance vs. Capacitive Load



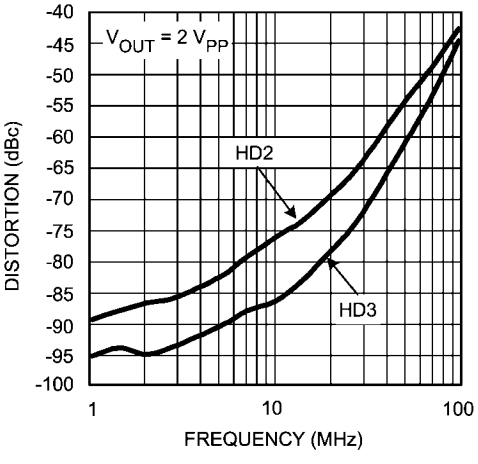
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Open Loop Gain and Phase



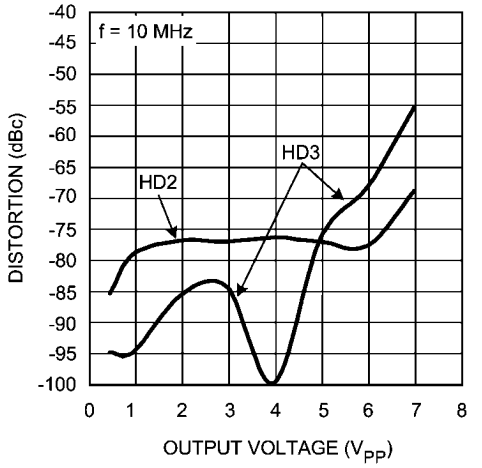
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Distortion vs. Frequency



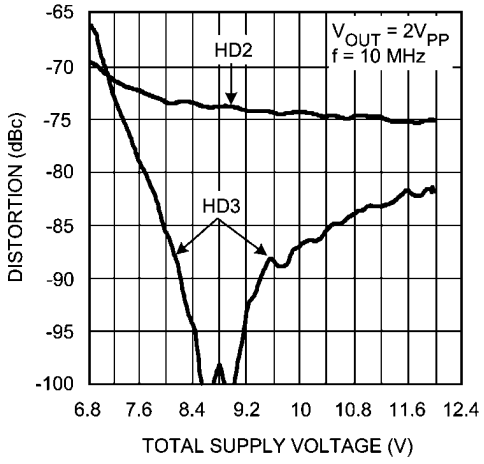
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10 MHz HD vs. Output Level



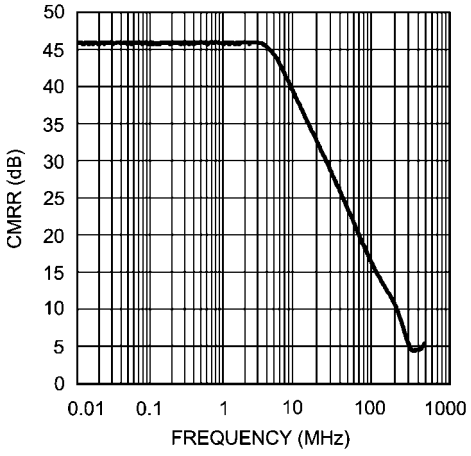
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Distortion vs. Supply Voltage



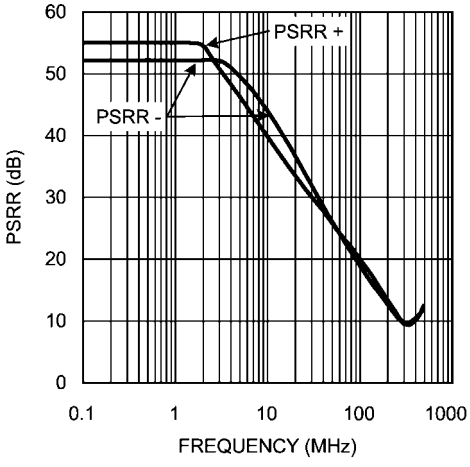
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CMRR vs. Frequency



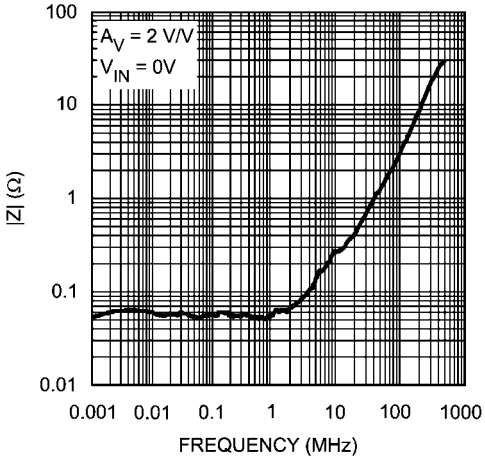
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PSRR vs. Frequency



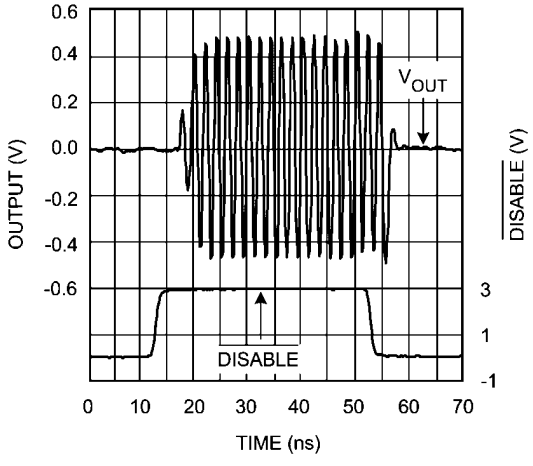
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Closed Loop Output Impedance |Z|



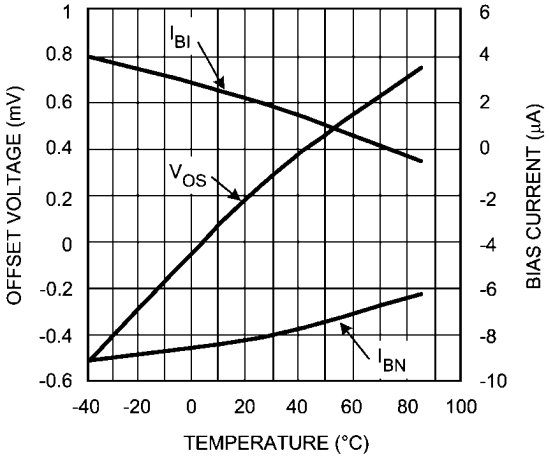
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Disable Timing



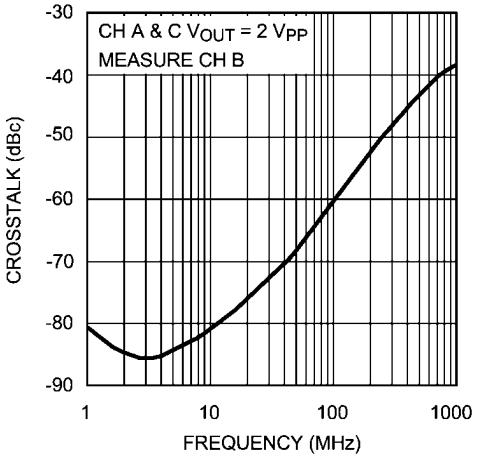
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DC Errors vs. Temperature



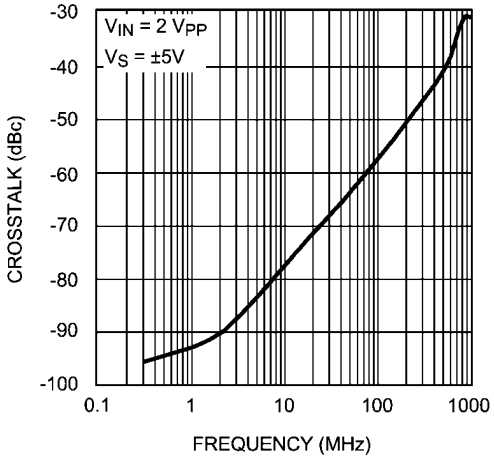
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Crosstalk vs. Frequency



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Disabled Channel Isolation vs. Frequency



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Application Information

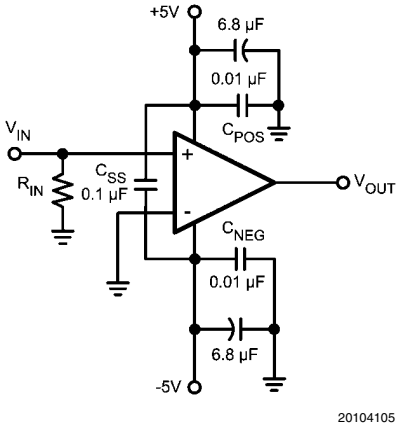


FIGURE 1. Recommended Non-Inverting Gain Circuit, Gain = +2

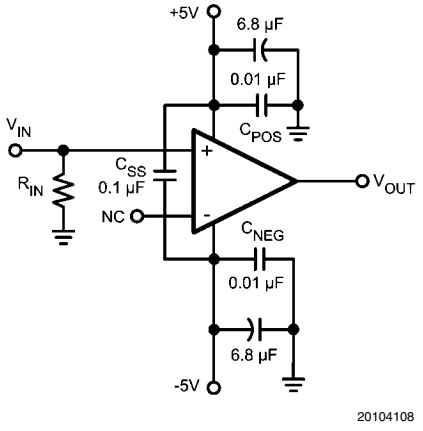


FIGURE 2. Recommended Non-Inverting Gain Circuit, Gain +1

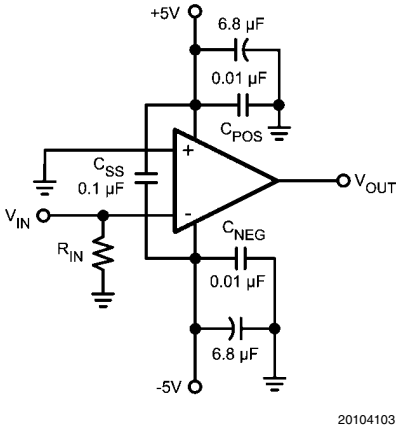


FIGURE 3. Recommended Inverting Gain Circuit, Gain = –1

GENERAL INFORMATION

The LMH6739 is a high speed current feedback selectable gain buffer (SGB), optimized for very high speed and low distortion. With its internal feedback and gain-setting resistors the LMH6739 offers excellent AC performance while simplifying board layout and minimizing the affects of layout related parasitic components. The LMH6739 has no internal ground reference so single or split supply configurations are both equally useful.

SETTING THE CLOSED LOOP GAIN

The LMH6739 is a current feedback amplifier with on-chip $R_F = R_G = 450\Omega$. As such it can be configured with an $A_V = +2$, $A_V = +1$, or an $A_V = -1$ by connecting pins 3 and 4 as described in the chart below.

GAIN A_V	INPUT CONNECTIONS	
	Non-Inverting	Inverting
–1 V/V	Ground	Input Signal
+1 V/V	Input Signal	NC (Open)
+2 V/V	Input Signal	Ground

The gain of the LMH6739 is accurate to ±1% and stable over temperature. The internal gain setting resistors, R_F and R_G, match very well. However, over process and temperature their absolute value will change. Using external resistors in series with R_G to change the gain will result in poor gain accuracy over temperature and from part to part.

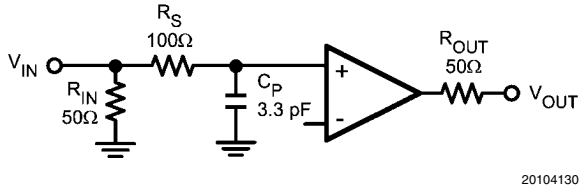


FIGURE 4. Correction for Unity Gain Peaking

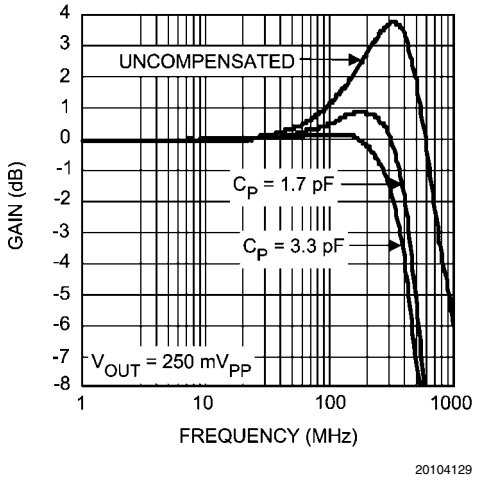


FIGURE 5. Frequency Response for Circuit in *Figure 4*

UNITY GAIN COMPENSATION

With a current feedback Selectable Gain Buffer like the LMH6739, the feedback resistor is a compromise between the value needed for stability at unity gain and the optimized value used at a gain of two. The result of this compromise is substantial peaking at unity gain. If this peaking is undesirable a simple RC filter at the input of the buffer will smooth the frequency response shown as *Figure 4*. *Figure 5* shows the results of a simple filter placed on the non-inverting input. See *Figure 6* and *Figure 7* for another method for reducing unity gain peaking.

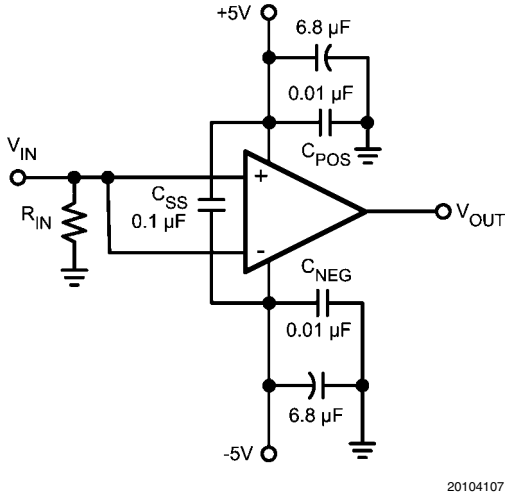


FIGURE 6. Alternate Unity Gain Compensation

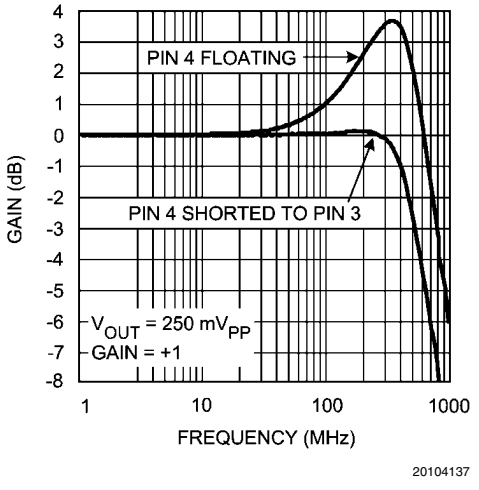


FIGURE 7. Frequency Response for Circuit in *Figure 6*

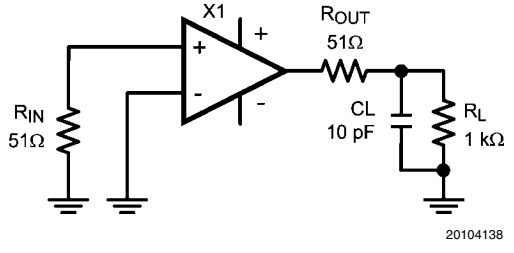


FIGURE 8. Decoupling Capacitive Loads

DRIVING CAPACITIVE LOADS

Capacitive output loading applications will benefit from the use of a series output resistor R_{OUT}. *Figure 8* shows the use of a series output resistor, R_{OUT}, to stabilize the amplifier output under capacitive loading. Capacitive loads of 5 to 120 pF are the most critical, causing ringing, frequency response peaking and possible oscillation. The charts "Suggested R_{OUT} vs. Cap Load" give a recommended value for selecting a series output resistor for mitigating capacitive loads. The values suggested in the charts are selected for .5 dB or less of peaking in the frequency response. This gives a good compromise between settling time and bandwidth. For applications where maximum frequency response is needed and some peaking is tolerable, the value of R_{OUT} can be reduced slightly from the recommended values.

LAYOUT CONSIDERATIONS

Whenever questions about layout arise, use the evaluation board as a guide. The LMH730275 is the evaluation board supplied with samples of the LMH6739.

To reduce parasitic capacitances ground and power planes should be removed near the input and output pins. Components in the feedback loop should be placed as close to the device as possible. For long signal paths controlled impedance lines should be used, along with impedance matching elements at both ends.

Bypass capacitors should be placed as close to the device as possible. Bypass capacitors from each rail to ground are applied in pairs. The larger electrolytic bypass capacitors can be located farther from the device, the smaller ceramic capacitors should be placed as close to the device as possible. The LMH6739 has multiple power and ground pins for enhanced supply bypassing. Every pin should ideally have a separate bypass capacitor. Sharing bypass capacitors may slightly degrade second order harmonic performance, especially if the supply traces are thin and /or long. In *Figure 1* and *Figure 2* C_{SS} is optional, but is recommended for best second harmonic distortion. Another option to using C_{SS} is to use pairs of .01 µF and .1 µF ceramic capacitors for each supply bypass.

VIDEO PERFORMANCE

The LMH6739 has been designed to provide excellent performance with production quality video signals in a wide variety of formats such as HDTV and High Resolution VGA. NTSC and PAL performance is nearly flawless. Best performance will be obtained with back terminated loads. The back termination reduces reflections from the transmission line and effectively masks transmission line and other parasitic capacitances from the amplifier output stage. *Figure 4* shows a typical configuration for driving a 75Ω Cable. The amplifier is configured for a gain of two to make up for the 6 dB of loss in R_{OUT}.

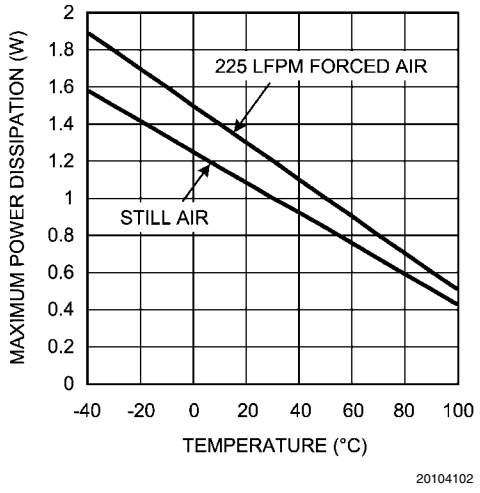


FIGURE 9. Maximum Power Dissipation

POWER DISSIPATION

The LMH6739 is optimized for maximum speed and performance in the small form factor of the standard SSOP-16 package. To achieve its high level of performance, the LMH6739 consumes an appreciable amount of quiescent current which cannot be neglected when considering the total package power dissipation limit. The quiescent current contributes to about 40° C rise in junction temperature when no additional heat sink is used (V_S = ±5V, all 3 channels on). Therefore, it is easy to see the need for proper precautions to be taken in order to make sure the junction temperature's absolute maximum rating of 150°C is not violated.

To ensure maximum output drive and highest performance, thermal shutdown is not provided. Therefore, it is of utmost importance to make sure that the T_{JMAX} is never exceeded due to the overall power dissipation (all 3 channels).

With the LMH6739 used in a back-terminated 75Ω RGB analog video system (with 2 V_{PP} output voltage), the total power dissipation is around 435 mW of which 340 mW is due to the quiescent device dissipation (output black level at 0V). With no additional heat sink used, that puts the junction temperature to about 140° C when operated at 85°C ambient.

To reduce the junction temperature many options are available. Forced air cooling is the easiest option. An external add-on heat-sink can be added to the SSOP-16 package, or alternatively, additional board metal (copper) area can be utilized as heat-sink.

An effective way to reduce the junction temperature for the SSOP-16 package (and other plastic packages) is to use the copper board area to conduct heat. With no enhancement the major heat flow path in this package is from the die through the metal lead frame (inside the package) and onto the surrounding copper through the interconnecting leads. Since high frequency performance requires limited metal near the device pins the best way to use board copper to remove heat is through the bottom of the package. A gap filler with high thermal conductivity can be used to conduct heat from the bottom of the package to copper on the circuit board. Vias to a ground or power plane on the back side of the circuit board will provide additional heat dissipation. A combination of front side copper and vias to the back side can be combined as well.

Follow these steps to determine the maximum power dissipation for the LMH6739:

1. Calculate the quiescent (no-load) power: $P_{AMP} = I_{CC}^* (V_S)$ $V_S = V^+ - V^-$
2. Calculate the RMS power dissipated in the output stage: P_D (rms) = rms $((V_S - V_{OUT})^* I_{OUT})$ where V_{OUT} and I_{OUT} are the voltage and current across the external load and V_S is the total supply current
3. Calculate the total RMS power: $P_T = P_{AMP} + P_D$

The maximum power that the LMH6739 package can dissipate at a given temperature can be derived with the following equation (See *Figure 9*):

$P_{MAX} = (150º - T_{AMB})/\theta_{JA}$, where T_{AMB} = Ambient temperature (°C) and θ_{JA} = Thermal resistance, from junction to ambient, for a given package (°C/W). For the SSOP package θ_{JA} is 120°C/W.

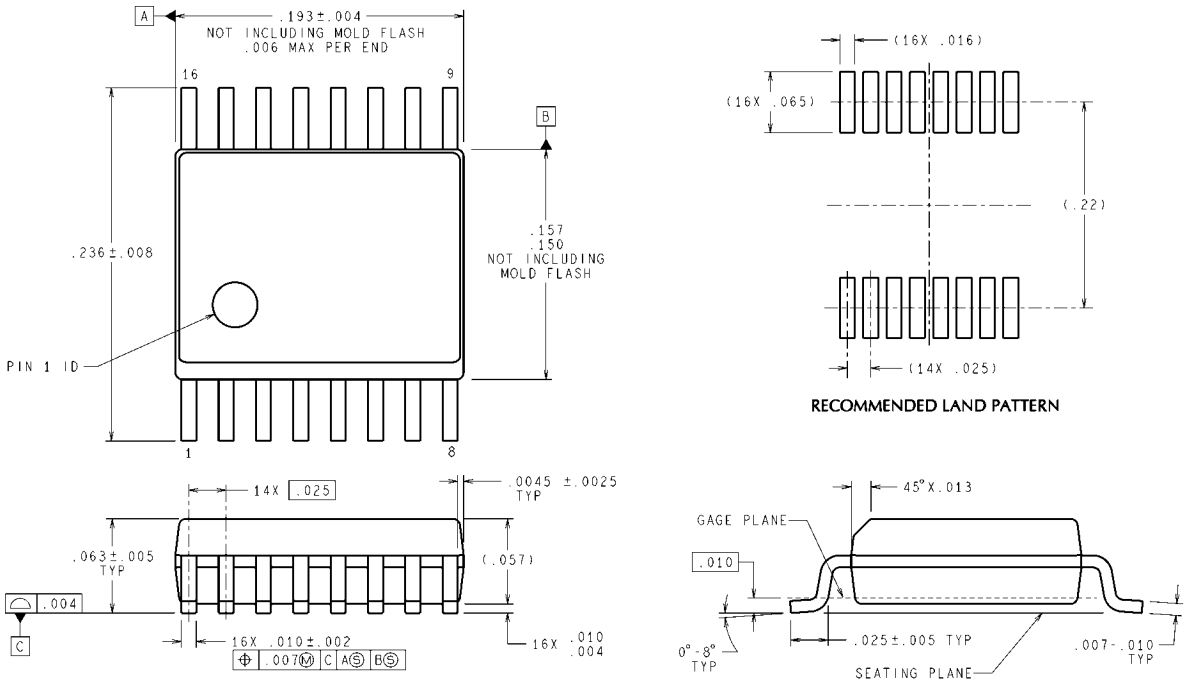
ESD PROTECTION

The LMH6739 is protected against electrostatic discharge (ESD) on all pins. The LMH6739 will survive 2000V Human Body model and 200V Machine model events.

Under closed loop operation the ESD diodes have no effect on circuit performance. There are occasions, however, when the ESD diodes will be evident. If the LMH6739 is driven by a large signal while the device is powered down the ESD diodes will conduct.

The current that flows through the ESD diodes will either exit the chip through the supply pins or will flow through the device, hence it is possible to power up a chip with a large signal applied to the input pins. Shorting the power pins to each other will prevent the chip from being powered up through the input.

Physical Dimensions inches (millimeters) unless otherwise noted



DIMENSIONS ARE IN INCHES
DIMENSIONS IN ( ) FOR REFERENCE ONLY

MQA16 (Rev B)

16-Pin SSOP
NS Package Number MQA16

Notes

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