HA16174P/FP

Power Factor Correction Controller IC

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Rev.1.00
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Description

The HA16174P/FP is a power-factor correction (PFC) controller IC.

This IC adopts continuous conduction mode as PFC operation.

Various functions such as over voltage detection, over current detection, soft start, feedback-loop disconnection detection, Power Good signal output, and holding function of PFC operation through momentary outage (PFC hold function) are incorporated in a single chip. This eliminates a significant amount of external circuitry.

The PFC function enables the continuation of PFC operation for a specified period when a momentary outage occurs, so that quick recovery after a sufficiently momentary outage is achieved*. The continuance time can be adjusted by an external capacitance.

The PFC output voltage is monitored by checking the Power Good signal. When the power-factor correction is "good," the Power Good signal is output after a delay time to secure stabilization of the PFC output voltage; when the power factor correction is not good, the output is stopped immediately. The delay time and power good stop level are adjustable by using an external circuit.

PFC operation can be turned on and off by an external control signal. By using this function, PFC operation can be disabled at low input voltage, allowing remote control from the secondary side.

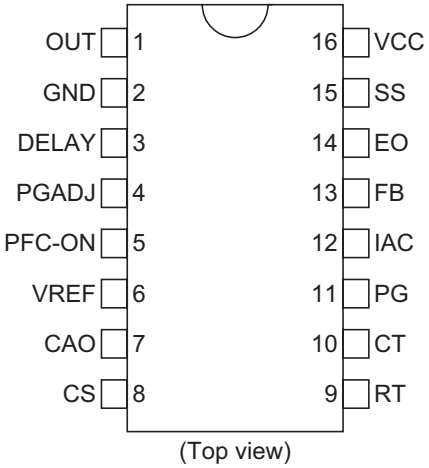
A soft-start control pin provides for the easy adjustment of soft-start operation, and can be used to prevent overshooting of the output voltage.

*: For details on the PFC hold function, refer to page 19.

Features

- Maximum ratings
  - Power-supply voltage Vcc: 24 V
  - Operating junction temperature Tjopr: –40 to 125°C
- Electrical characteristics
  - VREF output voltage VREF: 5.0 V ± 3%
  - UVLO operation start voltage VH: 10.5 ± 0.7 V
  - UVLO operation stop voltage VL: 9.0 ± 0.5 V
  - PFC output maximum ON duty Dmax-out: 95% (typ.)
- Functions
  - Continuous conduction mode
  - Hold function of PFC operation on momentary outage (PFC hold function)
  - Over voltage detection
  - Over current detection
  - Soft start
  - Feedback loop disconnection detection
  - Power Good signal output (open-drain output)
  - PFC function on/off control
  - Package lineup: SOP-16 and DILP-16

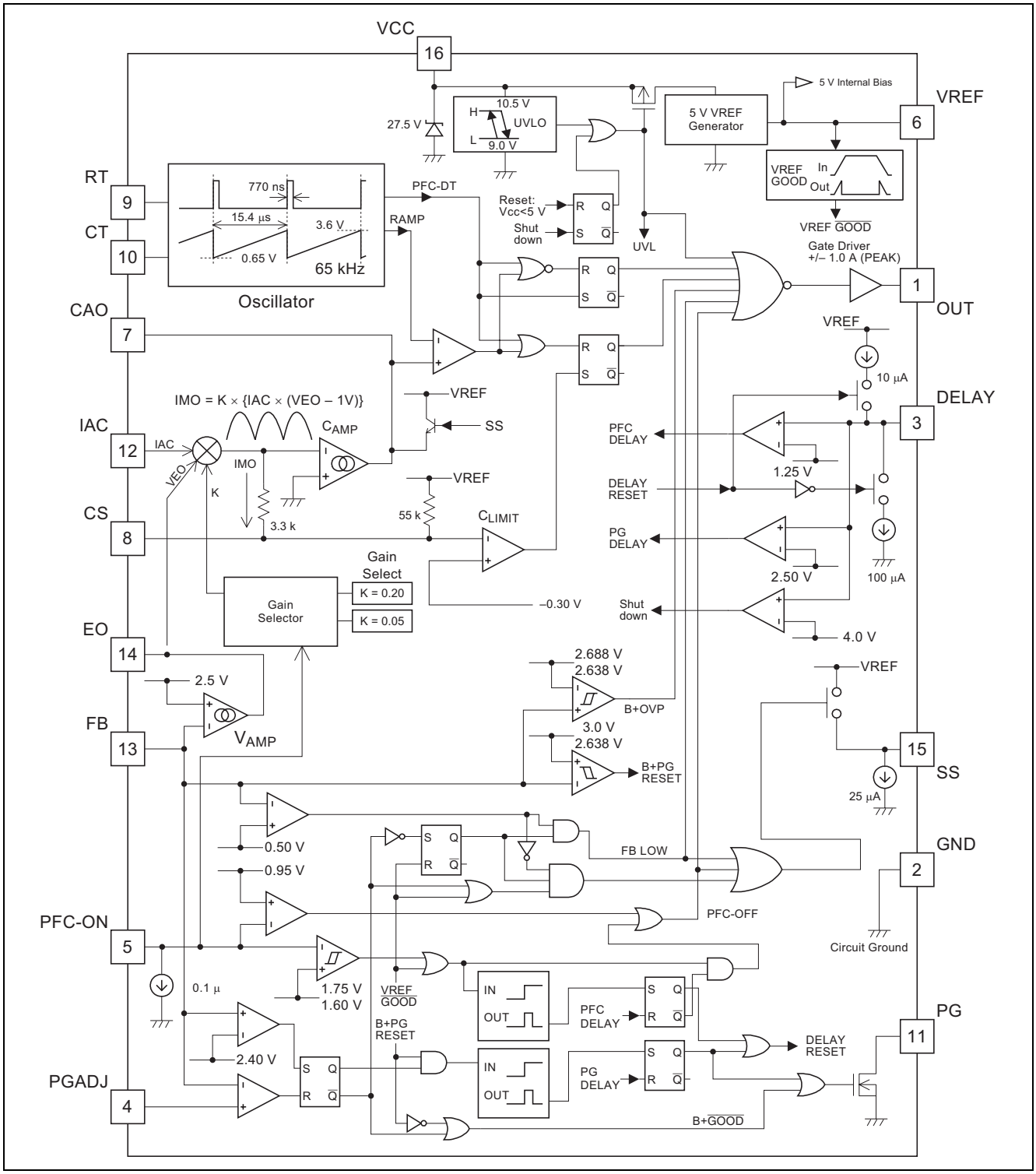
Pin Arrangement



Pin Description

Pin No.	Pin Name	I/O	Function
1	OUT	Output	Power MOS FET gate driver output
2	GND	—	Ground
3	DELAY	Input/Output	PG start up delay time and hold time adjust and IC shut down
4	PGADJ	Input	PG off threshold voltage input
5	PFC-ON	Input	PFC function on/off signal input
6	VREF	Output	Reference voltage output
7	CAO	Output	Current control error amplifier output
8	CS	Input/Output	Current sense signal input
9	RT	Input/Output	Timing resistor for operational frequency adjust
10	CT	Output	Timing capacitor for operational frequency adjust
11	PG	Output	Power good signal output (open drain output)
12	IAC	Input	Multiplier reference current input
13	FB	Input	Voltage control error amplifier input
14	EO	Output	Voltage control error amplifier output
15	SS	Output	Timing capacitor for soft start time adjust
16	VCC	Input	Power supply voltage input

Block Diagram



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit	Note
Supply voltage	VCC	24	V	
OUT peak current	Ipk-out	±1.0	A	3
OUT DC current	Idc-out	±0.1	A	
Terminal voltage	Vi-group1	–0.3 to Vcc	V	4
	Vi-group2	–0.3 to Vref	V	5
CAO voltage	Vcao	–0.3 to Vcaoh	V	
EO voltage	Veo	–0.3 to Veoh	V	
DELAY voltage	Vdelay	–0.3 to +6.5	V	
PFC-ON voltage	Vpfc-on	–0.3 to +6.5	V	
PFC-ON clamp current	Ipfc-on-clamp	300	µA	
RT current	Irt	–200	µA	
CT current	Ict	±800	µA	
IAC current	Iiac	1	mA	
CS voltage	Vi-cs	–1.5 to 0.3	V	
VREF current	Io-ref	–5	mA	
PG current	Io-pg	5	mA	
PGADJ voltage	Vpgadj	2.3	V	
Power dissipation	Pt	1	W	6, 7
Operating junction temperature	Tj-opr	–40 to 125	°C	
Storage temperature	Tstg	–55 to 150	°C	

Notes
1. Rated voltages are with reference to the GND pin.
2. For rated currents, inflow to the IC is indicated by (+), and outflow by (–).
3. The transient current when driving a capacitive load.
4. This is the rated voltage for the following pins:
   OUT, PG
5. This is the rated voltage for the following pins:
   VREF, FB, IAC, SS, RT, CT
6. HA16174P (DILP) type: θja = 120°C/W
7. HA16174FP (SOP) type: θja = 120°C/W
   This is value mounted on glass epoxy board of 10% wiring density and 40 mm × 40 mm × 1.6 mm.

Electrical Characteristics

(Ta = 25°C, VCC = 12 V, RT = 27 kΩ, CT = 1000 pF)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Supply	Start threshold	VH	9.8	10.5	11.2	V	
	Shutdown threshold	VL	8.5	9.0	9.5	V	
	UVLO hysteresis	dVUVL	1.0	1.5	2.0	V	
	Start-up current	Is	140	200	260	µA	VCC = 9.5 V
	Is temperature stability	dIs/dTa	—	–0.3	—	%/°C	*1
	Operating current	Icc	3.45	4.5	6.45	mA	IAC = 0 A, CL = 0 F
VREF	Output voltage	Vref	4.85	5.00	5.15	V	Isource = 1 mA
	Line regulation	Vref-line	—	5	20	mV	Isource = 1 mA, VCC = 12 V to 23 V
	Load regulation	Vref-load	—	5	20	mV	Isource = 1 mA to 5 mA
	Temperature stability	dVref	—	±80	—	ppm/°C	Ta = –40 to 125°C *1
Oscillator	Initial accuracy	fout	58.5	65	71.5	kHz	Measured pin: OUT
	fout temperature stability	dfout/dTa	—	±0.1	—	%/°C	Ta = –40 to 125°C *1
	fout voltage stability	fout-line	–1.5	0.5	1.5	%	VCC = 12 V to 18 V
	CT peak voltage	Vct-H	—	3.6	4.0	V	*1
	Ramp valley voltage	Vct-L	—	0.65	—	V	*1
	RT voltage	Vrt	1.07	1.25	1.43	V	
Soft start	Sink current	Iss	15.0	25.0	35.0	µA	SS = 2 V
Current limit	Threshold voltage1	VCL1	–0.33	–0.30	–0.27	V	PFC-ON = 2 V
	Delay to output	td-CL	—	280	500	ns	CS = 0 to –1 V
V_{AMP}	Feedback voltage	Vfb	2.40	2.50	2.60	V	FB-EO Short
	Input bias current	Ifb	–0.3	0	0.3	µA	Measured pin: FB
	Open loop gain	Av-v	—	60	—	dB	*1
	High voltage	Veoh	5.2	5.7	6.2	V	FB = 2.3 V, EO: Open
	Low voltage	Veol	—	0.1	0.3	V	FB = 2.7 V, EO: Open
	Source current	Isrc-eo	—	–120	—	µA	FB = 1.0 V, EO = 2.5 V
	Sink current	Isnk-eo	—	120	—	µA	FB = 4.0 V, EO = 2.5 V
	Transconductance	Gm-v	150	200	290	µA/V	FB = 2.5 V, EO = 2.5 V
C_{AMP}	Input offset voltage	Vio-ca	—	(–10)	0	mV	*1
	Open loop gain	Av-ca	—	60	—	dB	*1
	High voltage	Vcaoh	5.2	5.7	6.2	V	
	Low voltage	Vcaol	—	0.1	0.3	V	
	Source current	Isrc-ca	—	–90	—	µA	CAO = 2.5 V *1
	Sink current	Isnk-ca	—	90	—	µA	CAO = 2.5 V *1
	Transconductance	Gm-c	150	200	290	µA/V	*1

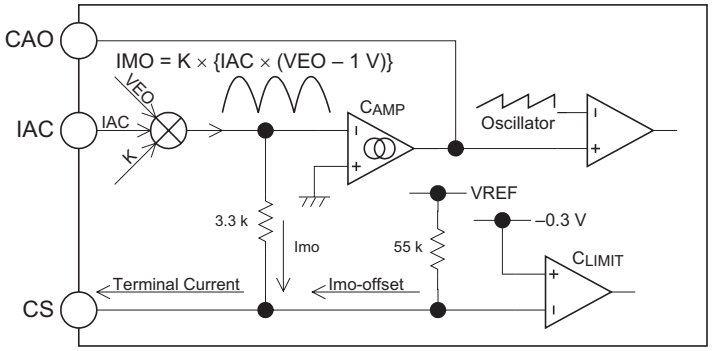
Note 1: Design spec.

(Ta = 25°C, VCC = 12 V, RT = 27 kΩ, CT = 1000 pF)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
IAC/ Multiplier	IAC PIN voltage	Viac	1.6	2.3	3.0	V	IAC = 100 µA
	Terminal offset current	Imo-offset	–136	–90	–73	µA	IAC = 0 A, CS = 0 V
	Output current (PFC-ON = 2.5 V)	Imo1	—	–20	—	µA	EO = 2 V, IAC = 100 µA *1,2
		Imo2	—	–60	—	µA	EO = 4 V, IAC = 100 µA *1,2
	Output current (PFC-ON = 5.5 V)	Imo3	—	–5	—	µA	EO = 2 V, IAC = 100 µA *1,2
		Imo4	—	–15	—	µA	EO = 4 V, IAC = 100 µA *1,2
	PFC-CS resistance	Rmo	—	3.3	—	kΩ	*1
	Gain voltage	Vpfc-gain	(3.4)	(4.1)	(4.7)	V	Gain = 0.125*1
OUT	Minimum duty cycle	Dmin-out	—	—	0	%	CAO = 4.0 V
	Maximum duty cycle	Dmax-out	90	95	98	%	CAO = 0 V
	Rise time	tr-out	—	30	100	ns	CL = 1000 pF
	Fall time	tf-out	—	30	100	ns	CL = 1000 pF
	Low voltage	Vol1-out	—	0.05	0.2	V	Iout = 20 mA
		Vol2-out	—	0.5	2.0	V	Iout = 200 mA (Pulse Test)
		Vol3-out	—	0.03	0.7	V	Iout = 10 mA, VCC = 5 V
	High voltage	Voh1-out	11.5	11.9	—	V	Iout = –20 mA
		Voh2-out	10.0	11.0	—	V	Iout = –200 mA (Pulse Test)
Shutdown	Shutdown voltage	Vshut	3.30	4.00	4.70	V	Input: DELAY
	Reset voltage	Vres	—	—	4.0	V	Input: Vcc
	Shutdown current	Ishut	120	190	260	µA	VCC = 9 V

Notes 1. Design spec.

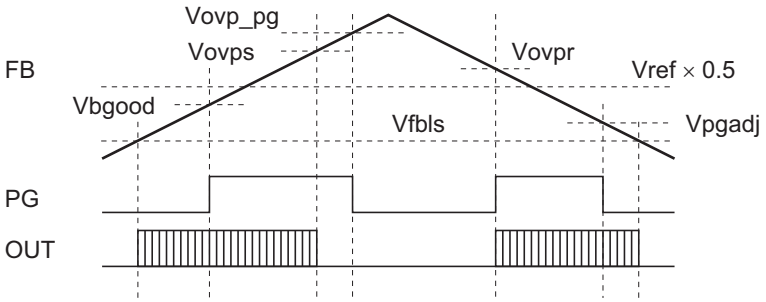
2. Imo1 to Imo4 defined as,
   Imo = (CS Terminal Current) – (Imo-offset)



(Ta = 25°C, VCC = 12 V, RT = 27 kΩ, CT = 1000 pF)

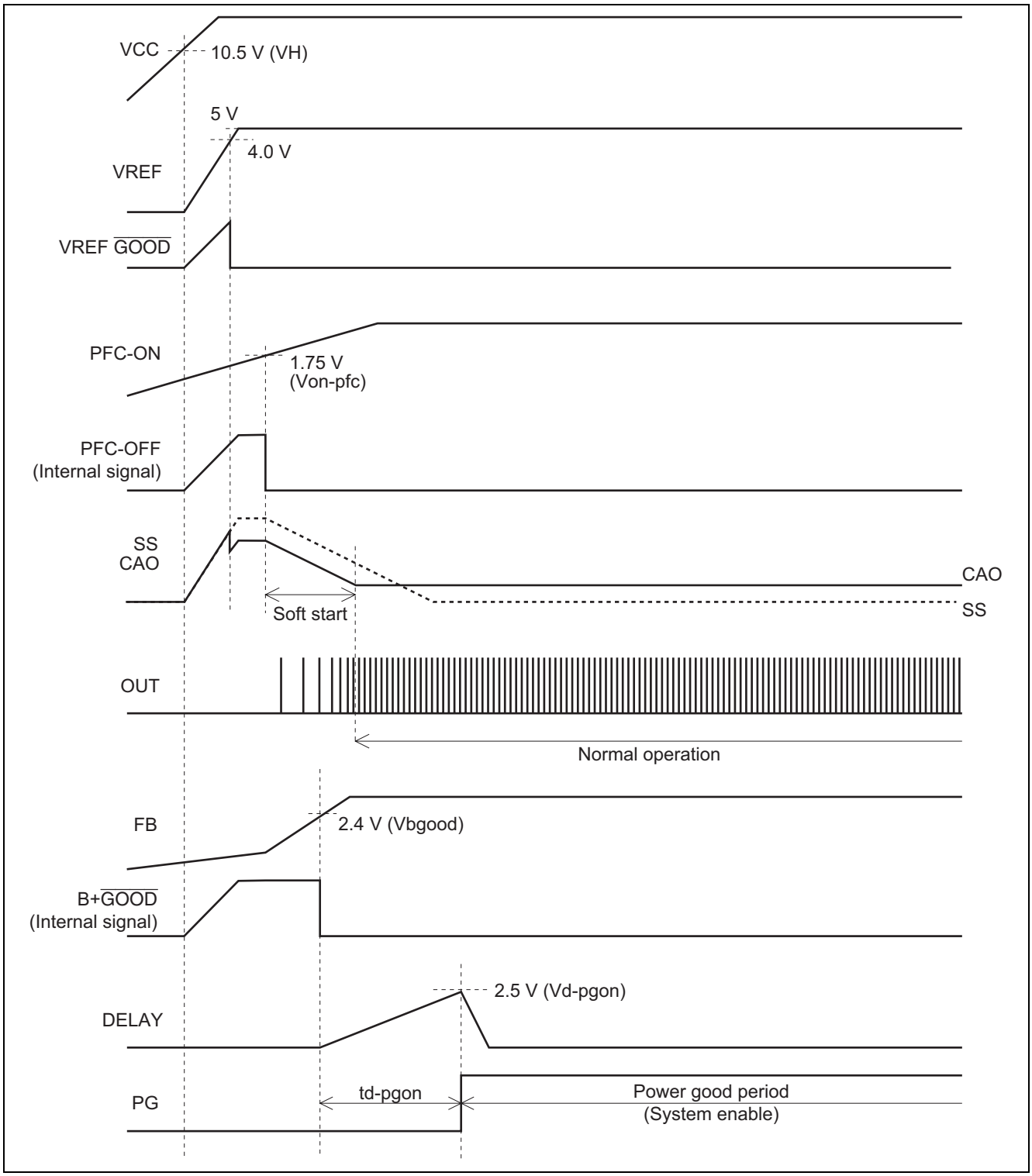
Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Supervisor/ PG	PFC enable voltage	Von-pfc	1.62	1.75	1.87	V	Input pin: PFC-ON
	PFC disable voltage	Voff-pfc	1.48	1.6	1.72	V	Input pin: PFC-ON
	PFC shutdown voltage	Vshut-pfc	0.5	0.95	1.2	V	Input pin: PFC-ON
	PFC disable delay threshold voltage	Vd-pfc	1.15	1.25	1.35	V	Input pin: DELAY
	Input current	Ipfc-on	—	0.1	1.0	µA	PFC-ON = 2 V
	B+ good voltage	dVbgood	–0.175	–0.1	–0.025	V	Input pin: FB *1
	PGADJ voltage	Vpgadj	1.42	1.50	1.58	V	Input pin: FB, PGADJ = 1.5 V
	PGADJ minimum voltage	Vpgadjmin	—	—	0.55	V	Input pin: FB
	B+ OVP set voltage	dVovps	0.125	0.188	0.250	V	Input pin: FB *1
	B+ OVP reset voltage	dVovpr	0.075	0.138	0.200	V	Input pin: FB *1
	B+ OVP PG OFF voltage	dVovp_pg	0.275	0.500	0.725	V	Input pin: FB
	FB low set voltage	Vfbls	0.45	0.50	0.55	V	Input pin: FB
	PG leakage current	Ioff-pg	—	0.001	1.0	µA	PG = 2 V
	PG shunt current	Ion-pg	2	—	—	mA	PG = 2 V
	PG start-up delay threshold voltage	Vd-pgon	2.3	2.5	2.7	V	Input pin: DELAY
	Delay to PG OFF	td-pgoff	—	0.2	1	µs	Input pin: FB
	DELAY source current	Isrc-delay	–14.5	–10	–7	µA	DELAY = 1 V
	DELAY sink current	Isnk-delay	70	100	145	µA	DELAY = 1 V

Note 1. dVbgood = Vbgood – Vref × 0.5
dVovps = Vovps – Vref × 0.5
dVovpr = Vovpr – Vref × 0.5
dVovp_pg = Vovp_pg – Vref × 0.5

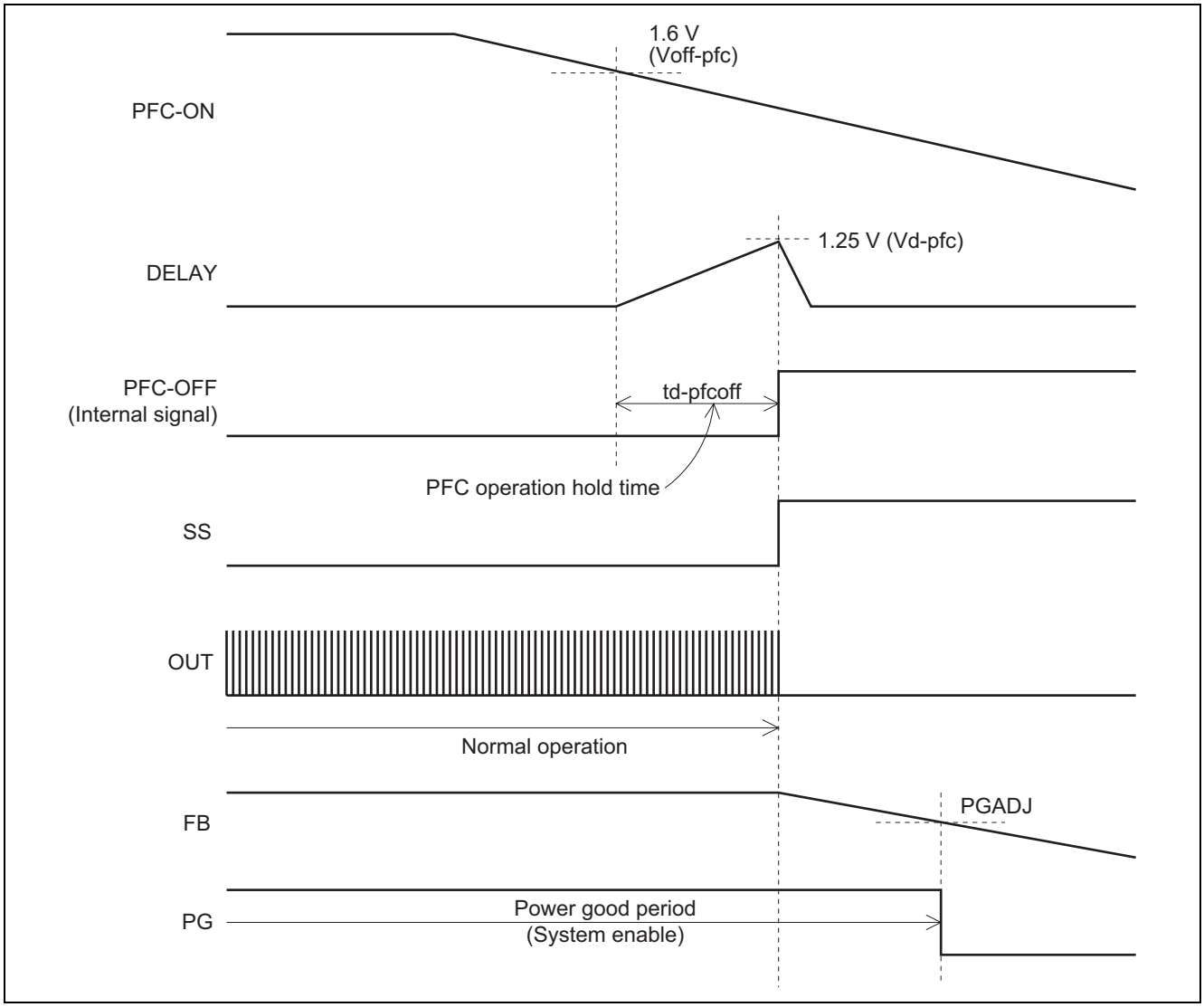


Timing Chart

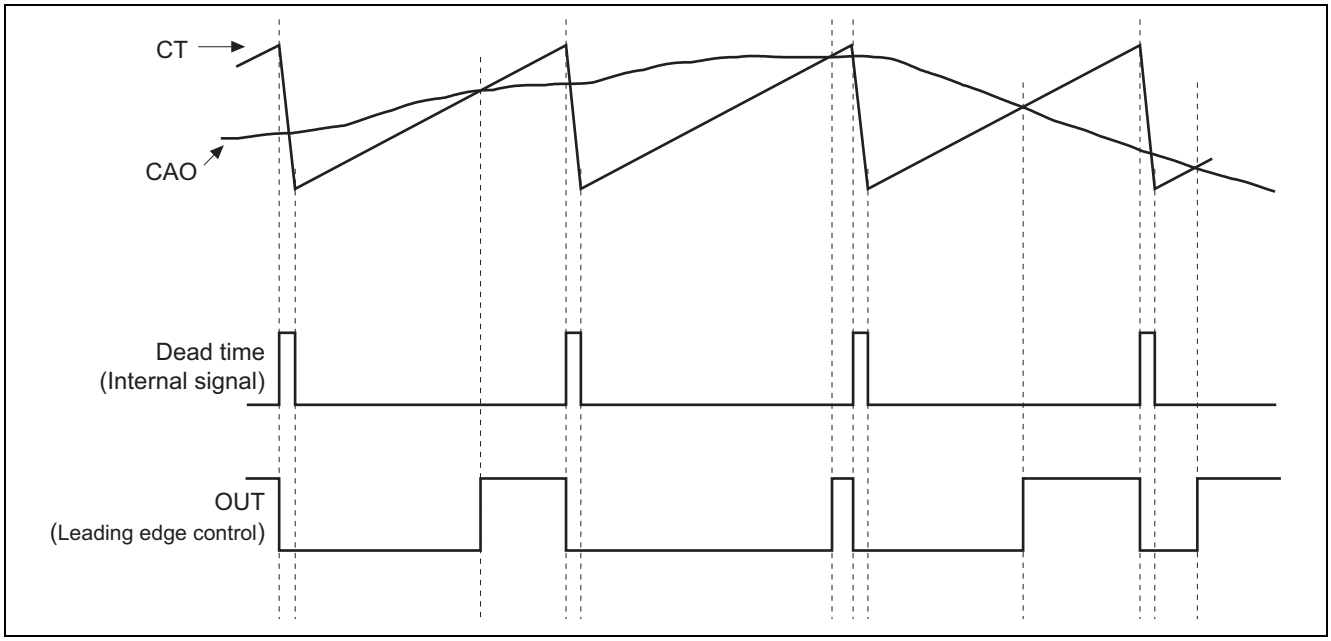
1. Start-up Timing



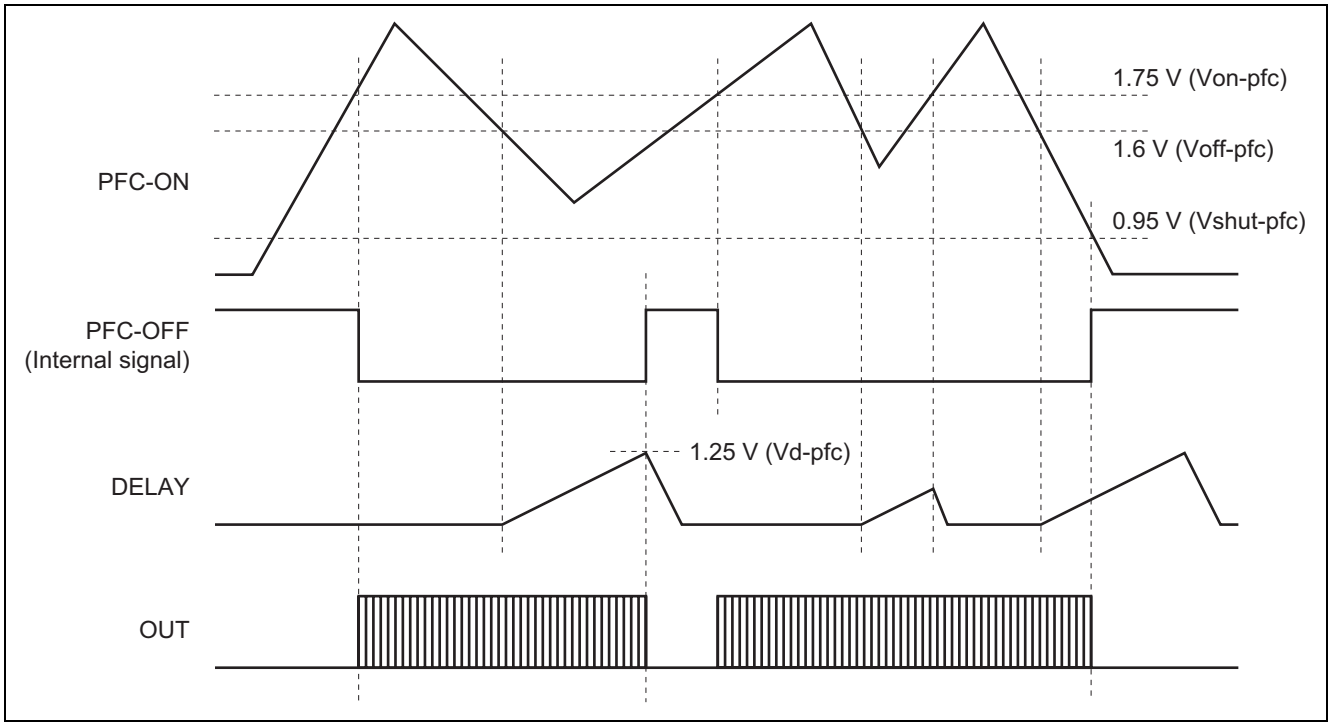
2. Stop Timing



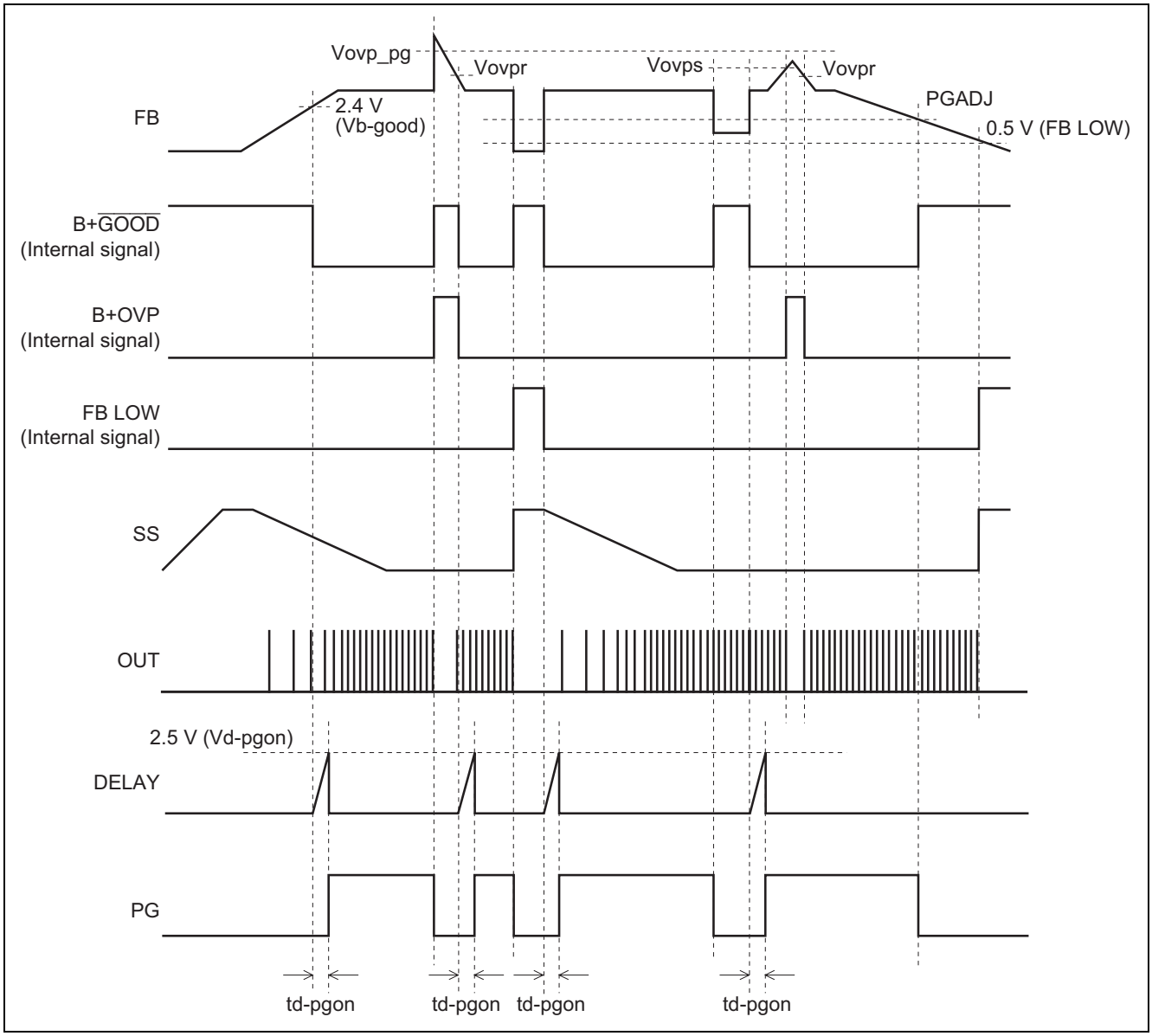
3. Oscillator, Gate Driver Output



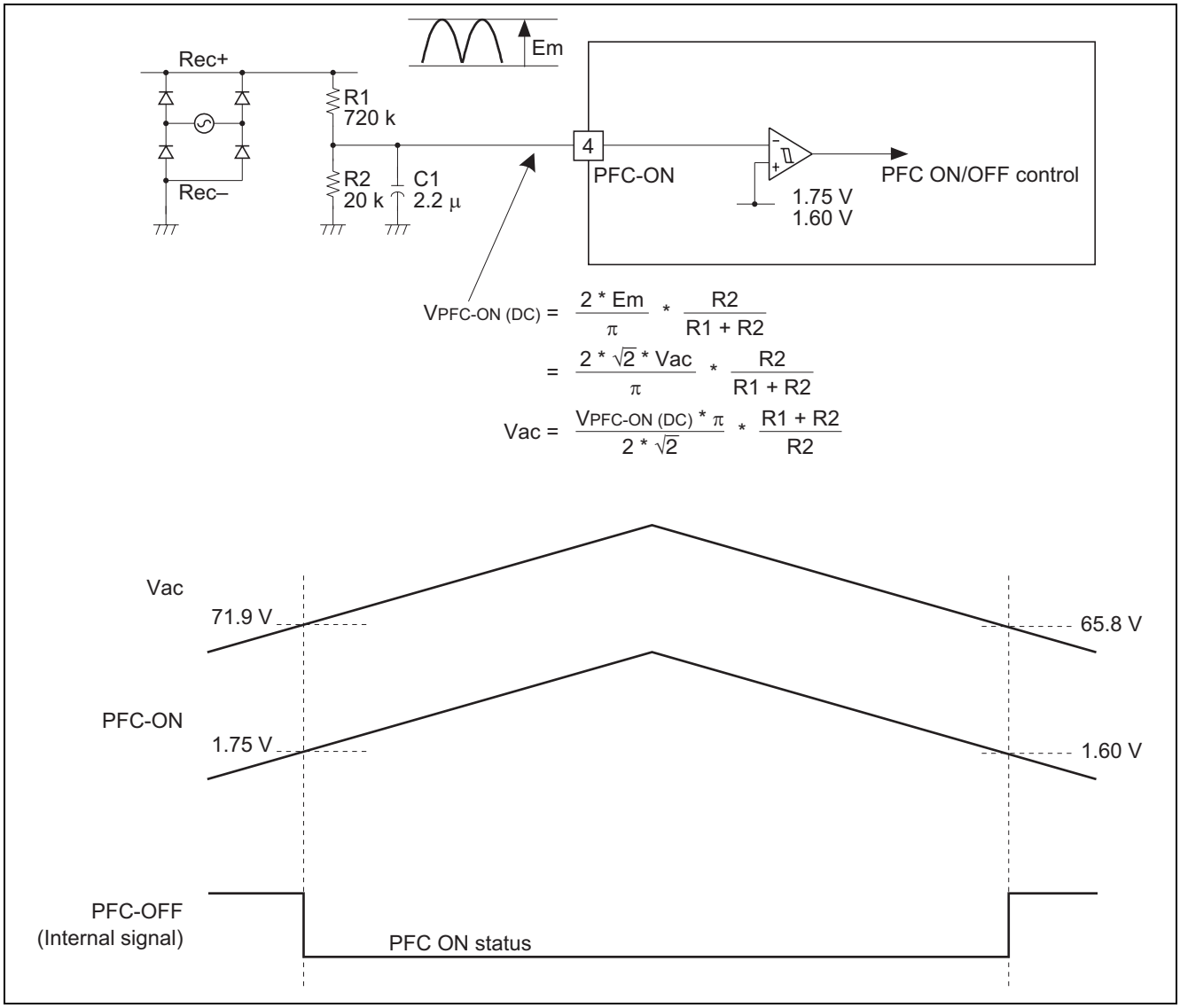
4. PFC Operation ON/OFF



5. FB Supervisor



6. PFC ON/OFF Function



Description of Pin Functions

OUT Pin:

The power MOS FET gate-drive signal is output from this pin, and takes the form of a rectangular waveform with an amplitude of VCC-GND.

GND Pin:

The ground terminal.

DELAY Pin:

This pin has three functions; (1) delay-time setting for output of the Power Good signal, (2) setting the PFC function hold time for cases of momentary outage, and (3) IC shutdown.

Normal operation is as a 100 µA constant-current sink.

(1) Power Good signal output delay
When the PFC output voltage is within the range from 96% (typ.) to 105.5% (typ.), this pin functions as a 10 µA source current. When the capacitor is charged until the voltage reaches 2.5 V (typ.), the Power Good signal is output and the delay-pin function becomes a 100 µA sink current. The delay time for Power Good signal output is set by the values of the external capacitor.

(2) Setting the PFC function hold time for momentary outage
When the PFC-ON pin is driven below 1.6 V (typ.) due to a momentary outage, the delay pin functions as a 10 µA source current. PFC operation continues until the capacitor is charged to 1.25 V (typ.). After the voltage on the delay pin reaches 1.25 V (typ.) the pin functions as a 100 µA sink current, and PFC operation terminates. The PFC function hold time can be set by the value of the external capacitor.

(3) Shutdown
When this pin is pulled up to 4 V (typ.) or higher, the IC enters the shutdown state. Accordingly, the VREF signal becomes low and the operating current becomes several hundred µA. The IC does not resume operation until Vcc falls to 4 V (max.) or below.

Note: (1) and (2) cannot be set independently.

PGADJ Pin:

This pin sets the stop level of power good signal. If the FB pin voltage falls below this pin voltage, the Power Good signal stops immediately. Do not set this pin voltage to 2.3 V or higher. When this pin is open-circuit, the Power Good signal stops when the voltage on the FB pin becomes lower than 0.55 V (max.).

PFC-ON Pin:

This pin is applied smoothing voltage of rectified AC voltage. When 1.75 V (typ.) or more is applied to this pin, PFC operation starts. When the voltage is 1.6 V (typ.) or lower, the PFC operation stops after the PFC operation hold time (refer to the description of DELAY pin operation). When the voltage is forcibly lower than 0.95 V (typ.), PFC operation stops even if the PFC operation hold time has not elapsed.

VREF Pin:

Temperature-compensated voltage with an accuracy of 5 V ± 3% is output from this pin. The pin should supply no more than 5 mA (max.) source current. This pin has no sink capabilities.

CAO Pin:

This pin is the current-error amplifier output, and is connected to the phase-compensation circuit of the current-error amp. The result of comparison of the voltage on this pin and the CT pin produces the pulse output from the OUT pin.

CS Pin:

Current detection pin. The current is controlled to be proportional to the AC voltage and the power factor is corrected. When the voltage on this pin drops to –0.3 V (typ.) or below, over current detection circuit operates, and OUT pin is stopped.

RT Pin:

A pin for frequency adjustment of the oscillator.

CT Pin:

A pin for frequency adjustment of the oscillator.

PG Pin:

Open-drain pin for output of the Power Good signal. The internal MOS FET is in the ON state when the output voltage of the PFC power supply is started up or in case of abnormality. When the output voltage becomes normal, the MOS FET is switched to the OFF state after the delay time.

IAC Pin:

This pin is for detecting the input AC voltage waveform. For processing within the IC, the AC voltage waveform is converted to current information.

FB Pin:

This pin is the input to the voltage error amp. This pin is applied to voltage divided PFC output with resistors. The feedback loop is intended to keep 2.5 V (typ.).

EO Pin:

This pin is the output of the voltage error amp. This pin is connected to the phase-compensation circuit of the voltage error amp. The voltage on this pin is the input signal to the internal multiplier.

SS Pin:

This pin is connected to GND or VREF via a capacitor. This pin is pulled up to the VREF pin voltage until PFC operation starts. When the voltage on the PFC-ON pin has reached 1.75 V (typ.) PFC operation is start and this pin flows 25 µA source current. Operation of the CAO pin is affected by that of the SS pin, the pulse width of the OUT pin is limited, and this prevents overshooting when start up.

VCC Pin:

IC power-supply pin. The IC starts up at 10.5 V (typ.), and stops at 9 V (typ.).

Description of Functions

1. UVL Circuit

The UVL circuit monitors the Vcc voltage. When the voltage is lower than 9.0 V, the IC is stopped. When the voltage is higher than 10.5 V, IC is started.

When operation of the IC is stopped by the UVL circuit, the driver circuit output is fixed low, output of VREF is stopped, and the oscillator is stopped.

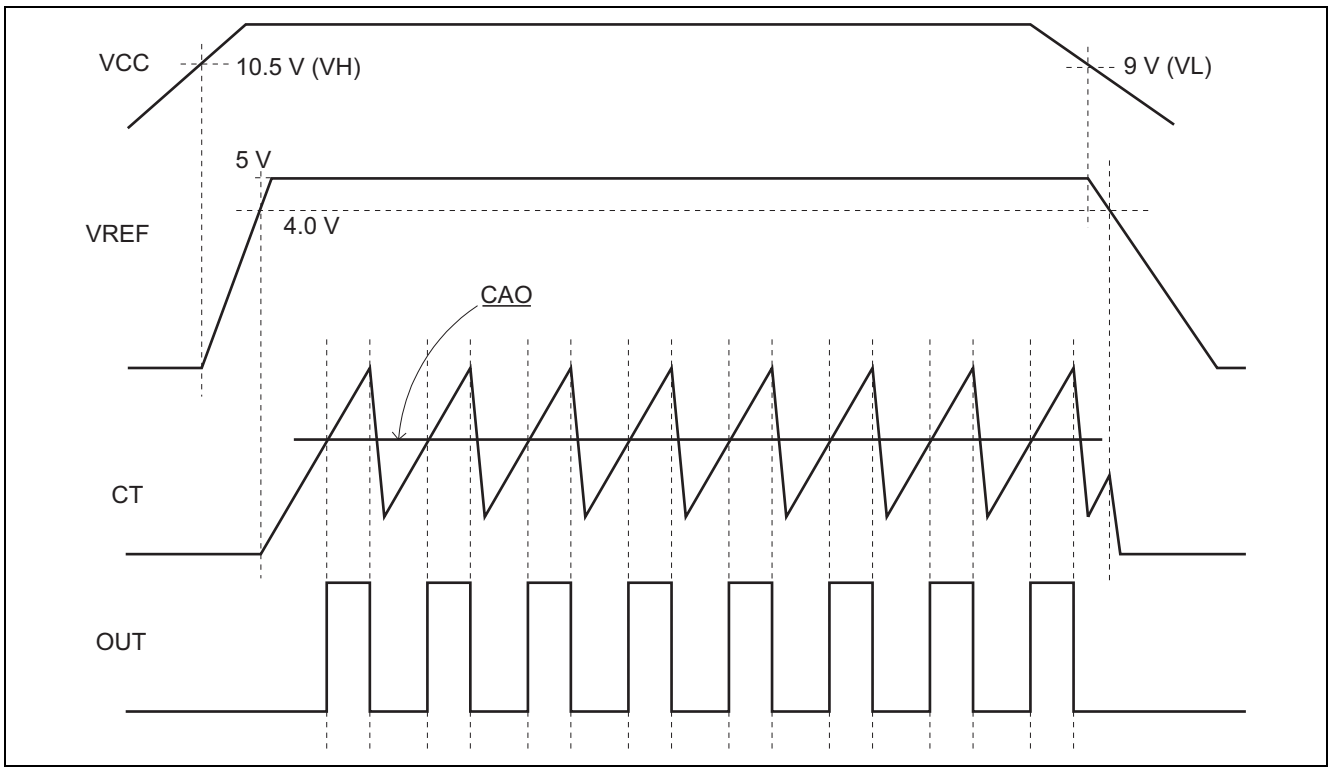


Figure 1 UVL Operation

2. Operating Frequency

The HA16174 operating frequency fosc is determined by adjusting the timing resistor Rt (the RT pin, pin 9) and the timing capacitance Ct (the CT pin, pin 10). The operating frequency is approximated by the following expression:

$$fosc = \frac{1.7 \times 10^6}{Rt\ (k\Omega) \times Ct\ (pF)} \quad (kHz)$$

When the IC is operated at high frequencies, the expression becomes less accurate due to IC internal delay time, etc. Please confirm operation the value with the actually mounted IC. The maximum operating frequency is 400 kHz. As a reference, the operating frequency data when the timing resistor and the timing capacitance are changed is shown in the below figure.

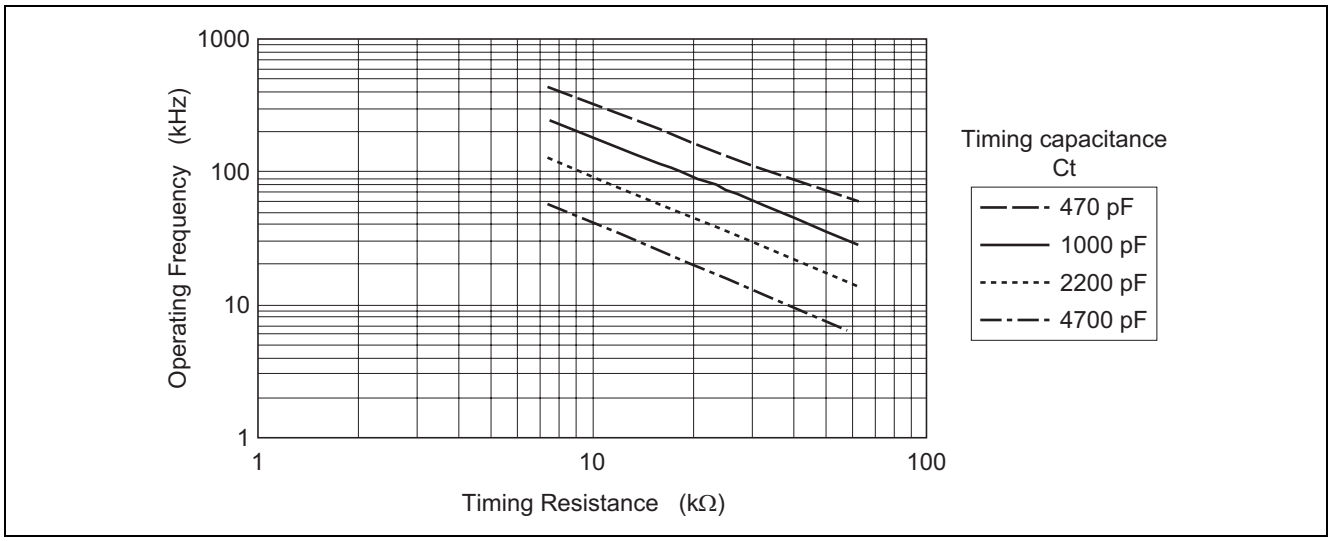


Figure 2 Operating Frequency Characteristics

3. Soft Start

This function prevents applying excessive stress on external components and overshooting of the PFC output voltage (B + voltage) when start up. The pulse width is gradually widening from 0% duty cycle. During soft-start operation, the SS and CAO signals lower with link.. The duty cycle is controlled by the CAO signal.

The soft-start time can be set by an external capacity.

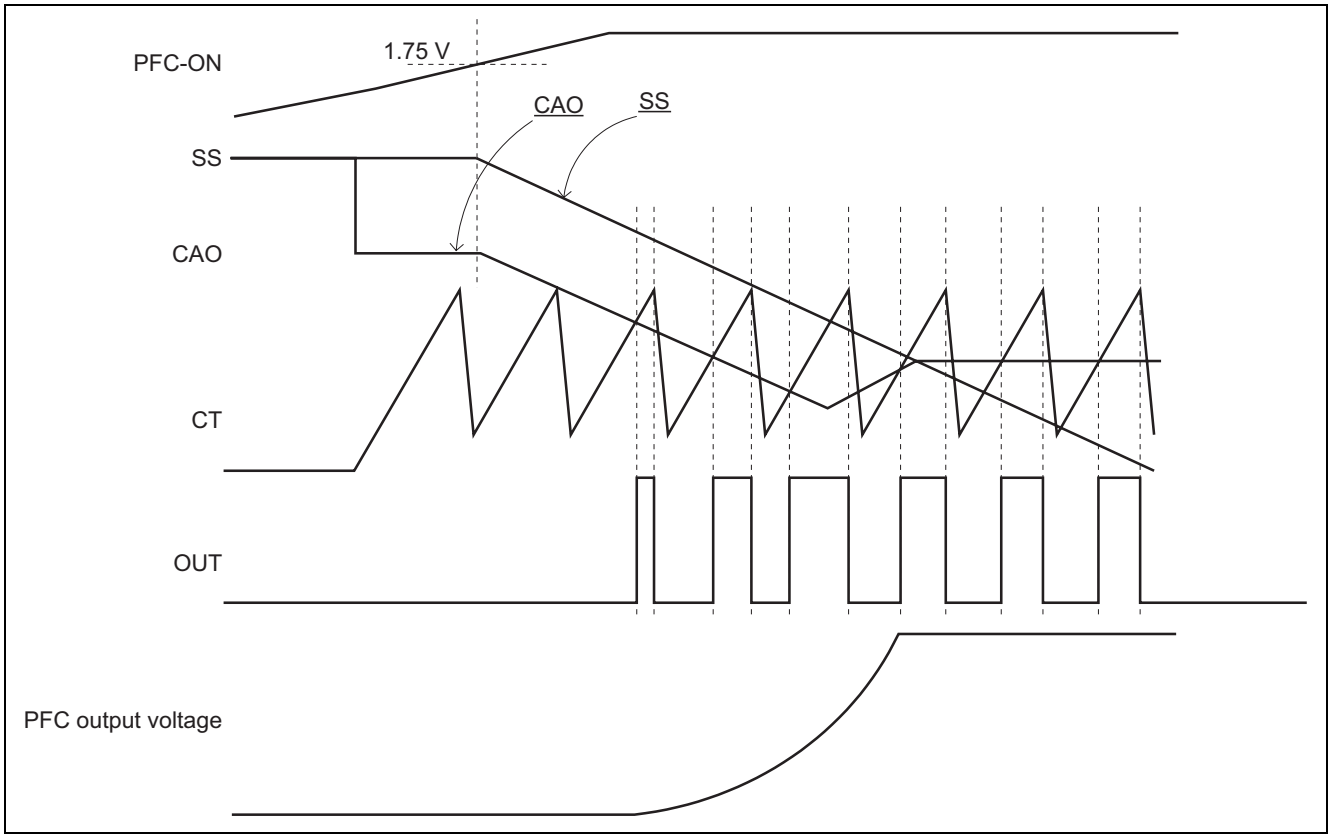


Figure 3 Soft-Start Operation Waveform

4. PFC-ON Pin Function

Several functions are assigned to the PFC-ON pin, and which is operational depends on the power-supply state. Details of their operation are given below. Note, however, that the functions do not operate when VREF voltage is lower than 4 V as UVL operation and shut down.

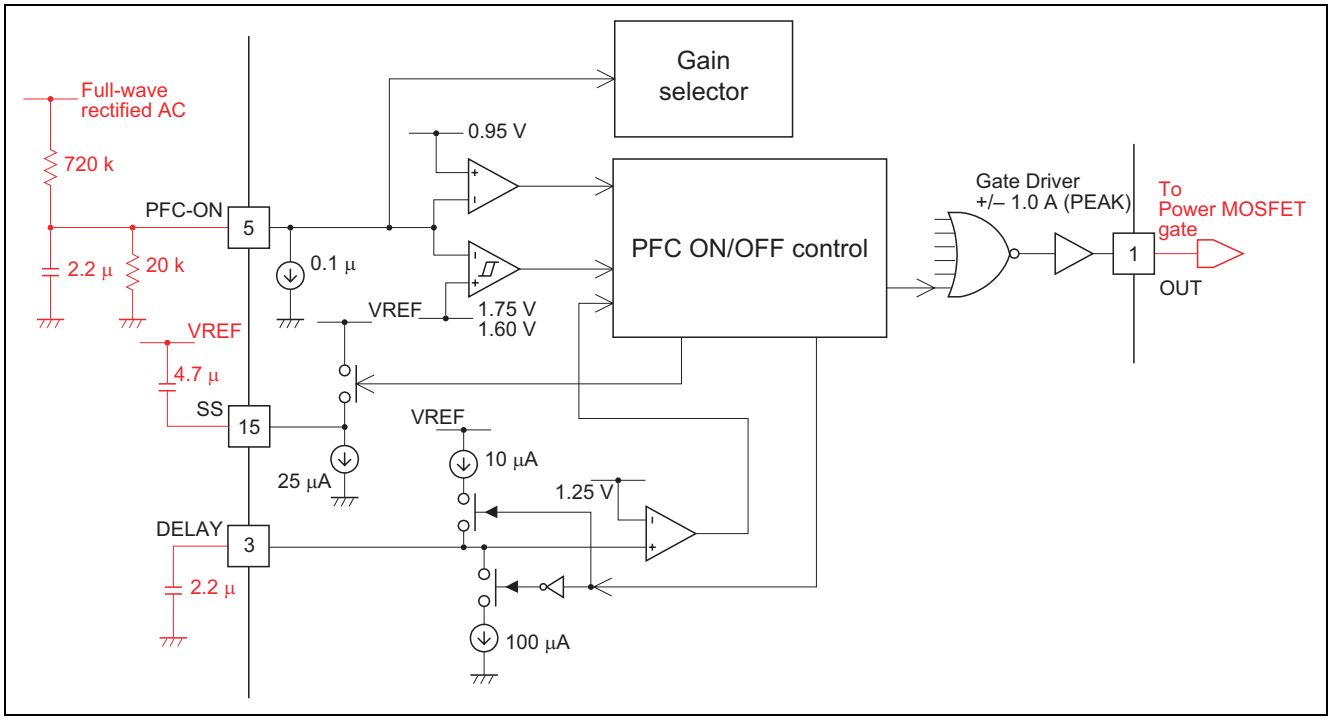


Figure 4 Internal Circuits Connected to the PFC-ON Pin

4-1. Power-Supply Startup Operation

When the AC voltage is applied, the voltage on the PFC-ON pin rises. After it exceeds 1.75 V, the voltage on the SS pin starts to be discharged and PFC operation starts up. The PFC output voltage is initially charged to a voltage of about $\sqrt{2} \times$ AC voltage; after PFC operation starts, it is boosted to the prescribed voltage.

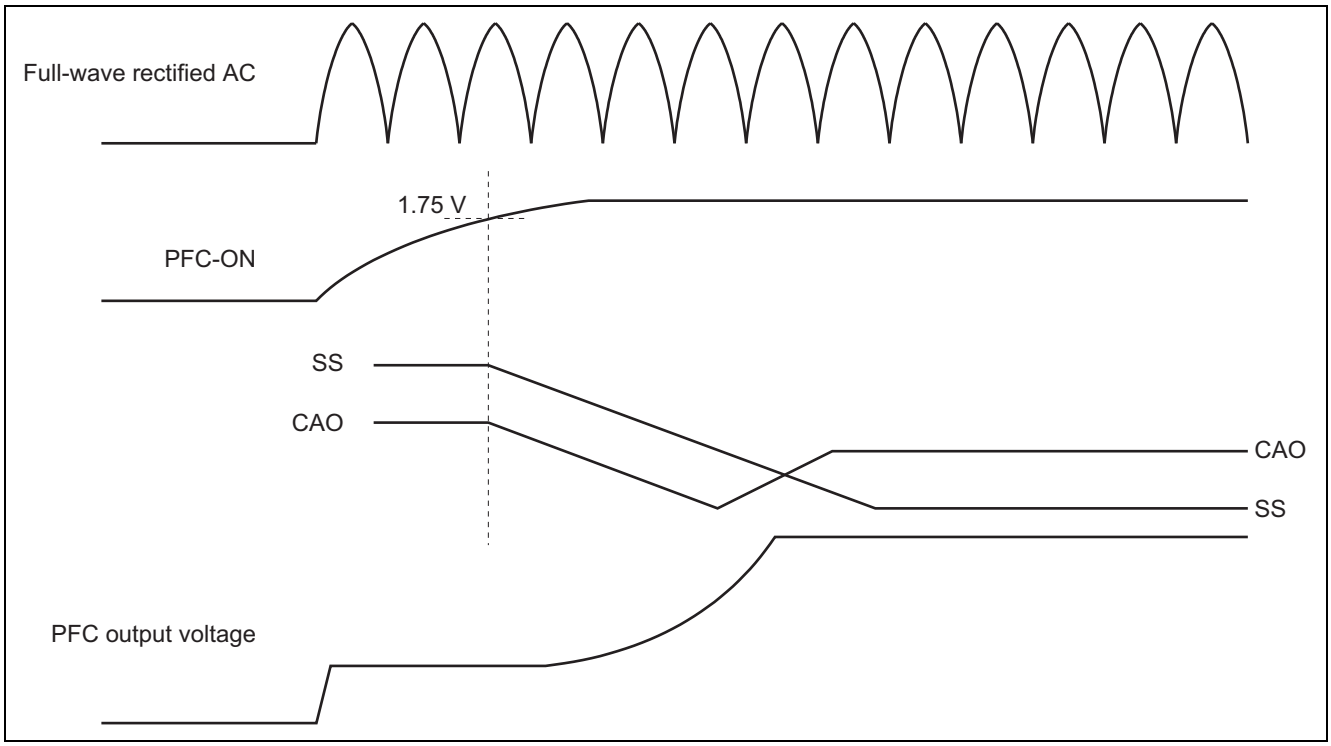


Figure 5 Waveforms in Operations at Startup

4-2. Operation on a Momentary Outage (PFC operation hold on momentary outage: PFC hold function)

(1) When the Momentary Outage is Short

During a momentary outage, the voltage on the PFC-ON pin is discharged. When it reaches 1.6 V, charging of the capacitor on the DELAY pin starts. The voltage on the PFC-ON pin continues to fall and, when it reaches 1.4 V, source current begins to flow through the pin. The lower the PFC-ON voltage, the greater the amount of current, so the PFC-ON pin voltage does not fall below the level determined by the external resistor and the source current. AC-voltage input is resumed, if the DELAY pin voltage doesn't reach 1.25 V before the PFC-On pin voltage rises above 1.75 V, the PFC output voltage resumes quickly. In this case, the soft-start function does not operate.

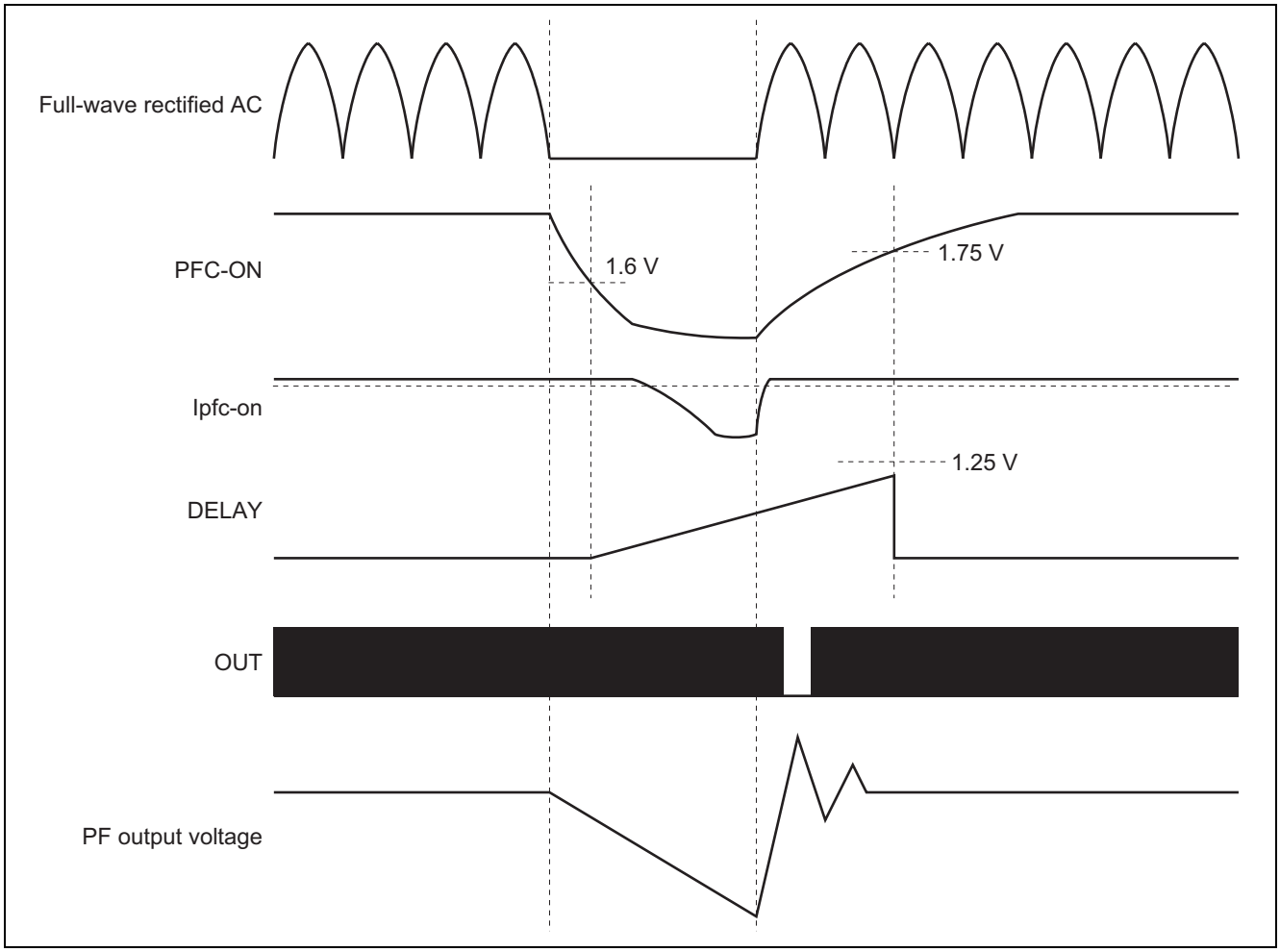


Figure 6 PFC Hold Function Operation Waveform 1

The hold time for PFC operation is adjusted by the value of the capacitance on the DELAY pin. Note, however, that if VCC voltage of IC is not normally supplied during a momentary outage, the PFC-ON hold function does not operate.

(2) When the Momentary Outage is Long

When the momentary outage is long enough that the DELAY pin voltage reaches 1.25 V, Output on the OUT is stopped, SS is reset, and PFC operation stops. When the supply of AC voltage resumes, the IC is restarted in a soft-start operation.

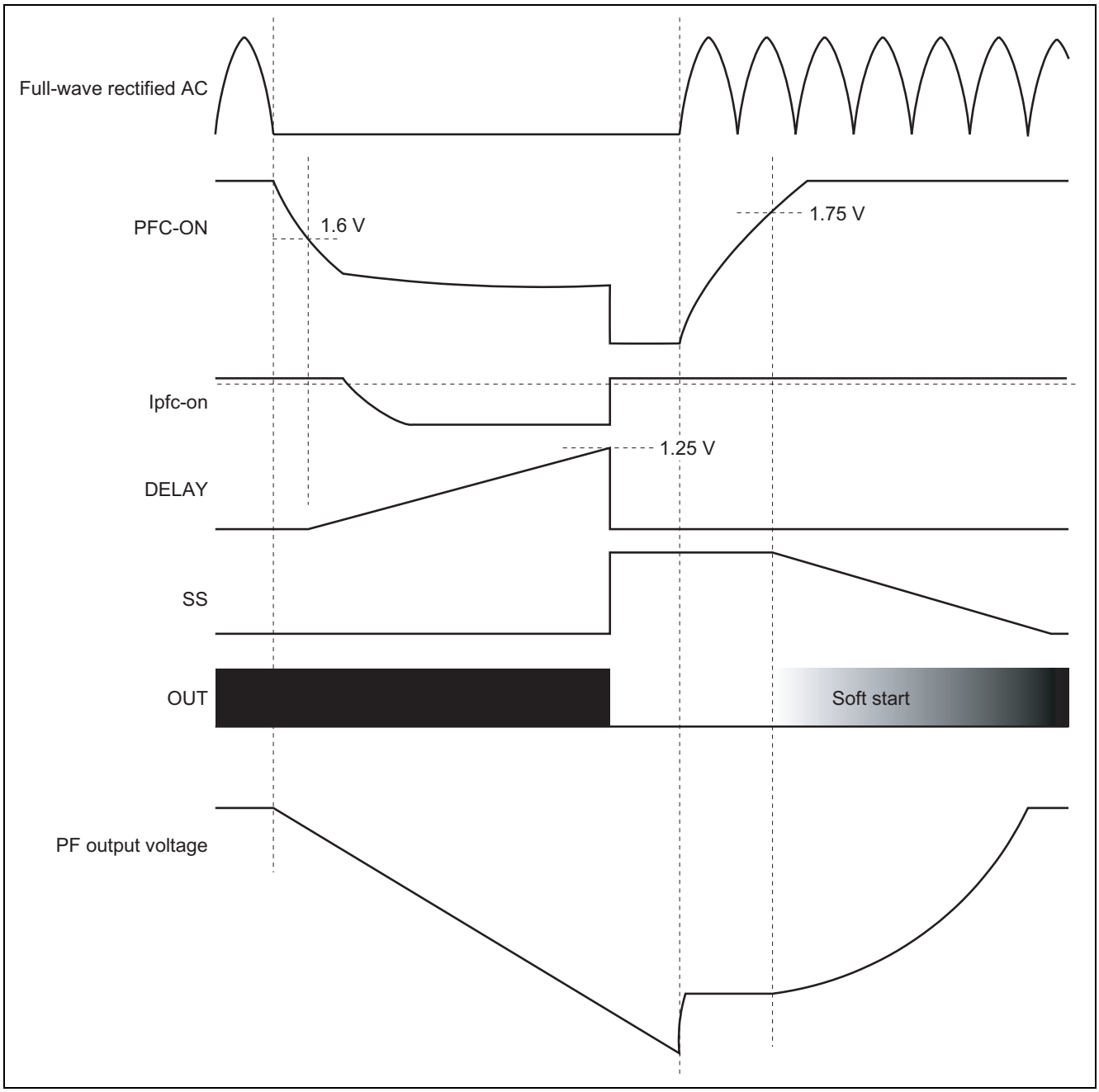


Figure 7 PFC Hold Function Operation Waveform 2

Note: When the PFC output voltage is driving a heavy load, the PFC output voltage falls rapidly, and the FB pin may fall below 0.5 V before the DELAY pin reaches 1.25 V. Here, the OUT pin is stopped, and the SS pin is reset by the FB pin low-voltage detection circuit.

(3) PFC Shutdown

By forcibly lowering the PFC-ON pin to 0.95 V, the PFC operation can be stopped even during the hold period. Output on the OUT pin is stopped, the SS pin is reset, and the PFC operation stops. When the PFC-ON pin is driven higher than 1.75 V, the IC is restarted in a soft-start operation.

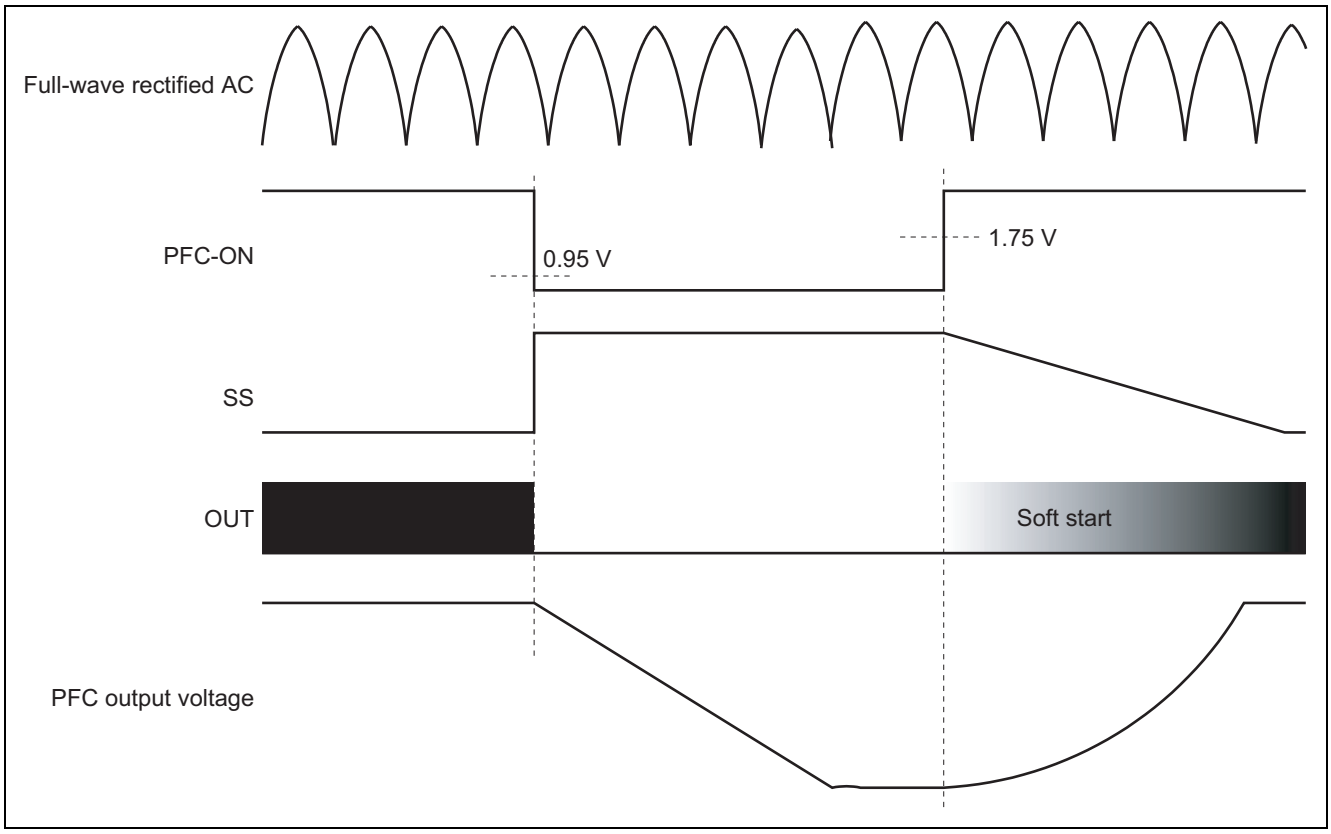


Figure 8 PFC Shutdown Function Operation Waveform

5. FB Pin Function

The FB pin is a feedback input for the PFC output voltage. This pin is applied to voltage divided PFC output with resistors. The PFC output voltage is controlled so that the applied voltage on FB is 2.5 V. The FB pin function provides protection against abnormal PFC output voltages. The protective functions are over voltage detection, low-voltage detection, and Power Good (PG) signal control. These functions do not operate when VREF voltage is lower than 4 V as UVL operation and shut down.

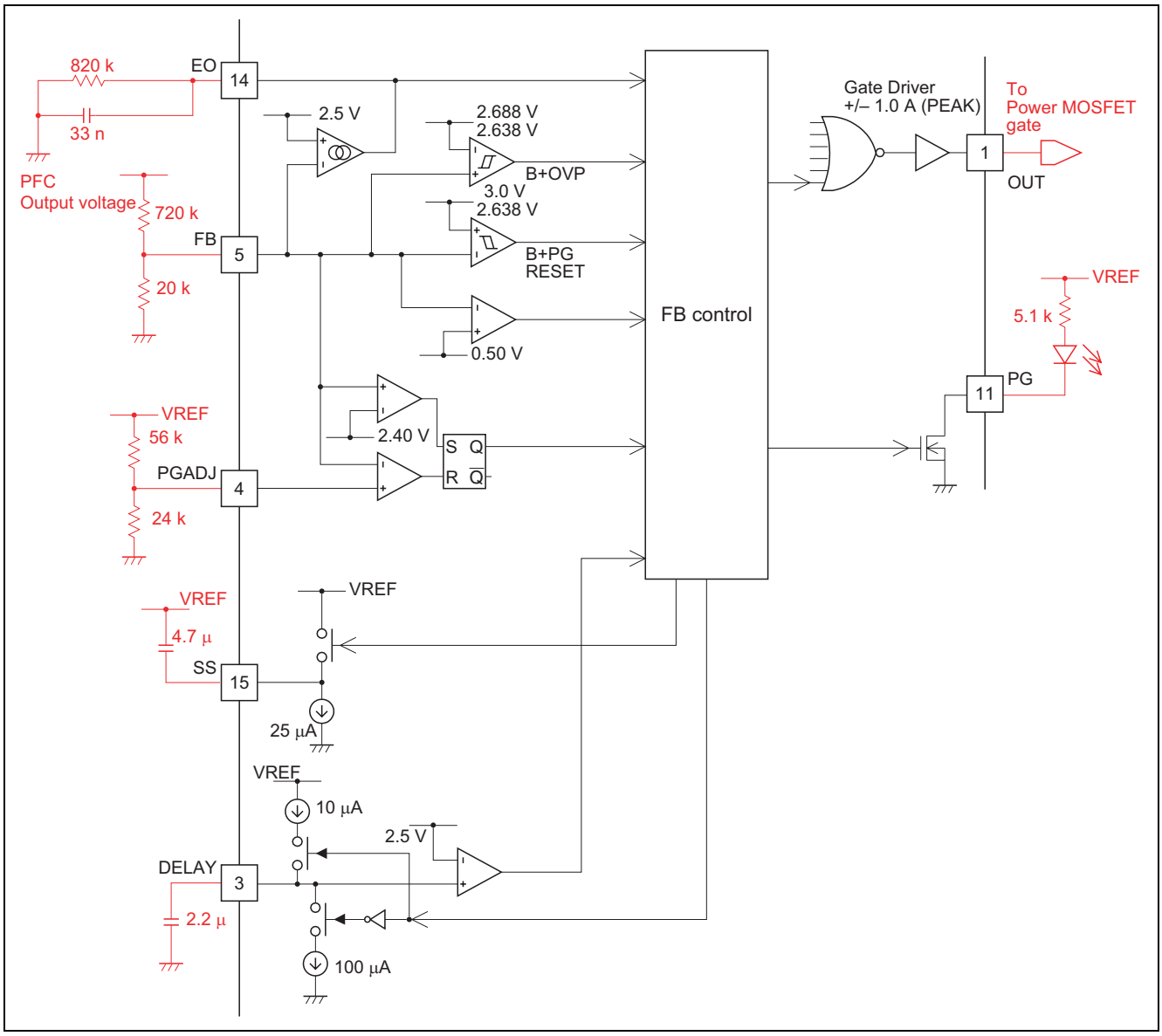


Figure 9 Internal Circuits Connected to the FB Pin

5-1. Power-Supply Startup Operation

When the AC voltage is applied, the PFC-ON pin voltage starts to rise; after it has reached 1.75 V, PFC operation starts. When PFC operation starts, the voltage on the FB pin starts to rise. When it has reached 2.4 V (equivalent to 96% of the PFC output voltage), the capacitor attached to the DELAY pin starts to charge up. When the voltage on the DELAY pin reaches 2.5 V, the internal MOS FET of the PG pin is turned off. Delaying the output of the PG signal avoids an unstable state of PFC output voltage, and assists in achieving correct on-and-off control in the back stages of the system.

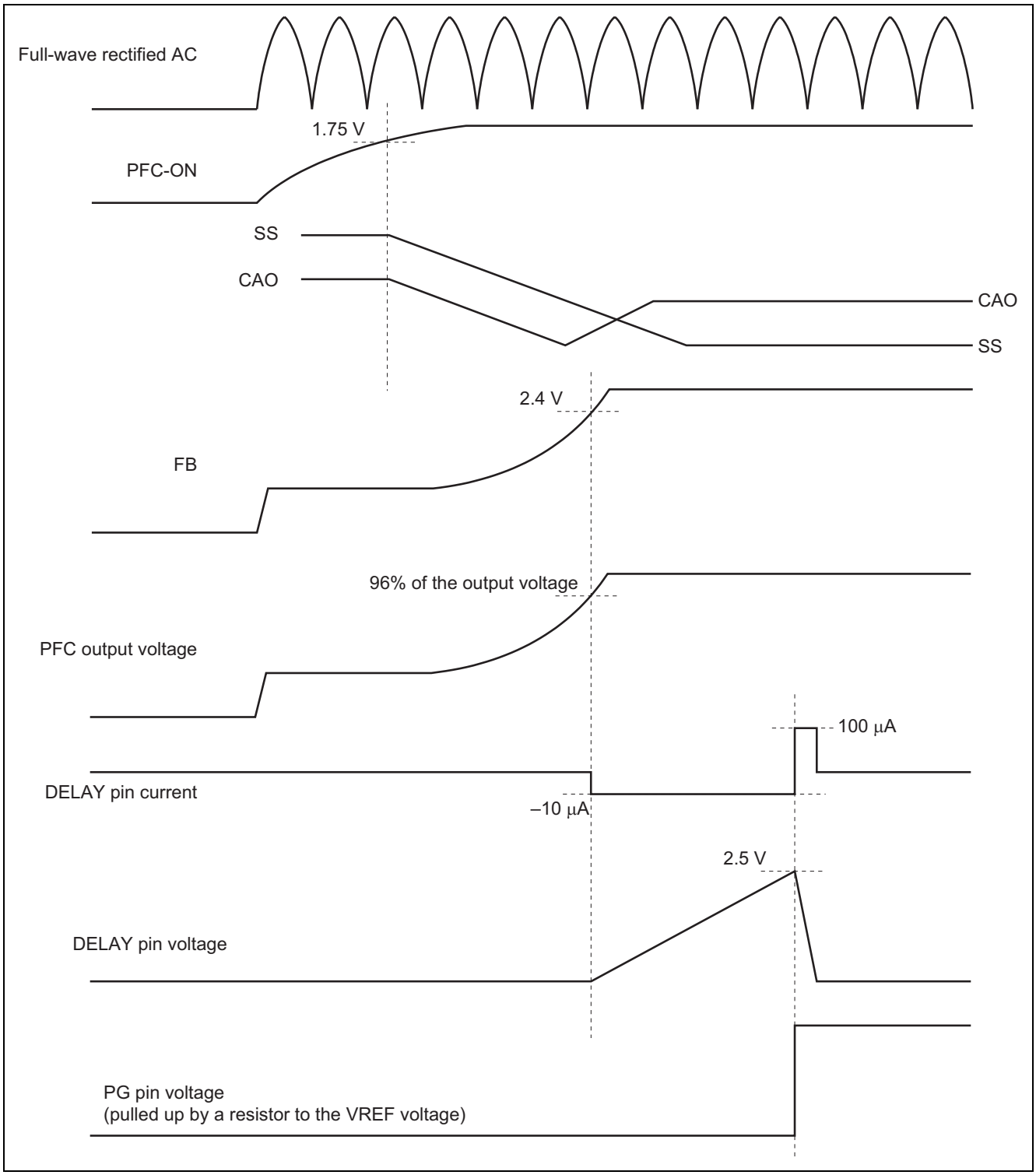


Figure 10 Waveforms in Operation to Delay PG Assertion

5-2. Operation when the Power-Supply Stops

When the supply of AC voltage stops the voltage on the FB pin falls. When the voltage on the FB pin is the same voltage on the PGADJ pin, the internal MOS FET of the PG pin is immediately turned on. When the FB pin voltage is lower than 0.5 V, PFC operation stops, and the SS pin is reset.

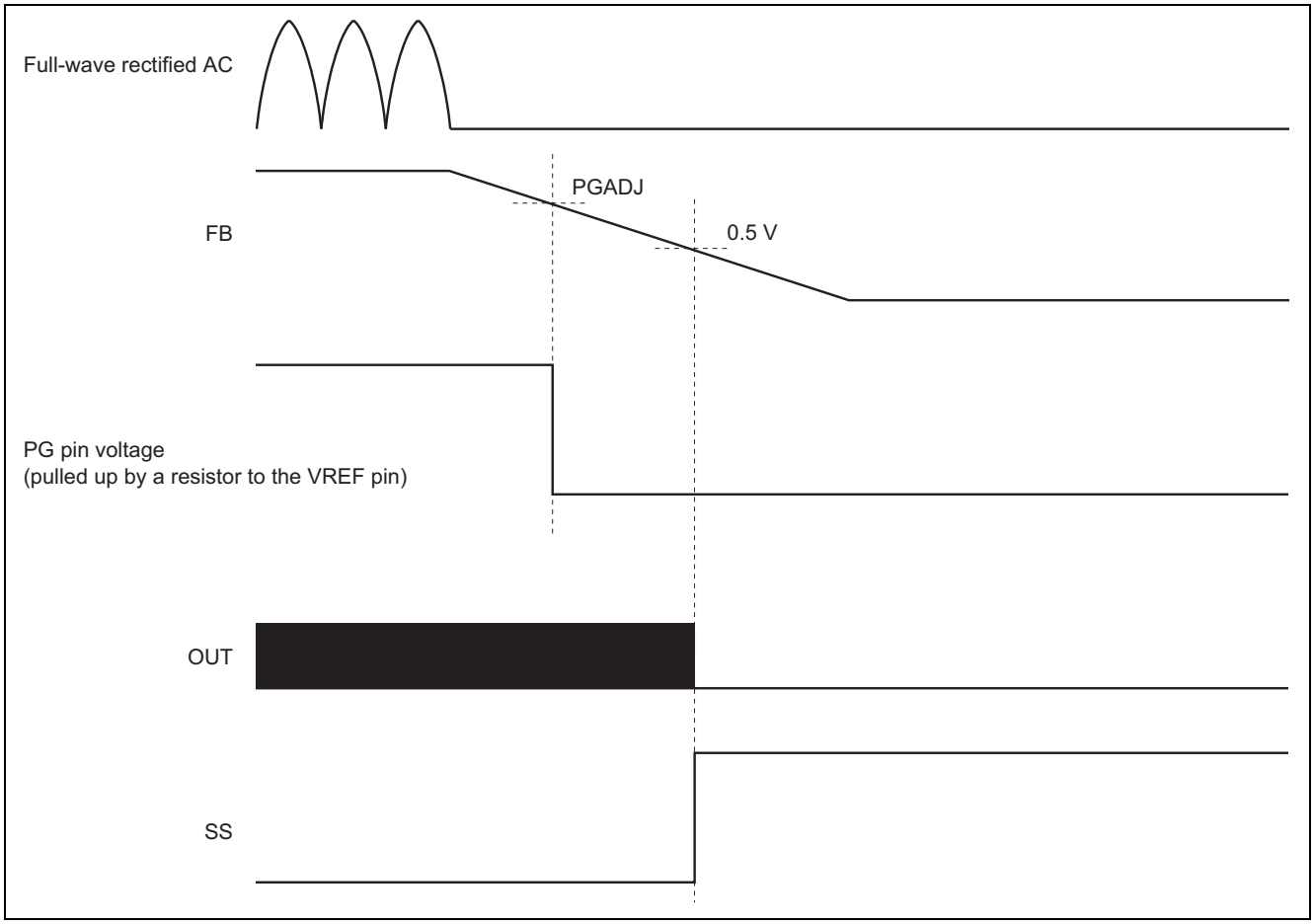


Figure 11 Waveforms in Operation to Stop PG Output

Note: When the load on the PFC output voltage is light, the PFC output voltage falls slowly, so the PFC-hold function may be activated before the voltage on the FB pin falls to 0.5 V. In this case, the PFC hold function takes over, stopping output on the OUT pin and resetting the SS pin.

5-3. Over Voltage Operation

When the PFC output voltage is larger than 7.5% of the prescribed voltage due to an abnormality in the system or a sudden change of AC voltage or load, operation of the OUT pin is terminated. When the PFC output voltage returns to within 5.5% of the prescribed voltage, operation of the OUT pin is restarted. If the PFC output voltage rises to 20% above the prescribed voltage, the condition is considered definitely abnormal, and output of the PG signal is also stopped. In this case, too, when the voltage returning to within 5.5% of the prescribed voltage is considered a return to normal conditions, operation of the OUT pin is restarted and the PG signal is output after the delay time due to operation of the DELAY pin.

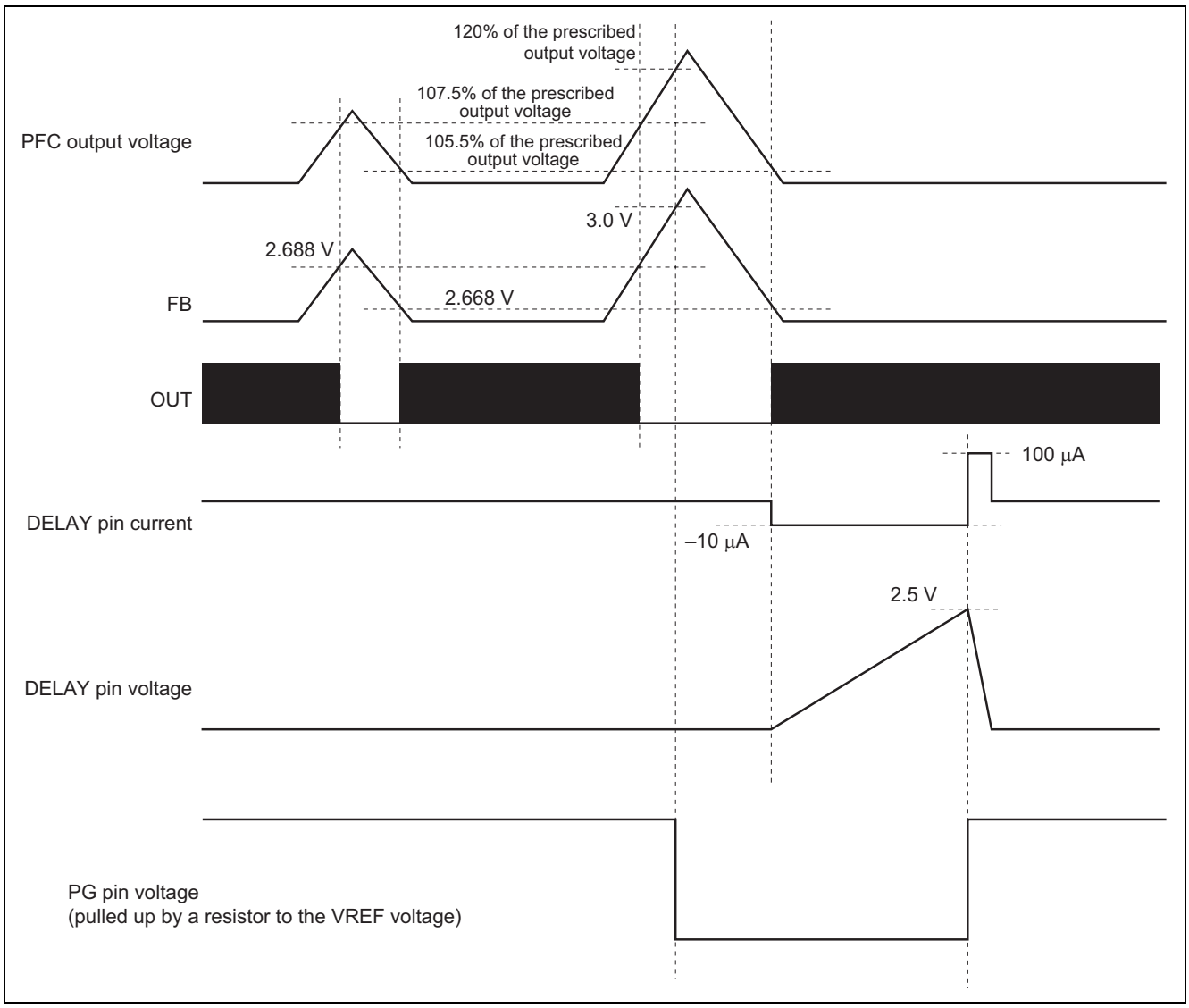


Figure 12 Waveforms of Operations after Over Voltage Detection by the FB Pin

6. IC Shutdown Function

When the DELAY pin is pulled up to 4 V, the IC shutdown function operates. During shutdown, the IC enters the standby state. To reset the circuit from the shutdown state, the voltage on VCC must be lowered to 4 V or less. After this reset, when the VCC pin voltage reaches 10.5 V, the IC is restarted.

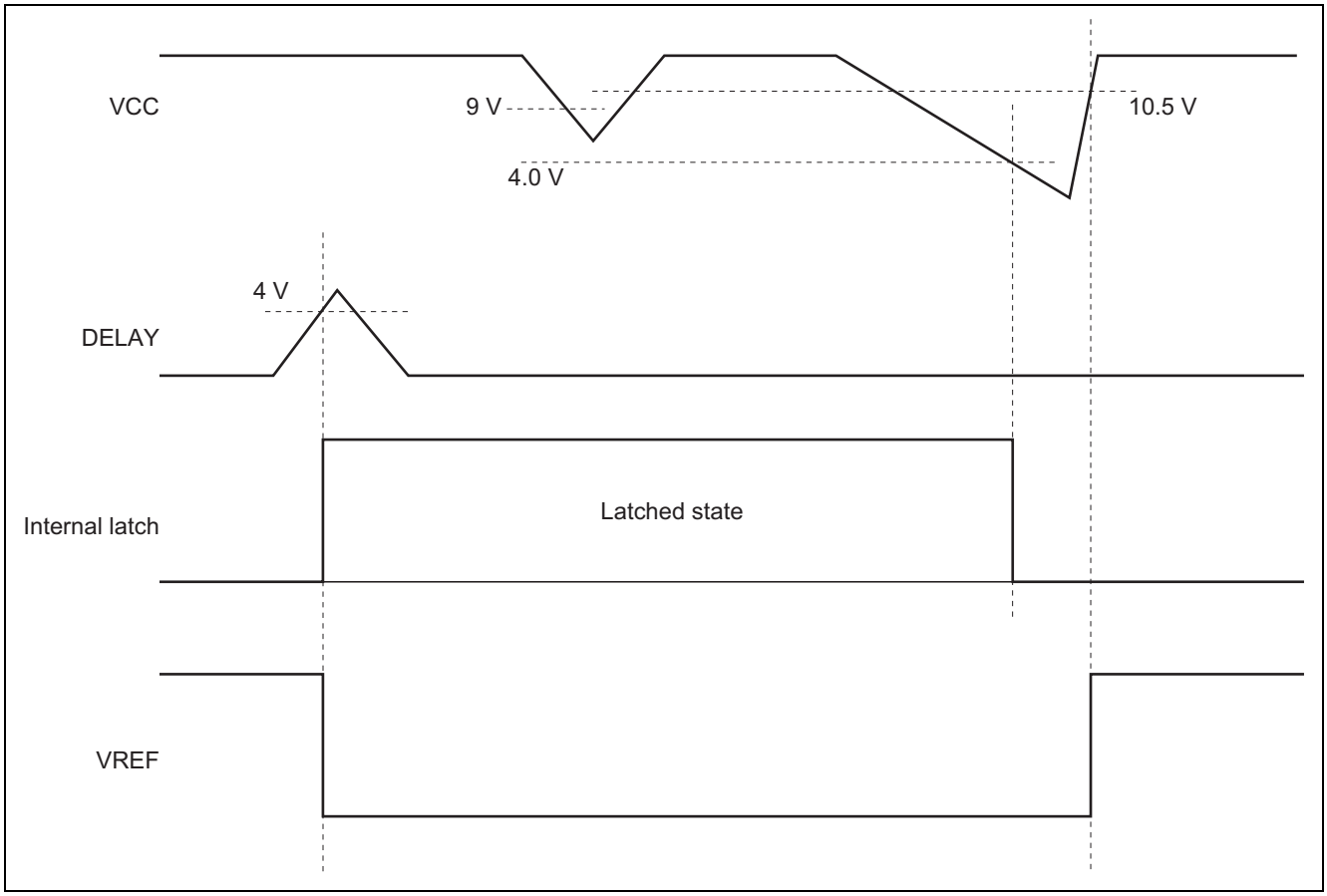
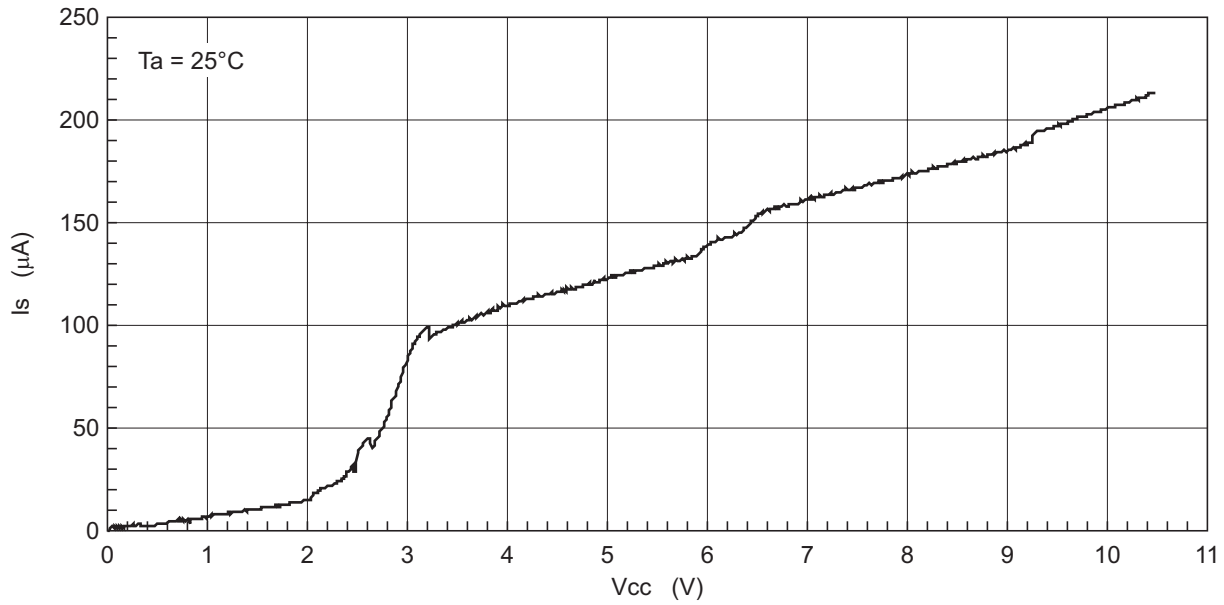


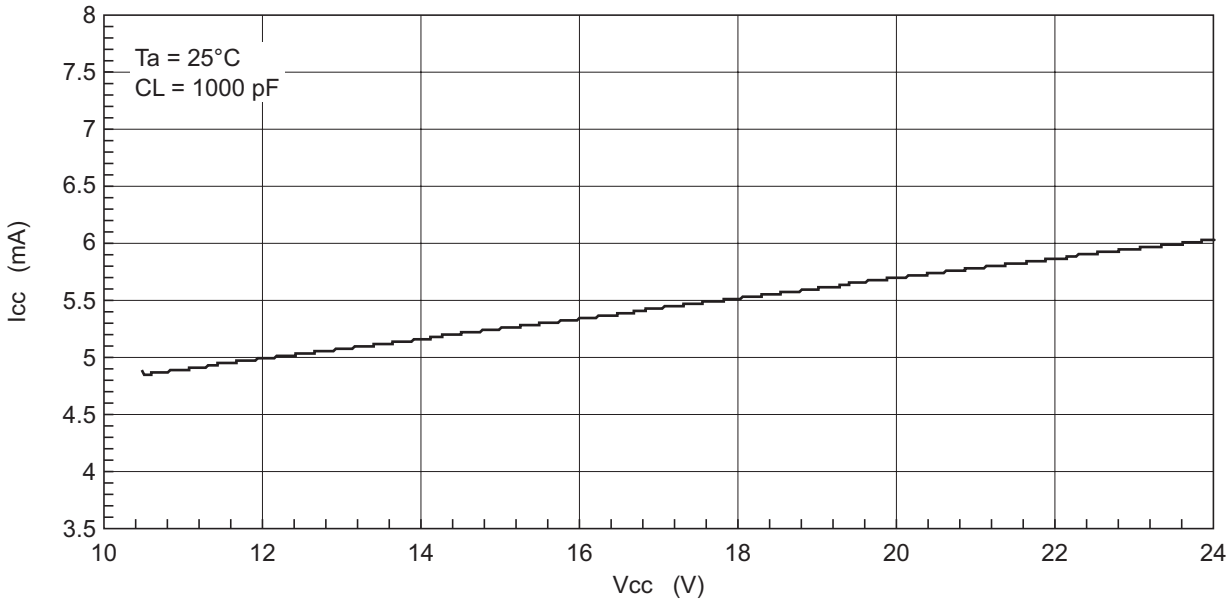
Figure 13 Waveform of Operations in IC Shutdown

Main Characteristics

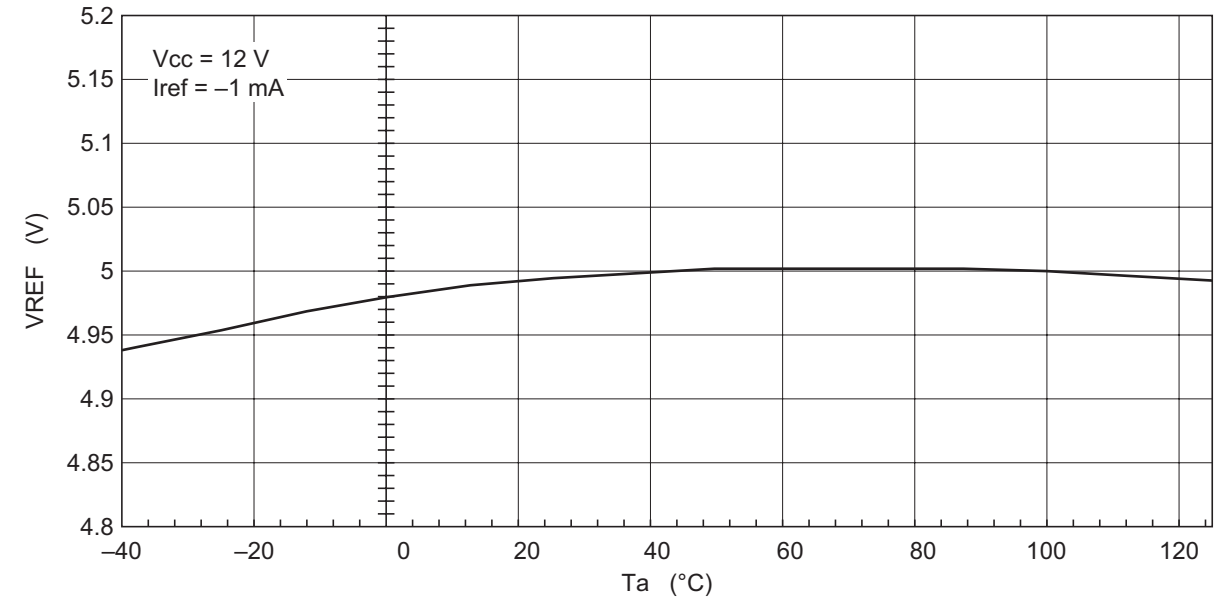
Standby Current vs. Power Supply Voltage Characteristics



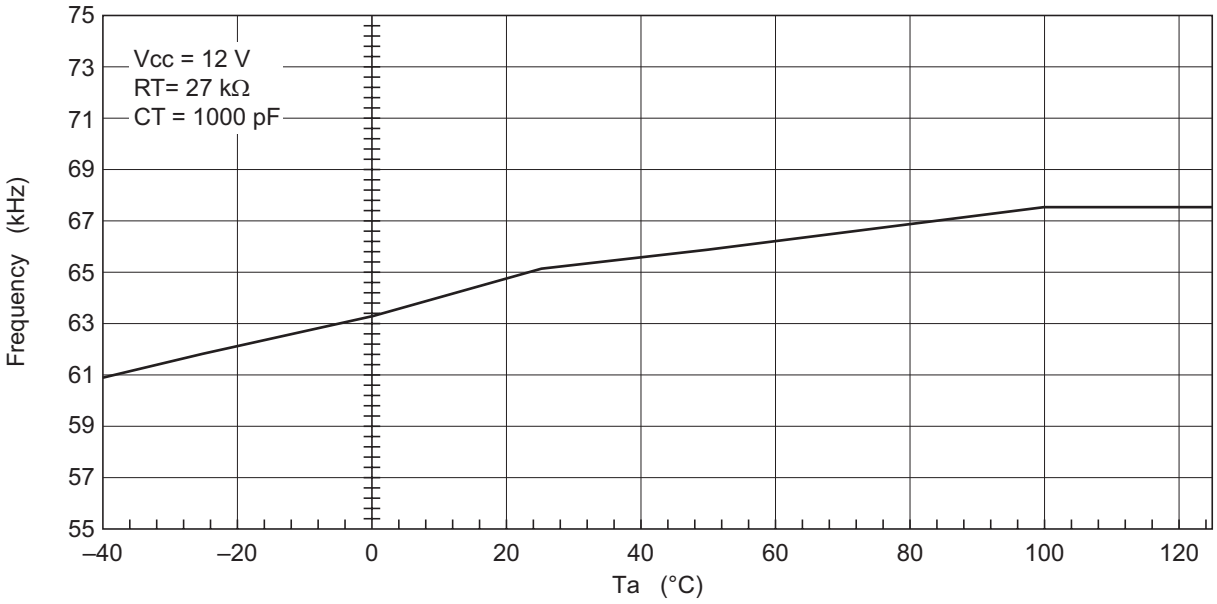
Power Dissipation vs. Power Supply Voltage Characteristics



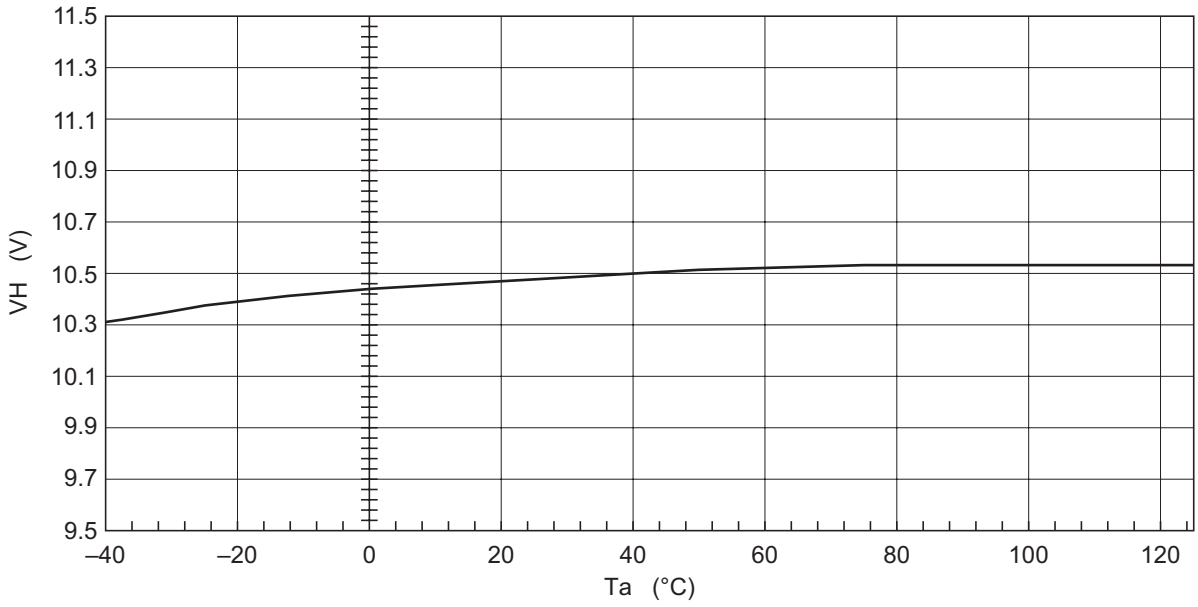
Reference Voltage Temperature Characteristics



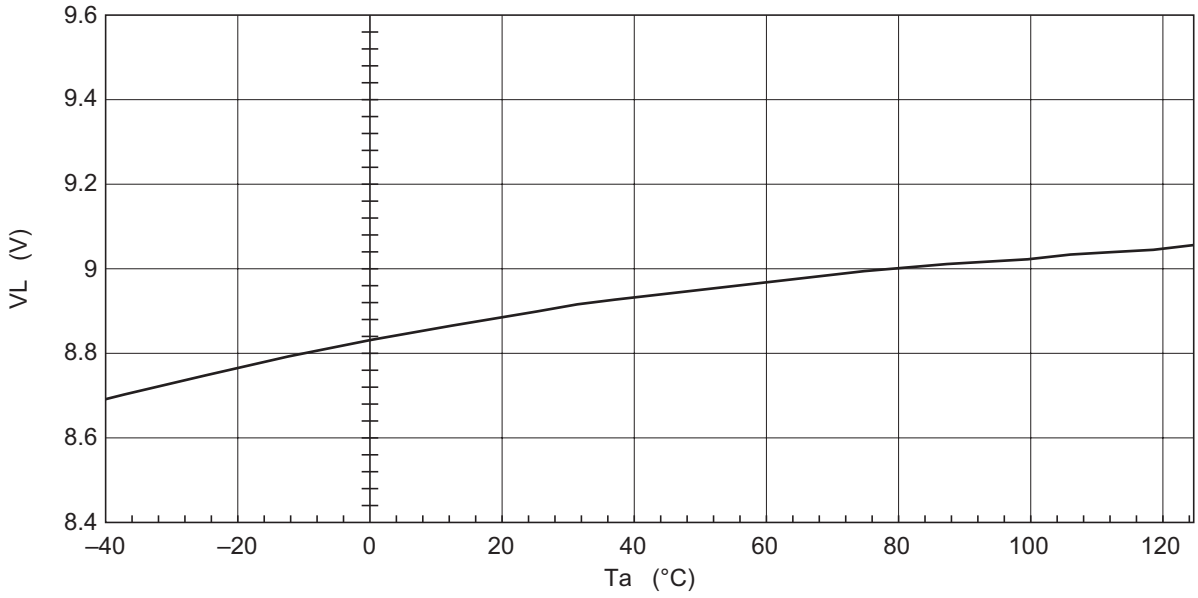
Operating Frequency Temperature Characteristics



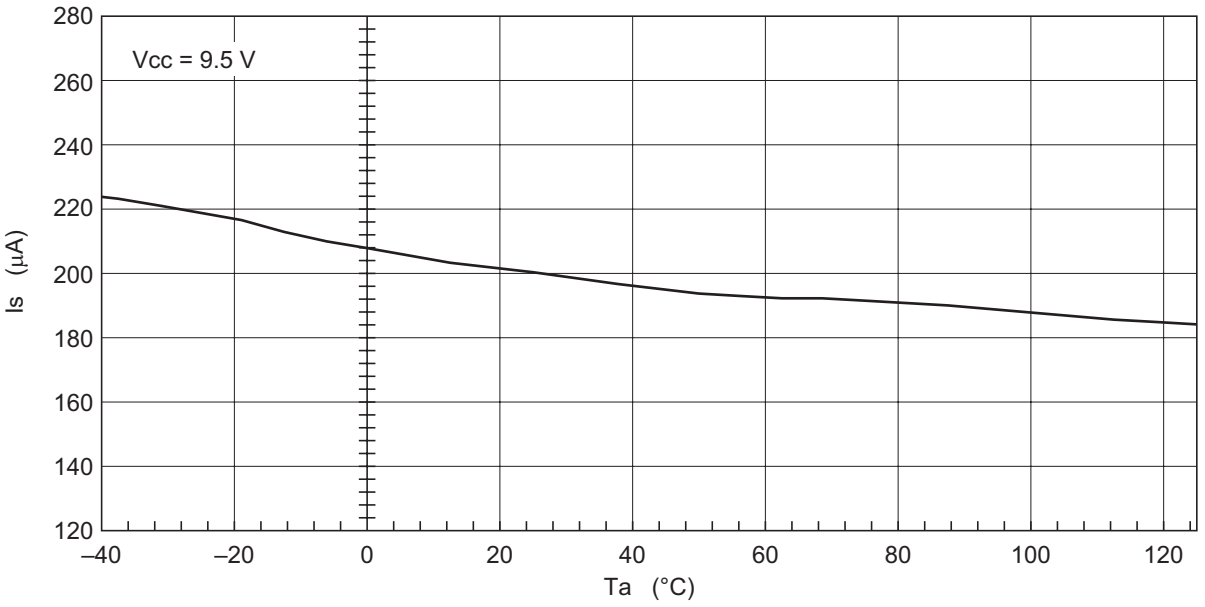
Start-up Voltage Temperature Characteristics



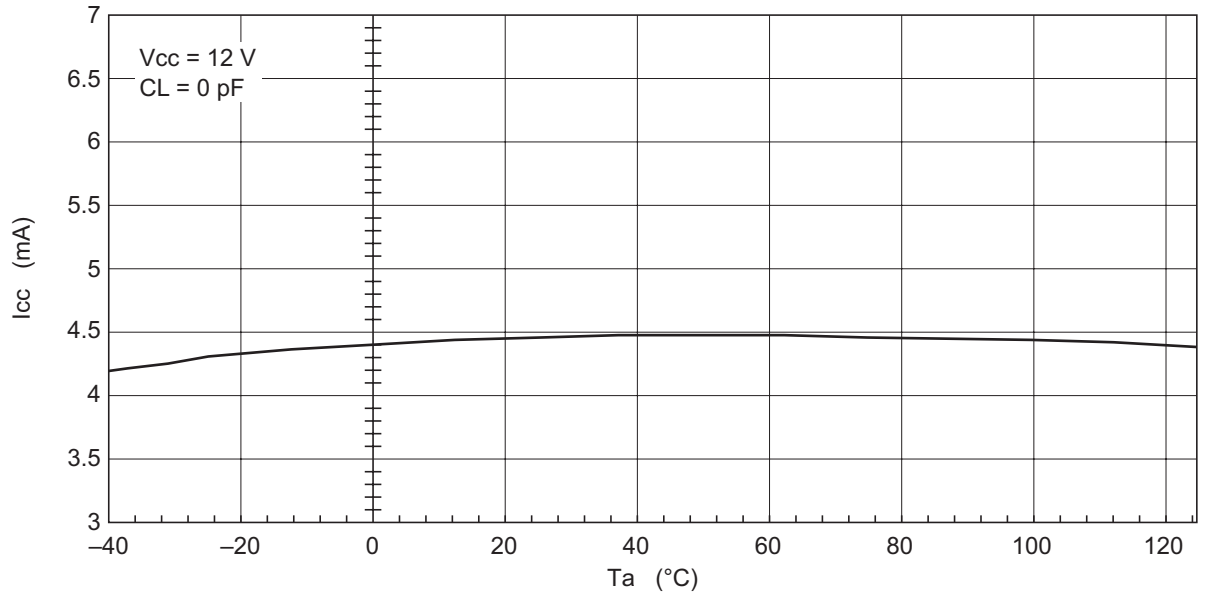
Shutdown Voltage Temperature Characteristics



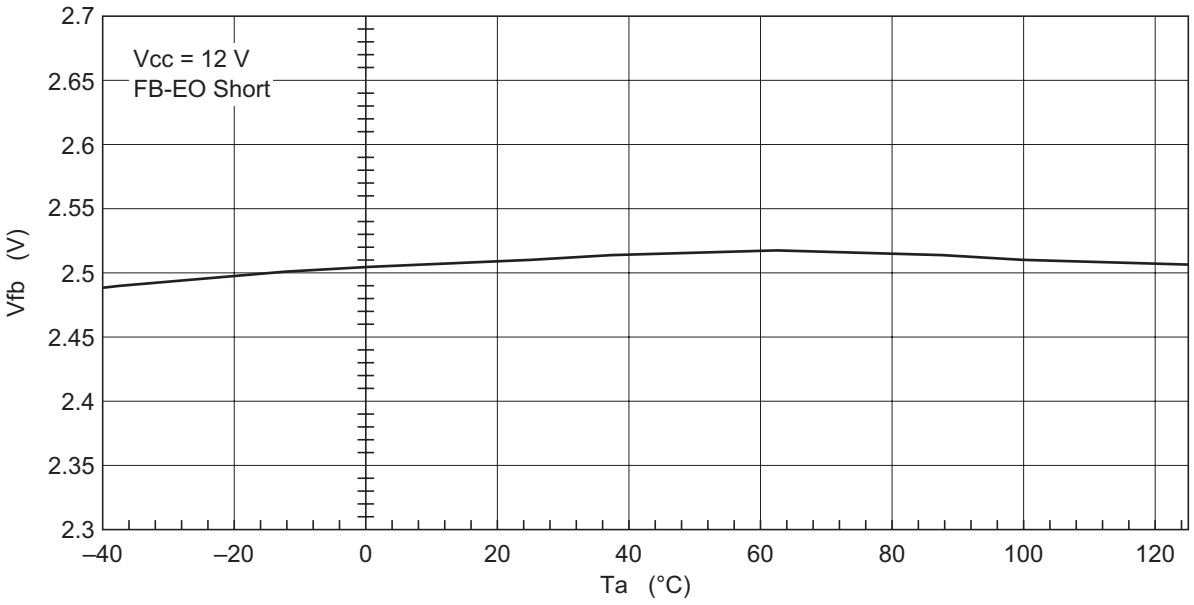
Standby Current Temperature Characteristics



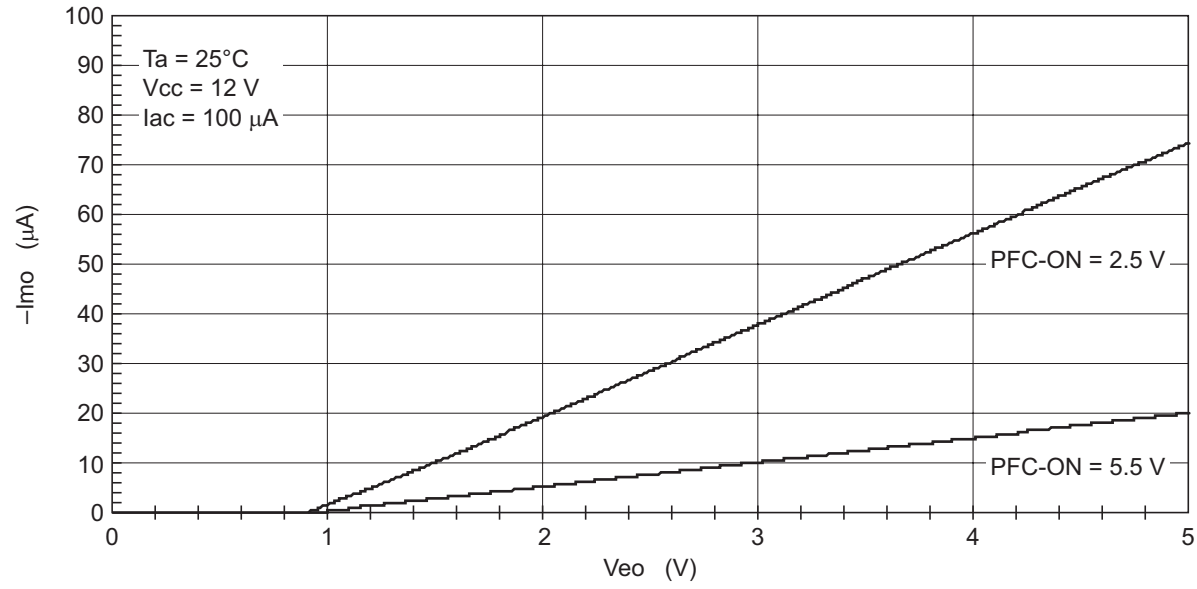
Operating Current Temperature Characteristics



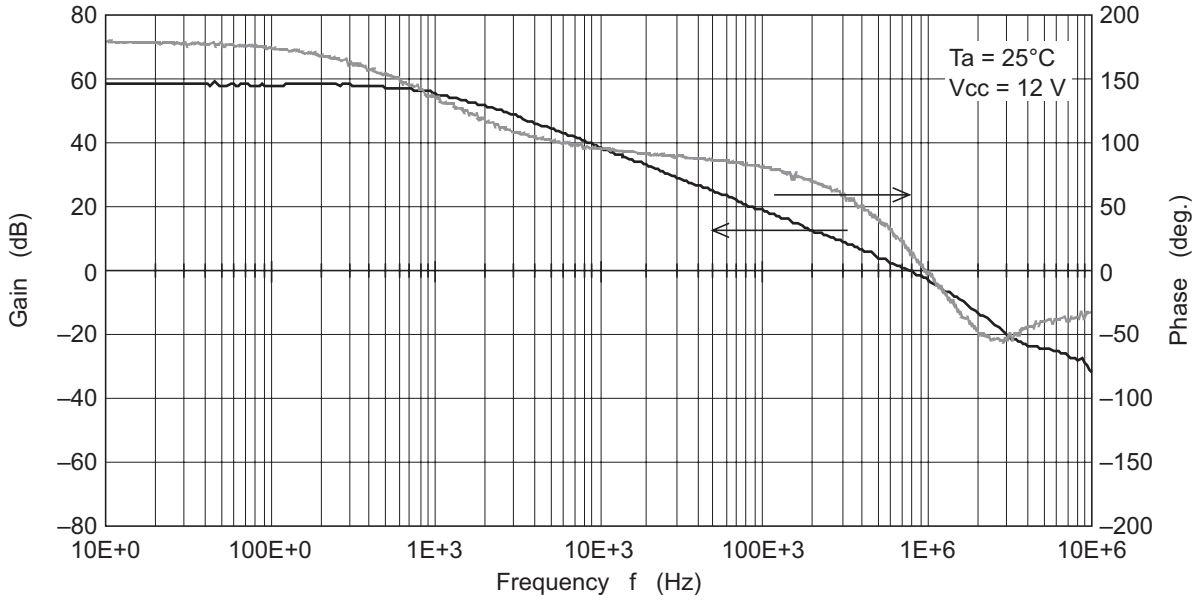
VAMP Feedback Voltage Temperature Characteristics



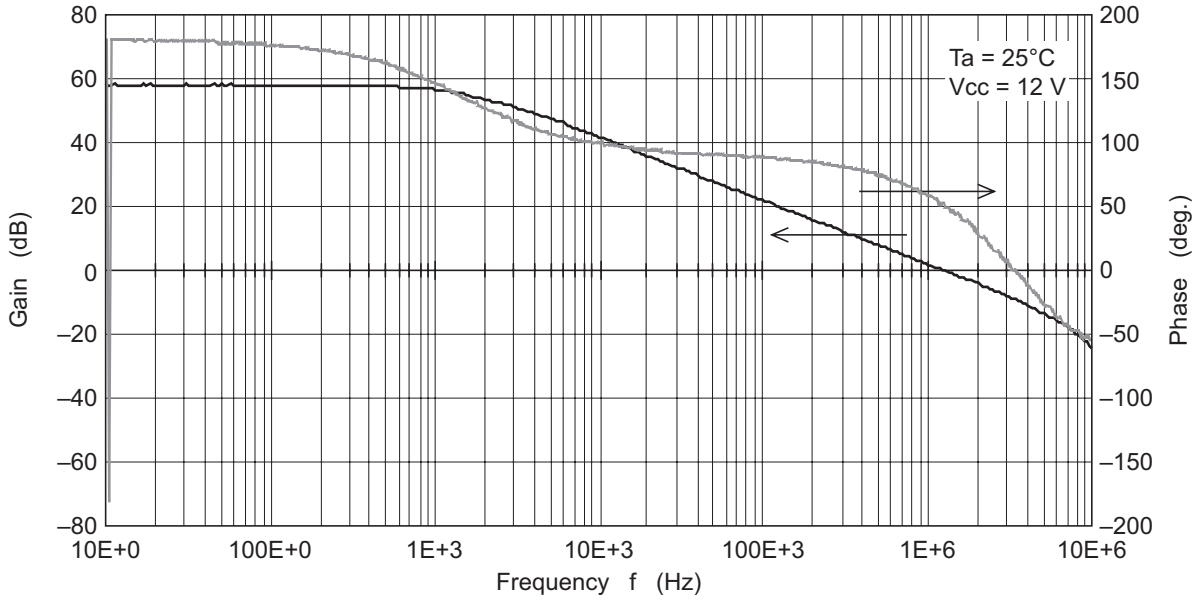
EO Pin Voltage vs. CS Pin Current Characteristics



Vamp Frequency Characteristics



Camp Frequency Characteristics



Precautions on Usage

1. DELAY Pin

The value of the external capacitor connected to the DELAY pin determines the PFC hold function hold time and the PG signal output delay time. However, since the above functions are achieved by the same pin, the times are related as follows.

PG delay time = 2 × PFC hold time

2. CS Pin

The CS pin is used to for detection in PFC control led current. When power supply is started up, the voltage drop of inrush current must not exceed the maximum rated value of the CS pin.

3. VREF Pin

For stabilization, be sure to connect a capacitor between the pin and ground. It possible to occur overshoot of VREF by connected capacitance. The degree of the overshoot will depend on the value of the connected capacitor. Pay particular attention to this point if you intend to use the VREF pin voltage as reference voltage for an external circuit.

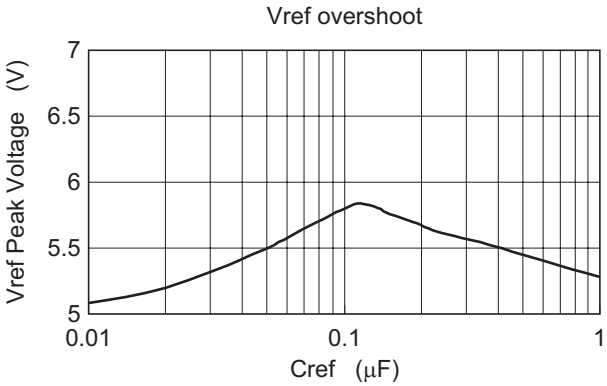


Figure 14 Overshoot on the VREF Pin vs. Capacitance

4. PFC-ON Pin

In design of worldwide power supply, it is possible that calculated voltage exceed maximum rated voltage of PFC-ON pin. Actually, as a clamp circuit is included in the PFC-ON pin, the voltage is clamped however, clamp current must not exceed 300 µA.

5. OUT Pin

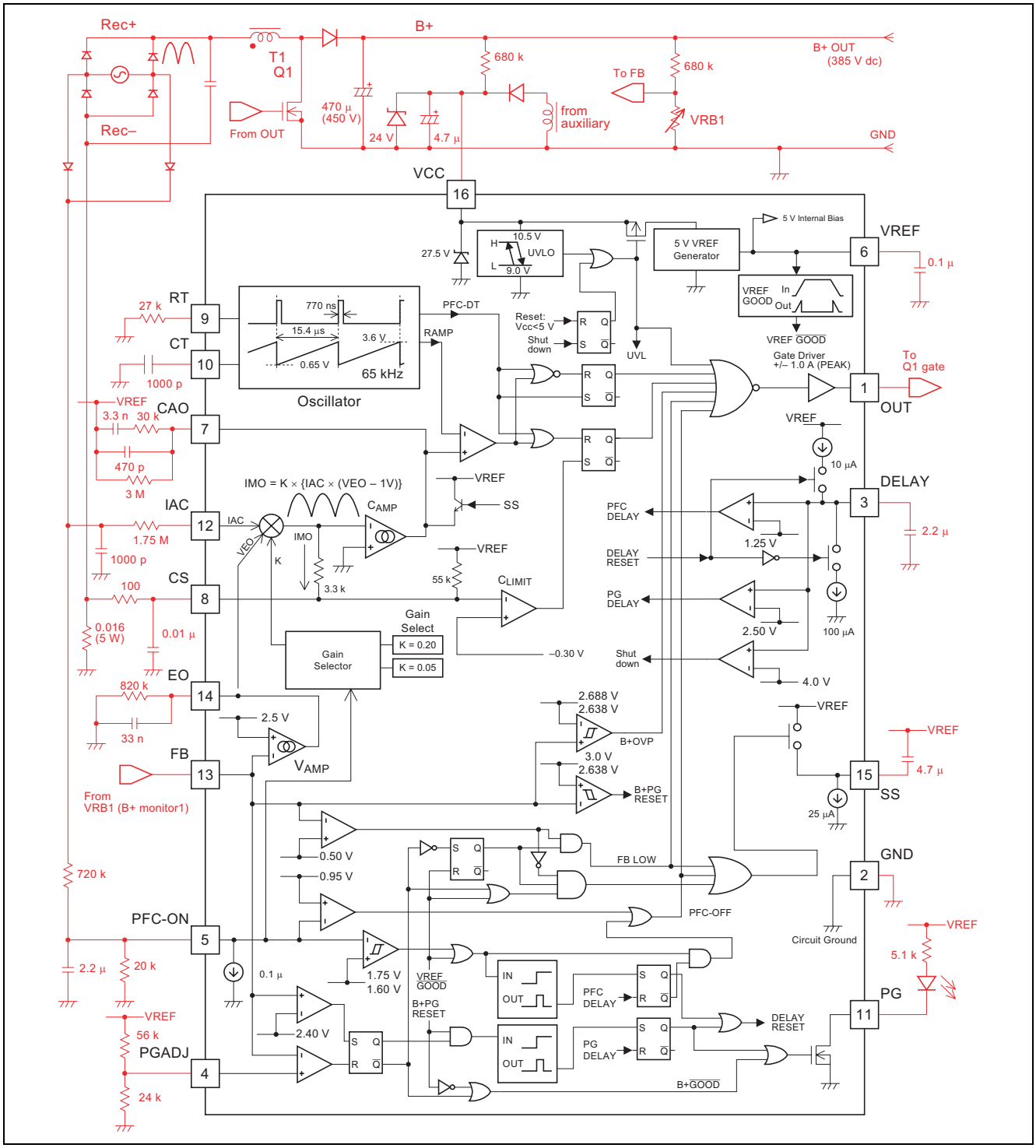
Undershooting or overshooting may occur due to the wiring of the OUT pin. These may bring to malfunctions of the IC. In such a case, prevent the undershooting or overshooting by using a Schottky barrier diode, etc.

6. Pattern Layout

In designing the pattern layout, pay as much attention as is possible to the following points.

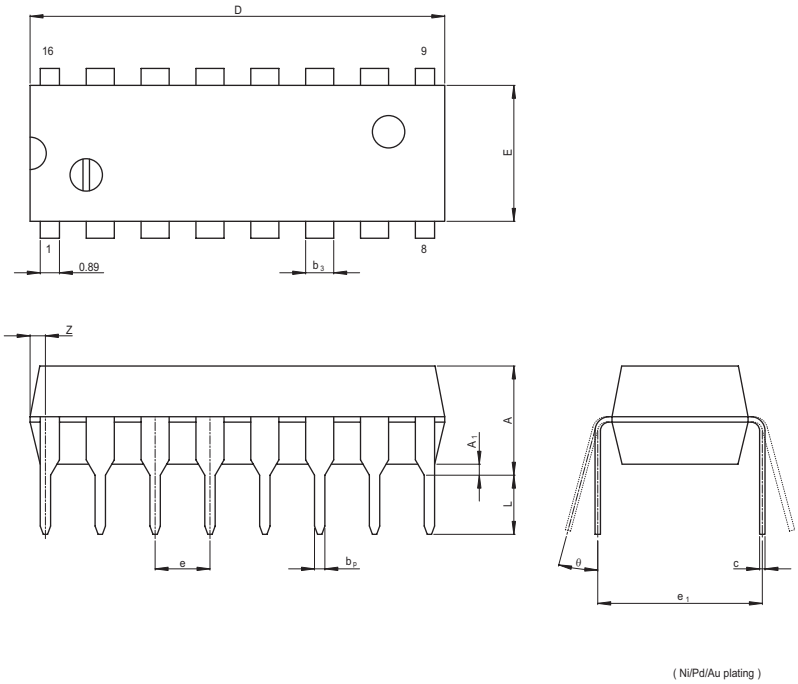
(1) Place the stabilizing capacitor for the VREF pin as close to the IC as possible, and keep the wiring short.
(2) Place the timing resistor of the RT pin as close to the IC as possible, and keep the wiring short.
(3) Place the phase compensation circuit for the CAO pin as close to the IC as possible, and keep the wiring short.
(4) Place the timing capacitor for the CT pin as close to the IC as possible, and keep the wiring short.
(5) Place the stabilizing capacitor for the VCC pin as close to the IC as possible, and keep the wiring short.
(6) Place the resistor for the PGADJ pin as close to the IC as possible, and keep the wiring short.
(7) Place the IC pins and their wiring as far from high-voltage switching lines (particularly the drain voltage for the power MOS FET) as possible and in general design the wiring to minimize switching noise.
(8) It is probable that stability of operation is achieved by inputting signals via filters to pins with input functions. Note, however, that such filter circuits can affect the bias conditions for pins that have both input and output functions.

System Diagram



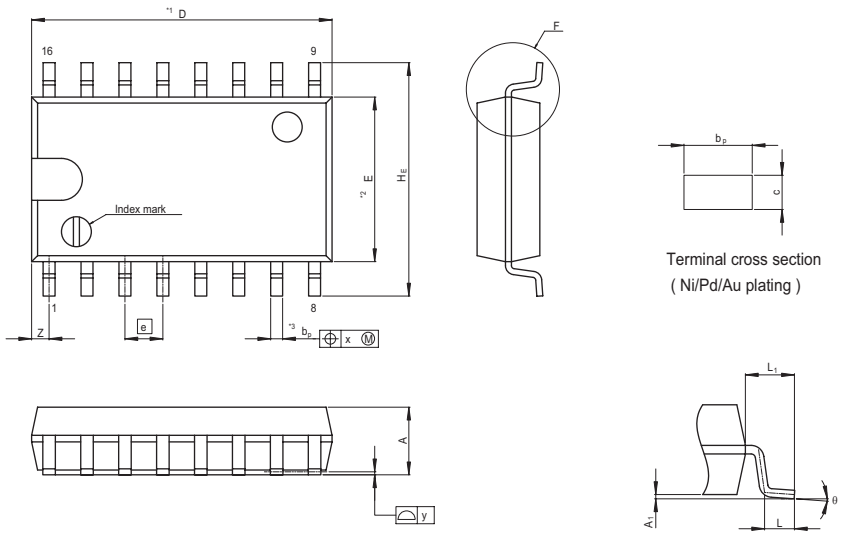
Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-DIP16-6.3x19.2-2.54	PRDP0016AE-B	DP-16FV	1.05g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
e_1	—	7.62	—
D	—	19.2	20.32
E	—	6.3	7.4
A	—	—	5.06
A_1	0.51	—	—
b_p	0.40	0.48	0.56
b_3	—	1.30	—
c	0.19	0.25	0.31
θ	0°	—	15°
e	2.29	2.54	2.79
Z	—	—	1.12
L	2.54	—	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP16-5.5x10.06-1.27	PRSP0016DH-B	FP-16DAV	0.24g



NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	10.06	10.5
E	—	5.50	—
A_2	—	—	—
A_1	0.00	0.10	0.20
A	—	—	2.20
b_p	0.34	0.40	0.46
b_1	—	—	—
c	0.15	0.20	0.25
c_1	—	—	—
θ	0°	—	8°
H_E	7.50	7.80	8.00
e	—	1.27	—
x	—	—	0.12
y	—	—	0.15
Z	—	—	0.80
L	0.50	0.70	0.90
L_1	—	1.15	—

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